New Jersey Institute of Technology

Electrical and Computer Engineering

Course Outline ECE 395 [**Microprocessor Lab**] Fall 2025

Instructor: Azeez Bhavnagarwala

To contact instructor: **bhavnaga@njit.edu**

Lab Session: **Mondays 6:00 PM – 9:50 PM** *Room:* **FMH 204**

Office hours: **Mondays 5PM-5:50 PM** (Room: 342, ECE Building, Tel: 973-596-3663) or by appointment

Course Pre-requisites: Microprocessors (ECE 252) is required. Please see instructor if you have not taken ECE 252 and have an equivalent background.

Summary Course Description: ECE 395 introduces students to Microprocessor Interfacing using a RISCV 32b microcontroller. In this laboratory, students get the opportunity to advance on the conceptual background developed in ECE 252 on the RISCV Instruction Set Architecture to real hardware on an industry-standard Platform IO Integrated Development Environment. The Course offers a basic set of 6 labs which begin with the use of Platform IO to observe and document operation of microprocessor core as it executes code, an introduction to memory-mapped IO and an in-depth understanding of use of the GPIO interface in microcontrollers. Subsequent labs use the above background to develop programing and interfacing techniques using interrupts and serial communication protocols

Course structure:

Grades in the course for each Lab are based on successful demonstration of each of 6 Labs to the instructor. (15% of total grade for each of 6 Labs). Also required are Lab reports for each Lab that articulate the purpose of the Lab a description of relevant considerations of the hardware and any issues encountered and how they were debugged. A demonstration of the lab to the instructor with an explanation of the lab and responses to questions from the instructor is required of each student for each of the 6 labs and carries 67% of the grade for each lab. A video of a demonstration of the lab along with a report (in Word) that documents student's original experience in the lab carries the remaining 33% of the grade for each lab. 10% of the overall grade is based on regularity of attending lab and discussion sessions and the originality of student videos and the discussion of the lab articulated in the Lab report

Course Textbooks (PDF uploaded to Canvas):

Computer Organization and Design RISC-V Edition, 2021

Digital Design & Computer Architecture RISC-V Edition, 2022

ECE 395 Schedule:

Week	ECE 395 Content	Meet
1	*Introduction to Microcontrollers, Peripherals & their interfacing. Setup Platform IO as an extension of Visual Studio Code. Demo a compile and run of 'Superblink'. Release of PreLab 1 assignment*	FMH 204A
2	**Lab 1:** Write and debug code on Platform IO. Observe and document operation of microprocessor core as it executes code	
3	*Memory-mapped I/O. Using the GPIO Interface in FE310-G002 RISCV SoC. Direct Memory Access. GPIO peripheral register offsets. Program the GPIO in C or Assembly. Example code reviewed*	
4	**Lab 2:** Configure MCU internal peripherals. Use the GPIO pins	
5		
6	*Programming and interfacing techniques that use interrupts. FSMs, Object Counters, Sensor evaluation, push-button interface*	
7	**Lab 3:** Finite State Machine implementation of an 'annunciator' using the RISCV SoC	
8		
9	*Managing communication with external devices. Hardware supported handshake, Polling, Interrupts, Communication Protocols/standards (UART, USB and a few others). Asynchronous serial communication*	
10	**Lab 4:** Serial Communication with UART	
11	**Lab 5**: Implement Calculator using UART	
12	*Enabling and disabling interrupts. Interrupt mechanisms, interrupt requests, vectored interrupts, interrupt timers*	
13	**Lab 6:** Demonstrate Interrupts with code	
14		
15	*Final Week: Refine Lab reports/Demo Videos, discuss future advanced project opportunities*	