New Jersey Institute of Technology

Electrical and Computer Engineering

Course Outline ECE 252 [**Microprocessors**] Fall 2025

Instructor: Azeez Bhavnagarwala

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Class Lecture: **Wednesdays 6:00 PM – 8:50 PM** *Room:* **WEST LECT 1**

Office hours: **Mondays 5PM-5:50 PM** (Room: 342, ECE Building, Tel: 973-596-3663) or by appointment

Course Pre-requisites: Digital Design and Computer Organization (ECE 251) is required. Please see instructor if you have an equivalent background.

Summary Course Description: ECE 252 *introduces* students to Microcontrollers and the trends that are shaping their design and use – markets for trillions of pervasive, low cost, connected and energy efficient IoT systems, increasingly integrated with hardware extensions to support execution of AI workloads in recent years. ECE 252 focusses on the RISC V instruction set architecture (ISA) - an 'open source' ISA that enables IoT systems to deliver on three key capabilities: higher performance, energy efficiency, & ultra-low cost.

ECE 252 reviews the basic organization of and components used by the processor and details the ISA with its encoding, formats and extensions. The class reviews the RISC V memory map and the RISC V GPIO complex that manages the connection of digital I/O pads to digital peripherals, including SPI, UART, and PWM controllers, as well as for regular programmed I/O operations. ECE 252 also develops the background for students to pursue ECE 395 (Microprocessor Lab) with use of an online RISC V simulator, an introduction to the Platform IO Integrated Development Environment and an introduction to IoT system design.

Course structure:

Your performance in the course will be assessed with your performance in **weekly HW assignments** (30% of total grade), that include RISCV simulations, design problems and a review of a relevant assigned publications, **Midterm** (30% of total grade) and a **final** (35% of total grade). Class Participation: 5%

Course Textbooks (PDF uploaded to Canvas):

Computer Organization and Design RISC-V Edition, 2021

Digital Design & Computer Architecture RISC-V Edition, 2022

Course Learning Outcomes

I Be able to quantitatively *compare performance & energy efficiency* of different computers, ISAs and hardware implementations for a given workload and assess best opportunities for improving performance

II Understand and be able to use the RISC V ISA – formats, encoding, extensions. Integrate mastery of RISCV ISA into coding assignments.

III Understand and be able to use the RISC V memory map and the RISC V GPIO complex that manages the connection of digital I/O pads to digital peripherals, Understand widely used communication protocols including USB, UART. Be able to use an online tool to program a RISC V controller.

Student Outcomes

1. an ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics (CLO I, II, III)
2. an ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors (CLO I, II, III)
3. an ability to communicate effectively with a range of audiences (CLO I, II)
4. an ability to function effectively on a team whose members together provide leadership, create a collaborative and inclusive environment, establish goals, plan tasks, and meet objectives (CLO I, II)
5. an ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions (CLO I, II, III)
6. an ability to acquire and apply new knowledge as needed, using appropriate learning strategies. (CLO I, II, III)

Academic Integrity:

"*Academic Integrity is the cornerstone of higher education* and is central to the ideals of this course and the university. Cheating is strictly prohibited and devalues the degree that you are working on. As a member of the NJIT community, it is your responsibility to protect your educational investment by knowing and following the academic code of integrity policy that is found at: *http://www5.njit.edu/policies/sites/policies/files/academic-integrity-code.pdf*.

Please note that it is my professional obligation and responsibility to report any academic misconduct to the Dean of Students Office. *Any student found in violation of the code by cheating, plagiarizing or using any online software inappropriately will result in disciplinary action. This may include a failing grade of F, and/or suspension or dismissal from the university.* If you have any questions about the code of Academic Integrity, please contact the Dean of Students Office at *dos@njit.edu*"

Use of Generative AI Tools:

Use of generative AI Tools outside the classroom is encouraged to enable students to explore or efficiently search and understand a broad range of topics related to microprocessors including those outside the scope of the course. However, use of these tools is not permitted during Midterm and Final Exam or as an aid in completing HW assignments.

Course Schedule:

Week	ECE 242 Content	Assignments
1	Introduction to Microprocessors	HW 1
2	Introduction to Basic Computer Organization	HW 2
3	Introduction to Instruction Set Architectures, RISC Computing	HW 3
4	RISC V Instruction Formats, Encoding	HW 4
5	Comparisons across the x86, ARM and RISCV Instructions	HW 5
6	Floating Point Arithmetic and IEEE 754 representation,	HW 6
7	Review Problems for Midterm	
8	Midterm	
9	Introduction to the Processor datapath & its components	HW 7
10	Instruction Execution in Hardware	HW8
11	Register and Calling Conventions, Compressed Instructions	
12	Introduction to Parallel processing and RISCV Vector Extensions What will a processor in an IoT look like in the near future - Fast (3-5GHz), very cheap (<$1), pervasive >1 Trillion sold/year, ultra-energy efficient (micro - nano watts) and very intelligent.	HW 9
13	Communication interfaces, GPIO, USB & UART	HW 10
14	HiFive Rev B Dev Board review for ECE 395	
15	Review Problem Sets for Final	
	Finals Week	**Final Exam**