ECE 495 Spring 2024
Computer Engineering Design Laboratory

Course Description:	This course emphasizes hardware design and debugging. Topics include combinational and sequential logic design using CAD tools, VHDL, and design based upon PLA/PLD.
Instructor:	Milad Shojaee FMH 218 ms2892@njit.edu
Lecture/Laboratory meet at:	M 10:00am–11:20am (ECEC 115) / Section 002, R 8:30am–12:50pm (FMH 204A)
Office Hours:	By Appointment
Prerequisite:	ECE 353 and ECE 394
Recommended Text:	J. Knoots, E. Hou, Laboratory and Supplementary Notes, ECE 495: Computer Engineering Design Laboratory, Ver. 3.0, ECE Dept. 2007. Any VHDL book.
Academic Integrity:	**Academic Integrity is the cornerstone of higher education and is central to the ideals of this course and the university. Cheating is strictly prohibited and devalues the degree that you are working on. As a member of the NJIT community, it is your responsibility to protect your educational investment by knowing and following the academic code of integrity policy that is found at: http://www5.njit.edu/policies/sites/policies/files/academic-integrity-code.pdf.** Please note that it is my professional obligation and responsibility to report any academic misconduct to the Dean of Students Office. **Any student found in violation of the code by cheating, plagiarizing or using any online software inappropriately will result in disciplinary action. This may include a failing grade of F, and/or suspension or dismissal from the university.** If you have any questions about the code of Academic Integrity, please contact the Dean of Students Office at dos@njit.edu
Course Learning Outcomes (CLO):	Student should be able to 1. design sequential circuits (using EEPROM) that meet a given design specification. 2. design hardware system that meets a given design specification and write VHDL program to implement them. 3. write lab reports documenting the results of the lab experiments.
Relevant ABET 1-7 Student Outcomes:	1. an ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics (CLO 1) 3. an ability to communicate effectively with a range of audiences (CLO 3) 6. an ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions (CLOs 1, 2)

Grading Policy: **Quizzes: 25%**
Lab.: 75%
Demo: 40%
Report: 35% Writing (20%)
Logic Diagram, Wiring Diagram, Software/Code comments, Timing Diagram, etc. (15%)

Laboratory report is due one week after the lab is completed. A sample lab report and the grading rubric are available on canvas.
The quizzes will be conducted during the lecture.

Tentative Schedule

Week	Content
1	Introduction
2	Lab 1: Event Driven Circuit
3	Lab 2: Introduction to Altera DE2 Board
4	Lab 3: T-bird Turn Signal
5	Lab 3: T-bird Turn Signal
6	Lab 4: Clocks and Timers Using LCD Display
7	Lab 4: Clocks and Timers Using LCD Display
8	Lab 5: Using VHDL Components
9	Spring Recess
10	Lab 5: Using VHDL Components
11	Lab 6: ALUs and the LPM Library
12	Lab 6: ALUs and the LPM Library
13	Lab 7: Microcoded CPU Design
14	Lab 7: Microcoded CPU Design
15	Lab 7: Microcoded CPU Design