Helen and John C. Hartmann
Department of Electrical and Computer Engineering
New Jersey Institute of Technology
Digital Design (ECE-251)
Academic Year: 2024-2025
Term: Fall 2024

Instructor: A. Yousef
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Office: 324 ECEC
Office Hours/ Extra Help: Available upon request via email and Zoom
Phone: 973-596-5692

Class Place & Time: Class Room: ECEC 100

Face-to-Face	Tuesday	6:00 PM – 9:00 PM – Lecture + Problem Solving
Face-to-Face	Tuesday	9:00 PM – 10:05 PM – Recitation + More Problem Solving + Solutions to Homework Assignments

Attendance: Required at class lectures and problem-solving sessions.
Cellular phones and Beepers: Shut off or in quiet mode.

Credits and Contact Hours: (3-1-3); 3 hrs. Lecture; 1 hr. Recitation, 3 credit hrs. = 4 contact hrs.

Method of Communique: NJIT Canvas – email

Text Book: (Required) Alan B. Marcovitz, Introduction to Logic Design, 3rd edition, McGraw-Hill, ISBN # 978-0-07-319164-5

(Optional) John D. Carpinelli, An Animated Introduction to Digital Logic Design, 1st Edition, Published by NJIT Library. https://digitalcommons.njit.edu/oat/1/ There is no cost to students or anyone, to use this book, either in a formal course or for self-study.

Lecture Notes: PowerPoint presentation slides supplied by professor.

Course Description: The design of combinational and sequential logic circuits used in digital processing systems and computers. Basic register transfer operations are covered. Topics include Boolean algebra, minimization techniques and the design of logic circuits such as adders, comparators, decoders, multiplexers, counters, arithmetic logic units, and memory systems.

Prerequisites: Phys 122

Course Learning Outcomes (CLO): The student will be able to:
1. Knowledge of the number systems and its conversion processes.
2. Use Boolean Algebra and minimize Boolean functions.
3. Construct various digital circuits using logic gates, latches, and flip flops.
4. Design and implement basic combinational and sequential logic circuits.

5. Design and implement digital logic systems.
6. Knowledge of various digital electronic circuit parameters.
7. Familiarity with the various logic families (TTL, CMOS, ECL, etc.).
8. Analyze digital circuits in a multitude of possible applications
9. Use **Cadence OrCAD/**PSPICE circuit modeling and analysis application software.

Relevant Student Outcomes:

1. An ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics (CLO 1-4)
2. An ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors (CLO 3)
3. An ability to communicate effectively with a range of audiences (CLO3)
4. An ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions (CLO 3-4)

Exams:

1. Test 1 (25%) – Oct. 22, 2024 (week 8)
2. Test 2 (25%) – Dec. 10, 2024 (week 14)
3. Quizzes (20%) – Every week, unless instructed otherwise
4. Final (25%) – Dec. 20, 2022 (week 16; tentative)
5. Tests and final exams are closed notes and books

Homework Assignments:

HW Assignments (5%)

1. Submittal of solutions to homework assignments after the assigned due date will not be accepted.
2. Honors class fulfills 15% more work in form of homework, test problems and projects.
3. Problems (marked with asterisk *) should be solved using Multisim or PSPICE (available in Computer Labs and for purchase as Student License).

DOWNLOAD PSPICE STUDENT VERSION:
https://www.ema-eda.com/products/cadence-orcad/orcad-academic-program

DOWNLOAD GETTTING STARTED WITH MULTISIM STUDENT VERSION:
http://www.ni.com/white-paper/10710/en

Course Withdrawal: Last day to withdraw from course: **Monday, November 11, 2024**

Mandates and Extenuating Circumstances:

1. To ensure consistency and fairness in application of the NJIT policy on withdrawals, student requests for withdrawals after the deadline *(end of the 10th week of classes)* will not be permitted unless extenuating circumstances are documented through the Office of the Dean of Students. The course instructor and the Dean of Students are the principal points of contact for students considering withdrawing from a course.
2. The student should contact the Dean of Students Office regarding extenuating circumstances for any reason (late withdrawal from a course, request for a make-up exam, request for an incomplete grade). The Dean

of Students make the determination of whether extenuating circumstances exist or not and will be notifying the instructor accordingly. Please do provide the instructor with your medical or other documents; such documents need to be submitted by the student to the Dean of Students. Except for cases determined by law, the instructor is not required to accommodate student requests even when extenuating circumstances are certified by the Dean of Students.

"Academic Integrity is the cornerstone of higher education and is central to the ideals of this course and the university. Cheating is strictly prohibited and devalues the degree that you are working on. As a member of the NJIT community, it is your responsibility to protect your educational investment by knowing and following the academic code of integrity policy that is found at: http://www5.njit.edu/policies/sites/policies/files/academic-integrity-code.pdf.

It is my professional obligation and responsibility to report any academic misconduct to the Dean of Students Office. Any student found in violation of the code by cheating, plagiarizing, or using any online software inappropriately will result in disciplinary action. This may include a failing grade of F, and/or suspension or dismissal from the university. If you have any questions about the code of Academic Integrity, please contact the Dean of Students Office at dos@njit.edu"

Undergraduate Grading Policy:

Undergraduate Grading Legend

Grades	Significance	Average Score
A	Superior	(90 – 100)
B+	Excellent	(85 – 89)
B	Very Good	(80 – 84)
C+	Good	(75 – 79)
C	Acceptable	(70 – 74)
D	Minimum	(65 – 69)
F	Inadequate	(<65)
AU	Audit	
I	Incomplete. Grade deferred--**given in rare instances** to students who would normally have completed the course work but who could not do so because of special circumstances. If this grade is not removed during the next regular semester, a grade of F will result.	
W	Withdrawn	
S	Satisfactory	
U	Unsatisfactory	

In all departments in the College of Science and Liberal Arts, a grade of C or higher is required in any lower division course (200 level and below) that serves as a prerequisite for another course.

Course Material:

Date	Week #	Chapter/ Sections	Topics
Sept 3	1	CH 1.1 – 1.2	• Course Syllabus and Expectations - Required Textbook & Grading Policy • Introduction to Digital Design – The Digital Revolution – The Design and Analysis Process Flow – Signal Types – Continuous, Discrete Time, Digital – Digital Switches and Bits • Introduction to Number Systems: Decimal, Binary, Arbitrary Radix/Base Representation • Conversion Between Bases – Decimal to Binary, Decimal to Octal, Decimal to Hexadecimal, Binary to Decimal, Octal to Decimal, Hexadecimal to Decimal, Octal to Binary & Binary to Octal Hexadecimal to Binary & Binary to Hexadecimal
Sept 9	1		*Last day to add/drop a class with 100% refund*
Sept 10	1		*W grade posted for course withdraws*
Sept 10	2	Ch. 1.2– 1.5	• Addition, Subtraction, Multiplication and Division of Binary, Octal and Hexadecimal Numbers • Representation of Positive & Negative Numbers Using Signed-magnitude, r's complement, (r-1)'s Complement • Binary Subtraction Using r's complement, (r-1)'s Complement • Overflow in Binary Addition • Binary Coded Decimal (BCD) Code and BCD Addition • Excess 3 Code and Excess 3 Addition • Introduction to Gray Code, Gray Code to Binary Conversion • What is Parity? Hamming Code Detection & Correction
Sept 17	3	Ch. 2.1 – 2.6	• Design Process for Combinational Systems • Truth Tables • Don't Care Conditions • Boolean Switching Algebra • Implementation of Functions with AND, OR and NOT Logic Gates • The Complement • From Truth Table to Algebraic Expressions
Sept 24	4	Ch. 2.7 – 2.12	• Simplification of Algebraic Expressions • Manipulation of Algebraic Functions & Nand Gate Implementations • Sum of Products (SOP), Products of Sums (POS) representations • Minimal Conical Form Conversion • A More General Boolean Algebra • Dual Form

Date	Week #	Chapter/ Sections	Topics
Oct 1	5	Ch. 3.1 – 3.4	• Introduction to Karnaugh Maps (K-Map) • Minimum Sum of Product Expressions Using the Karnaugh Map • Don't Cares • Product of Sums
Oct 8	6	Ch. 3.5 – 3.6	• 5 and 6-Variable K-Maps • Multiple Output Problems
Oct 15	7	Ch. 4.1, 4.3 Ch. 4.4, 4.6	• Quine-McCluskey Method for One Output • Prime Implicant Tables for One Output • Quine-McCluskey Method for Multiple Output • Prime Implicant Tables for Multiple Output
OCT 22	8	*Test 1 – First Half of Session*	
OCT 22	8	Ch. 5.1 – 5.5	• Clock Signals • Timing Diagrams • Delays in Combinational Logic Circuits (Propagation Delay) • Hazards, Hazard-Free Design • Adders, Subtractors, adder/Subtractors • Comparators • Binary Decoders • Encoders and Priority Encoders • Multiplexers • Demultiplexer
OCT 29	9	Ch. 5.6 – 5.8	• Gate Arrays – ROMs, PLAs, and PALs • Simulation of Combinational Systems
Nov 5	10	Ch. 6.1 – 6.3	• Sequential Circuits & Systems • State Tables and Diagrams • Latches • Flip Flops (Truth Table, Characteristic Table and Excitation Table)
Nov 11	11	*Last day to withdraw from class*	
Nov 12	11	Ch. 6.4 – 6.5	• Triggering Methods in Flip-Flops • Differences between Latch and Flip-Flops • Race Conditions • Analysis of Sequential Systems • Mealy and Moore State Machines
Nov 19	12	Ch. 7.1 – 7.3	• Flip-Flop Design Techniques • The Design of Synchronous Counters • The Design of Asynchronous Counters • The Design Sequence Pattern Detector • State Reduction and Assignment • Simulation of Sequential Systems
Dec 3	13	Ch. 8.1 – 8.2	• Shift Registers • Data Format and Classification of Registers

Date	Week #	Chapter/ Sections	Topics
			• Bidirectional Shift Register • Universal Shift Register • Types of Counters –Ripple and Synchronous Counters • 3-Bit & 4-Bit Asynchronous Up Counters • 3-Bit & 4-Bit Asynchronous Down Counters • Modulus of a Counter & Counting UP to Particular Value
Dec 10	14	*Test 2 – First Half of Session*	
Dec 10	14		• Review for Final Exam
Dec 17	*Final Exam*		