ECE 495 Section 003 Fall 2023
Computer Engineering Design Laboratory

Course Description:	This course emphasizes hardware design and debugging. Topics include combinational and sequential logic design using CAD tools, VHDL, and design based upon PLA/PLD.
Instructor:	Qirui Tian qt2@njit.edu
Lecture/Laboratory meet at:	Mon 1pm–2:20pm (ECEC 100) / Thu 1pm–4:30pm (FMH 204A)
Office hours:	Thu 12pm-1pm at FMH 105 or by appointment
Prerequisites:	ECE 353 and ECE 394
Academic Integrity:	**Academic Integrity is the cornerstone of higher education and is central to the ideals of this course and the university. Cheating is strictly prohibited and devalues the degree that you are working on. As a member of the NJIT community, it is your responsibility to protect your educational investment by knowing and following the academic code of integrity policy that is found at: http://www5.njit.edu/policies/sites/policies/files/academic-integrity-code.pdf.** Please note that it is my professional obligation and responsibility to report any academic misconduct to the Dean of Students Office. **Any student found in violation of the code by cheating, plagiarizing or using any online software inappropriately will result in disciplinary action. This may include a failing grade of F, and/or suspension or dismissal from the university.** If you have any questions about the code of Academic Integrity, please contact the Dean of Students Office at dos@njit.edu

Course Learning Outcomes (CLO):

Student should be able to

1. design sequential circuits (using EEPROM) that meets a given design specification.
2. design hardware system that meets a given design specification and write VHDL program to implement them.
3. write lab reports documenting the results of the lab experiments.

Relevant ABET 1-7 Student Outcomes:

1. an ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics (CLO 1)
3. an ability to communicate effectively with a range of audiences (CLO 3)
6. an ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions (CLOs 1, 2)

Grading Policy

Quizzes & Final:	25%	
Lab.:	60%	
Demo:	40%	
Report:	20%	Writing (10%) Logic Diagram, Wiring Diagram, Software/Code comments, Timing Diagram, etc. (10%)
Pre-Lab:	15%	Logic Diagram/Tables, Wiring Diagram, Software/Code, Timing Diagram, etc.

Out of the 75% for Pre-Lab and Lab.: Lab. 2 is 5%. Lab. 1, 3, 4, 5, 6 are 10% each. Lab. 7 is 20%.

Lab report is due one week after the lab is completed. A sample lab report is available on canvas.
The quizzes will be conducted during the lecture.

Tentative Schedule

Week	Content
1	Syllabus
2	Lab 2
3	Lab 1
4	Lab 1 & 3
5	Lab 3
6	Lab 4
7	Lab 4
8	Lab 5
9	Lab 5
10	Lab 6
11	Lab 6
12	Thanksgiving
13	Lab 7
14	Lab 7