ECE 394-003: Digital Systems Lab
Fall 2023

Instructor: **Ahmad ALBarqawi**
email: aka87@njit.edu

Office hours: By appointment
Meeting times: Wednesdays 11:30-2:20 pm, FMH 204A

Text: *Laboratory Manual and Supplementary Notes: ECE 394 – Digital Systems Lab*, by Edwin Hou and Arthur Glaser (available via the ECE Department Laboratory web page at http://centers.njit.edu/ecelab).

All components needed to perform the experiments in this course are included in the ECE labs kit that students have obtained for use in previous lab courses. Spare parts are available for purchase from the IEEE store.

Description: Experiments emphasize digital design from basic electronic circuits to complex logic. Topics include switching speed, basic sequential circuits, the arithmetic/logic unit, and computer memories.

Course Outcomes:

1) The student will be able to design and construct combinatorial circuits using discrete logic gates.
2) The student will be able to design and construct sequential circuits using flip-flops.
3) The student will be able to design and construct more complex digital circuits using more complex digital components, including shift registers, counters, memory, and ALUs.
4) The student will be able to use CAD tools to program PLDs to implement combinational and sequential digital designs.
5) The students will be able to communicate their designs via written laboratory reports documenting the results of the lab experiments.
6) The student will be able to work in teams enhancing skills in leadership and contribution to a team.

Student Outcomes:

(b) an ability to design and conduct experiments, as well as to analyze and interpret data (CLO 1, 2, 3)
(c) an ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability (CLO 1, 2, 3)
(g) an ability to communicate effectively (CLO 5, 6)
(k) an ability to use the techniques, skills, and modern engineering tools necessary for engineering practice (CLO 4)

Course Schedule:

Week	Experiment	Topic
2-3	1	Logic Gates and Logic Families
4	2	Combinatorial Circuits
5-6	3	Sequential Circuits
7	4	Shift Registers
8	5	Gate Function Detector
9	6	Counters
10	7	Memory and ALU
11-13	8	Project: 4-bit RPN Calculator
14	8	Project Presentations

Grading Policy:

Experiments 1-7		10% each
Prelab:	30% (individual)	(70% total)
Lab Report:	70% (group)	
Final Project (Experiment 8)		30%
Prelab:	20% (individual)	
Presentation:	40% (individual)	
Lab Report:	40% (group)	

Notes:

- Prelabs are due by the beginning of class in the week before an experiment is being performed. No Prelab is required for Experiment #1.
- Individual effort will be considered in grading of all items. Teamwork is vital to success.

Honor Code: The NJIT Honor Code will be upheld, and any violations will be referred to the Dean of Students.