ECE 353-001: Computer Architecture and Organization (3-0-3)
Fall 2023

Instructor: John Carpinelli, 315 ECEC, (973) 596-3536
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Office hours: Wednesdays and Thursdays 1:00-2:15, ECEC 315
Meeting times: Mondays and Wednesdays 10:00-11:20, ECEC 100

Recommended Text: *Computer Systems Organization and Architecture*, Addison-Wesley, John D. Carpinelli, Boston, MA, 2001, ISBN # 0-201-61253-4.

Description: This course emphasizes the hardware design of computer systems. Topics include register transfer logic, central processing unit design, microprogramming, ALU design, pipelining, vector processing, micro-coded arithmetic algorithms, I/O organization, memory organization and multiprocessing.

Course Outcomes:

1) The student will be able to design the instruction set architecture for a processor to meet specific computer requirements.
2) The student will be able to evaluate the tradeoffs in the design of an instruction set architecture and the processor that implements it.
3) The student will be able to design a system to meet a given specification using register transfer language.
4) The student will be able to design a basic CPU given the instruction set architecture using either hardwired or microcoded control.
5) The students will be able to design a hierarchical memory system to meet a given specification.
6) The student will be able to design an I/O system to meet a given specification.

Student Outcomes:

1. An ability to identify, formulate, and solve engineering problems by applying principles of engineering, science, and mathematics (CLOs 1, 2, 3, 4, 5, 6).
2. An ability to apply both analysis and synthesis in the engineering design process, resulting in designs that meet desired needs (CLOs 1, 2, 3, 4, 5, 6).
6. An ability to recognize the ongoing need for additional knowledge and locate, evaluate, integrate, and apply this knowledge appropriately. (CLOs 3, 4).

Course Schedule:

Week	Topic
0	Finite State Machines
1	Instruction Set Architectures
2	Basic Computer Organization
3,4	Register Transfer Languages
4,5	CPU Design - Hardwired Control, ***Test #1***
6,7	Microsequencers Control Unit Design
8,9	Computer Arithmetic, ***Test #2***
10,11	Memory Organization
11,12	I/O Organization
13	RISC Processing, ***Test #3***
14	Parallel Processing

Grading Policy:	Homeworks	10%
	3 Tests @ 20%	60%
	Final Exam	30%

Homework and Test Requirements:

All homework assignments and due dates for the course are posted on Canvas. Homeworks are due at 10:00 AM on the due date. All homeworks will be submitted electronically as PDF file uploads on Canvas.

All test dates and times are listed in the course calendar on Canvas, and will be given in person during regular class meeting times. All tests are closed book and closed notes, except students may use one 8.5" × 11" double-sided sheet of notes of their own creation (3 sheets for the final exam). Students may use calculators that do not have wireless communication capabilities (i.e. no cell phone calculators).

Academic Integrity:

Academic Integrity is the cornerstone of higher education and is central to the ideals of this course and the university. Cheating is strictly prohibited and devalues the degree that you are working on. As a member of the NJIT community, it is your responsibility to protect your educational investment by knowing and following the academic code of integrity policy that is found at: http://www5.njit.edu/policies/sites/policies/files/academic-integrity-code.pdf.

Please note that it is my professional obligation and responsibility to report any academic misconduct to the Dean of Students Office. Any student found in violation of the code by cheating, plagiarizing or using any online software inappropriately will result in disciplinary action. This may include a failing grade of F, and/or suspension or dismissal from the university. If you have any questions about the code of Academic Integrity, please contact the Dean of Students Office at dos@njit.edu.