Helen and John C. Hartmann
Department of Electrical and Computer Engineering
New Jersey Institute of Technology
Digital Design (ECE-251)
Academic Year: 2023-2024
Term: Fall 2023

Instructor: A. Yousef
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Office: 324 ECEC
Office Hours/ Extra Help: Available upon request via email and Webex
Phone: 973-596-5692

Class Place & Time: Class Room: GITC 1400

Face-to-Face	Tuesday	6:00 PM – 9:00 PM – Lecture + Problem Solving
Face-to-Face	Tuesday	9:00 PM – 10:05 PM – Recitation + More Problem Solving + Solutions to Homework Assignments

Attendance: Required (class lectures and problem-solving sessions).
Cellular phones and Beepers: Shut off or in quiet mode.

Credits and Contact Hours: (3-1-3); 3 hrs. Lecture; 1 hr. Recitation, 3 credit hrs. = 4 contact hrs.

Method of Communique: NJIT Canvas – email

Text Book: *(Required)* Alan B. Marcovitz, Introduction to Logic Design, 3rd Edition, McGraw-Hill, ISBN # 978-0-07-319164-5

John D. Carpinelli, An Animated Introduction to Digital Logic Design, 1st Edition, Published by NJIT Library. https://digitalcommons.njit.edu/oat/1/
There is no cost to students or anyone, to use this book, either in a formal course or for self-study.

Lecture Notes: PowerPoint presentation slides supplied by professor.

Course Description: The design of combinational and sequential logic circuits used in digital processing systems and computers. Basic register transfer operations are covered. Topics include Boolean algebra, minimization techniques and the design of logic circuits such as adders, comparators, decoders, multiplexers, counters, arithmetic logic units, and memory systems.

Prerequisites: Phys 122

Course Learning Outcomes (CLO): The student will be able to:

1. Knowledge of the number systems and its conversion processes.
2. Use Boolean Algebra and minimize Boolean functions.
3. Construct various digital circuits using logic gates, latches and flip flops.
4. Design and implement basic combinational and sequential logic circuits.
5. Design and implement digital logic systems.
6. Knowledge of various digital electronic circuit parameters.
7. Familiarity with the various logic families (TTL, CMOS, ECL, etc.).

8. Analyze digital circuits in a multitude of possible applications
9. Use **Cadence OrCAD/**PSPICE or **NI MultiSim** software for circuit modeling and analysis.

Relevant Student Outcomes:

1. An ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics (CLO 1-4)
2. An ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors (CLO 3)
3. An ability to communicate effectively with a range of audiences (CLO3)
4. An ability to develop and conduct appropriate experimentation, analyze, and interpret data, and use engineering judgment to draw conclusions (CLO 3-4)

Exams:

1. Test 1 (20%) – Oct. 3, 2023 (week 5)
2. Test 2 (20%) – Nov. 7, 2023 (week 10)
3. Test 3 (25%) – Dec 5, 2023 (week 14)
4. Final (30%) – Dec. 19, 2023 (week 16; tentative)
5. Tests and final exams are closed notes and books

Homework Assignments:

HW Assignments (5%)

1. Submittal of solutions to homework assignments after the assigned due date will not be accepted.
2. Problems (marked with asterisk *) should be solved using Multisim or PSPICE (available in Computer Labs and for purchase as Student License).
   DOWNLOAD PSPICE STUDENT VERSION:
   https://www.ema-eda.com/products/cadence-orcad/orcad-academic-program
   DOWNLOAD GETTTING STARTED WITH MULTISIM STUDENT VERSION:
   http://www.ni.com/white-paper/10710/en

Course Withdrawal: Last day to withdraw from course: **Monday, November 13, 2022**

Mandates and Extenuating Circumstances:

1. In order to ensure consistency and fairness in application of the NJIT policy on withdrawals, student requests for withdrawals after the deadline *(end of the 10th week of classes)* will not be permitted unless extenuating circumstances are documented through the Office of the Dean of Students. The course instructor and the Dean of Students are the principal points of contact for students considering withdrawing from a course.
2. The student should contact the Dean of Students Office regarding extenuating circumstances for any reason (late withdrawal from a course, request for a make-up exam, request for an incomplete grade). The Dean of Students make the determination of whether extenuating circumstances exist or not and will be notifying the instructor accordingly. Please do provide the instructor with your medical or other documents; such documents need to be submitted by the student to the Dean of Students. Except for cases determined by law, the instructor is not required to accommodate student requests even when extenuating circumstances are certified by the Dean of Students.

Undergraduate Grading Policy:

Grades	Significance	Average Score
A	Superior	(90 – 100)
B+	Excellent	(85 – 89)
B	Very Good	(80 – 84)
C+	Good	(75 – 79)
C	Acceptable	(70 – 74)
D	Minimum	(65 – 69)
F	Inadequate	(<65)
AU	Audit	
I	Incomplete. Grade deferred--**given in rare instances** to students who would normally have completed the course work but who could not do so because of special circumstances. If this grade is not removed during the next regular semester, a grade of F will result.	
W	Withdrawn	
S	Satisfactory	
U	Unsatisfactory	

In all departments in the College of Science and Liberal Arts, a grade of C or higher is required in any lower division course (200 level and below) that serves as a prerequisite for another course.

NJIT Honor Code:

"Academic Integrity is the cornerstone of higher education and is central to the ideals of this course and the university. Cheating is strictly prohibited and devalues the degree that you are working on. As a member of the NJIT community, it is your responsibility to protect your educational investment by knowing and following the academic code of integrity policy that is found at: http://www5.njit.edu/policies/sites/policies/files/academic-integrity- code.pdf.

It is my professional obligation and responsibility to report any academic misconduct to the Dean of Students Office. Any student found in violation of the code by cheating, plagiarizing, or using any online software inappropriately will result in disciplinary action. This may include a failing grade of F, and/or suspension or dismissal from the university. If you have any questions about the code of Academic Integrity, please contact the Dean of Students Office at dos@njit.edu"

Course Material: Chapter/Sections indicated in black font = Alan B. Marcovitz, Introduction to Logic Design, 3rd Edition
Chapter/Sections indicated in Green Italics font = John D. Carpinelli, An Animated Introduction to Digital Logic Design, 1st Edition

Date	Week #	Chapter/ Sections	Topics
Sept 5	1	CH 1 Sections 1.1 – 1.2 *CH 1 Sections 1.1 – 1.3*	**Course Overview:** • Course Syllabus and Expectations - Required Textbook & Grading Policy • Introduction to Digital Logic Design – About Digital Design, Analysis vs. Design, Design Process Flow, The Design Procedure, The Digital Revolution, Signal Types, The Need for ADC and DAC, Advantages & Disadvantages of Digital Systems, Switches and Bits **Introduction to Number Systems:** • Decimal, Binary, Arbitrary Radix/Base Representation • Conversion Between Bases – Decimal to Binary, Decimal to Octal, Decimal to Hexadecimal, Binary to Decimal, Octal to Decimal, Hexadecimal to Decimal, Octal to Binary & Binary to Octal Hexadecimal to Binary & Binary to Hexadecimal
Sept 11	2	*Last day to add/drop a class with 100% refund*	
Sept 12	2	*W grade posted for course withdrawal*	
Sept 12	2	CH 1 Sections 1.2 – 1.5 *CH 1 Sections 1.4 – 1.7*	• Addition, Subtraction, Multiplication and Division of Binary, Octal and Hexadecimal Numbers • Representation of Positive & Negative Numbers Using Signed-magnitude, r's complement, (r-1)'s Complement • Binary Subtraction Using r's complement, (r-1)'s Complement • Overflow in Binary Addition • Floating Point Numbers **BCD and Other Code Types:** • Binary Coded Decimal (BCD) Code and BCD Addition • Excess 3 Code and Excess 3 Addition • ASCII Code • Gray Code, Gray Code to Binary Conversion • What is Parity? Hamming Code Detection & Correction
Sept 19	3	CH 2 Sections 2.1 – 2.12 *CH 2 Sections 2.1 – 2.2* *CH 3 Sections 3.1 – 3.4*	***Combinational Systems:*** **The Design Process for Combinational Systems** • Don't Care Conditions • Development of Truth Tables **Switching Algebra** • Boolean Algebra Fundamentals • Boolean Algebra Properties – Postulates and Theorems • Manipulation of Algebraic Functions • Sum of Products (SOP), Products of Sums (POS) Representations • Implantation of Functions With Basic Logic Gates (AND, OR, NOT, NAND, NOR, XOR XNOR) • From Truth Table to Algebraic Functions • Simplification of Algebraic Expressions • Manipulation of Algebraic Functions and NAND Gate Implementations

Date	Week #	Chapter/ Sections	Topics
Sept 26	4	CH 3 Sections 3.1 – 3.9 *CH 2 Sections 2.3*	**The Karnaugh Map:** • Introduction to the Karnaugh Map (K-Map) • 2-Variable, 3-Variable & 4-Variable K-Map • Minimum Sum of Products Expressions Using K-MAP • Don't Care Conditions in K-Map • Minimum Products of Sums Expressions Using K-MAP • 5-Variable & 6-Variable K-Map • Multiple Output Problems
Oct 3	5	*Test 1 (2.5 hrs. exam)*	
Oct 10	6	CH 4 Sections 4.1 – 4.9 *CH 2 Sections 2.3*	**Function Minimization Algorithms:** • Quine-McCluskey Minimization Technique • Prime Implicant Tables for One Output • Quine-McCluskey for Multiple Output Problems • Prime Implicant Tables for Multiple Outputs
Oct 17	7	CH 5 Sections 5.1 – 5.5 *CH 4 Sections 4.1 – 4.8*	**Designing Combinational Systems:** • Beyond Logic - Propagation Delay, Fan-In, Fan-out, Buffers • Noise Margin • Adders (Half, Full, Ripple, Carry-lookahead Adders) • Subtractors and Adder/Subtractor • Comparators • Binary Decoders (BCD to Seven Segment Display Decoder) • Encoders and Priority Encoders • Multiplexers and Demultiplexers • Tri-State Gates • Code conversion (Decimal to BCD, Octal to Binary, Hexadecimal to Binary, BCD to Binary, Excess 3 to Binary)
Oct 24	8	CH 5 Sections 5.6 – 5.11 *CH 10 Sections 10.1 – 10.4*	**More Complex Combinational Systems** • Gate Arrays Programmable Logic Devices (PLDs) – ROMs, PLAs and PALs • ROM Lookup Circuits • Testing and Simulation of Combinational Systems
Oct 31	9	CH 6 Section 6.1 – 6.7 CH 6 Sections 6.1 – 6.4	***Sequential Systems:*** **Sequential Components:** • Modeling Sequential Circuits (Clock, Timing Diagrams) • Clock (Oscillator) Design • Asynchronous Sequential Circuits • Latches (NOR and NAND S-R Latch, D-Latch) • Differences between Latch and Flip-Flops • Truth Table, Characteristic Table and Excitation Table for D Flip-Flop, J-K Flip-Flop, T Flip-Flop • Master-Slave J-K Flip-Flop • Master-Slave D Flip-Flop • Triggering Methods in Flip-Flops • Race Conditions in J-K Flip-Flop

Date	Week #	Chapter/ Sections	Topics
			• Flip-flop Conversion: J-K to D, T to D, S-R to JK, S-R to T
Nov 7	10	*Test 2 (2.5 hrs. exam)*	
Nov 13	*Last day to withdraw from class*		
Nov 14	11	CH 7 Sections 7.1 – 7.7 *CH 8 Sections 8.1 – 8.5*	**Sequential Circuits:** • Finite State Machines (State Table, State Diagram & State Equations) • Mealy and Moore State Machines • Design Process • Design Example – Mealy State Machine • Design Example – Moore State Machine • Design Using a Counter • Design Using a Decoder • Design Refinement (Unused States, Equivalent States, Glitches)
Nov 21	12	*No Class*	
Nov 28	13	Ch. 8 Sections 8.1 – 8.11 *CH 7 Sections 7.1 – 7.8*	**More Complex Sequential Components:** • Linear Shift Registers • Shift Register Design using D and J-K Flip-Flops • Bidirectional Shift Registers • Shift Registers with Parallel Load • Combining Shift Registers • Binary Counter Design (Down-counter, Up/Down-Counter, Ripple-Counters) • Synchronous Counters • BCD Counters • Modulo-n Counters
DEC 5	14	CH 9 Sections 9.1 – 9.6	**Asynchronous Sequential Circuits:** • Overview and Model • Design Process • Analysis Example • Design Example • Unstable Circuits • Static and Dynamic Hazards • Recognizing and Resolving Static Hazards • Race Conditions (Critical and Non-Critical) • Resolving Critical Race Conditions
Dec 12	15	*Test 3 (2.5 hrs. exam)*	
Dec 12	15	*Classroom Review for Final Exam*	
Dec 19	16	*Final Exam (2.5 hrs. exam)*	