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ABSTRACT

CHARACTERIZATION OF LOW POWER HfO_2 BASED SWITCHING DEVICES FOR IN-MEMORY COMPUTING

by
Aseel Zeinati

Oxide based Resistive Random Access Memory (RRAM) devices are investigated as one of the promising non-volatile memories to be used for in-memory computing that will replace the classical von Neumann architecture and reduce the power consumption. These applications required multilevel cell (MLC) characteristics that can be achieved in RRAM devices. One of the methods to achieve this analog switching behavior is by performing an optimized electrical pulse. The RRAM device structure is basically an insulator between two metals as metal-insulator-metal (MIM) structure. Where one of the primary challenges is to assign an RRAM stack with both low power consumption and good switching performance.

This thesis investigates different HfO_2 based RRAM stacks and compares their electrical and MLC characteristics. By engineering the distribution of defects and oxygen vacancies in the switching layer, which have been done by exposing the dielectric with a hydrogen plasma treatment in the first device, using HfO_2 and Al_2O_3 as a bilayer, or by adding Zr to the HfO_2. While the plasma treated devices show a promising conductance quantization with low power consumption, the performance can be further enhanced by engineering the bottom electrode. The impact of introducing additional nitrogen at the bottom electrode, TiN, shows additional reduction in the switching power of the plasma treated devices.

CHARACTERIZATION OF LOW POWER HfO_2 BASED SWITCHING DEVICES FOR IN-MEMORY COMPUTING

by
Aseel Zeinati

A Thesis
Submitted to the Faculty Of
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May 2023

APPROVAL PAGE

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Zeinati, A., and Naser, S.; "Design and Implementation of RF Energy Harvester", Bs project in JUST, January 12, 2013.

“Verily, knowledge only comes by learning and continue learning, and forbearance only comes by cultivating forbearance.”

-The prophet Muhammad.

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Lastly, I would be remiss in not mentioning my sister Rahmah and my brothers; Mohammad, Abdelrahman, Saleh and Khaled for their emotional support.

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CHAPTER 1

INTRODUCTION

1.1. Background

Today's computing systems are built based on the Van Neumann architecture, with a separated memory and processing units. Data must move between the processing and the memory units back and forth and cause a memory wall problem. With the development of artificial intelligent and machine learning applications, with large data the Van Neumann architecture cannot meet the demand of these applications. To overcome such a problem in-memory computing is a promising solution with large datasets, discrete and random memory access [1, 2]. Figure 1.1a shows the conventional computing system that built using Van Neumann architecture performed an operation f on data set D, D must move back and forth and this costs latency and energy, where Figure 1.1b shows the in-memory computing system using crossbar structure [1].

In-memory computing is an alternate approach where computing performed within the memory unit that is organized in an array as a crossbar [3] shown in Figure 1.2 [6]. Each node in this crossbar has a memory element for an extremely low power consumption and high efficiency of data movement [4]. Each memory element in the crossbar could be charge-based memory in terms of presence or absence of the charge, such as SRAM, DRAM, and flash memory [7], or resistance-based memory in terms of the differences in the atomic arrangements

or orientation of ferromagnetic metal layers, such as RRAM, PCM, FeRAM and STTRAM [8].

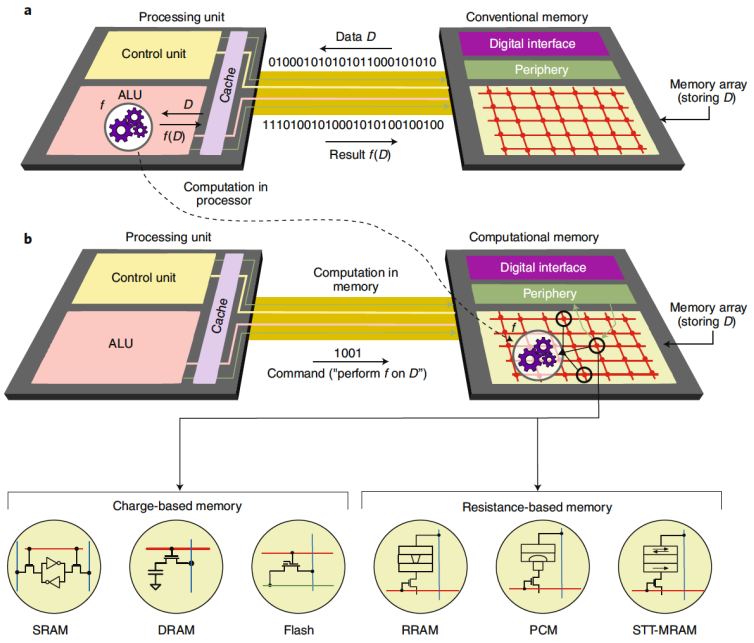


Figure 1.1 In-memory computing. (a) in a conventional computing system. (b) in-memory computing.
Source: [1].

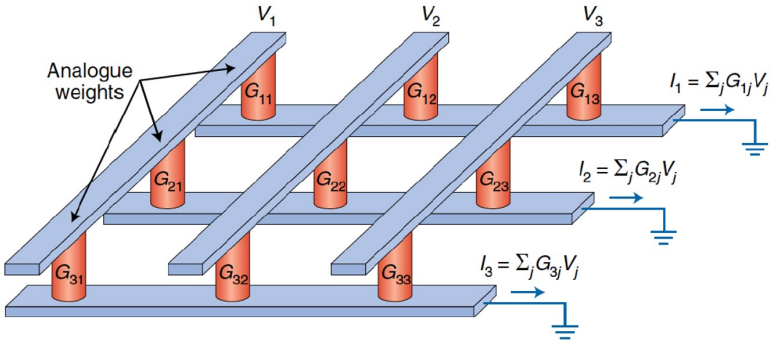


Figure 1.2 Crossbar arrays for in-memory computing.
Source: [6].

1.2. Emerging Nonvolatile Memory

Memory devices is the core of any computing system. There are two types of memory based on their ability to hold the information after removing the power source: volatile memory such as DRAM and SRAM which lose the information once the power is off, and nonvolatile memory that also can be classify in to two groups; baseline memory like flash memory and emerging memory like RRAM. Figure 1.3 shows the memory hierarchy [5].

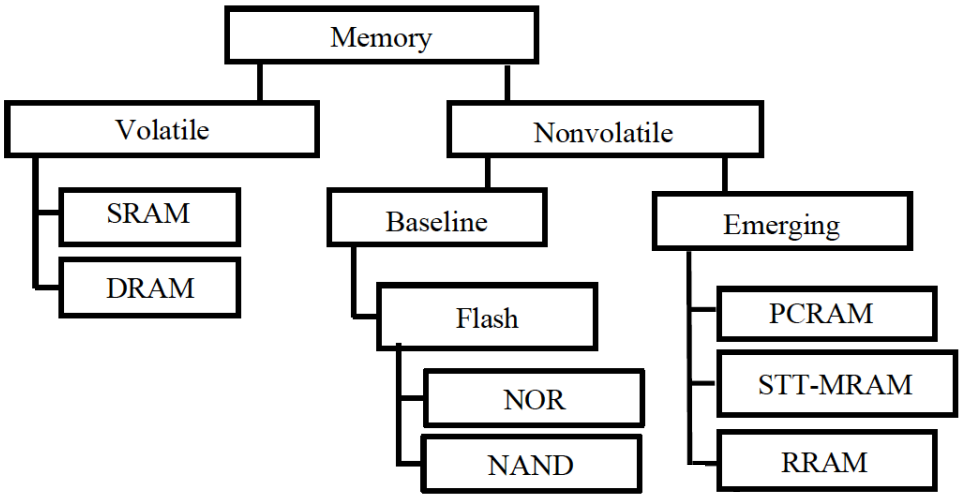


Figure 1.3 The memory hierarchy.
Source: [5].

SRAM consumes a large area due to its six-transıstor (6T) structure which reduce its density data storage [8]. While DRAM requires large programming voltages, and capacitor leakage issues limited the data storage capacity [9]. Flash memory has high density data storge since it can be stacked in 3D structure, but requires long programming read times (around milliseconds), and that increases its programming power [10]. All these memories SRAM, DRAM and Flash are

based on complementary metal oxide semiconductor (CMOS) technology that reach its scale limit due to Moore's law [11]. This opens the way to the emerging non-volatile memory technology due to its low consuming power, high density and doesn't have the scalability issue, since it has very simple structure. Some of the types of emerging non-volatile memory devices that's active in the research area are phase change memory (PCM), spin transfer torque magnetic random-access memory (STTRAM), and resistive random-access memory (RRAM).

The emerging non-volatile memory devices are resistance-based memory, which can be programed to store information through changing in their resistance state by applying an electric field.

1.2.1. Phase-Change Memory (PCM)

This type of memory takes a mushroom cell structure which is the shape of the switching volume above a heater, as shown in Figure1.4. By heating the material above its crystallization temperature with a sequence of longer width and lower amplitude pulses the device enter its low resistance state LRS (crystalline), while using a short width and high amplitude voltage pulses and subsequent rapid cooling will perform an abrupt melt-quench process the device enter its high resistance state HRS (amorphous). Repetitive crystallization reduces amorphous thickness gradually and led to multiple programmable states in PCM devices [12].

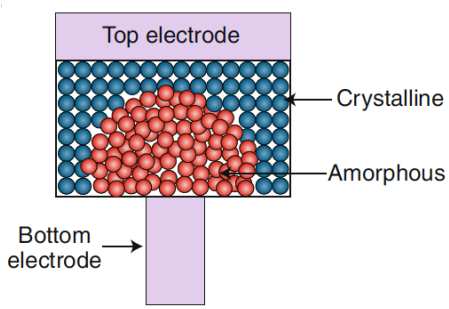


Figure 1.4 Phase-Change Memory (PCM) structure.
Source: [1].

1.2.2. Spin Transfer Torque Magnetic RAM (STTRAM)

This type of memory has a structure known as magnetic tunnel junctions as shown in Figure 1.5 which is basically two ferromagnetic layers sandwiching a spacer layer (commonly MgO). The device could be programed into two states depending on the electron spin inside the ferromagnetic layers by passing a spin-polarized current, which initiates a phenomenon called STT [13].

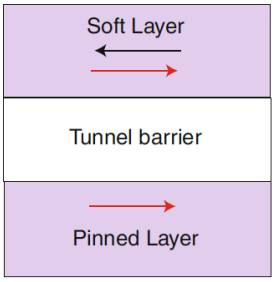


Figure 1.5 STTRAM structure.
Source: [1].

1.2.3. Resistive Random-Access Memory (RRAM)

This type of memory is built as metal insulator metal structure (MIM) structure as shown in Figure 1.6. The change in its resistance state done by applying a SET electric field to the top electrode. A conductive filament (CF) is formed and let the

device enter low resistive state (LRS), while applying a RESET electric field will rupture the CF and the device will enter the high resistance state (HRS).

There are two types of RRAM based on the switching mechanisms. The conductive-bridge RAM (CBRAM), which depend on the fast-diffusing Ag or Cu ions into the oxide to form a conductive bridge [14]. The other type is the binary metal oxide RRAM, where the CF is formed by oxygen vacancies (V_o) after the oxygen ions leave the oxide toward the top electrode.

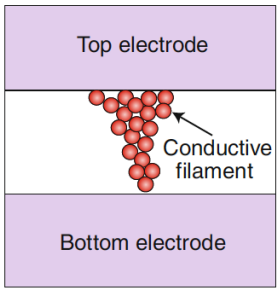


Figure 1.6 RRAM structure.
Source: [1].

1.3. Motivation of this Work

The motivation of this work is to investigate different RRAM stack that works that will have multilevel programable devices with low power consumption, strong endurance, and a good reliability. These devices need to have an appropriate distribution of V_o to reduce power and enhance performance. This can be achieved by modifying process conditions for the switching layer deposition and for engineering the electrode materials. The characteristics can be evaluated using pulse operation. Then the promising RRAM device can be used for in memory computing with low power consumption.

1.4. Thesis Organization

Chapter 1 introduce the computing systems and the needs of in-memory computing approach, with list of some of non-volatile memories and their properties.

Chapter 2 presents previous studies on selecting RRAM stack materials. Comparison of the top electrode metal such as Ru and TiN and comparison of the different deposition process such as hydrogen plasma treatment in HfO_2. Different position of the caping layer Al_2O_3 in a HfO_2/Al_2O_3 bilayer structure is also discussed.

Chapter 3 describe the experimental setup of this work. The electrical characterization such as the forming process, the pulse operations with width variation, amplitude variation, and the endurance test are outlined.

Chapter 4 presents the results of four devices with different switching dielectrics, HfO_2-Treated, HfO_2, HfO_2/Al_2O_3 and hafnium-zirconium oxide (HfZrO) with same top and bottom electrodes.

Chapter 5 presents the experimental setup, the devices structures, the results of three devices that have the same top electrode and the switching dielectric but with different bottom electrodes to study the impact of controlling the nitrogen level in the bottom electrode.

Chapter 6 present the conclusion of the is work followed by the suggestion of the future work.

CHAPTER 2

RRAM TECHNOLOGY REVIEW

RRAM devices is known as memristor (short for memory and resister) was discovered by a distinguished faculty member in the Electrical Engineering and Computer Sciences Department of the University of California Berkeley Leon Chua in 1971 as the fourth fundamental element beside resistors, capacitors and inductors as shown in Figure 2.1.

Hewlett Packard (HP) labs formulate a physics-based model of a memristor and fabricated nanoscale MIM devices in 2008 and proved the work of the memristor as a resister with memory (state). The I-V characteristics of HP's first working RRAM device is shown in Figure 2.2. The inset in Figure 2.2 shows the dielectric layer, TiO_2, sandwiched between two electrodes made of Pt. [15, 16].

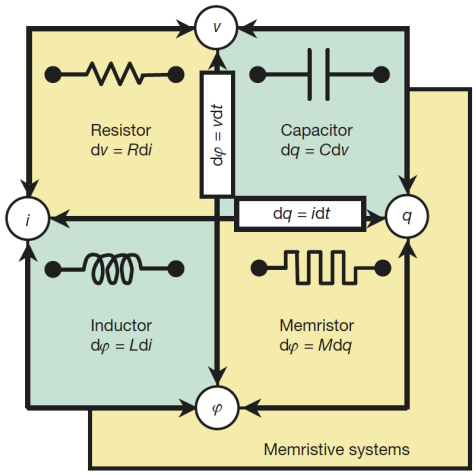


Figure 2.1 The four fundamental two-terminal circuit elements: resistor, capacitor, inductor and memristor.
Source: [16].

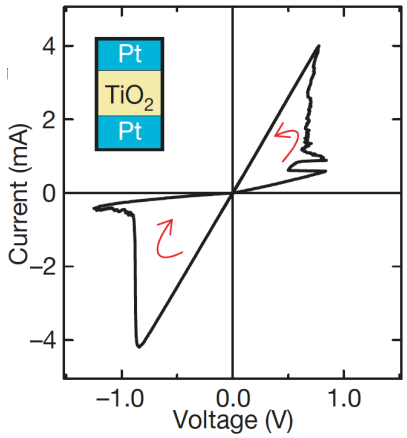


Figure 2.2 HP first working memristor with simulated I-V curve.
Source: [16].

The properties of the memristor make it a promising device to be used for in-memory computing systems. Because of its simple structure the device is highly scalable. This device can make the memory system high speed, allow high storge density, enhance endurance and retention. It has the advantage of being compatible with the conventional CMOS fabrication environment.

2.1. RRAM Switching Mechanism

The switching mechanism for the fresh RRAM devices starts with forming process. Where the device initially in the HRS with randomly distributed defects in the oxide layer, also known as the switching layer, as shown in Figure 2.3.A [18]. The bottom electrode (BE) is grounded, and a DC sweep with compliance current (I_{cc}) is applied to the top electrode (TE). Figure 2.3.B shows how the oxygen ions move toward the TE after applying the DC sweep and a conductive filament (CF) formed inside the switching layer. The CF lowers the resistance value of the device like a dielectric soft breakdown where the device entered the LRS. This process is called

the forming process. When the electric field reversed the CF ruptured and the device entered HRS again, this process called RESET. After the forming and RESET process a SET operation is performed by applying the electric field with an I_{cc}. The I_{cc} prevents the device from being damaged. During the SET operation the CF is reconstructed, and the device entered the LRS as shown in Figure 2.3 (E).

After forming, the RRAM device consumes less power for SET process because the CF is partially ruptured during the RESET process. The top of the CF after RESET becomes a virtual BE. The I-V curve, shown in the left side of Figure 2.3 [17,18], represents the above behavior.

The former discussed RRAM switching mechanisms is for a mode of RRAM devices called bipolar RRAM where the RESET performed by applying electric field with an opposite polarity of the SET electric field. In the other mode of RRAM known as unipolar, the SET and RESET both have the same polarity. Figure 2.4 shows the I-V curves of the two-operations mode unipolar and bipolar.

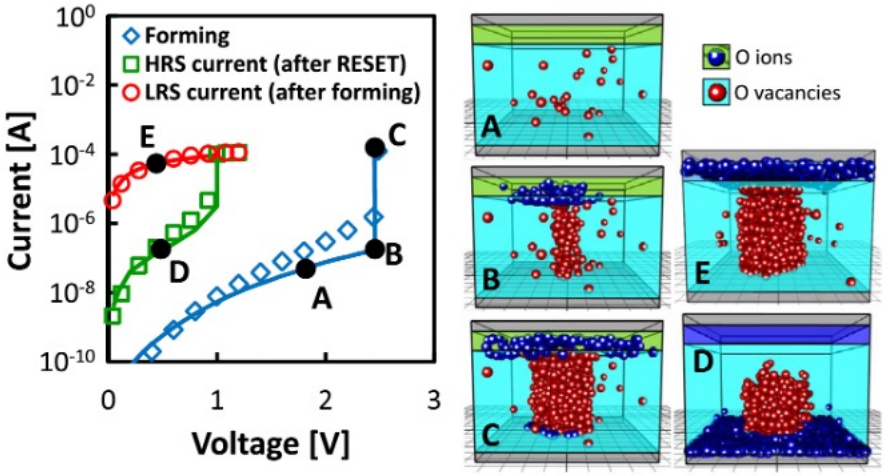


Figure 2.3 I-V characteristics of forming, LRS after SET and HRS after RESET of RRAM device and evolution of oxygen ions and oxygen vacancies distributions during forming (A)-(C), after RESET (D) and after SET.
Source: [18].

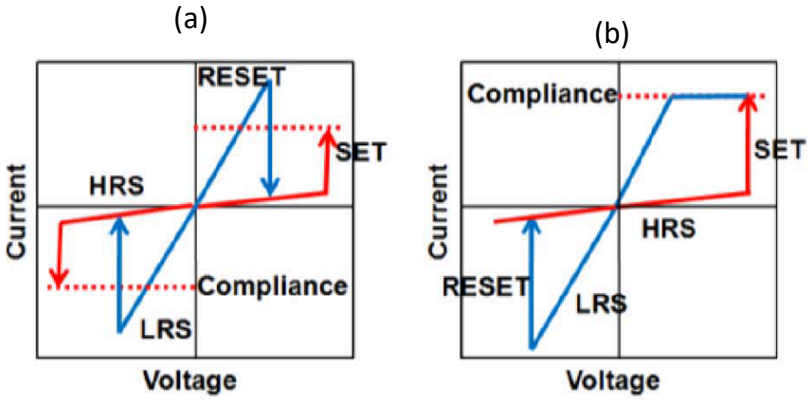
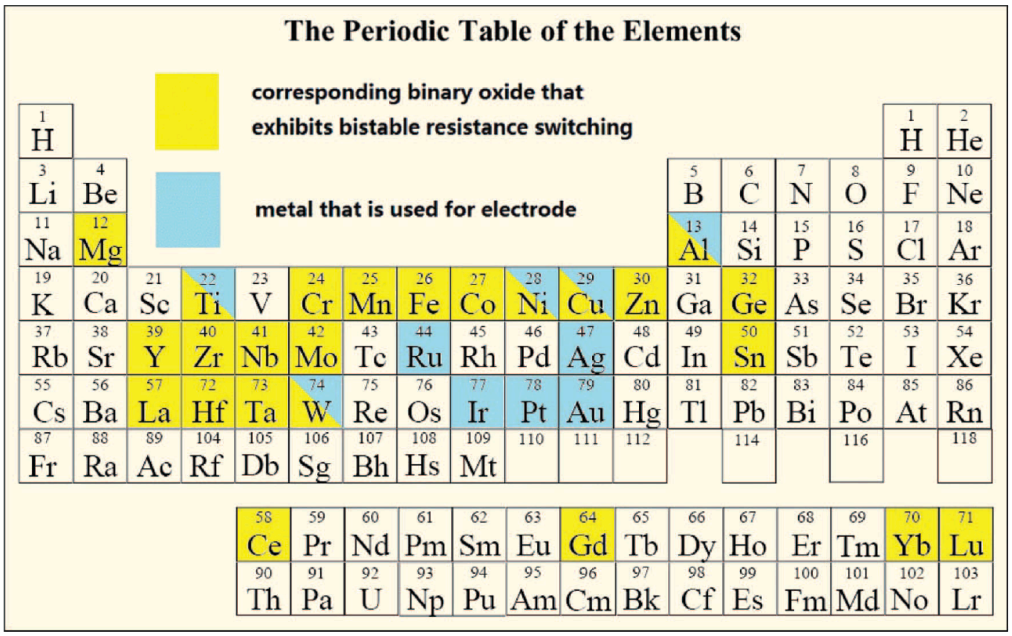


Figure 2.4 I-V curves showing the two modes of operation: (a) unipolar, (b) bipolar. Source: [19].

Table 2.1 The Materials That Have Been Used for Binary Metal Oxide RRAM. Metals of the Corresponding Binary Oxides Used for the Resistive Switching Layer Are Colored in Yellow. Metals Used for the Electrodes Are Colored in Blue. Source: [17].



2.2. RRAM Structure

The RRAM structure as mentioned before is basically an oxide sandwiched between two electrodes. While characterizing the RRAM devices the material of the oxide and the two electrodes impact the electrical and physical properties.

When the RRAM devices is used in the computing systems it will be integrated with conventional CMOS in a one-transistor–one-resistor (1T1R) device structure.

There are many of metal oxides that could be used as the switching layer in RRAM devices, such as HfO_x, AlO_x, NiO_x, TiO_x, and TaO, they also known as transition metal oxides. The materials for the oxide layer and the electrodes are summarized in Table 2.1 [17].

The TE, such as TiN, Pt, Ru, TaN act like an oxygen ion receiver when the electric failed is applied to it. The switching characteristics of the RRAM devices relays on the interface between TE and the switching layer that's explain the focus of several studies on the properties of this interface and how to control the oxygen ions flow on it. On the other hand, the BE properties also impact the performance of the RRAM devices.

2.3. HfO_2 as Switching layer

HfO_2 is a high k martial with a band gab of (~5.6 ev) that has been used in fabricating RRAM devices since 2012 [20]. It's one of the most mature oxides that have been used as a switching layer in RRAM because it is enriched with defects [18]. In addition, its computable with CMOS technology, very well understood dielectric, has a good endurance, high reliability, and consumes low power.

The functional properties of HfO_2 depend on its defect structure [21], the stoichiometric HfO_2 is one of the options to be used as switching layer in RRAM but due to its lack of oxygen vacancies (V_o) it consumes large power than the non-stoichiometric HfO_x. the former HfO_x has more defects but it's very difficult to

control which led to unstable CF, in addition to complicated fabrication process of this type of oxides.

Increasing the density of V_o near the top electrode seems to streamline the switching characteristics. While controlling V_o distribution in HfO_2 is, therefore, required doped HfO_2, by introducing hydrogen plasma treatment in the middle of HfO_2 layer [22], or by making HfO_2/Al_2O_3 bilayer structure [23].

2.3.1. HfO_2 with Hydrogen Plasma Treatment

It has been reported that more V_o near the TE reduced the switching power and improve the performance of the RRAM device [22]. The study that has been done in [24] investigated the efficient position to introduce the H-plasma as shown in Figure 2.5. When the H-plasma was inserted between 4nm and 1nm of HfO_2 as appeared in Figure 2.5a, thinner cap layer was not able to reoxidize the defects and the distribution of V_o related defects became uniform throughout the dielectric thickness. That led to a higher forming voltage. For thicker cap layer as Figure 2.5b the reoxidation followed by V_o migration toward the top reduces the forming voltage, while introducing the H-plasma in the midpoint of the HfO_2 layer as shown in Figure 2.5c increases the V_o related defects close to the TE that significantly decreased the switching power for filament formation. Figure 2.6 [22] shows I-V curve of two DC sweep applied to the TE of TiN/ HfO_2 with H-plasma in the midpoint/TiN stack with the lowest I_{cc}= 50nA [22].

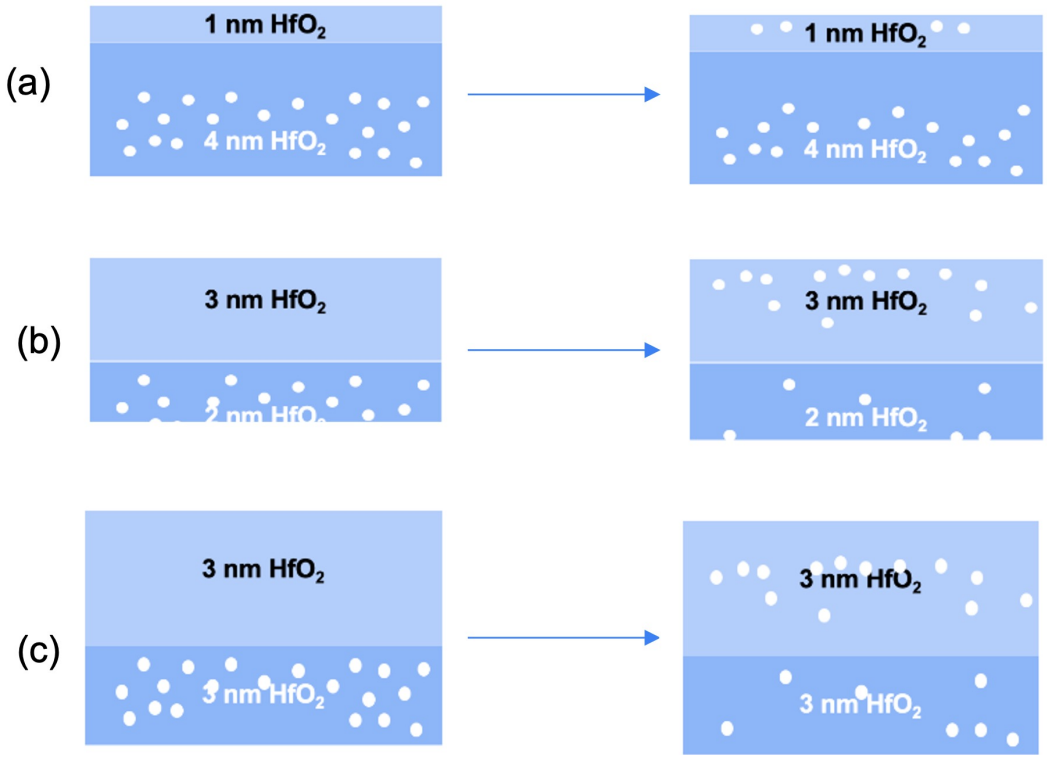


Figure 2.5 The impact of introducing H-plasma in the HfO_2 layer, (a) after depositing 4 nm of HfO_2 then followed by 1 nm of HfO_2, (b) after 2 nm of HfO_2 then followed by 3 nm of HfO_2 (c) in the midpoint of 6 nm HfO_2 layer.

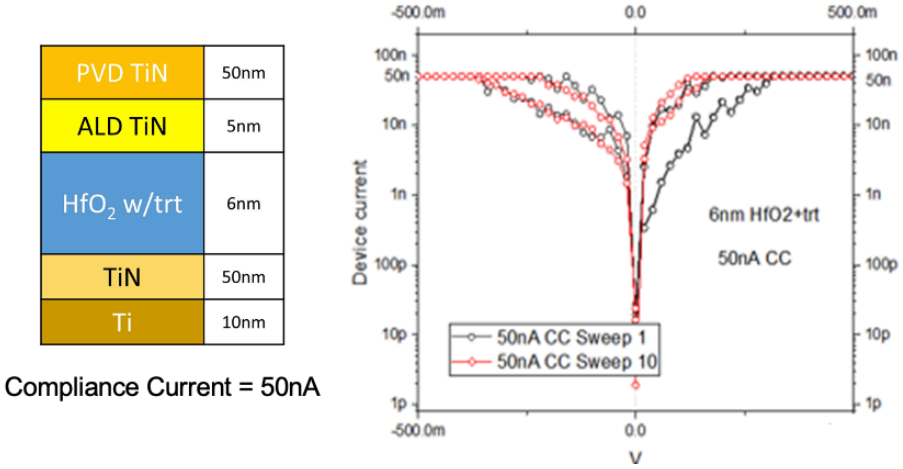


Figure 2.6 On the left the schematic of the device, on the right the I-V curves of two DC sweep of RRAM stack using HfO_2 with H-plasma in the midpoint and TiN as TE.
Source of the I-V curves: [22].

2.3.2. HfO_2/Al_2O_3 bilayer

There are several methods to control the V_o distribution near the TE rather than introducing H-plasma treatment. Caping the HfO_2 with Al_2O_3 showed reasonable control on V_o. The position of this caping layer has been investigated in [26]. The study shows the impact of depositing 1 nm Al_2O_3 between the switching layer and the BE as shown in Figure 2.7, and of depositing 1 nm Al_2O_3 between the switching layer and the TE as shown in Figure 2.8. The former device shows lower forming power because the V_o are formed relatively faster in Al_2O_3 layer than in HfO_2 layer, once they are formed in Al_2O_3 they stimulate generation for more V_o in HfO_2. In addition, the study found that reducing the thickness of the Al_2O_3 didn't improve the behavior of the device as shown in Figure 2.9 [26].

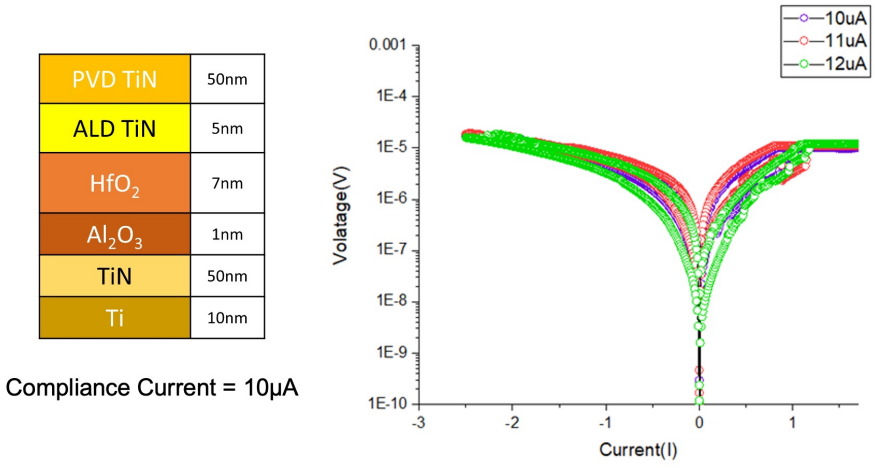


Figure 2.7 On the left the schematic of the device, on the right the I-V curves of three DC sweep of RRAM stack using 7 nm HfO_2 with 1 nm Al_2O_3 near BE.
Source of the I-V curves: [26].

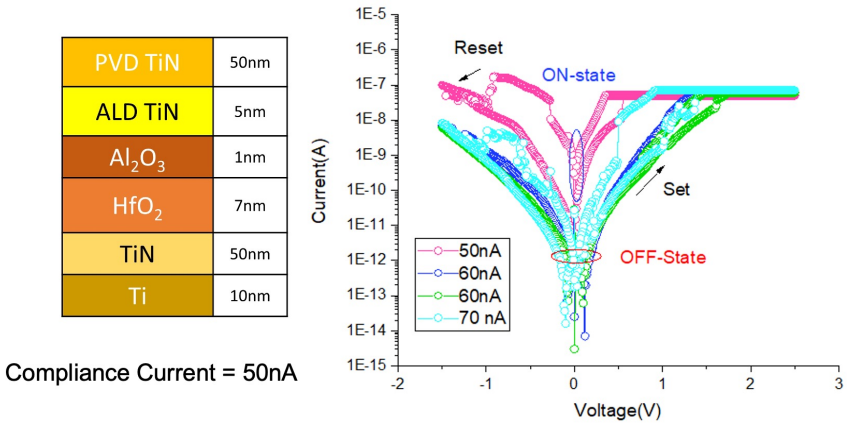


Figure 2.8 On the left the schematic of the device, on the right the I-V curves of four DC sweep of RRAM stack using 7 nm HfO_2 with 1 nm Al_2O_3 near TE.
Source of the I-V curves: [26].

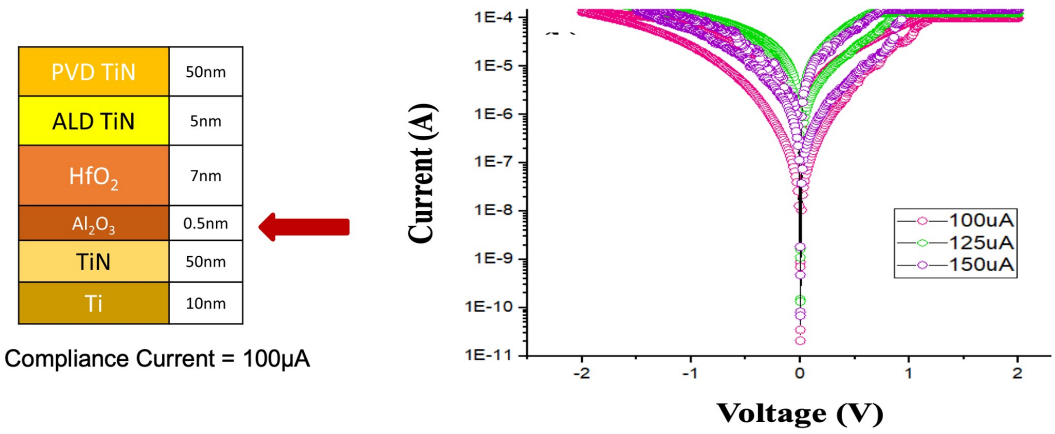


Figure 2.9 On the left the schematic of the device, on the right the I-V curves of three DC sweep of RRAM stack using 7nm HfO_2 with 0.5 nm Al_2O_3 near BE.
Source of the I-V curves: [26].

2.4. Impact of Top Electrode

The properties of the TE playing a significant role in power reduction since the interface of it with the switching layer impact the V_o distribution. Higher work function determines a stable resistive switching but the change in barrier height between metal and the dielectric dominates the switching power. Figure 2.10

imported from [22] shows how using Ru as a TE with treated switching layer with H-Plasma instead of TiN with the same switching layer (Figure 2.6) reduced the I_{cc} from 50 nA to 3 nA. The work function of Ru/HfO_2 is (4.6 eV) which is slightly higher than TiN (4.5 eV). Also, the defects in the switching layer and metal-induced gap states control the barrier height and effect the switching behavior [22].

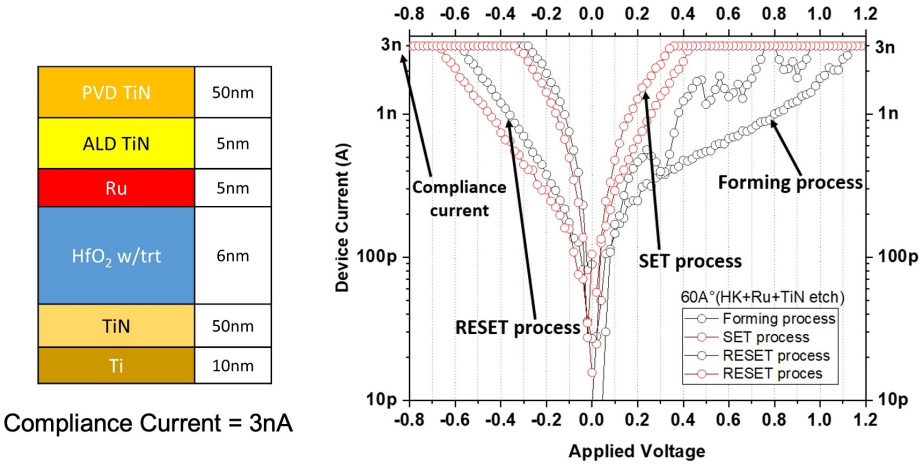


Figure 2.10 on the left the schematic of the device, on the right the I-V curves of two DC sweep of RRAM stack using HfO_2 with H-plasma in the midpoint and Ru as a TE.
Source of the I-V curves: [22].

2.5. MLC for In-Memory Computing

The purpose of studying different RRAM stack is finding the low power device to be used for in-memory computing. Such a device should have multi-level cell characteristics (MLC) where we can store more than two bits per the device. This behavior could be achieved in RRAM devices by several method like applying different DC sweeps while changing I_{cc}. The former method is not practical for in-memory application since it consumes large power while programing, where other method like applying programing pulses shows a reasonable characteristic that

make the RRAM devices a promising non-volatile memory to be used in a crossbar for in-memory computing [18]. The programing pulses could be a SET or RESET train of pulses, either by fixing the pulse amplitude and varying the pulse width, or by fixing the pulse width while varying the pulse amplitude, in this work we performed both methods and compared their advantages and disadvantages.

While studying the MLC for any device we are looking for enough conductance (G) window between any two states, uniformity of each conductance state, a good cycling endurance for each state, thermal stability of the stored data in each state, and good immunity of read disturbance [19], Figure 2.7 shows some MLC characteristics that have been mentioned for a pulse measurement of an RRAM device that has a dielectric of 6nm HfO_2 with H-Plasma treatment at the midpoint.

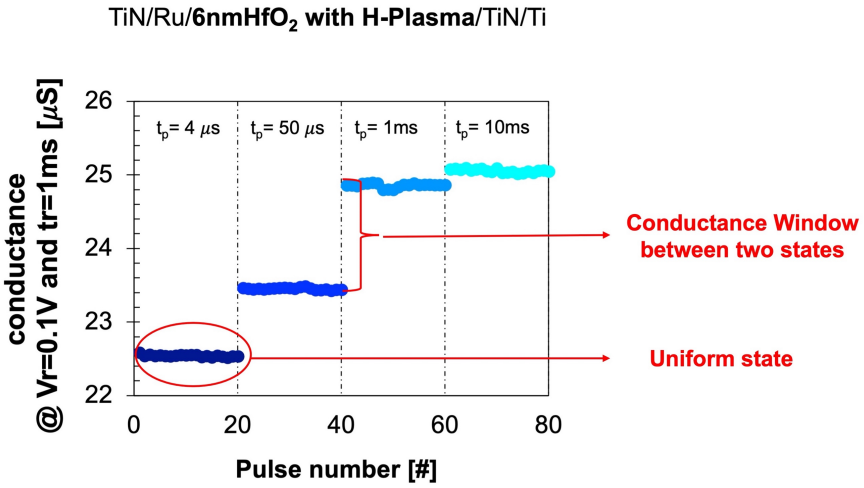


Figure 2.11 MLC Characteristics of pulse measurements data for treated HfO_2.

CHAPTER 3

EXPERIMENTAL SETUP

3.1. Devices Structures

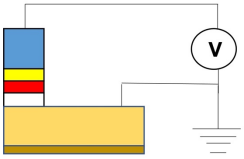
The challenges of selecting the RRAM stack are active research for better reliability, good endurance, reasonable quantization in MLC, and low power consumption. In this work we investigated seven different stacks, that have similar active area diameter of 300 μm.

The first four devices have been compared with fixed TE as (PVD TiN/ ALD TiN/Ru), and BE as (PVD TiN/ PVD Ti), while varying the dielectric in the switching layer. All the switching layers deposited using atomic layer deposition technique (ALD) which is executed on TEL Trias^{+TM} platform with shower-head type 300mm reactor [25].

Later in chapter 5 the other three devices will be presented. These devices have similar TE as (PVD TiN/ ALD TiN) and switching layer as HfO_2 with H-Plasma treatment, but different BE to study the impact of controlling TiN.

The four devices with different switching layer schematic shown in Figure 3.1, where device-A dielectric is 6nm HfO_2 treated with H-Plasma in the middle, where introducing the plasma showed significant impact on the switching behavior [22] as mentioned in the previous chapter and will be prove by the results in the following chapter. Device-B dielectric is 7nm stochiometric HfO_2, which has lack of V_o that effect the switching behavior. Device-C dielectric is bilayer 7nm HfO_2 followed by 1nm Al_2O_3, where the Al_2O_3 cap increase the V_o near the TE [23].

Device-D dielectric is 7nm HfZrO, where introducing the Zr to the HfO_2 changed the filament microstructure, reduces the effect of the filament thickness [26].



layers	material	Thickness (nm)
Top electrode	PVD TiN	50
	ALD TiN	5
	Ru	5
Switching layer	****	****
Bottom electrode	TiN	50
Adhesion layer	Ti	10

****		
Device-A	HfO_2 w/trt	6nm
Device-B	HfO_2	7nm
Device-C	HfO_2	7nm
	Al_2O_3	1nm
Device-D	HfZrO	7nm

Figure 3.1 Schematic of the four devices with different switching layers showing the material stack and relative thickness of each layer.

3.2. Electrical Characterizations Tools and Connections

A Keysight B1500 semiconductor device parameter analyzer connected to two wave generator fast measurement units (WGFMU) were used to perform both the current-voltage (I-V) characteristics and pulsed measurements. Where Figure 3.2 shows the measurement setup. The benefit of using WGFMU is keeping the same set-up while moving from dc sweep to pulse application, where it is a mandator to start with forming the device using dc sweep before performing the pulse measurement. In the other hand the WGFMU doesn't provide a compliance current limitation which requires us to carefully select the pulse amplitudes to avoid device damaged during the experiment. One of the WGFM channels connected to the TE of the RRAM device, and the other channel connected to the grounded BE. This connection allows the analyzer to perform the voltage pulses on the TE using the

first channel. And then measure the current pulses using the second channel that connected to the BE, which will be the invers of the measurement that will be read from the analyzer since the BE is grounded.

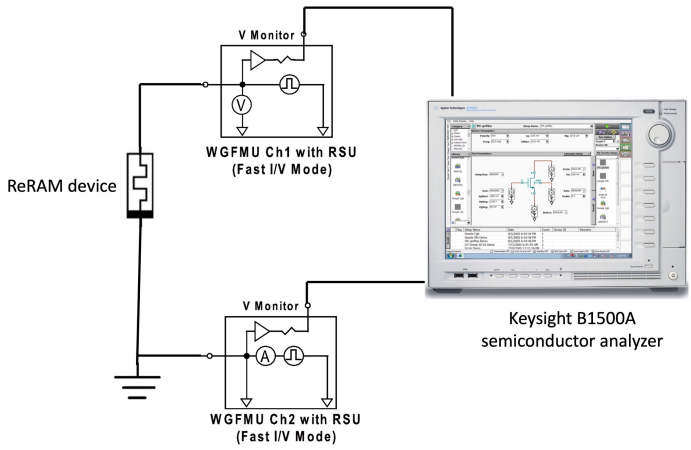


Figure 3.2 Block diagram of pulse measurement set-up.

Source: [27].

3.3. Forming Process

The conductive switching characteristics are achieved by the formation and rupture of a CF due to the V_o distribution in the switching layer. Initially, the fresh device is in a high resistance state (HRS). When the voltage is applied to the TE the oxygen ions move toward it while leaving a line of oxygen vacancies inside the oxide to form CF like the soft breakdown of the dielectric [28]. A I_{cc} limitation is required during this process to avoid irreversible permanent dielectric breakdown. Once the CF is formed the device enter the low resistance state (LRS). When a reversed voltage is applied after the formation a part of the CF will be removed due to the recombination of the oxygen ions with the oxygen vacancies which will switch the

device back from LRS to HRS [23]. We formed all the RRAM devices by applying a DC double sweep to the TE while the I_{cc} was carefully increased from 1nA to 250μA.

3.4. Pulse Operation

In this work we performed three pulse operation on the four RRAM devices (device-A, device-B, device-C, device-D) after forming and resetting each device with voltage sweep.

3.4.1. Width-Varying Pulsed Operation

The first experiment was by applying a train of 80 SET pulses without resting where the pulse width changed every 20 pulses (t_p= 4μs, 50μs, 1ms, 10ms) to make sure that the conductance level reaches a good saturation while keeping the pulse amplitude constant at (V_p= 2V). Figure 3.3 shows Schematic diagram of complete program cycle of width-varying pulsed operation, where we applied a non-distractive read pulse of pulse amplitude (V_r=0.1V) and pulse width (tr=1ms) after each pulse to read the conductance of the CF.

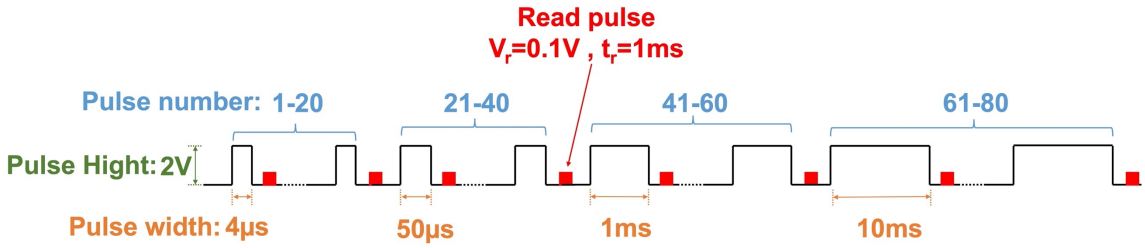


Figure 3.3 Schematic diagram of programed cycle of SET width-varying pulsed operation (off scale).

When the pulses train is applied to the TE the potential drop across the oxide barrier reduces due to the generation of new V_o which in turns lower the probability

to generate more vacancies and reach a saturation level [18]. Increasing t_p gives more time to create new vacancies within the pulse and make the oxide rich of substantial number of traps and trap-assisted tunneling contributes to additional conduction reaching higher conductance levels [18, 19].

3.4.2. Amplitude-Varying Pulsed Operation

In the second experiment we followed the first experiment steps, but we kept the pulse width constant at (t_p=1ms) while changing the pulse amplitude (V_p=0.8V, 1.0V, 1.2V, 1.4V) every 20 pulses. Figure 3.4 shows Schematic diagram of complete program cycle of amplitude-varying pulsed operation.

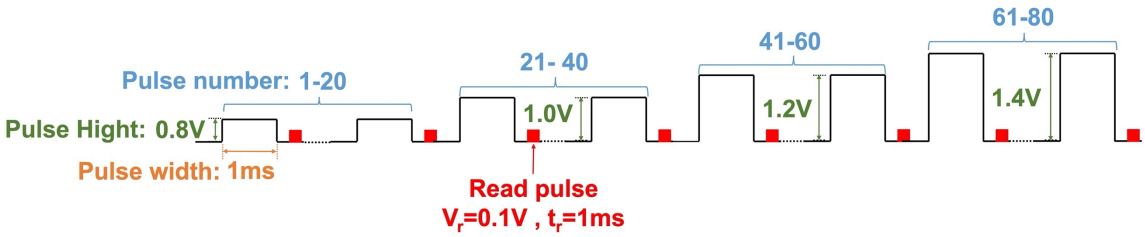


Figure 3.4 Schematic diagram of programed cycle of SET amplitude-varying pulsed operation (off scale).

When a sequences of pulses with varying either pulse width or pulse amplitude are applied to the switching device, it will form one of these shapes of CF while increasing t_p or V_p; a thick CF of larger diameter or multiple conducting thin filaments through the insulator stack [23].

3.4.3. Endurance Test

The main factor limiting the large utilization of RRAM devices in commercial systems is regarding to variability and reliability issues that appear in RRAM devices, which are usually evaluated by performing switching endurance tests [29].

The last experiment in the pulse operation was performing 10k endurance cycles for every programing pulse width (t_p= 4μs, 50μs, 1ms, 10ms).

CHAPTER 4

RESULTS AND DISCUSSIONS

4.1. Forming Process Results

We formed all the RRAM devices by applying a dc double sweep to the TE while the I_{CC} was carefully increased from 1nA to 250μA. Figure 4.1 shows the forming I-V curves of the four RRAM devices that were under investigation in this study, and Table 4.1 list the forming voltages ($V_{forming}$), the minimum I_{CC} that form the device, and forming power (I_{CC} x $V_{forming}$).

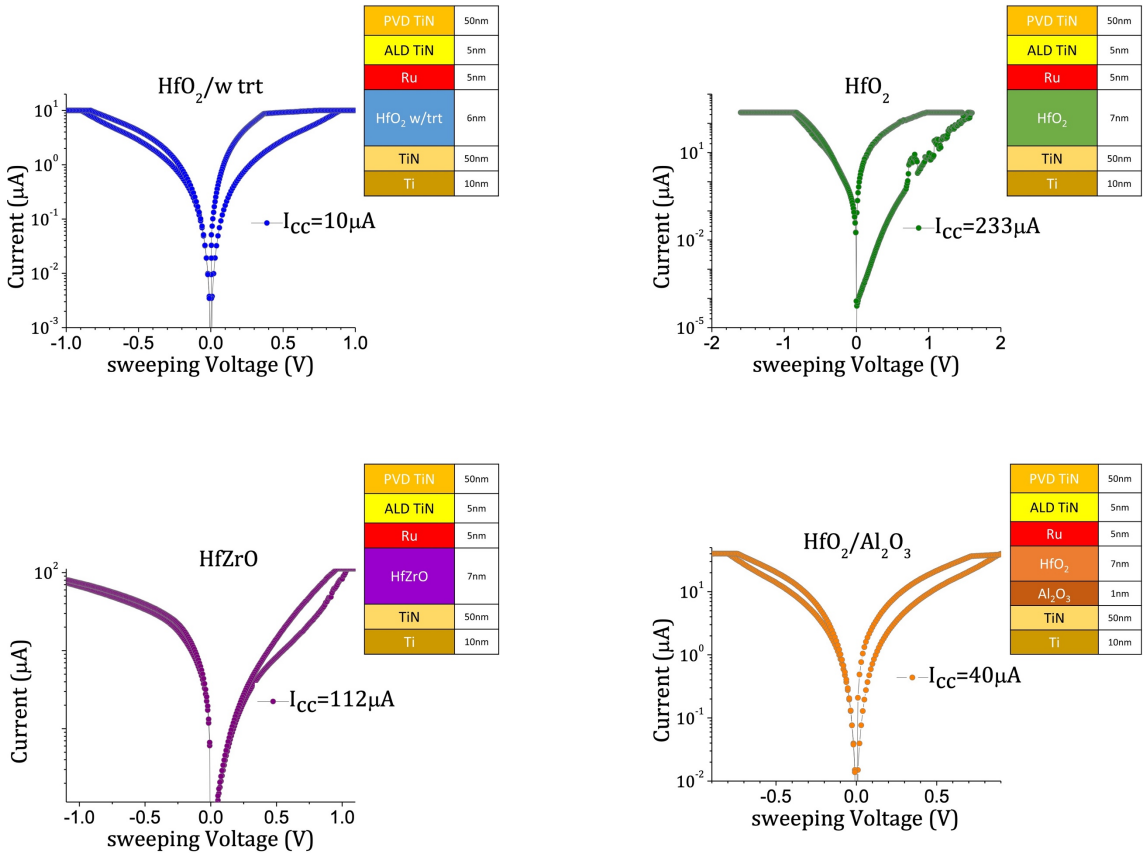


Figure 4.1 Forming I-V curves of the four RRAM devices with oxide control showing the minimum I_{CC}.

Table 4.1 List The Forming Voltages ($V_{forming}$), The Minimum I_{CC} That Form The Device, And Forming Power (I_{CC} X $V_{forming}$)

Device	Device's Dielectric	I_{cc}	$V_{forming}$	Forming Power ($I_{cc}xV_{forming}$)
Device-A	6nmHfO_2 w/trt	10 µA	0.94 V	9.4 µW
Device-B	7nm HfO_2	233 µA	1.36 V	316.88 µW
Device-C	7nm HfO_2/ 1nm Al_2O_3	40 µA	0.89 V	35.6 µW
Device-D	7nm HfZrO	112 µA	1.04 V	116.48 µW

It is clear from Table 4.1 that the device with treated HfO_2 denoted as device-A shows the lowest forming power which attributed to the extra oxygen vacancies due to hydrogen plasma that have been introduced during the deposition of a 6nm thick HfO_2 layer as shown in Figure 4.2. This process step may enrich the oxide HfO_2 near the top electrode with oxygen vacancies which in turn will reduce the switching power and improve the switching behavior compering to the oxide without the plasma treatment [22].

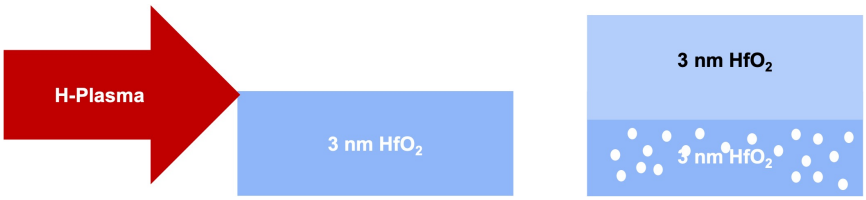


Figure 4.2 Treated device deposition steps, deposit 3 nm HfO_2 by ALD then introduce H-Plasma and after that deposit another 3 nm HfO_2 by ALD.

Since higher concentration of oxygen vacancies near to the top electrode reduces the switching power [23], the device with bilayer HfO_2 and Al_2O_3 denoted as device-C becomes the second on the low forming power list after device-A. That

attributed to the insertion of 1nm Al_2O_3 buffer layer under the 7nm HfO_2. hence the oxygen vacancies are formed relatively faster in Al_2O_3 layer than in HfO_2 layer, once they are formed in Al_2O_3 they stimulate generation for more oxygen vacancies in HfO_2 [23]. For the device with HfZrO denoted as device-D Therefore, the addition of Zr into HfO_2 mends the filament microstructure, reduces the effect of the filament thickness which will improve the reliability after stress [26]. The last on the low forming power list is the device with stochiometric HfO_2 denoted as device-B which prove that the lowest of oxygen vacancies near the top will consume the highest forming power.

4.2. Width-Varying Pulsed Operation Results

For device-A (6nm HfO_2 with H-plasma treatment) Figure 4.3 shows the four expected states with no overlap and a good window between states for pulse widths (t_P= 4μs, 50μs, 1ms), we noticed reduction in window between states generated from pulse widths (1ms) and (10ms) which is the opposite case with device-D (7nm HfZrO) the good window between states appeared with higher pulse widths as shown in 4.6.

While Figure 4.4 of device-B with no treatment shows two states out of four expected states, which may be caused by a formation of interfacial oxide layer between the electrode and the oxide that make the device stuck with the same LRS [19].

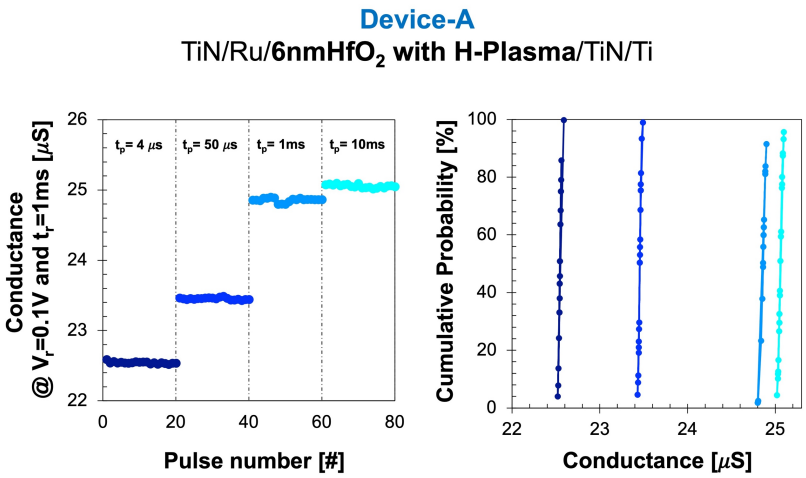


Figure 4.3 Measured conductance modulation obtained by applying successive SET pulse sequences with increasing t_p and the experimental cumulative probability distributions of the states for device-A (6nm HfO_2 with H-plasma treatment).

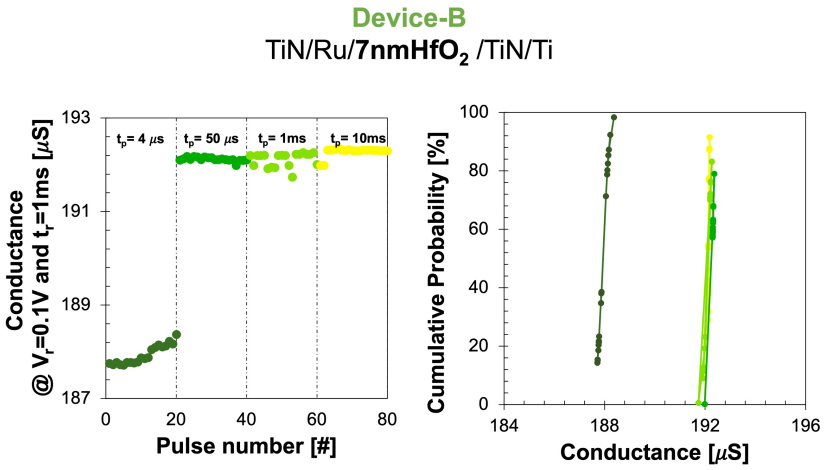


Figure 4.4 Measured conductance modulation obtained by applying successive SET pulse sequences with increasing t_p and the experimental cumulative probability distributions of the states for device-B (7 nm stochiometric HfO_2).

Pulsed with high width gives more time during the pulse to generate more oxygen vacancies which will apply more stress to the device. That make device-D and device-C stabler than device-A under high stress as shown in Figures 4.5 and

4.6. Table 4.2 shows summary of the comparison that made in this section between the four RRAM devices.

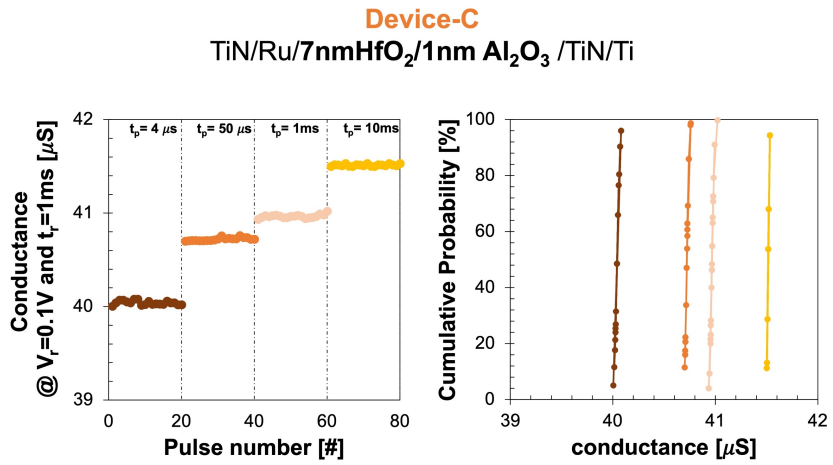


Figure 4.5 Measured conductance modulation obtained by applying successive SET pulse sequences with increasing t_p and the experimental cumulative probability distributions of the states for Device-C (7nm HfO_2/1nm Al_2O_3).

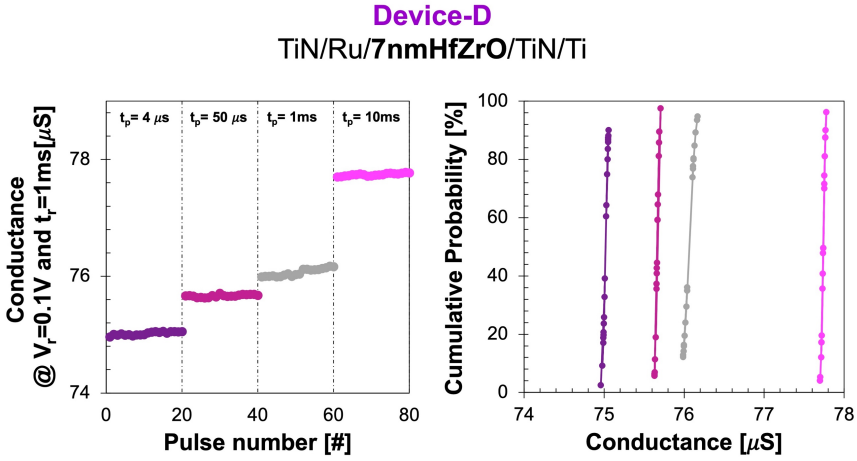


Figure 4.6 Measured conductance modulation obtained by applying successive SET pulse sequences with increasing t_p and the experimental cumulative probability distributions of the states for Device-D (7nm HfZrO).

Table 4.2 Comparison Of Conductance States That Have Been Generated In The Four RRAM Devices With Width-Varying Pulsed Operation

Device	Device's dielectric	Number of states out of 4	Conductance Window between		
			G1-G2	G2-G3	G3-G4
Device-A	6nmHfO_2 w/trt	4	0.927 µS	1.322 µS	0.276 µS
Device-B	7nm HfO_2	2	3.993 µS	0	0
Device-C	7nm HfO_2/ 1nm Al_2O_3	4	0.678 µS	0.234 µS	0.56 µS
Device-D	7nm HfZrO	4	0.618 µS	0.318 µS	1.716 µS

4.3. Amplitude-Varying Pulsed Operation Results

It was found that the conductance level increased with small change while increasing the pulsed width with fixed pulse amplitude from the previous section. But for a fixed pulse width the increasing in the conductance level was found to be larger while increasing pulsed amplitude with noticeable fluctuation within the same conductance level. The fluctuation from cycle to cycle within the same device and same state level attributed to the stochastic nature of the oxygen vacancies/ ions processes, as mentioned in [30], it could be smothered with low pulse width since we demonstrated the amplitude-varying with high pulse width (t_p=1ms).

Device-A (6nm HfO2 with plasma treatment) Figure 4.7 shows higher range of conductance level with amplitude-varying pulsed operation than that had been achieved with width-varying pulsed operation, but with better MLC characteristics. It could be because with width-varying we use 2V amplitude (higher voltage regime) which produce Fowler–Nordheim (F–N) tunneling that cause induvial electrons to escape from the device and lower the conductance value [31] [32], but it cannot

be proved with rustles that was taken in the room temperature only. After that we perform amplitude-varying at lower voltages but with large pulse width that allow more oxygen vacancies to be generated in the oxide and make it rich of substantial number of traps and trap-assisted tunneling leads to higher conduction [32].

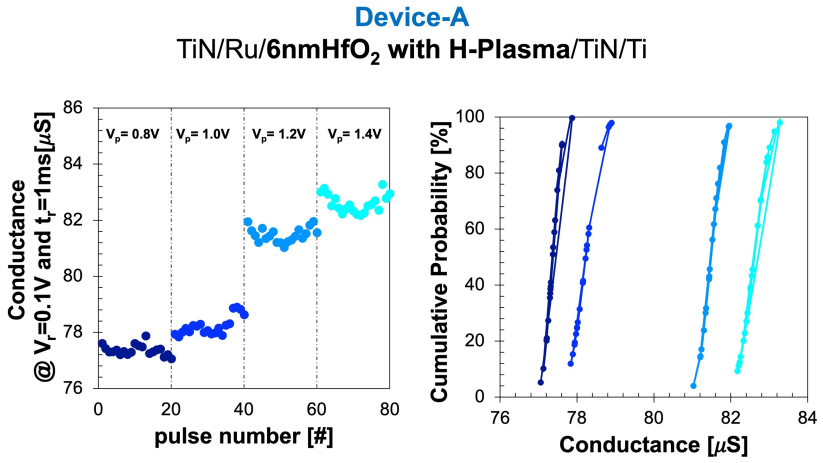


Figure 4.7 Measured conductance modulation obtained by applying successive SET pulse sequences with increasing V_p and the experimental cumulative probability distributions of the states for device-A (6nm HfO_2 with H-plasma treatment).

While device-C (7nm HfO_2/1nm Al_2O_3) Figure 4.8 shows settled conductance state range with both pulsed operations and has the best endurance compared to the other three devices, since it exposes stability with 10k endurance cycles with small degradation of (1ms) pulse width but with the lowest fluctuations in all states as shown in Figure 4.13. These features of device-C make it possible to obtain quasi-analog behavior, which is important for in-memory computing [33].

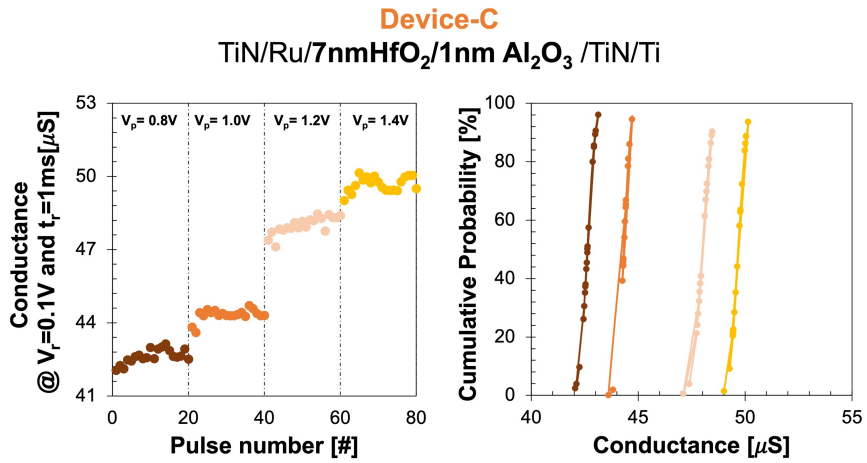


Figure 4.8 Measured conductance modulation obtained by applying successive SET pulse sequences with increasing V_p and the experimental cumulative probability distributions of the states for Device-C (7nm HfO_2/1nm Al_2O_3).

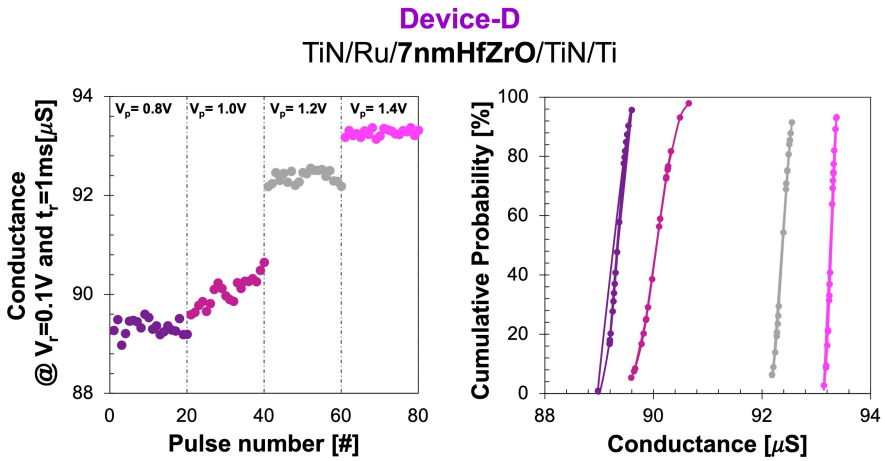


Figure 4.9 Measured conductance modulation obtained by applying successive SET pulse sequences with increasing V_p and the experimental cumulative probability distributions of the states for Device-D (7nm HfZrO).

For device-D (7nm HfZrO) Figure 4.9 shows four conductance states that was demonstrated out of four expected states, with remarkable smoothness at pulse amplitudes (1.2V and 1.4V) due to the addition of Zr as mentioned earlier that mends the filament microstructure since the HfZrO has high dielectric constant

under processing conditions [26] [34] [35], however device-C shows more stability than device-D with 10k endurance cycles experiment as clear in Figures 4.13 and 4.14. Hence the effect of amplitude-varying is stronger than width-varying as mentioned previously the behavior of device-B was improved to demonstrate three discrete states out of four with no overlapping as shown in Figure 4.10.

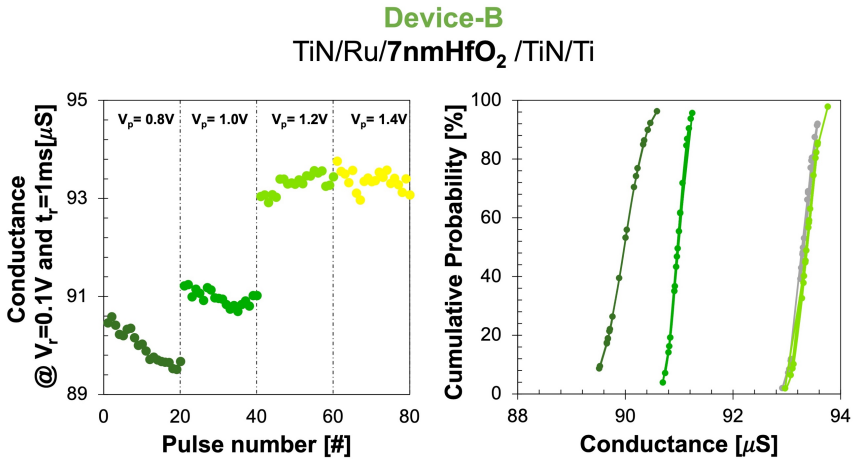


Figure 4.10 Measured conductance modulation obtained by applying successive SET pulse sequences with increasing V_p and the experimental cumulative probability distributions of the states for device-B (7 nm stochiometric HfO_2).

It is clear from Figure 4.11 that the effect of changing pulse amplitude is stronger than changing the pulse width on the RRAM devices for all type of dielectrics in this study. While the width-varying leads to linearity between conductance stats the amplitude-varying shows exponential behavior [31]. The linearity eases controlling the states of the device, however a large window between states makes the amplitude-varying operation better to achieve a good MLC characteristic since it will reduce the read/write disturbance. Table 4.3 shows

summary of the comparison that made in this section between the four RRAM devices.

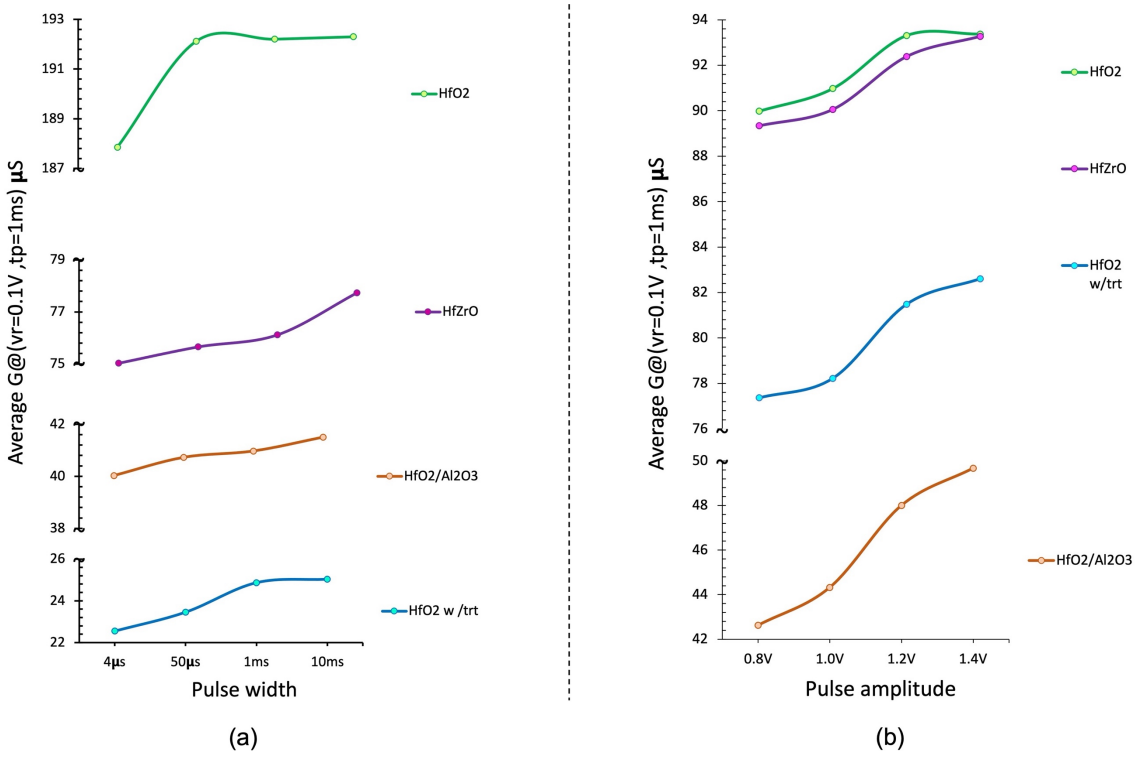


Figure 4.11 Average RRAM conductance was plotted against varying (a) SET pulse width and (b) SET pulse amplitude.

Table 4.3 Comparison Of Conductance States That Have Been Generated In The Four RRAM Devices With Amplitude-Varying Pulsed Operation

Device	**Device's dielectric**	**Number of states** out of 4	**Conductance Window Between**		
			G1-G2	G2-G3	G3-G4
Device-A	6nmHfO_2 w/trt	4	0.862 µS	3.255 µS	1.123 µS
Device-B	7nm HfO_2	3	0.996µS	2.33µS	0.066µS
Device-C	7nm HfO_2/ 1nm Al_2O_3	4	1.699 µS	3.681 µS	1.670 µS
Device-D	7nm HfZrO	4	0.721 µS	2.320 µS	0.891 µS

4.4. Endurance Test Results

A reasonable endurance was obtained with all RRAM devices that were fabricated in this study with some disparity between them. Figure 4.12 shows the endurance of device-A (6nm HfO_2 with plasma treatment), as with pulse width t_p=4μs we observed after 100 cycles a small raising in the conductance values due to new oxygen vacancies that has been generated while increasing the number of pulses. However, with pulse width t_p=1ms after 450 cycles the conductance level degraded with small amount that could be caused by overstress of the CF [33].

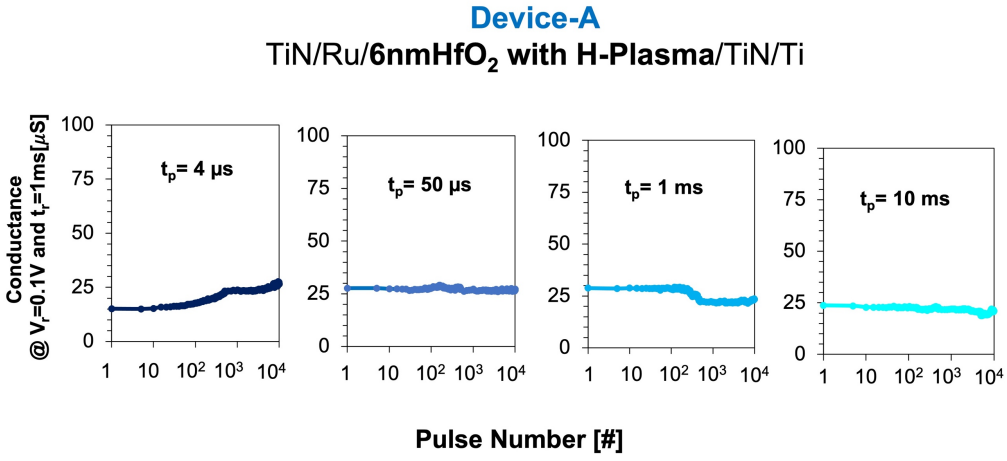


Figure 4.12 Measured conductance values just after SET transition during 10k endurance cycles for every programing pulse width (tp= 4μs, 50μs, 1ms, 10ms) for the device-A (6nm HfO_2 with H-plasma treatment).

Figure 4.13 shows the endurance of device-B (7nm HfO_2) where the fluctuation starts with pulse width t_p=50μs which is expected with such a device with no buffer layer.

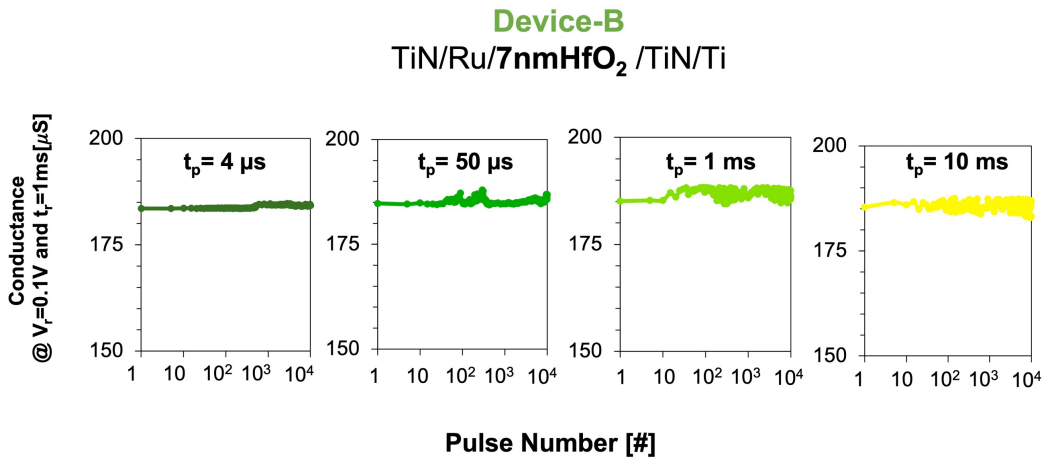


Figure 4.13 Measured conductance values just after SET transition during 10k endurance cycles for every programing pulse width (tp= 4μs, 50μs, 1ms, 10ms) for the device-B (7 nm stochiometric HfO_2).

Figure 4.14 shows excellent endurance that obtained with device-C (7nm HfO_2/1nm Al_2O_3) due to Al_2O_3 below HfO_2 caping which could allow more control on the formation of CF that consist of oxygen vacancies over the Al atoms that diffused form Al_2O_3 layer and reduces oxygen vacancies generation energy near the Al atoms [16].

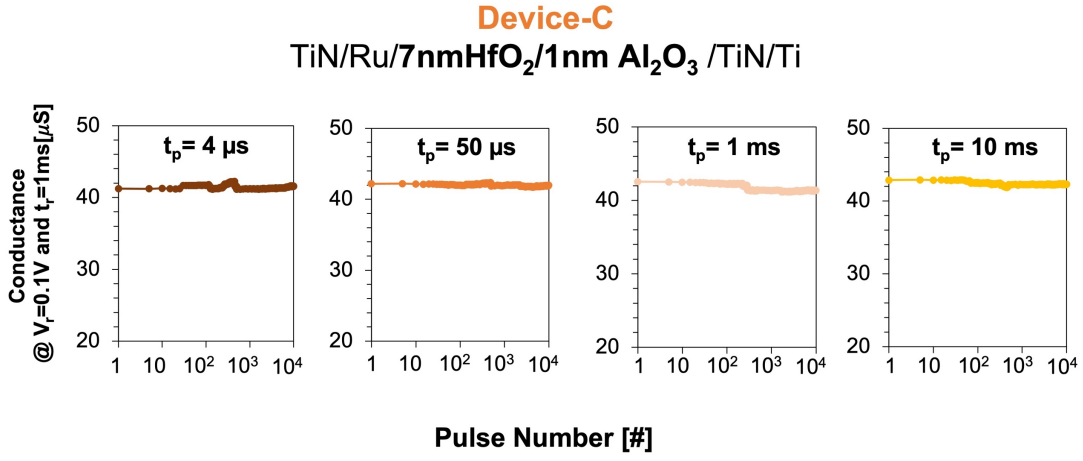


Figure 4.14 Measured conductance values just after SET transition during 10k endurance cycles for every programing pulse width (tp= 4μs, 50μs, 1ms, 10ms) for the device-C (7nm HfO_2/1nm Al_2O_3).

Figure 4.15 shows changed in conductive value in device-D after 200 cycled for all programing pulsed widths, could be attributed to its bond structure [14].

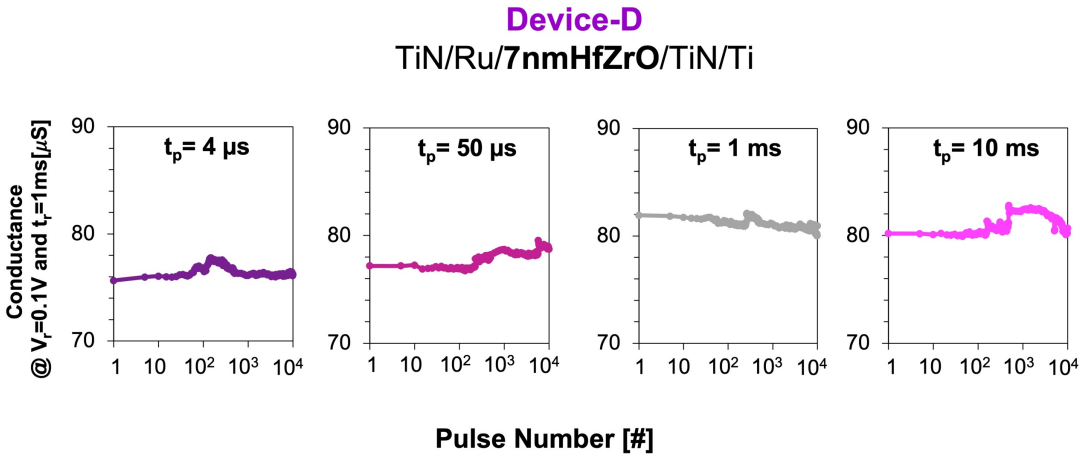


Figure 4.15 Measured conductance values just after SET transition during 10k endurance cycles for every programing pulse width (tp= 4μs, 50μs, 1ms, 10ms) for the device-D (7nm HfZrO).

4.5. Conductance quantization

Since device-A (6nm HfO_2 with H-plasma treatment) shows the lowest forming power and a reasonable conductance quantization, we perform another pulsed operation with proper pulse width variation and pulse amplitude, by applying 120 SET pulses with fixed V_p=1V and changing tp every 10 pulses starting with t_p=4μs with increasing step 20μs.

Figure 4.16 shows the conductance quantization with no overlap between the states. Which make the treated device a promising candidate to be used as a two-terminals device in a crossbar for in-memory computing and for implementing artificial synopses for neuromorphic computing.

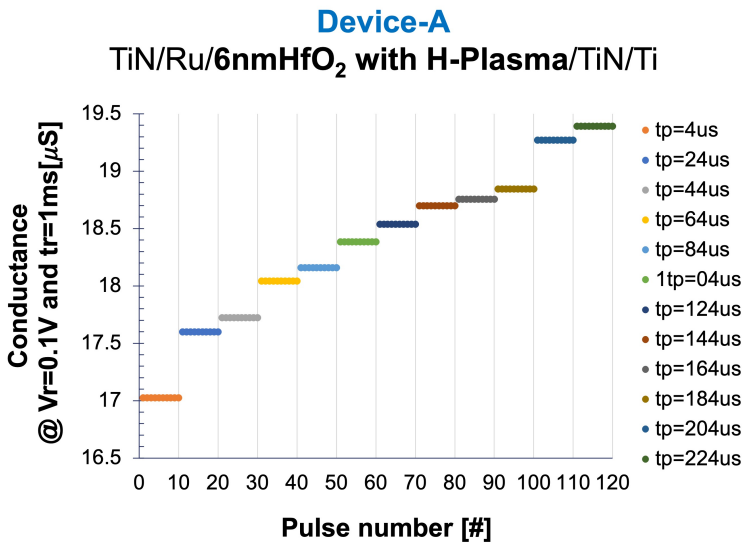


Figure 4.16 Quantization of measured conductance obtained by applying successive SET pulse sequences with increasing t_p for device-A (6nm HfO_2 with H-plasma treatment).

CHAPTER 5

IMPACT OF BOTTOM ELECTRODE ON SWITCHING CHARACTERISTICS

5.1. Device Structures

Engineering the distribution of defects or oxygen vacancies near the top and bottom electrodes has a significant impact on reducing the switching power and improving the multi-level cell (MLC) characteristics of the device. A graded distribution with higher concentration of oxygen vacancies closer to the top electrode (TE) due to hydrogen plasma treatment and lower concentration near the bottom electrode (BE) reduces switching power [22]. Figure 5.1 shows a schematic of the V_o distribution inside the oxide.

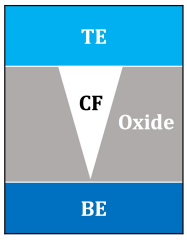


Figure 5.1 Schematic of RRAM device showing the desirable V_o distribution inside the oxide layer, which is more V_o near the TE.

This chapter presented the results of studying three RRAM stacks as shown in Figure 5.2 that have the same TE (50nm PVD TiN/5nm ALD TiN) and dielectric (HfO_2 with hydrogen plasma treatment at the mid-point) but with different BE for each stack: TiN (device-E (control)), TiN plus Mo with thermal anneal (device F), and TiN plus Mo with plasma nitridation (device G).

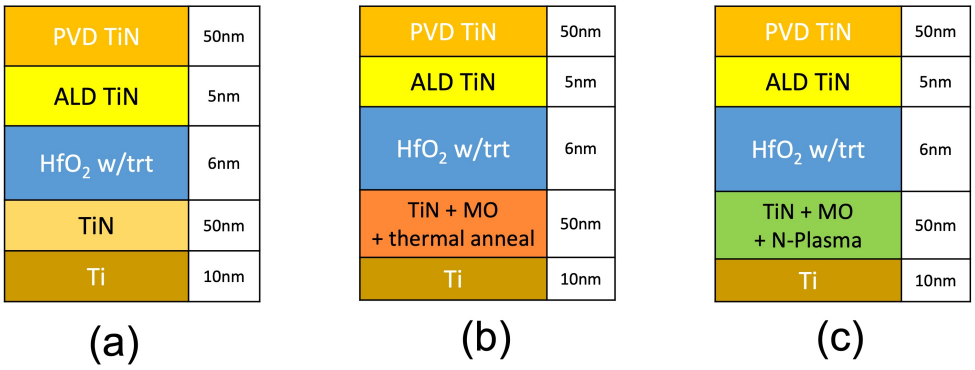


Figure 5.2 Schematic of RRAM stacks that have the same TE and dielectric but different BE (a) TiN (device-E (control)), (b) TiN plus Mo with thermal anneal (device-F), (c) TiN plus Mo with plasma nitridation (device-G).

5.2. Forming Process and Results

We formed all the RRAM devices by applying a DC double sweep to the TE and grounded the BE where the I_{CC} was carefully increased from 1nA to 50μA. While forming the devices device-G with (TiN plus Mo with plasma nitridation) at the BE shows switching at 1nA, then we apply lower I_{CC} and found several devices on the wafer that switched at 500pA. Figure 5.3 shows the forming I-V curves of the three RRAM devices, and Table 5.1 list the forming voltages ($V_{forming}$), the minimum I_{CC} that form the device, and forming power (I_{CC} x $V_{forming}$).

Selecting inert metal as a BE provides a lower V_o concentration at the interface between the BE and the dielectric [36]. which in turn reduces the switching power as noted with device-G (TiN plus Mo with plasma nitridation). It is possible that the presence of nitrogen prevents the decrease in V_o concentration near the BE. Where the N_2 molecules reach the grain boundary then the active nitrogen atoms connect to the Hf ion dangling bonds as their lone-pair electrons.

Since the bonding energy of the Hf–N bond is very low (535ev) compared to Hf–O bond (801ev) [37], then the oxygen ions move toward the TE and reduce the forming voltage.

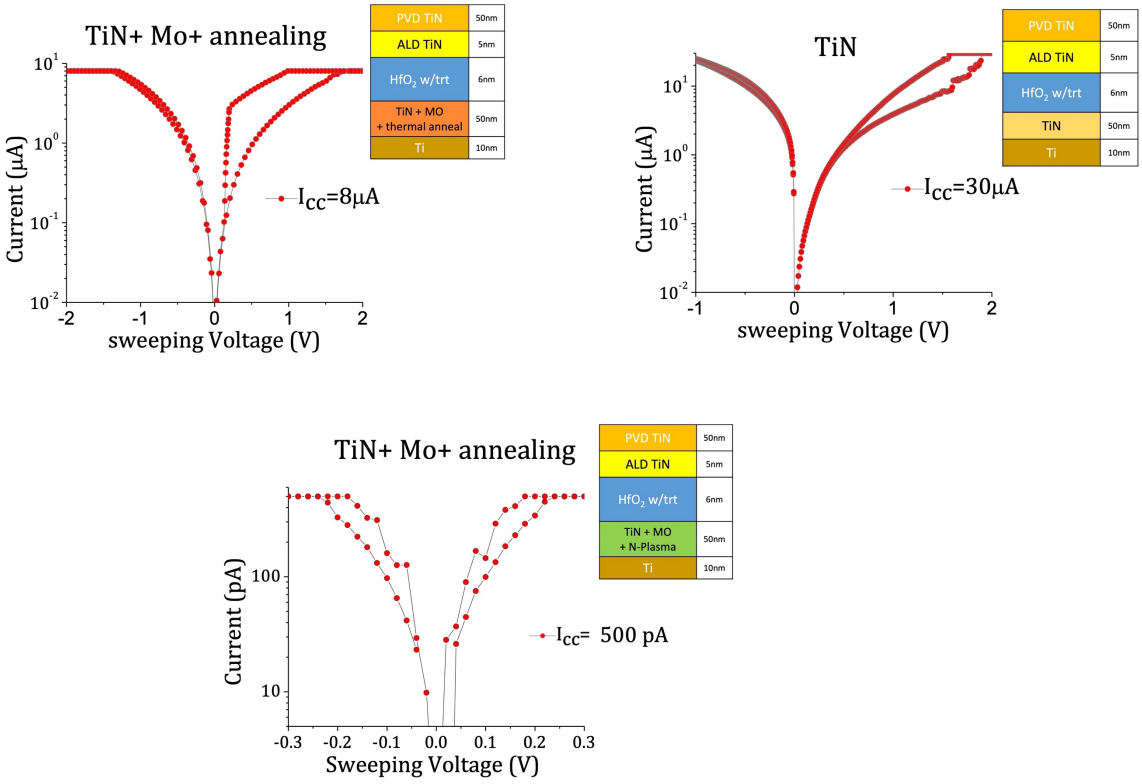


Figure 5.3 Forming I-V curves of the three RRAM devices with BE control showing the minimum I_{CC}.

On the other hand, a higher concentration of V_o at the BE and the dielectric interface leads to a larger magnitude of band bending and increases the height of Schottky barrier. This possibly leads to an increase in the switching power in device-E and device-F as compared to device-G [37]. Device-E (TiN) switched at I_{CC} =30μA and device-F (TiN plus Mo with thermal anneal) switched at I_{CC} =8μA,

which is superior compared to device-E in switching power. This suggests that the alloy of TiN with Mo is reducing the V_o near the BE.

Table 5.1 List The Forming Voltages ($V_{forming}$), The Minimum I_{CC} That Form The Device, And Forming Power (I_{CC} X $V_{forming}$)

Device	Device's BE	I_{cc}	$V_{forming}$	Forming Power (I_{cc}x$V_{forming}$)
Device-E	TiN	30 µA	1.8 V	54 µW
Device-F	TiN + Mo + thermal anneal	8 µA	1.6 V	12.8 µW
Device-G	TiN + Mo + plasma nitridation	500 pA	0.25 V	125 pW

5.3. RESET Pulsed Operation and Results

To study the MLC characteristics of the devices, we performed a train of 36 RESET pulses with fixed amplitude V_p= -1V and pulse width starting at 4µs and increasing by 20µs every 3 pulses, while we applied V_r=0.1V and t_r=10µs after each pulse to measure the conductance Figure 5.4 shows the schematic of the pulse train.

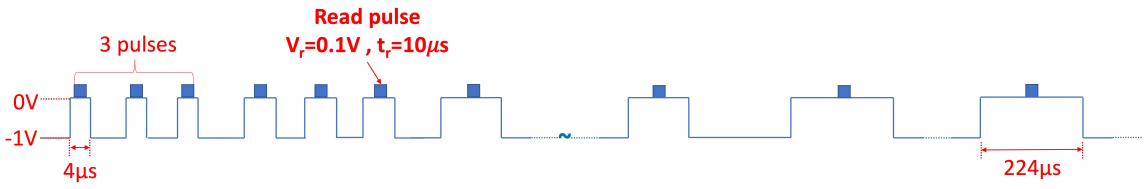


Figure 5.4 Schematic diagram of programed cycle of RESET width-varying pulsed operation (off scale).

Figure 5.5a shows that device-F (TiN plus Mo with thermal anneal) has good MLC with no overlap between the states while device-E has unstable MLC behavior as shown in Figure 5.5b due to time constant variation.

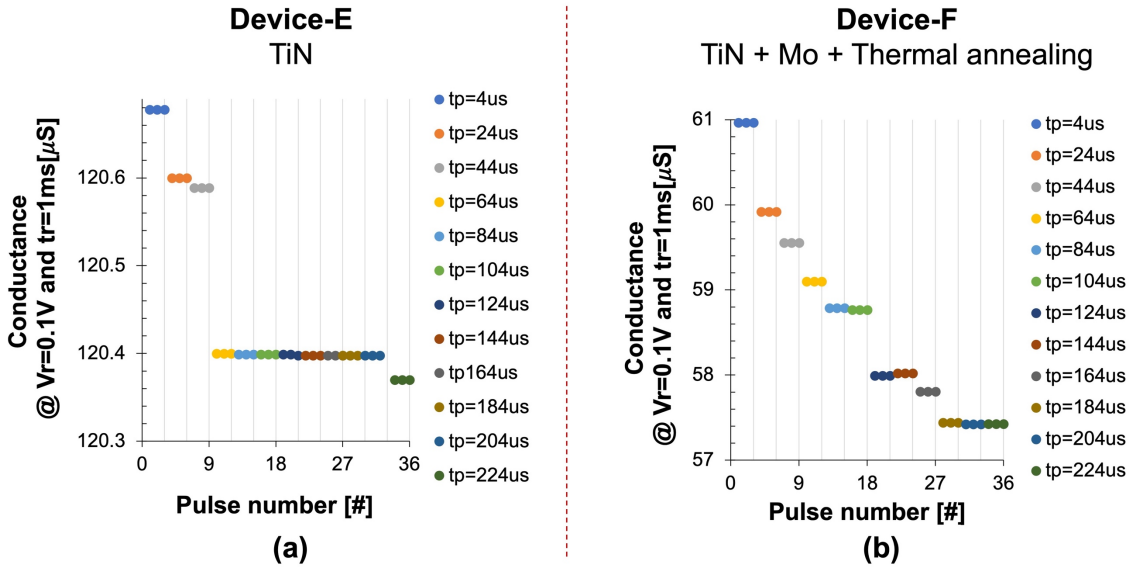


Figure 5.5 Measured conductance modulation obtained by applying successive RESET pulse sequences with increasing t_p and for (a) Device-E (TiN) (b) Device-F (TiN+ Mo+ Thermal annealing).

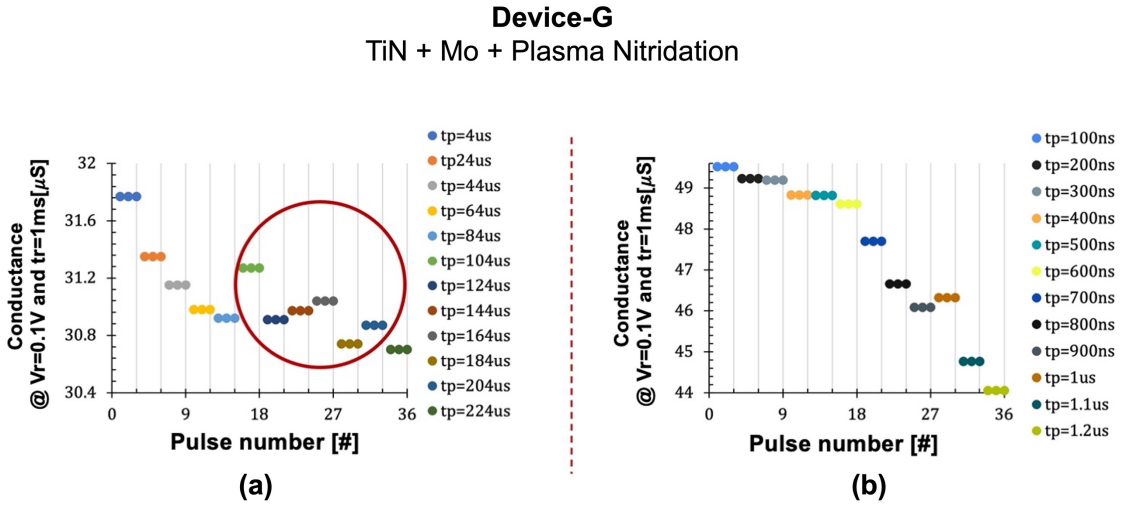


Figure 5.6 Measured conductance modulation obtained by applying successive RESET pulse sequences with increasing t_p and for Device-G (TiN + Mo+ Plasma Nitridation) (a) t_p in microseconds (b) t_p in nanoseconds.

Figure 5.6a shows the results of device-G for the same RESET pulse train that was applied to devices-E and devices-F. Since device-G switched at a very

low current and voltage, the conductance quantization was unstable after 15 pulses due to overstress of the conductive filament. Wherefore we programed anther RESET pulse train with nanoseconds pulse width. We performed a train of 36 RESET pulses with fixed amplitude V_p= -0.5V and pulse width starting at 100ns and increasing by 100ns every 3 pulses, while we applied V_r=0.05V and t_r=100ns after each pulse to measure the conductance Figure 5.6b shows the improve conductance quantization of device-G.

CHAPTER 6

CONCLUSION AND FUTURE WORK

6.1. Conclusion

RRAM is a promising device to be used for in-memory computing due to its low power consumption, compatibility with CMOS, high density storge, high reliability, MLC characteristics and reasonable endurance. Since selecting the material of each layer of the RRAM device is impact the switching behavior and the power consumption by the device, in this work chapters 3 and 4 presented the study four different dielectrics: (a) HfO_2 with plasma treatment (b) HfO_2, (c) HfO_2/Al_2O_3 bilayer, and (d) HfZrO. By forming and characterizing the multi-level conductance behavior with pulse width variation, pulse amplitude variation and endurance test.

The H-plasma Treated HfO_2 showed the lowest power requirement and excellent multi-level conductance quantization for pulse width variation measurements, due to the presence of the H-plasma at the midpoint of the switching layer. In addition to the Ru as TE, where its deposition process plays a role in power reduction as found from previous studies. While proper selection of pulse width and amplitude can make the devices perform efficiently.

HfO_2/Al_2O_3 bilayer showed stability in conductance range in both pulse width and amplitude variation, while the forming power is higher than the treated device, but the endurance test is showing better uniformity.

The results show how the distribution of V_o plays a significate role in conductance quantization. The more V_o near the TE and lower near the BE reduce the power consumption and improve the MLC characteristics.

After studying the impact of the dielectric, we studied tree different devices with varying the BE, while chapter 5 presented the process and the results. compared to TiN we have observed that TiN Annealed Mo devices showed much lower switching energy and conductance quantization. It can be assumed that bottom electrode metal/alloy can have some significant impact on RRAM performance.

While we are evaluating devices with TiN-Mo exposed N-plasma as bottom electrode we surprised with several devices that switched at 500 pA. The presence of N-plasma also led to better conductance quantization with nanoseconds pulse width than in microsecond pulse width.

6.2. Future Work

For future work, studying the impact of different nitrogen flow in BE will be the next step in this research. In addition to the physical analysis such as High-resolution transmission electron microscopy (TEM) and X-ray photoelectron spectroscopy (XPS) that could be used to examine the structure and concentration of V_o for better understanding of the electrical analysis results.

REFERENCES

[1] Sebastian, A.; Gallo, M.L.; Khaddam-Aljameh, R.; Eleftheriou, E., “Memory devices and applications for in-memory computing”, Nature Nanotechnology, vol. 15, 2020, DOI: https://doi.org/10.1038/s41565-020-0655-z.

[2] Zou, X.; Xu, Sh.; Chen, X.; Yan, L.; Han, Y., “Breaking the von Neumann bottleneck:
architecture-level processing-in-memory technology”, Science China, vol. 64, 2021, DOI: https://doi.org/10.1007/s11432-020-3227-1.

[3] Mittal, S., “A Survey of ReRAM-Based Architectures for Processing-In-Memory and Neural Networks”, Mach Learn Knowl Extr, 2018, DOI: https://doi.org/10.3390/make1010005.

[4] Chen, W. H.; Li, K. X.; Lin, W. Y., “A 65 nm 1 Mb nonvolatile computing-in-memory ReRAM macro with sub-16 ns multiplyand- accumulate for binary DNN AI edge processors” In: Proceedings of IEEE International Solid-State Circuits Conference, San Francisco, 2018. DOI:10.1109/ISSCC.2018.8310400.

[5] Chen, A., “A review of emerging non-volatile memory (NVM) technologies and applications”, Solid-State Electronics 125, 2016, DOI: 10.1016/J.SSE.2016.07.006.

[6] Ielmini, D., Wong, H.-S.; “In-memory computing with resistive switching devices”, Nature Electronics, vol. 1, 2018, DOI:10.1038/s41928-018-0092-2.

[7] Zhirnov, V. V.; Marinella, M. J.,” In Emerging Nanoelectronic Devices”, eds Chen, A. Ch. 3 Wiley Online Library, 2015.

[8] Wong, H.-S. P.; Salahuddin, S., “Memory leads the way to better computing”, Nature Nanotechnology, vol. 10, 2015, DOI:10.1038/nnano.2015.29.

[9] Xie, Y.; Zhao, J, "Emerging Memory Technologies," in IEEE Micro, vol. 39, no. 1, pp. 6-
7, February 2019, DOI: 10.1109/MM.2019.2892165.

[10] Banerjee, W., “Challenges and Applications of Emerging Nonvolatile Memory Devices,” Electronics, vol. 9, no. 6, p. 1029, 2020, DOI: https://doi.org/10.3390/electronics9061029.

[11] Chi, P.; Li, S.; Cheng, Y.; Lu, Y.; Kang, S. H.; Xie, Y., “Architecture design with STTRAM:
Opportunities and challenges”, ASP-DAC, 2016, DOI: 10.1109/ASPDAC.2016.7427997.

[12] Chakraborty, I.; Ali, M.; Ankit, A.; Roy, S.; Sridharan, Sh.; Agrawal, A.; Raghunathan, A.; Roy, K., “Resistive Crossbars as Approximate Hardware Building Blocks for Machine Learning: Opportunities and Challenges”, proceedings of the IEEE, vol. 108, no. 12, 2020, DOI: 10.1109/JPROC.2020.3003007.

[13] Slonczewski, J. C., “Current-driven excitation of magnetic multilayers,” J. Magn. Magn. Mater., vol. 159, pp. L1–L7, 1996, DOI: https://doi.org/10.1016/0304-8853(96)00062-5.

[14] Valov,I.; Waser, R.; Jameson, J. R.; Kozicki, M. N., “Electrochemical metallization memoriesVFundamentals”, Nanotechnology, vol. 22, 2011, DOI: 10.1088/0957-4484/22/25/254003.

[15] Chua, L., "Memristor-The missing circuit element," IEEE Transactions on Circuit Theory, vol. 18, no. 5, pp. 507-519, 1971, DOI: 10.1109/TCT.1971.1083337.

[16] Strukov, D. B.; Snider, G. S.; Stewart, D. R.; Williams, R. S., “The missing memristor found”, Nature, vol. 453, 2008, DOI:10.1038/nature06932.

[17] Yu, Sh.; Wong, H.-S. P., “A phenomenological model for the reset mechanism of metal oxide RRAM”, IEEE Electron Device Lett., vol. 31, 2010, DOI: 10.1109/LED.2010.2078794.

[18] Padovani, A; Woo, J; Hwang, H; Larcher, L, “Understanding and Optimization of Pulsed SET Operation in HfOx-Based RRAM Devices for Neuromorphic Computing Applications”, IEEE electron device letters, vol. 39, 2018, DOI: 10.1109/LED.2018.2821707.

[19] Wong, H.-S. P.; Lee, H. Y.; Yu, Sh.; Chen,Y.; Wu, Y.; Chen, P. Ch.; Lee, B.; Chen, F.T.; Tsai, M. G., “Metal–Oxide RRAM”, Proceedings of the IEEE, 2012, DOI: 0.1109/JPROC.2012.2190369.

[20] Qin, S.; Ma, Y.; Wang, Q.; Zhang, J.; Zhang, G.; Yang, L.; Liu, R., “Study on ion dynamics of hafnium oxide RRAM by electrode thermal effect”, Energy report, vol. 9, 2023, DOI: https://doi.org/10.1016/j.egyr.2022.11.132.

[21] Kaiser, N.; Vogel, T.; Zintler, A.; Petzold, S.; Arzumanov, A.; Piros, E.; Eilhardt, R.; Molina-Luna, L.; Alff, L., “Defect-Stabilized Substoichiometric Polymorphs of Hafnium Oxide with Semiconducting Properties”, ACS, 2022, DOI: https://doi.org/10.1021/acsami.1c09451.

[22] Patel, Y.; Misra, D.; Triyoso, D.; Clark, R.; Tapily, K.; Consiglio, S.; Wajda, C.; and Leusink, G., “RRAM Devices with Plasma Treated HfO2 with Ru as Top Electrode for In-Memory
Computing Hardware”, ECS Transactions, 104(3), p. 35, 2021, DOI: 10.1149/10403.0035ecst.

[23] Misra, D.; Zhao, P.; Triyoso, D.; Clark, R.; Tapily, K.; Consiglio, S.; Wajda, C.; and Leusink, G., “Dielectrics and Metal Stack Engineering for Multilevel Resistive Random-Access Memory”, ECS J. Solid State Sci. Technol. 9, 05300, 2020, DOI: 10.1149/2162-8777/ab9dc5.

[24] Consiglio, S.; Higuchi, H.; Ando, T.; Jamison, P.; Seo, S.-Ch.; Kong, D., Kim, Y.; Tapily, K.; Clark, R.D.; Hopstaken, M.; Cartier, E.; Tsunomura, T.; Wajda, C.S.; Soave, R.; Narayanan, V.; Leusink, G.J., “Process-Induced ReRAM Performance Improvement of Atomic Layer Deposited HfO2 for Analog In-Memory Computing Applications”, ECS Transactions, vol. 102, no. 2, 2021, DOI: 10.1149/10202.0019ecst.

[25] Jain, B.; Huang, Ch.; Misra, D.; Tapily, K.; Clark, R.; Consiglio, S.; Wajda, C; Leusink, G., “Multilevel Resistive Switching in Hf-Based RRAM”, ECS Transactions, vol. 89, no. 3, 2019, DOI: 10.1149/08903.0039ecst.

[26] Bhuyian, M.; Poddar, S.; Misra, D; Tapily, K.; Clark, R. D.; Consiglio, S.; Wajda, C. S.; Nakamura, G.; Leusink, G. J, “Impact of cyclic plasma treatment on oxygen vacancy defects in TiN/HfZrO/SiON/Si gate stacks”, Applied physics letters, vol.106, 2015, DOI: https://doi.org/10.1063/1.4921307.

[27] Agilent B1530A Waveform Generator/ Fast Measurement Unit manual.

[28] Yu, Sh.,” Resistive Random Access Memory (RRAM), Synthesis Lectures on Emerging Engineering Technologies”, 2016.

[29] Lanza, M; Waser, R; Ielmini, D; Yang, J. J, “Standards for the Characterization of Endurance in Resistive Switching Devices”, ACS nano, vol.15, 2021, DOI: 10.1021/acsnano.1c06980.

[30] Yu, Sh.; Guan, X.; Wong, H.-S. P.; “On the stochastic nature of resistive switching in metal oxide RRAM: Physical modeling, Monte Carlo simulation, and experimental characterization”, IEEE International Electron Devices Meeting, IEDM, 2011, DOI: 10.1109/IEDM.2011.6131572.

[31] Zahiruddin, A; Karsten, B; Joshua, H; Nathaniel C., “Pulse width and height modulation for multi-level resistance in bi-layer TaO_x based RRAM”, Appl. Phys. Lett., vol.111, 2017, DOI: https://doi.org/10.1063/1.4993058.

[32] Yu, Sh.; Guan, X.; Wong, H. S. P, “Conduction mechanism of TiN/$HfO_{(x)}$/Pt resistive switching memory”, Appl. Phys. Lett., vol. 99,2011, DOI: 10.1063/1.3624472.

[33] Wu, Y.; Yu, Sh.; Wong, H.-S. P., “AlOx-Based Resistive Switching Device with Gradual Resistance Modulation for Neuromorphic Device Application”, IEEE International Memory Workshop, 2012, DOI: 10.1109/IMW.2012.6213663.

[34] Ramo, D.M.; Sushko, P. V; Gavartin, J. L; Shluger, A. L, “Oxygen vacancies in cubic ZrO_2 nanocrystals studied by an ab initio embedded cluster method”, Phys. Rev. B, vol.78, 2008, DOI: https://doi.org/10.1103/PhysRevB.78.235432.

[35] Ramo, D.M.; Gavartin, J. L; Shluger, A. L; Bersuker, G, “Spectroscopic properties of oxygen vacancies in monoclinic HfO_2 calculated with periodic and embedded cluster density functional theory”, Phys. Rev. B, vol.75, 2007, DOI: https://doi.org/10.1103/PhysRevB.75.205336.

[36] Yong, Z.; Persson, K. ; Ram, M.; D’Acunto, G.; Liu, Y.; Benter, S.; Pan, J.; Li, Z.; Borg, M.; Mikkelsen, A.; Wernersson, L. ; Timm, R.,” Tuning oxygen vacancies and resistive switching properties in ultra-thin HfO_2 RRAM via TiN bottom electrode and interface engineering”, Applied Surface Science, 2021, DOI: https://doi.org/10.1016/j.apsusc.2021.149386.

[37] Wang, M.-H.; Chang, T.-Ch.; Shih, Ch.-Ch., “Performance improvement after nitridation treatment in HfO_2-based resistance random-access memory”, 2018, Applied Physics Express, DOI: 10.7567/APEX.11.084101.

[38] Chen, C.Y.; Goux, L.; Fantini, A.; Redolfi, A.; Clima, S.; Degraeve, R.; Chen, Y.Y., “ Understanding the Impact of Programming Pulses and Electrode Materials on the Endurance Properties of Scaled Ta2O5 RRAM Cells”, IEEE International Electron Devices Meeting, 2014, DOI: 10.1109/IEDM.2014.7047049.

[39] Chuang, K.-Ch.; Chu, Ch.-Y.; Zhang, H.-X.; Luo, J.-D., “ Impact of the Stacking Order of HfOx and AlOx Dielectric Films on RRAM Switching Mechanisms to Behave Digital Resistive Switching and Synaptic Characteristics”, IEEE Journal of the Electron Devices Society, 2019, DOI: 10.1109/JEDS.2019.2915975.

[40] Wang, G.; Long, Sh.; Yu, Z.; Zhang, M., “ Impact of program/erase operation on the performances of oxide-based resistive switching memory”, Nanoscale Research Letters, 2015, DOI: https://doi.org/10.1186/s11671-014-0721-2.

[41] Yuan, F.-Y.; Deng, N.; Shih, Ch., “ Conduction Mechanism and Improved Endurance in HfO2-Based RRAM with Nitridation Treatment” , Nanoscale Research Letters, 2017, DOI: https://doi.org/10.1186/s11671-017-2330-3.

[42] Nail, C.; Molas, G.; Blaise, P.; Piccolboni, G.; Sklenard, B., “Understanding RRAM endurance, retention and window margin trade-off using experimental results and simulations”, IEDM, 2016, DOI: 10.1109/IEDM.2016.7838346.

[43] Pérez, E.; Pérez-Ávila, A. J.; Romero-Zaliz, R., " Optimization of Multi-Level Operation in RRAM Arrays for In-Memory Computing", 2021, DOI: https://doi.org/10.3390/electronics10091084.

[44] García, H.; Dueñas, S.; Ossorio, Ó. G.; Castán, H., "Current Pulses to Control the Conductance in RRAM Devices", IEEE Journal of the Electron Devices Society, 2020, DOI: 10.1109/JEDS.2020.2979293.

[45] Chen, W.-Ch. ; Zhang, Y.-C. ; Chen, P.-H., "Investigation on the current conduction mechanism of HfZrOx ferroelectric memory", Applied Physics, vol. 53, 2020, DOI: 10.1088/1361-6463/aba6b5.

[46] Yu, Sh.; Wu, Y.; Jeyasingh, R.; Kuzum, D.; Wong, H. S., " An electronic synapse device based on metal oxide resistive switching memory for neuromorphic computation" , IEEE Transactions on Electron Devices, 2011, DOI: 10.1109/TED.2011.2147791.

[47] Pavoni, E.; Mohebbi, E.; Stipa, P.; Mencarelli, D.; Pierantoni, L.; Laudadio, E., " The Role of Zr on Monoclinic and Orthorhombic HfxZryO_2 Systems", A First-Principles Study. Materials, 2022, DOI: 10.3390/ma15124175.

[48] Mannocci, P.; Farronato, M.; Lepri, N.; Cattaneo, L. ; Glukhov, A.; Sun, Z.; Ielmini, D., "In-memory computing with emerging memory devices: Status and outlook", APL Machine Learning, 2023, DOI: https://doi.org/10.1063/5.0136403.

[49] Mutlu, O.; Ghose, S.; Gómez-Luna, J. ; Ausavarungnirun, R., "Processing data where it makes sense: Enabling in-memory computation", Microprocessors and Microsystems, vol 67, 2019, DOI: https://doi.org/10.1016/j.micpro.2019.01.009.

[50] Ielmini, D., "Brain-inspired computing with resistive switching memory (RRAM): Devices, synapses and neural networks", Microelectronic Engineering, vol 190, 2018, DOI: https://doi.org/10.1016/j.mee.2018.01.009.

[51] Rafiq, S.; " Application of Resistive Random Access Memory (RRAM) For Non-von Neumann Computing", SUNY, 2023, DOI: http://hdl.handle.net/20.500.12648/7333.