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ABSTRACT

CHARACTERIZATION OF SELF-HEATING EFFECTS AND ASSESSMENT OF ITS IMPACT ON RELIABILITY IN FINFET TECHNOLOGY

by
Peter Christopher Paliwoda

The systematically growing power (heat) dissipation in CMOS transistors with each successive technology node is reaching levels which could impact its reliable operation. The emergence of technologies such as bulk/SOI FinFETs has dramatically confined the heat in the device channel due to its vertical geometry and it is expected to further exacerbate with gate-all-around transistors.

This work studies heat generation in the channel of semiconductor devices and measures its dissipation by means of wafer level characterization and predictive thermal simulation. The experimental work is based on several existing device thermometry techniques to which additional layout improvements are made in state of the art bulk FinFET and SOI FinFET 14nm technology nodes. The sensors produce excellent matching results which are confirmed through TCAD thermal simulation, differences between sensor types are quantified and error bars on measurements are established.

The lateral heat transport measurements determine that heat from the source is mostly dissipated at a distance of 1µm and 1.5µm in bulk FinFET and SOI FinFET, respectively. Heat additivity is successfully confirmed to prove and highlight the fact that the whole system needs to be considered when performing thermal analysis. Furthermore, an investigation is devoted to study self-heating with different layout densities by varying the number of fins and fingers per active region (RX).

Fin thermal resistance is measured at different ambient temperatures to show its variation of up to 70% between -40°C to 175°C. Therefore, the Si fin has a more dominant effect in heat transport and its varying thermal conductivity should be taken into account. The effect of ambient temperature on self-heating measurement is confirmed by supplying heat through thermal chuck and adjacent heater devices themselves.

Motivation for this work is the continuous evolution of the transistor geometry and use of exotic materials, which in the recent technology nodes made heat removal more challenging. This poses reliability and performance concerns. Therefore, this work studies the impact of self-heating on reliability testing at DC conditions as well as realistic CMOS logic operating (AC) conditions. Front-end-of-line (FEOL) reliability mechanisms, such as hot carrier injection (HCI) and non-uniform time dependent dielectric breakdown (TDDB), are studied to show that self-heating effects can impact measurement results and recommendations are given on how to mitigate them. By performing an HCI stress at moderate bias conditions, this dissertation shows that the laborious techniques of heat subtraction are no longer necessary. Self-heating is also studied at more realistic device switching conditions by utilizing ring oscillators with several densities and stage counts to show that self-heating is considerably lower compared to constant voltage stress conditions and degradation is not distinguishable.

CHARACTERIZATION OF SELF-HEATING EFFECTS AND ASSESSMENT OF ITS IMPACT ON RELIABILITY IN FINFET TECHNOLOGY

by
Peter Christopher Paliwoda

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To Alicia

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LIST OF SYMBOLS

Symbol	Unit	Description
A	m^2	Area
C	J m^{-3} K^{-1}	Volumetric specific heat
D_N	m^2 s^{-1}	Electron diffusion coefficient
D_P	m^2 s^{-1}	Hole diffusion coefficient
e	C	Unit charge
E	J	Energy of one particle
E_a	J	Activation energy
E_f	J	Chemical potential
$\mathcal{E}$	V m^{-1}	Magnitude of electrostatic field
f		Distribution function
f_0		Equilibrium distribution function
f_e		Distribution function for electrons
f_p		Distribution function for phonons
f_{0e}		Distribution function for electrons at equilibrium
f_{0p}		Distribution function for phonons at equilibrium
F	N	External force
g_e	K^{-1} s^{-1}	Defined by equation on page 9
g_p	K^{-1} s^{-1}	Defined by equation on page 9

G	W m^{-3} K^{-1}	Electron-phonon coupling factor
I	A = C s^{-1}	Electric current
I_d or I_{ds}	A	Drain current
I_0	A	Saturation current
$\boldsymbol{J_e}$	A m^{-2}	Electron current flux vector
$\boldsymbol{J_h}$	A m^{-2}	Hole current density
$\boldsymbol{J_u}$	W m^{-2}	Flux of the total system energy
$\boldsymbol{J_{u,e}}$	W m^{-2}	Flux energy of electrons
k	m^{-1}	Phonon wavevector
k, k or k_{th}	W m^{-1} K^{-1}	Thermal conductivity
k_B	J K^{-1}	Boltzmann constant
k_e		Thermal conductivity of electron
L_N	m	Electron minority-carrier diffusion length
L_P	m	Hole minority-carrier diffusion length
m	kg	Electron effective mass
n		Phonon wavevector branch
n	m^{-3}	Electron concentration
n_i	m^{-3}	Intrinsic carrier concentration
N_A	m^{-3}	p-type dopant (acceptor) concentration
N_D	m^{-3}	n-type dopant (donor) concentration
p	m^{-3}	Hole concentration
q	C	Electronic charge (magnitude)
$\dot{q}$	W m^{-3}	Energy source term

R_{TH}	K W^{-1}	Thermal resistance
Q	W = J s^{-1}	Power dissipated
$\boldsymbol{Q_e}$	W m^{-2}	Electron heat flux
$\boldsymbol{Q_p}$	W m^{-2}	Phonon heat flux
r		Space coordinate vector
t	s	Time
t_{eff}	s	Effective time
T	K	Temperature
T_{amb}	K	Ambient temperature
T_e	K	Electron temperature
T_{op}	K	Temperature at operating condition
T_p	K	Phonon temperature
u	J m^{-3}	Total system energy per unit volume
u_e	J m^{-3}	Internal energy per unit volume for electrons
u_p	J m^{-3}	Internal energy per unit volume for phonons
v	m s^{-1}	Molecular instantaneous random velocity
v_s	m s^{-1}	Speed of sound for longitudinal phonons
v	m s^{-1}	Velocity
V	V	Voltage bias
V_b	V	Bulk voltage bias
V_d	V	Drain voltage bias

V_g	V	Gate voltage bias
V_s	V	Source voltage bias
V_D	V	Diode forward bias voltage
V_T or V_{Tlin}	V	Threshold voltage
Λ	m	Mean free path
τ	s	Relaxation or time constant
τ_e	s	Relaxation or time constant for electrons
τ_p	s	Relaxation or time constant for phonons
Π_e	V	Peltier coefficient
ψ_e	J	Combined Fermi energy and electrostatic potential energy of electrons
ψ_h	J	Combined Fermi energy and electrostatic potential energy of holes

CHAPTER 1

INTRODUCTION

The filing of the patent in 1925 by an Austrian-Hungarian physicist, Julius Edgar Lilienfeld on a method and apparatus for controlling electric currents [1] started an electronic era, which without a doubt changed many aspects and quality of our lives and still continues to do so. Modern microprocessors comprise of billions Metal-Oxide Semiconductor Field Effect Transistors (MOSFETs) which occupy a space of a fingernail-sized chip. The rise of computers enabled scientists and engineers to solve many complex problems in less time and gave means to continuously improve upon. The need for high performance computing and the competitive nature of the semiconductor industry motivates continuous scaling of the integrated circuit performance, power and circuit area which is ramped into manufacturing in two year cycles. The technology node names; 22nm, 14nm, 10nm, 7nm, et cetera, follow a 70% scaling trend of the transistor's linear physical dimension which enables doubling of circuit density every ~2 years as predicted by Moore's law [2].

While in early transistor technology nodes (>20nm) dynamic power was dominant, off-state leakage power will dominate <20nm nodes, which at the time of this writing is already one of the major power problems of cutting edge electronics. Nevertheless, active power dissipation is still on the rise, posing reliability and device performance degradation concerns.

Figure 1.1 clearly shows that transistor count continues to follow an exponential growth over time, however performance of the single-thread shows signs of saturation

and multi core solutions are utilized. The increase of >100x in typical microprocessor power over the past three decades (Figure 1.1) is an alarming reality, which requires an assessment and solutions in areas at risk.

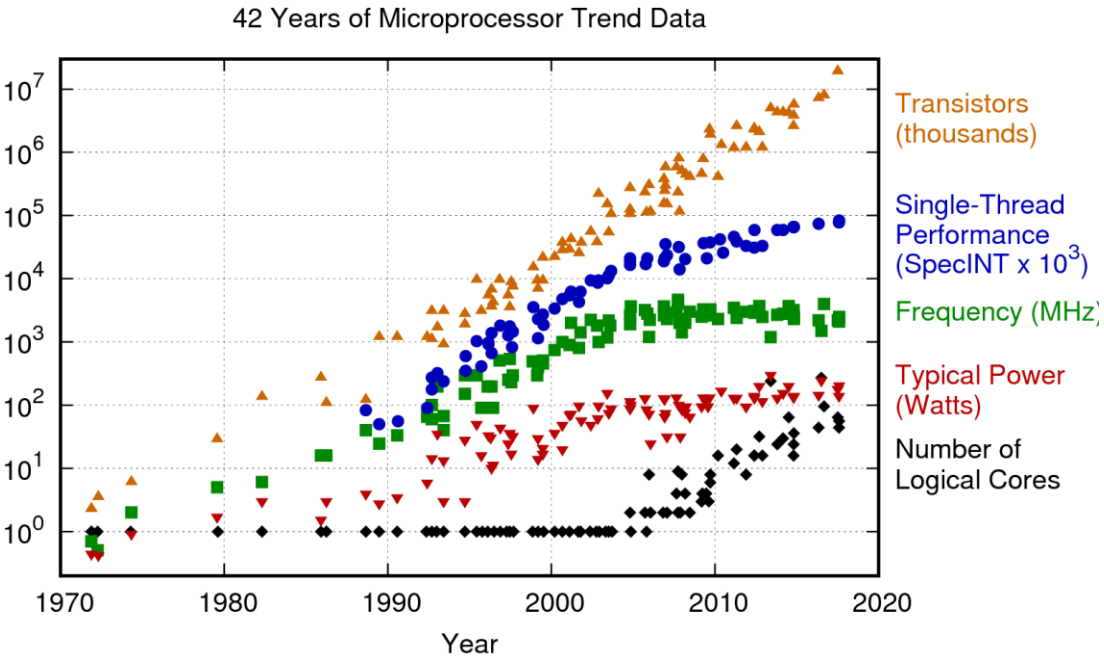


Figure 1.1 Historical comparison of transistor count, performance, power usage and number of logical cores over 42 years.
Source: Original data by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond and C. Batten; 2010-2017 added by K. Rupp

Many clever techniques have been developed to deal with both static and dynamic power dissipation. For dynamic power, frequency scaling helped to reduce power in less prioritized computational tasks and voltage scaling has been implemented to deal with off state power dissipation which both reduce power consumption and extend battery life in hand held electronics. Furthermore, many package cooling techniques have been implemented to dissipate power faster such as more effective heat sinks or on-package liquid cooling systems which are needed in high computational applications such as data servers. Better understanding of heat conduction and generation in current and future

semiconductor technologies can be achieved both through thermal characterization and TCAD modeling. Such learning can aid in further improving the reduction of self-heating impact on device performance and reliability, which this dissertation will address.

The increase of total heat rate of modern microprocessors has been addressed at interconnect and chip level [3, 4]. However, a similar thermal issue also faces circuit designers at nanometer length scales, in the transistor channel itself where considerable heat is released from the kinetic energy of the current flow. To further emphasize this concern, recent changes of the transistor geometry and introduction of new heterogeneous materials, has made the heat dissipation more difficult, making this topic important to research. Figure 1.2 illustrates the comparison of the thermal conductivities of common semiconductor and dielectric materials as a function of temperature.

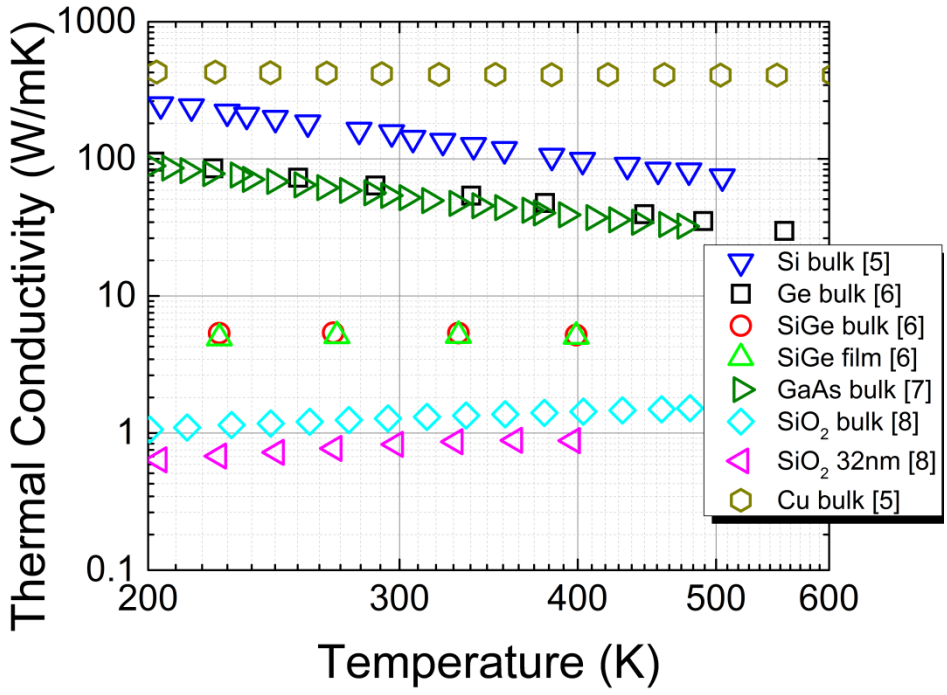


Figure 1.2 Thermal conductivities of common materials used in semiconductor manufacturing and their modulation with respect to temperature. Reduction in thermal conductivity is observed in alloy materials and dielectrics if compared to bulk Si or Ge.

Significant reduction of thermal conductivity in bulk Si is observed at increased temperatures, which has an opposite, but negligible effect in dielectrics and constant effect in copper material. Moreover, a clear reduction of thermal conductivity is observed in alloys and dielectrics if compared to Si or Ge. Search of new semiconductor materials with improved electrical and thermal properties is an active effort. Some success was observed in [9], where a thermal conductivity of 1300 (W/mK) in defect free (III-V) BAs material was reported. The findings in this dissertation will often rely on Figure 1.2 for explanation purposes.

While in operation, active and passive nanoscale electronic devices dissipate power locally in the form of heat. In a transistor, applied voltage to the channel leads to creation of an electric field that accelerates free charge carriers which gain energy and heat up. Electrons can deviate (scatter) from their path due to other electrons, phonons (lattice vibrations), interfaces or lattice imperfections. However, when scattered with phonons, electrons lose energy which in effect heats up the lattice via mechanism known as joule-heating or self-heating (SH). Electron-phonon scattering is a sum of inelastic and elastic scattering processes, of which the inelastic process is responsible of transforming the electron's kinetic energy into form of heat or lattice vibrations.

Heat transport can occur through the process of conduction, convection or radiation. Heat conduction requires a medium to transfer energy, as is the case in semiconductor material, where the heat transfer is caused by a temperature difference due to the random motion of the silicon lattice. Convection heat transfer involves a bulk fluid motion with overlaps a temperature gradient and radiation heat transfer does not require a

medium, it can propagate through vacuum, where energy is carried by electromagnetic waves.

In metals, both electrons and phonons are considered heat carriers, but majority of energy flux is carried by electrons due to their abundance and greater velocity in such a medium. In semiconductors on the other hand, again both electrons and phonons act as heat carriers, but majority of heat is carried by phonons because concentration of free electrons in a semiconductor is much lower than in metals. Therefore, semiconductor doping concentration level will govern how much energy flux can be carried by electrons in a transistor channel, but it is usually negligible.

1.1 Motivation

While in bulk planar transistors heat dissipates by the process of conduction, vertically from the channel into the bulk material and laterally to source and drain contacts. In bulk FinFETs the same heatsink pathways are more confined due to its vertical geometry and poorly thermally conductive gate oxide which wraps the fin, making its narrow bulk connection the preferred heatsink pathway. Still, the channel operates at high voltage and current density which in combination with heat and poor thermal dissipation leads to a considerable self-heating effect.

1.1.1 Self-Heating Effects on Semiconductor Devices

Temperature has a direct and or inverse impact on many semiconductor parameters which can vary device performance and its reliability. The main performance parameters which are sensitive to temperature are; threshold voltage, channel mobility, off-

state/junction/gate leakage and subthreshold slope of which only off-state/junction and gate leakage in Poole-Frenkel carrier transport mode show strongest thermal modulation. In the front-end-of-line devices, degradation mechanisms such as bias temperature instability (BTI), PMOS hot carrier injection (HCI) and time dependent dielectric breakdown (TDDB) are all aggravated by increase in temperature. HCI and non-uniform TDDB at constant voltage stress are most prone to self-heating effects due to channel current, which is present during stress. Nevertheless, self-heating due to switching, in highly dense and power hungry complementary logic circuits can also affect neighboring metal lines and accelerate other degradation mechanisms such as electronmigration (EM). Therefore, self-heating effects need to be understood in two operating conditions, switching as is the case in standard logic circuits and constant voltage stress as seen during reliability testing for end-of-life projections.

Local self-heating can potentially affect device performance due to inconsistency in threshold voltage (V_T) and aggravate the effects of reliability mechanisms [10, 11, 12, 13]. With increasing switching speeds of successive technology nodes and thus rising dynamic power dissipation, the reliability degradation is accelerated for both the transistors and upper metal lines due to increased heat. This causes a reliability risk for metal lines, neighboring the power hungry circuit blocks, such as the clock buffers, which can create heat persistence modes leading to local hot spot effects. For design considerations and benchmarking across different technologies, quantifying self-heating and understanding its impact on reliability is essential for successful technology scaling.

1.2 Objective

The objective of this dissertation is to demonstrate different self-heating measurement methodologies on bulk FinFET and SOI FinFET devices and verify the results through predictive TCAD thermal simulation. Further objective is to study the impact of self-heating on reliability characterization assessment and its correlation to performance degradation. The resources utilized to perform the experimental work include; Cascade Microtech Elite 300 wafer prober, Keysight B1500A semiconductor analyzer, Keysight B2201A switching matrix and state of the art bulk/SOI 14nm FinFET wafer samples provided by GLOBALFOUNDRIES, Inc. Prober thermal chuck was used for testing at different temperatures. Because most reliability degradation mechanisms are accelerated at higher temperatures due to its Arrhenius relationship, study of self-heating effects on device performance and degradation are crucial for correct device end-of-life projections. Thus, methods to de-convolute self-heating from reliability testing and reduce its impact on device performance are needed, which will be addressed in this dissertation. Special structures were designed to study self-heating effects both in AC and DC conditions with different layout densities. With the established and verified self-heating characterization methods, this work compares the level of SH between bulk FinFET and SOI FinFET technologies. Furthermore, the dissertation assesses the impact of layout density and ambient temperature on SH characterization. Moreover, this work will evaluate the impact of self-heating on device reliability and ring-oscillator performance and propose methods to mitigate these effects. This dissertation will then summarize all the learning, draw conclusions and list areas which still need further exploration.

1.3 Heat Conduction in Semiconductors

To accurately quantify amount of heat generated in semiconductor devices under nominal operation or stress conditions, both experimental measurements and predictive simulation need to be employed. Experimental measurements aid in verifying the accuracy of the simulated results and simulation helps to quantify heat in regions which are difficult to resolve through experimental measurement. In bulk silicon the mean free path of an electron and phonon ranges from 5-10nm and 200-300nm, [14, 15] respectively. The classical heat conduction can no longer be well predicted by classical Fourier law equations as current feature size (7nm at the time of this writing) is well below the mean free path length scales, therefore quantum size effects need to be considered. To achieve correct models, the process needs to start with *ab-initio* density functional theory (DFT) simulations to predict electron/phonon transport properties in semiconductor materials and across wire/via interfaces to be then fed into continuum TCAD simulations of the 3D heat diffusion equation which incorporates the thermal conductivity of materials. Thermal conductivity of a semiconductor material can be well approximated by Equation (1.1) [5].

$$k = \frac{Cv^2\tau}{3} = \frac{Cv\Lambda}{3} \tag{1.1}$$

where C is the volumetric specific heat, v is the molecular instantaneous random velocity of a phonon, τ is the relaxation time also known as the time constant and $\Lambda = v\tau$ is the mean free path (average distance carrier of heat travels before scattering and losing its excess energy). *Ab-initio* methodologies have been developed that allow the calculation of C, v, and τ for bulk materials. Phonon boundary scattering can be accounted for in

Equation (1.1) by adding an extra term to the relaxation time using Matthiessen's rule. The classical heat conduction Equation (1.2) [5] can be written as,

$$C\frac{\partial T}{\partial t} = \nabla \bullet (k\nabla T) + \dot{q} \tag{1.2}$$

where $\dot{q}$ can be identified as the energy source term. Equation 1.2 cannot properly resolve heat transfer quantity at small time scales of phonon relaxation times (nanoseconds) or at length scales shorter than an acoustic phonon mean free path (<10nm) [16]. At such scales a more elaborate formulation is needed which can discretize phonons energy and account for their frequency and different modes. The Boltzmann Equations (1.3) [5] for electrons and phonons, which accounts for coupled non-equilibrium Electron-Phonon transport without recombination, can be respectively written as

$$\begin{aligned}
&\frac{\partial f_e}{\partial t} + \mathbf{v} \bullet \nabla_{\mathbf{r}} f_e + \frac{\mathbf{F}}{m} \bullet \nabla_{\mathrm{v}} f_e = g_e\left(T_e - T_p\right) - \frac{f_e - f_{0e}}{\tau_e} \\
&\frac{\partial f_p}{\partial t} + \mathbf{v} \bullet \nabla_{\mathbf{r}} f_p = -g_p\left(T_e - T_p\right) - \frac{f_p - f_{0p}}{\tau_p}
\end{aligned} \tag{1.3}$$

where the subscripts e and p denote electron and phonons, respectively, f is the probability distribution function, **v** is the velocity, **r** is the space coordinate vector, **F** is the external force on the electron, m is mass, T is temperature, τ is the relaxation time and g can be related to the relaxation time as $g_{e,p} = \frac{2mv_s^2 E f_0}{k_B^2 T_e^2 T_p \tau}$ [5] for electrons and phonons.

From the Boltzmann Equations (1.3) for electrons and phonons, one can derive the energy conservation Equations (1.4) for electrons and phonons, respectively [5].

$$\frac{\partial u_e}{\partial t} + \nabla \bullet \boldsymbol{Q_e} - G(T_e - T_p) = \left(\mathcal{E} + \frac{\nabla E_f}{e}\right) \bullet \boldsymbol{J_e}$$
$$\frac{\partial u_p}{\partial t} + \nabla \bullet \boldsymbol{Q_p} + G(T_e - T_p) = 0 \qquad (1.4)$$

Where, in energy conservation equation for electrons; $\boldsymbol{Q_e}$ is the heat flux carried by electrons, including both heat conduction flux and Peltier heat flux, $\mathcal{E}$ is the electric field, $\boldsymbol{J_e}$ is the current density of electrons and the right-hand side is considered as Joule heating and thus a heat source term [5]. In the energy conservation for phonons (1.4), $\boldsymbol{Q_p}$ is the phonon heat flux. Because of difficulty in solving Boltzmann equations, the solutions can be achieved through Monte Carlo methods [17, 18] or finite volume methods [19] to calculate for thermal conductivity of a given material. The equations listed in (1.3) and (1.4) are limited to single type of charged carrier. However, a realistic semiconductor has both electrons and holes, where the recombination of an electron and hole can lead to emission of heat or light. The next section will focus on the formulation of a source term $\dot{q}$, which accounts for recombination.

1.4 Heat Source in Semiconductors

Heat source in a transistor occurs due to current flow through the channel and therefore power dissipated can be expressed as the product of current and voltage (1.5).

$$Q = VI \qquad (1.5)$$

While Equation (1.5) offers good first order characterization results, it does not account for power loss in the instrumentation wire, semiconductor interconnect, vias and contacts.

For accurate transistor channel self-heating quantification such power drops need to be accounted for. Furthermore, it is important to understand that electrons do not entirely give up its energy in the semiconductor channel through scattering with phonons. Electrons also dissipate considerable amount of power in the contacts especially near the grounded source region where due to peak electric field, gain most energy. The rest of heat energy is dissipated in the interconnect wiring. Due to the fact that semiconductor material has both electrons and holes, which can recombine and release energy as either heat or light during transport, it is important in modeling to know where this takes place. The energy source term was discussed in [20, 21] where both treated the formulation of energy conservation as in Equation (1.6) [5].

$$\frac{\partial u}{\partial t} + \nabla \bullet \boldsymbol{J_u} = 0 \tag{1.6}$$

Where in Equation (1.6), u is the total energy per unit volume, and $\boldsymbol{J_u}$ is the flux of the total system energy. Neither [20] nor [21] formulations include nonlocal transport effects and thus their usability in modeling heat transport in nanoscale devices should be taken with doubt. The extension to include nonlocal transport and nonequilibrium between carriers was derived in [5], where Equation (1.6) was casted onto equation (1.2) by deriving the energy source term, $\dot{q}$ which includes these effects. This can be accomplished by first, including electrons, holes and phonons into u of Equation (1.6). Where, the rate of internal energy change can be expressed as in Equation (1.7) [5].

$$\frac{\partial u}{\partial t} = C\,\frac{\partial T}{\partial t} + \left[\psi_e - T\left(\frac{\partial \psi_e}{\partial T}\right)_n\right]\frac{\partial n}{\partial t} - \left[\psi_h - T\left(\frac{\partial \psi_h}{\partial T}\right)_p\right]\frac{\partial p}{\partial t} \tag{1.7}$$

Where in Equation (1.7), C is the volumetric specific heat of electrons, holes and phonons, p is the concentration of holes, and ψ_h is combined Fermi energy and electrostatic potential energy of holes [5]. Second, the energy flux of electrons of the total system in (1.6) is composed of the heat flux and the flux of electrochemical potential as expressed in (1.8) [5],

$$\boldsymbol{J_{u,e}} = \boldsymbol{Q_e} - \frac{\psi_e}{e}\boldsymbol{J_e} = \left(\Pi_e - \frac{\psi_e}{e}\right)\boldsymbol{J_e} - k_e \nabla T \tag{1.8}$$

where Π_e is the Peltier coefficient, $\boldsymbol{J_e}$ is the electron current flux vector, and k_e the electron thermal conductivity. Similar expression (1.8) can also be derived for energy flux of holes. Substituting equations (1.7) and (1.8) into equation (1.6), one can arrive at Equation (1.9) with the following expression for the energy source term [5], to be ultimately substituted into Equation (1.2).

$$\dot{q} = -\nabla \bullet \left[\left(\Pi_e - \frac{\psi_e}{e}\right)\boldsymbol{J_e} + \left(\Pi_h - \frac{\psi_h}{e}\right)\boldsymbol{J_h}\right] - \left[\psi_e - T\left(\frac{\partial \psi_e}{\partial T}\right)_n\right]\frac{\partial n}{\partial t} + \left[\psi_h - T\left(\frac{\partial \psi_h}{\partial T}\right)_p\right]\frac{\partial p}{\partial t} \tag{1.9}$$

Where, in Equation (1.9) $\boldsymbol{J_h}$ is the hole current density. The divergence term includes the energy gain from the external field, the Joule heating, the Thomson effect, and the heat generation by recombination [5]. The time-dependent terms in Equation (1.9) signify the loss of carrier energy during transient processes.

1.5 Dissertation Organization

1.5.1 Chapter 2

Chapter 2 will discuss the state of the art in self-heating research showing the understanding of problem statement and physics involved. Furthermore, quantification of self-heating will be presented with different thermally sensitive parameters which enable temperature characterization at wafer level test. Circuit layout density impact on self-heating will be explained and reliability implications examined based on research completed thus far. The research will be summarized and used as basis for subjects studied in the following chapters.

1.5.2 Chapter 3

Self-heating measurement methodologies including several sensor layout designs will be shown in Chapter 3. Detailed wafer level temperature characterization procedure will be explained. Moreover, self-heating measurement results will be compared and additivity of heat confirmed. Method and quantification of temperature error bar from measurements will be shown and self-heating sensor verification through stress cycle performed. The measurement results will be verified through TCAD thermal simulations, which will also reveal more learning on resolution of heat at regions unresolvable by measurement. Chapter 3 will also compare levels of self-heating between bulk FinFET and SOI FinFET technology to show ~5x more in the latter. Self-heating sensing techniques will be summarized and compared against each other and conclusions presented.

1.5.3 Chapter 4

Chapter 4 will focus on an experimental investigation of several effects on self-heating characterization such as layout density, measurement of the radial lateral heat dissipation distance affected by heat source in bulk and SOI front-end-of-line circuits and the impact of ambient temperature on heat conductivity in semiconductor devices. Characterization of ambient temperature effects on self-heating measurement will be verified both by introducing the heat by wafer level prober thermal chuck and by adjacent heater devices themselves. This will ultimately prove that, ambient temperature can substantially affect self-heating characterization and thus the thermal conductivity at FinFET level. The summarized findings in this chapter will be essential for further investigation of self-heating effects on reliability in FinFET technology presented in Chapter 5.

1.5.4 Chapter 5

Verified test structures and a more robust understanding of self-heating characterization will bring this dissertation to study the reliability impact due to self-heating effects which will be the focus of Chapter 5. Specific structures for the design of experiments will be presented, including discrete structures for DC regime examination as seen in accelerated reliability testing and ring-oscillators for AC conditions as seen by standard logic circuits of electronic products. Self-heating due to device/circuit ON time in both operating cases will be quantified and its effects on hot carrier reliability and performance presented. Furthermore, to mitigate the effects of self-heating during DC hot-carrier degradation testing, a method of using moderate constant voltage stress will be presented which greatly reduces the impact of self-heating on device end-of-life projections. Non-uniform

time dependent dielectric breakdown (TDDB) testing will examine the impact of self-heating on device time to breakdown and identify the general region of the breakdown along the channel. Additionally, in Chapter 5, results of experimental work will show no detrimental performance reliability impact due to self-heating effects on standard cell logic circuits, operating in switching conditions, based on measurements completed on different circuit densities at accelerated stress voltage conditions.

1.5.5 Chapter 6

Lastly, Chapter 6 will make conclusions based on the study cases of this dissertation and state recommendations based on the learning. Furthermore, future work will be discussed by highlighting key items which still need exploration and solutions.

CHAPTER 2

STATE OF THE ART

Thin body silicon FET devices such as bulk/SOI FinFET are now a reality. These novel devices make heat removal challenging which poses a problem to understand and deal with. Self-heating in semiconductors has been researched for the past 5 decades [22, 23, 24] with many advancements being made in its understanding and measurement capabilities both through characterization and TCAD thermal modeling. The state of the art in topics focusing on phonon effects and understanding of thermal conductivity in semiconductors, quantification of transistor self-heating, impact of layout on self-heating and transistor reliability will be presented in this chapter.

2.1 Phonon Confinement Effects

It has been shown that semiconductor channel thickness can modulate its thermal conductivity [15, 25, 26, 27, 28]. With major re-structuring of transistor geometry, advancing from planar to FinFET, emphasizes the need in understanding its impact on device performance or reliability. FinFET was introduced with many advantages, such as increased voltage headroom or higher drive currents, on the other hand its thermal characteristics is worse when compared to planar technology. Figure 2.1 compares how thermal conductivity scales with silicon layer thickness in bulk SOI, InP and GaAs substrates. The illustrated decrease in thermal conductivity for thinner SOI is due to phonon boundary scattering modes which increase with the decrease in layer thickness [27]. Quantum mechanics treat heat carriers such as electrons and phonons as material waves. Systems of finite size (i.e FinFET) can influence energy transport by altering the

wave characteristics by forming standing waves and creating new modes, which do not exist in bulk materials [5]. Standing waves, as the name implies, can oscillate the heat energy in one place without fast displacement. Thus, Figure 2.1 concludes that more self-heating can be expected from transistors built on SOI, InP or GaAs [25, 27] substrates compared to bulk silicon. Furthermore, increase in self-heating is also expected from fin engineering, where the fin aspect ratio can increases due to growing fin height and thinning of the fin, to ultimately boost the device performance.

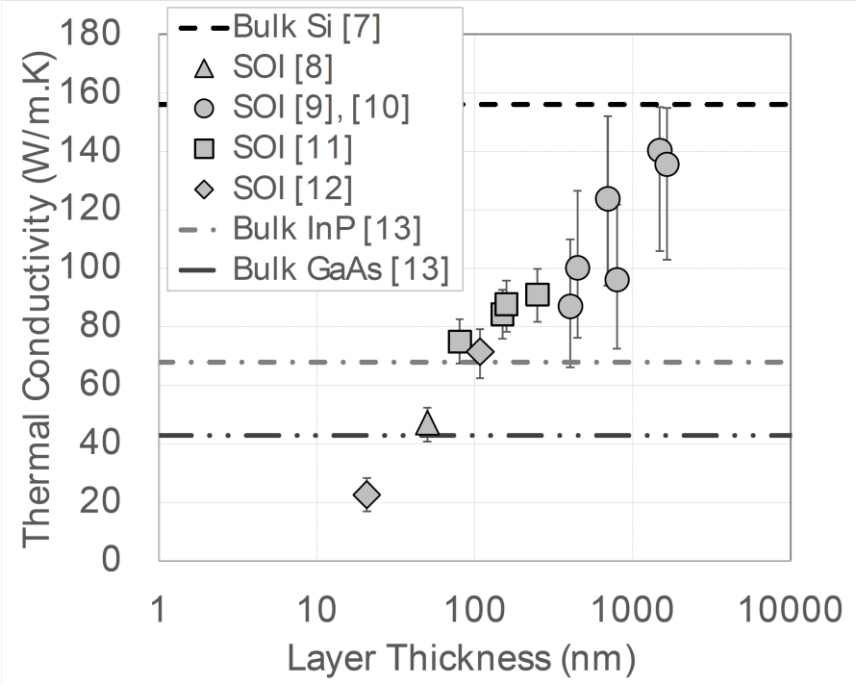
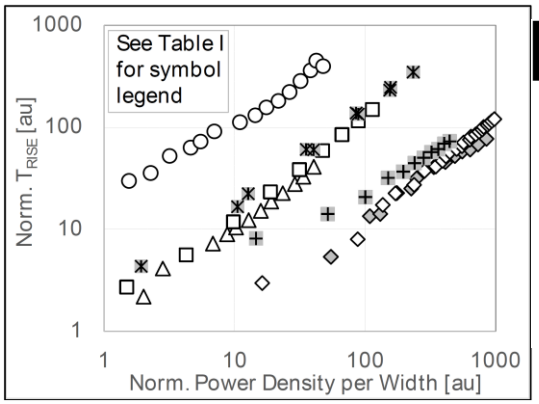


Figure 2.1 A summary of thermal conductivity data at 300 K for various bulk and SOI materials, showing strong scaling of thermal conductivity with Si layer thickness.
Source: C. Prasad, S. Ramey and L. Jiang, "Self-heating in advanced CMOS technologies," IEEE International Reliability Physics Symposium (IRPS), Monterey, CA, pp. 6A-4.1-6A-4.7, 2017.

Thermal conductance degradation is also device architecture and topology dependent. While planar SOI transistors allow for thermal transport in the lateral direction and limit it in the vertical direction, the SOI FinFETs limit thermal transport in

both directions. Device topology and architecture dependence on self-heating can be compared by studying the reciprocal of thermal conductivity, the thermal resistivity, which is a ratio of temperature rise to power, dissipated over distance as represented by the slope of Figure 2.2.



Symbols	Reference	Substrate	Transistor Topology	Drawn Gate Length	Self-Heat Measurement
△	[14]	PDSOI	Planar	130 nm	Gate/Metal TCR
◆	[15]	PDSOI	Planar	2 µm	AC conductance & Noise thermometry
◇	[15]	FDSOI	Planar	3 µm	Gate/Metal TCR
□	[16]	Bulk Si	Tri-gate/FinFET	30 nm	Gate/Metal TCR
✱	[17]	Bulk Si	Tri-gate/FinFET	28 nm	Gate/Metal TCR
+	[17]	Bulk Si	Tri-gate/FinFET	160 nm	Gate/Metal TCR
○	[18]	Bulk Si	GAA Nanowire	130 nm	AC conductance

Figure 2.2 A normalized plot of temperature rise (T_{RISE}) as a function of power density per transistor width across different device architectures and substrate types, demonstrating the impact of phonon confinement on local self-heating effects.
Source: C. Prasad, S. Ramey and L. Jiang, "Self-heating in advanced CMOS technologies," IEEE International Reliability Physics Symposium (IRPS), Monterey, CA, pp. 6A-4.1-6A-4.7, 2017.

The greater thermal headroom of bulk Si substrate in Figure 2.2 is the first observation, where the laterally confined 28-30nm bulk FinFETs (squares & asterisks) measure similar temperature rise when compared with 130nm planar PDSOI (triangles) or noting matching results of 2-3um planar SOI substrate topology (diamonds) to 160nm bulk silicon FinFET (crosses). The gate-all-around transistor (circles) shows an order of magnitude higher self-heating when compared to same gate length planar PDSOI and gives insight as to what self-heating levels can be expected in future device architectures [29, 30].

Most heat in the channel of bulk FinFET technology is dissipated down the fin and into the bulk substrate with small fraction of heat also dissipating through the

source/drain contact regions as shown in Figure 2.3. It has also been shown [31] that thermal conductivity from the fin to substrate decreases as the fin aspect ratio increases, demonstrated in Figure 2.4, due to a thermal bottleneck, which makes phonon scattering modes more pronounced.

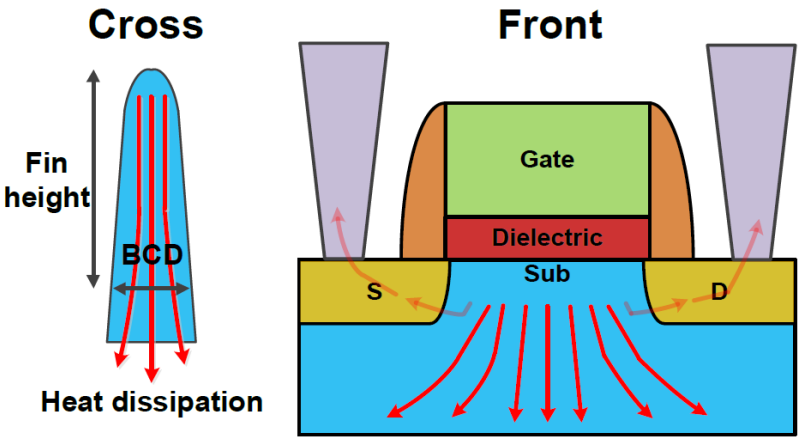


Figure 2.3 FinFET self-heat, during transistor operation gets dissipated via several nano-meters of Fin width to bulk substrate and also through the contacts.
Source: H. C. Sagong, K. Choi, J. Kim, T. Jeong, M. Choe, H. Shim, W. Kim, J. Park, S. Shin, and S. Pae, "Modeling of FinFET Self-Heating Effects in multiple FinFET Technology Generations with implication for Transistor and Product Reliability," Symposium on VLSI Technology (VLSI Technology), Honolulu, 2018.

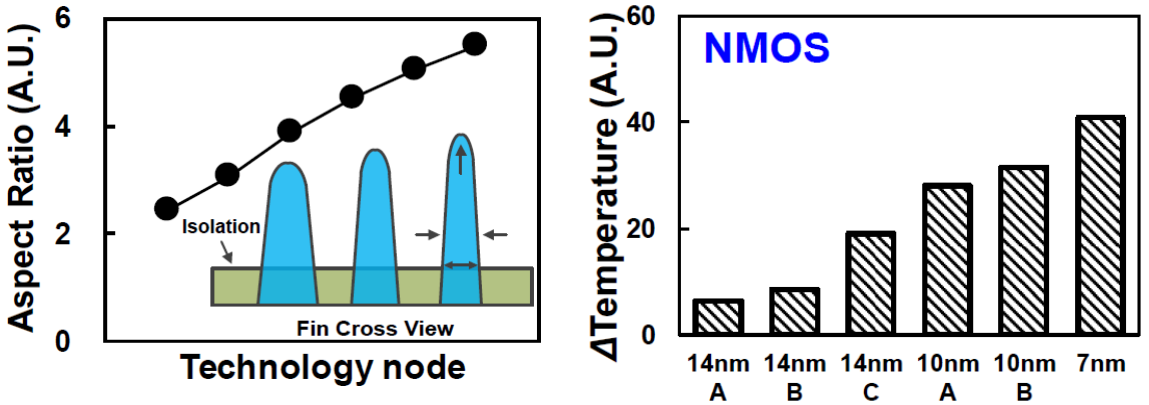


Figure 2.4 With increased aspect ratio in advancing technology node (left) NMOS FinFET and PMOS (not shown) exhibits self-heating temperature increase (@same power).
Source: H. C. Sagong, K. Choi, J. Kim, T. Jeong, M. Choe, H. Shim, W. Kim, J. Park, S. Shin, and S. Pae, "Modeling of FinFET Self-Heating Effects in multiple FinFET Technology Generations with implication for Transistor and Product Reliability," Symposium on VLSI Technology (VLSI Technology), Honolulu, 2018.

2.2 Quantification of Self-Heating

Quantification of self-heating in transistors can be measured via analytical methods; such as imaging, microscopy or spectroscopy, through electrical characterization methods and TCAD thermal simulations. Analytical methods require a specialized instrumentation setup as well as measurement sample preparation, which is beneficial for accurate measurements, such as the thermal time constant [32] determination, but may not be suitable for self-heating effects study on reliability, which is a goal of this dissertation. This dissertation mostly focuses on characterization methods of self-heating via electrical measurements, which offers a convenient and fast study of its impact on device reliability. However, predictive TCAD simulation is also used to calibrate the results and account for any heat loss. The accuracy of quantifying heat via electrical methods depends on the proximity of the sensor to the transistor generating heat. Since transistor electrical and material properties are temperature sensitive, this offers the convenience for simple heat sensor designs. Listed in Table 2.1 are parameters in solid state devices which exhibit modulation with the change of local temperature, thus offering ways to measure semiconductor device average temperatures.

Table 2.1 Transistor Parameters with Thermal Dependence

Parameter	Dependence	Sensitivity
Threshold voltage V_T	Inverse with absolute value	Intermediate
Junction linear current	Direct	Intermediate
Junction leakage current	Direct	Strong
Gate metal resistance	Direct	Weak to strong
Subthreshold slope	Direct	Strong
Channel linear mobility	Inverse	Intermediate to strong
Saturation currents	Inverse	Weak

Device currents in off-state region as well as subthreshold slope have the strongest response to change in temperature, while currents in device saturation region show a weaker response. Device currents in the linear region show an intermediate sensitivity to heat, however offer the benefit of being de-coupled from off-state noise levels. For this reason, intermediate sensitivities are preferred parameters used in this dissertation to make an effective average temperature measurement. Leakage currents are not chosen in this dissertation as these sensing parameters are masked by noise levels, which measurement instrumentation cannot distinguish to accurately resolve the true value. It is important to mention that the heat sensitive parameters listed in Table 2.1 offer a choice to the designer; however heat loss due to heater to sensor proximity should be accounted for and considered in the first stages of the experiment design.

Close sensor-to-heater proximity is ideal for self-heating measurements; therefore special care must be given in sensor/heater design to avoid current leaking from heater to sensor which can give misleading results. Both, neighboring or localized self-heating sensors themselves offer near accurate temperature measurement capability. Figure 2.5 shows a linear temperature rise due to heat dissipated in a transistor using a metal-stack sensor for measurement [10]. This sensor (interconnect at metal1 level) utilizes its temperature sensitive coefficient of resistance (TCR) to compare self-heating in different gate stacks of varied transistor performance. The result is a temperature rise due to power dissipated in the heater transistor structures as depicted in Figure 2.5, where the slope represents the thermal resistance R_{TH}, which measures the temperature difference by which a material resists heat flow and is often used as a metric in self-heating measurements.

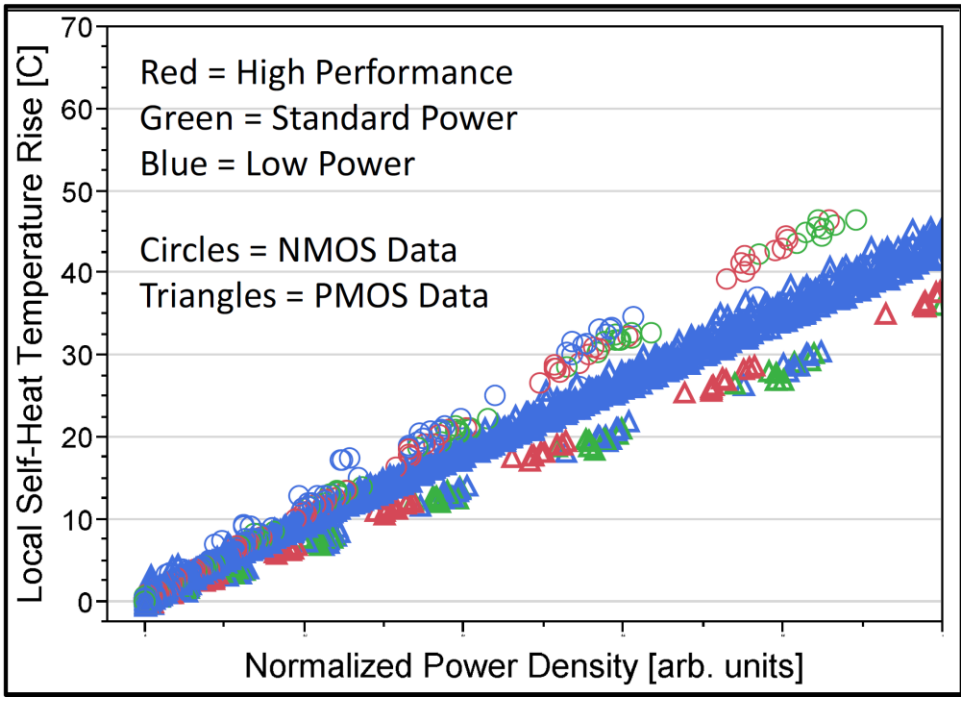


Figure 2.5 Measurement of local self-heat temperature rise on the metal sensor.
Source: C. Prasad, L. Jiang, D. Singh, M. Agostinelli, C. Auth, P. Bai, T. Eiles, J. Hicks, C. H. Jan, K. Mistry, S. Natarajan, B. Niu, P. Packan, D. Pantuso, I. Post, S. Ramey, A. Schmitz, B. Sell, S. Suthram, J. Thomas, C. Tsai and P. Vandervoorn, "Self-heat reliability considerations on Intel's 22nm Tri-Gate technology," IEEE Reliability Physics Symposium (IRPS),pp. 5D.1.1-5D.1.5, 2013.

2.3 Layout Impact on Self-Heating

Quantification of self-heating due to layout density can enable integrated circuit designers make optimal choices and reliable circuit designs. It was shown, that the general lateral influence region of the local self-heat is observed well within 1 um [10] for bulk FinFET technology. Furthermore, there is a clear distinction (Figure 2.6) between the levels of heat generated as a function of increasing active heater count (active heater gates). This means that self-heating is correlated to the density of the circuitry around it as well as the layout itself. Currently, these layout effects remain poorly understood, which this dissertation will address.

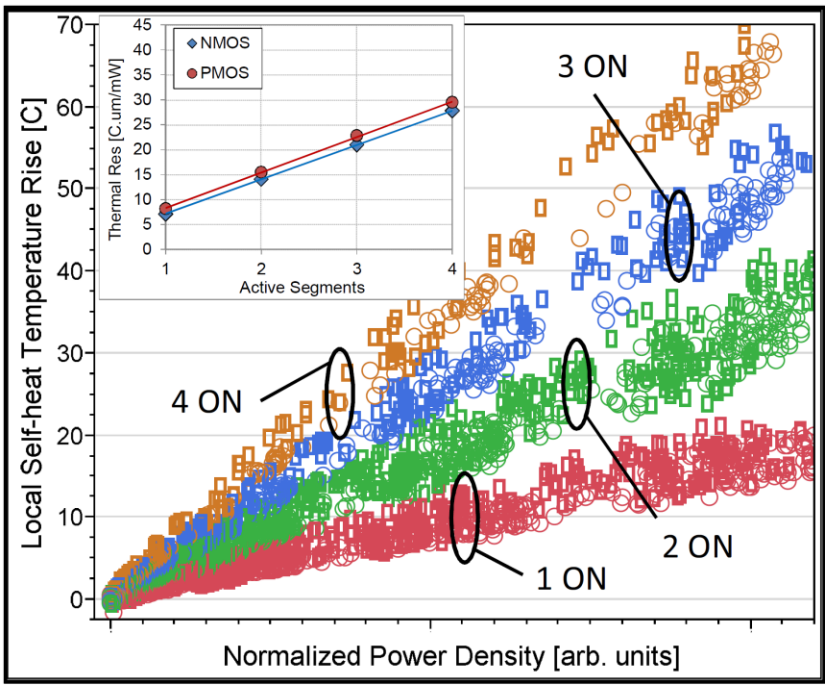


Figure 2.6 Response of thermal resistance to the number of powered heater segments.
Source: C. Prasad, L. Jiang, D. Singh, M. Agostinelli, C. Auth, P. Bai, T. Eiles, J. Hicks, C. H. Jan, K. Mistry, S. Natarajan, B. Niu, P. Packan, D. Pantuso, I. Post, S. Ramey, A. Schmitz, B. Sell, S. Suthram, J. Thomas, C. Tsai and P. Vandervoorn, "Self-heat reliability considerations on Intel's 22nm Tri-Gate technology," IEEE Reliability Physics Symposium (IRPS),pp. 5D.1.1-5D.1.5, 2013.

2.4 Reliability Implications due to Self-Heating

The end-of-life (EOL) degradation is an important reliability metric which predicts how long devices will operate dependably in the field. Since heat can accelerate device degradation for most reliability mechanisms, it is important to study how much self-heating contributes to this effect. Illustrated in Figure 2.7 are several layout scenarios that were measured for hot carrier injection (HCI) EOL, modulated by the dependence of device layout density. Design #6 in Figure 2.7 is expected to generate most localized heat due to highest number of gates and fins per active region, thus reducing the effective EOL as reflected in Figure 2.8.

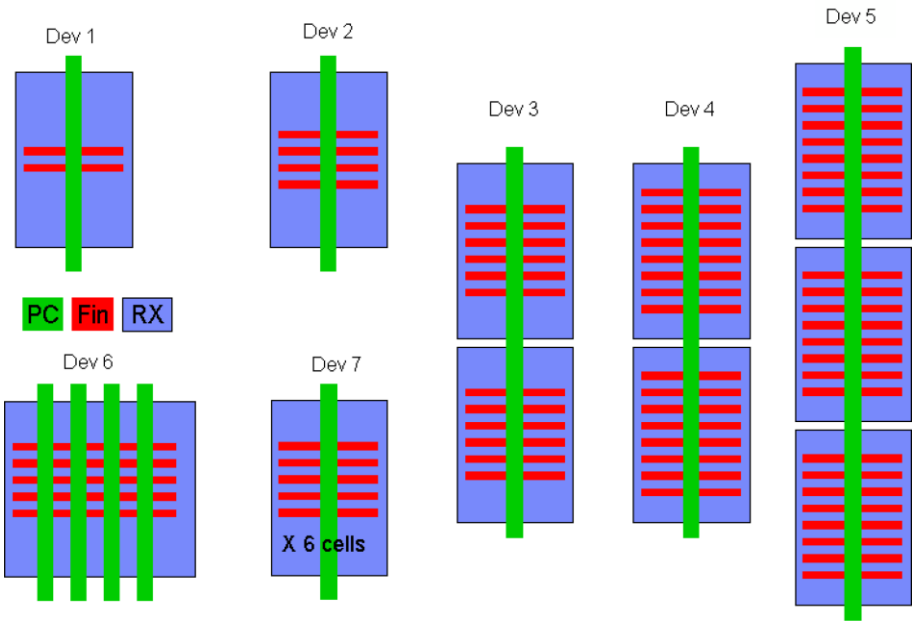


Figure 2.7 FinFET device layouts studied which are referenced in Figure 2.8.
Source: S. Mittl and F. Guarín, "Self-heating and its implications on hot carrier reliability evaluations," 2015 *IEEE International Reliability Physics Symposium (IRPS), Monterey, CA, pp. 4A.4.1-4A.4.6, 2015.*

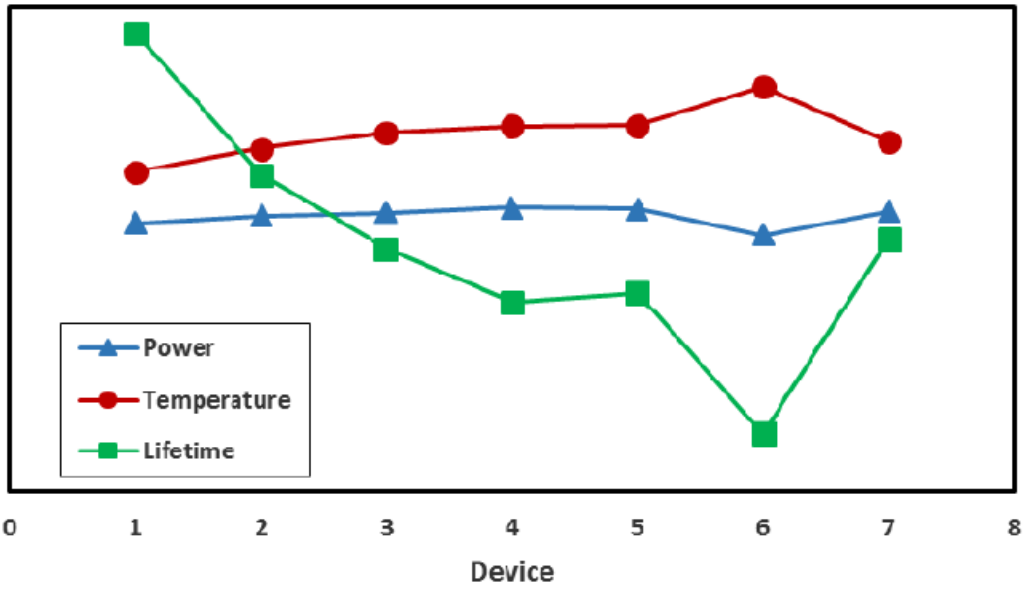


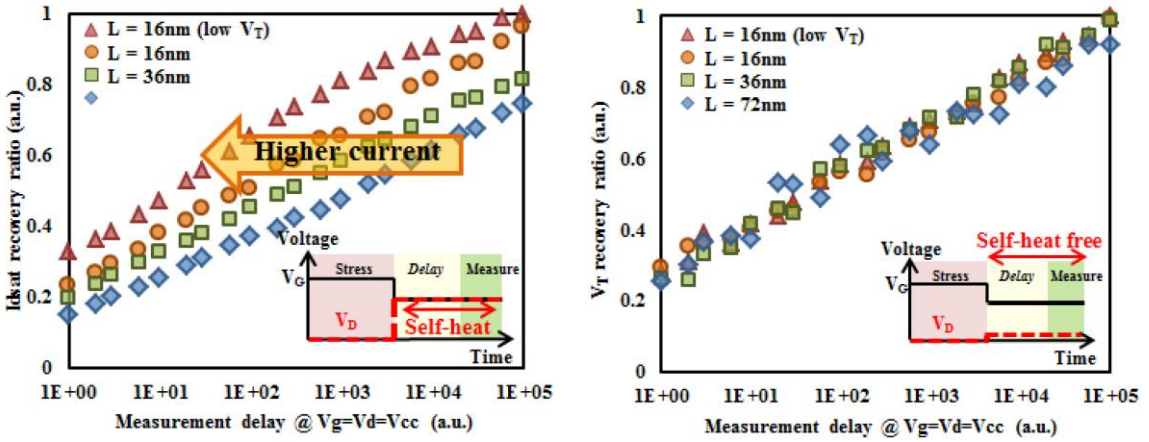
Figure 2.8 Stress power per unit width, calculated device stress temperature and extracted Lifetime for various layouts.
Source: S. Mittl and F. Guarín, "Self-heating and its implications on hot carrier reliability evaluations," 2015 *IEEE International Reliability Physics Symposium (IRPS), Monterey, CA, pp. 4A.4.1-4A.4.6, 2015.*

Table 2.2 defines thermal dependencies of common reliability mechanisms and their modulation strength for standard CMOS technologies. Strong modulation of PMOS negative bias temperature instability (NBTI) and intermediate modulation of PMOS hot carrier injection (HCI) can be associated with the choice of materials used for metal gate stack which differ from NMOS devices.

Table 2.2 Thermal Dependence of Reliability Mechanisms **[25]**

Mode	Thermal Dependence	Modulation Strength
PMOS Negative Bias Temperature Instability	• Direct	• Strong (high Arrhenius activation)
NMOS Positive Bias Temperature Instability	• Direct	• Weak (small Arrhenius activation)
NMOS Hot Carrier Injection	• Thin and thick oxides = mixed results	• Very weak (negligible Arrhenius activation)
PMOS Hot Carrier Injection	• Thin oxides = direct • Thick oxides = mixed results	• Intermediate (medium Arrhenius activation)
Gate Integrity	• Direct • Local vs. global impacts need to be comprehended	• Strong (high Arrhenius activation) for both NMOS and PMOS

While faster degradation at elevated constant voltage stress conditions is expected due to self-heating in FinFETs than planar transistor structures, bias temperature instability (BTI) reliability mechanism is expected to show higher thermal-recovery effects [11] in drain saturation current as shown in Figure 2.9a. This could be further confirmed by same devices showing no difference in V_T recovery because of low sensing power condition used as shown in Figure 2.9b. Recovery is beneficial to the device reliability; however the permanent degradation component of BTI determines device life time, which can be accelerated by self-heating of the neighboring transistors.



(a) (b)

Figure 2.9 IdSat recovery ratio vs. delay time; higher Idsat for lower channel length and threshold voltage exhibits more recovery due to higher temperature induced by self-heating effect (a). Since V_T does not raise high temperature due to self-heating effect, degradation can be fairly compared without any disturbance (b).
Source: S. E. Liu, J. S. Wang, Y. R. Lu, D. S. Huang, C. F. Huang, W. H. Hsieh, J. H. Lee, Y. S. Tsai, J. R. Shih, Y.-H. Lee and K. Wu, "Self-heating effect in FinFETs and its impact on devices reliability characterization," IEEE International Reliability Physics Symposium (IRPS), Waikoloa, HI, pp. 4A.4.1-4A.4.4, 2014.

Based on findings reported in [11], it's recommended to use short relaxation times in stress testing while measuring drain saturation current (IdSat) in order to mitigate self-heating enhanced recovery effects in FinFETs. Alternatively, V_{Tlin} shift from BTI constant voltage stress can be used as a degradation parameter to avoid self-heating effects [11] as the transistor channel does not conduct significant current during sense times. Recommended BTI relaxation time is 1-10µs based on an IdSat degradation results shown in Figure 2.10a, where FinFET and planar devices were compared. These recovery effects remain a subject of debate in the community, and no consensus has been reached concerning the matter. Thus, further investigation is needed to address this issue. Figure 2.10a shows that FinFET degrades less because more recovery takes place with longer relaxation and self-heating effect present. However, at sense time of 1µs, it's showing to have matched degradation results with that of a planar device [11]. Similarly Figure

2.10b proves that shorter relaxation time (1μs) changes the slope value only by 3.5% during stress, where with 1 second relaxation time, slope changes by 20%.

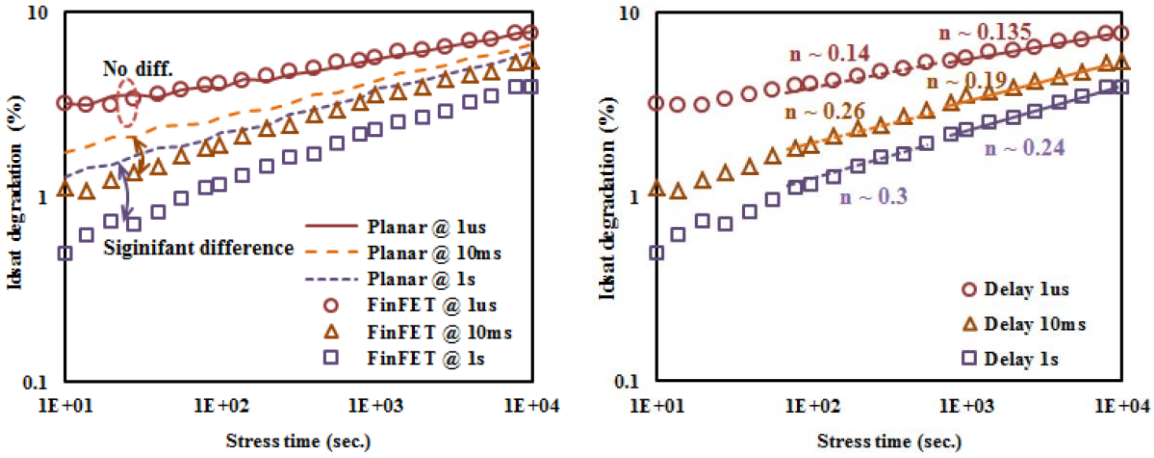
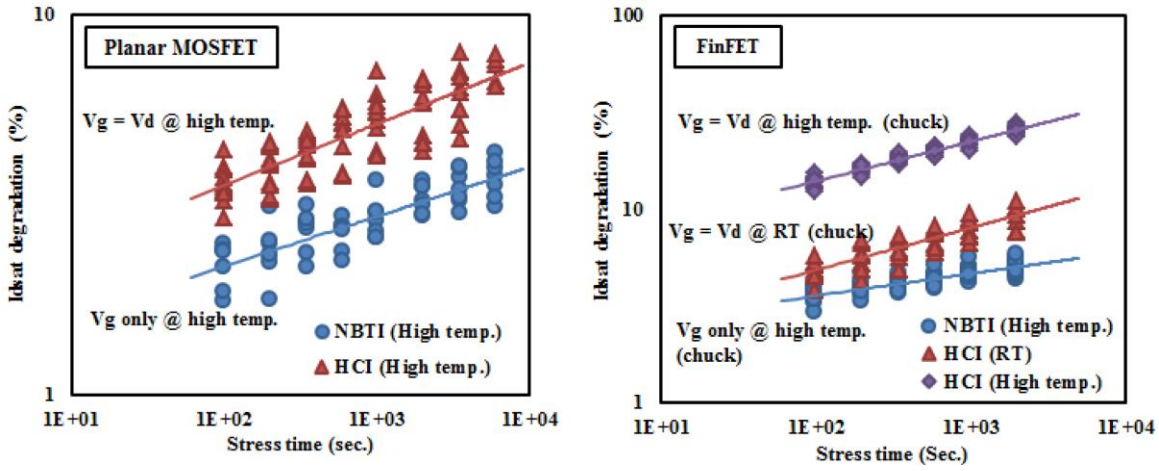


Figure 2.10 Planar/FinFET Idsat degradation vs. stress time at different measurement delay (a). Degradation slope is affected by self-heating effect (b).
Source: S. E. Liu, J. S. Wang, Y. R. Lu, D. S. Huang, C. F. Huang, W. H. Hsieh, J. H. Lee, Y. S. Tsai, J. R. Shih, Y.-H. Lee and K. Wu, "Self-heating effect in FinFETs and its impact on devices reliability characterization," IEEE International Reliability Physics Symposium (IRPS), Waikoloa, HI, pp. 4A.4.1-4A.4.4, 2014.

In hot carrier injection (HCI) constant voltage stress test, self-heating effect has a significant impact on device degradation. Some reports predict that self-heating effect leads to worse HCI degradation in FinFETs than in planar devices due to extra BTI effect under higher temperature [11]. This can be observed in Figure 2.11 when compared to planar HCI degradation at high temperature (Figure 2.11a), FinFET is showing similar results tested at room temperature due additional BTI degradation activated by self-heating (Figure 2.11b). However, these claims remain controversial; as the same devices show increased BTI recovery and increased BTI degradation. Therefore, quantification of both effects remains unclear.



(a) (b)

Figure 2.11 Planar (a) and FinFET (b) devices PHCI & NBTI degradation vs. stress time. NBTI takes significant part in HCI degradation which is shown in planar devices. FinFET HCI stressed at room temperature suffers high temperature NBTI effect due to self-heating effect.

Source: S. E. Liu, J. S. Wang, Y. R. Lu, D. S. Huang, C. F. Huang, W. H. Hsieh, J. H. Lee, Y. S. Tsai, J. R. Shih, Y.-H. Lee and K. Wu, "Self-heating effect in FinFETs and its impact on devices reliability characterization," IEEE International Reliability Physics Symposium (IRPS), Waikoloa, HI, pp. 4A.4.1-4A.4.4, 2014.

Temperature rise due to self-heating effect can lead to underestimation of life-time predictions if unaccounted for. To correct for self-heating effect work presented in [11] has corrected for the HCI stress time using equation 2.1.

$$t_{eff} = te^{\frac{E_a}{k_B(T_{amb}+T_{op})}-\frac{E_a}{k_B(T_{amb}+R_{TH}I_dV_d)}} \quad (2.1)$$

Where t is the stress time, t_{eff} is the effective time, k_B is Boltzmann constant, E_a is the activation energy, T_{amb} is the ambient temperature, T_{op} is the temperature in the normal operation, and $R_{TH}I_dV_d$ is the temperature rise due to self-heating effect during DC stress. While this model provides an attempt to account for self-heating effect in HCI, it is still

to be calibrated by actual self-heating data that has been validated at circuit level (e.g., ring oscillator) where the nature of the signal is in switching mode.

2.5 Summary

The current state of the art research the field of self-heating and its impact on reliability was presented in this chapter. The findings ultimately shaped the goal of this dissertation which is outlined in Chapter 1. The FinFET device which is studied in this dissertation was clearly shown in this chapter to have increased self-heating effects due to phonon boundary scattering. To measure temperature rise due to power dissipated in the devices many sensor parameters were presented of which linear currents and device metal resistance are adapted for the rest of this dissertation because of their measurability and proximity benefits, respectively. Studies on CMOS device reliability have shown the need in accounting for self-heating for proper EOL projections. Methods on correction were presented, however the techniques are time consuming and may not be suitable for foundry businesses where many wafers are ramped through the manufacturing line. The findings in the chapter will be used to further improve the sensor devices and reliability assessments as presented in the next chapters.

CHAPTER 3

SELF-HEATING MEASUREMENT METHODOLOGIES

This chapter describes three different measurement methodologies for the electrical characterization of FinFET self-heating at wafer-level. The different sensor types designed are the threshold voltage (V_T) of an adjacent FET, the forward bias (V_D) of an adjacent pn-junction or the gate resistance (R_G) of the device itself. This chapter will report that self-heating is underestimated by 35% when sensed at the adjacent device. This chapter also confirms that heat from local and surrounding sources are additive. While methods to measure self-heating have been developed and discussed [10, 13], little attention is paid to measurement errors which are important when small temperature changes need to be resolved. This chapter will address the measurement errors and present a verification of the sensor's stability through temperature cycling. Finite element simulations of heat transport are used to interpret heater-sensor temperature gradients, which will validate the measurements and provide further insight to the temperature difference between sensor and heater structures. Finally, last section in this chapter compares the level of self-heating between bulk FinFET and SOI FinFET technologies.

3.1 Introduction

Thin body silicon FET devices such as bulk/SOI FinFET are used in large volume CMOS manufacturing. Power dissipation in these geometrically confined structures is challenging. Consequently local self-heating can potentially affect device performance and exacerbate the effects of some reliability mechanisms [10, 11, 12, 33]. In general, it was reported that self-heating in core devices of advanced technology nodes, increases

the hot-carrier (HC) degradation during stress because of the increased temperature at high stress currents [12]. Additionally, it was reported in [11] that NBTI recovery is accelerated when using the saturation drain current degradation as metric for comparison due to increased temperature during BTI sense readout which accelerated the de-trapping. In [33], it was shown that SH due to non-uniform TDDB stressing reduces the lifetime significantly. For emerging devices with high-mobility materials such as Ge, self-heating can increase by more than 100% [34]. Therefore, the quantification of self-heating is crucial for continued technology scaling. While the effects of self-heating represent an active field of research [35, 36, 37, 38, 39] in the semiconductor community, the techniques of self-heating measurement are rarely discussed [10] in detail. In addition, a single electrical sense element is extremely limited by its proximity and effectiveness. This chapter presents several experimental methodologies to quantify self-heating using wafer level measurements. These measurements are also validated through TCAD predictive thermal simulations and correction factor is established for all the sensor types studied.

3.2 Sensor Layout Design

In order to characterize self-heating in bulk-FinFET devices, three types of sensors were designed in this dissertation. In type I, the sensor is a FET device surrounded by several heater FETs in the same active area (RX) (Figure 3.1a & Figure 3.2a).

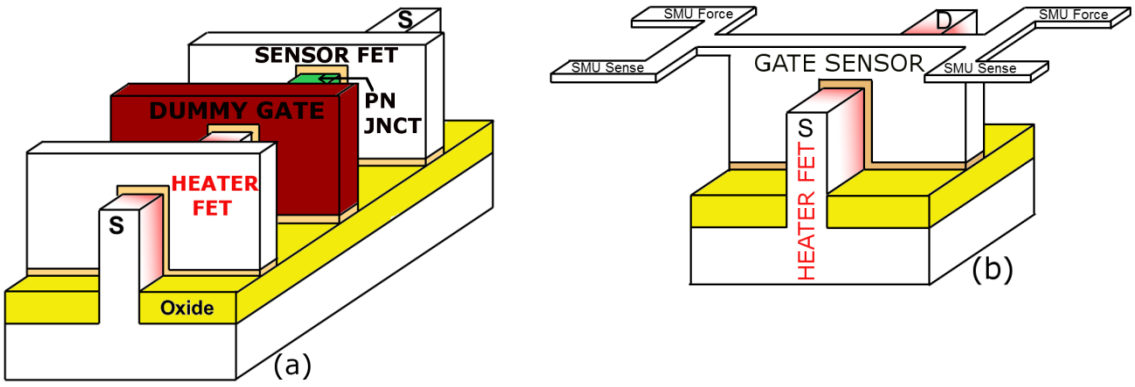


Figure 3.1 Illustrative figure showing the different heat sensing schemes: a) adjacent heat sensing using the electrical characteristic of a FET sensor device and PN-junction diode sensor b) local heat sensing using a 4-terminal kelvin contact to measure the thermal coefficient of resistance.

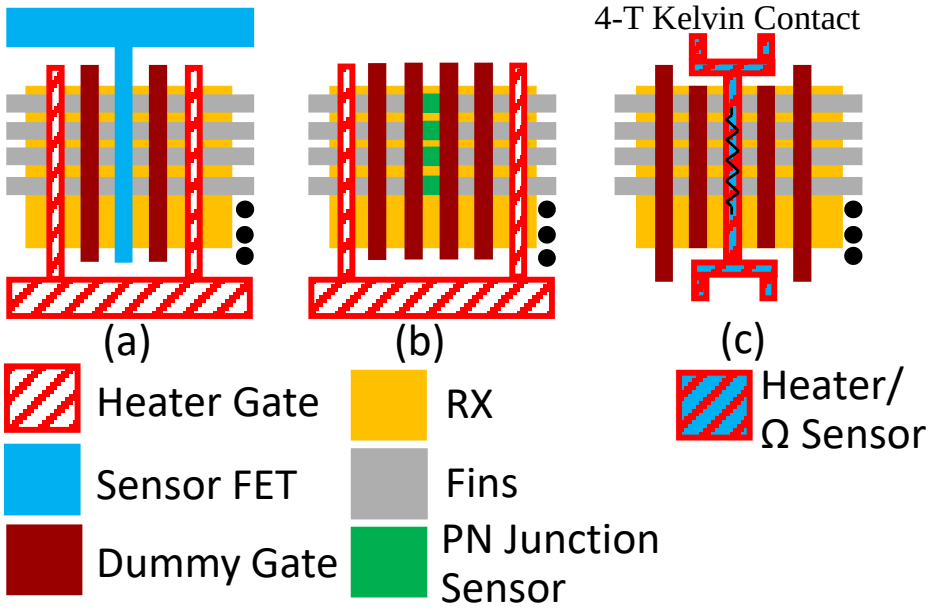


Figure 3.2 Illustrative figure showing the layout design of each sensor type a) Type I: V_{Tlin} sensor, b) Type II: PN-junction sensor, c) Type III: R_G sensor.

In this configuration, V_{Tlin} of the sensor FET is used to track the temperature change in the area surrounding the device. Similarly, type II sensor is a pn-junction diode surrounded by heater FETs (Figure 3.1a & Figure 3.2b). The forward bias (V_D) of the pn-junction is used to track the temperature change. The sensing condition (sensor) is set to

be in low conduction (1-2μA) in order to avoid any heat contribution from the sensors themselves. In addition, grounded dummy gates isolate the sensor from the heater, minimizing the impact of parasitic leakage on the sensing results. As power dissipates in the heater FETs, the surrounding temperature is increased, which is captured by the electrical response of the sensors (V_T or V_D respectively). Because of their design simplicity, type I and II thermo-sensors can easily be embedded near dense circuitry. However, the heat loss in the surrounding space should be accounted for before projecting the actual temperature of the heating device. This will be addressed in section 3.6.

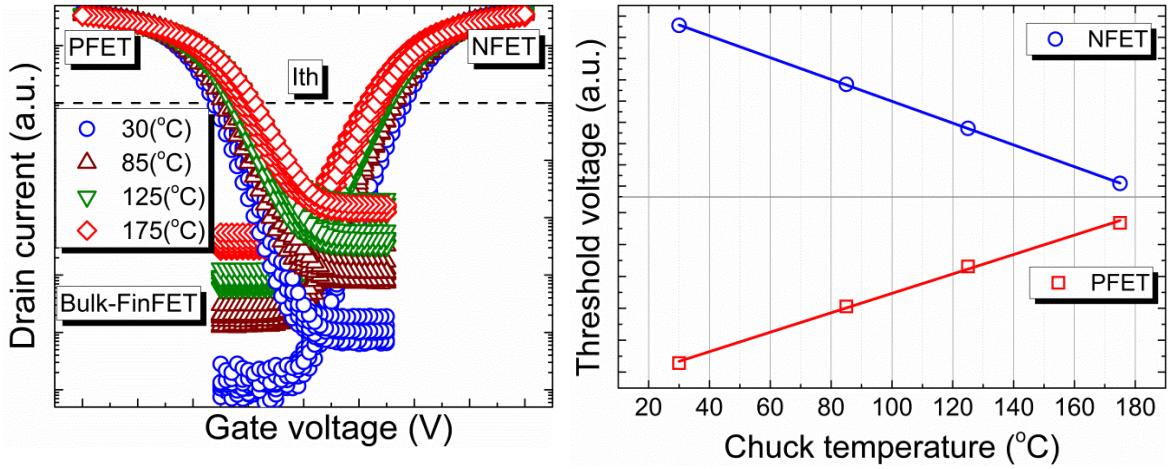
Sensor type III uses the gate resistance (R_G) temperature sensitivity to measure the temperature of the heating FET itself (Figure 3.1b & Figure 3.2c). In this configuration, the metal gate is designed to be a 4-terminal Kelvin contact which allows the direct measurement of R_G at the gate while the FET is being biased at the same time. Type III can be used in three configurations: 1) to sense the heat locally from the device itself, 2) to sense the heat dissipated in the neighboring devices, 3) a combination of both. Naturally, type III quantifies best the local self-heating since it is measured at the device gate. However, the implementation of such device near dense circuitry is not always trivial. Table 3.1 summarizes the three sensors designed which are used to measure self-heating effects in this dissertation.

Table 3.1 Sensing Methodologies

Sensor Type	Heater	Sensor	Thermal Metric	Sense Location
I. (Figure 3.2a)	FinFET	FinFET	V_T	Adjacent FET
II. (Figure 3.2b)	FinFET	P/N junction diode	V_D forward bias	Adjacent FET
III. (Figure 3.2c)	FinFET	Gate Metal	R_G Gate Resistance	Local FET

3.3 Self-Heating Measurement Procedure and Results

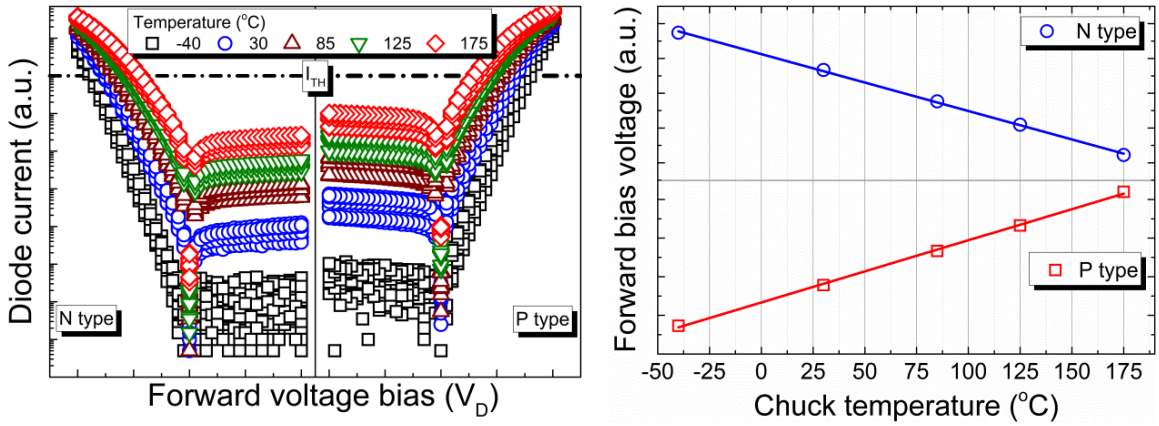
To extract the temperature change, all three methodologies follow a similar procedure. First, while the heater FETs are OFF, the thermally sensitive metric of each sensor is measured at four different chuck temperatures ranging between 30 to 175°C. This step serves as the calibration of the sensor. The linear current levels of the type I sensor increase with higher temperatures (Figure 3.3a), thus the threshold voltage decreases with temperature as shown in Figure 3.3b, which is in agreement with literature [40].



(a) (b)

Figure 3.3 I-V characteristics of the Type I FinFET sensor at different chuck temperatures showing VT thermal sensitivity (a) Type I: V_{Tlin} sensor, threshold voltage (VTlin) sensitivity to temperature change for NFET and PFET devices (b).

The forward diode current *I* of PN-junction (3.1) increases at higher temperatures, therefore decrease in forward bias V_D is observed as depicted in Figure 3.4a and Figure 3.4b.



(a) (b)

Figure 3.4 I-V characteristics of the Type II pn-junction sensor at different chuck temperatures showing its thermal sensitivity (a) and forward bias (V_D) sensitivity to temperature change for n-p and p-n diode (b).

This occurs mainly due to increase in saturation current I_0, which increases as intrinsic carrier concentration (n_i) increases with temperature as shown in (3.1)

$$I = I_0\left(e^{\left(\frac{qV_D}{k_BT}\right)} - 1\right), \qquad I_0 = qA\left(\frac{D_N n_i^2}{L_N N_A} + \frac{D_P n_i^2}{L_P N_D}\right) \tag{3.1}$$

where q is the electronic charge, k_B is the Boltzmann's constant, T is the temperature, $D_{n,p}$ are electron and hole minority carrier diffusion constants, $L_{n,p}$ are diffusion lengths for the minority carriers. Although the reverse bias leakage has a better sensitivity, at very low temperatures, the leakage is extremely small and is masked under the noise level. Thus, forward bias current was chosen to cover the widest range of temperatures (-40 to 175°C). Note that the sensing current for type I and II are set to be low (1-2µA) to avoid the heating of the actual sensor. Thus for example in type I sensor, V_{Tlin} is extracted with the constant current method [$V_{Tlin}=V_{gs}$ at I_{ds}=1-2µA (V_{ds}=50mV)]. Finally, the gate metal resistance is also sensitive to temperature as shown by its linear response

in Figure 3.5.

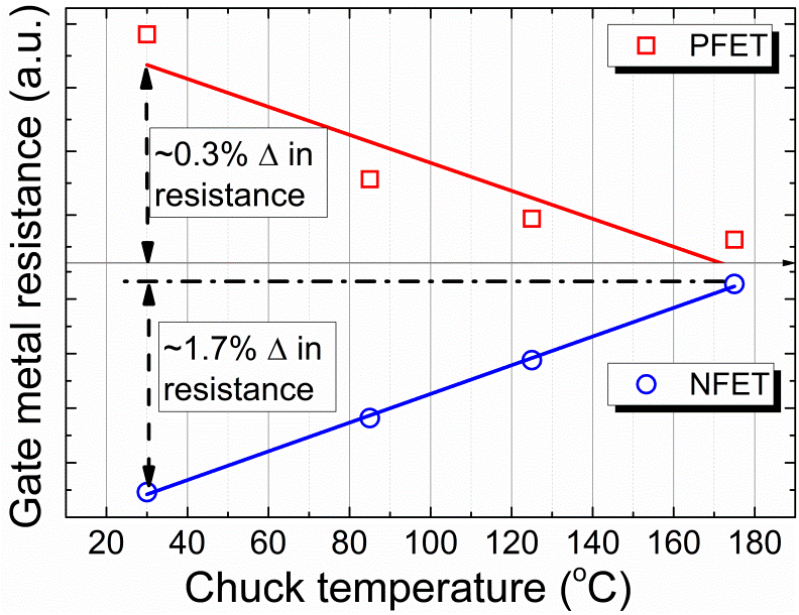


Figure 3.5 Gate resistance (R_G) sensitivity to temperature change showing the temperature coefficient of resistance (TCR) for NFET and PFET sensors.

In this first step, the temperature coefficients of V_T (Figure 3.3b), V_D (Figure 3.4b) and R_G (Figure 3.5) are determined by plotting the median of their distributions across the wafer in response to chuck temperature change. Next, at a constant chuck temperature, the metrics are re-measured while the heater FETs are biased in saturation (V_g=V_d) at several different power conditions as shown in Figure 3.6. This step determines each metric's sensitivity to power. Finally, the sensor metric response Δ, due to power dissipation in heaters is translated into a temperature change using the coefficient a from the first step (calibration). This can be visualized by analyzing the expression in Equation (3.2). The result is the correlation of temperature change (ΔT) to dissipated power per fin. The measurement itself, which is simply a current-voltage (I-V) sweep, can be performed in an auto-range mode, which has long integration time, but more accurate results can be

achieved. This measurement takes place at the same time as constant power is supplied to the heater transistors. The longer time for the measurement (auto-range mode) does not compromise any information loss, as the goal is to measure steady state temperature.

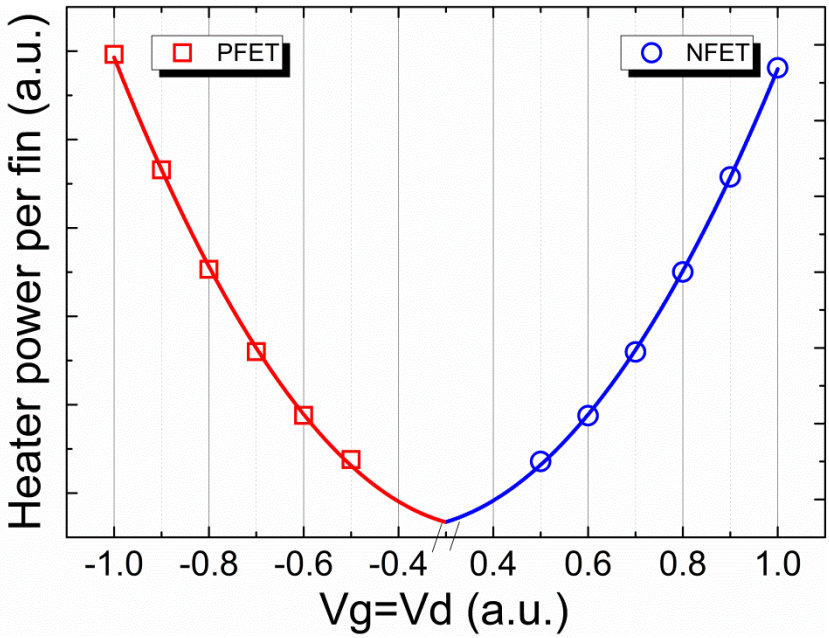


Figure 3.6 Heating conditions used in logic PFET/NFET structures. Functional dependence up to V_g=V_d=±1V can be described by Power = A·x·(x±Δ) with Δ being the device threshold.

The arithmetic work which calculates ΔT based on the change of the thermally sensitive parameters (V_T, V_D and R_G) due to different power dissipations in the heater transistor channel is represented in Equation (3.2), which contains all three temperature sensors as the same method applies to all.

$$[V_{T1}, V_{D1}, R_{G1} = aT_1 + b] - [V_{T2}, V_{D2}, R_{G2} = aT_2 + b] = \frac{[V_{T1}, V_{D1}, R_{G1} - V_{T2}, V_{D2}, R_{G2}]}{a} =$$

$$= \frac{[\Delta V_T, \Delta V_D, \Delta R_G]}{a} = (T_1 - T_2) = \Delta T \qquad (3.2)$$

In Equation (3.2) the coefficient a is the slope of the calibration shown in Figures 3.3-3.5.

3.3.1 Self-Heating Measurement Results

Self-heating of 5 and 20-fin logic devices (NFET and PFET) were measured using the three mentioned methodologies. Figures 3.3b, 3.4b and 3.5 show the temperature coefficients for each metric measured in the calibration step.

After calibration, the heater devices are turned ON and measurements of self-heating are made on the respective sensors (I-III) as shown in Figure 3.2. Note that the temperature change is based on differential method for each site to reduce the effect of variability across the wafer on the ΔT distribution. Through a rigorous study [41] explained in Section 3.4 it was shown that the error bars associated with power to temperature conversion are within ±0.5°C. Measurement results of self-heating are shown in Figure 3.7 for all sensor types and they are generally in quantitative agreement. The excellent agreement proves that any of the three sensor types can be used for self-heating evaluations depending on circuit application. The only notable difference is the active gate R_G configuration (sensor III) which is significantly higher as it resides closer to the hotspot and more efficient in capturing the average channel self-heating contribution from the 20-fin device itself (Figure 3.7). Comparing the adjacent self-heating results between NFET and PFET in Figure 3.7, higher self-heating can be observed in the PFET. The reason for higher self-heating in PFET devices can be associated with its alloy disorder at the source/drain regions due to SiGe, which creates a lattice mismatch and exhibits poor thermal conductivity [42].

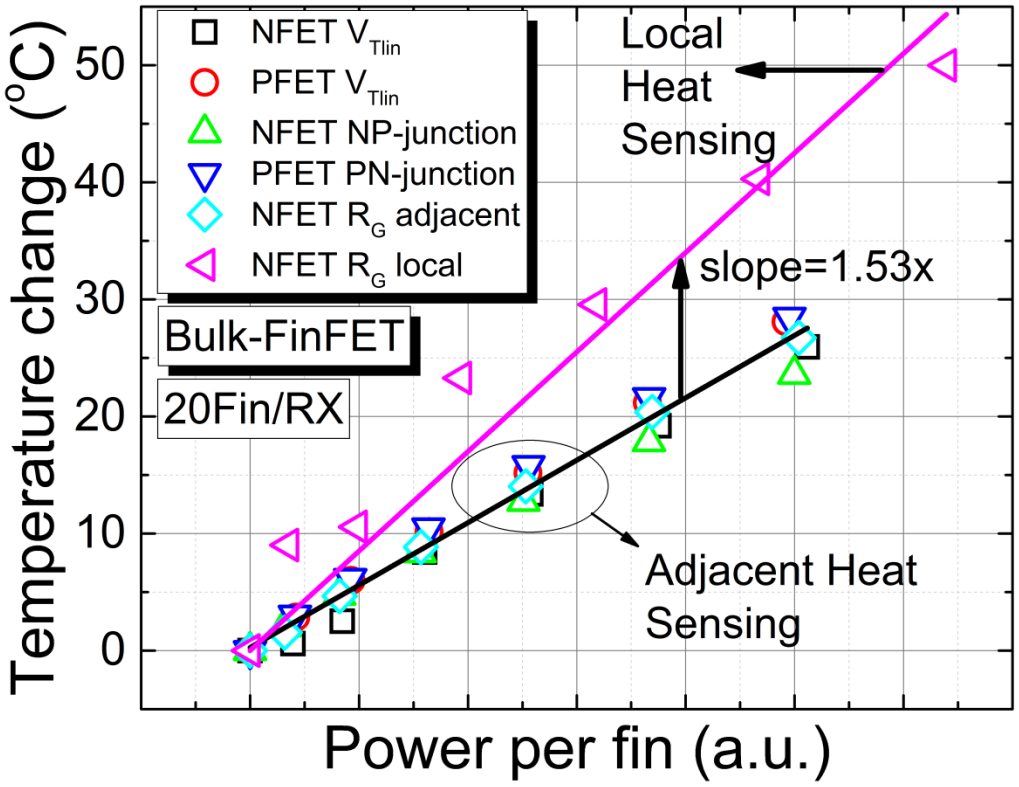


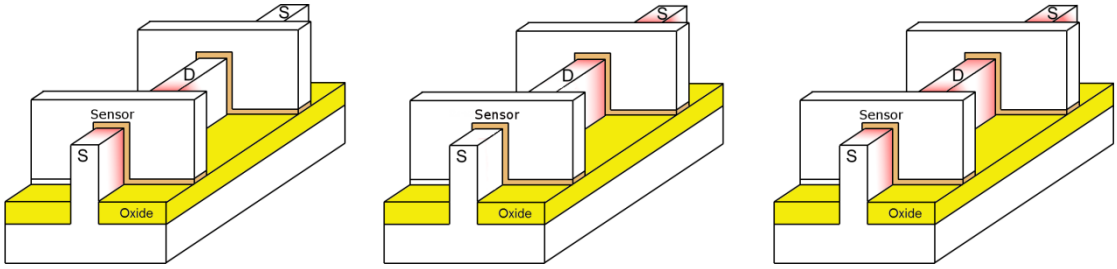
Figure 3.7 Self-heating characterization compared using three different sensing methodologies. Local sensing R_{TH} is ~ 1.5X higher than adjacent heat sensing.

Comparing the SH characteristics from different methodologies, it is shown that surrounding heat measurement underestimates the local (actual) device heat by ~35%. It therefore becomes critical to resolve the temperature decay in the principal directions when projecting device temperatures.

3.3.2 Additivity of Heat

Additivity of heat can often cause local hot-spots from neighboring components dissipating power thus aggravating their reliability and performance. This sub-section is devoted to a measurement confirmation that heat is additive. Type III sensor (R_G) can be used in two additional configurations: 1) for local self-heating, the device itself is turned ON while the adjacent FETs are OFF. 2) The combination of local and surrounding heat

is sensed by biasing both the sensor and the adjacent heater FETs simultaneously which allows us to study the additivity of generated heat in FinFETs as illustrated by the test cases in Figure 3.8.



(a) (b) (c)

Figure 3.8 Local (a), adjacent (b) and local & adjacent (c) self-heating measurement scenarios.

It is expected that the heat transfer is additive ($\Delta T_{TOT} = \Delta T_{local} + \Delta T_{adjacent}$). To prove this, in the first step, temperature change (ΔT_{local}) is measured via sensor type III, which tracks the gate resistance while heat is dissipated only in the channel beneath it (Figure 3.9 square) when the sensor device is ON. In the second step, the same sensor measures only heat generated in the adjacent heater devices ($\Delta T_{adjacent}$) as shown with circles in Figure 3.9. Lastly, the gate metal sensor, measures the heat while the local heater (below sensor) and the adjacent heater devices are dissipating power at the same time (ΔT_{TOT}), as depicted with triangles in Figure 3.9. It is important to mention that in the last step, the heater (sensor device) below the gate sensor dissipates a constant power throughout the actual measurement as the neighboring heaters increase in power dissipation. This is why ΔT_{TOT}, represented by triangles in Figure 3.9, is the result of heat from neighboring devices (Figure 3.9 circles) superimposed on the local heat at constant power (Figure 3.9 square), which confirms the heat is indeed additive.

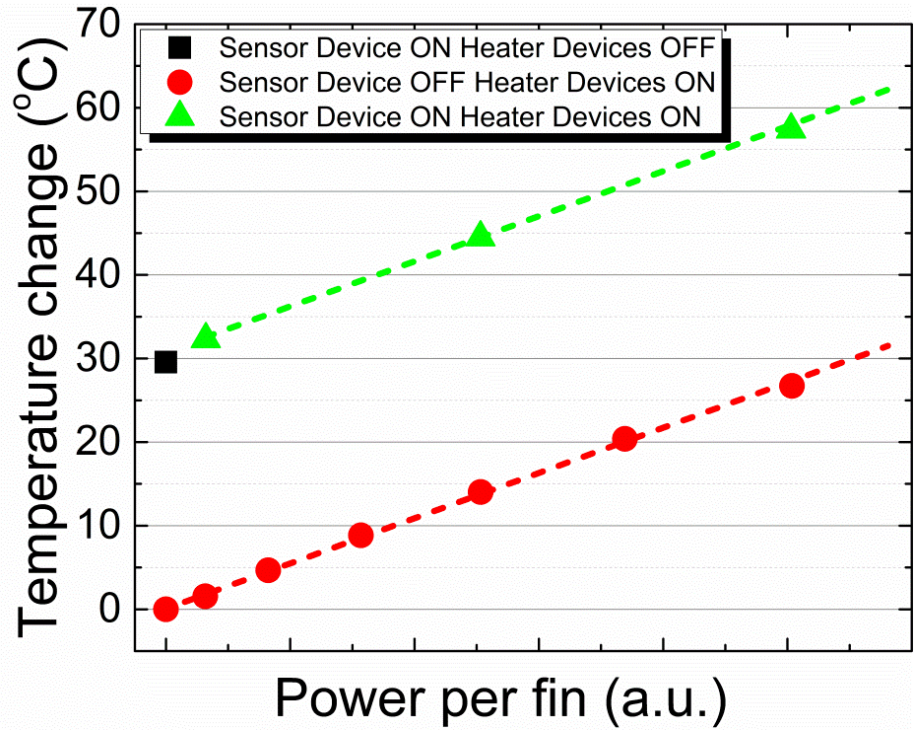


Figure 3.9 Characterization of heat sensing using sensor type III in three different configurations. By turning ON the sensor, the heater, or a combination of both, the heat from the two devices is additive.

3.4 Temperature Measurement Error

To assess the impact of stochastic process variation on the self-heating wafer level characterization, sensor error bar was established on the temperature measurement. The sensor chosen for this study was the pn junction, which uses the thermally sensitive forward voltage V_D as a sensing parameter. This was achieved via V_D variability study across 16 to 64 wafer die samples using statistical analysis to determine the upper and lower confidence bounds of the forward voltage change or corresponding temperature error. Figure 3.10 illustrates the pn junction forward bias voltage across 64 samples being normally distributed to the first order.

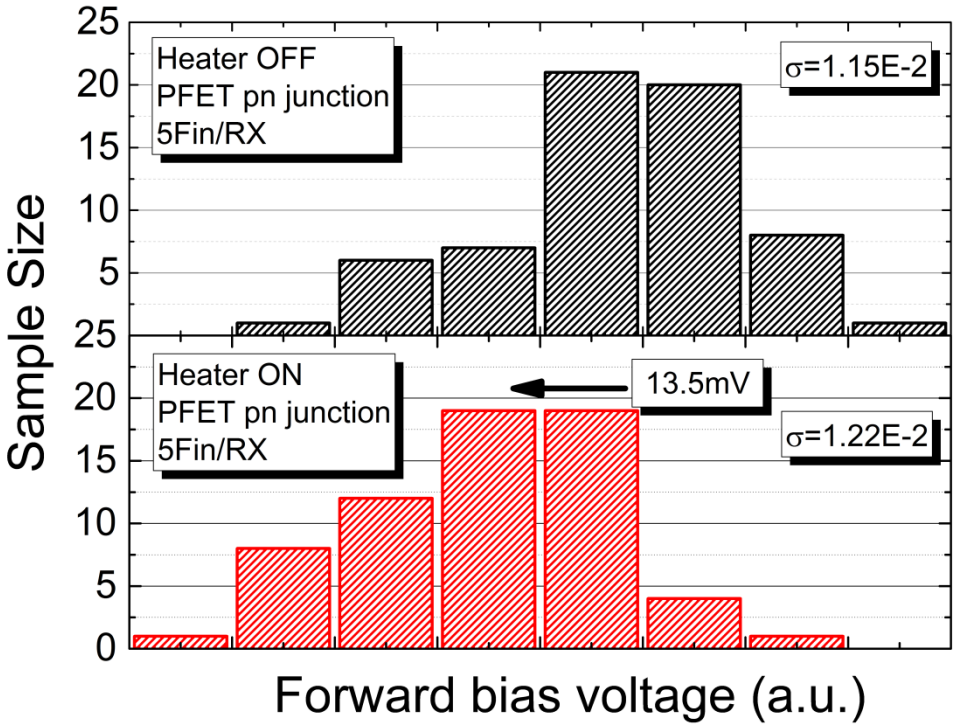


Figure 3.10 Normal distribution of pn junction forward bias voltage V_D, with heater OFF (upper) and ON (lower). Mean shift of V_D distribution at higher temperatures is observed.

Furthermore, the expected reduction of the mean forward bias voltage V_D is observed during self-heating. It should be noted that the standard deviation (σ) of the forward voltage is of similar magnitude as the self-heating induced forward voltage (upper and lower panels of Figure 3.10). To eliminate the sample process variation in the self-heating experiments the differential forward bias voltage ΔV_D (die-level V_D difference between heater ON and OFF from Figure 3.10) is calculated as shown in Figure 3.11. The mean value for the differential forward voltage ΔV_D in Figure 3.11 is consistent with the 13.5mV reduction shown in Figure 3.10. The standard deviation (σ) of the ΔV_D is greatly improved as the across wafer variation is removed. Thus, the differential calculation can greatly reduce the measurement error due to wafer process variation and provide more accurate temperature reading.

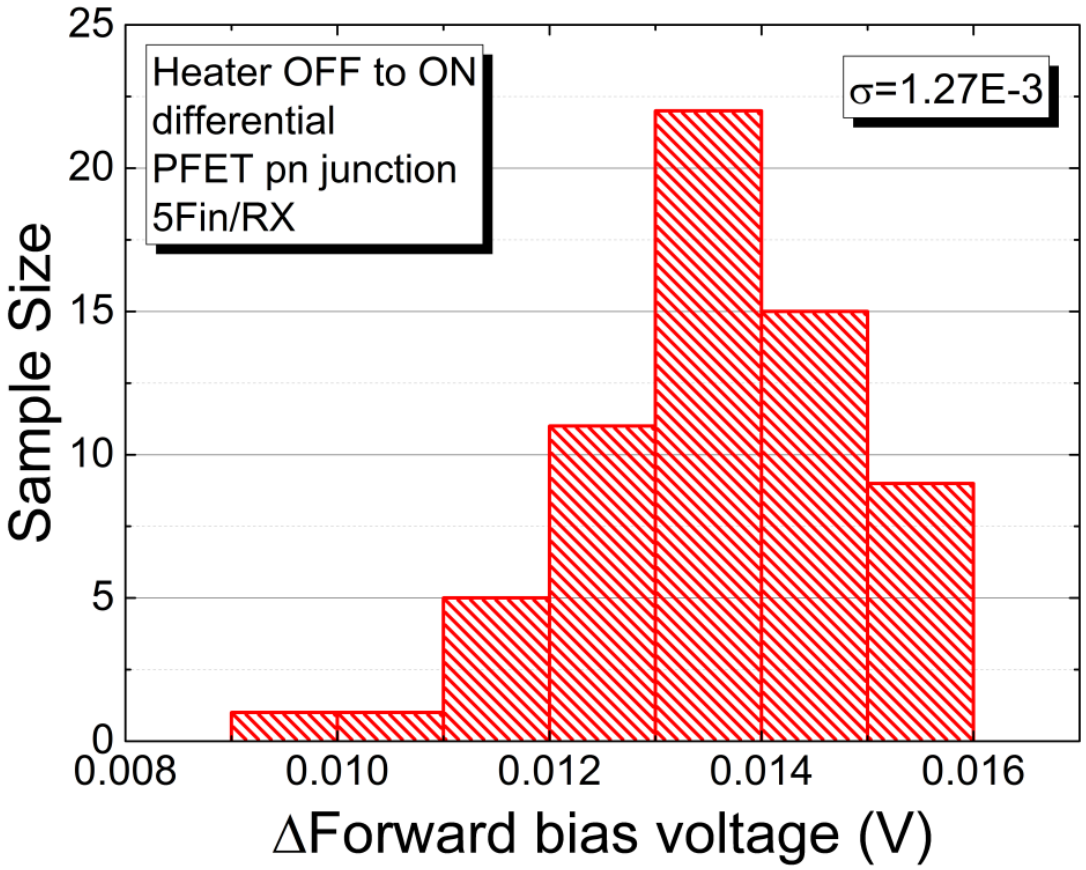


Figure 3.11 Normal distribution of pn junction differential forward bias voltage ΔV_D between heater ON and heater OFF.

By repeating the same exercise demonstrated in Figure 3.10, the same concept can be demonstrated by analyzing the probability plot of the pn junction forward voltage as shown in Figure 3.12, where a shift of the distributions is also observed due self-heating, this time with a distribution also showing a mid-power heater dissipation (heater partially ON). However, notable again in Figure 3.12, is the relatively high standard deviations of the measured pn junction forward voltage across the wafer at different power levels supplied to the adjacent heaters.

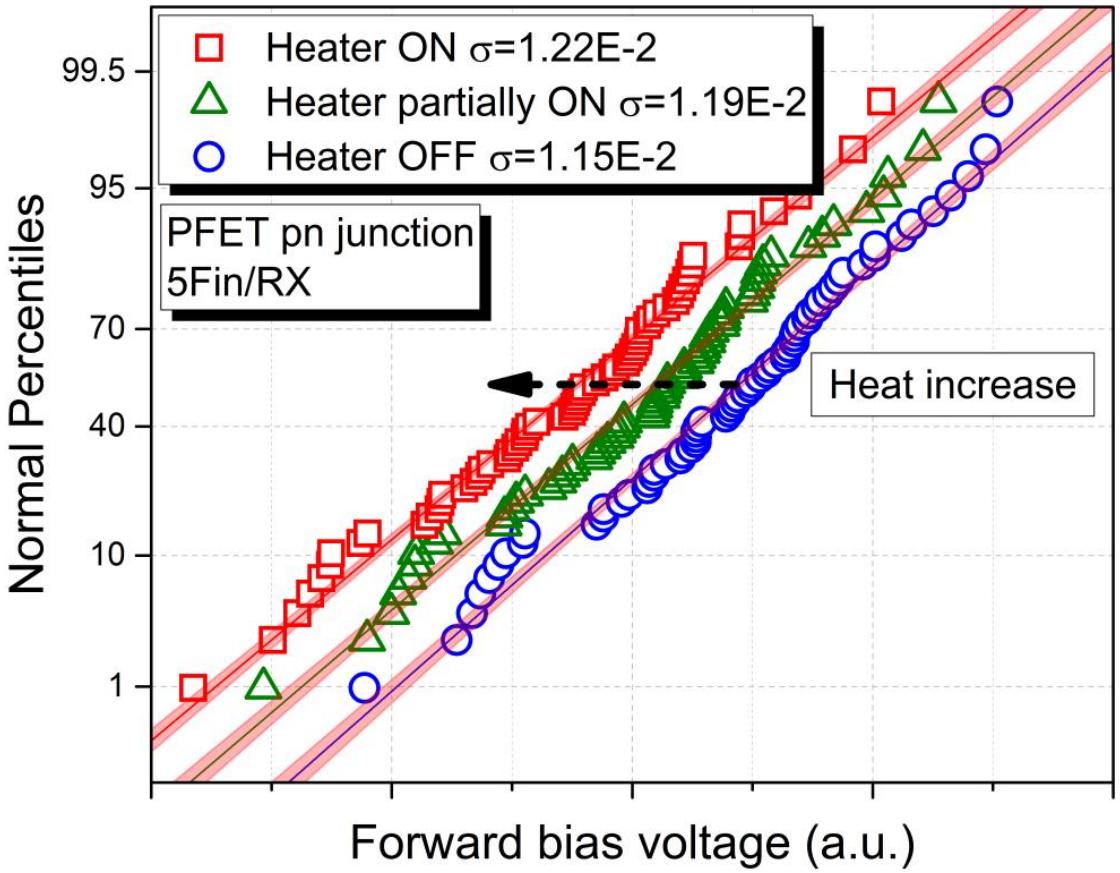


Figure 3.12 Probability plot for the forward bias voltage distribution at different heater power dissipations.

When plotting ΔV_D (Figure 3.13), calculated between the same wafer die samples of Figure 3.12, at different heater power dissipation levels, a reduction in standard deviation (σ) is clearly noticeable. This is again, due to the elimination of the across-wafer process variation by means of differential calculation, this time explained by probability plots. The differential method enables accurate temperature extraction as will be demonstrated next and for this reason, most self-heating measurements are plotted as ΔT vs power applied to heater structures. The question on what temperature error can be expected in wafer level self-heating measurements up to this point remains un-answered.

However, using standard deviations of V_D and ΔV_D just discussed, this will be answered next.

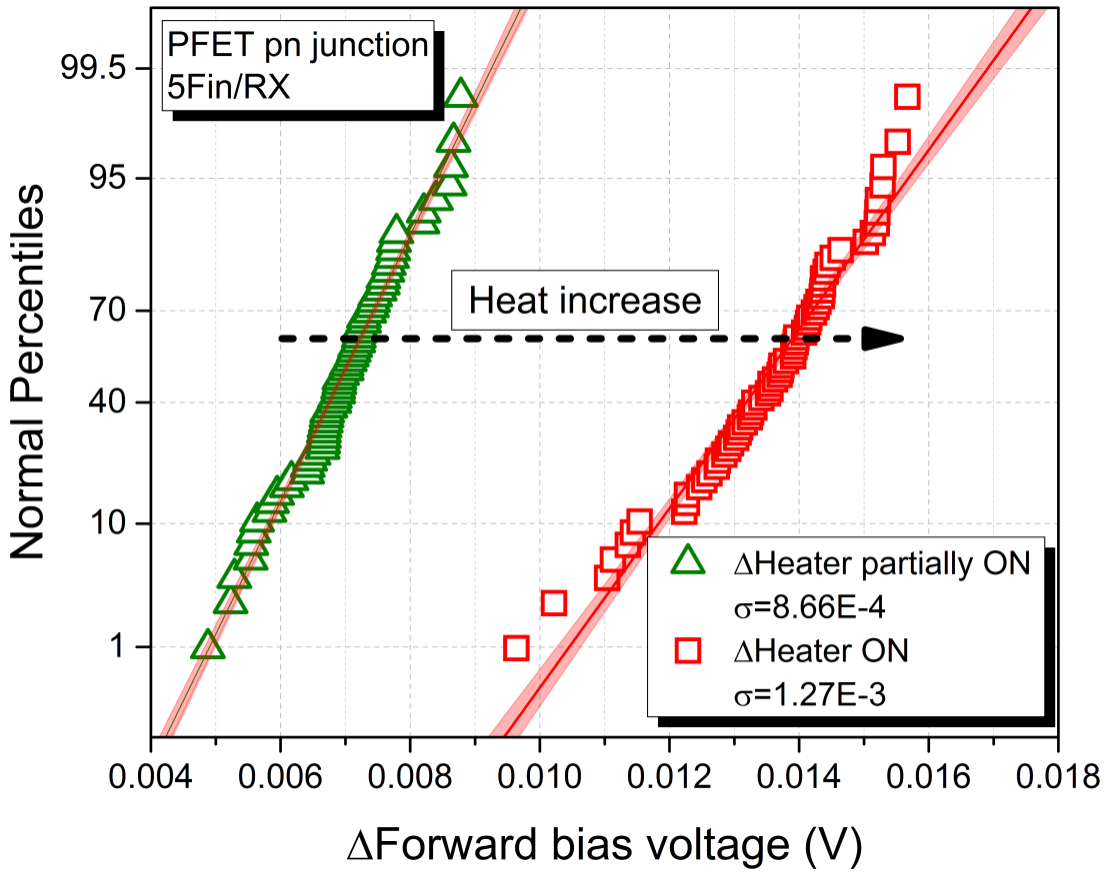


Figure 3.13 Probability plot of pn junction differential forward bias voltage ΔV_D between heater ON and heater OFF.

To finally evaluate the temperature error in our measurements, lower and upper 95% confidence limits (LCL, UCL) were extracted from Figures 3.12-3.13 for comparison, to illustrate the benefit of differential temperature extraction. Calculating the difference of LCL and UCL between the median forward voltage V_D and ΔV_D, then, translating the result into temperature via the temperature coefficient a from sensor calibration, the temperature error is estimated for different sample populations (16-64) as shown in Figure 3.14.

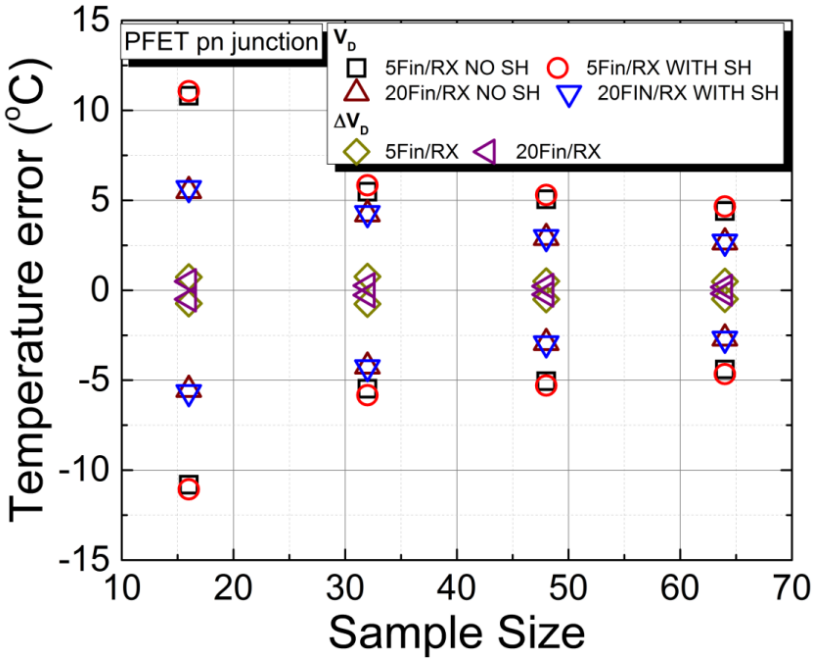


Figure 3.14 Temperature error based on pn junction forward bias voltage V_D and differential ΔV_D between heater ON and heater OFF for 5 & 20Fin/RX.

The high temperature error (±12°C for 5Fin/RX and ±6°C for 20Fin/RX) from forward voltage V_D, is due to high process variation, if compared to sensor's sensitivity. However, when extracting the self-heating induced temperature increase, based on the differential ΔV_D, the error is reduced to ~±0.5°C irrespective of fin per RX count. Figure 3.14 also demonstrates the benefit of increasing sample size of V_D and ΔV_D from 16 to 64 [43], which effectively reduces the temperature error by half. ΔT extraction via the differential method, which reduces the error to ~±0.5°C is expressed by Equation (3.3).

$$\Delta T = \frac{\sum_{i=1}^{N}\left(V_{D_{SH},i} - V_{D_{noSH},i}\right)}{N \cdot a} \tag{3.3}$$

Where in Equation (3.3), N is the sample size, i is the sample number, a is the temperature coefficient from sensor calibration and, $V_{D_{SH}}$/ $V_{D_{noSH}}$ are the forward bias voltage with self-heating and no self-heating, respectively.

3.5 Sensor Quality Verification

To verify sensor's ability to measure same temperature change repeatedly without distortion due to heat stress, an experiment was conducted using sensor type I (V_T sensor) in which the sensor parameter was re-measured in between chuck temperature cycles. The test scenario for this experiment, while modulating chuck temperature is illustrated in Figure 3.15.

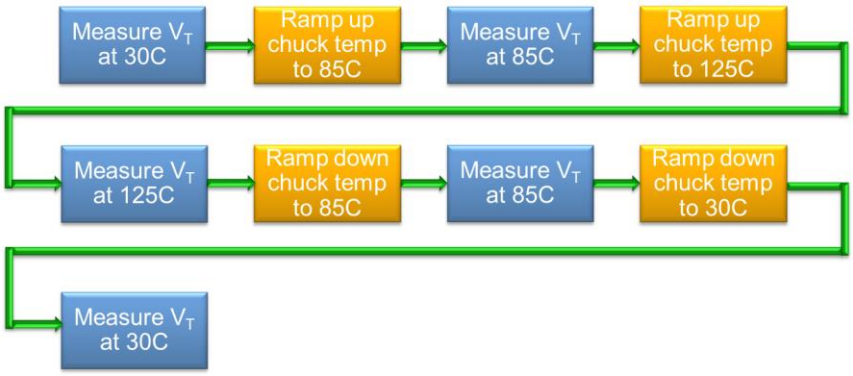


Figure 3.15 Test plan to verify sensor reliability and repeatability of measurements while modulating the chuck temperature.

The same test concept as in Figure 3.15 was conducted while modulating the heat in the adjacent and local to sensor heater structures, at a constant chuck temperature of 30°C as described in Figure 3.16.

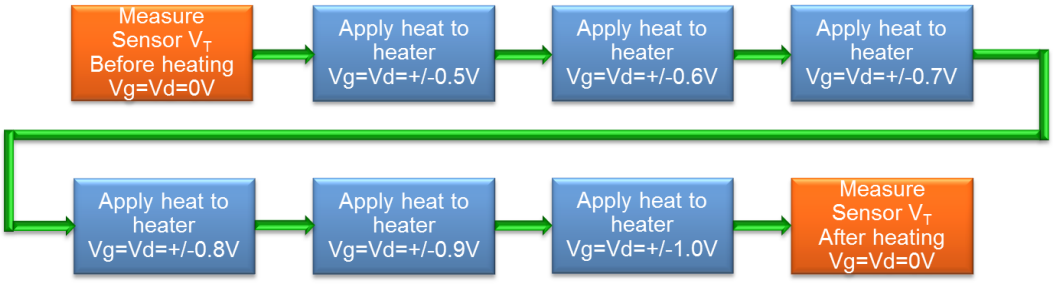
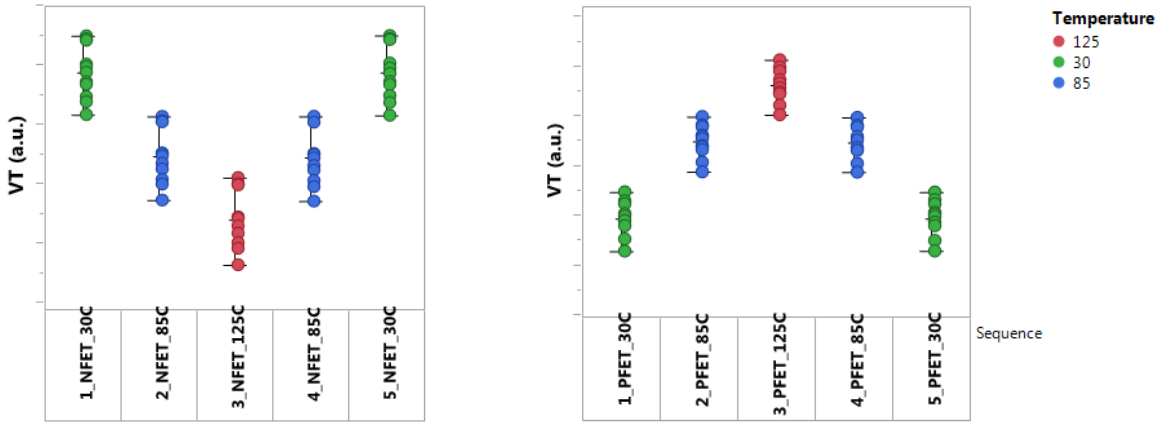


Figure 3.16 Test plan to verify sensor reliability and repeatability of measurements while modulating heat in the adjacent heater structures.

The results from test described in Figure 3.15 show that integrity of V_T is not compromised during the chuck thermal stress cycle as shown in Figure 3.17. This verification proves that chuck temperature modulation of V_T is reversible and does not affect the reliability of the sensor.



(a) (b)

Figure 3.17 Type I sensor,V_T measurement while modulating the chuck temperature NFET (a) and PFET (b)

The quality of the sensor devices is further supported by examining sensor's current characteristics at 30°C before and after applied chuck thermal stress cycle as illustrated in Figure 3.18. No hysteresis in the I-V characteristic is observed between before and after chuck temperature heating.

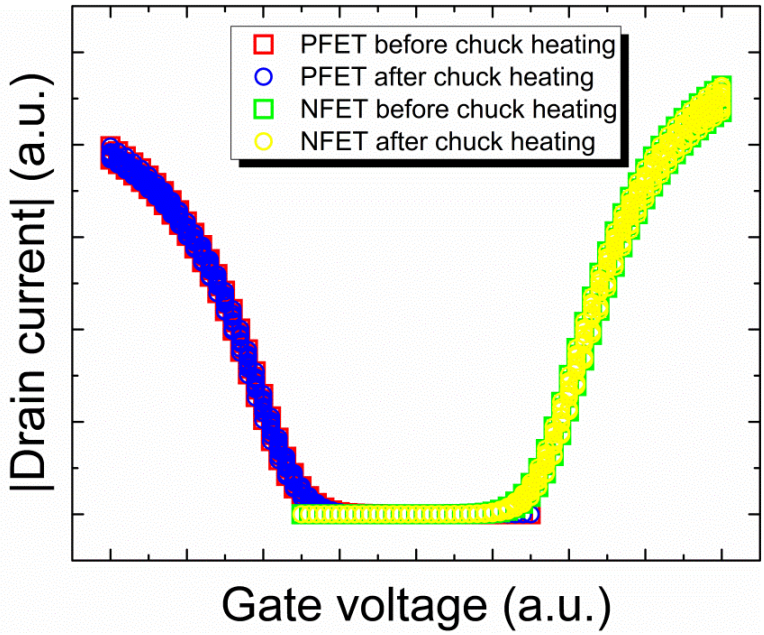
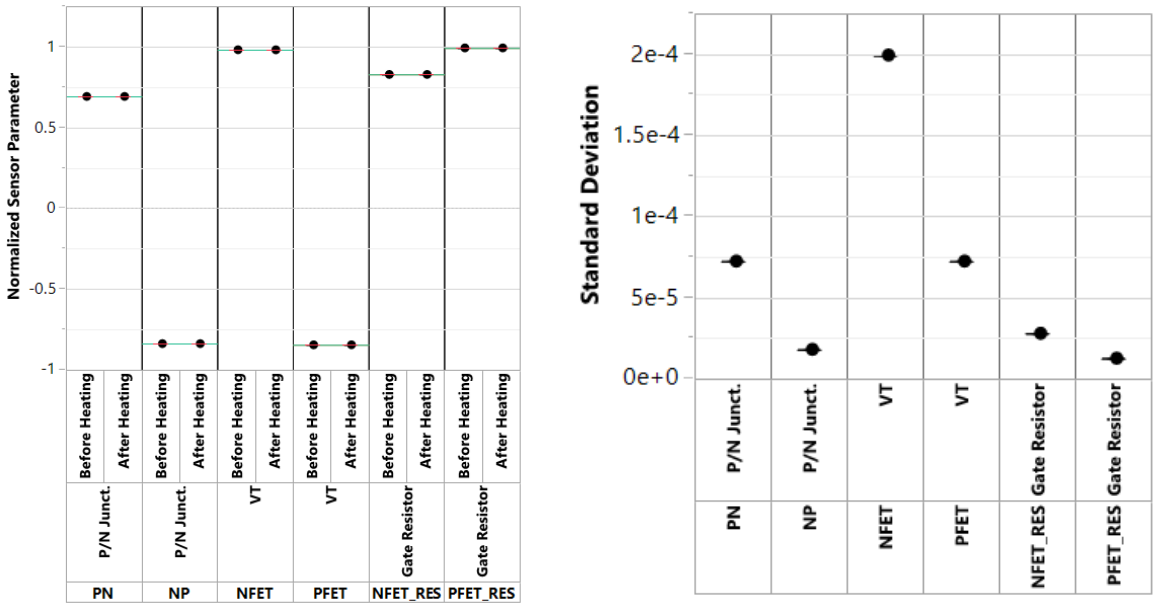


Figure 3.18 Hysteresis is not observed in the drain current characteristics of the sensor structure before and after modulation of the chuck temperature.

Lastly, using test flow described in Figure 3.16, all three sensors (Type I-III) were verified for sensing repeatability and quality while cycling the heat in the transistor heater structures. The results of Figure 3.19 prove the temperature sensors to be robust and reliable for self-heating measurements. Figure 3.19a shows the measurement of all three normalized sensor parameters (V_D, V_T, or R_G) before and after power (V_g=V_d > $V_{NOMINAL}$) is applied to the heater. No significant change in parameter values is observed. The standard deviations (Figure 3.19b) of all three sensor parameters are minimal and in fact, are significantly less than standard deviations reported in Figure 3.13, which suggests <<0.5°C error between temperature cycles can be expected. This is an important verification which allows the use of these sensor structures for further studies, which will be shared in this dissertation.



(a) (b)

Figure 3.19 No change observed in V_D,V_T, or R_G before and after heating the heater structure (a), also confirmed by low values of standard deviation of the thermal parameters from before and after heating (b).

3.6 Thermal Simulations

Finite element simulations of heat diffusion were performed on the test structures to physically model the temperature gradients and validate the physics of heat transport. The geometrical structure of the heater was modeled based on the respective bulk FinFET technology process assumptions. For simulations, an in-house (GLOBALFOUNDRIES, Inc.) device simulator FIELDAY was used. Heat source was modeled using a constant volumetric heat generation and a thermal-only simulation is performed on the large structures to keep the computational times tractable. The equivalent power density computed from electrical simulations is applied in the active fin regions and the steady-state heat flow Equation (3.4) is solved.

$$\nabla \cdot (k\nabla T) + \dot{q} = 0 \tag{3.4}$$

In Equation (3.4), k is the known thermal conductivity, $\dot{q}$ is the energy source term (power density) and T is the lattice temperature. Figure 3.20 schematically illustrates the heat transfer pathways in bulk FinFET technology for a high performance designs.

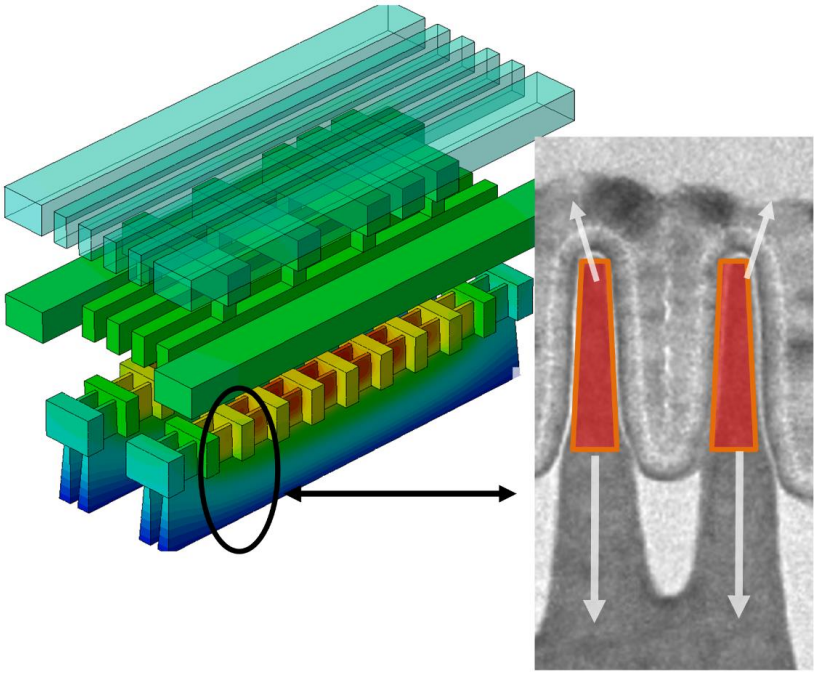


Figure 3.20 Schematic of heat transfer pathways in FinFET circuit.

Limited thermally conductive area through silicon fins, forces a significant portion of heat flow through the contacts and lower back-end, a mechanism well documented in SOI technologies [13, 44, 45]. In Bulk FinFET technology, large portion of the heat dissipates down into the bulk material. A key component of high fidelity thermal simulations is to accurately model the thermal properties of the front-end device and back-end interconnect stack. The properties are very sensitive to FET contacts and interconnect dimensions as well as the physical material interfaces. This has been a subject of notable studies in the previous decade [46, 28] and is extremely important to resolve when interpreting measurements in ultra-scaled FinFET technologies.

The predictive simulation methodology starts with a combination of process specific electrical properties, *ab-initio* phonon scattering and electron transmission computations to obtain thermal conductivity of various materials [47]. *Ab-initio* methods are used to accurately calculate phonon frequencies, velocities, mean free paths, and phonon-phonon scattering rates [48]. The impact of phonon boundary scattering on silicon thermal conductivity is taken into account by considering an additional term in the effective relaxation time using Matthiessen's rule. A Fuchs-Sondheimer model for thin films was used to obtain the boundary scattering rate [47]. These are fed into large scale finite element simulations with high fidelity structural resolution developed directly from design layouts. The simulations are applied to predict thermal resistance in bulk and SOI FinFETs (across a range of layout types).

Except for optical measurements, DC self-heating data is always affected by the proximity of the sensor to the hotspot [35, 36, 37, 38, 39], an effect which changes strongly with technology scaling and the measurement methodology. This discussion has been limited in existing studies. A key contribution of the thermal TCAD simulation is to resolve the temperature gradients that arise between transistor hotspot and the sensor location through simulations and several measurements. Both 5 and 20 Fins per active region (RX) were simulated. Figure 3.21 illustrates the physical 3-D layout of the 5 Fin NFET structure demonstrating the thermal contours and the location for all three sensors (Type I-III) in relation to the hot-spots (heaters), which will be reflected in the simulated results. The heater-sensor configuration is shown in Figure 3.21 represents a half-density active FET to provide heater-to-sensor isolation discussed in section 3.2.

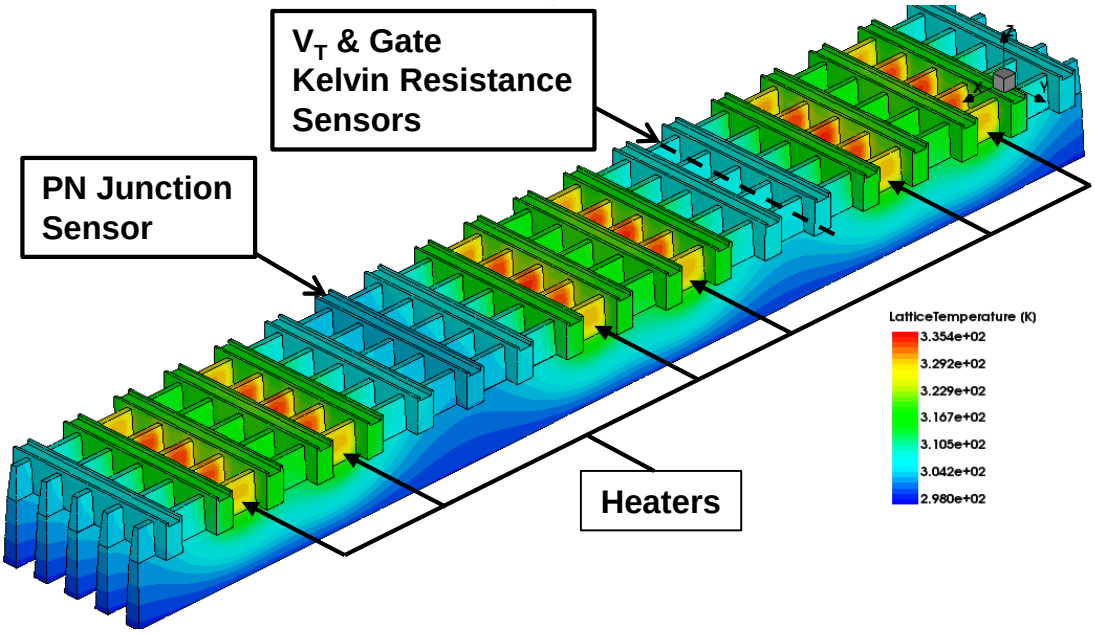


Figure 3.21 Thermal contours of local self-heat effects in NFET Bulk FinFET structure with 5 fins per active region RX.

The average temperature of the heater fins and sensor fins and the PN sensor region was obtained from these simulation results. It should be noted that the actual electrical measurements have a power drop across the BEOL metal lines which leads to underestimation of the slope parameter. The experimental measurements were corrected to include the effect of IR drop in the metal lines for fair comparison to the thermal TCAD results.

The simulation results show excellent predictive capability when compared to the IR drop corrected measurements without the use of any fitting parameters and offer a quantitative description on the physics of heat transfer. Figures 3.22-3.24 show the comparison of slope parameter for both 5fin and 20 fin NFET devices, between characterization and simulation results under the same power conditions. This confirmation validates the models and confirms the experimental results.

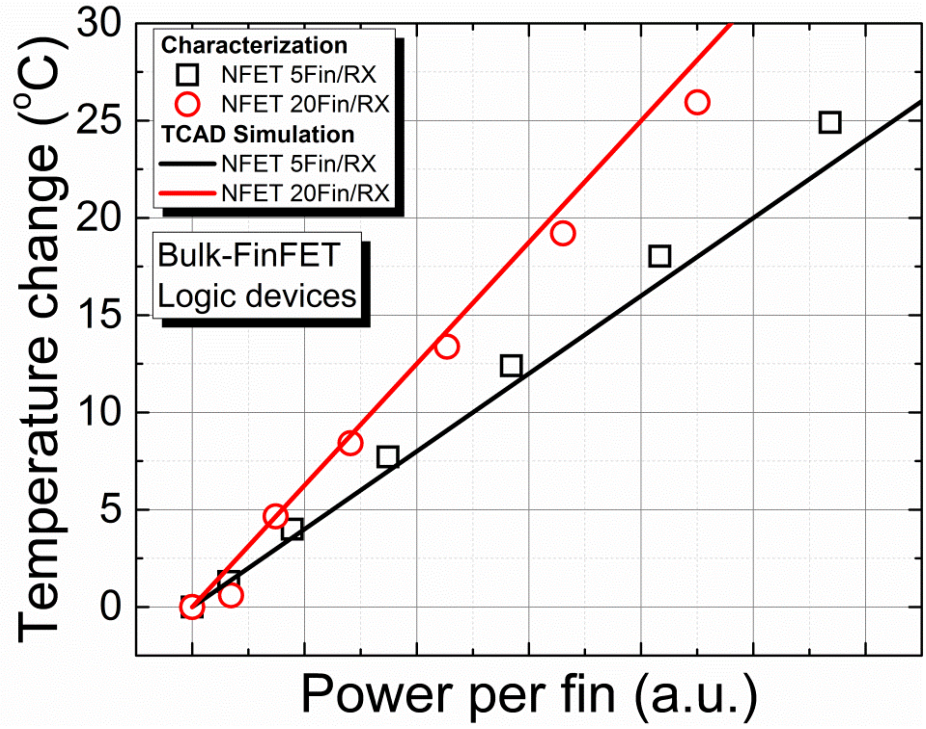


Figure 3.22 Comparison of self-heating for both 5 and 20 fin per active region RX using V_T (Type I) sensor.

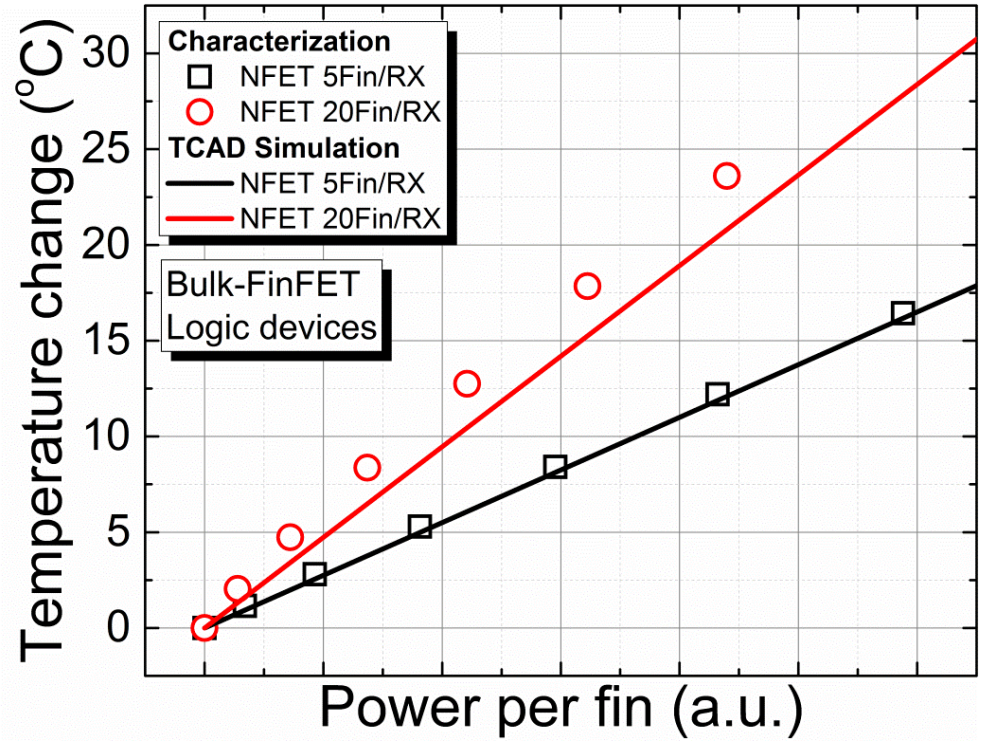


Figure 3.23 Comparison of self-heating for both 5 and 20 fin per active region RX using PN junction (Type II) sensor.

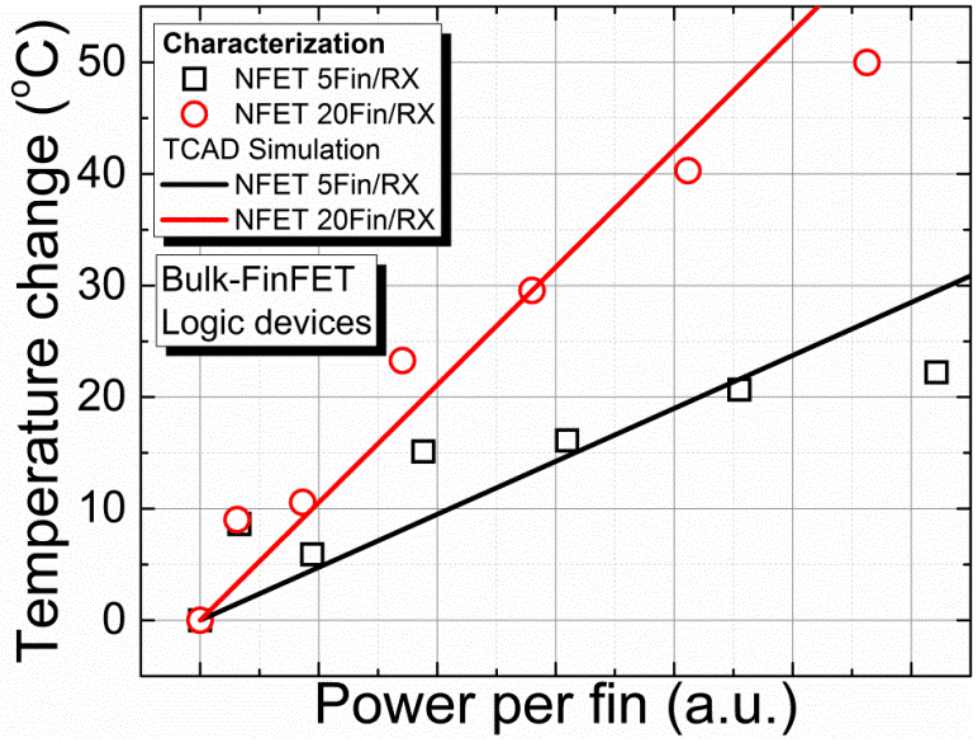
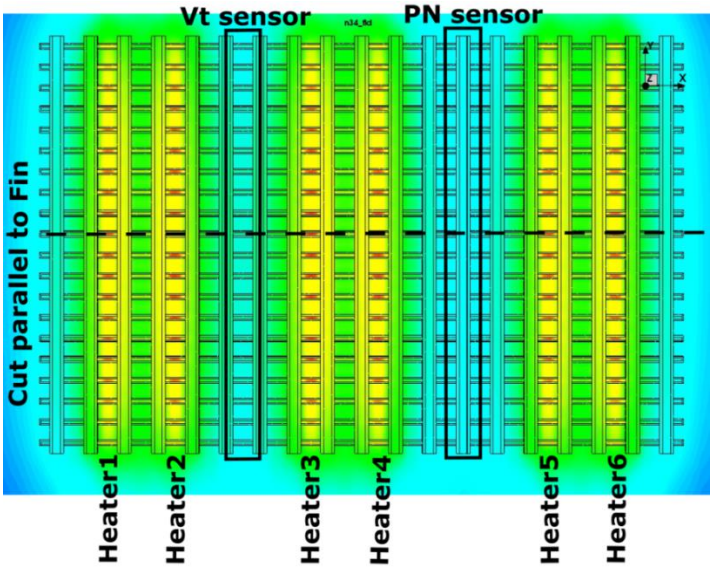


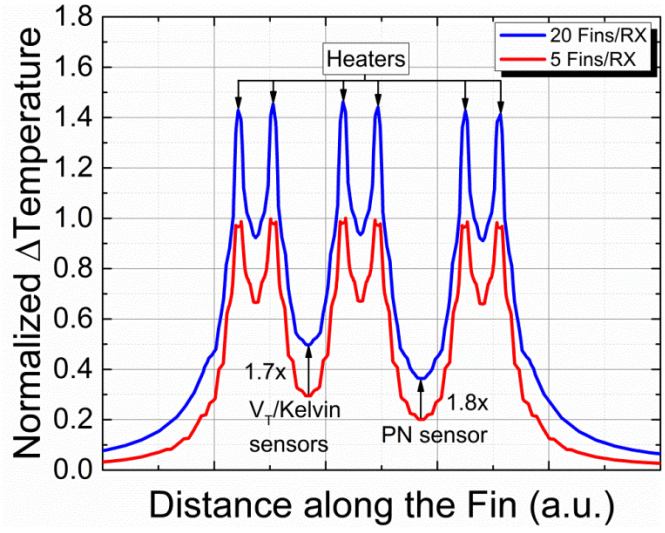
Figure 3.24 Comparison of self-heating for both 5 and 20 fin per active region RX using gate kelvin probe (Type III) R_G sensor.

Normalized temperature profile along the fin (Figure 3.25a) using thermal simulations are plotted and show that the lateral heat transfer along the fin length is higher for 20 fin heater compared to the 5 fin heater (Figure 3.25b). It is seen that at the location of V_T sensor (Type I), the temperature rise is 1.7x higher temperature for the 20 fin vs 5 fin heater due to the number of heat sources that reduce planar heat dissipation perpendicular to the fins. Figure 3.25b also shows that the peak heat in the channel in the source hot-spot region is ~3.3x higher compared with the location of the V_T sensor and ~3.7x higher with respect to pn junction sensor. It is important to understand the fact that channel source region hot-spot is at higher temperature than when sensed by metal gate sensor for the reason that the metal gate sensor reports average channel temperature. Also to be noted is that the PN junction sensor (Type II) is located 2.5 poly pitches away from the heaters and therefore should be heated less compared to the V_T sensor (Type I) which

is located 2 poly pitches away from the heaters. This slight difference is only evident in the simulation results (Figure 3.25b). The temperature rise value for the PN sensor is 1.8x higher in the 20fin compared to 5 fin configuration – a combination of higher self-heating and better sense strength in the 20 fin layout. These observations are in agreement with BEOL corrected hardware data (Figures 3.22 and 3.23).



(a)



(b)

Figure 3.25 Temperature profile cut (a) parallel to fins showing the difference in temperature (b) between V_T/Kelvin and PN junction sensor.

3.7 Self-Heating Comparison between SOI- and Bulk-FinFET Devices

The magnitude of self-heating in CMOS circuits is strongly dependent on technology topology as was discussed in Section 2.1. Figure 3.26 plots the measurement of self-heating against power for type I sensor, using threshold voltage (V_T) thermometry in 14nm bulk FinFET process against measurements across a range of fin sizes (2-20 fins). For comparison, self-heating response (R_{TH}) of the same sensor in a 2 fin SOI FinFET (with similar gate/fin pitch) technology is ~5x higher.

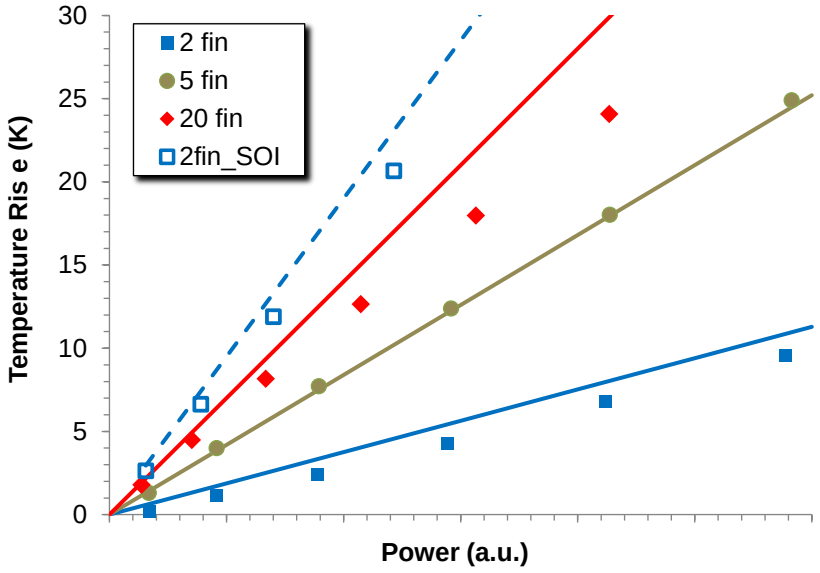
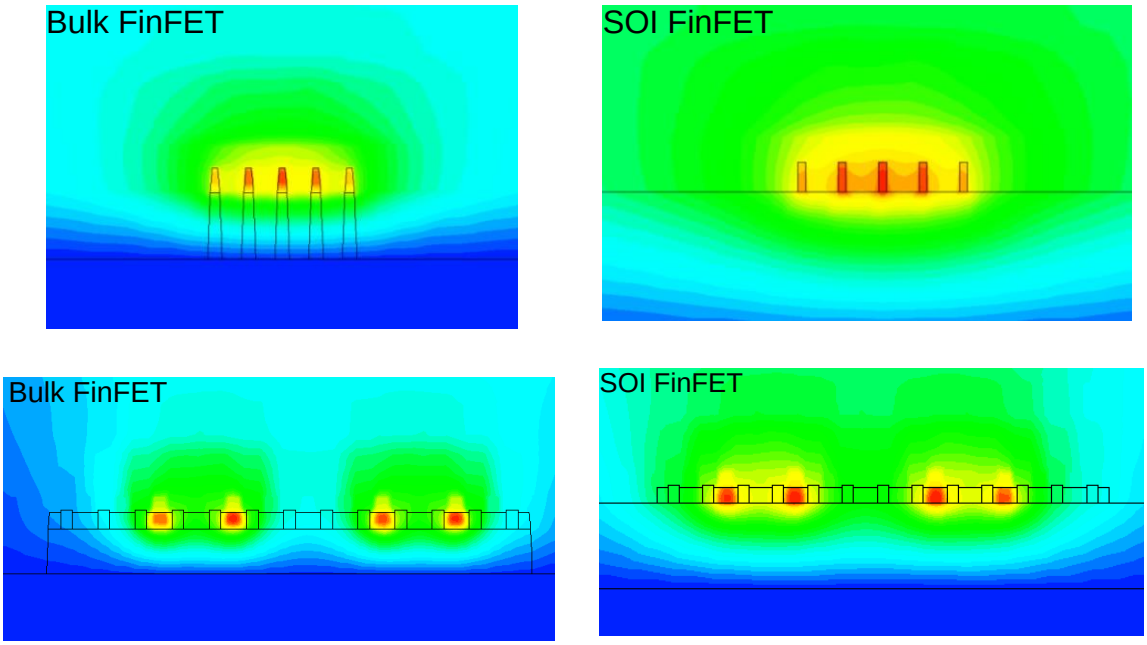


Figure 3.26 Self-heating measurements (symbols) and simulations (lines) of a V_T sensor with 2, 5 and 20 fins in bulk FinFETs and 2 fins in SOI FinFETs.

Higher temperature rise in SOI FinFET technology intuitively is expected because the buried oxide has poor thermal conductivity (Figure 1.2), which cuts off the heat sink pathway to the bulk silicon. This is well modeled in the TCAD thermal contour images for bulk FinFET and SOI FinFET devices as depicted in Figure 3.27.



(a) (b)

Figure 3.27 TCAD thermal simulation of heat spreading in bulk FinFET (a) and SOI FinFET (b).

Figure 3.27a clearly illustrates the ease of heat dissipation in the bulk FinFET through a wider more thermally conductive sub-fin. SOI FinFET (Figure 3.27b) on the other hand, suffers a higher in-plane spreading and shows a bigger "thermal footprint". Figure 3.27b shows more device heat being forced upward in SOI FinFET, posing a higher reliability concern for electromigration, degradation mechanism for the back-end-of-line metal stack.

A comparison of the average self-heating in bulk-FinFET devices and FinFETs fabricated on SOI substrates is summarized in Figure 3.27.

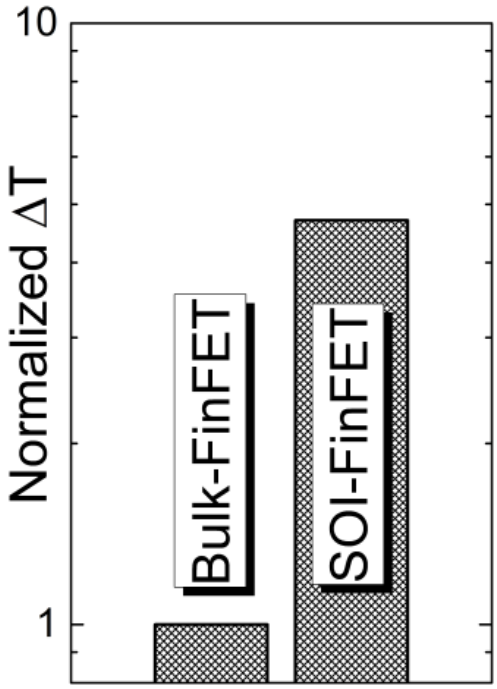


Figure 3.28 Comparison of self-heating induced average temperature change in n- and pFET sensor for SOI-FinFET and bulk-FinFET devices based on hardware calibrated thermal TCAD model.

The self-heating induced average temperature change, in the n- and pFET sensor is ~5x higher for FinFET devices fabricated on SOI compared to bulk Si substrates based on hardware calibrated thermal TCAD model. These results suggest that in bulk-FinFET devices heat flow to the Si substrate through the fins remains effective in limiting the temperature rise in the device.

3.8 Summary

Three self-heating measurement methodologies were explained in this chapter. The detail of sensor layout was presented emphasizing the importance in grounding the isolation gates between heaters and sensors (type I and II) for noise reduction. A case study showed that measurements on the three sensors are in excellent agreement in quantifying

the self-heating from 5 and 20-fin transistors when sensing adjacent heaters. Comparing the SH characteristics from different methodologies, it was showed that surrounding heat measurement underestimated the local device heat by ~ 35%. Thus the heat loss in the adjacent space should be taken in consideration when projecting device temperatures. Design of experiments has also proven that the temperature of the device is not simply determined by the local dissipated heat in the device, but a combination of the local heat and the heat from the surrounding.

The benefit of evaluating self-heating in a differential fashion has shown that the temperature error measurement due to wafer process variability can be reduced to as low as ±0.5°C. All sensors were verified for reliability by checking for measurement repeatability through wafer level prober chuck thermal cycling test as well as cycling power in heater structures themselves. The results proved sensors (Type I-III) to be reliable and reversible which allowed for their use in further investigation of self-heating effects in FinFET devices.

The characterization measurements were confirmed through detailed finite element thermal simulations of the used structures. This confirmed the accuracy of the electrical sensors, but also highlighted further differences in temperature gradients which could only be resolved through TCAD thermal simulation. The difference, in heat sensed by the V_T and pn junction sensor from the actual temperature at the source hot-spot region is actually ~3.3x and ~3.7x higher, respectively. This correction factor will be used for further studies presented in the upcoming chapters. Finally, the level of self-heating present in SOI FinFET is ~5x higher compared to bulk FinFET technology which was verified through characterization and simulation results.

CHAPTER 4

AMBIENT TEMPERATURE AND LAYOUT IMPACT ON SELF-HEATING CHARACTERIZATION

Self-Heating effects are going to be of increasing significance in future nodes. Understanding self-heating measurement results and its accuracy is of vital importance. Layout density can have significant contribution to self-heating effects which can impact the rate of device degradation. Furthermore, technology topologies, such as bulk FinFET or SOI FinFET can differ substantially in pathways heat is dissipated; this will be addressed in this chapter. Moreover, it will be presented for the first time through measurement, that the ambient temperature can affect self-heating measurement by up to 70%. Through a series of measurements at different temperatures and dissipated power, the results show that the Si fin has a more dominant effect in heat transport and its varying thermal conductivity should be taken into account.

4.1 Introduction

Three-dimensional structures (FinFET) are now the core of advanced nodes manufacturing. With these confined structures, self-heating has become a growing concern. The thermal resistance of the devices has increased going from planar to bulk FinFET and into SOI FinFET and it's expected to grow in future devices like gate-all-around transistors. Self-heating is extensively discussed in the literature [10, 11, 12, 33] to address the impact on reliability since for some mechanism the degradation levels is enhanced. This chapter will quantify the increase of self-heating with increased layout density by studying varied density of fins per active region RX. Lateral heat dissipation

will be measured in bulk FinFET and SOI FinFET technologies, where results will show more lateral spreading in SOI technology caused by the buried oxide, which forces the heat dissipation upward through metal stacks. Furthermore, ambient temperature (T_a) on self-heating characterization will be assessed. By performing self-heating characterization at different T_a, it will be shown that ambient temperature can modulate the self-heating by up to ~70%. This is particularly important in high temperature electronic applications where self-heating effects will be underestimated. Through these results, it will be shown that the contribution of the silicon heat conductivity is more significant than initially assumed and should not be ignored in self-heating assessment and modeling.

4.2 Experimental

Dedicated logic FinFET structures were designed to measure self-heating as presented in Chapter 3. The goal of the experiment is to check the influence of ambient temperature on self-heating assessment all while accounting for fin count (density) and heater to sensor proximity influence. In order to characterize the proposed dependencies, three types of sensors were utilized (Figures 3.1, 3.2) and verified [49, 50]. V_{Tlin} sensor was used to study density and proximity effects while PN-junction sensor was utilized for T_a dependence study. It is important to point out that PN-junction sensor is a source to substrate diffusion as depicted by green regions of the device (Figure 3.1a, 3.2b).

First sensor (Type I) utilizes transistor's thermally sensitive threshold voltage (V_T) while the second sensor (Type II) with a pn junction diode uses its thermally sensitive forward bias voltage (V_D). Both V_T and V_D sensors are sensitive to temperature in the linear (subthreshold) region. Therefore an adjacent transistor FET operating in saturation

is used as the heater. All three sensors are calibrated at several different chuck temperatures to extract their temperature coefficient as described in Chapter 3. During actual transistor heating the thermally sensitive parameters were recorded at several different heater power dissipations (V_{gs}=V_{ds}). The difference of parameter value change (ΔV_T, ΔV_D and ΔR_G) in response to power dissipation in the heater is translated into temperature change using their respective thermal coefficients. Both p-type and n-type FinFET logic structures were used in this study with different number of fins (2 to 20 fins).

To study lateral heat dissipation in FinFET technology, an additional structure was designed, which allows for thermal resistance measurement at different distances from the heat source as shown in Figure 4.2, where V_T (type I) sensor is placed on far-left.

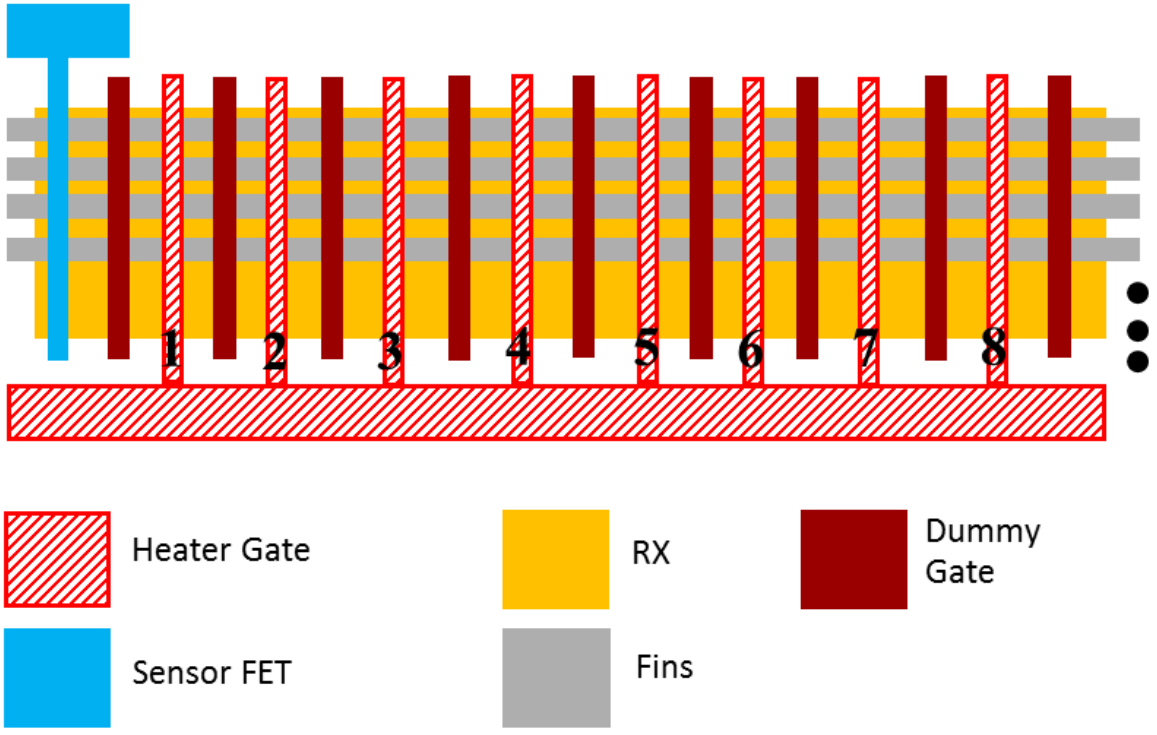


Figure 4.1 Layout for the lateral heat conduction test using FinFET technology.

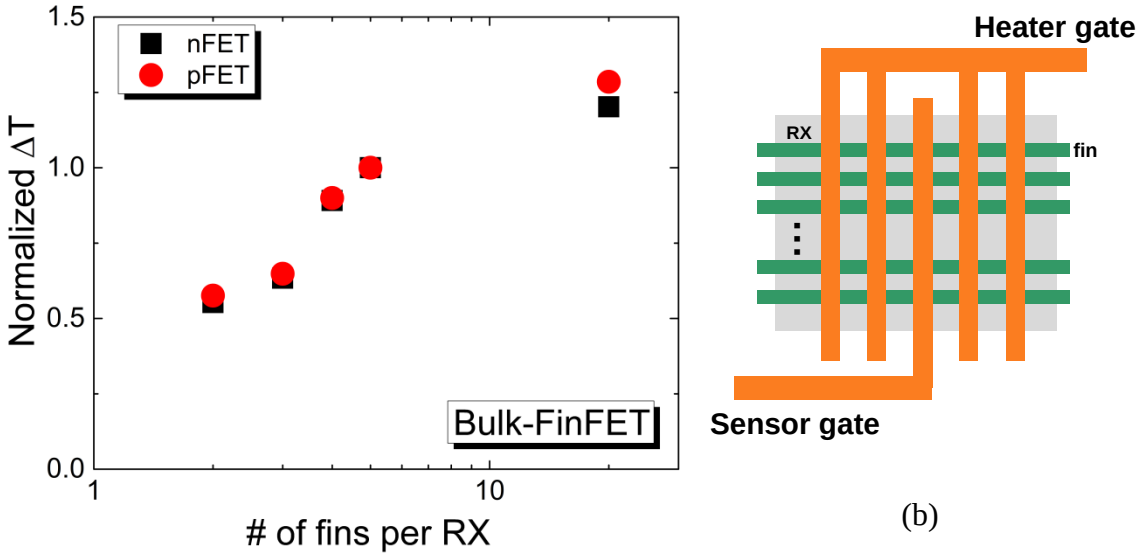
The sensor measures heat from the heater gates as they are turned ON, one by one (1-8) with same self-heating characterization technique described in Chapter 3.

4.3 Layout Impact on Self-Heating

Circuit layout density is always limited by design rules of a particular technology node. In FinFET technology, fin and PC pitches are usually fixed and other minimum spacing such as active regions (RX-to-RX) islands are defined. Among different knobs available to layout designers, are the number of active gates, fins and the spacing between RX-to-RX islands which have to adhere in accordance to the design rules. This section will show that the choice of layout density can modulate thermal properties of a circuit; where as expected, more heating impact is seen in denser designs. Discrete reliability layout test structures do not necessarily need to be compact, therefore less dense approach should be taken to minimize the impact of self-heating. This is especially true in high current driven reliability testing, such as hot carrier, where temperature can modulate results. Temperature sensors used in this study showed an excellent agreement as illustrated in Figure 3.7, proving any sensor can be utilized for the proposed studies here. It should be noted that V_{Tlin} and PN junction sensors underestimate the actual peak channel temperature by ~3.7x as shared in Chapter 3, however for most of the studies here, relative impact is studied and precise temperature is not needed to conduct the learning. The following sub-sections will show how density of fins impacts levels of self-heating and how heat dissipates laterally across bulk FinFET and SOI FinFET circuit technologies.

4.3.1 Layout Density

The level of self-heating is known to be strongly dependent on the density of the test structures [10, 11, 12]. Figure 4.2 shows a rise in normalized temperature with increasing fin count, ranging from 2 to 20 fins per active area. Temperature rise of 2x is observed as density of fins increases from 2 to 5 and 1.25x moving from 5 to 20 fins per active region. Saturation of heat is observed at 20 fins for bulk Fin FET technology.



(a) (b)

Figure 4.2 Temperature change versus number of fins per active area (RX) at constant power per fin for bulk-FinFETs normalized to the 5 fin device (a). Illustrative figure of structure used for study, showing variation of fin count per active region (b).

Due to a significant variation of temperature between layout densities, designs meant to be used in reliability testing can spread the fins across multiple islands to mitigate the effects of self-heating. However, the separation of RX islands also needs to be sufficient to eliminate any thermal cross talk due to lateral heat spreading, which will be the topic of the next sub-section.

4.3.2 Lateral Heat Dissipation

Thermal model of lateral heat dissipation can offer an advantageous guidance for self-heating aware layout designs. In test structure design, it is beneficial to know what spacing to use between active regions RX if thermal cross talk is to be minimized. For self-heating characterization, knowledge of lateral heat dissipation can also be used for heat loss corrections. Figure 4.3 shows how heat dissipates laterally with distance in a bulk FinFET circuit. The radial distance affected by self-heating is within radial distance of ~1µm, which was conveniently confirmed through measurement on test structure depicted in Figure 4.1. This learning will offer design guidance for structures used in experiments presented in Chapter 5.

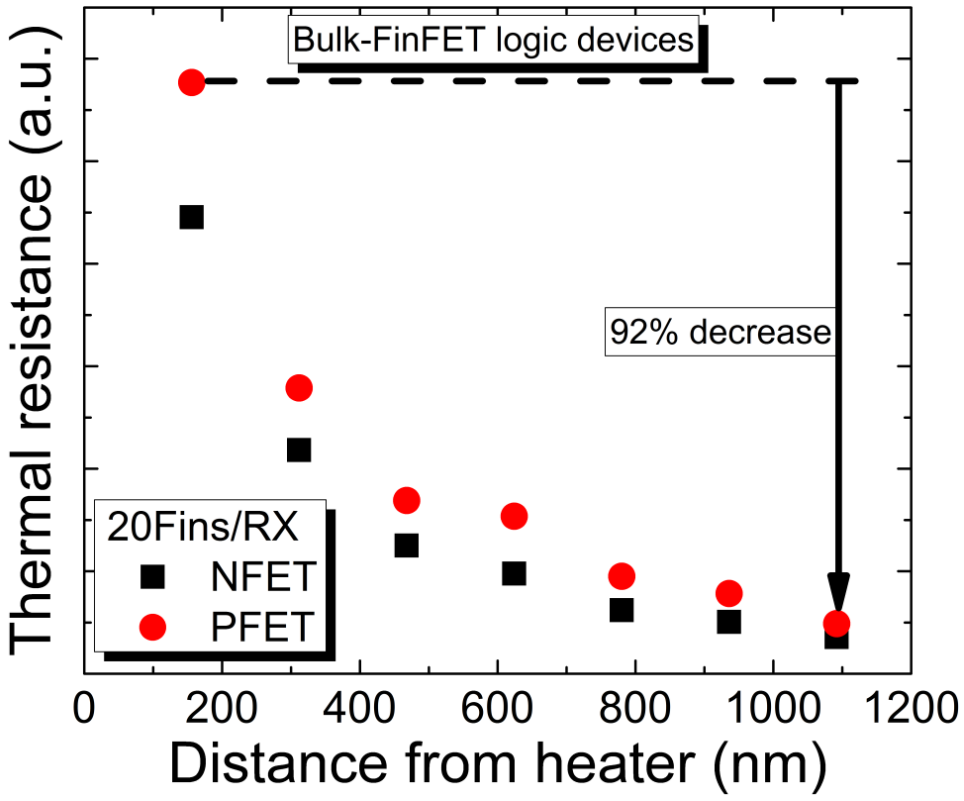
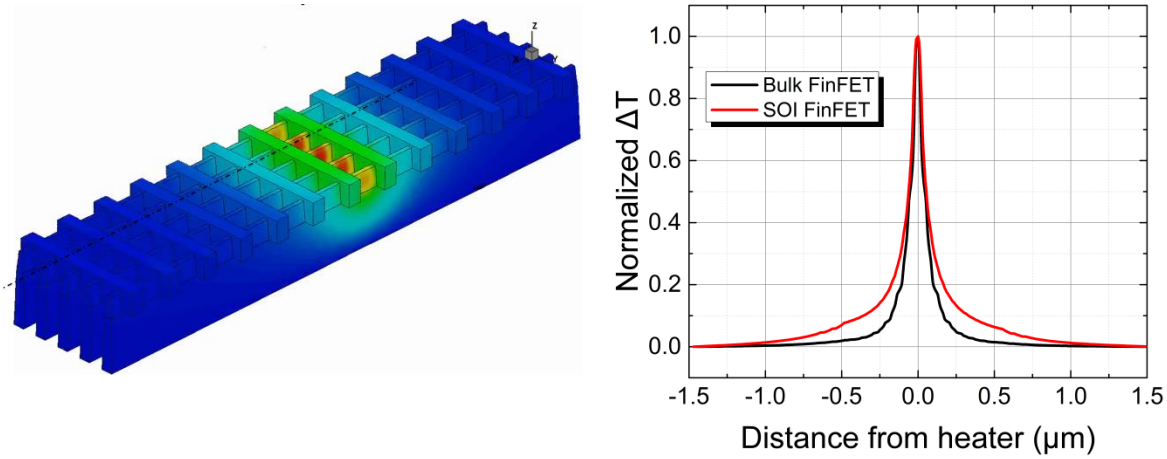


Figure 4.3 Self-heating sensed at different distances from the heater in Bulk-FinFET core logic devices.

Lateral heat dissipation study was also conducted on SOI FinFET technology through TCAD thermal simulation as shown in Figure 4.4, which is compared to bulk FinFET. Based on the learning in Chapter 3, Figure 4.4 confirms the expectation for SOI FinFET thermal conductivity to be slower. This is due to the buried oxide, which with poor thermal conductivity forces the heat generated in the fins upward and in the lateral directions.



(a) (b)

Figure 4.4 Bi-directional, lateral heat dissipation through TCAD thermal simulation performed along the cut on bulk FinFET (a) and SOI FinFET. SOI FinFET shows greater lateral spreading compared to bulk FinFET technology (b).

SOI FinFET in Figure 4.4 shows more lateral heat spreading, where the heat needs to travel ~500nm further compared to bulk FinFET to be totally dissipated.

4.4 Ambient Temperature Impact on Self-Heating

To study the effect of ambient temperature on self-heating characteristics in wafer level testing, two studies were implemented in the next two sections; first is by introducing heat through the prober thermal chuck and second by adjacent heater transistor devices

themselves. Measurement of ΔT will show to be higher at elevated ambient temperatures for the same power delivered to the heater, which makes this an important finding.

4.4.1 Chuck Temperature Dependence

The effect of T_a on self-heating was studied at several chuck temperatures ranging from -40°C to 175°C (Figure 4.5). The temperature increase in response to power dissipation is clearly dependent on ambient temperature regardless of the device type or density. The heat loss between sensor and heaters is not accounted for in the measurements of Figure 4.5; however it would not change the relative observation shown and therefore, is not relevant for the learning performed here.

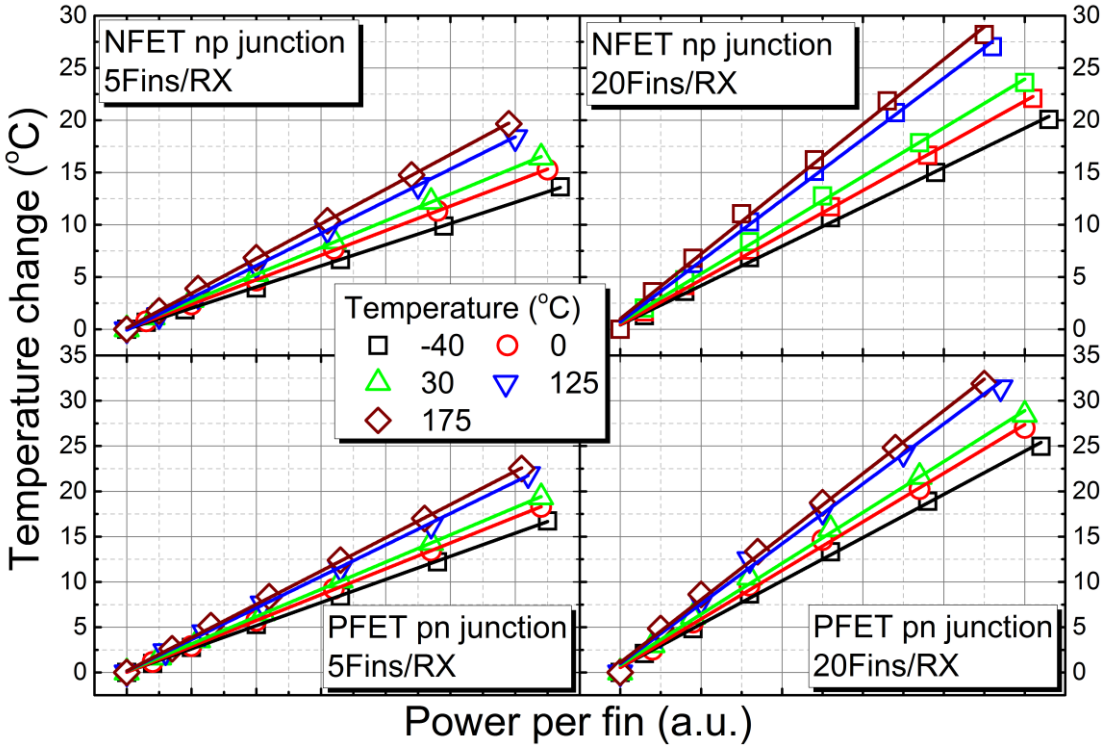


Figure 4.5 Self-heating characteristics for 5 and 20 Fin FET heaters, using FET np and pn junction sensors at different prober chuck temperatures (-40 to175°C).

The thermal resistance (slope) increases with temperature for all device types. The thermal resistance of the 20-fin n-type and p-type devices show 70% and 45% increase respectively as chuck temperature increases from -40 to 175°C (Figure 4.6).

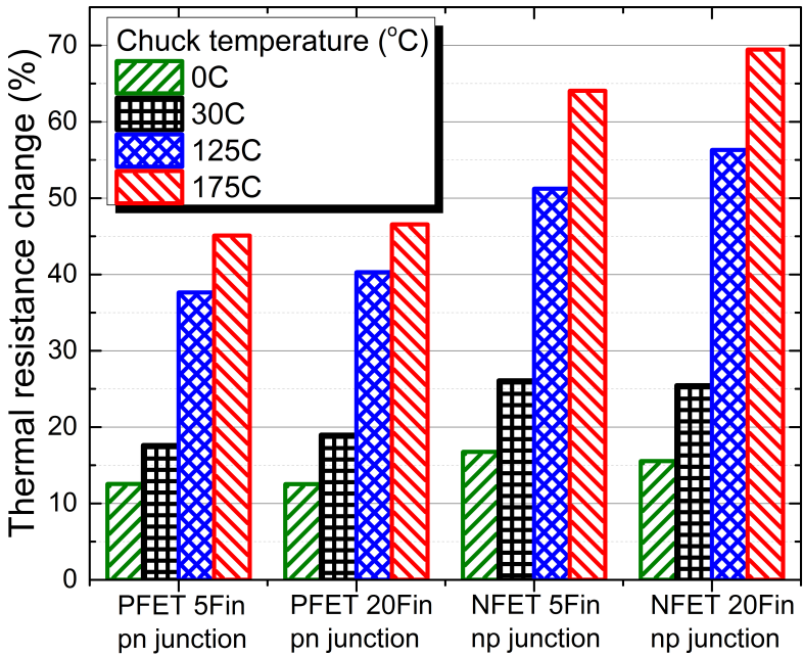


Figure 4.6 Thermal resistance increase relative to the resistance measured at -40°C. Up to 70% increase is observed.

Intuitively, this is somewhat expected because the thermal conductivity *k* of the silicon is temperature dependent and therefore self-heating measurement should depend on T_a. However, this is almost always overlooked in the literature as most of the self-heating studies are measured at single fixed temperature. Indeed, the change in *k* for Si fins and nanowires is much smaller than that in bulk Si (slopes in Figure 4.7 [5, 34]) which explains why it is usually considered to be negligible. Additionally, most of the SH studies focus on a narrow range of operating temperatures in which silicon fins *k* can be approximately constant.

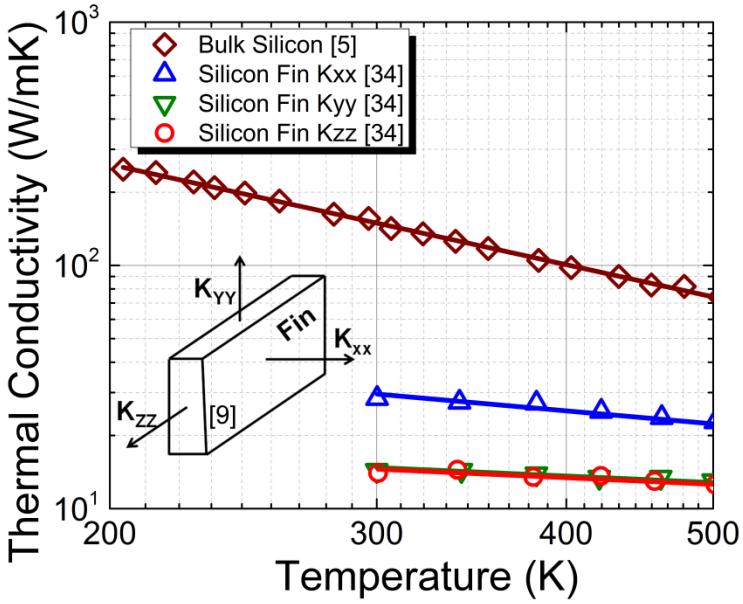


Figure 4.7 Theoretical thermal conductivity of silicon bulk compared to silicon fin.

Figure 4.8 shows the thermal conductivity (k_*) of the devices used here which exhibits a similar temperature dependence (slope) to that of Si fins (Figure 4.7) indicating a possible dominant effect from the Si fin.

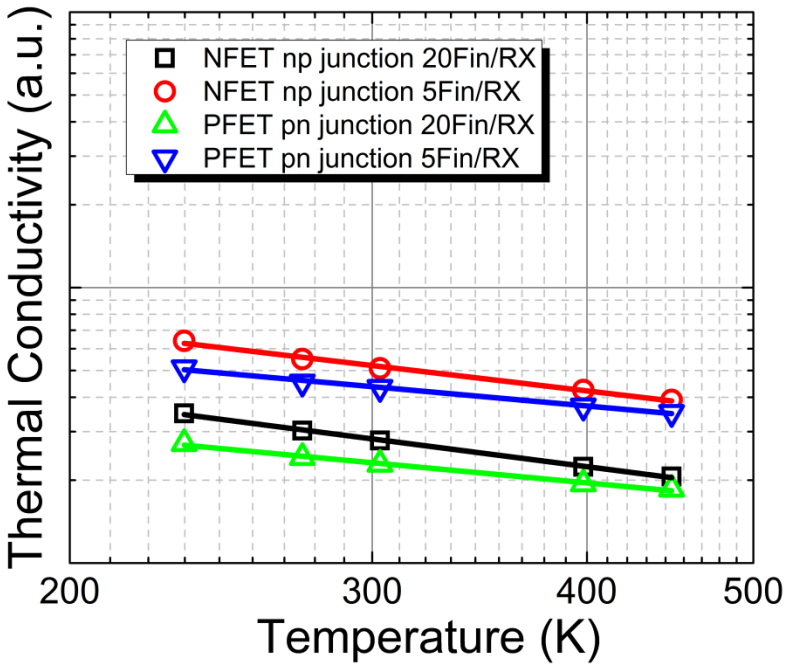


Figure 4.8 Thermal conductivity of tested devices versus ambient temperature.

Note that the device conductivity is presented in arbitrary units because it does not represent the pure material conductivity as shown in Figure 4.8. Unlike numerical simulations, self-heating measurement does not allow a distinction between the different device materials influencing the heat transport, including MOL and BEOL stacks where metal *k* is generally constant. Dielectrics *k* increases and silicon *k* reduces strongly with increased temperature in the temperature range studied here (-40 to 175°C). Instead, the whole device is considered as a system and its thermal resistance represents its temperature increase in response to power dissipation in the whole system.

4.4.2 Adjacent Heater Transistor Dissipated Power Dependence

If heat transport in FinFET is indeed dominated by silicon fins as shown by varying the ambient test temperature, the same should be true by changing the dissipated power in adjacent heater transistor devices. Thus, the heat to power transfer characteristic should not be linear as usually reported [10, 11, 12, 51]. In Figure 4.9, self-heating measurement was repeated while doubling the power dissipation in heater devices to increase the captured temperature range. This was conducted at (T_a = -40°C) and $V_g<V_d$ beyond saturation point to minimize the heater transistor degradation. As predicted, the slope starts changing (~8% increase) at higher temperatures in agreement with observations from Figures 4.5-4.7. This is a significant confirmation of same experiment conducted with chuck temperature variation. It could be argued that the increased self-heating effects observed in Section 4.4.1 by modulation of the chuck temperature might be associated with the fact that the metal chuck itself is contributing to this effect. However,

testing the same concept by modulating the adjacent heater transistor structures confirms the impact of T_a dependence on self-heating characterization.

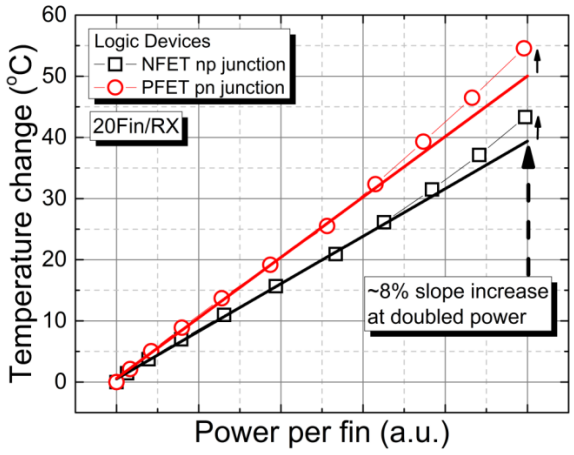
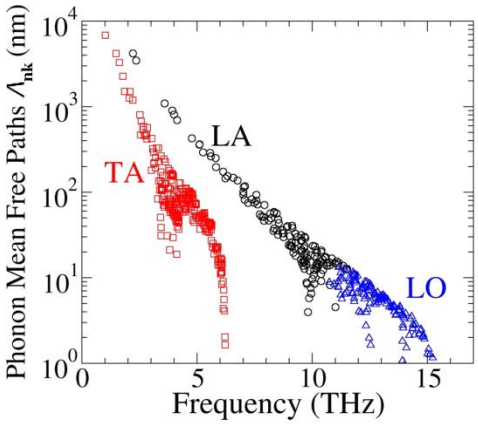


Figure 4.9 Self-heating at up to twice the power applied to the heater. 8% increase in slope is observed at high temperatures/power dissipation.

The ambient temperature impact on thermal conductivity in devices measured in Figure 4.5 and Figure 4.9 are directly tied to phonon boundary scattering modes which take place in the FinFET structure. Figure 4.10a shows the intrinsic phonon mean free



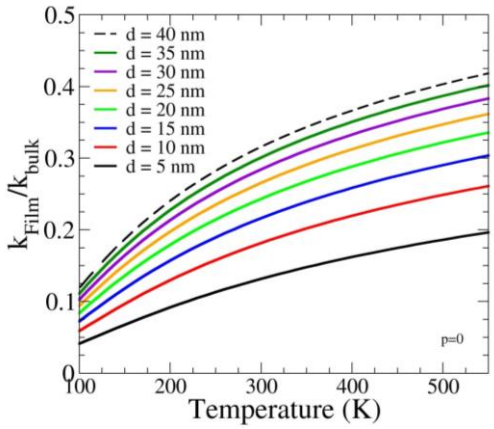


Figure 4.10 (a) Phonon mean free paths (nm) in bulk silicon at 300K for longitudinal (LA) / transverse (TA) acoustic branches across the frequency range (b) Thermal conductivity (k) reduction in Si fins as a function of temperature.

paths, $\Lambda_{\mathbf{nk}}$ for the primary branches responsible for heat conduction which span over 3 orders of magnitude and are significantly higher than the fin/subfin width. This implies a strong reduction in the thermal conductivity of silicon fins in comparison to planar bulk Si.

4.5 Summary

Several important findings in this chapter established learning which is essential for the experiments which will be presented in Chapter 5, where reliability aspect of self-heating impact will be studied. Specifically this chapter has shown that density of layout structures can significantly impact local temperature. Through series of experiments it was shown that increasing fin density from 2 to 5 fins per active region RX results in 2x temperature rise and 1.25x by going to 5 to 20 fins per RX. Saturation of heat is observable while reaching 20 fins per RX.

Lateral heat dissipation experiments and TCAD thermal simulation helped to determine the affected radial distance from a hot spot region, which for bulk FinFET technology is ~1µm and for SOI FinFET is ~1.5µm. This learning is applied to the design of structures used for experiments in Chapter 5, but it's also important to understand that the distance may vary depending on which technology is assessed.

Finally, ambient temperature was found to have a considerable effect on self-heating as it showed a 70% and 45% increase when measured at 175°C compared to -40°C for NFET and PFET devices, respectively. With increased fin count these effects are expected to be more pronounced. This increase is linked to the thermal conductivity of the silicon fins.

CHAPTER 5

SELF-HEATING EFFECTS ON HOT CARRIER AND TIME-DEPENDENT DIELECTRIC BREAKDOWN DEGRADATION AND ITS IMPACT ON RING-OSCILLATOR RELIABILITY

This chapter discusses the impact of self-heating (SH) on ring-oscillator (RO) reliability and its correlation to hot carrier (HC) and time dependent dielectric breakdown (TDDB) degradation. It is shown that HC degradation modulation due to self-heating is only significant for logic PFETs at highly accelerated conditions. It will be shown that self-heating effects on HC are greatly reduced at moderate acceleration. Furthermore non-uniform TDDB evaluation shows reduction of device lifetime due to self-heating effects. By stressing the ROs at extreme conditions, the findings in this chapter reveal that the self-heating impact on HC does not affect RO degradation.

5.1 Introduction

Self-heating has been reported as a rising concern in three-dimensional structures such as bulk/SOI FinFETs [10, 11, 12]. The confined heat is expected to accelerate some of the transistor reliability mechanisms, particularly hot carrier (HC) degradation [33, 50, 51]. A correction method has been proposed to account for self-heating effects when modeling hot carrier degradation [51]. However, the extent of self-heating effects on hot carrier at moderate acceleration levels is yet to be addressed. This chapter evaluates self-heating effects on hot carrier for different device densities, at different stress levels (DC) and shows that the hot carrier degradation difference due to self-heating effects is greatly reduced at moderate acceleration. Furthermore, time dependent dielectric breakdown (TDDB) is known to be one of the most important degradation mechanisms affecting the

reliability of CMOS devices. Therefore, this chapter will also study self-heating effects on TDDB performance by comparing uniform and non-uniform ($V_d \neq 0$) TDDB stress in bulk high-k/metal gate (HK/MG) FinFET technology. Non-uniform stress condition occurs mostly in RF applications because the devices are ON during operation. On the other hand, self-heating is supposed to be reduced during AC stress [51]. However, the extent of self-heating effects on hot carrier in logic circuits, such as Ring-Oscillator (RO), needs to be quantified. Several RO designs with different densities were measured for self-heating and correlated to RO degradation. This chapter shows that the heat generated by the different density ROs is negligible and that their degradation is identical.

5.2 Experimental Setup

Dedicated Ring-Oscillators (RO) are designed in 14-nm bulk FinFET technology to measure self-heating in logic circuits. Several RO designs are implemented with different densities (number of fins, number of fingers) and different number of stages (13 and 101 inverting stages having different oscillating frequencies). Metal sensor with kelvin contacts is placed immediately on top of the ROs (first metal layer) to allow measurement of RO self-heating (Figure 5.1). The sensing method with kelvin metal sensor uses same temperature rise extraction techniques discussed in Chapter 3. However, the temperature loss between sensor and RO circuit is accounted for with TCAD thermal simulations.

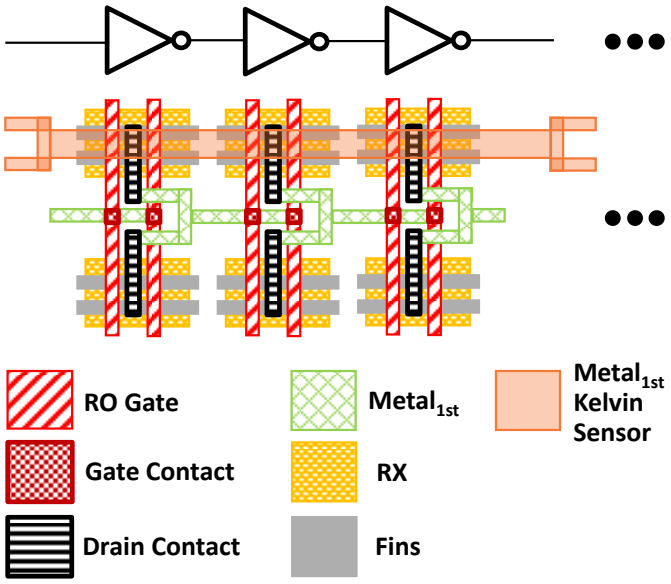


Figure 5.1 Illustrative figure showing the ring oscillator layout designs with metal (M1) temperature sensor with kelvin contacts.

Additionally, logic and IO FinFETs are designed to measure self-heating for 4 different architectures (Figure 5.2) with increasing densities but same total width (same drain current). This is to ensure that the hot carrier degradation is not modulated by different drain currents.

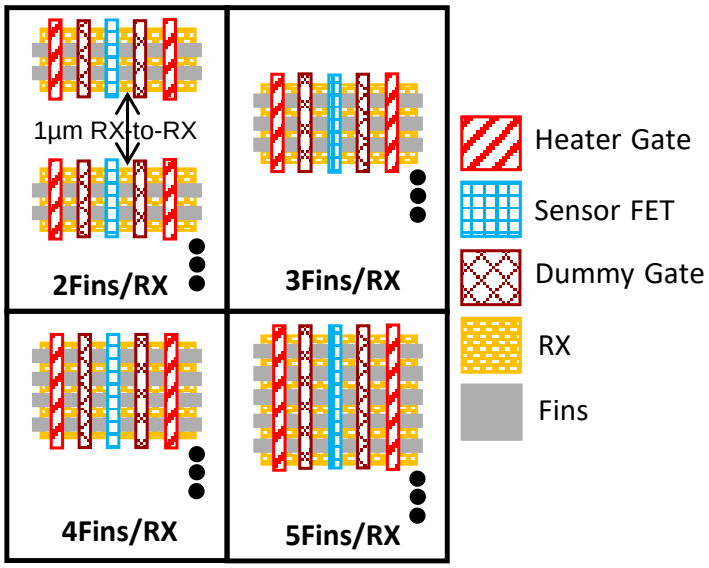


Figure 5.2 Illustrative figure showing the layout designs of the 4 FinFET devices used.

The SH measurement methodology in this study was described in [41, 50] and described in detail in Chapter 3.

For conventional HC at constant voltage stress, a biasing configuration is used as depicted in Figure 5.3, showing the test instrumentation source measurement unit (SMU) connections. The drain current is monitored in a logarithmic fashion during total stress time for 10Ksec.

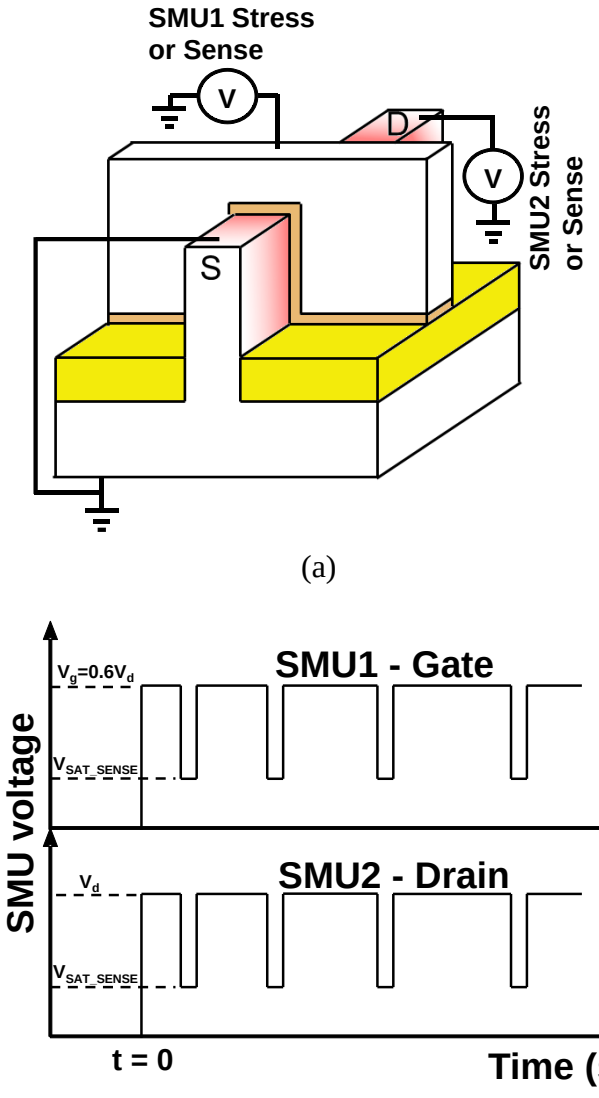
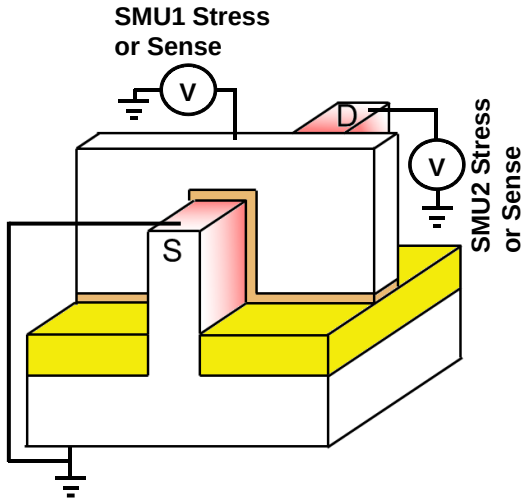
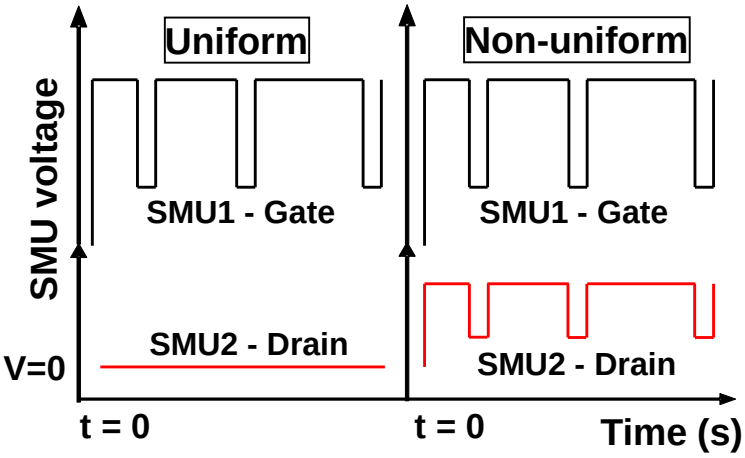


Figure 5.3 SMU connections for a conventional constant voltage HC stress (a) and waveform of an applied stress (b).

For the conventional uniform TDDB stress, the gate is biased in inversion mode ($V_g > 0$), while other terminals are grounded ($V_s=V_d=V_b=0$). Unlike uniform TDDB, non-uniform TDDB also biased the drain during stress ($V_d > 0$) causing a significant channel conductance. The gate leakage current is monitored at logarithmic time intervals for both stress types, while drain current is only monitored in non-uniform stress (Figure 5.4).



(a)



(b)

Figure 5.4 SMU connections for a conventional uniform and non-uniform constant voltage TDDB stress (a). Applied gate and drain bias during stress, showing the difference between TDDB stress types. The drain is biased and monitored for non-uniform TDDB (b).

Unlike constant voltage stress described for HC and TDDB where self-heating occurs during stress time, RO conducts current through the channel only during transients as depicted in Figure 5.5. Because heat has a very fast thermal dissipation time constant (on the order of several ns), the levels due to stress are expected to considerably lower in CMOS circuits if compared to constant voltage stress scenario in discrete devices.

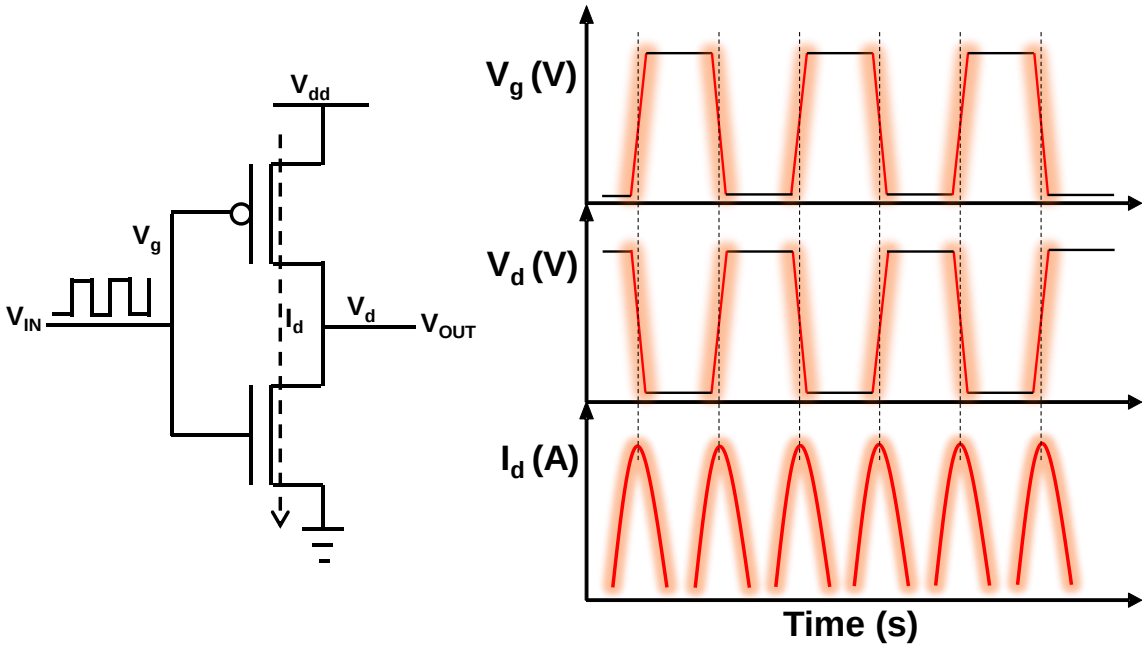


Figure 5.5 Illustrative figure showing during which times current flows through PFET and NFET devices while RO is in operation.

The following section will discuss the levels of self-heating expected at DC conditions for discrete devices and at AC conditions for the RO structures. Once temperature is quantified for operating and stress level conditions, the next section will discuss the impact of self-heating on reliability of the devices discussed in this section at both DC and AC conditions.

5.3 Results and Discussion

5.3.1 Self-Heating Characterization at DC and AC Operation

Figure 5.6 shows the locally measured temperature change of the different RO designs at different bias condition. The first observation is that for the same number of gate fingers, the heat increases with increasing number of fins.

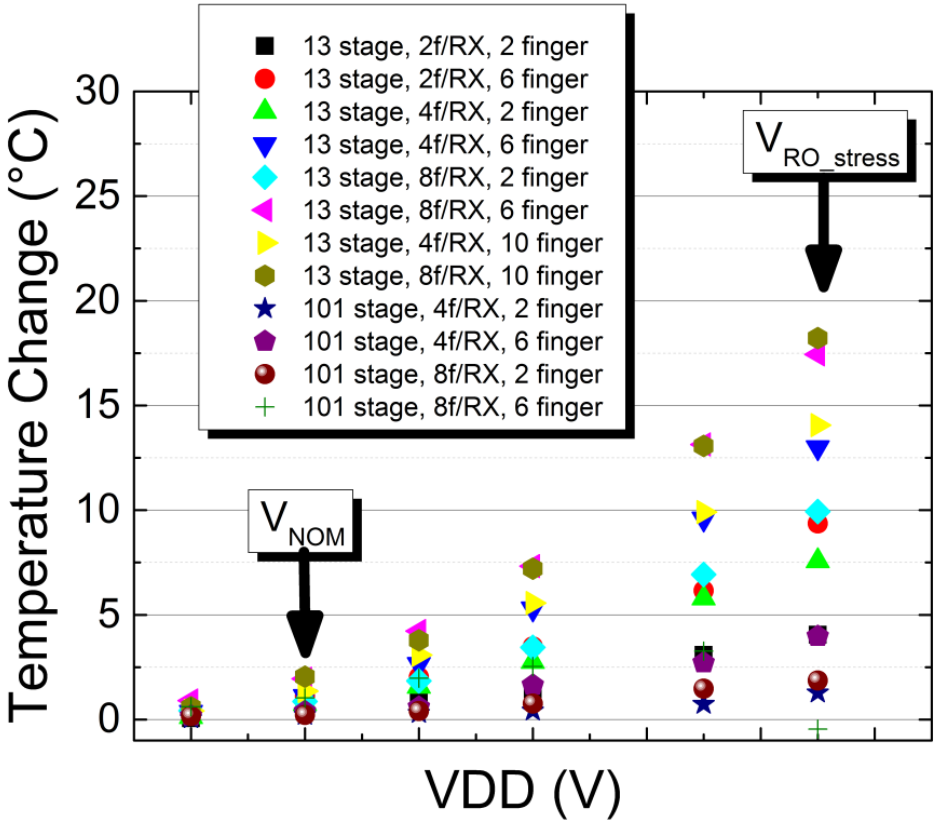


Figure 5.6 Measured Ring-Oscillator self-heating characteristics showing temperature increase vs. power supply. Note that the RO heating is <2.5°C at nominal condition and <18°C at extreme stress.

The temperature also rises with increasing number of fingers for the same fin count. Additionally, the 13-stage RO shows higher heating overall compared to the 101-stage RO because it oscillates at a higher frequency. However, the measured temperature

change at nominal voltage (V_{NOM}) for all ROs is <2.5°C. At extreme stress condition (V_{RO_Stress} > 2 x V_{NOM}), the 13-stage RO with the highest density (8Fin/10Finger) shows a temperature increase of ~18°C. To further illustrate the impact of RO density from Figure 5.6, only the maximum stress (V_{RO_Stress}) is plotted in Figure 5.7, which shows the temperature change versus the product of fins and PC fingers.

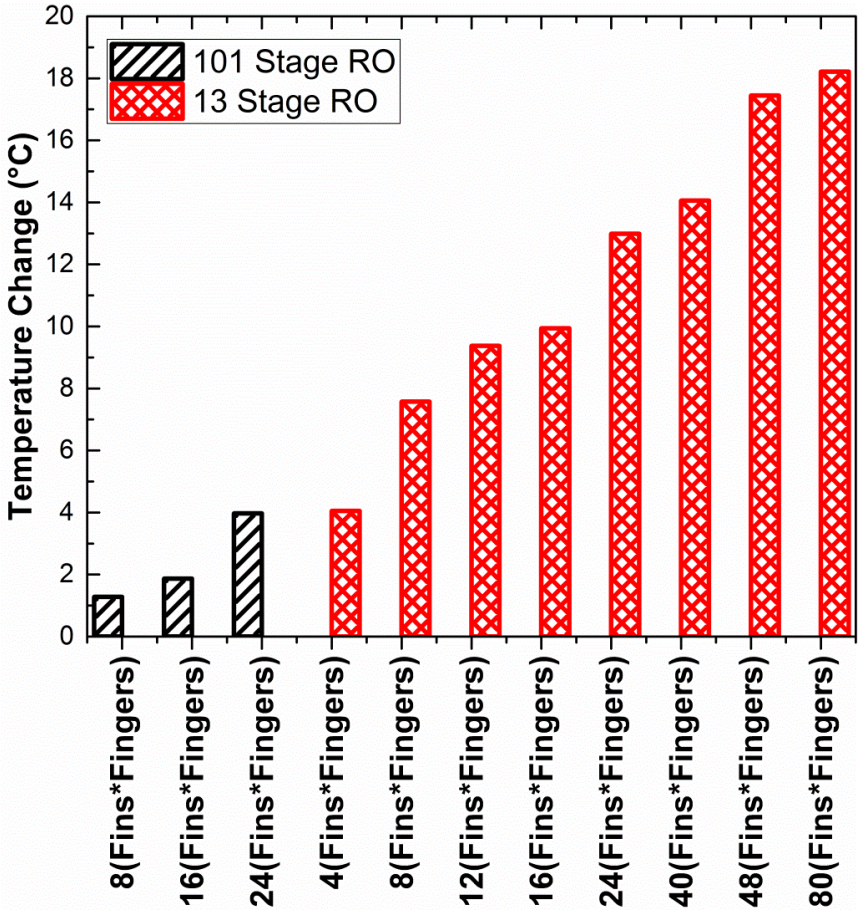


Figure 5.7 Detail of Figure 5.3, showing measured Ring-Oscillator self-heating characteristics showing temperature increase vs. layout density (fins*fingers) for V_{RO_Stress} condition only. Clear density and stage count dependence is observed.

Thus, the temperature increase due to self-heating in logic circuit is much lower than what has been reported under DC hot carrier conditions [10, 11, 12, 33, 51]. Self-

heating effect in discrete devices was examined next by measuring the local heating characteristics for all different device types (logic and IO NFET/PFET) with different densities (Figure 5.8) as function of the dissipated power per fin at DC conditions.

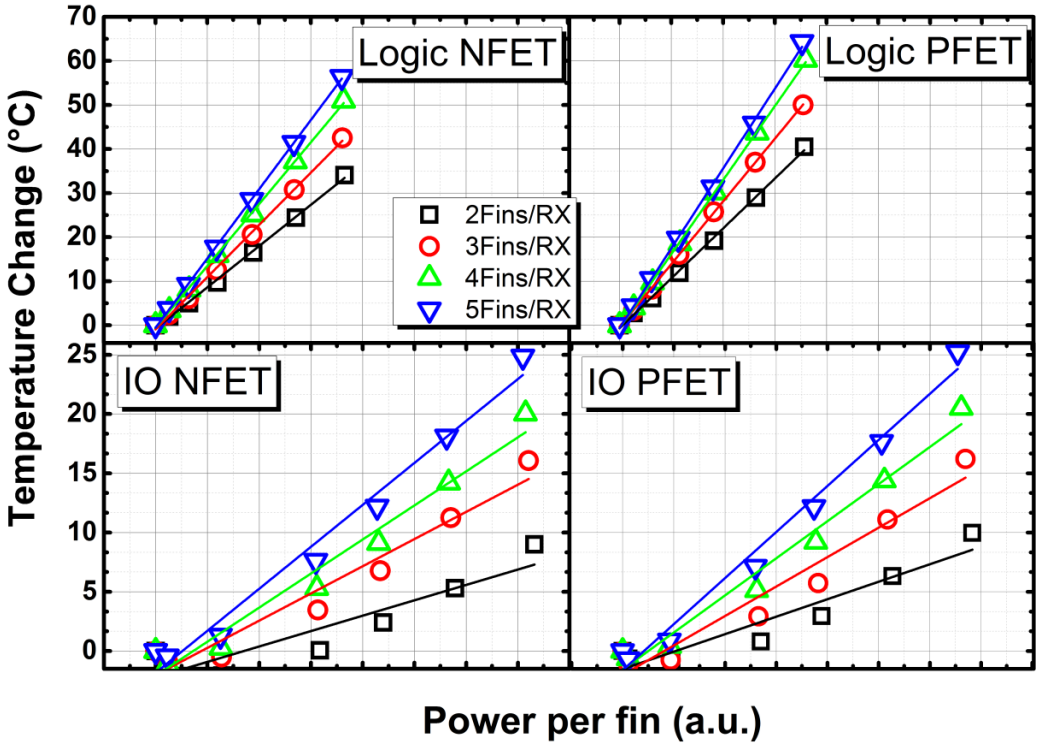


Figure 5.8 Measured Self-heating characteristics showing device source temperature as a function of dissipated power for different device types/densities. The IO devices show a lower heating compared to logic.

As expected, the logic devices show higher self-heating compared to IO devices because of the larger fin volume geometry of the IO devices allowing more heat transport while the heat is more confined in the logic FinFETs making the same process slower. Figure 5.8 also shows that the heat increases with increasing density, with 2Fin/RX showing the lower amount of self-heating. The results shown in Figure 5.8 quote true heater device temperature as heat loss between sensor and heater is accounted for by correction method shared in section 3.6.

5.3.2 Self-Heating Effect on Hot-Carrier at Constant Voltage Stress

The different devices were put under a HC stress for 10Ksec to measure the I_{dSat} degradation modulation due to density (i.e., heat) differences. The stress used was in mid-V_g mode to avoid negative bias temperature instability (NBTI) contribution in case of PFETs, (V_d=0.9V_{RO_STRESS}, V_g=0.6V_d, V_{RO_STRESS} is defined in Figure 5.6). Figure 5.9 shows the I_{dSat} degradation after HC stress (normalized to the 2Fin device).

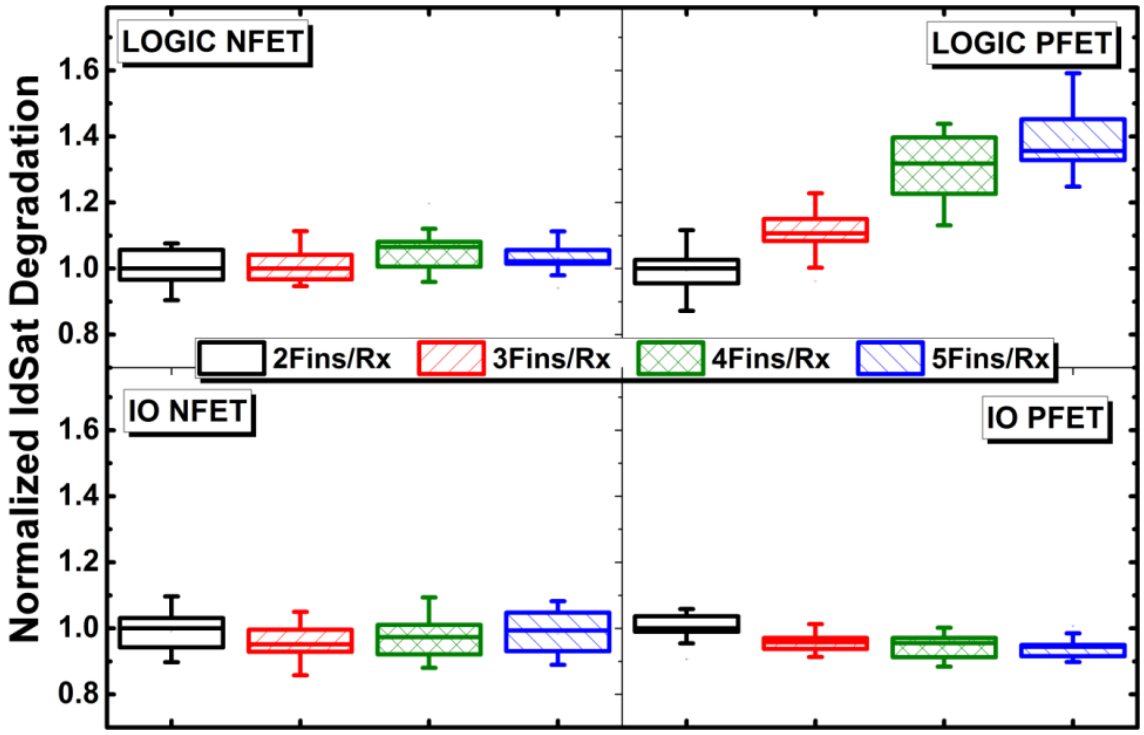


Figure 5.9 Hot carrier degradation for different device types/densities. Logic PFET hot-carrier degradation is modulated by self-heating (increasing with higher Fins/RX count).

The main observation is that significant HC degradation due to density dependence is observed only in logic PFET devices. This is due to the HC activation energy being low for logic NFET and IO devices (Figure 5.10) which results in similar degradation at different levels of SH. In the contrary, logic PFETs have a higher temperature acceleration (Ea~0.13eV) which explains the 35% increase in degradation for the measured densities.

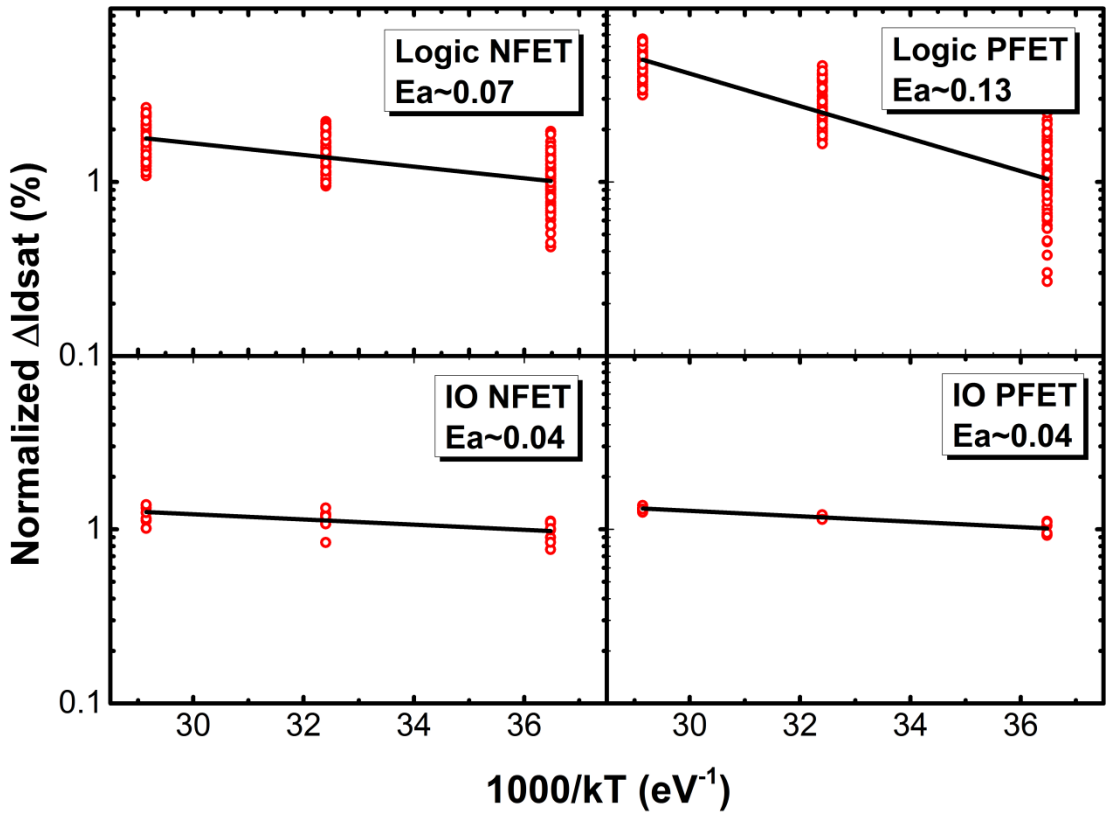


Figure 5.10 Hot carrier degradation as function of temperature showing the Arrhenius temperature acceleration of HC. The activation energy is extremely small except for logic PFET.

Subsequently, a series of DC hot-carrier tests was applied at different bias conditions ($V_g=V_{g1}=V_{g2}$, $V_{d1}=0.8V_{RO\_STRESS}$ and $V_{d2}=0.7V_{RO\_STRESS}$, where V_{RO_STRESS} is defined in Figure 5.6) and different ambient temperatures to examine the extent of SH impact on HC at moderate stress conditions. Figure 5.11 shows the measured HC degradation for all different conditions (open square symbols). The first observation is that the HC variability due to self-heating is greatly reduced at moderate stress because of the low self-heating at these conditions. Hence, it is important to use moderate acceleration when evaluating hot carrier degradation and extracting hot carrier model parameters, which this work recommends doing in order to avoid self-heating effects.

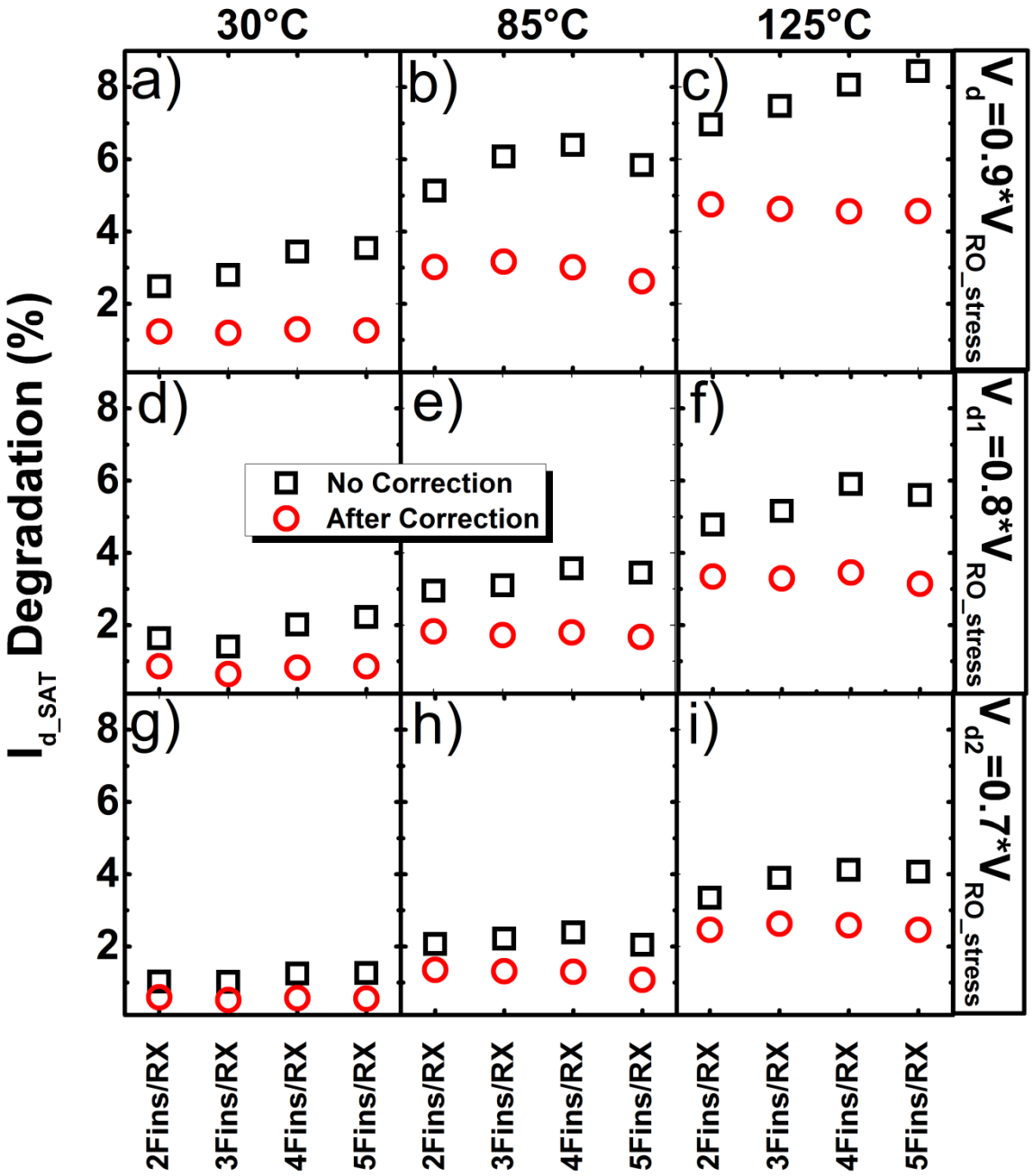


Figure 5.11 Logic PFET Hot carrier degradation at different acceleration levels before and after correction. The difference in degradation at extreme condition (c) is eliminated at moderate stress (g, h, i). The need for a correction is unnecessary at moderate acceleration.

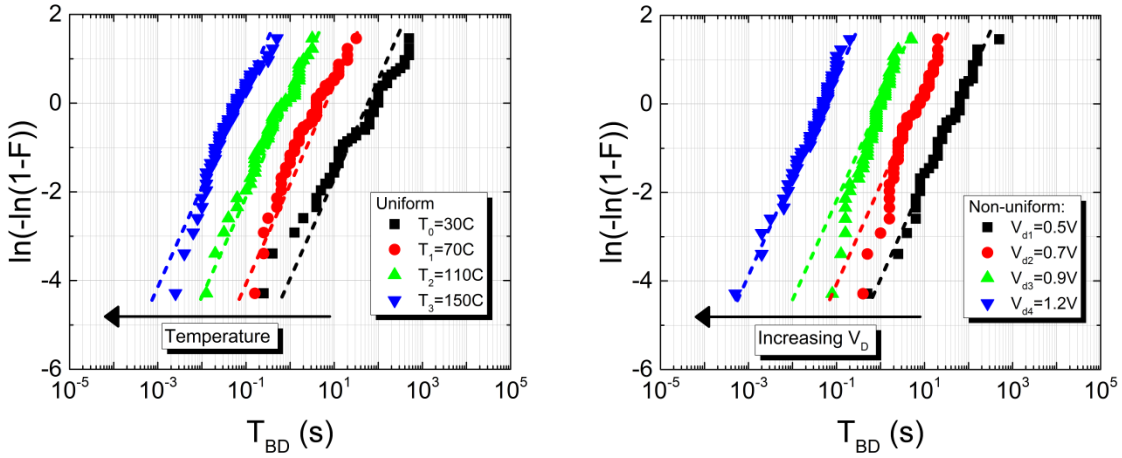
Additionally, because of the varying SH effects at different stress levels, the measured activation energy is slightly dependent on the density and bias being used (measured E_A values ranged between 0.1eV and 0.15eV).

Next, the correction method explained in [51] was used to correct for the extra heat induced by self-heating at stress. For the correction, E_A=0.13eV was used which is the activation energy of the 2 Fin device at the lowest stress condition (V_{d2}, from Figure 5.11). This is to ensure that the activation energy used in the correction is the least affected by self-heating. The open circles in Figure 5.11 show the corrected degradation. Note that at the highest acceleration (Figure 5.11c) the self-heating impact is greatly reduced after correction. However, at moderate acceleration, the correction is unnecessary since the self-heating impact is minimal (Figure 5.11g-i).

5.3.3 Self-Heating Effect on Uniform and Non-uniform TDDB at Constant Voltage Stress

Non-uniform TDDB is not a concern for standard logic circuits because the stress condition is only present during transients, which is a small portion of the operation time and thus translates to small fraction of overall self-heating. However, in analog applications, where the devices are in conduction mode for a substantial portion of the operating time, the self-heating effect should be accounted, for proper lifetime projections, which is why non-uniform TDDB will be assessed in this section.

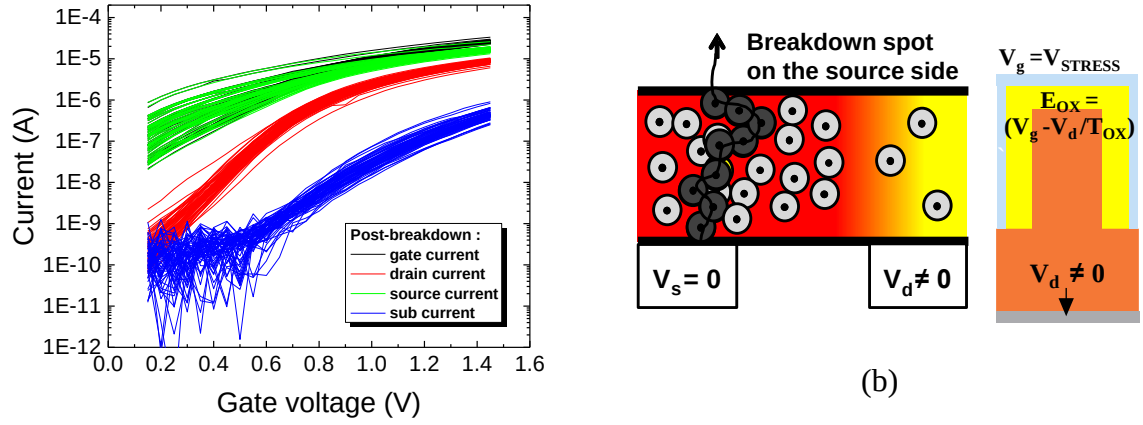
Figure 5.12a presents cumulative failure distributions at same gate stress conditions for uniform TDDB at different chuck temperatures, which can be compared to non-uniform stress (Figure 5.12b) at room temperature but different drain voltages (V_d).



(a) (b)

Figure 5.12 Failure distributions at V_g = 2.3V for different testing temperatures. TDDB lifetime decreases with increasing chuck temperatures (a). Failure distributions at V_g = 2.3V for different drain voltages. TDDB lifetime decreases with increasing V_d (b).

First observation from Figure 5.12 is the decreasing failure times with increased chuck temperatures or V_d conditions. Moreover, no significant change in Weibull slopes is observed, which indicates the breakdown mechanism is the same for uniform and non-uniform stress. Figure 5.13a shows the non-uniform post breakdown characteristic.

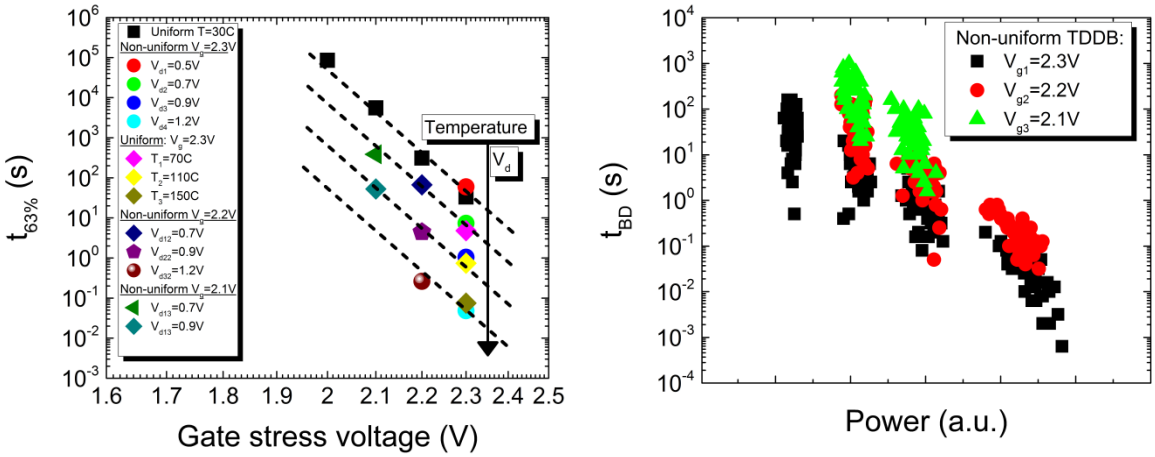


(a) (b)

Figure 5.13 Post stress non-uniform TDDB characteristic. At low V_g the post stress leakage flows entirely into the source side where the breakdown spot is located (a). Representation of field distribution in non-uniform stress, where lower field is observed on the drain side explaining the reason for post stress characteristic observation (b).

The post breakdown characteristic for non-uniform TDDB (Figure 5.13a) indicates that the location of the breakdown spot is located on the source side, where higher field is present as opposed to the lower field on the drain side due to applied bias. The field reduction on the drain side also reduces the total effective gate area under stress, which is expected to increase the characteristic lifetime as it competes with the reduction due to self-heating.

Figure 5.14a summarizes the test conditions used in uniform and non-uniform TDDB, of which the non-uniform case is compared to a power (self-heating) dissipation as depicted in Figure 5.14b.



(a) (b)

Figure 5.14 Voltage acceleration for combined stress conditions under uniform and non-uniform stress (a). Non-uniform lifetime correlation to power dissipated. Expected decrease in life time is observed at elevated power conditions (b).

Excellent voltage acceleration is observed for both uniform and non-uniform TDDB shown in Figure 5.14. Furthermore, for the same gate voltage, the lifetime reduces in a similar fashion by increasing the stress temperature, or by increasing V_d.

5.3.4 Self-Heating Impact on Ring Oscillator Reliability

Finally, the self-heating effect on ring-oscillators was examined with different densities. Note that the RO degradation is a combination of bias temperature instability (BTI) and HC degradation in both NFETs and PFETs [13, 33]. Thus, the only mechanism affected by self-heating (logic PFET hot carrier) only accounts for a fraction of the total RO degradation. Although in Figure 5.6 and Figure 5.7 it was shown that the RO heating is modulated by density, Figure 5.15 shows that the RO degradation at highly accelerated stress (V_{RO_STRESS}) does not show any density (i.e. heat) dependence. This is the confirmation this work sought to verify that self-heating effects on hot carrier variability at DC levels are not a concern in standard cell logic circuits.

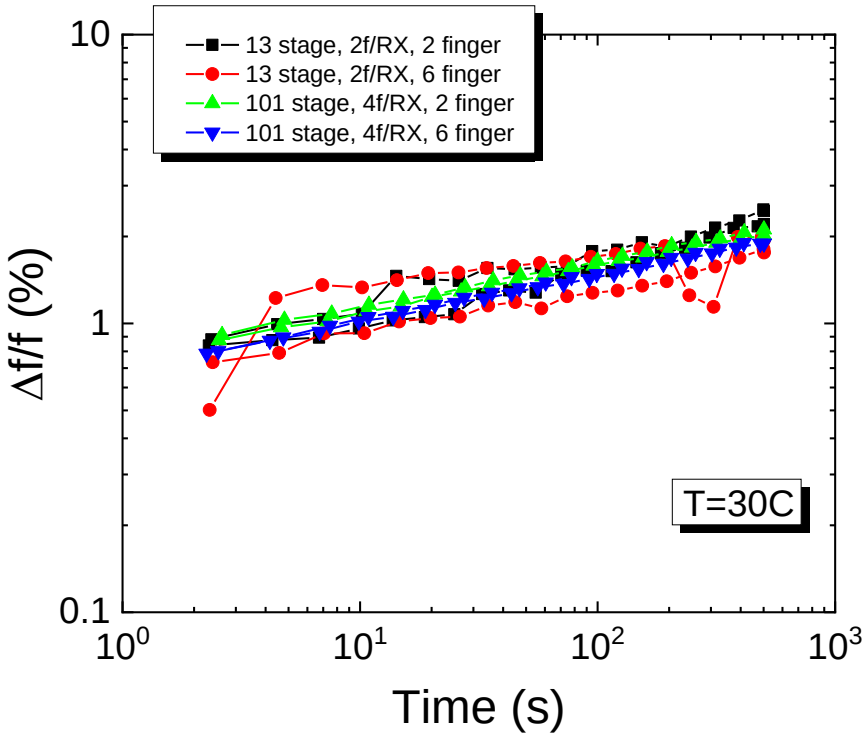


Figure 5.15 Ring-Oscillator degradation showing no impact of density or heating. The SH effects on HC observed in DC are not observed in standard cell logic circuits.

5.4 Summary

The influence of self-heating effects on hot carrier and TDDB degradation was examined in this chapter. It was shown that the hot carrier degradation variability due to self-heating effects is only a concern for logic PFET at extreme DC conditions and therefore moderate acceleration is recommended while evaluating hot carrier. Non-uniform TDDB demonstrated a reduction in device lifetime with self-heating conditions present. Furthermore, this chapter also verified that self-heating effects did not impact ring-oscillator degradation and should therefore not be overstated as a risk for standard cell logic circuits in bulk FinFET technology. However, these effects need to be further investigated for special circuits where conduction and power are significantly larger and temperatures of BEOL could reach unacceptable levels of as low as ~5°C.

CHAPTER 6

CONCLUSIONS AND FUTURE WORK

Work shared in this dissertation thus far, should give no doubt that self-heating exists in all integrated circuits and as technologies scale, power (heat) dissipation in these devices will only grow. Due to confinement effects and use of new materials in fabrication of state of the art electronics, thermal implications cannot be ignored. The elevated circuit temperatures were studied at different operating conditions giving insight to better self-heating characterization methods and ways of mitigating self-heating effects in reliability testing. This chapter draws conclusions on the learning and list areas of work which still need further research and improvement.

6.1 Conclusions

The main question this dissertation answered is what impact does self-heating have on device performance and reliability. Before addressing this question, first, problem objectives were stated and physics governing the source of heat and its dissipation in a semiconductor circuit well defined. The occurrence of self-heating was described in two different operating regimes; DC and AC as the former defines the condition device sees during reliability testing at constant voltage stress and latter is a condition standard logic circuit sees in switching mode. The review of state of the art in self-heating research has defined the areas still unexplored which this dissertation addressed to ultimately push the self-heating research forward.

The first major contribution of this dissertation was the design of improved self-heating structures. Many thermometry circuit devices previously developed capture the

heat dissipated in the channel, either locally or by an adjacent device. The improvement was implemented into the adjacent sensing circuits by placing grounded isolation gates between heater and sensor, which minimized the heater transistor currents mixing in with the sense currents of the sensor. The results from adjacent heat sensing techniques matched very well for type I-III sensors. Furthermore, the local sensing technique (R_G sensor) showed to measure heat more effectively, owing this to its close proximity to heat source. The concept of heat additivity was confirmed through measurement highlighting the fact that not only local heat, but also surrounding heat can contribute to the total effective heat, which is the cause of local chip hot spot regions.

The next contribution of this work was establishing an error bar of self-heating measurements, which based on the hardware used, a ~±0.5°C error can be achieved. The sensor devices showed reliable measurement capability which was verified with temperature cycling, however type III sensor can sustain damage during measurement, which will be discussed in the future work Section 6.2.1 with recommendation on how to fix this random occurrence.

By means of TCAD thermal simulations, this dissertation has added a key contribution in resolving temperature gradients that arise between transistor hotspots and the location of the sensor. This has provided a correction factor of ~3.3x for adjacent measurement results type II sensor (pn junction sensor). Therefore, temperature measured by type II sensor in reality is ~3.7x higher at the hot spot region of the transistor channel.

Based on the measurements and TCAD thermal modeling conducted in this dissertation, the level of self-heating for SOI FinFET technology can be expected to be ~5x higher compared to bulk FinFET. However, this factor may vary depending on the

choice of the buried oxide thickness used. Based on the SOI FinFET technology evaluated here, it has been shown that more lateral and upward heat spreading can occur compared to bulk FinFET technology, which is expected as the heat is limited by the buried oxide. This also suggests that SOI FinFET technology can experience more degradation due to self-heating effects in the FEOL devices as well as the BEOL metal stack.

This dissertation has also contributed to the evaluation of layout density impact on self-heating. Based on a study of bulk FinFET technology it has been established that thermal levels can increase by 2x going from 2 to 5 fins per active region RX and by 1.25x going from 5 to 20 fins per RX. The observation at 20 fins per RX is showing signs of thermal saturation because each chip location is only affected by circuitry within a radial distance. Radial lateral heat can reach as far as ~1µm in bulk FinFET and ~1.5µm for SOI FinFET technology based on experimental study conducted in this dissertation. This was an important learning which was applied to the next steps of this dissertation. A major contribution of this dissertation was the observation of ambient temperature impact on self-heating characterization. For the first time through measurement, it was shown that by varying the ambient temperature between -40 to 175°C thermal resistance of 20 fin per active region RX NFET and PFET devices can increase by as much as 70% and 45% respectively. This observation was proven by variation of the chuck temperature as well as adjacent heater transistors themselves. The results show that the Si fin has a more dominant effect in heat transport and its varying thermal conductivity should be accounted for, especially for high temperature applications where thermal response may be underestimated.

The impact of self-heating on device performance and reliability was studied in Chapter 5. Because self-heating occurs both at constant voltage conditions and switching conditions, accelerated testing for DC hot carrier degradation and in ring-oscillators AC performance degradation was studied. It was determined that self-heating effects only affects logic PFET hot carrier degradation at extreme stress because of its higher Arrhenius activation energy. Further study on DC hot carrier has shown that stressing devices at moderate conditions helps to mitigate the effects of self-heating. Therefore, this work recommends using moderate stress conditions in DC hot carrier testing to diminish self-heating impact. Furthermore, self-heating effects can be further reduced in reliability testing by implementing less dense test structures by use of multiple active regions RX. This work has also shown that self-heating effects did not impact ring-oscillator degradation and therefore should not be a risk for standard logic circuits. However, high density layout circuits should be further analyzed as its self-heating may impact upper metal lines and accelerate the effects of electron migration.

Lastly, the TDDB breakdown mechanism between uniform and non-uniform TDDB was shown to be the same. The introduction of heat via thermal chuck or devices themselves did not change the Weibull or voltage acceleration observations.

6.2 Future Work

6.2.1 Type III (R_G) Sensor Test Improvement

The temperature sensors used in this dissertation have provided reliable data from which key conclusions on the different experiments were made. However, type III sensor, when tested on other technology (FDSOI), randomly failed after device heating cycles. The

reason for the gate sensor failures was a mystery until the end of this dissertation closure, however a good hypothesis was established giving grounds for future work. Type III sensor uses the transistor metal gate to measure its thermally sensitive parameter R_G. At higher gate bias conditions, it was found that the gate resistor had open fails after sensing measurements. The reason for these fails is associated with the fact the two SMUs needed for the measurement cannot apply bias simultaneously to both ends of the R_G resistor, causing the sensor to be exposed to high electric fields for brief periods of time until both SMUs are turned on. The failure of the sensor occurred at high power dissipations in the heater structure due to higher biasing on the gate metal, which performs an IV sweep simultaneously. The sweep has to be centered on the high bias in order to bias the channel and make sensor measurement at the same time. This concept is illustrated in Figure 6.1 where sweep is applied to SMU1, keeping SMU2 fixed.

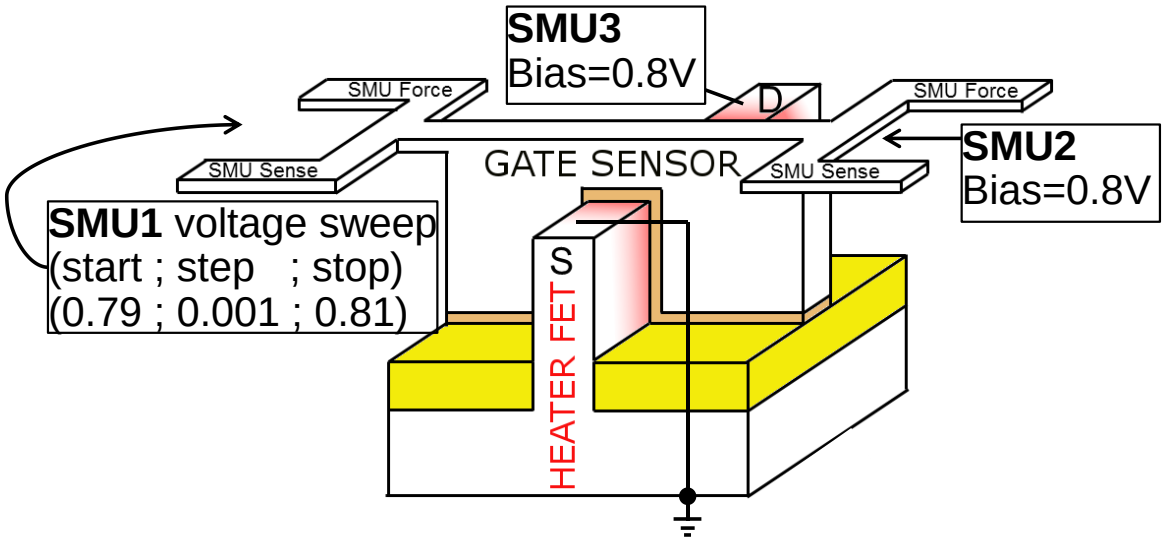


Figure 6.1 Illustrative figure showing a case when type III sensor (R_G) can fail during heat dissipation in the channel while taking sensor measurement via sweep across R_G.

It is clear from Figure 6.1 that the SMU1, IV sweep applies a maximum of 10mV at maximum across the gate sensor resistor while measuring the current. This is the case when both SMUs are ON at the same time. However, initially at start, using Agilent B1500A it is not possible to turn both SMUs simultaneously. In actuality, the instrument first turns on SMU1 followed by SMU2. Due to this instrument limitation, there is a fraction of time, SMU2 is at 0V bias before being turned ON and the sensor experiences a voltage potential difference of up to 0.81V. This high field across the small resistor R_G, causes it to fail (open) due to large currents flowing through it. Failure of the sensor can be prevented by eliminating the high voltage field by progressively stepping up to the desired bias in an alternating fashion (step on SMU1 followed by step on SMU2). The instrument options and settings would need to be reviewed if this could be achieved, which is planned for the future work.

6.2.2 Self-Heating Impact on Back-End-Of-Line Interconnects

Self-heating impact on 1st metal interconnect line (M1), due to high density ring-oscillator operation is not significant at nominal operating voltage conditions as reported in Chapter 5 of this dissertation. Temperature of <2.5°C was measured at M1 at nominal voltage conditions. This is not an alarming level for reliability of back-end-of-line interconnects in eletromigration degradation mechanism for FinFET technology used here. However, more dense circuit applications such as clock buffers still need to be studied for its impact of self-heating on upper metal lines. Temperature levels of ≥5°C due to FEOL self-heating at M1 lines can impact the circuit's reliable operation due to electromigration, which is a highly sensitive degradation mechanism at elevated

temperatures. Therefore, testing denser, worst-case scenarios of ring-oscillators are recommended to fully model the impact of self-heating at the upper metal lines. This is particularly critical for technologies such as SOI FinFETs where heat generated by front-end-of-line devices is being forced through the upper metal lines due to the buried oxide as discussed in Section 3.7, where self-heating impact is 5x higher compared to bulk FinFET technology.

6.2.3 Persistent Self-Heating

Study of the thermal time constant and the persistence of self-heating can unlock even greater understanding of its potential effects on device reliability. Further verification of the thermal time constant through measurement still needs verification. Due to very low thermal time constants in Si (on the order of nanoseconds), current measurement equipment cannot capture this effect by means of structures described in Chapter 3 and further development in this area is needed. Heat persistence can build up local hot spots which poses a reliability concerns for back-end-of-line metallization stack.

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