ABSTRACT

AMORPHOUS METAL OXIDE SEMICONDUCTOR THIN FILM TRANSISTORS FOR PRINTED ELECTRONICS

by
Mustafa Mohammad Yousef

There is an acute market need for solution-processable semiconductor inks that can form the essential components of the printed analog and digital circuits. Currently, the industry is migrating beyond simply printing conductive metals for interconnects and embracing higher integration by printing transistors directly on the same substrate. This thesis focuses on investigating solution-processed amorphous indium gallium zinc oxide (IGZO) as a semiconducting channel layer of a field-effect transistor to enable low-cost, large-area printed electronics that are physically flexible and optically transparent. Specifically, we aim to achieve field-effect mobility exceeding 1 cm^2/Vs, to overcome the limits faced in existing amorphous silicon and emerging organic transistor technologies, through optimizing IGZO ink and studying various thin-film processing conditions. Device approach using solution-processed, high-K aluminum oxide dielectric layer has also been examined in this study. In addition, the effect of low-temperature UV-assisted annealing has been studied which allow the fabrication to be compatible with plastic substrates.

AMORPHOUS METAL OXIDE SEMICONDUCTOR THIN FILM TRANSISTORS FOR PRINTED ELECTRONICS

by
Mustafa Mohammad Yousef

A Thesis
Submitted to the Faculty of
New Jersey Institute of Technology
in Partial Fulfillment of the Requirements for the Degree of
Master of Science in Electrical Engineering

Department of Electrical and Computer Engineering

December 2018

APPROVAL PAGE

AMORPHOUS METAL OXIDE SEMICONDUCTOR THIN FILM TRANSISTORS FOR PRINTED ELECTRONICS

Mustafa Mohammad Yousef

Dr. Dong-Kyun Ko, Thesis Advisor — Date
Assistant Professor of Electrical and Computer Engineering, NJIT

Dr. Haim Grebel, Committee Member — Date
Professor of Electrical and Computer Engineering, NJIT

Dr. Hieu Pham Trung Nguyen, Committee Member — Date
Assistant Professor of Electrical and Computer Engineering, NJIT

BIOGRAPHICAL SKETCH

Author: Mustafa Mohammad Yousef

Degree: Master of Science

Date: December 2018

Date of Birth: November 18, 1993

Place of Birth: Amman, Jordan

Undergraduate and Graduate Education:

- Master of Science in Electrical Engineering,
  New Jersey Institute of Technology, Newark, NJ, 2018

- Bachelor of Science in Mechanical Engineering,
  American University of Sharjah, Sharjah, United Arab Emirates, 2016

Major: Electrical Engineering

الى عائلتي و احبائي
To my family and beloved ones

ACKNOWLEDGMENT

I would like first to thank my thesis advisor Dr. Dong Kyun Ko for accepting me and giving me the opportunity to join his team. His support and help throughout my research were very valuable. He was available to offer the help needed whenever I faced any difficulties.

I also would like to thank the committee members Dr. Grebel and Dr. Heiu for the willingness in helping me while conducting my research. Furthermore, a special thanks to NJIT for accepting me into their electrical engineering Master of Science program and for providing the required high-quality facilities. NJIT maintains a suitable and diligent research environment which allowed me to break out from my shell to give my best in pursuing my degree.

Moreover, I would like to acknowledge my lab peer Shihab for assisting me in the lab work and for giving his opinion and thoughts in this project which led to successful conclusions.

Finally, I would like to convey my sincere gratitude to my family members for giving me their support and guidance and for inspiring me to continue my education.

TABLE OF CONTENTS

Chapter		Page
1	INTRODUCTION ……...	1
	1.1 Motivation …….....	1
2	BACKGROUND …….	3
	2.1 MOSFET …….	3
	2.1.1 MOS Capacitor ……	3
	2.1.2 Operation Principals of MOSFET ……...	9
	2.2 Thin Film Transistors …….....	16
	2.3 Amorphous Oxide Semiconductors ……	18
	2.3.1 Amorphous and Crystalline Forms …….	18
	2.3.2 IGZO and AOS Physics ……..	19
	2.4 High-k Dielectric Material ……..	22
	2.5 Spin Coating Deposition Method ……	23
	2.6 UV Assisted Annealing ……...	25
	2.7 IGZO Applications and Current State …….	26
3	PROCEDURE, RESULTS AND DISCUSSION ……	28
	3.1 Substrate Cleaning……...	28
	3.2 Mask Preparation ……	28
	3.3 IGZO Solution Synthesis ……	29
	3.4 High-Temperature Processed Devices ……	30
	3.4.1 Procedure …….	30

TABLE OF CONTENTS
(Continued)

Chapter **Page**

3.4.2 Results and Discussion …… 32

3.5 Low-Temperature UV-assisted annealing Devices …… 36

3.5.1 Procedure ……. 37

3.5.2 Results and Discussion …… 37

3.6 Improving UV assisted FET devices characteristics by modifying IGZO composition …….. 39

3.6.1 Procedure ……. 40

3.6.2 Results and Discussion …… 40

3.7 Additional Attempts …… 43

3.7.1 Using High-Temperature Annealing ……... 43

3.7.2 Using Low-Temperature UV-Assisted Annealing …….. 46

3.7.3 Using Different IGZO Composition ……... 46

3.8 Conclusion …….. 47

3.9 Scope of Future Work ……. 48

REFERENCES …….. 49

LIST OF TABLES

Table		Page
3.1	Electrical Parameters of Si/SiO_2 and Glass Devices …….	35
3.2	Electrical Parameters of Low Temperature Processed Glass Device and the Device Fabricated Using Separate UV Exposure and Annealing Process ……...	38
3.3	Electrical Parameters of 6:1:3, 6:2:3 and 8:2:3 IGZO Devices …….	42

LIST OF FIGURES

Figure		Page
1.1	Sharp's Production timeline comparing the properties of IGZO, a-Si and Poly-Si …….....	2
2.1	MOS capacitor structure which shows the arrangement of each semiconductor, insulator and metal layers …….....	3
2.2	Energy band diagram of a p-type MOS assuming a flat band with zero applied voltage ……...	4
2.3	Energy band diagram under accumulation mode of (a) n-type MOS capacitor (b) p-type MOS capacitor ……...	5
2.4	Energy band diagram under depletion mode of (a) n-type MOS capacitor (b) p-type MOS capacitor…….....	5
2.5	Energy band diagram under inversion mode of (a) n-type MOS capacitor (b) p-type MOS capacitor ……...	6
2.6	Capacitance VS voltage indicating (a) both high and low-frequency total capacitance for a p-type MOS (b) total capacitance at each operating mode of a p-type MOS ……...	9
2.7	MOSFET structure illustrating the arrangement of each component …....	10
2.8	Energy band diagram between the source/substrate/drain in n-channel MOSFET when zero voltage is applied …….....	11
2.9	Energy band diagram between the source/substrate/drain in n-channel MOSFET when (a) positive voltage is applied to the gate and (b) negative voltage is applied to the gate ……...	12
2.10	MOSFET structure illustrating (a) the creation of both the linear and (b) saturation regimes and shows (c) the pinch-off point that leads to drain current saturation ……...	13
2.11	Transfer characteristics illustrating the extraction of threshold voltage, saturation transconductance from (a) square root of I_D vs V_G and ON/ OFF currents and linear transconductance from (b) I_D vs V_G …….....	16
2.12	Output characteristics of n-channel MOSFET ……...	16

LIST OF FIGURES
(Continued)

Figure		Page
2.13	Demonstration showing (a) staggered bottom gate (b) staggered top gate (c) coplanar top gate and (d) coplanar bottom gate …….....	17
2.14	**(**a) Amorphous atomic structure (b) crystalline atomic structure ……	19
2.15	Comparison of Si and IGZO crystalline and amorphous atomic structures ……....	20
2.16	(a) Crystallinity of respective metal oxide semiconductor and (b) their corresponding hall mobility ……	22
2.17	Energy gap VS static dielectric constant for different Dielectric materials ……....	23
2.18	Solution processing method for depositing a semiconductor using spin coating after solution synthesis stage ……..	24
2.19	Schemes showing condensation and densification mechanisms of metal-oxide precursors by DUV irradiation. The blue cylinders donate the illumination from the mercury lamp ……...	25
2.20	Electrical parameters of different TFTs annealed for different duration ….	26
2.21	Brightness fluctuation of (a) AOS and (b) a-Si ……...	27
3.1	(a) Source and drain mask, (b) gate mask used for device fabrication, (c) n^+-Si/SiO_2 device structure and (d) glass/Al_2O_3 device structure ……	29
3.2	AFM Step Height (Thickness) Characterization of IGZO film …….....	31
3.3	(a) Transfer characteristics, (b) mobility calculations and (c) output characteristics of Si/SiO_2 device …….....	32
3.4	Log plot that compares drain current to leakage current of glass/Cr/Al_2O_3 device ……	33
3.5	(a) Transfer characteristics, (b) mobility calculations and (c) output characteristics of glass/Al_2O_3 device ……....	34
3.6	(a) SEM image showing the spread of pin holes on Al_2O_3 surface and (b) a comparison between the leakage current of the glass and Si/SiO_2 device ……....	36

LIST OF FIGURES
(Continued)

Figure		Page
3.7	(a) Transfer characteristics and (b) mobility calculations of the low temperature processed glass device ……	38
3.8	Transfer characteristics of 6:1:3 and 6:2:3 IGZO devices …….....	41
3.9	(a) Transfer characteristics of 6:2:3 and 8:2:3 IGZO devices, (b) mobility calculations and (c) output characteristics of the 8:2:3 IGZO device ……....	42
3.10	Al2O3 film when low-temperature annealing and low annealing period are targeted …….....	43
3.11	Non-uniform IGZO film is observed using deionized water as a solvent. Non-uniform film is observed …….....	44
3.12	Optical image showing (a) one layer IGZO film and (b) two-layer film …	45
3.13	SEM picture showing high purity Al2O3 film surface when deposited on SiO2 dielectric layer …….....	45
3.14	Optical image of Al_2O_3 film deposited onto Cr gate electrode after UV-assisted annealing was performed in (a) air and (b) N_2 environment …....	46
3.15	Electrical characteristics comparing devices with simultaneous and separate annealing processes where (a) is transfer characteristic, (b) transfer characteristics in logarithmic scale and (c) is the square root of I_D vs V_G used for mobility estimations ……...	47

CHAPTER 1

INTRODUCTION

1.1 Motivation

Amorphous metal oxide semiconductors (AMOS) are a promising class of materials that have made rapid progress in thin-film transistors (TFTs) for active matrix displays,[1-6] challenging silicon not only in traditional applications but opening the door to new and disruptive areas such as transparent,[7,8] flexible,[9-11] wearable,[12] and paper electronics.[13] Ternary metal oxides containing indium, gallium, and zinc (.i.e. IGZO) have been of particular interest due to their favorable electron mobilities (> 10 cm^2/Vs), ease of large-area manufacturing and excellent operational stability.[1, 14, 15] Interest in this new class of transparent semiconductor is heightened by the demonstrations[16] of 37'' liquid crystal displays (LCDs) and 19'' flexible active matrix organic light emitting diode (AMOLED) displays with global market projected to exceed $85 billion by 2025 in display application alone.[17] Figure1.1 summarizes the advantages of AMOS over amorphous silicon and poly-Si. AMOS is superior to traditional a-Si due to large spatial overlap between highly delocalized s-orbital states of metal ions in AMOS that give rise to these high electron mobilities which do not depend on the degree of film disorder[18, 19] and can reach values of corresponding crystalline counterparts.[20,21] Also, AMOS is preferable over poly-Si because they are size flexible[16]. They enable the fabrication of a large area substrate, whereas, the latter is polycrystalline that has grain boundaries that prevent maintaining the same electrical characteristics of large area substrates.[22, 23]

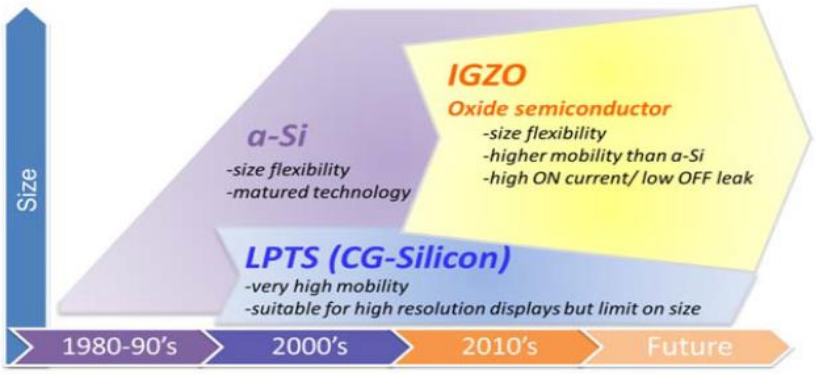

Figure 1.1 Sharp's Production timeline comparing the properties of IGZO, a-Si and Poly-Si.

Source: T. Matsuo, S. Mori, A. Ban and A. Imaya, "8.3:Invited Paper: Advantages of IGZO Oxide Semiconductor", *SID Symposium Digest of Technical Papers*, vol. 45, no. 1, pp. 83-86, 2014.

To date, IGZO fabrication processes use physical vapor deposition (PVD) processes such as radio frequency sputtering and pulsed laser deposition to deposit IGZO thin films.[15, 25-27] However, solution processing methods enable cheap and easy deposition of the material. Inkjet printing, for example, is one of the methods that can be used for this purpose. In addition, IGZO can be processed at room temperatures using UV assisted annealing thus opening the door for transparent and flexible electronics as the processing temperature can be dropped down the transition point of polymers and glass. In this study, building on the platform of metal-salt chemistry,[28-30] we will synthesize IGZO ink with various elemental compositions and investigate various thin-film processing methods. Thin-film transistors (TFTs) will be fabricated and device characterization will be carried which will be focused on achieving field-effect mobility exceeding 1 cm^2/Vs.

CHAPTER 2

BACKGROUND

2.1 MOSFET

Metal Oxide Semiconductor Thin Film Transistor (MOSFET) is primarily thought of as MOS capacitor and a BJT transistor combined. The MOS capacitor in the MOSFET is the essential component that determines the characteristics of the transistor. Thus, to understand the fundamental operating principle of the MOSFET, it is essential to understand how this capacitor works, what it consists of, and how it is related to the MOSFET operation.

2.1.1 MOS Capacitor

Metal Oxide Semiconductor (MOS) capacitor is a capacitor that manipulates charges in the semiconductor by applying a voltage. It usually operates under three modes which are accumulation, depletion, and inversion. It is clear from its name that it consists of three layers. The first layer is a metal, the second layer is an oxide layer that acts as a dielectric layer (an insulating layer), and the third is a semiconductor as shown in Figure 2.1.

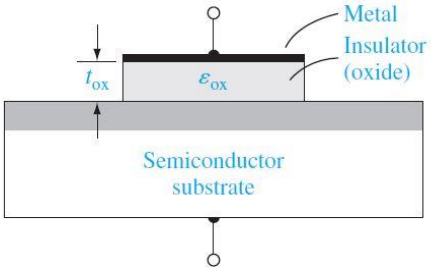

Figure 2.1 MOS capacitor structure which shows the arrangement of each semiconductor, insulator and metal layers.

Source: D. Neamen, *Semiconductor physics and devices*. New York: McGraw-Hill, 2012.

Figure 2.2 shows the equilibrium energy band diagram of ideal MOS capacitor constructed from p-type semiconductor, assuming that the metal, dielectric and semiconductor layers' work functions are all in line to form a flat band with no applied bias and no charges present in the oxide layer.

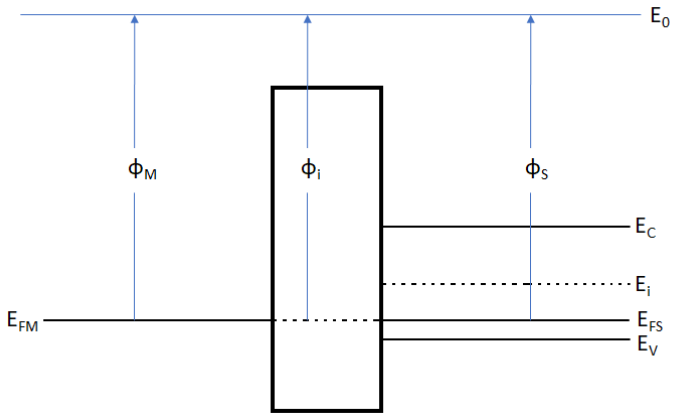

Figure 2.2 Energy band diagram of a p-type semiconductor MOS assuming a flat band with zero applied voltage. E_c represents conduction band, E_v represents the valence band, E_i the intrinsic level, E_{FS} the Fermi level of the semiconductor, E_{FM} the Fermi level of the metal and ϕ_M, ϕ_i, ϕ_S are the work functions of the metal, insulator and semiconductor respectively.

Furthermore, the energy band diagram will change as a sequence to the change in the applied bias. This change determines the modes at which the MOS capacitor is operating. The three modes of operation are explained in detail in the following section.

Accumulation:

If the semiconductor side is grounded and a negative bias is applied to the metal (forward-bias), the Fermi-energy level of the metal shifts up with respect to the p-type semiconductor. Also, a band bending in the semiconductor near the dielectric/semiconductor interface occurs. In this case, the charges start accumulating at the dielectric/semiconductor interface. In other words, the negative applied voltage on the metal side attracts positively charged carriers (holes) on the semiconductor side, as shown

in Figure 2.3(b). The opposite case for MOS based on n-type semiconductor (electron accumulation) is shown in Figure 2.3(a).

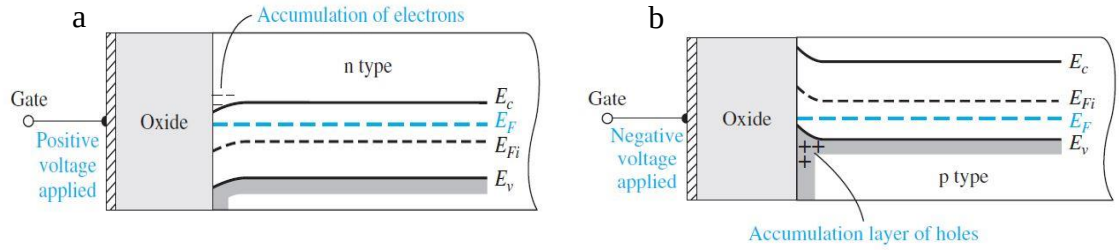

Figure 2.3 Energy band diagram under accumulation mode of (a) n-type MOS capacitor (b) p-type MOS capacitor. E_c represents conduction band, E_v represents the valence band, E_{Fi} the intrinsic level, E_F the fermi level of the semiconductor.

Source: D. Neamen, *Semiconductor physics and devices*. New York: McGraw-Hill, 2012.

Depletion:

A depletion mode takes place when a positive bias (reverse bias) is applied to the metal while grounding the p-type semiconductor. In this case, the holes on the p-type semiconductor side will be repelled. Also, an increase in depletion width occurs due to the charge neutrality condition (number of positive charges on the metal side should be equal to the number of negative charges – i.e., ionized acceptors – of the p-type semiconductor). Figure 2.4 shows (a) n-type based semiconductor MOS and (b) p-type based semiconductor MOS.

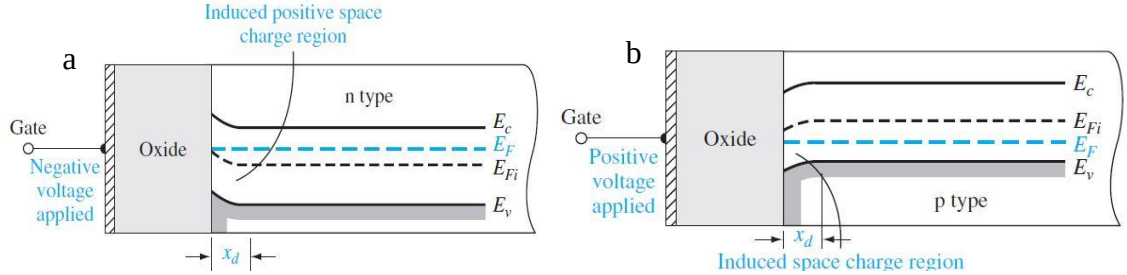

Figure 2.4 Energy band diagram under depletion mode of (a) n-type MOS capacitor (b) p-type MOS capacitor. E_c represents conduction band, E_v represents the valence band, E_{Fi} the intrinsic level, E_F the fermi level of the semiconductor.

Source: D. Neamen, *Semiconductor physics and devices*. New York: McGraw-Hill, 2012.

Inversion:

Inversion mode occurs when the reverse bias exceeds a certain threshold voltage. Exceeding the threshold voltage causes a deeper band bending in the semiconductor near the dielectric/semiconductor interface. The band bending is large enough such that the Fermi level rises above the intrinsic level, indicative of electron accumulation in p-type semiconductor (charge inversion), as shown in Figure 2.5(b). An opposing scenario occurs for MOS based on n-type semiconductor such the one shown in Figure 2.5(a). The onset of inversion occurs when $(E_F - E_i)_{interface} = (E_i - E_F)_{bulk}$, and the value of the reverse bias that creates this onset defines the threshold voltage. Also, the depletion width of the inversion mode is defined when the onset of inversion occurs, and it is higher than the depletion width in depletion mode because a higher reverse biased is applied.

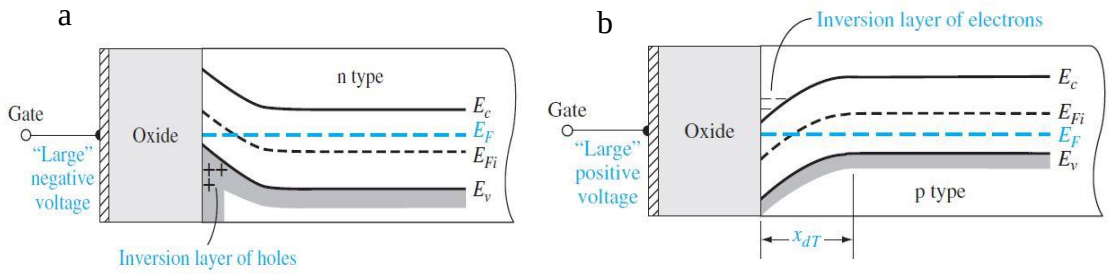

Figure 2.5 Energy band diagram under inversion mode of (a) n-type MOS capacitor (b) p-type MOS capacitor. E_c represents conduction band, E_v represents the valence band, E_{Fi} the intrinsic level, E_F the Fermi level of the semiconductor.

Source: D. Neamen, *Semiconductor physics and devices*. New York: McGraw-Hill, 2012.

Capacitance vs voltage characteristics is a powerful tool to study the operation of the MOS capacitor. There is a difference in the total capacitance of the MOS capacitor when it operates at different modes and different frequencies. The following explains how capacitance varies with respect to the operating mode:

1) Accumulation

Accumulation depends on attracting the majority carriers as previously mentioned and the carriers respond very quickly whether this mode is operated either at a low or high frequency. Thus, the capacitance does not change with a change in the frequency. The depletion region of the semiconductor is small since a forward bias is applied to reach this mode and accordingly the total capacitance of the MOS capacitor yields a high capacitance value. The capacitance can be calculated using the following equation where x_0 is oxide thickness, and the accumulation capacitance is equal to the oxide capacitance:

$$C_{Acc} = C_{ox} = \frac{\varepsilon_0 \varepsilon_{ox}}{x_0} * A \tag{2.3}$$

2) Depletion

This mode depends on repelling the majority carriers thus the carriers respond rapidly whether it is operating on a high or a low frequency. In this mode of operation, the depletion region capacitance is small, and the total capacitance varies with the varying depletion region width. The total capacitance can be estimated using the following equation:

$$\frac{1}{C_{Dep}} = \frac{1}{C_{ox}} + \frac{1}{C_s} \tag{2.4}$$

Where C_{ox} is identical to equation (2.3) and Cs is the semiconductor depletion region capacitance, and it is calculated using:

$$C_s = \frac{\varepsilon_0 \varepsilon_{ox}}{W} * A \tag{2.5}$$

W represents the depletion region width and can be calculated by the following equation where N is the dopant concentration:

$$W = [\frac{2\varepsilon_0 \varepsilon_{ox}}{qN} * \phi s]^{\frac{1}{2}} \tag{2.6}$$

3) Inversion

In Inversion mode, both majority and minority carriers contribute to creating a capacitance across the MOS structure. Electrons accumulated via inversion in the p-type semiconductor are minority carriers, and they give rise to C_{ox}. It is important to note that the total capacitance, in this case, varies depending on the frequency of the applied AC voltage. At low frequency both majority and minority carriers can follow up with the AC applied bias and the total capacitance is high and equal to the capacitance of the oxide layer. However, if a high frequency is applied, the minority carriers would not be able to follow up with the process because of their slow thermal generation process, and thus, the depletion region width oscillates around the maximum width (W_T) trying to maintain overall charge neutrality. The total capacitance at the inversion mode for high and low frequencies are summarized in the following two equations:

Low frequency: $C_{Inv} = C_{ox} = \frac{\varepsilon_0 \varepsilon_{ox}}{x_0} * A$ (2.7)

High frequency: $$\frac{1}{C_{Inv}} = \frac{1}{C_{ox}} + \frac{1}{C_s} \quad (2.8)$$

Figure 2.6(a) shows the capacitance vs voltage for both high and low AC frequencies of a p-type MOS capacitor. In addition, figure 2.6(b) summarize the total capacitance related to the three operating modes for p-type substrate MOS capacitor.

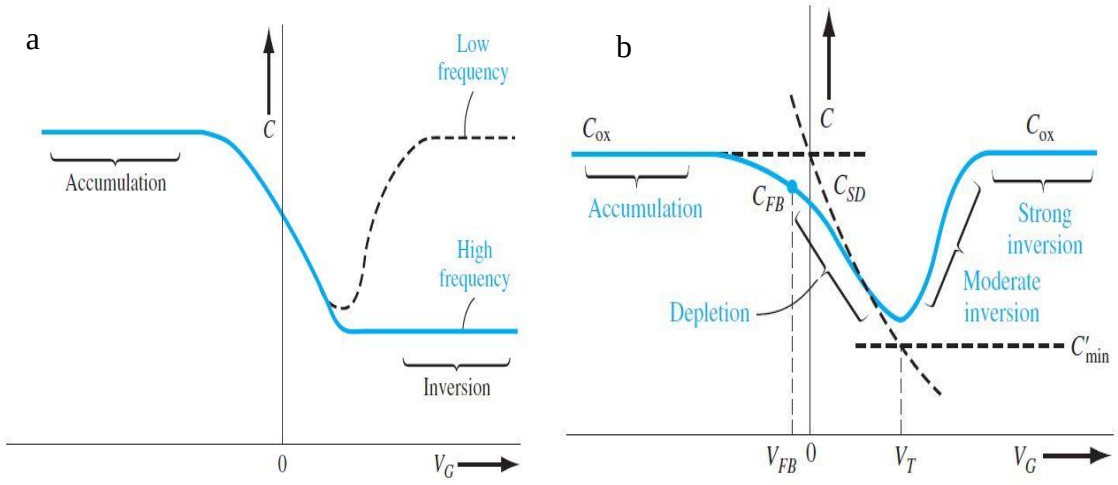

Figure 2.6 Capacitance vs voltage indicating (a) both high and low-frequency total capacitance for a p-type MOS (b) total capacitance at each operating mode of a p-type MOS.

Source: D. Neamen, *Semiconductor physics and devices*. New York: McGraw-Hill, 2012.

2.1.2 Operation Principals of MOSFET

The basic structure of a MOSFET includes a body, gate, dielectric layer, substrate (p-type or n-type), source and drain as depicted in Figure 2.7.

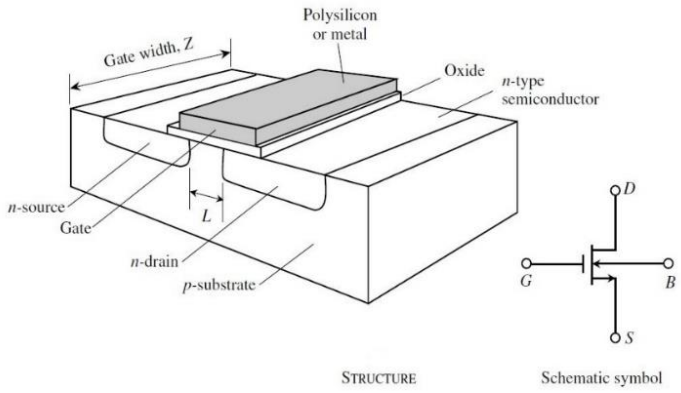

Figure 2.7 The basic structure of a MOSFET.

Source: D. Neamen, *Semiconductor physics and devices*. New York: McGraw-Hill, 2012.

MOSFET operates by grounding the source and biasing each of the drain and gate. By convention, the drain collects the charges coming from the grounded source, i.e., for n-channel MOSFET operation, the drain bias is positive. In an ideal case, the gate should not collect the channel current because the high insulating nature of the dielectric electrically separates the gate and source/drain. In practice, however, various defects in the oxides, such as pinholes, create a conductive path from gate to source/drain. The current in this conductive path is called the leakage current.

In the case of accumulation, a forward bias on the gate is applied. This creates a back to back n-p and p-n junctions at the source/substrate interface and substrate/drain interface. In other words, the MOSFET will be OFF no matter what voltage is applied to the drain because these back to back junctions will create two diodes such that one of them is forward biased and the other is reversed biased. Thus, the MOSFET is at OFF state.

If a reverse bias is applied to the gate but less than the threshold voltage, a depletion region is created within the MOS capacitor. Majority carriers are repelled leaving few

carriers at the semiconductor/dielectric interface. In this case, due to the highly resistive nature of the semiconductor channel, the MOSFET will stay at OFF state.

However, if a strong reverse bias is applied, an inversion will take place creating a conductive channel between the source and drain. Compared to the accumulation mode, this creates an n^+-n-n^+ conductive path for electrons to flow from source to drain. And the MOSFET turns ON.

It is instructive to understand the operation of MOSFET based on the energy band diagram. MOSFET consists of MOS capacitor to activate the channel and a BJT that allow the transport of carriers from source to drain. The BJT in n-channel MOSFET consists of n-type semiconductor source and drain and a p-type substrate. Figure 2.8 illustrates the energy band diagram between the source/substrate/drain in a MOSFET at no applied bias.

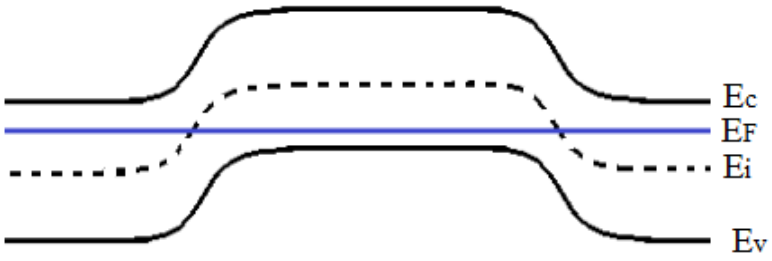

Figure 2.8 Energy band diagram between the source/substrate/drain in n-channel MOSFET when zero applied voltage**.** E_c represents conduction band, E_v represents the valence band, E_i the intrinsic level, E_F the Fermi level of the semiconductor.

When a positive bias is applied to the gate, the transistor turns ON since the potential barrier is reduced for majority carriers to transport from source to the channel and then from the channel to the drain as shown in Figure 2.9 (a). However, if a negative bias is applied to the gate, a larger barrier is formed preventing the majority carriers from transporting, and thus the MOSFET will stay at an OFF state as shown in Figure 2.9 (b).

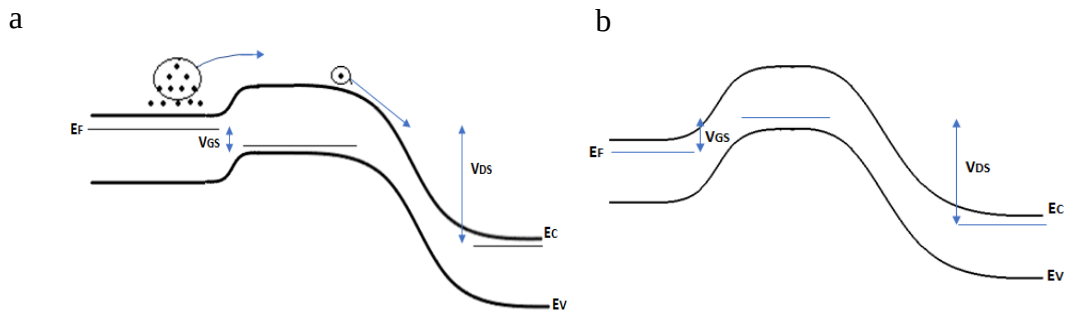

Figure 2.9 Energy band diagram between the source/substrate/drain in n-channel MOSFET when (a) positive voltage is applied to the gate and (b) negative voltage is applied to the gate**.** E_c represents conduction band, E_v represents the valence band, E_F the Fermi level of the semiconductor, V_{GS} is gate to source voltage and V_{DS} is drain to source voltage.

When inversion takes place, the channel acts as a simple resistor, and the source and drain are electrically connected allowing carriers to flow from one electrode to the other creating linear region current as in Figure 2.10 (a). The following equation relates current to voltage in the linear regime:

$$I_D = \frac{Z\mu_n C_{ox}}{L}\left[(V_G - V_T)V_D - \frac{{V_D}^2}{2}\right] \quad ; \quad 0 \le V_D \le V_{Dsat} \quad and \quad V_G \ge V_T \tag{2.9}$$

The applied drain voltage is said to be at a pinch-off voltage when it exceeds the applied gate voltage. A pinch-off in the channel occurs at this voltage because the gate to substrate potential becomes less than the threshold voltage where the active channel is eliminated at the far end next to the drain. In other words, the inversion charge density and the potential difference across the oxide are zero at that point thus the conductivity of the channel is reduced and as a result, the slop of the I_D vs V_D curve is reduced as well. This phenomenon leads the current to start saturating at a certain applied drain voltage. The stronger the drain voltage is applied while holding the gate voltage constant pushes this point further to the source side. In this case, the electrons transport from source to the zero-

charge density point and then they are swept by E-field to the drain as illustrated in Figure 2.10. The equation that represents this saturation regime is as follows:

$$I_D = I_{Dsat} = \frac{Z\mu_n C_{ox}}{2L}[(V_{GS} - V_T)^2] \quad ; \quad V_{Dsat} \leq V_{DS} \tag{2.10}$$

Where $$V_{DS(sat)} = V_{GS} - V_T \tag{2.11}$$

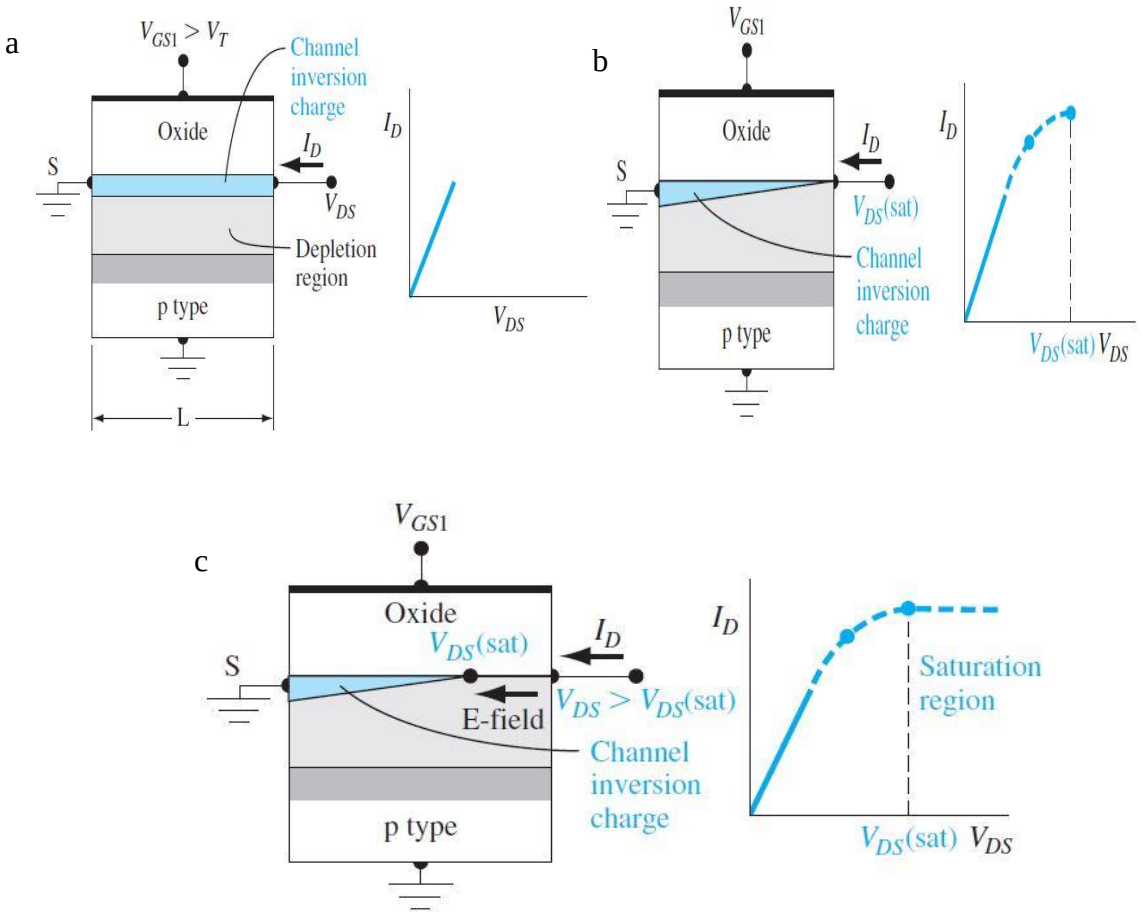

Figure 2.10 MOSFET structure illustrating (a) the creation of both the linear and (b) saturation regimes and shows (c) stronger pinch off point that leads to drain current saturation. V_{GS} is the gate to source voltage, V_{DS} is the drain to source voltage, V_T is the threshold voltage and I_D is the drain voltage.

Source: D. Neamen, *Semiconductor physics and devices*. New York: McGraw-Hill, 2012.

The graph shown in Figure 2.12 is called the output characteristics of a MOSFET. It is obtained by measuring I_D vs V_D as a function of varying V_G. Another important MOSFET characterization data is the transfer characteristic (Figure 2.11), which is obtained by measuring I_D vs V_G while keeping V_D fixed.

The Transfer characteristic and output characteristic can help in understanding the behavior of the MOSFET. The drain current increases as the gate voltage increases. Moreover, at a specific drain voltage in the output characteristics, each point of drain current for each applied gate voltages sums up to give the transfer characteristics behavior. Analysis of the transfer characteristics yields the following device parameters: threshold voltage, ON/OFF ratio, linear mobility, saturation mobility and subthreshold swing.

Threshold voltage is the voltage needed to create a conductive channel, or in other words, it is the voltage needed to turn the transistor ON. A common method for determining the threshold voltage is by finding the intersection between the x-axis and the tangential line of the linear regime in the transfer characteristics as shown in Figure 2.11 (b). This voltage is positive for n channel MOSFET when it operates in the enhancement mode, and it is negative when it operates in the depletion mode. Enhancement mode of operation is generally preferable since there will be no need to apply a constant voltage to turn the transistor OFF thus minimizing power consumption.

Furthermore, the ON/OFF ratio is the ratio between the maximum and minimum drain current.[32] Usually, the ON current depends on the carrier mobility and the number of capacitively induce carriers. The OFF current depends on the leakage current and electronic noise.[33] The ON current is the highest current reached when the transistor is ON and can be extracted from transfer characteristics. The OFF current is the minimum

current when the transistor is at OFF state and can also be extracted from the transfer characteristics. Figure 2.11 (b) shows the ON and OFF currents in the transfer characteristics.

The subthreshold swing indicates the value of the gate voltage to be applied to raise the drain current by one decade. It is affected by the semiconductor/dielectric interface, and it is an indication of how efficient the transistor turns ON and OFF.[32]

Mobility describes how fast the carriers transport within a semiconductor channel. The field effect mobility value can be affected by various factors including interface states, scattering that occurs from dielectric charges and surface roughness. Thus, yielding different values compared to the ones obtained from Hall effect measurements (Hall mobility).

Linear and saturation mobilities can be calculated using the following equations where $V_D<V_G-V_T$ (linear regime) for linear mobility and $V_D>V_G-V_T$ (saturation regime) for saturation mobility:

$$g_{lin} = \mu_n C_{ox} \frac{Z}{L} V_D \tag{2.12}$$

$$g_{sat} = \mu_n C_{ox} \frac{Z}{L} (V_G - V_T) \tag{2.13}$$

g_{lin} is linear transconductance, g_{sat} is saturation transconductance, μ is effective field-effect mobility, C_{OX} is the capacitance of the oxide layer per unit area, Z is channel width, L is channel length. The saturation transconductance is the slope of the linear regime

of the square root of I_D vs V_G plot, whereas the linear transconductance is simply the slope of the linear line in transfer characteristics as indicated in Figure 2.11.

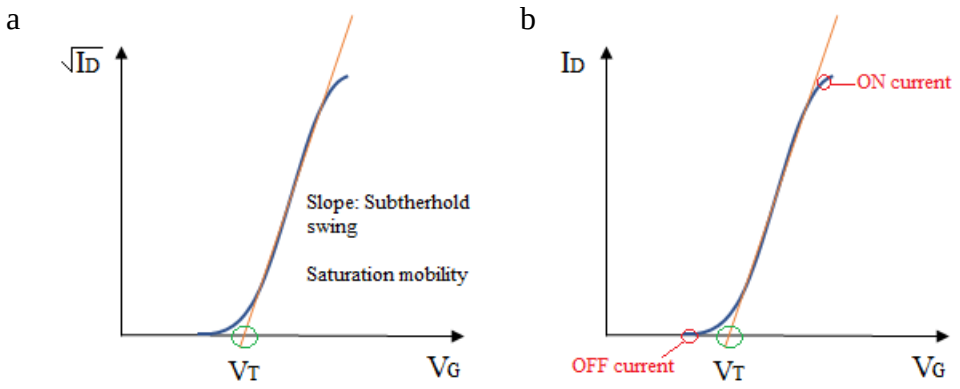

Figure 2.11 Transfer characteristics illustrating the extraction of threshold voltage, saturation transconductance from (a) square root of I_D vs V_G and ON/ OFF currents and linear transconductance from (b) I_D vs V_G.

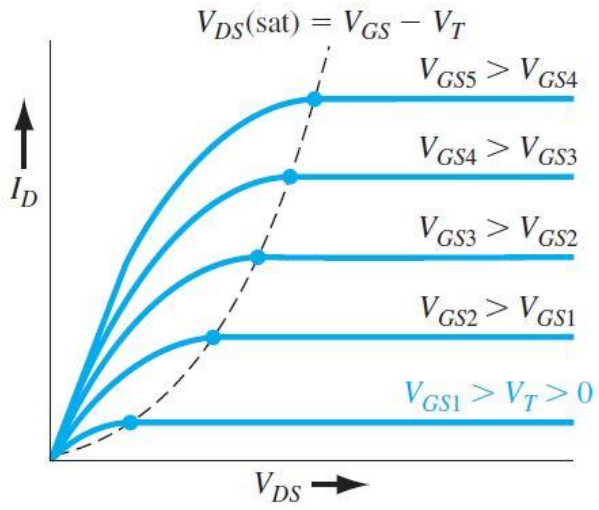

Figure 2.12 Output characteristics of n-channel MOSFET.

Source: D. Neamen, *Semiconductor physics and devices*. New York: McGraw-Hill, 2012.

2.2 Thin Film Transistors

Thin Film Transistor (TFT) is a special kind of transistors that shares the same operational principles of MOSFET. It is a three-terminal device with a source, drain and a gate. Like

the MOSFET the source is usually grounded, the drain collects these carriers, and the gate helps with building the conductive channel for the carriers to transport from source to drain.

One of the key differences between TFT and MOSFET is that TFT layers can be deposited in a different sequence rather than being built on the substrate thus giving more freedom in choosing the structure of the device among four common structures.[34, 35] These four structures can be classified as top gate or bottom gate as in MOSFET and also can be further classified into two categories depending on whether the gate is on the same side or opposing side of the electrodes (source and drain). These two categories are referred to as coplanar or staggered respectively.[34, 35] In other words, If the source and drain are between the semiconductor layer and the insulator layer, then it is said to be a staggered structure, however, if not then it's a coplanar structure. Figure 2.13 shows these four structures.

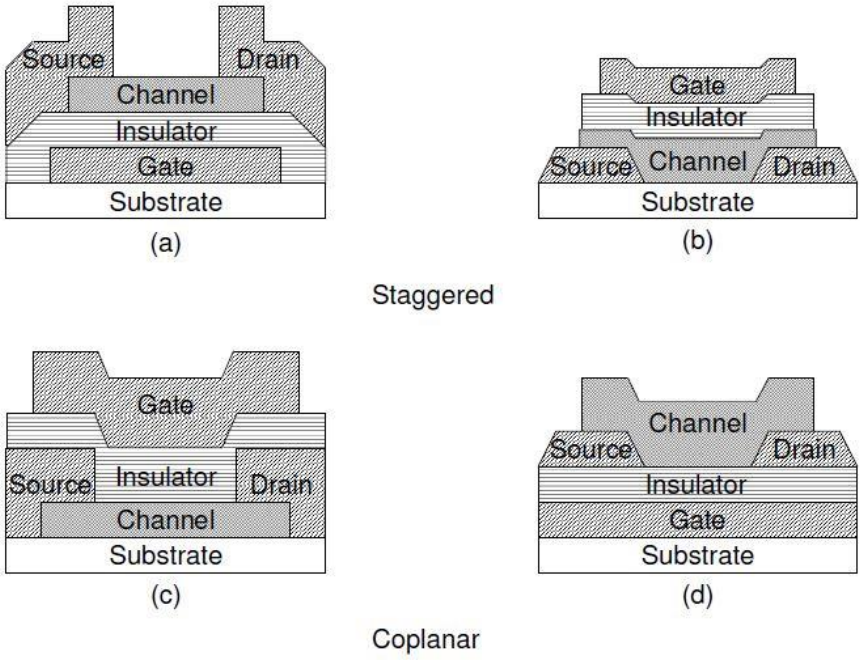

Figure 2.13 Demonstration showing (a) staggered bottom gate (b) staggered top gate (c) coplanar top gate and (d) coplanar bottom gate.

Source: C. R. Kagan and P. Andry, *Thin-film transistors*. Marcell Dekker, Inc., 2003.

Each of the staggered and coplanar structures has its applications. For example, while a coplanar structure is used with poly-Si TFT due to the need for a high annealing temperature and a flat uniform film,[36] the staggered structure is used with a-Si TFT because it reduces the series resistance as it ensures enough overlap between the electrodes and the active channel layer.[34] Additionally, bottom gate TFTs don't protect the thin semiconductor layer from environmental degradation, but they are still used because they allow easy modification of the semiconductor surface properties.[37]

In terms of device operation, the mechanism that turns the FET ON in a TFT is different from the one described in MOSFET. The channel conduction path of TFT is composed of metal/semiconductor/metal structure in contrast to BJT-like $n^+/p/n^+$ (or $p^+/n/p^+$) of MOSFETs. Thus, when the TFT is under accumulation mode, the transistor turns ON and do not necessarily have to reach an inversion stage.

However, the main electrical parameters in a TFT and MOSFET are alike which are mobility, threshold voltage, subthreshold swing and ON/OFF ratio. These parameters vary depending on different factors such as device structure, oxide semiconductor used, dielectric material and fabrication process. TFT parameters are obtained from transfer and output characteristics using the same analysis described in the MOSFET section.

2.3 Amorphous Oxide Semiconductors

2.3.1 Amorphous and Crystalline Forms

Amorphous materials started to grab most of the research attention on flexible and transparent electronics because their building structure allows better uniformity and lower processing temperatures. These materials are also known as vitreous materials. They are

non-crystalline solids that are made of interconnected structural blocks lacking the orientation, organization and long-range order and repetition. In other words, amorphous materials' atoms don't form an organized lattice pattern. However, both amorphous and crystalline phases maintain the short-range order at the atomic scale due to the nature of chemical bonding between the atoms. Amorphous solids differ from crystalline solids by the fact that their unorganized short-range patterns don't have crystalline grains and boundaries like the one found between two adjacent crystals in polycrystalline materials as shown in figure 2.13.

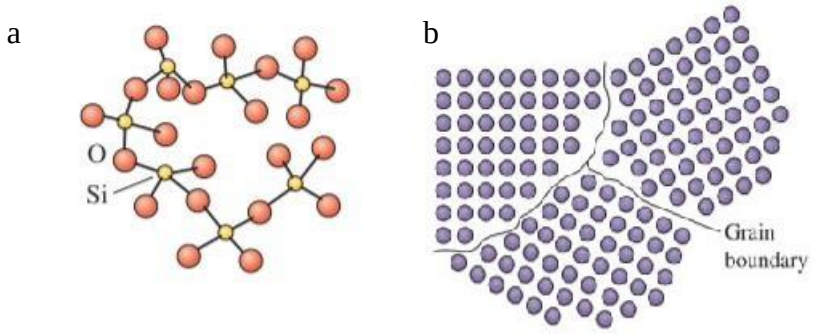

Figure 2.14 (a) Amorphous atomic structure (b) crystalline atomic structure.

Source: Y. Mastai, *Advances in crystallization processes*. Rijeka, Croatia: InTech, 2012.

2.3.2 IGZO and AOS Physics

Among various AMOS, a-IGZO stands strongly because of its' exceptional properties. IGZO elements are the most used elements for oxide semiconductors since each of Zn, Ga and In are not toxic and cheap.[39] Each element in a-IGZO plays a critical role in the overall performance of the material. For example, increasing the amount of Indium increases the mobility of the semiconductor.[40] This is because the s orbital cloud of Indium, responsible for electron conduction, is large and isotropic thereby increasing the overlap of electrons cloud and allowing the electrons to transport easily within the material even in amorphous

form.[41, 42] In contrast, the high directional sp3 orbital cloud of silicon has small overlapping that force the carriers to transport inefficiently resulting in low mobility of $\mu<0.1$ $cmV^{-1}s^{-1}$.[42- 44] Figure 2.14 compares the conduction orbital clouds of each neighboring atom in a-Si and IGZO for crystalline and amorphous phases, respectively.

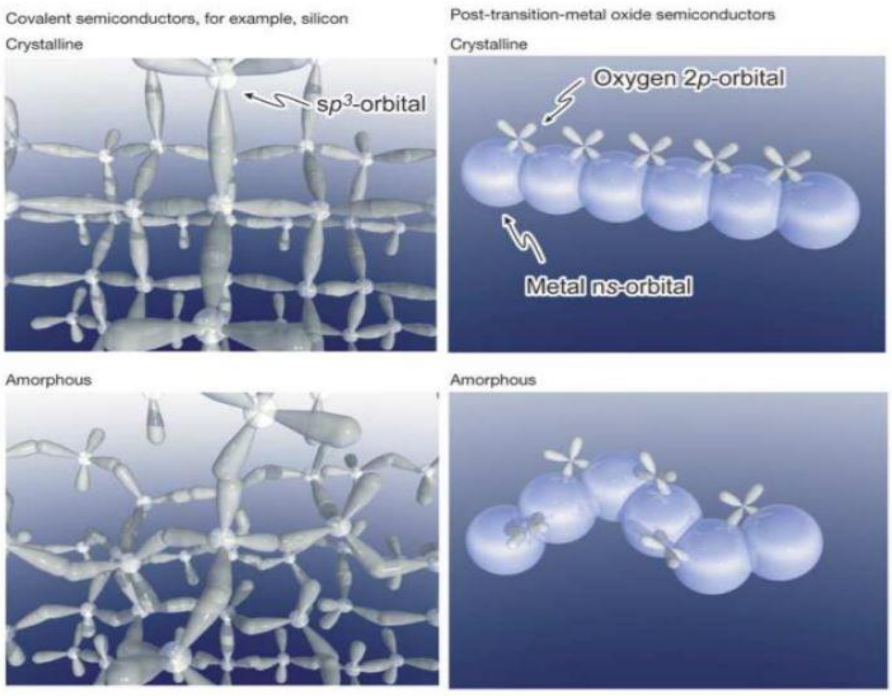

Figure 2.15 Shows a comparison of Si and IGZO crystalline and amorphous atomic structures.

Source: K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, H. Hosono, *Nature* 2004, 432, 488.

Moreover, gallium and zinc play critical roles in determining the electrical characteristics of the film. Gallium is known to increase the stability of the film since the bond between gallium and oxygen is stronger than that of zinc and indium, thereby contribute to creating a stable M-O-M structure[45].

On the other hand, zinc controls the doping of the semiconductor because it increases oxygen vacancies in the amorphous structure. These oxygen vacancies result in

unbonded metal atoms thus more electrons are left free, increasing the carrier concentration and doping consequently.

Various oxide semiconductors, including binary, ternary and quaternary compounds have been studied by Hosono et al.[39, 46] The binary oxide semiconductors like ZnO and In_2O_3 suffer from grain boundaries that cause high scattering of free carriers since they tend to crystallize. They also suffer from low stability, low ON/OFF ratio and high electrical resistivity of their TFTs.[47] Multicomponent compounds such as IGZO, IZO and ZGO are illustrated in figure 2.15 (a).[48] Mixing different atomic sizes disrupts the formation of crystalline form, allowing the desired amorphous phase to occur.[49] Also, it's clear from figure 2.15 (b) that the compounds with higher molarity of indium tend to have higher mobility, thus in agreement with the theory. This means that IGZO represents the most promising technology among other AMOS due to the advantageous combination of high mobility controlled by indium, large area structural stability controlled by introducing various atom sizes, and the ability to control oxygen vacancies and doping by controlling the quantity of gallium and zinc respectively.

It is preferable to start with 6:1:3 molar ratio of IGZO in device fabrication since it allows the formation of amorphous phase and at the same time maintains high mobility as can be seen from figure 2.15. After testing 6:1:3 devices, the performance can be further improved by optimizing different molar ratios to find the optimum molar ratio that gives the best performance along side maintaining a desired amorphous film.

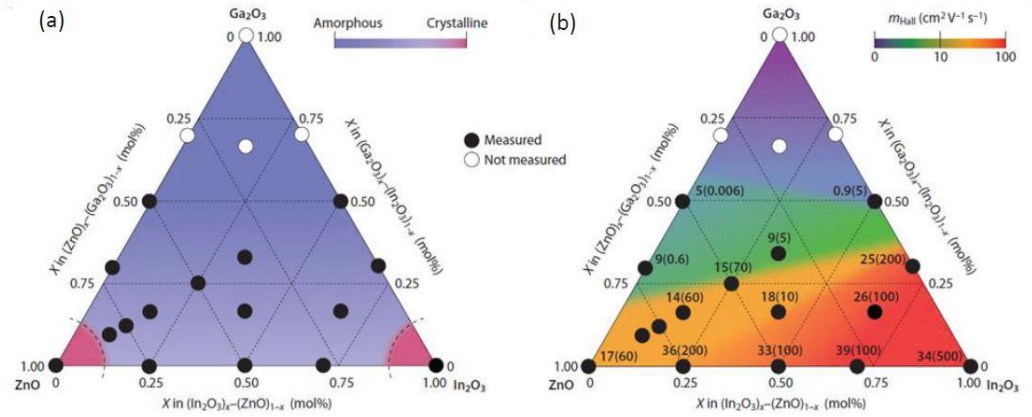

Figure 2.16 (a) Crystallinity of respective metal oxide semiconductor and (b) their corresponding hall mobility.

Source: K. Nomura, A. Takagi, T. Kamiya, H. Ohta, M. Hirano, H. Hosono, *Jpn. J. Appl. Phys.* **2006**, *45*, 4303.

2.4 High-k Dielectric Material

One of the most important components in TFT and MOSFET is the dielectric layer as it forms the core component of MOS capacitor. A thin dielectric layer is preferred because the thinner the layer, the lower the operating voltage of a TFT. However, if it becomes thin, there is an increased possibility of creating pin-holes. The tunneling effect also becomes stronger, leading to higher leakage current through the layer.[50-54] High-K dielectric materials are materials with a high dielectric constant which can induce a higher number of charges for an identical layer thickness and applied bias. The use of these materials can decrease the gate leakage thus increasing the gate capacitance and devices performance.[55-57] Al_2O_3 is one of the well-known high-k dielectric materials with a dielectric constant around 7 [58-59] compared to traditional SiO_2 which has a dielectric constant around 3.7. It also has a preferential wide band gap (around 8.9) as shown in the following figure.[60]

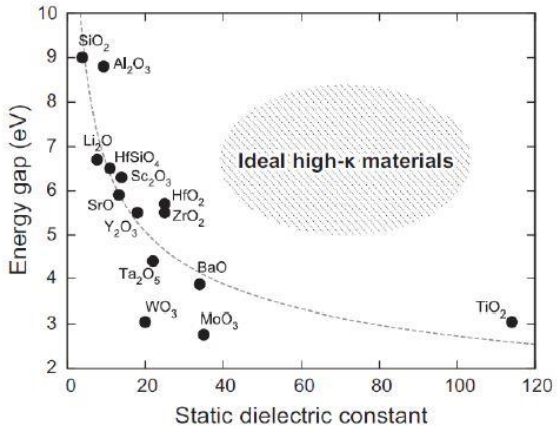

Figure 2.17 Energy gap VS static dielectric constant for different Dielectric materials.

Source: K. Yim, Y. Yong, J. Lee, K. Lee, H.-H. Nahm, J. Yoo, C. Lee, C. Seong Hwang, and S. Han, "Novel high-κ dielectrics for next-generation electronic devices screened by automated ab initio calculations," *NPG Asia Mater.*, vol. 7, no. 6, p. e190, Jun. 2015.

The wide band gap allows less tunneling of the carriers when depositing a very thin layer. Another useful feature of using Al2O3 as a dielectric layer is its low temperatures solution-process compatibility thus allowing low temperature and low-cost fabrication of a certain TFTs.

2.5 Spin Coating Deposition Method

To date, many physical vapor deposition (PVD) methods including radio frequency sputtering and pulsed laser deposition that rely on high-cost equipment have been reported to deposit IGZO.[61, 62] However, solution-processing methods of preparing IGZO or any other metal oxide semiconductor offers a significant advantage over PVDs including low-cost, high-throughput manufacturing and the ease of compositional modification, reproducibility, and applicability at atmospheric conditions.[63-66] Inkjet printing, for example, is particularly attractive as it removes the need for costly masking steps and reduces material waste. Solution processing methods start with the synthesis of the solution

or ink followed by deposition and end with the annealing stage. Synthesis of the solution is done by dissolving salts into a solvent to form a metal precursor with specific molarity. The deposition stage can be carried out using different techniques such as spin coating, spray coating, and inkjet printing.[67] Spin coating is chosen in this project because it is one of the most used methods for giving a uniform film. This process provides facile control of the thickness and quality of the film by adjusting process parameters such as spinning speed, duration, solute concentration, and heating.[68-71] It is done by applying a small amount of the prepared solution on a non-spinning substrate. The applied solution is then spread on the substrate by rotating it at a certain speed for a specific time to set the desired thickness. However, this method still has few disadvantages such as high material waste since most of the applied solution is spilled out of the rotating substrate. Figure 2.17[69] summaries this process:

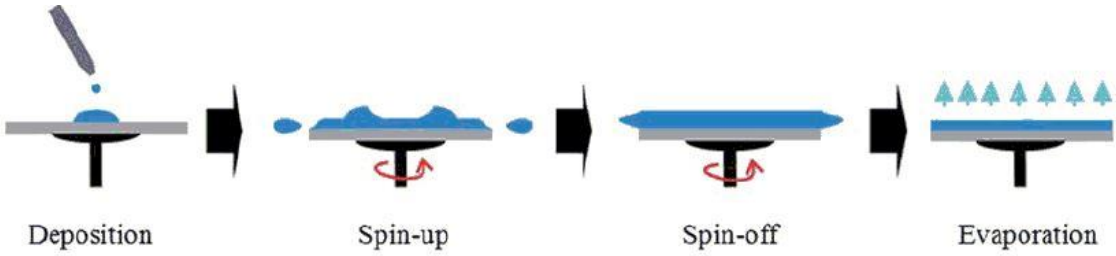

Figure 2.18 Solution processing method for depositing a semiconductor using spin coating after solution synthesis stage.

Source: Raut, Hemant Kumar, et al. "Anti-reflective coatings: A critical, in-depth review." Energy & Environmental Science 4.10 (2011): 3779-3804.

The substrate is then annealed at a high temperature to develop the active channel. During the annealing process, subsequent phenomena occur which are decomposition, hydrolysis, and dihydroxylation to form a metal-oxide-metal network.[72]

2.6 UV Assisted Annealing

The major problem of the commonly employed solution processed methods is that they require a very high annealing temperature which prevents the films from being fabricated on a transparent and flexible low transition temperature substrate. Lowering the annealing temperature while maintaining the electrical property of the film would constitute a significant breakthrough in IGZO thin film processing and their applications.

A recently discovered method to lower the annealing temperature of IGZO uses high-intensity UV exposure during heat treatment.[73] During this UV-assisted annealing, the film undergoes two stages. The first is condensation where the high energy photons break the alkoxy groups, decreasing the oxygen and carbon content and allowing a better metal-oxide-metal (M-O-M) structure.[73] The second stage is the densification process where the high energy radiation leads to a better arrangement of disordered M-O-M structure and further decreases the content of oxygen and carbon as shown in figure 2.18.[73] This approach can be used to decrease the processing temperature of solution processed IGZO since the thermal energy is provided by the DUV treatment and thus the need for high temperature to rearrange the M-O-M is eliminated when this method is used.

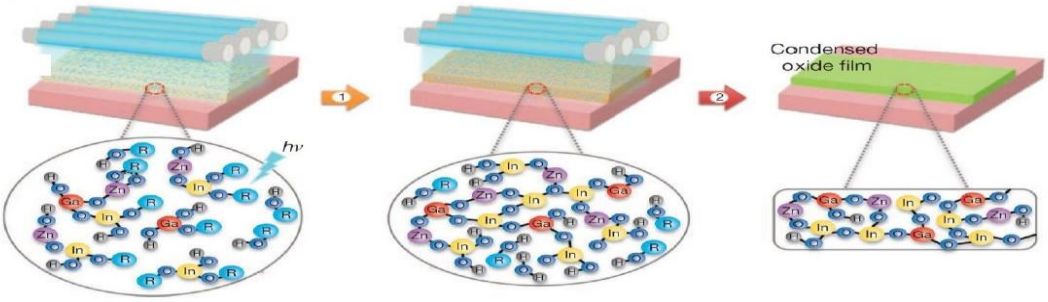

Figure 2.19 Schemes showing condensation and densification mechanisms of metal-oxide precursors by DUV irradiation. The blue cylinders donate the illumination from the mercury lamp.

Source: Y. H. Kim, J. S. Heo, T. H. Kim, S. Park, M. H. Yoon, J. Kim, M. S. Oh, G. R. Yi, Y. Y. Noh, S. K. Park, " *Nature* **2012**, *489*, 128.

2.7 IGZO Applications and Current State

A lot of research targets IGZO due to the ability to control the mobility and doping as well as easily maintaining the amorphous form. In general, a-IGZO TFT has a high mobility that can reach up to 80 cm^2/V.s if it is deposited using CVD methods and a mobility in the range of 4-30 cm^2/V.s if it is deposited using solution processing methods. This wide range of mobility variation depends on several factors such as the fabrication method used, the solvent used, annealing method, annealing temperature and annealing period. In addition, IGZO TFT has a very high ON/OFF ratio that is in the range of 10^6-10^7, however, this value is reduced as the annealing temperature is reduced. The high ON/OFF ratio comes from the fact that using AMOS TFT has a very low leakage current that results in a very low OFF current that is way less than poly-Si TFT OFF currents. The following figure shows the electrical parameters of several TFT devices fabricated for different durations such that the first and second stages were done at 100C and 400C respectively.

process	stage 1 time[a] (min)	stage 2 time[a] (min)	precursor	$\mu_{e,sat}$ (cm^2/V·s)	$V_{e,TH}$ (V)	S.S (V/dec.)	I_{on}/I_{off}
conventional annealing	5 min	60 min	IZO (1/1)	11.10	3.0	0.6	1.2×10^7
			IGZO (6/1/3)	8.4	−2.4	0.5	1.2×10^7
			IGZO (6/1.5/2.5)	4.8	2.9	0.6	1.6×10^7
		60 min	IZO (1/1)	27.8	−5.5	1.0	2.1×10^5
			IGZO (6/1/3)	21.2	−5.9	1.3	2.1×10^5
			IGZO (6/1.5/2.5)	15.1	−4.5	0.9	2.1×10^6
	5 min		IZO (1/1)	27.9	−7.7	1.9	4.7×10^5
		40 min	IGZO (6/1/3)	20.1	−8.1	1.9	4.7×10^5
			IGZO (6/1.5/2.5)	18.3	−8.4	1.7	2.2×10^5
			IZO (1/1)	25.9	−6.5	2.0	2.0×10^5
water vapor annealing (only stage 1)		20 min	IGZO (6/1/3)	21.2	−10.2	1.8	2.0×10^5
			IGZO (6/1.5/2.5)	16.3	−8.7	1.8	2.7×10^5
			IZO (1/1)	19.0	−4.6	1.7	1.7×10^5
	3 min	10 min	IGZO (6/1/3)	16.6	−0.7	1.8	5.3×10^4
			IGZO (6/1.5/2.5)	15.7	−2.4	2.1	1.1×10^5
			IZO (1/1)	19.2	−1.6	2.8	1.5×10^4
		5 min	IGZO (6/1/3)	17.4	−1.8	1.7	1.0×10^5
			IGZO (6/1.5/2.5)	16.4	−1.4	2.1	2.7×10^4

Figure 2.20 Electrical parameters of different TFTs annealed for different duration.

Source: W. Park, I. Son, H. Park, K. Chung, Y. Xu, T. Lee and Y. Noh, "Facile Routes To Improve Performance of Solution-Processed Amorphous Metal Oxide Thin Film Transistors by Water Vapor Annealing", *ACS Applied Materials & Interfaces*, vol. 7, no. 24, pp. 13289-13294, 2015.

The advantageous electrical parameters of AMOS including IGZO over poly-Si and a-Si allow the use in different fields and applications such as display applications,[24] memory applications,[24] UV photodetectors,[74] biosensors[75] and thermoelectric applications.[76] For example, The low leakage current of oxide semiconductors and the high ON/OFF ratio enable industries to use it in the production of LCD panels. This property allows low power consumption and it also allows the pixel to hold the potential of 1HZ thus only minor fluctuation in brightness occur.[24] Figure 3 shows the difference in brightness fluctuation for AOS and a-Si panels. It is clear that a-Si has much higher fluctuation than AOS devices.

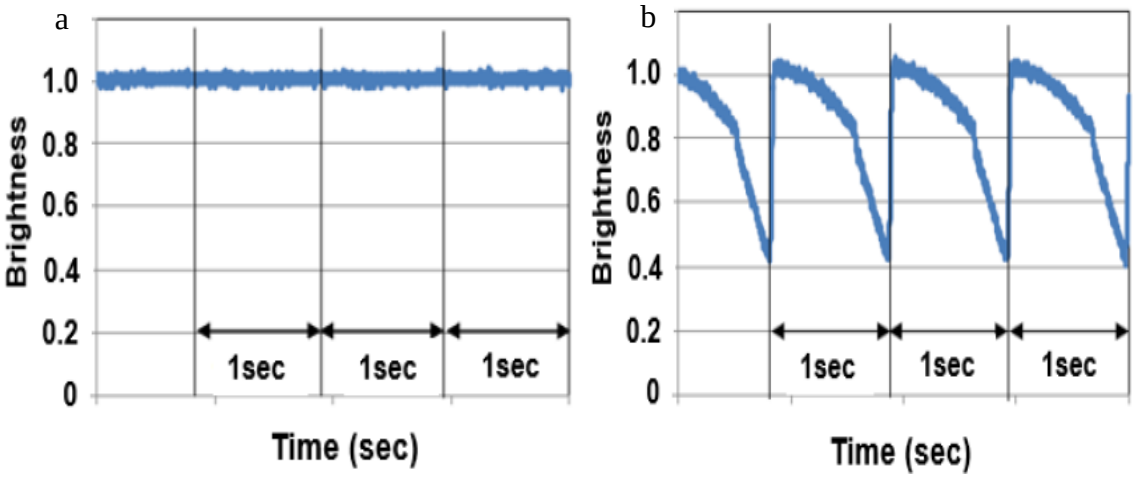

Figure 2.21 Brightness fluctuation of (a) AOS and (b) a-Si.

Source: T. Matsuo, S. Mori, A. Ban and A. Imaya, "8.3:Invited Paper: Advantages of IGZO Oxide Semiconductor", *SID Symposium Digest of Technical Papers*, vol. 45, no. 1, pp. 83-86, 2014.

In addition, the wide energy gap of IGZO allows the fabrication of transparent electronics since the visible light goes through the material without absorbing it. Moreover, the high mobility and ON/OFF ratio contribute to reducing the scale of the fabricated electronics since the channel length can be reduced.[24]

CHAPTER 3

PROCEDURE, RESULTS AND DISCUSSION

3.1 Substrate Cleaning

In this thesis, two types of substrates were used which are glass and n^+-Si/SiO_2. The primary objective is to fabricate the devices on a glass substrate, but the n^+-Si/SiO_2 substrate was fabricated as a reference device. All substrates in this study were initially cleaned by sonicating them in isopropyl for 10 minutes to remove particles and dust and air is blown to dry. The substrate was then baked for 5 mins at 200C to ensure that all organic residuals are removed. Afterwards, the surface of the substrate is cleaned using UV Ozone treatment for 20mins and tested to be hydrophilic which is compatible with our polar solvent-based IGZO inks.

3.2 Mask Preparation

Two masks are designed using Layout Editor, one mask for gate electrode fabrication (3000 x 15000 um area) and the other is for source and drain electrode fabrication as shown in Figure 3.1 (a) and (b). Channel lengths and widths are: 100 x 250 um, 100 x 500 um, and 100 x 1000 um. The building structure of the devices in this study is a staggered bottom gate and top contacts. Figure 3.1 (c) and (d) show the structure of the n^+-Si/SiO_2 and glass substrate-based devices respectively.

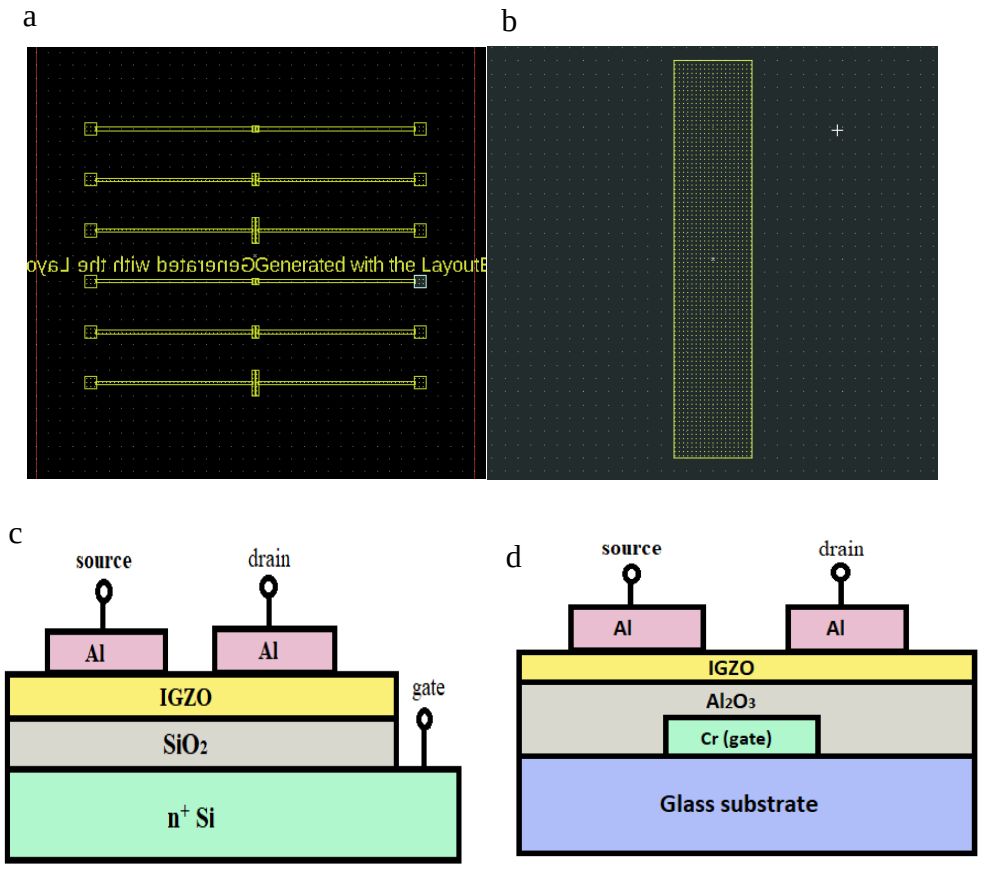

Figure 3.1 Shows (a) source and drain mask, (b) gate mask used for device fabrication, (c) n^+-Si/SiO_2 device structure and (d) glass/Al_2O_3 device structure.

3.3 IGZO Solution Synthesis

IGZO solution is prepared by mixing 511.41 mg of indium nitrate hydrate ($In(NO_3)$. xH_2O), 64 mg of gallium nitrate hydrate ($Ga(NO_3)_3$. xH_2O) and 120.73 mg of zinc nitrate dehydrate ($Zn(O_2CCH_3)_2(H_2O)_2$) with molarities of 0.085, 0.0125 and 0.0275 respectively, into 20 mL of 2-methoxyethanol (2-ME) to yield a 6:1:3 molar ratio solution which is the most commonly reported IGZO ratio.[29,30,77,78] The mixture is then left to be stirred at 75 °C for 12 hours.

The next step was to synthesis Al2O3 solution by dissolving 6.002 g of aluminum nitrate hydrate ($In(NO_3)$. $9H_2O$) into 20 mL of 2-methoxyethanol (2-ME) to reach a

molarity of 0.8. The mixture is also left to be stirred at 75 °C for 12 hours inside a N_2 glovebox.

3.4 High-Temperature Processed Devices

As a first step, a high-temperature annealing process was used to test the properties of IGZO using spin coating method as well as to have a producible reference for the next step which is low temperature processed devices. For this purpose, two types of substrates were used which are n^+- Si/SiO_2 and Glass. The focus of this study is glass-based substrate devices. However, SiO_2-based substrate devices are fabricated to have a solid comparison of its' data with the main devices of the project because most of the studies have used SiO_2 as a dielectric material. Furthermore, the high processing temperature is needed for fabricating the IGZO channel to allow a better arrangement of the M-O-M structure using the excess thermal energy that breaks the bonds between the atoms and rearrange them.

3.4.1 Procedure

A Si wafer (University Wafers Inc.) having a dry thermal oxide SiO_2 of 200nm in thickness is used as a substrate. IGZO is spin coated once with T1= 30s and SPD1= 2000 rpm. The substrate is then pre-annealed using water vapor annealing at a temperature of 120 °C and then post-baked at 400 °C for one hour. Al is deposited with a thickness of 100 nm using thermal evaporation to form a top source and drain contacts. Gate contact region is formed by scratching off the oxide at the corners of the substrate using diamond-tipped scriber. On the other hand, glass-based devices are fabricated by depositing chrome on a glass substrate with a thickness of 40 nm using thermal evaporation to form the gate electrode of the transistor. 15 minutes of UV was performed again to create a hydrophilic (good wetting)

surface. Dielectric layer Al_2O_3 is formed by spin coating 3 times to reach a thickness of 120 nm with T1= 20s and SPD1= 5000 rpm. For each coating step, one side of the gate is swap cleaned to expose the gate contact probing regions. The sample is then prebaked for 1 min at 50 °C and post-baked for 40 mins at 350 °C. IGZO is then deposited using the same procedure of the n^+- Si/SiO_2/IGZO device.

In addition, the thickness of the deposited IGZO layer has also been checked by AFM Step Height (Thickness) Characterization as it affects the drain and leakage currents. The thickness is observed to be around 70nm as shown below in figure 3.2.

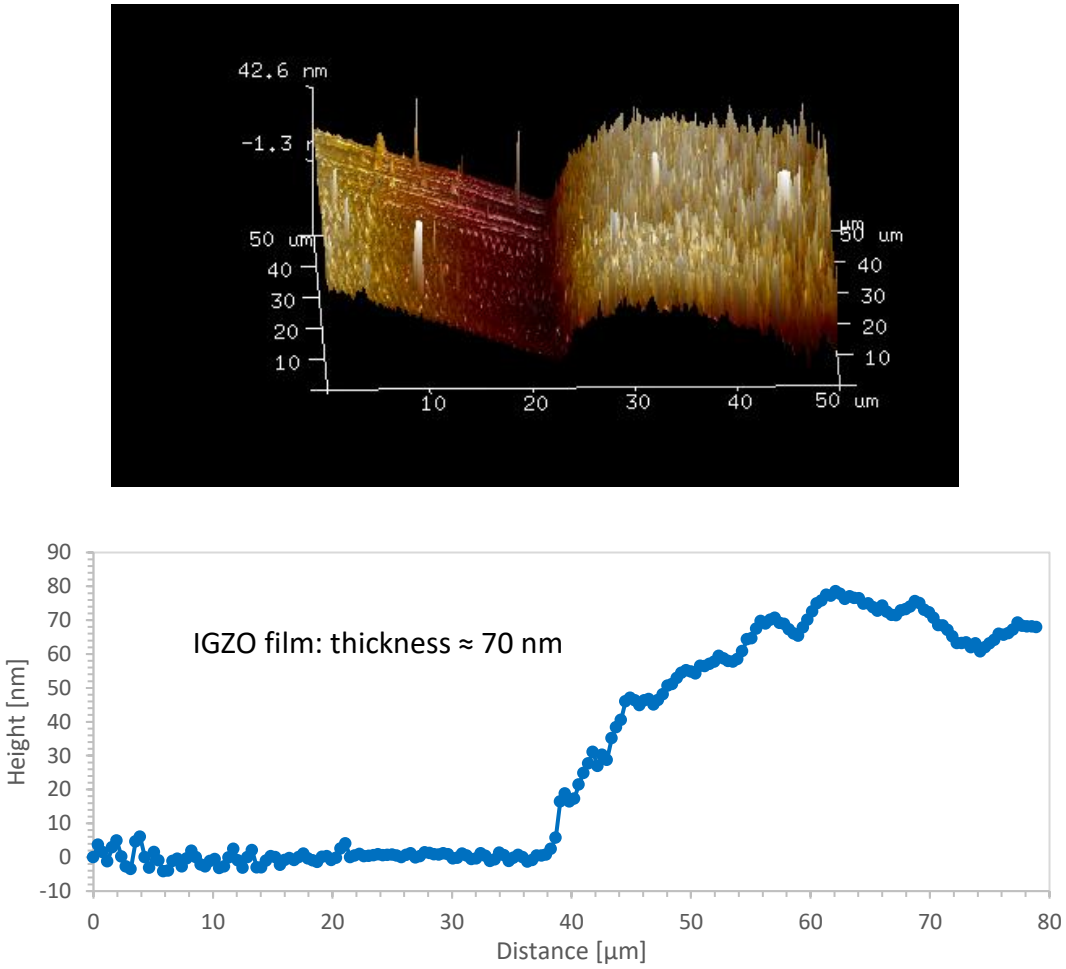

Figure 3.2 AFM Step Height (Thickness) Characterization of IGZO film.

3.4.2 Results and Discussion

1. Standard Si/SiO_2 device

Device analysis:

The mobility obtained from the high-temperature annealing process of the n^+-Si/SiO_2/IGZO device is 2.12 cm^2/Vs ± 15% . Also, the ON current is $5.3x10^{-5}$, and the OFF current is $2.48x10^{-6}$ thus the ON/OFF ratio is calculated to be $2.13x10^{1}$. The threshold voltage and the subthreshold swing are -3.33V ± 18% and 0.167 respectively. This high threshold voltage means that the transistor needs to be depleted to turn it OFF. Figure 3.3 shows the electrical characteristics of the Si/SiO_2/IGZO device.

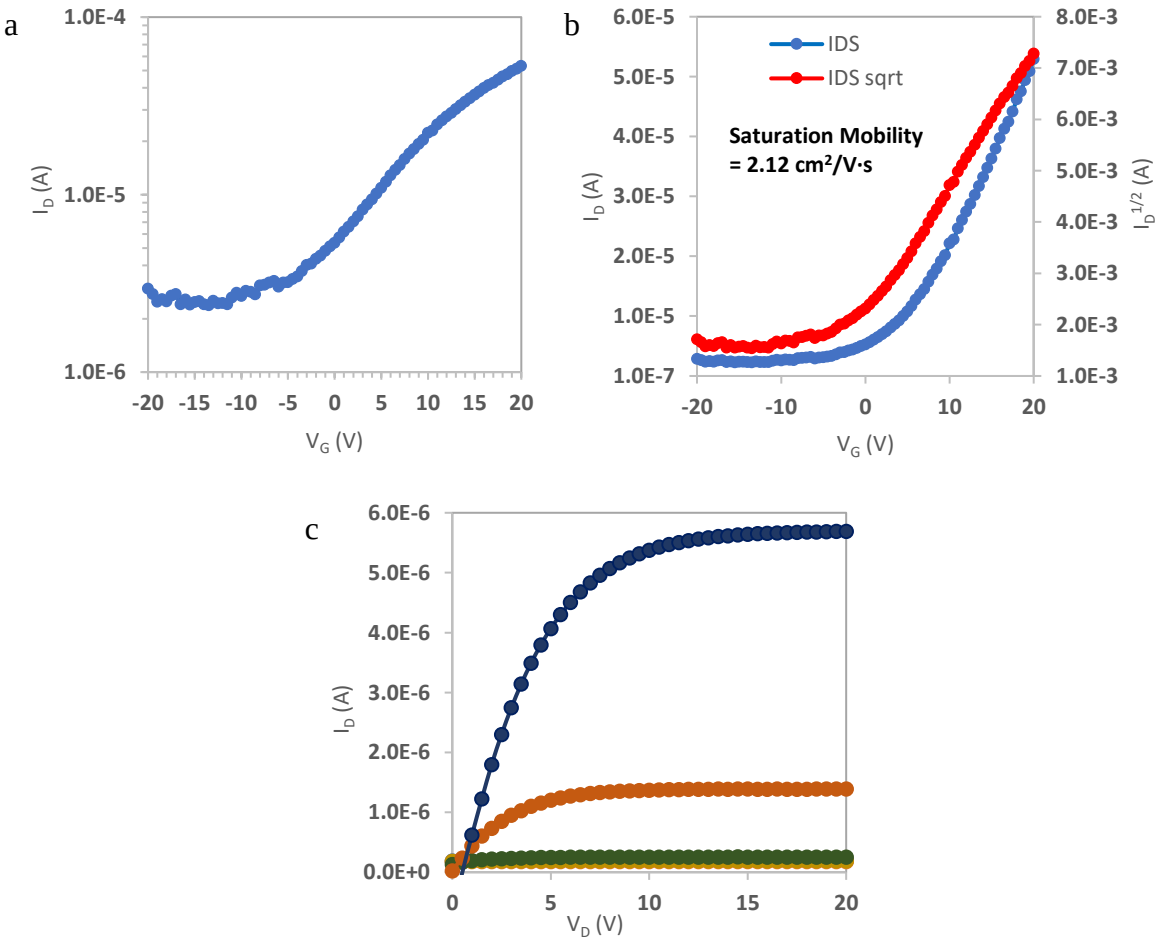

Figure 3.3 Shows (a) transfer characteristics, (b) mobility calculations and (c) output characteristics of Si/SiO_2 device.

Discussion:

The electrical parameters of the fabricated device resulted in mobility higher than a-Si mobility, however, lower than the mobility reported in other papers. Furthermore, the ON/OFF ratios reported were in the range of 10^4 which means that the high temperature processed Si had ON/OFF ratio lower by three orders of magnitude. The main reason for the low ON/OFF ratio is contributed to the fact that it had a high leakage current due to the existing pin holes on the SiO_2 surface which increased the OFF current and thus reduced the ratio consequently, however, this leakage current is close to the leakage current reported in other papers.

2. Glass/Al2O3 device

Device analysis:

Following the same procedure of the SiO_2 device for the glass devices yielded a very high leakage current that is comparable to the drain current as showing in figure 3.4. Thus, it is assumed that the high leakage current is due to the weak insulating Al_2O_3 layer.

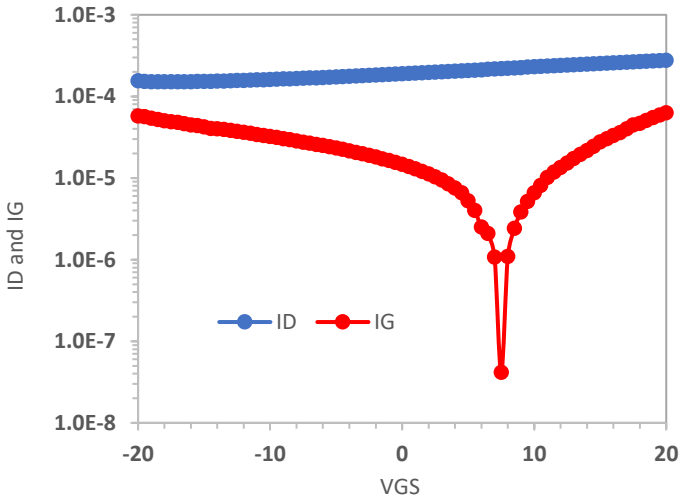

Figure 3.4 Log plot that compares drain current to leakage current of glass/Cr/Al_2O_3 device.

For further improvements, reducing this high leakage current of the glass device to reach a similar value of the SiO_2 device was targeted. It has been noticed that if Al_2O_3 solution is left to be aged in 2-Methoxyethanol for more than 2 days results in a clear yellow solution which gives a better insulating film that has a lower leakage current.

The high temperature processed glass device using the aged Al_2O_3 solution had a mobility of 1.94 $cm^2/Vs \pm 22\%$, ON current of $4.03x10^{-4}$, and OFF current of $1.88x10^{-5}$ thus the ON/OFF ratio is $2.14x10^{1}$. The glass device fabricated gave a V_{th}= -21.6V ± 25% which means that the glass devices consume a lot of power to turn it OFF than the reference Si device. In addition, the subthreshold swing obtained is 0.083. Figure 3.5 shows the electrical characteristics of the glass/Cr/Al_2O_3 device and table 3.1 summarizes the electrical parameters of the n^+- Si/SiO_2 and Glass based substrate devices.

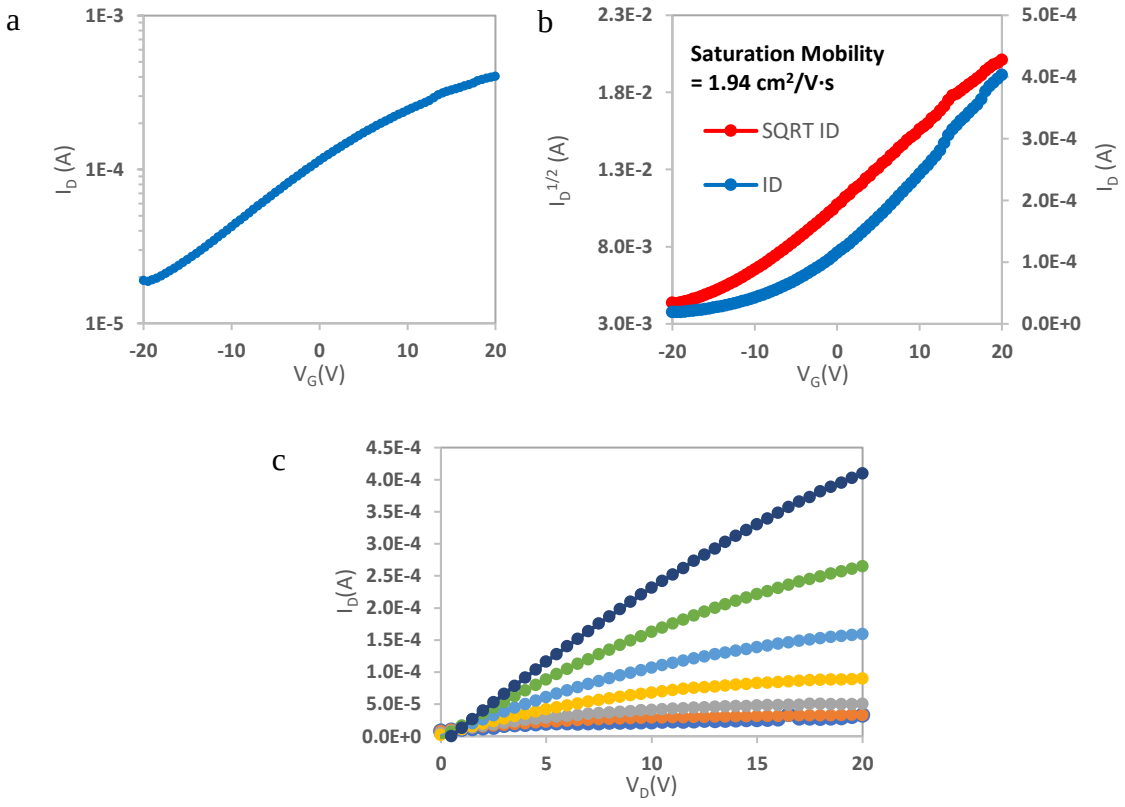

Figure 3.5 Shows (a) transfer characteristics, (b) mobility calculations and (c) output characteristics of glass/Al_2O_3 device.

Table 3.1 Electrical Parameters of Si/SiO_2 and Glass Devices

Device Based on Substrate and Dielectric Layer	μ_{sat} (cm^2/Vs)	ON/OFF ratio	Subthreshold Swing	Threshold Voltage (V)
n^+- Si/SiO_2	2.12	$2.13x10^1$	0.167	-3.33
$Glass/Cr/Al_2O_3$	1.94	$2.14x10^1$	0.083	-21.6

Discussion:

The mobility of the high temperature processed glass device is close to the mobility obtained from the n^+- Si/SiO_2/IGZO device mobility. The higher OFF current and lower ON current here is contributed to the existing cracks on Al_2O_3 layer that causes a high leakage current, however, similar to the leakage current found in the fabricated SiO_2 device as shown in figure 3.6 (b). A high magnification SEM image has been taken to verify the assumption made. It was observed that this high leakage current was due to pinholes on the Al_2O_3 surface similar to the pinholes of the SiO_2 as shown in figure 3.6 (a). These pinholes are holes that are usually created on thin films during the fabrication process and are responsible for the leakage current since they create a path for carriers from source/drain to gate. When the devices of the aged solution are tested, they yielded a lower leakage current in the range of 10^{-5} – 10^{-6} A. This leakage current is comparable to the standard devices and to some reported results as well.[79] Some people achieved to reduce it much further to reach a nano-scale but with the use of different gate material or by using different methods such as patterning.[28] Patterning reduces the leakage current since it will prevent

the whole channel from being activated and thus preventing the dielectric layer from leaking from all over the substrate and allowing it only to leak from that patterned channel.

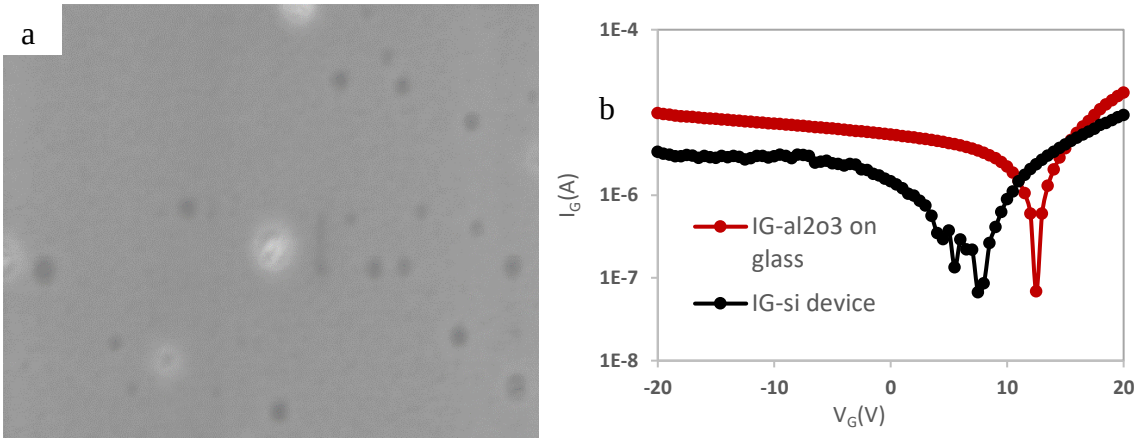

Figure 3.6 (a) SEM image showing the spread of pin holes on Al_2O_3 surface and (b) a comparison between the leakage current of the glass and Si/SiO_2 device.

Moreover, the subthreshold swing of the glass device is lower by a half when compared to the SiO_2 device. This device requires much more power to turn it OFF because the threshold voltage is higher by 18.27V and responds slowly to the change in voltage.

3.5 Low-Temperature UV-Assisted Annealing Devices

After obtaining a mobility of glass-based device close to the n^+-Si/SiO_2 device and higher than a-Si, another goal has been set which is to achieve high mobility from low-temperature UV-assisted annealing of glass-based devices. The UV exposure is employed because it supplies the thermal energy needed for breaking and rearranging M-O-M bonds under low-temperature annealing processes.[80-84] Electrical characteristics similar to the high-temperature annealing is targeted such as a mobility over 1 cm^2/Vs. Also, many literatures performed the annealing process and the UV exposure at the same time, however, the separation of these two processes have been tested since the exposure to high power UV is

known to break the bonds and annealing is known to re-bond and reorganize IGZO structure. Moreover, the effect of higher temperature UV assisted annealing has also been studied to understand further how important it is to increase thermal energy supplied by the annealing process when the film is exposed to UV. Increasing the UV-assisted annealing from 90 °C to 150 °C was expected to give a better TFT performance since a better arrangement of the amorphous phase is expected.

3.5.1 Procedure

The same previous procedure is followed to make a device on a glass substrate but with low-temperature UV assisted annealing of IGZO. After spin coating IGZO at 2000 rpm for 30 s the device was prebaked at 50C for 3 mins and then post-baked by UV assisted annealing at 90C for 2 hours. Then Al electrodes have been deposited using thermal evaporation. The high-intensity UV lamp emits 254 nm light with an intensity exceeding 17,000 μW/cm² in proximity to the mercury lamp surface. The Other set of devices have been made by increasing the annealing temperature to 150 °C compared to the previous 90 °C to check the TFT performance when additional thermal energy is introduced under UV exposure. Additionally, devices with separate annealing process and UV exposure have been made. These devices were processed by exposing IGZO to UV first and annealing the film separately afterward.

3.5.2 Results and Discussion

Device analysis:

The low-temperature UV assisted annealing glass devices yielded a 1.89 cm^2/Vs ± 26% mobility, 3.55 $x10^{-5}$ ON current and 1.62 $x10^{-7}$ OFF current. The threshold voltage obtained is 9V ± 15% and a subthreshold swing of 0.35. Figure 3.7 shows this device electrical

characteristics. In addition, the higher temperature using 150C under UV assisted annealing did not affect the electrical characteristics positively but rather gave the same results with minor differences such as a threshold voltage of 8.33V.

The separate processing treatment devices had a mobility of 4.69 $cm^2/Vs \pm 15\%$, a higher ON current of $2.43x10^{-4}$, lower OFF current of $7.22x10^{-8}$ thus ON/OFF ratio of $3.36x10^3$. The threshold voltage increased in this case reaching a value of 5.91V ± 30% and the subthreshold swing increased reaching a value of 0.74. Table 3.2 summarizes both the separate and simultaneous annealing treatment devices results.

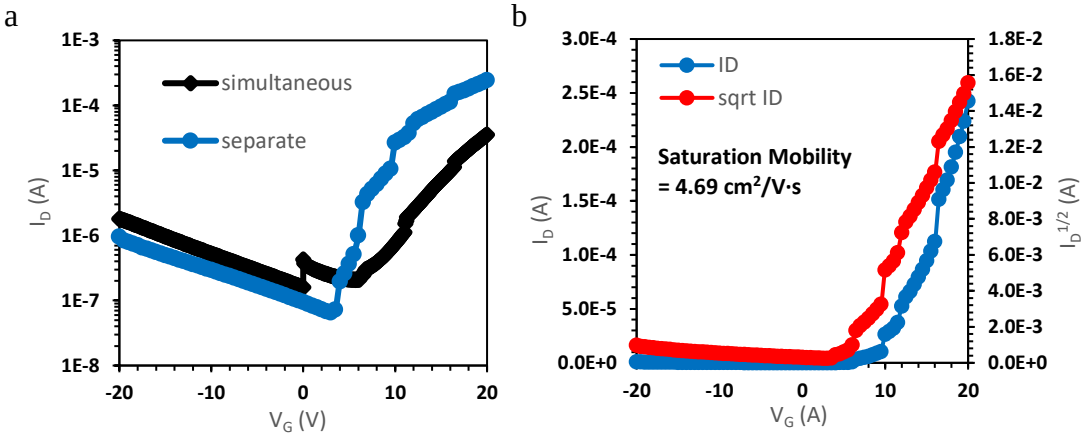

Figure 3.7 Shows (a) transfer characteristics and (b) mobility calculations of the low temperature processed glass device.

Table 3.2 Electrical Parameters of Low-Temperature Processed Glass Device and the Device Fabricated Using Separate UV Exposure and Annealing Process

Annealing process	μ_{sat} (cm^2/Vs)	ON/OFF ratio	Subthreshold Swing	Threshold Voltage (V)
90C UV assisted annealing	1.89	$2.21x10^2$	0.35	9
Separate UV/annealing	4.69	$3.36x10^3$	0.74	5.91

Discussion:

Even with the lower temperature used to fabricate these glass devices, the mobility is close to the one of high-temperature annealing which indicates that the carriers transport in this device channel is as efficient as in the channel of the high temperature annealed devices. This agrees with the fact that UV exposure allows a good rearrangement of the amorphous structure even at low temperatures. Moreover, the higher ON/OFF ratio indicates better structure obtained from a UV exposure as well. The threshold voltage is obtained to be 9V which means that the resulted glass device fabricated under low-temperature UV assisted annealing process does not need power to turn it OFF; however, 9V is needed to turn the transistor ON.

Furthermore, the separate processing treatment resulted in an increase in the ON current by one order of magnitude and a decrease in the OFF current. This means that an improvement in the ON/OFF ratio from 2.21×10^2 to 3.36×10^3 has occurred. Also, the resulting FET had a mobility of 4.69 cm^2/Vs which is higher than the mobility observed from simultaneous annealing. Moreover, the threshold voltage using this procedure was reduced from 9V to 5.91V. This concludes that separate annealing gives a better TFT performance and is in agreement with the mentioned theory as UV exposure break and rearrange the bonds between the molecules and then re-bond them through temperature annealing.

3.6 Improving UV-Assisted FET Devices by Modifying IGZO Composition

Within the device configuration and film processing conditions, analysis of previous data indicates that the IGZO FET performance should be improved by lowering the OFF current

and increasing the ON current. Lowering the OFF current can be achieved through de-doping the IGZO film by increasing the Ga content. Additionally, ON current can be improved by increasing the electron mobility by increasing the In content.

Firstly, De-doping IGZO by increasing the concentration of gallium is performed. The concentration of Ga in IGZO film is known to change the free electrons concentration by modifying the concentration of oxygen vacancy. Then, the Indium content in the de-doped IGZO is increased to increase the ON current.

3.6.1 Procedure

A change in the molar ratio of IGZO from standard 6:1:3 to 6:2:3 has been done and the electrical characteristics of the fabricated device have been tested. Moreover, after testing the 6:2:3 solution, a new solution has been made by increasing the molarity of indium in the de-doped IGZO by 30%, to yield a molar ratio of 8:2:3.

3.6.2 Results and Discussion

Increasing Ga content resulted in a decrease in the OFF current by one to two orders of magnitude, but the ON current decreased as well. Also, a decrease in the leakage current has been observed as expected. Introducing higher molarity of Gallium decreased the mobility of the carriers substantially to reach 0.3 $cm^2/Vs \pm 16\%$. The ON/OFF ratio changed from $2.21x10^2$ to $6x10^2$. The decrease in the ON current and the OFF current is contributed to the lower conductivity channel caused by increasing the molarity of gallium. The threshold voltage is further reduced from 9V to 3V ± 16%. Figure 3.8 compares the transfer characteristics of the 6:1:3 and 6:2:3 devices.

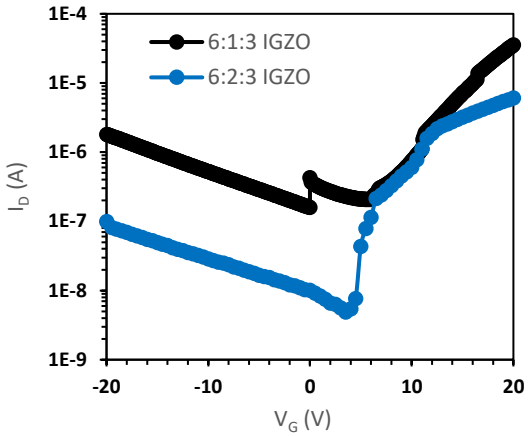

Figure 3.8 Transfer characteristics of 6:1:3 and 6:2:3 IGZO devices**.**

The reduction in ON/OFF ratio and mobility had to be compensated by increasing the Indium content. The increase in Indium content increased the ON current by around two orders of magnitude which was offset by an increase in the OFF current by order of magnitude, as shown below. The ON/OFF ratio changed from $6x10^2$ to $3.7x10^3$. Also, the resulting FET had a mobility of 7.59 cm^2/Vs ± 5% which is better than the 1.9 cm^2/Vs observed in low-temperature UV assisted annealing 6:1:3 device and better than 0.3 cm^2/Vs observed in low-temperature UV assisted annealing 6:2:3 device. In addition, the subthreshold swing increased to 0.66 which is higher than the 6:2:3 device subthreshold swing. This implies that the TFT turns ON and OFF faster. However, the threshold voltage was 5.15V ± 9% which is lower than the 6:1:3 device but higher than the 6:2:3 device. Table 3.3 summarizes the parameters of FET devices using different molar ratios and Figure 3.9 shows the transfer characteristics, mobility calculation and output characteristics respectively.

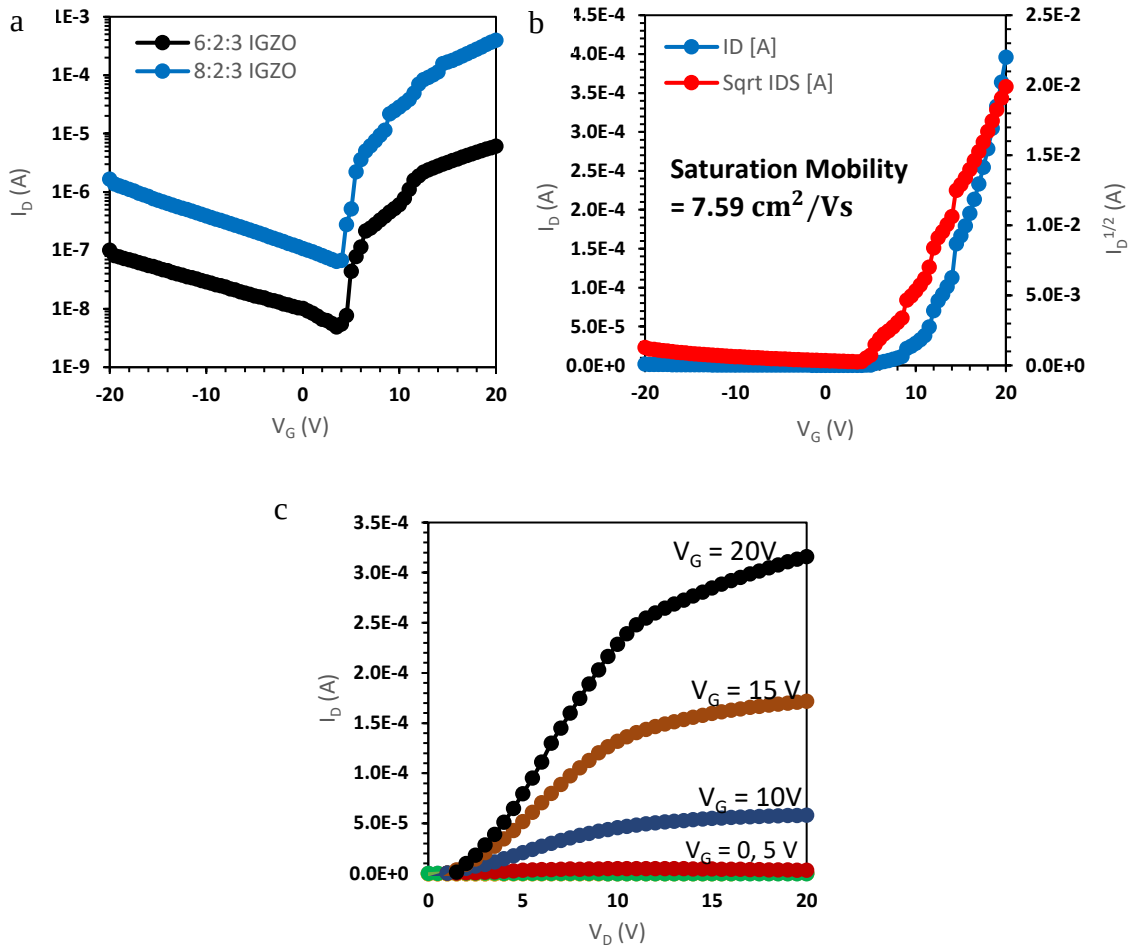

Figure 3.9 Shows (a) transfer characteristics of 6:2:3 and 8:2:3 IGZO devices, (b) mobility calculations and (c) output characteristics of the 8:2:3 IGZO device.

Table 3.3 Electrical Parameters of 6:1:3, 6:2:3 and 8:2:3 IGZO Devices

IGZO Molar Ratio	μ_{sat} (cm^2/Vs)	ON/OFF ratio	Subthreshold Swing	Threshold Voltage (V)
6:1:3	1.89	2.21x10^2	0.35	9
6:2:3	0.3	6x10^3	0.58	3
8:2:3	7.59	3.7x10^3	0.66	5.15

3.7 Additional Attempts

3.7.1 Using High-Temperature Annealing

Four other approaches have been tested using a high processing temperature to have a better uniform film and to have better electrical characteristics. The first approach was to check the Al2O3 film behavior if the annealing temperature is reduced by 100 degrees. Depositing three layers of Al2O3 solution on Si/SiO_2 with SiO_2 thickness of 100nm at 3000 rpm for 30s and annealing it for 5 mins at 100C and then for another 5 mins at 250C after each layer. Once the three layers are spin-coated the substrate is then annealed at 250C for 2 hours. Following this procedure resulted in a nonuniform film of Al2O3 over the substrate as shown in Figure 3.10.

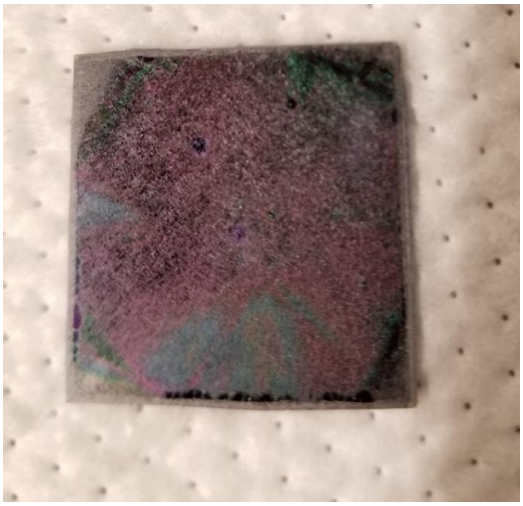

Figure 3.10 Al2O3 film when low-temperature annealing and low annealing period are targeted.

The second approach was targeted to improve the Al2O3 layer as well by using deionized water as a solvent, reducing the thickness of the three deposited layers by increasing the spin coating speed and lowering the processing temperature to 250C. A new Al2O3 solution is made using deionized water as a solvent. Using the new solution three

layers of Al2O3 is spin-coated on Si/SiO_2 with SiO_2 thickness of 100nm at 3000 rpm for 30s. The device is then annealed for 5 mins at 100C and then for another 5 mins at 250C. Once the three layers are spin-coated the substrate is annealed at 250C for 2 hours. Using this solution with this procedure gave a nonuniform film of Al2O3. The following figure shows the result of such a procedure

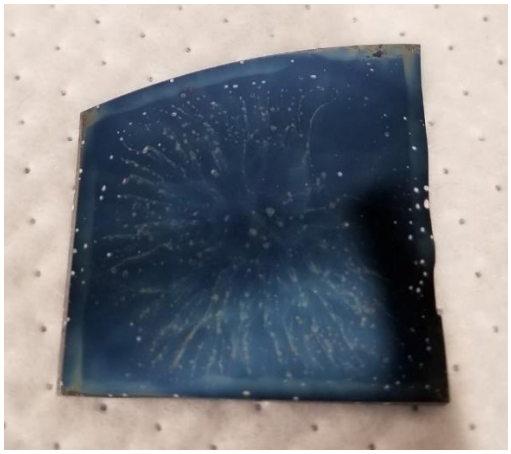

Figure 3.11 Non-uniform IGZO film is observed using deionized water as a solvent.

The third approach aimed at increasing the ON current by depositing two layers of IGZO using the same spin coating rotational speed. We went further to Deposited two layers of 0.1M IGZO instead of one layer. This was targeted as to increase the on current since the ON increases with the increase in the IGZO thickness. The result was that the IGZO film was non-uniform. This non-uniformity deteriorates the source/drain electrode deposition leading to FET devices with abnormal transfer and output characteristics. It was concluded that two-layer IGZO would not lead to high FET performances and thus it was not pursued further. A comparison of one-layer film and two-layer film of IGZO is shown in Figure3.12.

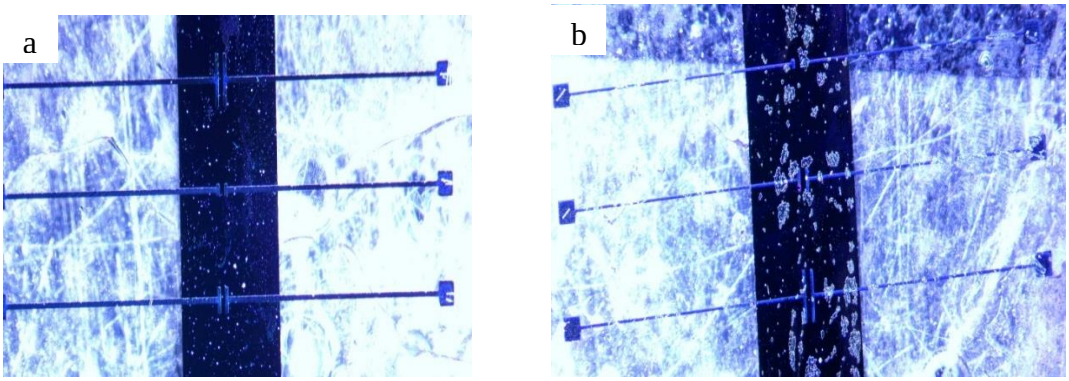

Figure 3.12 Optical image showing (a) one layer IGZO film and (b) two-layer film.

Moreover, the fourth approach aimed at decreasing the leakage and OFF currents by depositing Al_2O_3 on the n^+- Si/SiO_2. This approach was examined because the Al2O3 work as a second dielectric layer covering the pin holes spread on the Si/SiO2 substrate. Using Al2O3 mixture with a higher purity aluminum nitrate hydrate ($In(NO_3)$. $9H_2O$) of 99.997% with 18 hours stirring time and spin coating it at 5000 rpm for 30s on n^+- Si/SiO_2 with a SiO_2 thickness of 100nm has been done. Even though that this approach is expected to yield a lower leakage current, it was still high. Thus, it was concluded that depositing Al_2O3 on SiO_2 without adding any additives results in a lot of big cracks and scratches on the film coated. SEM picture of the film is shown in Figure 3.13.

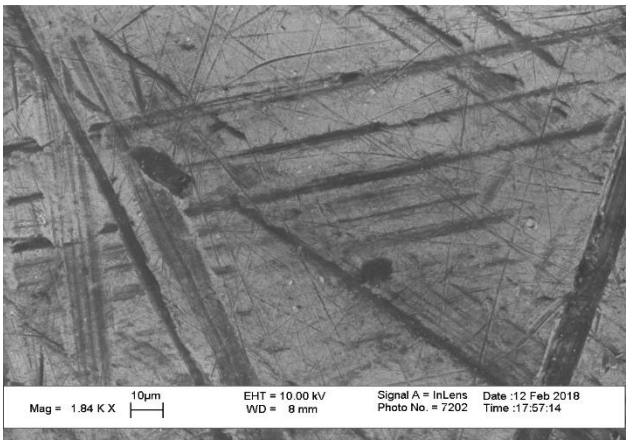

Figure 3.13 SEM picture showing high purity Al2O3 film surface when deposited on SiO2 dielectric layer.

3.7.2 Using Low-Temperature UV-Assisted Annealing

Performing UV assisted inside and outside the N_2 purged environment is another approach that has been done. UV-annealing performed outside the N_2 glovebox is expected to have different effects since oxygen molecules in the air would be excited by high power UV to create ozone molecules whereas this does not occur in the N_2 atmosphere. It has been noticed that UV-assisted annealing done in the air tends to crystallize the Al_2O_3 dielectric film, as shown below in Figure 3.14. These devices showed high gate leakage current dominating the transfer characteristics of the device. It was concluded that UV-assisted annealing should be performed in an air-free environment.

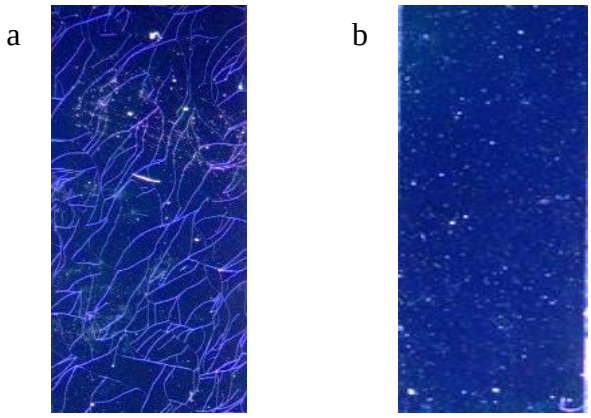

Figure 3.14 Optical image of Al_2O_3 film deposited onto Cr gate electrode after UV-assisted annealing was performed in (a) air and (b) N_2 environment.

3.7.3 Using Different IGZO Composition

Modifying Zn concentration in IGZO has also been tested to understand its' effect on the FET characteristics by increasing the molarity of zinc to 6:2:5. The results of the 6:2:5 solution has been compared with the result of 6:2:3 TFT. The 6:2:5 IGZO had a higher ON current by around one order of magnitude to that in the 6:2:3 but at the same time OFF

current increased by two orders of magnitude. Also, a strong ambipolar characteristic is observed, as shown below in Figure 3.15.

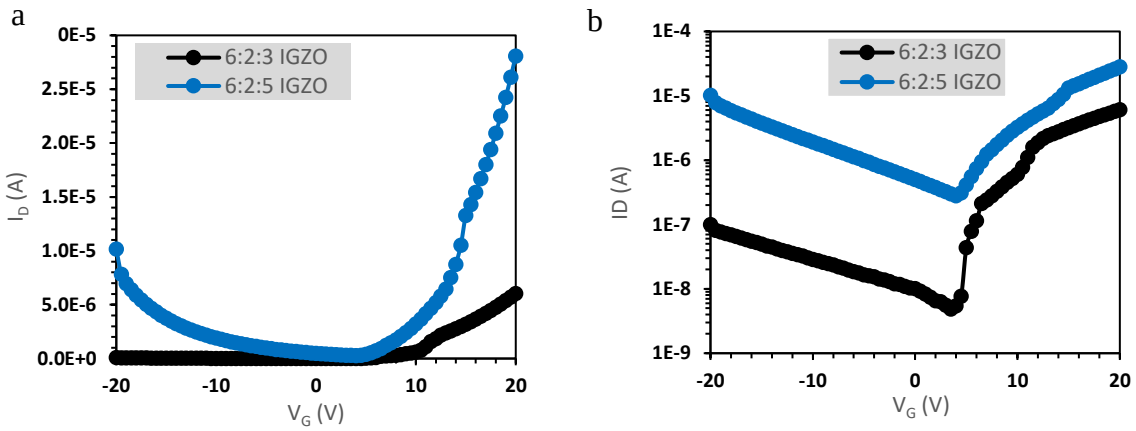

Figure 3.15 Transfer characteristics of 6:2:3 and 6:2:5 IGZO devices where (a) shows the bipolar effect and (b) shows the log plot of the transfer characteristics.

3.8 Conclusion

The focus of this thesis was to examine the electrical performance of low-temperature solution processed IGZO TFTs. The first step was to fabricate the devices using n^+-Si/SiO_2 and glass/Cr/Al_2O_3 based substrates at high annealing temperature. The mobilities of both devices were higher than the traditional a-Si. Thus, the effect of low-temperature UV assisted annealing on glass/Cr/Al_2O_3 was the next objective. The resulted mobility was 1.89 cm^2/Vs which is close to the mobility of the high processing temperature device. Separating UV exposure from the annealing process is then examined which yielded a mobility of 4.69 cm^2/Vs, a higher ON/OFF ratio, and a higher subthreshold swing. This concluded that the separation of UV exposure from the annealing process gives a better TFT performance. In addition, different IGZO compositions have been studied. The ON current, OFF current and mobility decreased when Ga molarity is increased as expected,

however, the subthreshold swing and ON/OFF ratio increased. Moreover, an increase in Indium content has been targeted afterwards to increase the mobility and the ON current. 8:2:3 IGZO TFT is fabricated using spin coating under low processing temperature and gave the best results. It had a mobility of 7.59 cm^2/Vs, ON/OFF ratio of $3.7x10^3$ and a subthreshold swing of 0.66.

It can be concluded from this thesis that the fabrication of IGZO TFTs using solution processed methods, such as spin coating, at low-temperature UV-assisted annealing, can be achieved. Thus, opening the door for printed, transparent and flexible electronics.

3.9 Scope of Future Work

By modifying the annealing procedure and IGZO composition, the ON current reached a value similarly reported in high-performance IGZO FET literature. Currently, the device is limited by high OFF current which predominantly arises from gate leakage in the Al_2O_3 dielectric film. Improving the gate leakage will significantly decrease the OFF current thereby improving the ON/OFF ratio and mobility as well (directing the leakage current to drain will also increase the ON current level and thus the slope in ID-VG curve). Future efforts can be directed to improving Al_2O_3 film processing and improving the device structure.

Another perspective that can be followed is patterning the IGZO to the channel instead of keeping it spread over the whole substrate. Doing so may decrease both leakage and off current by orders of magnitude if the origin of the leakage current is from activating the wide spread film.

REFERENCES

[1] E. Fortunato, P. Barquinha, and R. Martins, *Adv. Mater.* **2012**, *24*, 2945–2986

[2] P. Barquinha et al., *Transparent Oxide Electronics: From Materials to Devices*, 1st Ed., John Wiley & Sons Ltd., Hoboken, **2012**

[3] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors", *Nature*, vol. 432, no. 7016, pp. 488-492, 2004.

[4] J. Jeong, "The status and perspectives of metal oxide thin-film transistors for active matrix flexible displays", *Semiconductor Science and Technology*, vol. 26, no. 3, p. 034008, 2011.

[5] H. Ohara, T. Sasaki, K. Noda, S. Ito, M. Sasaki, Y. Toyosumi, Y. Endo, S. Yoshitomi, J. Sakata, T. Serikawa and S. Yamazaki, "21.3: 4.0 In. QVGA AMOLED Display Using In-Ga-Zn-Oxide TFTs with a Novel Passivation Layer", *SID Symposium Digest of Technical Papers*, vol. 40, no. 1, p. 284, 2009.

[6] J. Jeong, J. Jeong, J. Choi, J. Im, S. Kim, H. Yang, K. Kang, K. Kim, T. Ahn, H. Chung, M. Kim, B. Gu, J. Park, Y. Mo, H. Kim and H. Chung, "3.1: Distinguished Paper: 12.1- Inch WXGA AMOLED Display Driven by Indium-Gallium-Zinc Oxide TFTs Array", *SID Symposium Digest of Technical Papers*, vol. 39, no. 1, p. 1, 2008.

[7] Ito M, Kon M, Miyazaki C, Ikeda N, Ishizaki M, Ugajin Y and Sekine N 2007 *IEICE Trans. Electron.* **E90-C** 2105

[8] Park S-H K, Hwang C-S, Ryu M, Yang S, Byun C, Shin J, Lee J-I, Lee K, Oh M S and Im S 2009 *Adv. Mater.* **21** 678

[9] A. K. Tripathi et al., *Appl. Phys. Lett.* **2011**, *98*, 162102

[10] Y. Kim, J. Heo, T. Kim, S. Park, M. Yoon, J. Kim, M. Oh, G. Yi, Y. Noh and S. Park, "Flexible metal-oxide devices made by room-temperature photochemical activation of sol–gel films", *Nature*, vol. 489, no. 7414, pp. 128-132, 2012.

[11] Park J-S, Kim T, Stryakhilev D, Lee J-S, An S-G, Pyo Y-S, Lee D-B, Mo Y G, Jin D-U and Chung H K 2009 *Appl. Phys. Lett.* **95** 013503

[12] G. A. Salvatore et al., *Nat. Commun.* **2014**, *5*, 2982

[13] W. Lim et al., *Appl. Phys. Lett.* **2010**, *96*, 053510

[14] K. Banger, Y. Yamashita, K. Mori, R. Peterson, T. Leedham, J. Rickard and H. Sirringhaus, "Low-temperature, high-performance solution-processed metal oxide thin-film transistors formed by a ‘sol-gel on chip’ process", *Nature Materials*, vol. 10, no. 1, pp. 45-50, 2010.

[15] H. Yabuta, M. Sano, K. Abe, T. Aiba, T. Den, H. Kumomi, K. Nomura, T. Kamiya and H. Hosono, "High-mobility thin-film transistor with amorphous InGaZnO4 channel fabricated by room temperature rf-magnetron sputtering", *Applied Physics Letters*, vol. 89, no. 11, p. 112123, 2006.

[16] T. Kamiya., *Sci. Technol. Adv. Mater.* **2010**, *11*, 044305

[17] Display Bank, *Transparent Display Technology and Market Forecast*, **2011**

[18] H. Hosono et al., *J. Non-Crystl. Solids* **1996**, *200*, 165

[19] K. Nomura, T. Kamiya, H. Ohta, T. Uruga, M. Hirano and H. Hosono, "Local coordination structure and electronic structure of the large electron mobility amorphous oxide semiconductor In-Ga-Zn-O: Experiment and ab initio calculations", *Physical Review B*, vol. 75, no. 3, 2007.

[20] K. Nomura et al., *Nature*, **2004**, *432*, 488-492

[21] A. Takagi, K. Nomura, H. Ohta, H. Yanagi, T. Kamiya, M. Hirano and H. Hosono, "Carrier transport and electronic structure in amorphous oxide semiconductor, a-InGaZnO4", *Thin Solid Films*, vol. 486, no. 1-2, pp. 38-41, 2005.

[22] Higashi S, Abe D, Hiroshima Y, Miyashita K, Kawamura T, Inoue S and Shimoda T 2002 *Japan. J. Appl. Phys.* **41** 3646

[23] Kamiya T, Durrani Z A K, Ahmed H, Sameshima T, Furuta Y, Mizuta H and Lloyd N 2003 *J. Vac. Sci. Technol.* B **21** 1000

[24] T. Matsuo, S. Mori, A. Ban and A. Imaya, "8.3:Invited Paper: Advantages of IGZO Oxide Semiconductor", *SID Symposium Digest of Technical Papers*, vol. 45, no. 1, pp. 83-86, 2014.

[25] E. Fortunato, P. Barquinha, and R. Martins, *Adv. Mater.* **2012**, *24*, 2945–2986

[26] X. Ding, H. Zhang, J. Zhang, J. Li, W. Shi, X. Jiang and Z. Zhang, "IGZO thin film transistors with Al2O3 gate insulators fabricated at different temperatures ", *Materials Science in Semiconductor Processing*, vol. 29, pp. 69-75, 2015.

[27] Yabuta H, Sano M, Abe K, Aiba T, Den T, Kumomi H, Nomura K, Kamiya T and Hosono H 2006 *Appl. Phys. Lett.* **89** 112123

[28] Y. Rim, H. Lim and H. Kim, "Low-Temperature Metal-Oxide Thin-Film Transistors Formed by Directly Photopatternable and Combustible Solution Synthesis", *ACS Applied Materials & Interfaces*, vol. 5, no. 9, pp. 3565-3571, 2013.

[29] W. Park, I. Son, H. Park, K. Chung, Y. Xu, T. Lee and Y. Noh, "Facile Routes To Improve Performance of Solution-Processed Amorphous Metal Oxide Thin Film Transistors by Water Vapor Annealing", *ACS Applied Materials & Interfaces*, vol. 7, no. 24, pp. 13289-13294, 2015.

[30] J. Heo, J. Jo, J. Kang, C. Jeong, H. Jeong, S. Kim, K. Kim, H. Kwon, J. Kim, Y. Kim, M. Kim and S. Park, "Water-Mediated Photochemical Treatments for Low-Temperature Passivation of Metal-Oxide Thin-Film Transistors", *ACS Applied Materials & Interfaces*, vol. 8, no. 16, pp. 10403-10412, 2016.

[31] D. Neamen, *Semiconductor physics and devices*. New York: McGraw-Hill, 2012.

[32] S. M. Sze, K. K. Ng, *Physics of semiconductor devices*, John wiley & sons, 2006

[33] E. Fortunato, P. Barquinha, R. Martins, *Adv. Mater.* **2012**, *24*, 2945.

[34] C. R. Kagan and P. Andry, *Thin-film transistors*. Marcell Dekker, Inc., 2003.

[35] M. J. Powell, "The physics of amorphous-silicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 36, pp. 2753-2763, December 1989.

[36] J.-H. Lee, D. N. Liu, S.-T. Wu, *Introduction to flat panel displays*, Vol. 20, John Wiley & Sons, 2008.

[37] A. C. Tickle, *Thin-film transistors: a new approach to microelectronics*, John Wiley & Sons, 1969.

[38] Y. Mastai, *Advances in crystallization processes*. Rijeka, Croatia: InTech, 2012.

[39] H. Hosono, M. Yasukawa, H. Kawazoe, J. *Non-Cryst. Solids* 1996, 203, 334.

[40] Y. Kim, M. Han, J. Han and S. Park, "Effect of Metallic Composition on Electrical Properties of Solution-Processed Indium-Gallium-Zinc-Oxide Thin-Film Transistors", *IEEE Transactions on Electron Devices*, vol. 57, no. 5, pp. 1009-1014, 2010.

[41] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, H. Hosono, *Nature* 2004, 432, 488.

[42] Kamiya T and Hosono H 2010 *NPG Asia Mater.* **2** 1522

[43] H. Fritzsche, K.-J. Chen, *Physical Review B* **1983**, *28*, 4900.

[44] Fritzsche H and Chen K-J 1983 *Phys. Rev.* B **28** 4900

[45] Hoffman, R. L. "ZnO-channel thin-film transistors: Channel mobility." Journal of Applied Physics 95.10 (2004): 5813-5819.

[46] J. F. Wager, B. Yeh, R. L. Hoffman, D. A. Keszler, *Curr. Opin. Solid State Mater. Sci.* **2014**, *18*, 53.

[47] E. Fortunato, P. Barquinha, R. Martins, *Adv. Mater.* **2012**, *24*, 2945.

[48] K. Nomura, A. Takagi, T. Kamiya, H. Ohta, M. Hirano, H. Hosono, *Jpn. J. Appl. Phys.* **2006**, *45*, 4303.

[49] T. Kamiya, H. Hosono, *NPG Asia Mater.* **2010**, *2*, 15.

[50] E. J. Bae, Y. H. Kang, M. Han, C. Lee, and S. Y. Cho, "Soluble oxide gate dielectrics prepared using the self-combustion reaction for high-performance thin- film transistors," *J. Mater. Chem. C*, vol. 2, no. 28, p. 5695, 2014.

[51] H. Tan, G. Liu, A. Liu, B. Shin, and F. Shan, "The annealing effects on the properties of solution-processed alumina thin film and its application in TFTs," *Ceram. Int.*, pp. 1–7, 2015.

[52] S. Dutta, A. Pandey, I. Yadav, O. P. Thakur, A. Kumar, R. Pal, and R. Chatterjee, "Growth and electrical properties of spin-coated ultrathin ZrO2 films on silicon," *J. Appl. Phys.*, vol. 114, no. 1, p. 014105, Jul. 2013.

[53] G. X. Liu, A. Liu, F. K. Shan, Y. Meng, B. C. Shin, E. Fortunato, and R. Martins, "High-performance fully amorphous bilayer metal-oxide thin film transistors using ultra-thin solution-processed ZrOx dielectric," *Appl. Phys. Lett.*, vol. 105, no. 11, p. 113509, Sep. 2014.

[54] L. Xifeng, X. Enlong, and Z. Jianhua, "Low-Temperature Solution-Processed Zirconium Oxide Gate Insulators for Thin-Film Transistors," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3413–3416, Oct. 2013.

[55] G. D. Wilk, R. M. Wallace, and J. M. Anthony, "High-k gate dielectrics: Current status and materials properties considerations," *J. Appl. Phys.*, vol. 89, no. 10, pp. 5243–5275, 2001.

[56] P. Barquinha, L. Pereira, G. Gonçalves, D. Kuscer, M. Kosec, A. Vilà, A. Olziersky, J. R. Morante, R. Martins, and E. Fortunato, “Low-temperature sputtered mixtures of high-κ and high bandgap dielectrics for GIZO TFTs,” *J. Soc. Inf. Disp.*, vol. 18, no. 10, p. 762, 2010.

[57] Y. M. Park, A. Desai, A. Salleo, and L. Jimison, “Solution-Processable Zirconium Oxide Gate Dielectrics for Flexible Organic Field Effect Transistors Operated at Low Voltages,” *Chem. Mater.*, vol. 25, no. 13, pp. 2571–2579, Jul. 2013.

[58] Y. Su, C. Wang, W. Xie, F. Xie, J. Chen, N. Zhao and J. Xu, "Low-Voltage Organic Field-Effect Transistors (OFETs) with Solution-Processed Metal-Oxide as Gate Dielectric", *ACS Applied Materials & Interfaces*, vol. 3, no. 12, pp. 4662-4667, 2011.

[59] C. Avis, H. Hwang and J. Jang, "Effect Of Channel Layer Thickness On The Performance Of Indium–Zinc–Tin Oxide Thin Film Transistors Manufactured By Inkjet Printing", *ACS Applied Materials & Interfaces*, vol. 6, no. 14, pp. 10941- 10945, 2014.

[60] K. Yim, Y. Yong, J. Lee, K. Lee, H.-H. Nahm, J. Yoo, C. Lee, C. Seong Hwang, and S. Han, “Novel high-κ dielectrics for next-generation electronic devices screened by automated ab initio calculations,” *NPG Asia Mater.*, vol. 7, no. 6, p. e190, Jun. 2015.

[61] E. Fortunato, P. Barquinha, and R. Martins, *Adv. Mater.* **2012**, *24*, 2945–2986

[62] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors", *Nature*, vol. 432, no. 7016, pp. 488-492, 2004.

[63] Sunde, Tor Olav Løveng, et al. "Transparent and conducting ITO thin films by spin coating of an aqueous precursor solution." Journal of Materials Chemistry 22.31(2012): 15740-15749.

[64] Pasquarelli, Robert M., David S. Ginley, and Ryan O'Hayre. "Solution processing of transparent conductors: from flask to film." Chemical Society Reviews 40.11 (2011): 5406-5441.

[65] Lee, Ji-Hoon, et al. "Improved mechanical performance of solution-processed MWCNT/Ag nanoparticle composite films with oxygen-pressure-controlled annealing." Carbon 50.1 (2012): 98-106.

[66] Song, Keunkyu, et al. "Solution-processable tin-doped indium oxide with a versatile patternability for transparent oxide thin film transistors." Journal of Materials Chemistry 21.38 (2011): 14646-14654.

[67] J. S. Heo, J. W. Jo, J. Kang, C. Y. Jeong, H. Y. Jeong, S. K. Kim, K. Kim, H. I. Kwon, J. Kim, Y. H. Kim, M. G. Kim, S. K. Park, *ACS Appl. Mater. Interfaces* **2016**, *8*, 10403.

[68] Scriven, L. E. "Physics and applications of dip coating and spin coating." *MRS proceedings*. Vol. 121. Cambridge University Press, 1988.

[69] Raut, Hemant Kumar, et al. "Anti-reflective coatings: A critical, in-depth review." Energy & Environmental Science 4.10 (2011): 3779-3804.

[70] Girotto, Claudio, et al. "Exploring spray coating as a deposition technique for the fabrication of solution-processed solar cells." *Solar energy materials and solar cells* 93.4 (2009): 454-458.

[71] Ohara, Taku, Yoichiro Matsumoto, and Hideo Ohashi. "The film formation dynamics in spin coating." Physics of Fluids A: Fluid Dynamics (1989-1993) 1.12 (1989): 1949-1959.

[72] Kim, Si Joon, Seokhyun Yoon, and Hyun Jae Kim. "Review of solutionprocessed oxide thin-film transistors." Japanese Journal of Applied Physics 53.2S (2014): 02BA02.

[73] Y. H. Kim, J. S. Heo, T. H. Kim, S. Park, M. H. Yoon, J. Kim, M. S. Oh, G. R. Yi, Y. Y. Noh, S. K. Park, " *Nature* **2012**, *489*, 128.

[74] S. Chang and B. Ju, "Ultraviolet and visible light detection characteristics of amorphous indium gallium zinc oxide thin film transistor for photodetector applications", *International journal of advanced smart convergence*, vol. 1, no. 1, pp. 61-64, 2012.

[75] H. Lu, Y. Chueh, T. Tseng, C. Wang and C. Chaou, "Application of Amorphous Indium Gallium Zinc Oxide Thin Film Transistor Biosensors in Creatine Kinase Detection", *Procedia Technology*, vol. 27, pp. 258-259, 2017.

[76] K. Umeda, M. Uenuma, D. Senaha, J. Felizco, Y. Uraoka and H. Adachi, "Amorphous Thin Film for Thermoelectric Application", *Journal of Physics: Conference Series*, vol. 1052, p. 012016, 2018.

[77] J. Kim, E. Park, M. Kim, H. Cho, D. Lee, J. Kim, Y. Khang, K. Park and Y. Kim, "Bias and illumination instability analysis of solution-processed a-InGaZnO thin- film transistors with different component ratios", *Thin Solid Films*, vol. 645, pp. 154-159, 2018.

[78] "On the Origin of Improved Charge Transport in Double-Gate In–Ga–Zn–O Thin- Film Transistors: A Low-Frequency Noise Perspective - IEEE Journals & Magazine", *Ieeexplore.ieee.org*, 2018. [Online]. Available: https://ieeexplore.ieee.org/abstract/document/7192611/. [Accessed: 12- Sep- 2018].

[79] W. Xu, H. Wang, F. Xie, J. Chen, H. Cao and J. Xu, "Facile and Environmentally Friendly Solution-Processed Aluminum Oxide Dielectric for Low-Temperature, High-Performance Oxide Thin-Film Transistors", *ACS Applied Materials & Interfaces*, vol. 7, no. 10, pp. 5803-5810, 2015.

[80] Van de Leest, R. E. UV photo-annealing of thin sol-gel films. Appl. Surf. Sci. 86, 278–285 (1995).

[81] Imai, H. in Handbook of Sol-Gel Science and Technology: Processing, Characterization and Applications Vol. 1 (ed. Sakka, S.) 639–650 (Kluwer, 2005).

[82] Clark, T. Jr. et al. A new application of UV-ozone treatment in the preparation of substrate-supported, mesoporous thin films. Chem. Mater. 12, 3879–3884 (2000).

[83] Imai, H., Tominaga, A., Hirashima, H., Toki, M. & Asakuma, N. Ultraviolet-reduced reduction and crystallization of indium oxide films. J. Appl. Phys. 85, 203– 207 (1999).

[84] Park, Y. M., Daniel, J., Heeney, M. & Salleo, A. Room-temperature fabrication of ultrathin oxide gate dielectrics for low-voltage operation of organic field effect transistors. Adv. Mater. 23, 971–974 (2011).