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## ABSTRACT

### EXPERIMENTAL AND THEORETICAL EVALUATION OF IN-DEPTH DAMAGE DISTRIBUTION IN SAWN SILICON WAFERS

by  
**Srinivasamurthy Devayajanam**

As-sawn silicon wafers have surface damage that needs to be removed before any further processing into solar cells. This damage distribution can vary with cutting parameters such as wire size, slurry particle/diamond grit size, and wire usage. To date, there is no simple way to measure the degree of damage, damage depth, and damage distribution. But, this information is needed by the wafer manufacturers as well as solar cell manufacturers.

A technique based on sequential etching of silicon wafers and minority carrier lifetime ( $\tau_{\text{eff}}$ ) measurements is used to determine damage depth. In this technique, samples are sequentially etched to remove thin layers from each surface and minority carrier lifetime is measured after each etch step. Lifetime increases after each layer of damage is removed and reaches a plateau once the damage is totally removed. The thickness-removed at which the lifetime reaches a peak value corresponds to the damage depth. An accurate measurement of  $\tau_{\text{eff}}$  requires corrections to optical reflection, and transmission from silicon wafers to account for changes in the surface morphology and in the wafer thickness. This technique also allows the in-depth distribution of the damage to be quantified in terms of surface recombination velocity (SRV).

Although this method is routinely used at the National Renewable Energy Laboratory to measure damage depth, determination of damage distribution from these data requires an accurate model that converts the minority carrier lifetime data into carrier

recombination distribution. Continuity equation for excess minority carrier density ( $\Delta n$ ) is solved for the material of interest (silicon wafer with surface damage layer), and carrier concentration is integrated and normalized to match the normalized lifetime vs thickness removed curve. A simplified model for determining the recombination distribution within a wafer having surface damage is presented. Potential improvements for this model are discussed.

**EXPERIMENTAL AND THEORETICAL EVALUATION OF IN-DEPTH  
DAMAGE DISTRIBUTION IN SAWN SILICON WAFERS**

by  
**Srinivasamurthy Devayajanam**

**A Dissertation  
Submitted to the Faculty of  
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Doctor of Philosophy in Materials Science and Engineering  
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**EXPERIMENTAL AND THEORETICAL EVALUATION OF IN-DEPTH  
DAMAGE DISTRIBUTION IN SAWN SILICON WAFERS**

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Dedicated to my mother, Lalitha Kumari Devayajanam  
and father, (Late) Venkata Rama Charyulu Devayajanam

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## LIST OF SYMBOLS

$\alpha$	Absorption coefficient
$\tau$	Minority carrier lifetime
$\Phi$	Light flux
$\Omega$	Resistivity
$\lambda$	Wavelength of light
©	Copyright
Å	Angstrom( $10^{-10}$ meters)
R	Reflectance
°C	Degrees Celsius
T	Transmittance
D	Diffusion coefficient
S	Surface recombination velocity

## LIST OF ABBREVIATIONS

Si	Silicon
Cz	Czochralski
FZ	Float zone
SiC	Silicon Carbide
ID	Inner diameter
OD	Outer diameter
SWC	Slurry wire cutting
DWC	Diamond wire cutting
TTV	Total thickness variation
PCD	Photoconductance decay
$\mu$ W	Microwave
$\mu$ S	Microseconds
SEM	Scanning electron microscopy
TEM	Transmission electron microscopy
XRD	X-ray diffraction
SRV	Surface recombination velocity

# **CHAPTER 1**

## **INTRODUCTION**

Silicon is the most widely used material in both photovoltaic and semiconductor industries. Silicon is grown in a variety of methods and, currently Czochralski (Cz) and Float-Zone (FZ) are the predominantly used crystal pulling techniques utilized by the industry to grow crystalline silicon ingots. Sawing is a process step required to cut a silicon ingot or a boule into bricks/wafers, and these wafers will then be used for device fabrication after a multitude of preparation steps. Sawing itself constitutes a large amount of material loss. Because silicon is a hard and brittle material, any cutting/sawing action results in a surface and subsurface damage that must be removed before a device is fabricated using it, resulting in additional material loss. This combined material loss due to cutting (kerf loss) and wafer preparation (damage removal) constitutes about half of the Si ingot. Hence, it is important to minimize the material loss, and the added costs associated with sawing and wafer preparation.

In this Chapter, an overview of silicon ingot sawing is presented. Subsequently, surface damage caused by sawing, including a detailed account of the types of surface damage and their origins are discussed. Finally, the need for an accurate evaluation of surface damage is elucidated.

### **1.1 Silicon Sawing**

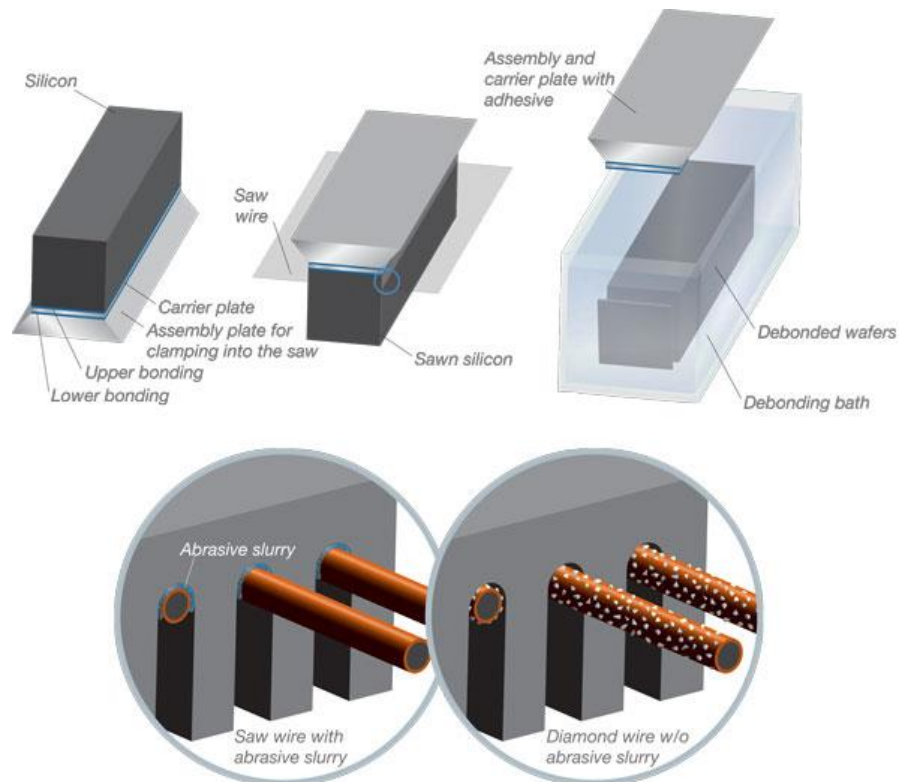
Many ingot sawing methods viz. outside diameter (OD) cutting, inside diameter (ID) cutting, and multi-wire sawing have evolved over the last 50 years with the objectives of

minimizing the kerf loss, making thinner wafers of uniform thickness, and minimizing the sub-surface damage (Herring, 1976; Kachajian, 1972; Lane, 1985; Tonshoff et al., 1997; Pauli, 2005). Although, multi-wire sawing methods are slower (half a day per cutting cycle), they offer lower kerf loss and high throughput because of their ability to cut larger ingot lengths (Wu, PhD thesis, 2012). Slurry wire cutting (SWC), a multi-wire sawing method uses steel wire and silicon carbide (SiC) particles in oil or ethylene glycol solution (most often referred to as slurry) as the abrasive medium. It has been the industry standard for silicon ingot sawing for more than a decade now (Moller, 2006), (Liedke et al., 2011). However, a newer technique consisting of diamond wire cutting (DWC) (using diamond abrasive particles (grit) patched to a copper alloy or resin on a metal wire), is garnering interest in both research community and industry, particularly for photovoltaic ingot slicing (X Yu et al., 2012). Figure 1.1 is an illustration of the slurry wire cutting and diamond wire cutting processes.

This new diamond impregnated wire is deemed to provide high throughput with a reasonable total thickness variation (TTV), low surface roughness, low kerf, and comparable or low surface damage values to that of slurry wire cutting. In this thesis work, focus will be on the determination of in-depth damage caused on crystalline silicon wafers cut by multi-wire sawing methods only.

The sawing and the wafer preparation must be considered together. For example, aggressive cutting to increase the throughput can increase the kerf loss as well as the surface damage. On the other hand, under etching/texturing/polishing performed in an attempt to reduce kerf may leave some residual damage on the device surface, which can

lead to a high surface recombination, defect generation during high temperature processing and concomitant degradation in device performance.



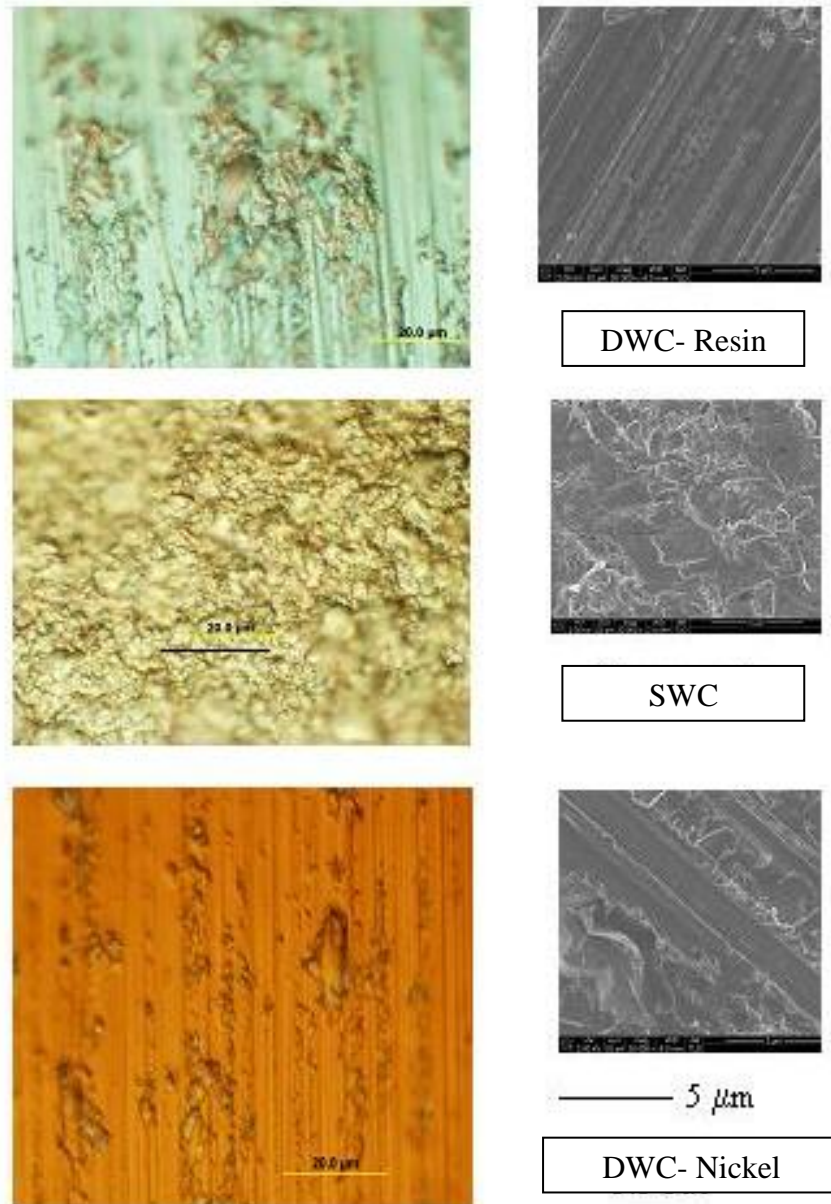
**Figure 1.1** Illustrations of SWC and DWC sawing techniques.

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## 1.2 Surface and In-depth Damage Caused by Sawing

Wire sawing (both SWC and DWC) produces surface damage and in-depth damage (which is several microns deep) on the wafers. The chipping or “tearing away” of small pieces of silicon from the path of the saw wire/grit is a micro-cleavage process. This can be seen in optical and SEM images of the as-sawn surfaces shown in Figure 1.2. This damage would be responsible for the wafer breakage because of micro cracks induced,

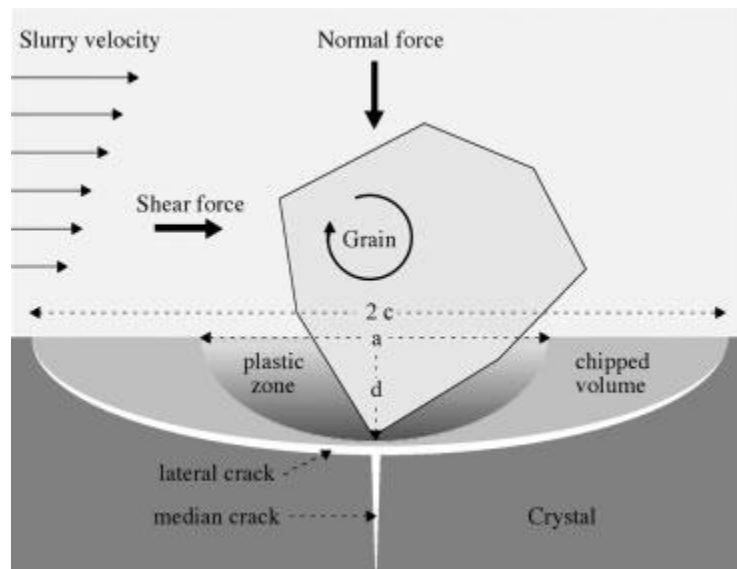
uneven wafer surface and residual damage if the wafer is not properly etched [Wu et al., 2012].



**Figure 1.2** Optical and SEM images showing lower and higher magnification images of the saw patterns/marks in DWC-Resin cut, slurry cut, and DWC-Nickel cut wafers (Sopori et al., 2013).

In SWC mechanism, the surface roughness ( $R_z$ ) is approximately equal to the indentation depth ( $d$ ) of the grains (or grit) and the extension of the damage zone equals the mean length of the crack ( $c$ ) [defined in Equation 1.1] generated by that grain and is shown in Figure 1.3 (Moller et al., 2004).

$$c = (\gamma\beta I_0 d / K_{IC})^{2/3} \quad (1.1)$$



**Figure 1.3** Illustration of a single grain indentation in silicon, also showing various crack types (Moller et al , 2004).

There are several other parameters viz. wire velocity/feed rate (Wurzner et al., 2015), cutting rate/down feed rate, force applied on the ingot/brick or the tension in wire, wire/grit usage (Bidiville, PhD Thesis, 2010), and wire reciprocation (back and forth motion used in multi-wire cutting methods) which determine the final damage depth and distribution in a wafer.

Silicon wafer manufacturers are rapidly moving from slurry wire cutting method to a more economical and environmental friendly diamond wire cutting for ingot slicing.

This brings a new set of issues to deal with viz. surface morphology (on contrary, very uniform for slurry cut), different depths and distributions of damage. However, newer etching methodologies can help resolve some of these issues. Recently, in 2014, it has been reported that the round run fringes caused by back and forth motion of the cutting wire can be completely removed from wafer surface by a new etching technique called vapor blast etching (Chen et al., 2014).

Surface damage caused by wire sawing on silicon wafers can be broadly categorized into two types.

(a) Superficial/surface damage, which can be classified into

(i) Roughness

(ii) Morphology (or phase transformation), and

(b) Sub-surface or in-depth damage, which can further be classified into

(i) Micro-cracks,

(ii) Periodic features (striations),

(iii) Stress and Dislocations.

Origins of these damage varieties and their quantitative representations are described in the following Sections.

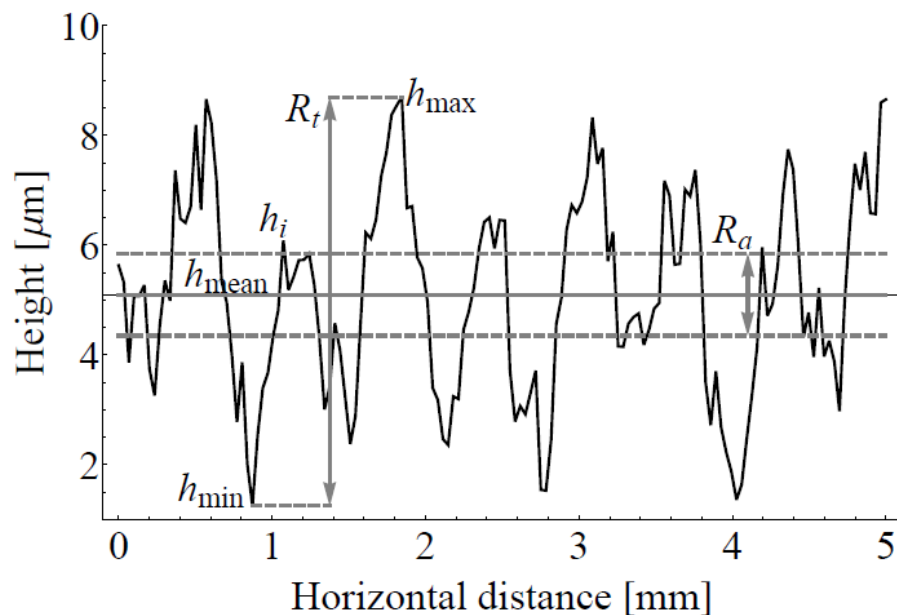
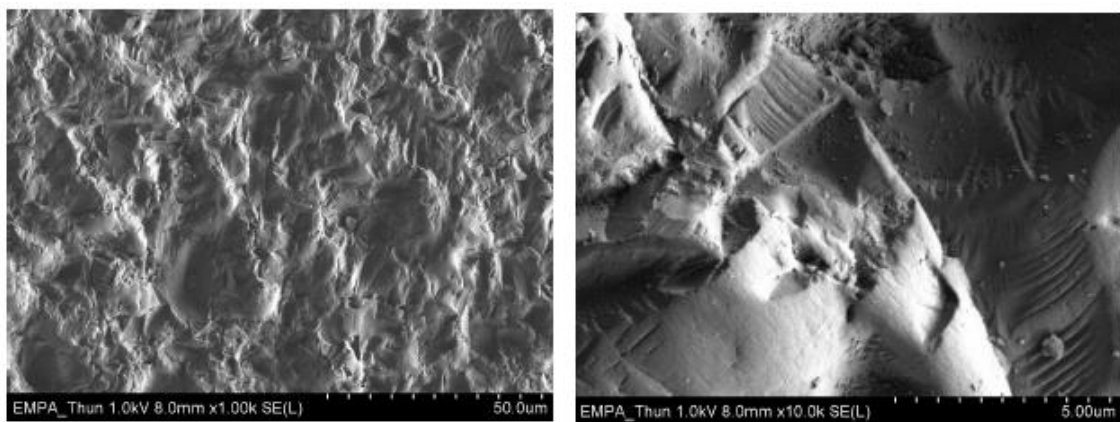
### **1.2.1 Roughness**

Surface roughness generation is an inherent macroscopic phenomenon associated with silicon ingot sawing. Figure 1.4 (a) and (b) depict the surface roughness caused by sawing. The average variation in height (i.e perpendicular to the large wafer plane)  $R_a$  [defined in Equation 1.2, (Wu, PhD thesis, 2012), and total roughness ( $R_t$ = peak to valley



difference, see Figure 1.4 (c)] are good measures of roughness and constant efforts are made by saw manufacturers to keep these values always under a few microns. The lower the  $R_a$  and  $R_t$  values, better the cutting method.

$$R_a = \frac{\sum_{i=1}^n |h_i - h_{mean}|}{n} \quad (1.2)$$



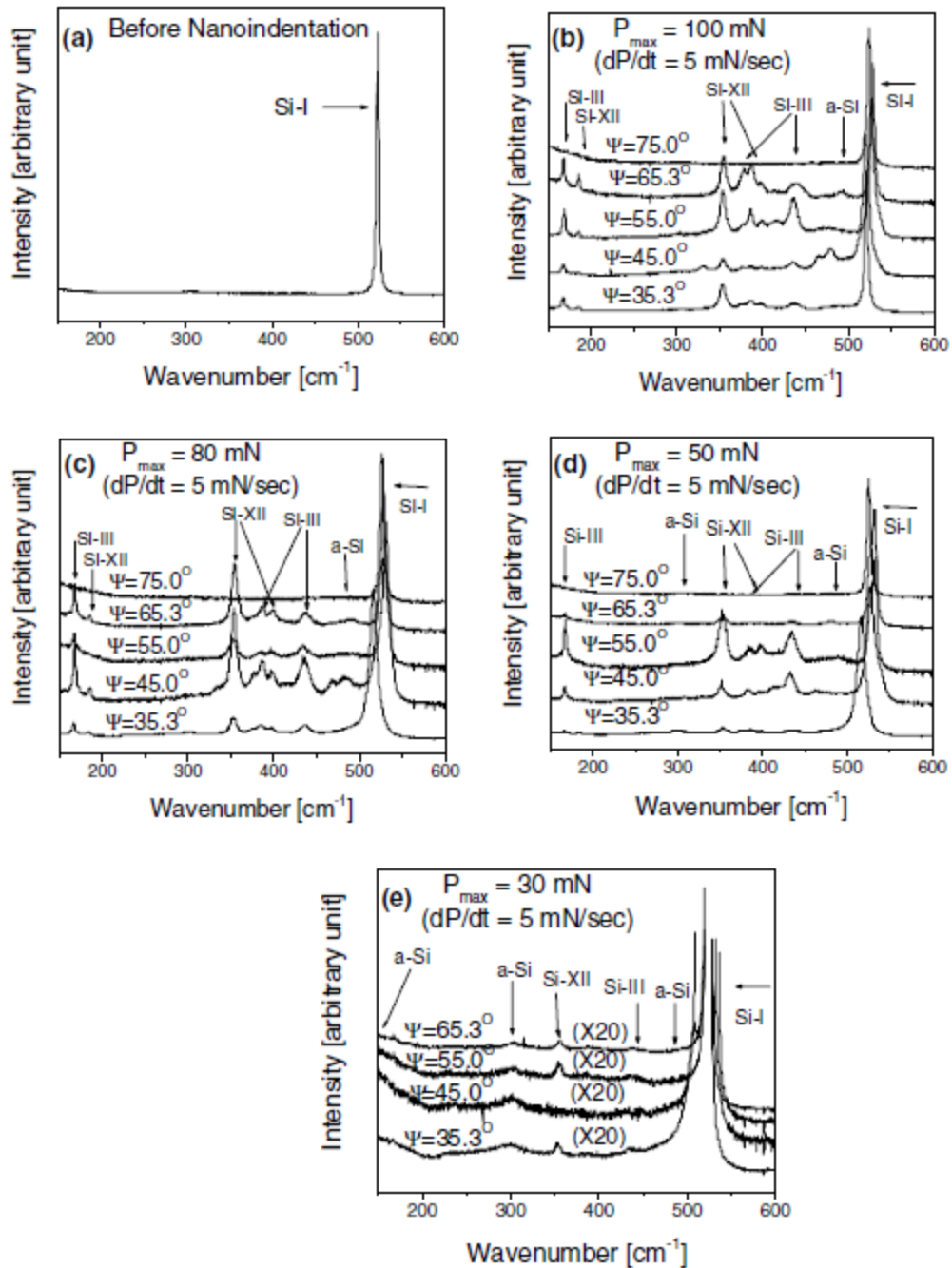
**Figure 1.4** SEM images showing surface roughness in (a) lower and (b) higher magnification. (c) Schematic of surface roughness and various terms associated (Wu, PhD thesis, 2012).

In multi-wire sawing methods, roughness generated depends on various parameters such as wire size, grit size, and cutting speed etc. Roughness is undesirable as it increases the amount of silicon material that needs to be removed before device fabrication. Measurements performed by Chen et al. (2010) on surface roughness of wafers sawn by SWC and DWC methods imply that the DWC is a better cutting mechanism because of less roughness it leaves on the wafer.

Studies by Wefringhaus et al. (2013) show that there is a direct correlation between the inhomogeneities in surface roughness of the as-cut wafers and the isotextured wafers. Wafer sawing process is attributed for this inhomogeneity. Roughness variation on isotextured wafers influences cell appearance (homogeneity of silicon nitride thickness / color), electrical performance will suffer from non-uniformities in reflection.

### **1.2.2 Morphology or Phase Transformation**

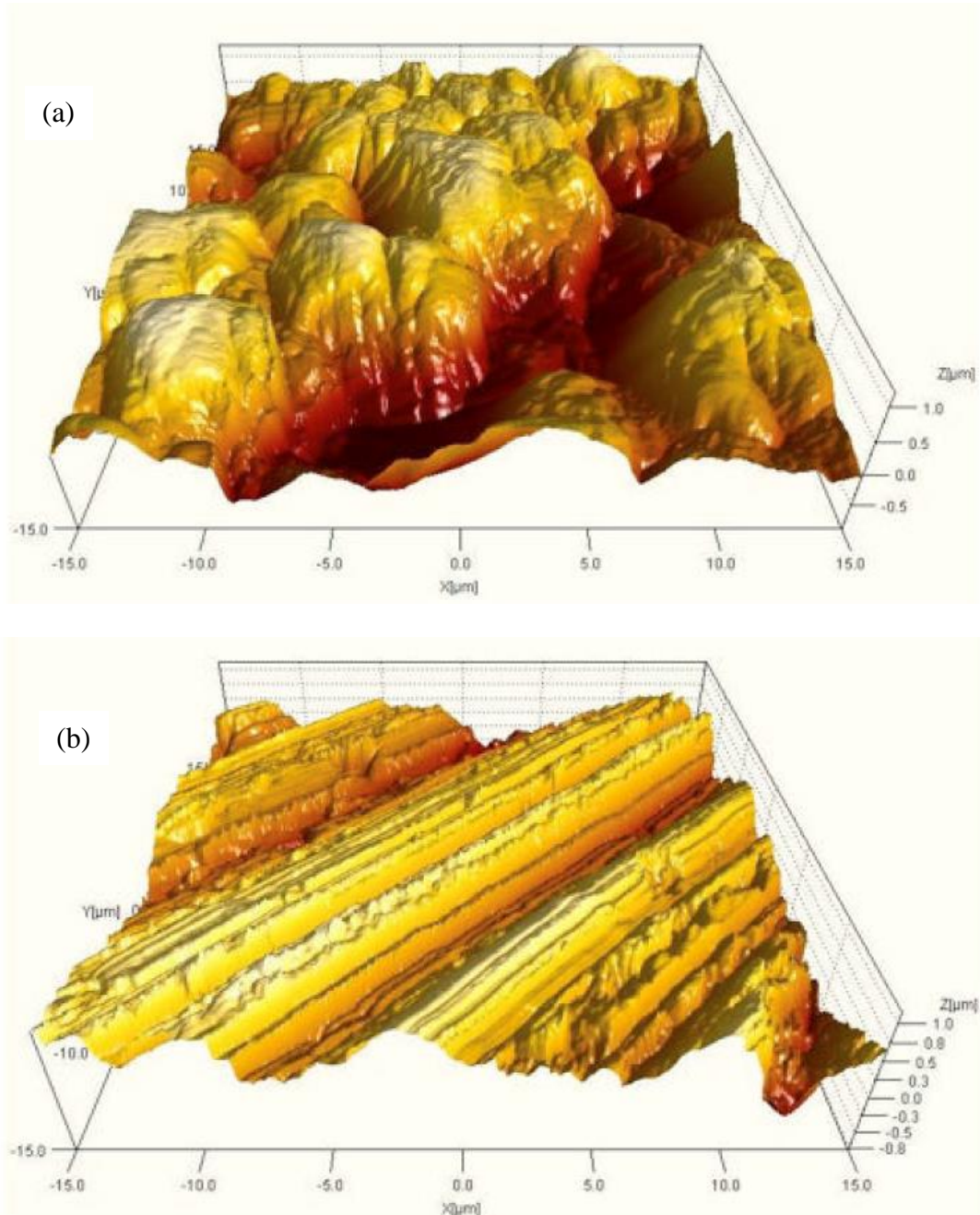
It is known that the local stress during multi-wire sawing (either SWC or DWC) cutting process can exceed few hundred MPa, and as a result of this large stress, silicon wafers are expected to experience lattice damage in the form of crystal defects such as dislocations as well as phase transformation (Yu et al., 2012; Bidiville, PhD thesis, 2010; Bidiville et al., 2009), similar to those observed in the case of micro-indentation (Domnich et al., 2002; Jian et al., 2010; Jang et al., 2005) or nano-scratching (Gassiloud, 2005) as seen in Figure 1.5.



**Figure 1.5** Raman spectra of crystalline silicon wafers surfaces indented with various indenters (of varying indenter angle  $\psi$ ) at various maximum loads (Jang et al., 2005).

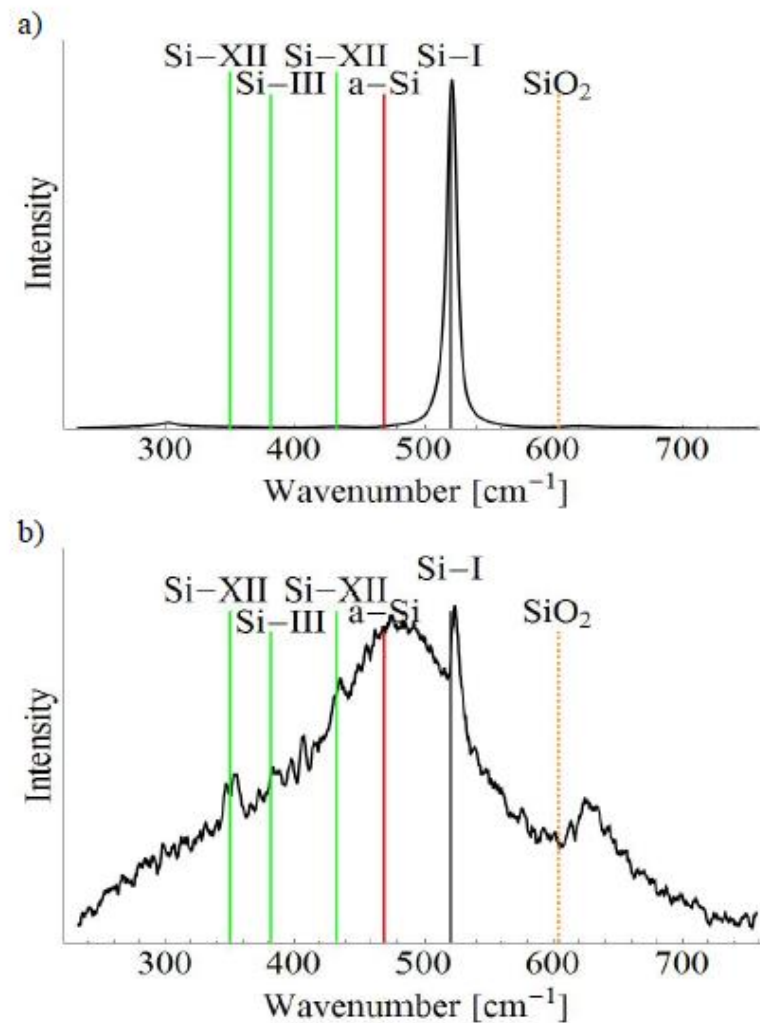
Since the SWC process is a three body abrasion process, it results in chipping of the wafer surface and, on the contrary, the two body abrasion process in DWC method

results in grooving of the wafer surface and occasional chipping (Moller, 2004). Atomic Force Microscopy performed on the wafers cut using these two kinds of sawing methods illustrates the difference [see Figure 1.6].



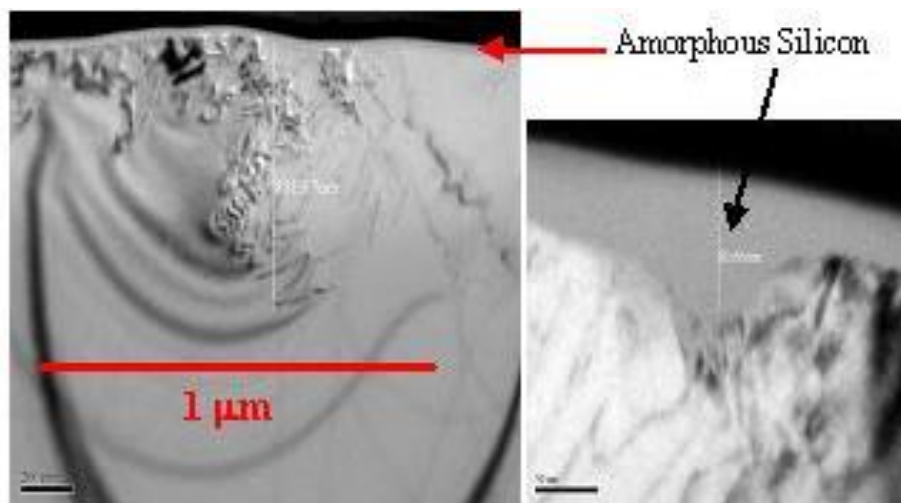
**Figure 1.6** AFM images of (a) SWC wafer and (b) DWC wafer (Holt et al., 2010).

The chipped off region on the surface preserves its crystalline form whereas the abraded or grooved region undergoes phase transformation and the same can be confirmed using Raman spectroscopy. Figure 1.7 is a Raman spectrum obtained from two different regions (chipped off and abraded) on a silicon wafer cut using DWC method. A multitude of silicon phases are observed in the grooved region whereas the signal from chipped region is that of crystalline silicon.



**Figure 1.7** Raman spectra of (a) chipped-off region (b) a smooth groove (Bidiville et al., 2009).

It is observed that commercial multi-wire sawing generates very shallow amorphous phase transformation damage (typically of the order of a few nm to a micrometer) and hence is not a significant contributor to the kerf loss. Figure 1.8 is a cross-sectional TEM image that shows the local damage by diamond wire sawing. It shows two important features: (i) a thin (50 -100 nm deep) amorphous region at the surface, and (ii) dislocation networks that can be nearly 1 $\mu\text{m}$  deep below the cutting surface. The amorphous phase is determined by a lack of diffraction pattern from this region, and occurs in all sawn samples. This amorphous phase present on the wafer surface can alter the etch parameters and in-turn change the way the wafers are etched (Holt et al., 2010).



**Figure 1.8** A cross-sectional TEM image of a DWC wafer sample showing formation of dislocation loops that are about 1  $\mu\text{m}$  deep and a layer of amorphous phase going to a depth of 0.8  $\mu\text{m}$  (Sopori et al., 2013).

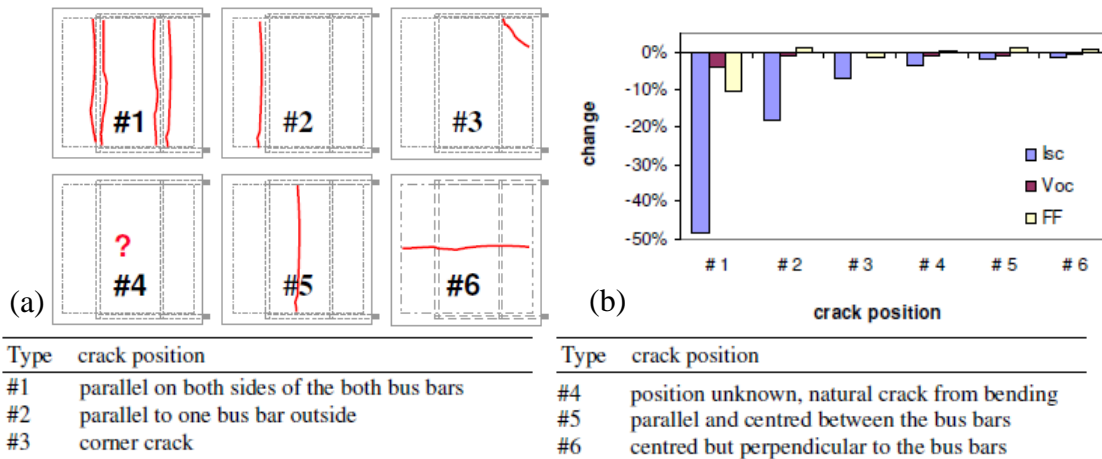
### 1.2.3 Micro-Cracks

Micro-cracks generated during sawing are several microns deep. By improper handling, they propagate during processing and negatively affect the mechanical strength of the wafer and electrical parameters of the cell made using that wafer. Length of the micro-



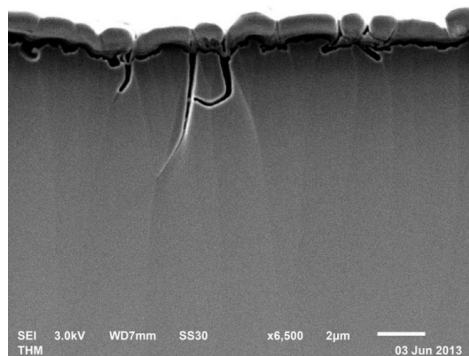
cracks and their position in the wafer are very critical in determining this effect.

Figure 1.9 shows the positions of various cracks and their impact on cell parameters.



**Figure 1.9** (a) Illustrations of single cell modules with different crack positions initiated manually, (b) change in cell parameters with respect to the crack position (note- Crack locations are numbered and described in the same figure) (Grunow et al., 2005).

Attempts have been made to detect the micro-cracks, and evaluate the relationship between the crack-length, their density and mechanical strength of the wafer (Abdelhamid et al., 2014; Demant et al., 2014; Trautmann et al., 2011). Figure 1.10 is an SEM micrograph of micro-cracks generated in a DWC wafer during sawing.



**Figure 1.10** SEM image of an as-sawn silicon wafer sample showing micro-cracks propagating into the wafer bulk (scale 2 µm).

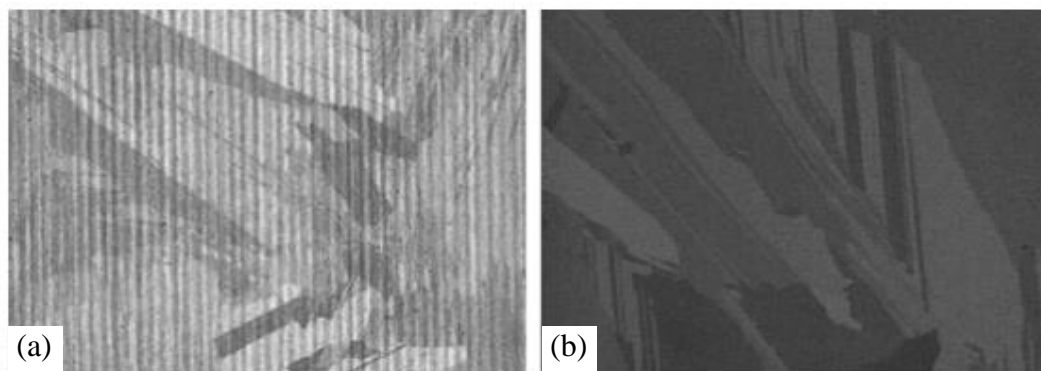
Source- <https://www.ise.fraunhofer.de/en/business-areas/silicon-photovoltaics/research-topics/feedstock-crystallization-and-wafering/projects/completed-projects/diasip-silicon-wafer-production-with-diamond-coated-sawing-wire>, retrieved, June25, 2015.

It is known that micro-cracks generated at the edge and surface are more deleterious, and in order to prevent the wafers from breakage during cell processing, specific amount of silicon has to be etched away from each wafer surface (Perez et al., 2009) to ensure complete damage removal.

Although there exists a vast variety of experimental techniques to detect the micro-cracks in silicon wafer, limitations such as minimum crack length required, and interference with scratches inhibit their reliable use. A comparison of these techniques for micro-crack detection is given by Abdelhamid et al. (2014).

#### 1.2.4 Periodic Features or Striations

Striations are stripe like features which run across the wafer along the cutting wire direction and are the most commonly and immediately noticeable feature of DWC. Often there is a height variation of a few microns associated with these striations and these are spaced a few hundreds of microns apart. Figure 1.11 shows typical striation patterns observed on a mc-Si wafer cut using DWC method; a wafer cut with SWC method is also shown for comparison.

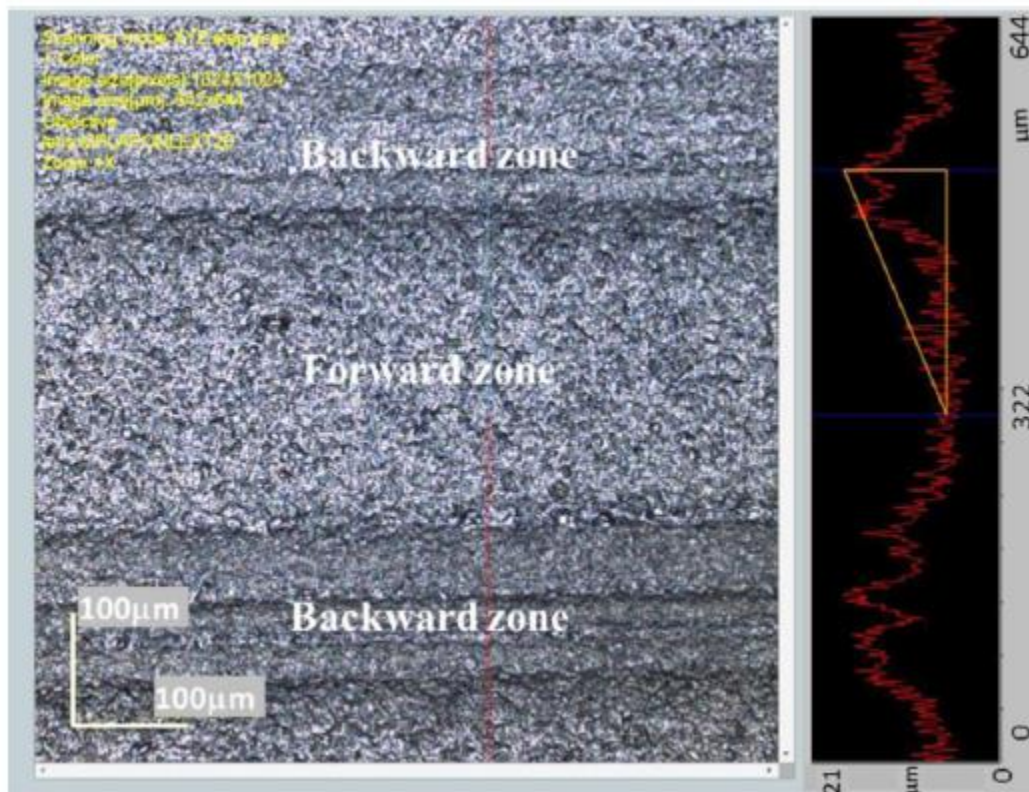


**Figure 1.11** Optical scanner images of (a) DWC wire cut and (b) SWC wire cut mc-silicon wafers (Chen et al., 2014).



Although striations can be categorized as simply a surface damage problem, the amount of kerf loss associated with the etching process to get rid of these patterns can be significant and places them under in-depth damage category. Recent attempts in eliminating these patterns from the wafer surfaces using a new vapor blast etching technique are presented by Chen et al. (2014).

Origins of the striations are the back and forth motion of the cutting wire (wire reciprocation) during ingot cutting (Wu et al., 2014; Kray et al., 2006). Since more wire is used in the forward cutting direction compared to the backward direction in order to feed fresh wire into the system, there is a difference in depth of surface roughness and width of these zones [see Figure 1.12].



**Figure 1.12** 3D Laser confocal microscope map of as sawn wafer surface cut by reciprocating wire saw (note-feature height scan is shown next to the map in the same image for reference) (Wu et al., 2014).

### **1.2.5 Stress and Dislocations**

As was discussed earlier in Section 1.2.2, the process of sawing induces large amount of stress on the silicon surface. Excessive stress leads to generation of dislocations and deteriorates the sample quality. The use of X-rays to efficiently image various types of defects in thin semiconductor films and substrates has been reported long ago (Rozgonyi et al., 1976). This technique can be used to analyze different types of dislocations, as well as for quantitative determination of stress in the material.

### **1.3 Need for the In-depth Damage Evaluation**

While saw manufacturers and wafer suppliers can easily measure TTV and other physical parameters of wafers, there are no easy ways to measure the degree, depth and distribution of damage. Yet, this information is needed by sawing companies for optimizing throughput. This information is also needed by the solar cell manufacturers to ensure that all the damage is etched away during wafer preparation before solar cell processing. Silicon wafer standard thickness is reducing (currently from 180 to 140 $\mu\text{m}$  for commercial 156mm x 156mm wafers) and is expected to reach 100 $\mu\text{m}$  mark in the near future. Hence, characterization of the surface and in-depth saw damage in sawn silicon wafers and quantification of its distribution is very crucial.

## **CHAPTER 2**

### **LITERATURE REVIEW**

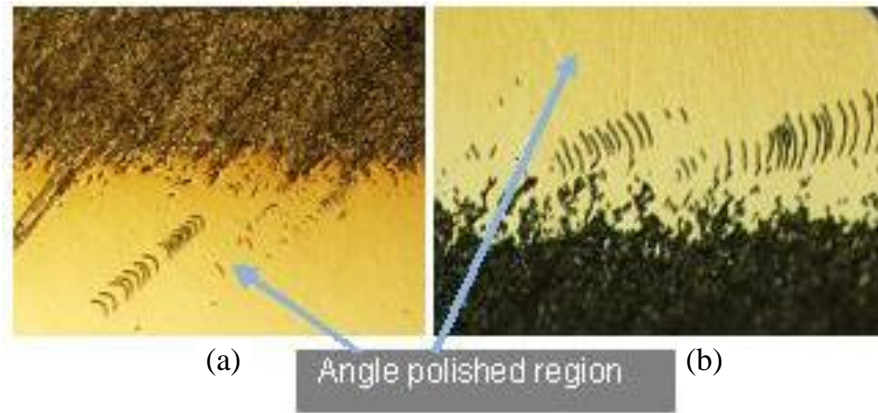
A number of approaches are being used by researchers to evaluate the surface and in-depth damage. One of the earliest methods developed for evaluation of polishing induced damage is based on the fact that damage present on a silicon wafer surface results in the formation of stacking faults (SF) when such a wafer is oxidized thermally. This phenomenon can be utilized for the manifestation of residual damage. A thin layer of silicon is etched away from the wafer surface (to get rid of the polishing induced surface damage); it is subjected to oxidation and inspected for the density of stacking faults (SF). This procedure is repeated until the SF density becomes negligible. The thickness removed per side corresponds to the depth of the polishing induced damage.

This repetitive oxidation and etching is a very tedious process. Therefore, the use of less labor and time intensive techniques such as XRD, SEM, laser scattering microscopy, resonance ultrasonic vibrations, acoustic microscopy, X-Ray topography, photoluminescence, surface photo voltage and angle polishing followed by defect etching have garnered more interest. In this chapter, a brief review of these measurement techniques and results obtained by various research groups using these methods are presented.

#### **2.1 Angle Polishing**

One of the most common approaches for measuring the depth of surface damage is to angle polish a small section of a wafer, which is then defect etched, followed by

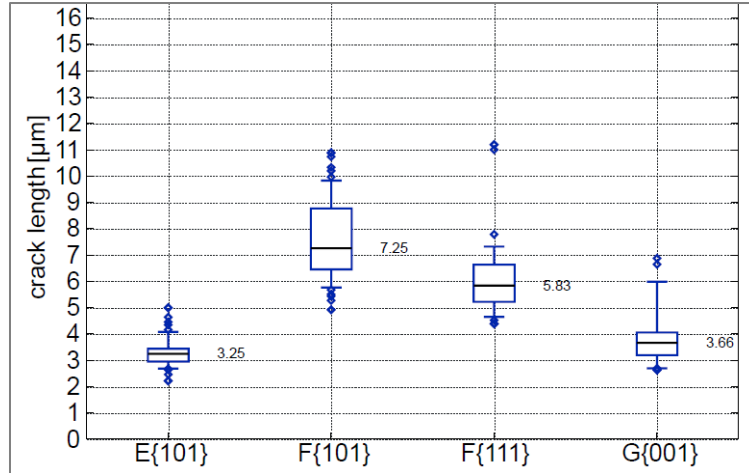
examination under an optical microscope to measure the depth of dislocations and micro-cracks below the surface. Figure 2.1 shows dislocation loops propagating into the bulk of the angle polished and defect etched samples taken from the wafers cut by SWC and DWC cutting methods.



**Figure 2.1** Optical microscope images of angle polished and defect etched (a) DWC and (b) SWC wafers (Sopori et al., 2013).

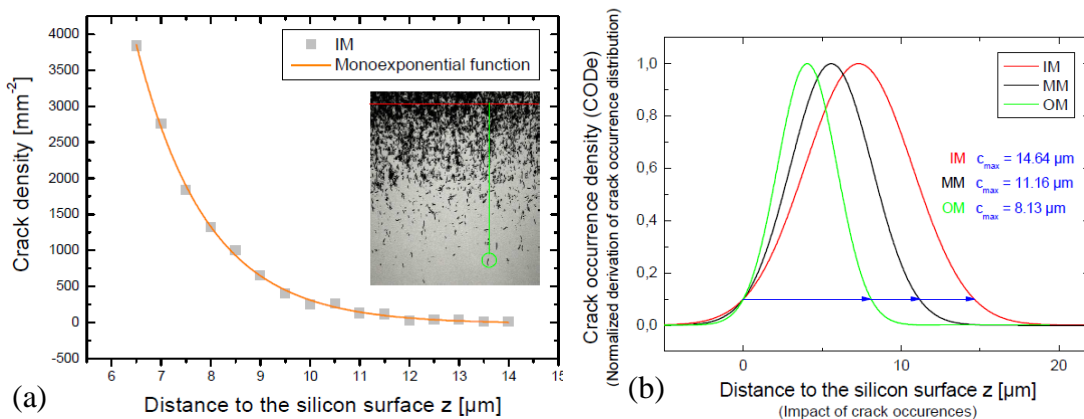
These images show a large defect concentration at the surface of the original as-sawn wafer. The defects show a striation pattern for the diamond cut and a 2-D pattern for the slurry cut wafer.

Crack depth analysis has been performed on different grains in angle polished mc-Si wafer samples by R Buchwald et al. (2013). Crack depths generated by sawing single crystal silicon wafers are compared with those in mc-Si wafers, crack depths are significantly lower in single crystal silicon. R Buchwald et al. (2013) found that the median of the maximum crack depth increases from the  $\{100\}$  plane to the  $\{111\}$  plane to the  $\{101\}$  plane [see Figure 2.2].



**Figure 2.2** Box plots of crack depth as a function of crystal orientation (Buchwald et al., 2013).

Crack counting and crack occurrence density evaluation at various locations on a wire sawn wafer is performed by Grun et al. (2012). From their studies, it is evident that the crack density decreases exponentially from the wafer surface. Also, the distribution of crack occurrence density shifts towards the surface from cutting wire entry point to the exit point on the wafer [Figure 2.3]. Similar findings were reported by Wagner et al. (2010).

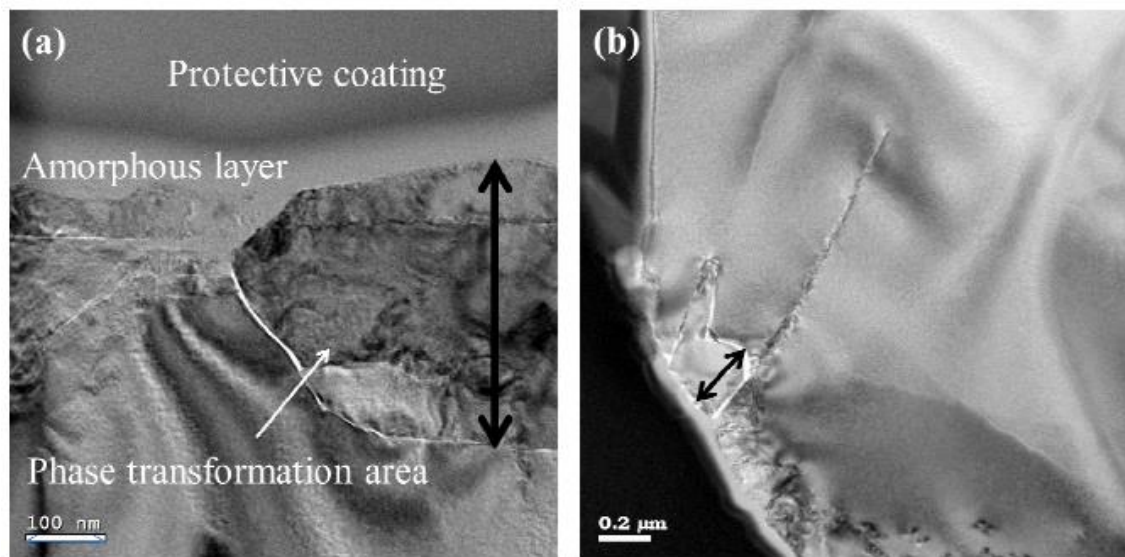


**Figure 2.3** (a) Sub-surface crack density distribution at a given area on wafer surface, (b) Distribution of crack density occurrence compared at three different locations on a given wafer surface (IM= wire entry point, MM= center of the wafer, OM= wire exit point,  $c_{max}$ =critical subsurface damage depth) (Grun et al., 2012).

All these procedures are quite tedious and the information generated is only from a small region. However, if the surface roughness is large, it becomes increasingly difficult to demarcate the original and the angle polished surfaces, reducing the accuracy of these techniques.

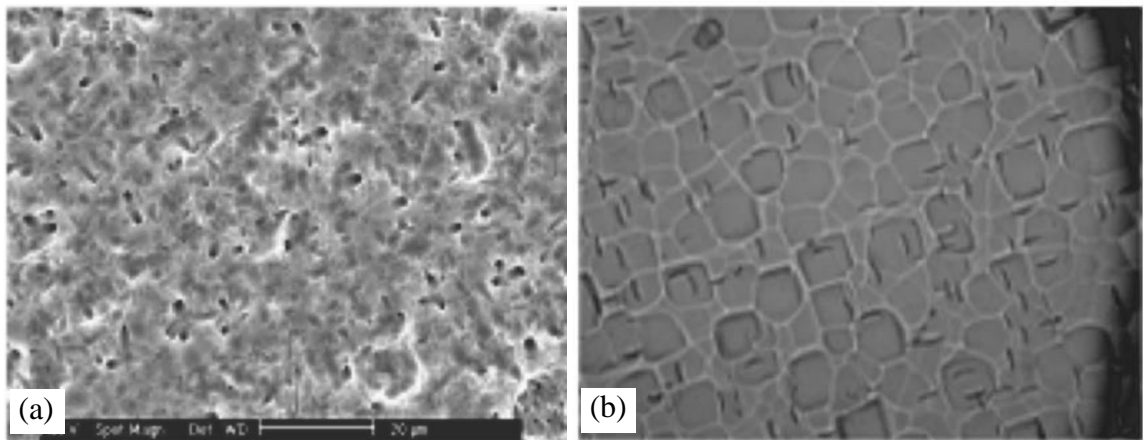
## 2.2 Electron Microscopy

Electron microscopy techniques yield reliable information but the information obtained is at the microscopic level. These methods are implemented in estimating the subsurface damage induced by grinding and polishing (Zarudi et al., 1996; Kang et al., 2005; Mchedlidze et al., 1995). DWC wire method employs multiple grit binders. Tsai et al. (2013) reported that a wire with resin-binder generates a thinner amorphous phase compared to the electroplated metal binder as seen in Figure 2.4. Again these measurements are very local and the results obtained cannot be generalized for the entire wafer surface.



**Figure 2.4** TEM micrographs of as-sawn DWC wafer surfaces cut with diamond grit impregnated in (a) electroplated grit binder, (b) Resin grit binder (Tsai et al., 2013).

Kim et al. (2005), in their experimental studies, reported that there is a critical value for the damage depth created on wafer surfaces. Above this critical value of the damage depth, it generates dislocation loops upon oxidation of the as-sawn wafer surface and wire sawing comes under this category. However, the same material with lower critical damage depth value (lapped or silica blasted surfaces) generates stacking faults upon oxidation. These features can be visualized in SEM images obtained from two different wafer surfaces etched in Wright solution for 5 min [Figure 2.5].



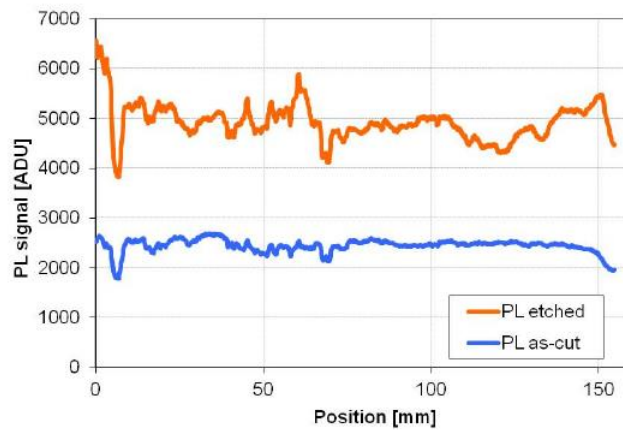
**Figure 2.5** SEM micrographs of oxidized, etched wafer surfaces showing (a) Dislocation loops generated because of heavier mechanical damage imparted by the wire sawing, (b) Stacking faults generated because of lighter mechanical damage induced by the lapping process (Kim et al., 2005).

Scanning Electron Acoustic Microscopy (SEAM), a well-established technique for depth discrimination of multilevel integrated circuits is used in characterizing the defects in wire sawn silicon wafers after saw damage etch (Meng et al., 2013). But more studies are required on this topic to confirm that this can be a reliable method.



### 2.3 Photoluminescence

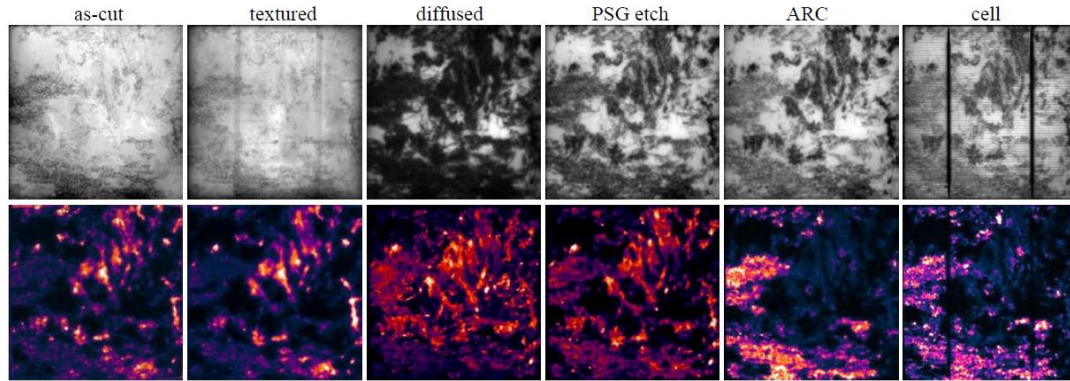
During the past decades, efforts have been made by researchers to utilize the method of photoluminescence (PL) for evaluation of silicon material quality. In-line qualitative analysis of damaged wafers is reported by Korsos et al. (2012). In their approach, photoluminescence images are obtained from as-cut and damage etched wafer surfaces. PL intensity line scans are obtained from these images for comparison. Figure 2.6 shows the increase in PL signal for the etched wafer.



**Figure 2.6** Photoluminescence line scans across the 156mm x 156mm wafer surface (Korsos et al., 2012).

Attempts are made to measure the sub-surface damage quantitatively using photoluminescence (PL). This approach is limited by the strict temperature dependence of the PL technique. A comparison of various techniques, including photoluminescence, for subsurface damage evaluation is given by Lu et al. (2007). Figure 2.7 shows qualitative comparison of band to band and defect-band images obtained from multiple mc-Si sister (sequential) wafers after each cell fabrication step. Image correlation of a starting wafer to the final cell would ideally provide information for predicting the performance of the wafers from that same ingot/location before the wafers are processed.

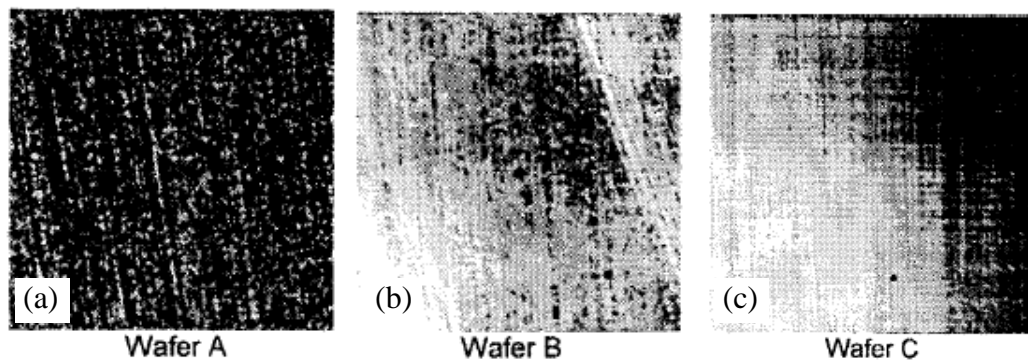




**Figure 2.7** Band-to-band (top row) and defect band (bottom row) PL images of sister wafers after each cell fabrication step (Johnston et al., 2012).

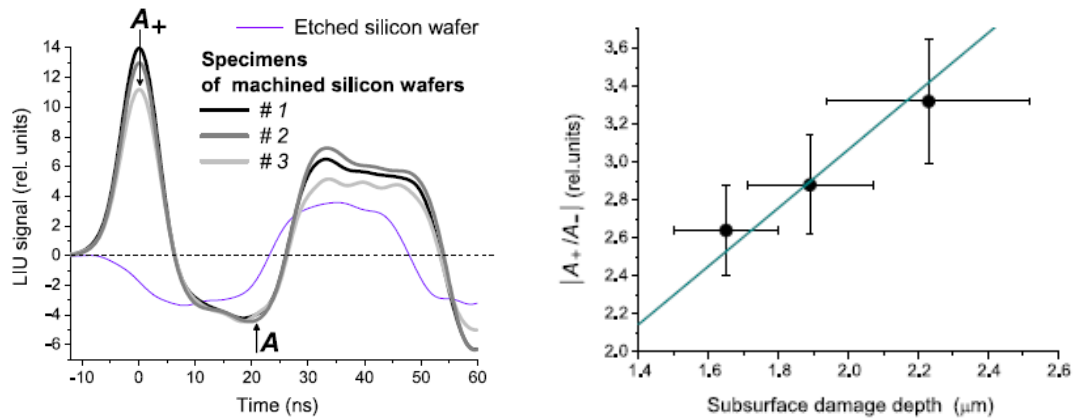
## 2.4 Lasers

Lasers are used by many researchers in multiple ways to evaluate subsurface damage. Zhang et al. (2002) used the concept of laser scattering to generate 2D scatter images of the subsurface damage. Laser scattering has the potential to scan the whole wafer within tens of minutes, and detect the deepest damage in the whole wafer. This is a big advantage over other methods (such as cross-sectional microscopy) that can only reveal SSD information at localized areas on the wafer. But the information generated (SUM-IMAGES) by this technique is only qualitative as seen in Figure 2.8.



**Figure 2.8** Raman laser scattering images of silicon wafers of same final thickness but with different sub-surface damage conditions, (a) #320 diamond grit, coarse grinding damage (wafer A), and #2000 diamond grit, fine grinding damage removal of (b) 10 $\mu$ m, and (c) 30 $\mu$ m (Zhang et al., 2002).

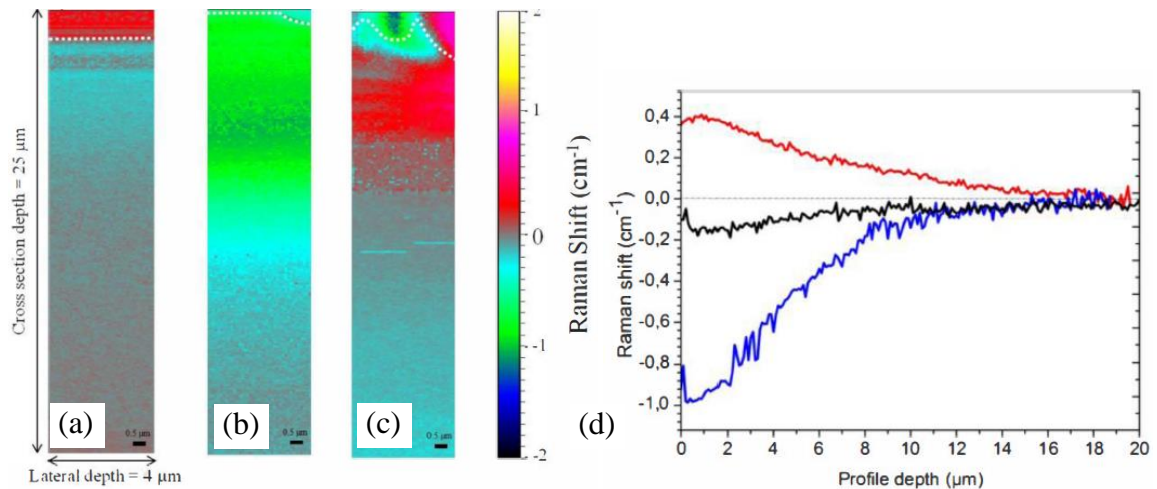
A A Karabutov et al. (2014) used the concept of laser ultrasonic method. They could estimate the damage depth using an empirical relation between subsurface damage depth and the ratio of amplitudes of compression and rarefaction phases of the laser induced ultrasound (LIU) signals [see Figure 2.9]. But the main disadvantage of this technique is, it has a minimum limit on the depth of the sub-surface damage it can detect (approximately 0.15 to 0.2  $\mu\text{m}$ ).



**Figure 2.9** (a) Temporal profiles of laser induced ultrasonic signals in silicon wafers with varying SSD (#1-1.65 $\mu\text{m}$ , #2-1.89 $\mu\text{m}$ , #3-2.23 $\mu\text{m}$ ), (b) Plot showing empirical relation between experimental (points) and ratio of amplitudes of compression and rarefaction phases of the LIU signal (Karabutov et al., 2014).

Recently, Photo Modulated Optical Reflectance (PMOR) measurements have been performed on SWC wafers by Bogdanowicz et al. (2012). Surface roughness was measured by the variation in average DC reflectance and the saw damage depth by the change in AC reflectance signal. The small measurement area (0.5 $\mu\text{m}$ ) limits the use of this technique for macroscopic evaluation of the damage. Also, accurate determination of the damage depth is hindered by the interference of surface roughness in altering the AC signal.

Lasers of varying wavelength are used for Raman spectroscopy analysis of cross-sections of silicon samples by Radet et al. (2011) for sub-surface damage analysis. Chemically mechanically polished (CMP), chemically polished (CP) and as-sawn slurry cut wafers are analyzed for the estimation of damage depth. Figure 2.10 shows a 2D spectral image of these three wafer cross sections and depth profiles of Raman shift obtained from the map.



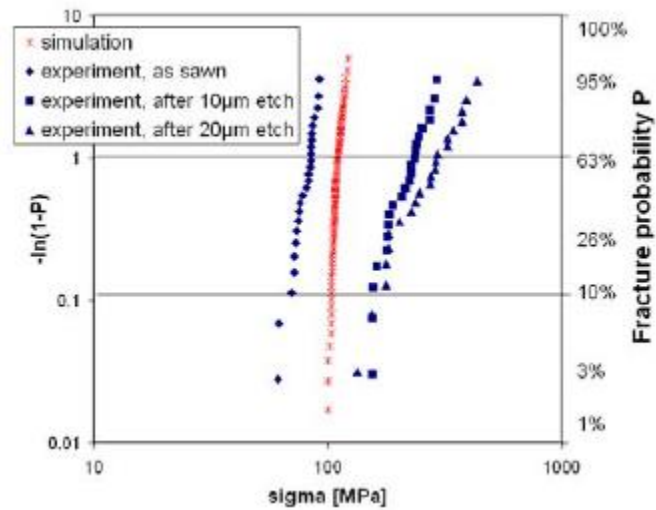
**Figure 2.10** 2D Raman spectra of (a) CMP, (b) CP, and (c) as-sawn SWC wafer cross-sections, (d) Raman shift depth profiles extracted from the 2D spectra, (RED line- as-sawn SWC, BLACK line- CMP, BLUE line-CP) (Radet et al., 2011).

## 2.5 Fracture Mechanics

Micro-cracks cause a severe deterioration in the mechanical strength of the wafer. Depth and location of these micro-cracks determine the overall fracture strength. From the literary works mentioned in Section 1.2.3, we learned that the micro-cracks located near the surface are more effective in causing the deterioration in mechanical strength. Attempts are made by various researchers to relate micro-crack density, crack-length and position to the mechanical strength of the wafers by experimental (two-point, three-point, and four-point bending tests, ring-on-ring tests, angle polishing, and defect etching), and

theoretical analysis (finite element analysis, and monte-carlo simulations) (Yang et al., 2013; Rupnowski et al., 2008; Saffar et al., 2014; Popovich et al., 2013; Jeong et al., 2000).

Figure 2.11 shows the comparison of theoretical wafer strength distribution (under a certain assumptions of crack density, shape, and lengths) with the experimental data obtained from as-sawn and damage etched silicon wafers.



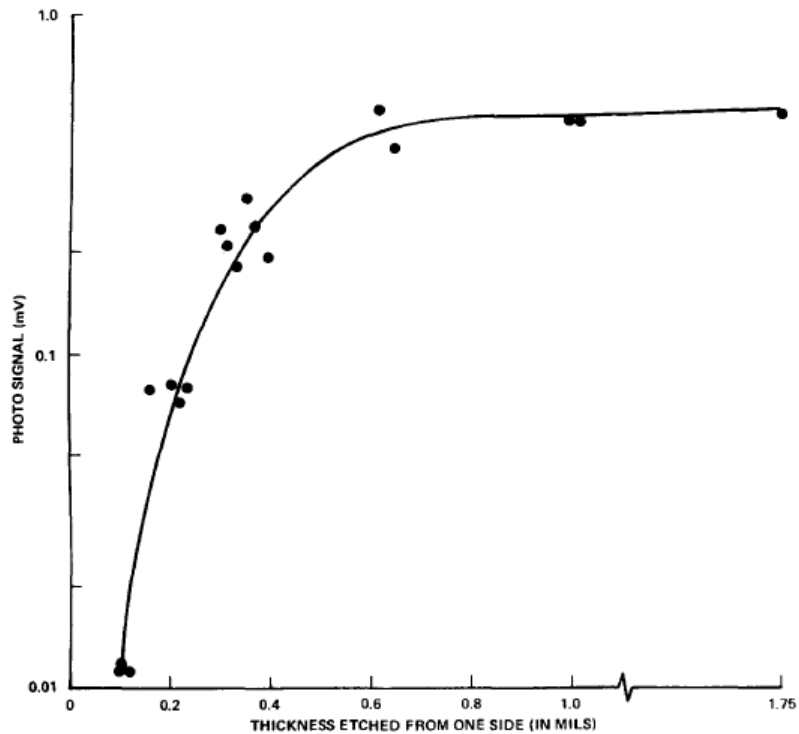
**Figure 2.11** Theoretical and experimental strength distributions of as-sawn, and etched silicon wafers (Rupnowski et al., 2008).

This approach suffers from the requirement of extensive experimental analysis on numerous wafers for supplying reliable and sufficient information for theoretical calculations for accurate evaluation of damage depth.

## 2.6 Electrical Characterization

Surface photo voltage developed on a semiconductor wafer as a means to observe the polishing damage has been realized long ago (Sopori, 1980). Change in the amplitude of photo voltage signal is directly related to the damage removal and saturation in the signal

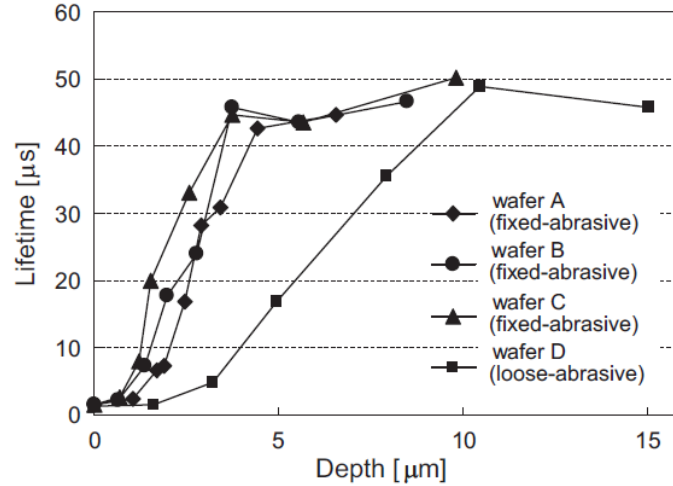
after subsequent chemical polishing or etching confirms the complete damage removal as seen in Figure 2.12.



**Figure 2.12** Change in surface photo voltage signal as a function of thickness removed from one side of the silicon wafer (Sopori, 1980).

Minority carrier lifetime measurement is another technique which can reliably yield information about the material quality, surface passivation. These measurements are very sensitive to the surface and sub-surface damage. Watanabe et al. (2010) demonstrated the use of minority carrier lifetime measurements on sequentially etched polycrystalline silicon wafers for damage depth evaluation. This technique is based on measurement of the effective minority carrier lifetime ( $\tau_{\text{eff}}$ ) of the wafers after sequential etching of thin layers from the damaged surface. The measured  $\tau_{\text{eff}}$  increases as the more and more thickness is removed from the surface. The thickness-removed that yields the peak value of  $\tau_{\text{eff}}$  represents the damage depth. Figure 2.13 shows minority carrier

lifetime plots of as-sawn polycrystalline wafers etched in steps and the corresponding incremental lifetime recorded.



**Figure 2.13** Minority carrier lifetime measured vs depth of damage layer removed from each side of the silicon wafer (plots of various polycrystalline wafers cut using SWC and DWC methods are shown) (Watanabe et al., 2010).

This method of sequential etching and minority carrier lifetime measurement has many advantages. It can be used for the subsurface damage depth evaluation in crystalline silicon wafers cut by different wire sawing mechanisms. The damage distribution can be obtained theoretically in terms of recombination velocity and can be correlated to various parameters such as wire/grit size, wire usage etc. (Sopori et al., 2013; Sopori et al., 2014).

## **CHAPTER 3**

### **EXPERIMENTAL METHODS AND TECHNIQUES**

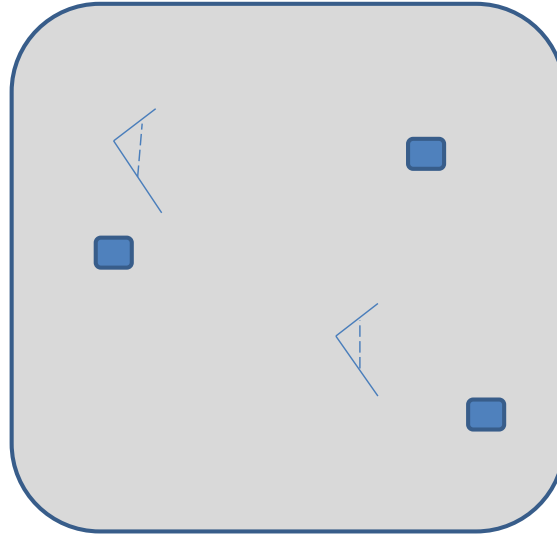
Experimental methods for the evaluation of silicon surface and in-depth damage have been developed and optimized since the beginning of the silicon industry. Researchers are still trying to develop a more reliable means of measuring the saw damage. Various methods have been discussed in the previous chapter. Some of those techniques are implemented in the damage analysis on as-sawn wafers.

In this chapter, a brief description of the experimental techniques adopted for the damage depth analysis, variations in saw damage on wafers cut by different sawing methods, etch rate as a means of estimating the depth and degree of damage will be presented. Finally, a relatively novel mechanism of using minority carrier lifetime for quantitative determination of saw damage on crystalline silicon wafers will be introduced.

#### **3.1 Optical Microscopy**

Optical microscopy is a quick and easy method for examining the sample surface. It immediately reveals the topography of the surfaces for qualitative analysis of damaged wafer surface. In R&D, there is an array of optical microscopes available, depending on the technology. A Nomarski microscope is used and the samples under investigation are the as-sawn silicon wafers cut with DWC method. Silicon wafers sliced with various wire sizes with and different grit sizes are obtained from the commercial wafer manufacturers. These wafers are cleaved into pieces of manageable size (approx. 4cm x 4cm for

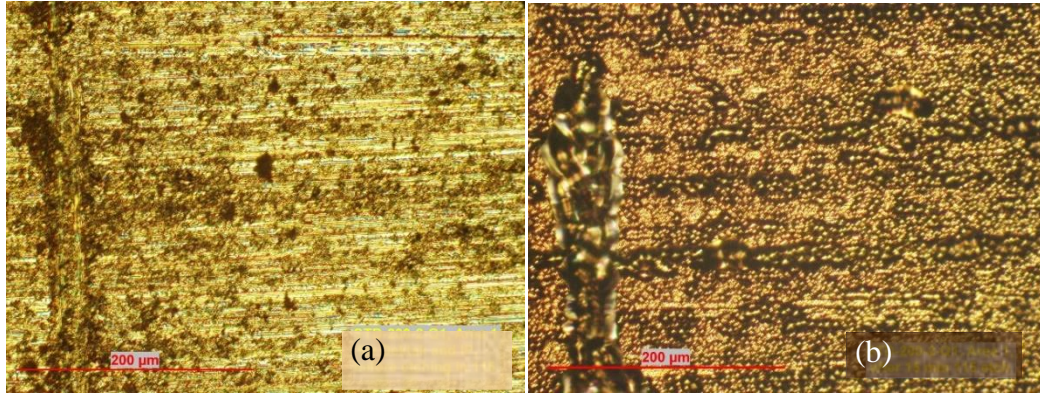
DEKTAK and 1cm x 1cm for angle polishing). At different locations on the sample surface, scribing is performed by a diamond scribe to identify the location before and after saw damage removal [Figure 3.1].



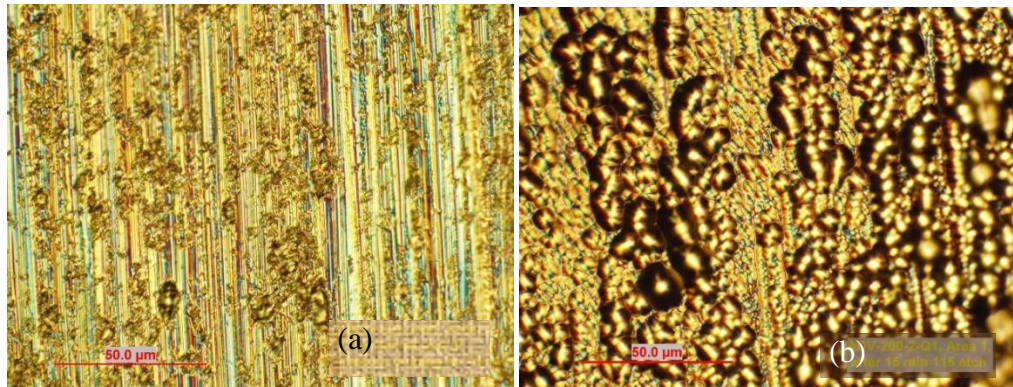
**Figure 3.1** Illustration of sample preparation method for optical microscopy, contact and optical profilometry. (Note- L shaped Scribing marks for reference, and dashed lines represent locations from where the Dektak scans are obtained. Colored squares are arbitrary locations chosen for optical microscopy).

Samples are etched for 15 min in 1:1:5 :: HF:HNO<sub>3</sub>:CH<sub>3</sub>COOH (here after referred to as 115 solution) mixture to ensure the complete removal of the saw damage. Figure 3.2 (a) shows silicon sample with vague characteristic striation patterns of DWC cutting method. After etching for 15 minutes, the same location is observed under the microscope for striations, change in topography, and uniformity of etching [see Figure 3.2 (b)]. Samples in Figures 3.2 and 3.3 are sawn using thicker wire/larger grit (120 $\mu$ m/12-25 $\mu$ m) while the samples in Figure 3.4 are sawn using thinner wire/smaller grit (100 $\mu$ m/10-20 $\mu$ m). Images shown in Figure 3.5 are 50 times magnified images of the sample surfaces shown in Figure 3.4.

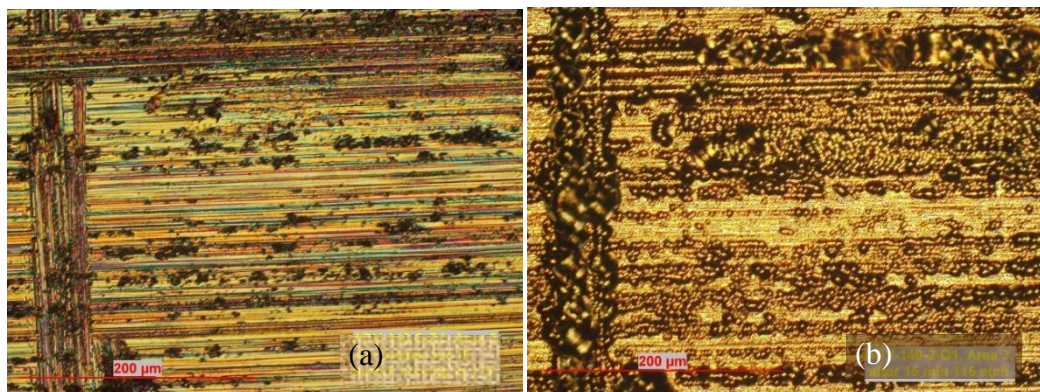




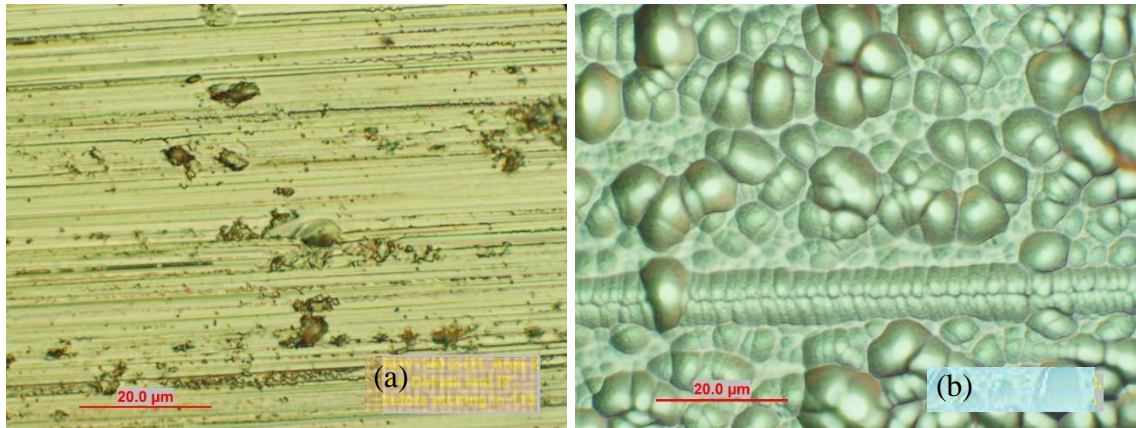
**Figure 3.2** Optical microscope images (at 10x magnification) of a DWC wafer (thick wire/grit) sample (a) before (or as-sawn surface), and (b) after damage removal etching in 115 solution for 15 min.



**Figure 3.3** Optical microscope images (at 20x magnification) of a DWC wafer (thick wire/grit) sample (a) before (or as-sawn surface), and (b) after damage removal etching in 115 solution for 15 min.



**Figure 3.4** Optical microscope images (at 10x magnification) of a DWC wafer (thin wire/grit) sample (a) before (or as-sawn surface), and (b) after damage removal etching in 115 solution for 15 min.



**Figure 3.5** Optical microscope images (at 50x magnification) of a DWC wafer (thin wire/grit) sample (a) before (or as-sawn surface), and (b) after damage removal etching in 115 solution for 15 min.

From the images shown in Figure 3.2 to Figure 3.4, following conclusions can be made: (i) The striation pattern generated during the DWC method causes non-uniformities in wafer surface roughness during the saw damage removal process. (ii) Thicker wire/grit size causes higher surface roughness. For estimating the variation in damage depth, further studies are required.

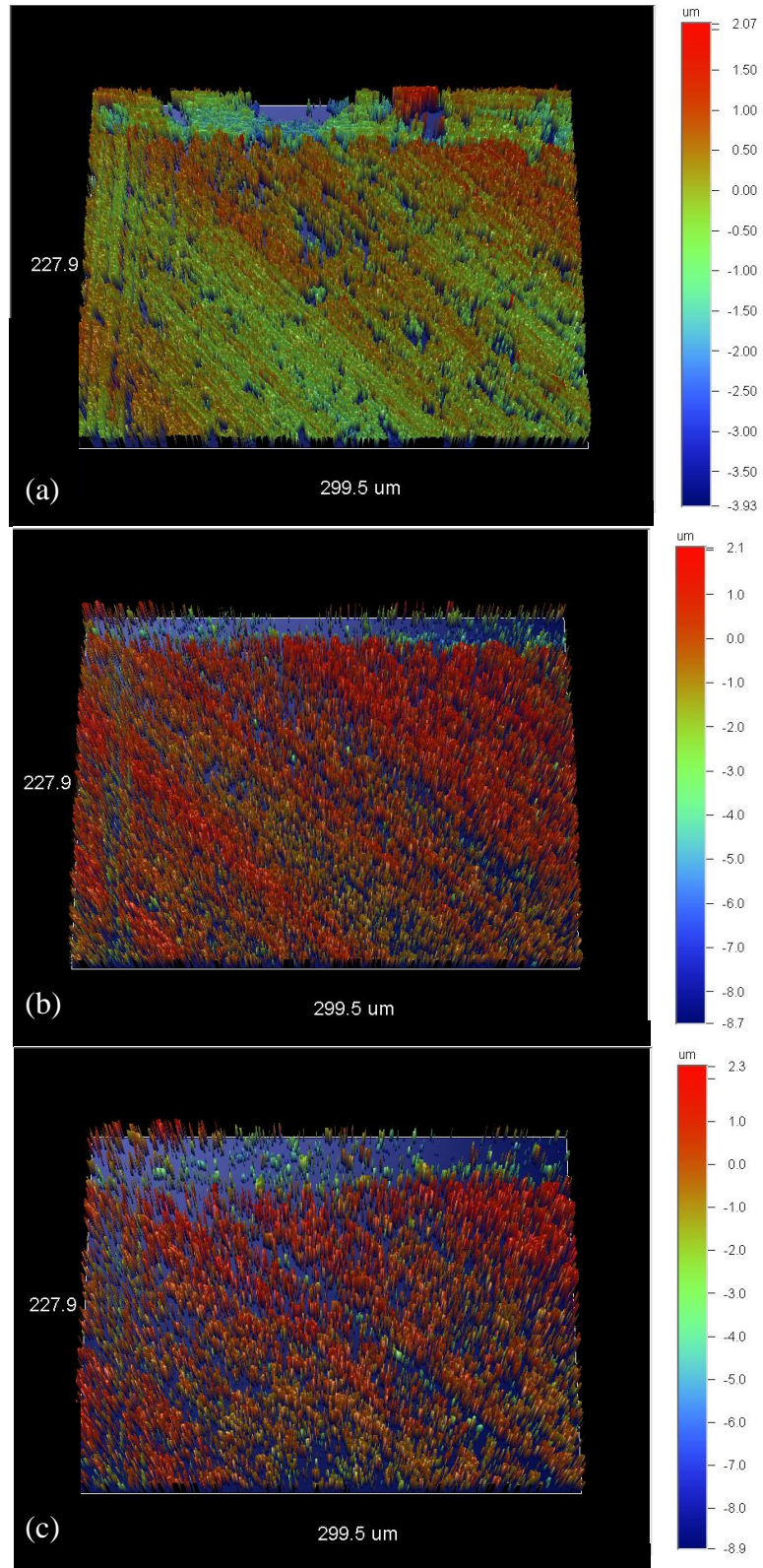
### 3.2 Optical Surface Profiling

As-sawn silicon wafers cut using DWC method with different wire/grit sizes are chosen for examination. These samples have been scribed (L shaped marks) for identification of the regions of interest as mentioned in Section 3.1. Variation in surface roughness is evident from the interference microscopy measurements. Each sample is etched twice for 2 minutes each time and vertical scanning interference (VSI) images are obtained after each etching step using a WYKO NT1100 optical profiler system.

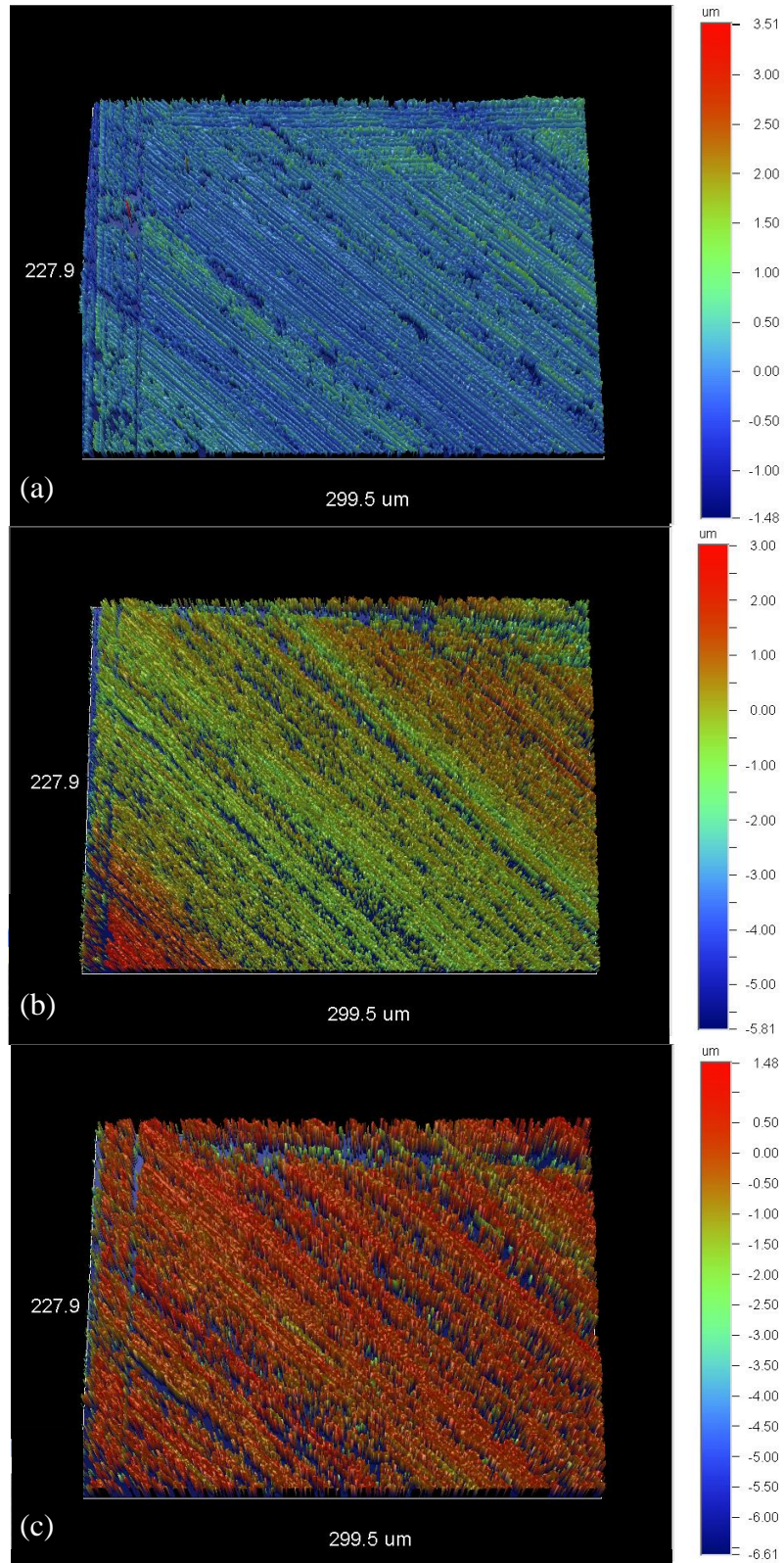
The original sample surface is shinier and after initial etching in 1:1:5 solution, the appearance of the sample surface becomes dull. After the second etch step, the

surface becomes rough making it difficult to obtain interference pattern and in turn the feature height from the surface. Figure 3.6 shows these three surface conditions (a) as-sawn, (b) after 2 min etching and (c) after 4 min etching of DWC wire sawn wafers cut with a thick wire/larger grit (120/12-25  $\mu\text{m}$ ). The original as-sawn surface roughness value is 6 $\mu\text{m}$ . After the first etching, roughness increases to approximately 10.77 $\mu\text{m}$  and subsequent etchings make it more difficult to obtain an interference pattern from the surface and reliable data from the measurements. Figure 3.7 shows a similar set of samples prepared from DWC wafers cut with a thinner wire/grit size (100/10-20 $\mu\text{m}$ ) compared to the earlier 120/12-25  $\mu\text{m}$  wire/grit size. Because of the lower surface roughness caused by the thinner wire and smaller grit, significant interference signal is still obtained from the wafer surfaces after second etch step. Debris from the sawing action may occasionally deposit over the sample surface and cause the absence of interference signal from the wafer surface as seen in of the Figure 3.6 (a).





**Figure 3.6** Optical profilometer images of DWC wafer (wire/grit size: 120/12-25  $\mu\text{m}$ ) surface in (a) as-sawn (b) 2 min etched and (c) 4 min etched condition.

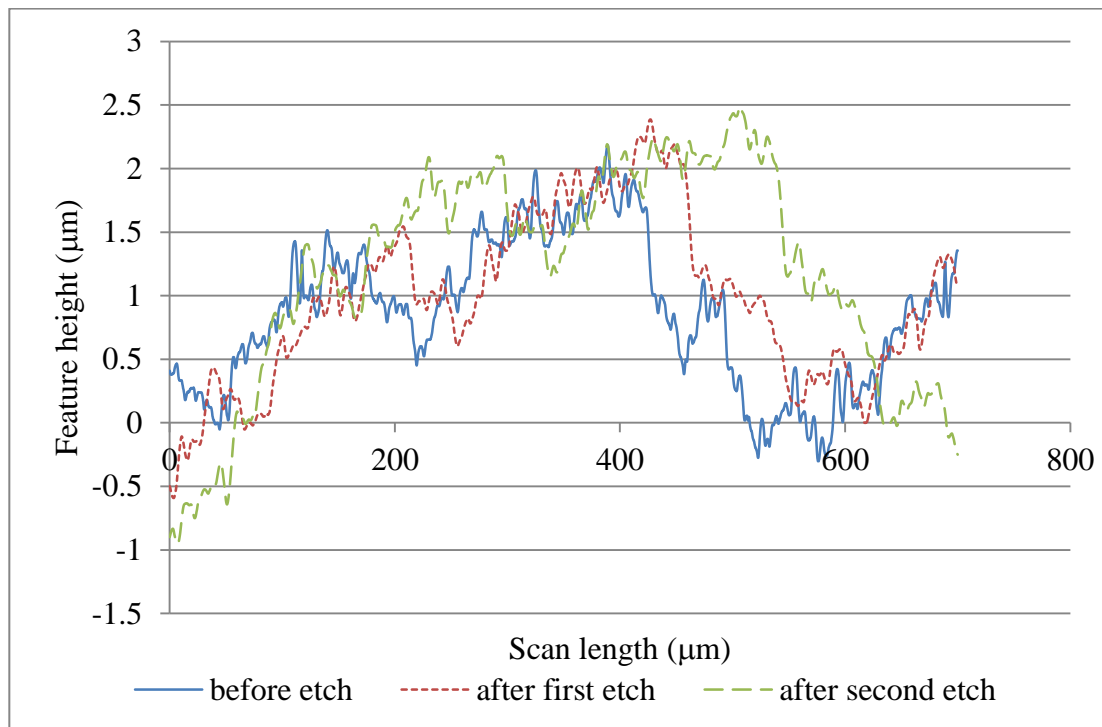


**Figure 3.7** Optical profilometer images of DWC wafer (wire/grit size: 100/10-20  $\mu\text{m}$ ) surface in (a) as-sawn (b) 2 min etched and (c) 4 min etched condition.

### 3.3 Contact Surface Profiling

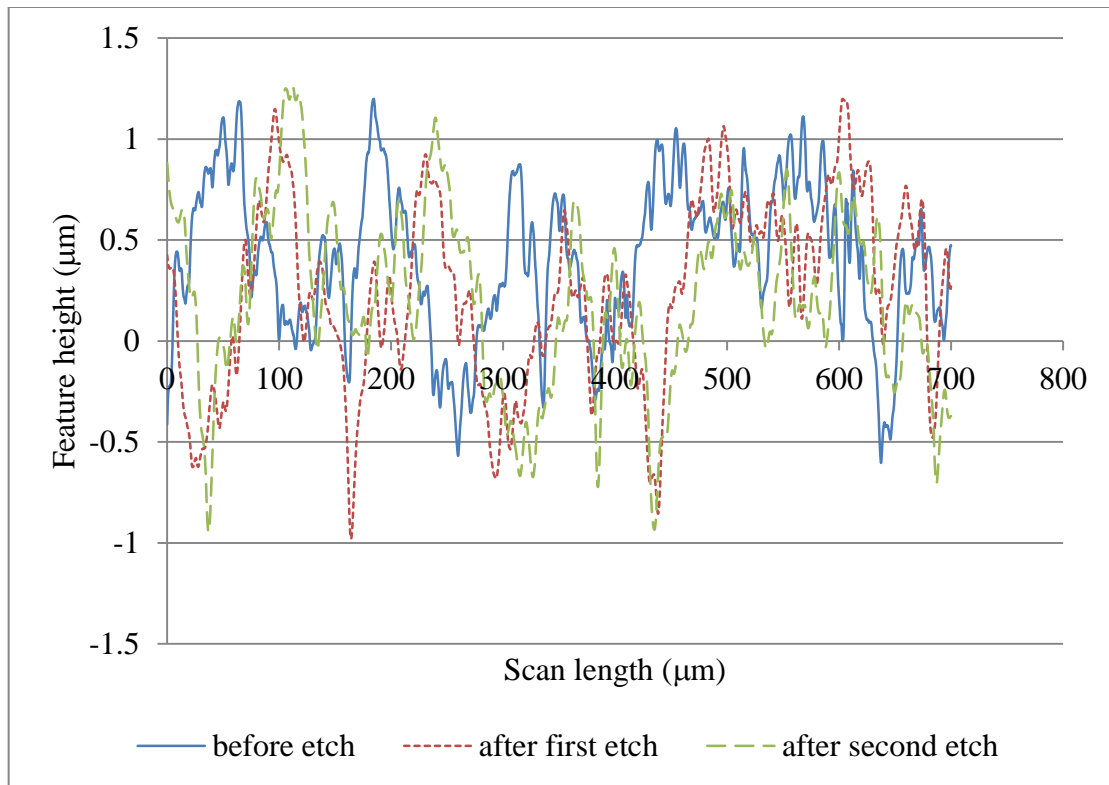
Contact surface profilometry is performed using a VEECO DEKTAK 8 system on crystalline silicon wafers cut by DWC method. Two areas are chosen on each wafer cut by different wire/grit size. Scanning is performed (on as-sawn and etched wafers used in Section 3.2) perpendicular to the sawing direction in order to capture the details of the cutting method.

Figure 3.8 shows comparison of three Dektak scans obtained on a DWC wafer surface in three different conditions- (i) as-sawn, (ii) 2 min etched, and (iii) 4 min etched. Note that the surface roughness is of the order of  $0.5 \mu\text{m}$ , and the feature height variation is up to  $3 \mu\text{m}$ .



**Figure 3.8** Dektak scans of as-sawn, 2 min etched (first etch) and 4 min etched (second etch) wafer surfaces. (Cutting wire/grit size -  $100/10\text{-}20 \mu\text{m}$ ).

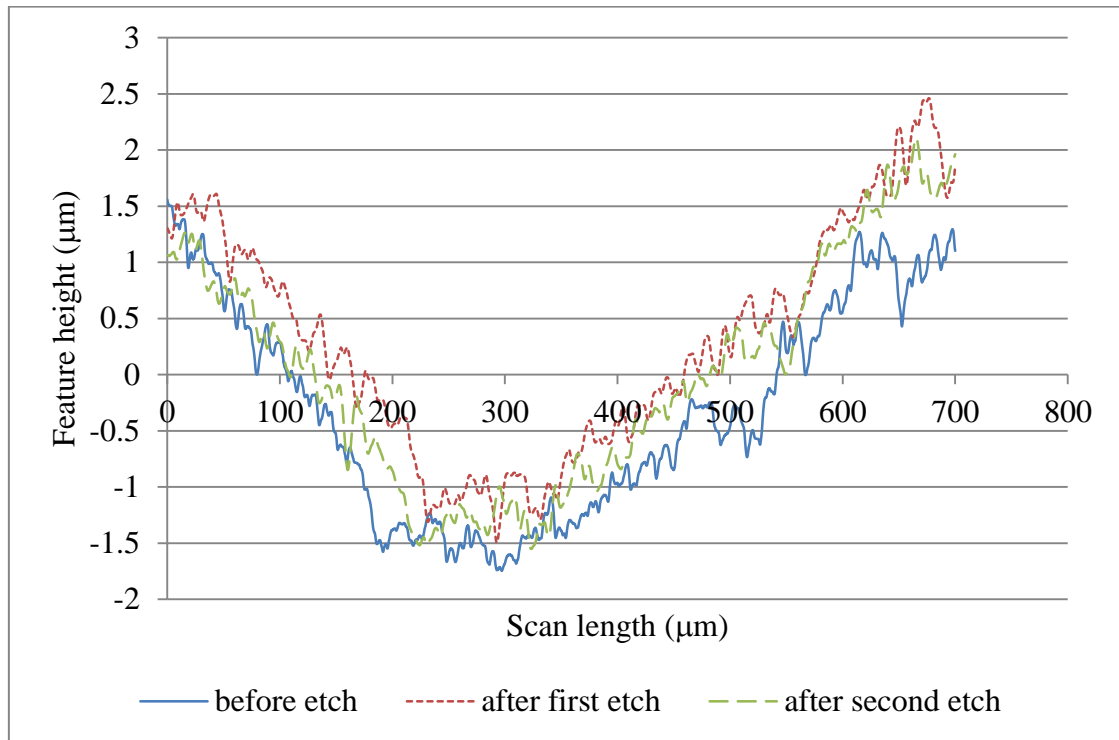
These wafers (results in Figure 3.8) are cut using a thin DWC wire (wire/grit size 100/10-20  $\mu\text{m}$ ) resulting in lower surface roughness. Figure 3.9 shows similar measurements on wafer samples cut using a thicker wire/grit (120/12-25  $\mu\text{m}$ ). Both surface roughness and variation in feature heights are more on these wafer surfaces.



**Figure 3.9** Dektak scans of as-sawn, 2 min etched (first etch) and 4 min etched (second etch) wafer surfaces. (Cutting wire/grit size - 120/12-25 $\mu\text{m}$ ).

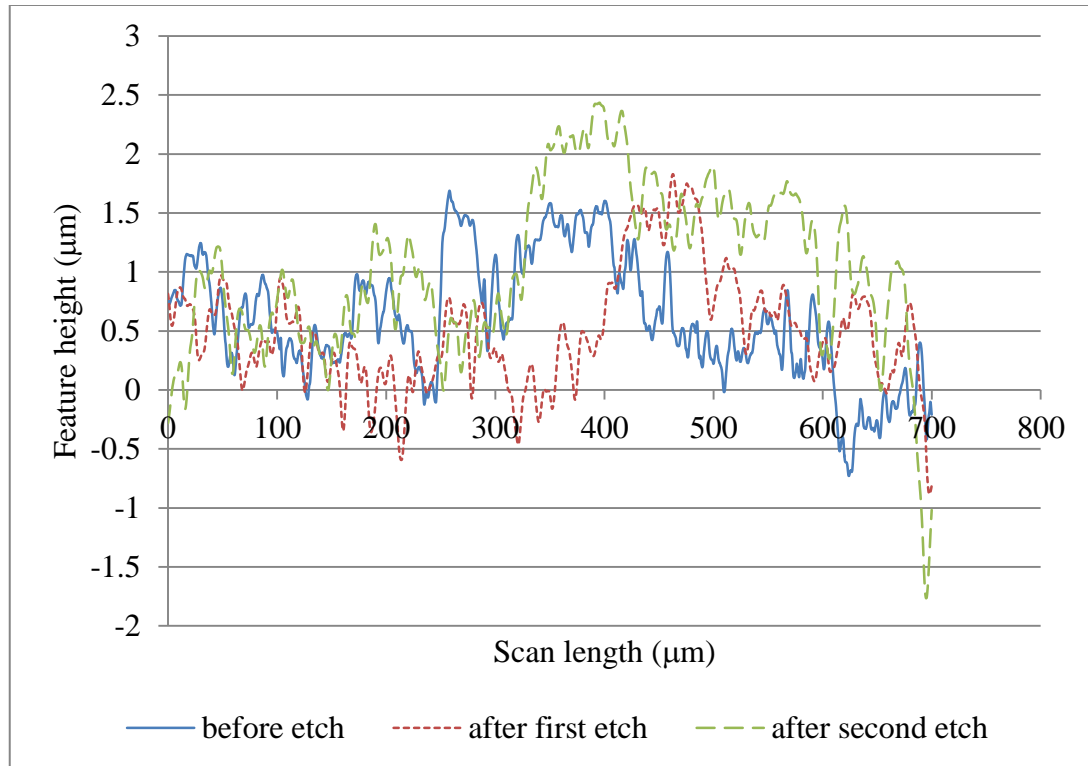
Figure 3.10 shows Dektak scans obtained from within a groove produced by the sawing action. Surface roughness is about 0.5  $\mu\text{m}$  and feature height is about 4  $\mu\text{m}$ . Figure 3.11 shows another area of interest on the wafers shown in Figure 3.9. From these measurements, it seems like the sharp peaks or valleys present in the as cut wafer surfaces are being rounded off after subsequent etching steps which must reduce the surface roughness at the microscopic level. It is an important factor in determining the

total surface area and number of dangling bonds present on a given surface, But, we have to note that the resolution of these Dektak scans are limited by the size of the stylus tip used for the scans (radius of the stylus tip used in these experiments is 5  $\mu\text{m}$ ).



**Figure 3.10** Dektak scans of as-sawn, 2 min etched (first etch) and 4 min etched (second etch) wafer surfaces over a groove produced by sawing. (Cutting wire/grit size - 100/10-20  $\mu\text{m}$ ).



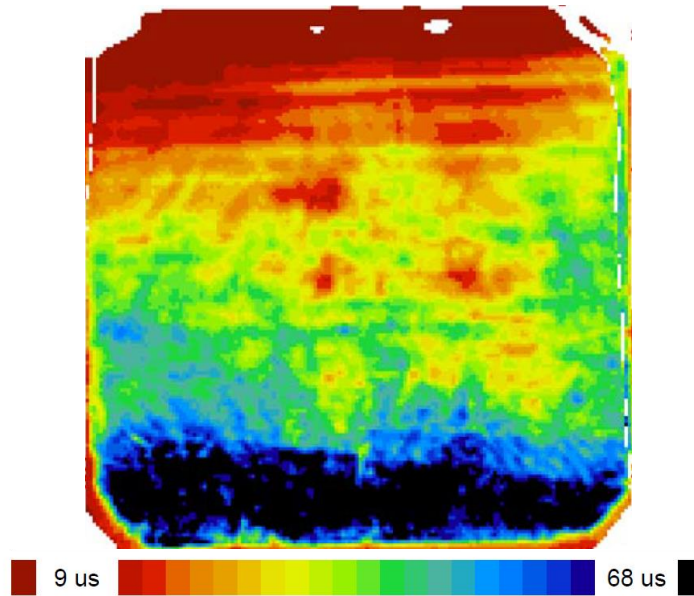


**Figure 3.11** Dektak scans of as-sawn, 2 min etched (first etch) and 4 min etched (second etch) wafer surfaces at a different area on the sample used in Figure 3.9. (Cutting wire/grit size - 120/12-25  $\mu\text{m}$ ).

### 3.4 Taper Etching and $\mu\text{w}$ -PCD Imaging

Local measurements discussed in earlier sections help in getting a microscopic idea of the damage present at a selected area of interest on the wafer surface. But, in order to estimate the damage over the entire surface area, a different approach is needed. As-sawn crystalline silicon wafers are cleaned in solvents (IPA and DI water), then cleaned in piranha for 20 minutes and the chemical oxide is etched off. Then the wafers are immersed in 115 solution and slowly removed from the etchant at a rate of approximately 3 inch/min resulting in tapered profile of existing/removed damage layer. The sample is passivated with Iodine-Ethanol (IE) and microwave PCD ( $\mu\text{w}$ -PCD) mapping is performed [see Figure 3.12]. This technique will yield the information of the distribution

of the damage on a given wafer surface. Since the damage is not removed completely with in that short time (approximately 2 min per wafer), lifetime values are lower.

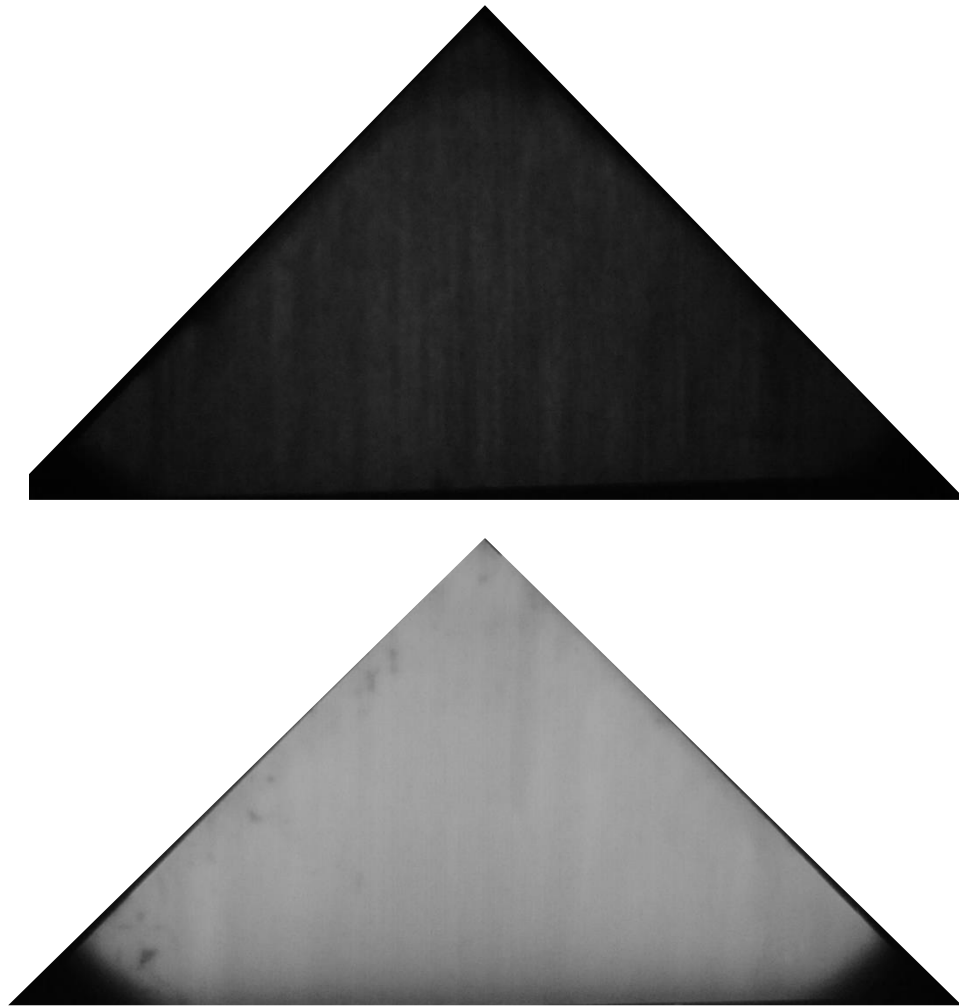


**Figure 3.12** Microwave PCD image of an as-sawn wafer surface after taper etching in 115 solution.

### 3.5 Photoluminescence

Photoluminescence technique is widely used for determining the silicon material quality and damage evaluation. With proper passivation, sufficient signal can be generated for detection by a CMOS camera for qualitative analysis of the material. But for quantitative analysis, proper calibration is required for converting the signal strength into the minority carrier lifetime values. Figure 3.13 shows the PL images of partially etched and completely etched (for damage removal) wafer quarters. Both images are obtained under similar conditions of exposure and image acquisition modes (10Amperes of current

through laser diodes and 2 seconds exposure time at ISO-6400, using a Nikon D5100 SLR Camera with InGaAs filter).



**Figure 3.13** Photoluminescence images of (a) partially etched wafer quarter surface and, (b) fully etched wafer quarter surface (damage removed completely). Both the samples are cleaned in piranha solution, HF dipped and passivated in Iodine-Ethanol solution.

### 3.6 Minority Carrier Lifetime

In an effort to estimate the in-depth saw damage accurately, the concept of sequential etching has been explored previously by a couple of researchers (Watanabe et al., 2010), (Sopori et al., 2014). Since minority carrier lifetime is an already established technique in determining the silicon material quality, it can be a reliable means for exploiting the

concept of sequential etching and damage depth evaluation. Figure 3.14 shows the WCT-120 standard offline wafer-lifetime tool used in this study. The principle of this machine is the measurement of change in the photoconductivity of the wafer as a function of time to calculate the effective minority carrier lifetime.



**Figure 3.14** Wafer-lifetime tool used for the evaluation of minority carrier lifetime.

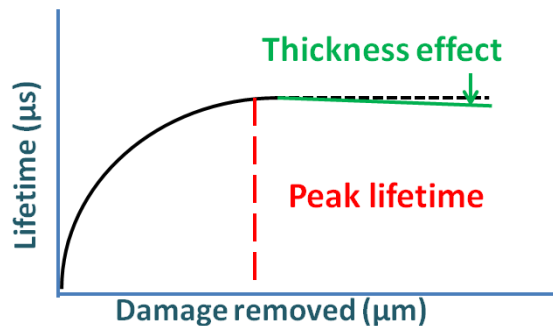
Source: <http://sintoninstruments.com/Sinton-Instruments-WCT-120.html>.

The following procedure outlines the concept used for the evaluation of in-depth damage in as-sawn silicon wafers.

- Crystalline silicon wafers are cut under different sawing conditions viz. cutting wire thickness, slurry or diamond grit thickness, wire usage are selected and prepared for sequential etching.

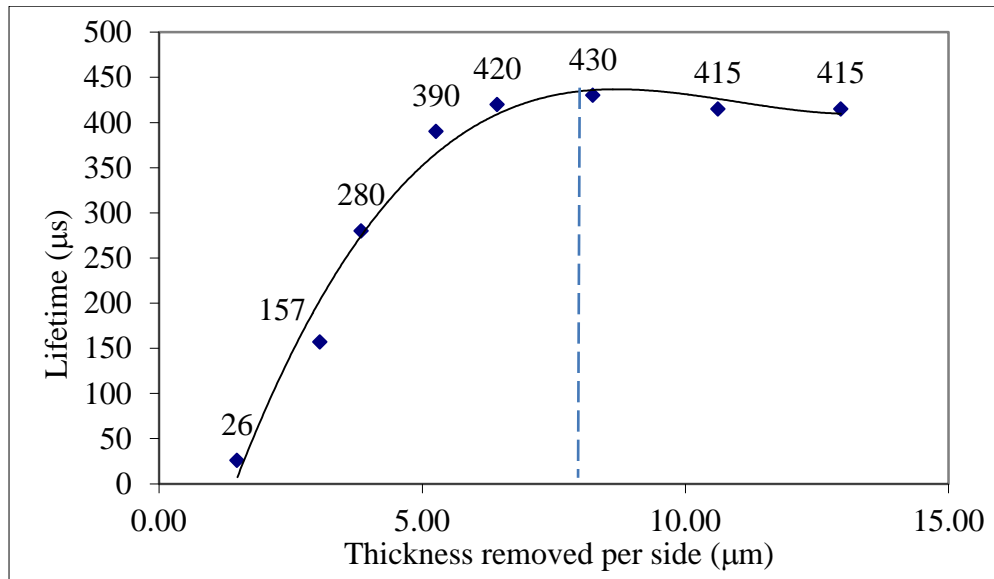
- Damage removal is performed by a slow etching solution (1 to 2  $\mu\text{m}/\text{minute}$ ) such as 115 etch (1:1:5 :: HF:HNO<sub>3</sub>:CH<sub>3</sub>COOH) to remove controlled layers of damage from each sample surface.
- These sequentially etched wafers are passivated (by means of a reliable liquid passivation mechanism, such as Iodine-Ethanol) and effective minority carrier lifetime ( $\tau_{\text{eff}}$ ) is measured.
- A steady increase in lifetime is expected as the damage is being removed and maximum  $\tau_{\text{eff}}$  is obtained for a sample with damage free surface.
- Silicon thickness removed from each side represents the damage depth. Figure 3.14 is an illustration of ideal  $\tau_{\text{eff}}$  vs damage removed curve.
- Correct optical coupling and wafer thickness values have to be used while obtaining the lifetime data from the measurements.

*Ideal lifetime vs Damage removal curve*



**Figure 3.15** Illustration of ideal curve of change in  $\tau_{\text{eff}}$  as a function of damage layer thickness removed from each surface of the wafer.

Figure 3.15 is an experimental outcome of the above mentioned procedure on a DWC wafer (wire/grit size-120 $\mu\text{m}$ /12-25 $\mu\text{m}$ ). A dashed line is used for demarcation of damage depth (approximately 8.25 $\mu\text{m}$ ). Data labels shown in the figure are minority carrier lifetime values in micro seconds. In order to demonstrate the concept, these experiments are repeated on a multitude of wafers cut under different sawing conditions and the results are presented in the next chapter.



**Figure 3.16** Lifetime as a function of thickness removed from one side of a DWC wafer (Dashed line representing the damage depth of approximately 8.25 $\mu\text{m}$ ).

## CHAPTER 4

### SEQUENTIAL ETCHING AND MINORITY CARRIER LIFETIME

Experimental techniques such as measuring minority carrier lifetime and its interpretation need to be performed with utmost care as this technique is sensitive to a myriad of parameters such as surface conditions, sample preparation, passivation medium and the measurement method adopted. Quasi steady state/Generalized mode is used in evaluating the damage depth in this chapter. WCT-100 and WCT-120 (newer version of WCT-100) tools from Sinton's Instruments are used for the measurements.

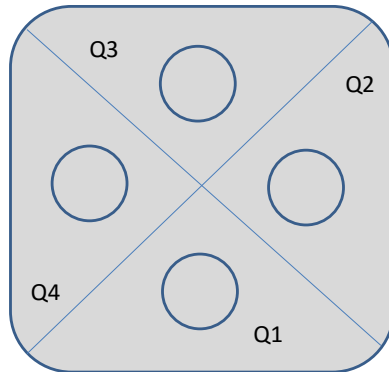
Both SWC and DWC wafers are chosen for this evaluation. Wafers cut using deferent wire/grit sizes and wire usage are chosen to investigate their effect on the damage distribution.

In this chapter, proper wafer preparation method, etching technique, reflectance and transmittance measurements, photoluminescence measurements, and minority carrier lifetime measurements performed on as sawn wafers are presented. The effects of each of the process parameters on the final outcome (evaluation of in-depth damage) are discussed in detail.

#### 4.1. Wafer Preparation

As-sawn silicon wafers are loaded with debris (from eroded wire or grit), organics from slurry, fine dust of morphed silicon, foreign materials from the sawing system and from wafer handling etc. Wafer preparation is a very crucial step as it affects all the subsequent processes and negatively influences the outcome if care is not taken.

In order to produce a data plot of damage depth versus thickness removed from each wafer surface, two as-sawn silicon wafers (156mm x 156mm) are cleaved into four quarters each (as shown in Figure 4.1) and weighed on a digital scale. This is done to avoid the errors in thickness measurements as the TTV on a wafer will vary greatly from one edge to the other.



**Figure 4.1** Illustration of sample preparation method for the damage depth evaluation, and location of minority carrier lifetime measurement region (marked in circles).

These wafer quarters are cleaned in solvent hood using iso-propyl alcohol, acetone and DI water, multiple times, to ensure that all the particulate contaminants and other debris are removed from the surface. Next the wafers are cleaned in Piranha (1:2 ::  $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2$ ) at  $80^\circ\text{C}$  and dipped in HF solution for 3 minutes to remove any organics that may interfere with the uniform etching of the wafer surfaces. Next, samples are sequentially etched in 115 solution (described in detail in Section 4.2) and then cleaned in piranha solution before passivating and measuring the minority carrier lifetime.

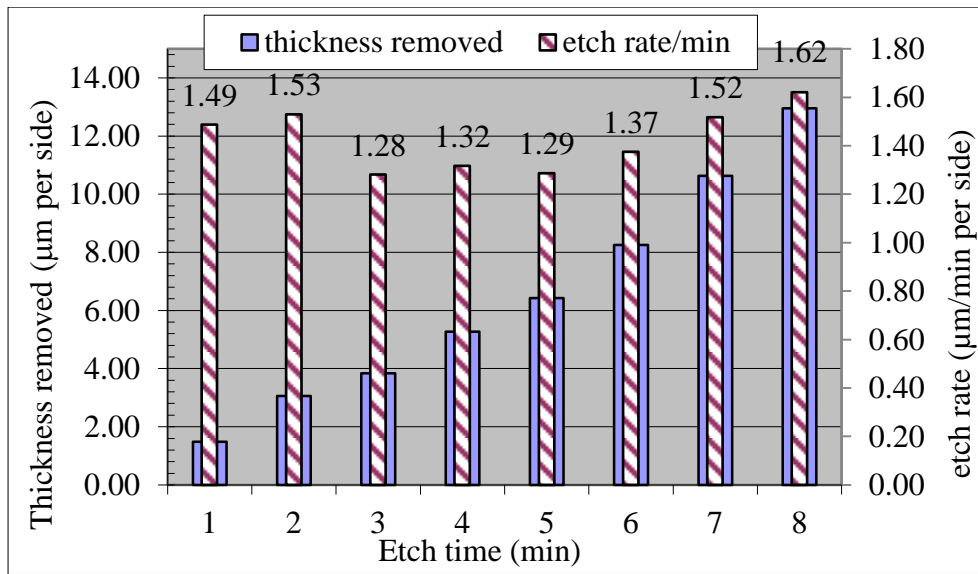
## 4.2 Etching

There are a variety of etchants available to etch the silicon sample surface. Here, in these experiments, an etchant that was previously developed for slow and uniform etching of Si



for similar experimental purposes is used. Like many other etchants, the etch rate of this etchant is sensitive to the damage at the surface and many other factors including activation time, surface roughness, agitation, volume of etch relative to the wafer size, etch duration.

All the eight wafer quarters are cleaned as described in the previous Section and etched in sequence one by one in one minute time increments. Figure 4.2 shows a bar chart representation of the thickness removed (on primary y-axis) and etch rate (on secondary y-axis) as a function of etch time of two DWC wafers cut into eight quarters (cutting wire/grit size 120/12-25  $\mu\text{m}$ ).

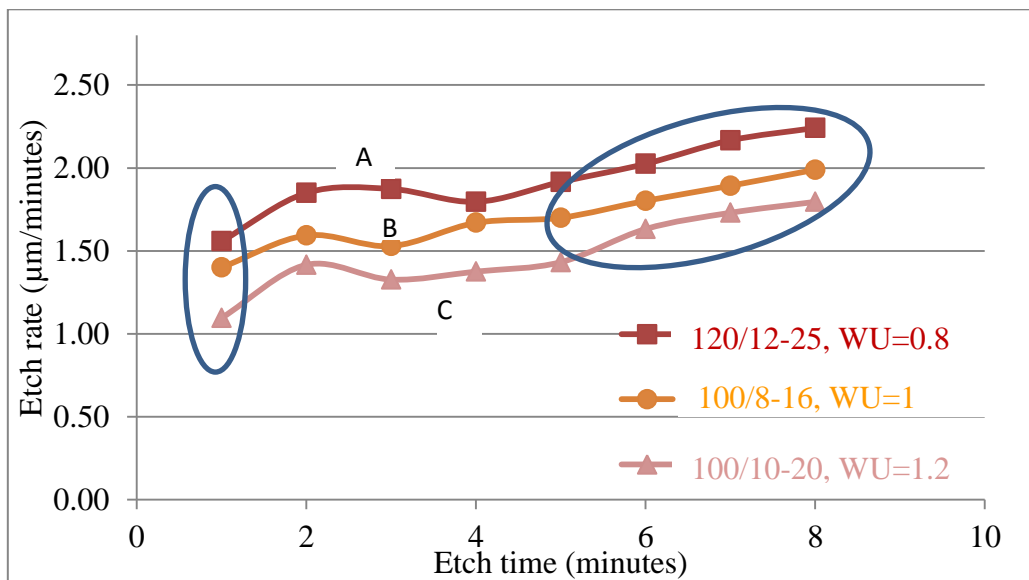


**Figure 4.2** Bar chart representation of sample thickness removed and etch rates vs etch time.

The initial lower etch rate can be explained by the low activity and presence of morphed silicon layers on the wafer surface. As silicon begins to etch in the solution, chemical activity of the solution increases, so as the etch rate. Suddenly, we find a low etch rate point in this sequence where the damaged region is supposedly etched off

completely. Then, slowly, the etch rates for the subsequent samples increase with etch time. From this point onwards, etch rate has only upward trend and is determined by the increase in etchant activity only. Figure 4.3 is a comparison of etch rates in DWC wafers cut by various wire/grit sizes. This non-uniform etch rate can be reconciled by keeping the following etch characteristics in mind:

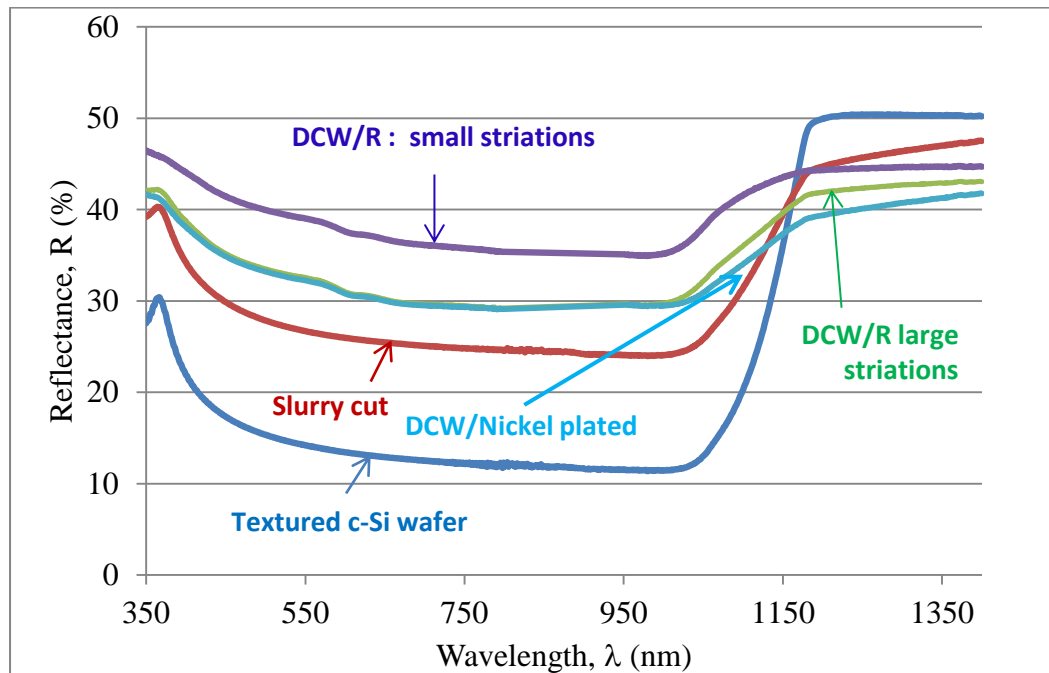
The initial reactivity of the etchant depends on the degree of the surface damage. Figure 4.3 shows etch rate vs etch time for three sets of samples, labeled as A, B, and C, cut by diamond wire sawing. Each set was cut under different conditions viz. wire size, diamond grit size, wire usage (WU- meters/wafer) etc. These cutting conditions introduce different degrees of damage at the surface and produce different in-depth damage distributions below the surface. Sample set A has the highest initial etch rate indicating highest degree of damage resulting from the most used wire, while sample set C has the lowest etch rate indicating the least degree of damage resulting from the lower wire usage.



**Figure 4.3** Etch rate as a function of etch time for three batches of DWC wafers cut under different sawing conditions.

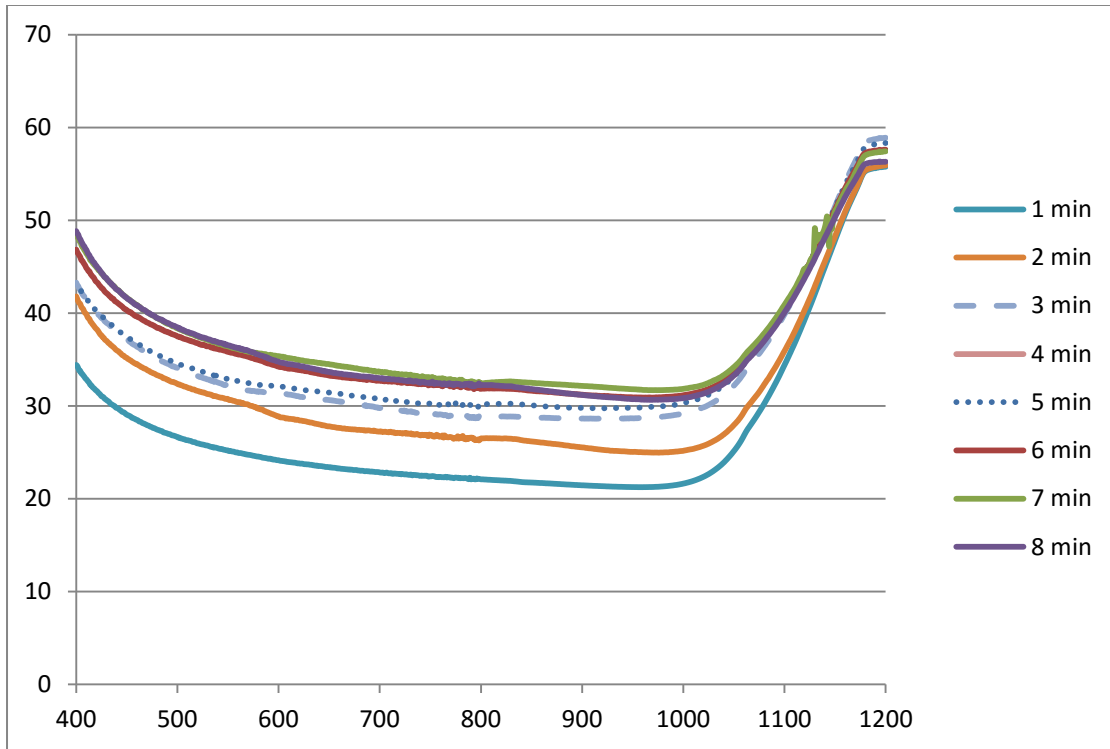
### 4.3 Changes in Reflectance and Transmittance

The original as-sawn surface is very shiny and reflectance values vary from 24% to 35% depending on the cutting method and wire/grit sizes. Reflectance spectra are obtained in diffused mode using a Cary 6000i Spectrophotometer by Agilent Technologies. Figure 4.4 shows reflectance spectra obtained from as-sawn crystalline silicon wafers cut by various sawing methods.



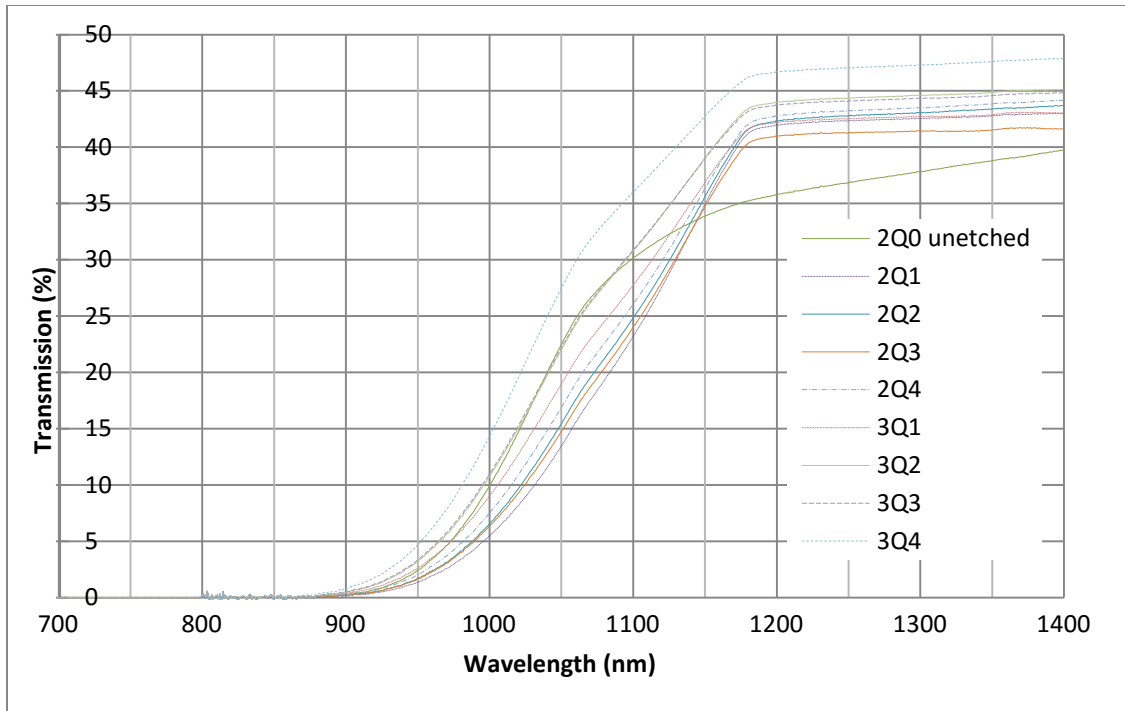
**Figure 4.4** Reflectance spectra of crystalline silicon wafers cut under different conditions.

After initial etching in 1:1:5 solution, all the samples change in appearance (become dull) and the reflectance value plummets to 22%. After each etch step, reflectance increases and saturates at around 30-32%. Similar results were reported previously by Holt et al. (2010). From Figure 4.5, we can deduce that the samples become rough after the initial 115 etching and, after four to five etch steps, their reflectance saturates.



**Figure 4.5** Reflectance spectra of DWC cut crystalline silicon wafer etched for different times.

Wafer manufacturers are able to produce thinner silicon wafers because of the advancements in the sawing technology. As the wafer thickness becomes smaller, they will become more susceptible to transmission losses. Thin (145  $\mu\text{m}$ ) as-sawn wafers are obtained from commercial silicon wafer manufacturers, and are etched further to remove the surface damage. Transmittance measurements are carried out using the spectrophotometer in diffused mode using an integrating sphere. Figure 4.6 shows that the transmittance spectra is fluctuating and is speculated to be related to the damage distribution in the wafer quarter and because of the TTV variations present in the wafer itself.



**Figure 4.6** Reflectance spectra of a thin (145µm) DWC cut crystalline silicon wafer etched for different times (from 2Q1 to 3Q4 in 0.5 min increments in etch time, removing approximately 1µm at a time).

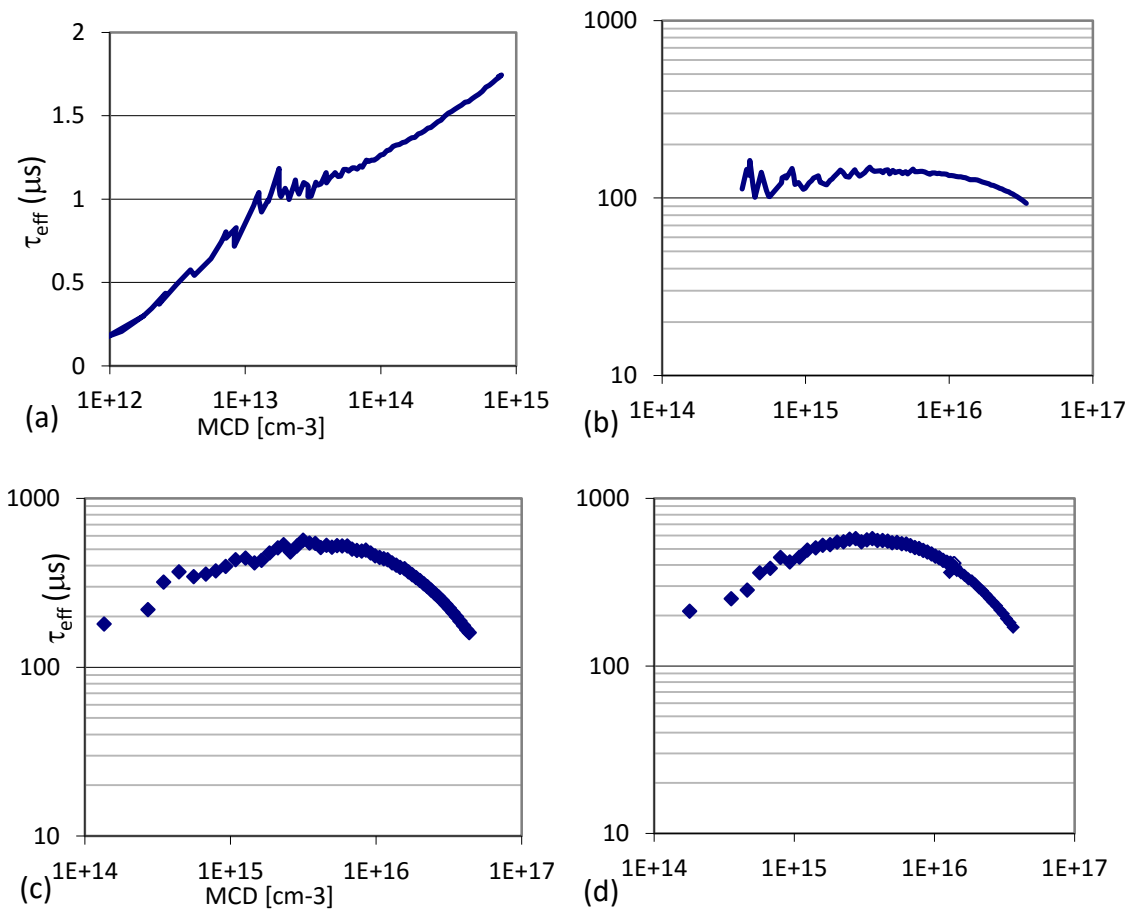
Accurate determination of these reflectance and transmittance data is necessary in obtaining correct optical coupling and that corrected coupling coefficient must be used in the lifetime measurements. Similar arguments were made regarding the transmission losses in silicon by Brody et al. (2001).

#### 4.4 Minority Carrier Lifetime

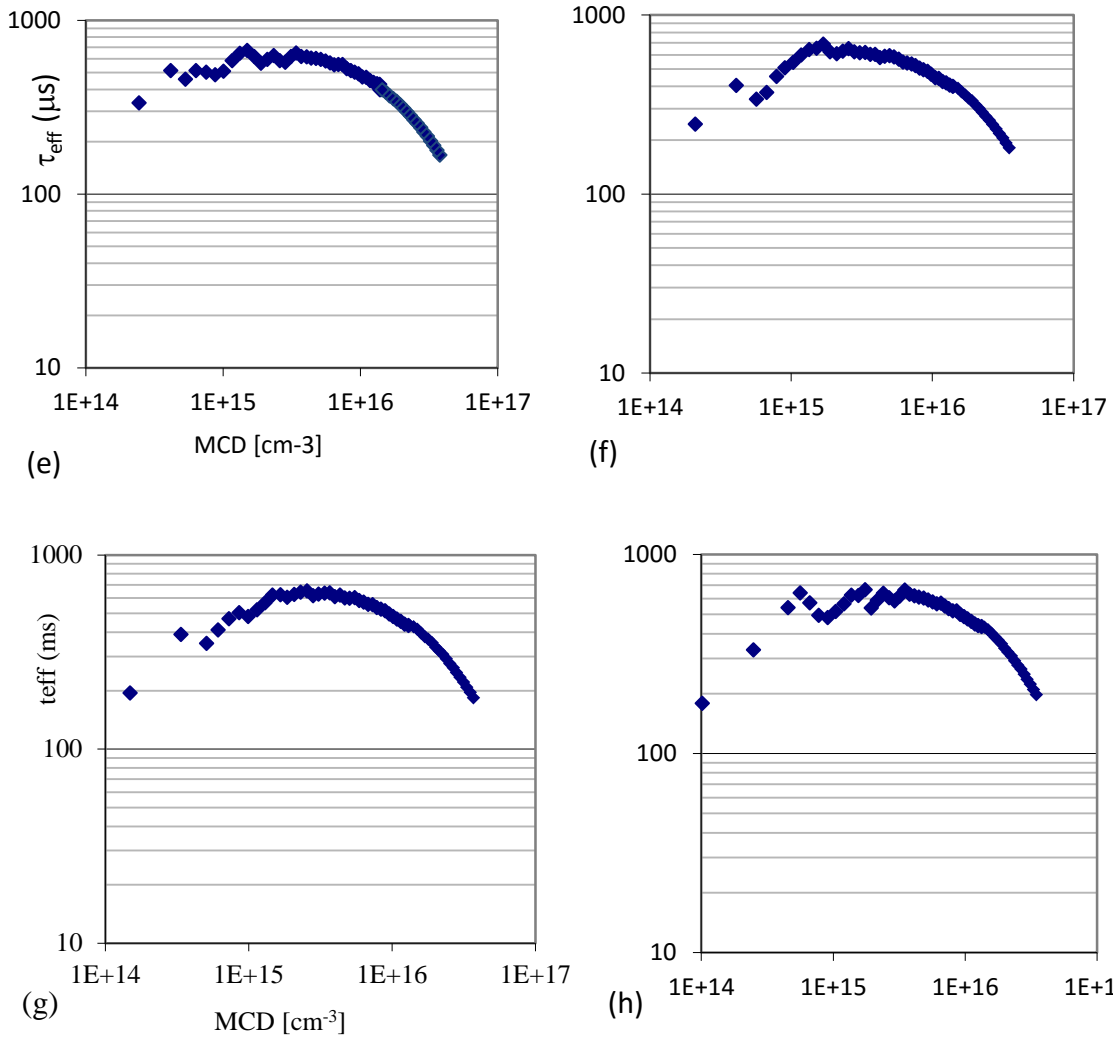
The etched and cleaned samples are placed inside a polyethylene bag and passivated with Iodine-Ethanol for lifetime measurements. Although the lifetime measurement can be done directly on etched wafers without an external passivation medium, the sensitivity of the measurement and its accuracy can be greatly enhanced by using passivation such as Iodine-Ethanol or Quinhydrone-Methanol. In this study, the minority carrier lifetime was

measured using Sinton tools (WCT-100 and WCT-120). These systems use flash lamps as light sources and measure photoconductance either in a quasi-steady state (typically used for lower lifetime wafers) or as a transient decay (longer lifetime wafers).

Figure 4.7 shows the effective minority carrier lifetime data plots as a function of minority carrier density for various samples etched for various times. These wafers are cut in DWC method with 120/10-20  $\mu\text{m}$  wire/grit size.

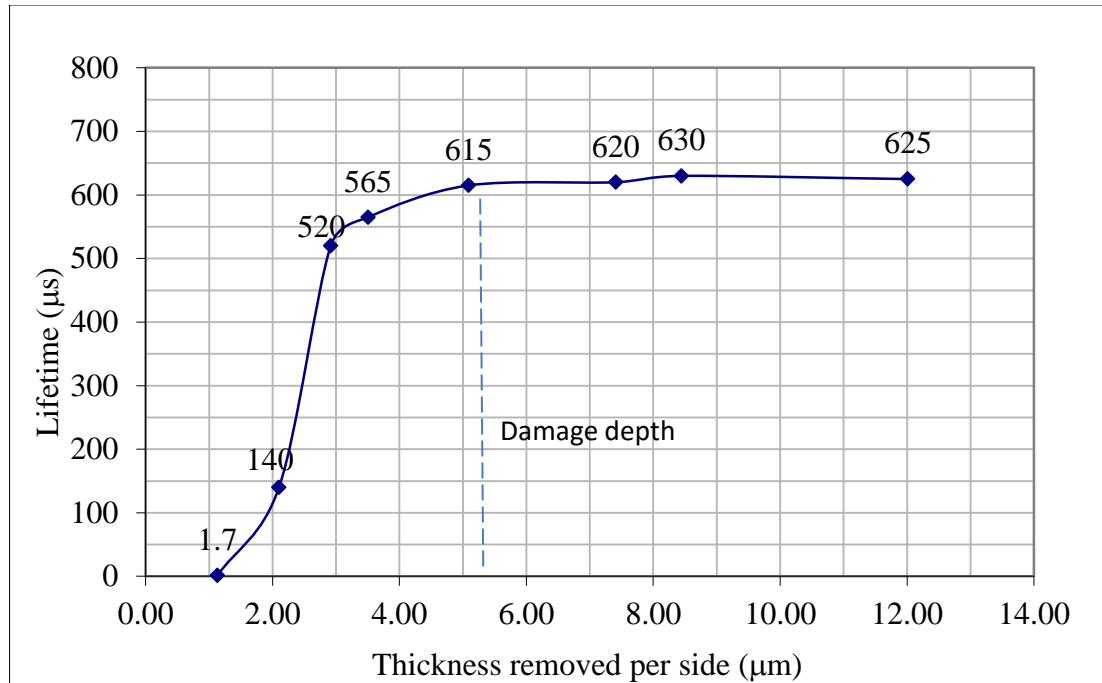


**Figure 4.7** Minority carrier lifetime measurements performed on sequentially etched DWC cut crystalline silicon wafer quarters. Samples are etched for different times (a) 0.5 min (b) 1 min, (c) 1.5 min, (d) 2 min, (Continued).



**Figure 4.7** (Continued) Minority carrier lifetime measurements performed on sequentially etched DWC cut crystalline silicon wafer quarters. Samples are etched for different times (e) 3 min, (f) 4 min, (g) 5 min and (h) 6 min.

Peak value of the minority carrier lifetime is taken from each data plot and used in generating the minority carrier lifetime versus thickness removed curve shown in Figure 4.8.

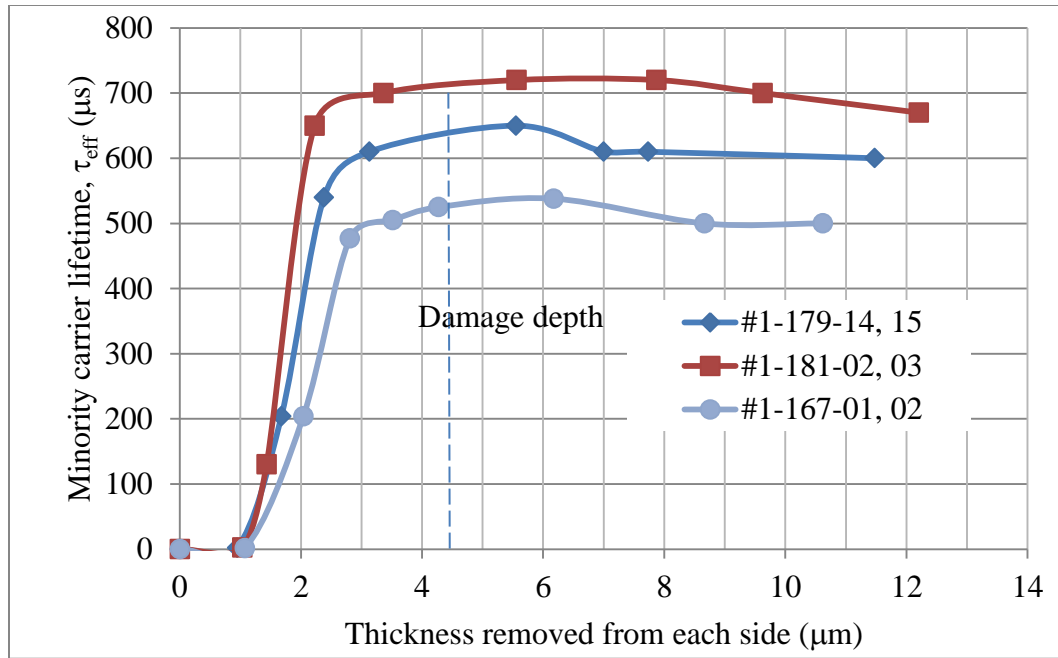


**Figure 4.8** Minority carrier lifetime vs thickness removed plot of DWC cut crystalline silicon wafer quarters. Samples are etched for different times (etch times mentioned in the caption of Figure 4.7).

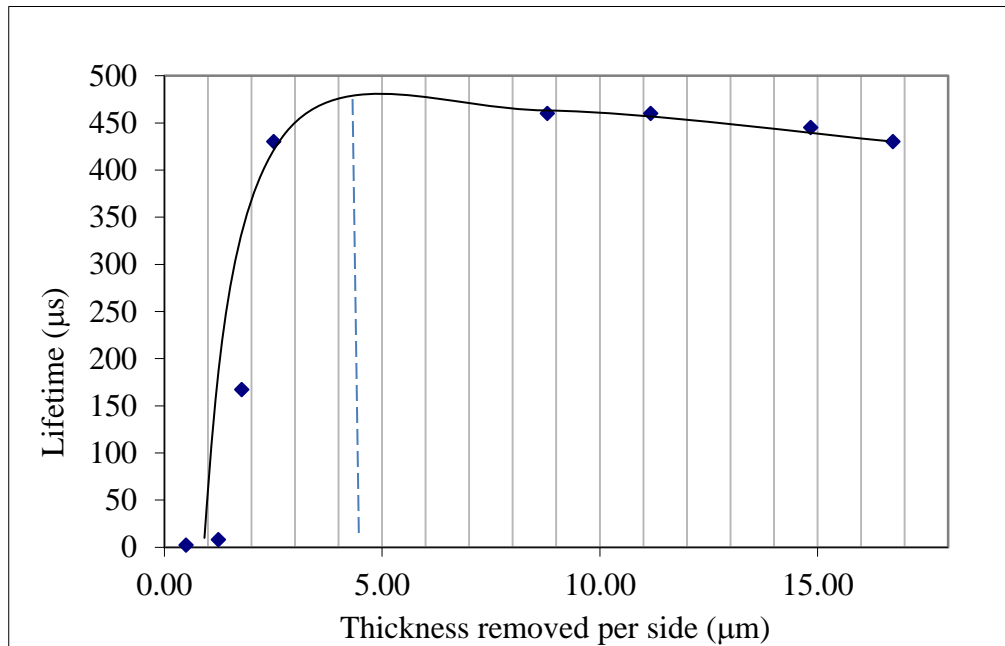
Similar measurements are performed on three more sets of wafers cut from three different ingots using 100/10-20 µm wire/grit [see Figure 4.9]. The resultant curves yield a damage depth that is very close to the damage depth found in wafers used in generating the data for Figure 4.8. Note that, although the material quality of these ingots is different, they yielded similar damage depth values.

Figure 4.10 shows DWC wafer cut using thin wire/grit (80/6-12 µm), and the surface damage generated is less than 5µm. This is in accordance with the fact that thinner wire/grit will generate lesser damage.





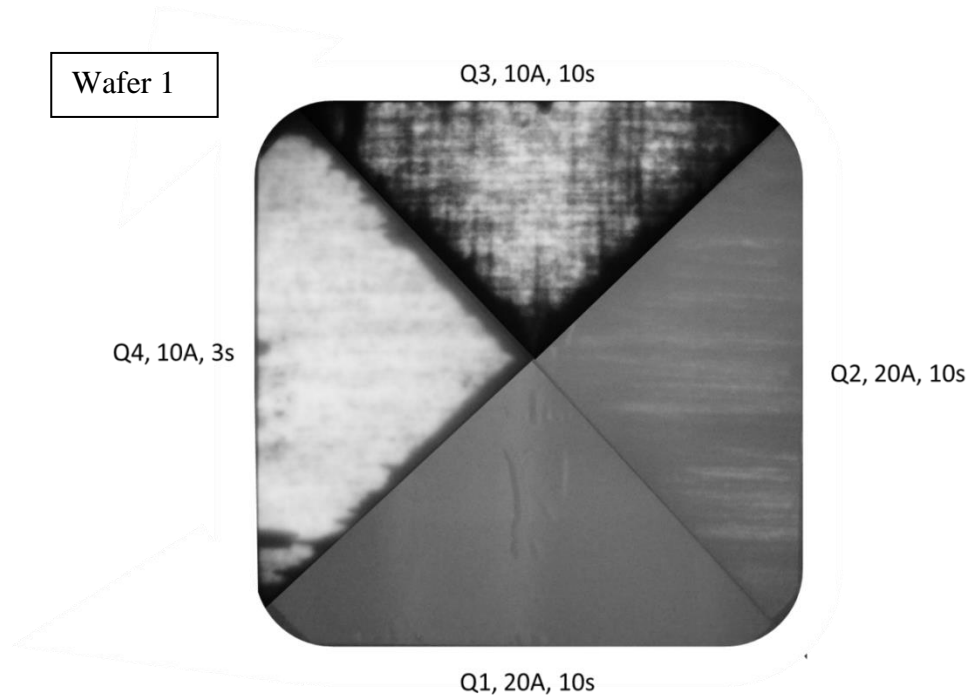
**Figure 4.9** Minority carrier lifetime vs thickness removed plot of DWC cut crystalline silicon wafer quarters from three different ingots (#179, #181, and #167). Samples are etched for different times (etch times mentioned in Figure 4.7 caption).



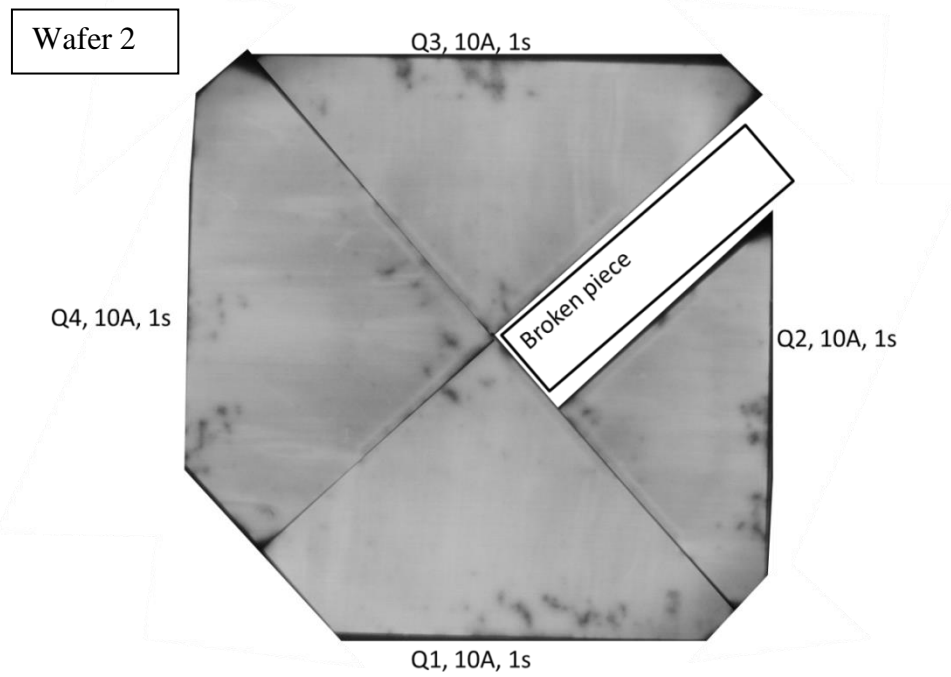
**Figure 4.10** Lifetime versus thickness removed plot of DWC cut wafer wire/grit size (80/6-12 μm).

## 4.5 Photoluminescence

Photoluminescence imaging is utilized in obtaining qualitative data on the wafer quarters etched for different times. Its resolution is more than that of microwave-PCD imaging and provides a more detailed qualitative analysis of residual damage on the etched wafer surface. Figure 4.11 shows PL images of a set of wafer quarters etched in incremental time steps. Quarter 1 and Quarter 2 does yield no and very feeble PL signal, respectively. From Quarter 3 onwards, intensity of the PL signal improves and saturates after a few etch steps. Figure 4.12 shows wafers quarters Q1 to Q4 which are etched for greater time steps than the quarters shown in Figure 4.11. Saturation of PL intensity is obvious from these images.



**Figure 4.11** PL images of wafer quarters etched in one minute incremental time steps (for 1, 2, 3 and 4 minutes) (in the order Q1 to Q4) (Current through laser diodes is mentioned in Amperes and exposure in seconds).



**Figure 4.12** PL images of wafer quarters etched in one minute incremental time steps (for 5, 6, 7, and 8 minutes) (in the order Q1 to Q4) (Current through laser diodes is mentioned in Amperes and exposure in seconds).

## CHAPTER 5

### THEORETICAL MODEL FOR EVALUATION OF IN-DEPTH DAMAGE

#### 5.1 Introduction

Many researchers have attempted to characterize and model the minority carrier lifetime in thin epitaxial layers grown on thick silicon substrates (Takahashi et al., 2000; Meakawa et al., 1995; Schroder et al., 2003; Boulou et al., 1977; Phillips et al., 1972; Park et al., 2001). Changes in either surface photo voltage or excess carrier concentration are used for characterizing thin epi layers in all these models. But no attempts were made to model the in-depth distribution of damage present in sawn silicon wafers.

Damage depth can be estimated from the minority carrier lifetime measurements performed on silicon wafers that are etched sequentially (to remove the damage layer thickness gradually). This effective minority carrier lifetime ( $\tau_{\text{eff}}$ ) can be converted into effective surface recombination velocity ( $S_{\text{eff}}$ ) which will be used to quantify the in-depth distribution of damage. However, models to convert lifetime data into local recombination velocity ( $S$ ) do not exist. This local recombination in damage layers will yield a more accurate distribution of in-depth damage distribution.

In this chapter, we present a simplified model for determining the in-depth damage distribution and compare it with the experimental results and discuss possible improvements to this model.

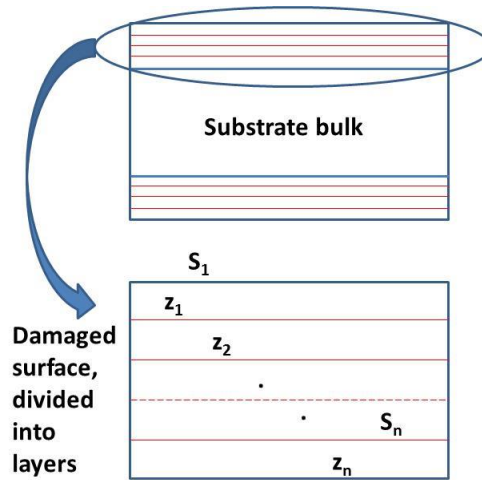
## 5.2 Theoretical Model

The effective surface recombination velocity ( $S_{\text{eff}}$ ) is an integrated effect of the carrier recombination in the whole damaged layer, and is not an accurate measure for the in-depth distribution of the damage. The reason is the following: the recombination in each sub-surface damage layer may vary greatly and it depends on the sample surface roughness, reflection, transmission, and absorption in those layers.

Local recombination ( $S$ ) in each of these layers has to be derived by solving the continuity equation for excess minority carrier density ( $\Delta n$  or  $\Delta p$ ) in each of these damage layers while accounting for all the losses due to the above mentioned parameters. The data plot of resultant  $S$  vs. damage thickness removed from each surface gives the real in-depth damage distribution for that sample. In order to obtain more detailed information, theoretical approach involving a layered model is proposed.

The proposed theoretical idea is as follows:

- In this method, whole damage region is divided into thin layers of different material characteristics and continuity equation is used for minority carrier concentration in these layers. Figure 5.1 is an illustration of such a layered structure of the damaged region.
- The minority carrier lifetime, thickness removed, and reflectance values (measured experimentally) and effective surface recombination (deduced from peak minority carrier lifetime measured) of the step etched wafers are used in these calculations.



**Figure 5.1** Illustration of layered model of the surface damage on a silicon wafer.

- Continuity equation for the excess carrier density in an n type wafer at a given depth ( $z$ ) can be written as,

$$\frac{\Delta n(z)}{\tau_n} = G(z) + D_n \cdot \frac{d^2[\Delta n(z)]}{dz^2} \quad (5.1)$$

where,

$\Delta n(z)$  = Excess minority carrier density,

$G(z)$  = Generation rate,

$D_n$  = Diffusion coefficient,

$\tau_n$  = Minority carrier lifetime,

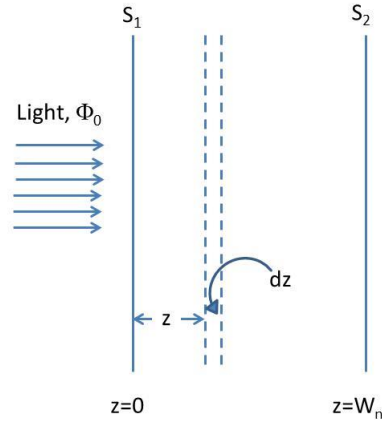
- Assuming the incoming light flux on the front surface of the wafer to be  $\Phi_0$ , the light flux at plane  $z$  is [see Figure 5.2],

$$\Phi(z) = \Phi_0(1 - R)e^{-\alpha z} \quad (5.2)$$

where,

$\alpha$  = Absorption coefficient of incoming light in silicon,

R= Reflectance,



**Figure 5.2** An illustration of a silicon wafer sample illuminated from one side.

- The generation rate is equal to the rate at which incident photons are being absorbed,

Within a finite length  $dz$ ,

$$\begin{aligned}
 G(z).dz &= \Phi(z) - \Phi(z + dz) \\
 &= \left[ \frac{d\Phi(z)}{dz} \right].dz \\
 &= (1 - R)\Phi_0\alpha e^{-\alpha z} dz
 \end{aligned} \tag{5.3}$$

So, using eq. (5.3), eq. (5.1) can be written as,

$$\frac{\Delta n(z)}{\tau_n} = (1 - R)\Phi_0\alpha e^{-\alpha z} dz + D_n \cdot \frac{d^2[\Delta n(z)]}{dz^2} \tag{5.4}$$

The general solution for this equation is,

$$\Delta n(z) = A. e^{-\frac{z}{L_n}} + B. e^{\frac{z}{L_n}} + C. e^{-\alpha z} \quad (5.5)$$

Substituting eq. (5.5) in eq. (5.4) yields,

$$C = \left[ \frac{(1-R)\Phi_0\alpha\tau_n}{1-\alpha^2 L_n^2} \right]$$

- We will define boundary conditions for the above equation (5.5) after each layer of damage  $z_1, z_2, z_3, \dots, z_n$  is removed from each wafer surface,

$$D_n \left[ \frac{d[\Delta n(z)]}{dz} \right] = S_1 \Delta n(z) \quad \text{at } z_n = 0 \quad (5.6)$$

and,

$$D_n \left[ \frac{d[\Delta n(z)]}{dz} \right] = -S_2 \Delta n(z) \quad \text{at } z_n = W \quad (5.7)$$

Applying these boundary conditions eq. (5.6) and eq. (5.7) to eq. (5.5) will yield the constants A and B,

$$A = C \left\{ \frac{\left[ (S_2 - \alpha L_n)(1 - S_1)e^{-\alpha W_n} + (S_1 + \alpha L_n)(1 + S_2)e^{\frac{W_n}{L_n}} \right]}{\left[ (1 - S_1)(1 - S_2)e^{-\frac{W_n}{L_n}} - (1 + S_1)(1 + S_2)e^{\frac{W_n}{L_n}} \right]} \right\}$$



$$B = C \left\{ \frac{\left[ (S_2 - \alpha L_n)(1 + S_1)e^{-\alpha W_n} + (S_1 + \alpha L_n)(1 - S_2)e^{-\frac{W_n}{L_n}} \right]}{\left[ (1 - S_1)(1 - S_2)e^{-\frac{W_n}{L_n}} - (1 + S_1)(1 + S_2)e^{\frac{W_n}{L_n}} \right]} \right\}$$

$W_n$ = wafer thickness after the removal of a damage layer (If  $z_n$  is the thickness of the damage layer removed in each step and  $W$  is the original wafer thickness, the resultant wafer thickness will be  $W_n=W-(2.z_n)$ )

- The resultant excess carrier concentration  $\Delta n(z)$  is integrated over the whole damage layer thickness to obtain the recombination rate at that surface using following equation,

$$\frac{1}{\tau_s} = \frac{-D_n \left[ \frac{d[\Delta n(z)]}{dz} \right]_{z_n}}{\int_0^{z_n} \Delta n(z) dz} = \frac{2S}{z_n} \quad \text{at } z = z_n$$

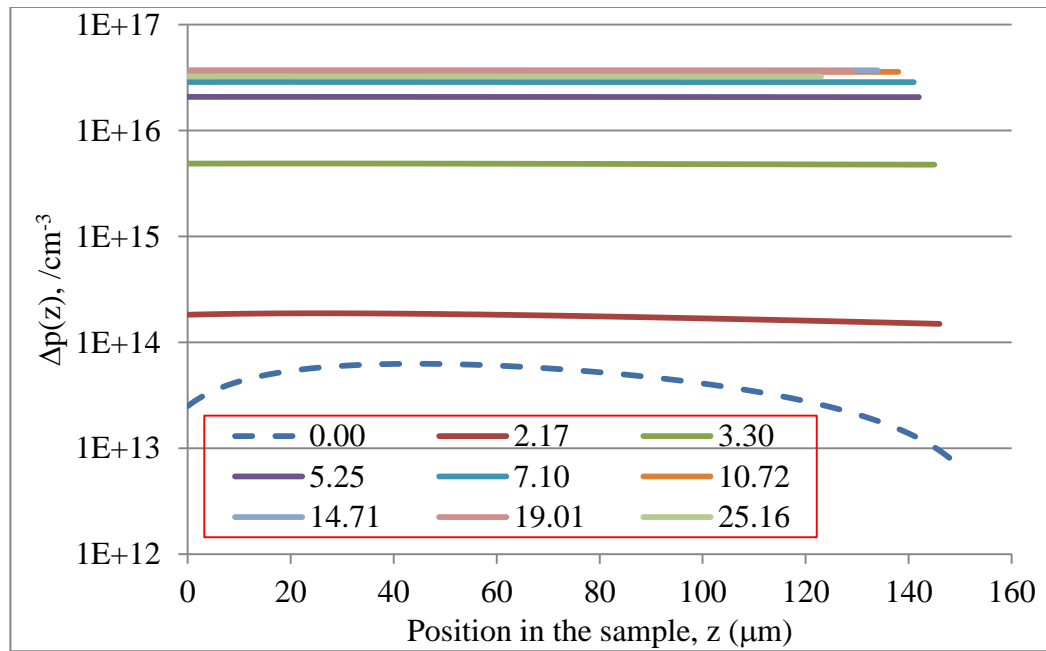
- Any changes in diffusion and/or absorption coefficient values result in the  $\Delta n(z)$  curve and in turn cause changes to  $S$ .  $S$  is plotted against the thickness removed from each side, the graph will represent a more accurate in-depth damage distribution.

### 5.3 Results and Discussion

As-sawn crystalline silicon samples (approx. 1 ohm-cm resistivity, both n type and p type) cut from different ingots using DWC method are chosen for analysis. Using the formalism mentioned in Section 5.2,  $\Delta p(z)$  plots for the entire sample thickness are

generated. Figure 5.3 shows the  $\Delta p(z)$  vs  $z$  plots for n type thin wafer (145  $\mu\text{m}$ ) etched for different times.

Absorption and diffusion coefficients are taken as  $\alpha=306 \text{ /cm}$ ,  $D_n=12 \text{ cm}^2/\text{s}$ . 900nm wavelength light of photon flux equivalent to 10 sun intensity is used for calculations. (While measuring the lifetime, the long-pass filter in the Sinton's system cuts off the visible light and only allows NIR spectrum of light). Reflectance data obtained from the measurements is used in these calculations.



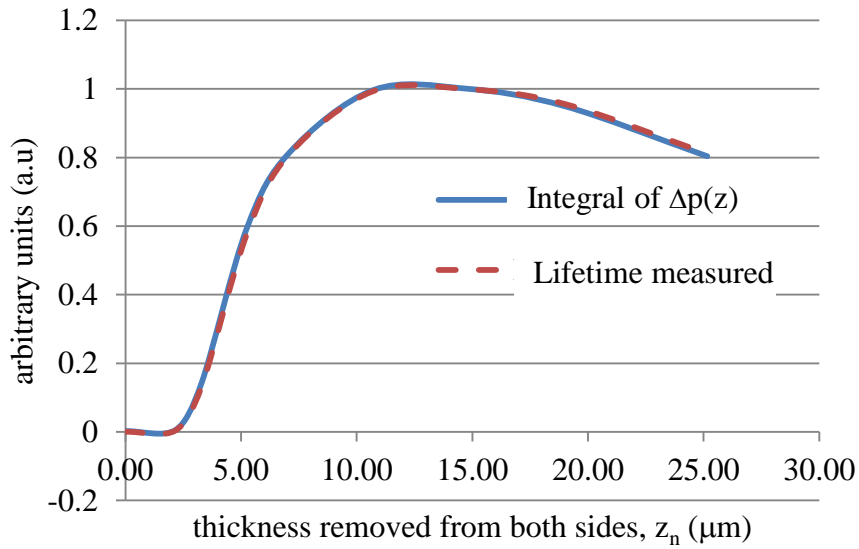
**Figure 5.3** Change in excess carrier density as a function of etch depth and location in the sample.

Table 5.1 provides the details of sample thickness and damage layer removed, and effective lifetime measured. Bulk lifetime of the material is estimated from the assumption that the peak lifetime (1590  $\mu\text{s}$  in this case) is realized when  $S_{\text{eff}}=2 \text{ cm/s}$ . From this bulk lifetime value,  $S_{\text{eff}}$  values for various steps have been calculated.

**Table 5.1** Material Property Values of n-type Si DCW Wafer Quarters Etched for Different Times

$\tau_{\text{Bulk}} (\mu\text{s})$	$S_{\text{eff}} (\text{cm/s})$	Damage removed both sides ( $\mu\text{m}$ )	Sample final thickness ( $\mu\text{m}$ )	$\tau_{\text{eff}} (\mu\text{s})$
3036	10475.44	0.00	147.69	0.7
3036	1020.94	2.17	145.52	7.11
3036	31.96	3.30	144.95	211
3036	5.41	5.25	142.44	918
3036	3.13	7.10	140.59	1290
3036	2.09	10.72	137.53	1580
3036	2.00	14.71	133.54	1590
3036	2.12	19.01	129.24	1520
3036	2.74	25.16	123.09	1290

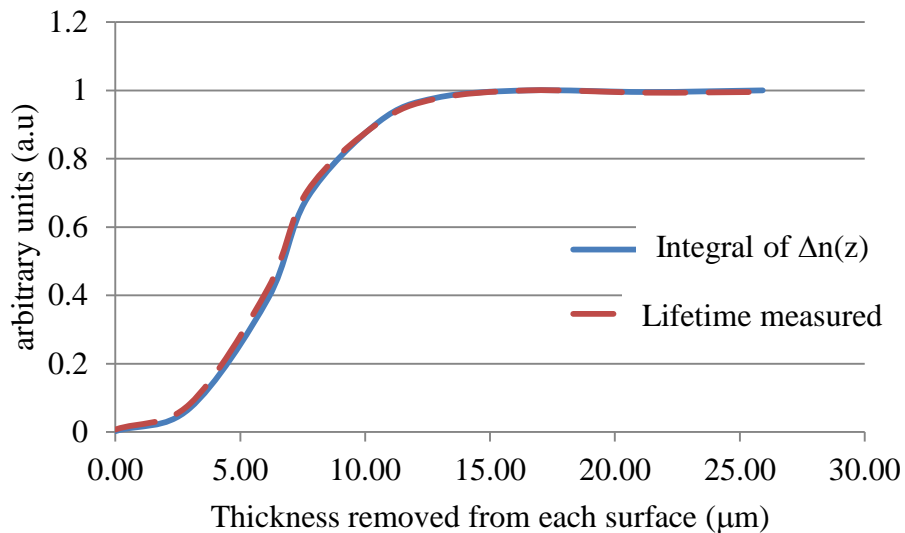
The integral of this excess carrier density is proportional to the sample conductivity. When these  $\Delta p(z)$  values are normalized and plotted against the normalized effective lifetime values, these two graphs will overlap and confirm the validity of the calculations.



**Figure 5.4** Normalized excess carrier density and lifetime plot as a function of thickness removed from each surface (n type 150  $\mu\text{m}$  thick wafer).

Change in diffusion coefficient or absorption coefficient does not result in significant shift in the  $\Delta p(z)$  profile. This can be justified because of the dominating effect of recombination term in the initial high damage layers. For these damage layers, the  $S_{\text{eff}}$  would be a proper term to define the local recombination distribution. As damage is being removed from the wafer surface, the diffusion and absorption coefficients reach the values of unperturbed silicon. The surface recombination becomes less effective compared to the diffusion and absorption parameters.

A similar calculation is performed for p type silicon and the absorption coefficient is assumed to be the same as for n type silicon, i.e.  $\alpha=306 \text{ /cm}$ , but the diffusion coefficient ( $D_n$ ) has been assumed to be  $36 \text{ cm}^2/\text{s}$ . Figure 5.5 shows change in  $\Delta n(z)$  as a function of etch depth.



**Figure 5.5** Normalized excess carrier density and lifetime plot as a function of thickness removed from each surface (p type 200  $\mu\text{m}$  thick wafer).

Table 5.2 provides the details of sample thickness and damage layer removed, and effective lifetime measured.

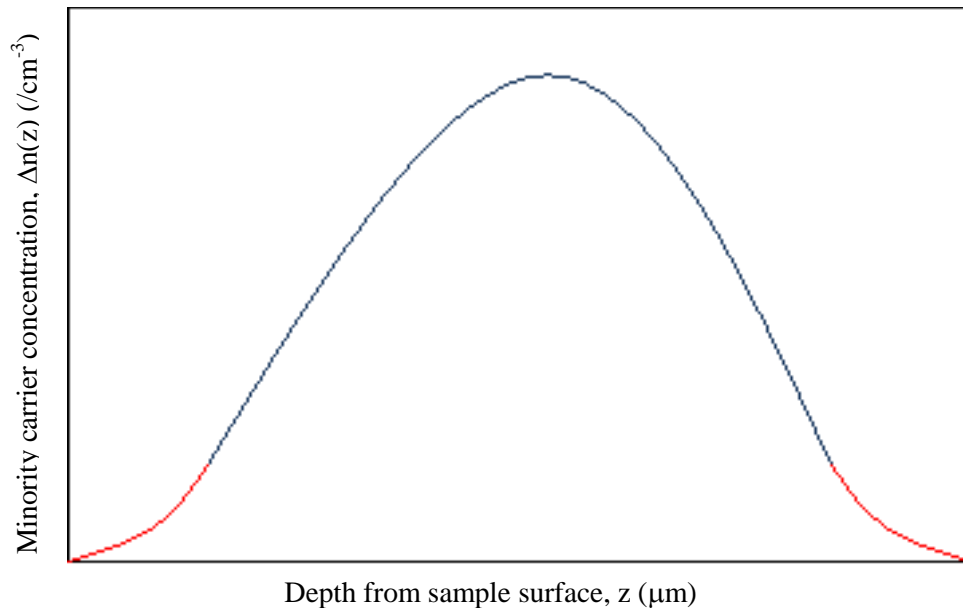
**Table 5.2** Material Property Values of p-type Si DCW Wafer Quarters Etched for Different Times

$\tau_{\text{Bulk}} (\mu\text{s})$	$S_{\text{eff}} (\text{cm/s})$	Damage removed both sides ( $\mu\text{m}$ )	Sample final thickness ( $\mu\text{m}$ )	$\tau_{\text{eff}} (\mu\text{s})$
463	9862.67	0.00	197.68	1
463	314.69	2.98	194.70	29
463	37.73	6.12	191.56	164
463	12.60	7.69	189.99	287
463	4.43	10.53	187.15	380
463	2.66	12.86	189.12	410
463	2.12	16.50	185.48	419
463	2.17	21.25	180.73	417
463	2.01	25.92	176.06	419

By considering the addition of damage layers (theoretically) on top of the single layer model discussed above, and solving for the excess carrier density in these layers, will yield a  $\Delta n(z)$  profile similar to the Gaussian shown in Figure 5.6. Local recombination distribution ( $S$ ) can be obtained using the following Equation (5.8) provided that  $D_n$  and  $\alpha$  of the layers are known accurately.

$$D_n \left[ \frac{d[\Delta n(z)]}{dz} \right] = S \cdot \Delta n(z) \quad \text{at } z = z_n \quad (5.8)$$

This local recombination value ( $S$ ) obtained from the above equation when plotted against the damage removed from each surface will yield an accurate in-depth damage distribution profile.



**Figure 5.6** Illustration of Excess carrier density as a function of depth in silicon wafer for a three layer model (A bulk layer and a damage layer on each side of it), red colored parts of the curve illustrate the minority carrier concentration profiles in the damaged layers.

## CHAPTER 6

### CONCLUSIONS

Experimental and theoretical exploration of the in-depth damage of as-sawn silicon wafers from this work will allow the following recommendations:

1. Sequential etching of silicon surfaces can be performed with accuracy and minority carrier lifetime measurement has been established as a reliable means for the evaluation of damage depth in crystalline silicon wafers.
2. Crystalline silicon wafers cut with various wire/grit sizes are analyzed using the sequential etching and minority carrier lifetime measurement technique. Grit size and wire usage have high impact on damage depth. The lower wire usage and bigger grit sizes produce high damage on the wafer surface.
3. Degree of damage can be estimated from etching experiments. A lower initial etch rate implies that the degree of the surface damage is lower. Lower wire usage i.e. more fresh wire fed into the system for cutting wafers will result in lesser surface roughness and smaller in-depth damage.
4. Theoretical evaluations suggest that absorption in damaged layer has minimal influence on effective minority carrier lifetime measurements; generally, effective surface recombination velocity ( $S_{\text{eff}}$ ) is sufficient to describe the in-depth distribution of damage.
5. Accurate knowledge of diffusion coefficient ( $D_n$ ) and effective minority carrier lifetime of the damage layers is necessary for solving the multilayer model for the determination of in-depth damage distribution in silicon wafers.

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