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ABSTRACT

STUDY OF DEEP LEVEL DEFECTS OF n^+-CdS/p-CdTe SOLAR CELLS

by
Poonam Rani Kharangarh

Among various photovoltaic materials, polycrystalline cadmium telluride thin film is now the most promising material, due to its low production cost excellent stability and reliability. Current-voltage and capacitance-voltage measurements of CdTe photovoltaic devices at different temperatures can provide valuable information about non-idealities in the n-p semiconductor junction. There are certain limitations which limit the efficiency of CdTe solar cells. There is no real distinction between defects and impurities in CdTe solar cells as both act as beneficial dopants or detrimental traps unlike Si where intentional shallow dopants and traps are distinctly different. Therefore, the role of defect states on CdTe solar cell performance, the effect of processing on defect states, and simple and effective characterization techniques must be investigated and identified.

In this research the thin film n^+-CdS/p-CdTe solar cells made with evaporated Cu as a primary back contact, are characterized by using the temperature dependence of the reverse bias diode current (J-V-T) to determine the energy levels of deep defects. The results of the J-V-T measurements on solar cells made at NJIT show that while modest amounts of Cu enhance cell performance, an excessive high temperature annealing step degrades device quality and reduces efficiency. This work addresses the error that can be introduced during defect energy level estimation if the temperature dependence of the carrier capture cross-section is neglected. Therefore, the location of traps is derived using a Shockley-Read-Hall recombination model with modified assumptions.

A Cu-related deep level defect with activation energy of 0.57eV is observed for Cu evaporated back contact cells and an intrinsic defect with activation energy 0.89eV is found. Frequency dispersion in Capacitance-Voltage measurements confirms the presence of Cu-related deep level traps for cells with a Cu evaporated back contact, whereas no such defects are observed in carbon paste contact. The behavior is believed to be due to diffusion of excess Cu from the contact. It is further observed that majority carrier deep level traps (Cu-related or intrinsic) contribute differently to the degradation of electronic properties of the CdTe solar cells.

A simple and effective characterization technique based on temperature dependent capacitance spectroscopy (TDCS) is used to identify majority carrier trapping defects in thin film n^+-CdS/p-CdTe solar cell, made with evaporated Cu as a primary back contact. The distinct deep level traps, observed by TDCS seem to be due to the ionization of impurity centers located in the depletion region of n^+-CdS/p-CdTe junction.

STUDY OF DEEP LEVEL DEFECTS OF N^+-CdS/P-CdTe SOLAR CELLS

by
Poonam Rani Kharangarh

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APPROVAL PAGE

STUDY OF DEEP LEVEL DEFECTS OF n^+-CdS/p-CdTe SOLAR CELLS

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To my beloved parents and dear husband, Nishant and
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LIST OF ABBREVIATIONS

AC	Alternating Current
AM1.5	Standard solar spectrum after 1.5 terrestrial atmospheres
Å	Angstrom (10^{-10} meters)
AS	Admittance Spectroscopy
CB	Conduction Band
CBD	Chemical Bath Deposition
CdTe	Cadmium Telluride
CdS	Cadmium Sulphide
CSS	Closed Spaced Sublimation
C-V	Capacitance Voltage
C-V-T	Temperature dependent Current Voltage
DLTS	Deep Level Transient Spectroscopy
EHP	Electron hole pair
HRT	Highly Resistive Transparent Layer
J-V	Current Voltage
J-V-T	Temperature Dependent Current Voltage
PL	Photoluminescene

QE	Quantum Efficiency
SRH	Shockley Read Hall
TCO	Transparent Conducting Layer
TDCS	Temperature Dependent Capacitance Spectroscopy
TSC	Thermally Stimulated Current
TSCAP	Thermally Stimulated Capacitance
VB	Valence Band

CHAPTER 1

INTRODUCTION, MOTIVATION AND OBJECTIVES

1.1 Introduction

The photovoltaic solar cell converts solar energy directly into electricity. The first practical solar cells were made using crystalline silicon. Because of the cost of materials and manufacturing of crystalline silicon, thin film alternatives were explored. The three principal thin film technologies are amorphous silicon (a-Si), copper indium gallium selenium (CIGS), and cadmium telluride (CdTe). Each technology has its relative strengths and weaknesses. Thin film solar cell technology has relatively low production cost because of the reduced material purity and the relatively simple in-line processing steps and equipment. However, light to current conversion efficiency is important, since this enters into the total cost seen by the end-user. Amorphous silicon thin film solar cells appear unattractive because of their low efficiency~6%. Copper Indium Gallium Selenium (CIGS) has much higher absorption than silicon, so a layer of CIGS can absorb more light than a silicon layer of the same thickness because of high efficiency~20.4%.

The first CdTe thin film solar cells were prepared by Cusano [1] in 1963 with the structure of CdTe/$Cu_{2-x}Te$. In this structure CdTe was used as the n layer and $Cu_{2-x}Te$ as the p layer. The cells have efficiencies close to 6% but were not stable. The first CdTe/CdS solar cells were proposed by Andirovich [2] in 1968, who achieved 1% efficient devices at that time. Due to the energy crisis in the early 1970's, more funding was put into the PV research. The progress of CdTe/CdS solar cell has been very fast. In 1981, Kodak achieved 10% efficient devices. AMETEK achieved 12% devices in 1990. After 1990, USF, Photon Energy and BP alternatively led the research. In 1992,

Ferekides and J. Britt achieved 15.8% efficient devices. This record remained for nearly 10 years. In 2001 X. Wu [3] from NREL achieved a new record efficiency of 16.5%. This record was only recently broken (Feb 2013) when First Solar (FSLR) [4] demonstrated an 18.7% laboratory efficiency with 1 sun illumination for the thin film n^+-CdS/p-CdTe hetero-structure. Thin-film photovoltaics modules currently have a worldwide production of about 12% of the total module production, which is dominated by crystalline silicon technology. However, much improvement is theoretically possible as CdTe has a near-optimal band gap ~ 1.5eV corresponding to an ideal efficiency of 29% [5]. It is important to realize that the assumptions that make for an ideal diode are (1) a shallow dopant energy level as close as possible to the band edge, (2) a very low or nonexistent recombination-generation R-G center concentration with energy level between the Fermi and intrinsic energy levels and (3) Perfect (Ohmic contacts).

The typical polycrystalline n^+CdS/p-CdTe cell which uses TCO (transparent conducting oxide) as a front contact and a copper-containing back contact, is shown in Figure 1.1.

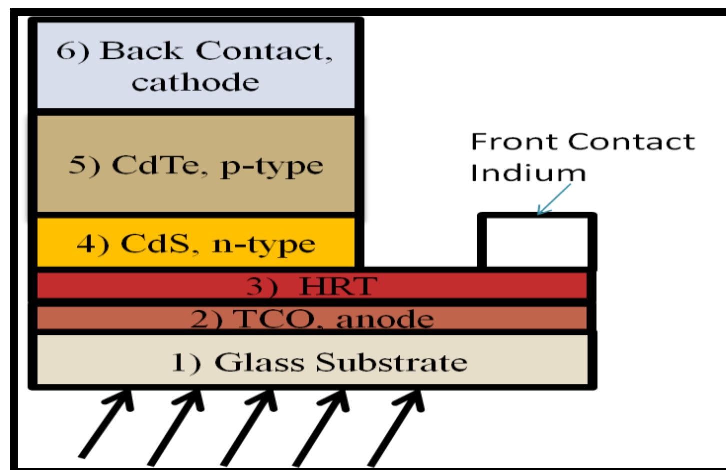


Figure 1.1 Device structure of CdTe Solar Cell.

CdTe is called a defect semiconductor because its native defects are responsible for electrical properties. The electrical properties (which strongly affect the solar cell efficiency) depend on recombination centers, diffusion and defects/impurities and need to be controlled by processing consistent with low cost. In today's practical thin film photovoltaic devices, various measurement techniques and a number of physical mechanisms are used to interpret the nature of the defects. In the last decade, the results of several investigations of defect levels in CdTe have been reported [6 - 28]. It is known that Cd vacancies are the predominant defects in thin-film polycrystalline CdTe material. These vacancies are present both with singly and doubly charged states and produce defect states near the mid-gap [14]. Also, the cadmium vacancy (V_{cd}^{2-}) sites behave as doubly ionized acceptor levels. The activation energy of these levels is reported as 0.33eV [15], 0.73eV [16] 0.6eV [17] and 0.8eV [18]. Te vacancies are identified with 0.38eV [19]. This complicates the data interpretation and leads to discrepancies in proper identification of shallow and deep trap levels [9].

It is known that an impurity acts as a trap or a generation and recombination (G-R) center depending on the trap energy level E_t, the location of the fermi level in the band gap, the temperature, and the capture cross-section of the impurity/trap. But in the case of CdTe solar cells, some of the observed activation energies of dopant levels are non-shallow. The partially ionized dopants, therefore, play the role of both an advantageous dopant as well as a detrimental trap [12]. The consideration of simplified assumptions, which may be completely valid for silicon, may not be accurate in CdTe solar cells. In addition, the performance of CdTe solar cells are highly influenced by the deep levels as

the deep levels control the efficiency and charge transport properties. CdTe involves a large concentration of intrinsic defects, produced during the fabrication process.

Copper and Chlorine are common elements found in CdTe as both are used during the fabrication process. Chlorine in CdTe (introduced into the solar cell processing as a $CdCl_2$ treatment to passivate the CdTe grain boundary dangling bonds) can appear as the shallow level chlorine substituting tellurium (Cl_{Te}^{+}) with the ionization energies reported as 0.014-0.017eV [8,17]. Chlorine also acts as a singly charged acceptor forming a V_{Cd}^{2-}/Cl_{Te}^{+} complex with reported values 0.052eV [17], 0.14-0.17eV [15, 17]. The Cu-based ohmic back contact to p-CdTe has been a significant cause of concern as Cu forms deep/semi-shallow defect sites that limits the cell efficiency. Cu related defects can decrease the lifetime, and hence reduced the open circuit voltage (V_{oc}) and fill factor (FF). Copper creates acceptor levels by substituting into Cd sites. Different techniques are used to find the Cu-related defects/traps in CdTe [7-11]. Also, the properties of the traps, related to copper, have been extensively studied [17]. Cu is a fast diffuser and it creates substitutional, interstitial and complex defects, so-called AX centers. However, Cu is assumed to be the p-type dopant in the $n^{+}p$ CdS/CdTe [18, 19]. It was also shown [29, 30] that during this step, Cu diffuses throughout the CdTe layer and is consistent with the reported high diffusion coefficients of Cu in CdTe [31, 32]. The ionization energy is reported as 0.3-0.35eV [13]. However, this Cu_{Cd}^{-} energy level is controversial with a wide range of results obtained from the activation energy of data from different techniques. Interstitial copper also has a majority carrier trapping defect which is reported to be deep level with activation energy ~ 0.55eV [17]. Studies [3-5] have shown that interstitial Cu impurities can behave as donors but can be converted to acceptors when

interacted with Cd vacancies and other Cu ions. Balcioglu et al. studied the Cu-related deep level impurities in polycrystalline CdTe/CdS solar cells [6]. Although significant work has been done about the properties of CdTe and CdS films, there remains a lack of fundamental understanding about the identification of electronic defect states in polycrystalline CdTe. Also, the role of Cu in CdTe is not clear so far. Therefore one must understand the role of defect states on a diode current and the effect of processing on the defect states.

The main characterization techniques used for study of deep levels in CdTe solar cells are based on admittance spectroscopy (AS), photoluminescence (PL), photo induced current transient spectroscopy (PICTS) and deep level transient spectroscopy (DLTS) measurements [6-28]. DLTS characterizes the deep levels by monitoring the transients of junction capacitance. But for highly resistive materials, DLTS is not as useful due to the small junction capacitance and difficulties in injecting free carriers with a voltage pulse. In addition, the transient analysis in DLTS is done through application of a pulse, where the pulse width and height were managed to accurately evaluate the CdTe layer. The activation energy E_a, trap concentration N_t, and the capture cross-section σ_∞, can be estimated from the Arrhenius plot, ln (T^2/e_p) versus 1/T. The simpler techniques known as temperature dependent Current- Voltage (I-V), temperature dependent capacitance spectroscopy (TDCS), temperature dependent capacitance voltage (C-V-T), thermally stimulated current (TSC) and thermally stimulated capacitance (TSCAP) techniques can be employed to estimate all the above parameters to identify the deep level traps [28]. As compared to admittance spectroscopy, which operates in the frequency domain, all these techniques are easy and quick techniques to evaluate defect levels in CdTe solar cells.

1.2 How to Improve the Performance of CdS/CdTe

Table 1.1 compares the world-record CdTe solar cell with the ideal one. It has been seen that J_{sc} is already 88% of theoretical value, while V_{oc} is only 79%.

Table 1.1 Comparisons of World Record and Ideal Solar Cell

	NREL-Wu Cells	Ideal*	Record/Ideal
V_{oc}(mV)	847	1070	79%
J_{sc} (mA/cm^2)	25.88	29.5	88%
FF(%)	75.5	89	85%
Eff(%)	16.5	29.2	57%

Note * “Ideal” calculated values from [5].

From the Table 1.1 it is clear that there is a big difference between V_{oc} and J_{sc}. There are three main factors that limit V_{oc}. The first factor, is the back barrier. V_{oc} is not significantly affected by the back barrier height when the back barrier is small. On the other hand, V_{oc} is significantly decreased for a large back barrier height. The second factor, is the low hole concentration since low back barrier height can only be achieved by using the correct back contact materials. It was seen the V_{oc} increases with the increasing of doping concentration. Typical hole concentration in p-CdTe is about ~ $1x10^{14}$ cm^{-3}. In this dissertation, ZnTe:Cu with graphite conducting paste with Cu evaporation is used as a dopant to increase the doping concentration for CdTe films. The third factor is the uniformity of the CdS layer, CdTe layer, and back contact. If the CdS film thickness is not uniform and there exists a low areal density of pinholes, a weak

diode between CdTe and CdS will form and reduce the V_{oc}. The non-uniformity could be due to localized surface state, the diffusion of impurities, or the contamination from the process. High resistive buffer layer (HRT) between TCO and CdS can reduce the required thickness of CdS and maintain high V_{oc}. Undoped SnO_2 and In_2O_3 have been used as buffer layers. Great care has to be taken prior to each deposition step to avoid contamination.

1.3 Purpose of Research

To improve the efficiency of n^+-CdS /p-CdTe solar cells by correlating processing with diode ideality, the basic techniques, I-V-T (current-voltage versus temperature), admittance spectroscopy (capacitance as a function of frequency and temperature), and deep level transient spectroscopy (DLTS) can be used to characterize the solar cells. These techniques were used to identify a set of extrinsic and intrinsic defects in CdTe and characterized their electrical and structural properties. These experiments contributed to the understanding of electrical properties of intrinsic/extrinsic defects in CdTe, the high/low p or n type doping of CdTe or high/low trap concentration by identifying the trap energy levels, which improves the solar cell efficiency and investigate the role of Cu metal impurity, part substitutional Cu_{Cd}^- and part interstitial Cu_i^+ in CdTe and dual behavior of defects or impurities as dopants and traps. I-V-T, AS and DLTS techniques are well defined for Si and III-V technologies with clearly defined intentional shallow dopants and deep level traps. But some new theoretical development is needed for II-VI CdTe, which does not have distinct shallow dopants and deep traps. Again, the aim is to improve the CdTe solar cell efficiency by proper performing and understanding electrical measurements (IV, AS, DLTS).

1.4 Thesis Organization

The thesis is divided into three major parts. The first part (Chapters 2, 3, 4) deals with the theory of deep level study of CdTe solar cells. Chapter 2 reviews the theory of defects in semiconductor devices, and their impact on solar cell performance. This chapter also examines the deep level study and establishes Shockley Read Hall (SRH) recombination theory showing that one of the limiting factor to the cell performance. Chapter 3 describes the standard solar cell characterization techniques including current - density voltage (J-V), quantum efficiency (QE), capacitance - voltage (C-V), admittance spectroscopy (AS), deep level transient spectroscopy (DLTS), thermally stimulated current(TSC), and thermally stimulated capacitance (TSCAP) as well as the fabrication process of CdTe solar cells in Apollo Research Center in New Jersey Institute of Technology (NJIT). The second part (Chapters 5, 6 and 7) discusses the experimental results. Chapter 5 describes the device characterization of variously processed cells by J-V and inconsistencies of SRH recombination equation. This chapter also describes the degradation of solar cells when they heated up during the measurement up to more than 100^0C. Chapter 6 examines and interprets the experimental results of variously processed cells by C-V. Chapter 7 describes a very simple technique based on temperature dependent capacitance spectroscopy (TDCS), which was used to identify the majority carrier trapping defects in thin film n^+-CdS/p-CdTe solar cells. This chapter presents the experimental results of cells processed with copper and explains how to find out the energy level and trap concentration of defects. Finally, the third part, Chapter 8, summarizes the whole work and proposes the future experiments.

CHAPTER 2

SOLAR CELL DEVICE PHYSICS

2.1 p-n Junction Diode

Materials can be classified into three groups based on their conductivity: (1) Conductors, whose resistivity is $<10^{-4}$ Ω-m (2) Insulators, whose resistivity is $>10^{12}$ Ω-m and (3) Semiconductors, whose resistivity is between conductors and insulators. Semiconductors can be classified into p type and n type based on their majority carriers. The most important characteristic of semiconductors is that their conductivity can be modified by adding impurities, which are called dopants. For p type materials, the majority carriers are holes. For n type materials, the majority carriers are electrons. When these two types of materials contact with each other, a p-n junction is formed. Because of the concentration gradient, the electrons diffuse into the p side and recombine with holes near the junction, while holes diffuse into the n side and recombine with electrons near the junction. The diffusion movement of these carriers forms the diffusion current. Adjacent to the p - n interface, there are no free carriers on both sides. This region is called the depletion region (also called space charge region (SCR)). The result of the diffusion leads to the buildup of positive charge on the n side and negative charge on the p side, and an internal electric field is established. This internal electric field tries to drift holes back to the p side and electrons back to the n side which led to the formation of drift current. Without any bias, the drift current is equal to the diffusion current, so the net current is zero. In equilibrium, the fermi energy level is the same in both the n- and p-bulk regions.

Figure 2.1 shows the band diagram of p-n junction in equilibrium. The magnitude of the band bending is the built- in potential V_{bi} is given by

$$V_{bi} = \frac{kT}{q} \ln\left[\frac{N_A N_D}{n_i^2}\right] \tag{2.1}$$

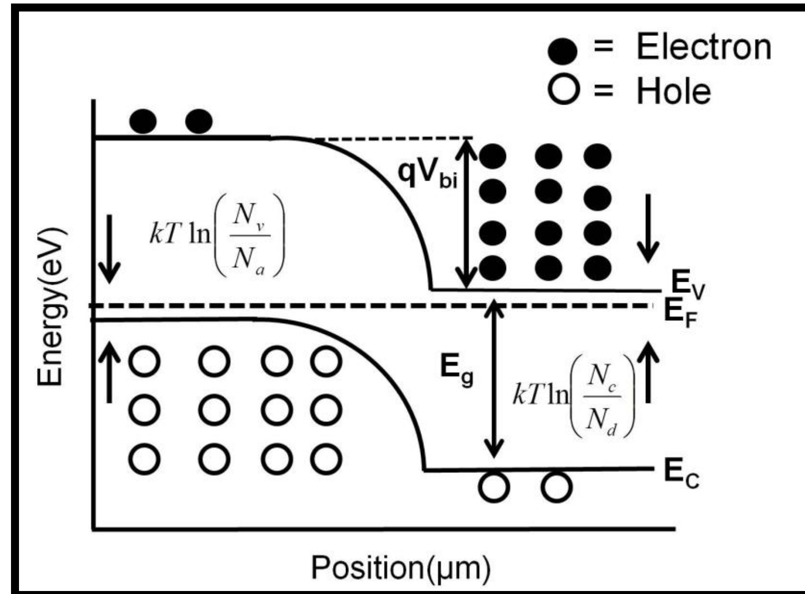


Figure 2.1 Energy Band Diagram of p-n junction in equilibrium.

When a dc bias V is applied across a p - n junction, the equilibrium state is broken by flowing a steady current, is given by the current-voltage relationship

$$J = J_0\left[\exp\left(\frac{qV}{AkT}\right) - 1\right] \tag{2.2}$$

where, A is the ideality factor, k is Boltzmann constant, T is absolute temperature, q is the electronic charge, and J_0 is reverse saturation current density. Since, A=1 for an ideal diode which does not have recombination in the depletion region. The p-n junction is forward biased when the positive terminal is connected to p side; otherwise, it is a reverse

bias. Figure 2.2 shows the band diagram of forward and reverse biased [33]. Note that V in Equation 2.2 is the same as V_a in Figure 2.2.

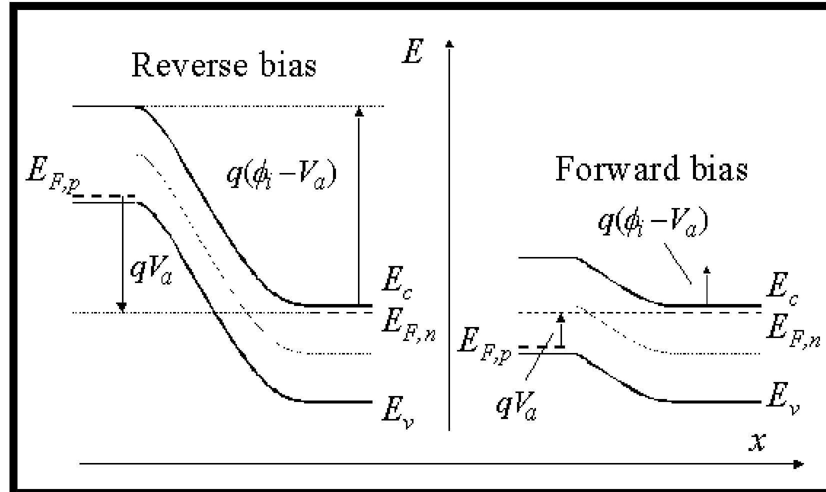


Figure 2.2 Energy Band Diagram of the forward (right) and reverse biased (left) p-n junction [33].

p-n junction can be homo junction or hetero junction, depending on the materials that form the junction. Homo-junctions are formed when p and n type layers of the same materials are in contact, and hetero-junctions are formed when different materials with different energy band gaps are in contact. For a homo-junction, the bands gaps are equal, hence no band offset where the layers meet. For a hetero-junction, conduction and valence band offsets, are formed. However, satisfactory conversion efficiency has been achieved in hetero junction n-CdS/p-CdTe devices, with the existence of the band offsets, and interfacial states due to lattice mismatch at the junction. The energy band diagram in Figure 2.2 is a homo-junction.

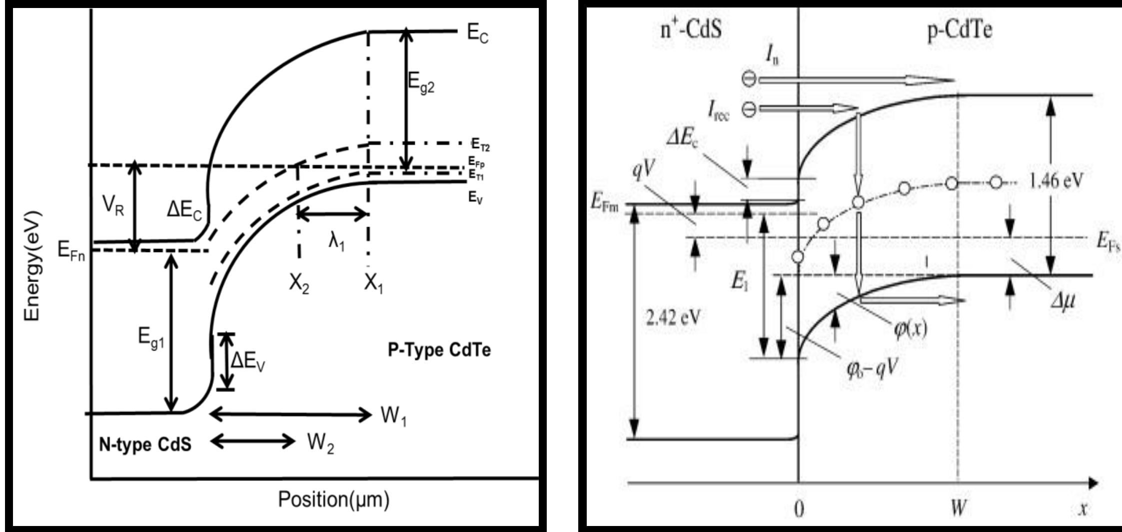


Figure 2.3 Band diagram for CdTe/CdS under reverse (left) /forward (right) bias [34] conditions.

The typical band structures of the CdS/CdTe hetero-juntion solar cells in reverse and forward and biased conditions are shown in Figure 2.3. In addition (see left figure) x_1 and x_2 are the locations in which trap level crosses the Fermi level under reverse bias (V_R), respectively. The transition distances λ_1 is defined as the point where the trap level E_T, crosses the fermi level E_F and is independent of reverse bias. James Sites simulated the effect of ΔE_c [35]. He found that even a small spike ΔE_c could limit the ability to increase V_{oc} with band gap. Photons with energy (< 3.5eV, 355nm) will pass through the SnO_2 layer. Part of photons (~ 30-60%, depending on the CdS thickness) with energy 2.43eV<E<3.5eV are absorbed by CdS. Most of the light with energy 1.45eV<E<2.43eV is absorbed by CdTe resulting in electron-hole pairs that contribute to light current as long as the electron-hole pairs are separated to the correct contact. But ehp generated in CdS are not easily collected and have “blue loss”. As a result, to reduce the blue loss the thickness of CdS layer should be minimized.

2.2 Photovoltaic Devices

2.2.1 Introduction and Operation of Solar Cell

In essence, a photovoltaic device consists of a p-n junction. When photons with energy greater than the band-gap are absorbed in the vicinity of this junction, the photo excited carriers are driven in opposite directions: electrons toward the n-type region, and holes toward the p- type region.

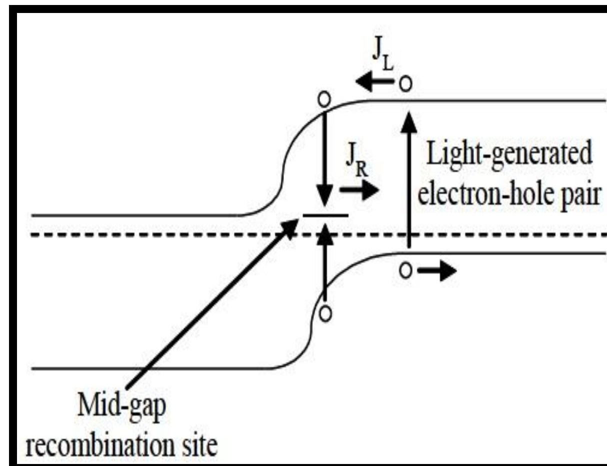


Figure 2.4 Schematic drawing of generation-recombination of electro-hole pair when light falls on a diode (p-n junction).

If no electrical connections exist between the n and p regions of the device, the potential difference set up by this charge separation biases the p-n junction in forward direction and reduces the built in field. At equilibrium, the majority carriers that overcome the lowered potential barrier ($\Phi_b - qV$) and recombine exactly cancel out the photo-generated current of the minority carriers. The potential difference between the p and n regions in this case can be measured and is known as the open circuit voltage (V_{oc}). If an external circuit with zero resistance connects the n and p regions, the photo

generated current (J_{sc}) can be measured. The total light generated current can be written as function of the spectral composition of the incident light as [36]

$$I_L = q\int \eta(\lambda)N_{ph}(\lambda)d\lambda \tag{2.3}$$

Where η (λ) is the thermal quantum efficiency, N_{ph} is the number of incident photons with wavelength between λ and λ + d λ.

If a finite resistance is inserted in the external circuit, the photo voltage builds up to a certain value while the photo current is reduced by an amount equal to the injection current corresponding to this voltage.

Summarizing the considerations above, the current density of a p-n junction diode depends on recombination of excess carriers in the space-charge region (scr) and quasi-neutral region (qnr) [37] and is given by

$$J = J_{sc} + J_{0,scr}[\exp[\frac{q(V-IR_s)}{A_1k_BT}]-1] + J_{0,qnr}[\exp[\frac{q(V-IR_s)}{A_2k_BT}]-1] + \frac{V-IR_s}{R_{sh}} \tag{2.4}$$

where J_{sc} is the short circuit current-density, A_1 (>2) and A_2 (=1) are the idealities factor, k_B is the Boltzmann factor, R_s is the series resistance, R_{sh} is the shunt resistance and T is the temperature. Equation (2.4) is further complicated by voltage-dependent J_0, R_s, R_{sh}, A_1, and A_2 and V is the output voltage.

Equation (2.4) can be reduced to the diode equation form when R_{sh} becomes very large and R_s is very small and

$$J = -J_{sc} + J_0\left[\exp\left(\frac{qV}{AkT}\right)-1\right] \tag{2.5}$$

where J_{sc} is the short circuit current density, or current that is produced when light excites electron-hole pairs close to the junction that can be collected (see Figure 2.4), A is now

the effective ideality factor which includes recombination-generation and collection efficiency where an ideal diode has A = 1 (1 < A < 2) and J_0 is an effective reverse saturation current density. Note that current density depends on the temperature.

Using the definitions that J_{sc} corresponds to V = 0 and V_{oc} corresponds to J = 0,

$$J_{sc} = J_0\left[\exp\left(\frac{qV_{oc}}{AkT}\right) - 1\right]$$

Or

$$V_{oc} = \frac{AkT}{q}\left[\ln\left(\frac{J_{sc}}{J_0} + 1\right)\right] \tag{2.6}$$

The diode current can be treated as tunneling through a potential barrier whose value Φ_B can be calculated from J_0 from the equation (37)

$$\phi_B = -\frac{kT}{q}\left[\ln\left(\frac{J_0}{A^* T^2}\right)\right] \tag{2.7}$$

where A* is the effective Richardson constant is given by

.

$$A^* = \frac{4\pi q m^* k^2}{h^3} = qN_V\sqrt{\left[\frac{k}{2\pi m^* T^3}\right]} \tag{2.8}$$

Here, h is Plank's constant, N_v is the effective density of states in the valence band, and m* is effective mass.

The electronic behavior of a solar cell can be represented by an equivalent circuit model, as shown in Figure 2.5. The photo generation mechanism is represented by the current generator, and the dark current is represented by the diode which is oriented opposite to the current generator.

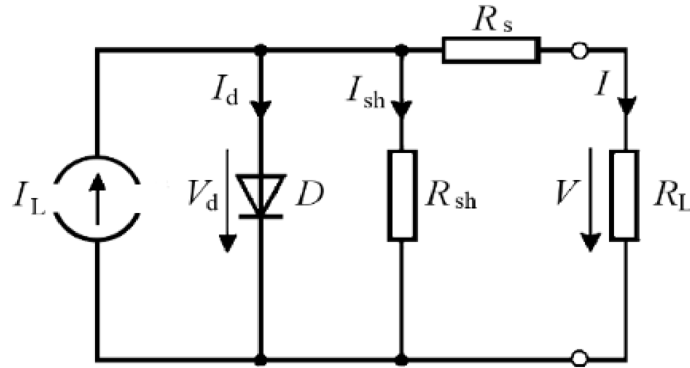


Figure 2.5 Equivalent circuit model of a solar cell [38].

2.2.2 Parameters Analysis of J-V Curve

The solar cell performance is determined by its parameters, i.e., short circuit current density (J_{sc}), open circuit voltage (V_{oc}), fill factor (FF) and efficiency (η) are shown in Figure 2.6. The J-V in forward bias > V_{oc}, are characterized by a higher R_s for the dark diode as compared to the illuminated diode. J_{max} is the current density at the voltage V_{max} corresponding to the maximum power (dP/dV = 0) point of the 1-sun illuminated solar cell. The fill factor FF = (J_{max} V_{max}) / ((J_{sc} V_{oc}) and the solar cell efficiency is η = (J_{max} V_{max}) / P_{light} where P_{light} = 100mWcm^{-2} is the light power area density for 1 sun illumination.

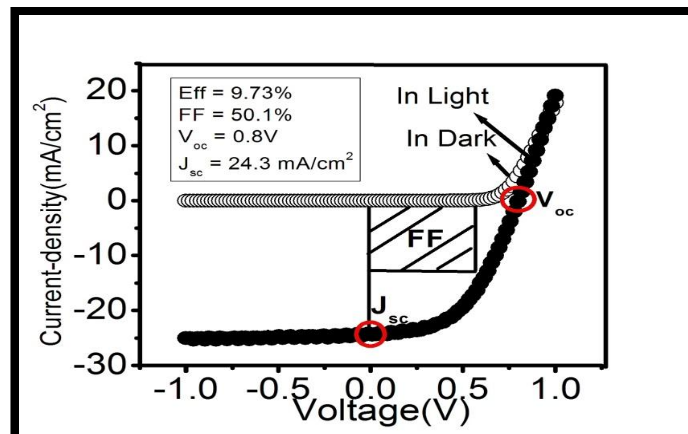


Figure 2.6 J-V curve of CdTe solar cell.

Also, ideality factor, series resistance and shunt resistance are important parameters for the solar cell performance which is shown in Figure 2.7. Note that the ideality factor, A, for the dark diode is greater than 2 for all solar cells but is closest to the SRH value of 2 in the case of cell [39]. R_s is calculated using the general formula $R_s = \left[\frac{d\{\ln(J)\}}{dV} \right]^{-1}_{J=0}$ at high forward bias (0.6 to 1.3 V) as shown in Figure 2.7 and R_{sh} is calculated by using $R_{sh} = \left[\frac{dJ}{dV} \right]^{-1}_{V=0}$ in reverse bias (-1 to -2V) from the J-V curve as shown in Figure 2.7.

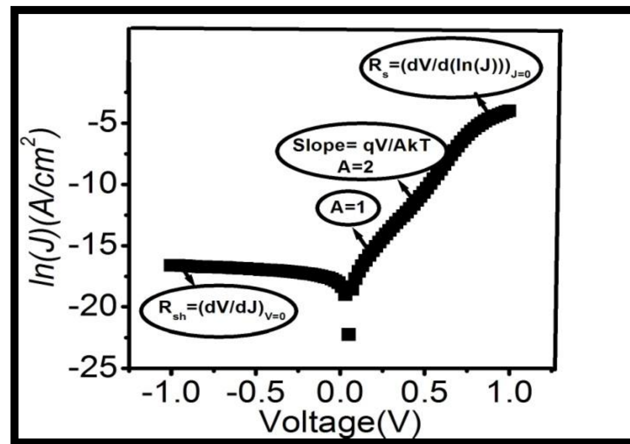


Figure 2.7 *ln*(J) - V curve of CdTe solar cell.

The series resistance, R_s, is composed of the bulk resistance of the semiconductor materials and that of the front and back contacts. Shunt resistance, R_{sh}, is caused by leakage across the p-n junction and around the edge of the cell. R_s will have a major effect at high currents but open circuit voltage is not affected by R_s, because no current flows at V_{oc}, while R_{sh} will affect the device at small voltages when the diode current is

very small, comparable with the shunt current. Both R_s and R_{sh} can reduce the fill factor by a predictable amount. High values of R_s and low value of R_{sh} can also reduce J_{sc} and V_{oc}, respectively. An ideal solar cell will have high shunt resistance ($R_{sh} = \infty$) and low series resistance (R_s =0).The effects of R_s and R_{sh} on J-V curve are shown in Figure 2.8 and 2.9.

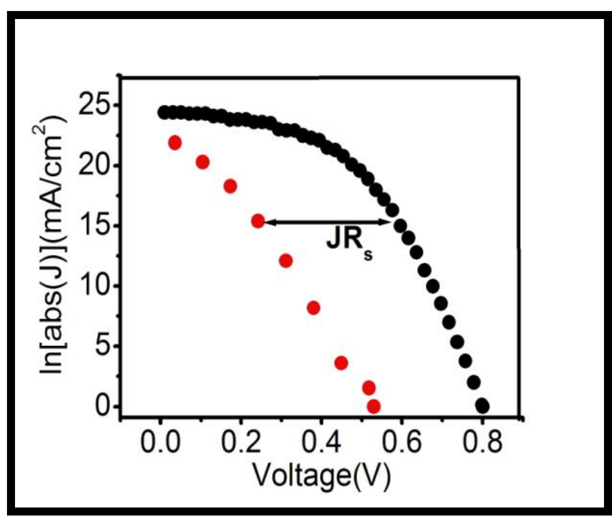


Figure 2.8 Effect of series resistances on the J-V curves.

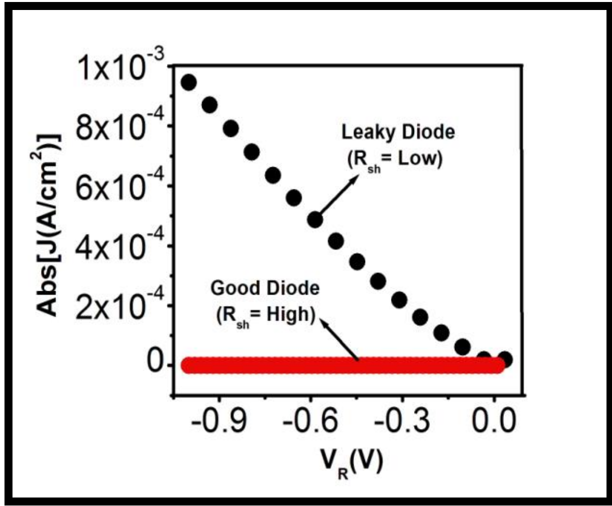


Figure 2.9 Effect of shunt resistances on the J-V curves.

2.3 Hetero-junction Solar Cells

2.3.1 Shockley Read Hall Recombination

Shockley-Read-Hall (SRH) model is used to describe the carrier generation and recombination current. Since the impurity is a generation- recombination (G-R) center and both the conduction and valence bands participate in recombination and generation. There are four basic processes (shown in Figure 2.10) involved in the carrier generation and recombination through the traps. If a trap is occupied by a hole, an electron may drop into the trap from the conduction band and recombine with the hole, or the trap may emit the hole to the valence band. If the trap is initially filled with an electron, the trapped electron may be emitted to the conduction band or a valence band hole may move into the trap and recombine with the trapped electron. There are two approaches to do this: either by taking the assumption with a constant minority carrier life time τ, or the input parameters are capture cross-sections, σ_e and σ_h, and the defect distribution N_d (E).

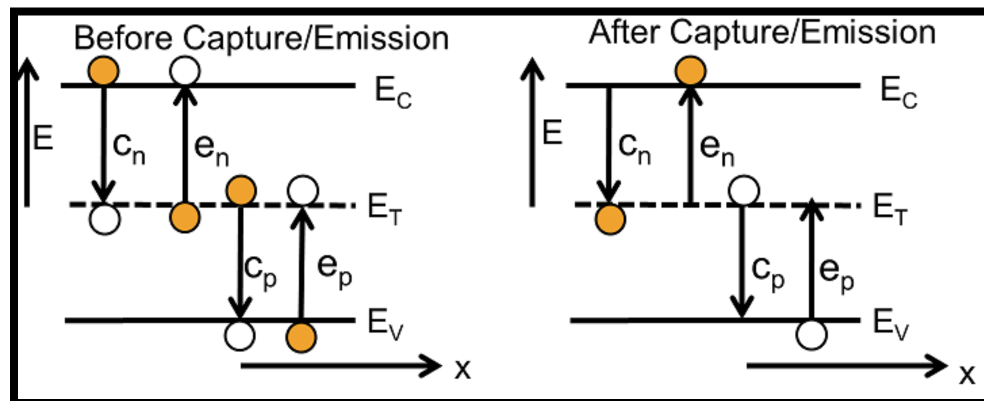


Figure 2.10 Electron energy band diagram for a semiconductor with carrier generation and recombination through traps, (a) electron capture, (b) electron emission, (c) hole capture, (d) hole emission.

In the SRH formalism, a defect state can change its charge state only by one elementary charge; therefore, one cans always the following distinction: A donor-like (acceptor-like) defect state is likely to donate (accept) an additional electron. The two possible charge states for donors (acceptors) are positive and neutral. It follows that the free electrons (holes) will be coulomb attracted to the ionized donor-like (acceptor-like) defect state, whereas holes (electrons) will have no strong interaction with the donor-like (acceptor–like) defects, giving very small hole into the ionized donor like defect, or the transition of an electron into a neutral donor like defect is rare. One problem with the SRH picture is that impurities in CdTe have various charge states with various defect energy levels. These multi-levels are not distinguished in the classical SRH formalism. In this work (Chapters 5-7), an impurity is present which acts as a trap or a G-R center strongly depends on cross-section of temperature dependence impurity. Under steady–state condition, a single energy level recombination center is characterized by three numbers: the capture cross-section for electrons, the capture cross section for holes, and the energy involved in these transitions.

Thin film CdTe solar cells contain high concentration of defects, and impurities, and they distort the regular electron density pattern in the crystal structure. This creates the localized electronic states or traps within the band gap which interact with the free electrons in the conduction band by capturing and emitting electrons, and with the free holes in the valence band by capturing and emitting holes as illustrated in Figure 2.10.

2.4 Chapter Summary

This chapter summarizes the parameters that describe a solar cell are extracted from the current density–voltage (J-V) curve. It has been observed that the measured J-V characteristics deviate from the ideal case of the diffusion model. The existence of a finite series resistance R_s reduces the voltage drop across the diode to $V\text{-}IR_s$. The correlation between the ideality (i.e., how close the diode is to the Shockley ideal diode of the electrical J-V characteristics and solar cell efficiency is presented. Since, the recombination is the reverse process where electrons and holes from the conduction, respectively, valence band recombine and are annihilated. The generation and recombination centers in the space charge region of a junction diode limits the current density for the observed J-V characteristics. It clearly shows that, a detailed understanding of recombination theory for the defect transition states.

CHAPTER 3

REVIEW OF EXISTING WORK FOR CDS/CDTE SOLAR CELLS

3.1 Impact of Fabrication on CdTe Solar Cells

CdS/CdTe solar cells are usually fabricated in a superstrate structure where the light is incident through the glass substrate. Device with efficiency of 16.5% was achieved using a CTO/ZTO layer [40]. The CdS/CdTe alloy properties were studied in detail by various groups including the one at the University of Toledo [41- 44].

A transparent conducting oxide layer is deposited on top of the glass substrate and serves as the front electrode. Glass panels coated with SnO_2 are commercially available [45]. Other materials considered for use as a front contact by themselves or in combination with SnO_2 include Cd_2SnO_4 [46] and Zn_2SnO_4 [47]. Routine high efficiency CdS/CdTe solar cells have been most successfully fabricated using SnO_2 as TCO [43].

The CdS layer has a band gap of 2.4eV at room temperature [48] and the measured resistivity range is of the order of 10ohmcm to 1Mohm by post deposition treatments [49, 50]. A typical film thickness of 80-100nm is deposited on the TCO layer by various methods, including sputtering [51], chemical bath deposition [52] and aerosol [53]. The CdS layer thickness has to be optimized to make it as thin as possible to sustain the hetero-junction. This is required to minimize the photocurrent losses due to absorption in CdS. Poor collection efficiency is possible due to a low built in electric field [54]. The inter-diffusion at CdS/CdTe interface is enhanced by the post-deposition $CdCl_2$ heat treatment [55]. Typical donor concentrations of 10^{16}-10^{17} /cm^3 were reported. The doping concentration of this layer can be altered by acceptor type impurity and

defect compensation. Currently, a lot of effort is put into fabricating solar- cell devices with this window layer as thin as possible [56].

The primary purpose of an absorber layer is to efficiently collect the light energy incident on it and convert it to electricity. CdTe was found to be an ideal junction partner for CdS with an electron affinity mismatch of only 0.3eV and has a thickness 2-10μm, depending on the deposition method. Structurally, CdTe is known to form columnar grains of > 1 μm in size [57]. High efficient solar cells annealed around 400^0C in the presence of $CdCl_2$ vapors [24, 58] were reported. Furthermore, $CdCl_2$ treatment [59] helps in recrystallization, increase in grain size, increase in hetero-junction barrier height, and a decrease in the dark reverse saturation current and substantial increase in the open circuit voltage. The presence of cadmium vacancies as native defects is what makes it p type. It has a high absorption coefficient of 10^4 - 10^5 cm^{-1} which means only 1-2μm thick CdTe is enough to absorb all the incident light above its band gap of 1.44eV.

The formation of a stable, low resistance contact to p-type CdTe is a major challenge due to high work function of CdTe and the inability to obtain low resistivity (high level doping) CdTe. Within the framework of the Schottky theory [60], a good contact to a p- type semiconductor is obtained when a metal with a work function higher than the hole affinity of the semiconductor is used. The work function of CdTe is ~5.78eV [61]. The work function of commonly used metals range from 4.2 - 5.6eV. Thus no metal exists that can make a barrier free or at least quasi-ohmic contact to CdTe. The energy band diagram of ohmic and non–ohmic metal and p-type semiconductor contacts is shown in Figure 3.1.

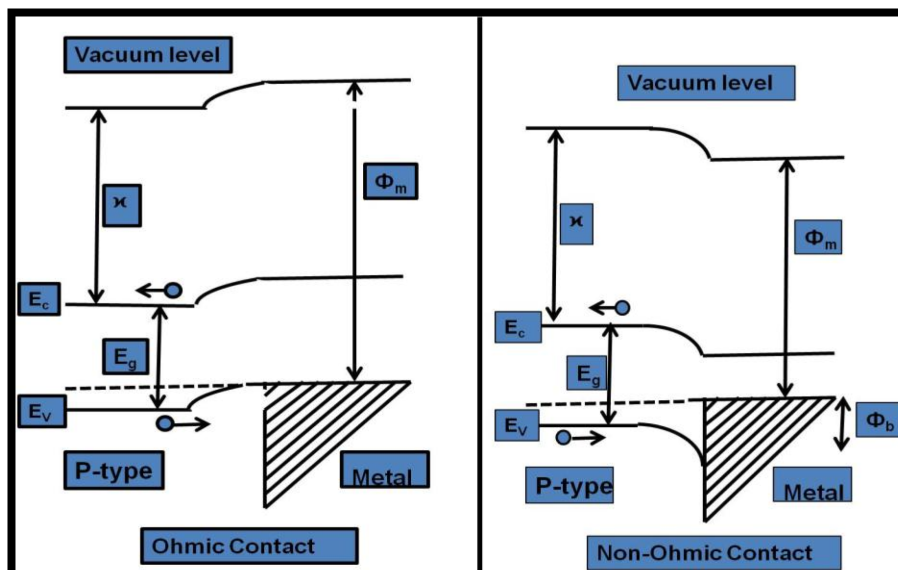


Figure 3.1 Energy Band Diagram of Ohmic and non Ohmic Metal/p-type semiconductor contacts.

Most metal contacts to CdTe are rectifying. Doping polycrystalline CdTe at the contacting interface is problematic due to the existing potential barrier. The barrier height is controlled by impurity/dangling bond states and carrier density in the bulk adjacent to the barriers. Compensation of the dopant by oppositely charged grain boundary states also exists. The effective carrier density and effective mobility are reduced due to the presence of grain boundaries. This barrier height has to be minimized to reduce the surface recombination velocity and improve device efficiency. The most common and successful approach to obtain ohmic or pseudo-ohmic contacts to CdTe has been to modify the CdTe surface to make it Te rich or Cd deficient (p^+). This promotes tunneling carrier transport between the semiconductor and metal. Graphite paste doped with HgTe:Cu has been previously used to obtain high efficiencies [62]. An anneal step at temperature around 150^0C is generally used in the back- contact formation process for the diffusion and activation of the dopant [63]. Formation of p-type Cu_2Te and $Hg_{1-x}Cd_xTe$

interlayer help tunneling of holes across the contact. Details of other contacting procedures and contacts can be found in elsewhere [64].

3.2 Factors Affecting Stability

It is well known that routine fabrication of high efficiency CdTe/CdS devices is possible with the help of Cu doped back contacts. Some researchers had demonstrated solar cells with Cu free back contacts with high efficiencies [65, 66], however, their long term stability has not yet been established. Preliminary stability studies have shown that the decay of Cu acceptor states and the formation of non-radiative recombination centers can have a significant impact on the stability of CdTe solar cell devices that use Cu for the formation of a back contact. Grecu et al. [67] showed that Cu doped CdTe samples exhibit a significant "aging" behavior, attributable to the instability of Cu acceptor states as verified by Hall measurements. The aging appears to be reversible by annealing at 150 - 200^0C tempertaure. Grecu et al. [67] also explained the efficiency degradation of some CdTe solar- cell devices which use Cu for the formation of a back contact. The samples annealed with Cu in a Cd or Te overpressure had a dramatic influence of the Cu-related aging behavior. He observed that the samples annealed with Cu in a Cd overpressure show a substantially amplified PL degradation when compared with similar samples annealed in a Te overpressure. The most suspected cause of cell instability is the diffusion of Cu from the back contact into the junction and the CdS region. Cu is known to be a fast diffuser in polycrystalline CdTe.

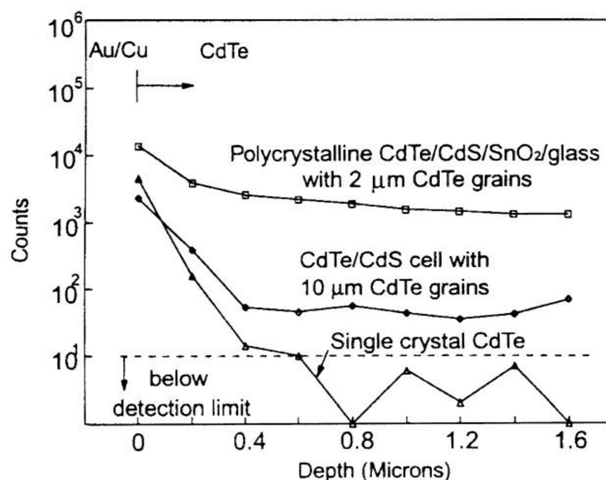


Figure 3.2 Comparison of Cu SIMS profiles in thin films of polycrystalline CdTe for samples with different degrees of crystallinity [65].

Grain Boundary (GB) diffusion is the most likely mechanism of transport of Cu into the cell junction. Because Cu^{+} and Cd^{2+} ions are similar in size, Cu^{+} was thought to substitute readily for Cd^{2+} in CdTe. However, the lattice defects are slow diffusers compared to the defects at GB. With the doping of Cu in the entire CdTe layer, Cu has been detected at the CdS/CdTe interface. Cu can form recombination centers and shunt pathways limiting the lifetime of the cell.

3.3 Impact of Defects on Device Performance

Imperfections in a crystal lattice are called defects. Individual atomic or complex-related defects are called point defects. Defects are usually classified as shallow, non-shallow, or intermediate. Shallow defects are defined as defects within a few kT of the band edge, such that a hole [electron] from an acceptor [donor] has a high probability of being thermally excited into the valence [conduction] band at typical device operating temperatures. Deep defects, sometimes called mid-gap defects, are located near the

middle of the band gap and typically act as recombination sites for electrons and holes. Intermediate defects are any defect with ionization energy between that for shallow and deep levels.

3.3.1 Shallow Defects

When discussing shallow defects, one must look at both donors and acceptors. The relative effects of a donor or acceptor will depend on whether the semiconductor is n- or p-type. For simplicity, consider the case of a p-type semiconductor. An increase in the number of shallow acceptors will increase the number of holes in the valence band and increase the carrier concentration. If all other factors are held constant, this will decrease J_o (the reverse saturation current of the diode). From Equations 2.4 and 2.6, a decrease in J_o will increase V_{oc} but leave J_{sc} unchanged, and the efficiency of the device will increase. Conversely, a shallow donor level added to p-type material will increase J_o, which lowers V_{oc}, and reduces device efficiency.

3.3.2 Non-Shallow Defects

Deep (mid-gap) defects in the junction region act as recombination centers for holes and electrons (see Figure 2.4). This causes a recombination current, J_R, in the direction opposite to the photocurrent, and this recombination current is added into the ideal expression with small series resistance and large shunt resistance for total current given in Equation 2.4 becomes

$$J = -J_{sc} + J_{01}\left[\exp\left(\frac{qV}{A_1 k_B T}\right) - 1\right] + J_{02}\left[\exp\left(\frac{qV}{A_2 k_B T}\right) - 1\right] \tag{3.1}$$

Note that $J_{02} = qn_iW/2\tau$, so in theory J_{sc} is not affected by the recombination current

(in reality, however, there may be a change in the depletion width, which would affect J_{sc}). Here we also consider A_1 =1 and A_2 =2.

The V_{oc} will be slightly affected by the presence of a recombination current. Solving Equation (3.1) when J=0,

$$0 = -J_{sc} + J_{01}\left[\exp\left(\frac{qV_{oc}}{k_B T}\right) - 1\right] + J_{02}\left[\exp\left(\frac{qV_{oc}}{2k_B T}\right) - 1\right]$$

$$0 = -J_{sc} - J_{01} - J_{02} + J_{01}\left[\exp\left(\frac{qV_{oc}}{k_B T}\right)\right] + J_{02}\left[\exp\left(\frac{qV_{oc}}{2k_B T}\right)\right]$$

$$0 = -J_{sc} - J_{01} - J_{02} + \exp\left(\frac{qV_{oc}}{k_B T}\right)\left[J_{01} + J_{02}\exp\left(-\frac{qV_{oc}}{2k_B T}\right)\right]$$

$$V_{oc} = \frac{k_B T}{q}\ln\left[\frac{J_{sc} + J_{01} + J_{02}}{J_{01} + J_{02}\exp\left(-\frac{qV_{oc}}{2k_B T}\right)}\right] \tag{3.2}$$

The current-voltage parameter that will be most affected by the recombination current arising from deep (mid-gap) defect states is the FF. The shape of the bend in the J-V curve (Figure 1.6) is influenced by the diode ideality factor, A. For A values close to 1, the bend of the curve is fairly “square,” producing large values for J_{max} and V_{max}. However, larger values of A will cause the curve to be less “square” and the values for J_{max} and V_{max} will be smaller. The A factor is governed by the types of recombination occurring in the device. As the amount of recombination via mid-gap states increases, the value for A will also increases, which will cause losses in the fill-factor.

3.3.3 Intermediate Defects

Defects with activation energies intermediate to the shallow and deep defects have some probability that they will ionize to the band, adding to the V_{oc} and J_{sc}, and some probability that they will act as recombination centers, decreasing V_{oc}. Although both ionization and recombination can occur for intermediate defects, the relative probability of the two mechanisms will depend on the ionization energy of the defect. A defect with energy closer to that of a shallow defect (smaller ionization energy) will be more likely to ionize than to act as a recombination center. Conversely, a defect with energy closer to mid-gap (larger ionization energy) is more likely to act as a recombination center than to ionize to the band, and would tend to lower FF and V_{oc}.

Defects in a solar cell can greatly influence its efficiency, and hence identification of such defects is important. Identifying a defect is a key step to potentially increasing the device efficiency. This defect must also be related to solar-cell performance and linked to the process that introduced this defect. If the defect proves to be detrimental to device operation, then it may be necessary to change the process to eliminate or mitigate that defect. Although it is nontrivial to change the processing techniques to remove a defect without harming performance through some other mechanism, it is important to take that first step and identify the defects introduced by that process.

The localized intrinsic/impurity defect states in a semiconductor can be classified as follows: 1) Vacancies – missing atom from the lattice; 2) Interstitials – extra atom between normal lattice sites; and 3) Substitutionals – an atom occupying another element's lattice site.

Vacancies and self-interstitials are called intrinsic defects while substitutional and external interstitial atoms are called extrinsic defects. Schottky defects involve vacancies like an anion or cation or both missing from the lattice (ex: Cd or Te vacancy in CdTe). Frenkel defects are formed when an atom migrates from its lattice site to an interstitial position (ex: Cadmium vacancy and cadmium interstitial). Point defects are the main dopants in thin film semiconductors. Complex defects formed by combination of atomic defects also exist such as [Cu_{Cd}^{-} – Cl_{Te}^{+}], [V_{Cd}^{2-} - $2Cl_{Te}^{+}$], [Cu_{Cd}^{-} - Cu_{i}^{+}] etc.

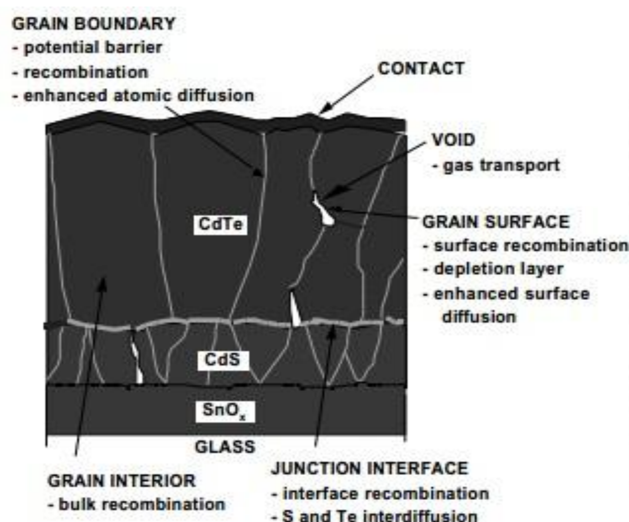


Figure 3.3 CdS/CdTe cell structure showing polycrystallinity and related issues [66].

Figure 3.3 shows the defect sites in the hetero-junction CdS/ CdTe structure. CdTe is a called a defect semiconductor because its native defects are responsible for its electrical properties, i.e., donor-like cadmium interstitial, Cd_{i}^{+} (donates an electron to the lattice) for its n-type conductivity, and acceptor-like cadmium vacancies, V_{Cd}^{-}(accepts an electron from the lattice) account for its p-type conductivity. Various native defects possible in CdTe are cadmium vacancy, $V_{Cd}^{-/2-}$, cadmium interstitial, $Cd_{i}^{+/2+}$, tellurium vacancy, $V_{Te}^{+/2+}$, tellurium interstitial, $Te_{i}^{-/2-}$. These can also form complexes with

residual impurities or dopants. The existence of metastable states [68] have been found changing from shallow to deep traps or vice versa with or without change in charge [69]. Illumination and thermal excitation could cause these metastable transitions.

The defects of interest for this study are intrinsic singly and doubly ionized cadmium vacancies, extrinsic copper sustitutionals, interstitials and complexes as well as chlorine related defects. The density of these defects found in CdTe/CdS polycrystalline structures has been found to exceed or equal intrinsic layer doping concentrations of CdS or CdTe.

Copper and Chlorine are found to be useful elements in CdTe to increase in efficiency. Cu is used during the back contact process and Cl is used during the $CdCl_2$ high temperature anneals. Copper is also known to occupy cadmium vacancies V_{Cd}^-, acting as an ionized acceptor like defect. As an interstitial, Cu can exist as a neutral atom or as an ionized donor Cu_i^+. Similarly Cl can exist as a neutral atom or a more stable Cl_i^- as an acceptor. Cl also substitutes sulfur vacancies forming donor like defects.

The research groups [65] have shown large accumulation of Cu and Cl at the junction interface and in CdS. This is possibly due to higher GB and lattice defects at the metallurgical interface and the fact that CdS grains are much smaller compared to CdTe resulting in a larger grain boundary area. The ionic dopant species like Cu and Cl and their complexes accumulate at these interfaces and GBs due to GB diffusion. This discussion underscores the complex defect mechanisms involved in the polycrystalline CdS/CdTe structure. The Chapters 5, 6 and 7 discuss in briefly about the Cu related defects and the degradation mechanisms.

3.4 Current Literature Survey Related to Deep Level Defects of CdTe Solar Cells

With the success of fabricating high efficiency thin film solar cells, the CdTe community has focused on understanding the deep level defect study. This section will summarize the defect analysis of CdTe Solar cells with different techniques. A review of existing literature on the defects in CdTe/CdS solar cells is discussed below.

Seymour et al. [10] studied the electronic states controlling the performance of CdTe Solar Cells. He tested J-V Characterization of different processed cells (1) with Cu and $CdCl_2$ treatment; (2) without Cu and $CdCl_2$ treatment; as expected, with Cu back contact and with $CdCl_2$ treatment cells had the highest efficiency as compared to without Cu and $CdCl_2$ treatment. Seymour et al. [10] from J-V-T measurements also observed that as the cells initially cools, the increasing Schottky barrier rollover effect can be seen that shows the exponential thermal dependency of the reverse diode saturation current. As the cells continue to cool, the Schottky barrier increase further. As the cells cools further J_{sc} decreases rapidly indicating that the free carriers are freezing out and the cell is losing its ability to collect the photocurrent.

Niemegeers et al. [70] explained a simple analytical theory to measure the roll over and cross over behavior of the IV characteristics of thin film CdTe solar cell to see the effect of the Au/CdTe back contact. It involves a classical description of the CdS/CdTe junction and the CdTe/back contact structure and is extended with a new description of minority carrier current in the CdTe contact region. This extension is crucial in describing the light dependence of the forward IV curves, and hence crosses over. The same model also explains the measured CV curves. He also showed that

analysis of the capacitance measurement can yield additional information about the doping density of CdTe in the vicinity of the contact.

Demtsu et al. [71] clearly showed that even though small amounts of Cu (5 nm) improve performance by increasing V_{oc} and improving back barrier properties, Cu can also have a detrimental effect on current collection. Increased Cu resulted in a strong but systematic decrease in minority carrier lifetime caused by an increase in deep-level trap density. This voltage-dependent collection effectively reduced J_{sc} and contributed to reduced fill-factors and overall reduced performance. The multiple effects of Cu revealed by choosing different concentration of Cu can describe by using the J–V characteristics. From 0 to 5 nm, there is a significant decrease in the current collection because of the abrupt decrease in lifetime by traps and the reduced depletion width caused by increase in carrier concentration. This same increase in the carrier concentration resulted in increased V_{oc}. From 5 nm to 20 nm the changes were small. At 100 nm (excess Cu), FF was reduced dramatically and a current-limiting effect (roll-over) started to appear. It is possible that this is due to the formation of a rectifying contact at the back-contact layer that impedes hole transport, but this requires further systematic study.

Seymour et al. [10] and Li et al. [27, 72, and 73] had studied the defects states of CdTe Solar Cells by AS. AS studies of unstressed and stressed CdTe solar cells showed that the total concentration of different types of traps can exceed the doping level of CdTe [27]. The characteristic times of traps vary widely along with their energy level positions. High concentrations of slow (deep) traps can be attributed to grain boundary states. Trap bands found with energies $E_v + 0.35eV$ are attributed to Cu_{Cd}^- substitutionals. The energy level of these traps is a band with a width of about 0.05eV.

Chin et al. [12] pointed out the dual role of doping and trapping of semiconductor defect levels and their ramification to thin film photo-voltaics. He explained that the semiconductor localized intrinsic/impurity defect levels dual role for carrier doping and trapping have been treated differently and inconsistently. He proposed that instead of ionization or activation energy, transition Gibbs free energy level should be used for the dual roles of doping- trapping.

Chin et al. [74] explained that very low levels of Cu can reduce the already low conductivity of the CdTe thin film, while increasing the Cu concentration can increase both conductivity and minority carrier lifetime. Specifically, a contacting temperature to 250°C - 300° C can produce high efficiency devices that demonstrate long minority carrier lifetimes. Increase the contacting temperature beyond ~300°C can yield a CdTe thin film that becomes insulating, or even to n-type. Such a complicated and puzzling effect on the property and quality of the CdTe thin film turning from a poor p-type, to a poorer p-type, to a better p-type, to insulating, and then to n-type is all due to different levels of Cu involvement in the CdTe thin film.

Chin et al. [75] presented a generic approximate graphical method for determining the equilibrium fermi level and majority carrier density of a semiconductor with multiple donors and multiple acceptors compensating each other. The graphical method will help to guide the design, adjustment, and improvement of the multiply doped semiconductors. By using the graphical method, we may be able to derive the known equations, such as the non-shallow dopant's partial ionization, in a simpler and visually insightful way.

Komin et al. [6] had studied the defects present in CdTe/CdS solar cells by DLTS technique. Isett et al. [76] studied about the deep level impurities and current collection in

CdTe solar cell by using DLTS. He found that heat treatment at 373K changes the energy distribution of the deep levels. He also found that heat treatment with illumination produces an energy level distribution greatly different from the produced by heat treatment without illumination. Lourenco et al. [77] observed a deep level with a continuously varying activation energy and capture cross section. Degradation was maximum in the presence of copper in the back contact. Stress Induced degradation at elevated temperatures and bias, both in dark and under illumination was reported [78-79] also recovery of degraded devices was reported without stress conditions [80].

Zoth et al. [81] used low temperature C-V measurements to analyze the change in carrier concentration in the space charge region of Schottky contacts to p- type Cu doped CdTe. The change in the carrier concentration is consistent with the formation and dislocation of defect complexes. The acceptor and donor states could not be identified in this method but Cu_{Cd}^{-} and Cu_i^{++} respectively were viewed as the most likely candidates. Authors [82] are recognized that there is a significant correlation between the loss of solar cell efficiency and CdTe doping density as determined by C-V measurements.

Chou et al. [83] studied the dual role of copper; it helps to form an ohmic contact as well as diffuses all the way to the junction and form recombination centers and shunt paths. Grain boundaries [83] were suggested to the main conduits for the Cu diffusion towards the junction. Kaydanov et al. [84] suggests that most of the Cu diffusion takes place during the back contact formation, especially during the anneal step. It was suggested [85] that devices with and without insufficient Cu are more susceptible to the presence of residual impurities, which could be more difficult to control. In CdTe, Cu can exist interstially as a positive ion (Cu_i^{+}) giving rise to a shallow donor state, can

participate in various complexes of the type Cu_i^+ - V_{cd}^- [86, 87] or can substitute for a Cd atom, to form a deep acceptor state [87, 88].

Numerous software packages were developed to simulate the electronic behavior of solar cells (ex AMPS (Analysis of Microelectronics and Photonic Structures) was written by S. Fonah and coworkers of Pennsylvania State University [89], SCAPS [90] is written and maintained at the University of Gent. Burgelman et al. [91] focused all simulated characteristics: J (V, T), C (V, T), C (f, T) and QE (λ) by using numerical simulation software SCAPS developed in lab [91, 92]. For numerical simulation to study of deep defects, they started from a very basic parameter set [93, 94].The simulated parameters listed in table 1[95] leads to design prescription for selected parameters are agreement in measurements.

3.5 Chapter Summary

This chapter summarizes the role of defects and related stability issues of CdTe solar cells. Due to stability problem caused by back contact, a lot of attention brought comes into the account. There are discrepancies in the literature about the activation energies of the various reported deep and shallow traps along with the capture cross section, type of the traps (holes or electrons) and the assignments of shallow and deep traps. It is very difficult to draw a clear line to distinguish between shallow and deep levels by literature survey. In the next chapters, some of the possible ways to detect the defects will be discussed.

CHAPTER 4

DEVICE FABRICATION AND ELECTRICAL CHARACTERIZATION TECHNIQUES

4.1 Introduction

This chapter reviews the properties of all the materials in a CdS/CdTe heterojunction solar cells which are relevant to device performance and stability. A generic CdS/CdTe superstrate device structure is shown in Figure 1.1. All thin film CdS/CdTe solar cells studied in this dissertation were fabricated at Apollo CdTe Solar Cell Research Center, NJIT. The device structure (Figure 1.1) used in this research consists of a front contact layer (SnO_2), n-type layer (CdS), p-type layer (CdTe) and a back contact layer (Cu evaporation + graphite paste doped with anneal of ZnTe:Cu at 160^0C/280^0C) on soda lime glass substrate.

4.2 Fabrication of PV Devices

4.2.1 Deposition of Thin Films at National Renewable Energy Lab (NREL)

The device structure of all layers of the CdTe solar cell as fabricated in NREL for the reproducibility study is shown in reference [62].The substrate were made on 76 × 76 × 1.1 mm Corning 7059 glass. The fluorine doped tin oxide layer is the transparent contact that provides current collection from the front of the device. The CdS layer with thickness of 800 - 1000 Å was grown by chemical-bath deposition (CBD) with the constituents (i.e. cadmium acetate ($CdAc_2$)(8ml), ammonium acetate (NH_4Ac)(4.6ml), ammonia (NH_4OH)(15ml) and thiourea ($CS(NH_3)_2$)(8ml)), which are introduced into 550

ml of DI water in the reactor. The CdS layer is called as n type layer. The CdS layer was removed from the back of the substrate by wiping with a swab dipped in concentrated HCl and the CdTe (8 - 10 μm in thickness) was deposited by close-spaced sublimation (CSS) at T_s = 600 °C using flashlamp heated graphite susceptors and in 0.02 Torr He/O_2. The CdTe layer is called as the absorber layer for the incident light. After CdTe deposition, a $CdCl_2$ treatment was performed. The Kapton tape (3M 5413 polymide film) was used to mask a portion of the CdTe surface for the chosen area. The cells were then etched in 88: 1: 35 phosphoric acid: nitric-acid: DI-water (NP etch) to provide a clean, Te-rich surface. HgTe:Cu-doped graphite paste is then brushed on the cell as the back contact. Since, the HgTe: Cu-doped graphite layer produces an ohmic contact to the CdTe (because the work function of HgTe: Cu is higher than work function of semiconductor). The paste is made by stirring 4 g HgTe:Cu (which is about 2 atomic% Cu) powder into 10 g graphite paste (Acheson Electrodag 114). Then, the back contact was annealed by placing the device in a tube furnace at 280^0C with a 100 sccm He flow for 30 min. A thin layer of silver paste (Acheson Electrodag 6S-33C) was then applied to the back contact. Since, the silver layer decreased the lateral resistivity of the back contact. The device was then placed in an oven at 100^0C for 1 h to cure the silver paste.

4.2.2 Deposition of Thin Films at Apollo CdTe Solar Energy Research Center (NJIT)

Cadmium telluride solar cells were fabricated in the superstrate configuration with the structure: glass/TCO/n^+-CdS/p-CdTe/graphite/metal back contact. A set of samples of CdTe solar cells, with different areas respectively, were made on 4” x 4” glass substrates at the Apollo CdTe Solar Cell Research Center at NJIT. Commercially-available soda-

lime glass coated with SnO_2: F/HRT was used as a substrate for the depositions. The CdS (~ 80 nm in thickness) was deposited by chemical bath deposition (CBD) at 88 °C using cadmium chloride, thiourea, ammonium acetate and ammonia, and then annealed at 400 °C. The CdTe (6-10 μm in thickness) was deposited by close-spaced sublimation (CSS) at T_s = 600 °C using ohmically heated graphite susceptors and in 10 - 15 Torr He/O_2 [96, 97]. The CdTe was then soaked in $CdCl_2$/methanol at 80 °C, followed by a furnace anneal under controlled conditions (380 °C, He/O_2, 300 Torr) in order to improve CdTe structure and minority carrier lifetime. The $CdCl_2$ treatment also appears to promote intermixing of the CdS into the CdTe [98], and the presence of S in the CdTe may serve to passivate defects. To form the back contact, a nitric-phosphoric (NP) acid etch was used to remove the surface oxide. For cells**,** 15 nm of Cu was directly evaporated on the sample for 20 min followed by application of micron size Cu particles (2 atomic% Cu) were mixed with ZnTe powder that was then mixed into carbon conductive paste followed by annealing in Helium at 160 °C for 30 minutes and then application of a metallic rear electrode. The overall process was similar to that described by Rose et al. [62] with the exception of the heating method of the graphite susceptors. The ohmically heated NJIT process inherently gives a thicker CdTe film because of its slower rise time to the desired temperature of 600°C.

4.3 Electrical Characterization Techniques

The fabricated solar cells were characterized by dark and light J-V measurements, C-V measurements, spectral response measurements, DLTS, AS, TSC, and TSCAP measurements.

4.3.1 Current Density versus Voltage (J-V)

In operation of solar cell, there are essentially two independent inputs which can adjust output current: applied voltage across the device and incident light intensity, both of which are usually implemented into the classical Equation [39]

$$J(\lambda, P_{\lambda}, V) = \{J_{0,SRH}(e^{qV/AkT} - 1) + J_L(\lambda, P_{\lambda})\} f(V) \quad (4.1)$$

where, the output current equals addition of two terms: $J_{0,SRH}$ (N_t, E_t, σ_n, σ_p, $V^{1/2}$, T) is reverse bias diode current by SRH recombination and light current f(V) is collection transfer function (holes from CdTe to CdS contact and electrons CdS to CdTe contact).

However, classical Equation fails to interpret experimental data of polycrystalline thin film n^+-CdS/p-CdTe solar cells where (1) forward current responds to optical power input and (2) light current depends on applied voltage bias and light power. Based on these observations, it is proposed that both reverse current can be affected by N_t, E_t, σ_n, σ_p, $V^{1/2}$, T variables and photocurrent can be affected by two independent variables: wavelength and power of light injection P(λ), the Equation (4.1) can be written in more explicit way.

$$J(\lambda, P_{\lambda}, V) = \{J_R(N_t, E_t, \sigma_n, \sigma_p, V^{1/2}, T) + J_L(\lambda, P_{\lambda})\} f(V) \quad (4.2)$$

For quality crystalline solar cells, the model successfully describes the current-voltage characteristic very well. This model can apply when p-n junction (c-Si for example) has (1) very high concentration of shallow dopants, leading to much smaller depletion region compared to neutral region, (2) trapping/defects density in Si is extremely low, (3) high carriers mobility in well grown crystal structure.

The above three assumptions for n^+-CdS/p-CdTe are not valid. (1) CdTe is low-p doped and the depletion width on CdTe side can even reach to a few microns. (2) There

exist several non-shallow defects within band gap of CdTe. There are reported in calculation [99] and experiment [100]. (3) Mobility in polycrystalline CdTe could be much lower than that crystalline CdTe.

An important limitation of the J-V-T technique is that several defects can degrade CdTe performance, and proper separation can be a challenge using the activation energy from Arrhenius plot of *ln* I vs.1/ T.

4.3.2 Quantum Efficiency

Quantum Efficiency measures the solar cell current intensity as a function of light wavelength. The solar cell is exposed to a narrow wavelength light source and the short circuit or zero voltage current produced is measured as the wavelength is varied across the solar spectrum. The measured current intensity indicates the extent of EHP formation minus recombination.

A methodology for QE analysis of thin film solar cells is shown in Figures 4.1 and 4.2 [101, 102].

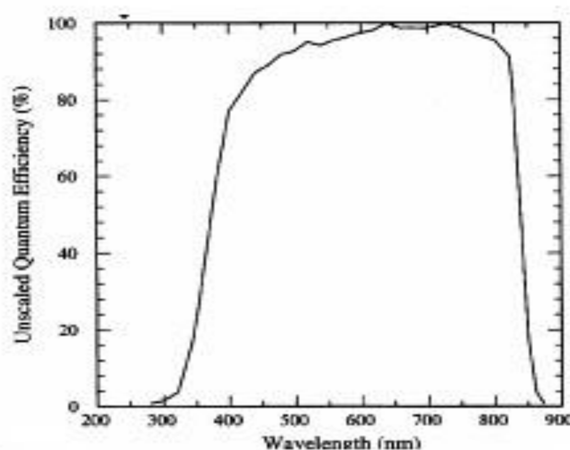


Figure 4.1 EQE curve for 16.5% efficient CdS/CdTe polycrystalline thin-film solar cells [103].

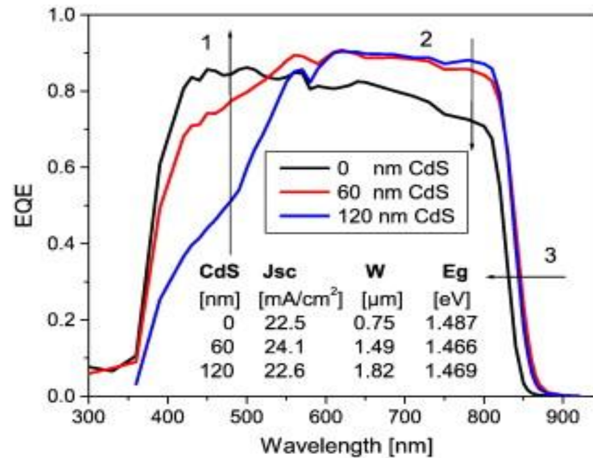


Figure 4.2 EQE curve of CdS Solar Cell with different thickness [104].

QE measurements are valuable to characterize the photocurrent, and can also be used to determine the individual losses responsible for reducing the measured J_{sc} from its ideal value. In general, the short-circuit current J_{sc} equals the light-current J_L and can be calculated by integrating the QE spectrum multiplied by the photon current J_{solar} being used, generally that of the standard AM1.5 spectrum. An ideal CdTe cell with band gap 1.45 eV and QE of 100% will yield a photocurrent of 30.5 mA/cm^2. Current losses can be optical, due to front reflection and absorption in the window, TCO and glass layers, or electronic losses due to recombination losses in the absorber.

4.3.3 Capacitance-Voltage Profiling

The capacitance of a solar cell can yield information about extraneous states within the band gap, and it can often give a credible profile of the carrier density within the absorber [103]. The capacitance magnitude is relatively small, corresponding to a small carrier density and a large depletion width [104].

CdTe solar cells are one sided junctions because of high doping for n-type CdS (~10^{17}cm^{-3}) relative to the p-type CdTe (~10^{14}cm^{-3}). Because of its relatively high doping level and narrow width, the CdS contribution to the depletion width is negligible.

The depletion region of the p–n junction solar cell can be approximated as a parallel plate capacitor, and the junction capacitance is given by

$$C = \varepsilon \frac{A}{W} \tag{4.3}$$

where, ε is the permittivity, A is the area, and W is the depletion width.

For a step junction the depletion width W given by

$$W = \sqrt{\left[\frac{2\varepsilon}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)(V_{bi} - V)\right]} \tag{4.4}$$

where q is the fundamental charge, V_{bi} is the built-in voltage, N_A is the acceptor concentration in the n-layer, and N_D is the donor concentration in the p-layer. From the above two Equations, the capacitance per unit area A, can be expressed as

$$\frac{A}{C} = \sqrt{\frac{2}{q\varepsilon}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)(V_{bi} - V)} \tag{4.5}$$

For a n^+–p junction, $N_D >> N_A$ thus

$$\frac{A}{C} = \sqrt{\frac{2}{q\varepsilon N_A}(V_{bi} - V)} \tag{4.6}$$

As the dc bias is changed, the charge density at the edge of the depletion width is changed, and in the absence of compensation N_A will correspond to the density of free carriers, p. From the slope of A^2/C^2 as a function of the applied voltage, the hole density $p = N_A$ can be estimated.

But there are some limitations concerning C-V measurements. The first limitation is to obtain the real doping concentration, it would be necessary to separate the impurity concentration from the real doping concentration. This could be done by determining the single capacitance values and relative C-V curve by an additional characterization method such as Hall Effect measurement method. The second limitation of CdTe solar cells fabricated by a variety of the techniques illustrated in Figure 14.6 of Chapter 14 [105] have shown hole densities between 1×10^{14} and $8 \times 10^{14}/cm^3$ as determined by the capacitance technique. The direct impact of the low hole density is that the fermi level is 250 to 350 meV from the valence-band maximum, and hence limits the junction barrier, and therefore V_{oc}. The speculation is that a bigger, and probably related, problem is that the low carrier densities are likely to be symptomatic of the excessive recombination states, which may be an impediment to higher efficiency cells. It suggests that the theoretical efficiency cells approach remain a challenge for the CdTe cells made to date.

4.3.4 Deep Level Transient Spectroscopy

The DLTS technique was pioneered by D. V. Lang [106]. It is sensitive and can detect trap concentration about 10^{-4} times or less the concentration of shallow impurities in semiconductors. It allows obtaining parameters from either minority (positive peak in the spectral result) or majority carrier traps (negative peak). DLTS is a powerful method to obtain defect properties of a material such as: trap energy level, carrier capture and emission rates, trap density, spatial and distribution of defects based on either capacitance, current or charge transient response of the device for a pulsed electrical or optical signal. DLTS observing the change in depth of SCR, due to emission of trapped charges, by measuring the capacitance transient.

In the simplest of the DLTS techniques, the reverse bias on a Schottky or p-n junction diode is pulsed to zero bias. At quiescent reverse bias V_R, all the deep levels above fermi level (E_F) are empty. During the pulse period, deep levels capture majority carriers from the conduction band. After the pulse the carriers trapped at the deep levels empty slowly.

The principle of capacitance transient measurements, due to majority and minority carrier emission, for a n^+p diode is shown in Figure 4.3. The relaxation to equilibrium deep level occupancy is monitored as a capacitance transient at constant voltage. The time constant of the transient increases when temperature decreases.

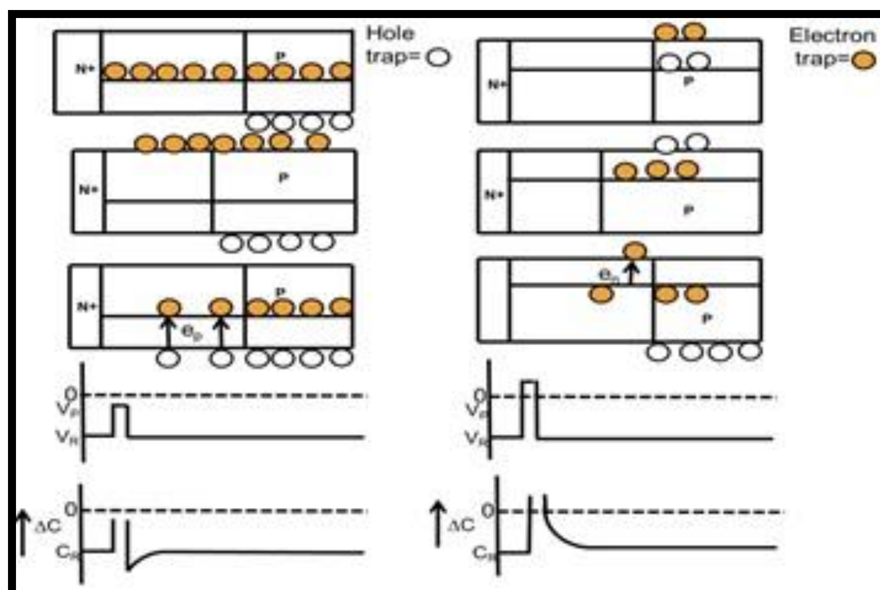


Figure 4.3 Principle of majority (left) and minority (right) carrier capacitance transient with pulse sequence and occupation of deep levels and width of space charge layer at various moments.

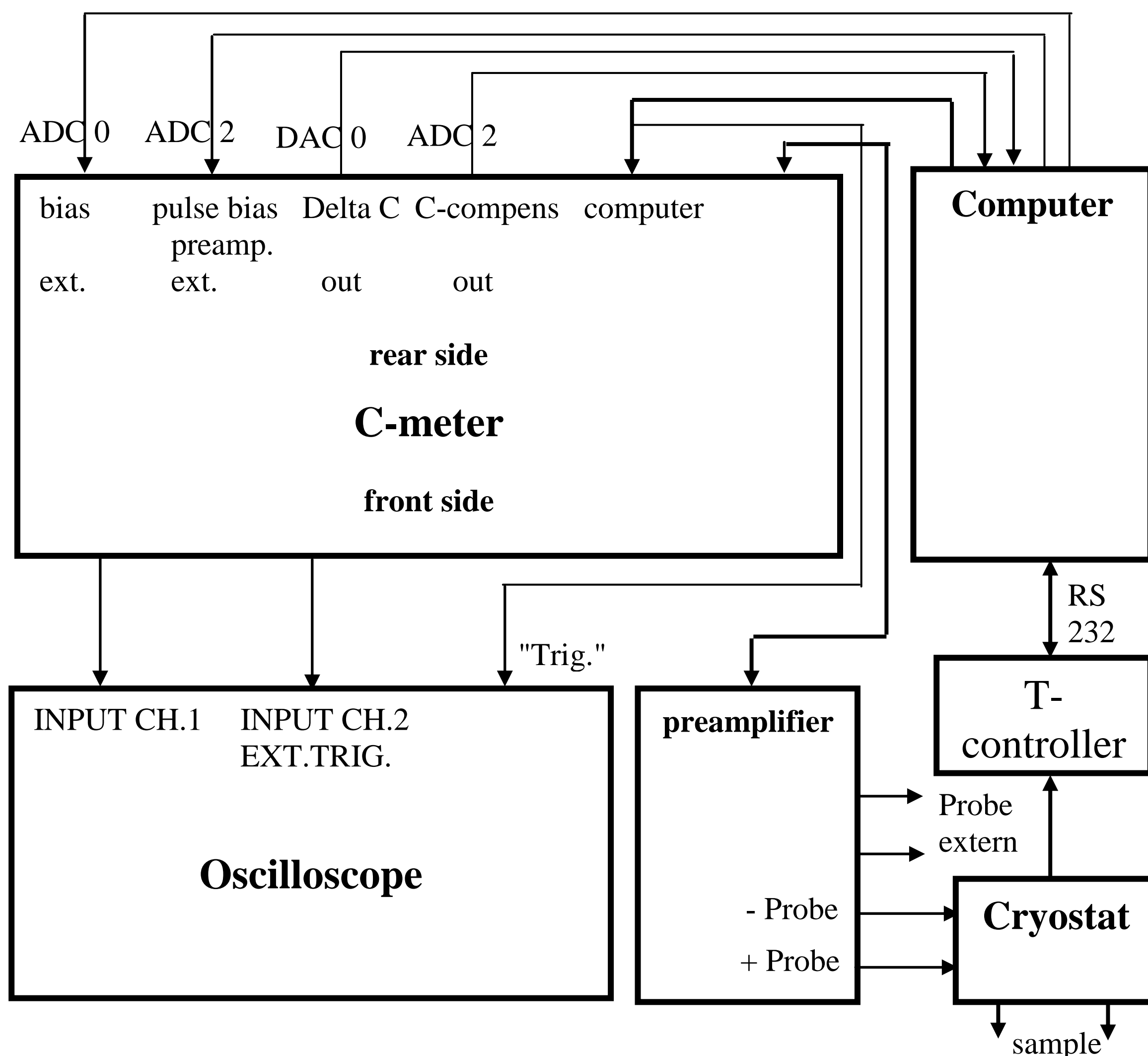


Figure 4.4 Wiring scheme of the DLTS setup[107].

A deep level transient spectroscopy system, based on the capacitance transient is shown in Figure 4.4. The deep level occupancy is periodically altered by repeatedly pulse a reverse biased diode to zero bias to study the majority carrier traps. The resulting decaying signal is sampled at two times t_1 and t_2. The sampling is done by using boxcar averager and gated averager.

As the sample temperature is varied the DLTS signal is

$$S_m = C(t_1) - C(t_2) \qquad (4.7)$$

Or $$S_m = [\exp(-t_1/\tau_m) - \exp(-t_2/\tau_m)][C(0) - C(\infty)]$$

This goes through a maximum as shown in Figure 4.6

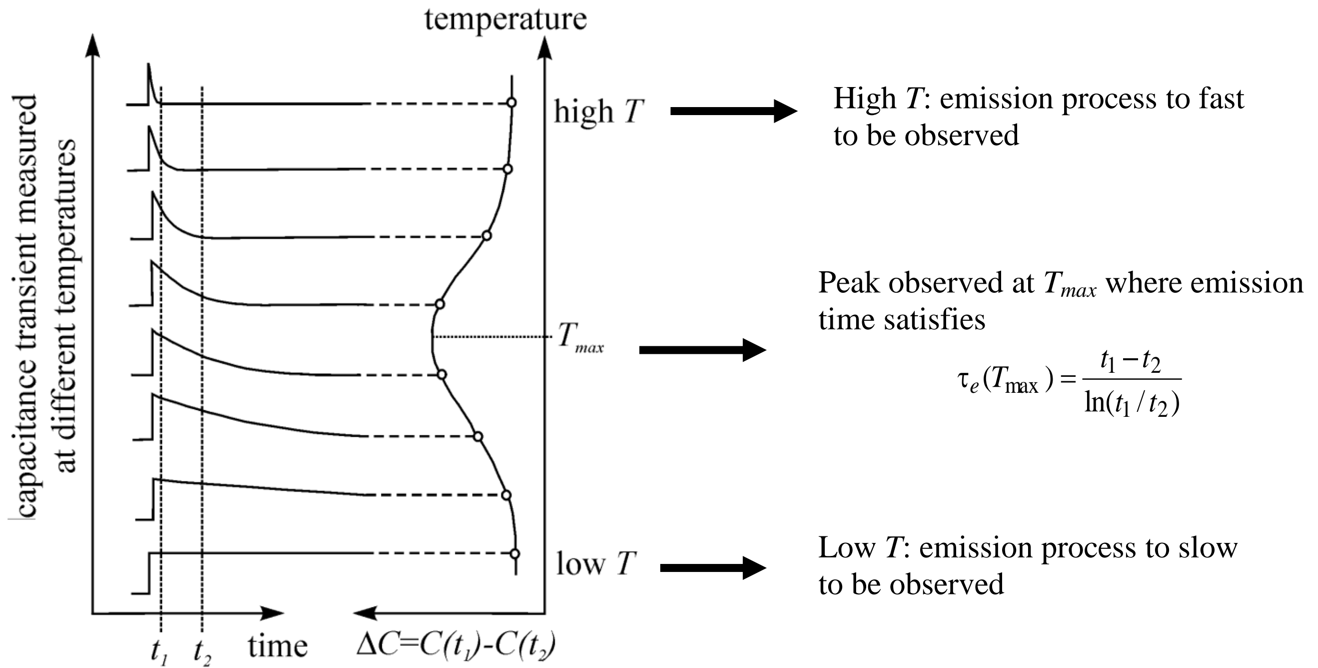


Figure 4.5 Principles of DLTS [106].

The time constant of the capacitance transient τ_m is related to t_1 and t_2 as

$$\tau_e(T_{\max}) = \frac{t_1 - t_2}{\ln(t_1/t_2)} \qquad (4.8)$$

The activation energy of the traps can be measured by using equation can be written as

$$\ln\left(\frac{e_p}{T^2}\right) = \ln\left[\frac{\sigma_\infty v_p N_v}{T^2}\right] + \left(\frac{-\left(E_t - E_V + E_a\right)}{1000k_b}\right)\frac{1000}{T} \qquad (4.9)$$

By taking the slope of the line in the plot in $ln(e_p/T^2)$ vs. 1000/T.

The varaition of the deep level trap density is measured by monitoring the DLTS peak height as a function of pulse amplitude, with constant reverse bias. The capture cross-section can be estimated by monitoring the variation of the peak height as a function of the filling pulse width.

There are some limitations of DLTS: High leakage currents could influence the DLTS peak amplitude in that it will have rate window dependence. This dependence could be attributed to competition between carrier capture due to leakage current and thermal emission, often leading to errors in the trap energy extracted from the Arrhenius plot. Interfacial layers can affect DLTS results in two ways: by introducing peaks that are associated with interface states, and by modifying the overall capacitance transient which is observed with thermal emission in the bulk of the semiconductor. Also, an instrument, where the temperature of the sample has to be precisely controlled, ~ 0.1K is desirable. Very shallow trap levels could not be instrumentation, where the temperature of the sample has to be precisely controlled, ~ 0.1K is desirable. Very shallow trap levels could not be measured due to freeze-out of free charge carriers. Detection of very deep trap levels might be difficult since the change of the occupation might be very small. Minority carrier trap levels could only be detected by forward biasing if $c_p >> c_n$. To perform DLTS scans one needs to change the temperature of the sample, it is important to take into account the temperature dependence of the band gap.

4.3.5 Admittance Spectroscopy

Admittance Spectroscopy (AS) [108] has been an effective tool for the study of the electrical properties of defects in semiconductors. In thin film solar cell research, the use of this technique is particularly extensive [109] to distinguish between beneficial doping

and harmful trap. AS measures the junction capacitance as a function of frequency ω, and temperature T. By measuring the admittance $Y(\omega,T) = i\omega C(\omega,T) + G(\omega,T)$ (which has an imaginary capacitance term and a real conductance term), of the applied alternating voltage, a sinusoidal voltage of small amplitude is applied to the sample and the resulting current is detected phase sensitively. During measurement, a frequency sweep is performed. The frequency dependent admittance Y (ω, T) is obtained by division of the resulting current by the excitation voltage. The periodic potential applied induces an alternating shift of the Fermi level E_F or quasi-Fermi level of the majority carriers E_{Fn} or E_{Fp}.

The admittance of the heterostructure is a superposition of the free carrier capacitance across the width of the space charge region (SCR) and the contribution from the charging and discharging of deeper defect levels within the SCR of the junction. The rectifying junction capacitance is given by the SCR capacitance [110].

$$C_d = \frac{A\varepsilon}{W} = \sqrt{\frac{q\varepsilon N_A}{2V_{bi}}} \tag{4.11}$$

where, ε, is the semiconductor's dielectric permittivity, W is the space charge region width, N_a is the acceptor concentration in p-type absorber, and V_{bi} is the built-in voltage.

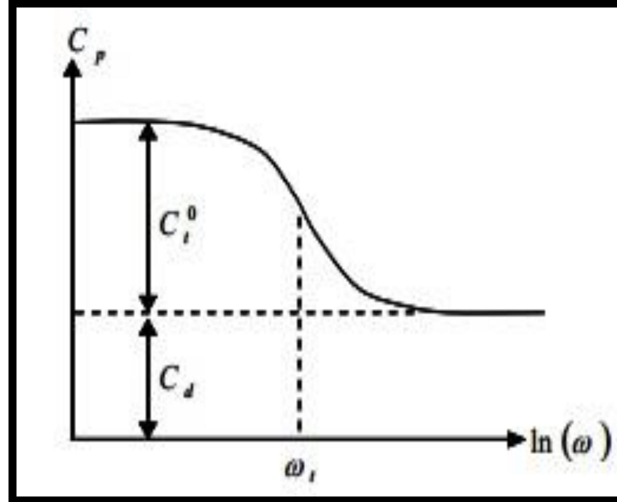


Figure 4.6 Illustration of capacitance C_p as a function of AC frequency signal *ln*(ω). C_d is the depletion width contribution while C_t^0 is the trap contribution to the capacitance [111].

If deeper carrier traps are present, the band bending in the SCR causes the Fermi level E_F to cross the trap level E_t at some distance from the interface, at the crossing point x_t shown in Figure (2.3). The oscillating voltage with the frequency ω causes the electric charge accumulated by traps to oscillate in the vicinity of x_t. The trapped electric charge follows the applied voltage oscillations and contributes to the total capacitance only if their frequency does not exceed the characteristic trap frequency ω_t. Therefore, in the case of low frequencies $\omega_{lf} << \omega_t$, the trap related capacitance C_t is equal to C_{lf} , where C_{lf} is the low frequency capacitance. In high frequency ($\omega_{hf} >> \omega_t$) measurements the junction capacitance C_d is determined by C_{hf}, where C_{hf} is the high frequency capacitance. AS involves measuring the junction capacitance as a function of frequency and temp is well known. Accordingly, in the case of a single majority carrier trap level the total junction capacitance can be described by the Equation [112].

$$C_p(\omega) = C_d + \frac{C_t^0}{1+\left(\frac{\omega}{\omega_t}\right)^2} \quad (4.12)$$

$$\omega_t = \frac{1}{\tau} = c_p + e_p + c_n + e_n \tag{4.13}$$

$$\text{Where} \begin{cases} c_n = \sigma_n v_n n = \alpha\beta n \\ c_p = \sigma_p v_p p = \alpha\beta^{-1} p \end{cases} \quad \text{and} \quad \begin{cases} e_n = \sigma_n v_n n^* = \alpha\beta n^* \\ e_p = \sigma_p v_p p^* = \alpha\beta^{-1} p^* \end{cases} \tag{4.14}$$

$$\text{Note that} \begin{cases} n^* = n_i \exp\left(\frac{G_t - E_i}{kT}\right) = N_C \exp\left(\frac{G_t - E_C}{kT}\right) = n \exp\left(\frac{G_t - E_{Fn}}{kT}\right) \\ p^* = n_i \exp\left(\frac{E_i - G_t}{kT}\right) = N_V \exp\left(\frac{E_V - G_t}{kT}\right) = p \exp\left(\frac{E_{Fp} - G_t}{kT}\right) \end{cases} \tag{4.15}$$

Where, τ, is the characteristic trapping time that depends on the trap density N_t, the acceptor concentration N_a and on the SCR-width w. The inflection frequency ω_t can be obtained from the analysis of the first derivative of the capacitance, dC/dω that should demonstrate a peak at the frequency ω_t. The temperature dependence of the inflection frequency ω_t ($\omega_t = 1/\tau$ [113]) is described by the Equation

$$\omega_t(T) = 2e_t(T) = 2N_{c,v} v_{th} \sigma_{n,p} \exp\left(\frac{-(E_t + E_\sigma)}{kT}\right) = 2\xi_0 T^2 \exp\left(\frac{-(E_t + E_\sigma)}{kT}\right) \tag{4.16}$$

where e_t is the emission rate, $N_{c,v}$ is the effective density of states in the conduction and valence band, υ_{th} is the thermal velocity of the minority carriers at the interface, $\sigma_{n,p}$ is the capture cross-section for electrons and holes, E_A=E_t-E_v is the activation energy of the defect level E_t with respect to the valence band edge E_v in p-type absorber and ξ_0 covers all the temperature independent parameters. The activation energy of a defect level E_A can be obtained from the temperature dependence of the capacitance spectra, i.e., from the Arrhenius plot of the quantity *ln*(ω_t/T^2) versus 1000/T.

AS has some limitations. It is however clear that interpretation of measurements from AS is a difficult task and that AS alone does not allow reaching reliable or useful conclusions. The complex nature of most practical PV devices means that one or more of

these conditions may often be violated in the admittance measurements. Also it is limited to majority carriers.

4.3.6 Thermally Stimuated Current (TSC)

Thermally Stimulated Current (TSC) is the simple technique to study the deep states (energy level and concentration) in semiconductors [114-116]. In this method, traps are filled by the excitation of the semiconductor at a low enough temperature such that upon ceasing the illumination the trapped carriers cannot be freed by the thermal energy available at that temperature. The temperature is then raised at a constant rate. The liberated carriers contribute, in an applied field, to an excess current until they recombine with carriers of the opposite type or join the equilibrium carrier distribution. This excess current, measured as a function of temperature during heating, is called a TSC curve. In previous years, this technique has been extended to amorphous semiconductors. Several experiments have been carried out in hydrogenated amorphous silicon (a-Si:H) [117-119]. A TSC curve for a single trap level has one maximum whose position depends on the trap depth, the capture cross-section of the trap and the heating rate. By varying the heating rate, the trap depth and the capture cross section can be determined [120, 121]. If a discrete distribution of traps is present, the TSC curve may consist of several peaks, each originating from distinct trap energy.

TSC for a material with a single trap level in the fast as well as the slow re-trapping case is given by a general Equation [122]

$$I(T) = -A\exp\left[\frac{E_t}{kT} + \frac{B}{\beta}\int_{T_0}^{T}\exp\left(\frac{-E_t}{kT}\right)dT\right] \tag{4.17}$$

where, A and B are constants whose dependence on the various trapping parameters is given below.

For fast retrapping

$$A = Q\, n_{t0} N_c\, \mu\, E\, C/ N_t \qquad \text{and} \qquad B = N_c/\tau\, N_t \tag{4.18}$$

For slow retrapping

$$A = q\, n_{t0}\, \nu\, \tau\, \mu\, E\, C \qquad \text{and} \qquad B = \nu \tag{4.19}$$

where, E_t is the trap depth, β is the heating rate, T_0 is the initial temperature and k is the Boltzmann constant. At a time t after the heating has started, the temperature $T = T_0 + \beta t$, q is the electronic charge, n_{t0} is the number of electrons in traps at t=0, N_t is the total number of traps, μ is the mobility of electrons in the conduction band, ν is the escape frequency, τ is the lifetime of the electrons, E is the electric field, C is the cross-sectional area of the sample and N_c is the effective density of states in the conduction band

The condition of maxima in TSC (i.e., a peak in TSC) can be obtained by using the condition

$$\left.\frac{dI(T)}{dT}\right|_{T=T_m} = 0 \tag{4.20}$$

Therefore it is concluded that

$$\exp\left(\frac{-E_t}{kT_m}\right) = \frac{B}{\beta}\frac{kT_m^2}{E_t} \tag{4.21}$$

Equation (4.21) predicts that the TSC maxima temperature (T_m) will shift towards higher temperature with the increase in β. Moreover, a plot of *ln* (T_m^2/β) versus $1/T_m$ should be a

straight line whose slope is related to E_t. Also, for temperatures close to T_m, the Equation (4.17) can be approximated as [116]

$$I(T_m) = -A\exp\left[\frac{E_t}{kT} - 1\right] \tag{4.22}$$

From equation (4.22), if $E_t / kT_m >> 1$, a plot of ln $I(T_m)$ versus $1/T_m$ is a straight line for different heating rates whose slope is related to $E_{t.}$

Figure 4.7 shows emission of trapped charges in a TSC curve. TSC observing release of trapped charge directly, by measuring the current due to emission of trapped carriers In this experiment, the traps are filled with the sample at low temperature then, upon heating, the trapped carriers are released to the appreciate band and there is an increase in free carrier density and hence in the conductivity. The amount of trapped charge is finite, being determined by the number of traps, and as the temperature is increased further all the trapped carriers are eventually falls, so there is a peak in a plot of the current change as a function of temperature. The temperature at which this peak occurs is related to the energy level of the trap and the area under the peak is related to the trap concentration. The TSC change is measured as a change in current flowing between two contacts on the surface of sample with a fixed voltage applied across the sample.

The current change depends upon the carrier recombination processes which tend to restore the free carrier density in the band to its equilibrium value; consequently the magnitude of the current change depends upon the effective carrier life time, as well as the carrier mobility and the applied electric field. By contrast the electric field in the thin depletion region of a barrier is much greater than the field along the sample in current

experiment, and is sufficiently great that carriers emitted to the band are swept out of the depletion region before they can recombine. In this case the current change is due to an increase in the number of electrons entering the external circuit and does not depend on the carrier lifetime, nor explicitly upon the electric field because carrier emission is the rate limiting step.

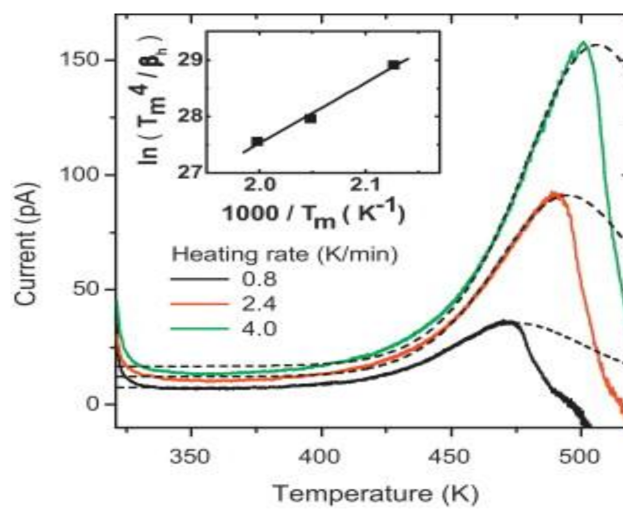


Figure 4.7 The injection of charges and emission of trapped charges in a TSC curve [123].

The limitation of this technique is that TSC experiments cannot be operated at higher temperatures. Because of increase in background current this makes it difficult to detect small current changes due to emission from deep states near the middle of the gap.

4.3.7. Thermally Stimulated Capacitance (TSCAP)

To overcome the problem related to the TSC experiment, the depletion capacitance rather than the current can be measured. As the free carriers are released from the traps the space charge density increases and the depletion region contracts producing a step change in capacitance as a function of temperature. The temperature at which this occurs is related to the energy level of the trap, and the height of the step depends on the trap

concentration. These are termed thermally stimulated capacitance (TSCAP) experiments. In this method, the initial charge states of the traps are set to fill the traps with majority carriers at reverse bias in the dark and at low temperature. The junction temperature is then increased so that the trapped carriers in the depletion layer are thermally excited out, giving junction capacitance changes with increasing temperature. The temperatures of maximum (majority carrier traps) dC/dT, T_m (maximum temperature in the peak) give estimates of the thermal activation energies of the majority trap energy levels. This method demonstrates that the capacitance change due to filling of the majority-carrier traps in the depletion region can be employed to detect levels.

4.4 Chapter Summary

This chapter summarizes the fabrication process of CdTe solar cells. All electrical characterization techniques used to find out the all possible defects in CdTe are also discussed.

CHAPTER 5

DEVICE CHARACTERIZATION OF CdTe SOLAR CELLS BY USING J-V TECHINQUE

5.1 Device Analysis of NJIT Cells in Dark and Illumination

The J-V characteristics were analyzed in the dark and under 1 sun illumination (~ 100mW/cm^{-2} for filtered xenon lamp) from the side through the “transparent” glass substrate. Using a Keithley 236 Source Meter temperature dependent J-V measurements were carried out. The data were collected by using labview program, which can calculate open circuit voltage (V_{oc}), short circuit current density J_{sc}, fill factor (FF) and efficiency η respectively. The solar simulator was calibrated before taking the J-V measurements. From dark J-V curve, all cell parameters i.e., R_s, R_{sh}, J_0 and A can be determined and from light J-V curve, other parameters i.e., V_{oc}, J_{sc}, FF can be found. Sample temperature was varied from 25ºC to 100ºC on a micromanipulator probe station.

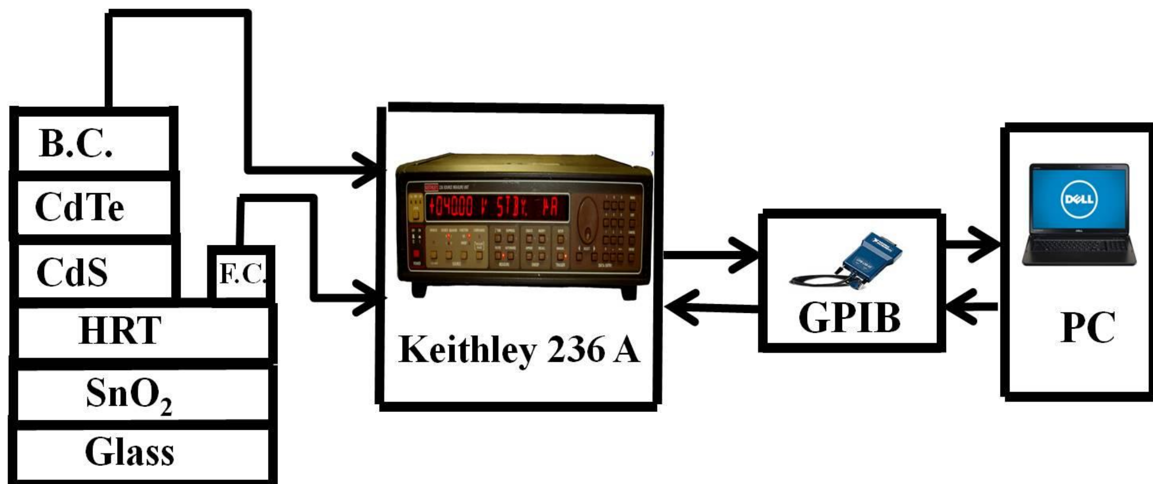


Figure 5.1 Schematic diagram of experimental set up for I-V measurements.

5.1.1 Shockley Read Hall Recombination Theory

The usual interpretation of transport with a SRH generation leakage current mechanism in the depletion region is consistent with the role of impurities occupying substitutional as well as interstitial positions on the Cd or Te sub-lattice. However, correlation of reverse-bias diode leakage current with traps is not as simple as the correlation for the crystalline Si homo-junction. SRH recombination-generation in the depletion region of polycrystalline p-CdTe/n^+-CdS hetero-junction solar cells is an important transport mechanism. The CdS/CdTe mixed interface and the depletion into CdS cannot be ignored since the light-generated minority carriers must traverse these regions to be collected at the appropriate contact. Furthermore, the traps in CdTe are crystal defects which have multiple charged energy levels between the Fermi level and intrinsic level. The crystal defects also behave as non-shallow dopants since they have energy levels between the Fermi level and the valence band. Below, we discuss the classical interpretation and the complications introduced for the p-CdTe/n^+-CdS heterojunction and elaborate the discussion of SRH R-G.

Since the ideality factor A>2 (measured from 0 to V_{oc} in dark J-V curve for each cell) is measured and see the reverse bias leakage current increasing with reverse bias, SRH R-G in the core diode is explored. Here, the saturation generation current is proportional to the number of traps in the core diode depletion region.

The generation current in the depletion layer in CdTe is given by [39]

$$J_{gen} = \int_0^W qGdx \tag{5.1}$$

The net generation rate G (in steady state, equal to the negative of the recombination rate –U) for n trap levels is

$$G = \sum_{j=1}^{n} \frac{\sigma_{nj}\sigma_{pj}v_{th}N_{tj}(pn - n_i^2)}{\sigma_{nj}[n + n_i \exp(\frac{E_{tj} - E_i}{kT})] + \sigma_{pj}[p + n_i \exp(\frac{E_i - E_{tj}}{kT})]} \qquad (5.2)$$

Where, q is the electronic charge, w is the space charge depletion width with a trap density $N_{t,}$ and energy level E_t relative to the intrinsic energy level E_i, n_i is the intrinsic carrier concentration, σ_n and σ_p are the electron and hole capture cross-sections and v_{th} is the thermal velocity calculated using the effective mass.

For large reverse bias (V >>kT/q), equation mentioned briefly in reference [124] reduces to

$$G = \frac{n_i}{2\sqrt{\tau_{n0}\tau_{p0}} \cosh[\frac{(E_t - E_i)}{kT} + \frac{1}{2}\ln\frac{\tau_{p0}}{\tau_{n0}}]} \qquad (5.3)$$

where $\tau_{n0} \sim 1/\ \sigma_n\ v_{thn}\ N_t$ and $\tau_{po} \sim 1/\ \sigma_p\ v_{thp}\ N_t$ are the electron and hole lifetimes is the depletion region. This result detailed in reference [124] indicates that the traps are most effective when

$$\frac{(E_t - E_i)}{kT} + \frac{1}{2}\ln\frac{\tau_{p0}}{\tau_{n0}} = 0 \qquad (5.4)$$

The lifetime effect on generation current can be ignored for a certain range of lifetime ratio range. With the assumption that $|(E_t\text{-}E_i)/kT| >> ln(\tau_{p0}/\tau_{n0})$, the cosh reduces to an exponential and, in this case, the trap energy level can be simply obtained from Arrhenius plot of the reverse bias generation current. Note that the assumption that τ_{p0} and τ_{n0} are not too different may not be true in CdTe/CdS solar cell.

With the simplifying assumption that $|(E_t\text{-}E_i)/kT| >> ln(\tau_{p0}/\tau_{n0})$, the generation current can be written as [39]

$$J_{gen} = \frac{qn_i W}{\tau_g} \tag{5.5}$$

where q is the charge, n_i is the intrinsic carrier concentration, W is the depletion width and τ_g is the generation life time. The diode current is then the form of equation (1) with $J_0 = J_{gen}$ and ideality factor A=2. However, omission of the temperature dependence of σ can introduce errors for CdTe.

Alternative Method

The generation current in the depletion layer in CdTe is given by [39]

$$J_{gen} = \int_0^W qGdx \tag{5.6}$$

The net generation rate G (in steady state, equal to the negative of the recombination rate –U) for n trap levels is

$$G = -U = \sum_{J=1}^{N} \frac{\alpha N_{t1}(pn - n_i^2)}{\beta(n + n_j^*) + \frac{1}{\beta}(p + p_j^*)} \tag{5.7}$$

where q is the electronic charge, W is the space charge layer width with a uniform trap density N_t/W and energy level E_t relative to the intrinsic energy level E_i, n_i is the intrinsic carrier concentration, $p_j^* = n_i \exp((E_i - E_{tj})/kT)$, and $n_j^* = n_i \exp((E_{tj} - E_i)/kT)$.

Since SRH recombination is the capture of an electron by the center followed by the capture of a hole by the same center, or vice versa, it is appropriate to introduce two new parameters

$$\alpha = \sqrt{\sigma_n \sigma_p v_n v_p} \ , \quad \beta = \sqrt{\frac{\sigma_n v_n}{\sigma_p v_p}} \tag{5.8}$$

α, is the geometric mean of the two processes involving an electron and a hole and represents each trap levels overall capability of SRH G-R. β represents the ratio of electron capturing and hole capturing of a SRH center. For a general semiconductor, β not equal to 1 since σ_n and σ_p are not equal because of the Coulomb interaction between the SRH center and the carrier.

In reverse bias, n and p in equation (5.7) can be neglected as compared to p_j^* and n_j^*. The Equation (5.7) reduces to

$$G = -\sum_{j=1}^{n} \frac{\alpha N_{t1} n_i^2}{\beta n_1^* + \frac{1}{\beta} p_1^*} \tag{5.9}$$

The basic assumptions relevant to a trap below mid-gap,

$$(\beta)\,(n_j^*) > (1/\beta)\,(p_j^*) \tag{5.10}$$

Equation (5.9) for n trap levels can be written as

$$G = -\sum_{j=1}^{n} \frac{\alpha N_{tj} n_i}{\beta \exp(\frac{E_{tj} - E_i}{kT})} \tag{5.11}$$

Or

$$G = -\sum_{j=1}^{n} \frac{\alpha}{\beta} N_{tj} n_i \exp(\frac{E_i - E_{tj}}{kT})) \tag{5.12}$$

The carrier generation rate is enhanced at higher temperature because a trap can emit electrons and capture hole very quickly.

The generation current for n trap levels is given by Equation (5.6) as

$$J_{gen} = \sum_{j=1}^{n} qG_j W \tag{5.13}$$

where q is the charge, W is the depletion width and $G_j^{'s}$ are the generation rates for each trap level given by equation (5.13) for the previously discussed simplifications..

The trap energy level can be obtained by simplifying the Equation (5.13) and is

$$E_t = -\sum_{j=1}^{n} [\frac{1}{2} E_g - (E_i - E_{tj})] \tag{5.14}$$

5.1.2 Dark and Light J-V Analysis

This section discusses about the characterization of NJIT cells with reference cell from National Renewable Energy Lab (NREL) by using J-V measurements under dark and 1sun illuminated conditions. The set of data summarizes the performance changes in the device with different parameters, viz., short circuit current density J_{sc}, open circuit voltage V_{oc}, fill factor FF, efficiency η, short circuit resistance R_{sc}, open circuit resistance R_{oc}, maximum current density J_{max}, maximum voltage V_{max}, reverse saturation current density J_o, ideality factor A and barrier height Φ_b. Different J-V curves are observed shown in Figure 5.2. This is expected because of the processing differences for these cells.

The relevant parameters of NJIT cells with reference cell from NREL are listed in Table-5.1. The observed ideality factor, *A*, in dark is greater than 2 in both the cells. NREL cells have the highest R_{sc} but they have same R_{oc}. Note that R_{sc} and R_{oc} are measured near short circuit current density and open circuit voltage and ideality factor is measured from zero to V_{oc}.

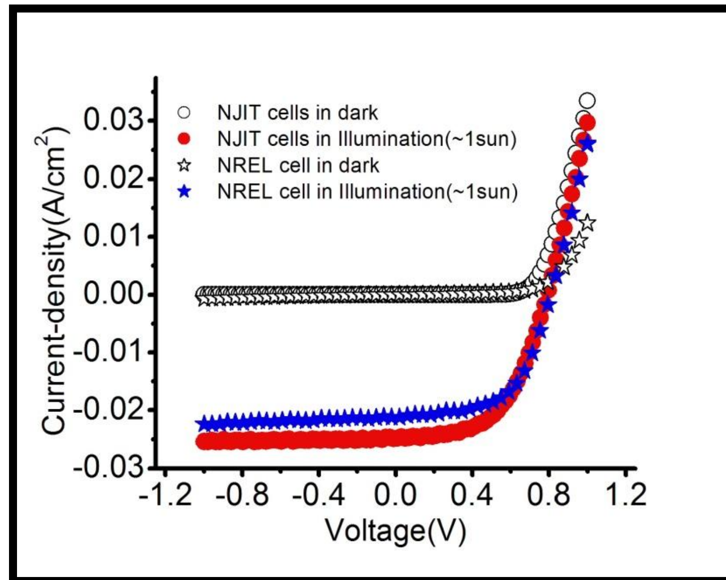


Figure 5.2 J-V Characteristics of NJIT cells with reference cell (NREL) in dark and illumination conditions.

TABLE 5.1 Extraction of Different Parameters from Figure 5.2

Cells (NJIT)	NJIT Cells	NREL Cells
J_{sc}(mA/cm^2)	25	21.2
V_{oc}(V)	0.81	0.82
FF(%)	53.2%	57.1%
η(Eff)(%)	10.8%	9.93%
A	4.44	6.77
R_{oc} (Ohm/cm^2)	8	8
R_{sc}(Ohm/cm^2)	148	296
J_0(dark) (mA/ cm^2)	2.6×10^{-5}	1.34×10^{-2}
Φ_B(V)	0.68	0.65

5.1.3 Identification of Defects using J-V-T Measurements

It is well known that, the activation energy of the reverse leakage current should in principle be half of the band-gap if recombination or generation mechanism dominates. To identify the nature of traps from their position in the energy gap, J-V-T measurements are done. As mentioned earlier, devices are analyzed at a reverse bias of -1V at different temperatures. Such a plot at -1V is shown in Figure 5.3 (a, b) for two different processed solar cells. Figures 5.3 (a, b) presents the Arrhenius plots of the leakage current of all diodes under consideration, measured at -1V in temperature range of 40^0C–120^0C .The temperature dependence revealed in Figures 5.3 (a, b) by the slopes of Arrhenius plots provides useful insight into the presence of one trap level. If recombination through localized mid-gap states within the CdTe depletion region is dominant, then a plot of *ln* (J_0T^{-2}) vs. 1000/T should yield activation energy approximately equal to half of the CdTe band gap [99,125]. This is not true in each cell. NREL cells shown in Figure 5.3 (a) has very small activation energy and does not fit into the above SRH discussion or mid-gap recombination and NJIT cell shown in Figure 5.3 (b) has activation energy close to the band gap of CdTe solar cell. More careful study is required, possibly including the nature of the CdS/CdTe interface.

Table 5.2 The results from the Arrhenius plot of $ln(J_0T^{-2})$ vs. 1000/T.

Cells	NJIT	NREL
Experimental Results	E_t=1.47eV	E_t =0.1eV

The activation energy (E_t) from Arrhenius plot for NJIT cell (which was measured from Room Temperature to 80ºC) of 1.47eV which is equal to the band gap of CdTe solar cell. The energy level of 1.47 eV for the NJIT cell means that the diode was free of “traps”. At temperature below 100^0C, the diffusion current from outside of the depletion region dominates.

No deep levels were observed in NREL cells. The activation energy of the shallow levels observed in cells is 0.10eV. This level is possibly due to V_{Cd}^{2-}/Cl_{Te}^{+} [9] defect that are widely observed in CdTe solar cells. Note that even though NREL sample had also used HgTe:Cu paste (2 atomic% Cu), only shallow levels were observed. Balcioglu et al. [7] also observed increase in deep level defect concentration for different ratio of HgTe:Cu to graphite in HgTe:Cu-doped graphite paste during the back contact formation.

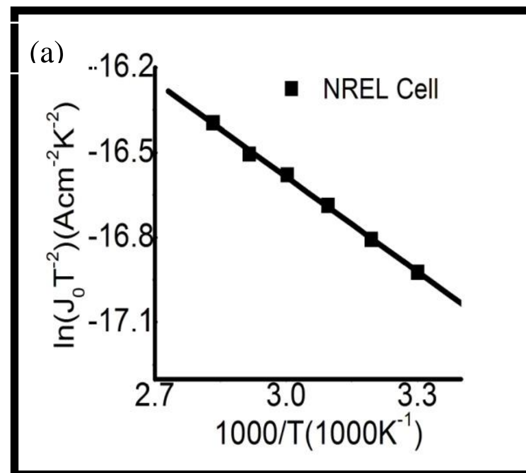


Figure 5.3 (a) Experimental results for *ln* (J_0T^{-2}) versus 1000/T for NREL solar cell.

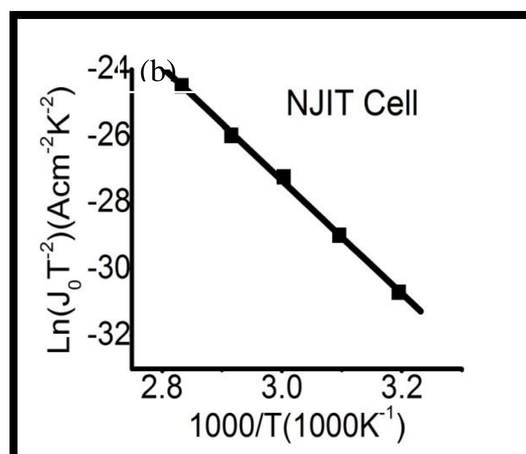


Figure 5.3 (b) Experimental results for *ln* (J_0T^{-2}) versus 1000/T for NJIT solar cells.

5.1.4 Effect of Temperature and Illumination on Hetero-junction Solar Cells

Pudov et al. [126] investigated the CdTe solar cells fabricated with five different concentrations of copper, including zero, used in back- contact formation using current – voltage J-V in the temperature range -35°C to +25°C . He observed that J_{sc} and QE were similar for all Cu-levels. Elevated temperature stress induced very little change in J-V when sufficient Cu (20nm) was used in the contact. Grecu et al. [67] found that the degradation is enhanced by illumination and could be reversed by re-annealing the samples at temperatures around 150- 200^0C. He also found that the results from Hall measurements support the PL observations, and indicate that the carrier concentration in polycrystalline CdTe films drops by about of five after one week storage at room temperature.

Figure 5.4 (a) shows that J-V measurements are done with increasing temperature from 23ºC to 80ºC to see the leakage mechanism in solar cells. Figure 5.4 (b) shows that samples, made in NJIT were heated up 110ºC and measured with decreasing temperature. Figure 5.4 (c) shows that J-V-T measurement of the degraded samples measured from

120ºC to 50ºC. The severe degradation of diode leakage of the preheated sample (Figures 5.4 (b) and (c)) may be related to Cu diffusion and the related Cu deep level defect.

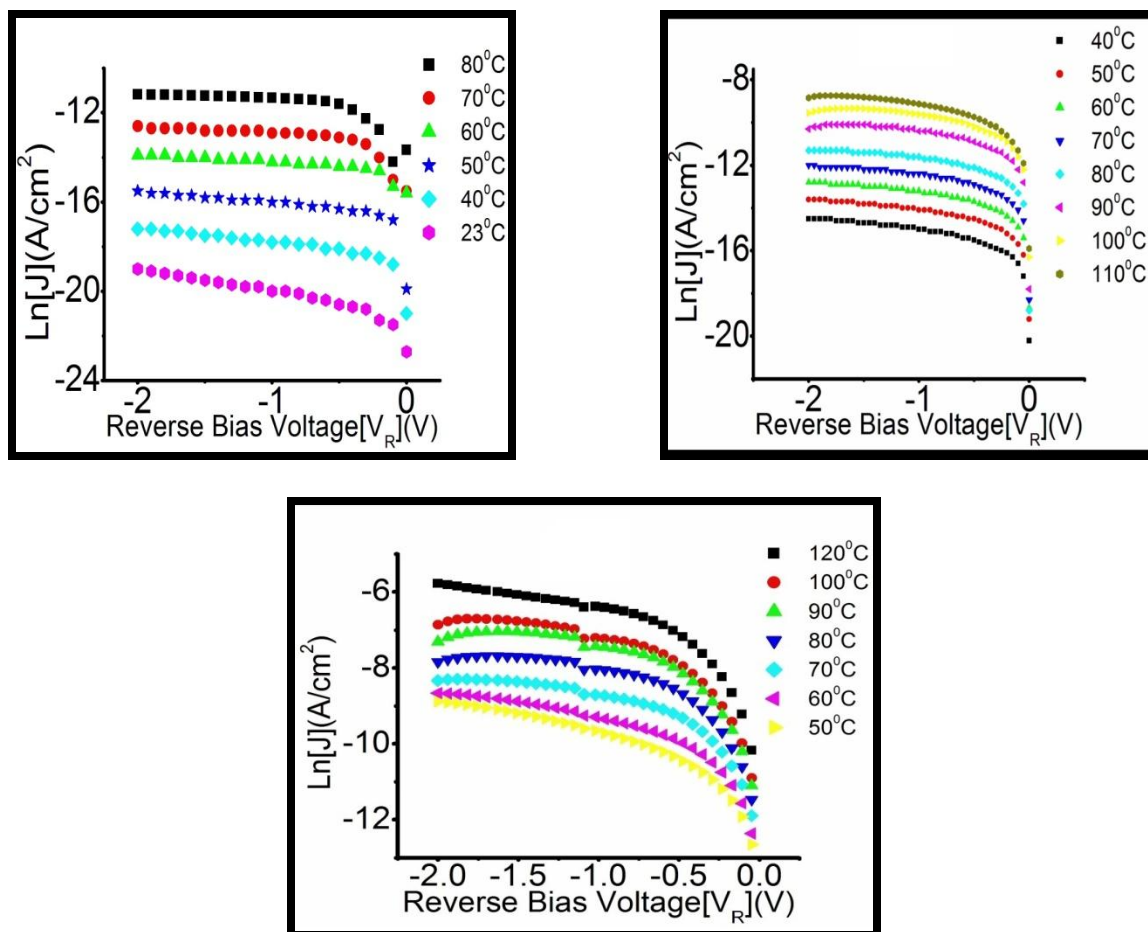


Figure 5.4 Effect of temperature in CdTe solar cells in reverse bias Current-Voltage characteristics: a) J-V-T was done from 23ºC to 80ºC, b) from 40ºC to 110ºC, and c) reverse order (from 120ºC to 50ºC).

Since the solar cell quickly degrades with measurement at temperatures greater than ~100°C, measurements are done below this temperature (~100°C) as in Figure 5.4 (a)). The results of the J-V-T measurements on solar cells made at NJIT show that while modest amounts of Cu enhance cell performance, an excessive high temperature process step degrades device quality and reduces efficiency (Figure 5.4 (b) and (c)). The location

of and the amount of trap are derived from the voltage dependence of diode leakage using a SRH recombination model (briefly explained in Section 5.1).

In an ideal model of solar cell, collection efficiency under different voltages remains one (all ehp generated by light are collected). However, for non-ideal case, J-V curve is always affected by output parameters like shunt resistance and series resistance. Recently, it has been revealed that dark current term also depends on spectral bias, which is not included in the dark current term (Equation 2.4). In this experiment, similar phenomenon is also observed with various light intensities. The current density-voltage characteristics of two samples have been tested under different irradiance levels. One sample is a good CdTe solar cell with typical efficiency ~10% while the other one is a bad CdTe/CdS cell with typical efficiency ~5%, with low shunt resistance, both of which are to demonstrate their behavior of dark current term.

Figure 5.5 (b) shows that the cells have low shunt resistance in comparison with good solar cell (shown in figure 5.5 (a)). The CdTe solar cells are tested under illumination ranging from 0% to 100% of AM 1.5, as shown in Figure 5.5 (a) and (b). Both series effect and shunting effect are subtle since the slopes remain nearly flat and constant.

Two important results have been obtained when $R_{sh} >> R_s$ in low forward bias. The dark current shifts with increase in illumination, and observed voltage-dependent slope variation in poor quality cells rather than good cells. The first phenomenon can be explained by the exponential growth of diode current term and linear growth of leakage current term in Equation 2.4. However, the light-induced variation of slope is interesting because it is not included in this equation. Based on such inconsistency, different

explanations have been proposed: carrier tunneling and voltage dependent collection efficiency. Both low shunt resistance and high series resistance contribute to the non-ideal behavior of I-V curve both in forward bias and reverse bias. Light current is not linear with light intensity. Therefore, the corresponding reasons are explained as follows.

The first reason might be that there is a large portion of the photocurrent J_L flowing through shunt resistance, which is called leakage current and output current, reduces correspondingly when $R_s >> R_{sh}$. On the one hand, the cell is severely affected by the shunting effect in the forward bias, causing a sharp drop and steep slope nearby V_{oc}. On the other hand, series effect becomes dominant as reverse voltage increases, inducing the obvious increment of current.

The another reason might be that by doing the analysis of the J-V measurements at different light intensities, which indicates an increase in intensity–dependent leakage conductance. This may be due to interface defect states whose occupancy is changed by the intensity of illumination. An alternate explanation is a current dependent voltage loss at the p-bulk contact.

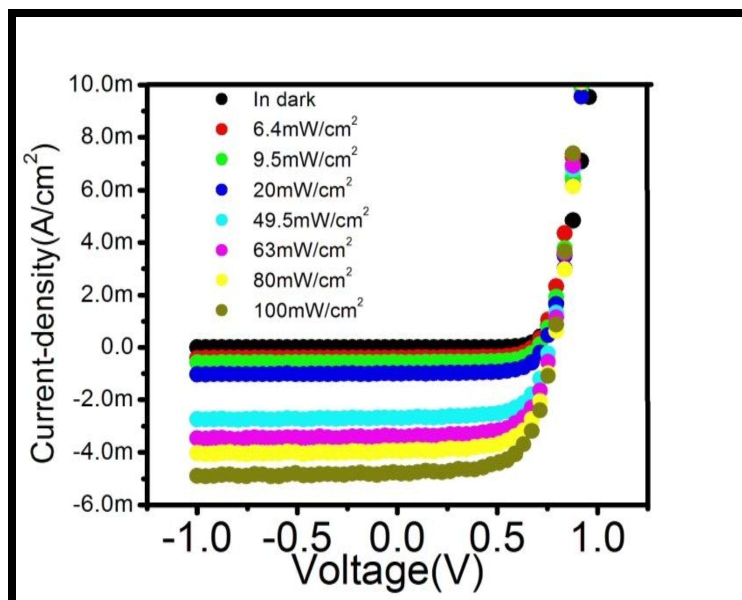


Figure 5.5 (a) Effect of Illumination with different intensity in good quality CdTe solar cells.

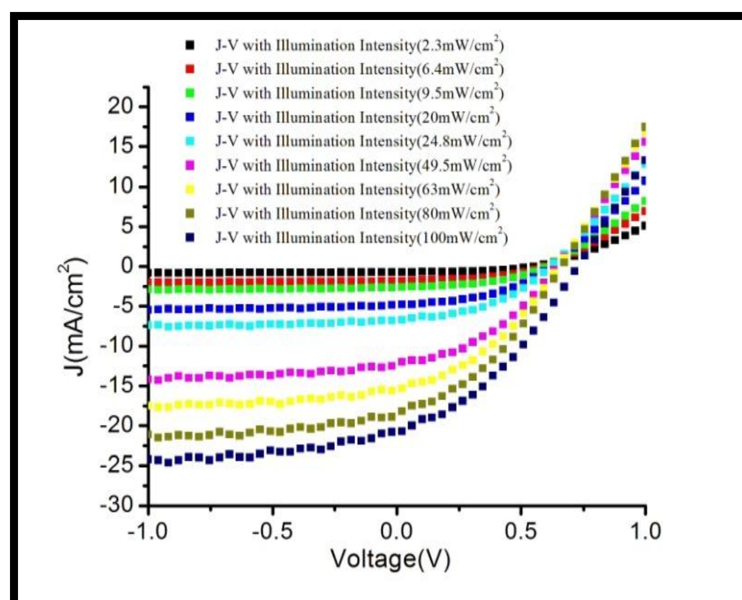


Figure 5.5 (b) Effect of Illumination with different intensity in poor quality CdTe solar cells.

5.2 Effect of Degradation Due to Copper Diffusion in CdTe Solar Cells

This section investigates the shallow/deep level impurities with different processed cells by using temperature dependent current-voltage (J-V-T). Since, J-V-T measurements indicate that a large concentration of defects is located in the depletion region. It further suggests that while modest amounts of Cu enhance the cell performance by improving the back contact to CdTe, the high temperature (greater than ~100°C) process condition degrade device quality and reduce the solar cell efficiency. This is possibly because of the well-established Cu diffusion from the back contact into CdTe. By J-V-T theory it was observed that Copper containing contacts initially perform well, but their high temperature performance can be a problem, as the copper under circumstances diffuses through the CdTe layer and forms Cu related substitutional or interstitial defects.

Figure 5.6 shows J-V under dark and 1sun illuminated conditions for NJIT cells under different conditions, the parameters for which are summarized in Table 5.3. Different J-V curves are observed for these cells. This is expected because of the heating effect for each cell.

The diode current-voltage characteristics in dark for model – n^+-CdS /p-CdTe solar cells is

$$J(\lambda, P_\lambda, V) = \{J_{0,SRH} [\exp(^{qV/AkT}) - 1] + J_L(\lambda, P_\lambda)\} f(V) \qquad (5.15)$$

where J_o is the reverse bias “saturation” current (saturates for the ideal diode but is a function of applied voltage or SRH R-G), V is the applied bias, A is the ideality factor (A=1 for the ideal diode and A=2 for SRH R-G). J_L is the light current and f (V) is collection transfer function (holes from CdTe to CdS contact and electrons CdS to CdTe contact).

In this section, reverse bias diode current is dominated by Shockley-Read-Hall recombination $J_{0,SRH}$ (N_t, E_t, σ_n, σ_p, $V^{1/2}$, T) when measurements are done with $J_{0,SRH}$ (N_t, E_t σ_n, σ_p, T) vs. temperature T at large reverse bias $V \geq -1V$ without illumination between the temperature range from 25°C - 100°C.

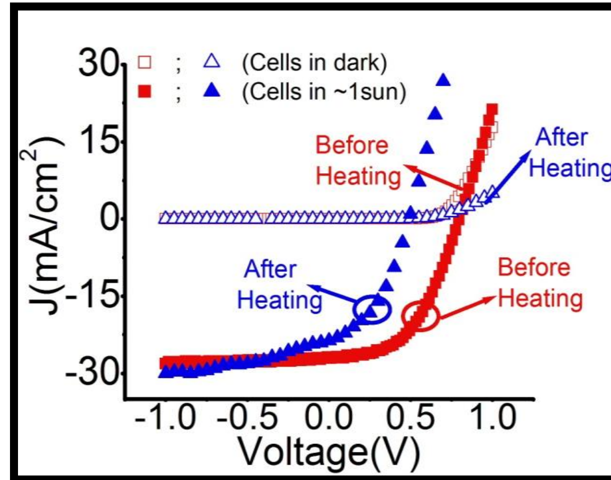


Figure 5.6 J-V Characteristics of NJIT cells in dark and illumination condition.

Table 5.3 Extraction of Different Parameters from Figure 5.6

Cells (NJIT)	(Before Heating)	(After Heating)
J_{sc}(mA/cm^2)	25	23.7
V_{oc}(V)	0.81	0.48
FF (%)	53.2%	49.5%
η(Eff)(%)	10.8%	4.79%
A	4.44	3.35
J_0(dark)(mA/cm^2)	2.65×10^{-5}	1.94×10^{-5}

Devices were analyzed at a reverse bias of -1V. Several trap levels are found in all cells in the temperature range of 40^0C-120^0C (shown in Figure 5.4). The measurement of J-V-T suggests that the difference between cells is the diffusion of Cu at higher temperature. The lower open-circuit voltage (V_{oc}) of NJIT cells might correspond to trap related SRH recombination in the p - n junction depletion region. Assuming SRH R-G is the dominant reverse bias leakage mechanism, a slope of ln (J_0T^{-2}) vs. 1000/T should yield the trap energy level.

To identify the observed activation energies from J-V-T with a specific deep level is difficult. Published data for deep levels for CdTe give different activation energies from different techniques. Our simple technique cannot distinguish if more than one deep level is operative as a generation center, the measured activation energy may be average of several levels, further complicating the analysis. Further, an analysis of the J-V at various temperatures provides the information on the distribution of generation centers.

Cu used in CdTe solar cell is well known to be a fast diffuser and especially since polycrystalline CdTe has relatively rough surface, when the solar cell is heated up more than 100^0C, Cu can easily move into or through the CdTe layer leaving in the back contact region. Assuming that it is a positive ion (Cu_i^+), however, the junction field of the cell will resist the forward diffusion. Hence, the rate of diffusion would be expected to be dependent on the bias across the cell. Recently, capacitance transients were used by Enzenroth, et al. [127] and Lyubomirsky et al. [128] determine the diffusion parameters of mobile Cu_i^+ ions in CdTe and materials based upon a transient ion drift (TID) method was first developed by Heiser and Mesli [129]. In particular, Enzenroth et al. [127] used the TID approach to quantify an increase in mobile Cu_i^+ as a function of increased Cu

added during cell fabrication. The presence of mobile charge, in particular, Cu_i^+ could be the cause to get deep traps in cells when the measurements were done for the sample was heated up.

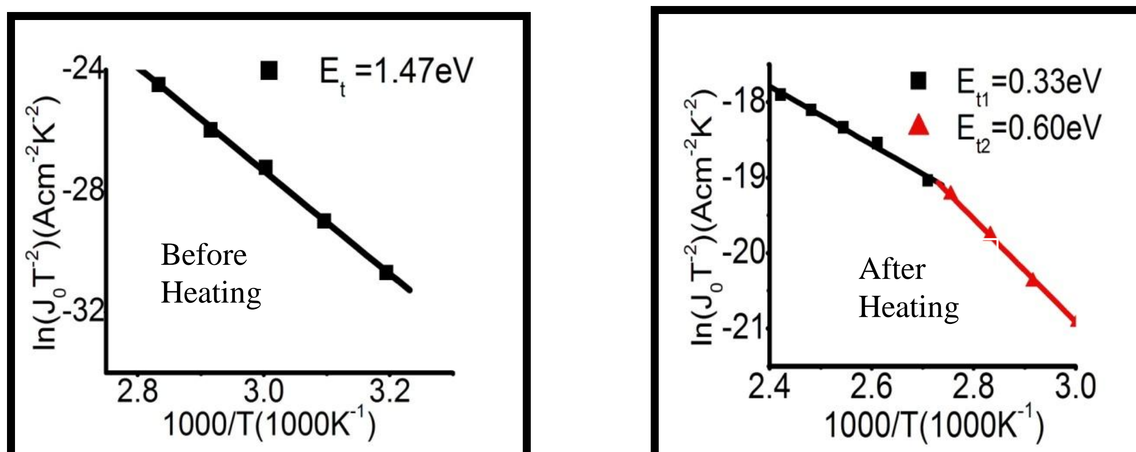


Figure 5.7 (a) Experimental results for *ln* (J_0T^{-2}) versus 1000/T for good CdTe/CdS solar cells and (b) Experimental results for *ln* (J_0T^{-2}) versus 1000/T for post heated CdTe/CdS solar cells.

The activation energy (E_t) for Arrhenius plot for cells (which were measured from Room Temperature to 80ºC, shown in Figure 5.7(a)) of 1.47eV which is equal to the band gap of CdTe solar cell. At temperature below 100^0C, the diffusion current from outside of the depletion region dominates.

The activation energies obtained for cells (Measured with aging at 110ºC to RT). Figure 5.7(b) clearly shows that more than one trap are present when the samples are heated up above 100^0C. It also shows that in the low temperature region, the activation energies are larger than high temperature region. This point to the fact that the reverse currents in the low temperature region are dominated by one trap and in high temperature region is dominated by another trap level.

Figure 5.7 (b) clearly shows that E_{t1} 0.33eV is possibly due to substitutional Cu_{Cd}^- (effect of σ (T) proper) when the measurements were done from higher (~120^0C) to lower

temperature ($\sim 40^0$C), the possibility of finding the semi – shallow level defects related to impurities (Cu) increased because of Cu diffusion at higher temperature. At higher temperature, the junction reverse current is dominated by generation current produced within the depletion region. They agree well with the reported finding by Balcioglu et al. [7] during the study of CdTe solar cells with ODLTS technique with Cu as a back contact layer. The samples, grown with higher concentration of copper in HgTe:Cu (3 atomic% Cu) pastes [7], might have contributed towards the formation of the copper-related defect (E_v+0.35eV). This level, however, could not be detected at low reverse biases [7] since it does not contribute significantly to the carrier transition process. Theoretical calculations have shown that Cu_{Cd}^- is expected to form a level at E_v+0.22eV [99]. Also these defect levels agree well with the reported finding by Komin et al. [130] with DLTS technique with Cu as a back contact layer showed activation energy of Cu-related defects within the range of 0.27-0.35eV.Regardless of the actual energy level for Cu_{Cd}^- it is likely that this observed defect in cells can form under the conditions of excess amount of Cu.

The defect in Figure 5.7 (b) that is observed in cells with activation energy 0.60eV was discussed by considering the nature of this defect (Measure with aging at 120ºC to RT). This deep trap level (E_v+0.6eV) is clearly associated with Cu_i^{2+} as the activation energy of this defect was observed earlier [27, 73] by admittance spectroscopy. It is shown that the observed peak (~0.55eV) [27, 73] is a deep level due to Cu and the peak appears when Cu is added to the back contact formation process.

5.3 Evaluation of Cu Related Deep Defects in CdS/CdTe Solar Cells

This section investigates CdTe solar cells with back contacts formed by either (I) 15nm Cu evaporation followed by application of carbon conductive paste embedded with micron sized Cu particles in ZnTe powder named as cell^1 and (ii) only with the above mentioned conducting paste, named as cell^2 are evaluated. A Cu-related deep level defect with an activation energy of $E_a \cong 0.57$eV is observed for Cu evaporated back contact cells and an intrinsic defect with activation energy $E_a \cong 0.89$eV is found for cells prepared only by ZnTe:Cu embedded carbon paste.

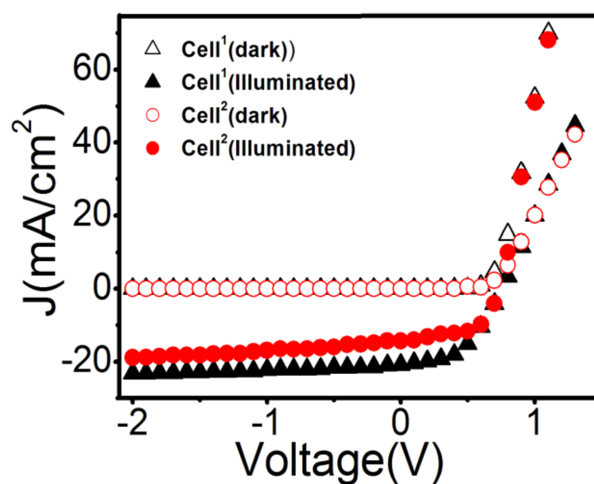


Figure 5.8 Dark and 1-Sun illuminated J-V curves for both the solar cell types, Cell^1 and Cell^2.

Figure 5.8 shows the J-V curves under the dark and 1-sun illuminated conditions for sets of samples named cell^1 and cell^2, where cell^1 has excess copper in comparison of cell^2. Results suggest that open circuit voltage is similar in both the sets of cells but cell^2 has a large drop in short circuit current density (J_{sc}). This indicates that photocurrent is voltage dependent in cell^2 due to enhanced leakage, caused possibly by reduction in

lifetime of photo-generated carriers. At room temperature, the ideality factor, A in dark condition for sets of cell[2] (1.9) is higher than sets of cell[1] (1.3) indicating that the diffusion current and recombination current are comparable since typical A value lies between 1 and 2 [39]. However, recombination current is dominant in sets of cell[2]. Table 5.4 outlines all the parameters observed for both the sets of cells. The barrier height is measured in both the sets of cells by using equation in reference [30]. The efficiency in cell[1] devices is higher than as compared to cell[2] devices were observed. Presence of varying degree of copper on the back contact has definitely some impact on the quantum efficiency (QE) [131, 126]. Work is currently in progress to evaluate its detailed impact on band-gap energy and the results will be published elsewhere.

Generally, the J-V relation in heterojunction with illumination of a generic solar cell with parasitic resistance can be described by any of the diffusion models, either the emission model or the recombination model [39] where the relation is represented by the standard diode equation [39]

$$J = J_0\left[\exp\left(\frac{q(V - R_s J)}{AkT}\right) - 1\right] - J_L + \frac{(V - R_s J)}{R_{sh}} \tag{5.16}$$

where q is the electronic charge, A is the effective ideality factor which includes recombination-generation and collection efficiency, T is the absolute temperature , J_0 is an effective reverse saturation current density, V is applied voltage, R_s is the series resistance, k is Boltzmann constant R_{sh} is the shunt resistance and J_L is light current density. R_s is calculated using the general formula $R_s = \left[\frac{d\left\{\ln\left(\frac{J}{J_0}\right)\right\})}{dV}\right]^{-1}$ at high forward

bias (0.6 to 1.3 V) from the J-V curve and R_{sh} is calculated by using $R_{sh} = \left[\frac{dJ}{dV}\right]^{-1}_{V=0}$ in reverse bias (-1 to -2V) and included in the Table 5.4. Note that the current is dependent on temperature *T*.

Table 5.4 The Relevant Parameters of Both Cells from Figure 5.8

Cells (NJIT)	Cell[1]	Average Values of sets of Cell[1]	Cell[2]	Average Values of sets of Cell[2]
J_{sc}(mA/cm^2)	20.9	20.2	14.3	14.2
V_{oc}(V)	0.75	0.7	0.75	0.72
FF(%)	54%	51%	55%	51%
η(Eff)(%)	7.7%	7.23%	5.9%	5.2%
A	1.3	1.6	1.9	2.5
J_0(dark)(mA/cm^2)	3.6×10^{-5}	3×10^{-5}	1.6×10^{-4}	1×10^{-4}
Φ_B(V)	0.52	0.48	0.54	0.50
R_s(Ω/cm^2)	0.47	1.73	0.82	2.89
R_{sh}((Ω/cm^2)	2.01×10^6	5.77×10^6	2.7×10^5	4.8×10^5

Analysis of the J-V-T (reverse bias) at constant voltage yield the following relation to estimate the activation energy

$$E_a = - kT * \{ln(J_0 / J_{00})\} \quad (5.17)$$

where J_{00} is a constant and E_a is the activation energy. If $ln(J_0T^{-2})$ versus 1000/T plot yields a straight line, the activation energy of the charge carriers, can be estimated from

the slope. Figure 5.8 shows the Arrhenius plot of $ln(J_0T^{-2})$ vs. 1000/T in the reverse bias at -1V within the temperature range of 40^0C-100^0C for each cell. One deep defect/electron-trap is identified in sets of $cell^1$ with activation energy of 0.57eV while deep defect/hole-trap is identified in sets of $cell^2$ with activation energy of 0.89eV respectively.

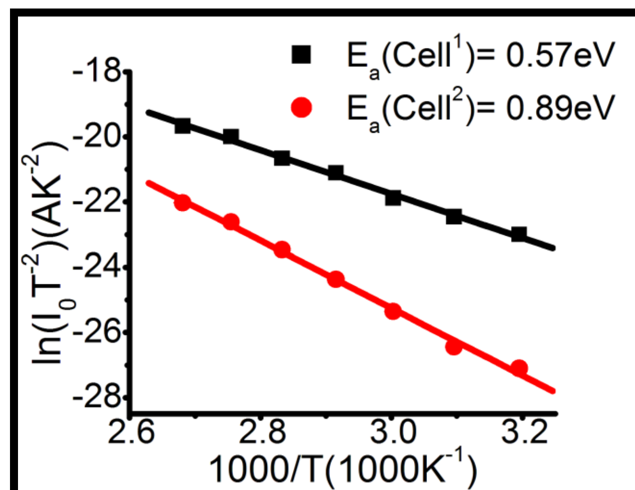


Figure 5.9 Activation energy of each cell at reverse bias voltage (V_R =1V).

To identify the nature of traps from their position in the energy gap, J-V-T measurements are done. The trap energy level 0.57eV of sets of $cell^1$ can be attributed to a deep defect related to copper. This is in good agreement with the activation energy (0.55 eV) for a Cu-related defect obtained from back contact processing, involving Cu and determined by using the current-voltage characteristics [27]. Also, a deep level trap due to interstitial copper with activation energy of 0.55eV is observed earlier determined by admittance spectroscopy [23]. It is well known that once the amount of Cu exceeds a threshold level at the back contact it diffuses to the CdTe layer to form Cu related defects either by forming substitutional complexes (Cu_{Cd}^-) or interstitial defects (Cu_i^{2+}).

Balcioglu et al. [7] found through optical deep-level transient spectroscopy (ODLTS) measurements in polycrystalline CdTe/CdS solar cells that the most probable Cu-related defect is a deep donor and may be a doubly ionized Cu interstitial ion (Cu_i^{++}). The observed concentration of the Cu_i^{++} defect corresponded well to the Cu diffusion profile monitored by secondary ion mass spectroscopy (SIMS) with a Cu piled up at the CdTe/CdS interface [7, 132]. It is, therefore, possible that this deep defect level is originated from the Cu-containing back contact due to diffusion of excess Cu that was evaporated. Since sets of cell[1] samples had higher concentration of copper with 15 nm evaporated copper in addition to ZnTe:Cu (2 atomic% Cu) paste, possible formation copper-related defect (E_v+0.57eV) can be inferred, where E_v is the energy at valence band edge. No such Cu-related defects were observed in sets of cell[2] samples simply due to the limited availability of Cu at the back contact. Note that sets of cell[2] only used ZnTe:Cu paste (2 atomic% Cu). The observed energy level of 0.89eV is believed to be an hole trap. By using photo-induced current transient spectroscopy (PICTS), Rakhshani et al. [133] also observed this level, which was identified as the positive Cd_i^{2+} interstitial defect. It is, therefore, reasonable to assume presence of intrinsic defects like Cd_i^{2+}.

5.4 Detection of Traps by using Thermally Stimulated Current Technique (TSC)

In this chapter, to identify the nature of traps from their position in the energy gap as determined by I-V-T measurements at reverse bias with different heating rates is attempted. Since, dark current is small through a reverse - biased barrier, so it is possible to detect small change in current due to carrier emission. As mentioned earlier, devices were analyzed at a reverse bias of 0.5V at different temperatures. I-V-T measurements

were done in dark by using Keithley 236 Source Meter. The samples have to be mounted in a special designed sample holder in cryostat. Thereafter, the samples are cooled down to room temperature and proper care is taken during measurements. I-V-T measurements are done at different heating rates 0.06K/sec, 0.08K/sec, and 0.17K/sec. At these heating rates, the set of samples are heated from 150K to 350K shown in Figure 5.9.

A single trap level in the fast/slow re-trapping case is given by general equation is given by

$$I(T) = A\exp\left[\frac{-E_t}{kT} - \frac{B}{\beta}\int_{T_0}^{T}\exp\left(\frac{-E_t}{kT}\right)dT\right] \qquad (5.18)$$

$$or\exp\left[\frac{E_t}{kT_m}\right] = \frac{B}{\beta}\frac{kT_m^2}{E_t}$$

where E_t ,is the energy level of trap, k is the Boltzmann's constant, T_m is the maximum peak temperature in dI/dT versus Temperature plot, and β is the heating rate for the thermal scan at a rate of 0.06, 0.08, and 0.17 K/s .

In this experiment, traps are filled with sample at low temperature then upon heating, the trapped carriers are released to the appropriate band and there is an increase in free carrier density and hence increase in current. Since, the amount of trapped charges are finite being determined by number of traps, and as the temperature is increased further all the trapped carriers are eventually released. Since excess carriers in the band recombine, the current eventually decreases, so there is a peak in a plot of current change as a function of temperature. The temperature at which this peak occurs is related to energy level of trap. It is clear from the figure (see Figure 5.10) that a maximum in I-V-T

plot is observed at a particular temperature T_m. and observed peaks shifts to higher temperature as the heating rate is increased.

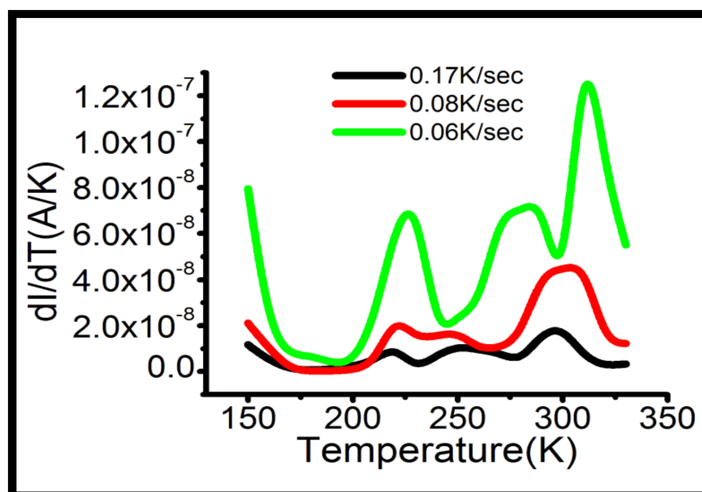


Figure 5.10 Temperature dependence of I–V in CdTe solar cell.

By using equation (5.18), $\ln(T^2_m/\beta)$ vs. $1000/T_m$ should be a straight line whose slope will give the value E_t/k. Our experimental results show a straight line curve between $\ln(T^2_m/\beta)$ vs. 1000/T (see Figure 5.11). The activation energy calculated from the Arrhenius plot of $\ln(T^2_m/\beta)$ vs. 1000/T is within the range of 0.08-0.10eV. When the measurements are done from lower temperature ~150K to a higher temperature to ~350K, the observed three shallow level defects are believed to be related to A center as it neutralize the native V_{cd}^- acceptor. Due to compensation mechanism of A center, the Cadmium vacancies are not easily revealed in cholrine containing CdTe films (CdTe:Cl). Since A center play a significant role in the compensation process. Cadmium vacancies (V_{cd}) tend to form A - center with Cl donor leaving concentration of isolated V_{cd} are low. In addition, this shallow trap levels seems to be associated with a hole trap as the

activation energy of this defect was also observed by Photo induced current transient spectroscopic (PICTS) [37, 133].

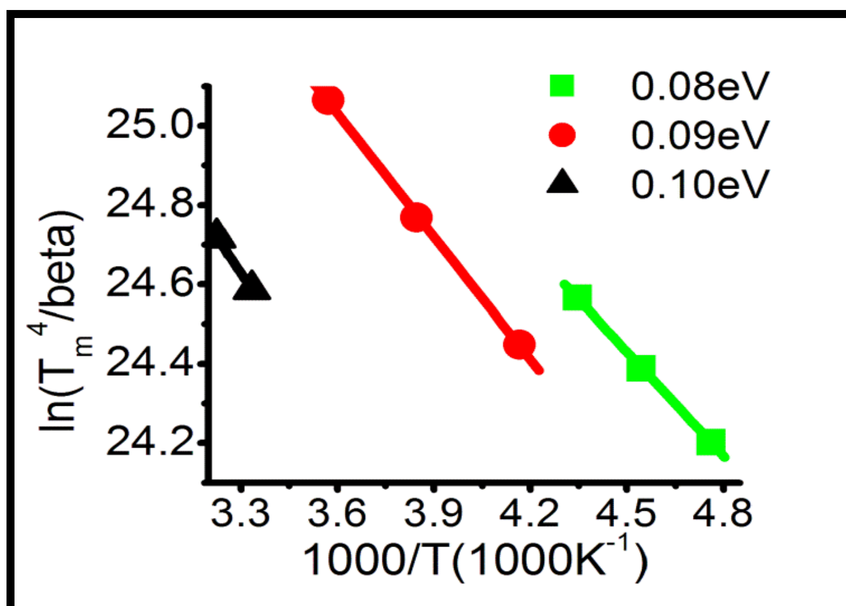


Figure 5.11 *ln*(T^2_m/ β) versus 1000/T_m curve in CdTe solar cells.

5.5 Chapter Summary

J-V-T measurements of variously processed n^+-CdS/p-CdTe solar cells have been presented. The applicability of reverse bias (-1V) generation current (SRH R-G theory) is discussed, which is used to correlate the various traps with the experimentally measured activation energies resulting from the plot of $ln\ (J_0T^{-2})\ vs.\ 1000/T$. Even though using a simple J-V-T theory to definitely identify defects in CdTe is difficult because of the large number of closely spaced trap energy levels with possibly very different capture cross-sections. The simple J-V-T measurement is a powerful tool for characterizing process reproducibility and establishing process control. It is observed that once the amount of Cu used to form the back contact exceeds a threshold level it diffuses to CdTe layer and

forms Cu related substitutional or interstitial defects. The thin film n^+-CdS/p-CdTe solar cells made with evaporated Cu as a primary back contact are also characterized, using the temperature dependence of the reverse bias diode current (J-V-T) to determine the energy levels of deep defects. Since the solar cell quickly degrades (probably because of the well-established Cu diffusion from the back ohmic contact into CdTe) with measurement at temperatures greater than ~100°C, measurements are done below this temperature (~100°C). The results of the J-V-T measurements on solar cells made at NJIT show that while modest amounts of Cu enhance cell performance, an excessive high temperature process step degrades device quality and reduces efficiency. Results identify the physical trap though the energy (activation) level. The location of and the amount of trap are derived from the voltage dependence of diode leakage using a SRH recombination model. J-V measurements at different illumination intensity were also discussed for detailed analysis by using neutral filters respectively. A measureable trap number density will increase the diode saturation current from the voltage independent Shockley value to the usually larger and voltage-dependent SRH value proportional to W (V)/τ. The increase in leakage conductance with intensity is probably due to interface defects states whose occupancy is changed by the intensity of illumination. An alternate explanation is that carrier lifetime in the depletion region decreases with light intensity.

CHAPTER 6

DEVICE CHARACTERIZATION OF CDTE SOLAR CELLS BY USING CAPACITANCE-VOLTAGE TECHNIQUE

6.1 Capacitance – Voltage (C-V) Analysis

The C-V characteristics are analyzed in the dark by using an Agilent HP 4284A impedance analyzer. Temperature dependent C-V-T measurements are carried out. The data are collected by using labview programme, which can calculate doping concentration, N_A and V_{bi} of the device respectively. Sample temperatures are varied from 25ºC to 100ºC on a micromanipulator probe station. The C-V measurements are done at different frequencies ranging from 100Hz -1MHz. The doping concentration and built in potential of the device can be obtained from C-V measurements for uniformly and non uniformly doped materials. Slope of $(A/C)^2$ curve at reverse bias provides doping concentration N_A and intercept gives built in potential V_{bi}.

Figure 6.1 shows that schematic diagram of C-V measurement set up of two diode model. In earlier work, Stollwerck and Sites showed that a CdTe cell with a back contact barrier could be modeled by a series connection of two diodes with opposite polarities [129]: the CdS/CdTe main junction diode and the CdTe/metal-contact back diode. Based on a similar two-diode model, Niemegeers and Burgelman et al. developed a simple analytical theory that explained the observed rollover in thin-film CdTe solar cells [66]. Other groups have also studied the current limiting effect of the back contact on the performance of CdTe solar cells [130,131]. However, the effects of series resistance and the leakage conductance at the main and back diodes were not included in the simplified model. McCandless et al have used a two-diode model to study the effect of back contact,

and the barrier height was determined from the temperature dependence of the series resistance [132]. Recently, the details of the CdTe/metal contact have been investigated by using a similar two-diode model (Figure 6.1) from capacitance–frequency characteristics [21].

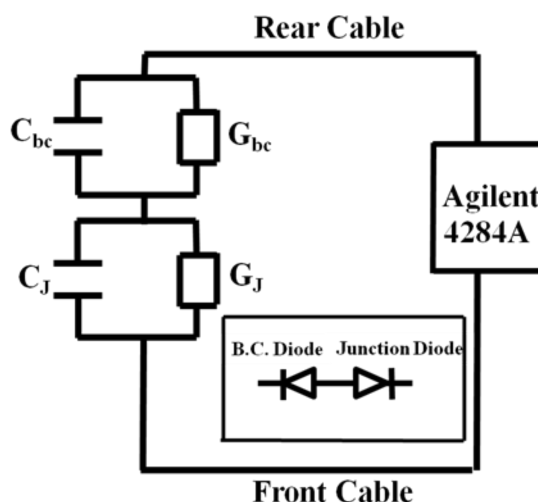


Figure 6.1 Schematic diagram of C-V measurement set up of Two Diode Model.

6.1.1 Bias Dependent Dark C – V Analysis

This section discusses about the characterization of NJIT cells with reference cell from NREL by using C-V measurements under dark conditions. C-V measurements have been used to determine the doping density profiles of the lightly doped side of a p-n junction diode. A modulation voltage of 5mV is applied and the d.c. bias is typically varied from 0.5V to -1V. Table 6.1 shows the values of the free acceptor concentration calculated from voltage biased capacitance and built in potential for all cells in dark at 100 kHz. Strictly, the slope of $1/C^2$ as a function of reverse bias voltage gives a free carrier concentration for the case of shallow acceptors; a case is not true for CdTe. Figure 6.2 shows the variations in junction capacitance as a reverse bias at 100 kHz for all different

processed cells. N_a is derived from an abrupt junction approximation fit to the data is Figure 6.2. The doping concentration (N_a) in dark for NREL cell is one order higher than NJIT cells is observed. Cells having a lower apparent doping level may indicate that the method for introducing Cu from the back contact process is more effective in these cells by allowing the donor copper interstitials Cu_i^+ (which we will talk in section 6.4) to substitute the double acceptor vacancy trap in the p-type CdTe material [18]. It is very interesting to note that Cu may cause dramatic changes of the character of the CdTe thin films. As NJIT cell shows the low level p doping due to presence of p_{Cd}, it suggests that the conductivity of cells can become even lower in the beginning of the Cu contacting treatment because the inclusion of Cu impurity in the form of interstitial Cu_i may compensate the p-dopant therefore the hole density is lower in case of NJIT cells rather than NREL cells. Also Cu_{Cd} has higher transition energy levels (0.35eV) than p_{Cd} (0.14). This also explains why carrier density reduces in NJIT cells. The experimental demonstrations of the variation of quality of cells with different back contact annealing or different Cu treatment temperatures are further discussed in section 6.3.

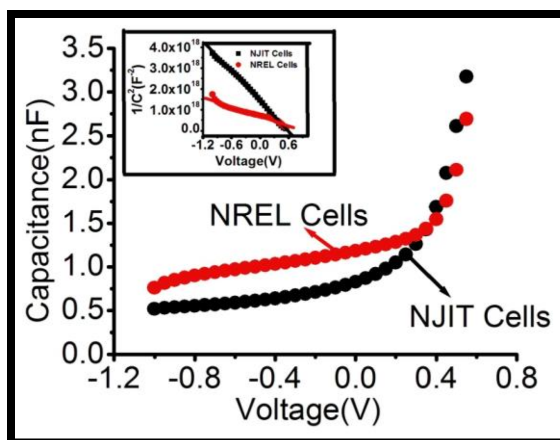


Figure 6.2 Capacitance versus voltage characteristics of differently processed CdTe solar cells.

Table 6.1 Comparison of Doping Carrier Concentration of Each Cell from Figure 6.2

Parameters	NREL Cells	NJIT Cells
V_{bi}(V)	0.9	0.65
N_a (100kHz) (cm^{-3})	1.86×10^{14}	7×10^{13}

6.1.2 Frequency Dependent C – V Analysis

Figure 6.3 shows that the C–f curves of a thin film solar cell decay from a low-frequency capacitance (CLF) to a high frequency capacitance (CHF) due to the presence of deep level traps. A broad distribution of deep trap levels gives rise to a gradual decay of the C – f curves over several decades of frequency. Several phenomenon can give rise to such simple mechanism, including one single deep trap level, an energy barrier at a contact, dielectric relaxation in a bulk layer, and interface states. The interpretation of slowly decaying C–f curves in terms of a distribution of trap states in the energy gap is classical and well documented, e.g., [133]. The interpretation of step-wise decaying C–f curves in terms of various single level traps goes back to the early work of Sah [134].

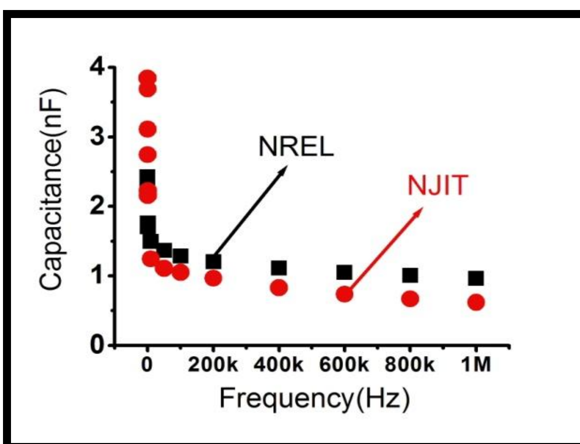


Figure 6.3 Capacitance vs. frequency dispersion of different processed CdTe solar cells.

C-V characteristics of sets of CdTe solar cells named as $cell^1$ and $cell^2$ in the dark at different frequencies are shown in Figure 6.4. The observed frequency dispersion is opposite in nature for both the sets of cells. The reverse biased capacitance for sets of $cell^1$ shows that as the frequency increases capacitance reduces significantly below the low frequency level. Depending on the thickness of absorber layer the entire CdTe absorber layer can be fully depleted. Because of the large amount of free carriers ($10^{23}cm^{-3}$) available in the back contact metal, a further increase of reverse bias brings virtually no change in depletion width in the p-CdTe layer.

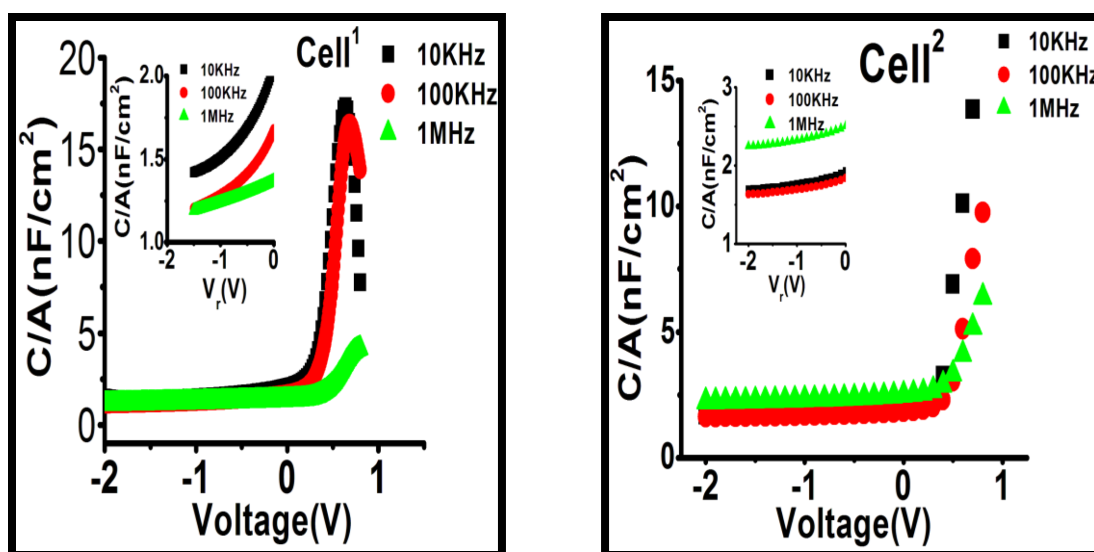


Figure 6.4 Capacitance versus voltage at different frequency for different processed CdTe solar cells, namely $cell^1$ and $cell^2$.

6.1.3 Temperature Dependent C-V Analysis

The capacitance of a solar cell can yield information about extraneous states within the band gap, and it can often give a credible profile of the carrier density within the absorber layer. To further confirm the presence of shallow or deep defects in CdTe solar cells, temperature dependent C-V measurements are carried out. A modulation voltage of 5mV

was applied and capacitance is measured within the range of -2V to 0.8 V for reverse/ forward biased CdS/CdTe junction. In this case, the thickness of the CdTe layer is 12µm and C-V measurement explores only part of the CdTe thickness from the junction. In addition, the depletion width can be further reduced due to the presence of defects related to impurity.

The temperature dependent reverse and forward bias C-V characteristics of CdTe solar cell at 100khz are shown in 6.5 respectively. The capacitance magnitude is relatively small in cell[2], corresponding to a small carrier density ($p = 7\times10^{13} cm^{-3}$) in comparison with cell[1] ($p = 1.1\times10^{15} cm^{-3}$).The fact that the curves are relatively flat in chosen frequency (100 kHz) strongly suggests that they are not significantly affected by extraneous states. The reduction in net carrier density of interface traps due to compensation (deep donors) at the CdTe/CdS junction. The interpretation is the rapid increase in hole density in cell[2] takes place as the depletion edge enters the back contact region. As it can be seen in Fig 6.5(a) and (b) the capacitance increases with increase in temperature of both cells, especially in depletion region.

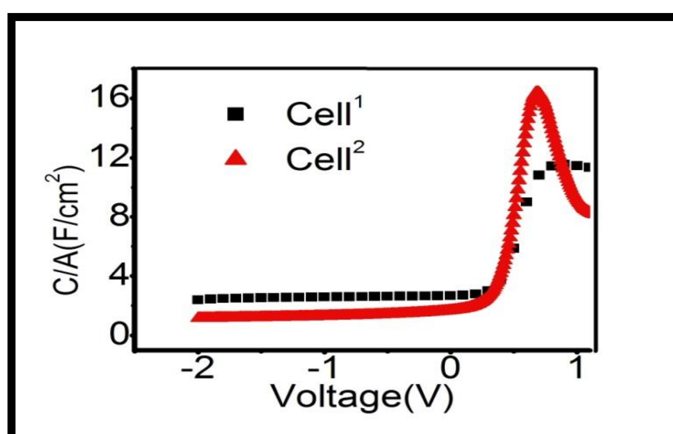


Figure 6.5 (a) Capacitance versus voltage at different frequency for different processed CdTe Solar Cells.

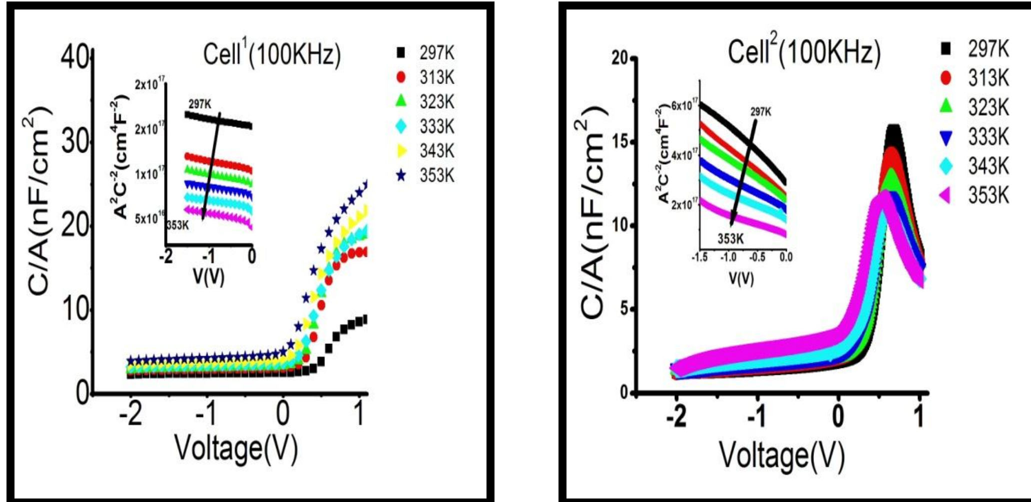


Figure 6.5 (b) Capacitance versus voltage at fixed frequency (100 kHz) for CdTe solar cells (namely cell[1]) at different temperatures and (c) Capacitance versus voltage at different frequency (100 kHz) for different processed CdTe solar cells (namely cell[2]).

Figure 6.6 shows the spectrum from temperature differential capacitance measured at 100 kHz in reverse bias for each cell form 25ºC to 80ºC in the dark for fixed time (10msec) to partially fill the traps with majority carriers, which gives a peak dC/dT temperature of approximately 343K for cell[1] is quiet same for each reverse bias. The temperatures of maximum (majority-carrier traps) dC/dT, T_f, give estimates of the thermal activation energies of the majority or minority trap energy levels. Thus at 323K and 343K, dC/dT can be observed for a trapping level as semi shallow as E_t=E_v+0.17/0.22 eV for cell[1] and E_t=E_v+0.12/0.08eV for cell[2].

It is evident from Figure 6.6 that the major change was seen when T= T_f , in other words E_f crosses/below E_t shown in band diagram (Figure 2.3). Using this approach, two positive signals in temperature differential capacitance spectrum corresponds to majority traps. The peak location of majority traps did not change at various reverse bias voltages.

The activation energy extracted from the peak from temperature differential capacitance measurements.

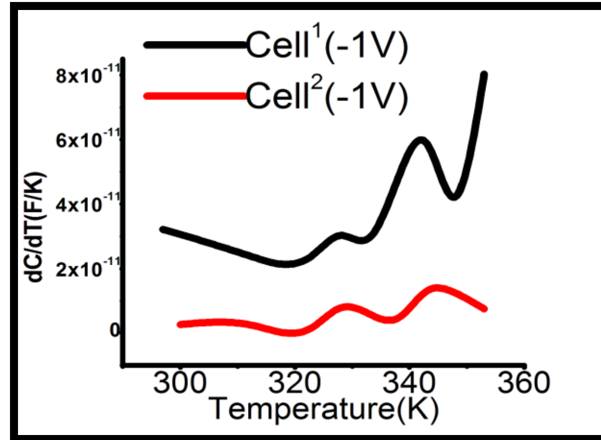


Figure 6.6 Differential capacitance transients of CdTe solar cells.

The capacitance transient exhibits characteristics that change with temperature (T) and time (t) [135]. Experimentally a non equilibrium occupation of traps is created and then relaxation of trapped charge is studied by monitoring capacitance transients. Its canonical form is

$$C(t, T) = C_0 \exp(-e_p t) \tag{6.1}$$

where the emission rate e_p is,

$$e_p = \sigma(T)v(T)N_C(T)\exp\left[-\frac{\Delta G(T)}{k_B T}\right] \tag{6.2}$$

Where v is the thermal velocity of the holes in the band, given by

$$\frac{1}{2}m^* v^2 = k(T) \tag{6.3}$$

N_v is the density of states in the valence band

$$N_v = 2\left[\frac{2\pi m^* kT}{h^2}\right]^{\frac{3}{2}} \tag{6.4}$$

where m* is the effective hole mass (m^*_h =0.8m_e) and the temperature dependence of σ_p must be considered. In many cases, temperature dependence of the capture cross section is exponential

$$\sigma_n(E, T) = \sigma_o(E)\exp(-\Delta E_\sigma(E)/kT) \tag{6.5}$$

where σ_0 and ΔE, are constants inherent to the trap.

The capacitance transient in equation (6.1) after substituting Equations (6.2), (6.3), (6.4) and (6.5) can be expressed as

$$\ln\left[\frac{\left(\ln\frac{C}{C_0}\right)}{tT^2}\right] = -\Delta G/kT - \sigma_p \tag{6.6}$$

The derivative form of the Arrhenius equation, indicates that ωdC/dω = dC/d[ln(ω)] and dC/dT are equivalent to each other except for a proportional factor that consists of the intrinsic defect parameters (E_a) and fixed temperature(or frequency).

For temperature –derivative method, the derivative of C with respect to T can be written as

$$\frac{dC}{dT} = -\frac{N_t(E_w)k_B qw[\ln(2\nu_0 - \ln(\omega))]}{U_d} \tag{6.7}$$

where N_t (E_ω) is the defect density of states, U_d is the built in voltage and w is the depletion width. By using temperature derivative method, we can find single or multiple defects. The temperature derivative method is found superior.

The results obtained from C-V-T measurements shows that cell[1] has trap concentration N_t (5.7 x10^{17} cm^{-3} at 328K and 1.57x10^{17} cm^{-3} at 343K) which is higher than the doping concentration, also in cell[2], the obtained trap concentration is (1.8x10^{18}

cm^{-3} at 328K and $4.75x10^{17}cm^{-3}$ at 343K) which is also higher than the doping concentration.

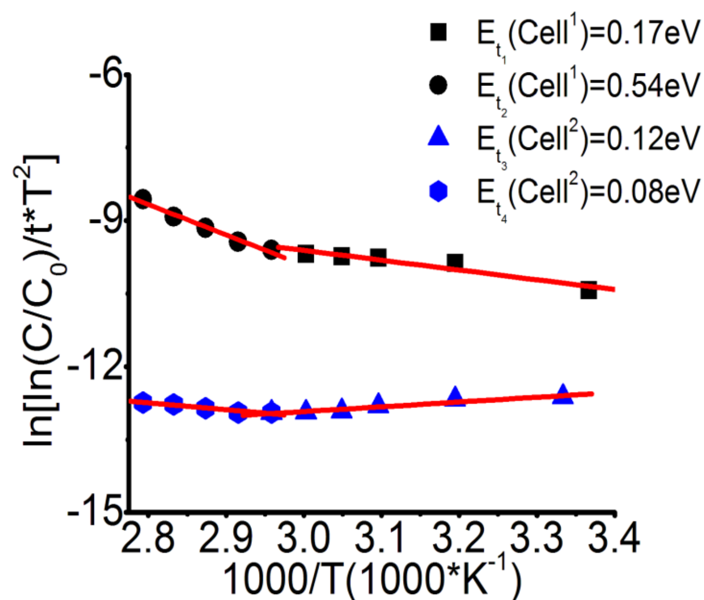


Figure 6.7 $ln(ln(C/C_0)/t*T^2)$ versus 1000/T for different processed CdTe solar cells.

Table 6.2 Temperature Dependent Values of Various Parameters Determined from C-V Characteristics of Cell[1]

T(K)	$N_a(cm^{-3})$	$E_{FP}(eV)$	$W_D(cm)$	$N_t(cm^{-3})$
293	$4.22 x10^{15}$	0.18	$1.8x10^{-4}$	-
323	$1.4x10^{15}$	0.35	$8.35x10^{-5}$	$5.7 x10^{17}$
343	$1.76x10^{14}$	0.26	$7.4x10^{-4}$	$1.57x10^{17}$

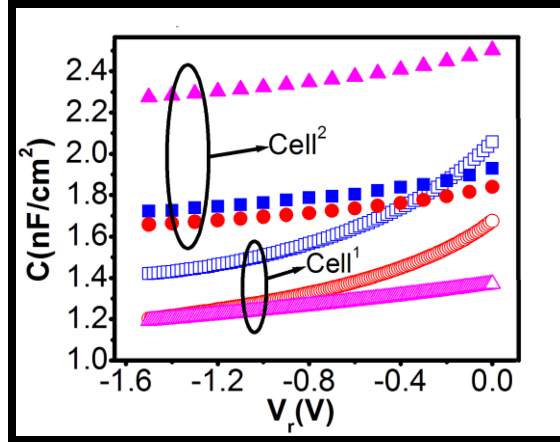
Table 6.3 Temperature Dependent Values of Various Parameters Determined from C-V characteristics of Cell[2]

T(K)	$N_a(cm^{-3})$	$E_{FP}(eV)$	$W_D(cm)$	$N_t(cm^{-3})$
300	$7x10^{13}$	0.28	$2x10^{-3}$	-
323	$7x10^{13}$	0.38	$2.6x10^{-4}$	$1.8x10^{18}$
343	$1.4x10^{14}$	0.38	$2.6x10^{-4}$	$4.75x10^{17}$

6.2 Effect of Cu Incorporation at the Back Contact Layer: Two Diode Model

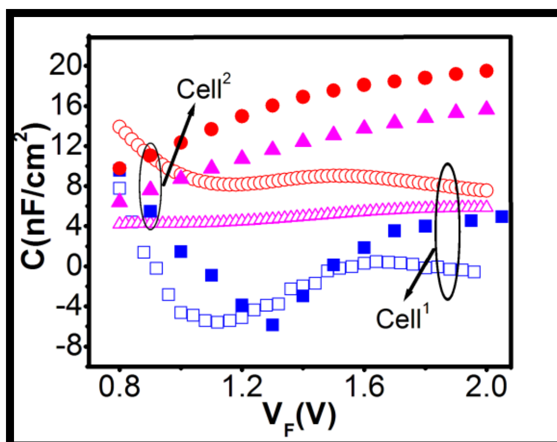
This section confirms the frequency dispersion in C-V measurements due to the presence of Cu-related deep level traps for different processed cells with Cu back contact. The behavior is believed to be due to diffusion of excess Cu from the contact. It is further observed that majority carrier deep level traps (Cu-related or intrinsic) contribute differently to the degradation of electronic properties of the CdTe solar cells.

Reverse biased C-V characteristics of sets of cell[1] (15nm Cu evaporation followed by application of carbon conductive paste embedded with micron sized Cu particles in ZnTe powder) and cell[2] (only with the above mentioned conducting paste) in the dark are shown in Figure 6.8 at different frequencies. The observed frequency dispersion is opposite in nature for both the sets of cells. The reverse biased capacitance for sets of cell[1] shows that as the frequency increases capacitance reduces significantly below the low frequency level (Figure 6.8).



Figures 6.8 Reverse biased C-V characteristics (-2V to 0V) acquired in the dark for sample groups cell[1] (open symbols) and cell[2] (solid symbols) at frequencies □■ 10 kHz, ○● 100 kHz and △▲ 1 MHz respectively.

For sets of cell[2], on the other hand, capacitance increases with frequency. The frequency dependence is due to the finite time constant associated with the high concentration defects that are present in the depletion layer [136]. In sets of cell[1] when the signal frequency is increased, the reciprocal of emission time constant, the charge variation on the Cu-related deep centers (0.57eV) in CdTe, cannot follow the signal voltage in the depletion layer and hence cannot contribute to the capacitance [20, 137]. For CdTe, the concentration of deep level defects is comparable to the doping level due the presence of Cu. In other words, depending on the Cu-related deep electron trap concentration the depletion layer edge was shifted as a function of frequency modifying the depletion layer width. In case of sets of cell[2], due to the lack of Cu-related defects and the energy level of the observed defect level (0.89eV) above the intrinsic Fermi level are responsible for the observed reverse effect.



Figures 6.9 Frequency dependent of forward biased (0.8V to 2.0V) capacitance measured in the dark at frequencies □■ 10 kHz, ○● 100 kHz and △▲1 MHz for cell[1] (open symbols) and cell[2] (solid symbols) respectively.

Figure 6.9 shows the forward-biased frequency dispersion of sets of cell[1] and cell[2] samples in the dark respectively. Assuming a two-diode model as described by Demtsu et al. [138] when a forward bias is applied across the device a voltage equivalent to built-in potential is dropped across the CdTe/CdS junction, whereas the contact junction becomes reverse biased. According to this assumption, the CdTe thin film solar cell can be split into two depletion regions, the depletion region of the CdTe/CdS junction and a depletion region at back contact barrier region. Under dark condition, when the solar cell is forward biased the back contact junction is reversed biased [30, 139] limiting the current density. So the measured capacitance in forward bias represents mostly the contact junction capacitance [30]. As can be seen in Figure 6.9, both the sets of samples have similar frequency dispersion behavior. Higher capacitance was observed for 100 kHz in both cases and once the frequency goes up (1 MHz) capacitance decreased. At 10 kHz there may be strong interference from the junction capacitance [30] in series with the contact capacitance showing a minimum in capacitance value in both devices. The time constant of intrinsic defects (~10 ms) determines this behavior of frequency dispersion and is

similar for both the cases. Only intrinsic traps adjacent to the contact, therefore, contributed to the capacitance, as most of the available Cu had diffused towards the CdTe/CdS junction and piled up in the depletion region. Only intrinsic traps adjacent to the contact, therefore, contributed to the capacitance, as most of the available Cu had diffused towards the CdTe/CdS junction and piled up in the depletion region. This further confirms the observation in the J-V characteristics and the assumption that defect level in the depletion layer of cell[1] samples is Cu-related.

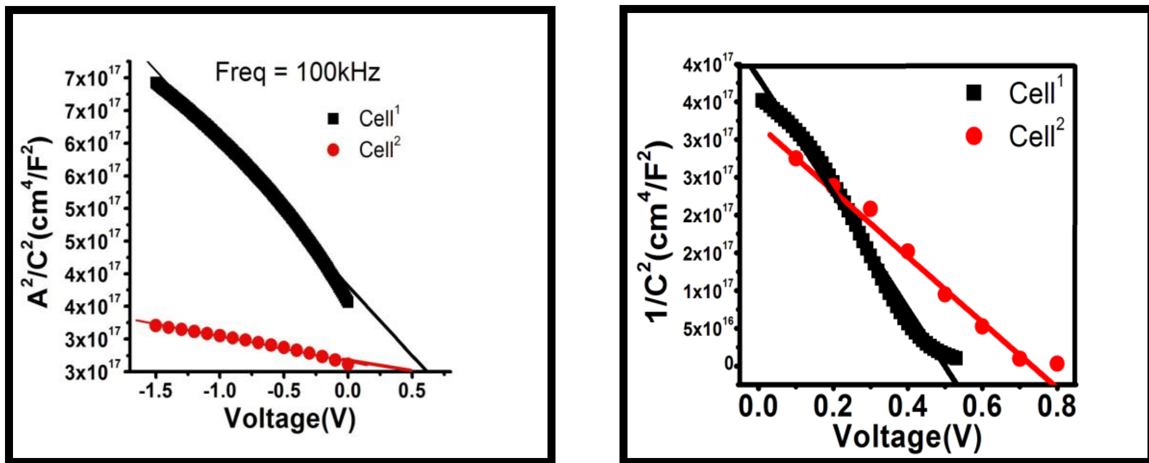


Figure 6.10 $1/C^2$ versus V curve of each cell in the dark at frequency 100 kHz **(a)** in reverse bias and **(b)** in forward bias.

Figures 6.10 (a) and (b) show $1/C^2$ versus V curves [36] of two cells in reverse bias and forward bias at 27^0C. It is apparent that the variations in back contact processing strongly influences the voltage dependence of the cell capacitance. At reverse bias sets of cell[1] exhibits a larger effective capacitance than sets of cell[2]. However, due to the p-CdTe Schottky barrier of the back contact, the measured C is smaller than p-n junction's real capacitance. Therefore, the experimental results from the dark $1/C^2$ versus V curves lead to a hole density for sets of cell[1] = $7x10^{13}cm^{-3}$ instead of real acceptor concentration N_a.

As we know if the Cu substitutional acceptors are compensated by donor states Cu interstitial Cu_i then hole density is lowered which is few order lower than the acceptor concentration, which is consistent with the measured value of hole density in cell[1] [13]. The donor compensation of acceptor is only significant when $p < N_a < N_d$. The hole density for sets of cell[2] = $3.52x10^{14}cm^{-3}$ seems have donor states due to less amount of copper. A high trap density ($N_t = 10^{15}cm^{-3}$) of defects resulting for deep donors at the CdS/CdTe junction could also contribute to the reduction in hole density. Contribution of higher amount of Cu in evaporated back contact in sets of cell[1] compared to sets of cell[2] is further confirmed.

Hence, frequency dispersion in C-V measurements confirms the presence of Cu-related deep level traps for cells with Cu evaporated back contact whereas no such defects were observed in carbon paste contact. The behavior was believed to be due to diffusion of excess Cu from the contact. It is further observed that majority carrier deep level traps (Cu-related or intrinsic) contribute differently to the degradation of electronic properties of the CdTe solar cells.

6.3 Detection of Traps using Capacitance Transients Technique

C-V-T measurements are analyzed in dark by using an Agilent 4284 LCR Meter. The samples have to be mounted in a special designed sample holder in cryostat. Thereafter, the samples are cooled down to room temperature and proper care is taken during measurements. C-V-T measurements are done at different heating rates 0.06K/sec, 0.08K/sec, and 0.17K/sec. At these heating rates, the set of samples are heated from 150K to 350K.

The capacitance of a solar cell can yield information about extraneous states within the band gap, and it can often give a credible profile of the carrier density within the absorber layer. The temperature dependent reverse bias C-V characteristics of CdTe solar cell at 100 kHz at reverse bias with different heating rates are shown in Figure 6.12 respectively.

$$\exp\left[\frac{E_t}{kT_m}\right] = \frac{B}{\beta}\frac{kT_m^2}{E_t} \tag{6.8}$$

In this method, the initial charge states of the traps are set to fill the traps with majority carriers at reverse bias in the dark and at 150K. The junction temperature is then increased so that the trapped carriers in the depletion layer are thermally excited out, giving junction capacitance changes with increasing temperature. The temperatures of maximum (majority carrier traps) dC/dT, T_m give estimates of the thermal activation energies of the majority trap energy levels. Observed peaks shifts with different heating rates were shown in Figure 6.11. The total capacitance change around each T_m gives the concentration of carriers trapped at that level. This method demonstrates that the capacitance change due to filling the majority-carrier traps in the depletion region can be employed to detect levels. Thus starting C-V-T measurements at 150K, the shallow level can be detected from a depletion region.

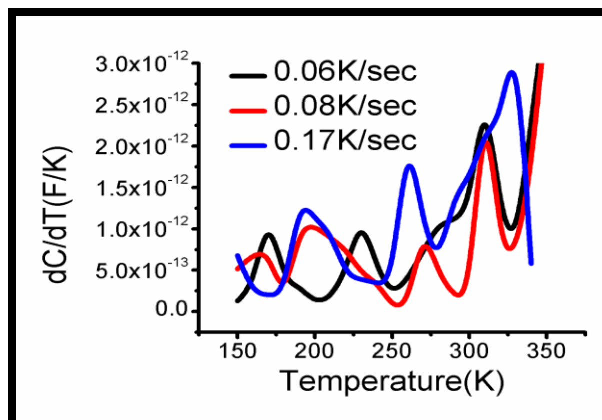


Figure 6.11 Temperature dependence of C – V in CdTe solar cell.

The $ln(T^2_m/\beta)$ vs. 1000/T (see Figure 6.12) plot from C-V-T measurement shows a straight line curve when the equation (6.8) is used. The slope of this curve provides the value of the activation energy, E_t/k, estimated to be within the range of 0.07-0.08eV. It clearly shows that when the measurements were extended to lower temperatures (~150K) the possibility of finding the shallow level defects related to V_{Cd}–Cl_{Te} becomes easier. Note that the activation energies observed from both I–V-T (mentioned above) and C-V-T measurements are identical. This further confirms the presence of this shallow trap level. In addition, it is clearly associated with hole trap, observed earlier by Photo induced current transient spectroscopic (PICTS) method [36, 128].

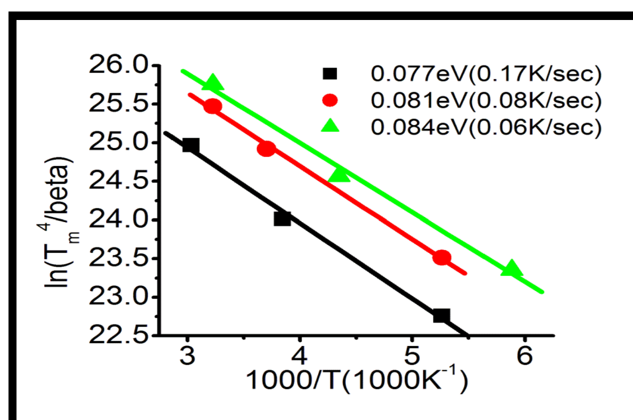


Figure 6.12 $ln(T^2_m/\beta)$ versus 1000/T_m curve in CdTe solar cells.

6.2 Chapter Summary

The observed results indicate that presence of an intrinsic defects in the depletion layer significantly degrades the CdTe solar cell performance [32]. This is evident in the reduction of efficiency in case of sets of cell^2. As discussed earlier the recombination current is dominant in sets of cell^2 indicating the influence of intrinsic defects. Frequency-dependent C-V characteristics also support the presence of majority carrier traps. This clarifies why the efficiency is low in sets of cell^2. On the other hand, even though there is a large concentration of Cu-related deep levels in sets of cell^1 these sites contribute to the hole concentration in the CdTe layer. Since the obtained hole concentration of p-CdTe keeps in the range of 10^{14}-10^{15}cm^{-3}, instead of desired level of 10^{16}-10^{17}cm^{-3}, resulting in lower junction band bending and back contact difficulty which contribute to a lower efficiency as compared to the reported value of 17.3% efficiency.

CHAPTER 7

STUDY OF DEEP DEFECTS USING TEMPERATURE DEPENDENT CAPACITANCE SPECTROSCOPY (TDCS)

By investigating the reverse bias junction capacitance, TDCS allows the identification the energy levels of depletion layer defects. The trap energy levels and trap concentrations are derived from temperature-dependent capacitance spectra. Three distinct deep level traps are observed from the high-temperature ($T > 300K$) TDCS due to the ionization of impurity centers located in the depletion region of the n^+-CdS/p-CdTe junction. The observed levels are also reported by other characterization techniques. TDCS seems to be a much simpler characterization technique for accurate evaluation of deep defects in n^+-CdS/p-CdTe solar cells.

TDCS has also been effectively used to investigate several high resistive materials with special emphasis for GaAs substrates [95]. In capacitance spectroscopy [59], a measurement at low frequency was used such that carriers can fully respond to small signal changes of bias.

In this work, CdTe solar cells fabricated with Cu-evaporated back contacts were characterized to demonstrate the effectiveness of TDCS technique. The temperature dependent C-V characteristic is monitored as a function of time. CdTe solar cells with Cu-evaporated back contacts demonstrated the capacitance peaks at a frequency of 100 kHz indicating the trap charge build up due to deep levels. After incorporating the temperature dependence of a cross-section in the activation energy, the observed deep levels were attributed to doubly ionized cadmium vacancies and Cu-related sites identical to reported experimental results [6 -30] obtained for deep defects. It is demonstrated that

TDCS offers a rapid and convenient means of detecting and characterizing the properties of the deep centers. In addition, the detailed theoretical background of the trap activation energy and temperature dependence of capture cross-sections have been described.

7.1 Basic Equations of TDCS

In the CdTe layer, the deep level impurity serves as a Generation-Recombination (G-R) center and both the conduction and valence bands participate in the recombination and generation process. The capacitance of the depletion layer varies as a function of time as the charge response changes with time when voltage is applied. Since the contribution of interface traps to the capacitance has already been considered the deep level impurities or traps in the semiconductor bulk can respond to the capacitance-time profile. The contribution of traps is a complicated function of the density and energy level of the traps as well as the sample temperature and frequency of the ac voltage. A potential problem arises for deep-lying dopant atoms not fully ionized at the measurement temperature. Unlike the dopants (phosphorous, arsenic and boron) in silicon that are ionized completely, some of the deep level impurities in p-type CdTe are only partially ionized at room temperature. Therefore, in the quasi neutral region (qnr), the hole density is no longer equal to N_A in qnr.

The detailed theoretical background of alternating current (ac) capacitance in the n^+-CdS/p-CdTe solar cell diode has been provided by various authors [140-142]. Here one recalls some essential points as applicable to the discussion. The dc bias is set to -1V and holes as the majority carriers are considered. By assuming that the dielectric relaxation time is smaller compared to the emission time of gap states under the small ac

signal, it is noteworthy that only gap states near the Fermi level can bring changes in their occupancy and thus bring significant contribution to the capacitance.

The time constant τ can be written as τ_p for holes. The hole emission rate, e_p which is the inverse of the time constant can be stated as

$$e_p(T) = \frac{1}{\tau_p} = N_v(T)\sigma(T)v_{th}(T)\exp\left[-(\frac{E_t - E_v}{kT})\right] \tag{7.1}$$

where τ_p is the time constant at a particular temperature for ionization of a deep trap in the part of the potential barrier where there are no free carriers; this is related to temperature, k is Boltzmann's constant; E_t is the trap energy level; E_v is the valence band energy, N_v is the effective density of state in the valence band; σ (T) is the capture cross section which depends on the temperature; v_{th} is the mean thermal velocity.

The temperature dependent cross-section can be stated as

$$\sigma(T) = \sigma_\infty \exp\left[-(\frac{E_\sigma}{kT})\right] \tag{7.2}$$

where E_σ is the energy contribution from the temperature-dependent cross-section and σ_∞ is a constant. Including equation (7.2), the equation (7.1) can be rewritten as

$$e_p(T) = \frac{1}{\tau_p} = N_v(T)\sigma_\infty v_{th}(T)\exp\left[-\left\{\frac{(E_t + E_\sigma) - E_v}{kT}\right\}\right] \tag{7.3}$$

Equation (7.3) can be rewritten as

$$e_p(T) = \frac{1}{\tau_p} = N_v(T)\sigma_\infty v_{th}(T)\exp\left[-\left\{\frac{E_a - E_v}{kT}\right\}\right]; \tag{7.4}$$

where $E_a = E_t + E_\sigma$, is the combination of trap energy and the trap energy component of cross-section.

In the general case, the capacitance depends on time and temperature; if the temperature dependence is incorporated via the time-constant, the capacitance of an abrupt junction in a Schottky diode may be put as

$$C^2(t,\tau) = \frac{q\varepsilon\varepsilon_0 \left\{N_s + N_A^{\ -}\right\}}{2(V_{bi} - V)} \tag{7.5}$$

where q is the electronic charge, ε is the permittivity of the material; ε_0 is permittivity in free space; N_s is the shallow acceptor concentration; V_{bi} is the built-in potential, V is the applied bias voltage, and N_A^- is the concentration of an ionized impurity which varies as follows:

$$N_A^- = N_A\left[1 - \exp(-\frac{t}{\tau})\right], \tag{7.6}$$

Including the expression of N_A^- , equation (7.5) can be rewritten as

$$C^2(t,\tau) = \frac{q\varepsilon\varepsilon_0\left[N_s + N_A\left\{1 - \exp(-\frac{t}{\tau}\right\}\right]}{2(V_{bi} - V)} \tag{7.7}$$

Now, differentiate Equation (7.7) first with respect to time and then with respect to τ, one can be write as

$$2C\frac{dC}{dt} = \frac{q\varepsilon\varepsilon_0 N_A}{2(V_{bi} - V)}\left(\frac{1}{\tau}\right)\exp\left(-\frac{t}{\tau}\right) \tag{7.8}$$

$$\frac{\partial}{\partial\tau}\left(C\frac{dC}{dt}\right) = \frac{q\varepsilon\varepsilon_0 N_A}{4(V_{bi} - V)}\left[\left(-\frac{1}{\tau^2} + \frac{t}{\tau^3}\right)\exp\left(-\frac{t}{\tau}\right)\right] \tag{7.9}$$

The temperature at which there is the maximum change in capacitance is obtained by equating Equation (7.9) to zero, which gives

$$t = t_x = \tau_p \tag{7.10}$$

Then by choosing sampling time t_x, τ_p can be determined, the hole time constant, which can be obtained from Equation (7.9) corresponding to a definite temperature.

To find the cross-section and trap energy, one can choose temperatures T_{s1} and T_{s2} at time t_1 and t_2 respectively in Equation (7.4) to get two Equations

$$\frac{1}{\tau_{p1}} = N_v(T)\sigma_\infty v_{th}(T)\exp\left[-(\frac{E_a - E_v}{kT_{s1}})\right] \text{ and } \frac{1}{\tau_{p2}} = N_v(T)\sigma_\infty v_{th}(T)\exp\left[-(\frac{E_a - E_v}{kT_{s2}})\right] \quad (7.11)$$

whose solution gives E_t and σ_∞ where τ_{p1} and τ_{p2} are the time constants at temperatures T_{s1} and T_{s2} respectively.

From (7.8) and (7.10), the maximum temperature derivative for the capacitance for a concentration of majority carriers can be obtained as:

$$N_A = \frac{4(V_{bi} - V)}{q\varepsilon\varepsilon_0} C_p \tau_p \frac{dC}{d\tau} \quad (7.12)$$

The parameters, therefore, can be conveniently estimated from the capacitance change as a function of time when temperature is varied.

7.2 TDCS Display of Capacitance Transient Data to Estimate E_a and σ_a

Figure 7.1 shows the change in capacitance at different temperatures as a function of time measured using a 100 kHz signal after the reverse bias (-1V) applied at time t=0 ms for CdTe solar cells in the dark condition. As can be seen, the capacitance increases and saturates within 10 ms at 300 K. At higher temperatures capacitance increases rapidly in the beginning (~10 ms) and then slowly increases till 50 ms (range of the measurements). It is clear that the initial charge states of the majority carrier traps are immediately filled by the applied reverse bias (-1V) in the depletion region and tend to detrap with time at a

particular temperature thereby changing the capacitance. The energy band diagram of trapping and detrapping is shown in Figure 7.2 of CdS/CdTe heterojunction. At a reverse bias of 1 V and at t=0 traps in the depletion region are completely filled (Figure 7.2(a) and at t =∞ (50 ms in our case) the device comes to an equilibrium value once the detrapping process ends (Figure 7.2(b)) shrinking the depletion region width. When the device temperature was varied from 300K to 353K at a constant frequency under reverse bias, the trapped carriers in the p-type depletion layer were thermally excited out. This led to an increase of junction capacitance with increasing temperature. The change in capacitance was sampled at both 10 ms and 20 ms.

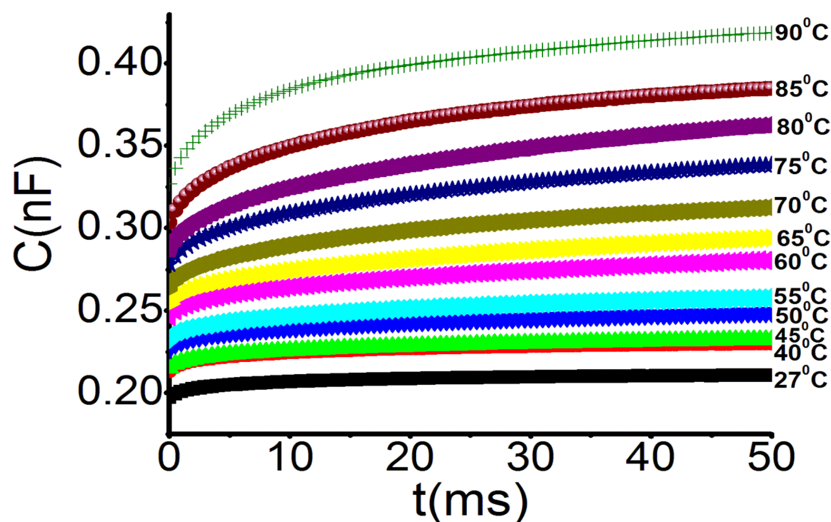


Figure 7.1 Time dependence of the capacitance measured at 100 kHz when a reverse bias (V_r =1V) was applied at time, t = 0 for CdTe solar cells.

To obtain a spectrum tangents are drawn to the curves at the points corresponding to the chosen times, for instance 10 ms and 20 ms, and the slope dC/dt is plotted as a function of temperature. Then by choosing t, τ_p can be determined, which is shown by

(7.5) that corresponds to a definite temperature. By substituting τ_p into (7.11) gives the corresponding values for E_a and σ_∞ with τ_{pl} =10 ms and τ_{p2} = 20 ms and the temperatures T_{sl} and T_{s2} corresponding to the peak values in dC/dt. If σ_∞ is known, then E_a can be found from equation (7.4); if on the other hand, σ_∞ is unknown, by choosing t successively as equal to τ_{pl} and τ_{p2} to get two equations in (7.11) whose solution gives E_a and σ_∞. The concentration of majority carriers N_A is given by (7.12), in which C_p corresponds to the maximum slope.

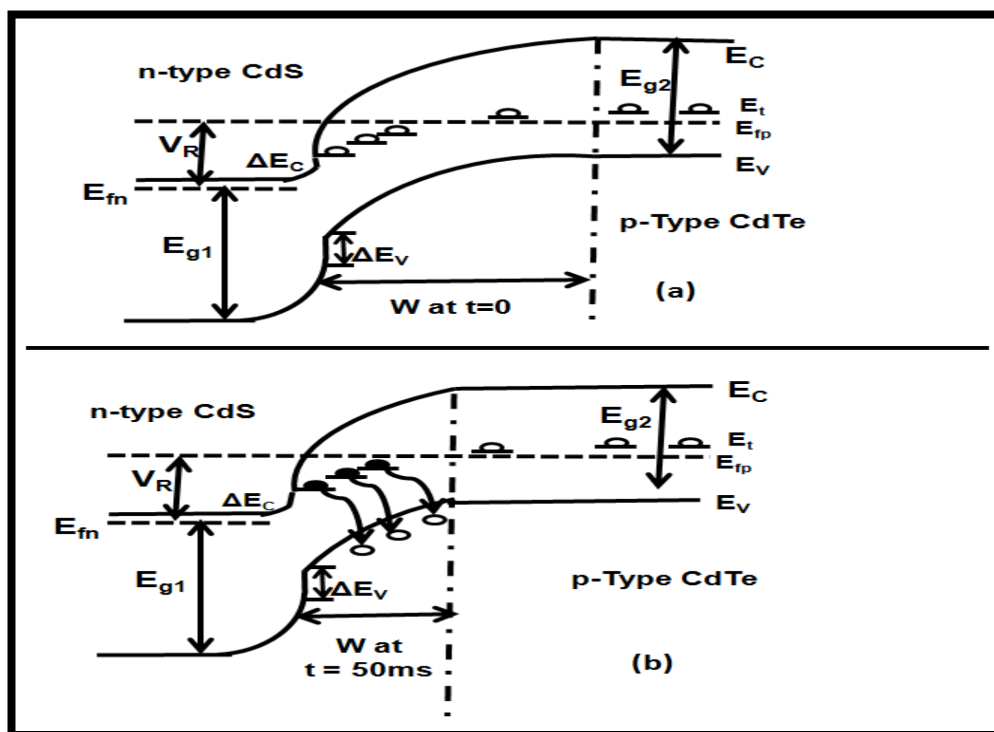


Figure 7.2 Energy band diagram of CdTe solar cell for reverse bias conditions (a) at t=0, (b) at t = 50ms. The symbols represent their usual meanings. ΔE_c and ΔE_v show the discontinuities (offsets) of the conduction and valence bands respectively, W is the depletion width, V_R is the reverse bias voltage, E_{g1} and E_{g2} are the energy band gaps of CdS and CdTe, respectively. E_{fp} and E_{fn} are the quasi Fermi levels and E_t is the trap energy level.

As evident from the TDCS spectrum, with the rate of change of capacitance (Figure 7.3) as a function of temperature, a significant change was observed when T= T_s. In other words, when E_f crosses E_t, the TDCS peak amplitude changes with the steady application of reverse bias, since the peak height is proportional to the number of filled/emptied traps. Typically, this requires the use of emptying times for majority carriers (holes) that are high enough to empty most of the traps. In this study, using a time range from 0 ms to 50 ms, a significant change in peak height was observed. The peaks observed at sampling time 20 ms and 10 ms are shown in Figure 7.3(a) and Figure 7.3(b) respectively. The peaks designated as H1, H2 and H3 indicate that the detected traps were completely emptied within 10 msec (Figure 7.3 (b)). For the next 10-20 msec, there is a significant change in peak height (Figure 7.3(a)) for detected traps. Peaks also shifted with time indicating that the traps are of deep intrinsic/impurity defects. Using this approach, three positive signals in TDCS corresponding to majority traps were observed. The corresponding values of capture cross-section also suggest that they arise from deep level defects. The peak location of majority traps did not change as reverse bias voltages were increased or decreased.

The activation energy is extracted from the peak from TDCS spectra. The temperature of maximum value dC/dt curve, Ts_{11} for H1 at 10 ms gives the estimate of the thermal activation energy of the majority carrier trap energy levels. The total capacitance change around each T_{s11} and T_{s21} for H1 at 10 ms and 20 ms gives the concentration of carriers trapped at that level. Employing the TDCS measurements at 300K deep levels can be detected assuming a maximum detectable thermal emission rate due to time constant. Thus this method demonstrates that the capacitance change due to

emptying of majority-carrier traps in the depletion region can be used to characterize the deep levels.

The trap energy level can be simply estimated from TDCS plot of the reverse bias voltage. Each spectrum in TDCS consists of three peaks representing three deep energy traps H1, H2 and H3 (Figure 7.3). These plots measure activation energy of 0.65 eV for trap H1, 0.52 eV for trap H2 and 0.80 eV for trap H3. The detailed estimated values for the trap levels are listed in Table 7.1.

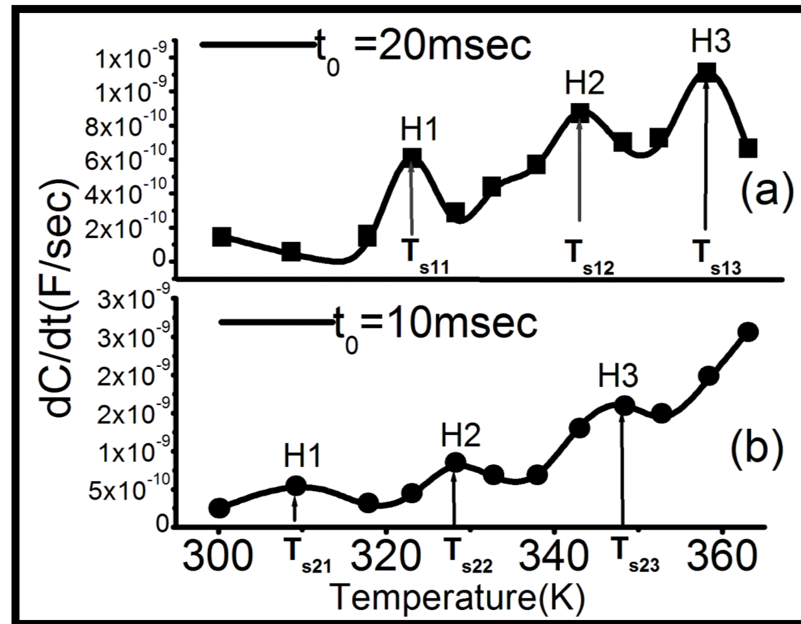


Figure 7.3 Rate of change of capacitance measured at different temperatures at 100 kHz in reverse bias (V_r =1V) for CdTe solar cells.

The defect H1 is attributed to doubly ionized cadmium vacancy (V_{Cd}^{2-}) substitutions with energy level E_v + 0.65 eV and cross- section (σ_t) ~ 3×10^{-13} cm^2. Rakhshani et al. detected this trap in CdTe thin-film solar cells by PICTS [17], with its σ_t ~ 4.8×10^{-13} cm^2. Moreover, Ringel et al. also observed the same defect due to V_{Cd}^{2-} with σ_t ~ 8.2×10^{-16} by DLTS during the annealing process after the $CdCl_2$ dip [24]. Also, this

is consistent with V_{Cd} and/or Cl diffusion from the CdTe surface into the bulk as a result of the 400^0C anneal. Since Cl ions are known to be readily form defect complexes with cadmium vacancies to form deep and shallow levels, it is likely that the E_v+ 0.64 eV trap defects [11, 142].

The H2 seems to be the signature of (trap energy level E_v +0.52 eV and $\sigma_t \sim 1\times10^{-15}$ cm^2) Cu related deep level defect. This is in good agreement with activation energy (494 ± 9) meV determined by Admittance Spectroscopy and also with activation energy (552 ± 10) meV determined by back barrier height, assuming thermionic emission mechanism from current-voltage characteristics [27]. It was shown that the observed peak was a deep level due to Cu and the peak appears when Cu is added to the back contact formation process [15]. Note that the annealed Cu-evaporated back contact with Cu doped ZnTe in carbon conductive paste of CdTe thin-film solar cells are being investigated here. Seymour [10, 20] et al. observed the activation energies 0.52 eV and 0.54eV with cross- sections 7 $\times10^{-12}$ cm^2 and $9\times10^{-12}cm^2$ respectively by using admittance spectroscopy from a number of CdTe solar cells that were with Cu back contact and $CdCl_2$ treatment similar to ours. It is, therefore, reasonable to assume that Cu_i^{2+} is likely to be present in our devices (~0.55eV) as Cu was evaporated during back contact formation. We had reported this trap for Cu evaporated samples earlier [21].

The H3 level with energy value E_v + 0.80 eV and $\sigma_t \sim 4\times10^{-12}cm^2$ obtained in the cells absorber layer was caused by the positive Cd_i^{2+} interstitial defects. Since the deep level associated with doubly charged cadmium vacancy was observed, it may be postulated that vacancy formation was suppressed, and the creation of interstitial favored in our devices. Rakhshani et al. [128] have investigated the trap level with activation

energy (0.88eV) and $\sigma_t \sim 1.1\times10^{-11}cm^2$ in CdTe thin-film solar cells. In an earlier work [21] we also observed this trap level. In addition, Rakhshani et al. [17] verified hole trap with value E_v + 0.80 eV and $\sigma_t \sim 3.9\times10^{-13}cm^2$ by using PICTS. Similarly, studies involving the thermally stimulated conductivity technique [143] revealed that traps in depletion region appeared most frequently in material grown at high Cd pressure.

Table 7.1 Temperature Dependent Values of Various Parameters Determined from C-V characteristics from Figure (7.3)

Trap Level	T_{s1}(K) corr. to peak in dC/dt when t = 10 msec	T_{s2}(K) corr. to peak in dC/dt when t = 20 msec	$N_A(cm^{-3})$	E_a(eV)	$\sigma_\infty(cm^2)$
H1	313	323	$1.4x10^{11}$	0.65	3×10^{-13}
H2	328	343	$2x10^{11}$	0.52	1×10^{-15}
H3	348	358	$0.3x10^{12}$	0.80	4×10^{-12}

From Table 7.1, it was observed that the estimated the carrier concentration in CdTe seems to be lower than the reported in the literature [144] [$N_A = 10^{14}cm^{-3}$]. Although the multiple dopant states are the most fundamental parameters to be controlled in device processing they make it difficult to determine each state's concentration and its corresponding doping level. While a high copper impurity concentration was observed ($N_{Cu} = 10^{17}cm^{-3}$) [145], a much less hole density was reported (10^{14} - $10^{15}cm^{-3}$) [134] for the same samples. Note that published experimental values of p or N_A of thin film CdTe are extracted from C-V measurements. By calculating with equation ($p \sim (\sqrt{N_vN_A/g_A}) \exp(-((E_A-E_V)/2kT))$) [107] and considering $N_V = 1.8 \times10^{18}cm^{-3}$ [27], $N_A = 1.6 \times10^{14}cm^{-3}$, g_A =4, and E_A-E_V = 0.55eV [27] the estimation of $p = 2.2 \times10^{11}cm^{-3}$ is consistent with

experimental value from the calculated data. It also confirms that if Cu is present in interstitial form, p may be few orders lower than the acceptor concentration. Same calculations can be done for doubly ionized vacancy of cadmium. As a result, the band bending at the junction is small due to lower concentration of hole in p-type CdTe solar cell.

The reported defect types, activation energy E_a and capture cross-section σ_∞ in Table 7.2 along with data observed from the TDCS technique have been summarized. Most of the other studies with different techniques revealed that traps related to cadmium vacancy in depletion region appeared most frequently in CdTe material grown at high Cd pressure [11, 17, 22, 25, 26, and 142]. The deep traps related to copper defects appeared due to excess of copper in the back contact [21, 27, and 144]. It can be seen that TDCS results are compatible to other measurement techniques. Since TDCS is rather a simpler technique it can be employed to quickly identify the deep levels in CdTe Solar cell before more extensive techniques like DLTS are used. While other techniques like J-V-T can be employed to identify the deep level defects minor errors can be introduced due to field driven conduction in addition to trap-assisted conduction. Besides, accurate calculation of defect concentration and capture cross-section may not be possible [21]. Therefore, for quickly evaluation of deep defects TDCS seems to be a more effective tool is to be believed.

Table 7.2 Role of Capture Cross-section Energy of Defects Compared With Other Studies in CdTe Solar Cells. The Symbols Carry their Usual Meaning as Defined Earlier

Trap Type	This work (TDCS)		Other Techniques [Ref]	
	Activation Energy, E_a (eV)	Cross-section σ_∞ (cm^{-2})	Activation Energy, E_a (eV)	Cross-section σ_∞ (cm^{-2})
V_{cd}^{2-}	0.65	3×10^{-13}	0.63 (DLTS [22])	1.0×10^{-15}
			0.64 (DLTS [24])	8.2×10^{-16}
			0.65(PICTS [17])	3.0×10^{-13}
			0.64(DLTS [11, 142])	-
Cu_i^{2+}	0.52	1×10^{-15}	0.57(J-V-T [21])	-
			0.50 (AS [95])	8.42×10^{-12}
			0.52-0.54 (AS [144])	$7 - 9\times10^{-12}$
Cd_i^{2+}	0.80	4×10^{-12}	0.89(J-V-T [21])	-
			0.75(DLTS [22])	4.0×10^{-14}
			0.80 (PICTS [17])	3.9×10^{-13}
			0.88 (PICTS [25])	1.1×10^{-11}

7.3 Chapter Summary

TDCS measurement at fixed reverse bias to estimate various trap characteristics from plot of temperature-dependent capacitance transients in n^+-CdS/p-CdTe solar cells have been presented. The activation energies with experimentally measured data have been successfully derived. By using TDCS method, single or multiple defects can found. Three deep level traps using TDCS in CdTe solar cells with copper-evaporated back contacts

were analyzed. Based on the capture cross-section and a literature surveys, The trap energy level E_t = 0.65ev, 0.80eV is attributed due to singly and doubly ionized Cd vacancy and one trap with E_t = 0.52eV is due to Cu-related deep level. The TDCS method is turned out to be superior technique to estimate deep defect characteristics in CdTe solar cells.

CHAPTER 8

CONCLUSIONS AND FUTURE WORK

8.1 Summary

J-V-T measurements of variously processed n^+-CdS/p-CdTe solar cells are presented. The applicability of reverse bias (-1V) generation current (SRH R-G theory) correlate the various "traps" with the experimentally measured activation energies resulting from the plot of ln (J_0T^{-2}) vs. 1000/T have been discussed. The simple J-V-T measurement is a powerful technique for characterizing process reproducibility and establishing process control. It is observed that once the amount of Cu used to form the back contact exceeds a threshold level it diffuses to CdTe layer and forms Cu related substitutional or interstitial defects. By J-V-T theory it is observed that Copper containing contacts initially perform well (copper forms a shallow acceptor in CdTe), but their high temperature performance can be a problem, as the copper under circumstances diffuses through the CdTe layer and forms Cu related substitutional or interstitial defects.

I-V-T and C-V-T measurement at fixed reverse bias to correlate the various traps n^+-CdS/p-CdTe solar cells are also presented. The experimentally measured activation energies from plot of capacitance transients and current transients of variously processed n^+-CdS/p-CdTe solar cells are reported. Based on the literature surveys, the trap energy level with E_t = 0.07-0.10 eV is attributed due to be A- center V_{Cd}–Cl_{Te}. I-V-T and C-V-T techniques turned out to be superior and fast measurement techniques for the defect characterization

Two different Cu containing back contacts by temperature dependent J-V characteristics which further confirmed by the observed frequency dispersion behavior of Cu-related deep level traps are identified. A Cu-related deep level was observed for high Cu containing back contact whereas an intrinsic deep defect level was observed for low Cu containing back contact due to the diffusion of Cu during post-processing annealing. The performance of device made with evaporated-Cu contact is comparable to that of standard Cu-doped devices [33]. The presence of majority carrier traps (Cu-related or intrinsic) contributes differently to the efficiency and degradation of the electronic properties of the CdTe solar cells.

8.2 Future Work

In this work, with the application of small amount of evaporated Cu (20-nm), annealed at 160^{0}C, and with silver and Indium paste as electrodes, devices with reasonably good initial performance have been demonstrated. Furthermore, temperature dependent dark I-V curves trend was observed which suggests that once the amount of Cu used to form the back contact exceeds a threshold level it diffuses to CdTe layer and forms Cu related substitutional or interstitial defects. This is an indication that during long-term stability study; the diffusion of Cu in these devices might also be low, which would hopefully result in a better stability. This reasonably educated speculation should be experimentally verified. In light of this, at Apollo Cells, similar devices using this back-contact recipe have already been fabricated, and the reproducibility is quite good, these devices will be exposed to same conditions, in the near future, to test their stability.

The CdTe thicknesses of the devices studied were 12 μm, which is common for Apollo Solar Cells, and very recently, in a separate project from this thesis work, devices with relatively thinner CdTe (2 - 6μm) with respectable efficiencies were fabricated, using the evaporation of Cu with ZnTe: Cu-doped graphite paste back-contact. In the future, similar devices with this relatively thinner CdTe and that incorporate evaporated-Cu and metal electrodes are under consideration. This back-contact approach that consists of evaporated-Cu is easily controllable and in combination with a thin-CdTe layer will result in significant contribution in lowering the cost of commercialized CdTe solar cells.

APPENDIX

LABVIEW CONTROL PROGRAM

Current-Voltage (I-V), Capacitance – Voltage (C-V) and Capacitance Frequency(C-F) measurements can be automatically controlled by the Labview software. Figures A.1, A.2 and A.3 show their control panels respectively. In I-V characterization, window is designated to observe two parameters, current as a function of total applied voltage on the solar cell. Numbers in the boxes “Start V”, “Stop V” , “Points” indicate that 51 interval points and “Swp Delay” indicate that the delay time are scanned from -1V to 1V with the Compliance 0.1Ampere of the equipment .

Here are two methods to measure the source voltage and measure current to sweep from -1V to 1V and up to 100mA from equipment named as Keithley 236 Electrometer.

Method A.1 (a): Front Panel Controls

Set SOURCE MEASURE to Source V Measure I

Set FUNCTION to Sweep

Set COMPLIANCE to 100mA. On the Data Key Pad, enter in 25 EXP 3 and press ENTER.

Press CREATE and select LINEAR STAIR, press ENTER

Set START as -1V, press ENTER

Set STOP as 1V, press ENTER

Set STEP to 0.01V, press ENTER

Set Delay to 0.1 sec, press ENTER

Set BIAS to 0.0V, press ENTER

Select BEST FIXED RANGE, press ENTER

Press ENTER to SAVE.

Press OPERATE

Press TRIGGER to start sweep

When sweep in complete press RECALL to see data. Use the wheel to scroll through the data points

Method A.1 (b): From computer control

The following commands are as follows

F0,1X This is to set source V measure I for a sweep.

B0,2,0X Set Bias to 0V on 11V range no delay.

G5,0,2X Send Source and Measure value with prefix and suffix with all sweep data

L25e-3,9X Set compliance to 25mA on 100mA range

Q1,1,5,0.1,2,100X Configure sweep of 1V to 5V in 100mV steps with 100msec delay between steps

N1X Enable the OUTPUT

H0X Trigger to start sweep

When sweep is complete, read with GPIB READ. All sweep points will come back with Source and Measure value for each step in the sweep

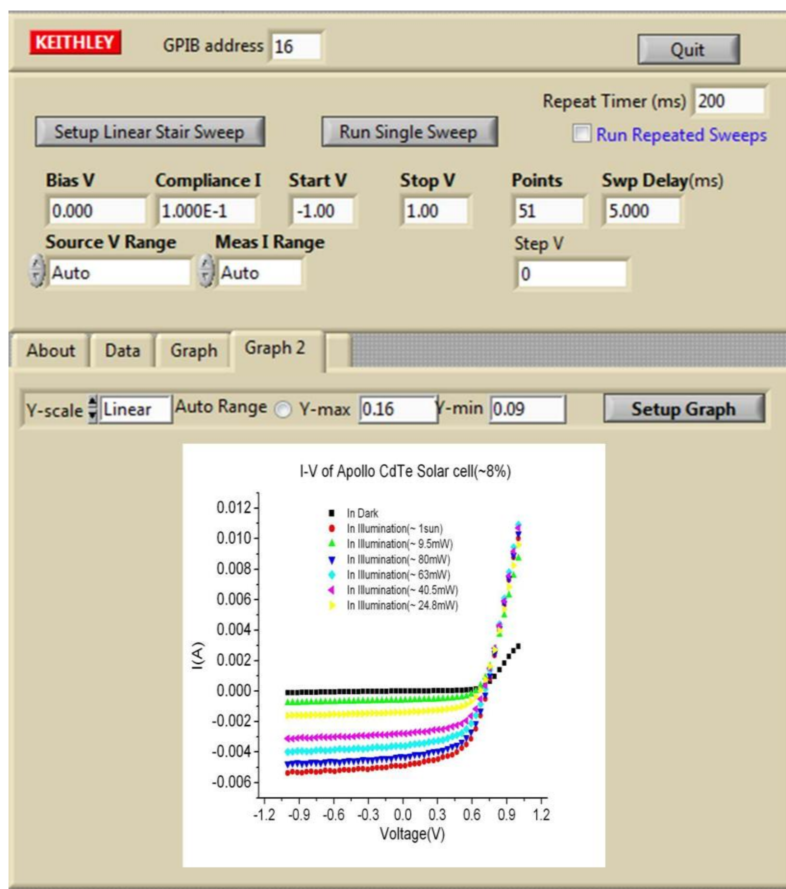


Figure A.1 Control panel window of current-voltage characterization.

In C-V and C-F measurement window, initial input values include range of scanning voltage, sampling points, time delay and resistance.

In C-V characterization, front panel window was designated to observe two parameters, capacitance as a function of bias voltage on the solar cell at a particular frequency. Numbers in the boxes "DC Bias MIMIMUM", " DC Bias MAXIMUM" , "DC Bias STEP" indicate and "SINGLE Freq" indicate that the dc bias are scanned from -1V to 1V with the steps at a particular frequency respectively. The Box named as primary value gives the measured capacitance of the diode and secondary value gives the conductance. The graph shows the behavior of the diode how the capacitance changes with varying dc bias at a fixed frequency.

Given the measured capacitance C, the total bias voltage on the solar cell equals:

$$V_a = V_{dc} + V_{ac}$$

where V_a represents the applied voltage by the voltage source, V_{dc} and V_{ac} represent the dc and ac voltages with internal resistor R respectively. For small signals, V_{ac} is negligible and therefore applied voltage is just the dc bias voltage.

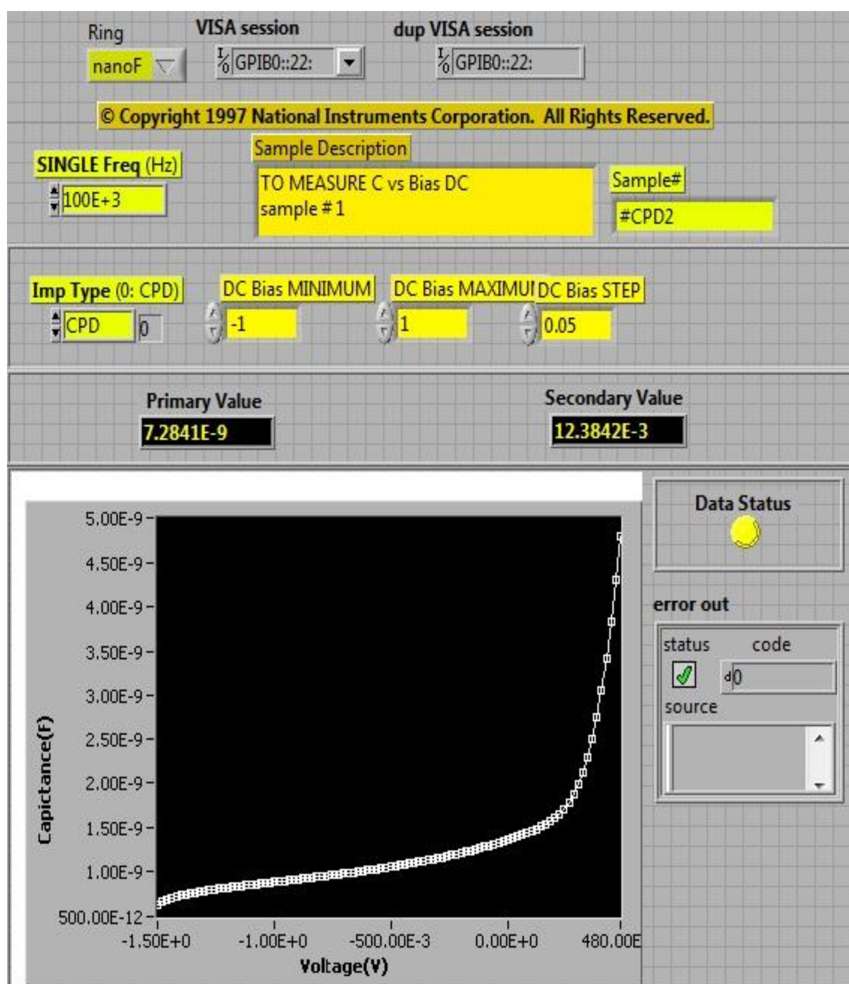


Figure A.2 Control panel window of capacitance-voltage characterization.

Figure 3 shows that the front panel window of capacitance versus frequency measurements. In C-F characterization, the boxes named as “Start Freq”, “Stop Freq”, “Number per decade” indicate that the interval points are scanned from -1V to 1V with a fixed applied dc bias voltage.

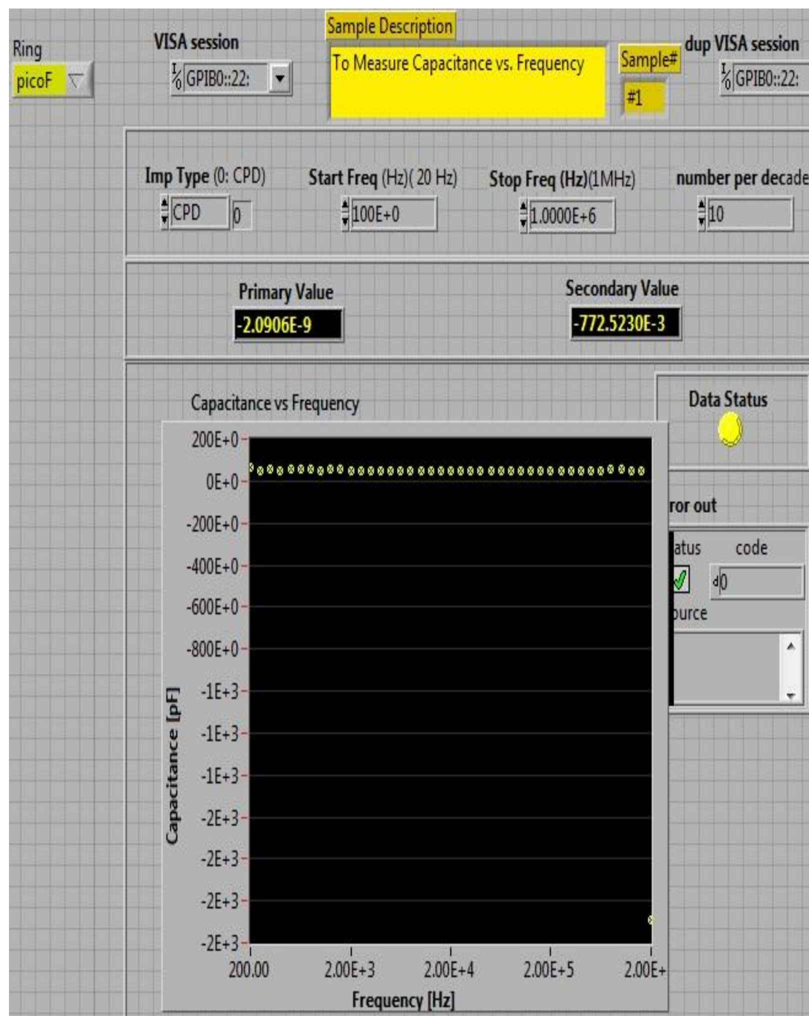


Figure A.3 Control panel window of capacitance-frequency characterization.

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