ABSTRACT

TiN/HfO_2/SiO_2/Si GATE STACKS RELIABILITY: CONTRIBUTION OF HfO_2 AND INTERFACIAL SiO_2 LAYER

by
Nilufa Rahim

Hafnium Oxide based gate stacks are considered to be the potential candidates to replace SiO_2 in complementary metal-oxide-semiconductor (CMOS), as they reduce the gate leakage by over 100 times while keeping the device performance intact. Even though considerable performance improvement has been achieved, reliability of high-κ devices for the next generation of transistors (45nm and beyond) which has an interfacial layer (IL: typically SiO_2) between high-κ and the substrate, needs to be investigated. To understand the breakdown mechanism of high-κ/SiO_2 gate stack completely, it is important to study this multi-layer structure extensively. For example, (i) the role of SiO_2 interfacial layers and bulk high-κ gate dielectrics without any interfacial layer can be investigated separately while maintaining same growth conditions; (ii) the evolution of breakdown process can be studied through stress induced leakage current (SILC); (iii) relationship of various degradation mechanisms such as negative bias temperature instability (NBTI) with that of the dielectric breakdown; and (iv) a fast evaluation process to estimate statistical breakdown distribution.

In this dissertation a comparative study was conducted to investigate individual breakdown characteristics of high-κ/IL (ISSG SiO_2)/metal gate stacks, in-situ steam generated (ISSG)-SiO_2 MOS structures and HfO_2-only metal-insulator-metal (MIM) capacitors. Experimental results indicate that after constant voltage stress (CVS) identical degradation for progressive breakdown and SILC were observed in high-κ/IL and SiO_2-

only MOS devices, but HfO_2-only MIM capacitors showed insignificant SILC and progressive breakdown until it went into hard breakdown. Based on the observed SILC behavior and charge-to-breakdown (Q_{BD}), it was inferred that interfacial layer initiates progressive breakdown of metal gate/high-κ gate stacks at room temperature. From normalized SILC ($\Delta J_g/J_{g0}$) at accelerated temperature and activation energy of the time-to-breakdown (T_{BD}), it was observed that IL initiates the gate stack breakdown at higher temperatures as well. A quantitative agreement was observed for key parameters of NBTI and time dependent dielectric breakdown (TDDB) such as the activation energies of threshold voltage change and SILC. The quality and thickness variation of the IL causes similar degradation on both NBTI and TDDB indicating that mechanism of these two reliability issues are related due to creation of identical defect types in the IL.

CVS was used to investigate the statistical distribution of T_{BD}, defined as soft or first breakdown where small sample size was considered. As T_{BD} followed Weibull distribution, large sample size was not required. Since the failure process in static random access memory (SRAM) is typically predicted by the realistic TDDB model based on gate leakage current (I_{FAIL}) rather than the conventional first breakdown criterion, the relevant failure distributions at I_{FAIL} are non-Weibull including the progressive breakdown (PBD) phase for high-κ/metal gate dielectrics. A new methodology using hybrid two-stage stresses has been developed to study progressive breakdown phase further for high-κ and SiO_2. It is demonstrated that VRS can be used effectively for quantitative reliability studies of progressive breakdown phase and final breakdown of high-κ and other dielectric materials; thus it can replace the time-consuming CVS measurements as an efficient methodology and reduce the resources manufacturing cost.

$TiN/HfO_2/SiO_2/Si$ GATE STACKS RELIABILITY: CONTRIBUTION OF HfO_2 AND INTERFACIAL SiO_2 LAYER

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A Dissertation
Submitted to the Faculty of
New Jersey Institute of Technology
in Partial Fulfillment of the Requirements for the Degree of
Doctor of Philosophy in Electrical Engineering

Department of Electrical and Computer Engineering

January 2011

APPROVAL PAGE

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Nilufa Rahim, and Durga Misra, "Correlation of Negative Bias Temperature Instability and Breakdown in HfO_2/TiN Gate Stacks", ECS Transactions, 28(2), pp. 323-330, 2010.

Naser A. Chowdhury, X. Wang, G. Bersuker, C. Young, Nilufa Rahim, and Durga Misra, "Temperature Dependent Time-to-Breakdown (T_{BD}) of TiN/HfO_2 n-channel MOS Devices in Inversion", Microelectronics Reliability, 49(5), pp. 495-498, 2009.

Nilufa Rahim, and Durga Misra, "Temperature Effects on Breakdown Characteristics of High-κ Gate Dielectrics with Metal Gates", IEEE Transactions on Device and Materials Reliability, 8 (4), pp. 689-693, 2008.

Nilufa Rahim, and Durga Misra, "$TiN/HfO_2/SiO_2/Si$ Gate Stack Breakdown: Contribution of HfO_2 and Interfacial SiO_2 layer", Journal of the Electrochemical Society, 155 (10), pp. G194-G198, 2008.

Nilufa Rahim, and Durga Misra, "Role of Hydrogen in $Ge/HfO_2/Al$ Gate Stacks Subjected to Negative Bias Temperature Instability", Applied Physics Letters, 92(2), pp. 023511, 2008.

Naser A. Chowdhury, D. Misra, and Nilufa Rahim, "Negative bias temperature instability in TiN/Hf-Silicate based gate stacks", International Journal of High Speed Electronics and Systems, 17(1), pp. 127-141, 2007.

Durga Misra, Reenu Garg, Purushothaman Srinivasan, Nilufa Rahim, and Naser A.Chowdhury, "Interface Characterization of high-κ dielectrics on Ge substrate", Materials Science in Semiconductor Processing, 9 (4-5 SPEC ISS.), pp. 741-748, 2006.

Nilufa Rahim, and Durga Misra, "Low Voltage SILC Analysis for High-κ/Metal gate Dielectrics", Advanced Gate Stack, Source/Drain, and Channel Engineering for Si-Based CMOS 5: New Materials, Processes, and Equipment, ECS Transactions, 19 (1), pp. 283-287, 2009.

Nilufa Rahim, and Durga Misra, "NBTI Behavior of $Ge/HfO_2/Al$ Gate Stacks", 46th annual Proceedings of the 2008 IEEE international reliability physics symposium, pp. 653-654, 2008.

Nilufa Rahim, and Durga Misra, "Breakdown Characteristics of High-κ Gate Dielectrics With Metal Gate", International Symposium on Dielectrics for Nanosystems 3: Materials Science, Processing, Reliability, and Manufacturing, ECS Transactions, 13(2), pp. 91-97, 2008.

Nilufa Rahim, Naser A. Chowdhury, and Durga Misra, " Role of Bulk HfO_2 and Interfacial layer in Breakdown Characteristics of $TiN/HfO_2/SiO_2/Si$ Gate Stacks", 5th International Symposium on Physics and Technology of High-κ gate Dielectrics, ECS transactions, 11(4), pp. 629-638, 2007.

Nilufa Rahim, and Durga Misra, "Low Voltage SILC Analysis for High-κ/Metal gate Dielectrics", Advanced Gate Stack, Source/Drain, and Channel Engineering for Si-Based CMOS 5: New Materials, Processes, and Equipment, 215th Electro Chemical Society Conference, San Francisco, CA , May 24- May 29, 2009.

Nilufa Rahim, and Durga Misra, "Elevated Temperature Breakdown Study for High-κ/Metal Gate Stacks", The Dana Knox Student Research Showcase, NJIT, Newark, NJ, April 8,2009.

Nilufa Rahim, and Durga Misra, "NBTI Behavior of Ge/HfO_2/Al Gate Stacks", 46th annual IEEE international reliability physics symposium, Phoenix, AZ, April 2008.

Nilufa Rahim, and Durga Misra, "Breakdown Characteristics of Metal Gate/HfO_2 based Multi-layer Gate Stacks", National Science Foundation GK-12 Annual Meeting, NSF Headquarter, Arlington, VA, Feb. 29, 2008.

Nilufa Rahim, Naser A. Chowdhury and Durga Misra, "Role of Bulk HfO_2 and Interfacial layer SiO_2 Layer in Breakdown characteristics in TiN/ HfO_2/SiO_2/Si Gate stacks", 212th Electro Chemical Society Conference, Washington DC, Oct. 7-Oct. 12, 2007.

Nilufa Rahim, Naser A. Chowdhury and Durga Misra, "Role of Experimentally Observed Defect Energy Levels in Carrier Transport and Charge Trapping in Metal Gate/Hf-SilicateBased Gate Stacks", 210th ECS conference, Cancun, Mexico, Oct. 29- Nov. 3, 2006.

To my family

ACKNOWLEDGMENT

I am heartily thankful to my dissertation advisor, Dr. Durgamadhab Misra, whose supervision, encouragement, and support throughout this research work enabled me to develop an understanding of the subject. He not only guided me through when I needed assistance in ideas, also helped me enormously to be independent. I am very much grateful to Dr. Ernest Wu for guiding me during my Co-Op at IBM. I was able to learn a lot from him and most importantly I was motivated by him immensely. I also want to thank all my committee members, Dr. Haim Grebel, Dr. Leonid Tsybeskov, Dr. Marek Sosnowski and Dr. Roland Levy for their valuable suggestions.

This research work was supported by various funding source as NSF, ECE department and C2PRISM of NJIT, IBM at Vermont. I am expressing my gratitude for supporting my work.

I am indebted to Dr. John Aitken, my manager during my Co-Op at IBM, for his continuous inspiration, encouragement and support. My colleagues and friends at NJIT have always given me technical and moral support during this time of research work. I want to take this opportunity to thank Amrita Banerjee, Dr. Naser Chowdhury and Dr. Purushothaman Srinivasan in this regard.

Lastly, I am extremely thankful to my family specially my parents who have taught me to dream. Heartfelt gratitude to my husband, Abdullah Ahmed who supported me single handedly, my sister, Selina Mala for her support. Finally, thanks to my son, Shayaan Ahmed, who was my most inspiration in this journey.

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LIST OF SYMBOLS

K	Dielectric constant
B	Weibull slope, Beta
η	Characteristic life (Eta)
Å	Angstrom (10^{-10} meters)
Γ	Voltage acceleration factor, Gamma
k_B	Boltzmann constant
φ_{ms}	Work function difference
φ_t	Trap energy
ψ_s	Surface potential

CHAPTER 1

INTRODUCTION, MOTIVATION AND OBJECTIVES

1.1 Introduction

In today's world, microelectronics became an integral part of our lives. So, continuous effort in microelectronics research is essential to achieve higher performance and functionality of various electronic devices that eventually will improve quality of life in the world. Metal-oxide-semiconductor field-effect transistor (MOSFET) is the basic device in integrated circuit (IC). Continuous scaling of MOSFET for the past few decades has followed an evolutionary path. The supply voltage, V_{dd}, channel length and physical thickness of dielectrics are scaled to achieve higher circuit speed/performance, increased bit density and lower power dissipation which tremendously improve the computing power at a reasonable cost.

To meet the requirements of diverse applications, MOSFETs have been categorized into different families, such as high performance (HP) logic family (i.e. microprocessors), low operating power (LOP) logic family (i.e. notebook) and low standby power (LSTP) logic family (i.e. cell phone). High performance logic devices require smaller threshold voltage (V_{th}), shorter channel length and thin dielectric for fast switching speed. But for LSTP logic family, power dissipation is the main concern which requires low standby leakage current. The scaling of devices via thinning of gate dielectric and shortening of channel length causes substantial gate tunneling current and subthreshold leakage current. For LSTP logic devices, direct tunneling current has become a significant portion of leakage current for sub 2 nm oxide [1]. Based on the International Technology Roadmap for Semiconductor (ITRS) 2009 report, the physical

gate length of the transistor have been shrunk below 45-nm node and equivalent oxide thickness (EOT) of the dielectric scaled down to less than 0.9 nm [2].

Table 1.1 LSTP Technology Requirements from ITRS 2009 Winter Meeting [1]

Year of production	2010	2013	2016	2019	2022
Technology node	45	32	22	16	11
Physical gate length (nm)	27	20	15.3	11.7	8.9
V_{dd} (Low operating power supply voltage)	0.95	0.80	0.75	0.65	0.60
Off state current under high drain bias (nA/um) at 25^0C	0.1	0.1	0.1	0.1	0.1

Replacement materials for the gate dielectric were expected below 90 nm to maintain the pace of Moore's Law. However, the widespread adoption of channel strains engineering postponed gate dielectric replacement by a few generations. Strained silicon boosted the transistor performance and power consumption to maintain progress without the introduction of revolutionary materials. But thinning of oxynitride, or SiON, the current gate dielectric is at the end of the road. With SiON providing only about a 50 percent improvement in dielectric constant (κ), a fundamental shift in materials was required. Further scaling of SiON would create unacceptably high gate leakage current and reduce device reliability. The 1-nm-thick layer of SiON, required for 45-nm device targets, is essentially just three atomic layers thick. Not only is leakage a huge problem, but there is no margin left for thickness variation. The revolution of new material (high-κ/metal gate) has solved this problem. The advantage of using a high-dielectric-constant material is that it has a greater dielectric constant (κ) than SiO_2 (k_{SiO2} = 3.9) and thus can

afford larger physical thickness to minimize leakage while maintaining similar capacitance values. But the new dielectric material needs to satisfy the minimum requirements for transistor application. Some of these requirements are listed in the table below [1.2].

Table 1.2 Minimum Requirements of High-κ Gate Dielectric

1. Higher permittivity than SiO_2 and oxynitride ($9 \leq \kappa \leq 25$).
2. Larger bandgap and conduction band offset.
3. Lower leakage current than SiO_2 for similar EOT.
4. Thermodynamically stable on Si.
5. Good interface quality with low interface states ($\leq 5 \times 10^{10}$ eV/cm^2).
6. Good reliability.

The research on high-k materials as the new gate dielectric started off with Tantalum Oxide (Ta_2O_5) and Strontium Titanate ($SrTiO_3$), as these materials were already studied for DRAM applications [3,4]. As the research for new dielectric material continued, several other oxides have been proposed such as Titanium Oxide (TiO_2), Aluminum Oxide (Al_2O_3), Yttrium Oxide (Y_2O_3), Zirconium Oxide (ZrO_2), Hafnium Oxide (HfO_2) [5-7] etc. to replace SiO_2. Among these high-k dielectrics, HfO_2 has been considered as the potential candidate because of various reasons; such as 1) high dielectric constant of ~25-30 (~6-7 times that of SiO_2), 2) energy band gap of 5.68eV, though much lower than SiO_2 but with band offsets greater than 1eV (1.5eV for electron and 3.4eV for holes), 3) free energy of reaction with Si is about 47.6Kcal/mol at 727^{o}C making it more stable material on Si substrate in comparison to other high-κ dielectrics,

4) unlike other silicides, silicide of Hf can be easily oxidized [8] to form HfO_2. All these properties of HfO_2 make it an attractive alternative for SiO_2.

In high-κ HfO_2 gate stacks, SiO_2-rich interfacial layer (IL) which is between the Si substrate and the high-κ layer is needed to facilitate the growth of the high-k layer, as well as attain sufficient channel mobility. This interfacial layer forms either as a result of oxidizing growth conditions [9] or because they are intentionally grown as nucleation layers before high-κ deposition [10]. For oxidizing growth condition, oxygen (O) is released and diffused to Si during HfO_2 deposition. This O release forms thick bottom interface SiOx that severely limits scaling. It was also proven by transmission electron microscopy (TEM) and EOT that this bottom interface SiOx grows uncontrollably [11-14].

There are manifold advantages of intentionally grown SiO_2 interfacial layer. First, the thickness and quality of this SiO_2 IL can be controlled, which would eventually help in gate stack EOT scaling. Second, the use of an oxide bottom layer enables HfO_2 nucleation with almost no barrier, linear growth rate, growth at constant density, and the most two-dimensionally continuous HfO_2 films [10]. So, interfacial SiO_2 is essential for the ease of nucleation of HfO_2 on Si. Also, the presence of this interfacial layer of SiO_2 improves carrier mobility and reduces positive bias temperature instability (PBTI).

However, these high-κ materials exhibit a higher defect density compared to SiO_2, aggravating some major device reliability issues including the bias temperature instability, the reduction in channel mobility, time dependent dielectric breakdown, and hot carrier induced degradation etc for the complete gate stack. The knowledge of stress induced defects, charge to breakdown can improve the understanding of their effects on

device reliability, as reliability remains to be the most critical factor to hold back its successful incorporation into the mainstream commercial intergraded circuits [15-18].

1.2 Motivation and Approach

The high-k material currently being considered for gate dielectric applications results in a multilayer structure that includes a SiO_2-like layer either spontaneously or intentionally formed at the interface [19]. A schematic of the gate stack is shown in Figure 1.1 where the interfacial layer was intentionally formed. The reliability of high-k gate dielectric stacks is influenced by both interfacial layer and high-κ layer. Stress induced breakdown is one of the vital issues of the reliability of the high-κ gate stacks. The difficulty in the breakdown study of the gate stack arises as the potential drop/electric field across interfacial and high-κ layers are different due to the differences in the value of the dielectric constant, κ and thickness [20]. This, along with the differences in their respective atomic structures [21], leads to the difference in the degradation in IL and high-κ layer as the stress bias is applied. It was also observed from transistor electrical characteristics and high resolution chemical and spectroscopic analysis that the high-k film modifies the stoichiometry of the underlying SiO_2 layer by rendering it oxygen deficient [22]. This oxygen vacancy may be responsible to induce a higher density of fixed charges in the IL associated with the Si-Si defects. The mechanism of device degradation under constant voltage stress of both polarities is still under debate due to the lack of techniques to separate the traps in the interfacial and the high-k layer. So, this research attempts to explore the gate stack in terms of its long term reliability which

would help its inclusion in future CMOS devices. More emphasis was given to identify the weak link between high-k layer and SiO_2-like IL.

To understand the breakdown characteristics of high-κ/SiO_2 gate stack, this work has followed an approach by investigating two other control structures along with the gate stack: one with only SiO_2 and other with bulk high-κ gate dielectric without any interfacial layer, while maintaining identical growth conditions and thickness as the gate stack. The high-κ dielectric without an interfacial layer was achieved by using a metal-insulator-metal (MIM) structure. The test structures are shown in Figure 1.2.

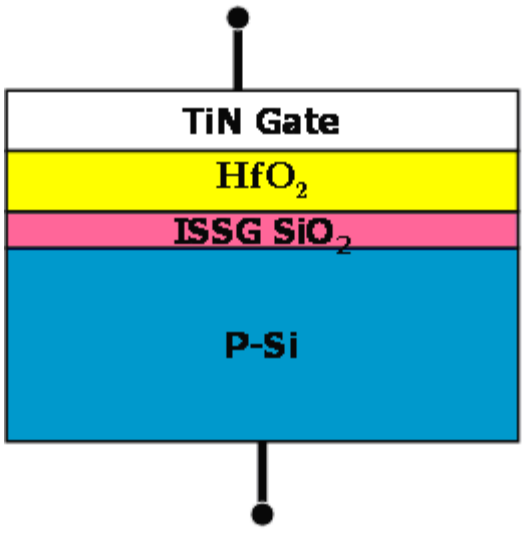


Figure 1.1 TiN gate with HfO_2/In Situ Steam generated (ISSG) SiO_2 on p-Si.

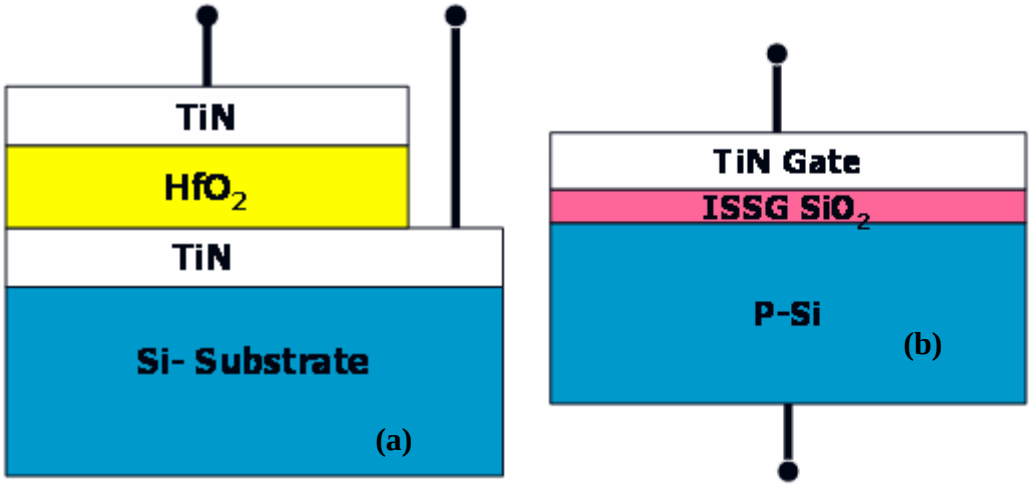


Figure 1.2 Two test structures to study breakdown characteristics (a) Metal-Insulator-Metal (MIM) capacitor with HfO_2 and (b) TiN gate with ISSG SiO_2.

This experimental design has enabled to understand the contribution of SiO_2 interfacial layers and bulk high-κ gate dielectrics in terms of the detail degradation and breakdown behavior of the composite gate stack.

1.3 Objectives

For high-κ /metal gate stacks, two important reliability issues relating to bulk traps are time dependent dielectric breakdown (TDDB) and stress-induced leakage current (SILC). Also, Negative bias temperature instability (NBTI) is a cause of concern for long term reliability where both bulk and interface are degraded. A brief description of these degradation mechanisms and their impact on reliability are mentioned below.

1.3.1 Time Dependent Dielectric Breakdown (TDDB)

When a voltage is applied across the gate oxide, a measurable tunneling current will flow if the gate voltage (V_g) is high enough and/or the oxide is thin enough. For thick oxides at fields above about 7 MV/cm the current is controlled by Fowler-Nordheim tunneling

through the triangular barrier [23-24], while for thin oxides (t_{ox} <3 nm) at voltages below about 3 V (corresponding to the barrier height between n-type silicon and SiO_2) the current is due to direct quantum mechanical tunneling. Electrons (or holes) flowing across the oxide will trigger several processes depending on their energy. At least three defect generation mechanisms have been identified: The first two, impact ionization and anode hole injection, occur at higher voltages and lead to hole trapping and hole-related defect generation [25-26] as the stress with time continues. The lowest-energy process so far identified, which dominates at the voltages where present MOSFETs operate, is the so-called trap creation process attributed to hydrogen release [27-28] or hole injection [29] from the anode. This process continues in the subthreshold region even at operating voltages down to 1.2 V or lowers [30-32]. These defects buildup (hydrogen or holes), form a conduction path between cathode and anode and eventually breaks down the oxides destructively. This catastrophic electrical breakdown is known as time dependent dielectric breakdown (TDDB).

1.3.2 Stressed-Induced Leakage Current (SILC)

Besides the as-deposited defects, additional bulk traps in high-κ gate stacks are created during constant voltage stress (CVS), leading to dielectric breakdown when a critical trap density is reached. These generated traps give rise to stressed-induced leakage current (SILC) through trap assisted tunneling even long before breakdown [33]. For high-κ gate stacks, especially nFETs show large SILC during positive bias temperature which eventually affects proper detection of breakdown time as well.

1.3.3 Negative Bias Temperature Instability (NBTI)

Negative bias temperature instability (NBTI) occurs in p-channel MOS devices stressed with negative gate voltages at elevated temperatures. The detrimental effects of NBTI on devices are threshold voltage (V_T) increase, absolute ‘‘off’’ current I_{off} increase and absolute drain current (I_{Dsat}) and transconductance (g_m) decrease. Typical stress temperatures lie in the 100– 250 °C range with oxide electric fields typically below 6 MV/cm, i.e., fields below those that lead to hot carrier degradation. Such fields and temperatures are typically encountered during burn in, but are also approached in high performance ICs during routine operation. Either negative gate voltages or elevated temperatures can produce NBTI, but their combined action produces a stronger and faster effect. V_T shifts due to NBTI has now become an important reliability concern for both digital and analog CMOS circuits. This is primarily due to the scaling of gate oxide for digital circuits without corresponding scaling of their supply voltages. So, the devices are exposed to moderately high electric field [34].

For various applications (i.e. automotive industry), it is possible that the operating temperature of semiconductor device will be much higher than room temperature. The above mentioned physical degradation mechanisms (TDDB, NBTI and SILC) will be accelerated with this temperature increase. So, a basic understanding of these degradation phenomena at elevated temperature is fundamental to allow accurate reliability predictions.

The objectives of this research are—

1. to critically and comprehensively examine the dielectric breakdown mechanism (specially, time dependent dielectric breakdown, TDDB) of the high-κ/IL gate stack on Si at both room and elevated temperatures.

2. to estimate the lifetime of these stacks at operating voltage from experimental results.

3. to investigate negative bias temperature instability(NBTI).

4. to probe into the origin of low voltage stress-induced leakage current (SILC).

5. to correlate NBTI, LV-SILC and TDDB effects for a comprehensive reliability model.

6. to develop methodology for investigating gate dielectric integrity.

1.4 Dissertation Organization

Chapter 2 discusses the reliability study of high-κ/metal gate devices from literature focusing on breakdown. Recent work involving MIM capacitors with high-κ and past research on thin SiO_2 reliability have also been discussed.

The fabrication process for high-κ/IL ($TiN/HfO_2/SiO_2/Si$) MOS devices, MIM capacitors and control SiO_2 devices used in the present work has been described in Chapter 3. The electrical characterization set up and details of the measurement procedures for this research are also discussed here.

Chapter 4 deals with the breakdown mechanisms of metal gate/high-κ/IL based gate stacks at room temperature. The roles of IL and high-κ layer in TDDB are determined from sets of TiN/HfO_2 based gate stacks, SiO_2-only MOS structures and HfO_2-only MIM capacitors. Four different degradation regimes i) Defect generation, (ii) Soft breakdown (SBD), (iii) Progressive breakdown (PBD) and (iv) Hard breakdown (HBD) under constant voltage stress (CVS) for HfO_2/SiO_2 gate stacks were discussed.

For accurate estimation of operating voltage extrapolation, it is required that time dependent breakdown study be evaluated at an elevated temperature. Hence, this chapter also expands the discussion on basic understanding of temperature dependence of high-κ/IL gate stack breakdown by investigating the response of the individual layers at elevated temperature.

Chapter 5 talks about the origin of low voltage stress-induced leakage current (SILC) and correlates to breakdown of the gate dielectric. The initiation of breakdown process can be understood by studying the low voltage SILC growth as a function of stress voltage. Then the issues of negative bias temperature instability (NBTI) to explore the traps formation and how it impacts the device degradation were also discussed. Also, a correlation of NBTI and TDDB is presented.

Chapter 6 narrates the new hybrid 2 step stress methodology developed to study progressive breakdown and final failure distribution of high-κ/IL gate stack and also thick and thin single layer SiO_2 dielectric. This chapter presents extensive experimental results of progressive breakdown time (T_{PBD}) and final failure time (T_{FAIL}) by voltage ramp stress (VRS) and compared it with traditional constant voltage stress. It has been shown that VRS method can be very useful and efficient to study non-Weibull T_{FAIL} distribution and thus save significant time and manufacturing cost.

Chapter 7 gives a summary of this research and a brief discussion on future work.

CHAPTER 2

RELIABILITY ISSUES OF HIGH-K DIELECTRICS: CURRENT STATUS

2.1 Introduction

Major efforts have been invested to replace SiO_2 by high-κ gate dielectrics. Promising results in terms of equivalent oxide thickness (EOT), leakage current reduction and integration have been obtained with SiO_2/high-κ stacks [35]**.** Except at very low fields, the generation of traps in the dielectric is the most important aspect of degradation prior to breakdown. The dielectric reliability of these stacks (high-κ/interfacial SiO_2) is evaluated by measuring time-to-breakdown (T_{BD}) during constant voltage stress (CVS) or constant current stress (CCS). The degradation mechanisms in double-layer stacks might be quite different from single layer degradation and the material properties of high-κ dielectrics might allow for additional physical mechanisms [35]. Besides, several mechanisms may be taking place at the same time during stress. The microscopic origin of the degradation occurring in these layers is not well understood yet. It has been claimed by Torii *et al.* [36] that the hole-injection-induced release of hydrogen from Si-H terminations causes IL (interfacial layer) breakdown. This mechanism also accelerates negative bias temperature instability (NBTI).

For ultra thin oxides (SiO_2) with poly gate, very strong T_{BD}/Q_{BD} temperature dependence has been found for thin oxides as compared to thick oxides [25, 37-42] shown in figure 2.1. As the gate stack considered for high-κ has an interfacial layer of thin SiO_2, it is speculated that there will be strong T_{BD}/Q_{BD} temperature dependence for high-κ/IL gate stack as well. So, to evaluate the reliability of MOS devices with this

new dielectric stack, it is imperative to look into critical reliability issues such as TDDB, NBTI, and stress-induced leakage current (SILC) at both room and elevated temperatures. Additionally, a correlation between various degradation mechanisms need to established.

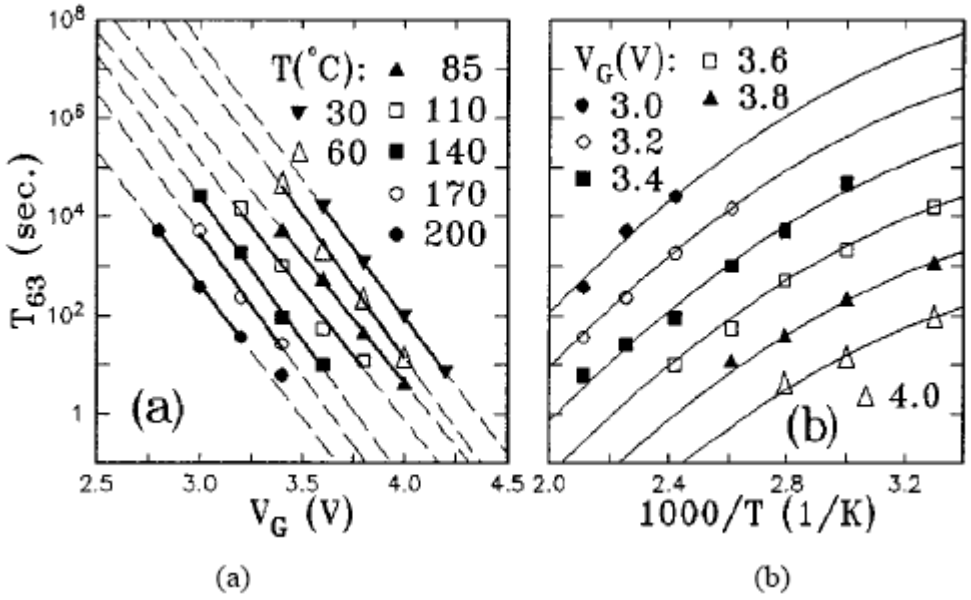


Figure 2.1 (a) T_{BD} versus V_G and (b) T_{BD} versus temperature for 2.15-nm oxides (SiO_2) using p+poly/n-Si capacitors (+ V_G) [43].

To study breakdown, issues such as soft breakdown, hard breakdown, the physical and chemical nature of the interface layer and the bulk high-κ layer, polarity dependence due to asymmetric band structure, charging effect by pre-existing traps, thickness dependence, and area scaling are critical for the accurate reliability projection of this new dielectric material.

2.2 Breakdown Behaviors of HfO_2 under DC Stress

2.2.1 Trap Generation in Bulk Oxide

Various temperature dependent leakage current and threshold voltage instability measurements have been performed to explain the physical origin of electron traps in Hf-based dielectrics [44]. From V_t instability, an equilibrium of electron tunneling from channel to traps and detrapping by Frenkel-Poole conduction can be explained. From this F-P model, the extracted trap energy was found to be 0.35eV. There have been reports of different trap energy levels present in the bulk Hf-oxide varying from 0.35eV to 1.5eV from HfO_2 conduction band. The source of these defects were claimed to be oxygen vacancy related defects. [45].

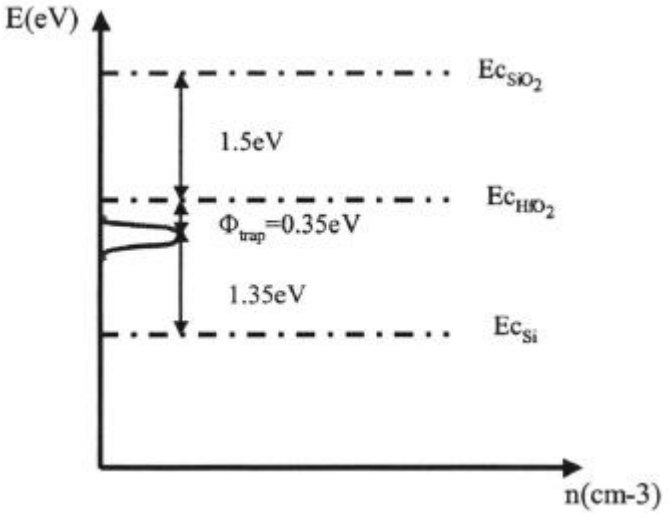


Figure 2.2 Fermi-derivative energy distribution of the traps. Here trap energy was found to be φ_t=0.35eV [44].

2.2.2 Stress Induced Leakage Current (SILC)

It was first reported in the early 1980s that currents measured on thin oxides (4-5 nm in thickness) at low applied electric fields increased after stressing at high fields [46]. The low-field current measurements were performed at low voltages, referred to as the direct tunneling (DT) regime, as illustrated in Figure 2.3 (a). The DT current is produced by electrons tunneling from the cathode contact to the anode contact without entering the oxide conduction band. The stressing was performed at higher fields where the electrons tunneled first into the oxide conduction band before entering the anode [as shown in Figure 2.3 (b). This latter type of tunneling phenomenon is called Fowler-Nordheim (FN) tunneling. It was assumed that the increase in the DT current was caused by oxide film deterioration due to the presence of hot electrons in the oxide conduction band and related to the presence of positive oxide charges generated near the anode during FN stress [47].

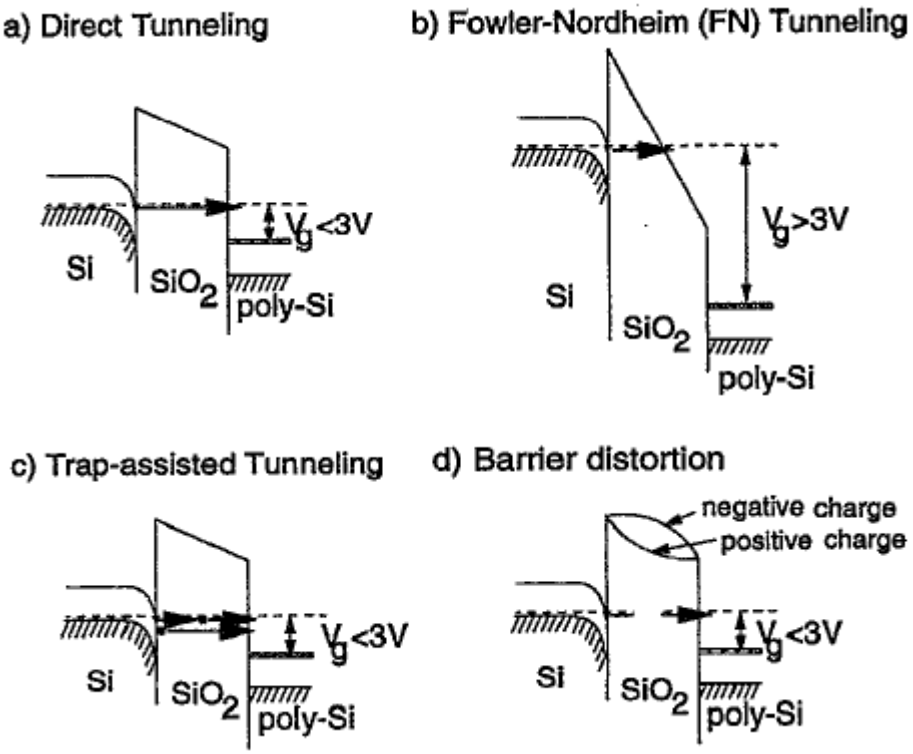


Figure 2.3 Schematic energy-band diagram showing (a) direct tunneling of electrons from the cathode to the anode contact, (b) Fowler-Nordheim tunneling of electrons from the cathode to the bottom of the SiO_2 conduction band with subsequent ballistic transport through the oxide to the anode, (c) two examples of trap-assisted tunneling in the direct tunneling regime including the use of both interfacial and bulk oxide sites, and (d) direct tunneling with barrier (field) distortion caused by trapped negative and positive oxide charges [47].

This current in the DT regime is known as stress-induced leakage current (SILC) shown above in Figure 2.4. Many different models are being used to explain SILC. Rofan *et al.* have proposed that SILC is caused by interface-state generation [48-49], Dumin *et al.* claim that it is due to bulk-oxide electron-trap generation [50] .Also, the positive charge model with the charges due to trapped holes injected from the anode was reported [51-53].

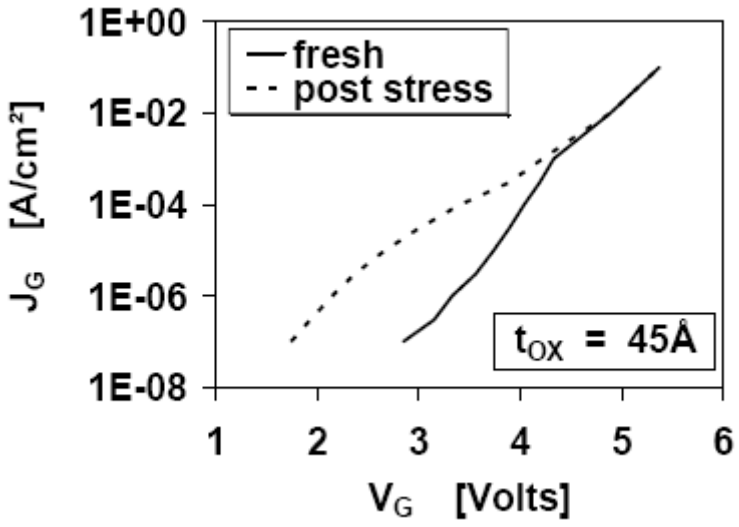


Figure 2.4 Fresh and post ramp-stress I-V characteristics for 4.5nm NMOS oxides [47].

Later DiMaria *et al.* [47] took an attempt to correlate all different possibilities of SILC and showed that the SILC can be best explained by the generation of neutral electron traps in the oxide layer. These sites allow more SILC to flow through the oxide layer by acting as "stepping stones" for tunneling carriers. This phenomenon is often referred to as trap-assisted tunneling [Figure 2.3 (c)]. Furthermore, the generation of these neutral sites was shown to be caused mainly by the "trap creation" (TC) phenomenon which is related to hydrogen release by hot electrons [38, 53-62].

In summary, neutral electron traps generated in the bulk has been found to be causing SILC through trap assisted tunneling. To determine the trap origin in ultra thin SiO_2 oxide, it was suggested that these neutral electron trapping centers could be hydrogen-induced defects produced during the release of hydrogen at the anode by hot electron impact ionization, followed by the transport of hydrogen in the SiO_2 layer, resulting in bond breaking and bulk trap generation [63–65].

Once a stress is applied, charge trapping and trap generation takes place simultaneously. The generation of new trap states follows a power law function with time (and fluence) [47],

$$N(t) = b_t t^m \tag{2.1}$$

$$N(Q) = b_{Qt} Q^m \tag{2.2}$$

Here N(t) and N(Q) are the number of traps generated as a function of time and injected charge respectively, b_t and b_Q are constants.

SILC is defined as $\Delta J(t) = J(t) - J(0)$. Here J(0) and J(t) are the current density before and after stress time, t respectively. The normalized SILC increase is a useful metric because it is proportional to the density of stress generated traps [47] and is given by

$$\Delta J/J_0 = N(t) = b_t t^m \tag{2.3}$$

Where $\Delta J/J_0$ is the normalized SILC.

The following figure shows normalized SILC with accumulated stress time of high-κ/SiO_2 gate stacks. A power law dependence of SILC is observed for all three gate stacks [66].

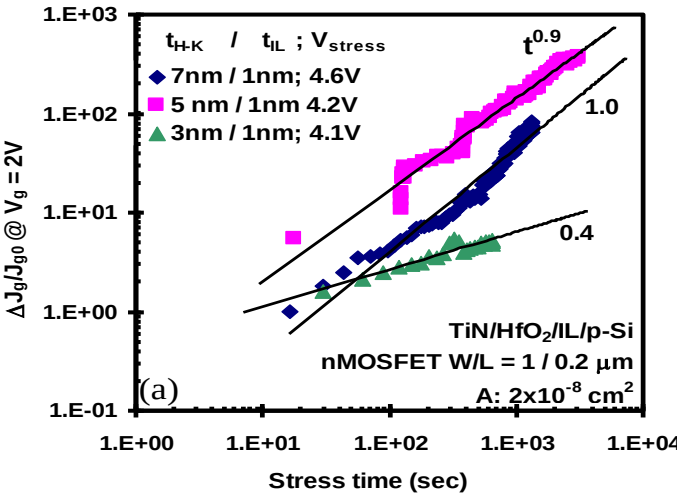


Figure 2.5 SILC evolutions with stress time for various splits of high-κ gate stacks. SILC is sensed at V_g = 2 V [66].

2.2.3 Soft Breakdown of HfO_2 with Constant Voltage Stress

Soft breakdown (SBD) can be defined as localized increase of current through the gate insulator observed in thin oxides stressed at low voltages. The conduction mechanism during SBD is non-Ohmic. By definition, soft breakdown is considered to occur from a weak localized percolation path between the gate electrode and the substrate. The traps are generated during stress and randomly occupy lattice sites of the oxide. Conduction between two neighbor traps is possible when the distance between these traps is less or equal to 0.9 nm [67]. A percolation path is formed between cathode and anode when a critical number of electron traps are generated in the gate dielectric layer and at the interface, as shown in Figure 2.6 [67–71]. This would give rise to an increase in the gate current.

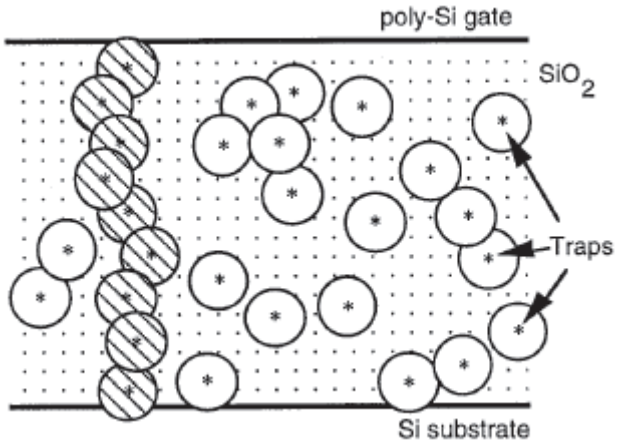


Figure 2.6 Schematic illustration of the new spheres model for intrinsic oxide breakdown simulation based on trap generation and conduction via traps. A breakdown path is indicated by the shaded spheres [67].

The typical breakdown behavior of HfO_2 (EOT = 1.4 nm, physical thickness 4.8-5 nm) gate dielectrics, describing soft and hard breakdown is shown in Figure 2.7 [52]. Typically a soft breakdown is detected after a 2%-5% increase in gate current during stress (CVS).

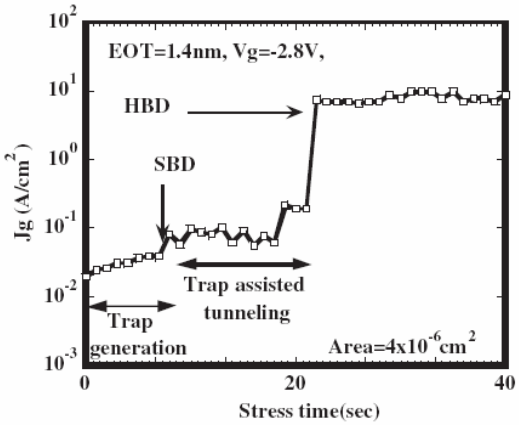


Figure 2.7 Gate current density during constant voltage stress showing soft breakdown of HfO_2 MOS capacitors with EOT 1.4 nm [52].

As described earlier the degradation processes for high-κ dielectric involving trap creation, percolation and subsequent wear out of each of the conduction paths created, ultimately lead to hard breakdown. All these mechanisms act in parallel on a stressed device. It has been shown in Figure 2.8 [69]. Hence, soft breakdown (SBD) and hard breakdown (HBD) are localized and randomly distributed over the device area [72].

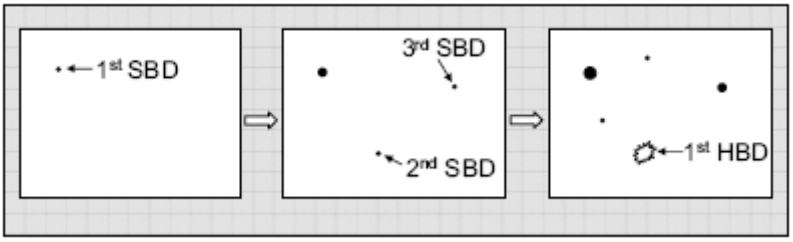


Figure 2.8 Competing sequences of trap generation, percolation (small black dots) and subsequent wear out (dots growing) on a given capacitor [69].

Fluctuation of the leakage current after soft breakdown results from the trapping–detrapping of electrons in the percolation clusters making the current through the dielectric noisy. In the case of SiO_2, device size (channel length for FETs) is a factor for the current increase after the onset of soft breakdown. The radius of soft breakdown path of high-κ dielectrics or the origin of soft breakdown can be very different from that of single layer structure like SiO_2, since high-κ dielectric stacks are in general bi-layer structures (an interface and a bulk high-κ layer).

Soft breakdown and SILC can be differentiated by the magnitude of the gate current increase as shown below. During SBD, significantly higher increase (at least two orders of magnitude) in the sense current is observed than SILC at low applied voltage as shown in Figure 2.9 [73].

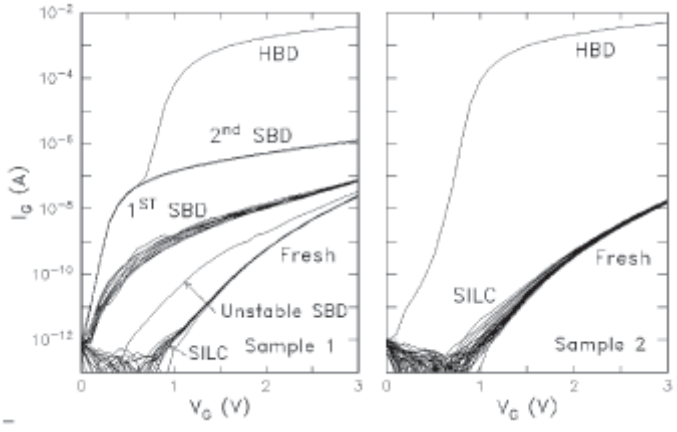


Figure 2.9 Gate current measured interrupting stress for ultrathin SiO_2 oxide showing SILC, SBD and HBD [73].

2.2.4 Progressive Breakdown (PBD regime)

After SBD, the device continues to degrade until catastrophic hard breakdown occurs. In small area devices, after the 1^{ST} breakdown event, the progressive breakdown (PBD) regime is typified by quantized jumps in the current following the occurrence of each successive breakdown event [74]. For ultra thin SiO_2, PBD in nFETs (inversion) has been found as local degradation of a single breakdown spot where as for pFETs stressed in inversion have multiple competing breakdown events during PBD phase [75-76]. Figure 2.10 shows the PBD phase of high-κ/metal gate pFET devices. As circuit functionality is not affected by the 1^{st} BD, progressive breakdown time will give extra margin to product lifetime. Hence characterization of progressive breakdown is critical for practical circuit reliability projection.

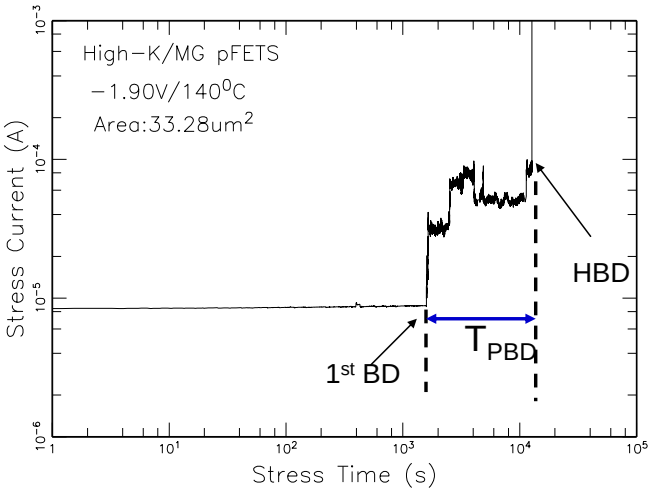


Figure 2.10 Example of the time dependence of gate leakage I_g during CVS at V_G = -1.9 V, in TiN/HfO_2/SiO_2 pFETs of 3.328 x 10^{-7} cm^2 gate area. Progressive breakdown time, T_{PBD} is the time of growth of percolation path which is the time between HBD and 1st BD [77].

This gradual gate current (I_g) growth can be seen mostly in small area devices. Progressive breakdown is associated with an increase of noise in the gate current

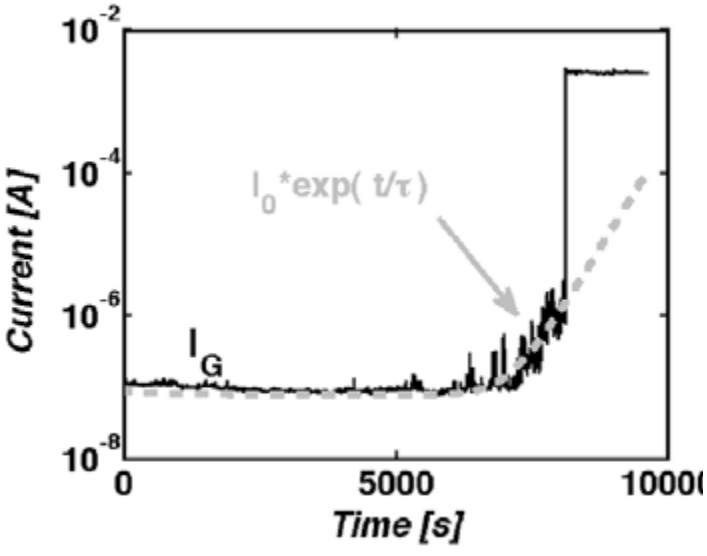


Figure 2.11 Example of exponential growth of the current I_G during the PBD phase. The dotted line is the exponential fit to the measured current [74].

As shown in Figure 2.11, the PBD current shows exponential growth with characteristic time τ and I_0 represents the current flowing through the initial percolation path at the

given stress voltage. As SBD does not necessarily render transistors inoperative, reliability projection techniques have been proposed to increase the time to failure beyond the 1^{ST} breakdown event [78]. One of these models is known as the prevalence method [79-80], where the hard breakdown distribution is shifted from the first breakdown time by a factor that depends on the stress conditions. Another technique is the successive breakdown method [80], which provides a methodology for determining the time at which a specified leakage criteria is exceeded following the occurrence of multiple soft breakdown events. With metal gate/high-κ dielectric, a shorter progressive breakdown stage is observed than with poly-Si gate [18].

2.2.5 Hard Breakdown (HBD)

HBD and SBD are independent failures occurring at different spatial locations [82-83]. Hard breakdown is characterized by an Ohmic I-V relationship and a post breakdown resistance < 10KΩ. As the stress voltage increases, the time delay between SBD and HBD diminishes [84], and the 1^{ST} breakdown becomes predominantly HBD above about 5V [85-86]. In thick oxides stressed at high voltages, HBD is catastrophic and results in a low resistance short between the two electrodes. In ultra-thin dielectrics stressed at low voltages, the HBD and SBD regimes are differentiated by the magnitude of the post breakdown resistance. For an example, effective resistance of the dielectric was around 8.5 Ohm after soft breakdown [68].

2.3 High-κ/IL Breakdown Mechanism

The multilayer high-κ/IL gate stack demonstrates a different breakdown process as compared to single SiO_2 or SiON layer. For gate injection mode, Okada *et al.* [87] has

described the mechanism of the gradual increase of the gate current during electrical stress [Figure 2.12].

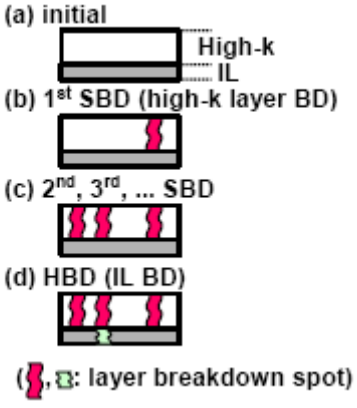


Figure 2.12 The proposed mechanism for the gradual increase of gate leakage through pMOSFETs ($HfAlO_x/SiO_2$ = 5.1/2.2 nm) under negative stress. (a) Before breakdown, (b) after the first SBD of the high-κ layer, (c) successive multiple SBDs occur, (d) until the HBD occurs due to the layer breakdown of the interfacial layer (IL) [87].

Defects are generated in both the high-κ and IL-SiO_2 which results in a conduction path formation in the high-κ layer. This conduction path formation induces SBD in high-κ layer. Further stressing results in successive SBDs at multiple spots on the device. Defect generation in the IL-SiO_2 finally induces the conduction path formation throughout the interfacial layer. This results in HBD of the stacked dielectric film.

It was also found in [52] that the Soft breakdown of HfO_2 (EOT = 1.4 nm) is predominantly observed as the first breakdown event in the gate injection experiment (stress voltage from -2.6 to -2.8 V). The time between soft and hard breakdown significantly decreases as stress voltage increases. However, a study on Ta_2O_5/SiO_2 stack suggested a different mechanism where the high voltage breakdown of the dielectric stack was completely determined by the interfacial SiO_2 layer. This is due to the high electric field across the interfacial layer, which in turn leads to bulk Ta_2O_5's breakdown

immediately after interface degradation [88]. It is known that breakdown field, E_{BD} reduces sharply with increase in dielectric constant [89]. Approximately $E_{bd} \sim (k)^{-1/2}$ relation exists over a very wide range of dielectric materials (over nearly 2–3 decades of dielectric constant) [90-91]. Figure 2.13 shows the reduction in breakdown strength with dielectric constant [92].

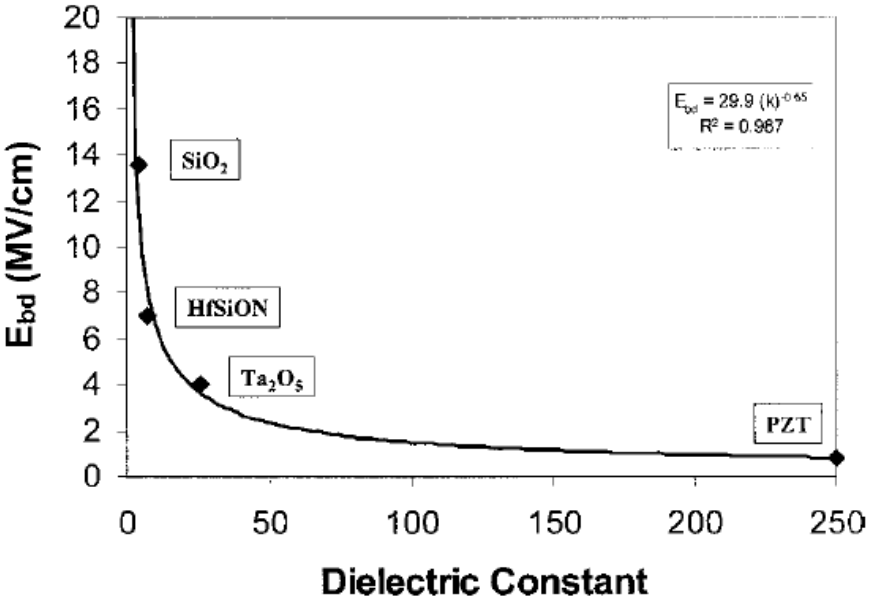


Figure 2.13 Observed breakdown strength with dielectric constant [91].

The charge trapping within the interfacial layer, therefore, not only triggers soft breakdown of HfO_2 but also influences its Weibull distribution. The difference in the Weibull slope, β's of soft and hard breakdowns of HfO_2 may also be due to the effect of interfacial layer. The charge fluence and electric field across the interfacial layer are much larger than across the bulk HfO_2 layer under substrate injection, and there are different defect generation modes as well as different charge fluences between bulk HfO_2 and interface layer under gate injection. Obviously, these differences depend on the composition and the thickness of the interface layer. Based on the thickness dependence

and the percolation model, it is inferred that defect generation and charge trapping in bulk HfO_2 affect hard breakdown [52].

As far as statistical distribution of time-to-fail (T_{FAIL}) of high-κ/metal gate stacks is concerned, it was found that T_{FAIL} distribution does not follow Weibull distribution for the entire percentile. A large sample size experiment on different area shows that T_{FAIL} distribution has lower slope at high percentile whereas the slope get steeper at low percentile [93].

2.4 NBTI of High- κ/Metal Gate

A brief description of the state-of-the-art understanding on Negative bias temperature instability (NBTI) mechanism in SiO_2 will be presented first. Even though high-κ/metal gate have dual layer dielectrics and different structural properties, the interfacial layer is still SiO_2. So, the basic knowledge of NBTI in SiO_2 would help understand the NBTI in high-κ gate stacks as well.

2.4.1 Degradation Mechanism of NBTI for SiO_2

Negative bias temperature instability (NBTI) has been a persistent reliability concern for thermally grown, better quality SiO_2. It has generated a lot of attention to understand the physics of this degradation mechanism which is specific to pMOSFETs. NBTI causes variation in transistor parameters like threshold voltage, drain current, transconductance etc when pMOSFET is biased in inversion. This degradation becomes an issue for the projected lifetime of the transistor.

The revised classical Reaction-Diffusion [R-D] theory which is very popular in the NBTI community states that (a) NBTI degradation is field-driven and interface traps,

N_{IT} at the Si-SiO_2 interface contributes to it [94], (b) $\Delta V_T \sim A \exp(-nE_D/kT)t^n$, with n = 0.16 to 0.25 depending on the measurement delay between stress and sense and activation energy, $E_D \sim 0.5eV$, [95-96] and (c) a fraction of the interface traps recover once the NBTI stress is removed [97].

Based on R-D theory of NBTI, it was assumed that NBTI arises due to the hole-assisted breaking of Si-H bonds at the Si-SiO_2 interface (Figure 2.14). The rate of trap creation is described below [98].

$$\frac{dN_{IT}}{dt} = k_F\left(N_0 - N_{IT}\right) - k_R N_H(0) N_{IT} \tag{2.4}$$

Where N_0 is the initial number of Si-H bond at Si/SiO_2 interface, N_{IT} is generated interface traps due to the broken Si-H bonds at time t by NBTI stress, $N_H(0)$ is the hydrogen concentration at the interface close to Si, k_F is the dissociation rate constant. Once a hole is captured due to negative bias at the gate, it weakens Si-H covalence bond which is then broken at moderate temperature. These broken Si bonds act as traps and contribute to the threshold voltage shift and decrease in transconductance.

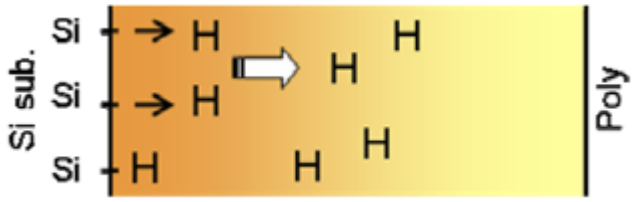


Figure 2.14 The dissociation of Si-H bonds at the Si-SiO_2 interface triggered by hole is shown schematically. Passivation along with dissociation of these Si-H bonds also occurs at the same time [99].

It was found that the power-law exponent, *n* in ΔV_T depends on the diffusing species where *n*=1/2 for proton, *n*=1/6 for molecular H_2 and *n*=1/4 for atomic H diffusion. To project ΔV_T correctly, power-law *n* has to as accurate as possible. As this exponent, *n* is very much sensitive to the measurement delay, various new techniques called 'on-the-fly' method [100-101] and ultra-fast V_T methods [102] have been developed.

2.4.2 Degradation Mechanism of NBTI in High- κ

As it was mentioned earlier, NBTI study of high-κ gate stacks becomes challenging due to its dual layer structure. Both HfO_2 and SiO_2 may contribute to ΔV_T. The high density of pre-existing traps as well as the fast transient charge trapping/detrapping (FTC) observed in high-κ films should also be considered for NBTI study [103-107]. As ΔV_T was observed with a reverse bias (positive V_g) applied during relaxation, it was found that ΔV_T is mostly reversible as shown in Figure 2.15 [108-109]. Change in threshold voltage, ΔV_T was found to follow power-law dependence with stress time with low exponent around 0.16 [110].

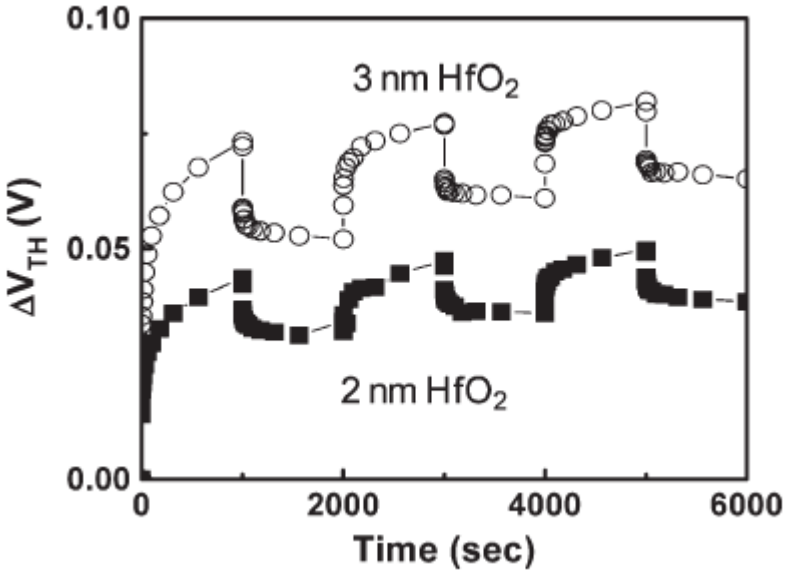


Figure 2.15 Reversible threshold voltage change by applying alternating negative (V_T-1V) and positive bias (+1V) for 1000s cycle. Two gate stacks has 2 and 3 nm HfO_2 with identical 1.1 nm ISSG-SiO_2 as interfacial layer. Both stress and relaxation phases show fast and slow components [109].

2.5 PBTI of High-κ/Metal Gate

Positive bias temperature instability (PBTI) is more serious reliability concern for high-k/metal gate nFETs than it was for SiO_2 and electron trapping was found to affect PBTI predominantly. Kerber *et al.* [111] discussed on electron trapping in SiO_2/HfO_2 dual layer gate stacks in detail and claimed that electron traps in the HfO_2 are the source of the excess charge trapping in HfO_2 resulting in severe PBTI. These electron traps are presumably oxygen vacancies in the high-κ layer [112]. There have been reports of alternative explanation of PBTI induced ΔV_T instability where stress-induced defects generation were assumed to be the cause of the degradation [113-114]. Strong relaxation effects were also observed during PBTI in nFETs with SiO_2/HfO_2 dual layer gate stacks.

Cartier *et al.* showed a direct correlation ($\Delta I_g/I_g \sim dV_t^3$) of stress-induced leakage current and ΔV_T at both room and accelerated temperatures due to PBT stress shown in Figure 2.16 [33]. Early findings show that V_T instability and SILC generation are due to the same defects which are Oxygen vacancy related shallow defects generated in the HfO_2. These defect sites then work as stepping stone during trap-assisted tunneling process causing SILC.

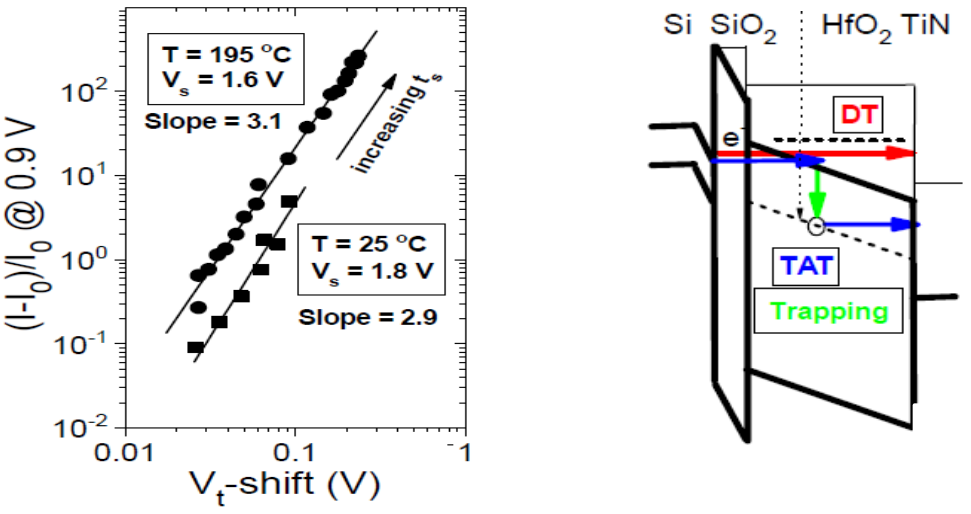


Figure 2.16 (left) SILC and Vt-shift shows direct correlation at both room and high temperature. (Right) High-κ/MG band diagram during PBT stressing showing tunneling and charge trapping in the bulk HfO_2. DT is direct tunneling and TAT is trap-assisted tunneling [33].

As high-κ nFETs show large noise in the gate current due to SILC, this makes the detection of Time-to-breakdown even more complicated during TDDB test.

2.6 Breakdown by Ramped Voltage Stress

Ramped voltage stress (RVS) technique is a fast measurement method to evaluate gate dielectric reliability [115-117]. In this method, gate voltage is ramped at a certain ramp

rate ($\Delta V/\Delta t$) until catastrophic BD occurs. From the I-V characteristics, breakdown voltage V_{BD} distributions can be found for the device in stress. So far, V_{BD} method has been used to study intrinsic breakdown behavior of gate dielectric. The statistical distribution of this intrinsic V_{BD} has been found to follow Weibull distribution.

Also from industry point of view, to reduce defect density in the dielectric or to achieve near zero ppm (parts per million), continuous process improvement, increased qualifications and screening require time consuming test. This ultimately increases manufacturing cost. Hence to replace time consuming constant voltage stress, RVS has been applied as an alternate fast method to qualify gate dielectric integrity. Original idea of the conversion from RVS to TDDB is based on the integration of cumulative damage proposed by Berman [115]. Kerber *et al.* had reported that VRS and CVS results are congruent for high-κ devices in terms of voltage acceleration, Weibull distribution and thermal activation [118]. Figure 2.17 (left) shows how 1st BD has been defined in time domain during CVS. Then, breakdown voltage (V_{BD}) from ramp voltage stress was translated to T_{BD} and compared with directly measured T_{BD}. This is shown in Figure 2.17 (right). This has been applied to 1st BD. But from a practical circuit/chip reliability point of view, 1st BD does not essentially alter circuit functionality [119]. Therefore, this fast RVS technique needs to be verified on failure time with a higher specified fail current (I_{FAIL}). This time-to-fail (T_{FAIL}) will include progressive breakdown time as well. So, a bending at low percentile is expected which would change T_{FAIL} distribution to non-Weibull at low percentile. If CVS is employed to produce this non-Weibull T_{FAIL} distribution, a very large sample size (~1000) is required. This would be even put more constraint on manufacturing time and cost.

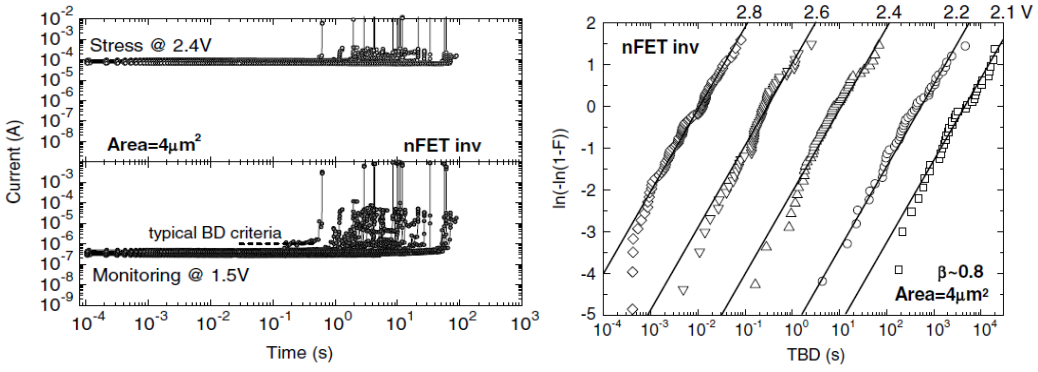


Figure 2.17 (left) Current-time traces during CVS for high-κ nFEts. (Right) Time-to-breakdown (T_{BD}) distributions with Weibull slope, β ~ 0.8 determined from current time traces (left figure) using a breakdown criteria of 1 μA at monitoring condition [118].

Progressive breakdown time has become an essential parameter for accurate reliability projection. Hence an appropriate technique is required to characterize progressive breakdown time. It will be discussed in chapter 6 that this RVS method can be utilized to exclusively characterize progressive breakdown time as well.

2.7 Chapter Summary

This chapter summarizes several reliability issues of high-κ/metal gate and SiO_2 oxide focusing mainly on dielectric breakdown physics. Even though there has been considerable performance improvement of this new dielectric material, reliability issues such as TDDB, RVS, NBTI, PBTI for the multilayer gate stacks are not well understood yet. Hence, reliability seems to act as showstopper for the integration of this new dielectric material in future CMOS technology nodes. Therefore, systematic BTI investigation of high-κ and interfacial layer is required. For TDDB, studying progressive

breakdown phase and time to fail based on specific failure current would be more meaningful in terms of circuit or product reliability point of view.

CHAPTER 3

DEVICE FABRICATION AND ELECTRICAL CHARACTERIZATION

3.1 Introduction

This chapter describes the fabrication detail of MOS devices based on TiN/HfO_2 gate stacks and HfO_2-only Metal-Insulator-Metal (MIM) capacitors. The electrical characterization techniques performed to study breakdown of the dielectrics are also discussed.

3.2 TiN/HfO_2 based MOS Devices Fabrication

Various deposition process have been attempted to deposit HfO_2 thin films. Physical methods like e-beam evaporation [120], sputtering [121] in addition to chemical methods like anodization [122], atomic layer deposition (ALD) [123-125], and chemical vapor deposition [126-127] have been used for the deposition of thin HfO_2 films. Chemical methods demonstrated more advantages compared to physical methods due to their better controllability of growing uniform layers on the substrate and easy composition control. Even Though thin HfO_2 films are very difficult to synthesize, ALD and MOCVD (metal organic CVD) have been found most promising among these chemical processes. In ALD process, precursors are given alternately into the deposition chamber. Self-limiting heterogeneous reactions take place on the substrate surface. The film grows one monolayer at a time and the deposition cycle determines the total thickness of the film. For MOCVD, a metal organic compound is used as one of the precursors. An essential requirement for MOCVD process is that the precursors

should have the appropriate physical properties and decomposition characteristics. For MOCVD process, a cold wall reactor is used with the precursors being delivered to the heated substrate by a carrier gas [128]. Detail description on the MOCVD process has been described in the reference [128]. It was found that ALD grown HfO_2 films are amorphous while MOCVD grown films are more of crystalline structure. Also, the amount of interfacial SiO_2 is greater in MOCVD grown films compared to ALD films [129].

For the gate stack of $TiN/HfO_2/SiO_2/p\text{-}Si$ considered in this research, HfO_2 film was deposited by various cycles of atomic layer deposition (ALD) on p-type Si substrate (ρ =0.01-0.02 Ohm-cm). For these blanket HfO_2 films, oxidation was performed using precursors tetrakis (ethylmethylamino) hafnium (TEMAHf, $Hf[N(CH_3)(C_2H_5)]_4$) and O_3 [130]. Wafer temperature was held at 330^0C while an ALD cycle was being performed. An ALD cycle has TEMAHf pulse, inert purge, O3 pulse, and inert purge. To achieve a growth rate of 0.08nm/cycle, wafer temperature, reactor pressure, TEMAHf and O_3 pulse times were constant [131]. As for the HfO_2 and substrate interface preparation, differently processed interfacial SiO_2 layers were grown before HfO_2 deposition [132]. Pre and post deposition annealing were done at 700^0C for 60s in NH_3. N^+-ringed nMOS capacitors and nMOSFETs were fabricated using the standard CMOS process flow.

The high-κ based metal-insulator-metal (MIM) capacitors were fabricated with a 4nm ALD HfO_2 (with 10% SiO_2) deposited on bottom TiN electrode. As-deposited HfO_2 (or more specifically Hf Silicate) is found to be amorphous and after 500^0C post deposition anneal. Both top and bottom electrodes were deposited by ALD. The root-mean-square surface roughness of titanium nitride (TiN) layer was less than 1nm as

measured by atomic force microscopy [133]. For top electrode, TiN/W stacks were deposited. The MIM structures used were annealed after deposition at 800^0C in N_2 ambient for 20s. These Hf-silicate samples changed to crystalline due to the post deposition annealing at this high temperature. MIM capacitors of gate area 10^{-5} cm^2 were used.

3.2.1 Interfacial Layer Growth

For SiO_2–only gate structure, 2 nm ISSG SiO_2 growth was replicated similar to gate stack with a 60s post-DA in NH_3 at 700^0C. Interfacial SiO_2 was also grown chemically. TiN, deposited by ALD, was used for top gate electrode.

All these state-of-the-art wafer level devices were fabricated at International SEMATECH cleanroom facility, Austin, Texas using standard CMOS process flow.

3.3 Electrical Characterization

Measurements of the electrical properties, parameters extracted from these measurements and control over these parameters lead to stable and high performance MOS devices. Bulk oxide and oxide-substrate interface are two major regions of the MOS system. Charges in these two regions are undesirable because they adversely affect the device performance and stability. The MOS capacitors and transistors are being used to study the electrical characteristics as they have the advantage of simplicity of fabrication and analysis. Following measurements techniques have been employed in characterizing the charges present in MOS capacitors and transistors using HfO_2 as gate dielectric.

3.3.1 Capacitance-Voltage (C-V) Measurement

The high frequency (HF) and low frequency (LF) capacitance-Voltage (CV) measurements were carried out using HP 4284 at the frequency range of 1 MHz to 100 Hz. The flatband voltage from this C-V graph has been calculated from NCSU CVC program [134]. From C-V measurements on MOS capacitors, important parameters like flatband voltage (V_{FB}), interface trap density (D_{it}), surface potential (ψ_s) have been calculated. Also, C-V curves with double sweep provide hysteresis values.

3.3.2 Conductance Measurement

To study slow and fast traps at the oxide/semiconductor interface, it is essential to investigate conductance measurements at various frequencies. Hence these conductance measurements were carried out at various frequencies using HP4184. The frequencies were 1 KHz, 100 KHz, 1 MHz. This was used to measure the interface state density of capacitors which was computed using equation (3.1) and (3.2) [135].

$$\frac{G_P}{W} = \frac{wG_m C_{ox}^{\ 2}}{G_m^{\ 2} + W^2 (C_{OX} - C_m)^2} \tag{3.1}$$

$$D_{it} = \frac{2.5}{q}\left(\frac{G_P}{W}\right)_{\max} \tag{3.2}$$

Where G_m is the conductance measured, C_{ox} is the accumulation capacitance, w is the frequency, and C_m is the capacitance at the particular frequency and gate voltage.

3.3.3 Stress Measurement

High field stress in gate oxides of MOS devices is known to generate defects such as interface states, electron traps, positively charged donor-like states etc. When the defect density reaches a critical value, gate oxide goes to catastrophic breakdown. Oxide integrity was studied by time-dependent measurements by applying constant bias and simultaneously measuring current at different nodes of MOSFET devices. As the constant bias is applied, electrons would flow from cathode to anode contact. Figure 3.1 shows this schematically with a band diagram of a dual layer gate stack during constant voltage stress (CVS) in substrate injection mode. Due to the high field stress, electrons travel by direct tunneling through thin interfacial layer and trap-assisted tunneling through thicker high-κ layer. For CVS, gate current was always measured during stress.

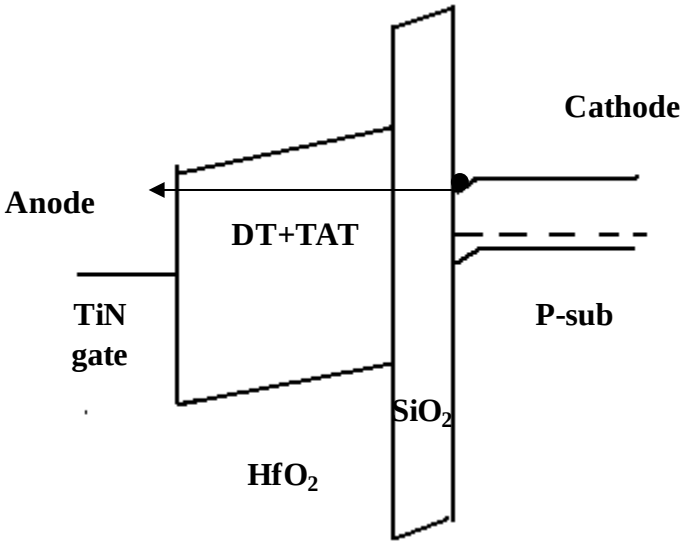


Figure 3.1 Schematic of a band diagram during constant voltage stress (CVS) showing the flow of electrons from cathode to anode side.

3.3.3.1 Constant Voltage Stress. Constant voltage stress (CVS) is implemented by applying positive or negative bias on gate while keeping drain, source and substrate grounded as shown schematically for a MOSFET in Figure 3.2. During stress, gate current is measured to estimate charge by integrating gate current over time as shown in equation 3.3 [135] and also to record time-to-breakdown (T_{BD}) based on the specified fail current.

$$Q_{inj} = \int_{t_1}^{t_2} J_g(t)dt \tag{3.3}$$

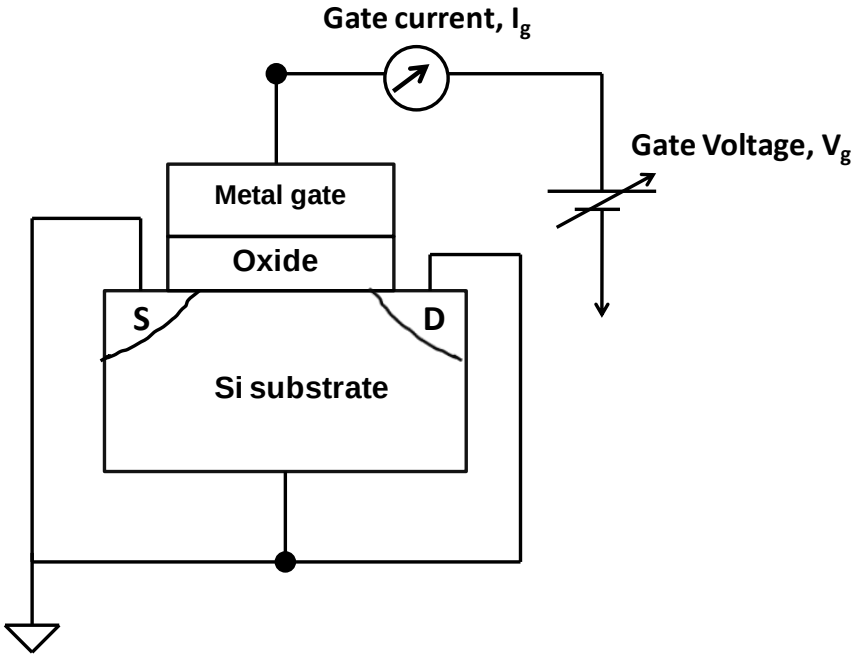


Figure 3.2 Constant voltage stress (CVS) set-up for MOSFET. For time-dependent dielectric measurement, source, drain and substrate are grounded and bias voltage is applied at the gate. Gate current, I_g is measured simultaneously.

The voltage drop across the stack for the applied bias Vg follows the following potential balance:

$$V_g = \Psi_S + V_{stack} + V_{FB} \tag{3.4}$$

where Ψ_S is the surface potential, V_{FB} is flatband voltage. For bulk doping density ≈ 10^{17} cm^{-3}, V_{FB} ≈ -0.5 V (determined from NCSU CVC program [129]) for high-κ/SiO_2 gate stack and for SiO_2- only capacitors, V_{FB} ≈ -0.7 V were found. For surface potentials Ψ_S (which is $2\phi_b$) for gate stack and SiO_2-only capacitors were measured 0.95 V and 0.918 V respectively.

The band diagram of a MOS structure at flatband with a high-κ dual layer stack is shown in Figure 3.3. As the high-κ gate stacks consist of a thin interfacial SiO_2, a thicker high-κ layer and metal gate, any applied gate voltage (V_g) will partly drop over the interfacial layer and the high-κ, whereas the distribution depends on the physical layer thicknesses and the κ-values. At applied bias, the potential distribution across the stack is calculated as follows [66].

$$V_{OX} = E_{H-K} \times T_{H-K} \times (1 + \frac{EOT_{IL}}{EOT_{H-K}}) \tag{3.5}$$

$$V_{OX} = E_{IL} \times T_{IL} \times (1 + \frac{EOT_{H-K}}{EOT_{IL}}) \tag{3.6}$$

Here, V_{OX} is the voltage across the gate stack, $E_{H\text{-}K}$ and E_{IL} are fields across, $T_{H\text{-}K}$ and T_{IL} are the physical thickness, and $EOT_{H\text{-}K}$ and EOT_{IL} are the effective oxide thickness of high-κ and interfacial layers respectively.

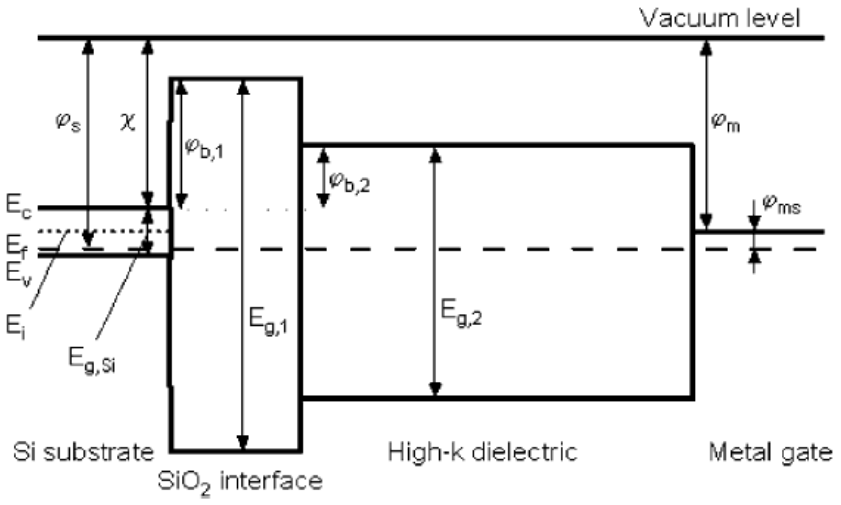


Figure 3.3 The energy band diagram in flatband condition with E_c the Si conduction band, E_v the Si valence band, E_f the semiconductor Fermi level, E_i the intrinsic Fermi level, E_g the band gap, φ_s the semiconductor work function, φ_m the metal work function, $\varphi_{b,1}$ the potential barrier for the interface and $\varphi_{b,2}$ for the high-κ, φ_{ms} the work function difference and χ the semiconductor electron affinity. The EOT of the stack is 1.6 nm with p-Si substrate, 1 nm interfacial SiO_2, 3 nm high-κ dielectric (k = 20, $\varphi_{b,2}$ = 1.5 eV) and a mid gap metal gate electrode. [136].

In case of gate injection (V_g<0) the leakage current is determined by electron tunneling through the high-κ and the interfacial layer (Figure 3.4a). For substrate injection (V_g >0), the electrons tunnel through the interfacial layer and just partly (or even not) through the high-κ before entering the high-κ conduction band (Figure 3.4b).

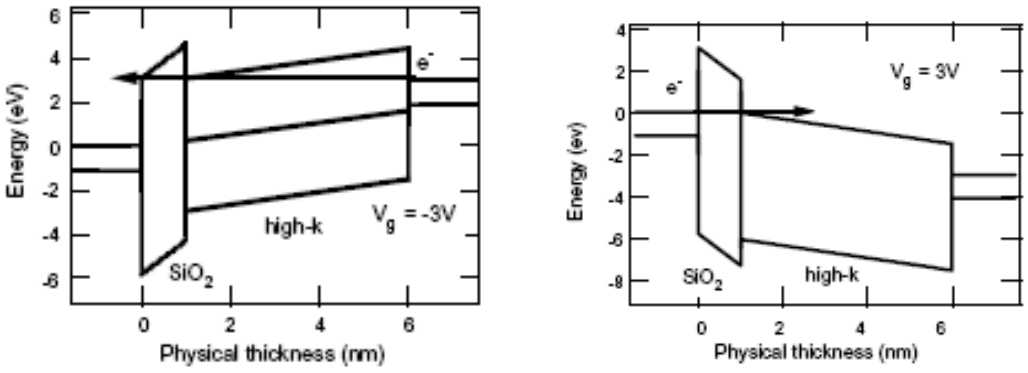


Figure 3.4 (a) Gate injection: If a negative bias at the gate is applied electrons tunnel from the gate electrode through the high-κ and then the interfacial layer. (b) Substrate injection: With a positive bias applied electrons tunnel from the Si substrate towards the electrode. Already at relative low voltages electrons start to enter the high-κ conduction band and tunnel only through the interfacial layer [136].

3.3.3.2 Negative Bias Temperature Instability (NBTI). The basic equation for a p-channel MOSFET threshold voltage is given by

$$V_T = V_{FB} - 2\Phi_F - |Q_B|/C_{ox} \qquad (3.7)$$

where $\Phi_F = (kT/q)ln(N_D/n_i)$, $|Q_B| = (4qKs\varepsilon_o\Phi_F N_D)^{1/2}$ and C_{ox} is the oxide capacitance per unit area. The other symbols have their usual meaning. The flatband voltage is given by

$$V_{FB} = \Phi_{MS} - Q_f/C_{ox} - Q_{it}(\Phi s)/C_{ox} \qquad (3.8)$$

where Q_f is the fixed charge density and Q_{it} the interface trap density. The only parameters that can lead to threshold voltage shifts are the fixed charge density Q_f and the

interface trapped charge density Q_{it} . Either or both of these charge densities are changed when negative bias is applied to the gate for long stress times and/or elevated temperatures. For NBTI measurements, stress-sense-stress sequence was followed using an HP 4145B semiconductor parameter analyzer.

3.3.3.3 Stress Induced Leakage Current (SILC) Measurement. SILC has been used as a tool for the analysis of the trap generation and breakdown physics of gate dielectrics. For oxide thickness less than 6.5 nm, post-stress current though the oxides is a steady state signal [47]. Figure 3.5 shows the fresh and post-stress I-V characteristics of high-κ nMOS devices stressed in inversion. The gate current was sensed at low gate voltage range (0V to +1.6V) interrupting constant voltage stress. It can be noted that the total gate current $I_{g,measured} = I_{tunnel} + I_{SILC}$ where the tunneling current is the current through the ideal oxides without any traps [137]. The density of neutral electron traps increases during stress and a gradual increase in SILC is observed [138]. But the tunneling current does not change as the stress continues. In this research, the change in gate current after stress compared to before stress current [$(I_g(t)-I_g(0))/I_g(0)$] sensed at low bias voltage has been considered to account for the change in SILC or oxide trap density.

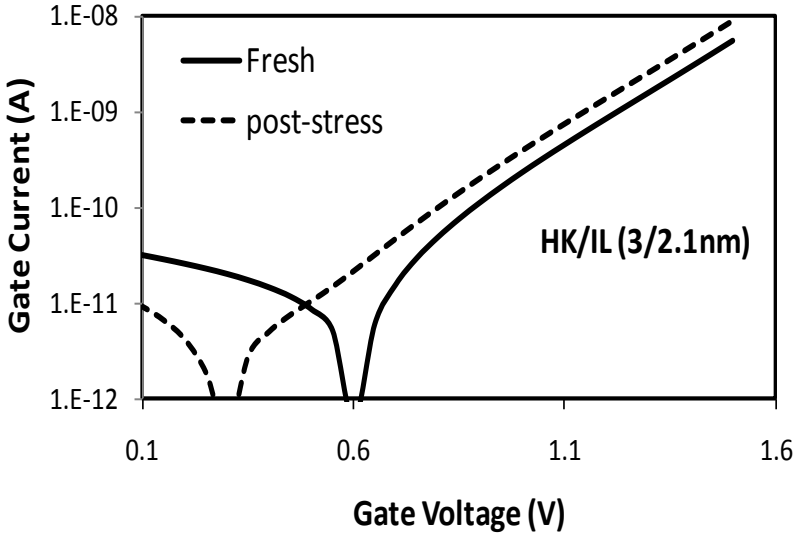


Figure 3.5 Fresh and post ramp-stress I-V characteristics for high-κ nMOS devices in inversion. Stress voltage was 2.4V and post-stress current measured at low voltage shown in the figure was measured after 1000 seconds stress.

3.3.3.4 Differential Resistance. Differential resistance, $R_{diff.,}$ calculated from the SILC data, could be a measure of dielectric degradation [138]. It is defined as $R_{diff.} = \Delta V_g / \Delta I_g$. Initial I-V was measured for a low voltage range (for example, 0 to 1.5V) before the stress was started and it can be defined as I_0. Stress was then interrupted periodically to measure current at that same low voltage range and this current can be defined as I_{sense}. For each stress time, ΔV_g is the difference of the consecutive sense voltages and similarly ΔI_g is the change in current for that corresponding ΔV_g. R_{diff} is calculated from these two values of ΔV_g and ΔI_g. R_{diff} drops for the entire sense voltage range as the oxide goes into soft breakdown and drops significantly as hard breakdown occurs. It behaves like a conductor (low and constant resistance with gate voltage) after HBD.

3.3.4 TDDB (Time Dependent Dielectric Breakdown) Measurement

To study the dielectric breakdown behavior, it is necessary to examine the Time Dependent Dielectric Breakdown characteristics. The breakdown time is measured using either constant current or constant voltage stress. A breakdown is detected when a permanent low resistance path is formed between the cathode and the anode or the stress current reaches specified high value of current level. CVS was given in this case and the gate current variation with stress time (I-t) was monitored to obtain the time to breakdown (T_{BD}). For all three gate stacks considered here, devices were subjected to high filed stress during CVS but still below their breakdown voltages. For the gate stack with thick high-κ, applied CVS was 5.1 V which is below the break down voltage of the gate stack. For MIM-C, V_{BD} was around 3V and CVS was performed at 2.6V. For ISSG SiO_2-only capacitors, the experimentally measured breakdown field was 17 MV/cm and the applied electric field for CVS was 13.75MV/cm (2.2 V).

The charge to breakdown (Q_{BD}) was computed using (3.7). Q_{BD} is defined as the charge flowing through the oxide until it breaks down.

$$Q_{BD} = \int_0^{t_{BD}} I_G dt \tag{3.9}$$

Where t_{BD} is the time to break down and the I_g is the gate current during stress. Q_{BD} of high-κ/SiO_2 interfacial layer, high-κ only and SiO_2-only were used as a comparison. The devices having extrinsic defects (early failures) were screened out by capacitance–voltage

(C–V) and leakage current measurements at low voltage using a HP4284A LCR meter and a HP 4145 semiconductor parameter analyzer, respectively.

3.3.5 Weibull Statistics of Time-to-Breakdown

It is known that time-to-breakdown is a random variable and the distribution of T_{BD} follows Weibull statistics. The cumulative distribution failure (CDF) for the Weibull distribution is:

$$F(t) = 1 - \exp(-(\frac{t}{\eta})^{\beta}) \tag{3.10}$$

β is the shape parameter or Weibull slope, and η is the scale parameter or characteristic life. The measurements were carried out for more than 15 devices in each case to obtain the oxide breakdown statistics. The Weibull slope decreases with decreasing thickness, reflecting the larger statistical spread in the smaller trap densities required to form a breakdown path across thinner oxides [67]. From (3.8), when t = η, then F(t) ~ 0.63. η is often referred to as $t_{63\%}$. An example of a Weibull distribution of the experimental time-to-fail data has been shown in Figure 3.6. As nMOS capacitors with a thick SiO_2 (6.2 nm) was stressed and T_{BD} (or T_{FAIL}) was measured based on the fail current (100 μA). It is observed that the cumulative failure probability of experimental T_{BD} data (symbols) follows Weibull distribution as shown by the line. Maximum likelihood estimation was used for parameter extraction. Weibull parameters like characteristic time, η or t63% and slope β were found from the fit as 7110 seconds and 2.5 respectively.

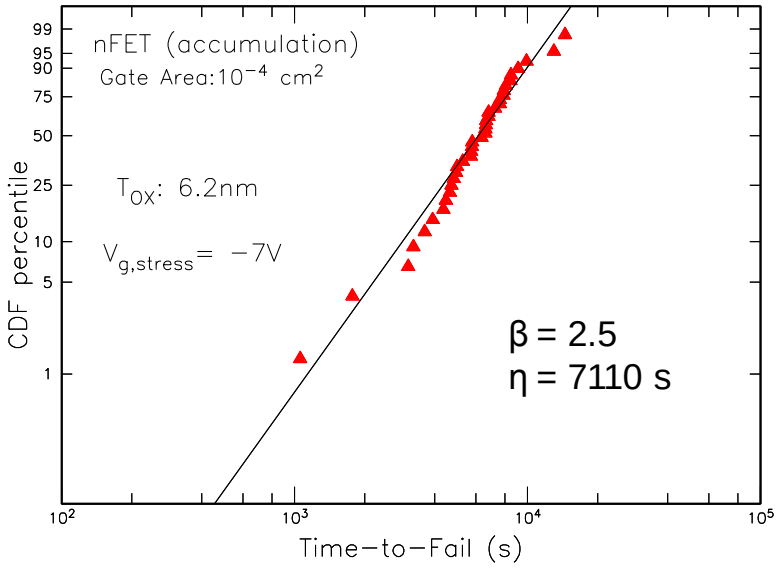


Figure 3.6 Weibull distribution of T_{BD} for thick SiO_2 nFET capacitors in accumulation. Symbols represent experimental T_{BD} data and line is a Weibull fit using maximum likelihood estimation (MLE). Weibull slope, β was 2.5 and η (or $t_{63\%}$) was 7110 seconds found from the fit.

To explain the method to plot the raw T_{BD} data in the Weibull scale, first the breakdown times have been sorted in the ascending order giving a rank to each T_{BD} data point from 1 to n, where n is the total population. Then for the lowest T_{BD} data point, cumulative failure probability was calculated as $F_1=1/n$, $F_2=2/n$. For the highest T_{BD} data point, F_n = 99.99% was chosen instead of 1 (n/n) as failure probability of 100% can not be plotted in Weibit scale where Weibit (W) is defined as $W \equiv \ln[-\ln(1-F)]$.

3.3.6 Voltage Ramp Stress (VRS) Measurement

Voltage ramp stress was applied to study gate dielectric integrity. Ramp rate is defined as the ratio of voltage step to time step ($\Delta V/\Delta t$). In the literature, there is confusion regarding the selection of ramp rate for ramp voltage study [139]. It was shown that ramp rate up to 1 V/s worked for the V_{BD} to T_{BD} conversion, but 2.014 V/s fails as the ramp

rate was too high. But it was found that this effect was due to larger voltage step, not for high ramp rate. Ramp rate can be made faster by reducing the time step. For this work, voltage step was chosen as small as 1mV to approximate linear ramp and also to avoid granularity effect. For time steps, several values such as 100ms, 10ms and 1ms were taken into consideration. Minimum time step was determined by the instrument resolution limit. With this voltage and time step combination, it was found that ramp rate can be higher than 2 V/s.

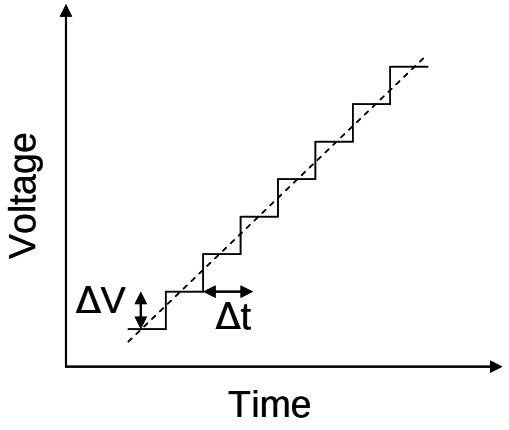


Figure 3.7 Schematic of voltage ramp stress. Small voltage step was chosen to approximate linear ramp and also avoid the granularity effect.

From current-voltage (I_g-V_g) curve as shown in Figure 3.8 (a), V_{FAIL} was extracted based on the exponential law I=A*exp(BV) [140]. Also, it is worth to mention that interpolation was applied to calculate V_{FAIL} for a specific fail current, I_{FAIL}. Statistical distribution of V_{FAIL} for high-κ pFETs is shown in Weibit scale (Ln(-Ln(1-F)) in Figure 3.8 (b).

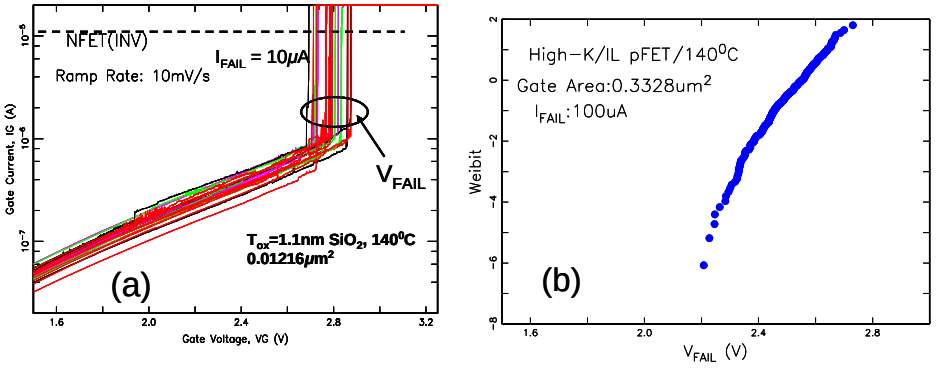


Figure 3.8 (a) Fail voltage (V_{FAIL}) was extracted from the I_g-V_g curve based on a specific failure current, I_{FAIL} (10μA here), (b) an example of V_{FAIL} distribution for high-κ pFETs. Specific failure current was 100 μA in this case as high-κ pFETs show significant progressive breakdown phase.

3.4 Chapter Summary

This chapter summarizes process information of Hf-based oxides and SiO_2-based interfacial layer. All electrical characterization techniques used in this thesis were also discussed.

CHAPTER 4

CONSTANT VOLTAGE STRESS AND TIME DEPENDENT DIELECTRIC BREAKDOWN (TDDB)

4.1 Introduction

In this chapter, we have considered a TiN/HfO_2/SiO_2/Si gate stack which has an EOT of 2.6 nm with the physical thickness of 2.1 nm ISSG SiO_2 interfacial layer and 3 nm HfO_2. Details of the device fabrication are provided in chapter 3. This gate stack represents the multi-layer structure that can be scaled to an EOT of 1 nm. Individual layers with identical process conditions were considered separately. TiN/4nmHfSiO (10% SiO_2)/TiN metal-insulator-metal capacitor (MIM-C) have been selected for high-κ layer. The reason for selecting this capacitor structure (high-κ on metal) is to eliminate the formation of any interfacial layer as compared to when deposited on Si. If the high-κ oxide is deposited directly on Si substrate, due to the oxygen diffusion to the interface of high-κ and Si, it usually forms an interfacial layer between them.TiN/2nm in-situ steam grown SiO_2/Si MOS capacitors were considered for evaluation of interfacial layer. Four different degradation regimes i) Defect generation, (ii) Soft breakdown (SBD), (iii) Progressive breakdown (PBD) and (iv) Hard breakdown (HBD) were monitored under constant voltage stress (CVS) for HfO_2/SiO_2 gate stacks.

The above mentioned four degradation phases were observed in gate current at time dependent dielectric breakdown (TDDB) stress voltage. Defect generation phase can be studied quantitatively by measuring gate current at low sense voltage. This current is called stress-induced leakage current (SILC). SILC behavior was studied by

the increase in gate current and differential resistance calculated from SILC. Analysis of low voltage SILC (LVSILC) at high stress voltages would help to identify the gate stack degradation in terms of trap energy distribution and trap location. Therefore, LVSILC was then analyzed in the context of stress and sense voltage dependence. Also, to isolate the contribution of interfacial layer (IL) in SILC formation, two structures with same high-κ layer but different IL were examined.

Studying breakdown behavior at room temperature provides some fundamental characteristics of the dielectric material. But for practical purposes, circuits would operate at considerably higher temperature than room temperature due to the high density. Also, high-κ gate stacks show high temperature dependence in SILC and time-to-breakdown (T_{BD}). Hence, a closer investigation of SILC and T_{BD} at accelerated temperature would provide more accurate estimation of these parameters at operating condition.

4.2 Constant Voltage Stress at Room Temperature

4.2.1 Gate Current Analysis with Stress Time

Figure 4.1 shows the gate current change with stress time when CVS was applied on high-κ/IL gate stack (3nm HfO_2/2.1nm ISSG SiO_2) of area 10^{-8} cm^2. Four different regimes of degradation can be observed as indicated in the figure (Defect generation/charge trapping, soft breakdown, progressive breakdown and hard breakdown).

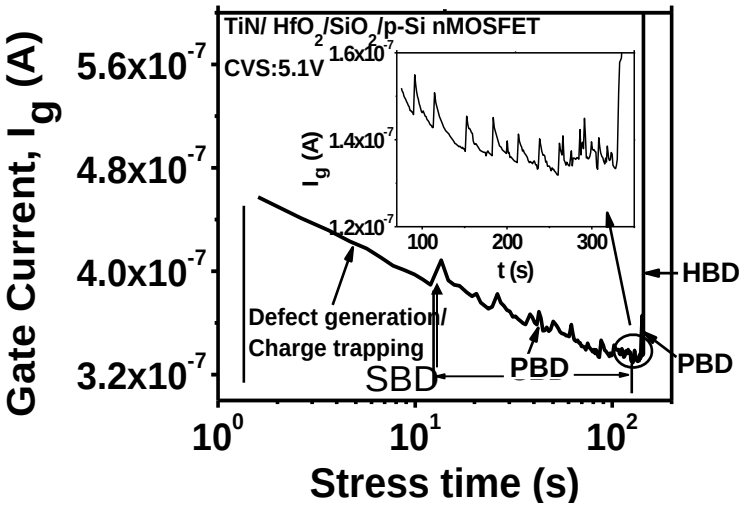
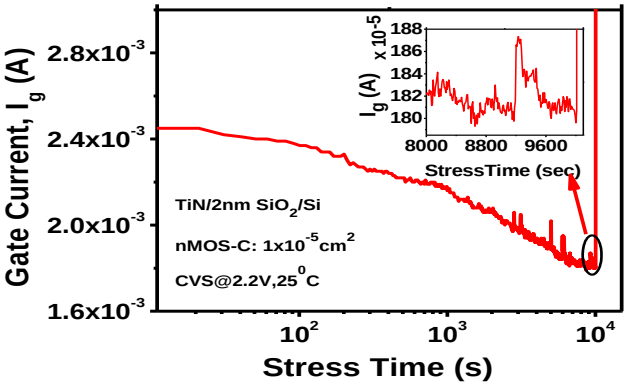


Figure 4.1 Gate current with stress time at CVS (5.1V) at 25^0C for TiN/HfO_2/IL (SiO_2)/Si under substrate injection. Different degradation phases as trapping, SBD, PBD and HBD can be observed. It is important to note that PBD time is observed to be very short for this stress condition.

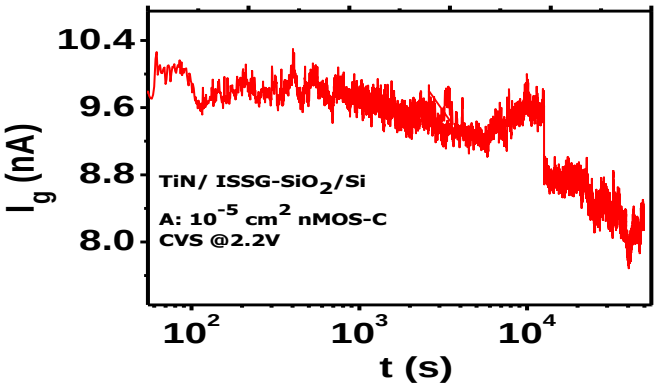
During initial stress period, a gradual decrease in stress current (~19%) was observed. It was mostly due to charge trapping in either HfO_2 layer or interfacial layer. The stress current then becomes noisy, a signature of defect generation. This regime is widely known as soft breakdown (SBD). In substrate injection mode, soft breakdown starts with the formation of localized conduction path in the interfacial SiO_2 layer [141]. The process continues further for several hundred seconds. This regime was followed by progressive breakdown as shown in the inset of the Figure 4.1 where gate current was sharply increasing but noisy pattern of stress current were still visible. Due to aging of the percolating path in the gate dielectric, progressive breakdown is observed [141-142]. Following the progressive breakdown, an immediate thermal run away (HBD) can be seen causing the entire gate stack to breakdown (Figure 1).

To analyze the contribution of IL individually, nMOS-C of TiN/2nm ISSG SiO_2/p-Si is being subjected to constant voltage stress at 2.2V. Three different degradation regimes (trap generation, SBD, HBD) are visible as shown in Figure 4.2(a). The first 2000s current shows gradual decrease due to the defects like interface traps generation. After 2000 sec, complex fluctuations in the gate current can be observed (in the inset of Figure 4.2 (a)) which definitely indicates a soft breakdown of this ultra thin ISSG SiO_2 gate oxide [32, 78]. Soft breakdown typically occurs when a critical number of traps form an unstable conducting path between cathode and anode at different locations of the dielectric [143]. As the stress continued, energy dissipation of these localized areas increases and drives the capacitor into thermal runaway or hard breakdown. Figure 4.2(b) shows that during TDDB measurement of ultra thin ISSG SiO_2 a clear soft breakdown was visible within short period of stress, but it rarely reached the hard breakdown till 50000 seconds. Gate voltage was used 2.2 V as compared to 5.1 V for the gate stack. Ultra thin thermally grown SiO_2 showed this type of breakdown behavior at low applied voltages [32].



(a)

Figure 4.2 (a)**,** (b) Gate current evolution at CVS (2.2V, 25^{o}C) for TiN/SiO_2/Si nMOS capacitor.



(b)

Figure 4.2 (a), (b) Gate current evolution at CVS (2.2V, 25°C) for TiN/SiO_2/Si nMOS capacitor (continued).

When CVS was applied on MIM-C (TiN/4nm HfSiO/TiN), a small increase (~2.5%) was observed compared to high-κ/IL gate stack until it reached the hard breakdown shown in Figure 4.3. The inset of Figure 4.3 shows very minimal change in stress current for this MIM-C prior to HBD. Similar breakdown characteristics were also observed by F. Mondon *et al.* [143] for thin high-κ MIM-C.

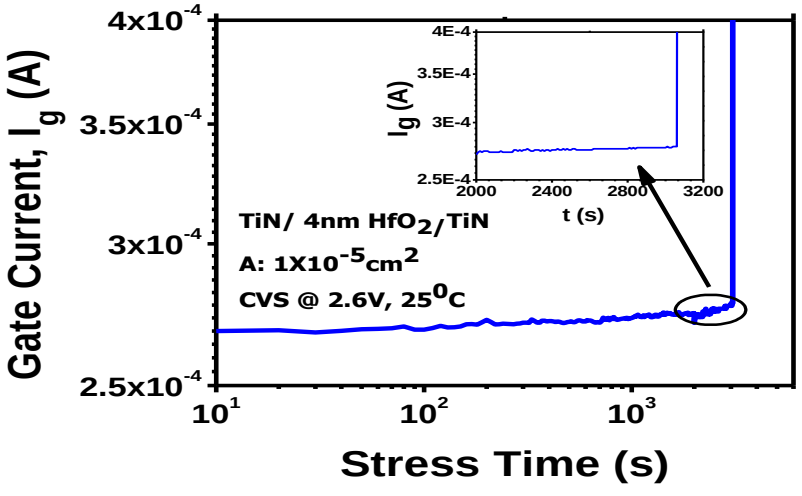


Figure 4.3 Gate current with stress time at CVS (2.6V, 25°C) for ALD TiN/HfSiO(10% SiO_2)/TiN MIM-C.

4.2.2 Analysis with Electric Field Dependence

The breakdown field across the ISSG SiO_2 and that of high-κ gate dielectric can be estimated by apply a ramped voltage stress (RVS). Instantaneous increase of I_g by an order of magnitude is considered as hard breakdown (HBD). Figure 4.4 shows I-V characteristics for RVS applied on ISSG SiO_2 nMOS-C in inversion regime (substrate injection). Voltage across oxide, $V_{ox} = V_g - V_{FB} - \phi_s$, where ϕ_s is the surface potential. For bulk doping density ≈ 10^{17} cm^{-3}, V_{FB} ≈ -0.7 V (determined from NCSU CVC program [134], and breakdown voltage, V_{BD} ≈ 3.0 V, E_{BD}^{SiO2} ≈ 17 MV/cm, which is comparable to the theoretical value of 15 MV/cm [144].

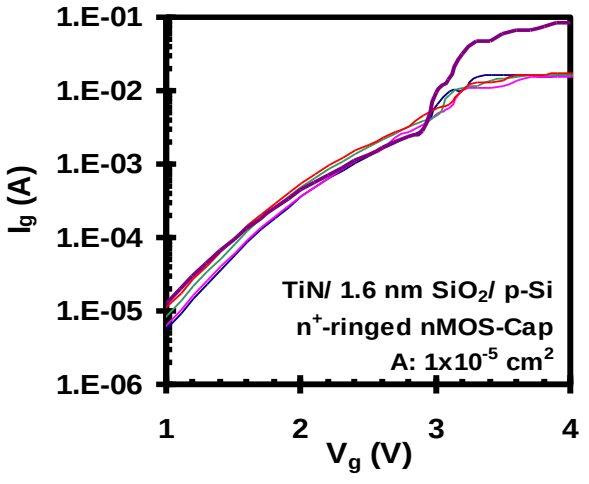


Figure 4.4 I-V characteristics under ramped voltage stress (RVS) applied on n^+-ringed nMOS-C. E_{BD} ≈ 17 MV/cm is comparable with the theoretical value of ~ 15 MV/cm.

Figure 4.5 shows breakdown characteristics of MIM capacitor with 4 nm $HfSi_xO_y$ (10% SiO_2) as insulating material. E_{BD}^{HfSiO} ≈ 6.5 MV/cm, which is comparable to the theoretical value of 7 MV/cm for HfSiON [144]. McPherson showed that E_{BD}

$\propto \kappa^{-0.5}$. For Hf-silicate, $\kappa \approx 10$ to 15 [145], and for HfO_2, $\kappa \approx 20$- 25; hence, E_{BD}^{HfO2} may be expected to be in the range of 4–5 MV/cm in our films. This is within the theoretical limits of 3.9 to 6.7 MV/cm [144]. This further indicates that the dielectrics follow the trends for hard breakdown. The field across ISSG SiO_2 seems to severely suffer from the soft breakdown degradation compared to high-κ layer.

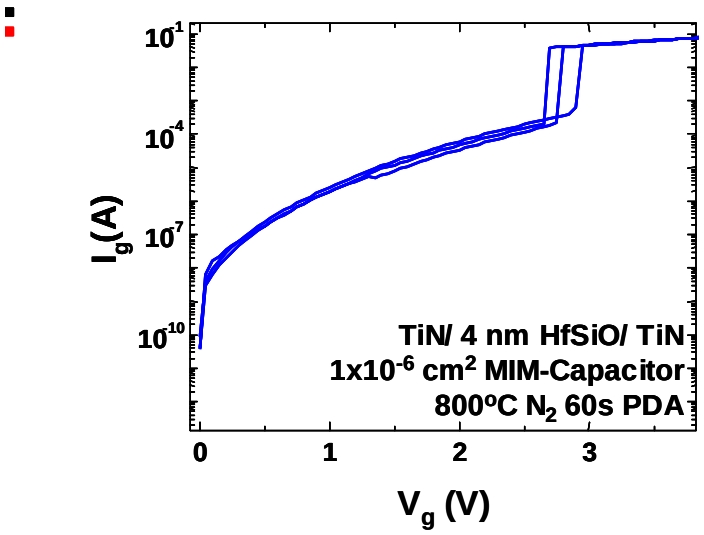


Figure 4.5 I-V characteristics under RVS applied on $HfSi_xO_y$ (10% SiO_2) based MIM capacitors. $E_{BD} \approx 6.5$ MV/cm is comparable with the theoretical value of ~ 7 MV/cm.

It is, therefore clear that the gate stack enters into the SBD mode as the IL enter the SBD. The conduction process in high-κ is due to the standard trap assisted tunneling. It is possible that the interfacial layer never enters into hard breakdown but the gate stack is driven into the hard breakdown regime when the high-κ layer suffers from it as evidenced by the MIM-C breakdown characteristics. The progressive breakdown regime prior to gate stack hard breakdown is mainly due the degradation state of the interfacial layer [141].

4.3 Analysis with Stress-Induced Leakage Current

To further understand the breakdown process of high-κ/IL structures, stress induced leakage current was measured at low gate voltage. SILC represents the defects formation in oxide during CVS [146]. For TiN/HfO_2/SiO_2 (IL)/Si gate stack, due to defect generation, gate current increased at low gate voltage (Figure 4.6) when sensed after interrupting the applied stress voltage. More than two orders of magnitude increase in gate current (I_g) at V_g = 1V clearly defines the soft breakdown regimes in SILC. After approximately 513 seconds when hard breakdown occurred, saturation in gate current was observed.

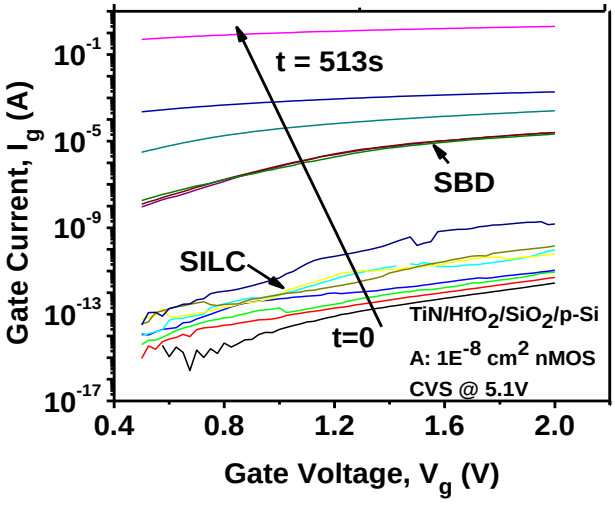


Figure 4.6 Stress induced leakage current (SILC) in TiN/HfO_2/IL (SiO_2)/Si. These I_g-V_g measurements taken at stress intervals show gradual increase in gate current for the measured voltage range. Few orders of magnitude increase in I_g is observed from SILC to soft breakdown mode.

For the 2nm ISSG SiO_2 capacitors (Figure 4.7), soft breakdown was clearly observed when gate current was measured within the range of V_g = 0-1.5V. Two orders of magnitude gate current increase at V_g = 0.5V indicates a significant conducting path formation inside the SiO_2 dielectric after soft breakdown. On the other hand, when gate

current was measured periodically interrupting stress voltage on MIM-Capacitors, no such change in gate current was observed till 2000s. Once the HfO_2 dielectric went into thermal breakdown or HBD, a sudden increase in I_g (almost 3 to 4 orders of magnitude) could be observed (Figure 4.8). SILC is limited in MIM-Capacitors used here compared to the ISSG SiO_2 capacitors. It is therefore, possible that observed SILC in gate stack is mainly due to the increase in gate current because of soft breakdown of the IL.

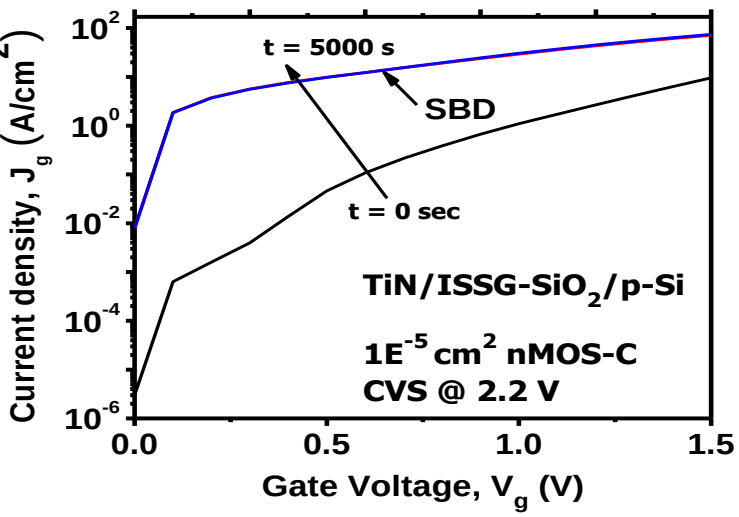


Figure 4.7 Stress induced leakage current (SILC) in TiN/SiO_2/Si nMOS-C.

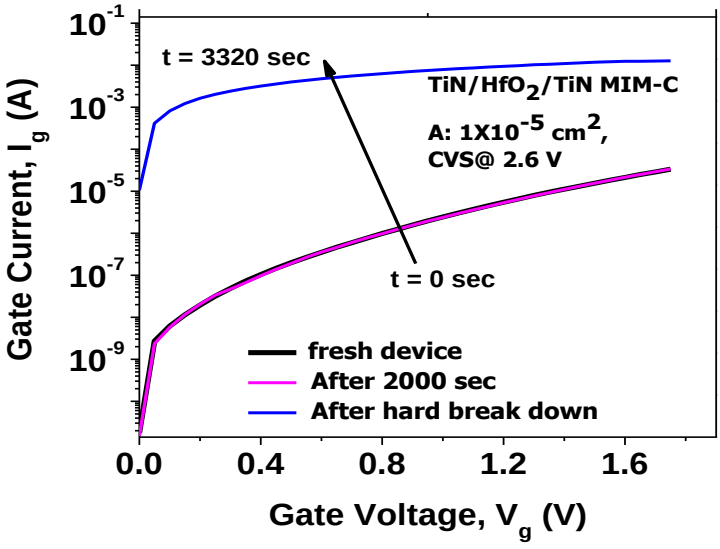
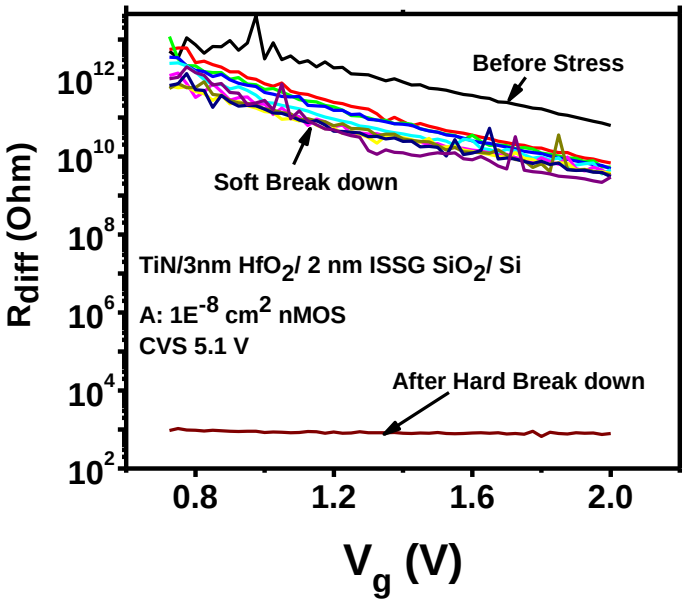


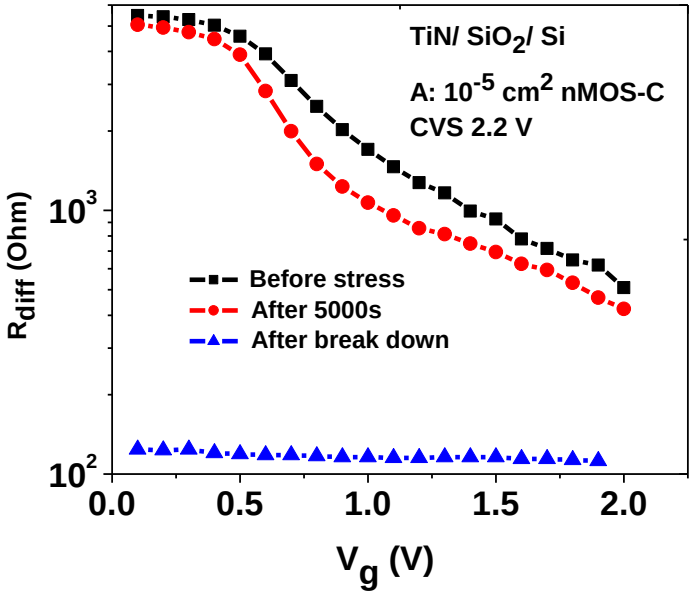
Figure 4.8 Stress induced leakage current (SILC) in TiN/HfO_2/TiN MIM-C. Sense current did not show any SILC in the form of a gate current increase.

4.3.1 Analysis with Differential Resistance

Differential resistance, R_{diff} ($\Delta V_g/\Delta I_g$), calculated from the SILC data, could be a measure of dielectric degradation [141]. Figure 4.9(a) shows gradual decrease of differential resistance of the gate stack (high-κ/IL) with stress time. R_{diff} drops significantly as the oxide goes into soft breakdown and then hard breakdown. It behaves like a conductor (low and constant resistance with gate voltage) after HBD. ISSG SiO_2 capacitors showed decrease in R_{diff} (Figure 4.9b) after soft breakdown (measured after 5000s), then after hard breakdown it reduces significantly and finally becomes constant. On the contrary, MIM-C (Figure 9c) showed no change in R_{diff} untill it reaches hard breakdown.

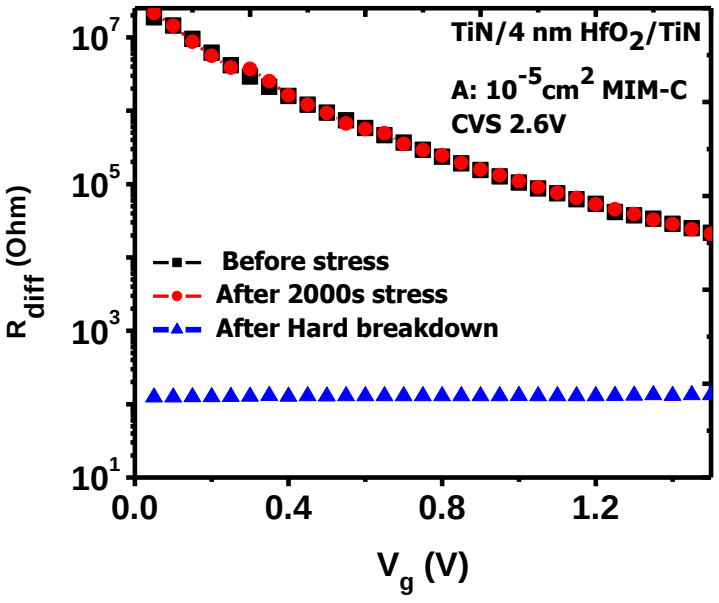


(a)



(b)

Figure 4.9 Differential resistance of the dielectric for (a) HfO_2/IL gate stack; (b) ISSG SiO_2-only nMOS-C; (c) metal-insulator-metal capacitors.



(c)

Figure 4.9 Differential resistance of the dielectric for (a) HfO_2/IL gate stack; (b) ISSG SiO_2-only nMOS-C; (c) metal-insulator-metal capacitors (continued).

It is, therefore, clearly evident from breakdown, SILC and differential resistance that the ISSG interfacial SiO_2 enters the soft breakdown mode much earlier and drives the gate stack into SBD mode and this initiates the gate stack breakdown process as the field across the high-κ layer increases. When the HfO_2 layer enters the HBD regime the entire gate stack suffers from hard breakdown.

4.3.2 Voltage dependence of SILC

In thick oxides (>4 nm), electrical stress-induced defects are mainly located in the bulk of the oxides and the stress-induced gate leakage (SILC) is dominated by bulk-trap-assisted tunneling and is independent of the size and polarity of sense voltages [147]. It represents a direct measure of trap density and thus is adopted as a monitor to assess oxide degradation [148]. But for thin dielectrics, use of low voltage SILC or LVSILC for gate voltage <1 V is widely used to investigate the stress induced defects at and near the

interface [149, 150]. For gate oxide thickness below 3.5 nm and stress voltages below 5 V, tunneling via interfacial traps created from stress causes SILC [150]. This LVSILC can be detected in low gate voltage regime. At the onset of higher sense voltages, this effect diminishes. For high-κ/metal gate nMOSFET, SILC during positive bias temperature stress (PBT) has drawn a lot of attention [33, 141,151]. The origin of SILC such as trap filling, trap creation, trap location or the nature of the traps for this multi-layer gate stack is still unclear.

In the previous section, SILC was mainly observed in the thin interfacial layer of high-κ gate stacks. A separate SILC study was performed on HfO_2-only and SiO_2-only devices. It was found that SILC was minimal in HfO_2-only devices but significantly observed for the SiO_2 devices [152]. It is also known that the intrinsic trap density in high-κ layer is much higher than in the interfacial layer. In a multi-layer gate stack, therefore, it is important to evaluate the stress-induced defect generation in the thin interfacial layer. SILC behavior of two different gate stacks with identical high-κ layer but different interfacial layer thickness has been studied. In addition to the multi-layer gate stack, a control device with SiO_2/metal gate has been considered. These SiO_2 reference devices were fabricated following identical process conditions as the interfacial layer of the high-κ gate stack. Normalized SILC has been defined as $\Delta I_g(t_s)/I_{g0} = [I_g(t_s) - I_{g0}]/I_{g0}$. Here I_{g0} and $I_g(t_s)$ are the current density before stress and after time, t_s respectively at a particular sense voltage.

4.3.2.1 Stress Voltage Dependence of SILC. Metal gate/high-κ nMOS capacitors were subjected to high field stresses in inversion and gate current was measured periodically interrupting stress. For each stress voltage $V_{g,stress}$, normalized SILC ($\Delta I_g/I_{g0}$) was calculated at low sense voltage from I_g-V_g curve measured for all stress intervals. A log-log plot of $\Delta I_g/I_{g0}$ with stress time shows power-law dependence for the experimental stress time window up to 1000 seconds (Figure 4.10). In this case, power-law exponent was found to be 0.66 for all stress voltages. This power law dependence was observed for short stress time, but for longer stress periods, saturation was observed for all stress voltages.

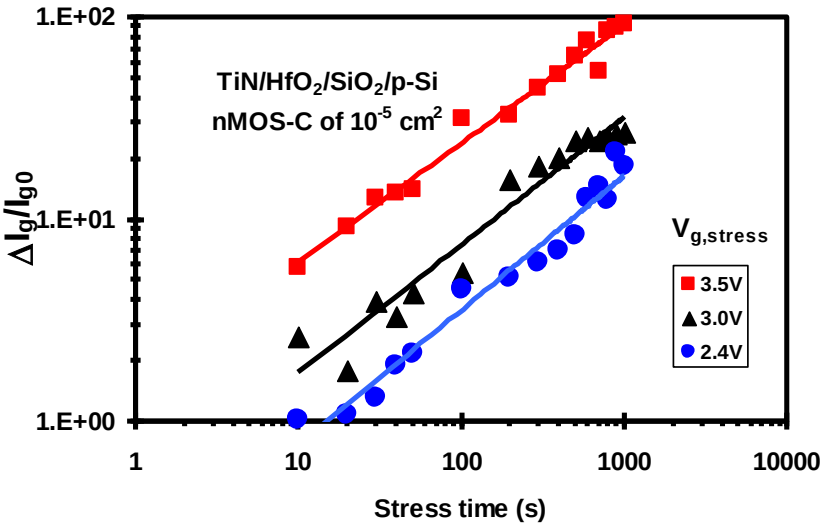


Figure 4.10 Stress voltage dependence of stress-induced leakage current for $TiN/HfO_2/SiO_2$ (3 nm/2.1 nm) nMOS capacitors (10^{-5} cm^2). For all stress voltages, SILC follows power law.

It was earlier reported that SILC has a power-law dependence on stress time [50], and the exponent of the power-law was reported to be 0.5 [152], which led to the explanation that trap generation is related to a (hydrogen) diffusion process through the

oxide. For the gate stack considered here, the power-law exponent of 0.66 indicates different precursor defects which are oxygen vacancies.

4.3.2.2 Sense Voltage Dependence of SILC. As shown in Figure 4.11, a peak in LVSILC is observed at low bias voltage (V_g = 0.3 V and 0.35V) after CVS at 2.4V and 3.5V respectively for the TiN/HfO_2/SiO_2/p-Si gate stack.

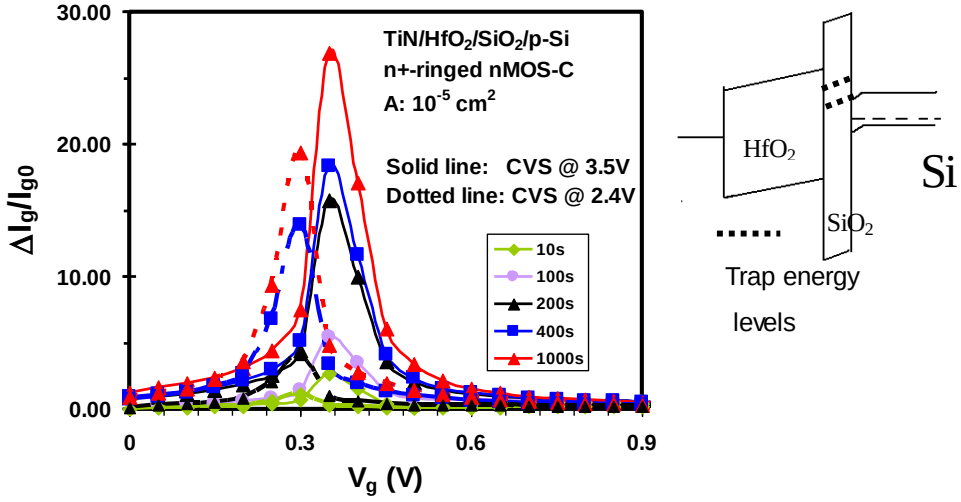


Figure 4.11 Sense voltage dependence of stress-induced leakage current for TiN/HfO_2/SiO_2 (3 nm/2.1 nm) nMOS capacitors (10^{-5} cm^2). Two different constant voltage stresses were applied at substrate injection mode. The lines are drawn for visual guide. The right figure is a schematic of the trap energy levels in the interfacial SiO_2 layer.

This behavior is mainly because of correspondence of the energy levels of electrons in Si conduction band with that of trap energy levels in the interfacial oxide. This has been schematically shown above. The trap energy levels in the interfacial layer matches with discrete energy levels of electrons in Si channel which could be detected by sensing LVSILC. Peak position shifts slightly with increasing stress voltage because of possible formation of discrete defect levels close to the interface.

An investigation of the SiO_2-only device (2 nm ISSG SiO_2 nMOS-C) reveals a LVSILC behavior that shows a strong sense- voltage dependence (Figure 4.12). The peak is observed around V_g=0.6V for this SiO_2-only devices. This dominant component is due to trap-assisted tunneling through newly generated oxide defects in the SiO_2 layer. This peak position of the normalized SILC for SiO_2-only devices (V_g = 0.6) varies from that of high-κ/metal gate stack (V_g = 0.3 or 0.35V). This difference is possible due to their thickness (EOT) variation. The similarity in SILC degradation indicates that interfacial layer plays a crucial role in the degradation of the gate stack by generating defects in short stress time. It was also discussed before that interfacial layer was degrading first in the gate stack breakdown process [152-154]. For that purpose, several degradation criteria such as gate leakage current characteristics during stress, differential resistance measured from SILC data and charge to breakdown were compared. Hence, it can be said that defects level located in the interfacial layer originates SILC and subsequently degrades gate stack to go into breakdown.

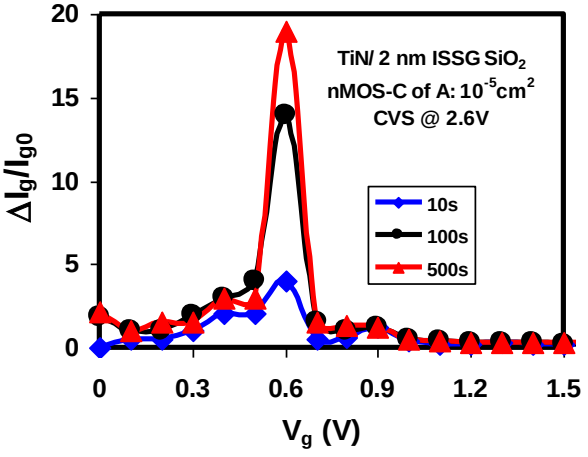


Figure 4.12 Sense voltage dependence of stress-induced leakage current for 2 nm SiO_2-only nMOS capacitor (10^{-5} cm^2) with metal gate. Constant voltage stress was performed at substrate injection mode (+2.6V).

4.3.3 Normalized SILC Comparison: Varying Interfacial Layer

Two different gate stacks with identical high-κ (3nm HfO_2) have been subjected to same constant voltage stress. Both of these gate stacks have ISSG SiO_2 layer as interfacial layer and thickness were 2.1 nm and 1.1 nm. Figure 4.13 shows current variation of these stacks before stress. Due to the total EOT difference, thinner interfacial SiO_2 stack shows higher leakage current. In addition, because of the interaction between the high-κ and the thinner interfacial layer the intrinsic trap density increase in a thinner layer as compared to a rather thicker interfacial layer (2.1 nm).

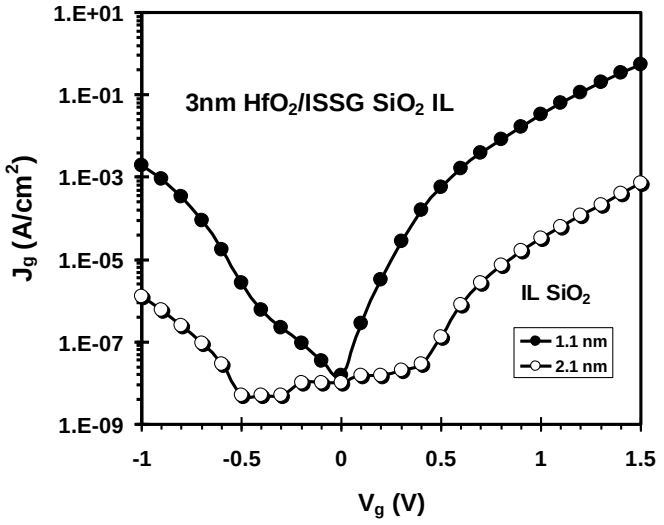


Figure 4.13 Before stress current comparison for different interfacial SiO_2 layer thickness. Both of these gate stacks have 3 nm HfO_2 layer.

As the normalized SILC growth was analyzed for both gate stacks, devices with thinner IL has lower $\Delta I_g/I_{g0}$ as a function of stress time as the current in the fresh device was higher (Figure 4.14). But a higher rate of increase (0.66 compared to 0.53) with stress time is observed for 2.1 nm SiO_2 layer gate stack as compared to 1.1 nm interfacial layer. Therefore, even though high-κ layer thickness was same for these two stacks, this

SILC growth is due to higher defects generation in the thicker interfacial layer. It was reported that high-κ layer does not really suffer from SILC where as interfacial oxide does degrade [35]. Assuming minimal contribution from high-κ layer one can conclude that thicker and better quality oxide degrades at a higher rate due to stress-induced defect formation in the interfacial layer.

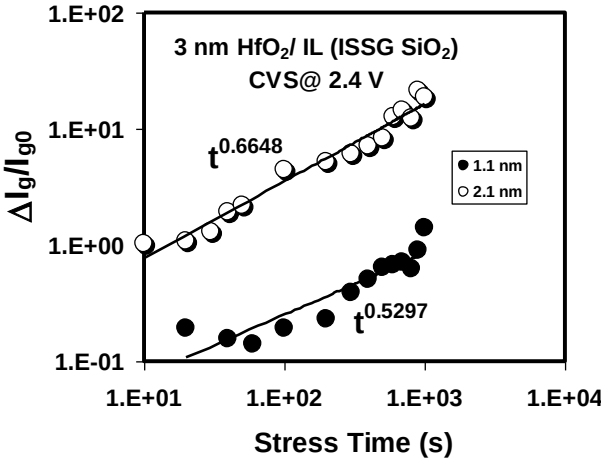


Figure 4.14 Normalized SILC comparison varying interfacial layer thickness. Thicker interfacial layer (2.1nm) showed more defect generation than thinner IL. High-κ thickness was 3 nm for both gate stacks.

4.4 Charge to Breakdown (Q_{BD}) Analysis

To further ascertain the impact of interfacial layer, the charge-to-breakdown (Q_{BD}) characteristics were estimated for the individual layers and the gate stack. When MIM-C was subjected to CVS with electric field 6.5MV/cm, Q_{BD} was observed to be $4.18\times10^{4} C/cm^{2}$. Separate breakdown study on single ISSG SiO_2 layer with 13.75MV/cm electric field showed a Q_{BD} of $4.94\times10^{7} C/cm^{2}$. The higher observed Q_{BD} value is mainly due to substrate injection [154]. Analytically, the leakage current characteristics of fresh ISSG SiO_2 capacitors show higher density of fixed charges in the dielectric. Also, in ultra-thin SiO_2, soft breakdown occurs fast whereas hard breakdown

takes longer time in most cases [32]. That resulted in a higher Q_{BD} when it was subjected to constant voltage stress. For the gate stack considered, the calculated breakdown charge, Q_{BD} was found to be $3.95\times10^{3} C/cm^{2}$ with average fields across the interfacial layer, E^{IL} ~ 18 MV/cm and high-κ, $E^{H\text{-}\kappa}$ ~3.5 MV/cm. The fields were estimated similar to the reference [142]. It is known that because of the difference in dielectric constant between ISSG SiO_2 and HfO_2 most of the voltage drop occurs mostly across the ISSG SiO_2. Figure 4.15 shows Q_{BD} distribution with electric filed across the dielectrics for MIM capacitor, ISSG SiO_2 and high-κ/IL gate stack under substrate injection.

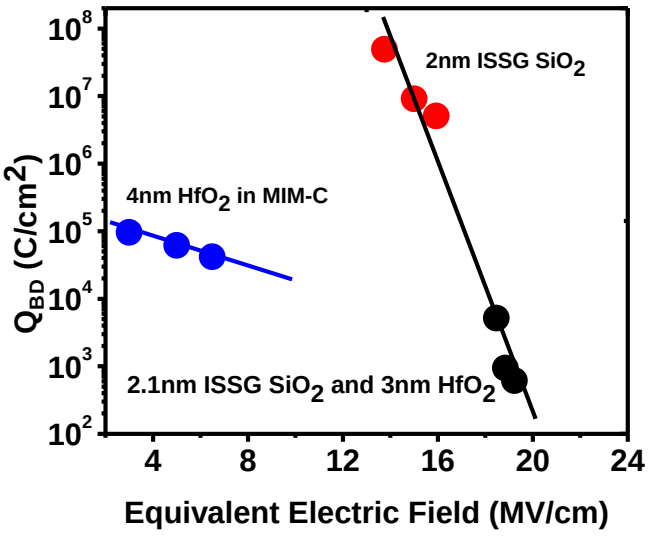


Figure 4.15 Q_{BD} vs. equivalent electric field for high-κ gate stack, MIM capacitor and SiO_2-only devices under substrate injection. An agreement is observed for the gate stack and SiO_2-only devices.

A good agreement between gate stack and ISSG SiO_2 data for identical interfacial layer thickness is visible. This further confirms that the breakdown of ISSG SiO_2 layer determines the breakdown of the entire gate stack. Additionally, because the interfacial layer went into soft breakdown within short period of stress under substrate injection, it

immediately caused hard breakdown in high-κ layer subjecting the entire gate stack to HBD.

4.5 Constant Voltage Stress at Elevated Temperature

Gate stacks with high-κ gate dielectrics with metal gates are typically implemented in multiple layers as mentioned earlier in this chapter. It was reported that possible trap creation in the interfacial layer dominates the breakdown mechanism in a metal/high-κ/interfacial layer/Si gate stack when subjected to a constant voltage stress (CVS) at room temperature [141, 154]**.** For accurate estimation of operating voltage extrapolation, it is required that time dependent breakdown study be evaluated at an elevated temperature. Further understanding of temperature dependence of high-κ/IL gate stack can be achieved by investigating the response of the individual layers in the breakdown process. Temperature dependence of SiO_2 breakdown has been studied extensively [155-159]. For ultra-thin SiO_2, temperature dependence of time to breakdown (T_{BD}) and Weibull slope, β was described as thickness effect based on the percolation model [160]. It has been also suggested by Wu *et al.* that the strong temperature dependence on ultra thin oxides is due to the voltage-dependent defect generation rate [43]. Identical mechanism can be considered for the gate stack as the interfacial layer often is SiO_2, even though the interfacial oxide is not thermally grown. For high-κ gate stack, it has been reported that thermochemical breakdown mechanism is the primary degradation mechanism at high temperature [161]**.** Okada *et al.* [162] also reported that temperature dependence of TDDB lifetime in high-κ stacked gate dielectrics depends on the minority current through the high-κ dielectric and the trap creation. Along with T_{BD} study on the

high-κ/IL gate stack, it is critical to look at the SILC at elevated temperatures because both the initial current and the SILC are temperature dependent [151]. The SILC behavior of high-κ/SiO_2 gate stack has been studied in the literature [151,163]. It has been observed that SILC is due to assisted tunneling via trapped positive charges and neutral traps generated in the high-κ dielectric layer during stress in gate injection mode [32]**.** It was also reported that for substrate injection the bulk HfO_2 trap density is directly related to the SILC and at low stress voltage SILC will not be a reliability constraint at room temperature. Therefore, for further understanding of breakdown mechanism of high-κ/IL gate stack, it is essential to look at the temperature dependence of T_{BD} and SILC of the multi-layer gate stack structure as well as the behavior of individual layers.

In this Chapter, SILC study on high-κ/IL gate stack, IL-only and high-κ-only suggests that IL is significantly contributing to stress current in breakdown at elevated temperature. In addition, we observe that the Weibull slope, an important parameter for the reliability projections, depends on the oxide thickness and the BD distributions become broader as oxide thickness decreases [32]. The activation energy of time to BD extracted from Weibull distributions show that the defects formation in high-κ layer is also contributing to the overall breakdown at high temperature**.** It was, therefore, demonstrated that (i) IL causes higher SILC for the high-κ/IL gate stack at elevated temperature for substrate injection, (ii) Weibull slope of T_{BD} increases with temperature for the entire gate stack, and (iii) an Arrhenius temperature dependence of T_{BD} in oxide breakdown.

4.6 Temperature Dependence of SILC

When ultra thin oxides were subjected to CVS, they showed low voltage SILC due to trap-assisted tunneling through positively charged oxide traps and also normalized SILC ($\Delta J/J_0$) is proportional to trap density [149]. Figure 4.16 shows the normalized SILC increase with stress time in ISSG SiO_2-only oxides when sensed in depletion regime (V_{sense} = + 0.6V). Because $\Delta J/J_0$ is proportional to injected charge and follows power-law dependence [164], at room temperature, it shows an increase with stress time with an exponent of 0.1. Due to enhanced defect creation at higher temperature (50^0C is the investigated temperature here), the normalized SILC has a higher exponent (0.5). It is possible that higher SILC at higher temperature is also caused by the temperature enhanced conductance via existing traps, which can be seen from the I_g-V_g curve taken at room temperature and at a high temperature before stress. But an observed increase in SILC with stress time at higher

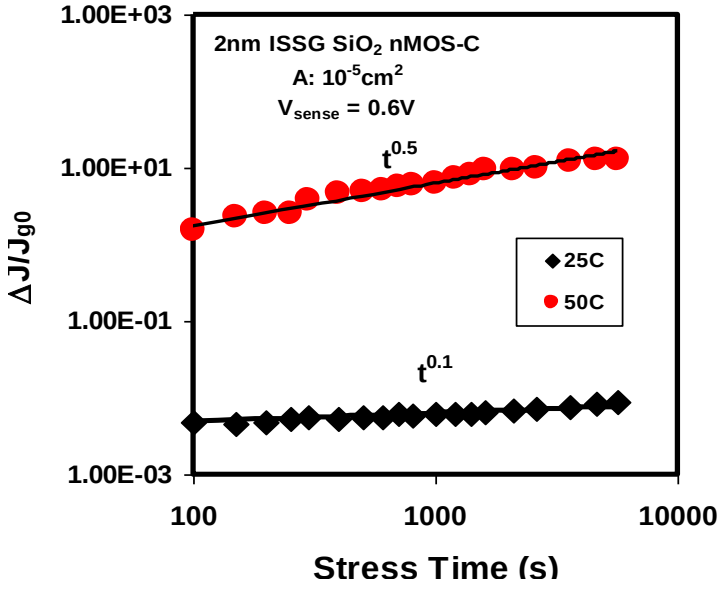


Figure 4.16 Temperature dependent time evolutions of the SILC of TiN/ISSG SiO_2 nMOS capacitors under substrate injection.

temperature indicates enhanced trap generation in the oxides. It can be noted that the total gate current $I_{g,\ measured} = I_{tunnel} + I_{SILC}$ where the tunneling current is the current through the ideal oxides without any traps [137]. The density of neutral electron traps increases during stress and a gradual increase in SILC is observed [138]**.** But the tunneling current does not change as the stress continues. The results have considered change in measured current (I_{g2}-I_{g1}) at two different stress times to account for the change in SILC or oxide trap density. For the stress voltage used in the experiment of ISSG SiO_2–only capacitors (2.2V) and the current density data shown in the stress time range (100 sec+), the SILC component is the changing component in leakage current density [137]. Therefore, ΔJ_g accounts for the change in SILC only.

The high-κ/IL gate stack was then subjected to constant voltage stress at different temperatures and low voltage SILC was measured under substrate injection (Figure 4.17a).

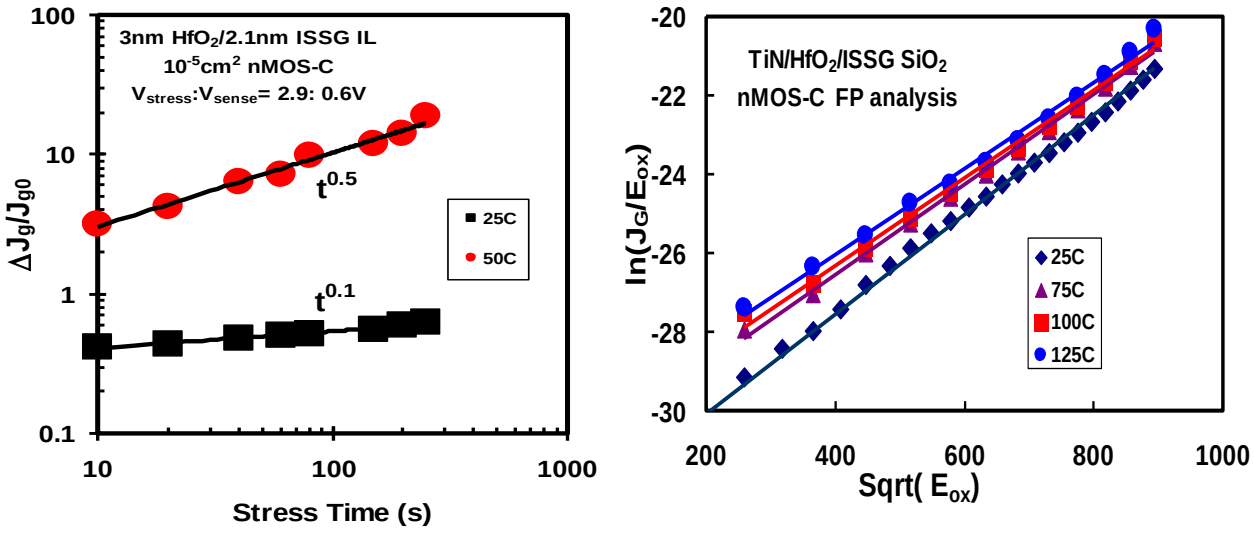


Figure 4.17 (a) Temperature dependent time evolutions of the SILC and (b) Frenkel-Poole plot for leakage current of TiN/HfO_2/ISSG SiO_2 nMOS capacitors under substrate injection.

Normalized SILC of this gate stack shows dependence on both stress time and temperature. The power exponent increases due to enhanced trap creation in the gate stack. The evolution of $\Delta J/J_0$ of the gate stack which has ISSG SiO_2 shows similar dependence on injected charge and temperature, which indicates a significant increase in SILC in the interfacial layer. This observed field and temperature dependence of the leakage current in high-κ/IL gate stack may be due to temperature sensitive Frenkel-Poole (FP) conduction mechanism [165] through the gate stack. As the temperature was increased, electrons tunnel through interfacial layer and then conduct through the intrinsic traps in HfO_2. According to F-P model, the leakage current density, J_G and Electric field, E has the following relation

$$J_G \propto E \exp\left[\frac{-q\left(\phi_B - \sqrt{qE/\pi\xi_0^*}\right)}{\mathrm{K}_B T}\right] \tag{4.1}$$

Where ϕ_B is the barrier height or trap depth K_B is the Boltzmann constant and T is temperature. Figure 5.2b shows a Frenkel-Poole plot (ln (J_G/E_{OX}) vs. $\sqrt{}(E_{OX})$ is straight line) of the leakage current through gate stack for electrons injected from the substrate at all four observed temperatures. As the barrier height is modulated by the electric filed, the emission probability increases, leading to an enhancement in the emission rate and an increase in J_G. Because the barrier height has temperature dependence, a slight change in the slope can be observed with temperature.

MIM capacitors show a three orders of magnitude increase in leakage current at 50 ^{0}C compared to room temperature when sensed at V_g = 0.6V but was not sensitive to the stress time (Figure 4.18) as observed in case of interfacial layer and in the gate stack. This indicates minimal defects generation in HfO_2 of MIM-C during stress at elevated temperature. The increase in stress current in gate stack is, therefore, mostly due to the current increase in IL and conduction through intrinsic traps in the high-k layer. It can also be noticed that the power law dependence of SILC in SiO_2-only capacitors is similar to that of the gate stack. Temperature activated defect generation can be explained in terms of hydrogen release model that contributes to defect generation and breakdown of thin SiO_2 as proposed by Ribes *et al.* [166] based on the multi-vibrational excitation of Si-H bonds near Si-SiO_2 interface releasing hydrogen. Desorption of hydrogen creates weak link in the oxides leading to dielectric breakdown.

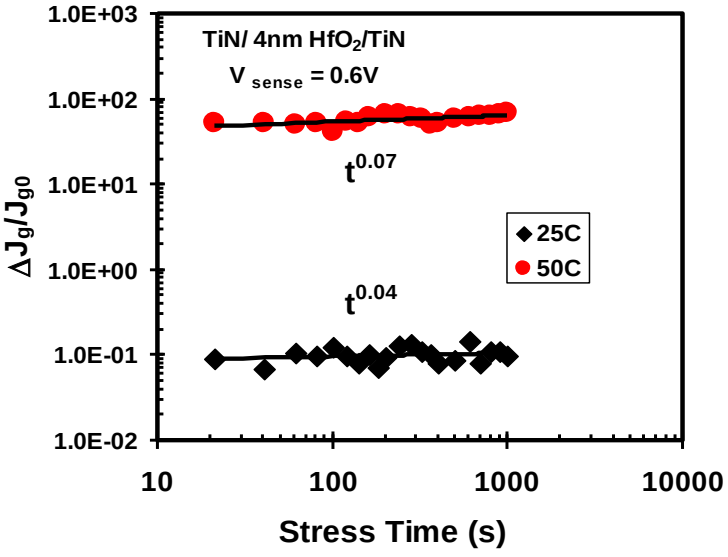


Figure 4.18 Change in leakage current in HfO_2 based MIM capacitor with Stress time at room temperature and 50^0C. At V_g = 0.6V sense voltage, leakage current has low dependence on stress time.

The gate stack considered here has an interfacial layer consisting of an interfacial SiO_2 on Si substrate. So, hydrogen release is possible source of defects creation in the gate stack during SILC and/or TDDB. Further work needs to be done to provide a comprehensive understanding based on a specific degradation mechanism in the high-κ layer, especially for MIM capacitors.

4.7 TDDB: Temperature Dependence

As TDDB data of the gate stack was analyzed under substrate injection, the thermochemical model can be used since this model is useful at low applied field and low leakage current [167].

$$\ln(T_{BD}) \propto \frac{\Delta H_0}{k_B T} - \gamma E_{OX} \tag{4.2}$$

Where T_{BD} is time-to-breakdown; ΔH_0 is the enthalpy of activation for bond breakage, γ is the field acceleration parameter given by the physical parameters; E_{ox} is the externally applied electric field and k_B is Boltzmann's constant. It further shown that ΔH_0 and γ decreases and increases with κ as shown below.

$$\Delta H_0 = \Delta H_0^* - p_0\left(\frac{2+\kappa}{3}\right)E_{OX} \tag{4.3}$$

$$\gamma = \frac{p_0\left(\frac{2+\kappa}{3}\right)}{k_B T} \tag{4.4}$$

Where ΔH_0^* is the activation energy in the absence of field and p_0 is molecular dipole-moment component opposite to local field. The temperature dependence on the time-to-breakdown data is observed for the high-κ/IL gate stack (Figure 4.19).

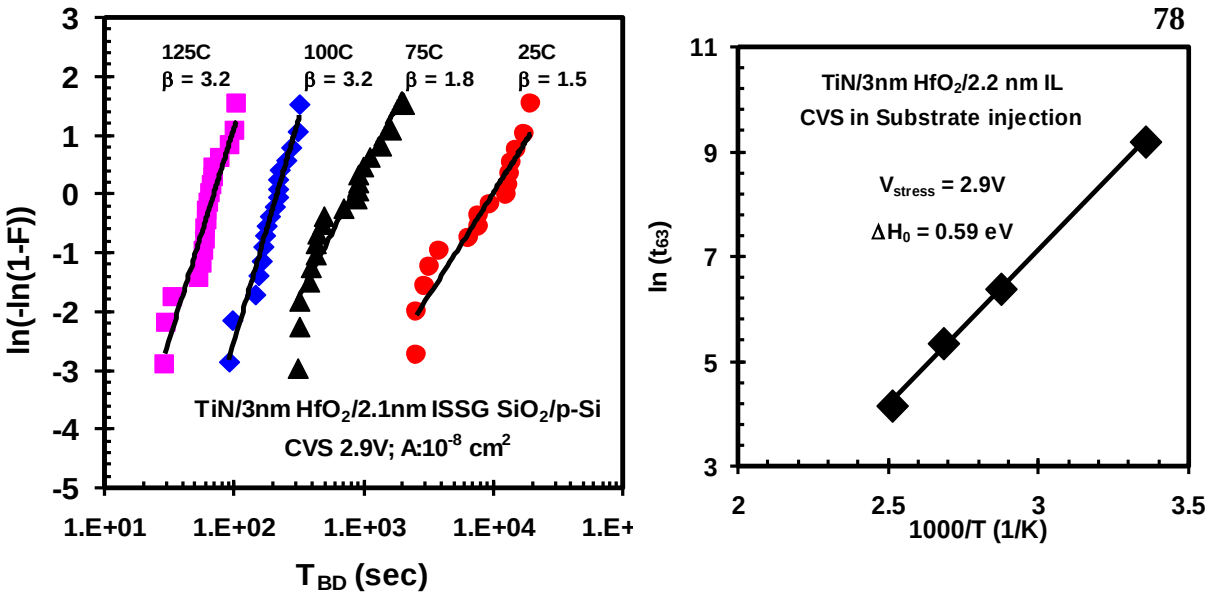


Figure 4.19 Weibull plots of T_{BD} at different temperatures for 3nm HfO_2/2.1nm ISSG SiO_2 capacitors and Arrhenius plot of T_{BD}.

The low Weibull slope, β =1.5 was observed at room temperature from the single mode distributions of mostly intrinsic population. The higher β value at elevated temperature could be due to temperature sensitive defects and possible redistribution in high-κ layer. The activation energy derived from the Arrhenius plot of the 63% value of time-to-breakdown. For this HfO_2/SiO_2 gate stack, ΔH_0 was found to be 0.59eV. Yamaguchi *et al.* [161] also observed activation energies approximately ~0.55eV for thermal activation process in high-κ materials and current induced degradation on dielectric breakdown. It is known that the trap creation and distribution in high-κ materials are highly temperature dependent [168]**.** Because of temperature enhanced detrapping various energy levels are exposed at higher temperatures.

The MIM capacitors with HfO_2-only showed higher temperature dependence as we analyze their statistical distribution plots (Figure 4.20).

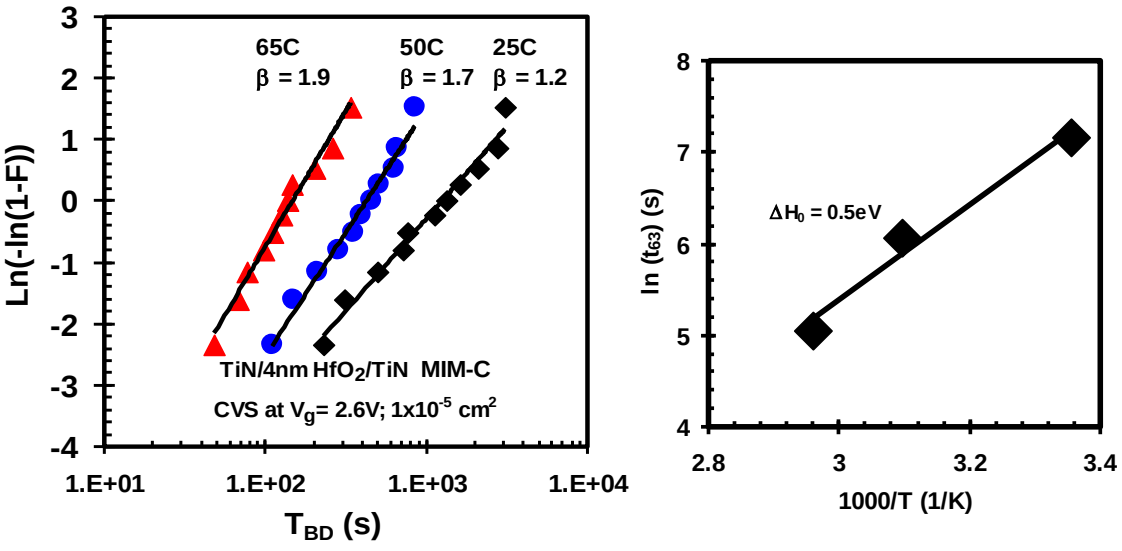


Figure 4.20 Weibit plot of T_{BD} at different temperatures for 4nm HfO_2 based MIM capacitors and Arrhenius plot of T_{BD}.

The T_{BD} distribution of MIM-C is found to be sensitive to temperature. It can be noted that lower electronegativity for Hf (which has electronegativity of 1.3) compared to Si (1.8) causes a higher field acceleration parameter of time-to-breakdown for high-κ material than Si [169]. The activation energy in the presence of field was found to be 0.5eV. It is possible that the post deposition anneal at 800^0C forms a microcrystalline Hf-silicate in MIM structure [133]**.** Although, Weibull slope, β is affected by the degree of crystallinity of Hf-silicate films, filed acceleration factor γ changes insignificantly. Therefore, for qualitative comparison purposes $TiN/HfO_2/SiO_2$ and MIM can be evaluated in breakdown study of the high-κ layer.

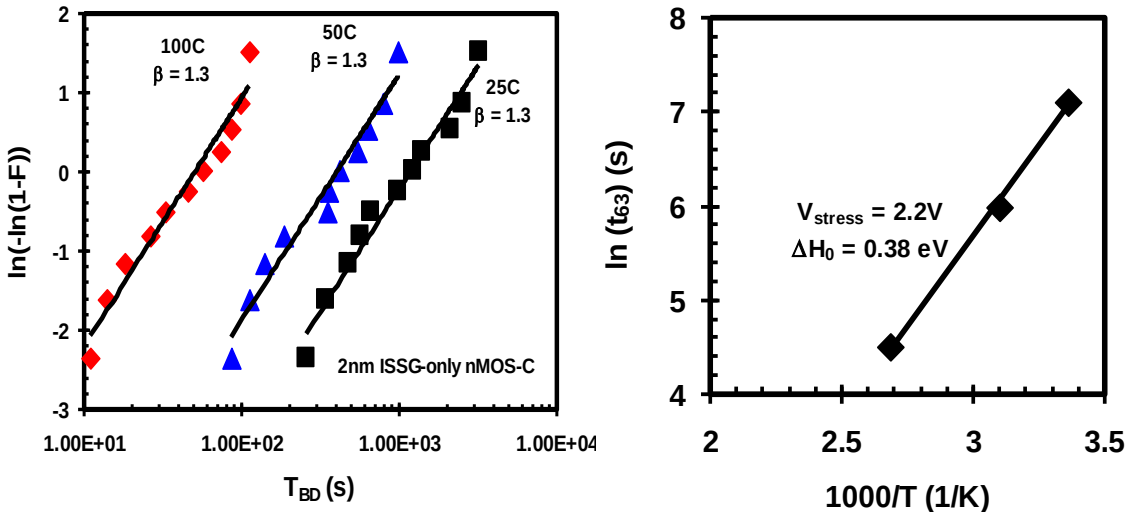


Figure 4.21 (a) Weibit plot of T_{BD} at different temperatures for 2nm ISSG SiO_2 based nMOS capacitor and (b) Arrhenius plot of T_{BD}.

Figure 4.21 (a) shows cumulative distribution failure of time to failure (T_{BD}) results obtained for different temperature at a given stress voltage V_g = 2.2V for ISSG SiO_2-only capacitors. The time at which soft breakdown begins was used as the definition of device failure for these ultra thin oxides. The Weibull slope was found to be 1.3, constant at all observed temperatures. The β value of 1.3 is reported for conventional SiO_2 [43]. Since no significant temperature dependence of the Weibull slope was observed it is believed that trap distribution in ISSG SiO_2-only layer did not change significantly. The temperature activation energy of 0.38eV was obtained from Arrhenius plot (Figure 4.21(b)) for these oxides. This further confirms that the breakdown process in these gate stacks depends on both stress induced leakage current and defect creation and distribution in the dielectric layers. The low activation energy in ISSG SiO_2-only layer makes it responsible for initiating the gate stack breakdown at higher temperature.

The trap distribution in the high-κ layer, on the other hand, contributes to the ultimate breakdown of the gate stack when temperature is increased.

4.8 Chapter Summary

TDDB characteristics of the gate stack (TiN/HfO_2/ISSG SiO_2/p-Si) were studied. To separate out the contribution of HfO_2 and SiO_2 layer in gate stack breakdown, MIM-C of HfO_2 film and ISSG SiO_2 capacitors were individually investigated. Both high-κ /IL and in-situ steam growth SiO_2 based MOS devices showed similar progressive breakdown and SILC degradation, but MIM capacitor showed only the hard breakdown behavior as a constant stress current was observed until hard breakdown. Higher SILC growth rate was observed for gate stack with thicker interfacial layer (IL) compared to gate stack with thinner IL. It can be inferred that discrete levels of trap generation in the interfacial layer primarily causes low voltage SILC in metal/high-κ gate stacks and initiates the gate stack breakdown. Based on observed I-t, SILC, R_{diff} and Q_{BD}, it can be concluded that breakdown of interfacial layer initiates breakdown of metal gate/high-κ/SiO_2/Si gate stacks at room temperature.

TDDB characteristics of the gate stack (TiN/HfO_2/ISSG SiO_2/p-Si) were also studied at elevated temperature. The normalized SILC shows power-law dependence with stress time at both room and high temperature. The exponent in power law dependence seems to be sensitive to stress temperature. The stress dependent $\Delta J_g/J_{g0}$ and activation energy found from Weibull distribution of the time-to-breakdown data show IL initiates the gate stack breakdown at higher temperature. The Weibull slope, β increases with temperature for the gate stack and HfO_2-only MIM capacitors. Therefore, it can be added

that the breakdown of the high-κ layer ultimately causes catastrophic breakdown of the gate stack during substrate injection at elevated temperature.

CHAPTER 5

CORRELATION OF NEGATIVE BIAS TEMPERATURE INSTABILITY AND BREAKDOWN

5.1 Introduction

The CMOS devices with HfO_2 have shown significant improvement in terms of minority carrier mobility and device performance [170]. Recently, various reliability issues for this new dielectric stack are getting a lot of attention. Separate studies on Negative Bias Temperature Instability (NBTI) and Time Dependent Dielectric Breakdown (TDDB) have been performed extensively on high-κ/metal gate stacks [87, 92, 144, 171-175]. All these gate stacks are normally multi layer structures with high-k and an interfacial layer (IL) of SiO_2. Therefore, high-κ layer and IL can contribute differently to any stress-induced degradation depending on various parameters such as quality, thickness.

It was explained using physics based model that the change in threshold voltage, ΔV_{th} during NBTI is predominantly due to depassivation of Si-H bonds at the oxide/Si interface [172]. The subsequent diffusion of hydrogen also generates defects in the bulk of the dielectrics in addition to leaving behind a positively charged interface defect. In another model, based on dispersive transport of protons (H^+) in the gate stack, it is suggested that hydrogen from the interstitials near the Si/SiO_2 interface diffuses into the gate stack and induces over coordinated oxygen centers [173]. Besides, because of the interaction of high-κ with the IL which contributes to additional defect formation in IL [176], the SiO_2 IL in gate stack may exhibit harsher degradation kinetics during NBTI as compared to conventional SiO_2. For TDDB in gate injection mode, on the other

hand, bulk defects are generated in both the high-κ and IL-SiO_2 prior to dielectric breakdown. When the traps start to overlap, it results in a conduction path formation that leads to soft breakdown (SBD) in high-κ gate stack [87]. As the stress continues, successive SBDs are created in the device that results in hard breakdown (HBD) of the gate stack. It was reported that defect generation in the IL-SiO_2 is the main cause of the conduction path formation and hard breakdown of the entire gate stack [177]. In any case, a constant voltage stress is applied in inversion mode at elevated temperatures and at room temperature for NBTI and for TDDB respectively. Defects generation process leads to threshold voltage variation in NBTI and in case of TDDB the dielectric breaks down when the number of defects reached a required level (N_{bd}). When the TDDB is performed at an elevated temperature the breakdown process is accelerated because of the temperature dependence of N_{bd} [162].

But there are very few reports exist on the correlation of these very important reliability issues. In case of NO-oxynitrides, Tsujikawa *et al.* [178] demonstrated the generation of bulk charge traps in the gate dielectrics during NBTI due to hydrogen atoms released from the interface and further demonstrated using stress induced leakage current (SILC) and TDDB that the same mechanism is responsible for both NBTI and TDDB in pMOSFETS. For high-κ gate stacks, Okada *et al.* has discussed TDDB and BTI reliabilities based on the impact of the intrinsic traps in high-κ layer [179]. The quality of high-κ layer and interfacial layer not only contributes to the different intrinsic defect formation but also responds to the degradation techniques differently [180]. Therefore, the nature of intrinsic defects can significantly impact the mechanism of NBTI and TDDB. Since the high-κ gate stack constitutes multiple layers of dielectric it is

imperative that the different combination of high-κ and IL needs to be studied to draw definite conclusions. Besides, it is also important to resolve whether the high-κ layer of interfacial layer is the weak-link for both the techniques. In this chapter, multiple gate stacks have been considered with different combinations of high-κ and interfacial layer thickness and process conditions to establish a direct correlation between the type of defects created by NBTI and TDDB. We have also performed TDDB measurements at elevated temperatures to evaluate the type of defect formation. It was also observed that both NBTI degradation and TDDB depend mostly on the quality and thickness of the interfacial layer.

Table 5.1 Gate Stacks with Various High-κ and Interfacial Layer Quality and Thickness

Lot #	Gate	HfO_2	IL	PreDA	PostDA
1	ALD TiN	ALD 2.6 nm	1.1nm ISSG	None	NH_3 700^{0}C 60s
2		ALD 3nm	0.7nm ISSG; 1.1nm ISSG or ChemO	NH_3 700^{0}C 60s	NH_3 700^{0}C for ISSG and 600^{0}C for ChemO 60s
3		ALD 5nm	1.1 nm ChemO	None	NH_3 600^{0}C 60s

TiN/HfO_2/SiO_2/Si gate stacks were used for this study (Figure 5.1). The list of various splits considered here is included in Table 7.1. For some samples, 2.1 in-situ steam grown (ISSG) interfacial layer (IL) was grown first on Si substrate, and then etched back to 1.1 and 0.7 nm. For some other devices, chemical SiO_2 oxide (Chem_O) of thickness (1.1 nm) was also used as IL. Two different interfacial layers, processed at different conditions (ISSG and Chem_O), were used to implement different quality of the IL oxide as it was reported earlier that ISSG oxide is of better quality than Chem_O in terms of defects [180]. For all the samples considered in this study, HfO_2 film (3 and 5

nm) was deposited by ALD method using TEMA ($Hf[N(CH_3)(C_2H_5)]_4$) precursors and O_3 oxidation [130]. For the gate electrode, a 10 nm TiN metal gate was deposited by ALD at 530^0C. The deposition rate of TiN film was 1.2 Å/cycle for this process condition. n+ poly silicon was then deposited on top of TiN layer. All pMOSFETs were fabricated using standard CMOS process flow which included 1000^0C dopant activation and forming gas anneals. Pre-deposition surface treatment by annealing in NH_3 ambient at 700^0C for 60s was done for all sample types. Also 60s Post-DA has been carried away in NH_3 at 700^0C. For NBTI and breakdown electrical measurements, stress-sense-stress sequence was followed using an HP 4145B semiconductor parameter analyzer. Approximately 15-20 samples were used for each measurement to plot the average data.

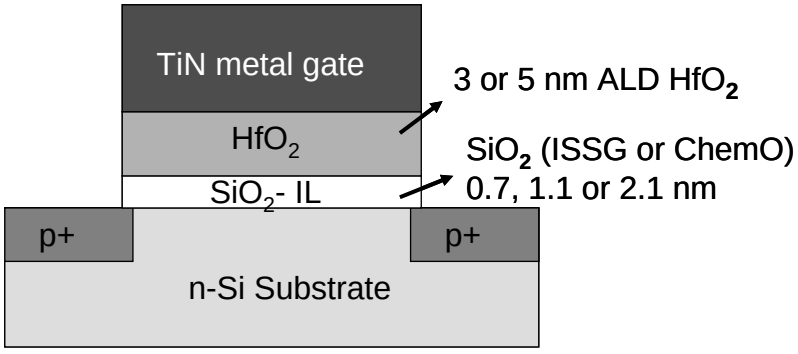
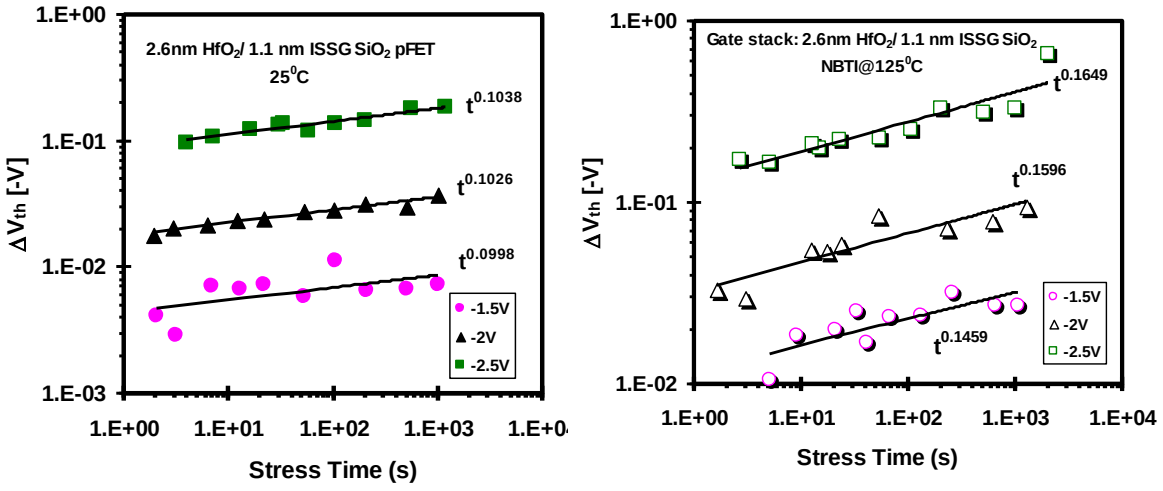


Figure 5.1 Schematic of the gate stack of $TiN/HfO_2/SiO_2/n\text{-}Si$.

5.2 NBTI Degradation with Time and Temperature

Figure 5.2 shows NBTI time evolution for various stress voltages. The room temperature data in Figure 5.2(a) suggests that the time dependence of ΔV_{th} follows a power law with an exponent value *n* of ~0.1 for the measured time range. The low exponent value is possible due to the multi-layer structure of the gate stack compared to a single oxide

layer. Exponent values ~0.1 was also observed during NBTI for multi-layer high-κ gate stacks [181-182]. It can be further explained by initial charge trapping at the trap sites in the early stage of stress, especially due to hole capture at these sites [179, 181- 182]. Also, this time exponent did not vary with the applied stress voltages, which further confirms similar degradation mechanism for all applied voltages. The threshold voltage was determined from the linear drain current I_{DLIN}. For the 125^{o}C temperature, the time exponent value was found to be $0.14< n <0.16$. The *n* value (~0.16) is consistent with that of the conventional SiO_2 devices, predicted by the reaction-diffusion model for longer stress times [99]. Since the exponent, *n* represents the defect generation rate in the dielectric the variation from 0.1 and 0.16 for room temperature and 125^{0}C respectively in Figure 5.2(a) and 2(b) clearly shows the temperature dependence. As this gate stack has a SiO_2 (ISSG) interfacial layer between HfO_2 and silicon substrate, it is possible that this ΔV_{th} is mostly due to the generation of NBTI induced interface trap density, N_{it} and bulk traps created by holes or hydrogen-related species diffusion in the IL as well as high-κ layer [182]. A higher slope was expected (~0.25) if the change in threshold voltage, ΔV_{th} was only due to change in interface states [179]. The ΔV_{th} variation clearly indicates positive charge trapping which can occur in both the interfacial layer as well as high-κ layer. It is known that the occupied deep gap states due to neutral and positively charged oxygen vacancies in HfO_2 can act as hole traps [180].



(a) (b)

Figure 5.2 NBTI Time evolutions of gate stack (2.6nm HfO_2/1.1 nm ISSG SiO_2) for various gate stress voltages at (a) room temperature and (b) 125^0 C. The degradation rate (power-law exponent, n) is independent of the applied bias. A comparatively low n was observed for these high-κ gate stacks.

5.3 Time-to-Breakdown Comparison during NBTI and TDDB

To make a comparison study of time to breakdown, the time required to 10% increase of ΔV_{th} was defined as T_{BD} during NBTI. Time-to-breakdown, observed from both NBTI and TDDB was also recorded at various temperatures for gate injection mode as shown in Figure 5.3(a). Because of the higher defect generation rate at elevated temperature, an accelerated breakdown was observed for both the case for the measured temperature ranges. It can be mentioned that for the HfO_2/SiO_2 gate stack, an increase in Weibull slope, derived from statistical distribution of T_{BD}, was also observed with increase in temperature [183]. For both cases gradual degradation process was observed and temperature seems to be a key factor in enhancing the degradation process. Two major models, field-driven *E* and fluence-driven *1/E*, explain field and temperature dependence

of dielectric degradation during TDDB and seems to be complimentary [184]. The mechanism that contributes to defect generation and trapping due to both the techniques is mainly due the injection of high energy electrons from the cathode (gate in both cases) that generate a positive species, either holes or hydrogen-related species near the anode (substrate-IL interface) (Figure 5.3(b)). These positive species degrades the interface and create bulk traps in the interfacial layer as well as in high-κ layer. As a consequence field-induced degradation can be significant. This is similar to SiO_2 but the injection probability increases due to lower barrier height of high-κ layer during gate injection [185]. Even though TDDB is "percolation path" driven, i.e. bulk trap generation must necessarily occur to a certain extent before TDDB could happen, during TDDB, high-κ has a faster defect generation rate than IL, but the gate stack does not go into breakdown until the defects in the IL completes the percolation path from gate to substrate. Bulk traps generation do occur during TDDB and NBTI, but NBTI helps to isolate the defects created at the interface and interfacial layer which are crucial factor for determining complete gate stack breakdown. The identical degradation trend in both the cases as a function of temperature in Figure 5.3 (a), therefore, suggests that the origin of defects creation during NBTI and TDDB are related.

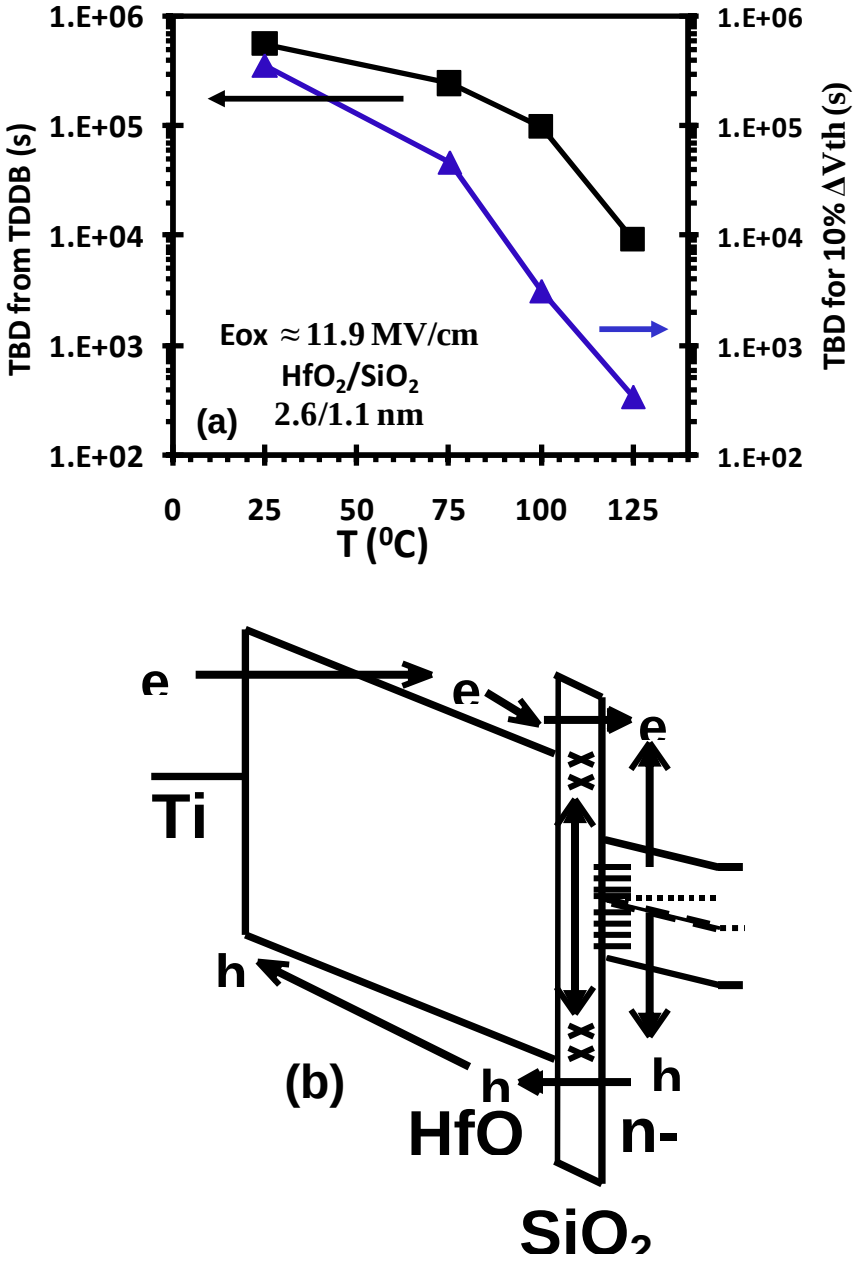
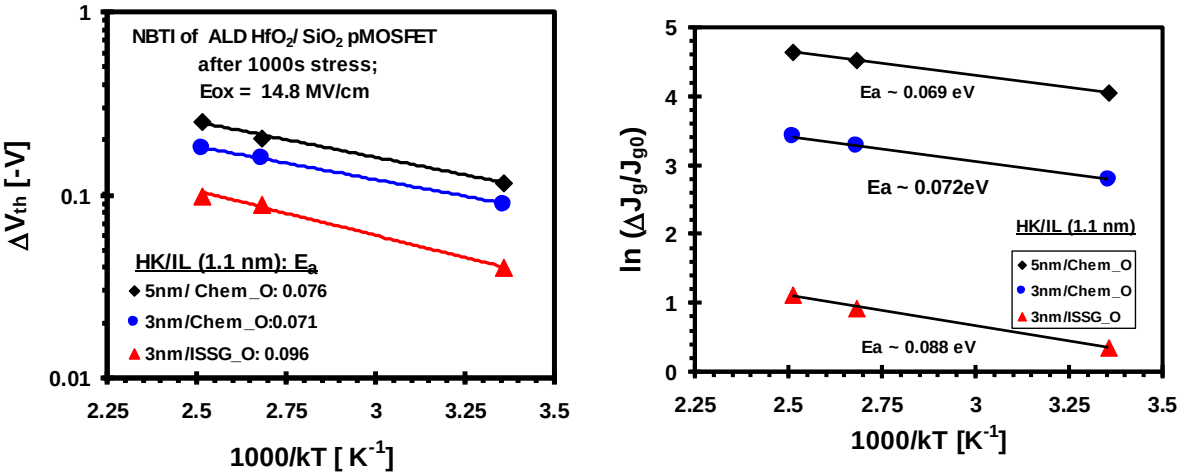


Figure 5.3 (a) T_{BD} (defined as, time for 10% increase in threshold voltage during NBTI) (triangles) and time-to-breakdown (squares) during TDDB at various temperatures show similar degradation trend and (b) shows the energy band diagram to depict the process of defects generation during the constant voltage stress.

5.4 Activation Energy of ΔV_{th} and SILC

To evaluate the temperature dependence of NBTI and TDDB, we further estimated the activation energies of defects created during both the degradation process. Figure 5.4 (a) shows the activation energy (E_a) extracted from NBTI measurements performed on various samples with different high-κ thickness and IL. The defects generated are typical of the Frenkel-pair with V_o^{++} [186]. Gate stacks with 3 nm and 5 nm HfO_2 and identical chemical oxide IL have demonstrated almost same E_a (around 0.07 eV). But when E_a of the gate stacks of chemical oxide and ISSG IL with identical high-κ (3 nm ALD HfO_2) were compared a difference in the activation energy is observed. This lower E_a of chemical oxide IL (0.07 eV) compared to ISSG IL (0.09 eV) indicates defect types and concentration in the interfacial layer can be different *i.e.* the quality of IL plays an important role. Degraeve *et al* [187] also suggested that NBTI degradation in high-κ gate stacks is dominated by the interface layer quality and it does not depend on the high-κ composition, thickness or quality. In addition, suppression of electron current during gate injection towards silicon substrate beyond the SiO_2 interface layer by a high quality interfacial layer is considered for NBTI improvement [186]. The inferior quality of the chemical oxide also tends to dominate the defect generation process and type of defect creation in the gate stack. Therefore it is found that E_a depends on the quality of the interfacial layer and independent of the high-κ thickness. Activation energies in this range were also obtained by Neugroschel *et al* during NBTI [109]. Stress induced leakage current (SILC), measured during TDDB at gate injection mode also demonstrates similar temperature dependence. Figure 5.4(b) shows the activation energies extracted from SILC evolution at different temperatures for the same type of devices as in figure 5.4(a).

SILC measurements were performed during the temperature dependent breakdown study. The chemical oxide IL devices show lower E_a compared to ISSG IL. It is important to note that the activation energies are comparable for both ΔV_{th} and SILC i.e. for NBTI and TDDB. Since the SILC measurements were performed independently during TDDB study the major contribution of the measured SILC should be from the generation of conducting defects during TDDB stress. During gate injection TDDB, a power law dependence of the SILC was also observed with stress time.



(a) (b)

Figure 5.4 Activation energies of threshold voltage change during NBTI for three different gate stacks with 3 and 5 nm high-κ thicknesses and 1.1 nm IL (a). Two of the devices had Chemical Oxide as IL and the third had ISSG oxide as IL. The gate stack with ISSG SiO_2 IL shows the impact of the quality of the IL (higher E_a). (b) Activation energies of SILC during TDDB of same gate stack. Similar observation can be made from E_a of SILC.

The positive charge build up due to NBTI would saturate SILC which was not observed. So, this gate current increase is due to newly generated defects in the oxide. As defects, created during stress, contribute to both ΔV_{th} and SILC, it is further confirmed

that NBTI degradation and TDDB degradation processes are originating due to similar types of defects.

5.5 NBTI and TDDB Dependence on IL Thickness

Both time-to-breakdown ($t_{63\%}$) and threshold voltage shift due to NBTI were measured for three different gate stacks with same high-κ layer (~3 nm) but with different SiO_2 IL (ISSG) thicknesses, as shown in Figure 5.5. The IL thicknesses considered here were 0.7, 1.1 and 2.1 nm and the gate voltage was -1.6 volt. The gate stack with thicker IL (2.1 nm) showed low ΔV_{th} indicating a reduced NBTI degradation. As the field across thinner IL was higher, the net defect concentration tends to be higher after NBT stress. Consequently a higher ΔV_{th} was observed for thinner IL. Additionally, if we assume that in all cases the contribution from interfacial defects is identical then the defect density in the interfacial layer increases because of NBTI as the thickness goes down. So, in terms of NBTI behavior, gate stacks with higher EOT showed lower degradation. Similar trends were also observed for breakdown characteristics. It can be observed that as EOT increases (2.1 nm IL), failure time increases due to the decrease in the gate leakage current. For these gate stacks as the interfacial layer thickness increases, the IL breakdown field, E_{BD}^{IL} increases but the high-κ breakdown field, E_{BD}^{HK} is reduced for same high-κ thickness [180]. Also, it was found that the breakdown field, E_{bd}^{IL} depends on the quality of the interfacial layer [180]. IL controls the breakdown and the thicker the IL, longer is the time-to-breakdown. So, better quality interfacial layer increases time to breakdown. The similar effect of IL scaling on TDDB failure distribution was also observed in literature [188, 189].

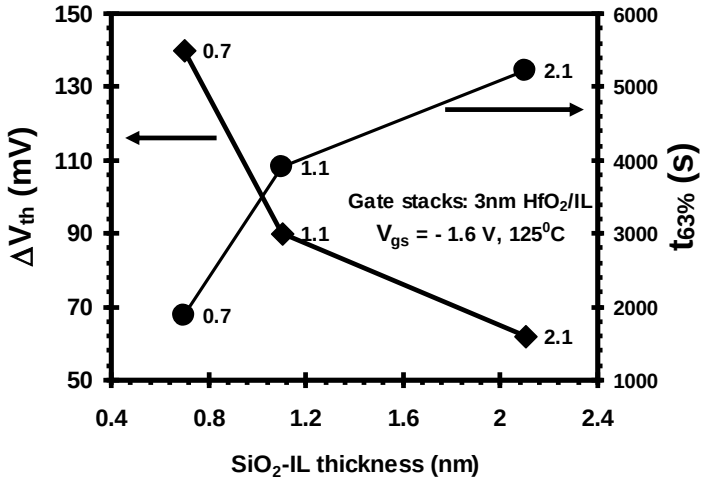


Figure 5.5 Threshold voltage change and time to breakdown for a 3nm HfO_2 gate stack. Three different SiO_2 IL (ISSG) were used (0.7, 1.1 and 2.1 nm). Gate stacks with lower EOT showed similar maximum degradation in both NBTI and TDDB domain.

It is known that the quality of the interfacial layer degrades slightly with decrease in thickness because of oxygen exchange between high-κ layer and IL [190]. As discussed earlier, during stress the thinner IL degrades rapidly as compared to thicker IL [188]. 2.1 nm IL, therefore, showed longer T_{BD} due to its improved quality over other IL oxides. This suggests that the origins of the traps contributing to NBTI and TDDB are mostly dominated by the interfacial layer.

5.6 NBTI and TDDB Dependence on High-κ Layer Thickness

To evaluate the contribution of bulk traps in the high-κ layer, gate stacks with different high-κ thickness were subjected to NBTI stress. HfO_2 thicknesses of 2.6nm, 3nm and 5nm were used with the same 1.1 nm ISSG SiO_2 interfacial layer. Figure 5.6 shows HfO_2

thickness dependence of the threshold voltage shift measured after 1000 seconds of stress at two different voltages.

As ΔV_{th} is dependent on the trapped charges in the IL and high-κ layer in addition to interface, the initial jump of from 2.6nm to 3 nm after 1000 seconds of stress (Figure 5.6) suggests that the charge trapping was also taking place in the high-κ layer.

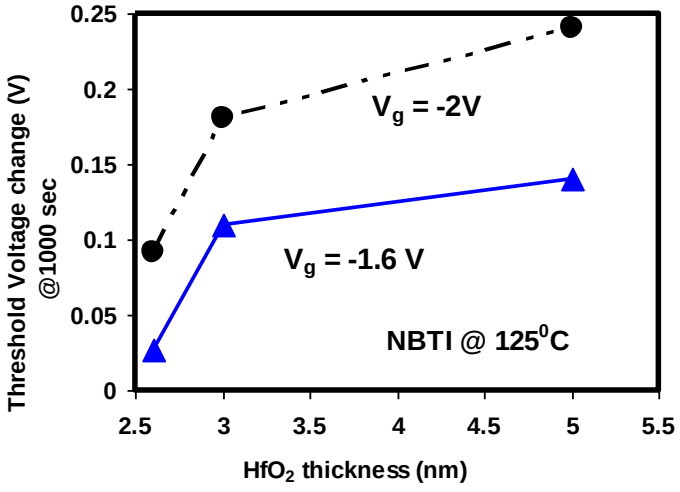


Figure 5.6 HfO_2 thickness dependence of the threshold voltage shift measured after 1000 seconds of stress. For this NBTI measurement, V_g was -2 and -1.6 V. The contribution of the bulk oxide layer is observed through charge trapping in that layer.

As the thickness of the high-κ layer increases, the rate of charge trapping reduces even though ΔV_{th} showed a moderate increase for 5nm HfO_2. It is well known that the intrinsic defect density in HfO_2 decreases when its thickness increases. As discussed earlier, it is mostly attributed to exchange of oxygen vacancies between the high-κ layer and IL [190]. If we assume uniform defect generation at the interface *i.e.* 1.1nm IL, the charge trapping in high-κ layer mostly followed the intrinsic defect distribution trends. From the above observations it can be inferred that the defects created by NBTI and

TDDB seem to be confined to the interface and in the interfacial layer. Under the gate injection mode, it is known that either hydrogen species or hole injection from the anode is responsible for interface and bulk defect creation during constant voltage stress. Defect creation and charge trapping in the interfacial layer mostly controls the breakdown process and threshold voltage shift during NBTI. For high temperatures stress the nature of defects seems to be related.

5.7 Chapter Summary

NBTI and TDDB reliabilities in HfO_2/SiO_2 gate stacks have been discussed. A quantitative agreement was observed for the activation energies for threshold voltage change and SILC. The quality and thickness variation of the IL causes similar degradation both on NBTI and TDDB indicating that these two reliability issues are due to identical defect types present in the IL. Based on the observed results, it can be further concluded that the interfacial layer plays the key role in NBTI and TDDB degradation for high-κ/metal gate pFETS.

CHAPTER 6

PROGRESSIVE BREAKDOWN AND NON-WEIBULL FAILURE DISTRIBUTION OF HIGH-K DIELECTRIC BY RAMP VOLTAGE STRESS

6.1 Introduction

In Chapter 4, breakdown behavior of high-κ gate stacks was discussed in terms of soft, progressive and hard breakdown. Soft breakdown or 1st breakdown was used to define time-to-breakdown (T_{BD}). Constant voltage stress was applied to investigate statistical distribution of T_{BD} for small sample size. Because the statistical distribution of T_{BD} followed Weibull distribution, large sample size was not required. But it is known that static random access memory (SRAM) failure can be predicted by the realistic TDDB model based on gate leakage current (I_{FAIL}) rather than the conventional first breakdown (BD) criterion [119]. Therefore, the relevant failure distributions (F_{FAIL}) at I_{FAIL} are non-Weibull including the progressive breakdown (PBD) phase for thin SiO_2 oxides and high-κ/metal gate (HKMG) dielectrics. However, conventional constant voltage stress (CVS) measurements are time consuming for non-Weibull statistics. On the other hand, although voltage ramp stress (VRS) technique has been known for a long time, it has only been used in the context of Weibull distributions associated with first BD definition [118, 191-192]. In this chapter, the PBD phase and non-Weibull final failure distributions of multi layer high-κ and SiO_2 gate dielectric were investigated by VRS technique. A new hybrid two-stage CVS/VRS methodology was developed to exclusively evaluate the PBD phase. Then, the VRS technique was applied to investigate the non-Weibull failure distribution at a specified current (I_{FAIL}) with large sample-size (~ 1000) experiments. An excellent agreement was achieved in

both cases in comparison with the conventional CVS technique, thus demonstrates that VRS is an effective technique to replace the CVS technique for investigation of post-BD and non-Weibull statistics in both SiO_2 and high-κ dielectrics.

6.2 Experimental Setup

High-κ/metal gate (HK/MG) devices used here with Hafnium based dielectrics and interfacial layer of SiO_2 (chemical oxide) were fabricated using conventional CMOS process flow on SOI substrate. The high-κ gate stacks had an interfacial layer of ~1.0nm thickness and high-κ layer thickness of <2.5nm. For ultra-thin SiO_2, rapid thermal oxidation (RTO) followed by remote plasma nitridation was applied. Thickness of this ultra-thin oxide was 1.1nm. For electrical measurements, both VRS and CVS were performed at 140^0C. Unit pFET devices were connected in parallel to construct large area test structures.

Here a hybrid 2 step stresses were developed to investigate specifically PBD phase. The concept of 2 stage breakdown naming partial and complete breakdown during Fowler-Nordheim (F-N) stress was reported earlier [193]. The partial breakdown was termed as B-SILC and Ohmic conduction was called as complete breakdown. Based on this concept, Linder et al., has developed 2-stage stress both by CVS to study oxide degradation rate [194]. For the new hybrid two-stage stress introduced in this chapter, a higher constant voltage was applied at the first stage with a low current compliance to arrest breakdown. This low current compliance would prevent the oxide to go into progressive breakdown. Then at second stage, ramp voltage was applied with a specified fail current on those samples. For small area nFETs with thin oxide, a current compliance

of 2μA was applied to arrest BD as shown in Figure 6.1 (a). High gate voltage of 2.8V was used in 1st stage to reduce 1st BD time. Once BD was detected, these devices were subjected to VRS with a higher fail current of 100 μA (Figure 6.1b).

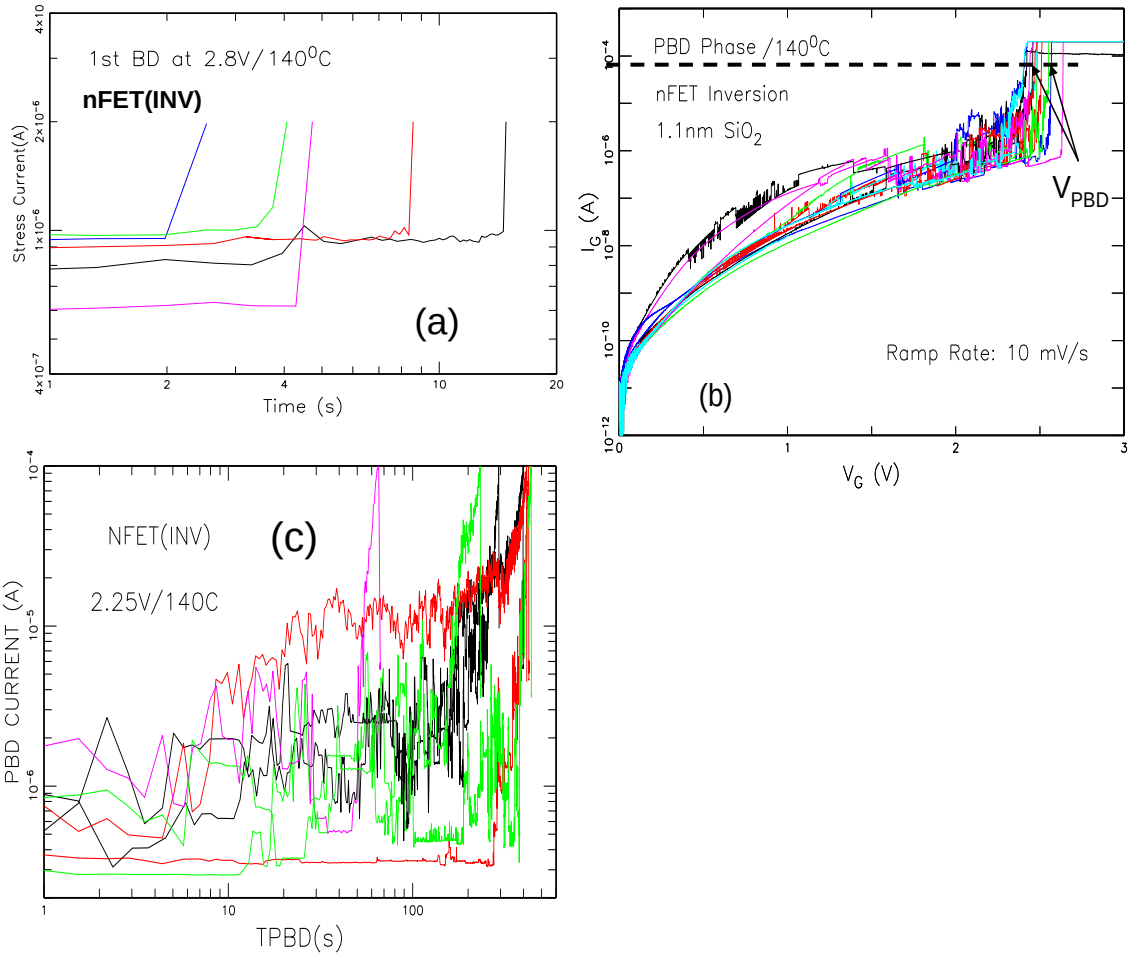


Figure 6.1 Hybrid two-stage VRS technique. (a) at first stage, BD was detected by CVS with a low current compliance (here 2 μA). For 2nd stage those samples were either subjected to (b) VRS to extract V_{PBD} or (c) CVS for direct T_{PBD} measurements with a specified fail current (200 μA).

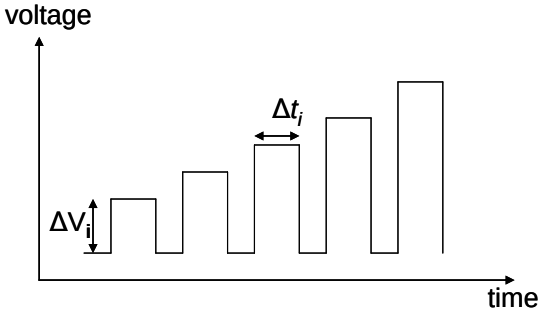
It was shown earlier that post soft breakdown gate current exhibits exponential dependence on the gate voltage [140]. This model which is based on quantum point

contact describes that the experimental post-SBD current can be fitted by exponential law I=A*exp(BV). Here V_{PBD} was extracted based on this exponential relation of progressive breakdown current and voltage. For comparison purpose, CVS was also carried out separately to directly measure T_{PBD} on the samples which were intrinsically broken at 1st stage shown in Figure 6.1c.

6.3 Conversion from Voltage Domain to Time Domain

Three different acceleration models have been considered first to demonstrate that this methodology is independent of the acceleration models for a narrow projection voltage window closer to V_{PBD} at 63% failure percentile.

The equivalence or conversion concept of V_{BD} to T_{BD} was first introduced by Berman [115].



$$t_{BD}(V_{REF}) = \sum_{i}^{N(V_{BD})} \Delta t_i A_F(V_i, V_{REF}) = \int_0^{V_{BD}/R} A_F(V_i, V_{REF})\,dt \tag{6.1}$$

Here A_F (V_i, V_{REF}) is the acceleration factor which depends on the acceleration model. $V_i = Rt$; R is the ramp rate during VRS.

For Power-law model: $T_{BD} = \kappa V_G^{-n}$ [195]. V or V_{REF} is the desired reference-voltage for its corresponding T_{BD} distribution after conversion and n is the power law exponent. Acceleration factor for this model is $A_F(V_i, V_{REF}) = \left(V_i / V_{REF}\right)^n$. Substituting this into equation (1) results in

$$t_{BD} = \frac{V_{REF}}{R(n+1)}\left(\frac{V_{BD}}{V_{REF}}\right)^{n+1} \tag{6.2}$$

The conversion between V_{BD} and T_{BD} for other two models can be derived based on the corresponding acceleration models [30, 192, 196-197].

For Exponential law of field or voltage:

$$T_{BD} = \tau_0 \exp(-\gamma V_G) = \tau_1 \exp(-\gamma_E E_{OX}) \tag{6.3}$$

$$V_{BD}(V_{REF}) = \frac{1}{\gamma R}\exp(-\gamma V_{REF})[\exp(\gamma V_{BD}) - 1] \tag{6.4}$$

For Exponential law of reciprocal field or voltage dependence:

$$T_{BD} = \tau_E \exp(G / E_{OX}) \tag{6.5}$$

Or, it's alternative form, $T_{BD} = \tau_V \exp(C / V_G)$.

$$T_{BD}(V_{REF}) = \exp\left(\frac{C}{V_{REF}}\right)\int_0^{V_{BD}/R}\exp\left(-\frac{C}{Rt}\right)dt$$
$$\cong \exp\left(\frac{C}{V_{REF}}-\frac{C}{V_{BD}}\right)\left(\frac{V_{BD}^2}{RC}\right) \quad (6.6)$$

γ, n and C are the voltage acceleration factors for the respective models and they can be determined from T_{BD} measurements at different voltages.

Now, the equations above are described in terms of 1st breakdown (BD). If equation 6.2 is carefully looked at, converted T_{BD} is basically integration of time steps during voltage ramping [$t_{BD}(V_{REF}) = \sum_i^{N(V_{BD})} \Delta t_i A_F(V_i, V_{REF})$]. Hence, this conversion is valid for V_{FAIL} to T_{FAIL} conversion. Also, it is known that $T_{FAIL} = T_{BD} + T_{PBD}$ as shown in Figure 6.2. If both T_{BD} and T_{FAIL} can be converted based on the above equations, same concept would allow T_{PBD} conversion if appropriate acceleration parameters are taken into account.

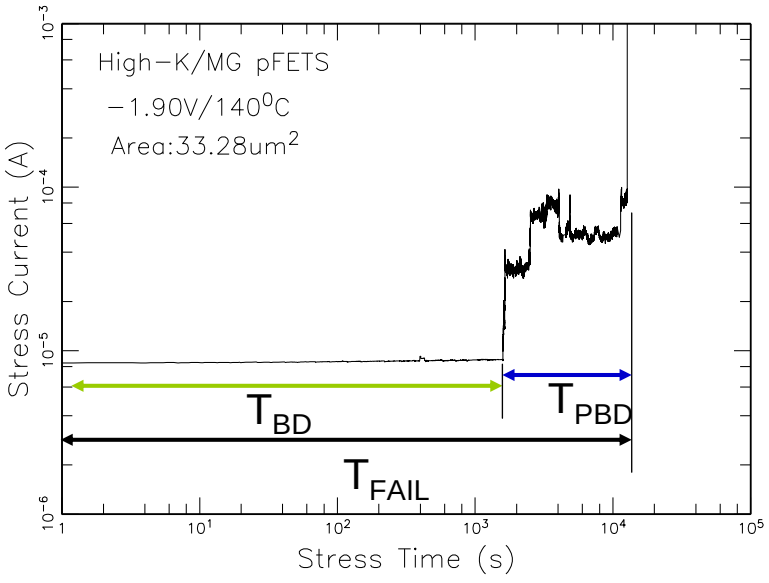


Figure 6.2 Typical stress current evolutions with time for high-κ/metal gate dielectrics. T_{FAIL} is summation of time to 1st breakdown (T_{BD}) and progressive breakdown time (T_{PBD}).

As it was discussed in the previous section, V_{PBD} was extracted based on the exponential relation of progressive breakdown current and voltage shown in Figure 6.1 (b). Then the extracted V_{PBD} distribution has been converted to T_{PBD} distribution based on the equations described above. Figure 6.3 shows this conversion of a steeper V_{PBD} distribution converted to a much shallower T_{PBD} distribution. This conversion requires a relevant voltage acceleration model. Three existing models for BD have been applied. Here solid line is for power-law model: $T_{PBD} \propto V^{-n}$, dotted line for exponential model: $T_{PBD} \sim \exp(-\gamma V)$ and the dashed line for 1/V model: $T_{PBD} \sim \exp(C/V)$ have been used for the conversion. The corresponding acceleration factors n, γ and C are 37.6, 16.795 1/V and 84.3V were determined from CVS T_{PBD} data. The conversion between V_{BD} and T_{BD} measurements for all three models has been shown in the Appendix with references. A

good agreement is observed for direct T_{PBD} from CVS and converted T_{PBD} from VRS for all three models. This is because the projected voltage, 2.1 V is close to $V_{PBD,63\%}$ which is 2.51V (not shown here). Differences would be visible between different models if the projection voltage is either too low or too high than $V_{PBD,63\%}$.

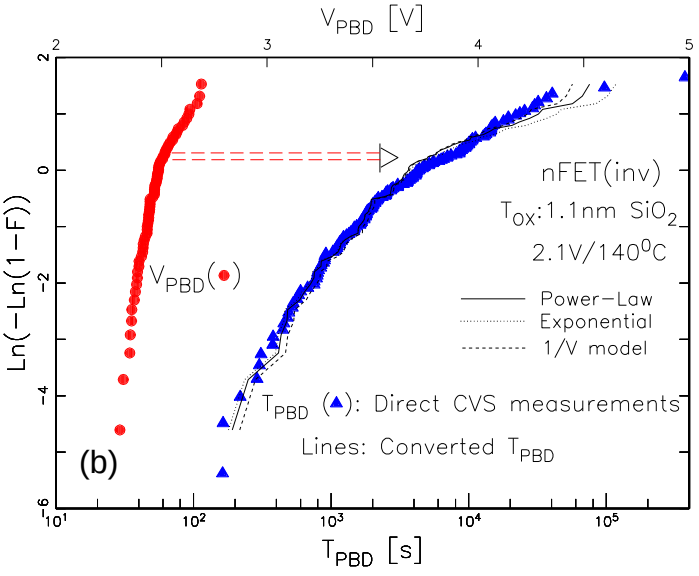


Figure 6.3 Conversion of V_{PBD} to T_{PBD} distribution. Symbols represent TPBD data from CVS stress. Very steep V_{PBD} distribution is translated to shallow T_{PBD} distribution due to the exponential dependence of T_{PBD} on V_{PBD}. Three popular models as power-law (solid line), exponential (dotted line) and 1/V model (dashed line) have been used as acceleration model for conversion. The T_{PBD} converted from V_{PBD} for a reference voltage of 2.1V agrees quite reasonably irrespective of the choice of the model. The variations among different models would be visible for a larger time window.

It has been clarified before choosing one of the three models that either one is applicable for a limited projection window. Also, it has been reported earlier that voltage scaling of progressive breakdown time of ultra-thin gate oxide can be modeled by a power-law model as $T_{PBD} \approx T_{PBD0} V_{G,PBD}^{-m}$ [198]. Hence power-law model has been used as the acceleration model throughout this chapter.

It was found that voltage acceleration (n) can be derived from either $V_{PBD,63\%}$ of different ramp rates of VRS or $T_{PBD,63\%}$ of different stress voltages of CVS. For time domain, $t_{PBD,63\%} \sim V_G^{-n}$ and for voltage domain, $R \propto V_{PBD,63\%}^{n+1}$ have been used. From VRS, n was found to be 37.48 and from CVS it was 37.79. Hence both methods yield values which are within statistical uncertainty as shown in Figure 6.4(a) and (b). Although for VRS, difficulties lie in selecting the range of practical ramp rates. As it is known that ramp rate is $\Delta V/\Delta t$ volt/sec. If ΔV is made too large to make ramp rate very fast, then the granularity effect would diverge the converted distribution from actual distribution. The other way to get faster ramp rate is low time step, Δt. But the resolution range of the measuring instrument sets the limit here. To expand the ramp rate in the slower region (assuming $\Delta t = 1s$) would be time consuming attenuating the benefit of fast VRS technique. For figure 6.4(b), ΔV was always fixed at 1mV and Δt was varied from 1ms to 100ms.

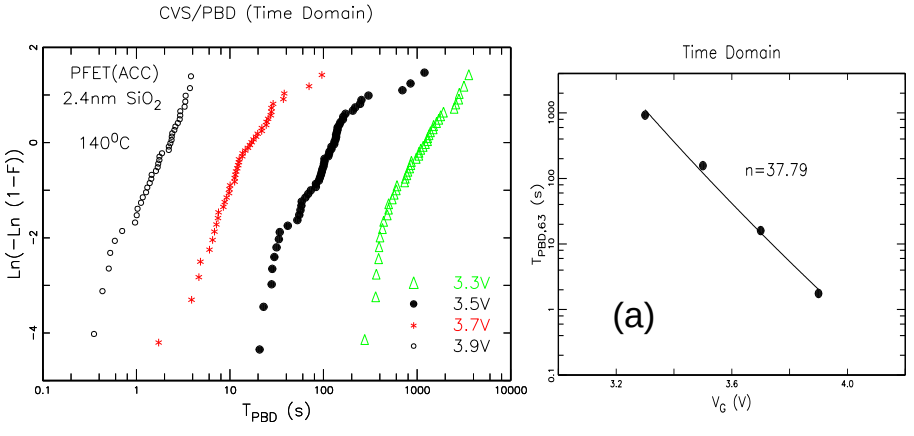


Figure 6.4 (a) Voltage acceleration derived from CVS/PBD (b) from VRS/PBD show power-law exponents within statistical uncertainty. For time domain, $t_{PBD,63\%} \sim V_G^{-n}$ and for voltage domain, $R \propto V_{PBD,63\%}^{n+1}$ have been used.

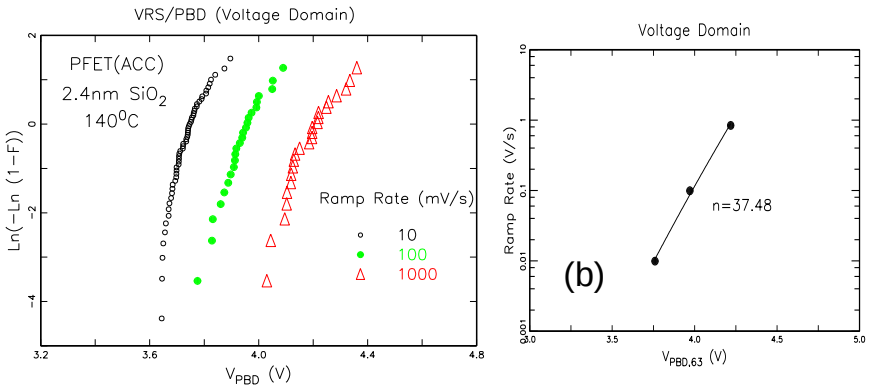


Figure 6.4 (a) Voltage acceleration derived from CVS/PBD (b) from VRS/PBD show power-law exponents within statistical uncertainty. For time domain, $t_{PBD,63\%} \sim V_G^{-n}$ and for voltage domain, $R \propto V_{PBD,63\%}^{n+1}$ have been used (continued).

6.4 Progressive Breakdown Time by VRS

To characterize time-to-progressive breakdown (T_{PBD}) with this hybrid method, detection of 1st BD at the first stage is very critical. This issue can be discussed in the context of ultra-thin dielectric in a pFET in inversion. When pFET devices are stressed by CVS, background tunneling current and stress-induced leakage current (SILC) due to the generation of defects make gate current very noisy and can easily mask the formation of 1_{st} BD (Figure 6.4). As the gate currents of ultra-thin pFETs were plotted in Log-Lin scale, some devices show spike in gate current within very short period of stress (<10s). So, it becomes challenging to fix a low current compliance which could arrest BD at first stage invariably on a large sample size. If the stress current of pFET devices (Figure 6.5) is compared to nFETs (Figure 6.1c) of identical oxide thickness and device dimensions, the difference in gate current noise is clearly visible.

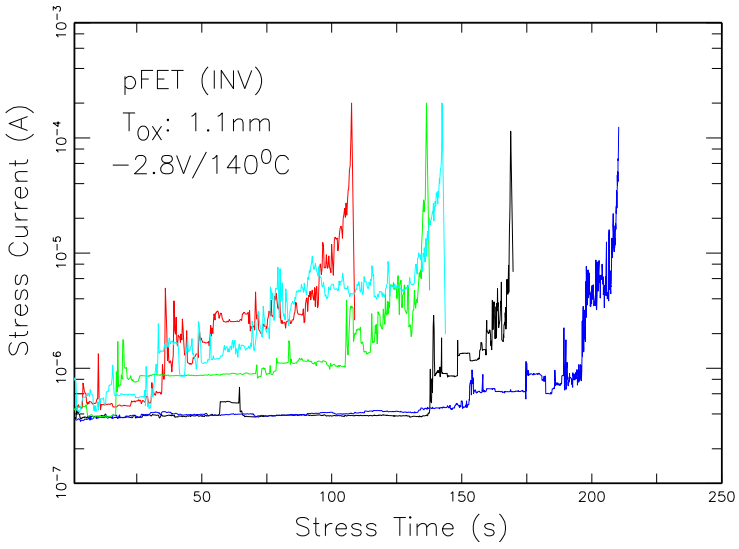


Figure 6.5 1st BD detection difficulties in ultra-thin oxide pFETs. The noise in early stress time seen in this figure would impede to fix a low current compliance level for 1st stage of the hybrid stress method.

It is known that there is a fundamental difference in the progressive breakdown phase for ultra thin n- and pFETs. For nFETs, progressive breakdown is a local degradation phenomenon where one single spot grows until catastrophic breakdown occurs. In case of pFETs, multiple BD spots compete during progressive breakdown phase [199]. VRS method would estimate T_{PBD} regardless of how PBD is evolving in n- and pFETs. But for this method to characterize PBD time, arresting breakdown at 1st stage is a prerequisite. If 1st stage stress was stopped on some samples even before a single BD was formed, then T_{PBD} at the second stage for those samples would be summation of (T_{PBD} + part of T_{BD}). Because of this limitation, T_{PBD} work was studied on ultra thin nFET devices only. It is worth to mention that this is true for PBD time only, not to confuse with time-to-fail (T_{FAIL}) which will be discussed later.

Historically, it is known that thick oxide (>3nm) shows a sudden hard breakdown at TDDB stress voltage. Hence, it is assumed that PBD phase does not exist for thick oxide. This is merely due to the fact that thick oxide has a very short progressive breakdown time compared to 1st breakdown time and detection of that T_{PBD} depends on the time resolution of the test set-up at the stress bias. In this scenario, hybrid VRS technique can separate the two BD phase if the stress bias and current compliance at the first stage are chosen carefully. A very short PBD phase was observed specially at high bias for this 6.2 nm SiO_2 dielectric. Figure 6.6 shows statistical distribution of progressive breakdown times obtained by the hybrid stress method.

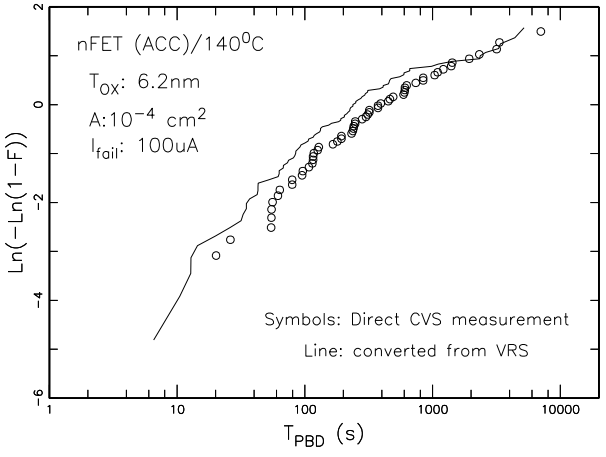
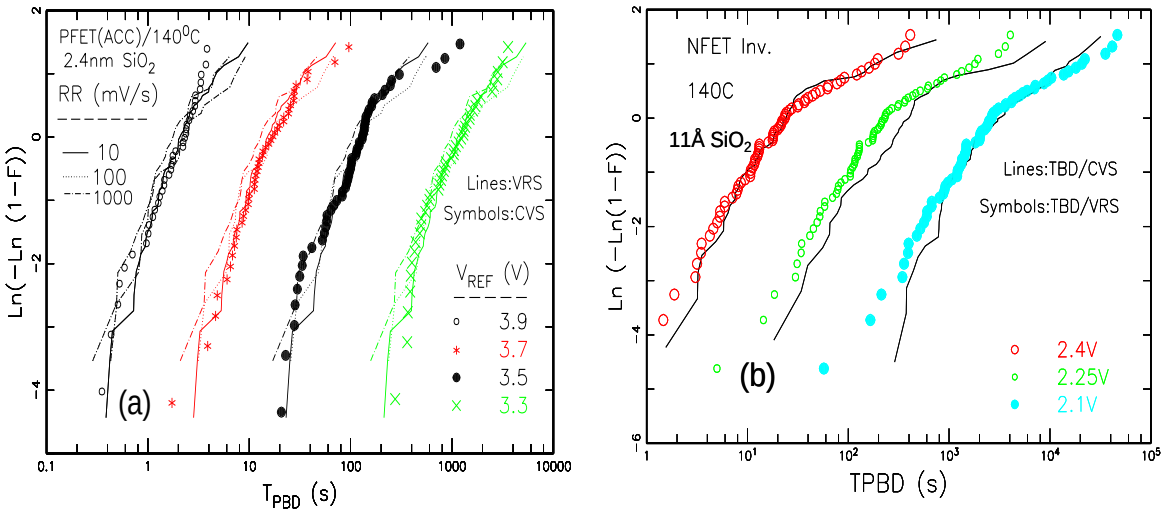


Figure 6.6 Comparison of residual times (T_{PBD}) for thick (6.2nm) oxide. These devices were intrinsically broken at 7V at 1st stage. For PBD phase or 2nd stage, V_{ref} was also 7V.

This method was then applied on thick oxide (2.4nm) pFETs in accumulation. Second stage ramp was performed for three different ramp rates ranging from 1V/s to 10mV/s. V_{PBD} from VRS was converted to T_{PBD} (lines) and compared to the directly measured T_{PBD} by CVS and an excellent quantitative agreement can be observed for all

three different ramp rates Figure 6.7 (a). The results also include different reference voltages from 3.3 to 3.9 volts. As we can see, T_{PBD} does not depend on the ramp rates.



(a) (b)

Figure 6.7 Comparison of residual times (T_{PBD}) for (a) thick oxide, 2.4nm, (b) thin oxide, 1.1nm SiO_2. An excellent agreement between CVS/T_{PBD} and VRS/T_{PBD} can be observed for different reference voltages and 100 μA fail current.

As it was discussed earlier, for ultra-thin (1.1nm), only nFETs have been studied. Comparable T_{PBD} were also obtained for ultra-thin oxide based on 100 μA fail current during PBD phase and a non-Weibull distribution is observed (Figure 6.7 b). It is worth to mention that similar failure current dependence of Time-to-PBD (T_{PBD}) is observed for both VRS and CVS for this thin (1.1nm) oxide (Figure 6.8) which indicates that these two mechanisms are essentially equivalent. Also, as I_{FAIL} was increased from 8μA to 100μA, T_{PBD} significantly increases at low percentile, a clear signature of post-BD characteristics since 1st BD does not depend on failure currents.

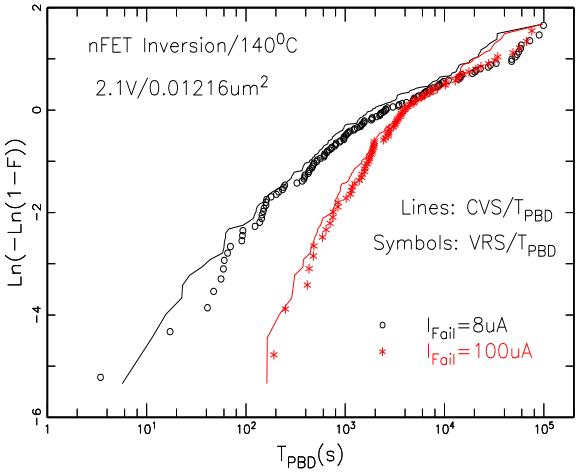


Figure 6.8 Similar failure current dependence of Time-to-PBD (TPBD) is observed for both VRS and CVS for thin (1.1nm) SiO_2.

For High-κ/IL gate stacks, existence of progressive breakdown is still a controversial topic. There are reports of the evidence of PBD [141, 200]. The fast VRS method was able to characterize T_{PBD} (and residual time). Figure 6.9 shows the results of the hybrid two-stage VRS technique for the high-κ/IL gate stacks in comparison with CVS technique. The VRS results also yield very shallow distribution of residual time (or PBD time) which is the unique characteristics ($\beta<<1$) of post-BD found for high-κ/IL gate stacks using CVS method [119].

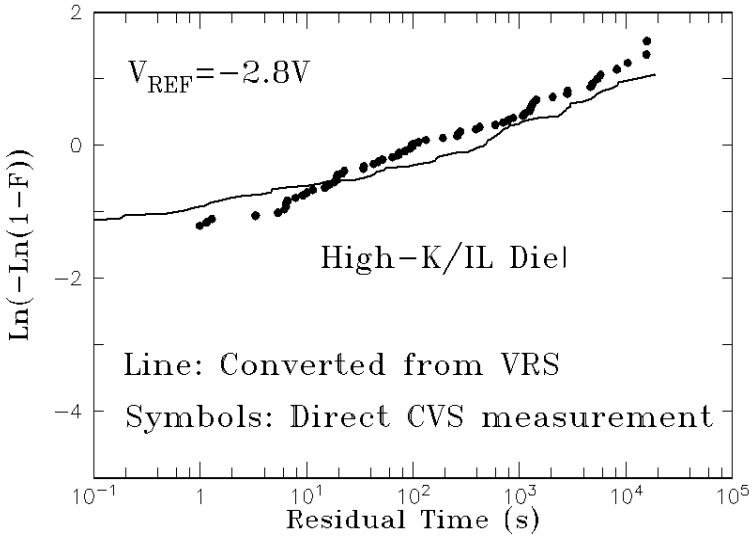


Figure 6.9 Comparison of residual times (TRES) of high-κ/IL dielectric pFET in inversion at 125^0C. Constant voltage of -3.1V was used in the first step.

6.5 Area Independence of Progressive Breakdown Voltage

It has been reported earlier in the literature that ultra-thin nFETs show single spot breakdown and that spot grows during progressive breakdown phase [201]. Therefore, T_{PBD} measured by conventional CVS method is independent of device area as it is a localized degradation phenomenon. For multiple breakdown events (found in ultra-thin pFETs) rather than single spot growth during PBD phase, the likelihood of breakdown events would be higher for large area devices. Hence T_{PBD} would show area dependence.

In this work, progressive breakdown voltage (V_{PBD}) was measured during second stage ramp for three different areas from 0.01216 to 0.608 μm^2 (2x to 100x). These larger area structures are made by connecting parallel array of unit cells of 0.00608 μm^2 (equivalent to 1x). It was found that V_{PBD} for these nFETs is also area independent shown in Figure 6.10. This is similar to the results mentioned above about area independent T_{PBD} by CVS. Hence VRS mimics the mechanism of the growth of a single BD spot

during progressive breakdown phase of ultra-thin nFETs by producing area independent V_{PBD}. This again validates that hybrid VRS method can be used to study PBD phase of dielectric breakdown.

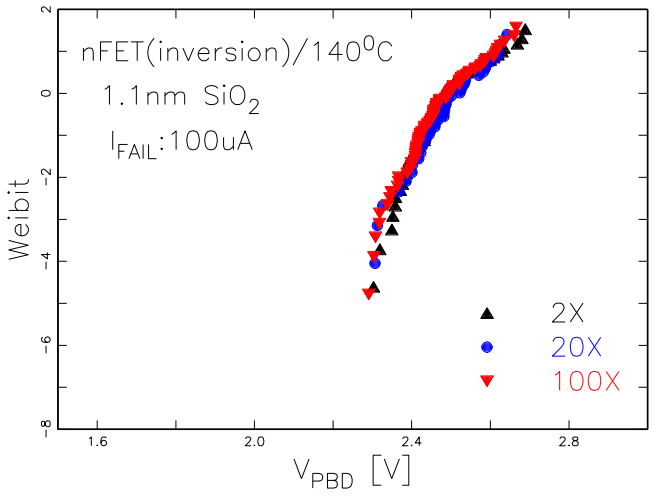


Figure 6.10 V_{PBD} distributions of ultra-thin oxides extracted during 2nd stage of hybrid stress. Three different area nFETs (2x to 100x, where x is 0.00608 μm^2) were investigated. Area independence of V_{PBD} indicates single spot BD during PBD phase.

The results observed here clearly demonstrate that the BD defects created by CVS and VRS techniques in post-BD phase share a common origin similar to the equivalence of VRS and CVS in the first BD phase [118, 191-192]. It has been suggested that extrinsic samples exhibit the same post-BD characteristics as intrinsic BD samples [202]. Thus, extrinsic defects created in manufacturing process can be regarded as partially broken samples analogous to stress-induced defects of intrinsic samples in the post-BD phase. The validity of VRS technique demonstrated in the post-BD phase points to a much efficient methodology to evaluate the voltage acceleration and defect density of extrinsic defects, thus providing valuable information for the improvement of microelectronics manufacturing process in production in a timely manner.

6.6 Time-to-Fail by VRS

6.6.1 Time-to-Fail of Thick and Thin SiO_2

Having established the validity of VRS technique in PBD phase, we then investigate the time-to-final fail (T_{FAIL}) by one stage voltage ramp based on failure current (V_{FAIL}). Note that T_{FAIL} is defined as $T_{BD}+T_{PBD}$. Figure 6.11 shows time-to-fail (T_{FAIL}) converted from V_{FAIL} by VRS and directly measured by CVS for thick SiO_2 (2.4nm) pFET in accumulation which shows excellent agreement. Here, lines are T_{FAIL} from VRS and symbols represent T_{FAIL} from CVS .The advantage of this VRS method is that one set of V_{FAIL} data can project T_{FAIL} distribution for different stress voltages. This can significantly reduce time and resources.

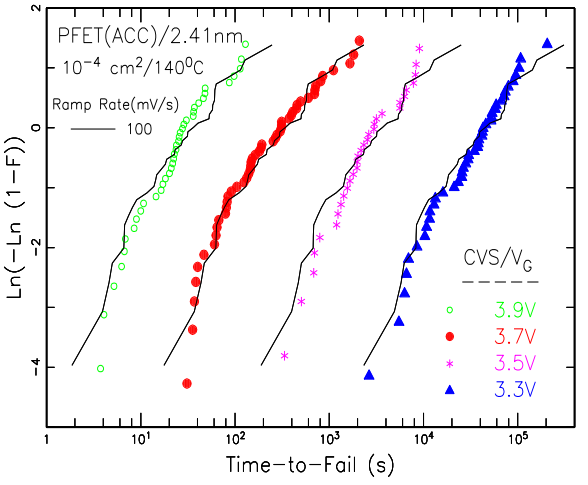


Figure 6.11 Time-to-fail (T_{FAIL}) extracted from CVS and converted from V_{FAIL} by VRS for thick SiO_2 (2.4nm) pFET in accumulation show excellent agreement. Lines are T_{FAIL} from VRS and symbols represent T_{FAIL} from CVS.

A large sample size study of around ~1000 devices was carried out on thin SiO_2 (11Å) for both p- and nFETs in inversion mode. Figure 6.12 (a) shows that VRS method can effectively reproduce non-Weibull T_{FAIL} distribution extracted by CVS. For nFETs,

characteristic life, $T_{FAIL,63\%}$ values agree well even though a disagreement is observed at low percentile which is due to statistical uncertainty in experiment.

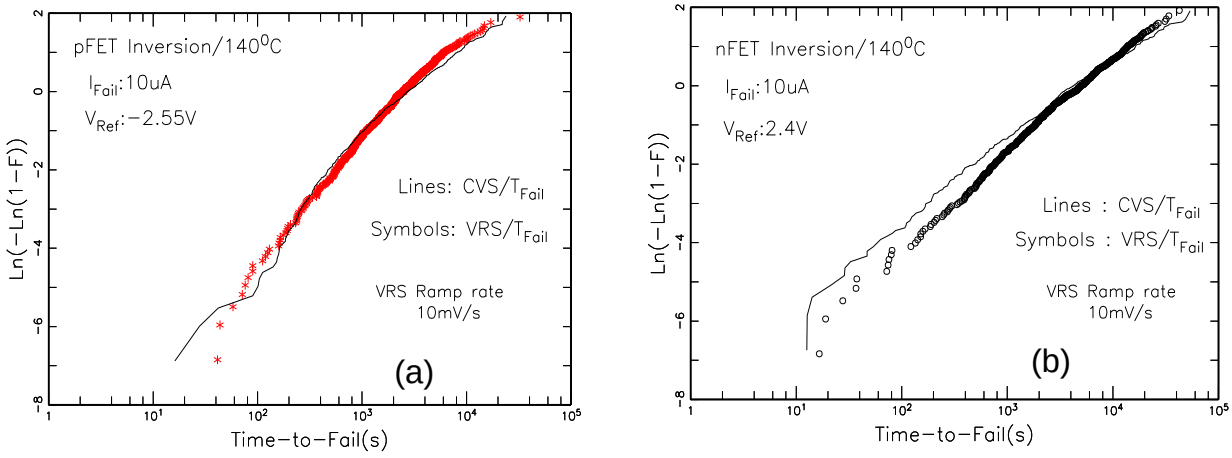


Figure 6.12 (a) Time-to-fail (T_{FAIL}) extracted from CVS and converted from V_{FAIL} by VRS for ultra-thin SiO_2 (1.1nm) pFET show excellent agreement on large sample size (~1000 devices each) and (b) For nFET, high percentile data agrees quite well.

Figure 6.13 investigates failure current dependence of time-to-fail for both methodologies. Both VRS (symbols) and CVS (lines) show similar failure current dependence. For low failure current such as 1μA, failure distributions behave more like Weibull distribution because of minimal contribution from progressive breakdown time or for short T_{PBD}, $T_{FAIL} \approx T_{BD}$. As I_{FAIL} was increased to 100μA for example, the low-percentile bending is prominent making this distribution a non-Weibull distribution. This is because as the failure current was increased, for significant T_{PBD}, $T_{FAIL} > T_{BD}$. From this the similarity between breakdown physics of these two breakdown mechanisms is suggested.

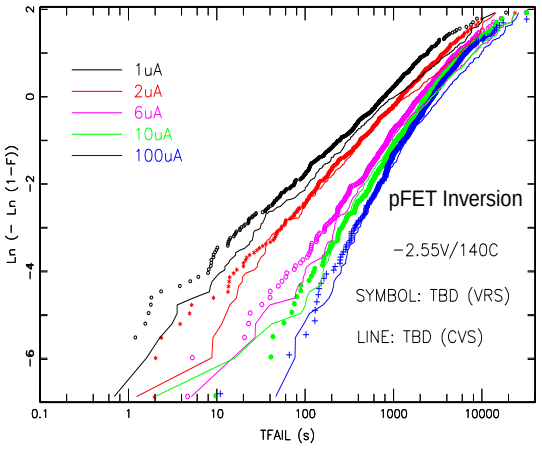


Figure 6.13 The final failure distributions as a function of fail currents for ultra-thin SiO_2 pFETs. For both CVS (lines) and VRS (symbols), strong failure current dependence of final fail time is observed.

6.6.2 Time-to-Fail of High-κ/SiO_2 Gate Stack

Poisson area scaling was performed on V_{FAIL} distribution of three different area high-κ pFET devices in inversion based on this equation, $Ln(-Ln(1-F_2)) = Ln(-Ln(1-F_1))+ ln(A_2/A_1)$ [13]. Here F_1 and F_2 are the failure distribution corresponding to areas A_1 and A_2. As discussed in the reference [13], this formula is applicable for weakest-link property and a uniform failure site distribution in the oxide area. So, a non-Weibull distribution can also be scaled using this formula. Both T_{FAIL} and V_{FAIL} distributions follow Poisson area scaling shown in Figure 6.14 (a), (b). Here a strong bending (or deviation from Weibull distribution which is evident in high percentile) at low percentile distribution is observed. This low-percentile distribution is of paramount importance when studying TDDB reliability of these new high-κ gate stacks as it represents product areas relevant to the circuit/chip reliability. Without going into the debate of whether this bending is due to the PBD phase in the gate stacks [200] or due to the different breakdown mechanism in High-κ and IL [93], it is worth to mention here that VRS

method can efficiently generate the shallow and steep distributions in high and low percentiles respectively.

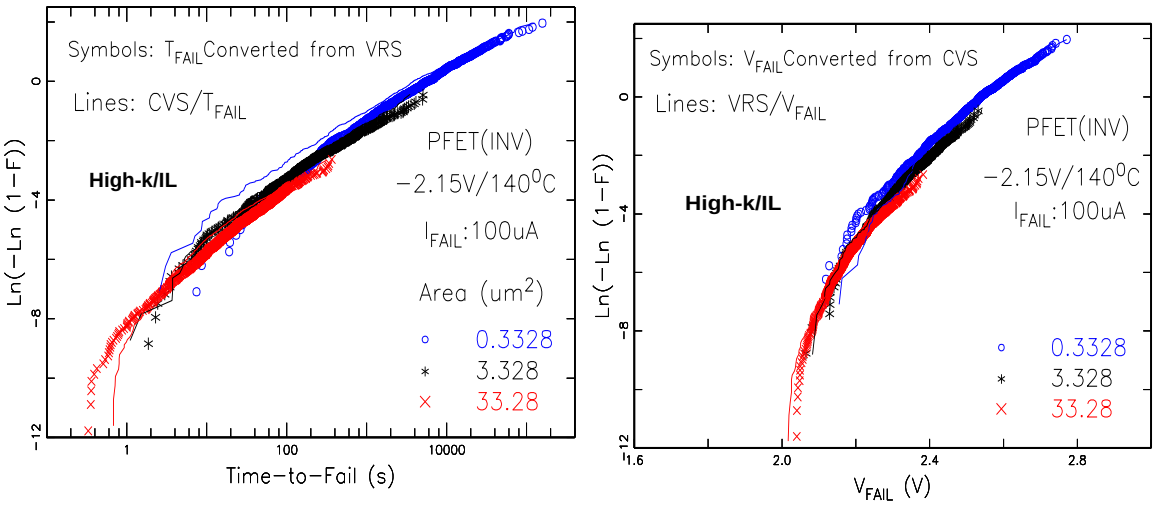


Figure 6.14 (a) T_{FAIL} distributions for 3 different area high-κ/IL pFETs in both time domain. Symbols represent T_{FAIL} converted from V_{FAIL} and lines are direct CVS measurements. (b) Similar comparison between direct and converted V_{FAIL} in voltage domain. Poisson area scaling has been applied in both cases.

It is important to point out the agreement between CVS and VRS is obtained simply using a constant voltage acceleration factor (exponent) to translate the V_{FAIL} data to T_{FAIL} for all the samples. Therefore, we can conclude that voltage acceleration is independent of distribution percentiles although defect generations in high-κ and IL layers can be different.

6.6.3 Temperature Acceleration of High-κ Gate Stack by VRS and CVS

$V_{FAIL,63\%}$ and $T_{FAIL,63\%}$ were measured by VRS and CVS at different temperatures from 85^{0}C to 140^{0}C on pFETs of 3.328μm^2 area (Figure 6.15). For CVS, reference stress voltage was fixed at -2.15V. Activation energy was extracted independently from $V_{FAIL,63\%}$ and $T_{FAIL,63\%}$. Power-law exponent (n) of 46 was used for conversion of

$V_{FAIL,63\%}$,. This acceleration factor was derived from CVS data at 140^0C. Both methods yield E_a~1.15eV. This not only confirms the equivalence of these two methodologies, it also assures that key reliability parameters can be extracted by faster VRS method with sufficient accuracy.

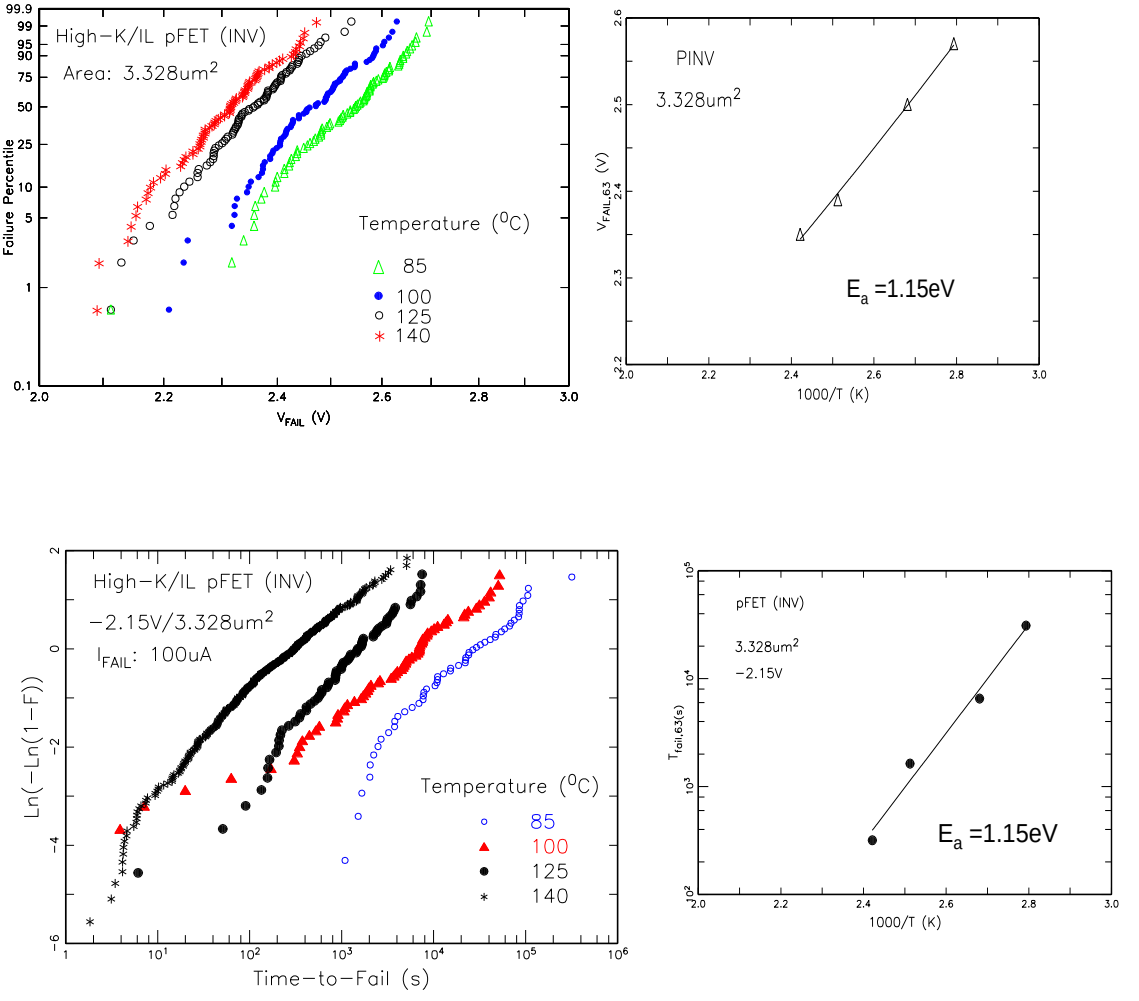


Figure 6.15 Thermal activation energy, E_a of V_{FAIL} (top) and T_{FAIL} (bottom) by VRS and CVS measurements. In both cases, E_a was ~1.15eV.

6.7 Weak Link

Based on results on gate stack, two other control structures (SiO_2-only and HfO_2-only) it was described in chapters 4 and 5 that interfacial layer is weak link in the gate stack breakdown. In this chapter, fast VRS technique also demonstrates the weak link in high-κ/SiO_2 gate stacks. The non-Weibull T_{FAIL} characteristics observed in thin SiO_2 is somewhat identical to that of the gate stack. This suggests that the interfacial SiO_2 in gate stack serves as the weak link in gate stack breakdown irrespective of measurement method. VRS technique however reduces the measurement time significantly.

6.8 Chapter Summary

A new methodology using hybrid two-stage stresses has been developed to study progressive BD phase for high-κ and SiO_2. This methodology was then applied to dielectrics of various thicknesses such as 6.2, 2.41, 1.1-nm SiO_2 and high-κ dielectric stack as well. It was found that reliability parameters of progressive breakdown time (T_{PBD}) distribution can be efficiently captured by VRS technique for high-κ/IL dielectric and other oxides. The voltage ramp stress technique can also reproduce non-Weibull or bending at low percentile distribution of time-to-final fail of high-κ/IL gate stacks similar to CVS on large sample size. Finally the activation energies of T_{FAIL} for both methods were consistently similar. So, this study demonstrates that VRS can be used effectively for quantitative reliability studies of progressive BD phase and final BD of high-κ and other dielectric materials; thus it can replace the time-consuming CVS measurements as an efficient methodology and reduce the resources and manufacturing cost.

CHAPTER 7

SUMMARY AND FUTURE WORK

7.1 Summary

Various reliability issues of high-κ dielectric for high-κ/metal gate stacks have been addressed in this research. Thorough investigation of defects origin and their contribution in time dependent dielectric breakdown (TDDB) are discussed. Both gate and Hf-based dielectric were atomic layer deposited (ALD). For the interfacial layer Silicon dioxide, in-situ steam growth and chemical oxidation have been considered.

A comparative study was conducted of the individual breakdown characteristics of HfO_2 and in-situ steam generated (ISSG)-SiO_2 MOS structures to high-κ/IL (ISSG SiO_2)/metal gate stack. Experimental results indicate that after constant voltage stress (CVS), identical progressive breakdown and stress-induced leakage current (SILC) degradation were observed in high-κ/IL and SiO_2-only MOS devices, but HfO_2-only metal-insulator-metal (MIM) capacitors showed insignificant SILC and progressive breakdown until it went into hard breakdown. Based on observed stress current behavior (I_g-t), SILC and charge-to-breakdown (Q_{BD}), it is believed that interfacial layer initiates progressive breakdown of metal gate/high-κ/SiO_2/Si gate stacks at room temperature. From normalized SILC ($\Delta J_g/J_{g0}$) at accelerated temperature and activation energy extracted from Weibull distribution of the time-to-breakdown data show IL initiates the gate stack breakdown at higher temperatures as well.

To better understand the defects origin, key parameters of negative bias temperature instability (NBTI) and time dependent dielectric breakdown (TDDB)

reliabilities in HfO_2/SiO_2 gate stacks have been compared. A quantitative agreement was observed for the activation energies of threshold voltage change and SILC. The quality and thickness variation of the IL causes similar degradation on both NBTI and TDDB indicating that these two reliability issues are due to identical defect types present in the IL.

Constant voltage stress has been applied to investigate statistical distribution of 1^{st} breakdown (T_{BD}) for small sample size. Because the statistical distribution of T_{BD} followed Weibull distribution, large sample size was not required. But the relevant failure distributions (F_{FAIL}) at I_{FAIL} are non-Weibull including the progressive breakdown (PBD) phase for high-κ/metal gate (HKMG) dielectrics. A new methodology using hybrid two-stage stresses has been developed to study progressive BD phase for high-κ and SiO_2. It was found that reliability parameters of progressive breakdown time (T_{PBD}) and non-Weibull T_{FAIL} distribution can be efficiently captured by voltage ramp stress technique. Even though ramp voltage stress technique has been used earlier to study 1^{st} breakdown Weibull distribution, there was confusion regarding the applicable highest ramp rate. It was reported that ramp rate higher than 1V/s, the conversion from VRS to CVS fails. But this work clarifies this confusion showing various ramp rates along with faster than 1 V/s and demonstrating excellent agreement between the CVS and VRS data.

In a nutshell, the impact of this research is that it presented a better understanding of the weak link for the high-κ gate stack breakdown. Correlation of NBTI and TDDB provides a comprehensive story of the role of high-κ and interfacial layer. Also, the developed VRS method would be useful to characterize both progressive BD phase and final BD of high-κ and any other dielectric materials. Eventually it would be able to

replace the time-consuming CVS measurements as an efficient methodology and reduce the resources and manufacturing cost.

7.2 Future Work

High-k nFETs suffer from significant positive bias temperature instability (PBTI) and stress-induced leakage current (SILC). When positive bias is applied during TDDB, SILC and PBTI makes the breakdown detection challenging. Cartier *et al.* showed a direct correlation ($\Delta I_g/I_g \sim \Delta V_T^3$) of stress-induced leakage current and ΔV_T at both room and accelerated temperatures due to PBT stress [33]. Early findings show that V_T instability and SILC generation are due to the same defects which are Oxygen vacancy related shallow defects generated in the HfO_2. More detailed work is required to isolate PBTI and TDDB for high-κ nFETs.

VRS method was applied to high-κ gate stack and ultra-thin SiO_2 to study time-to-fail distributions. Based on the non-Weibull distribution results found on these two structures, a conclusion was given in chapter 6 that interfacial layer was initiating breakdown in high-κ gate stack. But to make the study coherent, VRS method should also be applied to HfO_2-only control structure. This would provide additional confirmation on the weak link for the high-κ gate stack.

REFERENCES

[1] S. –H. Lo, D. A. Buchanan, Y. Taur, and W. Wang, *IEEE Electron Device Letters*, vol. 18, pp. 209-211, 1997.

[2] http://www.itrs.net/Links/2009Winter/Presentations/Conference/FEP_121609.pdf.

[3] P. K. Roy, and I. C. Kizilyalli, *Applied Physics Letters*, vol. 72, pp. 2835-2837, 1998.

[4] K. Eisenbeiser *et al.*, *Applied Physics Letters*, vol. 76, pp. 1324-1326, 2000.

[5] H. F. Luan *et al.*, *Technical Digest of International Electron Device Meeting*, p. 609, 1998.

[6] S. A. Campbell *et al.*, *IEEE Transactions on Electron Devices*, vol. 44, p. 104, 1997.

[7] Z. Jin, H. S. Kwok, M. Wong, *IEEE Electron Device Letters*, vol. 19, p. 502, 1998.

[8] S. P. Muraka, and C. C. Chang, *Applied Physics Letters*, vol. 37, p. 639, 1980.

[9] S. Stemmer, *Journal of Vacuum Science Technology*, vol. 22, p. 791, 2004.

[10] M. L. Green *et al.*, *Journal of Applied Physics*, vol. 92, p. 7168, 2002.

[11] X. Yu, C. Zhu, M. Yu, M. F. Li, A. Chin, C. H. Tung, D. Gui, and D.-L. Kwong, *Technical Digest of International Electron Device Meeting*, p. 31, 2005.

[12] T. Ma *et al.*, *IEEE Transactions on Electron Devices*, vol. 48, p. 2348, 2001.

[13] M. Li, Z. Zhang, S. A. Campbell, W. L. Gladfelter, M. P. Agustin, D. O. Klenov, and S. Stemmer, *Journal of Applied Physics*, vol. 98, p. 054506, 2005.

[14] N. Lu, H.-J. Li, M. Gardner, S. Wickramanayaka, and D.-L. Kwong, *IEEE Electron Device Letters*, vol. 26, p. 298, 2005.

[15] R. Choi, S. J. Rhee, J. C. Lee, B. H. Lee, and G. Bersuker, *IEEE Electron Device Letters*, vol. 26, p. 197, 2005.

[16] G. Bersuker, and P. Zeitzoff, *Topics in Applied Physics*, vol. 106, pp. 367-377, 2006.

[17] H. R. Harris, R. Choi, J. H. Sim, C. D. Young , P. Majhi, B. H. Lee, and G. Bersuker, *IEEE Electron Device Letters*, vol. 26, no. 11, pp. 839-841, 2005.

[18] G. Ribes, J. Mitard, M. Denais, S. Bruyere, F. Monsieur, C. Parthasaarathy, E. Vincent, and G. Ghibaudo, *IEEE Transactions on Device & Materials Reliability*, vol. 5, p. 5, 2005.

[19] H. R. Huff, and D. C. Gilmer, *High Dielectric Constant Materials, Springer*, Berlin, 2005.

[20] H. Wong, B. Sen, V. Filip, and M. C. Poon, *Thin Solid Films*, vol. 504, no. 1-2, pp. 192-196, 2006.

[21] J. W. McPherson, J. Kim, A. Shanware, H. Mogul, and J. Rodriguez, *IEEE Transactions on Electron Devices*, vol. 50, no. 8, pp. 1771-1778, 2003.

[22] G. Bersuker, B. Foran, K. van Benthem, S. J. Pennycook, P. M. Lenahan, and J. T. Ryan, *Journal of Applied Physics*, vol. 100, no. 9, 094108, 2006.

[23] R. H. Fowler, and L. Nordheim, Proc. R. Soc. London, Ser. A 119, p. 173, 1928.

[24] M. Lenzlinger, and E. H. Snow, *Journal of Applied Physics*, vol. 40, p. 278, 1969.

[25] D. J. DiMaria, E. Cartier, and D. Arnold, *Journal of Applied Physics*, vol. 73, p. 3367, 1993.

[26] D. J. DiMaria, E. Cartier, and D. A. Buchanan, *Journal of Applied Physics*, vol. 80, 30434, 1996.

[27] D. J. DiMaria, *Solid-State Electronics*, vol. 41, p. 957, 1997.

[28] J. H. Stathis, *IBM Journal of Research and Development*, vol. 46, p. 265, 2002.

[29] M. Alam, B. Weir, J. Bude, P. Silverman, and A. Ghetti, *Microelectronic Engineering*, vol. 59, p. 137, 2001.

[30] J. H. Stathis, and D. J. Di Maria, *Technical Digest of International Electron Device Meeting*, pp. 167-170, 1998.

[31] D. J. DiMaria, *Applied Physics Letters*, vol. 75, p. 2427, 1999.

[32] S. Lombardo, J. H. Stathis, B. P. Linder, K. L. Pey, F. Palumbo, and C. H. Tung, *Journal of Applied Physics*, vol. 98, 121301, 2005.

[33] E. Cartier, and A. Kerber, *IEEE International Reliability Physics Symposium Proceedings*, pp. 486-492, 2009.

[34] D. K. Schroder, and J. A. Babcock, *Journal of Applied Physics*, vol. 94, pp. 1-18, 2003.

[35] R. Degraeve, T. Kauerauf, A. Kerber, E. Catier, B. Govoreanu, Ph. Roussel, L. Pantisano, P. Blomme, B. Kaczer, and G. Groeseneken, *IEEE International Reliability Physics Symposium Proceedings*, pp. 23-28, 2003.

[36] K. Torii, K. Shiraishi, S. Miyazaki, Y. Yamabe, M. Boero, T. Chikyow, K. Yamada, H. Kitaji, and T. Arikado, *Technical Digest of International Electron Device Meeting*, pp. 129-132, 2004.

[37] C. Sah, *Solid State Electronics*, vol. 33, p.167, 1990.

[38] D. J. DiMaria, and J. W. Stasiak, *Journal of Applied Physics*, vol. 65, p. 2342, 1989.

[39] M. V. Fischetti, D. J. DiMaria, S. D. Brorson, T. N. Theis, and J. R. Kirtley, *Physical Review B*, vol. 31, p. 8124, 1985.

[40] Z. A. Weinburg and M. V. Fischetti, *Journal of Applied Physics*, vol. 57, p. 443, 1985.

[41] N. Klein, and P. Solomon, *Journal of Applied Physics*, vol. 47, p. 4364, 1976.

[42] I. C. Chen, S. Holland, K. K. Young, C. Chang, and C. Hu, *Applied Physics Letters*, 49, pp. 669, 1986.

[43] E. Wu, E. Nowak, A. Vayshenker, J. McKenna, D. Harmon, and R. Vollertsen, *IEEE Transactions on Device & Materials Reliability*, vol. 1, pp. 69, 2001.

[44] G. Ribes *et al.*, *IIRW Final Report*, pp. 75-78, 2005.

[45] T. P. Ma *et al.*, *IEEE TDMR*, 5, pp. 36-44, 2005.

[46] J. Maserijian, and N. Zamani, *Journal of Applied Physics*, vol. 53, p. 559, 1982.

[47] D. J. DiMaria, and E. Cattier, *Journal of Applied Physics*, vol. 78, no. 6, pp. 3883-3894, 1995.

[48] R. R. Rofan, and C. Hu, *IEEE Electron Device Letters*, vol. 12, p. 632, 1991.

[49] G. W. Yoon, A. B. Joshi, J. Kim, and D.-L. Kwong, *IEEE Electron Device Letters*, vol. 14, pp. 231-233, 1993.

[50] D. J. Dumin, *IEEE Transactions on Electron Devices*, vol. 40, p. 986, 1993.

[51] K. E. Schuegraf, and C. Hu, *IEEE Transactions on Electron Devices*, vol. 41, pp. 761, 1994.

[52] G. Hen-rink, T. Endoh, and R. Shirota, *Japanese Journal of Applied Physics*, vol. 33, p. 546, 1994.

[53] D. J. DiMaria, *Applied Physics Letters*, vol. 51, p. 655, 1987.

[54] D. J. DiMaria, *Journal of Applied Physics*, vol. 68, p. 5234, 1990.

[55] D. I. DiMaria, and J. H. Stathis, *Journal of Applied Physics*, vol. 70, p. 1500, 1991.

[56] M. M. Heyns, D. Krishna Rao, and R. F. Dekeersmaecker, *Applied Surface Science*, vol. 39, p. 327, 1989.

[57] A. V. Schwerin, and M. M. Heyns, edited by W. Eccleston, and M. Uren (Adam Hilger, New York), pp. 263-266, 1991.

[58] D. A. Buchanan, *Applied Physics Letters*, vol. 60, p. 216, 1992.

[59] A. V. Schwerin, M. M. Heyns, and W. Weber, *Journal of Applied Physics*, vol. 67, pp. 7595, 1990.

[60] T. Nishida, and S. E. Thompson, *Journal of Applied Physics*, 69, pp. 3986, 1991.

[61] Y. Nissan-Cohen, and T. Gorczyca, *IEEE Electron Device Letters*, vol. 9, p. 287, 1988.

[62] P. E. Blöchl, and J. H. Stathis, *Physics Review Letters*, 83, p. 372, 1999.

[63] V. V. Afanas'ev, and A. Stesmans, *Journal of The Electrochemical Society*, 146, p. 3409, 1999.

[64] A. Yokozawa, and Y. Miyamoto, *Journal of Applied Physics*, vol. 88, p. 4542, 2000.

[65] Y. -H. Kim, and J. C. Lee, *Microelectronics Reliability*, vol. 44, no. 2, pp. 183-193, 2004.

[66] N. A. Chowdhury, *PhD Thesis*, New Jersey Institute of Technology, 2007.

[67] R. Degraeve, G. Groeseneken, R. Bellens, M. Depas, and H. E. Maes, *Technical Digest International Electron Devices Meeting*, pp. 863-866, 1995.

[68] M. Houssa, T. Nigam, P. W. Mertens, and M. M. Heyns, *Journal of Applied Physics*, vol. 84, pp. 4351–4355, 1998.

[69] J. H. Stathis, and D. J. DiMaria, *Technical Digest International Electron Devices Meeting*, pp. 167–170, 1998.

[70] J. H. Stathis, *International Reliability Physics Symposium Proceedings*, pp. 132-149, 2001.

[71] Ph. J. Roussel, R. Degraeve, S. Sahhaf, and G. Groeseneken, *Microelectronic Engineering*, vol. 84, pp. 1925-1928, 2007.

[72] S. Bruyere, E. Vincent, and G. Ghibaudo, *International Reliability Physics Symposium Proceedings*, pp. 48-54, 2000.

[73] E. Y. Wu, and J. Sune, *IEEE Electron Device Letters*, vol. 24, no. 11, pp. 692-694, 2003.

[74] R. Pagano, S. Lombardo, F. Palumbo, P. Kirsch, S.A. Krishnan, C. Young, R. Choi, G. Bersuker, and J.H. Stathis, *Microelectronics Reliability*, vol. 48 , pp. 1759-1764, 2008.

[75] J. C. Tsang, and B. P. Linder, *Applied Physics Letters*, vol. 84, pp. 4642-4643, 2004.

[76] B. P. Linder, and J. H. Stathis, *Microelectronic Engineering*, vol. 72, pp. 24-28, 2004.

[77] N. Rahim, and E. Wu, abstract accepted for publication in IEEE International Reliability Physics Symposium, 2011.

[78] B. E. Weir *et al.*, *Technical Digest of International Electron Device Meeting*, p. 73, 1997.

[79] J. Sune, and E.Y. Wu, *Technical Digest of International Electron Device Meeting*, p. 147, 2002.

[80] J. Sune, E.Y. Wu, D. Jimenez, R.P. Vollertsen, and E. Miranda, *Technical Digest of International Electron Device Meeting*, p. 117, 2001.

[81] T. Kauerauf, R. Degraeve, M. B. Zahid, M. Cho, B. Kaczer, Ph. Roussel, G. Groeseneken, H. Maes, and S. De Gendt, *IEEE Electron Device Letters*, vol. 26, no. 10, pp. 773-775, 2005.

[82] J. Sune, G. Mura, and E. Miranda, *IEEE Electron Device Letters*, vol. 21, p.167, 2000.

[83] J. C. Jackson, T. Robinson, O. Oralkan, and D.J. Dumin, *Applied Physics Letters*, vol. 71, p. 3682, 1997.

[84] B. P. Linder, S. Lombardo, J.H. Stathis, A. Vayshenker, and D.J. Frank, *IEEE Electron Device Letters*, vol. 23, p. 661, 2002.

[85] M. A. Alam, B.E. Weir, P.J. Silverman, Y Ma, and D. Hwang, *Technical Digest of International Electron Device Meeting*, p. 529, 2000.

[86] J. Sune, E. Miranda, M. Nafria, and X. Aymerich, "Point Contact Conduction at the Oxide Breakdown of MOS Devices", *Technical Digest of International Electron Device Meeting*, p. 191, 1998.

[87] K. Okada, T. Horikawa, H. Satake, H. Ota, A. Ogawa, T. Nabatame, and A. Toriumi, *IEEE International Reliability Physics Symposium Proceedings*, pp. 189–194, 2006.

[88] R. Degraeve, B. Kaczer, M. Houssa, G. Groeseneken, M. Heyns, and J. S. Jeon, *Technical Digest International Electron Devices Meeting*, pp. 327–330, 1999.

[89] S. Zaima, T. Furuta, and Y. Yasuda, *Journal of The Electrochemical Society*, vol. 137, p. 1295, 1990.

[90] E. Rymaszzewski, T. Lu, M. Nielsen, and J. Kim, *Proceeding Electrochemical Society*, pp. 216, 1998.

[91] J. McPherson, J. Kim, A. Shanware, H. Mogul, and J. Rodriguez, *Technical Digest of International Electron Device Meeting*, p. 633, 2002.

[92] J. McPherson, J-Y. Kim, A. Shanware, and H. Mogul, *Applied Physics Letters*, vol. 82, no. 13, pp. 2121-2123, 2003.

[93] T. Nigam, A. Kerber, and P. Peumans, *IEEE International Reliability Physics Symposium Proceedings*, pp. 523-530, 2009.

[94] S. Mahapatra, P. B. Kumar, and M. A. Alam, *IEEE Transactions on Electron Devices*, vol. 51, pp. 1371–1379, 2004.

[95] S. Chakravarthi, A. T. Krishnan, V. Reddy, C. F. Machala, and S. Krishnan, *IEEE International Reliability Physics Symposium Proceedings*, pp. 273–282, 2004.

[96] H. Ershov, S. Saxena, H. Karbasi, S. Winters, S. Minehane, and J. Backcock, *Applied Physics Letters*, vol. 83, pp. 1647–1649, 2003.

[97] G. Chen, M. F. Li, C. H. Ang, J. Z. Zheng, and D. L. Kwong, *IEEE Electron Device Letters*, vol. 23, pp. 734–736, 2002.

[98] M. A. Alam, *Technical Digest of International Electron Device Meeting*, pp. 346–349, 2003.

[99] M. A. Alam *et al*., *Microelectronics Reliability*, vol. 47, pp. 853-862, 2007.

[100] S. Rangan, N. Mielke, and E. C. C. C. Yeh, *Technical Digest of International Electron Device Meeting*, p. 341, 2003.

[101] D. Varghese, D. Saha, S. Mahapatra, K. Ahmed, F. Nouri, and M. Alam, *Technical Digest of International Electron Device Meeting*, pp. 684-687, 2005.

[102] C. R. Parthasarathy, M. Denais, V. Huard, G. Ribes, E. Vincent, and A. Bravaix, *IEEE International Reliability Physics Symposium Proceedings*, pp. 471-477, 2006.

[103] E. N. Kumar, V. D. Maheta, S. Purawat, A. E. Islam, C. Olsen, K. Ahmed, M. A. Alam, S. Mahapatra, *Technical Digest of International Electron Device Meeting*, pp. 809-812, 2007.

[104] H. Reisinger, O. Blank, W. Heinrigs, A. Muhlhoff, W. Gustin, and C. Schlunder, *IEEE International Reliability Physics Symposium Proceedings*, pp. 448-453, 2006.

[105] A. Kerber, E. Cartier, L. Pantisano, R. Degraeve, G. Groeseneken, H. E. Maes, and U. Schwalke, *Microelectronic Engineering*, vol. 72, no. 1–4, pp. 267–272, 2004.

[106] G. Bersuker, J. Sim, C. S. Park, C. Young, S. Nadkarni, R. Choi, and B. H. Lee, *IEEE International Reliability Physics Symposium Proceedings*, pp. 179–183, 2006.

[107] J. H. Sim, S. C. Song, P. D. Kirsch, C. D. Young, R. Choi, D. L. Kwong, B. H. Lee, and G. Bersuker, *Microelectronic Engineering*, vol. 80, pp. 218–221, 2005.

[108] T. Yang, C. Shen, M. F. Li, C. H. Ang, C. X. Zhu, Y.-C. Yeo, G. Samudra, S. C. Rustagi, M. B. Yu, and D.-L. Kwong, *IEEE Electron Device Letters*, vol. 26, no. 11, pp. 826–828, 2005.

[109] A. Neugroschel, G. Bersuker, R. Choi, and B. H. Lee, *IEEE Transactions on Device and Materials Reliability*, vol. 8, no. 1, pp. 47-61, 2008.

[110] N. Rahim, and D. Misra, *Electrochemical Society Transactions*, vol. 28, no. 2, pp. 323-333, 2010.

[111] A. Kerber, E. Cartier, and L. Pantisano, *IEEE Electron Device Letters*, vol. 24, pp. 87-89, 2003.

[112] K. Tse, D. Liu, K. Xiong, and J. Robertson, "Oxygen vacancies in high-k oxides," *Microelectronic Engineering*, vol. 84, no. 9-10, pp. 2028–2031, 2007.

[113] C. D. Young, S. Nadkarni, D. Heh, H. R. Harris, R. Choi, J. J. Peterson, J. H. Sim, S. A. Krishnan, J. Barnett, E. Vogel, B. H. Lee, P. Zeitzoff, G. A. Brown, and G.

Bersuker, *IEEE International Reliability Physics Symposium Proceedings*, pp. 169–173, 2006.

[114] G. Reimbold, J. Mitard, X. Garros, C. Leroux, G. Ghibaudo, and F. Martin, *Microelectronics Reliability*, vol. 47, no. 4-5, pp. 489–496, 2007.

[115] A. Barman, *IEEE International Reliability Physics Symposium Proceedings*, pp. 204–209, 1981.

[116] E. Rosenbaum, J. C. King, and C. Hu, *IEEE Transactions on Electron Devices*, vol. 43, no. 1, pp. 70–80, 1996.

[117] A. Martin, P. O'Sullivan, and A. Mathewson, *IEEE International Integrated Reliability Workshop*, pp. 106–112, 1994.

[118] A. Kerber *et al*., *Microelectronics Reliability*, pp. 513-517, 2007.

[119] E. Wu *et al*., *Technical Digest of International Electron Device Meeting*, pp. 397-400, 2009.

[120] M. Alvisi, M. Di Giulio, S.G. Marrone, M.R. Perrone, M.L. Protopapa, A. Valentini, and L. Vasanelli, *Thin Solid Films*, 358, p. 250, 2000.

[121] C. L. Platt, B. Dieny, and A. E. Berkowitz, *Applied Physics Letters*, vol. 69, p. 2291, 1996.

[122] M. T. Thomas, *Journal of The Electrochemical Society*, 117 396, 1970.

[123] E. P. Gusev, E. Cartier, D.A. Buchanan, M. Gribelyuk, M. Copel, H. Okorn-Schmidt, and C. D'Emic, *Microelectronic Engineering*, vol. 59, p. 341, 2001.

[124] K. Kukli, M. Ritala, T. Sajavaara, J. Keinonen, and M. Leskela, *Chemical Vapor Deposition*, vol. 8, p. 199, 2002.

[125] J. F. Conley Jr., Y. Ono, D.J. Tweet, W. Zhuang, and R. Solanki, *Journal of Applied Physics*, vol. 93, p. 712, 2003.

[126] D. C. Gilmer, R. Hegde, R. Cotton, R. Garcia, V. Dhandapani, D. Triyoso, D. Roan, A. Franke, R. Rai, L. Prabhu, C. Hobbs, J.M. Grant, L. La, S. Samavedam, B. Taylor, H. Tseng, and P. Tobin, *Applied Physics Letters*, vol. 81, p. 1288, 2002.

[127] A. C. Jones, *Journal of Material Chemistry*, vol. 12, p. 2576, 2002.

[128] A. G. Thompson, *Materials Letters*, vol. 30, p. 255, 1997.

[129] A. A. Sokolov, A. A. Ovchinnikov, K. M. Lysenkov, D. E. Marchenko, and E. O. Filatova, *Technical Physics*, vol. 55, no. 7, pp. 1045–1050, 2010.

[130] J. Barnett, N. Moumen, J. Gutt, M. Gardner, C. Huffman, P. Majhi, J. J. Peterson, S. Gopalan, B. Foran, H.-J. Li, B. H. Lee, G. Bersuker, P. Zeitzoff, G. A. Brown, P. Lysaght, C. D. Young, R. W. Murto, and H. R. Huff, *Proceedings Materials Research Symposium* , vol. 811, p. 341, 2004.

[131] P. D. Kirsch, M. A. Quevedo-Lopez, H. –J. Li, Y. Senzaki, J. J. Peterson, S. C. Song, S. A. Krishnan, N. Moumen, J. Barnett, G. Bersuker, P. Y. Hung, B. H. Lee, T. Lafford, Q. Wang, D. Gay, and G. Ekerdt, *Journal of Applied Physics*, vol. 99, 023508, 2006.

[132] N. Chowdhury, G. Bersuker, C. Young, R. Choi, S. Krishnan, and D. Misra, *Microelectronic Engineering*, vol. 85, pp. 27-35, 2008.

[133] B. H. Lee, C. H. Kang, P. Kirsch, D. Heh, C. D. Young, H. Park, J. Yang, G. Bersuker, S. Krishnan, R. Choi, and H. –D. Lee, *Applied Physics Letters*, vol. 91, 243514, 2007.

[134] J. R. Hauser, and K. Ahmed, *International Conference on Characterization and Metrology for ULSI Technology*, pp. 235-239, 1998.

[135] D. K. Schroder, *Semiconductor Material and Device Characterization*, 2nd Ed., John Wiley and Sons, New York, pp. 386-388, 1998.

[136] T. Kauerauf, B. Govoreanu, R. Degraeve, G. Groeseneken, and H. Maes, *Solid-State Electronics*, vol. 49, pp. 695–701, 2005.

[137] T. Nigam, R. Degraeve, G. Groeseneken, M. M. Heyns, and H. E. Maes, *IEEE International Reliability Physics Symposium Proceedings*, p. 381, 1999.

[138] K. Okada, Extended Abstract of the SSDM, Yokohama, p. 92, 1997.

[139] A. Aal, IEEE Integrated Reliability Final report, pp 133-136, 2008.

[140] J. Sune, and E. Miranda, *Technical Digest of International Electron Device Meeting*, pp. 533-536, 2000.

[141] G. Bersuker, N. Chowdhury, C. Young, D.Heh, D. Misra, and R. Choi, *IEEE International Reliability Physics Symposium Proceedings*, vol. 45, pp. 49-54, 2007.

[142] M. Depas, T. Nigam, and M. Heyns, *IEEE Transactions on Electron Devices*, vol. 43, pp. 1499-1504, 1996.

[143] F. Mondon, and S. Blonkowski, *Microelectronics Reliability*, vol. 43, pp. 1259-1266, 2003.

[144] J. W. McPherson, J. Kim, A. Shanware, H. Mogul, and J. Rodriguez, *IEEE Transactions on Electron Devices*, vol. 50, no. 8, pp.1771-1778, 2003.

[145] M. Houssa, Editor. High-k Dielectrics, Bristol and Philadelphia: Institute of Physics Publishing, pp. 597-598, 2004.

[146] M. A. Alam, *IEEE Transactions on Electron Devices*, vol. 49, no. 2, 2002.

[147] D. Buchanan, J. Stathis, E. Cartier, and D. J. DiMaria, *Microelectronics Engineering, 36*, p. 329, 1997.

[148] G. H. Parker, and C. A. Mead, Applied *Physics Letter, 14*, p. 21, 1969.

[149] D. Ielmini, A. S. Spinelli, A. Rigamonti, and A. L. Lacaita, *IEEE Transactions on Electron Devices*, vol. 47, p. 1266, 2000.

[150] P. E. Nicollian, M. Rodder, D. T. Grider, P. Chen, R. M. Wallace, and S. V. Hattangady, *IEEE International Reliability Physics Symposium Proceedings, 37,* pp. 400-404, 1999.

[151] F. Crupi, R. Degraeve, A. Kerber, D. Kwak, and G. Groeseneken, *IEEE International Reliability Physics Symposium Proceedings*, vol. 42, p. 181, 2004.

[152] N. Rahim, and D. Misra, *Electrochemical Society Transactions*, vol. 13, no. 2, pp. 91-97, 2008.

[153] K. Okada, H. Kubq, A. Ishinaga, and K. Yoneda, *Symposium on VLSI Technology*, p. 158, 1998.

[154] N. Rahim, N. A. Chowdhury and D. Misra, *Electrochemical Society Transactions*, vol. 11, pp. 629-638, 2007.

[155] B. Kaczer, R. Degraeve, N. Pangon, T. Nigam and G. Groeseneken, *Microelectronic Engineering*, vol. 48, p. 47, 1999.

[156] J. W. McPherson, V. K. Reddy and H. C. Mogul, *Applied Physics Letters*, vol. 71, p. 1101, 1997.

[157] C. Petit, and D. Zander, *Microelectronics Reliability*, vol. 47, p. 401, 2007.

[158] R. Moonen, P. Vanmeerbeek, G. Lekens, W. De Ceuninck, P. Moens and J. Boutsen, *Microelectronics Reliability*, vol. 47, p. 1389, 2007.

[159] E. Y. Wu, J. Sune, E. Nowak, W. Lai, and J. McKenna, *Technical Digest of International Electron Device Meeting*, vol. 125, p. 6.3.1, 2001.

[160] B. Kaczer, R. Degraeve, N. Pangon, and G. Groeseneken, *IEEE Transactions on Electron Devices*, vol. 47, p. 1514, 2000.

[161] T. Yamaguchi, I. Hirano, R. Ijjima, K. Sekine, M. Takayanagi., K. Eguchi, Y. Mitani, and N. Fukushima, *IEEE International Reliability Physics Symposium Proceedings*, vol. 43, p. 67, 2005.

[162] K. Okada, T. Horikawa, H. Satake, S. Inumiya, Y. Akasaka, F. Ootsuka, Y. Nara, H. Ota, T. Nabatame, and A. Toriumi, *Symposium on VLSI Technology*, p. 34, 2007.

[163] P. Samantha, T. Y. Man, Q. Zhang, C. Zhu, and M. Chan, *Journal of Applied Physics*, vol. 100, p. 094507, 2006.

[164] A Meinertzhagen, C. Petit, D. Zander, O. Siimonetti, T. Maurel, and M. Jourdain, *Journal of Applied Physics*, vol. 91, p. 2123, 2002.

[165] J. Frenkel, *Physical Review*, vol. 54, p. 647, 1938.

[166] G. Ribes, S. Bruye`re, M. Denais , F. Monsieur , V. Huard, D. Roy, and G. Ghibaudo, *Microelectronics Reliability*, vol. 45, p. 1842, 2005.

[167] J. McPherson, and H. C. Mogul, *Journal of Applied Physics*, vol. 84, p. 1513, 1998.

[168] N.A. Chowdhury, and D. Misra, *Journal of Electrochemical Society*, vol. 154, p. G30, 2007.

[169] A. Shanware, J. McPherson, M. R. Visokay, J. J. Chambers, A. L. P. Rotondaro, H. Bu, M. J. Bevan, R. Khamankar, and L. Colombo, *Technical Digest of International Electron Device Meeting*, vol. 137, p. 6.6.1, 2001.

[170] P. Kirsch *et al.*, *Technical Digest of International Electron Device Meeting*, p. 629, 2006.

[171] S. Zafar, M. Yang, E. Gusev, A. Callegari, J. Stathis, T. Ning, R. Jammy, and M. Ieong, *Symposium on VLSI Technology*, pp. 128–129, 2005.

[172] S. Zafar, A. Kumar, E. Gusev, and E. Cartier, *IEEE Transactions on Device and Materials Reliability*, vol. 5, no. 1, pp. 45–64, 2005.

[173] M. Houssa, G. Pourtois, M.M. Heyns, and A. Stesmans, *Journal of Physics Condensed Matter*, vol. 17, no. 21, pp. S2075-S2088, 2005.

[174] K. Okada, H. Ota, A. Hirano, A. Ogawa, T. Nabatame, and A. Toriumi, *IEEE International Reliability Physics Symposium Proceedings*, pp. 661–662, 2008.

[175] R. Degraeve, T. Kauerauf, M. Cho, M. Zahid, L-Å. Ragnarsson, D.P. Brunco, B. Kaczer, P. Roussel, S. De Gendt, and G. Groeseneken, *Technical Digest of International Electron Device Meeting*, pp. 419–420, 2005.

[176] G. Bersuker, D. Heh, C.D. Young, L. Morassi, A. Padovani, L. Larcher, K. S. Yew, Y. C. Ong, D. S. Ang, K. L. Pey, and W. Taylor, *IEEE International Reliability Physics Symposium Proceedings*, pp. 373-378, 2010.

[177] N. Rahim, and D. Misra, *Journal of The Electrochemical Society*, vol. 155, no. 10, pp. G194-G198, 2008.

[178] S. Tsujikawa, K. Watanabe, R. Tsuchiya, K. Ohnishi, and J. Yugami, *Symposium on VLSI Technology*, pp. 139-140, 2003.

[179] K. Okada, H. Ota, T. Nabatame, and A. Toriumi, *IEEE International Conference on Integrated Circuit Design and Technology*, pp. 87-90, 2008.

[180] N. A. Chowdhury, D. Misra, G. Bersuker, C. Young, and R. Choi, *Journal of The Electrochemical society*, vol. 154, no. 12, pp. G298-G306, 2007.

[181] A. Neugroschel, G. Bersuker, R. Choi, C. Cochrane2, P. Lenahan, D. Heh, C. Young, C.Y. Kang, B.H. Lee, and R. Jammy, *Technical Digest of International Electron Device Meeting*, 2006.

[182] M. Jo, M. Chang, S. Kim, H-S. Jung, R. Choi, and H. Hwang, *IEEE Electron Device Letters*, vol. 30, no. 3, p. 291, 2009.

[183] N. Rahim, and D. Misra, *IEEE Transactions on Device and Materials Reliability*, vol. 8, no. 4, pp. 689-693, 2008.

[184] J. W. McPherson, R. B. Khamankar, and A. Shanware, *Journal of Applied Physics*, vol. 88, no. 9, pp. 5351–9, 2000.

[185] B.H. Lee, *Proceedings of IEEE International Conference on IC Design and Technology*, p. 83, 2009.

[186] M. Sato, K. Yamabe, K. Shiraishi, S. Miyazaki, K. Yamada, C. Tamura, R. Hasunuma, S. Inumiya, T. Aoyama, Y. Nara, and Y. Ohji, *Electrochemical Society Transactions*, vol. 11, no. 4, p. 615, 2007.

[187] R. Degraeve, M. Aoulaiche, B. Kaczer, P. Roussel, T. Kauerauf, S. Sahhaf, and G. Groeseneken, *Proc. 15th International Symposium on the Physical and Failure Analysis of Integrated Circuits*, pp. 1-6, 2008.

[188] B. P. Linder, A. Kerber, E. Cartier, S. Krishnan, and J. H. Stathis, *IEEE International Reliability Physics Symposium Proceedings*, pp. 510–513, 2009.

[189] A. Kerber, E. Cartier, B. P. Linder, S. Krishnan, and T. Nigam, *IEEE International Reliability Physics Symposium Proceedings*, pp. 505–509, 2009.

[190] P. McIntyre, "Bulk and Interfacial Oxygen Defects in HfO2 Gate Dielectric Stacks: A Critical Assessment," *Electrochemical Society Transactions*, vol. 11, no. 4, pp. 235-249, 2007.

[191] A. Kerber *et al*., *IEEE Electron Device Letters*, vol. 27, no. 7, pp. 609-611, 2006.

[192] S. C. Fan *et al.*, *IEEE International Reliability Physics Symposium Proceedings*, pp. 625-626, 2006.

[193] K. Okada *et al.*, *Symposium on VLSI Technology*, pp. 143-144, 1997.

[194] B. Linder *et al.*, *IEEE International Reliability Physics Symposium Proceedings*, pp. 403-408, 2003.

[195] E. Y. Wu, A. Vayshenker, E. Nowak, J. Sune, R.-P. Vollertsen, W. Lai, and D. Harmon, *IEEE Transactions on Electron Devices*, pp. 2244-2253, 2002.

[196] E. Rosenbaum, J. C. King, and C. Hu, *IEEE Transactions on Electron Devices*, pp. 70-80, 1996.

[197] A. martin, P. O'Sullivan, and A. Mathewson, *IEEE International Integrated Reliability Workshop Final report*, pp. 106-112, 1994.

[198] E. Wu, S. Tous, and J. Sune, *Technical Digest of International Electron Device Meeting*, pp. 493-496, 2007.

[199] T. Pompl, A. Kerber, M. Rohner, and M. Kerber, *Microelectronics Reliability*, vol. 46, pp. 1603-1607, 2006.

[200] E. Wu, J. Sune, B. Linder, R. Achanta, and S. Mittl, *submitted to International Reliability Physics Symposium Proceedings*, 2011.

[201] F. Monsieur, E. Vincent, D. Roy, S. Bruyere, J. C. Vildeuil, G. Pananakakis, and G. Ghibaudo, *IEEE International Reliability Physics Symposium Proceedings*, pp. 45-54, 2002.

[202] E. Wu, and J. Sune, *IEEE International Reliability Physics Symposium Proceedings*, pp. 36-45, 2006.