ABSTRACT

LOW JITTER PHASE-LOCKED LOOP CLOCK SYNTHESIS WITH WIDE LOCKING RANGE

by
Adnan Gündel

The fast growing demand of wireless and high speed data communications has driven efforts to increase the levels of integration in many communications applications. Phase noise and timing jitter are important design considerations for these communications applications. The desire for highly complex levels of integration using low cost CMOS technologies works against the minimization of timing jitter and phase noise for communications systems which employ a phase-locked loop for frequency and clock synthesis with on-chip VCO. This dictates an integrated CMOS implementation of the VCO with very low phase noise performance. The ring oscillator VCOs based on differential delay cell chains have been used successfully in communications applications, but thermal noise induced phase noise have to be minimized in order not to limit their applicability to some applications which impose stringent timing jitter and phase noise requirements on the PLL clock synthesizer. Obtaining lower timing jitter and phase noise at the PLL output also requires the minimization of noise in critical circuit design blocks as well as the optimization of the loop bandwidth of the PLL.

In this dissertation the fundamental performance limits of CMOS PLL clock synthesizers based on ring oscillator VCOs are investigated. The effect of flicker and thermal noise in MOS transistors on timing jitter and phase noise are explored, with particular emphasis on source coupled NMOS differential delay cells with symmetric

load elements. Several new circuit architectures are employed for the charge pump circuit and phase-frequency detector (PFD) to minimize the timing jitter due to the finite dead zone in the PFD and the current mismatch in the charge pump circuit. The selection of the optimum PLL loop bandwidth is critical in determining the phase noise performance at the PLL output. The optimum loop bandwidth and the phase noise performance of the PLL is determined using behavioral simulations. These results are compared with transistor level simulated results and experimental results for the PLL clock synthesizer fabricated in a 0.35 μm CMOS technology with good agreement.

To demonstrate the proposed concept, a fully integrated CMOS PLL clock synthesizer utilizing integer-N frequency multiplier technique to synthesize several clock signals in the range of 20-400 MHz with low phase noise was designed. Implemented in a standard 0.35-μm N-well CMOS process technology, the PLL achieves a period jitter of 6.5-ps (rms) and 38-ps (peak-to-peak) at 216 MHz with a phase noise of -120 dBc/Hz at frequency offsets above 10 KHz.

The specific research contributions of this work include (1) proposing, designing, and implementing a new charge pump circuit architecture that matches current levels and therefore minimizes one source of phase noise due to fluctuations in the control voltage of the VCO, (2) an improved phase-frequency detector architecture which has improved characteristics in lock condition, (3) an improved ring oscillator VCO with excellent thermal noise induced phase noise characteristics, (4) the application of self-biased techniques together with fixed bias to CMOS low phase noise PLL clock synthesizer for digital video communications ,and (5) an analytical model that describes the phase noise performance of the proposed VCO and PLL clock synthesizer.

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by
Adnan Gündel

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APPROVAL PAGE

LOW JITTER PHASE-LOCKED LOOP CLOCK SYNTHESIS WITH WIDE LOCKING RANGE

Adnan Gündel

Dr. William N. Carr, Dissertation Advisor — Date
Professor of Electrical and Computer Engineering, NJIT
Professor of Physics, NJIT

Dr. Jacob Klapper, Committee Member — Date
Professor of Electrical and Computer Engineering, NJIT

Dr. Roy H. Cornely, Committee Member — Date
Professor of Electrical and Computer Engineering, NJIT

Dr. Durga Misra, Committee Member — Date
Professor of Electrical and Computer Engineering, NJIT

Dr. Edip Niver, Committee Member — Date
Associate Professor of Electrical and Computer Engineering, NJIT

Mr. Saeed Abbasi, Committee Member — Date
Architect, Analog PLL, Advanced Micro Devices, Inc., AMD

BIOGRAPHICAL SKETCH

Author: Adnan Gündel

Degree: Doctor of Philosophy

Date: March 2007

Undergraduate and Graduate Education:

- Doctor of Philosophy in Electrical Engineering,
  New Jersey Institute of Technology, Newark, NJ, 2007
- Master of Science in Electrical Engineering,
  Middle East Technical University, Ankara, Turkey, 1987
- Bachelor of Science in Electrical Engineering,
  Middle East Technical University, Ankara, Turkey, 1984

Major: Electrical Engineering

Presentations and Publications:

Adnan Gündel and William N. Carr,
"A low jitter CMOS PLL clock synthesizer with 20-400 MHz locking range," in Proc. ISCAS-2007, 2007 IEEE International Symposium on Circuits and Systems.

Adnan Gündel and William N. Carr,
"Ultra low power CMOS PLL clock synthesizer for wireless sensor nodes," in Proc. ISCAS-2007, 2007 IEEE International Symposium on Circuits and Systems.

Adnan Gündel and William N. Carr,
"A micro-power $\Sigma\Delta$ A/D converter in 0.35-μm CMOS for low frequency applications," in LISAT-2007 Dig. Tech. Papers, 2007 IEEE Long Island Systems, Applications, and Technology Conference.

Adnan Gündel, S. Jorek, P. Janczykowski, A. Trezza, and R. Goldblatt,
"High performance low phase noise PLL clock synthesizer with LVDS outputs," in LISAT-2006 Dig. Tech. Papers, 2006 IEEE Long Island Systems, Applications, and Technology Conference.

Dedicated to my parents, H. Ali and Hatice Gündel

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CHAPTER 1

INTRODUCTION

1.1 Motivation

The use of phase-locked loops (PLL) for generating phase synchronous and frequency multiplied clocks by controlling phase and frequency with extremely high precision provides efficient solutions to requirements for low timing jitter and low phase noise in RF and high-speed data communication applications such as digital video, biomedical, wireless transceivers, microprocessors, serial link transceivers, and disk drive electronics. In most of these applications, clock signals are used as local oscillators to drive mixers or responsible for the clock and data recovery function for which the variation of clock edges, or timing jitter is an important performance parameter. As applications demand higher clock frequencies more stringent timing jitter requirements are imposed on the PLL because clocks with shorter periods are less tolerant to the random variation of the clock edges, i.e., to absolute jitter. For sensitive applications such as high-speed data processing and wireless transceivers, minimizing timing jitter is often one of the primary design tasks. This task requires careful attention to all of the noise sources in the active and passive circuit design blocks of the PLL and a careful analysis of the phase noise characteristic of the phase-locked loop system itself. In addition to timing jitter, spurious tones also limit the performance of high-speed communication systems.

Timing jitter occurs due to the random timing fluctuations of clock edges in the time domain. Spurious tones are caused by the systematic timing fluctuations in a clock signal. In the time domain, the presence of systematic timing fluctuations in a clock signal represents a periodic timing error. In the frequency domain, it manifests as the

undesired tones in the frequency spectrum. These two performance-limiting effects play a critical role in the operation of RF and high-speed communication systems and may impose constraints on performance requirements of those systems.

There are two major considerations for the analysis of timing error, or uncertainty in PLL clock synthesizers. The first analyzes random variations of the clock edges in time domain and is called timing jitter. The second is the phase noise, which is the frequency domain representation of the same phenomenon. In the frequency domain, the spectrum of a clock or oscillator signal centers at a single frequency but with the phase noise, it spreads the carrier power over neighboring channels and creates the phase noise skirts. Timing jitter occurs mostly due to thermal noise and 1/f noise in the active and passive devices of circuit design blocks of the PLL clock synthesizer. In particular, the phase noise of the voltage-controlled oscillator (VCO) is the most important source of timing jitter in PLL clock synthesizer applications among other sources that contribute to the phase noise of the PLL output signal. In addition to intrinsic noise sources in the circuit design blocks of the PLL, the noise on the frequency tuning voltage or current is also an inescapable source of phase noise. This can be a limiting factor in every voltage or current controlled oscillator (CCO) employed by communication systems. Sudden changes in supply voltage and substrate potential can also lead to frequency offsets and cause random phase fluctuations. This type of noise is often considered as the interference from the supply and substrate. In practice, among the other sources of noise, the effect of device thermal noise and 1/f noise, particularly noise in the VCO is fundamental and it often sets the performance limit for the PLL clock synthesizer.

Systematic variations in phase occur due to injection of signals from various parts of the circuit design blocks of the PLL causing perturbations in the phase of the clock or oscillator signals. However, these perturbations cause spurious tones instead of phase noise in the output spectrum of the PLL clock synthesizer. In PLL clock synthesizers, the spurious tones are mainly produced by the phase-frequency detector (PFD) circuit, the charge-pump (CP) circuit, and divider circuit located in the feedback loop of the PLL.

In high performance PLL clock synthesizer applications, a low phase noise VCO is needed for optimal performance. Achievement of low phase noise usually requires an oscillator with a high quality factor "Q" LC tank circuit. However, implementing a high-quality inductor in a standard CMOS process is limited by parasitic effects and often requires extra nonstandard processing steps. In addition, the integrated LC-tank oscillator generally has a narrow tuning range and therefore the performance of the PLL clock synthesizer is sensitive to the process variations. On the other hand, for fully-monolithic solutions, the ring-oscillator based VCO can be smoothly integrated in a standard CMOS process without taking extra processing steps because it does not require an inductor for the frequency tuning. Therefore, implementation of on-chip ring oscillators often results in a reduced cost and complexity in many PLL clock synthesizer applications requiring a low phase noise clock output. But the phase noise requirement of a particular application may raise questions as to their applicability for any particular clock synthesis.

This dissertation researches and formulates the design and implementation of an ultra-low jitter PLL clock synthesizer employing a differential delay cell ring oscillator VCO for fully monolithic high frequency applications. This research includes detail analysis to estimate the phase noise performance of the PLL clock synthesizer. In this

dissertation, circuit design techniques that lead to low phase noise and low timing jitter are described. The important design trade-offs at the circuit and system level are explored. Comparisons are made with other "state-of-the art" PLL clock synthesizer realizations published by other researchers in the open literature. Furthermore, this dissertation describes the circuit and physical design of the prototype ultra-low phase noise PLL chip.

1.2 Design Specifications

For demonstration purposes, an experimental prototype fabricated in a 0.35 μm CMOS process technology. The chip is designed based on the analysis of this work to meet the following specifications:

Table 1.1 Design Target Specifications

Frequency Range	20 MHz – 400 MHz
Input Reference Clock	10 MHz – 36 MHz
Maximum Operating Supply Current	25 mA
Power Supply Voltage Range	3 – 5 V
Clock Duty Cycle	45% – 55%
Maximum 1- σ Period Jitter (rms)	12 ps
Maximum peak-to-peak Period Jitter	100 ps
Phase Noise @ offsets ≥ 10 kHz	-118 dBc/Hz
LVDS Voltage Swing	400 mV
Device Technology	0.35-μm N-well CMOS

1.3 Thesis Organization

Chapter 2 introduces timing jitter and phase noise properties of the PLL clock synthesizers. The relationship between timing jitter and phase noise is discussed.

Chapter 3 is an introduction to the analysis and mathematical modeling of the charge-pump PLLs (CPLLs). In addition, issues concerning the noise modeling are discussed. In particular, the effects of timing jitter and phase noise at several levels of phase-locked loop system hierarchy, especially at the VCO level, are discussed.

Chapter 4 presents a detailed description of the system level design and behavioral modeling of the experimental PLL clock synthesizer fabricated in CMOS technology. A design procedures using models developed in Chapter 3 is presented. Useful expressions for the design of components of the PLL are derived. Circuit design techniques that help reduce jitter are presented. In addition, an efficient method for the prediction of the phase noise using behavioral simulation is presented.

Chapter 5 presents the circuit design of the design blocks of the PLL clock synthesizer and the experimental results for a prototype fabricated in a .35 μm CMOS process. Comparisons between behavioral level simulations and actual measurements are discussed. Furthermore, the conclusions based on the results of this work and suggestions for future work are presented in Chapter 6.

CHAPTER 2

JITTER AND PHASE NOISE IN PLL CLOCK SYNTHESIZERS

1.1 Introduction

A high performance low noise phase-locked loop frequency synthesizer is a key component in many of modern communication systems. A PLL frequency synthesizer often generates several sets of phase-synchronous and frequency-multiplied clock or oscillator signals from a very low noise input reference signal. PLL clock synthesizers can be considered as a special class of frequency synthesis and are particularly used for generating the system clock in high-speed data processing and communication applications such as microprocessors, digital signal processors, wireless transceivers, serial link transceivers, and disk drive electronics [1-7].

Timing errors limit the performance of communication systems. In PLL frequency synthesizer applications, timing errors in the clock or oscillator signals used by a communication system may impose constraints on performance requirements. When timing error due to phase fluctuations is present in the clock or oscillator signal, the timing information is severely obscured. Accurate characterization of timing errors produced by the PLL is crucial in many applications. Phase noise and timing jitter are the two most popular quantities for characterizing these errors. Both are manifestations of random variations in the phase of a signal. Timing jitter is the time domain characterization of this error. Phase noise is its frequency domain characterization. These random variations in the phase of the clock signal can limit the maximum speed of a high-speed data communications system, the bit error rate of a communications link and even the dynamic range of an A/D converter [8-10]. Phase noise in a typical frequency

synthesizer used by a wireless transceiver causes some down-conversion of the interfering signal into the same intermediate frequency (IF) as that of the desired signal. The resulting interference significantly degrades the dynamic range of the receiver. Therefore, improving the phase noise of the frequency synthesizer clearly improves the signal-to-noise-ratio (SNR) of the desired signal [11-14].

In many of communications applications timing jitter and phase noise are critical performance parameters and therefore important design considerations. Minimizing the timing jitter and phase noise in a PLL frequency synthesizer requires a careful analysis of circuit design blocks that make up the PLL and involves attention to the noise characteristics of the PLL system itself.

1.2 Basic Applications of Phase Locking

Modern communication systems often require the use of phase-locked-loops. A common requirement in modern communication systems is that the internal oscillator of the system must be forced to generate a signal that is phase coherent with the supplied reference signal. The reference signal may be generated within the system, or it may come from an external source. Phase locking in this manner is a common requirement in communication systems that synthesize and demodulate signals. In many of these applications, the signals are corrupted by noise. The noise makes difficult the process of generating a phase coherent local reference signal. Noise in the reference signal and circuit design blocks that make up the phase-locked loop may cause degradations in the performance of the system that uses signals generated by this phase-locked loop. Therefore, minimizing noise and developing low-noise techniques in phase-locked loops

are an active research area and the primary focus of many studies in phase-locked loop research.

Modern electronic applications that employ phase-locked loops include clock and data recovery, clock synchronization, clock synthesis that generate the system clock in sensitive applications, frequency synthesis which generate the local oscillator signals for the frequency translation in wireless transceivers, PLL modulator and demodulator applications, and phase-locked receivers.

In clock and data recovery applications, the PLL is used to generate a synchronized sampling signal from transitions in the incoming data stream [15-19]. Clock synchronization systems use a PLL to lock a local clock signal generated by a VCO, to an incoming clock signal that already exists. This method eliminates the skew between the data and clock signals, even when there are delay differences between two paths due to clock buffering and other factors [20-24]. In synchronous digital circuits such as high-speed microprocessor implementations, there is a clock signal that controls the operation of different logic blocks. For these applications, an internal clock is required at a higher frequency than the external reference. In this case the PLL clock synthesizer functions as a frequency synthesizer [25-32]. Other frequency synthesizer applications include RF transceivers where a number of closely spaced RF local oscillator frequencies need to be generated to select the desired incoming channel [14], [15]. A high frequency VCO can be locked to a low phase noise, low frequency crystal reference to obtain the desired RF frequency. The divide ratio in the feedback path of the PLL can be programmed to tune the output to the desired frequency [32]. Furthermore, the internal signals of a PLL may also be used for modulation, or demodulation in communication applications where the

signal information is contained in the phase or frequency of the signal itself [7], [33]. In digital communications employing modulation techniques such as BPSK, QPSK, and FSK, as well as analog communications using AM and FM techniques are integrated together with a PLL to modulate or demodulate the desired information [35-38]. Examples of these applications also include the coherent demodulation of the AM signals and radar receivers. In receiver applications requiring coherent demodulation, AM signals can be demodulated coherently by using a PLL. When the PLL is phase locked to carrier component of the AM signal, its VCO produces a sinusoid that is in phase quadrature with the received carrier. This method of AM demodulation can produce excellent results. In a noisy environment it can produce performance which far exceeds the classical envelope detector [37], [38].

There are several other applications such as radars used for moving target indication that require the reception of a Doppler-shifted signal. The amount of Doppler shift is often changing with time, and there can be a large amount of uncertainty in the frequency of the received signal. One possible solution to this problem is to use a noncoherent approach based on a wide bandwidth receiver that can capture the signal regardless of the Doppler shift. However, this approach may bear a significant noise penalty since the received noise power is proportional to receiver bandwidth. Large Doppler shifts would require large receiver bandwidths, and large bandwidths would lead to large amounts of received noise power and poor system performance. A phase-locked receiver is an excellent solution to the problem of receiving a Doppler-shifted signal. The receiver electronically tunes itself so that it tracks out Doppler shift on the received signal. Therefore, such a receiver can have a bandwidth that is comparable to that of the

signal, so no noise penalty has to be paid to accommodate the unknown carrier frequency of the signal [4], [38]. Examples of PLL based applications are summarized in Table 2.1.

Table 2.1 Application Areas of Phase-Locked Loops

1	Clock synthesis and synchronization • PLL clock generation for microprocessors, DSP, memory [20-27] • General purpose PLL clock generators [28-32]
2	Frequency synthesis • Local oscillator generation for wireless transceivers [14], [15]
3	Clock and data recovery circuits • Fiber optic data transceivers [39], [40] • Disk drive electronics [41] • Local area network transceivers [42-45] • DSL transceivers [46] • Serial link transceivers [67], [68]
4	Modulator and demodulators • Non-coherent modulator/demodulator in communications systems [34], [38], [47]
5	Phase-locked receivers • Radars [48] • Spacecrafts [49]

1.3 Non-Idealities in PLL Clock Synthesizers

Phase noise and spurious tones are two major non-idealities in PLL clock synthesizers. In this dissertation, the terms timing jitter and phase noise are used exclusively to refer to a

random variations in phase. For the systematic variations in phase the concept of spurious tones is used. The phase noise of the output signal in PLLs are the result of both phase noise on the input reference signal and by a number of intrinsic noise sources in the active and passive devices of circuit design blocks that make up the PLL. These noise sources may include thermal noise, 1/f flicker noise, supply and substrate noise, and switching noise of the power supply which may be a major noise source in some applications [20, 61, 62]. The supply and substrate noise generated by internal and external sources is highly data dependent and can have a wide range of frequency components that include low frequencies. Substrate noise tends not to have as large low frequency components as is possible for supply noise since no significant DC drops develop between the substrate and the supply voltages [50], [61], [62].

Systematic variations in the phase of the output of PLL due to interfering signals from various sources in the circuit can also cause timing errors. Interfering signals may be inadvertently coupled to a clock or oscillator signal through the power supply and substrate. In charge pump PLLs, the phase-frequency detector generates narrow identical pulses at both outputs UP and DN, which enable the sink and source current of the charge pump simultaneously. Since both currents are of equal amplitude and width, the net effect on the output voltage is zero. But several spikes occur on the output when currents are switched on and off. These spikes occur at reference frequency and modulate the VCO. This causes spurious tones in the output spectrum of the PLL at an offset from the carrier equal to the reference frequency. Other examples of interfering signals include unavoidable signals such as reference feed-trough in a PLL, which are inherent to the operation of the circuit. In the frequency domain, this type of interference results in

spurious modulation tones in the sidebands of the oscillator spectrum, referred to as spurious tones. In the time domain, modulation can cause an AC variation in the phase of a signal in addition to timing jitter [20].

The following two sections discuss a theoretical analysis of phase noise and timing jitter in frequency synthesizers. First, a phase noise model is developed. Second, an analysis of timing jitter is presented.

2.3.1 Phase Noise

The theoretical analysis of phase noise in modern frequency synthesizers is often the most challenging and crucial performance specification that must be met by a frequency synthesizer. It is also the specification that often proves the most difficult to model and simulate [12].

In this section, a review of basic phase noise concepts is presented, followed by a model that allows the designer to take noise data from individual circuit simulations and predict the overall phase noise performance of an entire PLL frequency synthesizer.

2.3.1.1 Phase Noise Concepts. Noise in PLL frequency synthesizers is contributed from all of the circuit blocks and components that make up the synthesizer. Synthesizer noise performance is usually described as phase noise, which is a measure of how much the output differs from an ideal impulse function in frequency domain. In many practical circuits, the effect of amplitude variations could be eliminated by processing the signal in a limiting stage but the effects of phase variations can not be eliminated. Since the output of the frequency synthesizer has fixed and limited amplitude we are primarily concerned

with noise that causes fluctuations in the phase of the output rather than noise that causes fluctuations in the amplitude. Therefore, the output of a synthesizer may be expressed as

$$V_{out}(t) = V_o \sin(\omega_o t + \phi_n(t)) \tag{2.1}$$

where $\omega_o t$ is the desired phase of the output and $\phi_n(t)$ is the time-variant random phase fluctuations of the output signal due to any noise sources in the PLL. Phase noise is often specified in units of dBc/Hz at a given offset, where dBc refers to the level in dB relative to the carrier.

The phase fluctuation term $\phi_n(t)$ in Equation (2.1) may be random phase noise or discrete spurious tones, also called spurs. The spurs are due to systematic variations in the phase of the output signal. Systematic variations occur as a result of non-ideal characteristics, such as current mismatch and unbalanced charge pump circuit causing charge injection to the loop filter [25], while the phase noise in an oscillator is mainly due to thermal noise, 1/f flicker noise, and power supply noise, which are random in nature. Assume the phase fluctuation is of a sinusoidal form as

$$\phi(t) = \phi_p \sin(\omega_m t) \tag{2.2}$$

where ϕ_p is the peak phase fluctuation and ω_m is the offset frequency from the carrier. Substituting Equation (2.2) into Equation (2.1) gives

$$V_{out}(t) = V_o \cos[\omega_c t + \phi_p \sin(\omega_m t)] \tag{2.3}$$

Expanding Equation (2.3) using trigonometric identities yield

$$V_{out}(t) = V_o[\cos(\omega_c t)\cos(\phi_p \sin(\omega_m t)) - \sin(\omega_c t)\sin(\phi_p \sin(\omega_m t))] \tag{2.4}$$

For a small phase fluctuation, the above equation can be simplified as

$$V_{out}(t) = V_o[\cos(\omega_c t) - \phi_p \sin(\omega_m t)\sin(\omega_c t)] \tag{2.5}$$

$$V_{out}(t) = V_o\left\{\cos(\omega_c t) - \frac{\phi_p}{2}\{\cos(\omega_c + \omega_m)t - \cos(\omega_c - \omega_m)t\}\right\} \tag{2.6}$$

In Equation (2.6) phase modulated signal includes the carrier signal tone and two symmetric sidebands at any offset frequency, $\pm\omega_m$, i.e., $\pm\Delta\omega$. A spectrum analyzer measures the phase noise power in dBm/Hz, but often phase noise is defined relative to the carrier power as

$$L\{\Delta\omega\} = \frac{P_{sideband}(\omega_0 + \Delta\omega, 1Hz)}{P_{carrier}(\omega_0)} \tag{2.7}$$

where $P_{sideband}(\omega_0 + \Delta\omega, 1Hz)$ represents the single sideband noise power at a frequency offset, $\Delta\omega$, from the carrier in a measurement bandwidth of 1-Hz as shown in Figure 2.1, and $P_{carrier}$ is the total power of the carrier at the frequency at which the synthesizer is operating.

Note that the definition in Equation (2.7) includes only the effect of phase fluctuations, $\phi_n(t)$ as described. The phase noise has the units of [rad^2/Hz] in the form as given in Equation (2.7). However, the phase noise units of dBc/Hz often makes more sense than this linear unit. It is also important to define the distinction between single-sideband and double-sideband phase noise. Single-sideband (SSB) phase noise is defined as the ratio of power in one phase modulation sideband per Hertz bandwidth, at an offset $\Delta\omega$ away from the carrier, to the total signal power.

The SSB phase noise power spectral density (PSD) to carrier ratio, in units [dBc/Hz], is defined as

$$L_{SSB}\{\Delta\omega\} = 10\log\left[\frac{P_{sideband}(\omega_0 + \Delta\omega, 1Hz)}{P_{carrier}(\omega_0)}\right] \tag{2.8}$$

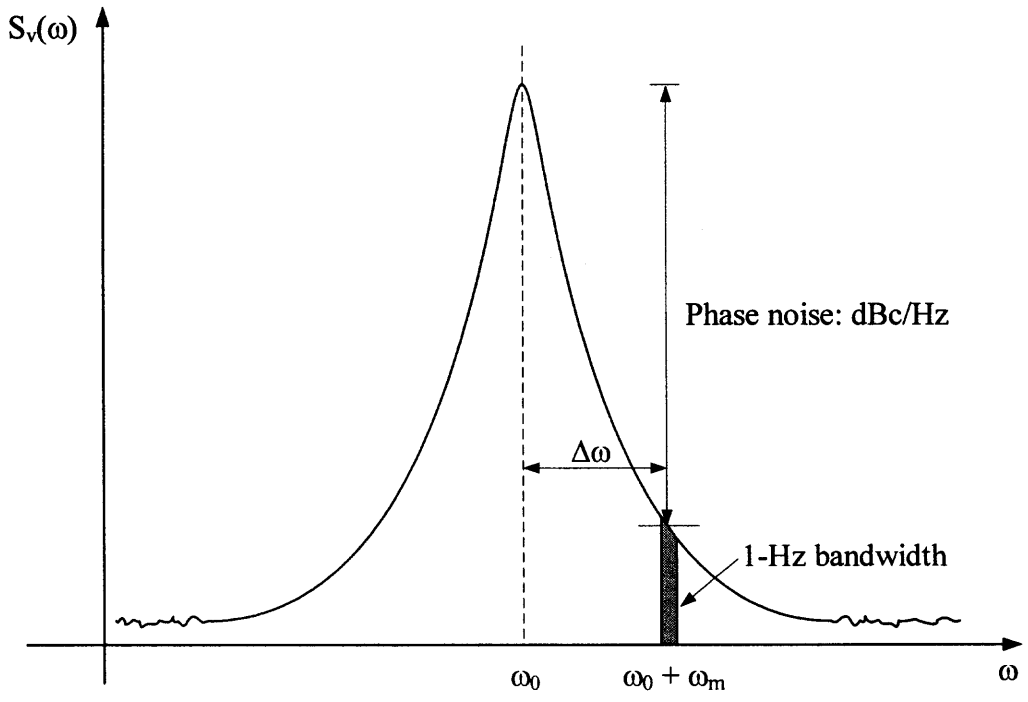


Figure 2.1 The phase noise per unit bandwidth.

Spectral density is usually specified at one or a few offset frequencies. Therefore, to be a meaningful parameter, both the noise density and the offset need to be specified, e.g., -120dBc/Hz at 1 MHz offset from the carrier.

If one plots $L_{SSB}\{\Delta\omega\}$ for a free-running oscillator as a function of $\Delta\omega$ on logarithmic scales, regions with different slopes may be observed as shown in Figure 2.2. There are regions in the sidebands where the phase can fall as $1/f^3$, $1/f^2$, and $1/f^o$ depending on the dominant noise process involved. As shown in Figure 2.2, at large offset frequencies there is a flat noise floor. At small offsets, one may identify regions with a slope of $1/f^2$ and$1/f^3$. The $1/f^2$ region is referred to as the "white frequency" variation region, since it is due to white noise, or uncorrelated fluctuations in the period of the oscillator [51], [52]. The behavior in this region is dominated by the thermal noise in the devices of oscillator circuit. For low enough offset frequencies from the carrier the

flicker noise of devices dominate other noise sources and the spectrum in this region falls as $1/f^3$ [8], [12].

Equation (2.5) can be combined with Equation (2.7) to obtain

$$L_{SSB}\{\Delta\omega\} = 10\log\left[\frac{\left(\frac{1}{2}\right)\left(V_{out}\phi_p/2\right)^2}{\left(\frac{1}{2}\right)V_{out}^2}\right] \tag{2.9}$$

$$L_{SSB}\{\Delta\omega\} = 10\log\left[\frac{\phi_p^2}{4}\right] = 10\log\left[\frac{\phi_{rms}^2}{2}\right] \tag{2.10}$$

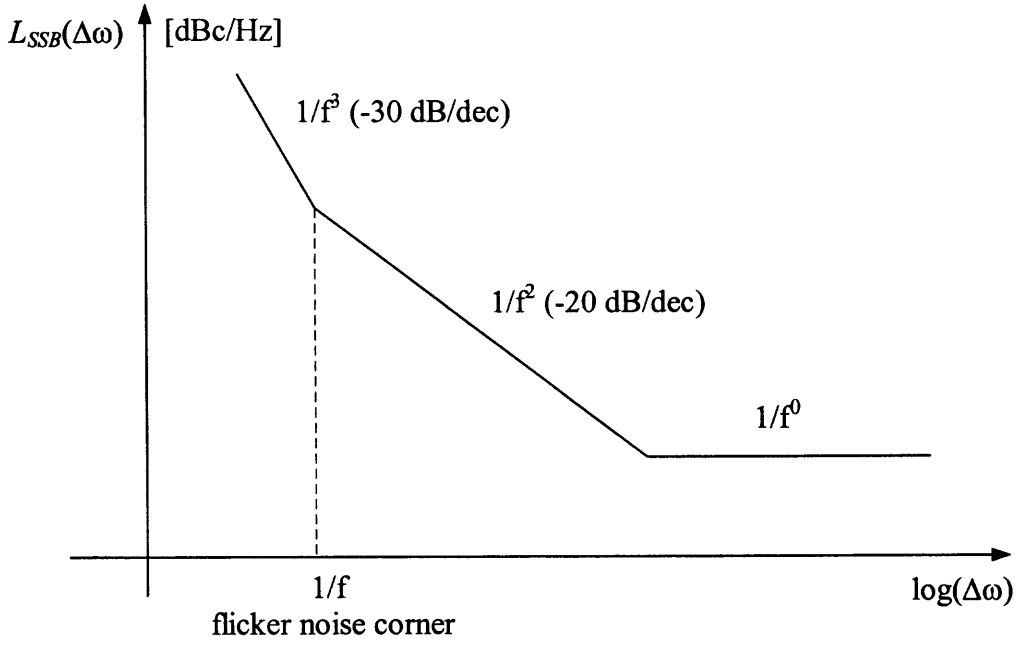


Figure 2.2 Power spectral density of phase fluctuations for a free-running oscillator.

where ϕ_{rms}^2 is the "rms" phase noise power density in units of [rad²/Hz]. Note that single-sideband phase noise is by far the most common type reported and often it is not

specified as SSB, but rather simply reported as phase noise. Alternatively double-sideband phase noise can be expressed by

$$L_{DSB}\{\Delta\omega\} = 10\log\left[\frac{P_{sideband}(\omega_0+\Delta\omega)+P_{sideband}(\omega_0-\Delta\omega)}{Pcarrier(\omega_0)}\right] \tag{2.11}$$

$$L_{DSB}\{\Delta\omega\} = 10\log\left[\phi_{rms}^2\right] \tag{2.12}$$

From either the single-sideband or double-sideband phase noise, the rms phase noise can be obtained in linear domain as

$$\phi_{rms}(\Delta\omega) = \frac{180}{\pi}\sqrt{10^{L_{DSB}(\Delta\omega)/10}} \tag{2.13}$$

$$\phi_{rms}(\Delta\omega) = \frac{180\sqrt{2}}{\pi}\sqrt{10^{L_{SSB}(\Delta\omega)/10}}\left[\text{deg}/\sqrt{Hz}\right] \tag{2.14}$$

It is also quite common to specify integrated phase noise over a certain bandwidth. The rms- integrated phase noise voltage of a synthesizer is given by

$$\sum PN_{rms} = \sqrt{\int_{\Delta\omega_1}^{\Delta\omega_2}\phi_{rms}^2(\omega)d\omega} \tag{2.15}$$

The limits of integration are usually the offsets corresponding to the lower and upper frequencies of the bandwidth of the information being transmitted.

In addition, it should be noted that dividing or multiplying a signal in the time domain correspondingly divides or multiplies the phase noise. Similarly, if a signal is translated in frequency by a factor of N, then the phase noise power is increased by a factor of N^2 as

$$\phi_{rms}^2(N\omega_0+\Delta\omega) = N^2\phi_{rms}^2(\omega_0+\Delta\omega) \tag{2.16}$$

$$\phi_{rms}^2\left(\frac{\omega_0}{N}+\Delta\omega\right)=\frac{\phi_{rms}^2(\omega_0+\Delta\omega)}{N^2} \tag{2.17}$$

Note that Equations (2.16) and (2.17) neglect noise introduced by the frequency translation. Otherwise, additional phase noise will be added. Also, note that the phase noise is scaled by N^2 rather than N because we are dealing with noise in units of power rather than units of voltage. For a divide ratio of $N=10$ this would be 20 dB. However, in applications such as clock synthesis, the input reference clock is usually derived from a crystal oscillator circuit having very low phase noise such as –150 dBc/Hz at offsets 10 kHz and above.

In practice, as described in [53-56], there are different methods of measuring phase noise and, depending on the particular method used to measure it, parts of the spectrum in Figure 2.2 may or may not be observed [12].

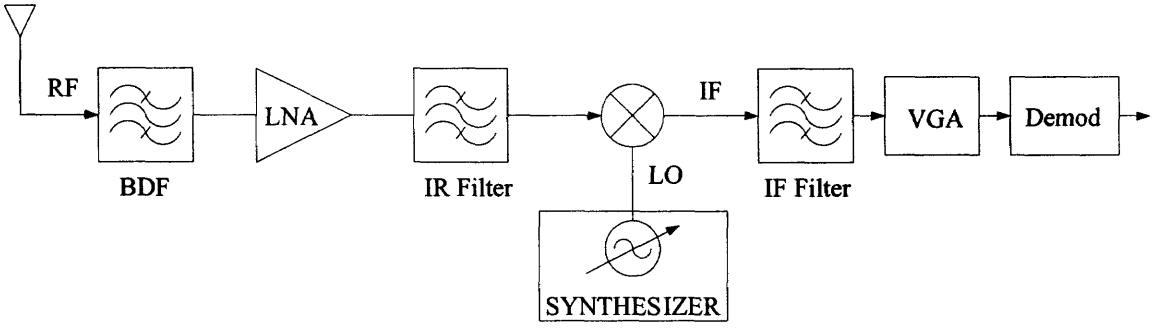


Figure 2.3 A superheterodyne radio receiver.

The destructive effect of phase noise can be seen in the front end of a superheterodyne radio reciver. As shown in Figure 2.3, a typical RF front-end consists of a low noise amplifier (LNA), a mixer, and a local oscillator (LO). Suppose the receiver tries to capture a weak desired signal in the presence of a strong signal (interference) in

an adjacent channel. If the LO has large phase noise, as shown in Figure 2.4, some downconversion of the interfering signal into the same intermediate frequency (IF) as that of the desired signal occurs as shown in Figure 2.4. Therefore, improving the phase noise of a frequency synthesizer clearly improves the signal-to-noise ratio (SNR) of the desired signal in a radio receiver.

Phase noise in the local oscillator of a receiver can cause some of the energy of interfering signals in adjacent channels to mix on top of the desired channel as indicated in Figure 2.4. This phenomenon is known as reciprocal mixing of the adjacent channels with the phase noise of LO. The particular example shown in Figure 2.4 can also be used to illustrate calculations of phase noise specification in a receiver. The phase noise requirement to achieve a desired SNR can be predicted using Equation (2.7) for a given interfering signal power. This prediction can be done by calculating the total inband noise power with respect to the carrier. The inband noise power relative to the carrier is calculated by integrating the phase noise spectrum over the band of interest. This relationship can be expressed by

$$P_{noise} = \int_{\Delta f_{\min}}^{\Delta f_{\max}} L\{\Delta f\} d(\Delta f) \tag{2.18}$$

where $\Delta f_{\min}$ and $\Delta f_{\max}$ are the offset frequencies from the center of the channel to the edges of the adjacent channel.

Assuming that the phase noise, $L\{\Delta f\}$, has $1/f^2$ slope between $\Delta f_{\min}$ and $\Delta f_{\max}$, i.e., $L(\Delta f) \cong K.\left(fo/\Delta f\right)^2$ Equation (2.18) reduces to

$$P_{noise} = L\left\{\sqrt{\Delta f_{\min}\Delta f_{\max}}\right\}.\left(\Delta f_{\max} - \Delta f_{\min}\right) \tag{2.19}$$

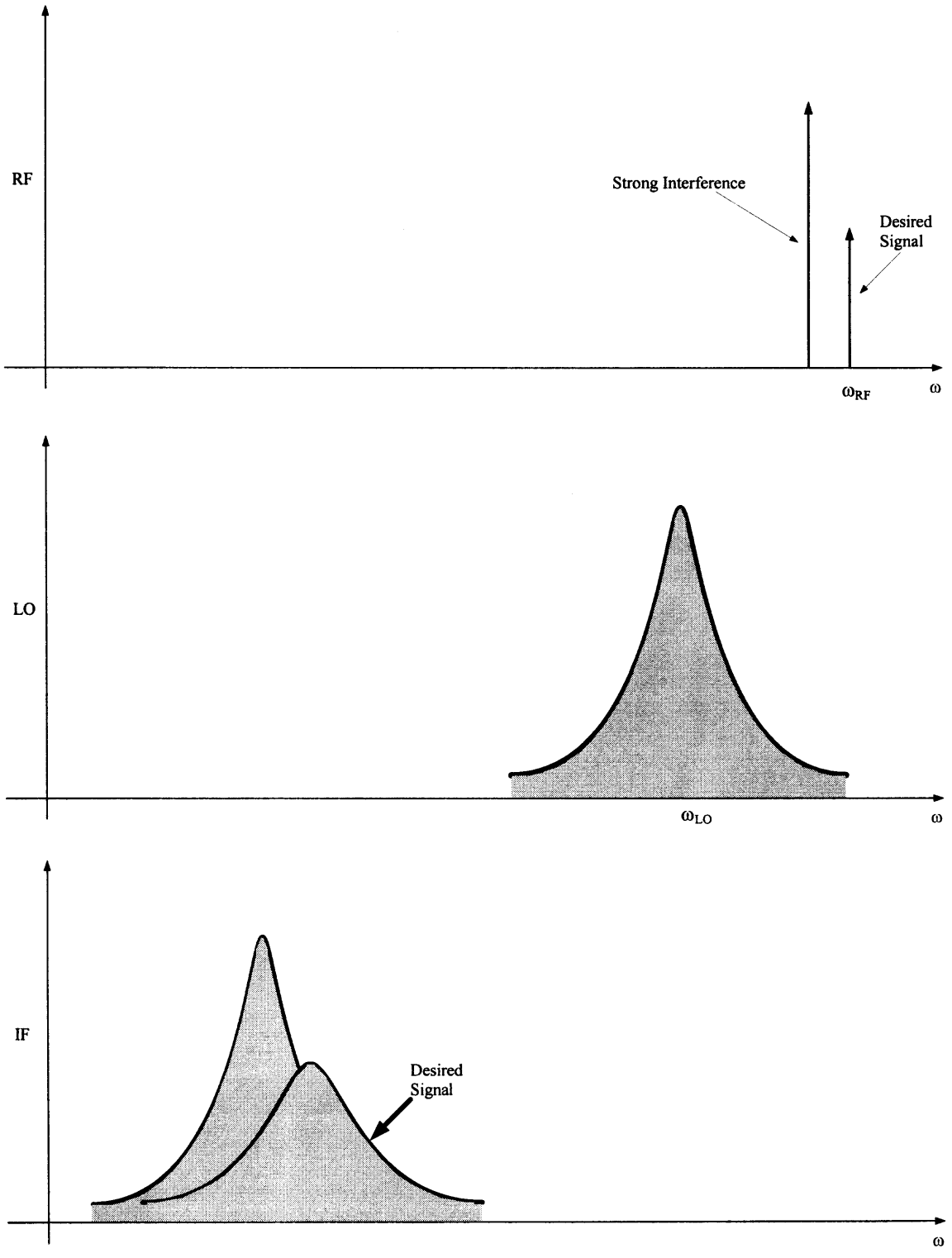


Figure 2.4 Effect of phase noise in presence of adjacent strong interferer.

The minimum SNR is given by

$$10\log(SNR_{\min}) = 10\log(P_{sig}) - 10\log(P_{\text{int}}) - 10\log(P_{noise}) \tag{2.20}$$

where P_{sig} and P_{int} are the desired and interfering signal powers, respectively.

In order to get an idea about the phase noise specifications required in modern wireless communications, several examples can be given to illustrate the calculation of phase noise requirement for the local oscillator of a receiver. Consider the example in Figure 2.4. Assume that the incoming signal spectrum in this example consists of a small desired signal at a power level of –75 dBm and the interfering signal in the adjacent channel with a power level of –60 dBm. If the SNR requirement is 15-dB at the output of the receiver and the adjacent signal power is at a level of –60 dBm (worst case) compared to the desired channel of power level of –75 dBm. The total phase noise energy allowable in the neighboring channel band is calculated from Equation (2.20) to be –30 dBc, i.e., -30 dB relative to the power of the carrier; 15 dBc for the SNR requirement and 15 dBc to cover the difference in incoming power levels. Assuming a channel spacing of 1.0 MHz in the particular wireless standard, this translates into a net power spectral density of –90 dBc/Hz, as illustrated in the following equation.

$$P = -30\frac{dBc}{1MHz} = -30 - 10\log(1.0\cdot 10^{6})\frac{dBc}{Hz} = -90\frac{dBc}{Hz} \tag{2.21}$$

For the second example, assume a channel spacing of 1 MHz, so that $\Delta f_{\min} = 100kHz$ and $\Delta f_{\max} = 1100kHz$. If an adjacent interfering signal is 40 dB stronger than the desired signal and the SNR requirement is 20 dB at the output of the receiver, the maximum allowable phase noise is calculated from Equation (2.20) to be –120 dBc/Hz at

a 330 kHz offset from the carrier. This specification is equivalent to a phase noise of –116 dBc/Hz at a 100 kHz offset.

The above calculations clearly indicate that very low levels of phase noise are required for the frequency synthesizer (LO) of a receiver, even though modest levels of SNR and required adjacent blocking channel power are permitted.

2.3.2 Timing Jitter

Uncertainties in transition instants of a periodic waveform that are responsible for phase noise can also be observed in time domain as timing jitter. The deviation of zero crossings of a waveform from their ideal position in time is called timing jitter. This is of great interest in high-speed communication systems such as optical communications because timing jitter represents the extent to which the zero crossings of a waveform are corrupted. There are more definitions of timing jitter. The deviation of each period from the ideal value can also be called timing jitter. These descriptions of jitter have subtle differences and therefore several definitions of timing jitter are given in the literature [61], [64].

As shown in Figure 2.5, the deviation of each transition point of $x_2(t)$ from its corresponding point in $x_1(t)$ can be measured to quantify the jitter. The waveform, $x_1(t)$ represents the ideal time base. This type of jitter is called "absolute jitter" because it is the result of comparison with an ideal time base, i.e., absolute points in time. Since the deviations shown in waveform $x_2(t)$ are random, a very large observation period is needed to determine the root mean square (rms) value of absolute jitter. The absolute jitter in a waveform is given by

$$\Delta T_{abs,rms} = \lim_{N\to\infty} \frac{1}{N} \sqrt{\Delta T_1^2 + \Delta T_2^2 + \cdots + \Delta T_N^2} \tag{2.22}$$

Referring to Figure 2.5 and using the transition points $\Delta T_1, \Delta T_2, ..., \Delta T_N$ of the waveform $x_2(t)$, another definition of timing jitter known as "cycle-to-cycle jitter" can be made. The cycle-to-cycle jitter is determined by measuring the difference between every two consecutive cycles of the waveform and taking the root mean square value as

$$\Delta T_{cycle-to-cycle,rms} \approx \lim_{N\to\infty} \frac{1}{N} \sqrt{(T_2 - T_1)^2 + (T_3 - T_2)^2 + \cdots + (T_N - T_{N-1})^2} \tag{2.23}$$

As mentioned above, absolute and cycle-to-cycle jitter are two most commonly used definitions of jitter to characterize the signals in time domain. Another type of jitter known as "period jitter" is also defined and proved useful when measuring signals in modern high frequency oscilloscopes [65], [66]. The period jitter is defined as the deviation of each cycle from the average period of waveform, $\overline{T}$, and is given by

$$\Delta T_{abs,rms} = \lim_{N\to\infty} \frac{1}{N} \sqrt{(\overline{T} - T_1)^2 + (\overline{T} - T_2)^2 + \cdots + (\overline{T} - T_N)^2} \tag{2.24}$$

Since phase noise and timing jitter are interrelated it is useful to establish a relationship between them. Modern measurement instruments and simulation tools can characterize or predict both quantities. However, it is often common practice to measure only one of these quantities in most of the applications. Therefore, use of several explicit formulae that convert one of these quantities into another may provide insight into the particular problem at hand. In PLL literature, several insightful expressions are already developed. These expressions have a lot of practical utility [51], [59], [60], [61], [64].

Several expressions are reiterated here to provide insight into the PLL clock synthesizer design.

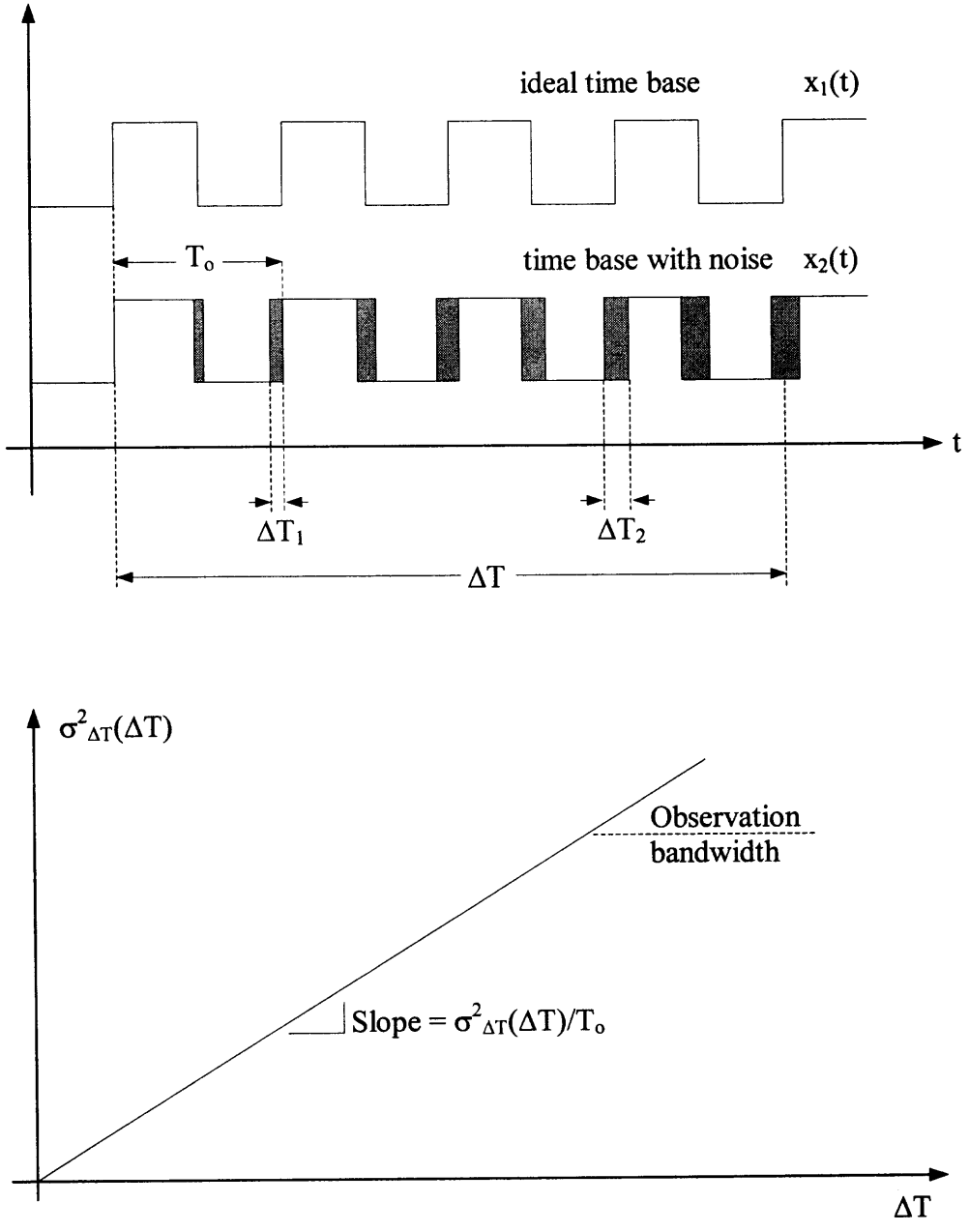


Figure 2.5 Clock jitter with measured variance versus delay time.

As formulated in Equation (2.23), the actual signal is compared with an ideal time base for the measurement of the absolute jitter. As indicated in Figure 2.5, the deviation

of each zero crossings is $\Delta T_j = (2\pi / T_o) \cdot \phi_{n,j}(t)$, where $\phi_{n,j}(t)$ denotes the value of random phase fluctuations in the vicinity of zero crossing number j [64]. The variance of absolute jitter can be defined as

$$\Delta T^2_{abs,rms} = \lim_{N\to\infty} \frac{1}{N} \sum_{j=1}^{N} \Delta T_j^2 \tag{2.24}$$

$$\Delta T^2_{abs,rms} = \left(\frac{2\pi}{T_o}\right)^2 \lim_{N\to\infty} \frac{1}{N} \sum_{j=1}^{N} \phi_{n,j}^2 \tag{2.25}$$

The summation term in Equation (2.25) can be approximated by an integral as

$$\Delta T^2_{abs,rms} = \left(\frac{2\pi}{T_o}\right)^2 \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} \phi_n^2(t) dt \tag{2.26}$$

The limit represents the average power of $\phi_n(t)$ and from Parceval's theorem [64], this term can be calculated as the area under the spectrum of $\phi_n(t)$ as

$$\Delta T^2_{abs,rms} = \left(\frac{2\pi}{T_o}\right)^2 \int_{-\infty}^{+\infty} S_{\phi n}(f) df = \omega_o^2 \sigma^2_{\Delta T} \tag{2.27}$$

The jitter variance $\sigma^2_{\Delta T}$ is different than the cycle-to-cycle jitter. This is the total error variance with respect to an ideal time base, as shown in Figure 2.5. This term represents the accumulated timing error from time zero to time ΔT. For a free running oscillator, a perturbation in the phase during one period of oscillation changes the starting point of the next. For uncorrelated Gaussian errors the jitter variance of the timing error increases with the measurement interval ΔT and grows linearly. The total timing error variance tends towards infinity for long enough time, but practical observation bandwidths limit the value to a finite number as indicated in Figure 2.5 [8], [12], [59].

As mentioned earlier, for "white frequency" variation region with $1/f^2$ phase noise sidebands shown in Figure 2.2, the Equation (2.26) predicts the linear ramp shown in Figure 2.5. For regions with other spectral shape, the total jitter variance exhibits a different shape. For PLL clock synthesizer applications the region of the phase noise spectrum influenced by $1/f$ noise of devices is not as important as other regions in phase noise spectrum [8].

As indicated in Figure 2.5, the timing jitter accumulation or growth in jitter variance $\sigma_{\Delta T}^2$ occurs because any uncertainty in an earlier transition affects all the following transitions, and its effect persists indefinitely. Therefore, the timing uncertainty when ΔT seconds have elapsed includes the accumulative effect of the uncertainties associated with transitions [12]. A typical measurement result of the standard deviation, $\sigma_{\Delta T}$ versus delay time ΔT exhibits regions with slopes of $1/2$ and 1 as shown in the logarithmic plot of Figure 2.6. In the region with the slope of $1/2$, the standard deviation of the jitter after ΔT seconds is

$$\sigma_{\Delta T(OL)} = \kappa\sqrt{\Delta T} \tag{2.28}$$

where κ is a time-domain figure of merit which depends on the VCO design.

Similarly, the standard deviation of the jitter in the region with slope of 1 may be expressed as

$$\sigma_{\Delta T(OL)} = \beta \cdot \Delta T \tag{2.29}$$

where β is another proportionality constant.

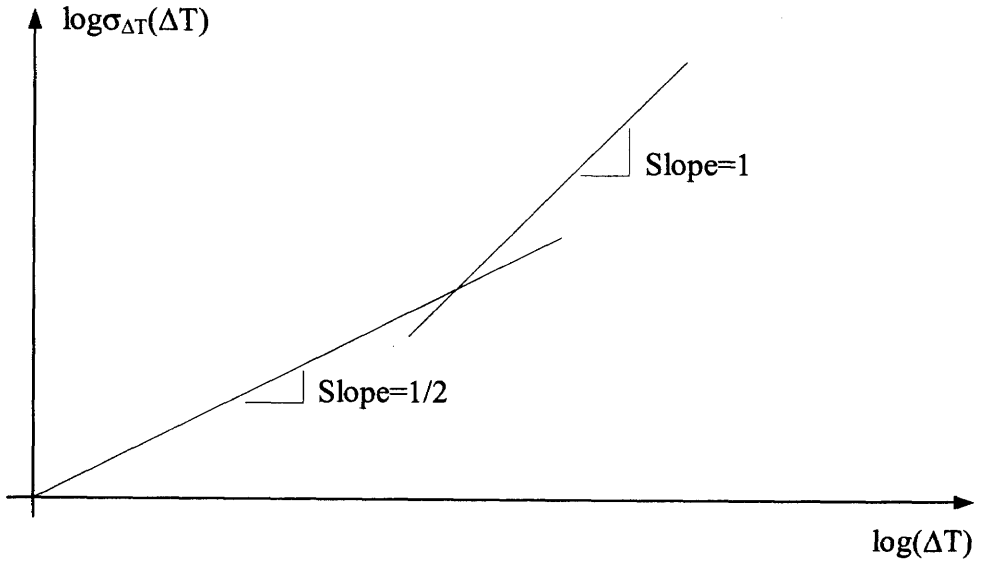


Figure 2.6 Root-mean-square (rms) jitter versus measurement time [12].

In most of high-speed communication applications, it is desirable for $\sigma_{\Delta T}$ to decrease at the same rate as the frequency increases to keep constant ratio of the rms timing jitter to the period. If this timing jitter is expressed in terms of the phase ($\Delta\phi = 2\pi\Delta T / T_o$), then the standard deviation of the phase error per cycle oscillation is given by

$$\sigma_{\Delta\phi} = \left(\frac{2\pi}{T_o}\right)\sigma_{\Delta T} = \omega_o \sigma_{\Delta T} \tag{2.30}$$

where T_o is the period of oscillation.

Equation (2.30) is also called "phase jitter" and is more useful measure in many applications. Phase jitter is defined as the standard deviation, $\sigma_{\Delta\phi}$, of the phase difference between the first cycle and m^{th} cycle of the clock. Several examples can be given using the definitions in Equations (2.28) and (2.29) to estimate the jitter for a required SNR in

data converters [12]. Consider applying a sinusoidal input voltage, $V_o \sin(\omega_o t)$, to the sample and hold circuit shown in Figure 2.7. If the sampling clock applied to a switch has timing jitter with a standard deviation of $\sigma_{\Delta T}$, the equivalent error in the sampled voltage, σ_V, is related to the timing jitter through the slope of the sinusoid as

$$\sigma_V = V_o \cos(\omega_o t)\sigma_{\Delta T} \tag{2.31}$$

In most applications, since there is no correlation between the sampling clock and the applied waveform, the SNR can be calculated by averaging the power of the error in Equation (2.31). Therefore, the relationship between the SNR and timing jitter can be given by [12]

$$SNR = \frac{V_o^2/2}{\sigma_{v,ave}^2} = \frac{V_o^2/2}{V_o^2\omega_o^2\sigma_{\Delta T}^2/2} = \frac{1}{\omega_o^2\sigma_{\Delta T}^2} \tag{2.32}$$

If an SNR of 40 dB is required at a sampling rate of 25 MHz, the rms-period jitter can be calculated using Equation (2.32) that it must be less than 63.5 ps.

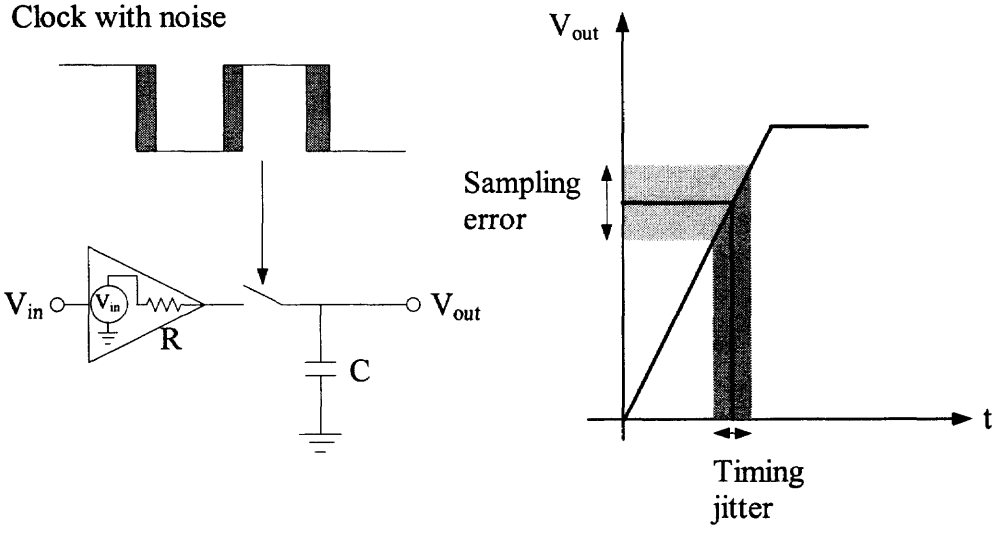


Figure 2.7 The effect of timing jitter sampling error in a sample-and-hold circuit.

CHAPTER 3

ANALYSIS AND MODELING OF CHARGE-PUMP PHASE-LOCKED LOOPS

3.1 Introduction to Phase-Locked Loops

A phase-locked loop is a closed-loop feedback control system that generates and outputs a signal in relation to the phase and frequency of an input reference signal. The general theory of the PLL is well established in literature. The literature base dealing with phase-locked loops is large and extensive [1], [3], [4], [5], [7], [33], [34], [71]. A typical PLL has the basic structure of the closed-loop system shown in Figure 3.1. Since each of the circuit design blocks shown in Figure 3.1 can be implemented in unique ways, there are a number of different types of PLLs. The charge-pump phase-locked loop (CPLL) architecture offers one of the most preferred PLL architecture for VLSI implementations in modern electronic systems because CPLLs are supposed to provide the simplest and most effective design platforms for monolithic implementations. Modern communication systems widely employ CPLLs to generate precision clock signals in a number of applications including wireless transceivers, serial link transceivers, microprocessors, and several other applications described in chapter two.

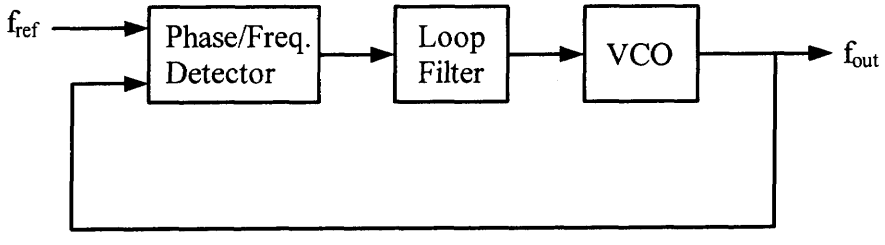


Figure 3.1 Phase-locked loop block diagram.

A typical CPLL architecture is shown in Figure 3.2. The major circuit design blocks of a basic CPLL generally consists of a phase-frequency detector (PFD), a charge-pump circuit (CP), a loop filter network (LF), and a voltage controlled oscillator (VCO). One of the main reasons for widely adopted use of the PFD/CPLL with a second-order loop filter (type-2 PLL) in modern communication systems is the error correction capability of the type-2 PLL which provides a zero static phase offset [88]. The PFD/ CPLLs in type-2 PLL configuration as shown in Figure 3.2 also provide flexible design tradeoffs by decoupling key design parameters such as the loop bandwidth, damping factor, and lock range. In PLL clock synthesizer applications, a divider is also used in the feedback path to multiply the input reference clock with this factor.

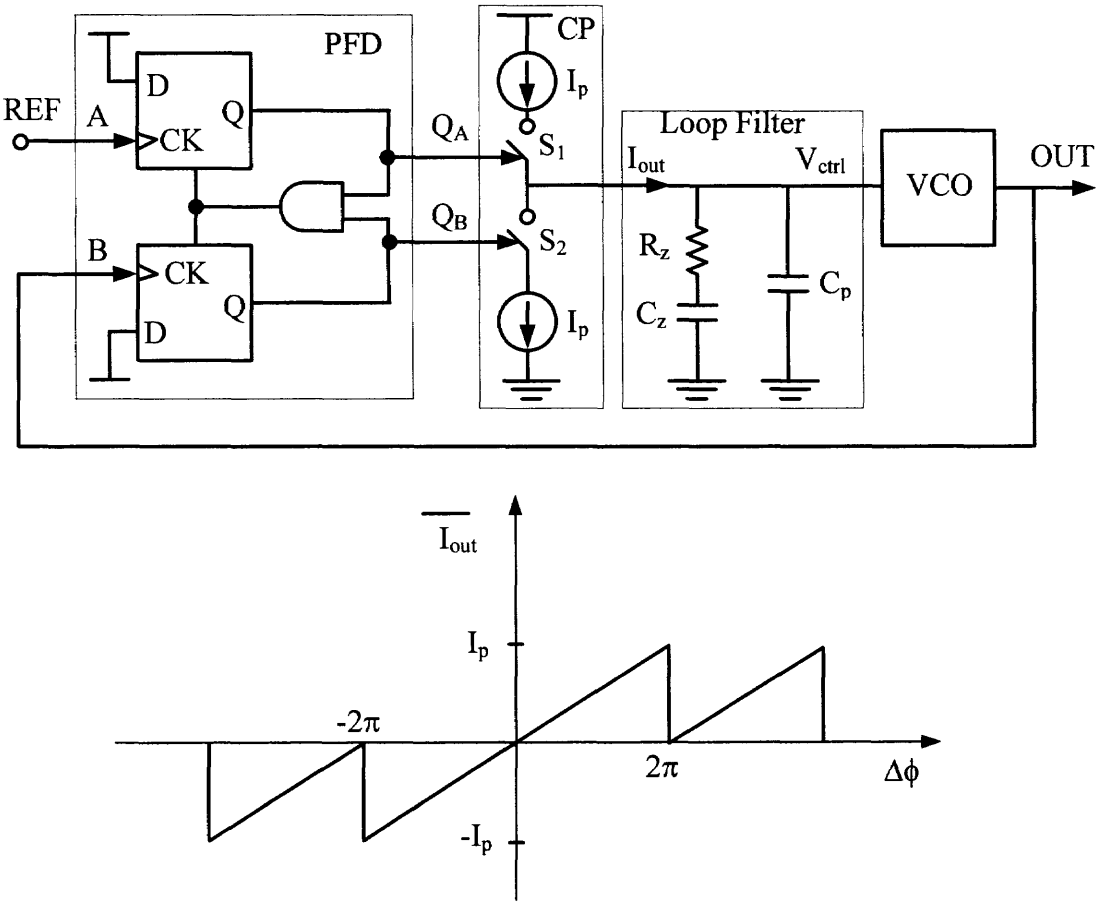


Figure 3.2 Third-order charge-pump PLL block diagram.

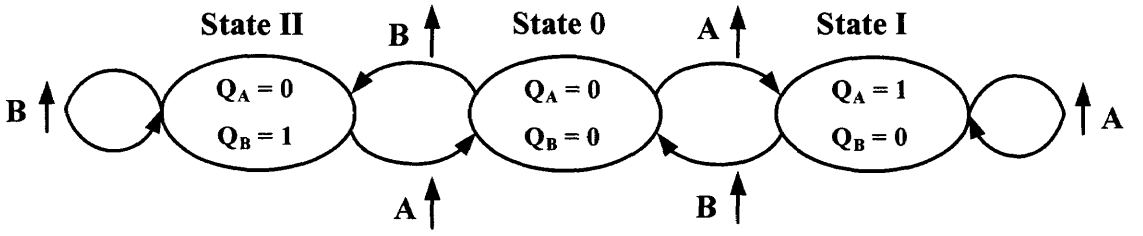


Figure 3.3 State diagram of phase-frequency detector.

The PFD is capable of comparing the phase of two signals and producing an output signal, which is a pair of digital pulses corresponding to the phase-frequency error between the input reference clock and the VCO output. The operation of the PFD can be explained by the use of the state diagram shown in Figure 3.3. The charge-pump circuit is conrolled by the digital pulses generated at the output of the PFD. The CP then converts the digital pulses into an analog current that is converted to a voltage using the passive loop filter network. The loop filter is a low pass filter used to filter the error signal coming form the phase detector and is designed to correctly compensate the feedback loop in the PLL. The resulting control voltage drives the VCO. The voltage-controlled oscillator produces an output frequency that is proportional to the control voltage at its input. The negative feedback loop forces the phase-frequency error to zero.

Due to sampled nature of the phase detector and the loop divider, the PLL cannot be treated as a continuous time system in its strictest sense. In addition, the loop components such as phase/frequency detector and VCO are not exactly linear. However, if the loop bandwidth is less than one-tenth of the reference input frequency then the loop components can be approximated by linear functions and the continuous time Laplace domain, i.e., s-domain representation can be used.

The continuous time approximation is not valid if the loop bandwidth approaches the input reference frequency. In that case, the discrete time or sampled nature of the loop should be taken into account in order to get accurate simulation results [73]. For this reason, the discrete time z-domain analyses should be employed to determine the loop dynamics of the PLL. The sampling also introduces stability problems that do not exist in continuous time networks. In addition, the sampling introduces inherent sampling delay which tends to decrease phase margins compared to continuous time analyzes. Sampling also causes aliasing of the noise at the offset of sampling frequency to the base band frequencies. For this reason, in monolithic implementations the loop bandwidth is usually constrained to less than one-tenth of the input reference frequency to maintain stability across process and temperature extremes. A discrete time model using the impulse invariant transformation was proposed by several authors [1], [72], [73], [88].

In this dissertation, an exact analysis for a third-order CPLL is presented. If the response of the components in a PLL is linearized, then for small perturbations in phase the small-signal AC model of the PLL shown in Figure 3.4 can be applied.

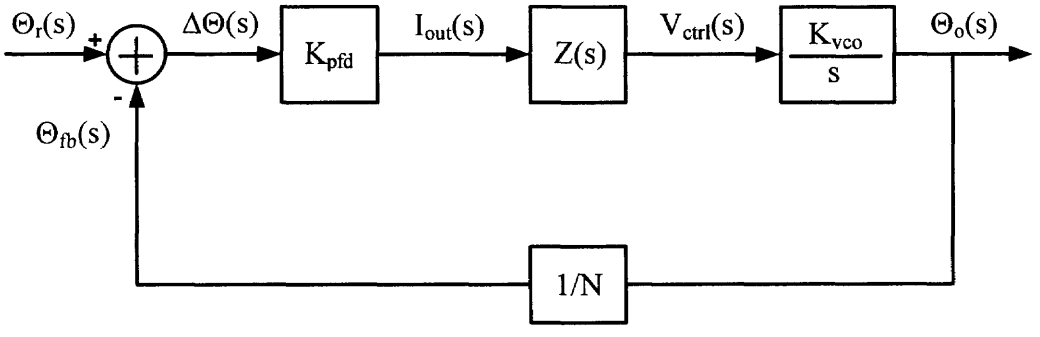


Figure 3.4 Steady-state phase domain model of CPLL.

3.2 Modeling the Linear CPLL

If the response of the circuit design blocks of the PLL is linearized for small perturbations in phase of the signal, the small-signal AC model of the PLL shown in Figure 3.4 can be applied. In this model, the phase of the output is compared to the input reference through the phase-frequency detector, and error signal proportional to the difference is produced. The constant of proportionality is the PFD gain, i.e., $I_p / 2\pi$, which is amps/radian for the CPLL applications. However, the error signal can also be a charge depending on the application. In this case, the forward gain of the loop is given by

$$G_{fwd}(s) = \frac{K_{pd} K_{vco} Z(s)}{s} \tag{3.1}$$

In this model, the VCO is an ideal integrator with gain of K_{vco}. The unit of K_{vco} is radian/volt. The open loop gain can be expressed as

$$G_{ol}(s) = \frac{K_{pd} K_{vco} Z(s)}{N \cdot s} = \frac{K_F}{N} \tag{3.2}$$

where K_F is the forward gain of the PLL and has units of radian/second. Putting all of these pieces together, a closed loop transfer function for a negative feedback loop is obtained

$$H(s) = \frac{\Theta_o(s)}{\Theta_r(s)} = \frac{G_{fwd}(s)}{1 + G_{ol}(s)} = \frac{K_{pd} K_{vco} Z(s)}{s + \dfrac{K_{pd} K_{vco} Z(s)}{N}} \tag{3.3}$$

The exact nature of the transfer function in Equation (3.3) is not definite until an expression for the loop filter is explicitly given. In the simplest form, Z(s) may be a constant factor, representing a gain or attenuation. In that case, the loop is a first-order system. More practical implementations employ a loop filter for Z(s), which adds another

pole to the system. The addition of that pole allows more flexibility in the design of the PLL and trade-offs in its performance parameters. To obtain a zero-stabilized, second-order loop, consider a loop filter function

$$Z(s) = R_z + \frac{1}{sC_z} = \frac{\tau_z s + 1}{sC_z} = K_{lf} \cdot \frac{\tau_z s + 1}{s} \tag{3.4}$$

where $K_{lf} = 1/C_z$.

The loop filter has a pole at the origin and a zero at a frequency $\omega_z = 1/\tau_z$, just below the unity gain of the PLL loop transmission. In this case, the closed loop transfer function can be defined as

$$H(s) = \frac{\Theta_o(s)}{\Theta_r(s)} = \frac{K_{pd}K_{vco}K_{lf}(\tau_z s + 1)}{s^2 + \frac{K_{pd}K_{vco}K_{lf}}{N}\tau_z s + \frac{K_{pd}K_{vco}K_{lf}}{N}} \tag{3.5}$$

The resulting CPLL in Equation (3.5) is of second-order and it can be expressed as

$$H(s) = \frac{\frac{I_p K_{vco}}{2\pi C_z}(R_z C_z s + 1)}{s^2 + \frac{I_p}{2\pi}\frac{K_{vco}}{N}R_z s + \frac{I_p}{2\pi C_z}\frac{K_{vco}}{N}} = N \cdot \frac{\omega_n^2(1 + \frac{s}{\omega_z})}{s^2 + 2\zeta\omega_n + \omega_n^2} \tag{3.6}$$

where the natural frequency ω_n and the damping factor, ζ are defined as

$$\omega_n = \sqrt{\frac{I_p K_{vco}}{2\pi C_z N}} \tag{3.7}$$

$$\zeta = R_z\sqrt{\frac{I_p C_z K_{vco}}{2\pi N}} = \frac{1}{2}\cdot\frac{\omega_n}{\omega_z} \tag{3.8}$$

Using Equation (3.8), the closed loop transfer function, $H(s)$, can be written in the following form:

$$H(s) = \frac{\Theta_o(s)}{\Theta_r(s)} = N \cdot \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{3.9}$$

The order of the system refers to the highest degree of the polynomial expression $1 + G_{ol} = 0 \cong C.E$, which is called the Characteristic Equation (C.E). The roots of the C.E in Equation (3.3) become the closed-loop poles of the overall transfer function $H(s)$. Substituting Equation (3.4) into Equation (3.2) yields

$$G_{ol}(s) = \frac{K_{pd} K_{vco} K_{lf} (\tau_z s + 1)}{s^2 N} \tag{3.10}$$

Since the open loop gain has two poles at the origin, this topology is called a type-2 PLL.

3.3 Stability of Type II PLL

Figure 3.5 illustrates the Bode plot of the open loop gain given in Equation (3.10). As shown in Figure 3.5, these plots suggests that if $I_p K_{vco}$ decreases, the gain crossover frequency moves toward the origin, degrading the phase margin. The degradation of the phase margin causes stability problems.

In addition to the frequency domain analysis of the magnitude and phase components of the transfer function, it is also possible to construct the root locus of the closed-loop system in the complex plane [6].

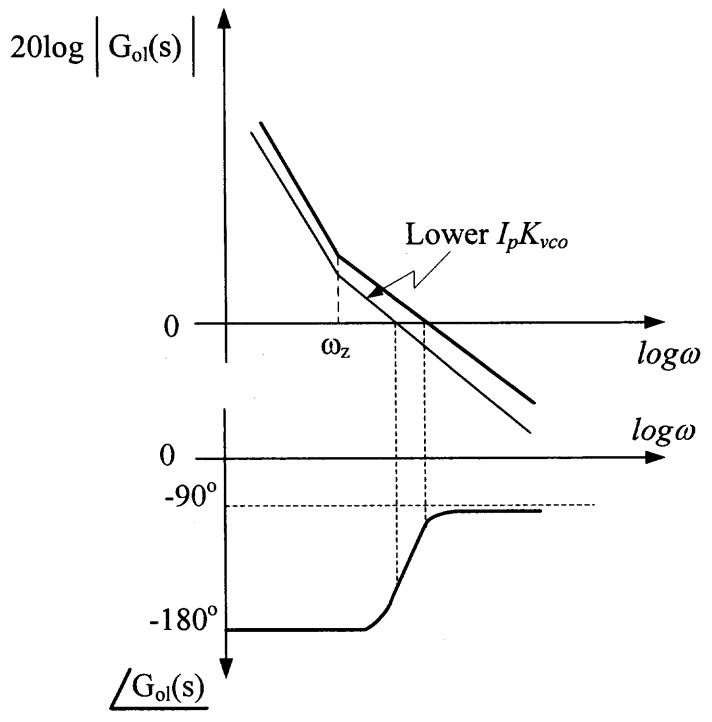


Figure 3.5 Stability degradation of CPLL.

For $I_pK_{vco}=0$, the loop is open and both poles lie at the origin (such condition exists when $I_p=0$. For $I_pK_{vco}>0$, we have, $s_{1,2}=-\zeta\omega_n\pm\omega_n\sqrt{\zeta^2-1}$, and since $\zeta\propto\sqrt{I_pK_{vco}}$, the poles are complex if I_pK_{vco} is small. The root locus of the type II PLL is shown in Figure 3.6. As I_pK_{vco} increases , s_1 and s_2 move on a circle centered at $\sigma=-1/(R_zC_z)$ with a radius $1/(R_zC_z)$ as shown in Figure 3.6. The poles return to the real axis at $\zeta=1$, assuming a value of $-2/(R_zC_z)$. For $\zeta>1$, the poles remain real, one approaching $-1/(R_zC_z)$ and the other going to $-\infty$ as $I_pK_{vco}\to\infty$. Since for complex s_1 and s_2, $\zeta=\cos\varphi$, as I_pK_{vco} exceeds zero, the PLL system becomes more stable [6].

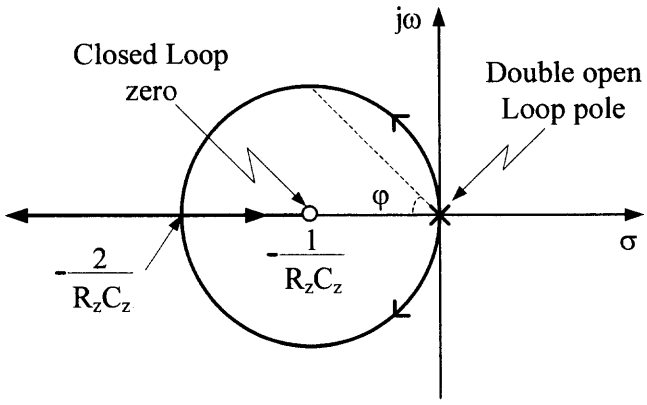


Figure 3.6 Root locus for a second-order PLL with a perfect integrator.

The type-2 PLL without a parallel capacitor, C_p suffers from a critical drawback. Since the charge pump drives the series combination of R_z and C_z, each time a current is injected into the loop filter, the control voltage experiences a large voltage jump. Even in the perfectly locked condition, the mismatches between I_{up} and I_{dn} and the charge injection and clock feed through of switches S_1 and S_2 introduce voltage jumps in V_{ctrl}. The resulting ripple severely disturbs the operation of the VCO, causing excessive jitter at the output of the VCO. A second capacitor in parallel with R_z and C_z combination is added to suppress the initial step. The passive loop filter is that of second order, yielding a third-order PLL and creating stability difficulties [88]. The capacitor C_p introduces a pole and therefore the phase degradation due to this pole has to be accounted for by a proper choice of the other loop parameters. As mentioned previously the second capacitor C_p is chosen much less than one-tenth of C_z in order not to cause a drastic change in the closed loop time and frequency responses of the second-order PLL. The dynamics of the third-order CPLL is discussed in the following section.

3.4 Third-Order CPLL

The three-state PFD creates UP and DN pulses depending on the phase difference between the positive edges of the reference and the VCO output. The CP converts the digital pulse to an analog control voltage through a passive loop filter. The loop filter consists of a resistor R_z in series with a capacitor C_z. The CP current source and the capacitor C_z form an integrator in the loop and the resistor introduces a stabilizing zero to improve the phase margin and therefore improve the transient response of the PLL. However, the resistor causes a ripple of value $I_p R_z$ on the control voltage at the beginning of each PFD pulse. At the end of the pulse, a ripple of equal value occurs in the opposite direction. This ripple has a modulation effect on the VCO output frequency and introduces excessive jitter in the output. A small capacitor C_p is included in parallel with R_z and C_z network as shown in Figure 3.2 to suppress the ripple induced jitter at the output of the VCO. The capacitor C_p introduces a pole in the transfer function of the passive loop filter, increasing the order of the system to three. In practice, the phase degradation due to this pole has to be accounted for by a proper choice of the other loop parameters.

In this dissertation, as explained in Section 1.1, the basic charge-pump model is created depending on assumptions of a small error meaning that the loop is linearized, and also the narrow bandwidth as compared to the input reference frequency. This approximation is called the continuous-time approximation [88]. Therefore, the selection of the loop components and parameters I_p, R_z, C_z, and C_p is determined by this approximation.

When the PLL is in near lock condition, a mathematical model for linear representation of the PLL behavior shown in Figure 3.7 can be used to predict the frequency and time domain characteristics of the CPLL. The gain of the PFD along with the CP can be shown to be $I_p / 2\pi$. The transfer function of the passive loop filter, $Z(s)$, can be derived using linear analysis. The PLL system is a type-2 third order charge-pump PLL. The type of the system refers to the number of poles at the origin for the open loop transfer function, $G_{ol}(s)$ as specified in Equation (3.2). The order of the system refers to the highest degree of the polynomial expression in the closed loop transfer function, $H(s)$.

From Figure 3.7(a), the forward transfer function as given in Equation (3.1) can be written as;

$$G_{fwd}(s) = \frac{I_p}{2\pi} \cdot Z(s) \cdot \frac{K_{vco}}{s} \tag{3.11}$$

where $I_p / 2\pi$ (amps/rad) is the gain of the PFD/CP and K_{vco} is the gain of the VCO.

The transfer function of the passive loop filter shown in Figure 3.7(b) is equal to

$$Z(s) = \frac{V_{ctrl}}{I_{out}} = \frac{sC_zR_z + 1}{s^2C_zC_pR_z + s(C_z + C_p)} = \frac{1 + s\tau_z}{s(C_z + C_p) \cdot [1 + s\tau_p]} \tag{3.12}$$

Two time constants can be defined for the transfer function of the filter

$$\tau_z = R_zC_z = \frac{1}{\omega_z} \tag{3.13}$$

$$\tau_p = R_z \cdot \frac{C_zC_p}{C_z + C_p} = \frac{1}{\omega_{p3}} \tag{3.14}$$

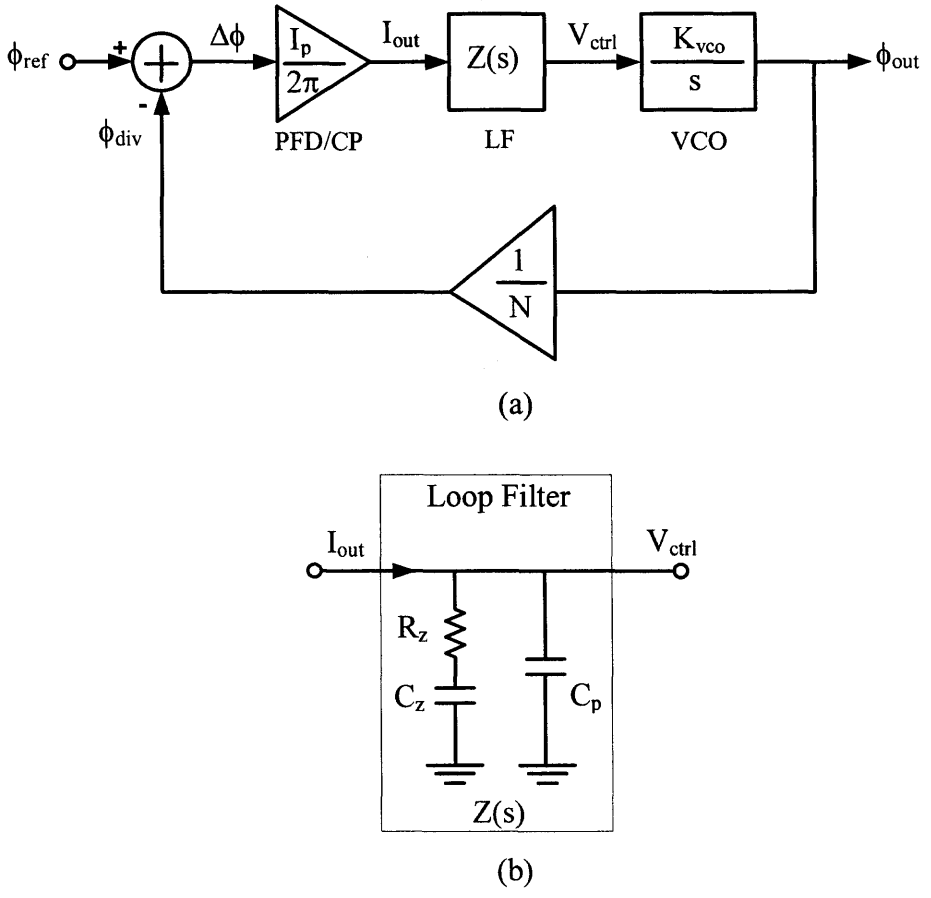


Figure 3.7 (a) Steady-state linear model for third-order CPLL (b) passive loop filter.

The open loop transfer function is written from Equation (3.2)

$$G_{ol}(s) = \frac{Ip}{2\pi} \cdot Z(s) \cdot \frac{K_{vco}}{s} \cdot \frac{1}{N} \tag{3.15}$$

Substituting Equation (3.13) into Equation (3.15) yields

$$G_{ol}(s) = \frac{I_p \cdot K_{vco}}{2\pi \cdot N} \cdot \frac{(1+s\tau_z)}{s^2(C_z + C_p)(1+s\tau_p)} \tag{3.16}$$

where the unit of K_{vco} is radian/volt.

Equation (3.16) can be expressed in terms of poles and zeros of the open loop transfer function as

$$G_{ol}(s) = \frac{I_p \cdot K_{vco}}{2\pi \cdot N} \cdot \frac{1}{s^2(C_z + C_p)} \cdot \frac{(1+\frac{s}{\omega_z})}{(1+\frac{s}{\omega_{p3}})} \tag{3.17}$$

where ω_z and ω_{p3} are given by

$$\omega_z = \frac{1}{R_z C_z} \tag{3.18}$$

$$\omega_{p3} = \frac{1}{R_z \cdot \left(\frac{C_z C_p}{C_z + C_p} \right)} \tag{3.19}$$

The crossover frequency ω_c, equals approximately

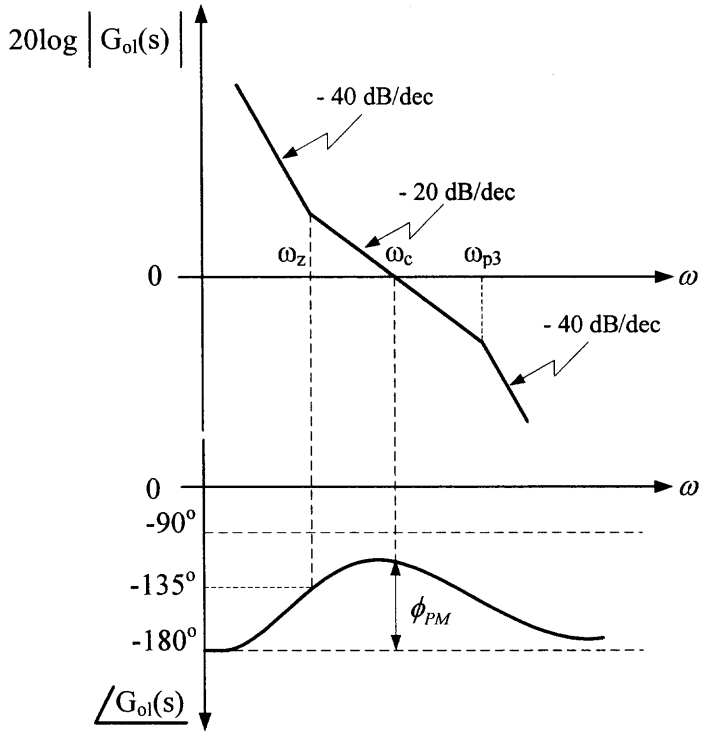
$$\omega_c = \frac{I_p}{2\pi} \cdot \frac{1}{N} \cdot K_{vco} \cdot R_z \cdot \frac{C_z}{C_z + C_p} \approx \frac{I_p}{2\pi} \cdot \frac{1}{N} \cdot K_{vco} \cdot R_z \tag{3.20}$$

The open loop frequency response, $G_{ol}(s)$, is used to determine the loop filter parameters by ensuring the loop stability [74, 75]. The loop has a zero and three poles. The Bode plot is shown in Figure 3.8. The phase margin degradation due to the third pole ω_{p3} is mathematically expressed by

$$\phi_{PM} = \tan^{-1}\left(\frac{\omega_c}{\omega_z} \right) - \tan^{-1}\left(\frac{\omega_c}{\omega_{p3}} \right) \tag{3.21}$$

A careful analysis of the Bode plot in Figure 3.8 reveals a relatively flat portion of the phase plot where the phase lag due to the third pole nearly cancels the phase lead introduced by the zero. Using Equation (3.21) and by choosing $\omega_z = \omega_c / 4$ and $\omega_{p3} = 4\omega_c$

yields a phase margin, $\phi_{PM} = \tan^{-1}(\omega_c / \omega_c / 4) - \tan^{-1}(\omega_c / 4\omega_c) \approx 60^o$, which is the typical design goal in most of the monolithic implementations.



$$\phi_p = \tan^{-1}\left(\frac{\omega_c}{\omega_z}\right) - \tan^{-1}\left(\frac{\omega_c}{\omega_{p3}}\right)$$

$$\omega_{p3} = \frac{1}{R_z \cdot \left(\frac{C_z C_p}{C_z + C_p}\right)} \simeq \frac{1}{R_z C_p}$$

$$\omega_z = \frac{1}{R_z C_z}$$

$$\omega_c = \frac{I_p}{2\pi} \cdot \frac{1}{N} \cdot K_{vco} \cdot R_z$$

Figure 3.8 Bode plot of third-order loop gain.

The goal in IC design is to maintain stability over process and temperature corners while having an optimal closed loop bandwidth. There is no direct trade off between ζ and ω_n in charge-pump PLL architecture as seen in Equations (3.7), (3.8), and (3.18). In addition, an optimal choice of the capacitor ratio C_z / C_p leads to a phase margin that is relatively immune to process variation [72]. The maximum phase margin can be obtained by taking the derivative of the phase margin, ϕ_{PM}, in Equation (3.21) and equating it to zero. The maximum phase margin occurs when

$$\omega_c = \omega_z \cdot \left(\sqrt{\frac{C_z}{C_p} + 1} \right) \tag{3.22}$$

Substituting Equation (3.22) into the phase margin expression given in Equation (3.21) yields

$$\phi_{PM_{\max}} = \tan^{-1} \cdot \left(\sqrt{\frac{C_z}{C_p} + 1} \right) - \tan^{-1} \cdot \left(\frac{1}{\sqrt{\frac{C_z}{C_p} + 1}} \right) \tag{3.23}$$

$$C_z = 2C_p \left(\tan^2 \phi_{PM} + \tan \phi_{PM} \sqrt{\tan^2 \phi_{PM} + 1} \right) \tag{3.24}$$

With a robust phase margin such as $\phi_{PM} \approx 60^o$, Equation (3.24) can be used to define the ratio between two capacitors of the passive loop filter.

Substituting Equations (3.11) and (3.17) into Equation (3.3), the closed loop transfer function of the third order CPLL can be expressed in the following form

$$H(s) = \frac{K_{pd} K_{vco} K_Z \omega_{p3} \left(1 + \frac{s}{\omega_z} \right)}{s^3 + \frac{\omega_{p3}}{N} s^2 + \frac{K_{pd} K_{vco} K_Z \omega_{p3}}{N \omega_z} s + \frac{K_{pd} K_{vco} K_Z \omega_{p3}}{N}} \tag{3.25}$$

where $K_Z = 1/(C_z + C_p)$.

The zero and third pole of the loop, ω_z and ω_{p3}, are given in Equation (3.18) and Equation (3.19), respectively. The common practice when designing a third-order CPLL is to initially neglect C_p, and design for a second-order system to meet the desired specifications. A small capacitance C_p is then added. The value of C_p can be calculated

using either Equation (3.24) and the specified ϕ_{PM}, or it can be chosen 20 times smaller than C_z to obtain a reasonable phase margin.

3.5 Transient Characteristics of CPLL

The derivations of the previous sections were based on the steady-state operation of the PLL, i.e., the PLL is near lock condition, in which a constant reference frequency is applied and the division modulus is fixed. However, the operation of the PLL must also incorporate the dynamic behavior of the loop at startup and when the division modulus or the input reference frequency is changed. The dynamic behavior of a CPLL at startup and when programming the loop divider ratio, is an important performance parameter. The objective of the analysis of the dynamic behavior is to study the time-domain response of the PLL. Assuming the loop is initially locked, the PLL behaves as a feedback system, which compares excess phase of the VCO output with the input reference phase. As shown in Figures 3.2 and 3.4, the PFD and CP circuits function as an error amplifier that compares two phases. However, the dimension of the signals change throughout the PLL from phase to current through the PFD and CP, from current to voltage through the LF, and from voltage to phase through the VCO.

For the sake of simplicity, the second order loop with the transfer function given in Equation (3.9) is used for the time domain analysis. In order to analyze $H(s)$, a relationship between the input and output frequencies is handy to use. The instantaneous frequency of a waveform is equal to the time derivative of the phase $\omega = d\phi / dt$. Since the frequency and the phase are related by a linear operator, the transfer function given by Equation (3.9) applies to variations in the input and output frequencies:

$$\frac{\omega_{out}(s)}{\omega_{in}(s)} = N \cdot \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{3.26}$$

This result predicts that if ω_{in} changes very slowly $(s \to 0)$, then ω_{out} tracks ω_{in}, because the loop is assumed locked. Equation (3.26) also indicates that if ω_{in} changes abruptly but the system is given enough time to settle $(s \to 0)$, then the change in ω_{out} equals that in $N \cdot \omega_{in}$. This observation aids the analysis of the PLL when performing transient analysis. It is also helpful to visualize the transient response of the PLL in terms of frequency quantities rather than phase quantities.

As indicated in the linear model of Figure 3.4, the phase of the output is compared to the input through the PFD. Then an error signal I_{out} proportional to the difference is produced. The constant of proportionality is the PFD gain, which is amps/radian for the CPLL applications

$$I_{out}(s) = K_{pfd}\left(\Theta_r(s) - \Theta_{fb}(s)\right) = \frac{I_p}{2\pi}\Delta\Theta \tag{3.27}$$

The error signal is applied to the loop filter with the transfer function $Z(s)$ given in Equation (3.12), and used to drive VCO. The VCO output frequency is given by an equation as

$$f_{out} = f_c + K_{vco} \cdot V_{ctrl} \tag{3.28}$$

where f_c is the free running frequency of the VCO with a control voltage of zero.

The output phase is the integral of frequency over time. Assuming that the loop has first attained lock between the input and the output, then the small signal phase at the output is given in the s-domain by

$$\Theta_o(s) = \frac{K_{vco}}{s} \cdot V_{ctrl}(s) \tag{3.29}$$

The factor $1/s$ is due to the integration. As it is obvious in Figure 3.4, a change in ω_{out} must be accompanied by a change in V_{ctrl}. Using the Equation (3.31) and considering the Laplace transform of the phase $\omega_{in} = d\Theta_r / dt$, the closed loop response can be expressed by

$$H(s) = \frac{\Theta_o(s)}{\Theta_r(s)} = K_{vco} \cdot \frac{V_{ctrl}}{\omega_{in}}(s) \tag{3.30}$$

Equation (3.30) indicates that monitoring the response of V_{ctrl} to ω_{in} yields the response of the closed loop system. The second-order transfer function of Equation (3.9) suggests that the step response of the system can be overdamped, critically damped, or underdamped. The analysis of the denominator, $s^2 + 2\zeta\omega_n s + \omega_n^2$, reveals that the system has two poles given by

$$s_{1,2} = -\zeta\omega_n \pm \omega_n\sqrt{\zeta^2 - 1} = \left(\zeta \pm \sqrt{\zeta^2 - 1}\right)\omega_n \tag{3.31}$$

Therefore, if $\zeta > 1$, both poles are real, the system is overdamped, and the transient response involves two exponentials with time constants $1/s_1$ and $1/s_2$. In the case of $\zeta < 1$, the poles are complex and the response to an input frequency step $\omega_{in} = \Delta\omega u(t)$ is equal to

$$\omega_{out}(t) = \left\{1 - e^{-\zeta\omega_n t}\left[\cos(\omega_n\sqrt{1-\zeta^2}\,t) + \frac{\zeta}{\sqrt{1-\zeta^2}}\sin(\omega_n\sqrt{1-\zeta^2}\,t)\right]\right\} \cdot \Delta\omega \cdot u(t) \tag{3.37}$$

$$\omega_{out}(t) = \left[1 - \frac{1}{\sqrt{1-\zeta^2}} e^{-\zeta\omega_n t}\sin(\omega_n\sqrt{1-\zeta^2}\,t + \theta)\right]\Delta\omega \cdot u(t) \tag{3.32}$$

where ω_{out} denotes the change in the output frequency and $\theta = \sin^{-1}\sqrt{1-\zeta^2}$.

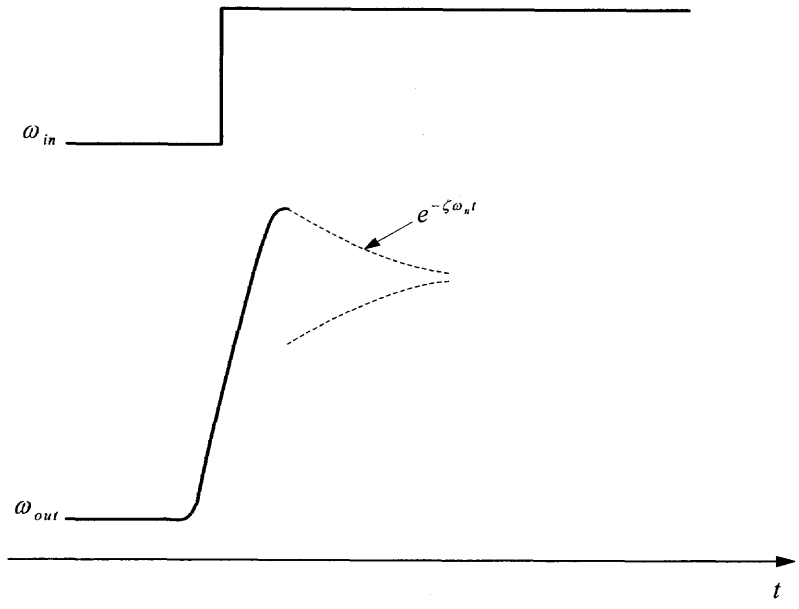


Figure 3.9 Response of PLL to an input frequency step.

Thus, as shown in Figure 3.9, the step response contains a sinusoidal component with frequency $\omega_n\sqrt{1-\zeta^2}$ that decays with a time constant $(\zeta\omega_n)^{-1}$. It is obvious from Equation (3.30) that the PLL exhibits the same response if a phase step is applied to the input and the output phase is monitored.

The settling speed or lock time of PLLs is of great concern in most applications. Equation (3.32) indicates that the exponential decay time determines how fast the output approaches its final value, implying that $\zeta\omega_n$ must be maximized. As shown in the linear model of Figure 3.7, even if the PLL is locked to the correct frequency there is still a small phase error, $\phi_{err}(t) = \phi_{ref}(t) - \phi_{div}(t)$. The design task is to find how long it takes for

the VCO output frequency to settle within a given frequency error. As indicated in Figure 3.9, in order to find the response of the PLL to a phase step, the closed loop transfer function given in Equation (3.9) is multiplied by a step function, and the inverse Laplace transform is taken to convert the response to a time domain function as given by Equations (3.31) and (3.32). The lock time follows readily from these two equations by taking the natural logarithm of Equation (3.32) and may be given by

$$t_{lock\_time} = \frac{-1}{\zeta\omega_n} \ln\left(\frac{f_{accuracy}}{f_2 - f_1} \sqrt{1-\zeta^2} \right) \tag{3.33}$$

where $f_{accuracy}$ is the specified accuracy of the PLL output frequency, f_1 and f_2 are two programmable frequencies of a PLL clock synthesizer in which the VCO output switches from the frequency f_1 to frequency f_2 by changing the N counter of the loop divider [76], [77].

Equation (3.33) predicts the settling or lock time for a second-order system. However, as discussed in Section 3.4, PLL clock synthesizers are never a system of second-order. Instead, a typical CPLL is a third-order system. Therefore, additional poles in the transfer function as indicated in Equations (3.25) are considered. A design methodology will be given in the next chapter.

3.5.1 Tracking Behavior of the PLL

In order to analyze the tracking characteristics of the CPLL, the phase error function $\phi_{err}(t) = \phi_{ref}(t) - \phi_{div}(t)$ that results from a specified input phase $\phi_{ref}(t)$ is evaluated. As shown in Figure 3.7, assuming the loop is initially locked, and the phase error is sufficiently small to justify the assumption of linearity.

The steady state phase error $\phi_{err,ss}$, which is the value of the phase error ϕ_{err} after transients have died away, may be calculated by means of the final value theorem of the Laplace transform as in the following:

$$\lim_{t\to\infty}\phi(t)=\lim_{s\to 0}s\phi(s) \tag{3.34}$$

There are two cases for the analysis of the dynamic characteristics of the loop. In the first case, assuming that the input reference has a phase step of magnitude $\Delta\phi$, the steady-state phase error for a first-order loop (specified in Equation (3.2)) may be expressed as

$$\phi_{err,ss}=\lim_{s\to 0}\left[s\cdot\phi_{ref}(s)\cdot\frac{1}{1+G_{ol}(s)}\right]=\lim_{s\to 0}\left[s\cdot\frac{\Delta\phi}{s}\cdot\frac{1}{1+\frac{K_F}{sN}}\right]=0 \tag{3.35}$$

In practice, the situation of switching from one frequency to another occurs when the division modulus in the clock synthesizer is abruptly changed to program a new output frequency. The forward gain of the PLL must be selected as high as possible to make the phase error $\phi_{err,ss}$ small.

As indicated in above discussion, the open loop gain expression given by Equation (3.2) is useful for determining phase disturbances at the output of the system in response to phase perturbations at the input. In addition to analyzing the steady-state behavior of the system, it is also important to determine the transient phase error caused by particular inputs. These inputs are commonly encountered inputs in PLL clock synthesizers. One of the most encountered situations in clock synthesis applications is the programmable change of the feedback division modulus to create a new output frequency. This situation is equivalent to a frequency step of magnitude $\Delta\omega$. In addition

to the transient analysis presented previously in this section, the transient behavior of the loop can also be analyzed using the phase error function $\phi_{err,ss}$ and considering a first-order loop as specified in the following equation:

$$\phi_{err}(s) = \frac{1}{1+G_{ol}(s)} \cdot \phi_{ref}(s) = \frac{s}{s+\omega_c} \cdot \frac{\Delta\omega}{s^2} = \frac{\Delta\omega}{s(s+\omega_c)} \tag{3.36}$$

Taking the inverse Laplace transform of Equation (3.36) yields

$$\phi_{err}(t) = \frac{\Delta\omega}{\omega_c}(1-e^{-\omega_c t}) \tag{3.37}$$

Equation (3.37) states that the final frequency is created after an exponential settling with a time constant $\tau_c = 1/\omega_c$. Using the time domain phase error function given in Equation (3.37) and by taking the natural logarithm of that equation, the settling time or lock time of the loop can be calculated as

$$t_{lock\_time} = \frac{-\ln \varepsilon}{\omega_c} \tag{3.38}$$

where $\varepsilon = f_{accuracy}/(f_2 - f_1)$ is the frequency accuracy term, which determines how the loop settles to a new frequency with a specified accuracy, e.g., 0.1%.

In a typical PLL clock synthesis application, assuming that the VCO output frequency is switched from 50 MHz to 150 MHz (this is equivalent to a frequency step of 100 MHz) with a specified frequency accuracy of 100 Hz, if the loop bandwidth is 180 KHz , the lock time (settling time) is calculated using Equation (3.38) to be 10.2 μs.

3.5.2 Acquisition

In the previous section, it is assumed exclusively that the loop is already in lock and therefore operates linearly. However, the loop starts with an unlocked condition during the power-up sequence, and must be brought into lock. This task may be accomplished by either the natural actions of loop or with the help of auxiliary circuits. The process of bringing a loop into lock is called acquisition. If the loop acquires lock by itself, the locking process is called self-acquisition and if it is assisted by auxiliary circuits, the process is called aided acquisition [1].

The transition of the loop from unlocked to locked condition is inherently a nonlinear process because the phase detector senses unequal frequencies at its inputs. Modern PLLs incorporate frequency detection in addition to the phase detection. This technique is called "aided acquisition" and performed by employing a phase and frequency detector. The idea is to compare ω_{in} and ω_{out} by means of a frequency detector, generate a DC component proportional to the frequency difference $\omega_{in} - \omega_{out}$, and apply this result to the VCO in a negative feedback loop. At the beginning, the frequency detector drives ω_{out} toward ω_{in} while phase detector remains idle. When $|\omega_{in} - \omega_{out}|$ is sufficiently small, the phase detector takes over, acquiring lock. The phase and frequency detection scheme increases the acquisition range to the tuning range of the VCO [3], [6].

3.6 Analysis of Phase Noise in PLLs

Every circuit design block of the PLL generates noise. A linear model of CPLL with noise sources is shown in Figure 3.10. Two main noise sources are that of the VCO, modeled by $\Theta_{vco,n}$, and the noise from the reference signal, $\Theta_{r,n}$. The noise of the phase

detector, frequency dividers, charge-pump, and loop filter can all be represented by $\Theta_{r,n}$. Therefore, these noise sources can be classified as the noise injected from the input reference signal and noise generated internally in the circuit design blocks. When used in a phase-locked loop system, the phase noise of a VCO is shaped by the action of the loop. In open loop applications, a free running VCO phase noise is simply called oscillator phase noise, while the phase noise of a VCO inside a phase-locked loop is called PLL output phase noise because the phase noise of the VCO is changed by the noise-shaping characteristic of the PLL. In addition to the noise introduced from the VCO, the reference signal has its own phase noise spectrum and the output phase noise of the PLL depends on this contribution as well. However, in PLL clock synthesizer applications, the input reference clock is often generated using a high-Q factor crystal resonator and has a very low phase noise characteristic. Therefore, the phase noise of the input reference clock doesn't contribute to the overall phase noise of the PLL.

The block diagram of a typical charge-pump PLL clock synthesizer suitable for monolithic implementations was shown in Figure 3.2 along with the corresponding steady state, linear phase domain model shown in Figure 3.4.

The first-order closed loop transfer function given in Equation (3.3), $H(s) = (K_{pd}K_{vco}Z(s))/(s + K_{pd}K_{vco}Z(s)/N)$ has a low pass nature. It determines how the noise injected from the input reference and phase detector is handled by the loop.

For the analysis of phase noise, the magnitude square of the first-order closed loop transfer function is calculated from Equation (3.3) as

$$H(s)=\frac{\Theta_o(s)}{\Theta_r(s)}=\frac{G_{fwd}(s)}{1+G_{ol}(s)}=\frac{K_{pd}K_{vco}Z(s)}{s+\frac{K_{pd}K_{vco}Z(s)}{N}} \tag{3.39a}$$

$$|H(s)|^2=\frac{\Theta_o(s)}{\Theta_r(s)}=\left|\frac{K_{pd}K_{vco}Z(s)}{s+\frac{K_{pd}K_{vco}Z(s)}{N}}\right|^2=\frac{N^2}{\left|1+\frac{sN}{K_{pd}K_{vco}Z(s)}\right|^2} \tag{3.39b}$$

Equation (3.39) states that the reference noise power is multiplied by N^2 within the loop bandwidth and shaped by the closed loop response of the PLL.

Figure 3.10(b) is used for deriving the effect of the input reference noise. Similarly, Figure 3.10(c) displays a model used for evaluating the effect of the VCO noise. The noise of the reference signal, phase detector, charge pump, loop filter, and feedback divider can all be represented by $\Theta_{r,n}$. The noise transfer functions from $\Theta_{r,n}$ to Θ_{out} and $\Theta_{vco,n}$ to Θ_{out} can be expressed as

$$H_1(s)=\frac{\Theta_{out}(s)}{\Theta_{r,n}(s)}=\frac{G_{fwd}(s)}{1+G_{ol}(s)}=\frac{N\cdot K_{pd}\cdot Z(s)\cdot K_{vco}}{N\cdot s+K_{pd}\cdot Z(s)\cdot K_{vco}} \tag{3.40}$$

$$H_2(s)=\frac{\Theta_{out}(s)}{\Theta_{vco,n}(s)}=\frac{1}{1+G_{ol}(s)}=\frac{N\cdot s}{N\cdot s+K_{pd}\cdot Z(s)\cdot K_{vco}} \tag{3.41}$$

Assuming initially that the loop filter has a constant transfer function, i.e., $Z(s)=K_{lf}$. The open loop transfer function then becomes

$$G_{ol}(s)=\frac{K_{pd}\cdot Z(s)\cdot K_{vco}}{N\cdot s}=\frac{K_{pd}\cdot K_{lf}\cdot K_{vco}}{N\cdot s}=\frac{K_F}{N\cdot s} \tag{3.42}$$

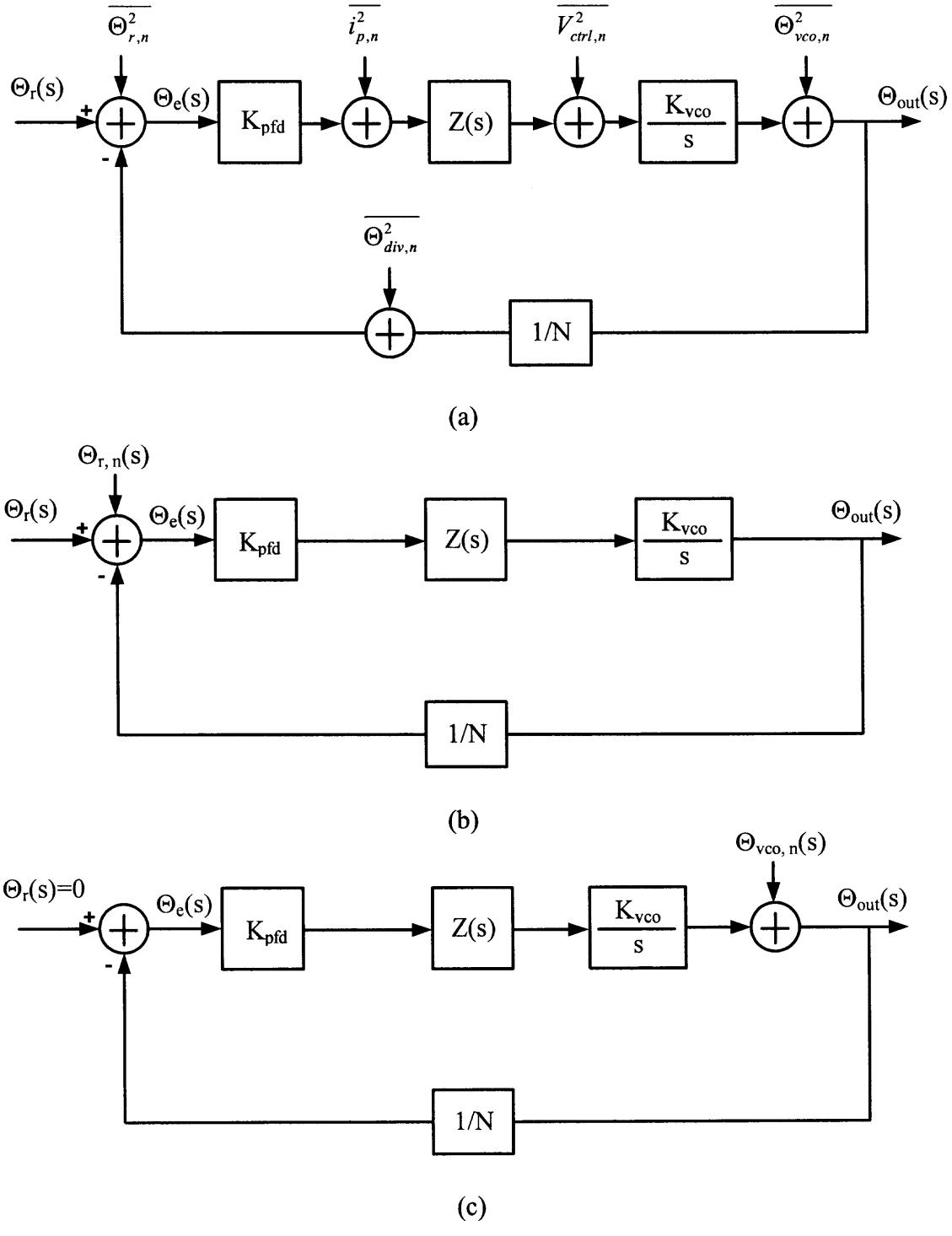


Figure 3.10 PLL noise model: (a) noise sources (b) reference noise (c) VCO noise.

Equations (3.40) and (3.41) are then simplified as

$$H_1(s) = \frac{\Theta_{out}(s)}{\Theta_{r,n}(s)} = \frac{G_{fwd}}{1+G_{ol}} = \frac{\frac{K_F}{N}}{1+\frac{K_F}{N \cdot s}} = N\frac{\omega_c}{s+\omega_c} \tag{3.43}$$

$$H_2(s) = \frac{\Theta_{out}(s)}{\Theta_{vco,n}(s)} = \frac{1}{1+G_{ol}} = \frac{1}{1+\frac{K_F}{N \cdot s}} = \frac{s}{s+\omega_c} \tag{3.44}$$

where ω_c is the crossover frequency of the open loop transfer function G_{ol} and given by

$$\omega_c = \frac{K_F}{N} \tag{3.45}$$

Equation (3.45) indicates that the noise from the reference signal has a low pass function with a 3-dB cutoff frequency ω_c. At low frequencies the transfer function becomes

$$H_1(s) = N\frac{\omega_c}{\omega_c \cdot (s/\omega_c + 1)} \approx N \tag{3.46}$$

This low frequency noise amplification is expected from the frequency multiplication of the PLL. However, at high frequencies $\Theta_{r,n}$ is attenuated and the attenuation increases by $20\log(n-m)$ dB/dec of the frequency, where n is the order of the loop and m is the order of $Z(s)$ [14].

The noise transfer function from VCO to the output has a high pass function. Noise at high frequencies passes without attenuation, i.e., $\Theta_{out}(s)/\Theta_{vco,n}(s) \approx 1$ because the feedback action of the loop is too slow to suppress the noise components. At low

frequencies there is a first order roll-off, as the loop feedback becomes stronger with smaller frequencies. The 3-dB cutoff frequency of the high pass function is also ω_c. Based on this first-order analysis, it can be stated that the PLL noise is dominated by reference noise at low frequencies and by VCO noise at higher frequencies. The noise of the feedback frequency divider, phase/frequency detector, and charge pump are simply added to the reference noise and usually negligible in a careful design as will be shown in Chapter 4. However, loop filter noise has to be taken into account especially when the VCO gain K_{vco} is large. The only source of noise in the loop filter of a third-order PLL is the series resistor R_z. The equivalent voltage noise of R_z and is given by definition

$$\overline{V_{n1}^2} = 4 \cdot k \cdot T \cdot R_z \cdot \Delta f \tag{3.47}$$

Referring to Figure 3.10(a), the transfer function from V_{n1} to the output is defined as

$$\frac{\Theta_{out}(s)}{V_{n1}(s)} = \frac{sC_z}{R_z C_z s + 1} \cdot \frac{\Theta_{out}(s)}{\Theta_{r,n}(s)} \tag{3.48}$$

Because of the additional zero in Equation (3.48) compared to Equation (3.43) the output noise due to the thermal resistor R_z, initially increases with frequency and then starts decreasing. Therefore, it is critical to make sure that the thermal noise of the resistor R_z does not contribute too much to noise peaking at low frequencies while maintaining low noise at higher frequencies.

Although above analysis considering a first-order loop is useful to understand the noise response of the PLL, it is instructive to derive the noise transfer functions for a second and third order CPLL. The noise transfer function of a second order CPLL, i.e.,

the CPLL with a first-order loop filter, can be defined the same as in Equation (3.6). Therefore, it is given by

$$H_1(s) = \frac{\Theta_{out}(s)}{\Theta_{r,n}(s)} = N \cdot \frac{\omega_n^2(1 + s/\omega_z)}{s^2 + 2\zeta\omega_n + \omega_n^2} \tag{3.49}$$

Similarly, for a second order CPLL, the noise transfer function from $\Theta_{vco,n}$ to Θ_{out} can be expressed as

$$H_2(s) = \frac{\Theta_{out}(s)}{\Theta_{vco,n}(s)} = \frac{s^2}{s^2 + 2\zeta\omega_n + \omega_n^2} \tag{3.50}$$

Figure 3.11 shows the response of the PLL to reference noise sources and the VCO noise. The total output phase noise for a PLL can be expressed in terms of the phase noise of the reference and the VCO. The noise transfer functions $H_1(s)$ and $H_2(s)$ are used to obtain

$$S_{out}(\omega) = S_{ref}(\omega) \cdot |H_1(\omega)|^2 + S_{vco}(\omega) \cdot |H_2(\omega)|^2 \tag{3.51}$$

As stated above the VCO is in the forward path of the feedback loop for its errors but only for frequencies within the bandwidth of the PLL. The transfer function $H_2(\omega)$ has a low pass characteristic. Therefore, the low frequency phase noise of the VCO is suppressed by the loop as shown in Figure 3.11(b), but high frequency phase noise passes directly to the output.

The transfer characteristic from input of the PLL to the output $H_1(\omega)$ has a low pass characteristic as shown in Figure 3.13(a). Therefore, the PLL rejects high frequency phase noise in the input reference but allows low frequency noise to pass.

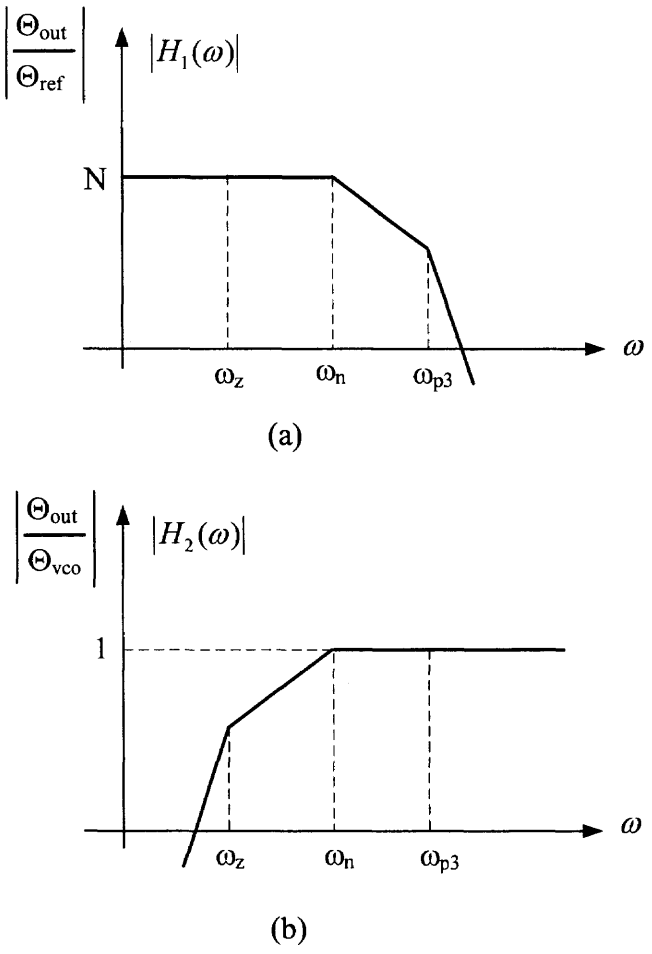


Figure 3.11 Noise transfer functions (a) for reference noise (b) for VCO noise.

The filter corner frequency for both H_1 and H_2 depend on the loop bandwidth ω_n of the PLL. Therefore, the choice of the PLL loop bandwidth involves a direct trade-off between the noise of the VCO and the reference. The loop bandwidth must be chosen carefully to obtain an optimum phase noise performance at the output of the PLL.

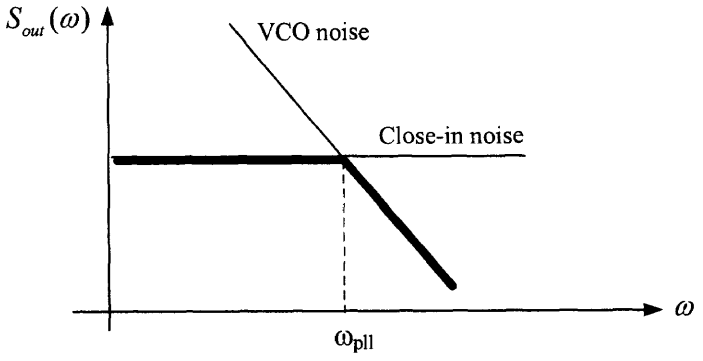
Programmable dividers are the integral parts of the PLL clock synthesizers. With a divide by N in the feedback path, the output frequency is equal to N times the reference frequency. For applications without a divider, N is effectively one. When considering applications with a frequency divider, the noise injected from the reference is

multiplied by an additional factor of N^2 as indicated in Equation 3.65), when referred to the output. For a divide ratio of $N=2$, this would be $20\log 2 \approx 6-dB$ and $N=10$, it is $20-dB$. However, in PLL clock synthesizer applications the reference is often derived from a low noise crystal oscillator circuit. The phase noise of such a reference oscillator is much lower than the VCO phase noise. Therefore, the output phase noise of the PLL is dominantly determined by the VCO phase noise.

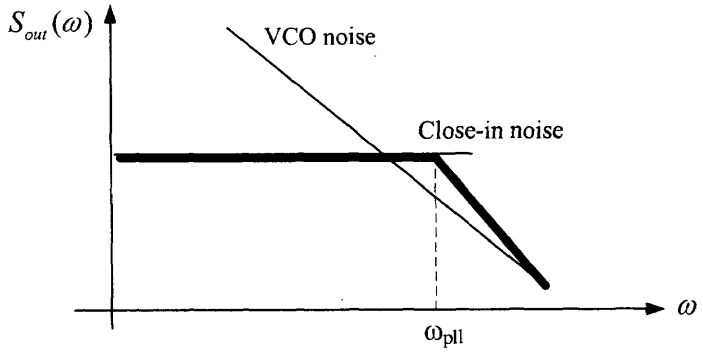
The choice of PLL loop bandwidth determines the shape of the PLL output noise. For a minimum residual phase error at the PLL output, the PLL loop bandwidth is chosen at the intersection of close-in noise and VCO noise as shown in Figure 3.12(a) [76], [78]. If the PLL loop bandwidth is not chosen properly as indicated in Figure 3.12(b) and (c), a performance degradation due to phase noise occurs at the output of the PLL.

The SSB phase noise specification of a PLL clock synthesizer is depicted in Figure 3.13. There are three dominant phase noise regions in Figure 3.13. The first region is due to the phase noise of the input reference signal. The second region is mostly contributed by PFD, charge-pump circuit, and divider circuits. The third region has a peak at ω_{pll} and is practically due to the VCO noise.

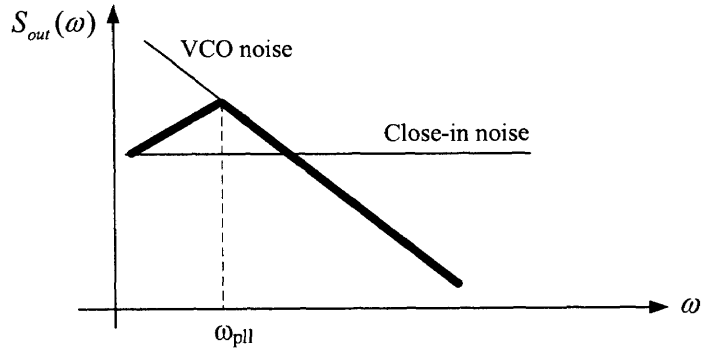
Using the models and analytical expressions introduced in this section, a phase noise optimization procedure for the PLL can be developed. First of all, the phase noise of the closed loop in-band components; the charge pump circuit, PFD, and passive loop filter must be reduced. In addition, the ring-oscillator based VCOs tend to introduce excessive close-in phase noise if not optimized. Secondly, the divider ratio N of the feedback divider is minimized. Finally the magnitude of the charge pump current I_p is increased while minimizing the gain K_{vco} of the VCO.



(a)



(b)



(c)

Figure 3.12 Selection of PLL loop bandwidth (a) optimum (b) too large (c) too narrow.

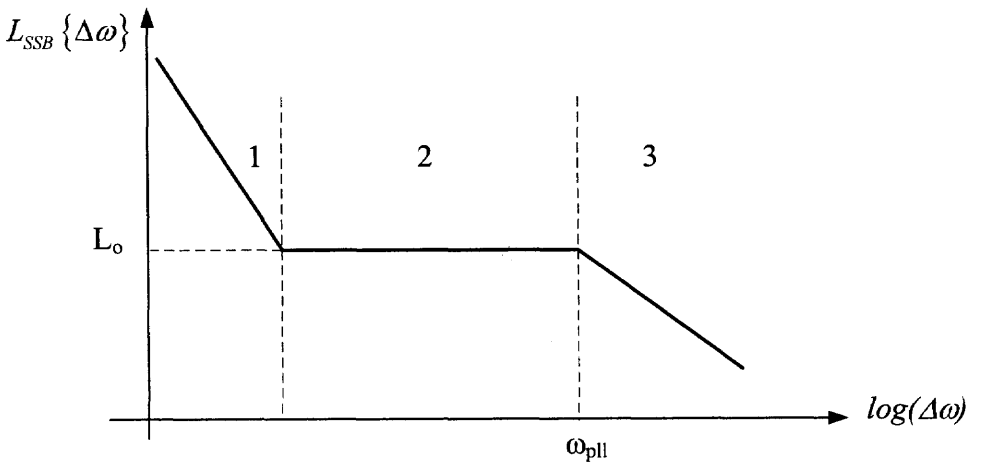


Figure 3.13 Phase noise specification of PLL clock synthesizer.

3.7 Analysis of Timing Jitter in PLLs

A detailed description of phase noise and timing jitter was given in Chapter 2. An approximate relationship between the phase noise and the cycle-to-cycle jitter of a free-running VCO is given by the following equation [61]

$$\Delta T_{cc} \approx \frac{4\pi}{\omega_o^3} S_\phi(\Delta\omega)\Delta\omega^2 \tag{3.52}$$

where ω_o denotes the oscillation frequency and $S_\phi(\Delta\omega)$ represents the relative phase noise power at an offset $\Delta\omega$.

As in the case of phase noise analysis of the PLL presented in Section 1.6, timing jitter in PLL's should take into account the effect of noise shaping by the PLL. A comprehensive coverage of this topic is presented in a number of references [57], [59], [63], [82], [83], [84], [85]. The timing jitter of the PLL output depends on the jitter of the input sources such as the reference signal and PFD, the jitter of the VCO, and the bandwidth of the loop. However, in PLL clock synthesizer applications, since the input

reference signal is generated using a low phase noise crystal oscillator, the jitter of the VCO is usually the primary source of jitter at the PLL output. In that case, the jitter performance of the PLL can be improved by choosing a higher loop bandwidth. Although the higher loop bandwidth is advantageous for low jitter at the PLL output, there is always a trade-off between the jitter performance, loop bandwidth, and transient response in PLL design [31]. Although Equation (3.52) describe the relationship between the phase noise and cycle-to-cycle jitter, the effect of noise shaping by the PLL should be taken into account for the case of PLL output jitter as shown in Figure 3.14

In chapter two, it was shown in Figure 2.5 that the total output jitter for a free-running VCO grows over time as the variance of the phase error from each cycle of oscillation adds. Equation (2.28) indicates that the jitter increases as the square root of the measurement interval. This equation for the open loop VCO case is repeated here for the sake of clarity as

$$\sigma_{\Delta T(OL)} = \kappa\sqrt{\Delta T} \tag{3.53}$$

Equation (3.53) can be understood by considering the jitter over the measurement interval ΔT to be sum of jitter contributions from many individual stage delays. If these jitter errors are independent, then the standard deviation of the sum increases as the square root of the number of delays being summed.

For the closed loop case, the plot of $\sigma_{\Delta T(CL)}$ versus ΔT is of the form shown in Figure 3.14. The plot shows two asymptotes intersect at the loop bandwidth time constant τ_{pll}. This can be used to solve for the closed loop σ_x in terms of the open-loop figure of merit κ

$$\sigma x = \kappa \sqrt{\frac{1}{4\pi f_u}} \tag{3.54}$$

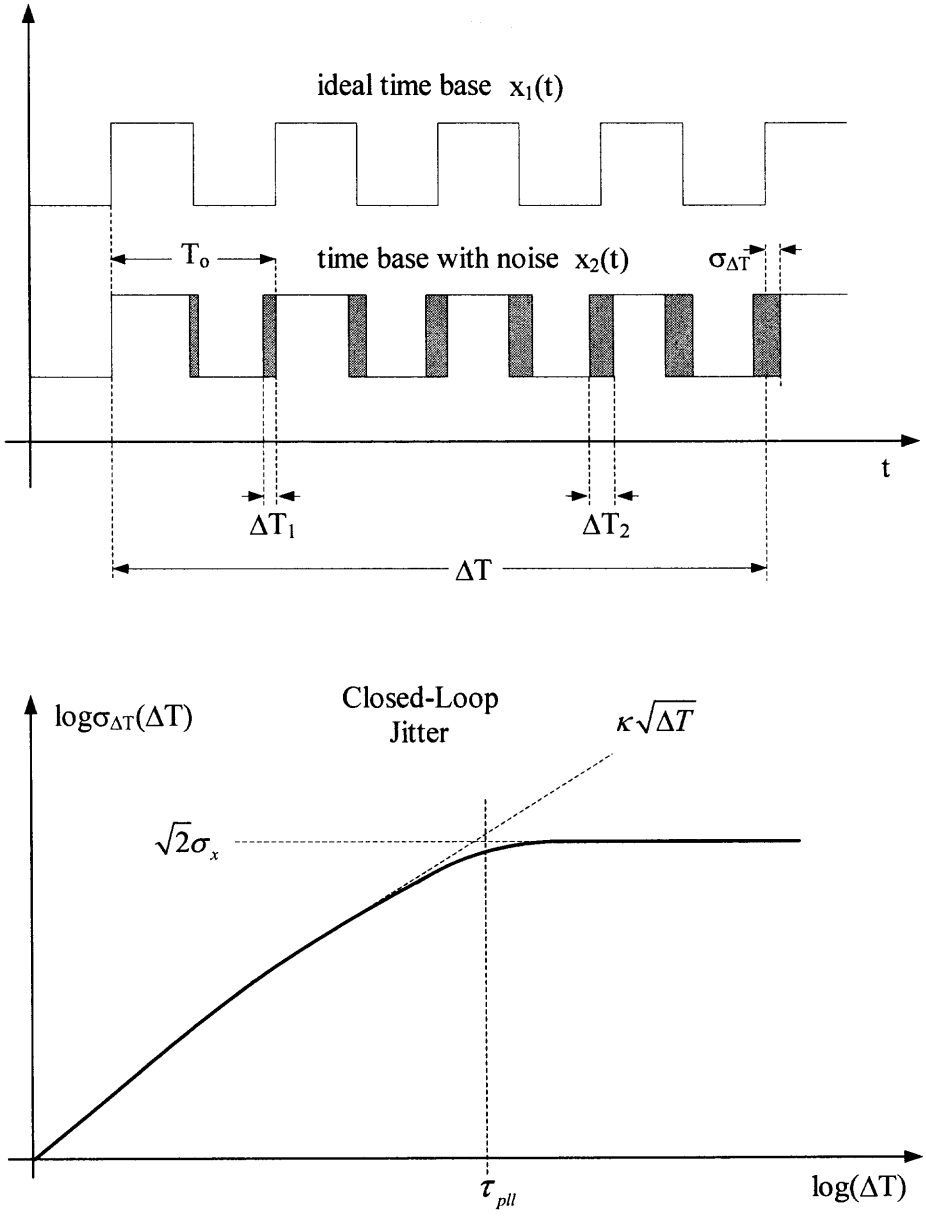


Figure 3.14 The jitter transfer function of the PLL output.

If f_u is a free parameter, the closed-loop jitter can be reduced simply by increasing f_u [82], [83]. It can be shown that for a loop bandwidth of $2\pi f_u$, the jitter rises with the square root of time (as in the case of the free-running VCO) until $t_1 = (2\pi f_u)^{-1}$ and saturates thereafter as shown in Figure 3.14 [82]. As given in [61], the total jitter accumulated over time t_1 by a free running oscillator is equal to

$$\Delta T_1 = \sqrt{\frac{f_o}{2}} \Delta T_{cc} \sqrt{t_1} \tag{3.55}$$

Substituting (3.52) in (3.55) yields the closed-loop jitter as

$$\Delta T_{PLL} = \frac{1}{\sqrt{2\pi f_u}} \sqrt{S_\phi(\Delta\omega)} \frac{\Delta\omega}{\omega_o} \tag{3.56}$$

CHAPTER 4

DESIGN OF A LOW JITTER PLL CLOCK SYNTHESIZER

4.1 Introduction

In the previous chapter a detailed analysis and modeling of the PLL were introduced. This chapter discusses the architecture and design of a PLL clock synthesizer that provides very low phase-noise and timing-jitter when operated from a 3.3 V power supply. Digital video applications require low period jitter and very low phase-noise at far-out offset frequencies from the carrier. A minimum phase noise of –115 dBc/Hz at 1 MHz offset and a maximum period jitter of 15-ps (rms) are often required for these applications.

The primary performance objective of this design is to achieve the specified phase-noise and timing-jitter performance with a 20-400 MHz locking range while operating from a single 3.3 V supply with the lowest possible power dissipation.

The general theory and analysis of phase noise and timing jitter were introduced in Chapter 2. This chapter opens with a discussion of the phase noise and timing jitter requirements of PLL clock synthesizers in sensitive applications. These requirements are followed by the key design considerations for the PLL clock synthesizers. Design tradeoffs between critical parameters of the PLL are then described. The synthesizer architecture and circuit design requirements for a low noise CPLL are then considered. The chapter concludes with the behavioral modeling and simulation of the PLL clock synthesizer.

4.2 Phase Noise and Jitter Requirements of PLL Clock Synthesizers

In high-speed data communication applications, PLL clock synthesizer must meet stringent requirements. The phase noise and jitter requirements are usually the most demanding among other performance expectations which the PLL clock synthesizer should meet. Therefore, the design of a high performance PLL clock synthesizer usually focuses on the minimization of phase noise and timing jitter.

Different applications have varying degrees of sensitivity to phase noise and timing jitter. Therefore, every application that employs a PLL clock synthesizer has its own unique requirement for the phase noise and timing jitter. In wireless applications, mobile phones require low phase noise for high selectivity operation [79], [80]. The local oscillator in a spectrum analyzer needs to be low to increase the dynamic range of the measurements it can take. PLL clock synthesizers for use in digital video applications may have a jitter requirement of less than 10 ps for operation at 200 MHz. Assuming a PLL with an output frequency of 216 MHz, a loop bandwidth of 500 KHz and an output period-jitter of 9.25 ps (rms) is designed, the equivalent phase noise at 1 MHz offset from a 216 MHz carrier can be found using Equation (3.56). The required phase noise at 1 MHz offset would be –109 dBc/Hz.

4.3 PLL Clock Synthesizer Design

PLL clock synthesizers use an indirect frequency synthesis technique to generate frequency-multiplied, phase-synchronous clock signals from an input reference signal that exhibits a low phase noise performance. The technique of frequency synthesis is one of the oldest techniques invented in electronics but still continues to find new

applications in electronics, communication, and instrumentation. This subject is well-documented in literature [1], [2], [3], [4], [5], [7], [69], [70]. An overview of frequency synthesis techniques is presented in this section with an emphasis on the single loop PLL frequency synthesizers.

This single loop architecture finds many applications in modern communication systems. Since this dissertation researches the low phase noise PLL clock generators in high-speed data processing and communication applications, the emphasis is given to the design details of PLL clock synthesizers. Nevertheless, several examples from wireless communication applications are useful to comprehend the role of PLL frequency synthesizers in general.

4.4 Synthesizer Architectures

One of the most common synthesizer architectures in modern communication systems is the CPLL based frequency synthesis technique introduced in Chapter 3. PLL frequency synthesis is an indirect method that generates a synthesized output signal from an input reference signal. This method multiplies the input reference frequency by a variable number that can be programmable. This programming is done by dividing the VCO output frequency by a variable number and adjusting the output frequency such that the divided VCO frequency becomes equal to the input reference frequency at each programming step. A typical example of the indirect frequency synthesis using a PLL is shown in Figure 4.1.

A CPLL frequency synthesizer basically consists of the reference oscillator, phase-frequency detector, charge-pump circuit, loop filter, VCO, and a feedback divider.

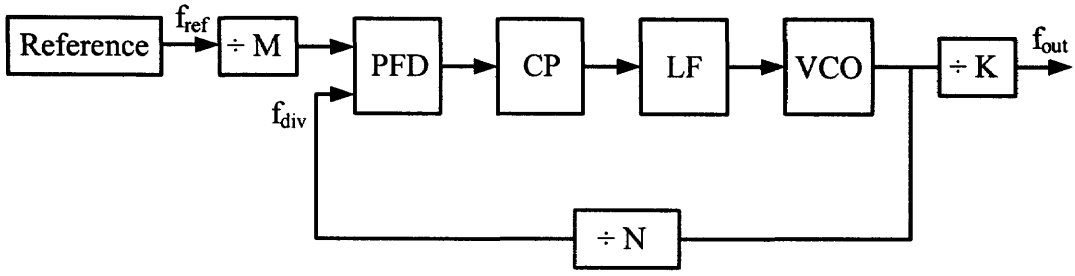


Figure 4.1 Frequency synthesizer using a single loop CPLL.

A buffer or a transmitter circuit may be needed at the output depending on the signal requirements of the application, which employs the synthesizer. In most of the IC-CPLL applications, the VCO is a tunable ring oscillator, which has a tuning range capable of covering a multiple of the reference frequency and is realized using an n-stage differential delay cell circuit with appropriate replica biasing. An LC-resonator-based VCO should be employed if the phase noise specification of the particular application can not be met by a ring oscillator VCO. The reference signal is often generated using a crystal oscillator due to advantages such as low phase noise performance of crystal oscillators, their excellent frequency accuracy, and temperature stability.

The operating frequency of the VCO is divided by a number, N, in the negative feedback loop. When the PLL is at steady-state, i.e., in equilibrium, the negative feedback loop forces the phase and frequency of the input reference signal to match that of the feedback signal, which is a divided version of the VCO output signal. Since the operating frequency of the VCO is divided by a number, N, in the negative feedback loop before the comparison takes place with the input reference frequency, the output frequency of the PLL in lock condition is given by

$$f_{out} = (\frac{N}{M}) \cdot f_{ref} \cdot (\frac{1}{K}) \tag{4.1}$$

Some applications may not need to employ the dividers used in the forward path of the synthesizer as shown in Figure 4.1. In that case, the output frequency of the synthesizer can be expressed as

$$f_{out} = N \cdot f_{ref} \tag{4.2}$$

Assuming a lock state for the CPLL is attained, referring back to Figure 3.7 if the operating frequency of the VCO is perturbed to compensate a change in loop dynamics, the phase difference between f_{div} and f_{ref} causes the PFD/CP circuit to change the error current I_{out} at its output. This current multiplied by the impedance of the LF changes the control voltage of the VCO and the VCO is tuned to another frequency within its tuning range. The function of the loop filter is to suppress the undesired components in the PFD output. The loop filter also determines the noise, acquisition range, lock speed, transient response, and stability of the PLL.

The feedback frequency divider is usually implemented as a programmable divider, allowing the output frequency to change in increments of the input reference frequency. Assuming a frequency of 216 MHz is required for a serial communication system, a feedback divider value of 8 can be used to synthesize this frequency if the input reference frequency of 27 MHz is provided. More advanced programming might be required in certain applications. For example, suppose a nominal local oscillator frequency (LO) of 1000 MHz is required in a wireless receiver system and the input reference frequency is only 1 MHz. A voltage-controlled oscillator, VCO as the LO of the receiver operating at a center frequency of 1000 MHz with the appropriate tuning range can be employed for this application. A programmable feedback divider must be designed capable of dividing by $N = \{1000,1001,1002,....,1010\}$, the output frequencies

in the range of $f_{out} = \{1000, 1001, 1002, ..., 1010MHz\}$ can then be synthesized with the selection of the appropriate divider ratio in the feedback path. The output frequency of the VCO is used to determine which incoming signal is translated to IF in the radio receiver. By changing the programming modulus in the feedback programmable divider, the LO can be moved in increments of the input reference frequency and used to tune in the desired channel. Figure 4.2 illustrates a common use of PLL frequency synthesizers in wireless systems. The BDF and IR filter stand for the band definition filter and image reject filter, respectively.

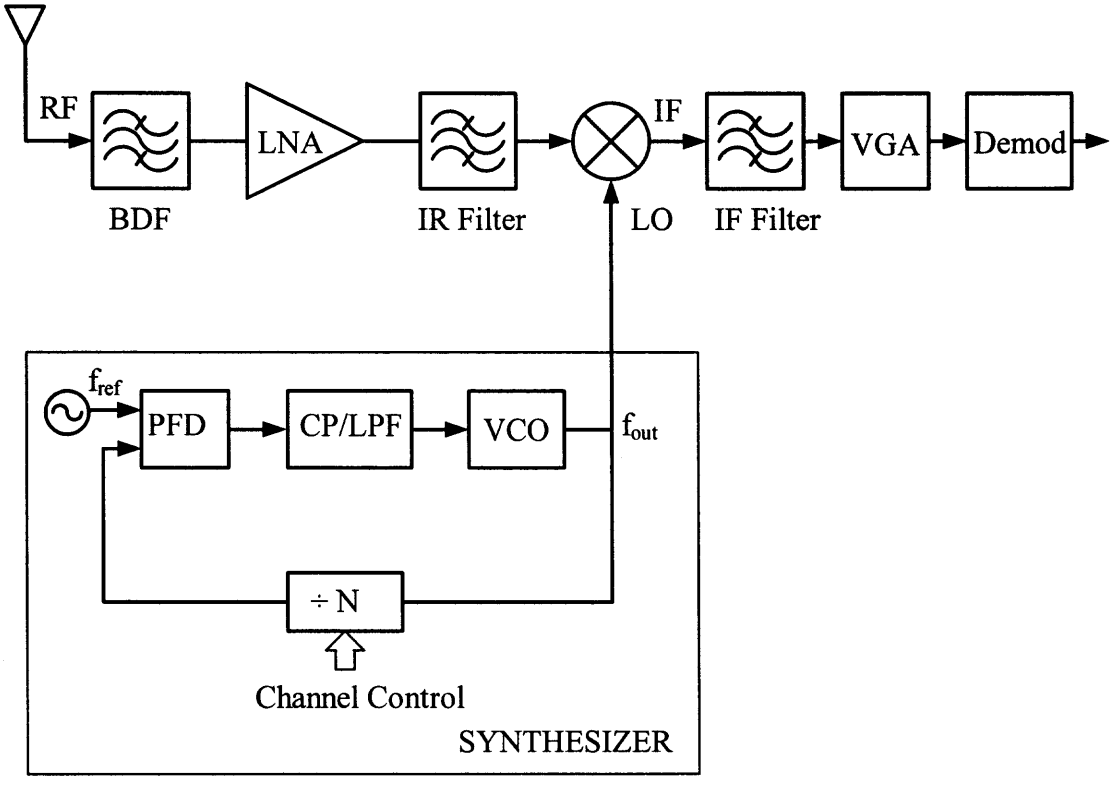


Figure 4.2 A superheterodyne radio receiver with PLL frequency synthesizer.

As shown in Figure 4.2, the channel spacing is set by the reference frequency. This is determined based on the wireless standard being implemented by the receiver. For

example, suppose a FDD CDMA cellular phone receiver is designed: the FDD CDMA standard specifies the channel spacing as 250 KHz and the number of channels as 20 Assuming the local oscillator (LO) starts with a frequency of 1950 MHz for the first channel, this integer-N frequency synthesizer would require a programmable feedback divider in the range of $N = \{7800, 7801, 7802, ..., 7820\}$.

The choice of reference frequency and divide ratio in the feedback divider involves important trade-offs. A programmable divider is usually employed for the feedback divider. These dividers can be implemented with a dual modulus prescaler architecture and additional counters to determine how many times to divide by each modulus for a given divider setting [81]. However, the selection of divider ratio is often more straightforward in most of PLL clock synthesizer applications. In that case, a simple divider circuit dissipating lowest possible power is chosen as implemented in [87].

4.5 Circuit Design Blocks of PLL Clock Synthesizer

Phase detectors, charge-pump circuits, loop filters, and voltage-controlled oscillators are the major circuit design blocks incorporated in most of PLL clock synthesizer applications. Although these circuits and devices may take several different forms in many different applications, the requirements of a particular application determine the form and therefore may impose constrains on the selection of PLL components. Since this dissertation deals with the VLSI implementation of a low phase noise PLL clock synthesizer in CMOS process technologies, the CPLL architecture offers the most appropriate circuits in low-voltage CMOS technologies. The CPLL contains a sequential phase-frequency detector followed by a CMOS charge-pump circuit and loop filter

network. The VCO is often a fully integrated ring oscillator based upon differential delay cell architecture because of their greater immunity to power-supply disturbances.

4.5.1 Phase-Frequency Detector (PFD)

The detection of both phase and frequency difference proves useful in many PLL applications because it significantly increases the acquisition range and lock speed of PLLs [3]. A phase-frequency detector (PFD) is a sequential logic circuit that acts as an extended-range phase detector. The PFD generates an output that is indicative of a phase/frequency error between its input signals. For this reason, circuits capable of phase/frequency detection have found widespread use in frequency synthesizer applications where SNR is high, and signal level transitions are well defined and predictable [38].

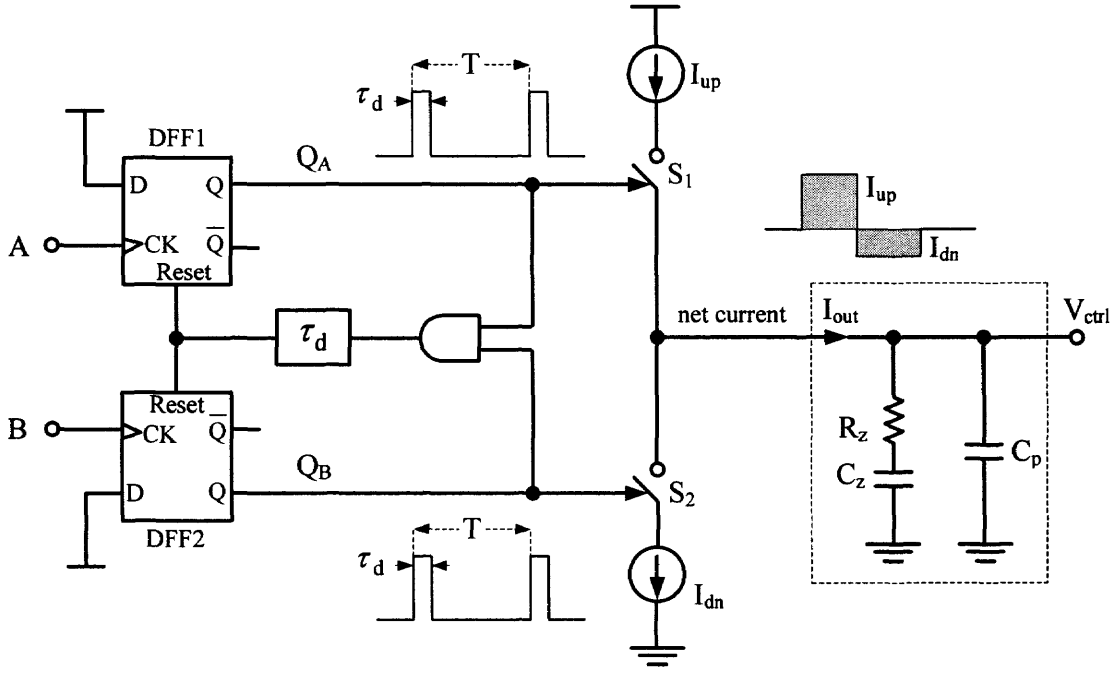


Figure 4.3 Operation of PFD and CP circuits.

As shown in Figure 4.3, the PDF circuit has two inputs as clock inputs, denoted here as A and B. Both of these inputs accept two-level signals whose timing information is carried in the instants of occurrence of their trigger edges [70]. The change in the state of the circuit occurs on the transitions of A and B. The digital circuit that makes up the PFD is implemented as an edge triggered sequential machine. The circuit consists of two edge-triggered D-type flip-flops with their D inputs connected to the power-supply rail V_{dd}, i.e., a logical one level.

The sequential PFD circuit generates two outputs that are not complementary. Figure 4.4 summarizes the function of the PFD for a three-state operation. As shown in Figure 4.4, if the frequency of input A, f_A, is greater than that of input B, f_B, $f_A > f_B$, then the PFD generates positive pulses at Q_A, while Q_B produces narrow reset pulses due to a periodic resetting of the D-flip-flops as shown in Figure 4.4. Conversely, if $f_A < f_B$, then positive pulses appear at Q_B, while Q_A produces narrow reset pulses. If $f_A = f_B$, then the PFD generates coincident narrow reset pulses at both Q_A and Q_B. This happens when the lock condition is reached by PLL. In circuit implementation, the outputs Q_A and Q_B are usually called the UP and DN signals indicating the charge/discharge action on the charge pump circuit.

The circuit that performs the above characteristic requires at least three logical states. These states are simply $Q_A = Q_B = 0$, $Q_A = 0, Q_B = 1$, and $Q_A = 1, Q_B = 0$. As previously mentioned the PFD circuit must be implemented as an edge-triggered sequential machine.

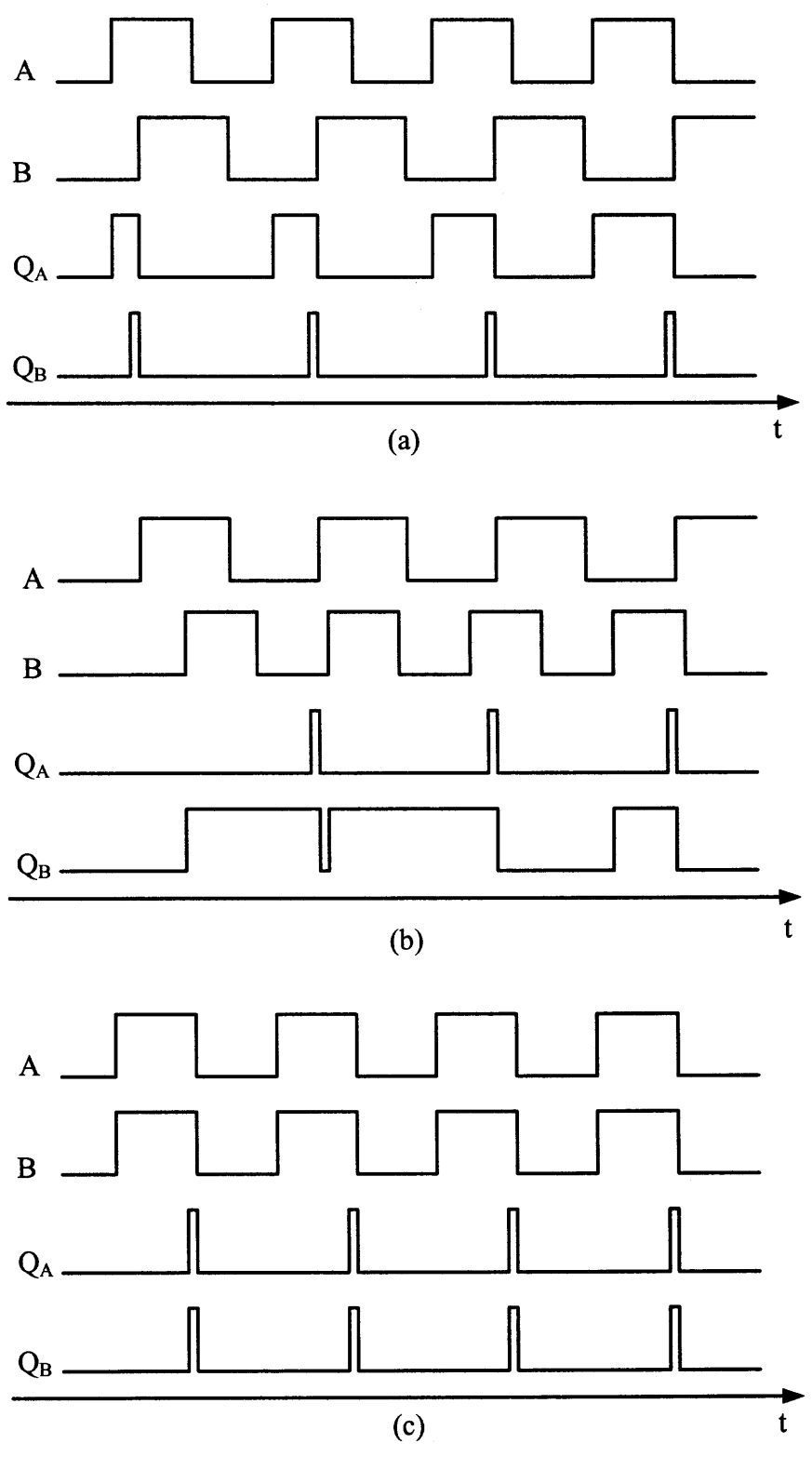


Figure 4.4 PFD response with (a) $f_A > f_B$ (b) $f_A < f_B$ (c) $f_A = f_B$.

The three-state operation of the PFD is summarized in Figure 4.5. If the PFD is in State 0, $Q_A = Q_B = 0$, a transition on A takes it to State I, where $Q_A = 1, Q_B = 0$. The PFD remains in State I until a transition occurs on B, upon which the PFD returns to State 0. Similarly, if the PFD is in State 0, $Q_A = Q_B = 0$, a transition on B takes it to State II, where $Q_A = 0, Q_B = 1$. On Figure 4.3, each switch of the CP circuit acts as a simple switch that closes when its input goes high. In most applications, a positive pulse UP causes the loop filter to integrate some current. This generates a voltage, V_{ctrl}, that slews the VCO in the proper direction.

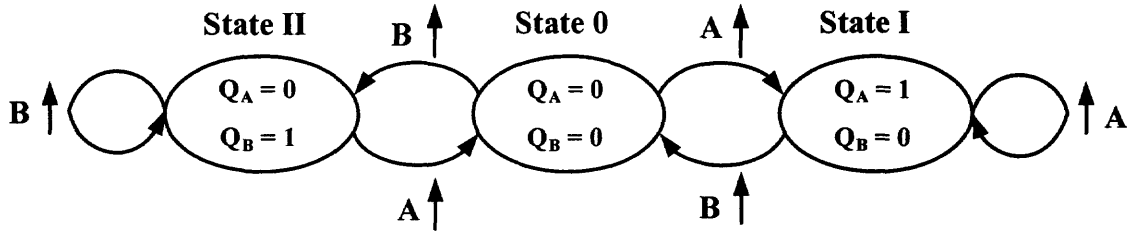


Figure 4.5 State diagram of phase-frequency detector.

4.5.2 Charge-Pump Circuit (CP)

A three-state charge pump can be analyzed in conjunction with a three-state PFD as shown in Figure 4.3. A simple charge-pump circuit consists of two switched current sources driving a loop filter. In CMOS implementation, S_1 and I_{up} are implemented with PMOS devices while S_2 and I_{dn} are realized with NMOS devices. Assuming a positive pulse of width T on Q_A $(UP), I_{up}$ charges the capacitor C_z of the loop filter with a charge equal to $I_{up}T$. If $f_A > f_B$, the positive charge accumulates on C_z steadily driving the control voltage of the VCO V_{ctrl} in the positive direction towards $+\infty$, yielding an

infinite DC gain for the PFD/CP combination. Similarly, if pulses appear on Q_B (DN), I_{dn} discharges C_z on every phase comparison as shown in Figure 4.5, driving V_{ctrl} in the negative direction towards $-\infty$. In the third state with $Q_A = Q_B = 0$, V_{ctrl} remains idle. Assuming the output quantity of the PFD/CP combination is current as shown in Figure 4.4, which is injected by the charge pump into the loop filter, the control voltage of the VCO, V_{ctrl}, can be expressed as [70]

$$V_{ctrl}(s) = I_{out}(s)Z(s) \tag{4.3}$$

Referring back to Figures 3.2 and 3.7, since the gain is the transfer function from the phase error $\Delta\phi$ to the output current of the charge pump I_{out}, the gain of the PFD is given by

$$I_{out}(s) = \frac{I_p - (-I_p)}{4\pi} \cdot \Delta\phi(s) \tag{4.4a}$$

$$I_{out}(s) = \frac{I_p}{2\pi} \cdot \Delta\phi(s) = K_{pfd} \cdot \Delta\phi(s) \tag{4.4b}$$

$$K_{pfd} = \frac{I_p}{2\pi} \tag{4.4c}$$

where K_{pfd} is the gain of the PFD/CP and has a unit of amps/radian.

4.5.3 Loop Filter (LF)

The loop filter is needed for the compensation of the negative feedback loop. The possible topologies for a passive loop filter are shown in Figure 4.6. The more complex passive filters [14] and as well as active filters [75] may be used depending on the requirements of the application. The loop filter sets the approximate gain crossover

frequency of the open loop response and also guarantees the stability of the PLL when other parameters of the PLL such as the gain of the PFD, K_{pfd}, gain of the VCO, K_{vco}, and feedback divider ratio, N, are all specified. Suppose the loop filter only consists of a capacitor C_z. It can be shown using the results of Chapter 3 that type-2 PLL is unstable because the closed loop transfer function contains two imaginary poles at $s_{1,2} = \mp j\sqrt{I_p K_{vco}/(2\pi C_z)}$. In order to stabilize the system, a zero in the loop gain must be introduced by adding a resistor R_z in series with the loop filter capacitor C_z as shown in Figure 4.6(b). In addition, as shown in Figure 4.6(c), a second capacitor C_p can be added to improve the suppression of high-frequency components coming out of the PFD/CP circuit. This capacitor reduces the ripple on the VCO control voltage, V_{ctrl}. A design methodology for an appropriate loop filter is described as part of behavioral simulations in the next section.

4.5.4 Voltage Controlled Oscillator (VCO)

Although there are many possibilities for the selection of VCOs that can be integrated into a low phase noise PLL clock synthesizer implemented in CMOS technologies, this particular design focuses on a ring oscillator VCO architecture. The ring oscillator VCO architecture is proven to be the most suitable architecture in terms of noise performance, tuning range, linearity, and power dissipation in CMOS process technologies. This doesn't imply that ring oscillator VCOs have the lowest noise performance. In CMOS technologies, first of all, compared to alternatives such as the LC resonator-based VCO, the ring oscillator VCO is exceptionally compact. Second, the ring oscillator VCO can

oscillate at very high frequencies. Furthermore, there are additional advantages in preferring ring oscillator VCOs over the LC resonator-based VCOs [63], 86].

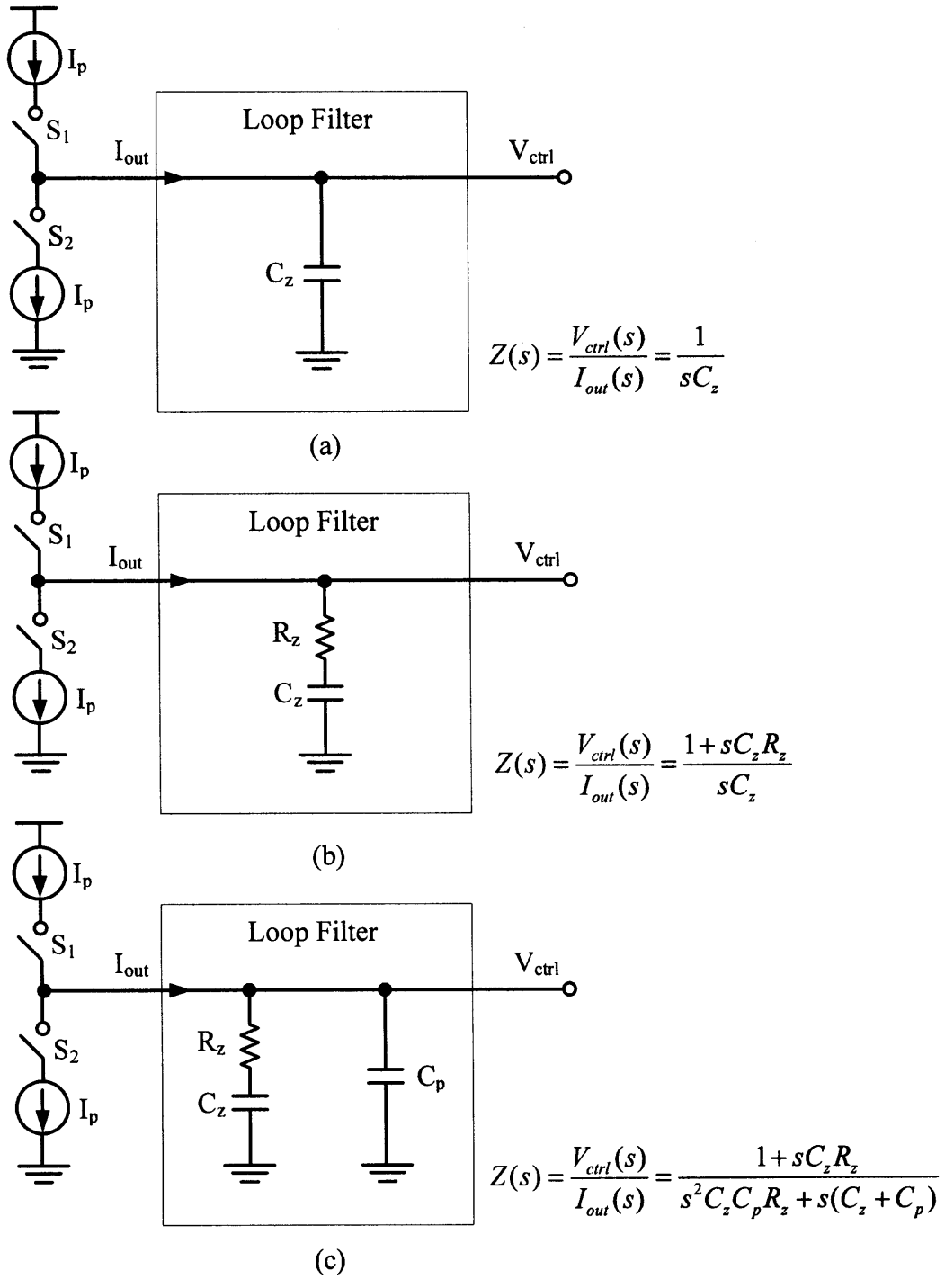


Figure 4.6 Charge pump and passive loop filter topologies used in CPLLs.

For a high performance PLL design requiring the use of a ring oscillator VCO, there are several critical issues regarding the design and realization of the VCO. The realization of the VCO with highest possible power supply noise rejection, low-jitter, low-phase noise, and wide tuning range with acceptable linearity requires careful attention to low level CMOS circuit design issues. Designing a robust ring oscillator VCO circuit with low drift characteristics due to changes in power supply voltage, temperature, and process corners is one of the most important design task in a typical PLL clock synthesizer design because the performance of the PLL depends on the quality of the VCO. In other words, the noise characteristic of the VCO mostly determines the phase noise characteristics of the PLL output. The issues regarding the transistor level circuit design of the ring oscillator VCO are discussed in the next chapter. This section describes the system level design of the ring oscillator VCO.

On today's mixed-signal ICs, almost all ring oscillators use differential delay stages [86], [93] because of their superior immunity to power-supply noise. The VCO consists of an appropriate number of differential delay cell stages together with a replica bias circuit. The replica bias circuit creates a regulated bias for the differential delay cells and comparator circuit as shown in Figure 4.7. The delay cell stages shown in Figure 4.7 are designed using an NMOS source-coupled pair with symmetric load elements.

Figure 4.8 shows a simplified circuit diagram of the four-stage ring oscillator VCO. As shown in Figure 4.8, the symmetric loads consist of a diode connected PMOS device in parallel with an equally sized PMOS device. The bias voltage of PMOS devices V_{bp} is nominally equal to the VCO control voltage V_{ctrl}. Since the top supply is the upper

swing limit, this voltage determines the lower voltage swing limit of the delay cell outputs. The delay changes with V_{ctrl} because the effective resistance of the symmetric load is varied by V_{ctrl}.

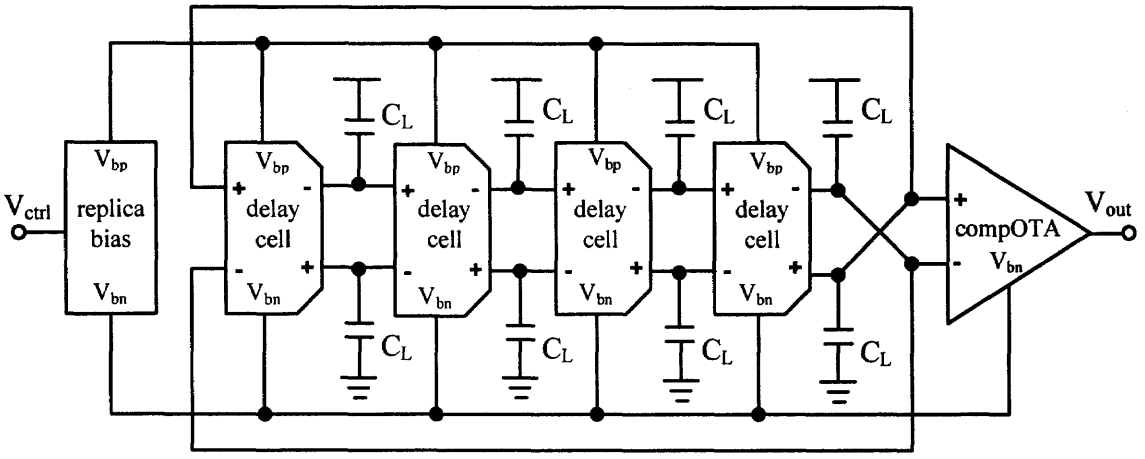


Figure 4.7 Block diagram of a four-stage ring oscillator VCO with replica bias circuit.

The differential delay cell circuit illustrated in the first stage of Figure 4.8 is designed to provide high supply noise immunity while being able to operate at low supply voltages. The key components of the delay cell that achieves these low-noise objectives are the PMOS symmetric load elements and the replica bias circuit as shown in Figure 4.8. The power supply noise sensitivity involves both static and dynamic components. The static power supply sensitivity is dominated by the small-signal output impedance of current sources. The replica bias circuit contains appropriate cascoding to achieve high output impedances. The dynamic supply sensitivity is determined by the symmetric load structure of the delay cell stages. The transistor level design and description of these circuits are given in the next chapter.

Each delay cell stage used in the ring oscillator is based on NMOS source coupled pair with PMOS symmetric load elements and a dynamically biased NMOS tail current

source, as shown in Figure 4.8. The coupling input is formed from an additional source coupled pair sharing the same loads and current source. The bias voltage of simple NMOS current source is continuously adjusted in order to provide a bias current that is independent of supply and substrate voltages. With the output swings referenced to the top supply, the current source effectively isolates the delay cell from the negative supply so that the delay remains constant with changing supply voltages. The load elements are composed of a diode connected PMOS device in shunt with an equally sized PMOS device.

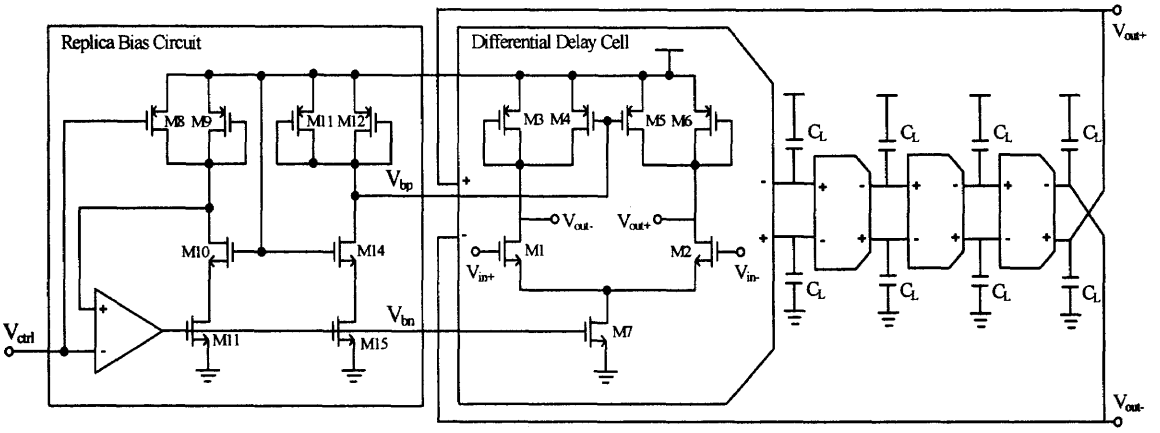


Figure 4.8 Differential delay cell based ring oscillator VCO with replica bias circuit.

This load structure is widely used in CMOS ring oscillator VCOs and called symmetric loads because their $I-V$ characteristics are symmetric about the center of the voltage swing. The control voltage, V_{ctrl}, is the bias voltage for the PMOS devices. It is also used to generate the bias voltage for the NMOS current source and provides control over the delay of the buffer stage. The $I-V$ characteristics of the symmetric load are shown in Figure 4.9. With the top supply as the upper limit of the swing, the lower limit of the swing is symmetrically opposite at the bias voltage of PMOS device M3, V_{ctrl}. As

shown Figure 4.8, V_{ctrl} is also used to generate the bias voltage of NMOS current source, V_{bn}, of the delay stage and therefore provides control over the time-constant delay of the differential delay stage.

It can be shown that the effective resistance of a symmetric load of Figure 4.9 is directly proportional to the small signal resistance of PMOS transistor when biased at V_{bp}, or equivalently at V_{ctrl}. Since M3 and M4 typically have device sizes greater than minimum channel length and are biased at V_{bp}, they are operated in the active region (the saturation region). Therefore, a simple quadratic equation can be used to represent the $I-V$ characteristics of the PMOS transistor. For this case under consideration, the drain current of one of the two equally sized PMOS devices biased at V_{ctrl} can be expressed as

$$I_D = \frac{\mu_p C_{ox}}{2} \cdot \frac{W}{L} \left(V_{ctrl} - V_{TP}\right)^2 \tag{4.5}$$

Taking the derivative with respect to V_{ctrl}, the small signal current gain can be expressed as

$$g_m = \frac{dI_D}{dV_{ctrl}} = \mu_p \cdot C_{ox} \cdot \left(V_{ctrl} - V_{TP}\right) = \sqrt{2 \cdot \mu_p \cdot C_{ox} \cdot I_D} \tag{4.6}$$

Hence, the effective resistance of the PMOS pair can be expressed as

$$\mathrm{R}_{EFF} = \left(\frac{dI_D}{dV_{GS}}\right)^{-1} = \frac{1}{g_m} = \frac{1}{\mu_p \cdot C_{ox} \cdot \left(\frac{W}{L}\right) \cdot \left[V_{ctrl} - V_{TP}\right]} \tag{4.7}$$

where g_m is called the transconductance of the transistor.

As depicted in Figure 4.9, the straight lines represent the effective resistance of the symmetric load and show the symmetry of its $I-V$ characteristics.

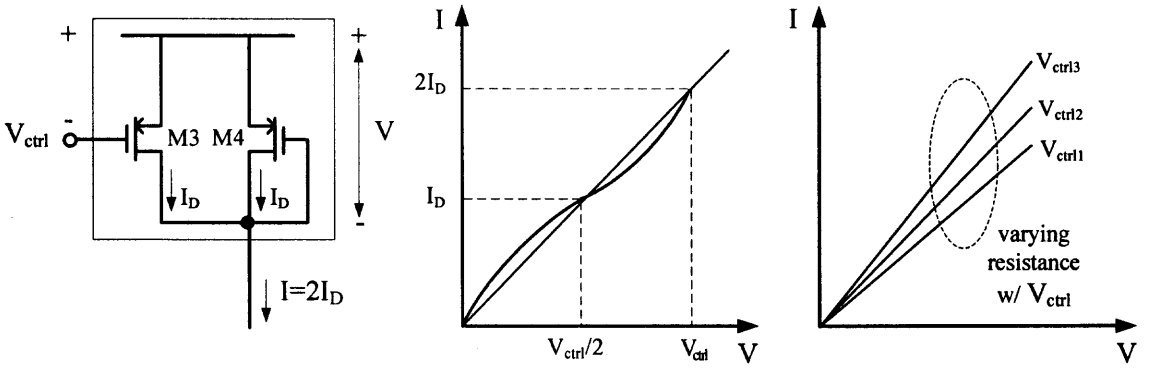


Figure 4.9 Symmetric load $I-V$ characteristics.

Since the effective resistance of the load changes with the VCO control voltage, V_{ctrl}, the time-constant delay of the differential stages also changes with the control voltage. In addition, the buffer bias current is adjusted by V_{bn} so that the output swings vary with the control voltage rather than being fixed in order to maintain the symmetric $I-V$ characteristics of the loads.

Another purpose of using symmetric loads in ring oscillator VCOs is to achieve high dynamic supply noise rejection. The CMOS realization of symmetric loads has additional advantages. The quiescent biasing point of a buffer with symmetric loads, which is at the center of the output voltage swing, is the point where the buffer's gain is largest. As a result, the oscillation frequency range will typically be very broad [86].

The gain of the VCO can be determined based on the circuit parameters. First, a relationship between the time-constant delay of the differential delay cell, effective resistance, and load capacitance is needed. The single-stage delay of the differential delay cell circuit can be defined as

$$t = R_{EFF} \cdot C_{EFF} = \frac{1}{g_m} \cdot C_{EFF} \tag{4.8}$$

where C_{EFF} is the effective capacitance of the delay cell stage and is given by

$$C_{EFF} = C_L + C_{par} \tag{4.9}$$

where C_{par} is the parasitic capacitance of CMOS devices and can be expressed as

$$C_{par} = \left(\frac{1}{2}\right)\cdot C_{g,N} + \left(\frac{1}{2}\right)\cdot C_{g,P} = \left(\frac{1}{2}\right)\cdot W_n L_n C_{ox} + \left(\frac{1}{2}\right)\cdot W_p L_p C_{ox} \tag{4.10}$$

Using a simplified replica-bias circuit shown in Figure 4.8, the bias generator sets the buffer bias current equal to the current through a symmetric load with its output voltage at V_{ctrl}. In this case, the two equally sized PMOS devices are both biased at V_{ctrl} and each source is half of the replica bias current [28].

Equation (4.8) can be combined with Equation (4.6) to obtain

$$t = \frac{C_{EFF}}{\mu_p \cdot C_{ox} \cdot (V_{ctrl} - V_T)} \tag{4.11}$$

Equation (4.11) is the single stage delay of a delay cell stage shown in Figure 4.9. Therefore, the total delay for an n-stage VCO can be defined as

$$\Sigma T = n \cdot t = \frac{C_T}{2 \cdot \mu_p \cdot C_{ox} \cdot (V_{ctrl} - V_T)} \tag{4.12}$$

where n is the number of the differential delay cell stages. The total capacitance, C_T, is defined as

$$C_T = 2 \cdot n \cdot C_{EFF} \tag{4.13}$$

Since the frequency is the reciprocal of the total delay, the oscillation frequency for an n-stage ring oscillator VCO can be expressed as

$$f_{osc} = \frac{1}{2 \cdot \Sigma T} = \frac{1}{2 \cdot n \cdot t} = \frac{\mu_p \cdot C_{ox} \cdot (V_{ctrl} - V_T)}{C_T} = \frac{\sqrt{2 \cdot \mu_p \cdot C_{ox} \cdot I_D}}{C_T} \tag{4.14}$$

As seen in Equation (4.14), the oscillation frequency is proportional to the square root of the bias current of the delay cell circuit. Taking the derivative of the oscillation frequency with respect to V_{ctrl}, the VCO gain K_{vco} is given by

$$K_{vco} = \left| \frac{df}{dV_{ctrl}} \right| = \frac{\mu_p \cdot C_{ox}}{C_T} \tag{4.15}$$

Equation (4.15) simply states that the gain of the VCO only depends on the MOS device parameters and total load capacitance of the ring oscillator.

4.6 Design Methodology and Behavioral Simulation

The system level design of the PLL clock synthesizer is an important task to create a CMOS chip that meets the target specifications. The system design of the PLL based on analytical methods developed in Chapter 3 and behavioral simulation help identify problems early in the design process. The component values of the circuit design blocks and the parameters of the PLL have to be properly determined. These parameters may need to be optimized to assure stability of the PLL before performing design tasks and transient simulations of the transistor- level circuits of the

Figure 4.10 shows a simplified design procedure for a successful CMOS IC development. First, all of the critical parameters of the PLL are specified. Second, the mathematical models developed in Chapters 3 and 4 are used to perform the analysis and synthesis of the loop filter, evaluation of the gain of the VCO, and verify the stability of the PLL. Third, the transistor-level phase noise characteristics of the crystal oscillator, PFD/CP, and VCO are obtained from SPECTR-RF simulations. The SPECTRE-RF

simulations employ BSIM3v3 [91], [92] noise models of MOS devices and respective circuit components.

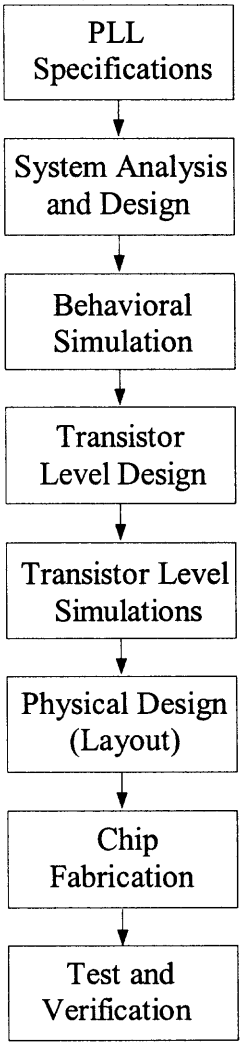


Figure 4.10 Design procedure for PLL clock synthesizer.

Since the input reference signal is generated using a crystal oscillator circuit, it provides better phase noise performance compared to the minimum levels expected from the PLL at any frequency offsets considered in this design. Although the large loop bandwidth is chosen for this design and the phase noise of input sources at offset frequencies below the loop bandwidth can't be filtered out, the phase noise of the

reference signal doesn't affect the expected phase noise of the PLL output due to its superior phase noise performance within the loop bandwidth of the PLL as will be shown later in this section. The only source of noise in a passive loop filter of a third order PLL is resistor R_z. The characteristics of phase noise due to R_z were discussed in Section 3.6. It is important to make sure that the thermal noise of this resistor does not cause too much noise peaking at low frequencies while maintaining low noise at high frequencies. The simulation to the phase noise of the VCO due to the thermal noise of R_z will be considered in this section. Fourth, the phase noise performance of the PLL is predicted using behavioral simulations developed in MATLAB/Simulink. Finally, the transistor-level circuit design is carried out, along with comprehensive simulation of circuits both in time and frequency domains. The SPECTRE-RF simulation of the entire PLL is also performed to determine the transient settling characteristics, timing jitter, and the phase noise.

The selection of VCO gain and charge pump current is one of the most critical step in the early phases of the design process to determine the potential success of the design. For low phase-noise performance, the VCO gain have to be chosen as low as possible while maintaining the required tuning range. The charge pump current should be increased to compensate the reduction in VCO gain for maintaining the open loop gain and stability of the PLL. An advantage that comes from the small value of the VCO gain, K_{vco}, is a reduced sensitivity to the noise generated by the circuit design blocks of the PLL such as the charge-pump circuit and loop filter resistor, which may introduce noise on the control voltage of the VCO, V_{ctrl}. Therefore, the choice of the optimum parameters for the PLL entail a trade-off between the VCO gain, K_{vco}, and charge-pump current, I_p

in order to achieve low phase-noise at the output of the VCO. This trade-off can be explained rewriting Equation (3.3) in the following form:

$$H(s) = \frac{N \cdot K_{pfd} \cdot K_{vco} \cdot Z(s)}{s \cdot N + K_{pfd} \cdot K_{vco} \cdot Z(s)} \tag{4.16}$$

The noise contribution of each circuit design block can be considered as an additive noise source at the output of the block. Figure 4.12 illustrates the linear model of the PLL with these noise sources. For a given value of the product $K_{pfd} \cdot K_{vco}$ and by keeping the values of N and $Z(s)$ constant, the closed loop transfer function $H(s)$ given in Equation (4.16) is proportional to the product $K_{pfd} \cdot K_{vco}$. Furthermore, the noise component of the charge pump current, $\overline{i_{p,n}^2}$, is proportional to the charge pump current I_p itself. Therefore, decreasing K_{vco} by a factor K and increasing I_p by the same factor doesn't change the loop bandwidth of the PLL. It doesn't affect the stability of the PLL as well. Although this trade-off may introduce a problem in some applications due to the reduced tuning range of the VCO, it is not an issue in this design because the VCO still have an appropriate tuning range as will be discussed in this section.

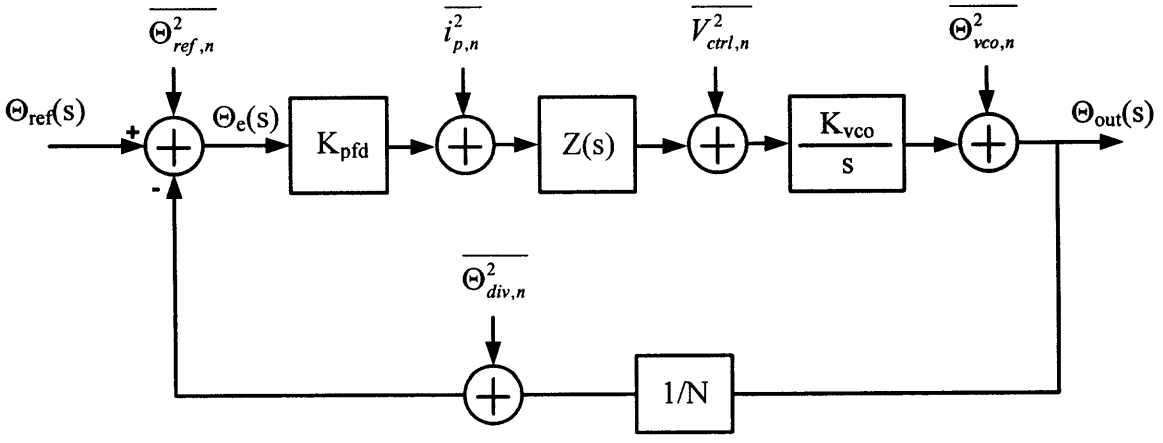


Figure 4.11 CPLL linear model with noise sources.

4.6.1 Design Methodology

The design methodology developed in this section can help to increase design productivity. The design of the loop filter is a challenging task because it determines the PLL settling characteristic, stability, and output phase noise. The loop filter is also responsible for the biggest contribution to the chip area due to the on-chip realization of large capacitance values using the integrated MOS device capacitors. The charge-pump circuit and associated loop filter topologies were shown in Figure 4.6. As will be discussed in the next chapter, switches of the CP circuit are implemented using transmission gate circuits which employs NMOS and PMOS devices to minimize the clock feedthrough and every transistor has its own control signal, the relative timing of which is optimized to avoid glitches at the output.

The second-order loop filter shown in Figure 4.6(c) is employed in the actaul design. As discussed in Chapter 3, the additional pole provides more spurious suppression. However, the extra phase lag associated with this pole introduces a stability issue. Therefore, the loop filter must be designed carefully to provide the required spurious suppression while maintaining the loop stability. The impedance equation given by Equation (3.12) for the loop filter shown in Figure 4.6(c) is repeated here to obtain

$$Z(s)=\left(\frac{b}{b+1}\right)\cdot\frac{\tau_z s+1}{sC_z\left(\frac{\tau_z s}{b+1}+1\right)} \tag{4.17}$$

where $\tau_z = R_z C_z$ and $b = C_z / C_p$. In this case, the open loop gain G_{ol} given by Equation (3.16) of the third order PLL can expressed as

$$G_{ol}=\frac{K_{vco}I_p}{2\pi N}\cdot\left(\frac{b}{b+1}\right)\cdot\frac{\tau_z s+1}{s^2C_z\left(\frac{\tau_z s}{b+1}+1\right)} \tag{4.18}$$

The phase margin ϕ_{PM} given by Equation (3.21) can expressed as

$$\phi_{PM} = \tan^{-1}(\tau_z \omega_c) - \tan^{-1}\left(\frac{\tau_z \omega_c}{b+1}\right) \tag{4.19}$$

Similarly, Equations (3.22), (3.23), and (3.24) repeated here to obtain

$$\omega_c = \frac{\left(\sqrt{b+1}\right)}{\tau_z} \tag{4.20}$$

$$\phi_{PM_{\max}} = \tan^{-1}\cdot\left(\sqrt{b+1}\right) - \tan^{-1}\cdot\left(\frac{1}{\sqrt{b+1}}\right) \tag{4.21}$$

where $\phi_{PM_{\max}}$ is the maximum phase margin. Thus, the maximum phase margin is only a function of b (the ratio of two loop filter capacitors C_z to C_p.)

$$C_z = 2C_p\left(\tan^2\phi_{PM} + \tan\phi_{PM}\sqrt{\tan^2\phi_{PM}+1}\right) \tag{4.22}$$

Since $|G_{ol}| = 1$ at the crossover frequency, if the gain crossover frequency is forced to meet $\omega_c = \sqrt{b+1}/\tau_z$, this leads to the following result:

$$\frac{K_{vco} I_p}{2\pi N}\left(\frac{b}{b+1}\right) = \frac{C_z}{\tau_z^2}\sqrt{b+1} \tag{4.23}$$

Thus from above discussions a design method for the loop filter can be described as in the following:

(1) Find K_{vco} for the ring oscillator VCO (refer to Figure 4.12)

(2) Chose a desired phase margin and find the value of b from Equation (4.21)
(if $\phi_{PM} = 62^\circ$ $b = 15$)

(3) Choose the crossover frequency ω_c and find time constant τ_z from Equation (4.20)

(4) Select C_z and I_p such that Equation (4.23) is satisfied.

(5) Using the results described in Section 3.6, the noise contribution of the loop filter resistor R_z is calculated. If the calculated noise meets the specifications, the design is complete. Otherwise, the value of C_z has to be increased. Step (5) has to be repeated.

(6) Using Equations (3.7), (3.8), (3.18), and (3.19) the open loop and closed loop parameters of the PLL can be calculated.

The continuous-time approximation based on $\omega_{ref}/10 \geq \omega_n$ makes sure that the continuous-time analysis is valid for the PLL. If the loop bandwidth, ω_n, becomes comparable with the input frequency, the continuous-time approximation used in Chapter 3 breaks down, necessitating discrete-time analysis [72], [73], [88]. In addition, equations were derived by Gardner [88] to define a stability limit implying an upper bound on ω_n.

Table 4.1 summarizes PLL parameters and component values of the loop filter (note that $\omega_n = 2\pi f_n$, $\omega_z = 2\pi f_z$, and so on). The simulated tuning characteristic of the ring oscillator VCO is shown in Figure 4.12.

Table 4.1 Parameters of CPLL and component values of loop filter

$f_{ref}/10$ (*MHz*)	I_p (μA)	K_{vco} (*MHz/V*)	C_z (*pF*)	R_z ($k\Omega$)	C_p (*pF*)	N	f_n (*kHz*)	f_z (*kHz*)	ζ	f_c (*MHz*)	f_{p3} (*MHz*)
2.7	80	170	250	2.1	15	2	815	302	1.35	2.21	6.05
2.7	80	170	250	2.8	15	4	575	227	1.27	1.46	4.55
2.7	80	170	250	3.5	15	6	470	181	1.3	1.22	3.66
2.7	80	170	250	4.1	15	8	408	160	1.27	1.05	3.18

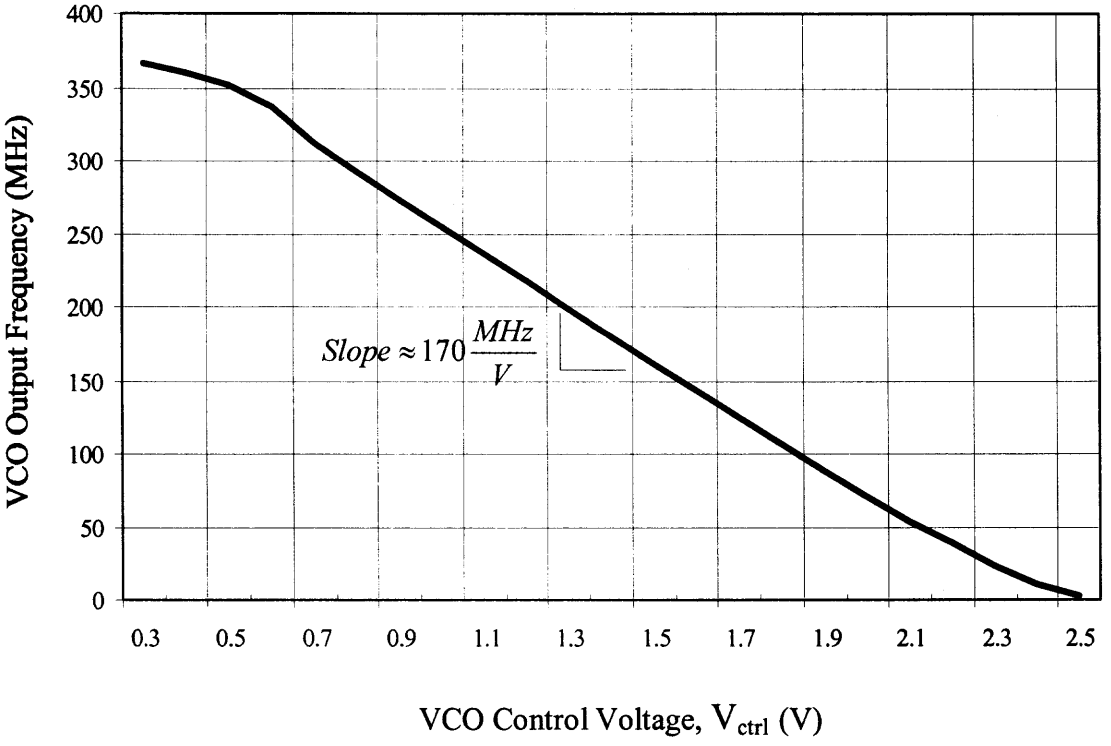


Figure 4.12 VCO tuning characteristics.

4.6.2 Behavioral Simulation

Based on the block diagram of the CPLL shown in Figure 3.2 and analytical methods developed in Chapters 3 and 4, a behavioral model is developed in MATLAB. This model is described in Appendix A.

Using the above behavioral model, the open loop gain Bode plot of the design given in Table 4.1 is determinde and shown in Figure 4.13. The multiple plots in Figure 4.13 correspond to the programmable values of division ratios $N = \{2,4,6,8\}$. In addition, the behavioral model also calculates the closed loop AC response of the PLL. The closed loop AC response of the PLL is shown in Figure 4.14.

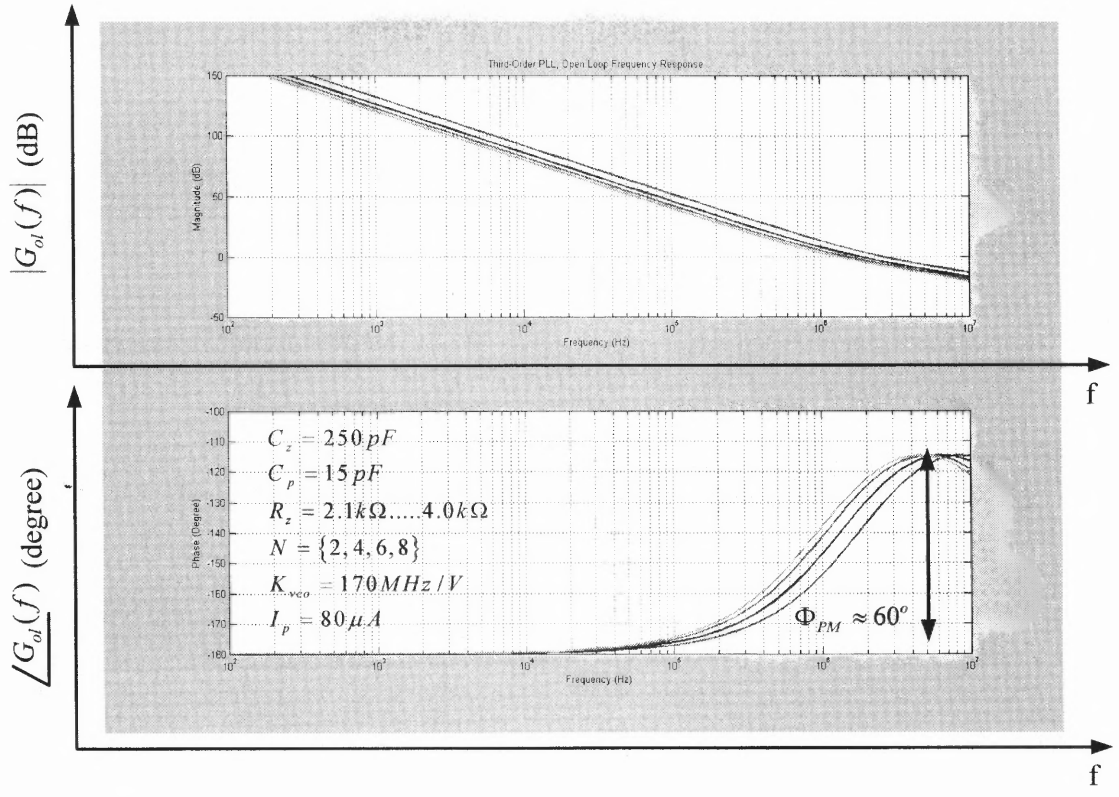


Figure 4.13 Open loop gain Bode plot and corresponding loop parameters.

The closed loop transient step response of the third-order CPLL was also calculated using the above behavioral model. For this purpose, "step(sys)" function of MATLAB is used to calculate the unit step response of the linearized third-order CPLL. In MATLAB, the "sys" variable represents a linear-time-invariant (LTI) model of the system considered. The unit step function applied and the corresponding closed loop transient response are shown in Figure 4.15. The LTI model of the third-order CPLL is entered in the MATLAB behavioral model. This model is simply a linearized model of the CPLL given by Equation (3.25). The duration of the simulation t is determined automatically by MATLAB's "step" function based on the CPLL's poles and zeros. Since the system is causal and relaxed at $t = 0$, the lower limit of time will be zero. These

calculations are made internally by MATLAB's "step" function. However, since both the impulse response of the system $h(t)$ and input excitation $u(t)$ are known, the response of the closed loop system can also be determined by a simple convolution operation of these two functions, which is designated symbolically by $u(t) * h(t)$. The multiple plots shown in Figure 4.15 represent the response of each case of the design example given in Table 4.1. In addition to the transient response based on the linear model of the third-order CPLL, the actual transient response of the nonlinear CPLL is obtained by the SPECTRE transient simulation using the actual transistor level circuits. Figure 4.16 shows the actual transient settling characteristics of the VCO control voltage V_{ctrl}. In this case, the step function (the input excitation) is produced by turning on DC power supply at $t = 0$.

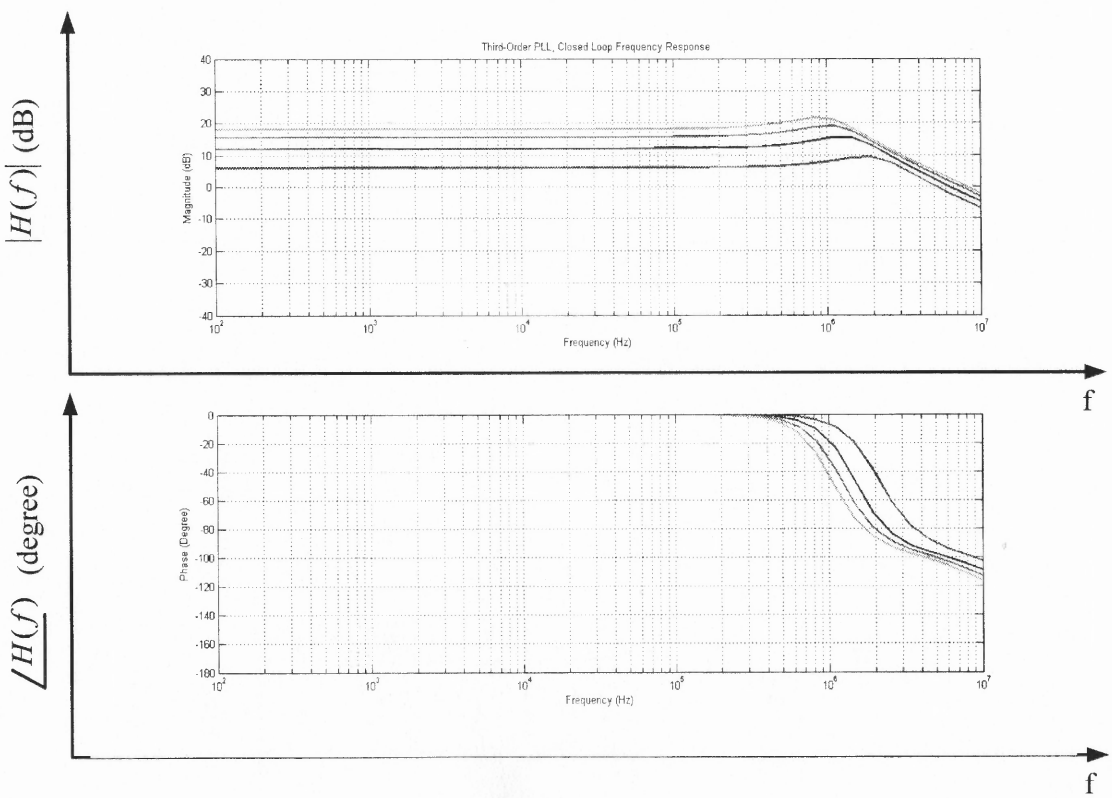


Figure 4.14 Bode plot of closed loop transfer function.

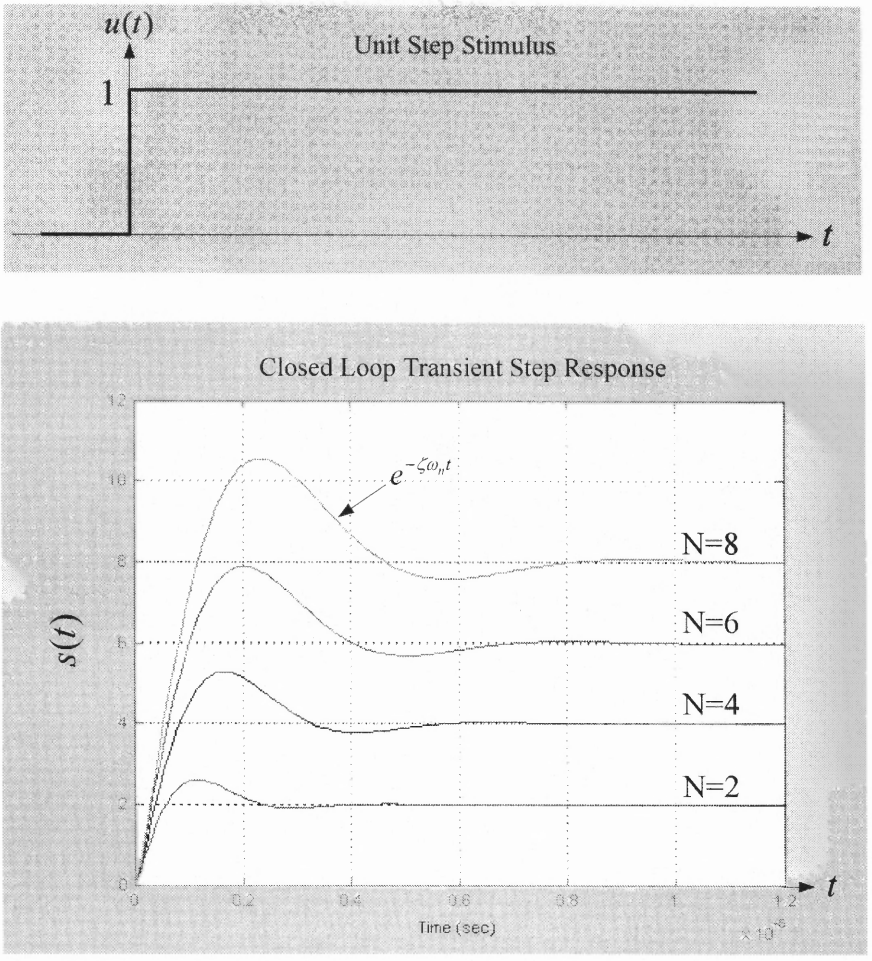


Figure 4.15 Step input response of linearized CPLL

The phase noise response of the PLL output is predicted using behavioral simulations before the transient analysis of circuits and the entire PLL is performed. The phase noise analysis program package given in [90] can predict the phase noise performance of the PLL output very accurately if the phase noise response of the individual circuit design blocks of the PLL are known. For this purpose, SPECTRE-RF simulation of phase noise of the circuit design blocks is carried out. SPECTRE-RF uses BSIM3v3 models for MOS devices to calculate the 1/f and channel thermal noise.

BSIM3v3 models for MOS devices are provided by Austria Micro Systems (AMS) as part of the CMOS process design kit [91], [92].

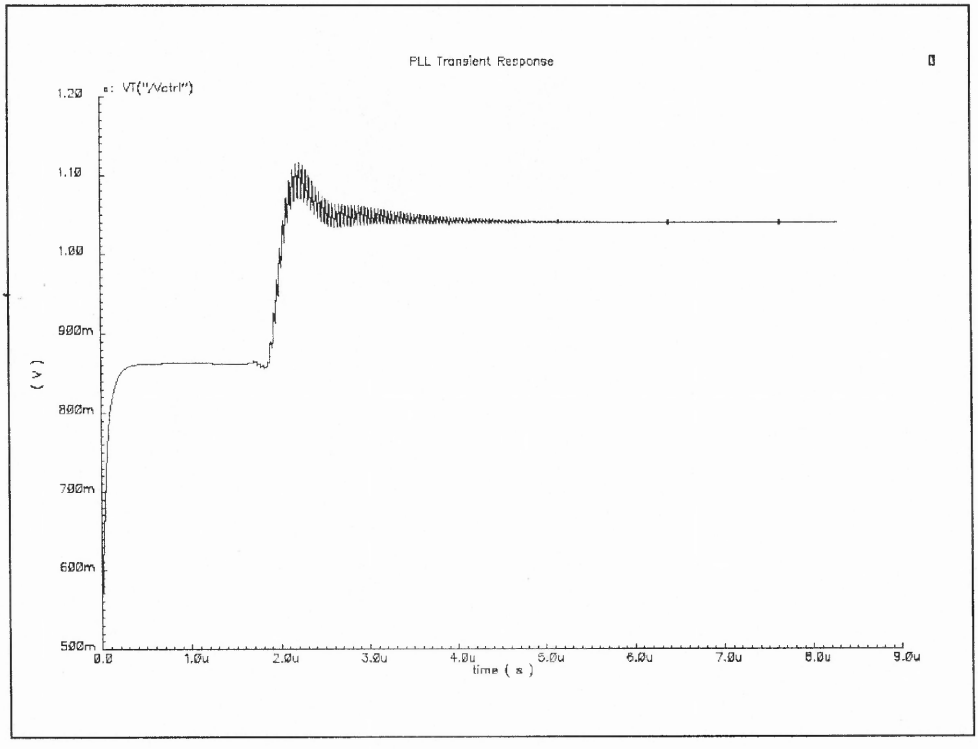


Figure 4.16 Actaul transient response of nonlinear CPLL.

As explained above, the SPECTRE-RF uses the BSIM3 models to estimate the true inherent phase noise of the circuit design blocks due to both flicker and white noise. Figure 4.17 illustrates the SPECTRE-RF simulated phase noise of the implemented PFD. For this simulation, two coincident pulses are applied to the reference and the feedback signals and the PSS/PNOISE simulation of the SPECTRE-RF calculates the phase noise at one of the PFD outputs. Similarly, the phase noise of the ring oscillator VCO including its bias circuits is determined by the SPECTRE-RF simulation and shown in Figure 4.18. A comprehensive analysis of the phase noise in ring oscillator VCOs has recently been

reported by Abidi [63] in a ring oscillator study. Figure 4.18 illustrates the phase noise performance of the implemented ring oscillator VCO, which is optimized for thermal noise using appropriate device sizes for the source coupled input NMOS transistors M1 and M2 of the differential delay cell shown in Figure 4.8.

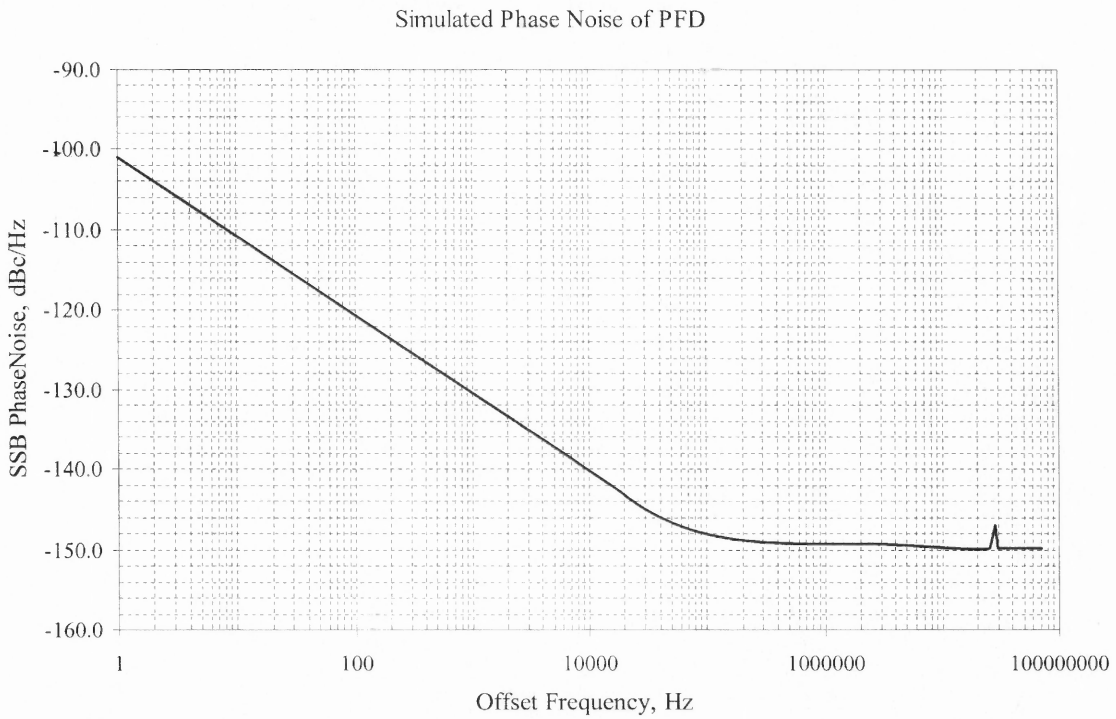


Figure 4.17 Simulated phase noise of PFD.

Every circuit design block of the PLL generates noise as shown in the linear model of Figure 4.11. The noise generated by the individual circuit design block contributes to the overall phase noise at the output of the PLL clock synthesizer. As discussed previously in Chapter 3, a larger loop bandwidth reduces the timing jitter of the VCO while allowing more noise from the input reference source. However, the input reference source is generated using a high-Q crystal resonator and exhibits low phase

noise. Therefore, larger loop bandwidths are preferred in this design to suppress the phase noise of the VCO at larger offset frequencies while maintaining very low phase noise from the crystal oscillator. The phase noise performance of the crystal oscillator which generates the input reference clock is shown in Figure 4.19. The phase noise of the loop filter resistor R_z is also taken into consideration.

Figure 4.20 shows the calculated VCO phase noise due to the thermal noise of resistor R_z using Equation (3.62). The calculated phase noise contribution of the thermal noise of the resistor to the VCO noise at 1 MHz offset frequency is –141 dBc/Hz, which is negligible compared to the intrinsic noise of the ring oscillator VCO.

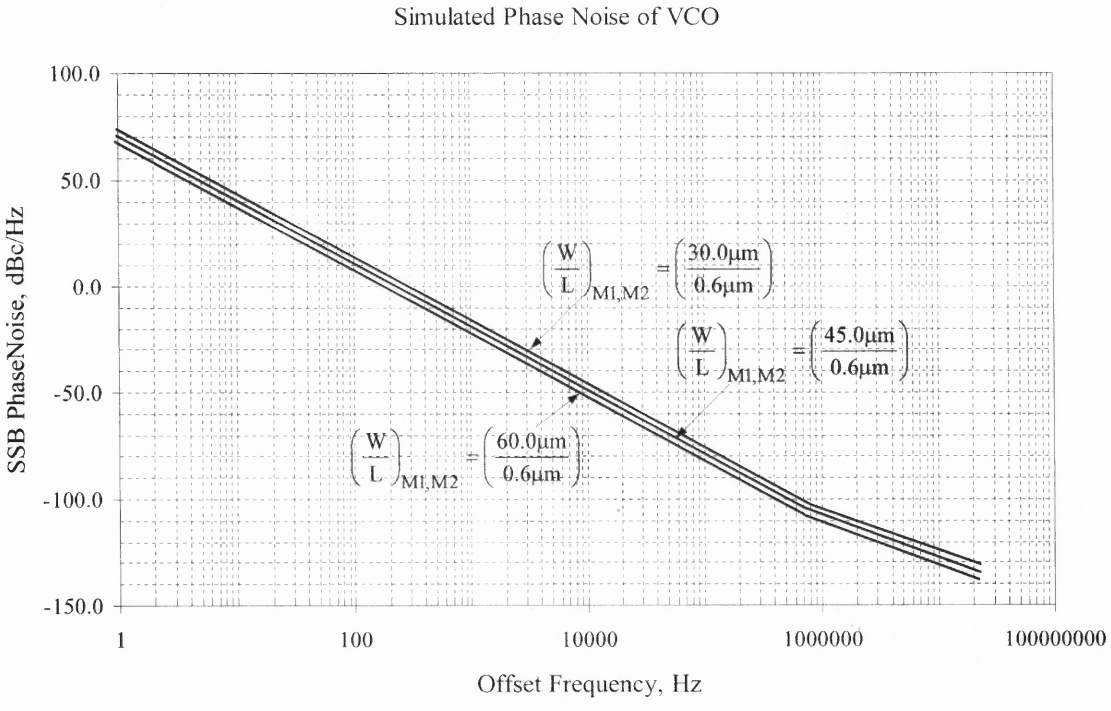


Figure 4.18 Simulated phase noise of ring oscillator VCO.

This phase noise analysis program can predict the phase noise response of the PLL output very accurately if the phase noise characteristics of the individual circuit design blocks of the PLL are provided. Using this program, an estimate of the PLL noise performance can be viewed by entering in noise parameters such as the magnitude of the PFD noise and VCO noise and observing the resulting phase noise response and rms jitter at the output of the PLL. This phase noise analysis program is developed based on a linear model similar to one illustrated in Figure 4.11 [94]. As discussed in Chapter 3, this model can be used to analyze the small-signal dynamic properties of the PLL and as well as its noise performance.

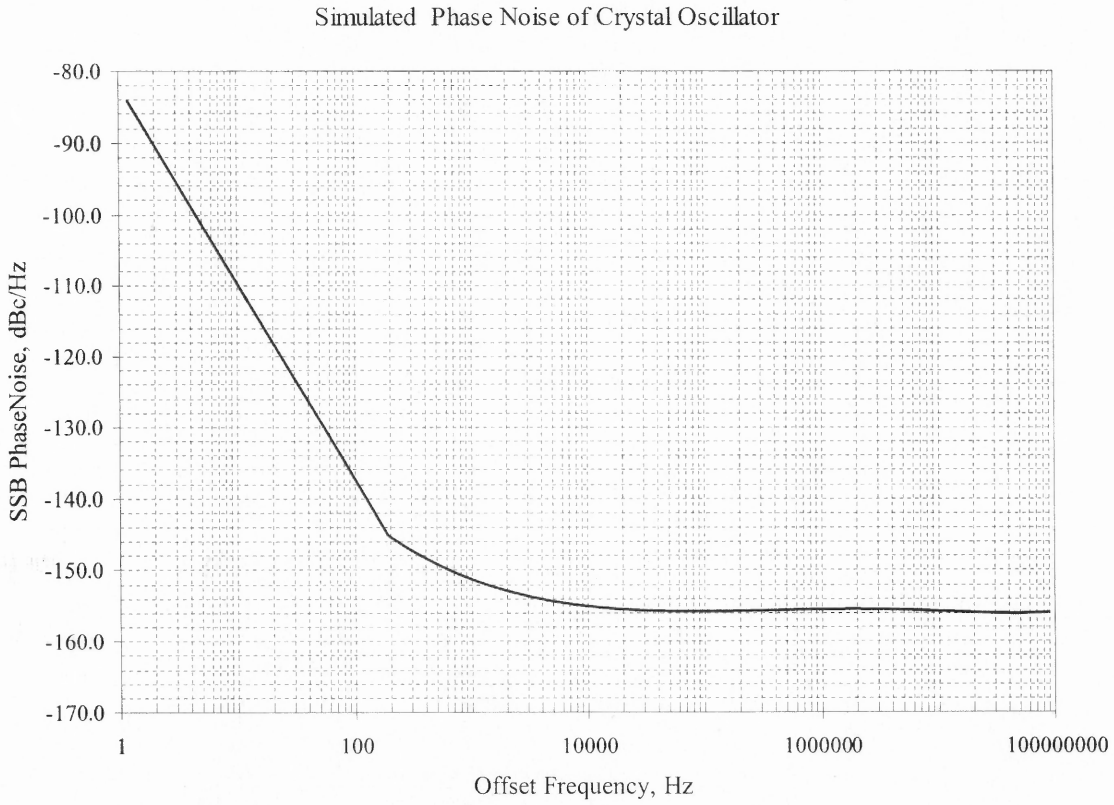


Figure 4.19 Simulated phase noise of crystal oscillator.

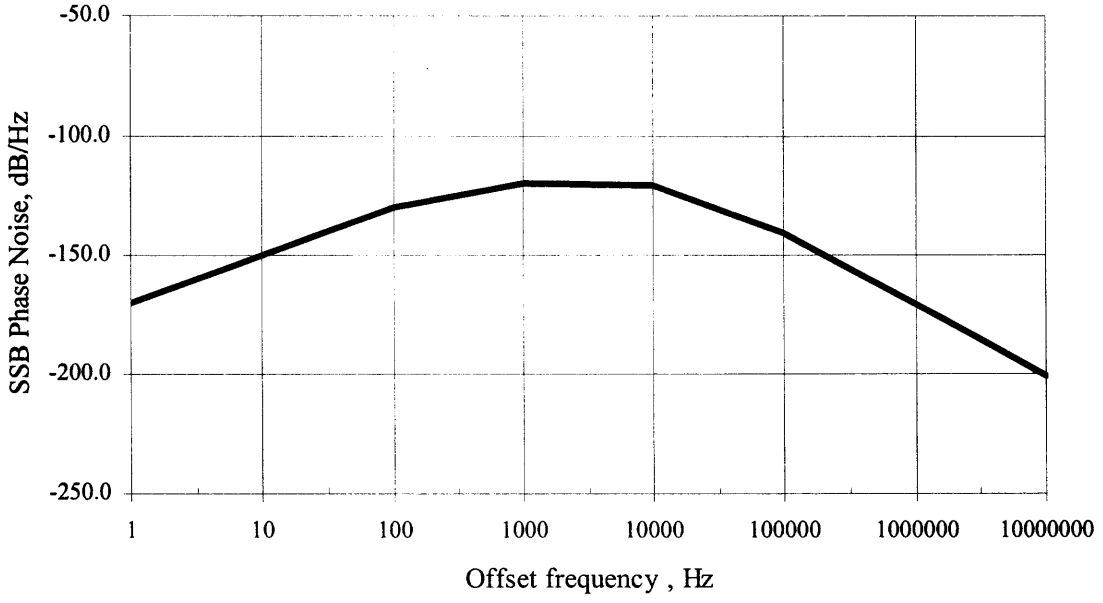


Figure 4.20 Simulated phase noise of VCO due to thermal noise of loop filter resistor.

Figure 4.21 illustrates the entry of the desired PLL parameters into the tool. The major parameters entered include the reference frequency, output frequency, and loop parameters of the PLL given in Table 4.1. This tool calculates the theoretical phase noise performance of a given PLL design. This analysis is based on the modeling approach described in [90]. The other analysis options of this program are not used in this design because more elaborate analysis on the loop is performed using the mathematical models developed and behavioral model in MATLAB.

In CPLL clock synthesizers, the phase noise is assumed to be influenced by two primary noise sources. These are the phase-frequency detector, PFD noise and VCO noise. The PFD noise is considered to be addition of white noise, which has a flat spectrum, and spurious tones. This noise is composed of noise due to reference and

divider jitter, charge-pump noise, and spurious tones of the reference frequency. The VCO phase-noise is assumed to roll off at –20 dB/decade, and is caused primarily by thermal noise sources in the ring oscillator VCO structure.

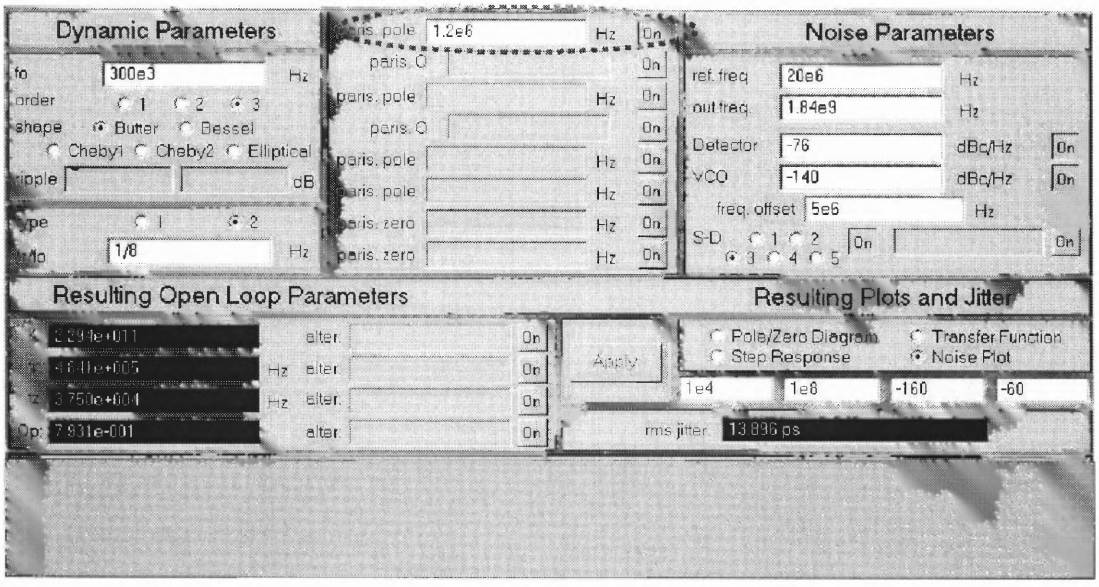


Figure 4.21 Entry of noise parameters to estimate phase noise [90].

As shown in Figure 4.18, the SPECTRE-RF simulated phase noise of the VCO has around –30 dB/decade slope in 1/f regions and –20 dB/decade in the thermal noise region, which is above 500 KHz. However, the low frequency 1/f noise is filtered out by the high-pass action of the PLL noise shaping characteristics as shown in Figure 3.13(b), before contributing the output noise of the synthesizer. The estimated phase noise response of the PLL is shown in Figure 4.22.

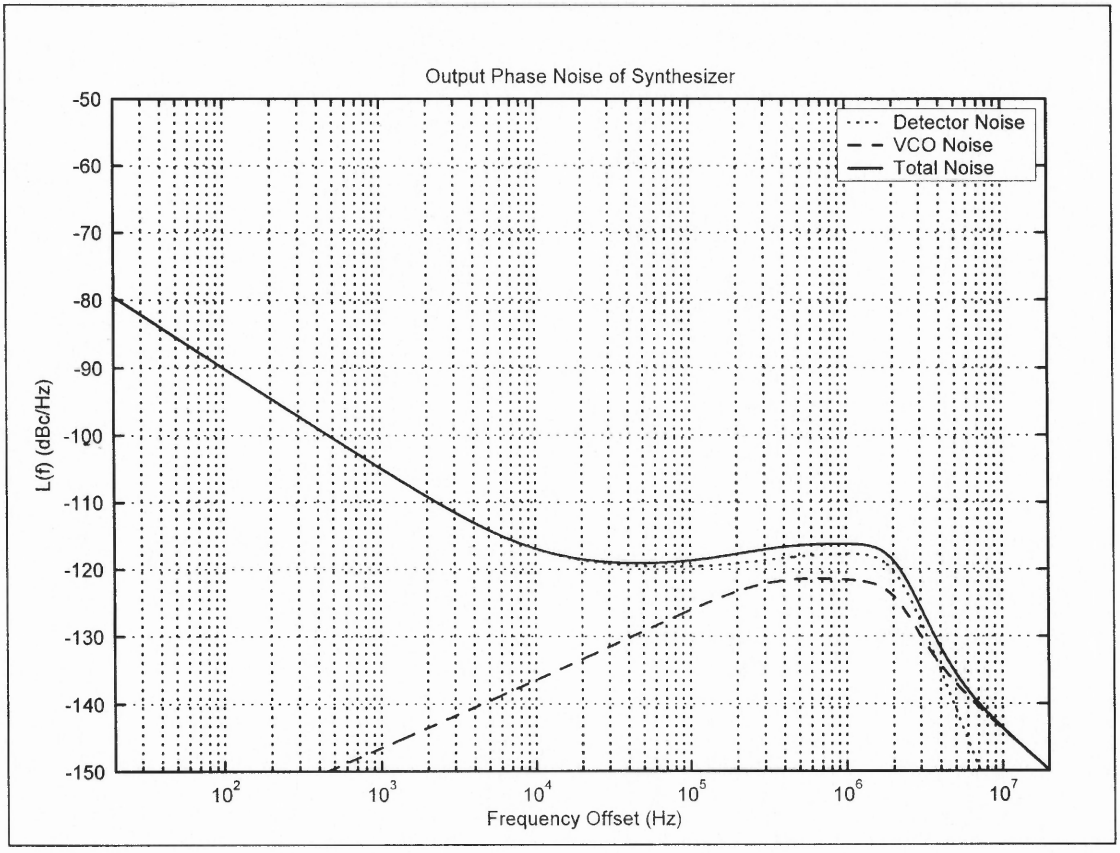


Figure 4.22 Prediction of phase noise performance of PLL at 216 MHz.

CHAPTER 5

IMPLEMENTATION OF AN EXPERIMENTAL PLL CLOCK SYNTHESIZER

5.1 Introduction

An experimental realization of the PLL clock synthesizer described in Chapter 4 was integrated in a 0.35 μm CMOS process technology with three metal layers and several resistive and capacitive devices that can be used for the implementation of on-chip passive networks such as the integrated loop filter of the PLL. The chip operates from a single supply voltage of 3.3 V. The entire PLL clock synthesizer has been integrated on a single chip including the crystal oscillator that generates the reference clock signal exhibiting a low phase noise characteristics. The crystal oscillator requires two load capacitors for the tuning of the parallel resonant circuit. These two capacitors are also integrated on the chip. The characterization setup used to test the experimental prototype is described in Appendix B.

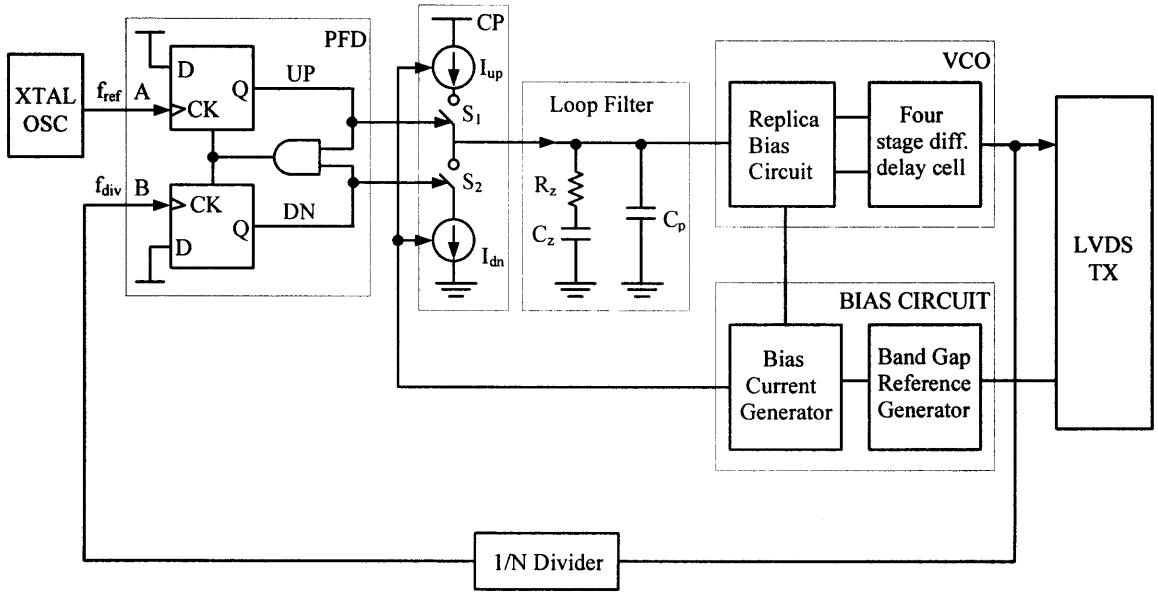


Figure 5.1 Block diagram of the experimental PLL clock synthesizer.

A block diagram of the experimental PLL clock synthesizer is shown in Figure 5.1. The circuit design blocks implemented in the experimental circuit but not shown in this figure are band-gap reference generator circuit, power-on-reset (POR) circuit, and bias circuits.

This chapter presents the description of the circuits used in the experimental PLL clock synthesizer. First, the PFD circuits are described. A brief discussion about the delay equalization at the output of the PFD circuit is discussed. Second, the charge-pump circuit is presented. The importance of the current matching and charge equalization is explained. Third, the circuit details of the loop filter network are presented. The general design of the loop filter was described in Chapter 4 but the circuit aspect of the loop filter is the subject of this chapter. Fourth, the ring oscillator VCO circuit, which is based on a differential delay cell architecture is described together with its replica bias circuit. Furthermore, the divider circuit and output buffers are described. Finally, the band-gap reference generator circuit and bias circuits used in the various circuit sections of the chip are presented.

5.2 PFD Circuit

Figure 5.2 shows the block diagram of the phase-frequency detector. Flipflops DFF1 and DFF2 are rising edge triggered D-type flipflops with their D input connected to the V_{dd}. The clock of DFF1 is connected to the reference signal, f_{ref}, and DFF2 is clocked with the output of the programmable divider in the feedback control path of the PLL, f_{div}. If the rising edge of f_{ref} arrives before the rising edge of f_{div}, the output UP is set to increase the voltage on the charge-pump loop filter and therefore speed up the VCO. Conversely, if the rising edge of f_{div} arrives prior to the rising edge of f_{ref}, DN is set to

discharge the loop filter capacitor and therefore slow down the VCO. In either condition the rising edge of the late signal resets both UP and DN. The next cycle starts with the rising edge of f_{ref} or f_{div}. The four inverters in the reset path generate enough delay to eliminate the dead zone of the charge pump [3], [6]. The selection of the number of inverters in the reset path that creates delay for the appropriate pulse width is one of the critical design parameters in PFD circuit. When the loop is locked the PFD generates narrow, coincident pulses on both UP and DN. As illustrated in Figure 4.5(c), if f_{ref} and f_{div} rise simultaneously, so do UP and DN (Q_A and Q_B), thereby activating reset. This means that even when the PLL is locked, UP and DN simultaneously turn on the charge pump for a finite period $T_{pulse} \approx 10T_D$, where T_D denotes the gate delay of one inverter and T_{pulse} is the pulse width of the reset pulse. The dead zone problem vanishes if T_{pulse} is long enough to allow UP and DN (Q_A and Q_B) to reach a valid logical level and turn on the switches S_1 and S_2 of the charge pump circuit as shown in Figure 5.1.

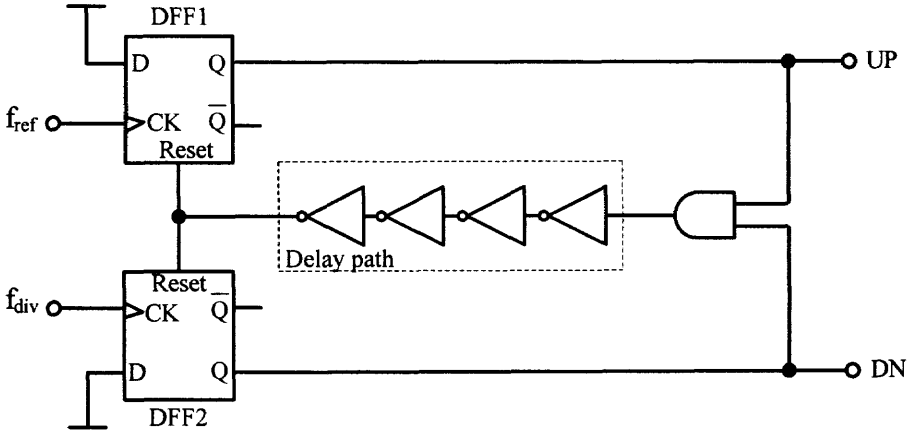


Figure 5.2 Block diagram of the phase-frequency detector (PFD).

Adding delay in the reset path can reduce the maximum operating frequency of the PFD. The maximum operating frequency in this implementation is 27 MHz and therefore the amount of the delay is not a serious problem in this implementation. In general, the maximum operating frequency is determined by the amount of time required to reset the PFD after receiving the last set of input transitions so that it is ready to detect the next set of input transitions. The gate-level implementation of the PFD is shown in Figure 5.3.

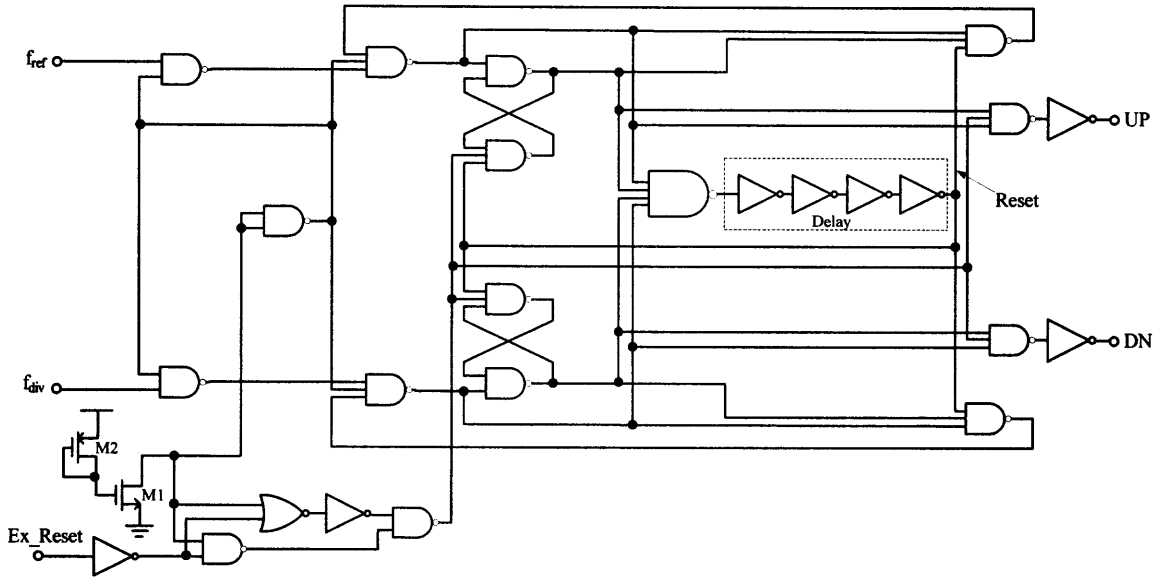


Figure 5.3 Schematic of gate level PFD with an external reset circuit.

This conventional architecture has a monotonic phase error transfer characteristic over the range of input phase error up to $-\pi - +\pi$ (2π radian) [26]. It is also insensitive to duty cycle because the PFD circuit is implemented as an edge-triggered sequential machine and circuit can change state only on the rising transitions of input signals f_{ref} and f_{div}. As illustrated in Figure 5.3, the PFD adds delay only in the output reset path by forming the outputs without including the reset signal generated by the four-input NAND

gate. Rather than obtaining the outputs from the three input NAND gates at the far right of Figure 5.3, the outputs are obtained from copies of the gates with the reset signal input deleted. The outputs are still reset, but through a slower path that includes the two NAND gates, which form the NAND gate based SR latches. Since the input reset path is unchanged, the maximum operating frequency is unaffected. The external reset circuit is required for changing the direction of the charge-pump circuit. It consists of a simple combinational logic circuit, a diode connected transistor M1, which creates a gate voltage to turn on M2 to pull down the inputs of several logic gates to ground.

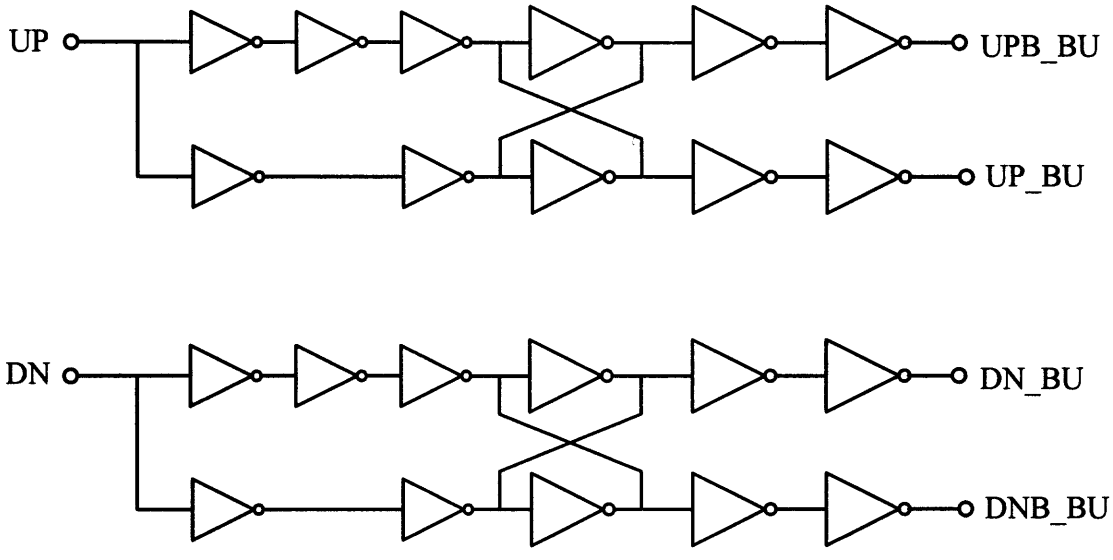


Figure 5.4 Schematic of delay matching circuit for signal path delay compensation.

The output of the phase-frequency detector is single ended and has to be converted to differential to drive the differential pairs in the charge pump circuit. This is achieved by driving charge-pump inputs by a complementary circuit shown in Figure 5.4. This circuit consists of odd and even number of inverter chains to match delays over process variations. An alternative approach for delay matching is to use a complementary clock generated by Shoji's delay balanced chain [98].

5.3 Charge Pump Circuit

Figure 5.5 shows the charge pump circuit using eight switches and two cascoded current sources. The key design issues in the charge pump circuit are the reduction of jitter and spurs due to the current mismatch and charge transfer transient during the switching transient between up and down currents I_{up} and I_{dn}. Design for high power supply noise rejection is also a challenging design area. The up current I_{up} and the down current I_{dn} are produced using a wide swing cascode current mirror in order to obtain better power supply noise rejection. Transistors M3, M5, M6, M8, and M9 make up the wide swing current mirror using NMOS devices. The basic idea of this type of current mirror is to bias the drain-source voltages of transistors M6 and M9 to be close to the minimum possible without allowing them into the triode region [96]. Similarly, transistors M7, M10, M11, M14, and M15 make up the second wide swing current mirror using PMOS devices.

In a standard charge pump PLL as shown in Figure 5.1, the lock mode PFD generates narrow identical pulses at both outputs UP and DN, which enable the sink and source current of the charge pump simultaneously. Since both currents are of equal amplitude and width, the net effect on the output voltage is zero. However, several spikes occur on the output when currents are switched on and off and these will modulate the VCO if no precautions are taken. These spikes occur at the reference frequency and cause spurs in the output spectrum of the PLL at an offset from the carrier equal to this reference frequency. Eight analog switches are used instead of four to reduce the reference spurs problems [97]. The four switches in the left branch of the charge pump

circuit of Figure 5.5 are used for this purpose. The UPB_BU and DNB_BU signals are the polarity-reversed UP_BU and DN_BU signals, respectively.

These inverters used in Figure 5.4 require careful consideration of the signal path delay compensation. The loop filter (LF) experiences a finite transient at each phase comparison instant because of charge sharing between LF, sink, and source current, parasitic capacitors and charge injection mismatching of analog switches $(MN2, MP2)$ and $(MN4, MP4)$. The opamp, $OP1$, reduces the transients caused by the charge transfer during switching instants [6].

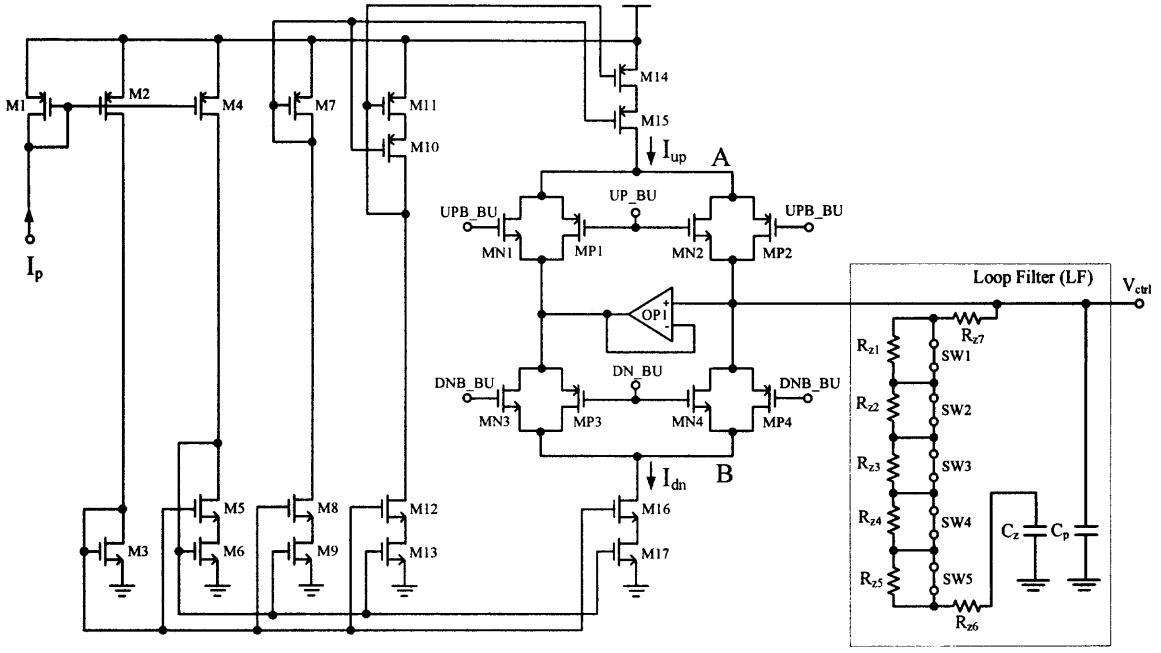


Figure 5.5 Schematic of the charge pump circuit and loop filter network.

Switches, $SW1$ through $SW5$, are used for switching of the loop filter resistor, $R_z = R_{z1} + R_{z2} + ...R_{z7}$. This provides the PLL with a dynamically changing damping factor during each programming step so that they guarantee the stability of the PLL. Since five programming steps exist in this design, $N = \{2,3,4,6,8\}$, $SW1$ is needed for

the divider ratio $N=2$, $SW2$ is needed for the divider ratio $N=3$, and so on. These switches are implemented as the transmission gates and shown in Figure 5.7. The transistor sizes for the charge pump circuit are summarized in Table 5.1. The capacitor and resistor sizes are summarized in Table 5.2. The resistors R_{z1} through R_{z7} are polysilicon resistors with a resistivity of around $50\Omega/\square$ (50 ohms per square). The tolerance of these poly resistors are about 25% over process variations, and the temperature coefficient, defined as

$$TC = \frac{1}{R} \cdot \frac{\partial R}{\partial T} \tag{5.1}$$

depends on doping and composition, and is typically $800 ppm/^{o}C$ for the 0.35 μm CMOS process technology [92] used for the implementation of the PLL clock synthesizer. The loop filter capacitors are made of NMOS devices and have a unit capacitance of around $4.5 fF/\mu m^2$. The charge-pump current, I_p is $80\mu A$ in this design and this current is mirrored from the bias current generator.

Table 5.1 Transistor Sizes in the Charge Pump Circuit

Transistor	**Size (μm)**	**Transistor**	**Size (μm)**
M1, M2	100/2	M12, M13	300/1.5
M3	45/1.5	M14, M15	600/1.5
M4	100/2	M16, M17	300/1.5
M5, M6	300/1.5	MN1, MP1	3/0.35
M7	90/1.5	MN2, MP2	3/0.35
M8, M9	300/1.5	MN3, MP3	3/0.35
M10, M11	600/1.5	MN4, MP4	3/0.35

The NMOS and PMOS wide-swing cascade mirrors described above generates the charge-pump's charge and discharge currents, I_{up} and I_{dn}.

Table 5.2 Resistor and Capacitor Sizes in the Charge Pump Circuit

Resistor	**Size**	**Capacitor**	**Size**
R_{z1}	500 Ω	C_z	250 pF
R_{z2}	500 Ω	C_p	15 pF
R_{z3}	500 Ω		
R_{z4}	500 Ω		
R_{z5}	500 Ω		
R_{z6}	800 Ω		
R_{z7}	800 Ω		

The schematic of *OP*1 is shown in Figure 5.6. This circuit is of a single stage operational amplifier (opamp) circuit architecture. The single-stage refers to the number of gain stages in the opamp. The gain stage is a differential input single ended output stage. No output buffer is needed at the output because *OP*1 drives high impedance nodes as shown in Figure 5.5. Since this opamp is a single stage circuit, the phase margin is 90° at the gain crossover frequency. Therefore, no compensation circuit is needed to ensure the stability of the amplifier. PMOS transistors M1 and M2 are used differentially at the input of the opamp to allow higher common mode levels at the charge pump circuit. NMOS transistors, M3 and M4, constitute an n-channel current mirror active load. The small signal DC gain of the opamp is no more than 30-dB over process variations but this much gain is enough for the successful operation of the opamp in the charge pump circuit. The transistor sizes of *OP*1 are summarized in Table 5.3.

Table 5.3 Transistor Sizes in the Opamp, *OP*1 of Figure 5.6

Transistor	Size (μm)	Transistor	Size (μm)
M1	320/1.0	M5	320/1.6
M2	320/1.0	M6	80/1.6
M3, M4	30/2.0	M7	10/3.0

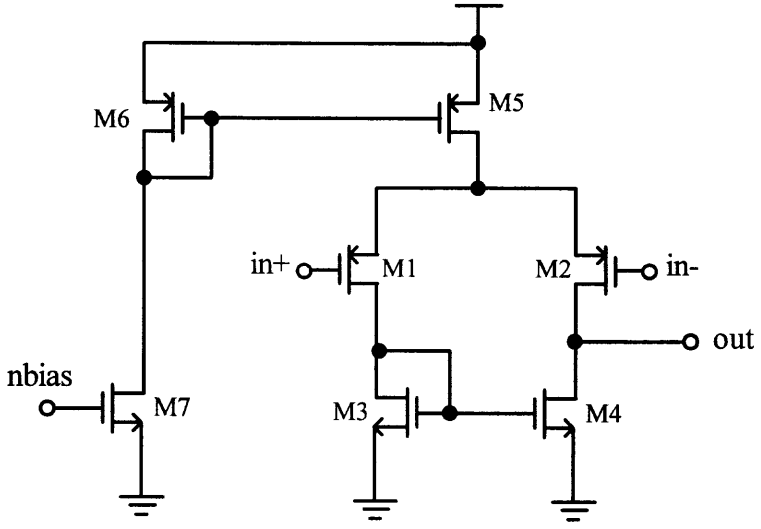


Figure 5.6 Schematic of opamp, *OP*1, used in the charge pump circuit.

The transistor sizes of the transmission gate are summarized in Table 5.4. The sizes of NMOS and PMOS transistor are chosen properly to reduce the on-resistance of the transmission gate, *TGATE*. The on-resistance of the *TGATE* is around $1.0k\Omega$ in this application.

Table 5.4 Transistor Sizes in the Transmission Gate of Figure 5.7

Transistor	Size (μm)	Transistor	Size (μm)
M1	20/0.35	M2	20/0.35

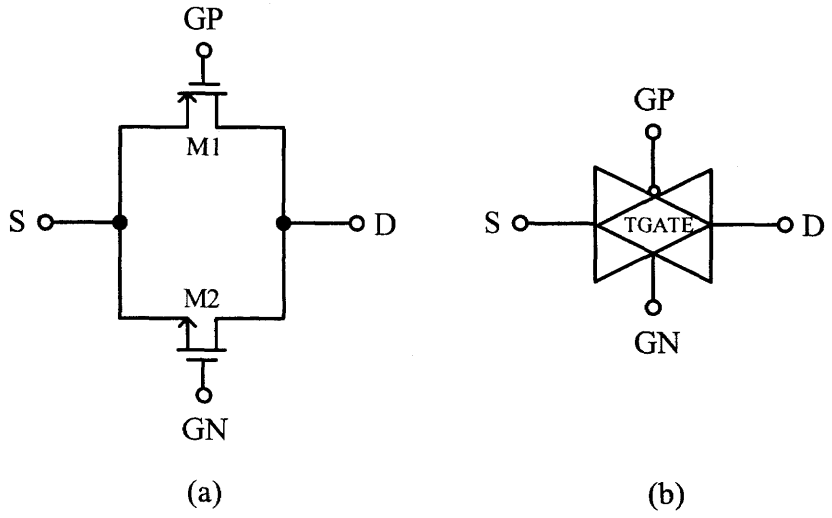


Figure 5.7 CMOS transmission gate used in the LF (a) schematic (b) symbol.

As shown in Figure 5.5, the nodes A and B experience different voltage swings during each charge pump cycle if the opamp, $OP1$, is not used between analog switches in a bridge configuration. When the switches are off, the sink and source currents pulls the drain of MP2 and MN4 to V_{dd} and V_{ss}, respectively. After the switches are turned on while the loop is at locked condition, the voltage at the drains of MP2 and MN4 increases/decreases from V_{dd} and V_{ss} toward the loop filter voltage held by PLL. At this point, both MP2 and MN4 are in triode region until the voltage at the drain of MP2 and MN4 is higher than the minimum saturation voltage. As a result, it will cause current mismatching at the output due to the different recovery time on each of the nodes and leads to the reference spur in the VCO.

This new circuit architecture shown in Figure 5.5 solves the problem of the charge sharing between the drain of MP2, MN4 and LF, when the switch is turned back on by using a unity gain amplifier and a dummy load, i.e., transistors (MN1, MP1) and (MN3, MP3). For instance, when the charge pump circuit is sinking current from the loop filter

the other current source is set by a dummy load with the same voltage at the LF as illustrated in Figure 5.5.

The current mismatch between the up and down currents I_{up} and I_{dn} is a critical performance parameter to minimize the jitter and spurious tones at the PLL output. Figure 5.8 shows the simulated systematic mismatch between the up and down currents as a function of the charge-pump output voltage, V_{ctrl}, as shown in Figure 5.5. The percentage error for $0.55V \leq V_{ctrl} \leq 2.65V$ is less than 0.5% and increases to large percentage values beyond this limit as shown in Figure 5.8.

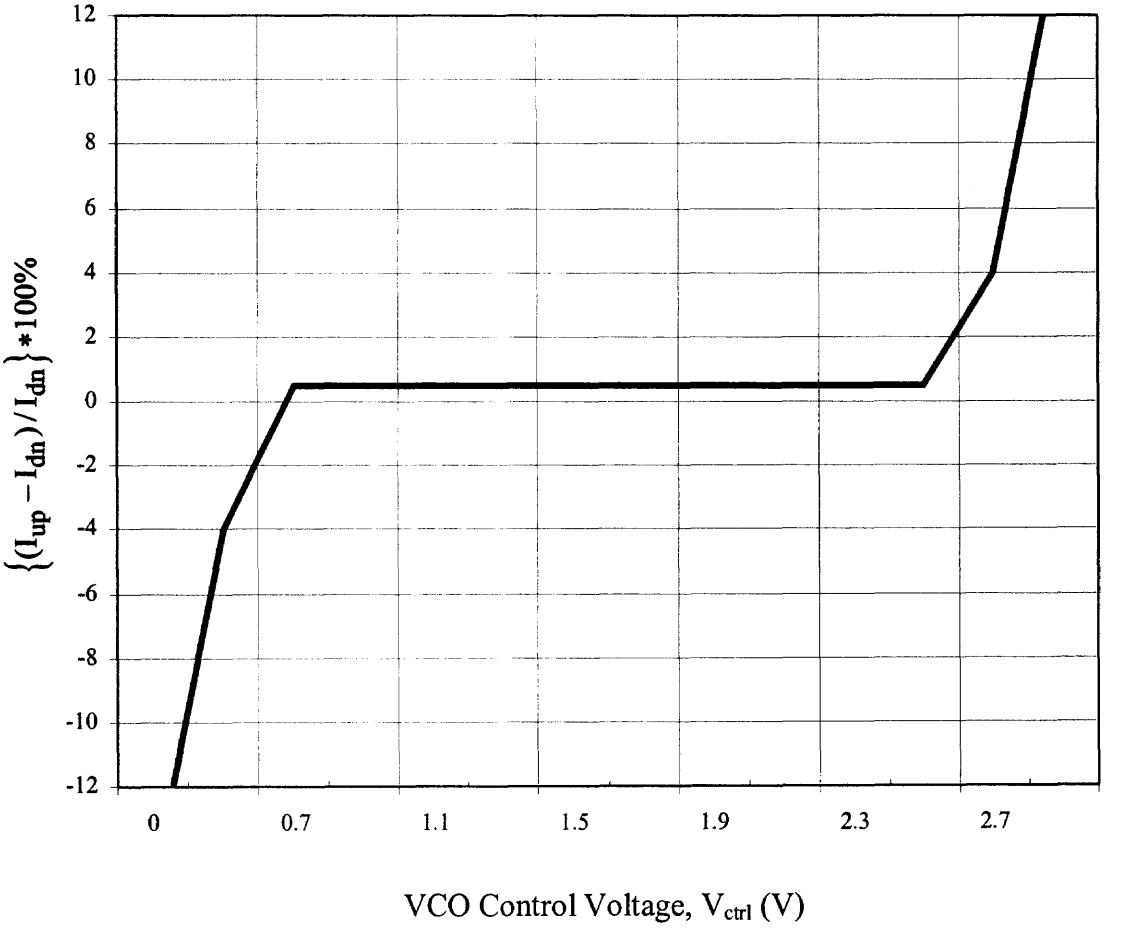


Figure 5.8 Systematic error between up and down currents as a function of V_{ctrl}.

5.4 VCO and Replica Bias Circuit

The block diagram of the four-stage ring oscillator VCO was presented in Chapter 4. It is repeated here for the transistor level description of the individual cells, as shown in Figure 5.9

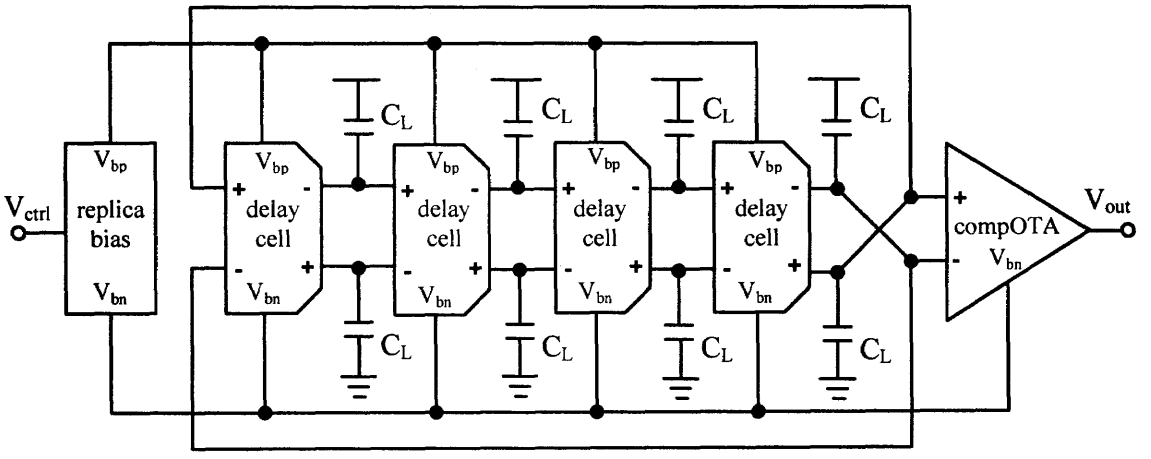


Figure 5.9 Block diagram of a four-stage ring oscillator VCO with replica bias circuit.

The low phase noise requirement of the PLL clock synthesizer is achieved by the use of a differential delay cell shown in Figure 5.10.

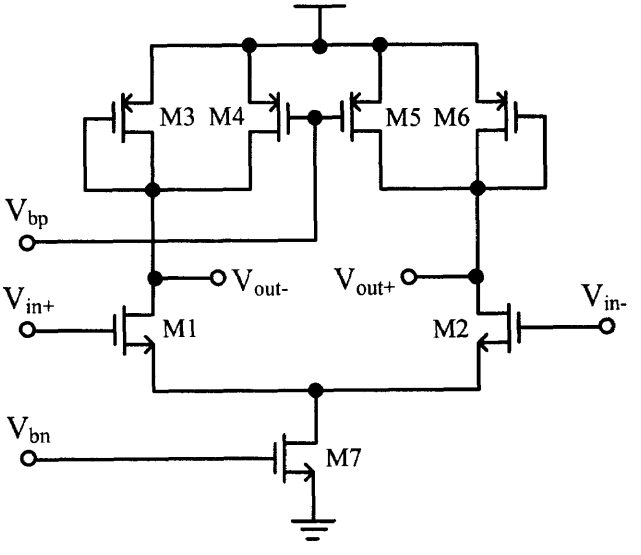


Figure 5.10 Schematic of the differential delay cell.

The differential delay cell, shown in Figure 5.10, contains a source coupled NMOS pair, M1 and M2 with PMOS resistive symmetric-load elements (M3, M4 and M5, M6). The bias voltage of the symmetric loads V_{bp} is nominally equal to the control voltage of the VCO, V_{ctrl}, which is applied to the replica bias circuit to produce the bias voltages, V_{bn} and V_{bp} of the differential delay cell. V_{bp} defines the limit of lower voltage swing of the delay cell outputs. The NMOS current source, M7, is dynamically biased with V_{bn} to compensate for drain and substrate voltage variations, achieving the effective performance of a cascade current source [28].

Figure 5.11 shows the schematic of the replica bias generator. This circuit produces the bias voltages of the differential delay cell, V_{bn} and V_{bp} from V_{ctrl}.

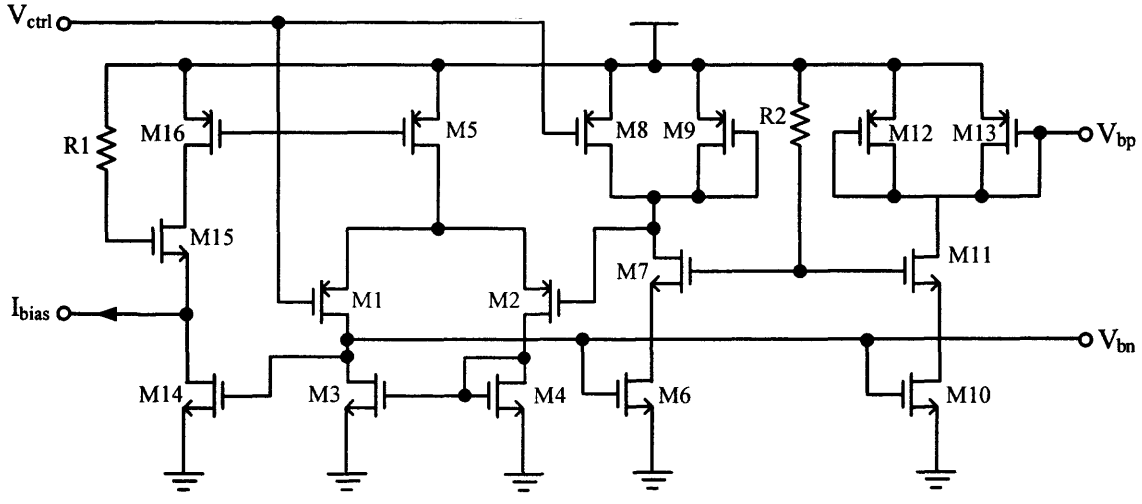


Figure 5.11 Schematic of replica bias circuit.

The primary function of the replica bias circuit is to continuously adjust the bias current of the differential delay cell of Figure 5.10 in order to provide the appropriate lower swing limit of V_{ctrl} for the delay cell stages of Figure 5.9. Therefore, it establishes a

current that is held constant and independent of the supply voltage. It performs this function by using a single-stage differential amplifier, which consists of transistors M1 through M5. The bandwidth of the replica bias circuit is set equal to the operating frequency of the differential delay cells so that the replica bias generator can track all of the power supply and substrate disturbances at frequencies that can affect the PLL. The bias current for this circuit is partly provided by the self-bias source of M14, and mostly by the input current source, I_{bias}. Since the bias generator that produces I_{bias} includes a start up circuit, the replica bias circuit doesn't need an additional one. The replica bias circuit also provides a buffered version of V_{ctrl} at the V_{bp} output using an additional half-buffer replica circuit, which includes transistors M10 through M13.

The transistor sizes for the differential delay cell and replica bias generator are summarized in Table 5.5 and Table 5.6, respectively.

Table 5.5 Transistor Sizes in the Differential Delay Cell of Figure 5.10

Transistor	**Size (μm)**	**Transistor**	**Size (μm)**
M1, M2	60/0.6	M5, M6	20/0.6
M3, M4	20/0.6	M7	200/2

Table 5.6 Transistor and Resistor Sizes in the Replica Bias Circuit

Transistor	**Size (μm)**	**Transistor**	**Size (μm)**
M1, M2	80/2	M8, M9	20/0.6
M3, M4	80/4	M12, M13	20/0.6
M5, M16	60/4	M14	2/50
M6, M10	200/2	M15	20/4
M7, M11	60/0.6	R1, R2	~250 Ω

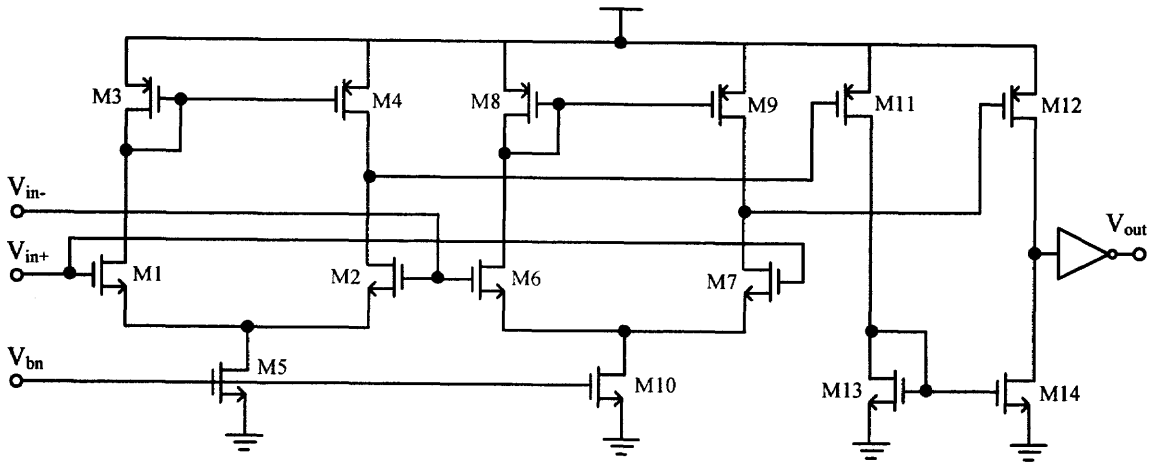


Figure 5.12 Schematic of compOTA with differential to single-ended converter.

Since a 50% duty cycle is required at the PLL output, a careful design for the comparator and differential to single-ended converter is required. Figure 5.12 shows the schematic of such circuit. This circuit consists of two opposite operational transconductance amplifiers (OTA), which drive two PMOS common-source amplifiers, M11 and M12, connected by an NMOS current mirror consisting of M13 and M14. The OTAs are constructed from the differential delay cell stages using the same NMOS current source bias voltage V_{bn}. These two OTAs provide signal amplification and a DC bias point for the PMOS common-source amplifiers. The PMOS current source amplifiers of M11 and M12 provide additional signal amplification and conversion to a single ended output through the NMOS current mirror of M13 and M14. In this circuit, since the two levels of amplification are differentially balanced with a wide bandwidth, the opposing differential input transitions have equal delay to the output. In high frequency design, this circuit is preferred over a divide-by two circuit for generating signals with a 50% duty cycle at the output because this operation is performed at a lower frequency and therefore dissipates less power. The transistor sizes for the compOTA circuit are summarized in Table 5.7.

Table 5.7 Transistor Sizes in the CompOTA Circuit

Transistor	Size (μm)	Transistor	Size (μm)
M1, M2	30/0.6	M8, M9	20/0.6
M3, M4	20/0.6	M11, M12	20/0.6
M5, M10	30/0.6	M13	30/0.6
M6, M7	30/0.6	M14	30/0.6

5.5 Feedback Divider Circuit

Figure 5.13 shows the basic divider circuits used in the feedback divider of the PLL clock synthesizer. D-type flip-flops are connected together to form mod-2, mod-4, mod-6, and mod-8 counters [99], [100], [101].

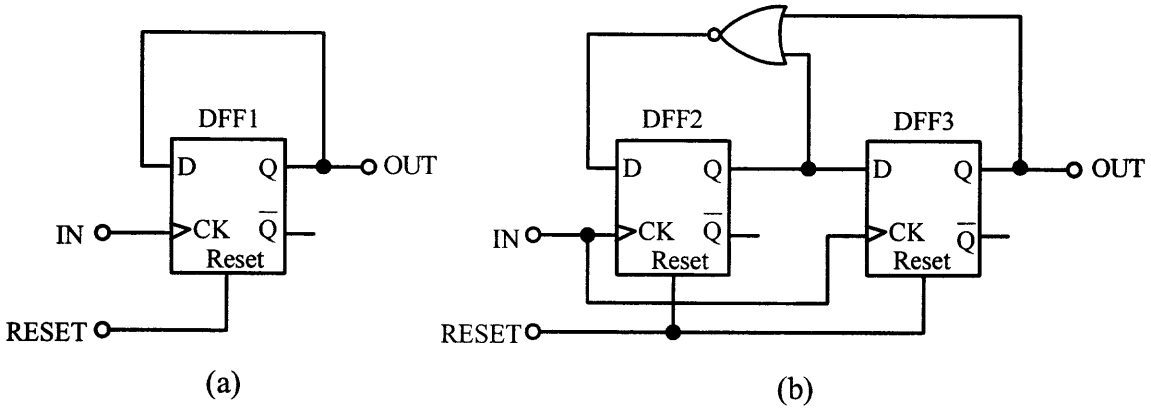


Figure 5.13 Schematic of divider circuits (a) divide by 2 (b) divide by 3.

The basic divider circuits shown in Figure 5.13 are used to program the feedback divider with divider ratios of $N = \{2,3,4,6,8\}$. For example, if the divider ratio of $N = 4$ is needed, mod-4 counter is built using a cascade of the two of the divide by 2 circuit shown in Figure 5.13(a). Similarly, if $N = 6$ is the selected divider ratio, then the divide

by 2 circuit shown in Figure 5.13(a) and divide by 3 circuit shown in Figure 5.13(b) are cascaded. The feedback divider circuit also includes the circuitry required to control the transmission gates (switches) across the resistors, $R_{z1}, R_{z2}, ..., R_{z7}$, of the charge pump circuit. This control circuit is a simple combinational logic realized using logic gates.

5.6 Band Gap Voltage Reference and Bias Circuits

A robust band gap reference circuit is designed using the parasitic bipolar transistors in 0.35 μm CMOS process technology. Figure 5.14 shows the schematic of the band gap reference circuit. The proportional to absolute (PTAT) bias current is produced using Q1, Q2, OP2, and cascode current mirror, which consists of transistors M1 through M7. The circuit that includes M11, M12, and M13 are the start up for the band gap generator.

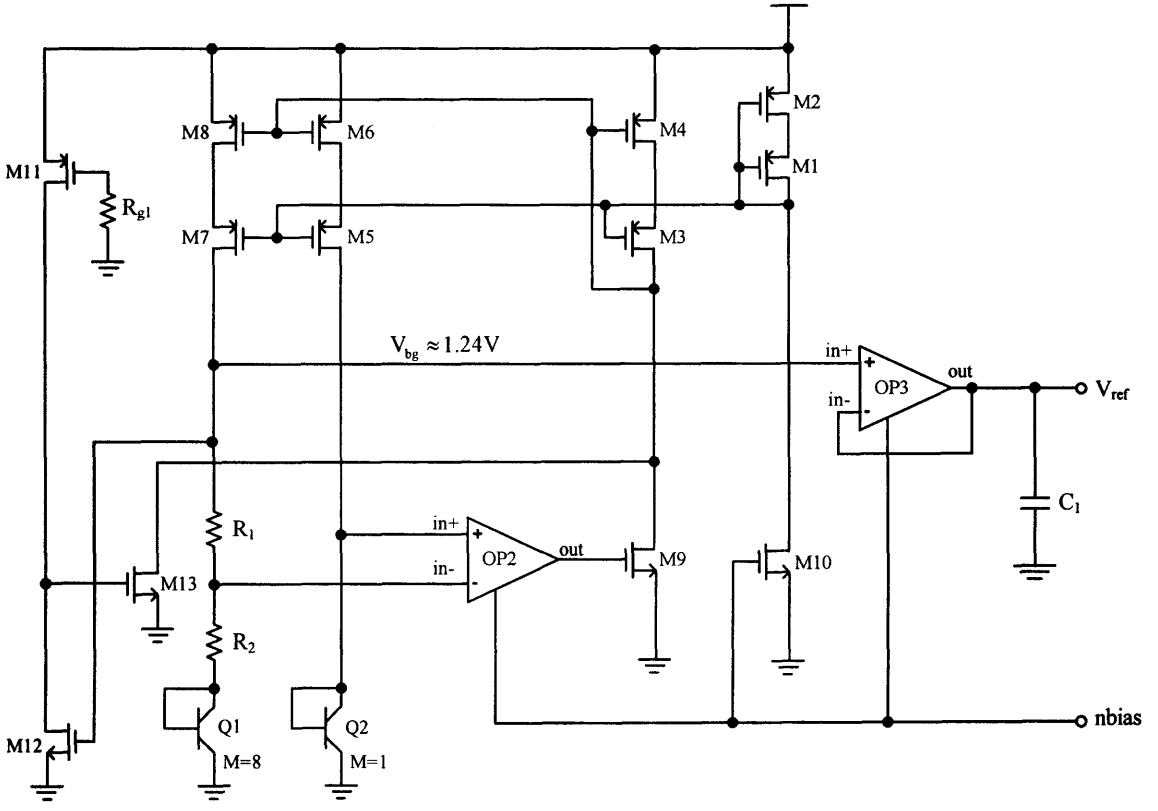


Figure 5.14 Schematic of a temperature independent bandgap voltage circuit.

The transistor and resistor/capacitor sizes for the band gap reference circuit are summarized in Table 5.8 and Table 5.9, respectively. The unity gain amplifier using OP3 is a buffer circuit that buffers the band gap reference voltage, V_{bg}, and outputs V_{ref} voltage. The schematic of OP2 and OP3 is shown in Figure 5.15. OP2/OP3 is a folded cascode operational transconductance amplifier (OTA) with PMOS input transistors. This architecture is preferred because of its larger DC gain and larger bandwidth [96]. The bias currents for the operational amplifiers, OP2 and OP3 are mirrored from a supply independent circuit shown in Figure 5.16. The transistor sizes for OP2/OP3 circuit are summarized in Table 5.10.

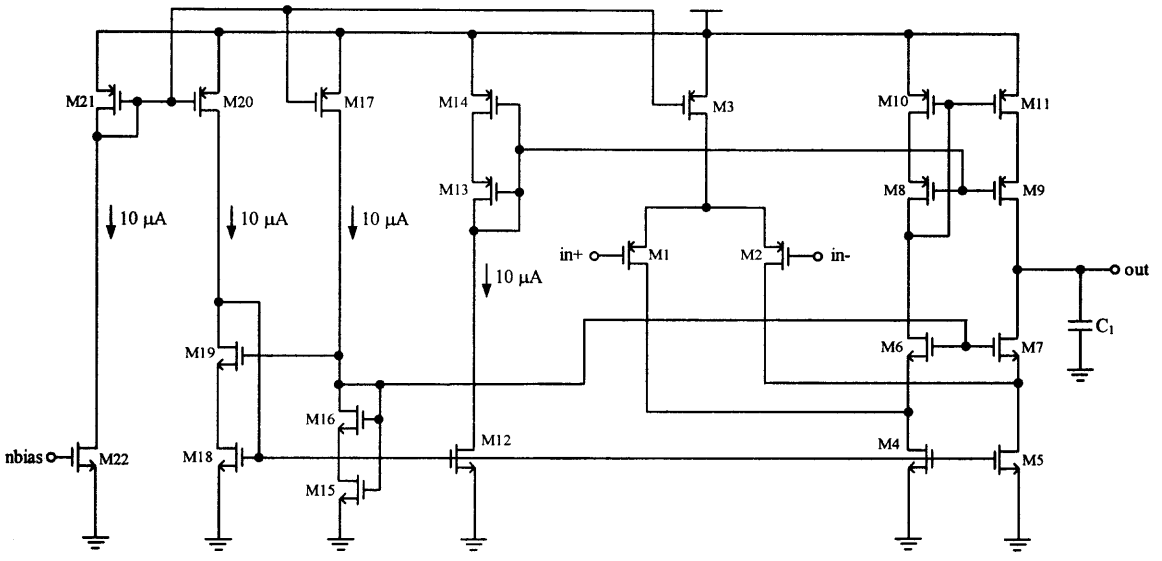


Figure 5.15 Schematic of the folded cascode operational amplifier, OP2/OP3.

Table 5.8 Resistor and Capacitor Sizes in the Bandgap Reference Circuit

Resisistor	**Size (µm)**	**Capacitor**	**Size (µm)**
R1	50 kΩ (poly)	C1	20 pF (gate)
R2	5 kΩ (poly)		

Table 5.9 Transistor Sizes in the Bandgap Reference Circuit

Transistor	Size (μm)	Transistor	Size (μm)
M1	20/5	M9	1/5
M2	10/5	M10	50/5
M3, M4	80/5	M11	1/50
M5, M6	80/5	M12	12/1.2
M7, M8	80/5	M13	1/10

Figure 5.16 illustrates a supply independent bias circuit. The reference current, I_{ref}, is derived from the output current I_{out}. The idea of designing this circuit is that if I_{out} is to be independent of the supply voltage, V_{dd}, then I_{ref} can be a replica of I_{out}. Figure 5.16 shows an efficient way of how I_{out} is copied using transistors M3, M4, M5, and M6 to define I_{ref}. With the sizes chosen in Figure 5.16, the output current is $I_{out} = K \cdot I_{ref}$. Several circuits mirror current references from this circuit using *nbias* and *pbias* as well as the current source I_{out}. The source coupled NMOS pair, M8 and M9 is used as a start up circuit together with other devices around them. Transistors M11, M12, and M13 create a threshold voltage, which initially turns on M8. M8 pulls down the gate of M5 to the ground to allow a current to flow and start the bias circuit at the power up.

As the voltage on node Y rises, due to the differential nature of the NMOS pair, M8 and M9, the current is steered to the other branch, i.e., to the drain of M9 and therefore the transistor M8 gets disconnected from the node X. The resistors R_1 and R_2 are two distinct resistors. R_1 is a poly-silicon resistor with positive temperature coefficient while R_2 is an n-well resistor with a negative temperature coefficient. The

objective here is to cancel out the resistance change over process and temperature variations. The transistor and resistor/capacitor sizes for the supply independent bias circuit are summarized in Table 5.11 and Table 5.12, respectively.

Table 5.10 Transistor and Capacitor Sizes in the Opamp OP2/OP3

Transistor	Size (μm)	Transistor	Size (μm)
M1, M2	160/1	M14	8/4
M3	100/2	M15	4/4
M4, M5	40/2	M16	10/1
M6, M7	30/1	M17, M20, M21	50/2
M8, M9	20/2	M18	20/2
M10, M11	20/1	M19, M22	30/1, 100/5
M12, M13	20/2	C_1	40 .(25/10)

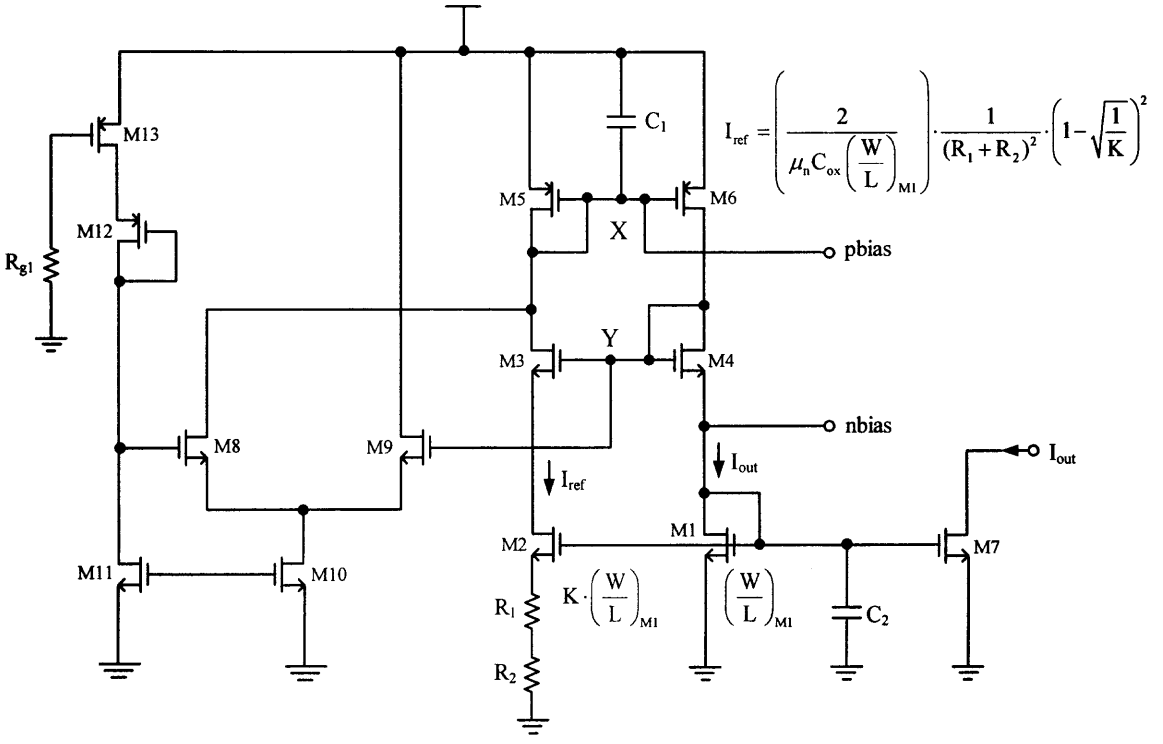


Figure 5.16 Schematic of the supply-independent bias circuit.

Table 5.11 Transistor Sizes in Supply-independent Bias Circuit

Transistor	Size (μm)	Transistor	Size (μm)
M1	200/5	M7	125/5
M2	50/5	M8, M9, M10, M11	10/1
M3, M4	125/5	M12	5/5
M5, M6	50/5	M13	10/4

Table 5.12 Resistor and Capacitor Sizes in Supply-independent Bias Circuit

Resisistor	Size (μm)	Capacitor	Size (μm)
R1	4 kΩ (poly resistor)	C1	1 pF (poly plate)
R2	2.2 kΩ (well resistor)	C2	1 pF (poly plate)

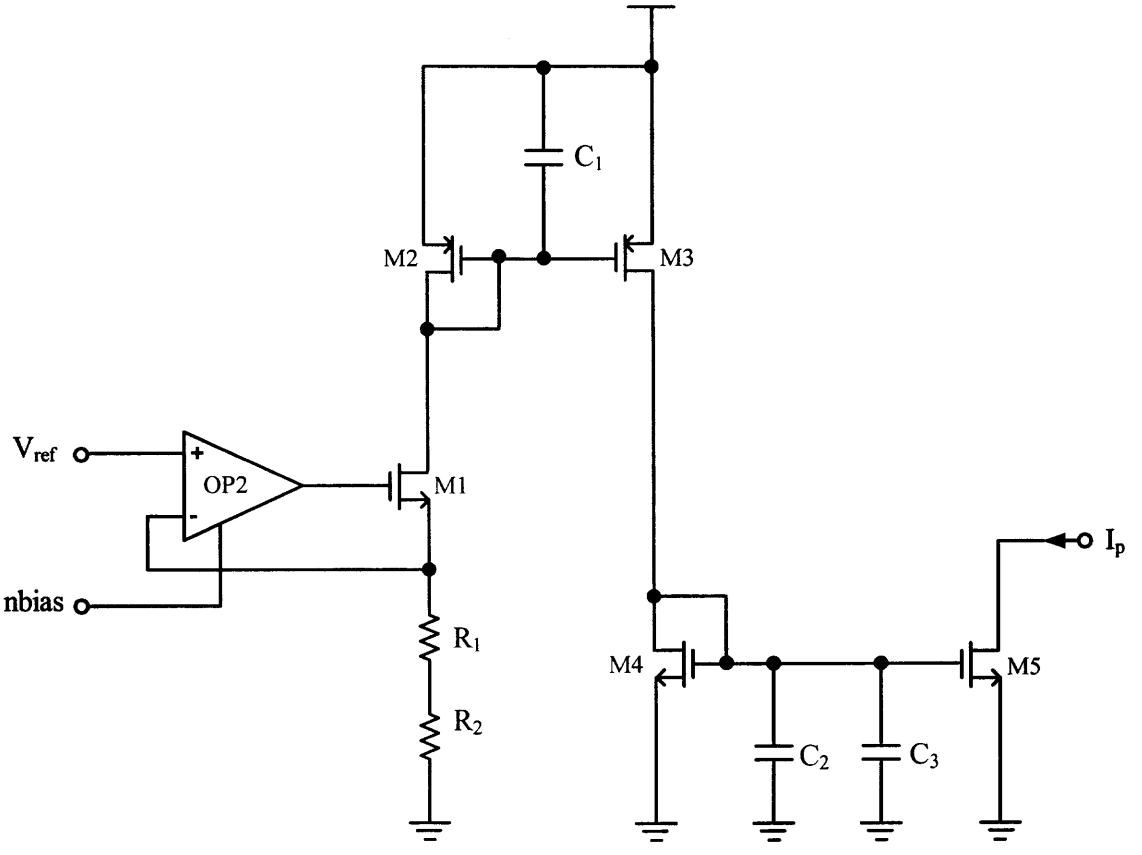


Figure 5.17 Schematic of $V-I$ converter.

Figure 5.17 illustrates a voltage-to-current converter circuit. The function of this circuit is to create the input current of the charge pump circuit from a stable band gap reference output of Figure 5.14. The unity gain amplifier around OP2, M1, R_1, and R_2 constitute a V-to-I converter, which takes the band gap output voltage, V_{ref}, as the reference voltage input and produces the current source of the charge pump circuit, I_p. The transistors M2 and M3 as well as M4 and M5 are current mirror circuits to be used to create the charge pump current. The transistor and resistor/capacitor sizes for the V-I converter are summarized in Table 5.13 and Table 5.14, respectively.

Table 5.13 Transistor Sizes in the V-I Converter Circuit

Transistor	**Size (μm)**	**Transistor**	**Size (μm)**
M1	200/2	M4	40/4
M2	320/2	M5	80/4
M3	80/2		

Table 5.14 Resistor and Capacitor Sizes in the V-I Converter Circuit

Resisistor	**Size (μm)**	**Capacitor**	**Size (μm)**
R_1, R_2	3.2 kΩ (poly resistor)	C_2	1 pF (poly plate)
C_1	1 pF (poly plate)	C_3	1 pF (poly plate)

5.7 Crystal Oscillator Circuit

Figure 5.18 shows the crystal oscillator circuit. The transistors M1 and M2 make up a CMOS inverter, which is required for the negative-g_m at the input to cancel out losses in the tank circuit. This is a Pierce oscillator in which a crystal is connected in the feedback

loop so that the circuit oscillates at the parallel resonance frequency of the crystal. The two load resistors C_1 and C_2 are used to pull the frequency of oscillation to the desired value. Resistors R_1 and R_2 are used for the gate protection of the CMOS inverters. The CMOS inverters, which are made out of M3 and M4 as well as M5 and M6 create a buffer to distribute the reference clock source. The circuit diagram of the crystal oscillator illustrates the model for the crystal tank circuit. This model is important to design and simulate the oscillator circuit. The output signal, *OSCOUT*, is a very low phase noise output, which is the input reference clock of the PLL clock synthesizer. The transistor and resistor/capacitor sizes for the V-I converter are summarized in Table 5.15 and Table 5.16, respectively.

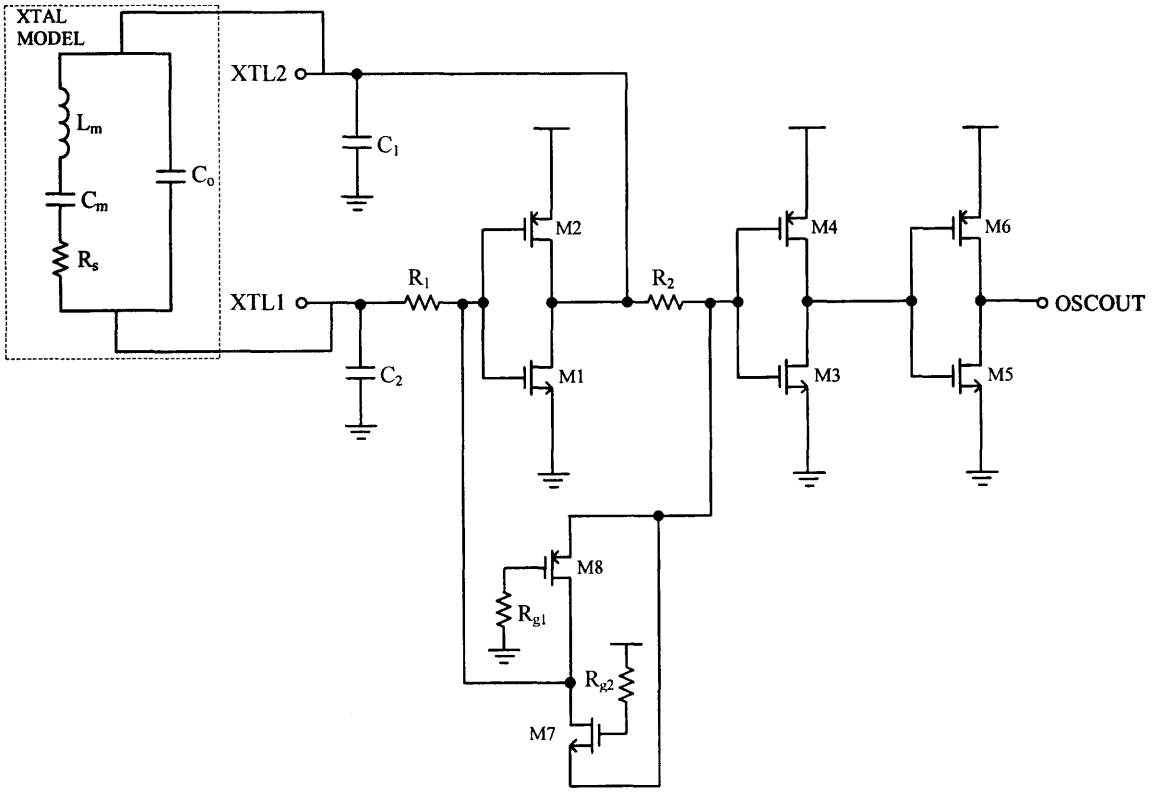


Figure 5.18 Schematic of the crystal oscillator circuit.

Table 5.15 Transistor Sizes in the Crystal Oscillator Circuit

Transistor	Size (μm)	Transistor	Size (μm)
M1	700/1	M5	9/1
M2	300/1	M6	21/1
M3	3/1	M7, M8	0.8/20
M4	7/1		

Table 5.16 Resistor and Capacitor Sizes in the Crystal Oscillator Circuit

Resisistor	Size (μm)	Capacitor	Size (μm)
R_1, R_2	1 kΩ (poly resistor)	C_1	2 . (50/50)
R_{g1}, R_{g2}	250 Ω (diffusion resistor)	C_2	2 . (50/50)

5.8 *LVDS Transmitter Circuit*

Figure 5.19 shows the low signal differential signaling (LVDS) transmitter circuit that is used as an output buffer with an 50 Ω output impedance (100 Ω differentially).

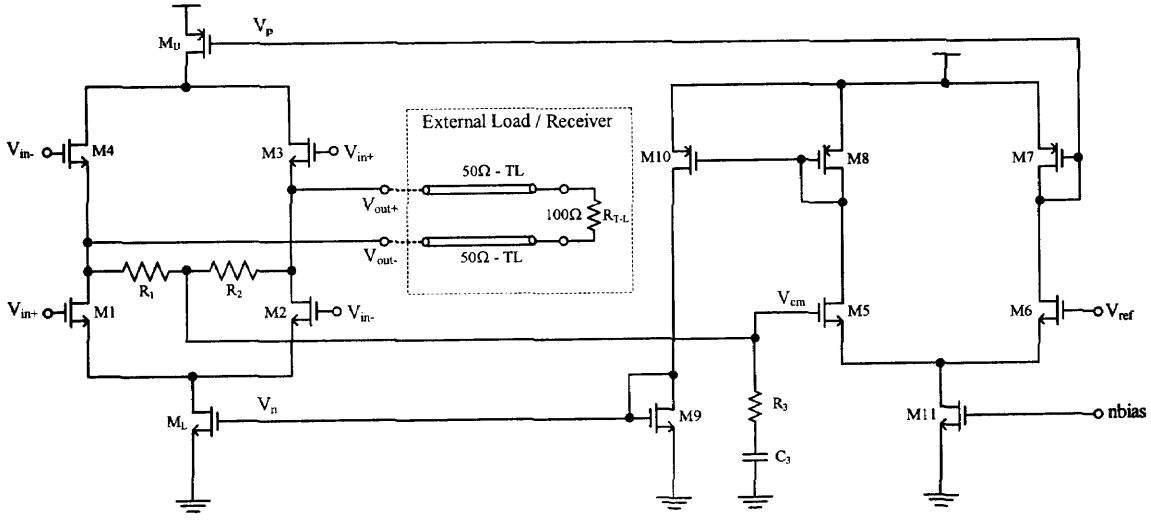


Figure 5.19 Schematic of LVDS transmitter circuit.

A typical LVDS transmitter behaves as a current source with switched polarity. The output current flows through the external load resistance, establishing the required differential output voltage swing. This design employs a standard LVDS transmitter configuration with four MOS switches consisting of M1 through M4, in bridge configuration as shown in Figure 5.19. When M1 and M3 are turned on, the polarity of the output current and voltage are both positive. If M1 and M3 are turned off, then the polarity of the output waveforms will be reversed. With a nominal 100-Ω load at the receiver, both the common mode voltage and differential swing at the output have to comply with the LVDS standard specifications [103], [104] over the full range of process, supply voltage 3.0-3.6V, temperature –40 °C-125 °C (PVT) variations:

$$250mV \le |V_{od}| \le 450mV \tag{5.2}$$

$$1.125V \le |V_{CM}| \le 1.375 \tag{5.3}$$

where V_{od} and V_{CM} are the differential output and the common mode voltages at the transmitter output, respectively.

In order to achieve higher precision and lower circuit complexity, a simple low-power common-mode-feedback control (CMFB) was implemented in the transmitter as shown in Figure 5.19. For this purpose, the band gap reference voltage, V_{ref}, is used as the reference level and compared with the common mode level using a differential amplifier. The common mode level of the LVDS output is obtained using a resistive network. High value resistors are used at the output in order not to load the output.

The two $100k\Omega$ resistors, R_1 and R_2, at the output of the switch circuit is used to sample the common mode level of the output and that signal is fed back to the differential amplifier, which consists of a source-coupled NMOS pair, M5 and M6 as well as diode connected loads, M7 and M8. The diode-connected transistors, M7 and M8, also generate the tail currents of the LVDS transmitter. Although the transistor M_L mirrors current from a buffer circuit using M9, the PMOS current source, M_U, mirrors directly from M7. The tail current in this application is nominally 4.0 mA, which creates around 400 mV of a differential voltage on a 100 Ω load. The transistor and resistor/capacitor sizes for the LVDS transmitter are summarized in Table 5.17 and Table 5.18, respectively.

Table 5.17 Transistor Sizes in the LVDS Transmitter Circuit

Transistor	**Size (μm)**	**Transistor**	**Size (μm)**
M1, M2	100/0.6	M5, M6	160/0.6
M3, M4	150/0.6	M7, M8	40/0.6
M_L	1200/0.6	M9	80/0.6
M_U	600/0.6	M10, M11	40/0.6

Table 5.18 Resistor and Capacitor Sizes in the LVDS Transmitter Circuit

Resisistor	**Size (μm)**	**Capacitor**	**Size (μm)**
R_1, R_2	100 kΩ (poly resistor)	C_3	10 pF (poly plate)
R_3	1.25 kΩ (poly resistor)		

5.9 Experimental Results

The performance of the PLL clock synthesizer in Figure 5.1 is characterized by using a evaluation board. The characterization setup is given in Appendix B.

Figure 5.20 illustrates a simulated timing diagram of critical signals (timing events) of the PLL clock synthesizer. This diagram is important to understand the sequence of events within the PLL as well as PLL's response to the external signals such as the pull up signal (PU). As shown in Figure 5.20, most of the critical signals are produced within the PLL internally such as the system power-on-reset (POR), PLL enable (PLL_ENB), and PLL internal power-on-reset (PLL_POR).

This design is fabricated in with 0.35-μm N-well CMOS process technology. The active die area of the chip is 3.35 mm^2. The PLL section occupies 0.8 mm^2. The die photograph is shown in Figure 5.22.

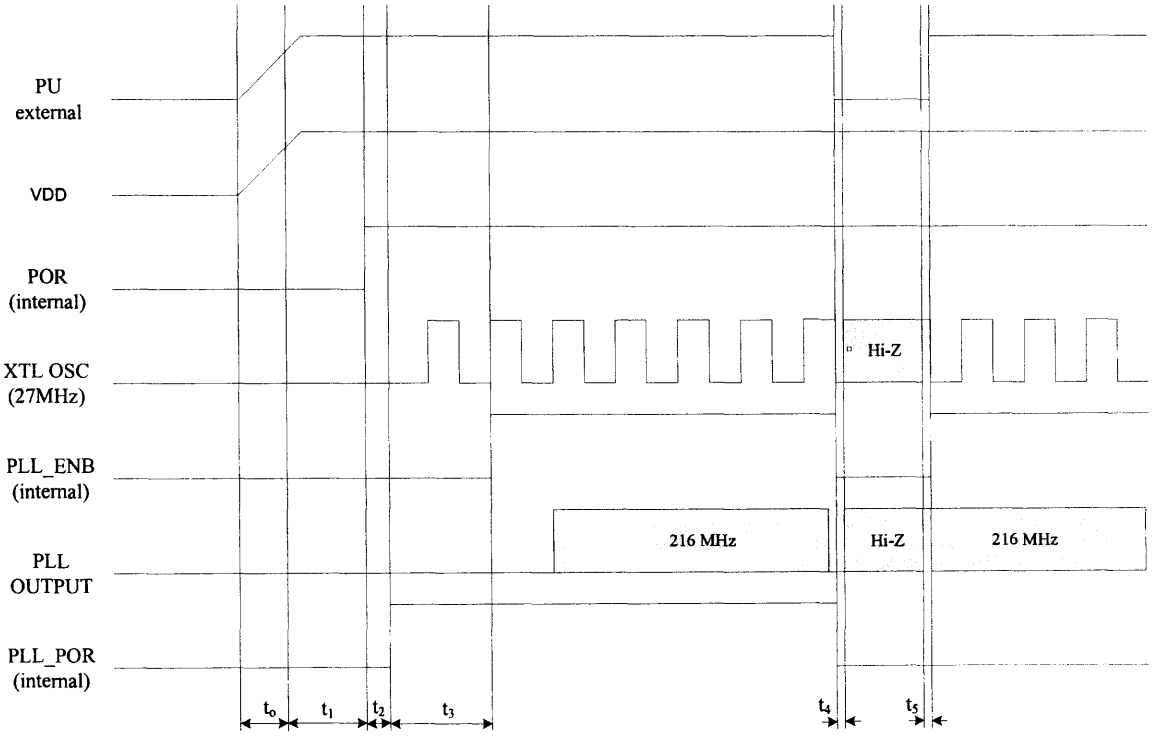


Figure 5.20 Simulated timing diagram of critical signals in PLL clock synthesizer.

The simulated timing is summarized in Table 5.19. Figure 5.23 displays a measured LVDS output waveform with AC parameters, period jitter and a histogram for the statistical data. The jitter histogram shows the PLL operating with a period jitter of 6.5-ps (rms) and 38-ps (peak-to-peak) at 216 MHz as measured with a LeCroy SDA Model 6000A analyzer. The jitter histogram is displayed in the second row of the oscilloscope screen (function F8). Each division on the jitter histogram display corresponds to 5.0 ps/div. The characterization of the period jitter is performed using a measurement function, per@lvl(C2) as shown in the sixth column in the measurement display, i.e., P6: per@lvl(C2). The rms-jitter is the readout from the "sdev" row under "Measure" category, i.e., the standard deviation or root mean square of large numbers of period measurements. The peak-to-peak jitter can be obtained from the "mean" value of the second column, i.e., P2: range(F8).

Figure 5.24 illustrates the phase noise performance of the PLL at an output frequency of 216 MHz. The phase noise is measured as –120 dBc/Hz at offset frequencies above 10 KHz. The phase noise response has a peak of –115 dBc/Hz at the loop bandwidth as expected. The experimental characterization of the PLL is summarized in Table 5.20 for operation at 216 MHz.

Measurement results clearly indicate that the implemented PLL clock synthesizer has resulted in an improved phase noise (and jitter). The performance of this chip are either better than or comparable to previously reported PLL clock synthesizers realized using ring oscillator VCOs in CMOS process technology [20], [24], [25], [26], [28], [29], [30], [31], [32]. The performance comparison of the implemented PLL with prior state-of-the-art designs is summarized in Table 5.21. The improvements are mainly due to the

phase noise optimization in the ring oscillator VCO as described in Chapter 4, the optimum loop bandwidth, and careful layout. Since the white noise is the dominant source of phase noise at higher offset frequencies such as 1 MHz, the minimization/ optimization of phase noise in ring oscillator VCO decreases the phase noise of the PLL output at higher offset frequencies. In addition, since the response of the PLL to the noise sources in the VCO has a high-pass characteristic, large loop bandwidth is favorable to filter out the VCO noise at higher offset frequencies. These two principles were applied to the design of the VCO and the PLL to minimize the effect of the intrinsic noise sources in MOS devices, primarily the thermal noise in MOS devices. Although both principles are equally important for the minimization of phase noise at the PLL output, there is a physical limit for the minimization of phase noise in a ring oscillator VCO. For this reason, alternative architectures for the VCO must be sought if the ring oscillator VCO can't meet the phase noise specification at the PLL output.

There are obvious noise sources in any CMOS IC implementation, other than the intrinsic noise sources of MOS devices. These are the power supply and substrate noise. The improvements made in the layout eliminated the effect of those noise sources which can degrade the phase noise performance of the PLL. One of these improvements is the use of guard rings and n-well to protect sensitive sections of analog circuit from the power-supply and substrate noise. It is well known that switching activity in large digital circuits introduces power-supply or substrate noise which perturb the more sensitive analog circuits in a PLL. The substrate coupling was reduced by employing double guard rings and n-well structure at the periphery of analog sections as shown in Figure 5.21. This guard ring structure isolates the sensitive analog sections from the substrate noise

produced by other sections. A guard ring is simply a continuous ring made of substrate ties that surrounds the circuit. The use of n-well also improves the operation of a guard ring by stopping the noise currents flowing near the surface. In addition, the use of separate power-supply pads for sensitive analog blocks are required to reduce the power-supply noise [105]. In this design, the major circuit design blocks of the PLL such as the charge pump and VCO are connected to a separate power-supply pad which is not shared with other circuits. Similary, the bias circuits and LVDS transmitter are also connected to their respective analog pads dedicated only to these circuits. This reduces the di/dt noise, which is due to the inductance of long connecting (internal) and bond (external) wires on the chip and minimizes the ground bounce.

Connections to analog circuit design blocks were made with wide metal lines having minimum width of 5-μm. For digital circuits, a separate power-supply pad was assigned and this pad is used explicitly for the digital circuits on the chip.

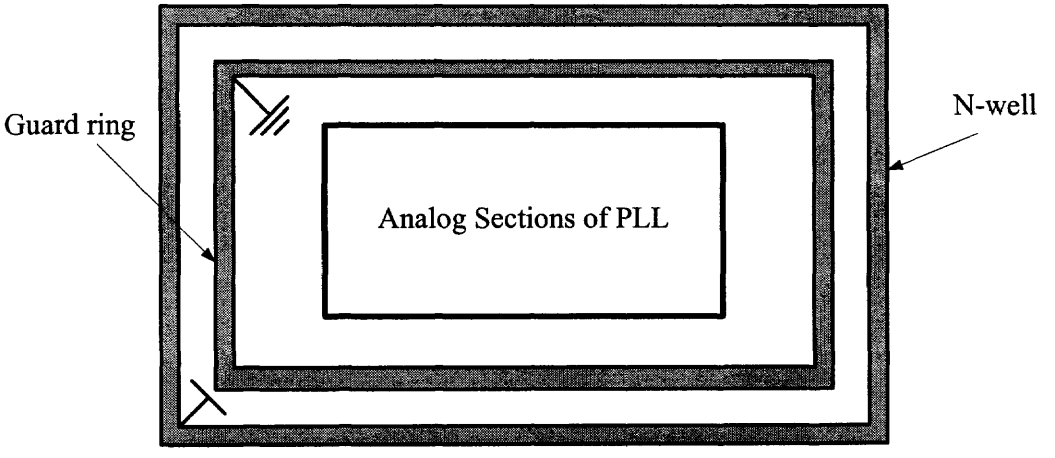


Figure 5.21 Isolation of sensitive sections of analog circuit from the substrate noise.

Table 5.19 Simulated Timing of Critical Signals in PLL Clock Synthesizer

Symbol	Duration	Symbol	Duration
t_0	100 ns	t_3	200 μs
t_1	8 μs	t_4	100 ns
t_2	1 μs	t_5	100 ns

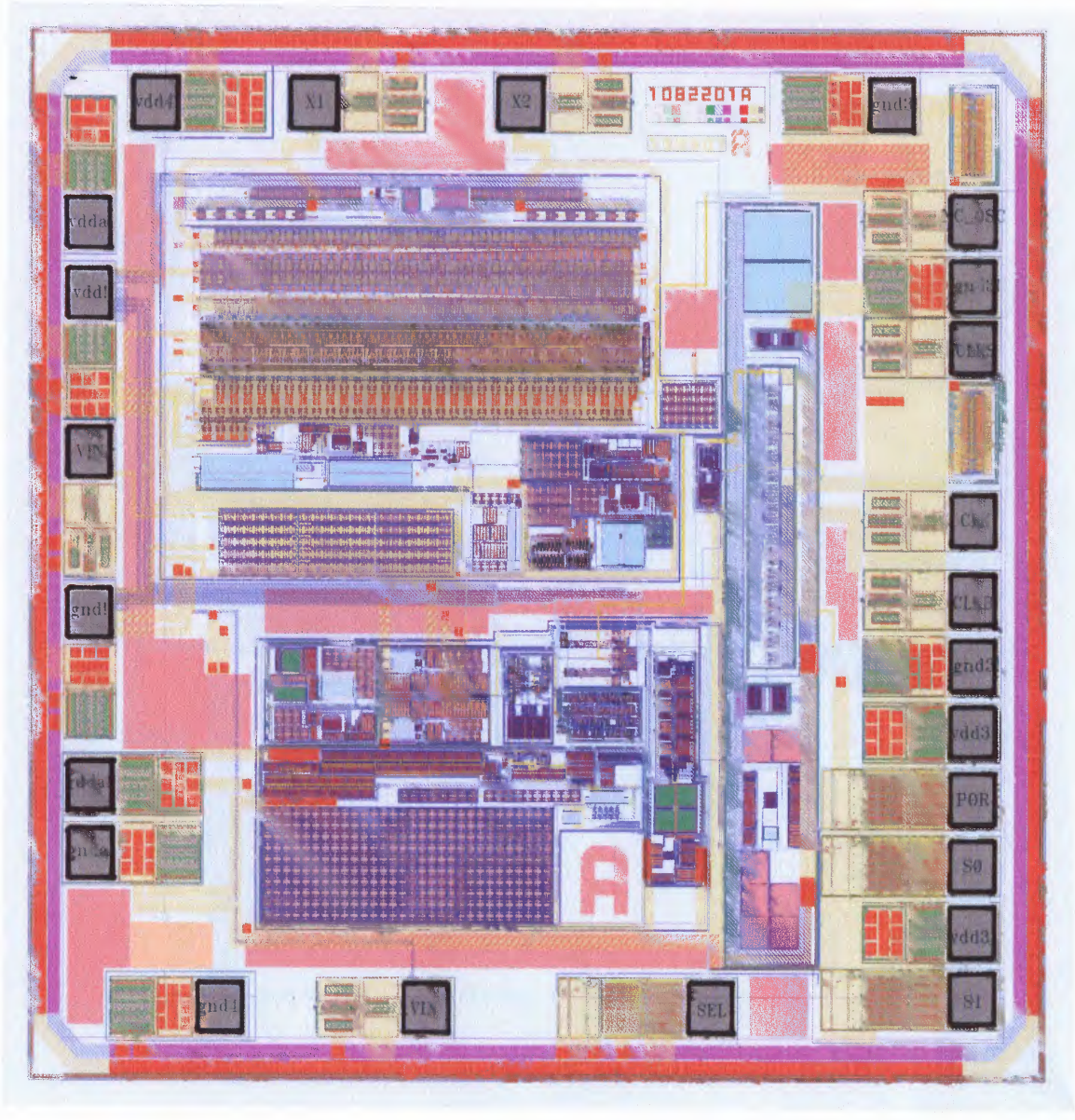


Figure 5.22 Die photograph of PLL clock synthesizer.

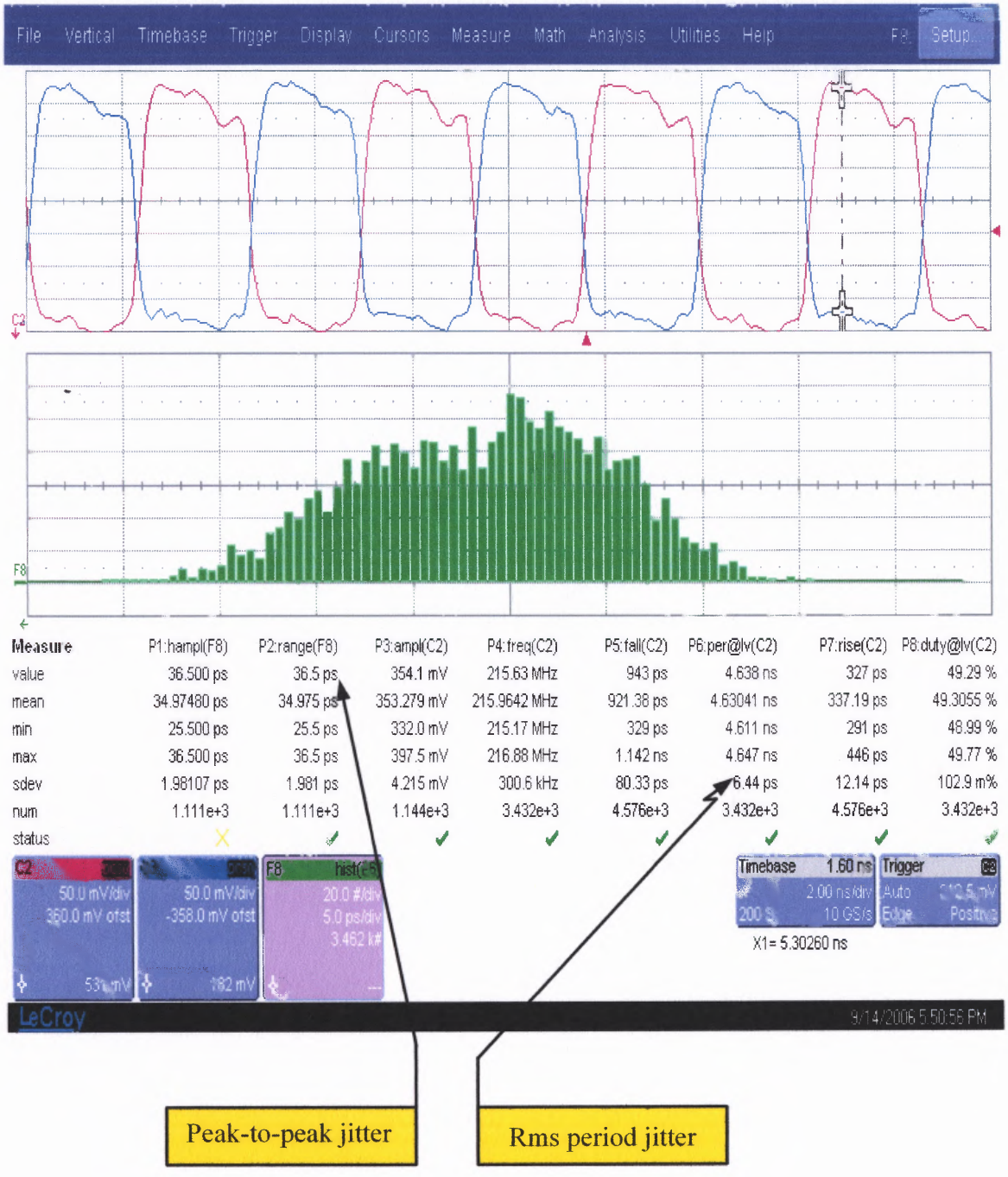


Figure 5.23 Measured LVDS waveform with a 100-Ω load.

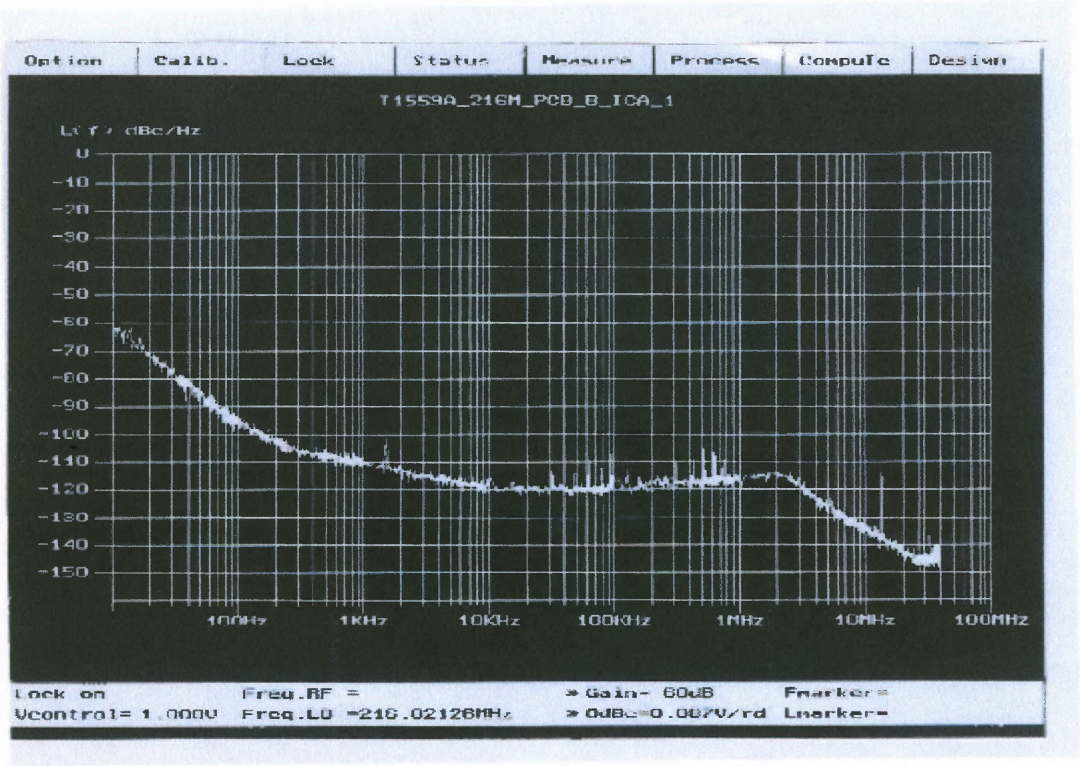


Figure 5.24 Spectral measurement of PLL phase noise performance.

Table 5.20 Performance Summary of PLL Clock Synthesizer

Frequency Range	20 MHz – 400 MHz
Input Reference	27 MHz
Operating Supply Current	35 mA
Power Supply Voltage	3-5 V
Power Dissipation	110 mW
Duty Cycle	49.3 %
1-σ Period Jitter	6.44 ps
Phase Noise offsets @ 10 kHz and above	-120 dBc/Hz
LVDS Differential Voltage Swing	800 mV
Device Technology	0.35-μm N-well CMOS
Die Area	3.35 mm^2

Table 5.21 Performance Comparison of the PLL with Prior State-of-the-Art Designs

Reference	Frequency Range (MHz)	Period Jitter (rms) (ps)	Period Jitter (peak-to-peak) (ps)	PhaseNoise (dBc/Hz)	Device Technology
Boerster [20]	340 - 612	10 @ 340 MHz	80 @ 340 MHz	N/A	0.4-μm CMOS
Horowitz [24]	30 - 650	N/A	20 @ 500 MHz	N/A	0.35-μm CMOS
Novof [25]	15 - 240	N/A	100 @ 100 MHz	N/A	0.5-μm CMOS
Young [26]	5 - 110	36 @ 50 MHz	288 @ 50 MHz	N/A	0.8-μm CMOS
Maneatis [28]	1 - 550	N/A	144 @ 250 MHz	N/A	0.5-μm CMOS
Yang [29]	0.3 - 165	13 @ 100 MHz	81 @ 100 MHz	N/A	0.8-μm CMOS
Maneatis [30]	30 - 650	18.8 @ 240 MHz	72 @ 240 MHz	N/A	0.13-μm CMOS
Kim [31]	300 - 400	3.1 @ 300 MHz	22 @ 300 MHz	N/A	0.6-μm CMOS
This work [87]	20 - 400	6.44 @ 216 MHz	36.5 @ 216 MHz	-120 @ 216 MHz $\Delta\omega > 10$ KHz	0.35-μm CMOS

Careful simulations of the overall environment including the package model of the chip were performed at the transistor level. The SPECTRE transient simulations determine the noise contributions of each of these sources. The circuit design and layout were improved based on the results of the transistor-level simulations.

CHAPTER 6

SUMMARY AND CONCLUSION

The fast growing demand of wireless and high speed data communications has driven efforts to increase the levels of integration in many communications applications. Phase noise and timing jitter are important design considerations for these communications applications. The desire for highly complex levels of integration generally is counter to the minimization of timing jitter and phase noise for communication systems, which employ a phase-locked loop for frequency and clock synthesis with on-chip VCO. This dictates an integrated CMOS implementation of the VCO with very low phase noise performance. The ring oscillator VCOs based on differential delay cell chains have been used successfully in communications applications, but thermal noise induced phase noise have to be minimized in order not to limit their applicability to some applications which impose stringent timing jitter and phase noise requirements on the PLL clock synthesizer. Obtaining lower timing jitter and phase noise at the PLL output also requires the minimization of noise in critical circuit design blocks as well as the optimization of the loop bandwidth of the PLL. This work has explored the fundamental performance limits and demonstrated with specific implementation of CMOS PLL clock synthesizers based on the ring oscillator VCOs.

An analysis of phase noise for the PLL output identified the thermal noise induced phase noise of the ring oscillator VCO as the limiting factor in determining the phase noise performance of the PLL clock synthesizer because the input reference signal has very low phase-noise characteristic in PLL clock synthesizer applications.

The phase noise performance of the ring oscillator VCO is determined by timing jitter and phase noise predictions of Chapters 2 and 3 and as well as the SPECTRE-RF simulation at transistor level. The phase noise performance of the PLL output was predicted using behavioral simulation introduced in Chapter 4. It was shown that the minimization of phase noise and timing jitter at the PLL output can be accomplished through careful consideration of design tradeoffs at the ring oscillator level and the PLL level described.

The specific research contributions of this work include (1) proposing, designing, and implementing a new charge pump circuit architecture that matches current levels and therefore minimizes one source of phase noise due to fluctuations in the control voltage of the VCO, (2) an improved phase-frequency detector architecture which has improved characteristics in lock condition, (3) an improved ring oscillator VCO with excellent thermal noise induced phase noise characteristics, (4) the application of self-biased techniques together with fixed bias to CMOS low phase noise PLL clock synthesizer for digital video communications, and (5) an analytical model that describes the phase noise performance of the proposed VCO and PLL clock synthesizer. In particular, it was shown that the experimental prototype implemented in a standard 0.35-μm N-well CMOS process technology achieves a period jitter of 6.5-ps (rms) and 38-ps (peak-to-peak) at 216 MHz with a phase noise of -120 dBc/Hz at frequency offsets above 10 KHz. For normal operation with the 3.3 V supply, the total power dissipation in the chip was only 110 mW.

The predictions based on mathematical models and behavioral modeling and as well as experimental results in this work indicate that with proper design the phase

noise and timing jitter at the PLL output can be kept low enough for contemporary communication systems. An interesting continuation of this work would be to apply this work to new standards of communications systems with the design tradeoffs available in the component and the PLL clock synthesizer levels.

APPENDIX A

MATLAB SOURCE CODE FOR MODELING THE THIRD ORDER CPLL

The following MATLAB source code was generated to verify the open and closed loop transfer characteristics of the linearized CPLL. In addition, the step response of the PLL is also calculated by using the "step" function in MATLAB.

```
%%%
%%% Third-Order PLL Parameters
%%%
Icp = 80e-6;
Kvco = 170e6;
K = Kvco*Icp/(2*pi);n

C1  = 250e-12;
C2  = 12.5e-12;
C12 = C1*C2/(C1+C2);
R1  = [2.1e3 2.8e3 3.5e3 4.0e3];
M   = [2 4 6 8];

wp = [1/(R1(1)*C12) 1/(R1(2)*C12) 1/(R1(3)*C12) 1/(R1(4)*C12)];
wz = [1/(R1(1)*C1)  1/(R1(2)*C1)  1/(R1(3)*C1)  1/(R1(4)*C1)];

%%%
%%% Open Loop Transfer Function
%%%
bo2 = [K/(C2*M(1)) wz(1)*K/(C2*M(1))];
ao2 = [1 wp(1) 0 0];

bo4 = [K/(C2*M(2)) wz(2)*K/(C2*M(2))];
ao4 = [1 wp(2) 0 0];

bo6 = [K/(C2*M(3)) wz(3)*K/(C2*M(3))];
ao6 = [1 wp(3) 0 0];

bo8 = [K/(C2*M(4)) wz(4)*K/(C2*M(4))];
ao8 = [1 wp(4) 0 0];
w = logspace(2,8);
%f = w/(2*pi);
f=w;
ho2 = freqs(bo2,ao2,w);
mago2 = 20*log10(abs(ho2));
phaseo2 = angle(ho2)*180/pi;

ho4 = freqs(bo4,ao4,w);
mago4 = 20*log10(abs(ho4));
```

```
phaseo4 = angle(ho4)*180/pi;

ho6 = freqs(bo6,ao6,w);
mago6 = 20*log10(abs(ho6));
phaseo6 = angle(ho6)*180/pi;

ho8 = freqs(bo8,ao8,w);
mago8 = 20*log10(abs(ho8));
phaseo8 = angle(ho8)*180/pi;

figure(1);clf
subplot(2,1,1), semilogx(f,mago2,'r','LineWidth',1.5)
hold on
subplot(2,1,1), semilogx(f,mago4,'b','LineWidth',1.5)
subplot(2,1,1), semilogx(f,mago6,'m','LineWidth',1.5)
subplot(2,1,1), semilogx(f,mago8,'c','LineWidth',1.5)
hold off
title('Third-Order PLL, Open Loop Frequency Response');
xlabel('Frequency (Hz)');
ylabel('Magnitude (dB)');
axis([1e2 1e7 -50 150]);
grid on

subplot(2,1,2), semilogx(f,phaseo2,'r','LineWidth',1.5)
hold on
subplot(2,1,2), semilogx(f,phaseo4,'b','LineWidth',1.5)
subplot(2,1,2), semilogx(f,phaseo6,'m','LineWidth',1.5)
subplot(2,1,2), semilogx(f,phaseo8,'c','LineWidth',1.5)
hold off
xlabel('Frequency (Hz)');
ylabel('Phase (Degree)');

axis([1e2 1e7 -180 -100]);
grid on
%%%
%%% Close Loop Transfer Function
%%%
bc2 = [K/C2 wz(1)*K/C2];
ac2 = [1 wp(1) K/(M(1)*C2) wz(1)*K/(M(1)*C2)];

bc4 = [K/C2 wz(2)*K/C2];
ac4 = [1 wp(2) K/(M(2)*C2) wz(2)*K/(M(2)*C2)];

bc6 = [K/C2 wz(3)*K/C2];
ac6 = [1 wp(3) K/(M(3)*C2) wz(3)*K/(M(3)*C2)];

bc8 = [K/C2 wz(4)*K/C2];
ac8 = [1 wp(4) K/(M(4)*C2) wz(4)*K/(M(4)*C2)];

hc2 = freqs(bc2,ac2,w);
magc2 = 20*log10(abs(hc2));
phasec2 = angle(hc2)*180/pi;

hc4 = freqs(bc4,ac4,w);
magc4 = 20*log10(abs(hc4));
phasec4 = angle(hc4)*180/pi;
```

```
hc6 = freqs(bc6,ac6,w);
magc6 = 20*log10(abs(hc6));
phasec6 = angle(hc6)*180/pi;

hc8 = freqs(bc8,ac8,w);
magc8 = 20*log10(abs(hc8));
phasec8 = angle(hc8)*180/pi;

figure(2);clf
subplot(2,1,1), semilogx(f,magc2,'r','LineWidth',1.5)
hold on
subplot(2,1,1), semilogx(f,magc4,'b','LineWidth',1.5)
subplot(2,1,1), semilogx(f,magc6,'m','LineWidth',1.5)
subplot(2,1,1), semilogx(f,magc8,'c','LineWidth',1.5)
hold off
title('Third-Order PLL, Close Loop Frequency Response');
xlabel('Frequency (Hz)');
ylabel('Magnitude (dB)');
axis([1e2 1e7 -40 40]);
grid on
subplot(2,1,2), semilogx(f,phasec2,'r','LineWidth',1.5)
hold on
subplot(2,1,2), semilogx(f,phasec4,'b','LineWidth',1.5)
subplot(2,1,2), semilogx(f,phasec6,'m','LineWidth',1.5)
subplot(2,1,2), semilogx(f,phasec8,'c','LineWidth',1.5)
hold off
xlabel('Frequency (Hz)');
ylabel('Phase (Degree)');
axis([1e2 1e7 -180 0]);
grid on
%%%
%%%
%%%
%%% Step Response of Close Loop
%%%
figure(3);clf
step(bc2,ac2,'r')
hold on
step(bc4,ac4,'b')
step(bc6,ac6,'m')
step(bc8,ac8,'c')
hold off
grid on
n =3
```

APPENDIX B

TEST SETUP

Figure B.1 depicts the test setup used to assess the performance of the experimental PLL clock synthesizer described in this dissertation. A list of the test and measurement instruments used to characterize the PLL clock synthesizer IC is given in Table B.1.

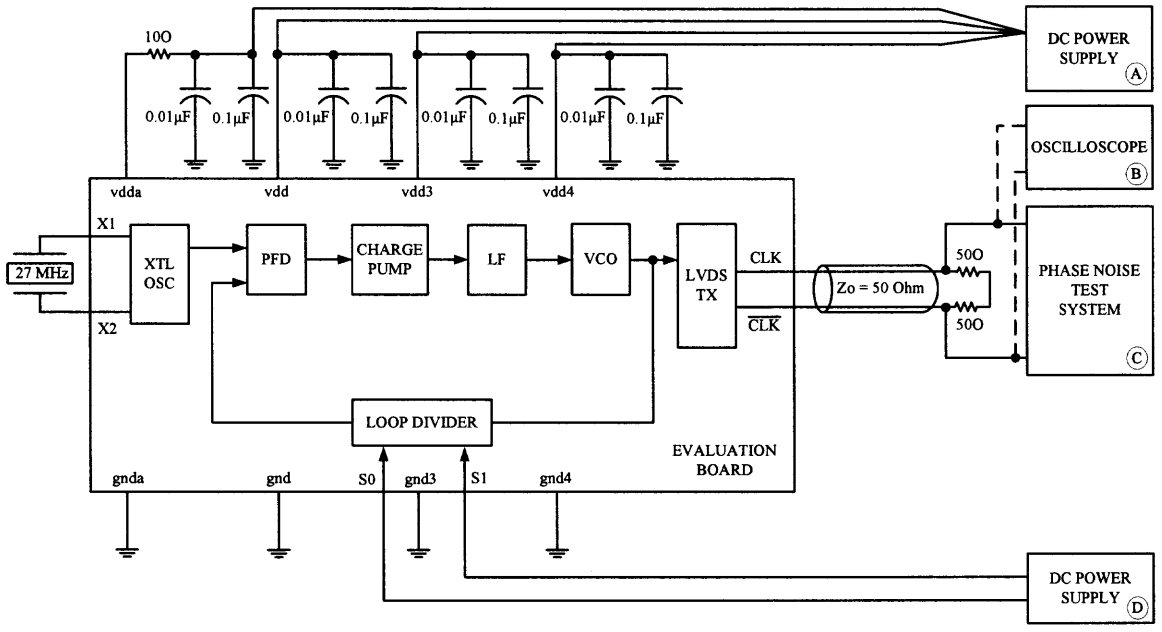


Figure B.1 Characterization setup of the experimental PLL clock synthesizer.

The evaluation board is made from two-sided printed circuit board with an FR4 dielectric layer. The 50-Ω micro-strip lines are created on the PCB. The ground planes on the top and bottom sides of the board are connected by means of a large number of vias.

The decoupling capacitors and resistors are all chip components. They must be located as close to pins of the IC as possible for proper phase noise and jitter measurement.

Table B.1 Test Setup Equipment List

Symbol	**Instrument**
A	Agilent E3600 Series DC Power Supply
B	LeCroy SDA Model 6000A Analyzer
C	Aeroflex PN9000 Phase Noise Test System
D	Agilent E3600 Series DC Power Supply

REFERENCES

1. F. M. Gardner, Phaselock Techniques, Third Ed., New York: Wiley & Sons, 2005.

2. V. Mannessewitch, Frequency Synthesizers; Theory and Design, Third Ed., New York: Wiley & Sons, 1987.

3. B. Razavi, Monolithic Phase-Locked Loops and Clock Recovery Circuits, First Ed., New York: Wiley & Sons, 1996.

4. J. Klapper and J. T. Frankle, Phaselocked and Frequency Feedback Systems, Second Ed., New York: Academic Press, 1972.

5. W. F. Egan, Frequency Synthesis by Phase Lock, New York: Wiley & Sons, 1981.

6. B. Razavi, Design of Analog CMOS Integrated Circuits, First Ed., New York: McGraw-Hill, 2001.

7. B. Razavi, Phase-Locking in High-Performance Systems, First Ed., New York: Wiley & Sons, 2002.

8. T. C. Weigandt, "Low-Phase-Noise, Low-Timing-Jitter Design Techniques for Delay Cell based VCOs and Frequency Synthesizers", Ph.D. Thesis, University of California, Berkeley, 1998.

9. J. Przybysz, D. Miller, E. Naviasky, "Two-loop Modulator for Sigma-delta Analog to Digital Converter," IEEE Transactions on Applied Superconductivity, vol. 5, no. 2, pp. 2248-51, June 1995.

10. R. Walden, "Analog-to-digital converter technology comparison," Proceedings of 1994 IEEE GaAs IC Symposium, pp. 217-219, Oct. 1994.

11. B. Razavi, "A study of phase noise in CMOS oscillators," IEEE J. Solid State Circuits, vol. 31, no. 3, pp. 331-343, Mar. 1996.

12. A. Hajimiri and T. H. Lee, The Design of Low Noise Oscillators, Boston: Kluwer Academic Publisher, 1999.

13. X. Li and M. Ismail, Multi-Standard CMOS Wireless Receivers: Analysis and Design, Boston: Kluwer Academic Publisher, 2002.

14. H. Rategh and T. H. Lee, Multi-GHz Frequency Synthesis and Division, Boston: Kluwer Academic Publisher, 2001.

15. L. Shahani et. al., "Low-power dividerless frequency synthesis using aperture phase detection," IEEE J. Solid State Circuits, vol. 33, no. 12, pp. 2232-2239, Dec. 1998.

16. T. H. Lee and J. F. Bulzacchelli, "A 155-MHz clock recovery delay- and phase-locked loop," IEEE J. Solid State Circuits, vol. 27, no. 12, pp. 1736-1746, Dec. 1992.

17. B. Thompson, H.S. Lee, L. DeVito, "A 300-MHz BiCMOS Serial Data Transceiver," IEEE J. Solid State Circuits, vol. 29, no. 3, pp. 185-192, Mar. 1994.

18. T. Hu, P. Gray, "A monolithic 480 Mb/s parallel AGG/decision/clock-recovery circuit in 1.2 μm CMOS," IEEE J. Solid-State Circuits, vol. 28, no. 12, pp. 1314-20, Dec. 1993.

19. M. Soyuer, "A monolithic 2.3 Gb/s 100-mW clock and data recovery circuit in silicon bipolar technology," IEEE J. Solid State Circuits, vol. 28, no. 12, pp. 1310-1313, Dec. 1993.

20. D. W. Boerstler, "A low-jitter PLL clock generator for microprocessors with lock range of 340-612 MHz," IEEE J. Solid State Circuits, vol. 34, no. 4, pp. 513-519, Apr. 1999.

21. M. G. Johnson and E.L. Hudson, "A variable delay line PLL for CPU-coprocessor synchronization," IEEE J. Solid State Circuits, vol. 23, no. 5, pp. 1218-1223, Oct. 1988.

22. J. Alvarez, H. Sanchez, G. Gerosa, R. Countryman, "A wide-bandwidth low-voltage PLL for PowerPC microprocessors," IEEE J. Solid State Circuits, vol. 30, no. 4, pp. 383-392, Apr. 1995.

23. T. Lee, K. Donnelly, et. al, "A 2.5V CMOS Delay-Locked Loop for an 18 MBit, 500 Megabyte/s DRAM," IEEE J. Solid State Circuits, Vol. 29, no. 12, pp. 1491-1496, Dec. 1994.

24. M. Horowitz, A. Chan, J. Cobrunson, J. Gasbarro, T. Lee, W. Leung, W. Richardson, T. Thrush, Y. Fujii , "PLL Design for a 500 MB/s interface," ISSCC Digest of Technical Papers, pp. 160-161, Feb. 1993.

25. I. Novof, J. Austin, R. Kelkar, D. Strayer, S. Wyatt, "Fully integrated CMOS phase-locked loop with 15 to 240 MHz locking range and ±50 ps jitter," ISSCC Dig. Tech. Papers, pp. 112-113, Feb. 1995.

26. I. A. Young, J. K. Greason, K. L. Wong, "A PLL clock generator with 5 to 110 MHz of lock range for microprocessors," IEEE J. Solid State Circuits, vol. 27, no. 11, pp. 1599-1607, Nov. 1992.

27. I. Young, M. Mar, B. Bhushan, "A 0.35μm CMOS 3-880MHz PLL N/2 Clock Multiplier and Distribution Network with Low Jitter for Microprocessors", ISSCC Digest of Technical Papers, pp. 330-331, Feb. 1997.

28. J. G. Maneatis, "Low-jitter process independent DLL and PLL based on self-biased techniques," IEEE J. Solid State Circuits, vol. 31, pp. 1723-1732, Nov. 1996.

29. H. J. Yang, L. K. Lee, R. S. Co, "A Low Jitter 0.3-165 MHz CMOS PLL Synthesizer for 3 V/5 V Operation," IEEE J. Solid State Circuits, vol. 32, no. 4, pp. 582-586, Apr. 1997.

30. J. G. Maneatis, J. Kim, I. McClatchie, J. Maxey, M. Shankaradas, "Self_Biased High-Bandwidth Low-Jitter 1-to-4096 Multiplier Clock Generator PLL," IEEE J. Solid State Circuits, vol. 38, no. 11, pp. 1795-1803, Nov. 2003.

31. K. Lim, C. Park, D. Kim, B. Kim, "A Low-Noise Phase-Locked Loop Design by Loop Bandwidth Optimization," IEEE J. Solid State Circuits, vol. 35, no. 6, pp. 807-815, Jun. 2000.

32. A. Gundel, S. Jorek, P. Janczykowski, A. Trezza, R. Goldblatt,"High performance low phase noise PLL clock synthesizer with LVDS outputs," IEEE Long Island Technology and Applications Conference, Proc. LISAT, pp. 145-151, May. 2006.

33. A. Blanchard, Phase-Locked Loops: Application to Coherent Receiver Design, Reissue Ed., New York: Wiley & Sons, 1992.

34. D. H. Wolaver, Phase-Locked Loop Circuit Design, First Ed., New York: Prentice-Hall, 1991.

35. J. Proakis and M. Salehi, Communication Systems Engineering, Second Ed., New York: Prentice-Hall, 2002.

36. J. Proakis, Digital Communications, Fourth Ed., New York: McGraw-Hill, 2001.

37. B. Sklar, Digital Communications, First Ed., New York: Prentice-Hall, 1988.

38. J.L. Stensby, Phase-Locked Loops: Theory and Applications, First Ed., Boca Raton: CRC Press, 1997.

39. P. Larsson, "A 2-1600-MHz CMOS clock recovery PLL with low-Vdd Capability," IEEE J. Solid State Circuits, vol. 34, no. 12, pp. 1951-1960, Dec. 1999.

40. L. Andersson, B. Rudberg, T. Lewin, et al., "Silicon bipolar chipset for SONET/ SDH 10 Gb/s fiber-optic communication links," IEEE J. Solid-State Circuits, vol. 30, no. 3, pp. 210-18, Mar. 1995.

41. S. Kiriaki, T. Viswanathan, et. al., "A 160-MHz analog equalizer for magnetic disk read channels," IEEE Journal of Solid-State Circuits, vol. 32, no. 11, pp. 1839-1850, Nov. 1997.

42. J. McNeill, R. Croughwell, L. DeVito, A.Gasinov, "A 150 mW, 155 MHz phase locked loop with low jitter VCO," Proceedings of IEEE International Symposium on Circuits and Systems - ISCAS '94, pp. 49-52, vol. 3, June 1994.

43. B. Thompson, H.S. Lee, L. DeVito, "A 300-MHz BiCMOS Serial Data Transceiver", IEEE J. Solid State Circuits, vol. 29, no. 3, pp. 185-192, Mar. 1994.

44. K. Kishine et. al., "A 2.5-Gb/s clock and data recovery IC with tunable jitter characteristics for use in LANs and WANs," IEEE J. Solid-State Circuits, vol. 34, no. 6, pp. 805-812, June 1999.

45. H. Werker et. al., "A 10-GB/s SONET-compliant CMOS transceiver with low crosstalk and intrinsic jitter," IEEE J. Solid-State Circuits, vol. 39, no. 12, pp. 2349-2358, Dec. 2004.

46. D. Johns, D. Essig, "Integrated circuits for data transmission over twisted-pair channels," IEEE J. Solid-State Circuits, vol. 32, no. 3, pp. 398-406, Mar. 1997.

47. S. Hussain, S. Barton, "Comparison of coherent and non-coherent modulation schemes for low-data rate hand-held satellite terminals subject to high phase noise," Proceedings of the Tenth International Conference on Digital Satellite Communications (Conf. Publ. No. 403), pp. 339-342, vol. 1, IEE, 1994.

48. J. H. Schrade, "A phase-lock receiver for the arraying of independently directed antennas," IEEE Transactions on Antennas and Propagation, vol. 12, no. 2, pp. 155-161, Mar. 1964.

49. J. B. Berner, J. M. Layland, P. W. Kinman, "Flexible loop filter design for spacecraft phase-locked loops," IEEE Transactions on Aerospace and Electronic Systems, vol. 37, no. 3, pp. 957-964, July 2001.

50. J. Maneatis, "Hidden complexities of PLLs are revealed," ISD magazine, pp. 1-5, Mar. 2002.

51. W. P. Robins, Phase Noise in Signal Sources London: Peregrinus, Ltd., 1982.

52. M.J. Underhill, "Fundamentals of Oscillator Performance," Electronics & Communication Engineering Journal, vol. 4, pp. 195-183, Aug. 1992.

53. A. L. Lance, W. D. Seal, F. G. Mendoza and N. W. Hudson, "Automatic phase noise measurements," Microwave J., vol. 20, no. 6, pp. 87-90, June 1977.

54. M. McNamee, "Automate for improved phase noise measurement," Microwaves, vol. 48, no. 5, pp. 80-81, May 1979.

55. D. Scherer, "The art of phase noise measurement," Hewlett-Packard RF and Microwave Measurement Symposium, May 1983.

56. R. Temple, "Choosing a phase noise measurement technique-concept and implementation," Hewlett-Packard RF and Microwave Measurement Symposium, Feb. 1983.

57. T. C. Weigandt, B. Kim, and P. Gray, "Analysis of timing jitter in CMOS ring oscillators," in Proc. ISCAS, vol. 4, pp. 27-30, Jun. 1994.

58. J. Craninckx and M. Steyaert, "Low-noise voltage controlled oscillators using enhanced LC-tanks," IEEE Trans. Circuits Syst.-II, vol. 42, pp. 794–904, Dec. 1995.

59. J. McNeill, "Jitter in Ring Oscillators," IEEE J. Solid-State Circuits, vol. 32, no. 6, pp. 870-879, Jun. 1999.

60. A. Hajimiri, S. Limotyrakis, and T. Leee, " Jitter and Phase Noise in Ring Oscillators," IEEE J. Solid-State Circuits, vol. 34, no. 6, pp. 790-804, Jun. 1999.

61. F. Herzel and B. Razavi, "A study of oscillator jitter due to supply and substrate noise," IEEE Trans. Circuits Syst. II, vol. 46, pp. 56-62, Jan. 1999.

62. P. Larsson, "Measurement and analysis of PLL jitter caused by digital switching noise," IEEE J. Solid-State Circuits, vol. 36, no. 6, pp. 1113-1120, July 2001.

63. A. A. Abidi, "Phase Noise and Jitter in CMOS Ring Oscillators," IEEE J. Solid State Circuits, vol. 41, no. 8, pp. 1803-1816, Aug. 2006.

64. B. Razavi, Design of Integrated Circuits for Optical Communications, First Ed., New York: McGraw-Hill, 2003.

65. "Total jitter measurement through the extrapolation of jitter histograms," LeCroy, Jan. 2005, Retrieved October 22, 2006 from the World Wide Web: http://www.lecroy.com/tm/Library/WhitePapers/.

66. "Understanding and characterizing timing jitter," Tektronix, Oct. 2003. Retrieved October 28, 2003 from the World Wide Web: http://www.tektronix.com/jitter/.

67. M. Meghelli, B. Parker, H. Ainspan, and M. Soyuer " SiGe BiCMOS 3.3-V clock and data recovery circuits for 10-Gb/s serial transmission systems," IEEE J. Solid-State Circuits, vol. 35, no. 12, pp. 1992-1995, Dec. 2000.

68. K. Lee, S. Kim, G. Ahn, and D. Jeong "A CMOS serial link for fully duplexed data communication," IEEE J. Solid-State Circuits, vol. 30, no. 4, pp. 353-364, Apr. 1995.

69. U. L. Rohde, Digital PLL Frequency Synthesizers, Englewood Cliffs: Prentice-Hall, 1983.

70. Private communication with Dr. Floyd M. Gardner.

71. R. E. Best, Phase-Locked Loops Design, Simulation, and Applications, Fourth Ed., New York: McGraw-Hill, 1999.

72. P. K. Hanumolu, M. Brownlee, K. Mayaram, U. K. Moon, "Analysis of charge-pump phase-locked loops," IEEE Trans. Circuits Sys., vol. 51, no. 9, pp. 1665-1674, Sept. 2004.

73. J. Hein and J. Scott, "z-domain model for discrete-time PLLs," IEEE Trans. Circuits Sys., vol. 35, no. 9, pp. 1393-1400, Nov. 1988.

74. W. F. Egan, Phase-Lock Basics, New York: Wiley & Sons, 1998.

75. J. Craninckx and M. Steyaert, "A fully integrated CMOS DCS-1800 synthesizer," IEEE J. Solid-State Circuits, vol. 33, no. 12, pp. 2054-2065, Dec. 1998.

76. C. S Vaucher, Architectures for RF Frequency Synthesizers, Boston: Kluwer Academic Publisher, 2002.

77. D. Banarjee, PLL Performance, Simulation and Design Handbook, Fourth Ed., National Semiconductor, Application Note, 1998.

78. A. Aktas and M. Ismail, CMOS PLLs and VCOs for 4G Wireless: Analysis and Design, Boston: Kluwer Academic Publisher, 2004.

79. B. Razavi, RF Microelectronics, Englewood Cliffs: Prentice-Hall, 1998.

80. X. Li and M. Ismail, Multi-Standard CMOS Wireless Receivers: Analysis and Design, Boston: Kluwer Academic Publisher, 2002.

81. S.Gehta, Design of Gigahertz CMOS Prescalers, MS Thesis, U. C. Berkeley, May 1997.

82. J. McNeill, "Jitter in ring oscillators," IEEE J. Solid-State Circuits, vol. 32, pp. 870-879, June 1997.

83. J. McNeill, "Jitter in ring oscillators," PhD Dissertation, Boston University, June 1994.

84. Y. M. Lin, B. Kim, P. R. Gray, "A 13 bit 2.5 MHz self-calibrated pipelined A/D converter in 3 μm CMOS," VLSI Circuits Digest of Technical Papers, pp. 33-34, June1990.

85. B. Kim, D. N. Helman, P. R. Gray, "A 30-MHz hybrid analog/digital clock recovery circuit in 2-μm CMOS," IEEE J. Solid-State Circuits, vol. 25, no. 6, pp. 1385-1394, Dec. 1990.

86. J. G. Maneatis, M. A. Horowitz, "Precise delay generation using coupled oscillators," IEEE J. Solid-State Circuits, vol. 28, no. 12, pp. 1273-1282, Dec. 1993.

87. A. Gundel and W. N. Carr, "Low jitter CMOS PLL clock synthesizer with 20-400 MHz locking range," in Proc. ISCAS, May. 2007.

88. F. M. Gardner, "Charge-pump phase-lock loops," IEEE Trans. Communications, vol. 28, no. 11, pp. 1849-1858, Nov. 1980.

89. R. Nonis, N. D. Dalt, P. Palestri, L. Selmi, "Modeling, design and characterization of a new low-jitter analog dual tuning LC-VCO PLL architecture," IEEE J. Solid-State Circuits, vol. 40, no. 6, pp. 1303-1309, June 2005.

90. M. H. Perrott, "PLL Design Using the PLL Design Assistant Program," [Document posted on Web site MIT] Retrieved May 20, 2006 from the World Wide Web: http://www-mtl.mit.edu/~perrott.

91. BSIM3v3 Manual, [Document posted on Web site UC Berkeley] Retrieved Oct 22, 2006 from the World Wide Web: http://www.eecs.berkeley.edu/Pubs/TechRpts/1999/3629.html

92. "0.35μm CMOS C35 Process Parameters, rev. 3.0," [Document posted on Web site Austriamicrosystems] Retrieved Apr. 15, 2006 from the World Wide Web: http://www.austriamicrosystems.com/

93. A. A. Abidi, "Phase Noise and Jitter in CMOS Ring Oscillators," IEEE J. Solid State Circuits, vol. 41, no. 8, pp. 1803-1816, Aug. 2006.

94. M. H. Perrot, T. Tewksbury, and C. Sodini "A modeling approach for sigma-delta fractional-N frequency synthesizers," IEEE J. Solid State Circuits, vol. 38, no. 8, pp. 1028-1038, Aug. 2002.

95. M. H. Perrot, "Fast and accurate behavioral simulation of fractional-N synthesizer and other PLL/DLL circuits," Design Automation Conference (DAC), pp. 498-503, 2002.

96. D. A. Johns, K. Martin, Analog Integrated Circuit Design, New York: Wiley & Sons, 1997

97. J. Craninckx and M. Steyaert, Wireless CMOS Frequency Synthesizer Design, Boston: Kluwer Academic Publisher, 1998.

98. M. Shoji, "Elimination of process-dependent clock skew in CMOS VLSI," IEEE J. Solid-State Circuits, vol. 21, no. 5, pp. 875-880, Oct. 1986.

99. H. Taub and D. Schilling, Digital Integrated Electronics, New York: McGraw-Hill, 1977.

100. R. H. Katz, Contemporary Logic Design, Redwood City: Benjamin/Cummings Publishing Company, Inc., 1994.

101. J. M. Rabaey, Digital Integrated Circuits, Upper Saddle River: Prentice-Hall, 1996.

102. B. Parzen, Design of Crystal and Other Harmonic Oscillators, New York: Wiley & Sons, 1983.

103. IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scal-able Coherent Interface (SCI), 1596.3 SCI-LVDS Standard, IEEE Std. 1596.3-1996, 1994.

104. Electrical characteristics of low-voltage differential-signalling (LVDS) interface circuits, TIA/EIA-644, National Semiconductor Corp., ANSI/TIA/EIA, 1996.

105. P. Larsson, "Measurement and analyis off PLL jitter caused by Digital switching noise," IEEE J. Solid-State Circuits, vol. 36, no. 7, pp. 1113-1119, Jul. 2001.