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ABSTRACT

FABRICATION AND CHARACTERIZATION OF BACK ILLUMINATED CMOS PHOTODIODE ARRAY

by
Amrita Banerjee

With the rapid development in low-cost CMOS technology, silicon photodiodes are currently recognized as promising choice for the imager core. In this research, the arrays of back illuminated photodiodes were designed, fabricated and demonstrated with CMOS imager fabrication process on silicon wafers. The main purpose of this work was to improve the contribution of these arrays on the imaging systems before committing their design on the chips.

In this CMOS process, first the n-well, p-well, n+ and p+ regions were simulated and fabricated by several implantation processes. The n-well region was implanted by phosphorus at an energy of 170 keV and dose of 7×10^{12} cm^{-2} to obtain a 1 μm deep well. p-well was implanted with boron at energy of 70 keV and dose of 1×10^{13} cm^{-2} with a depth comparable to n-well region. An annealing for 30 minutes was then held after completion of these two implantation steps to drive-in the dopants. Phosphorus implant (45 keV, 2×10^{14} cm^{-2}) and boron implant (30 keV, 2×10^{14} cm^{-2}) were made to form n^+ and p^+ regions respectively, with a depth around 0.4 μm. Some test structures were also designed during the device fabrication, to compare the sheet resistances with the simulated values of the implantation steps.

The dark current, simulated for the fabrication conditions, shows a value of 1.95pA at a reverse bias of -3V. The measured dark current, just after metallization, had a value of 15pA with same applied bias.

FABRICATION AND CHARACTERIZATION OF BACK ILLUMINATED CMOS PHOTODIODE ARRAY

by
Amrita Banerjee

A Thesis
Submitted to the Faculty of
New Jersey Institute of Technology
In Partial Fulfillment of the Requirements for the Degree of
Master of Science in Electrical Engineering

Department of Electrical and Computer Engineering

August 2006

APPROVAL PAGE

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To my family

ACKNOWLEDGMENT

Many people have assisted me during the course of this work. I am very grateful to my graduate advisor Dr. Durga Misra whose inspiration and guidance benefited me significantly; without his valuable and countless support, encouragement, and reassurance this work could not have been finished.

I would like to take this opportunity to extend my sincere gratitude to Dr. Marek Sosnowski for serving on my thesis evaluation committee.

My special thanks to Dr. Dentcho Ivanov for participating on my thesis committee and for his invaluable assistance regarding this project throughout the duration of this project.

I would like to thank Dr. Bedabrata Pain, JPL, NASA, for giving me a chance to work on his designed devices.

My special gratitude is for Dr. Rajendra K. Jarwal, in the Microelectronics Laboratory, for giving me valuable advice during my whole fabrication process.

I would like to thank my friends in NJIT who have given me moral support. Among these I feel particularly grateful to Nilufa Rahim, Reenu Garg, Naser Chaudury, Srinivasan Purusothaman.

I am greatly indebted to my family for supporting me all the time over my days, for this program.

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CHAPTER 1

INTRODUCTION

For over 20 years, Charge Couple Devices (CCDs) were leading the path in the field of camera electronics for all kinds of applications [5]. In recent years, Complementary Metal Oxide Semiconductor (CMOS) image sensors have taken a lead in this area of competition. CMOS imagers offer very significant advantages over CCDs, such as low voltage operation and low power consumption, system on a chip capability, higher speed, marginally superior responsivity, highly integrated, possibly less cost [6, 7, 8]. In earlier days, the main draw back of the CMOS imagers was limited fill factor, due to the metal lines, connecting each device. The back illumination of the photodiodes was impossible because of the thickness of the back- plane. With the rapid development in low-cost CMOS technology, silicon photodiodes are currently recognized as promising core of the imagers.

Therefore, in this project, the arrays of back illuminated photodiodes were designed, fabricated and demonstrated with CMOS imager fabrication process on silicon wafer to realize further development of these arrays for imaging systems before committing their design on the chips. It is expected to demonstrate, high quantum efficiency and almost 100% fill factor through back- illumination and low dark current, with front- side used for signal conditioning [1]. In back-illumination process the light incidents on the photodiode will be from the back-end of the wafer, so most of the photons, due to the limited depth of silicon available on the top film, are presumed to be

absorbed. There will be no metal wires to block the light at the back side. Hence, high fill factor is expected.

This work is done in collaboration with NASA's Jet Propulsion Laboratory (JPL), Pasadena, California. The main objective of this project is to increase the quality of photodiodes to insure the reliability of the CMOS (Complementary Metal Oxide Semiconductor) active-pixel sensors (APSs), to get zero image lag and to achieve low noise even under low light intensity.

Chapter 2 describes the working principle and some characteristics of a conventional photodiode, produced by CMOS process. It also describes the necessity of designing the back-illuminated photodiodes for efficient CMOS imagers.

Chapter 3 describes some TAURUS TSUPREM and SRIM simulation results to obtain the accurate dose of implantation in various layers. It also describes TAURUS MEDICI dark current model used to simulate the dark current behavior. This chapter also shows the test structures, which were implemented during the fabrication to measure the sheet resistance of different layers.

Chapter 4 describes the fabrication process, required to obtain the photodiodes with very low dark current. It includes the mask layouts, fabrication sequence, and process flow. It also shows experimental results, mainly the dark current generated in the photodiodes.

Chapter 5 states the conclusions of the thesis. It also specifies further steps to ensure the quality of these novel devices.

CHAPTER 2

BACKGROUND

2.1 Definition of a Conventional Photodiode

Optoelectronics is the science that deals with the interaction between light and mater. The consequences of the interaction may be utilized in devices that are sensitive to light or of devices that generate light. A photodiode is a device that is sensitive to optical radiation and generates electrical current in response to that radiation. This device has variety of applications such as measuring light intensity, controlling the lens exposure of a camera [2].

The main mechanism, behind the operation of a photodiode, is discussed here briefly. The absorption of the light creates electron-hole pairs that result in major increases in the conductivity of a p-n junction semiconductor. Optical energy is absorbed if its wavelength is less than a critical value, λ_{max}. For radiation that has energy $h\upsilon$ [here h is the planck constant and ν is the frequency of radiation] greater than the band gap energy of the semiconductor, each photon releases sufficient energy to create an electron-hole pair [3]. The energy of the photon, E is related to its wavelength, λ,

$$E = h\nu = \frac{1.24}{\lambda(\mu m)} eV \tag{2.1}$$

The critical frequency and wavelength for absorption are given by

$$\nu_{\min} \geq \frac{E_g}{h}, \lambda_{\max} = \frac{hc}{E_g} = \frac{1.24}{E_g(eV)} \mu m \tag{2.2}$$

where ν_{min} is the lowest frequency below which no absorption occurs, λ_{max} is the maximum critical wavelength, E_g is the bandgap energy in eV and c is the speed of light

in vacuum. Radiation, having wavelength greater than λ_{max} is not absorbed by the semiconductor, which is then said to be transparent to that wavelength radiation. If the wavelength of the radiation is smaller than λ_{max}, implying that the radiant energy is greater than the band gap, each photon produces an electron-hole pair with the balance of the energy absorbed as heat.

2.2 Working Principle of a Photodiode

A photodiode has two terminals p and n as shown in Figure 2.1. It is also assumed here that a window is kept open on the front side to allow the incident photons to impact the p/n junction.

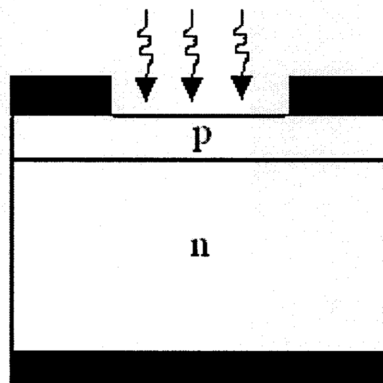


Figure 2.1 Cross section of a simple photodiode [2].

The diode is assumed to be reversed biased. An incident photon, having $\lambda < \lambda_{max}$, generates an electron-hole pair. These carriers cause a photo current in the diode, which is added to the thermally generated minority carrier current across the diffusion length. The carriers, generated within the depletion region W, are separated by the junction field, where electrons are collected in the n region and holes in the p region.

If the junction is uniformly illuminated by photon with hυ >E_g, the expression for the photo current, I_{op} will be,

$$I_{op} = qg_{op}A(W + L_n + L_p) \tag{2.3}$$

where, g_{op} is the number of photogenerated electron-hole pairs per second per unit volume, where A is the area, L_n and L_p are the diffusion length of electron and hole respectively and W is the depletion region width.

The total current, in the external circuit, is the thermally generated current and the photogenerated current. Since this current is directed from n to p, the diode equation will be,

$$I = I_{th}\left[e^{qV/KT} - 1\right] - I_{ph} \tag{2.4}$$

$$= qA\left[\left(\frac{L_p}{\tau_p}p_n + \frac{L_n}{\tau n}n_p\right)\left(e^{qV/KT} - 1\right)\right] - qAg_{op}(W + L_n + L_p) \tag{2.5}$$

Where, τ_p and τ_n are the hole and electron lifetime, respectively. p_n and n_p are the hole concentration in n region and electron concentration in p region, respectively. This equation can be considered in two parts- the current described by the usual diode equation, and the current due to optical generation. Thus the I-V curve of the diode is lowered by an amount proportional to the generation rate, which is shown in Figure 2.2.

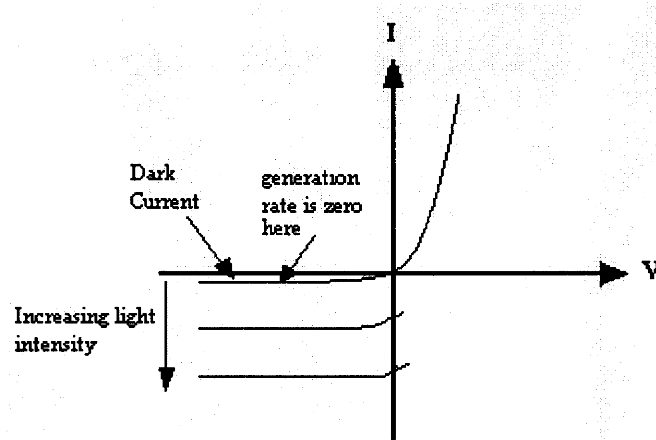


Figure 2.2 Photodiode characteristics [2].

To illustrate the process of the photogeneration of carriers, a schematic of a diode is shown in Figure 2.3 and also the four possible location of electron-hole pair generation is depicted in the Figure 2.3.

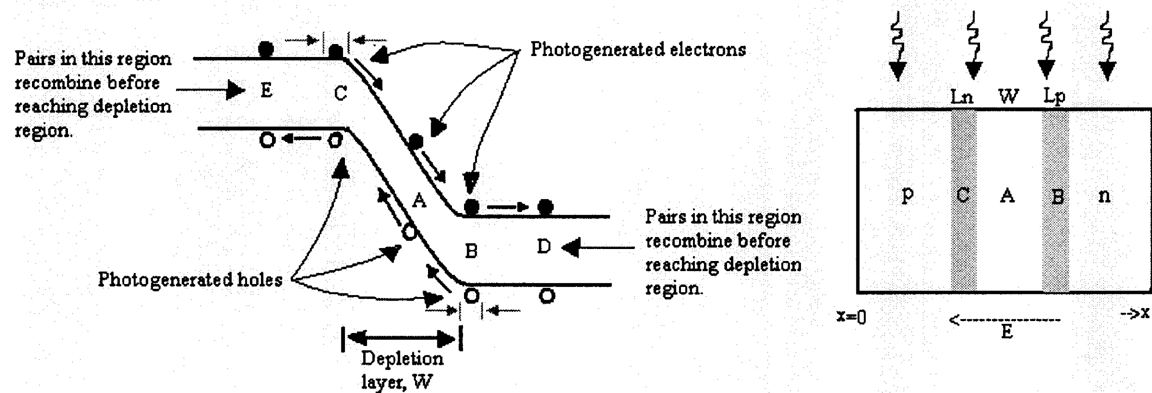


Figure 2.3 Four possible places for electron-hole pair generation [2].

If the photon is absorbed in the depletion layer, it generates an electron-hole pair, as shown at region A. Both the electron and hole generated here move under the influence of applied electric field. The holes move towards the p region and electron towards the n region and both contribute in the photogenerated current. The electron-hole pairs, photogenerated in C and B regions, lie in the bulk within one diffusion length (L_n and L_p for electrons and holes respectively), as seen in the Figure 2.2. These electrons

and holes are able to diffuse through the edges of depletion layers and drift through it, before recombining. So, the pairs generated in the C, B regions will be able to contribute to the photogenerated current too. But the electron-hole pairs generated in the bulk of p and n regions and lie beyond one diffusion length from the edges of the depletion region will not contribute any photo current to the device. When the device is short circuited (V=0), the short-circuit current from n to p is I_{op}. Thus the I-V characteristics of Figure 2.2 cross the negative I axis, which is proportional to g_{op}. When the device is open circuited current expression becomes zero and the voltage becomes

$$V_{oc} = \frac{kT}{q}\ln\left[{}^{I_{op}}\!/_{I_{th}} + 1\right] \tag{2.6}$$

$$\text{or, } V_{oc} = \frac{kT}{q}\ln\left[\frac{L_p + L_n + W}{\left({}^{L_p}\!/_{\tau_n}\right)p_n + \left({}^{L_n}\!/_{\tau_n}\right)n_p}\cdot g_{op} + 1\right] \tag{2.7}$$

For a symmetrical junction, $p_n = n_p$ and $\tau p = \tau_n$, we can rewrite the open circuit voltage expression by (neglecting generation within W)

$$V_{oc} = \frac{KT}{q}\ln\left[\frac{g_{op}}{g_{th}} + 1\right] \tag{2.8}$$

The term $g_{th} = p_n/\tau_n$ represents the equilibrium thermal generation- recombination rate. As the minority carrier concentration increases by optically generated electron-hole pairs, the life time, τ_n becomes shorter and p_n/τ_n becomes larger. As a result V_{oc} cannot increase with generation rate. The limit on V_{oc} is the equilibrium contact potential, V_o. V_o is the highest forward bias that can appear across the junction. The appearance of a forward voltage across an illuminated junction is known as *photovoltaic effect*, which is shown in Figure 2.4

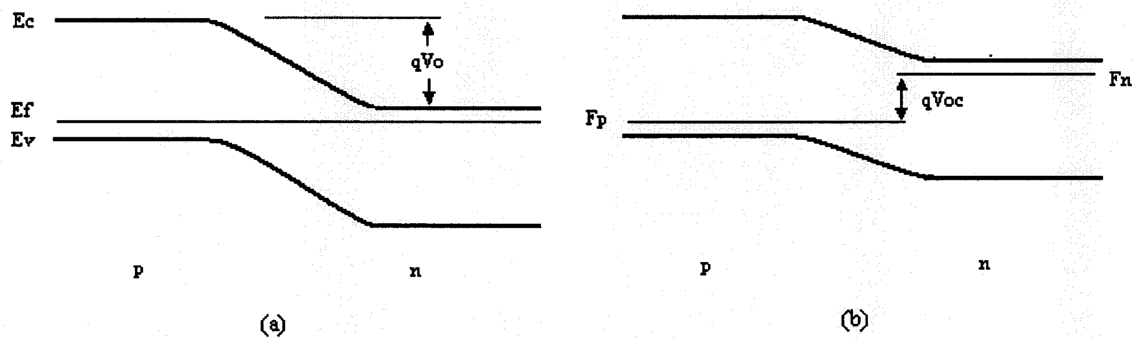


Figure 2.4 Effects of illumination on the open circuit voltage of a junction: (a) junction at equilibrium; (b)appearance of V_{oc} with illumination.

Depending on the application, the photodiode, can be operated in different quadrants of the I-V graph. In the first quadrant of the characteristic both current and voltage are positive. Because the photogenerated current is opposite in direction to the normal current, the total current is smaller than the normal diode current. The characteristics in third quadrant correspond to operation in the reverse direction, while the presence of light for $g_{op}>0$ increases reverse current, as shown in the Figure 2.5 (b). In this region diode is used as a light- sensitive switching circuit. In fourth quadrant the current is negative and the voltage is positive. In this case, the power is delivered to the outer circuit by the diode; here the device works as a photovoltaic cell.

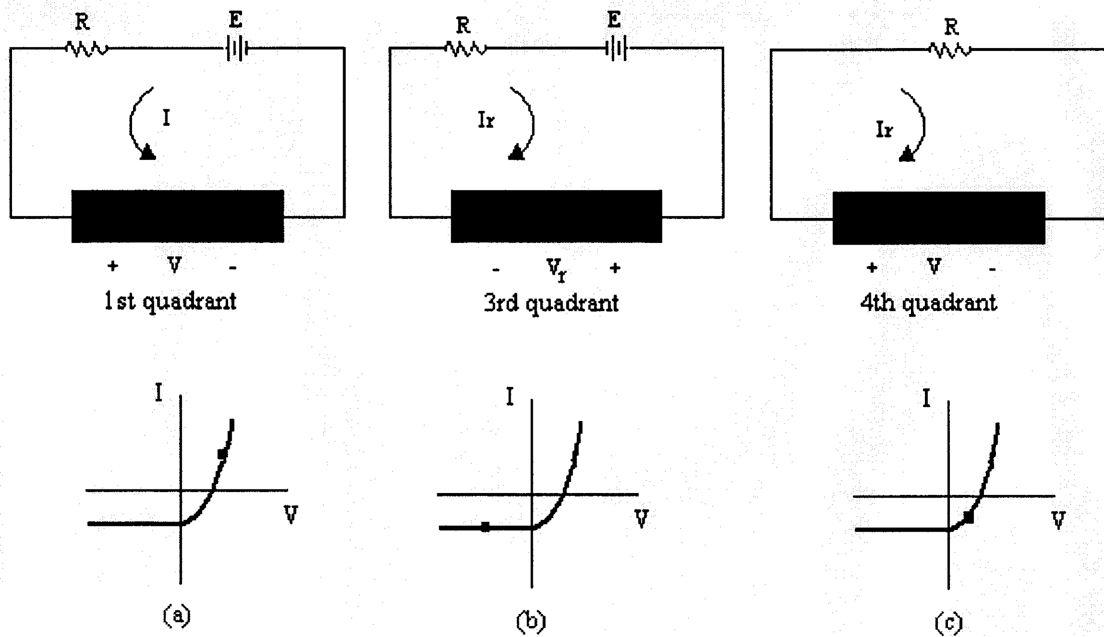


Figure 2.5 Operation of a photodiode at various quadrants of its I-V characteristics: (a) 1st quadrant, (b) 3rd quadrant and (c) 4th quadrant [2].

2.3 Characteristics of a Photodiode

2.3.1 Spectral Response

The magnitude of the photocurrent generated by a photodiode is dependent upon the wavelength of the incident light. Silicon photodiodes, exhibit a response from the ultraviolet through the visible and into the near infrared part of the spectrum. The spectral response peaks in the near infrared region between 800 nm and 900 nm.

There are several common ways to characterize the spectral response; following are the brief descriptions of few of them.

2.3.2 Overall Efficiency and Speed of Response

There are two main properties of a photodiode, the efficiency and the speed of response of the device. Here, the overall efficiency is the ratio of the power absorbed in the depletion region to the to the total power incident on the diode. In Figure 2.1 a fraction of light falling on the P region is absorbed in that region, determined by the widths of the P region and the depletion region. A fraction of light reaching the depletion region is absorbed while some of it is reflected back from the whole device. These factors cause the efficiency of the device to be less than 100%.

There are two factors that determine the portion of the light that is absorbed by the depletion region, namely: the Fresnel reflection factor, R_f and the attenuation factor, alpha (α).

The Fresnel factor determines the light reflected back from the P region, which is given by

$$R_f = \left(\frac{n_2 - n_1}{n_2 + n_1} \right)^2 \tag{2.9}$$

where, n2 and n1 are the refractive indices of the p region and the external medium respectively. Therefore, the fraction of light entering the p region is ($1-R_f$). The amount of light leaving the P region is determined by the attenuation factor, which can be written in the form given below

$$\Delta P(x) = P(x + \Delta x) - P(x) = P(x)\alpha\Delta x \tag{2.10}$$

where, P(x) is the power at point x and α is the attenuation factor. The attenuation factor is a function of the material and the wavelength of the incident light. Assuming that Δx is very small, the equation can be written in a different form given below

$$d^{P(x)}\Big/_{dx} = P(x)\alpha \tag{2.11}$$

The solution of this equation is related to the condition that the power entering the P region at x=0 is $P_o\,(1\text{-}R_f)$ (P_o is the incident on P), becomes

$$P(x) = P_0\left(1 - R_f\right)e^{-\alpha x} \tag{2.12}$$

where, P(x) is the power in the p region at any x and the fraction of power remaining at the end of the p region is $e^{-w_p\alpha}$ where w_p is the width of the p region. Therefore the power entering the depletion region (P_d) is

$$P_d = P_0\left(1 - R_f\right)e^{-\alpha w_p} \tag{2.13}$$

The depletion region will absorb some of the power, reducing the entering power by $e^{-\alpha W}$, so that the power absorbed by the depletion region becomes $P_d\,(1\text{-}\ e^{-\alpha W})$, where W is the width of the depletion region. The fraction of the power absorbed by the depletion region known as overall efficiency, η_0

$$\eta_0 = \left(1 - R_f\right)e^{-\alpha w_p}\left(1 - e^{-\alpha W}\right) \tag{2.14}$$

The speed of response of the photodiode is limited by the time taking to collect the carriers and by the capacitance of the depletion layer. Making the depletion region too wide increases the drift time of the carriers and reduces the frequency response. On the other hand, making it too thin results in a large depletion capacitance, which combined with the load resistance creates a huge time constant of R_LC.

To improve the efficiency and reduce the depletion capacitance the depletion region needs to be wider. There is a solution to solve this problem, which is to apply a large reverse bias across the diode which will increase the width of the depletion region as well as reduce the capacitance.

If the photodiode operates at 100% efficiency, the each photon of light striking the diode would result in one electron being added to the photocurrent. The quantum efficiency is related to the photodiode's responsivity by the following equation,

$$Q.E.[\%] = \frac{1.24x10^5 R(A/W)}{\lambda(nm)} \tag{2.15}$$

where, R is the responsivity, which can be expressed in practical units of amps of photodiode current per watt of incident illumination.

2.3.3 Linearity

Shown below is the equivalent circuit for a photodiode, under zero applied reverse bias. In this condition the photodiode current will divide between the internal junction or shunt resistance and the external load resistance.

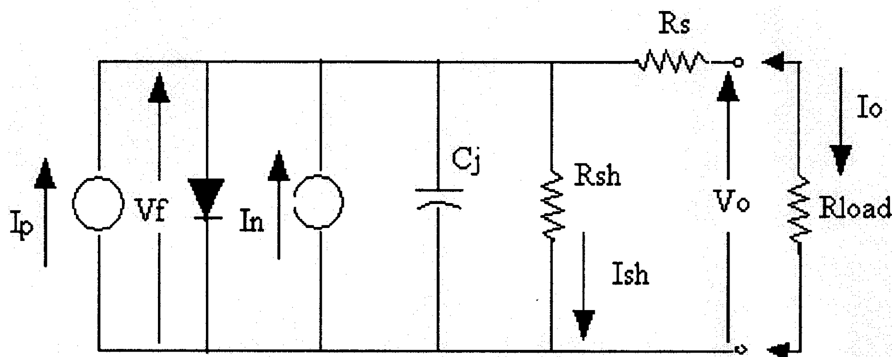


Figure 2.6 Equivalent circuit for a photodiode under zero applied reverse bias.

Symbols in equivalent circuit,

I_p = light generated photocurrent

V_f = forward voltage drop across diode

I_f = forward current through diode

I_n = noise current

C_j = junction capacitance

R_{sh} = shunt resistance

I_{sh} = shunt current

R_s = series resistance

V_o = output voltage

I_o = output current

For an ideal photodiode, R_s= 0 and R_{sh}= infinity.

$I_o=I_p-I_f$

If the external terminals are shorted a short circuit photocurrent I_{sc} will flow. When this happens, for the ideal case, V_f= 0= $I_{sc}R_s$ and $I_{sc}=I_p$

For real world case,

$$I_o = I_p - I_f - I_{sh}$$

$$I_{sc} = I_p - I_{sat}\left(e^{q(I_{sc}R_s)/KT} - 1\right) - (I_{sc}R_s)/R_{sh} \quad (2.16)$$

For the non ideal case, the second and third term of the above equation limit the linearity. In order to achieve good linearity, dark (shunt) resistance should be made as large as possible and the R_s should be made as small as possible.

2.3.4 Dark Current

The dark current is the leakage current that flows, when the photodiode is in the dark and a reverse vias is applied across the junction. This voltage may be as low as 10 mV or as high as 50 V and the dark currents may vary from pA to μA depending upon the junction area and the process used.

The dark current is temperature dependent. The rule of thumb is that the dark current will approximately double for every 10°C increase in ambient temperature. However, specific diode types can vary considerably from this relationship. One of the objectives of this project is to minimize the dark current as much as possible.

2.4 Back Illuminated Photodiodes

The structure of a conventional photodiode has been discussed earlier. There the light incidents on the device from the front side, as shown in Fig.2.1 and the electrical current created in the device is carried out by conductors to the front end electronics. This type of photodiodes is known as front illuminated photodiodes (FIP). FIP is named as such because the light is made to shine on the same side as the p- type diffusion or front. The major problem with the conventional front- illuminated photodiodes is the area used by the metal lines which run along the silicon surface. As the number of metal line increases it blocks the photodiode sensitive areas thus reducing the effective light sensitivity [4].

To resolve this problem back illumination photodiodes have been created. These photodiodes have the similar pattern of p- type regions as conventional photodiodes, but do not have the problem with the metal lines, because the photodiodes are illuminated from the back ends. Figure 2.6 shows a back illuminated photodiode (BIP) configuration.

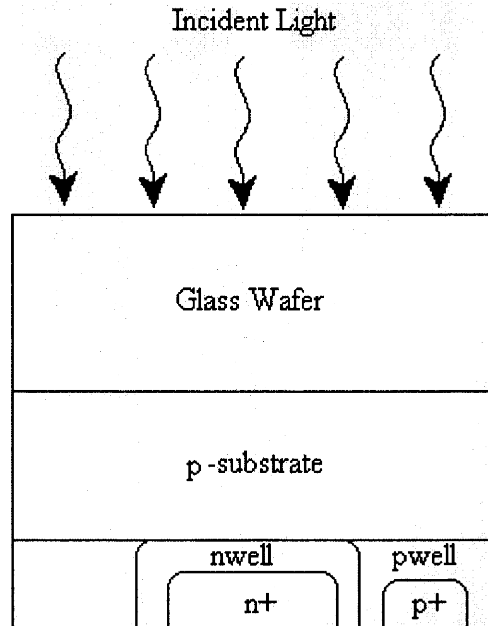


Figure 2.7 Cross-section through the back illuminated photodiode.

If a typical FIP is illuminated on its backside, the signal obtained will be small in comparison to normal front side illumination. This is because most of the photogenerated carriers created on the backside are lost due to the recombination as they travel through the substrate towards the anode on the front side.

There are three main criteria that make BIP more sensitive than a conventional FIP. First, the silicon used in the BIP has a longer minority carrier lifetime than is typically used in a FIP [4]. A long electron life time necessitates a p- type silicon wafer with high resistivity. The silicon used for this project has a resistivity around 50 Ω-cm. Second, the BIP is thinner than a typical FIP. While a typical FIP is 250 to 500 μm thick, the silicon wafer used in this project is made thinner to 60 μm. A thinner substrate helps to maximize the collected holes at the anode. The exact thickness chosen is a trade off between photodiode performance and fragility of the silicon chips. The third feature of

the BIP that may present in a FIP is the presence of p^+ region, which helps to separate the electron- hole pairs created by the light absorbed and pushed the holes away from the surface thus reducing the chance of surface recombination.

2.5 Modeling the Back-Illuminated Photodiodes

A photodiode is similar in structure to the p-n junction diode except that its junctions can be exposed to an external light source. The front of the wafer is heavily doped with the opposite dopant type compared to the substrate to form the p-n junction to produce a majority carrier diffusion across the junction. This p-n junction region is important in case of photodiode's efficiency as it converts the photons into electron-hole pairs. When photons of energy (hυ) penetrate and absorb into the silicon substrate with a higher energy compared to the band-gap energy of the silicon (1.12eV), then the absorbed photon will excite electron from valance band to the conduction band and leaves behind a hole in valance band, that's how it generates an electron-hole pair. When an electron-hole pair is generated inside the depletion region, these electrons and holes are rapidly drift in opposite direction by the built-in electron field. This produces the photocurrent flow. A p-type, <100> silicon wafer with resistivity of 50 Ω-cm was used for the fabrication. The n-well was formed by using phosphorus at energy of 170 keV and dose of $7x10^{12}$ cm^{-2} to obtain a depth of 1 μm. Similarly, boron was doped with energy of 70 keV and dose of $1x10^{13}$ cm^{-2} to obtain the p-well, with a depth same compared to n-well. An annealing for 30 minutes was then held after completion of these two steps to drive-in the charges. Once again, phosphorus implant (45 keV, $2x10^{14}$ cm^{-2}) and boron implant (30 keV, 2x 10^{14} cm^{-2}) were used to form n^+ and p^+ regions, respectively to obtain a depth around 0.4

μm. Figure 2.6 shows the layout schematic cross sectional view of the n-well/p-substrate photodiode. In this layout, the n-well and p-substrate become the cathode and anode regions, respectively of the photodiode. And n^+ and p^+ are used as the n-well and p-substrate ohmic contacts respectively. Hence, the p-n junction is formed.

In this process, a 200nm thick layer of silicon nitride was previously formed on the front side of the wafer to block the structures from any mechanical damage and the bonding pads were then opened to make the electrical connections. The key feature of this process is back thinning of the wafer, below the buried oxide. In this case, it is assumed that this procedure will allow the n-well/p-substrate device to directly exposed to the incident radiation and detect the penetration of high energy particles, as well as short range of low energy electrons in keV range [10,11]. The back-thinning will be performed by using both dry and wet etching in Reactive Ion Etching (RIE) and aqueous KOH, respectively. A support of a dummy wafer will be given to the front-side during the back thinning process. A highly transparent glass wafer will be then used to attach at the back-end of the wafer with optical glue. The dummy wafer will finally be removed to uncover the front end for required connections. By this unique process, it is expected to obtain good quality devices.

CHAPTER 3

SIMULATION, TEST STRUCTURES AND MEASUREMENTS

3.1 Simulation Results from SRIM

The energy and the dose that will be used for implantation in n-well, p-well, n+ and p+ regions were computed using the initial simulation results using SRIM (Stopping Range of Ions In Matter) and TSUPREM. The energy of the implanted ions will be selected depending upon the projected range that was obtained from both simulation results.

3.1.1 Simulation of Implanted Range

The SRIM simulations were carried out for both boron implantation and phosphorus implantation. The data extracted from the simulations results were the implantation-projected ranges and the implantation damages. The number of ions, selected for the simulation, was 99999 for all various cases to obtain the acquired results. The projected range for various conditions is demonstrated in Figure 3.1, where the projection view in the X-Y direction of the implanted ions in to the substrate is demonstrated. The X-axis shows the target depth (um) and the Y-axis has units of (atoms/cm^3) / (atoms/cm^2) which when multiplied by the dose of the implanted ions yields the concentration. The n-well was formed by using phosphorus at energy of 170 keV and dose of 7×10^{12} cm^{-2} to obtain a depth of 1 μm. Similarly, boron was doped with energy of 70 keV and dose of 1×10^{13} cm^{-2} to obtain the p-well, with a depth same compared to n-well. An annealing for 30 minutes was then held after completion of these two steps to drive-in the charges. Once again, phosphorus implant (45 keV, 2×10^{14} cm^{-2}) and boron implant (30 keV, 2×10^{14} cm^{-2}) were used to form n$^+$ and p$^+$ regions, respectively to obtain a depth around 0.4 μm.

Figure 2.6 shows the layout schematic cross sectional view of the n-well/p-substrate photodiode. In this layout, the n-well and p-substrate become the cathode and anode regions, respectively of the photodiode. And n^+ and n^+ are used as the n-well and p-substrate ohmic contacts respectively. Hence, the p-n junction is formed. The projected range and straggle were calculated and provided in Figure 3.1.

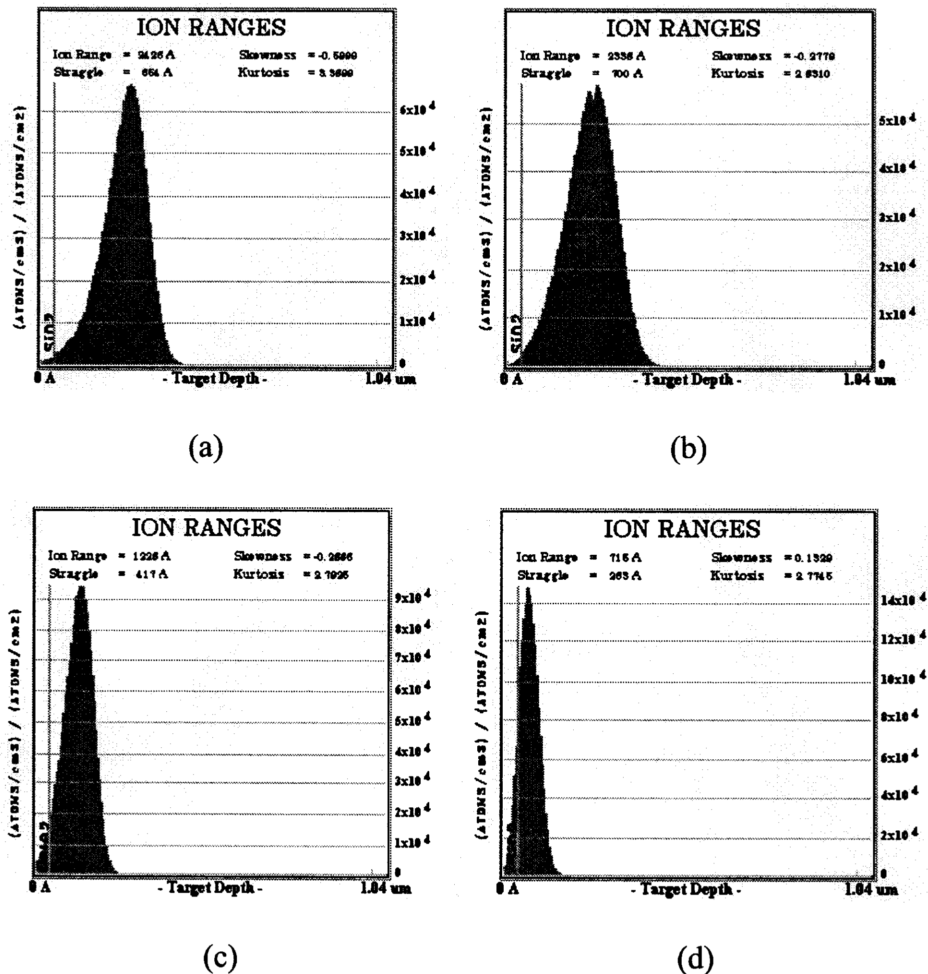


Figure 3.1 Various ion ranges in different regions, (a) in n-well, (b) in p-well, (c) in n^+ and (d) in p^+.

The peak concentration of implanted ions can be obtained from the given equation

$$N = 0.4 * \frac{\phi}{\Delta R_p} \quad \text{atoms/cm}^{-3} \qquad (4.1)$$

Where, Δ Rp is the projected straggle which is obtained from the simulation results. Φ is the dose of the ions, which is in atoms cm^{-2}. Table 3.1 shows the peak concentration for different regions obtained from the SRIM simulation results.

Table 3.1 Peak Concentrations of Dopants at Different Implanted Regions

	nwell	ppwell	n^+	p^+
Peak Concentration (atom/cm^3)	$4.3x10^{17}$	$5.7x10^{17}$	$1.9x10^{19}$	$3.0x10^{19}$

3.1.2 Damage Simulation

The damages created in the silicon substrate, due to implantation of various atoms was also observed by SRIM simulations. The damages, due to phosphorus and boron implantations with different doses and energies are shown in the Figure 3.2.

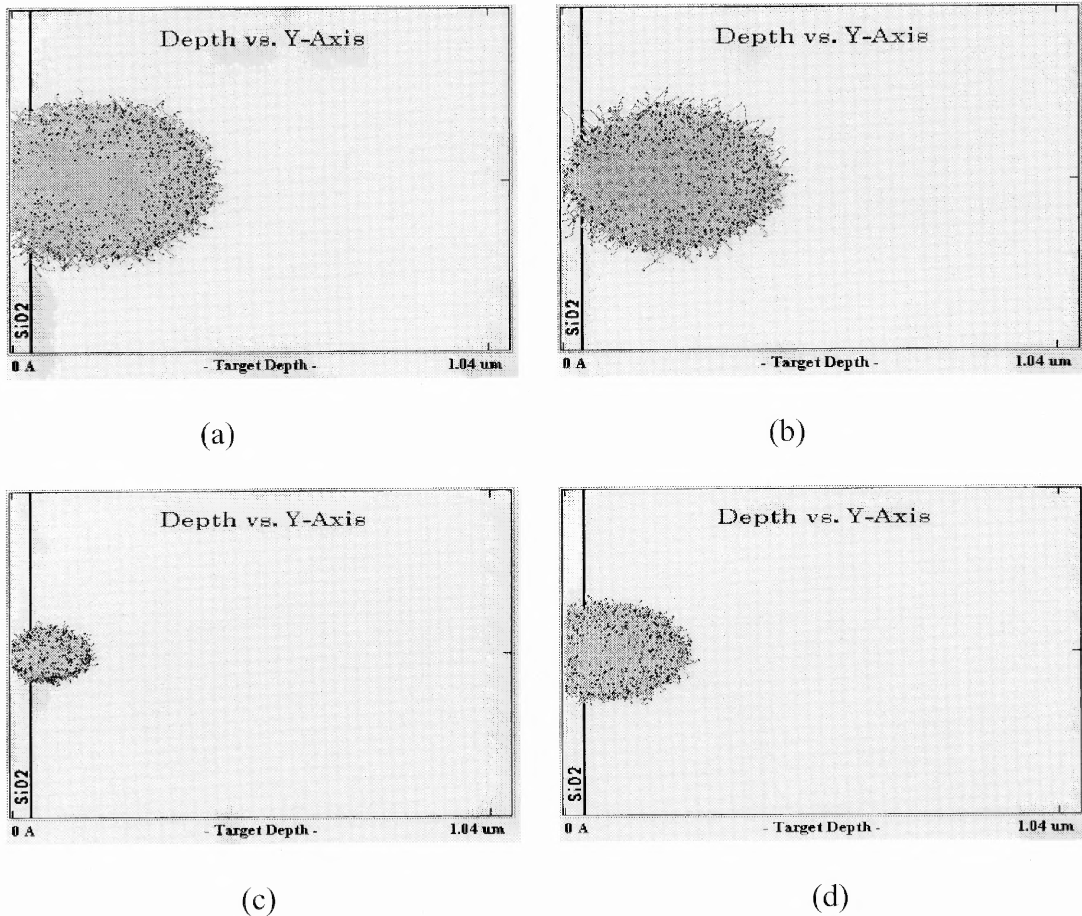


Figure 3.2 Defects generated at different regions, (a) in n-well, (b) in p-well, (c) in p^+ and (d) in n^+.

3.2 Simulation Results from TSUPREM

TSUPREM simulations were carried out for all four regions (n-well, p-well, n^+, p^+), before and after annealing. Here, mainly the doping concentrations for various energies and doses were observed to obtain specific depths of different regions. The required depth, to obtain shallow n-well and p-well junctions was chosen to be 1μ and for n^+ and p^+ regions the depth was assumed to be 0.5μ. Phosphorus, with a dose of $7x10^{12}$ atoms/cm^2 and energy of 170 KeV was first doped in the device to create n-well region with a required junction depth and similarly Boron was doped with a dose of $1x10^{13}$ atoms/cm^2 and energy of 70 KeV to create a p-well region with same junction depth. A

common 30 minutes annealing at 1100°C, in nitrogen atmosphere, was followed after n-well and p-well implantations to achieve the required distribution of dopants. The n^+ and p^+ regions were doped by phosphorus and boron atoms, respectively, with higher energies and doses and followed by a common annealing in nitrogen ambient for 5 minutes at 950°C to achieve required junction depths. The simulated results are shown from Figure 3.3 to Figure 3.10. The doping profiles of different regions are given in the Table 3.2.

Table 3.2 Doping Summery of Various Regions

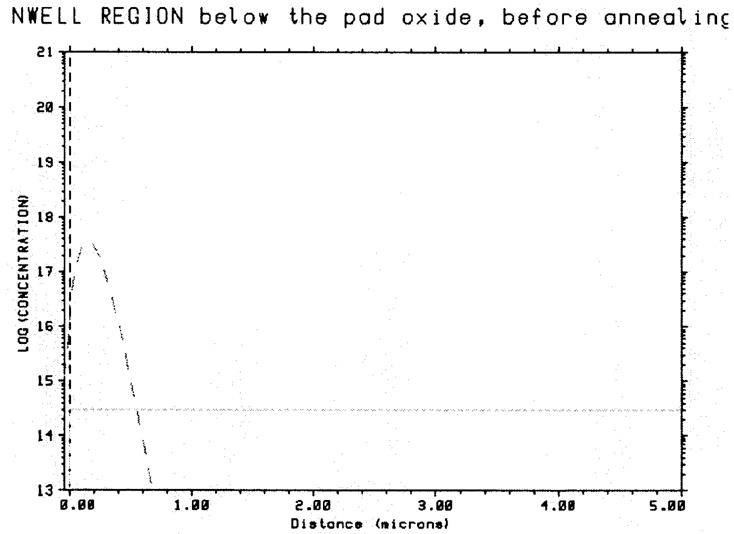
I/I	Species	Energy (KeV)	Dose (atom/cm^2)	Anneal
nwell	Phosphorus	170	$7x10^{12}$	1100°C/30min
pwell	Boron	70	$1x10^{13}$	
n+	Phosphorus	45	$2x10^{14}$	950°C/5min
p+	Boron	30	$2x10^{14}$	

Ion implantation, in semiconductor technology, is a process where high energy impurity atoms can be introduced into a single-crystal substrate in order to change its electronic properties [12]. There are some disadvantages of this process, mainly the damage to the semiconductor. Annealing at an elevated temperature can solve this problem [13]. The implantation process is generally carried out in such a way, so that, it can avoid the possibility of channeling. The common approach for it is tilting the slice by an angle of 7- 10° along the 110 direction to prevent the alignment with the major crystal axis [12]. Even though, it is extremely hard to prevent the channel effect, since some of the ions can be deflected towards the channeling path and form a tail by penetrating deeper to the semiconductor. Generally, the tail is not observed in heavily doped semiconductors and gaussian profiles are obtained in these situations.

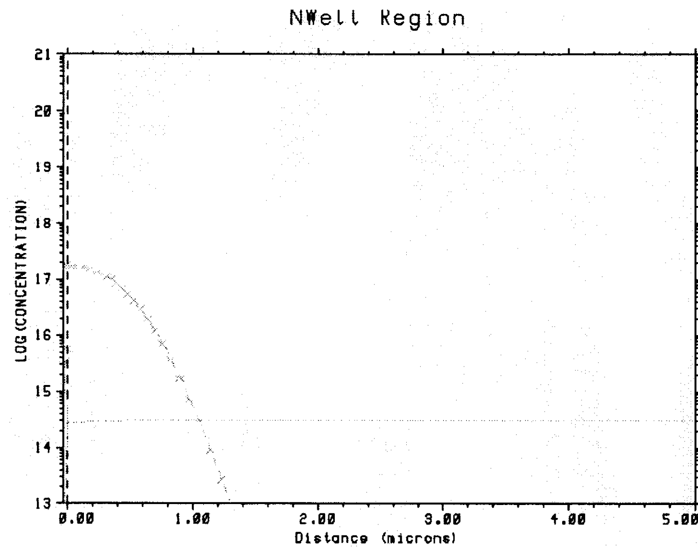
During ion implantation, the energetic ion makes collisions with the lattice atoms after entering the semiconductor. One ion can dislocate many of atoms before resting. The dislocated atoms, after getting transferred energies from the ions can also dislocate other atoms and thus produce a cascade of collisions. The damages created at different implanted regions are shown in Figure 3.2. It is clear from that figure is, light atoms (boron) have created less damage rather than the heavy atoms (phosphorus). In both cases, the volume of the damage is less than the volume of the target, where the impurity atoms hit.

Ion implantation damage results in the degradation in semiconductor quality by reducing the values of parameters such as mobility, minority carrier lifetime and space-charge generation lifetime. Generally, the peak of the ion damages take place near to the surface of the semiconductor [12], i.e., away from the depletion layer, which can be found from Figure 3.3 (a), 3.4 (a), 3.5 (a) and Figure 3.6 (a). During the annealing, the displaced atoms try to repair the damages. At the same time, more damage can create during annealing, which can be prevented by high temperature annealing at 1000-1200°C. At this temperature both the heavily and lightly doped impurity atoms get enough activation energy to move into the lattice sites and become electronically active, which increase the mobility and the lifetime of the atoms. After annealing the n-well and p-well regions, the profiles show in Figure 3.3 (b) and 3.5 (b), that the large fraction of the doses are in the silicon, while the profiles in Figure 3.4 (b) and 3.6 (b) show that the halves of their doses are in the oxide (due to comparatively large oxide thickness). In Figures 3.3, 3.4, 3.5 and 3.6, Gaussian distributions of dopants are observed after annealing at 1100°C for 30 minutes. Still after annealing at 950°C for 5 minutes, in Figures 3.7(b), 3.8(b),

3.9(b) and 3.10(b), it is observed that the distributions have little tails, which shows that still the there is some defects.

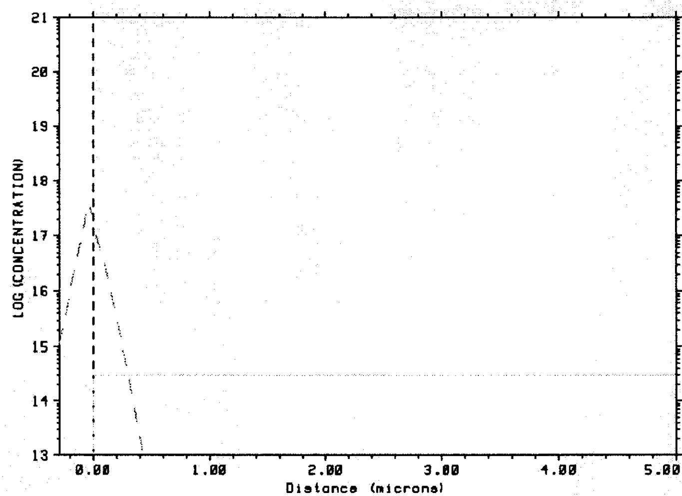


(a)

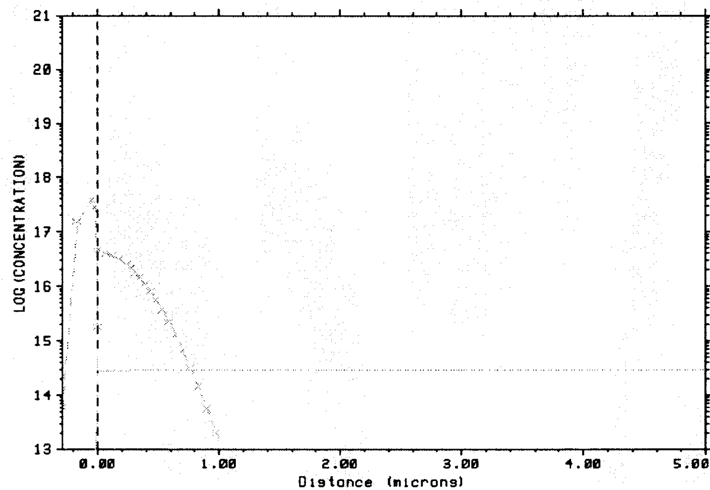


(b)

Figure 3.3 Doping concentrations of n-well region below the pad oxide, (a) before and (b) after annealing.

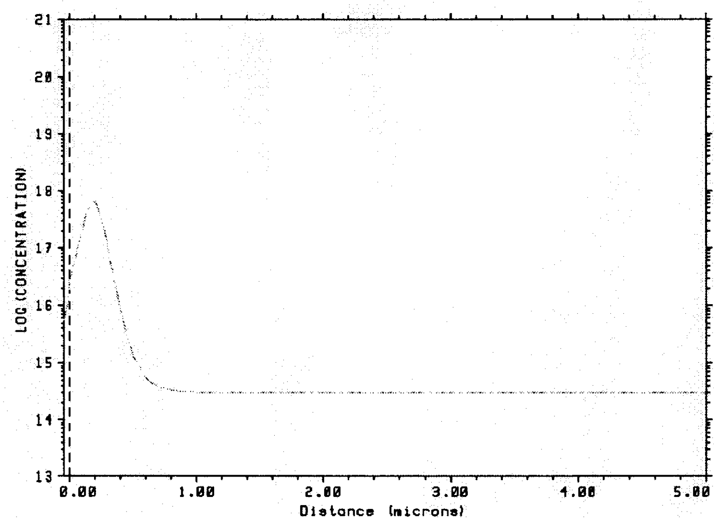


(a)

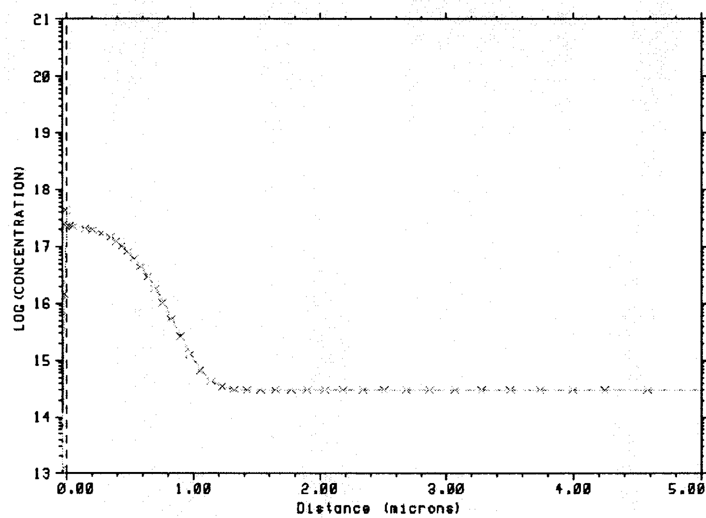


(b)

Figure 3.4 Doping concentrations of n-well region below the field oxide, (a) before and (b) after annealing.



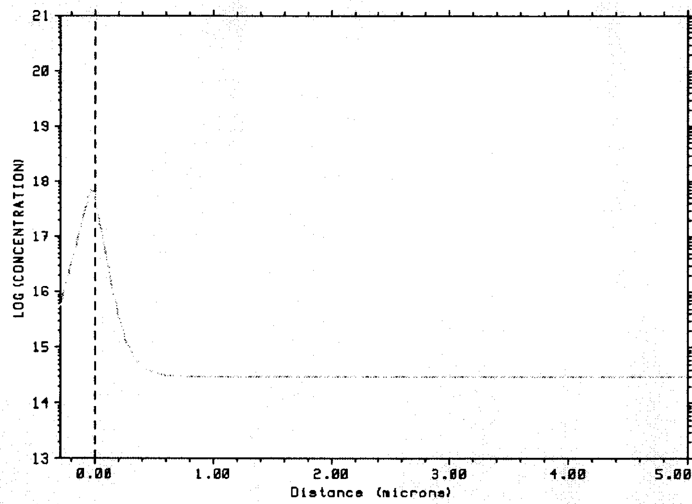
(a)



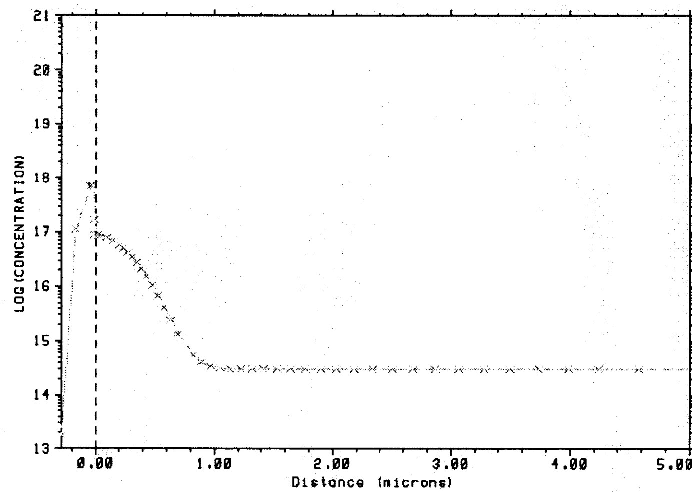
(b)

Figure 3.5 Doping concentrations of p-well region below the pad oxide, (a) before and (b) after annealing.

Figure 3.6 shows the doping concentration of p-well region just after the implantation. It also shows the dopant distribution after annealing at 1100°C for 30 minutes.

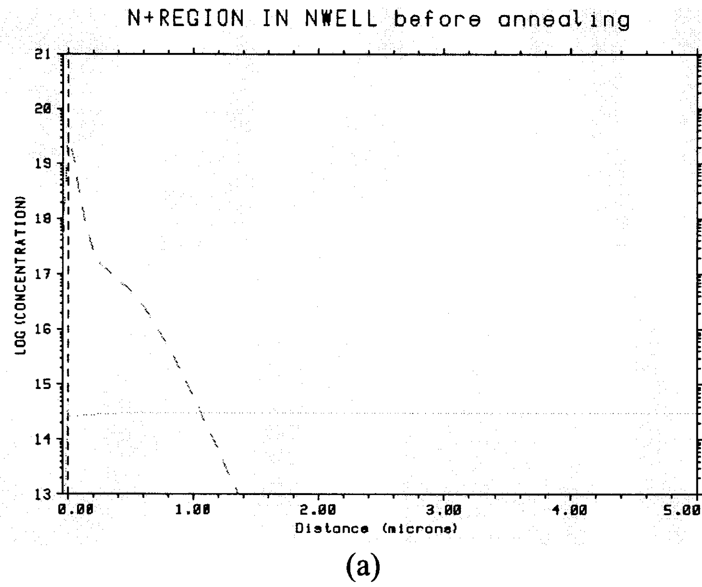


(a)

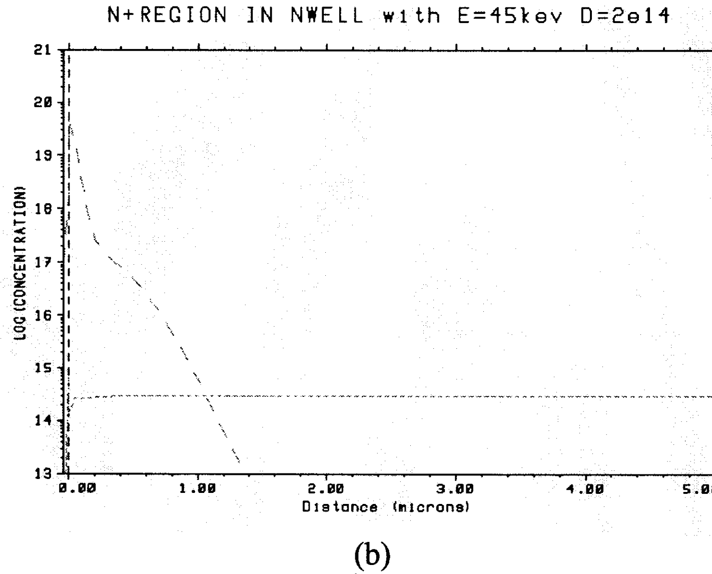


(b)

Figure 3.6 Doping concentrations of p-well region below the field oxide, (a) before and (b) after annealing.

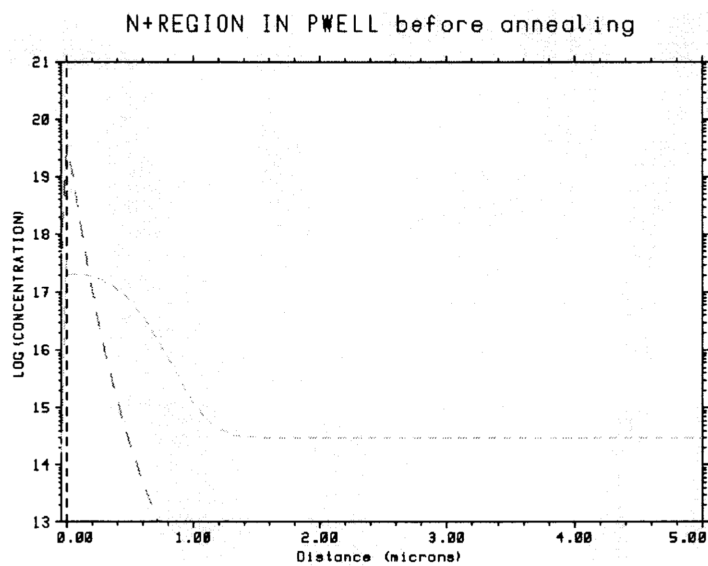


(a)

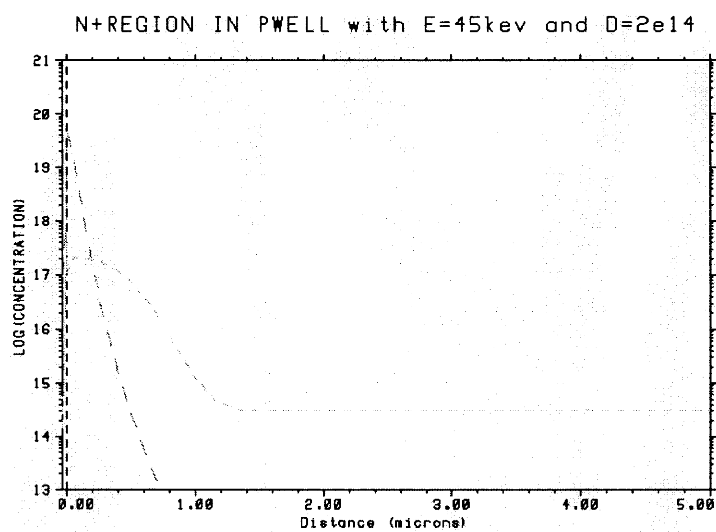


(b)

Figure 3.7 Doping concentrations of n^+ region in n-well, (a) before and (b) after annealing.



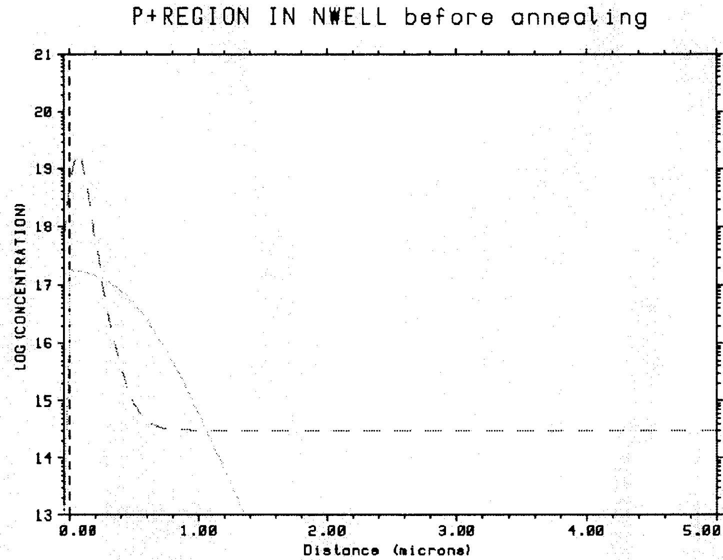
(a)



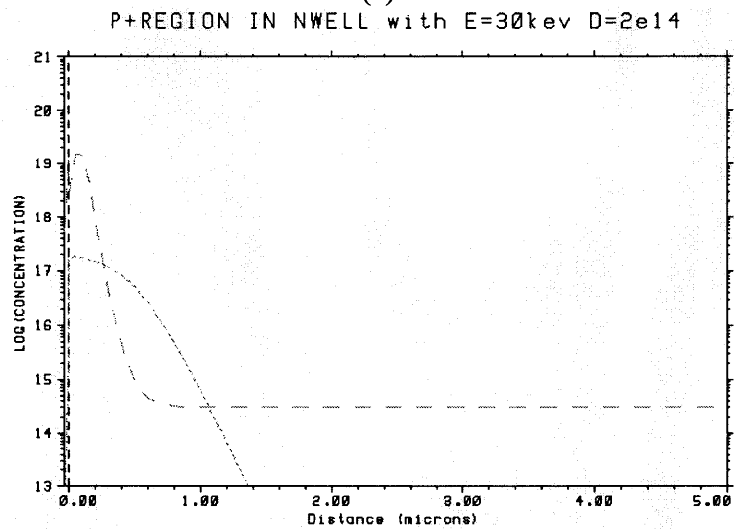
(b)

Figure 3.8 Doping concentrations of n^+ region in p-well, (a) before and (b) after annealing.

Figure 3.9 shows the doping concentration of p+ region just after the implantation. It also shows the dopant distribution after annealing at 950°C for 5 minutes.

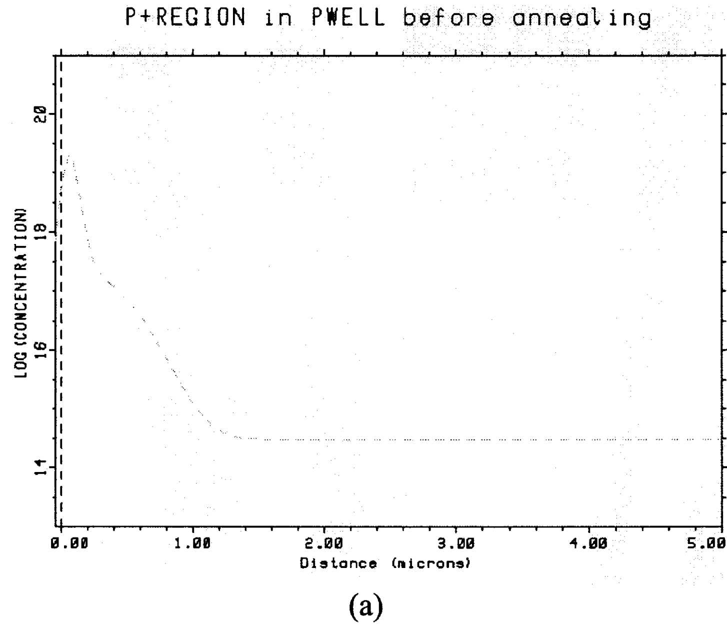


(a)

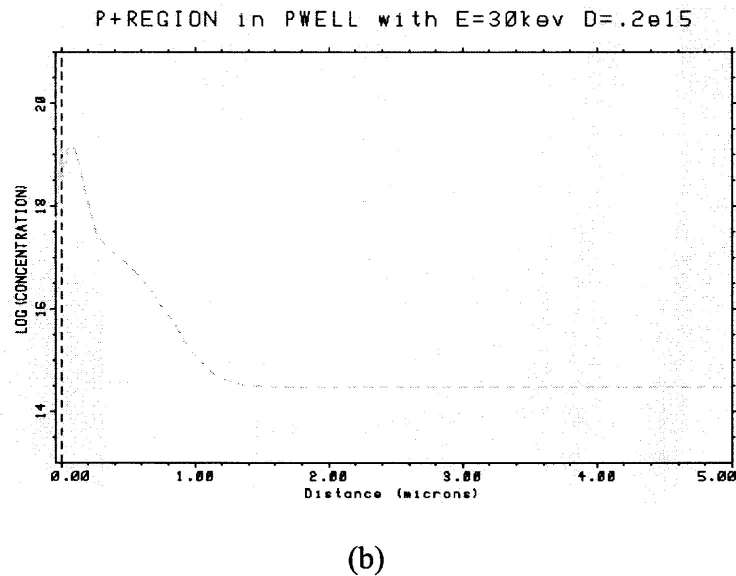


(b)

Figure 3.9 Doping concentrations of p^+ region in n-well, (a) before and (b) after annealing.



(a)



(b)

Figure 3.10 Doping concentrations of p^+ region in p-well, (a) before and (b) after annealing.

3.3 Simulated Leakage Current by TCAD MEDICI

The dark-current/ reverse bias voltage curve was simulated after specifying one diode structure and its doping concentrations for various regions. It is seen in the Figure 3.11 that the photodiode achieved no dark current till the voltage value of -1.5 V.

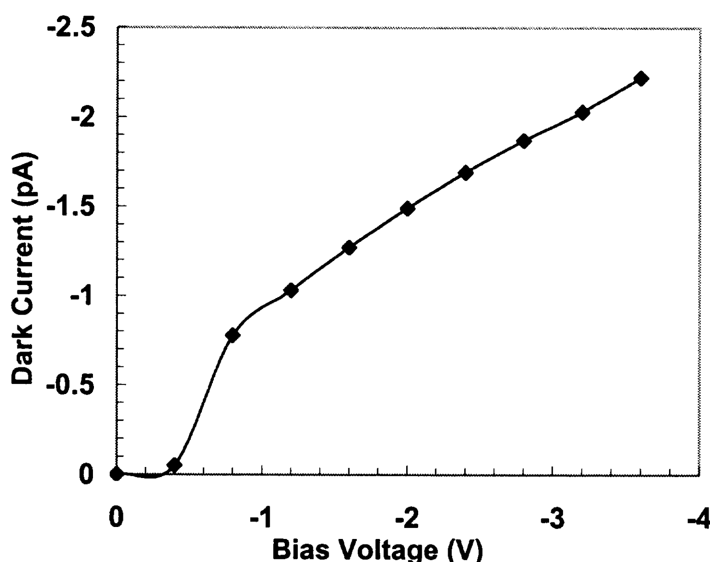


Figure 3.11 Dark current as a function of bias voltage.

3.4 Test Structures Modeling for Different Levels of Fabrication and Results

The microelectronic test chip is an auxiliary test device that is manufactured along with product circuits on wafers. It is made-up of device-like structure, which is necessary to measure variety of means to insure the proper device processing steps. Sometime, these structures are very important to measure the data that are impossible to get from product circuit. Test chips, or as they are sometime called, process control monitor (PCMs), are used in the multi-circuit wafer environment to determine acceptance or rejection of wafer lots, rather than by actual circuit performance. Here, mainly the test structures were formed to evaluate the uniformity of the semiconductor doping processes, the quality of the contacts.

3.4.1 Greek-Cross Structure

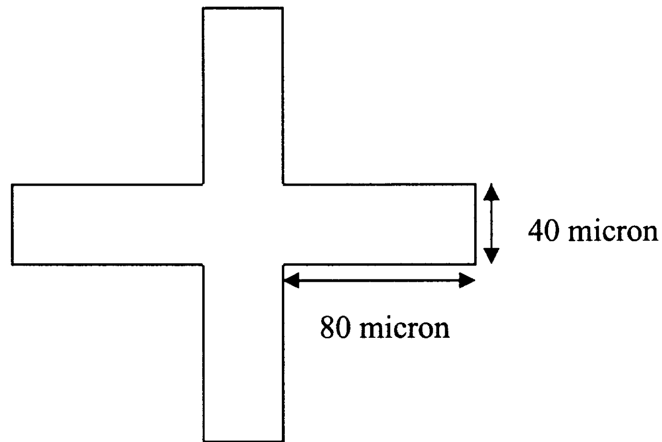


Figure 3.12 Greek-cross structure.

The above figure shows a modified four- point probing technique, called Greek- Cross structure, for measuring the sheet resistance (R_s) directly from the implanted areas. This structure was used to obtain R_s from n well, pwell, n^+ and p^+ regions in the same way.

The method for extracting sheet resistance from Greek- Cross structure is a simple process. Here current is forced between two adjacent arms (eg, north- east) and the voltage difference is measured between the other two (south- west) [14, 15]. The sheet resistance R_s is given by,

$$R_s = \pi/\ln(2) .V/I\ \Omega/\square \qquad (3.1)$$

where, V is the applied voltage between two adjacent nodes in volts and I is the measured current between other two adjacent nodes.

The current direction was reversed and the measurement repeated. The current forcing terminals were moved by 90° (now south- east) and two measurements of voltage repeated as above. This process can be repeated for 180° and 270° to get over all eight

different values of sheet resistances. It is suggested that use of eight measurements improve the accuracy of measured sheet resistance [10].

Layout of different greek-cross structures for different regions are shown below-

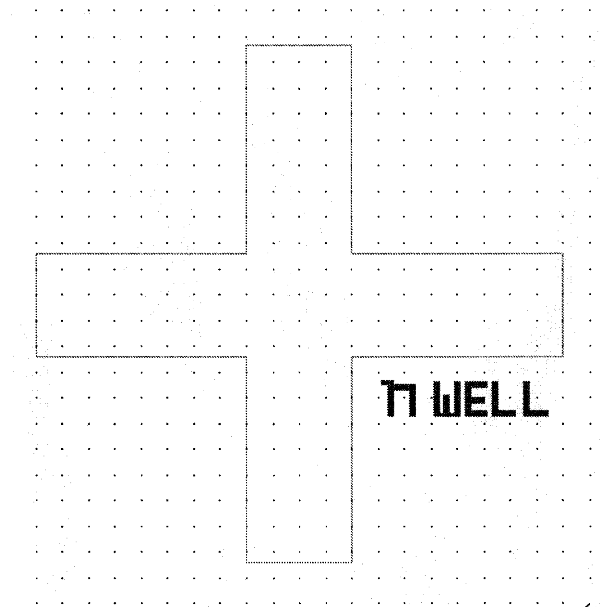


Figure 3.13 Greek-cross structure for n-well region.

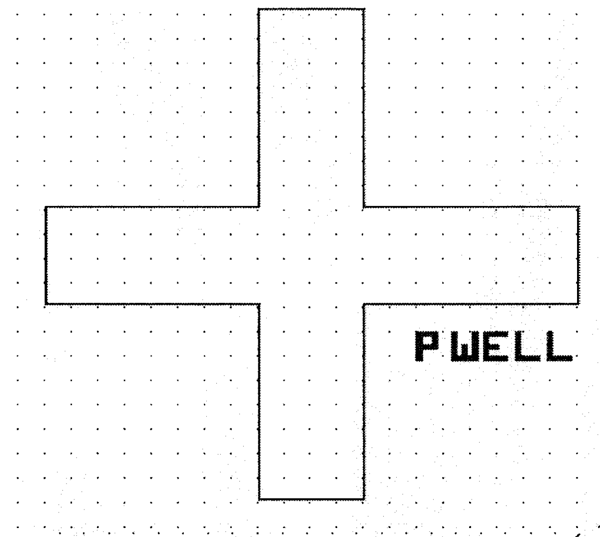


Figure 3.14 Greek-cross structure for p-well region.

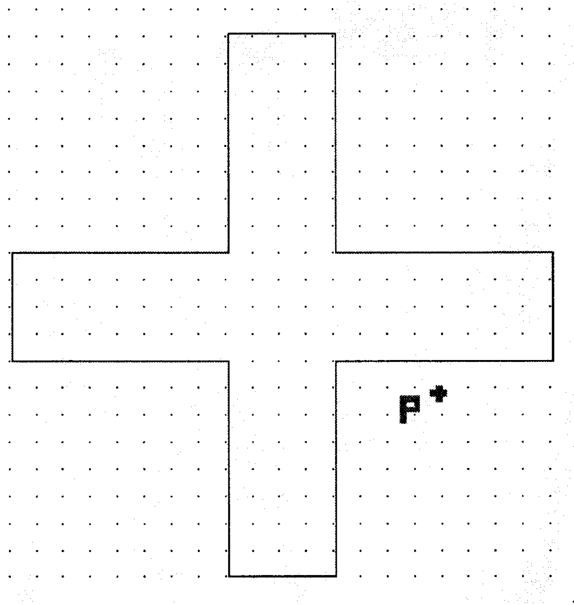


Figure 3.15 Greek-cross structure for p^+ region.

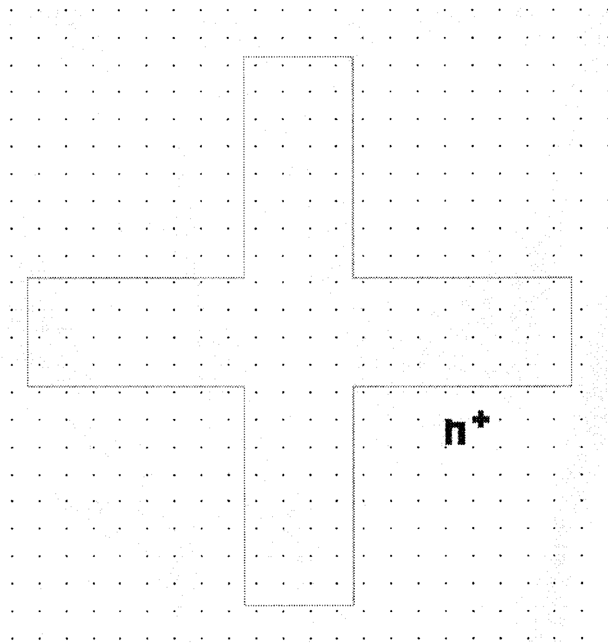


Figure 3.16 Greek-cross structure for n^+ region.

Table 3.3 Measured Sheet Resistances at Different Implanted Regions

	nwell KΩ/□	pwell KΩ /□	n^+ Ω /□	p^+ Ω/□
Measured Sheet Resistance	5.44	3.62	4.53	22.65
Calculated Sheet Resistance	6.90	3.90	5.56	27.78

3.4.2 Kelvin Resistor Structure

The kelvin resistor structure was used to extract the resistance density from electrical measurements. In this process, a specific current was given from the implanted level up into the metal level through the contact window as shown in Figure 3.17 (a). A voltage is measured between the two levels using two other terminals. The contact-resistance measured for the structure is the voltage divided by the source current.

The kelvin resistor structure was used for testing the active area-metal contact integrity. Kelvin resistors for the test chip were designed with contact size of 2 μ x 2 μ. The contact resistance is,

$$R_c = V_{14}/I_{32} \tag{3.2}$$

The resistance density is,

$$\rho_c = R_c \times A \tag{3.3}$$

where, A is the contact window area (cm^2), R_c is the contact resistance(Ω) and ρ_c is the contact resistance density ($\Omega\text{-}cm^2$)

Table 3.4 Measured Contact Resistances at Different Voltages in Kelvin Structure

	0.2V	0.5V	1V
Measured Contact Resistance (Ω)	6.87	6.41	5.26

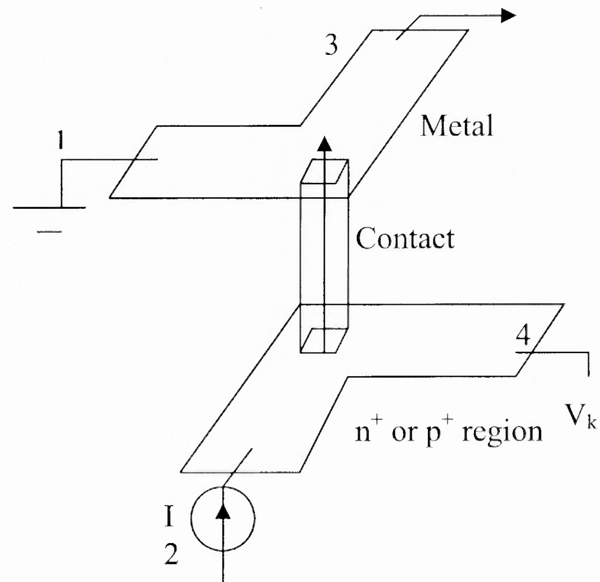


Figure 3.17(a) Kelvin resistor structure showing metal-n+ region contact.

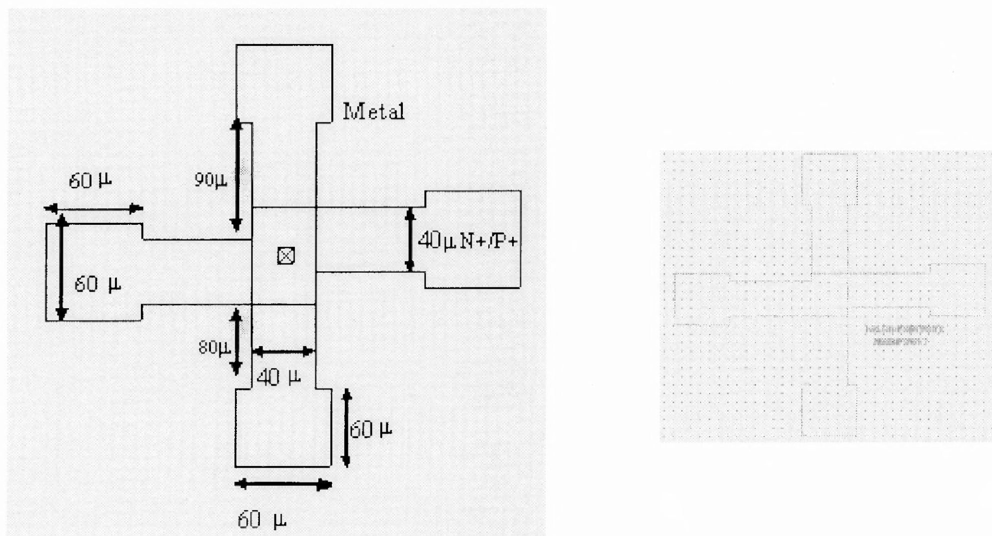


Figure 3.17(b) Kelvin resistor structure showing dimensions of each arm.

The top view of the kelvin resistor is shown in the Figure 3.16 (b), which mainly describes the connection between metal and n^+ region.

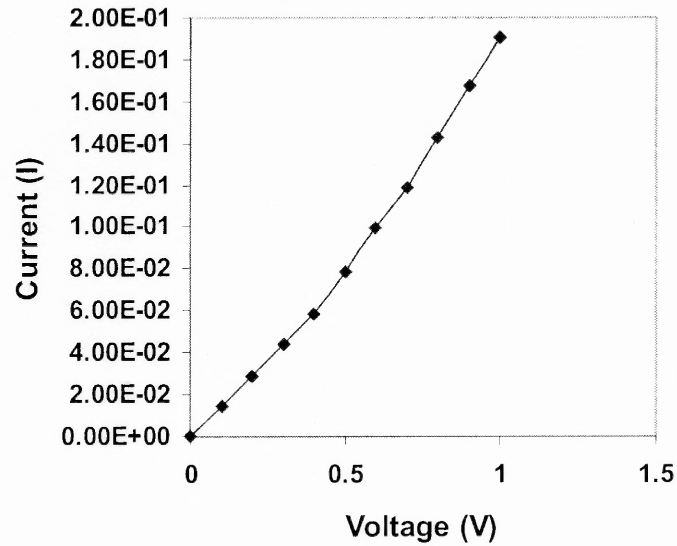


Figure 3.18 Measured current at different applied voltages in Kelvin structure.

3.4.3 Contact Reliability Test

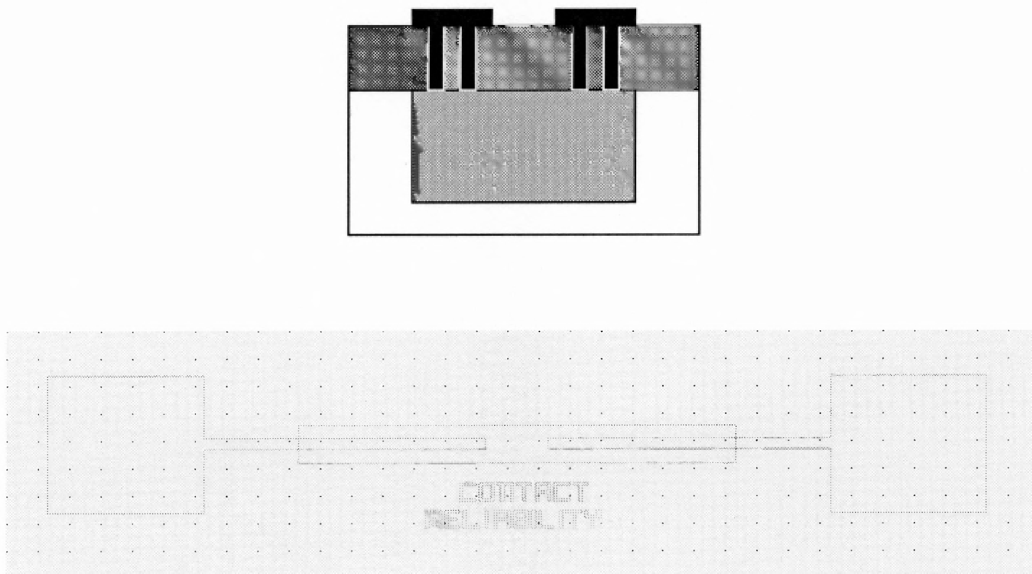


Figure 3.19 Cross section and layout of the structure to test the contact reliability.

In this case by using the contact reliability test structure, it was easy to estimate the resistance across the metals. The proper results ensured contacts were etched properly. Also by seeing the variation in resistances at different positions, it would be easy to

differentiate the quality of etching. By this test it will be able to determine the fault during fabrication.

Table 3.4 Measured Contact Resistances at Different Voltages

	0.2V	0.5V	1V
Measured Contact Resistance (Ω)	5.71	5.8	5.78

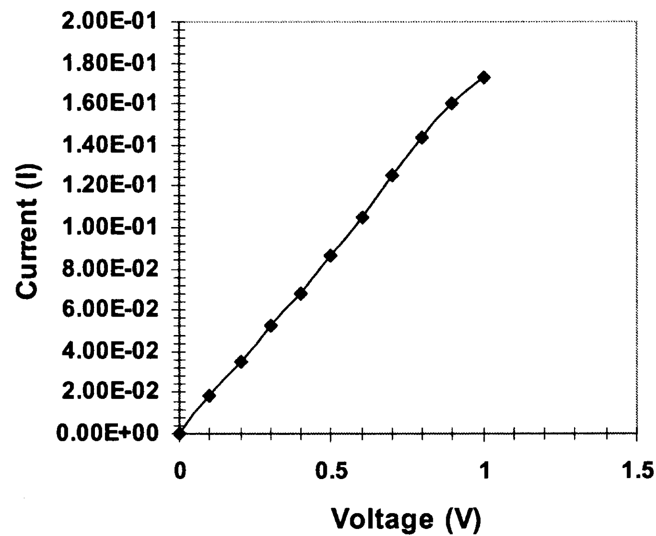


Figure 3.20 Measured current at different applied voltages for contact reliability test.

CHAPTER 4

DEVICE FABRICATION

4.1 Fabrication Steps

After simulation of leakage current and various implantation conditions, the devices were then fabricated. The most of the work was held in the Microelectronics Research Center at NJIT which is a class 10 clean room. The wafers were sent to Core Systems, CA for NWell, PWell, N^+ and P^+ implantations. The whole fabrication was completed in various steps using different instruments including: Wafer Inspection - microscope, Dektak profilometer, wet chemical station, semi-tool spin/rinse dryers, nanometrics FTM, inspection microscope, MTI coat and develop system, Drytek reactive ion etching system, varian sputtering system, BTU diffusion furnace, PECVD furnace, MG Industries gas cabinets etc. A detailed description of the individual process steps are given below in section 4.1.1 through 4.1.28.

4.1.1 Starting Material

The starting material for this process was 6 inch, p-type (boron doped), <100> oriented CMOS grade SOI wafers, with a sheet resistivity of 20-50 Ω-cm.

4.1.2 Cleaning the Wafers

The cleaning is an important part before each process mainly prior to any high temperature process because if there is any contaminant at that time, they will react and diffuse into the device at a higher rate in an elevated temperature.

As a first step of the cleaning process, the wafers were cleaned in the primary and secondary bath of m-pyrol (methyl pyrolidine) for 10 minutes each. M-pyrol is an acidic mixture which was used to remove the organic contaminants from the wafer surface at an elevated temperature of 95° C. P-clean, H_2SO_4 (75%) and H_2O_2 (25%), is an aqueous alkaline solution that removes organic contaminants from the wafers at an elevated temperature of 110°C. Wafers were subjected to P-clean after m-pyrol clean. A surface pre-clean at 100:1 H_2O: HF was done to remove thin oxide layer from the surface of the wafers, which may form for the atmospheric oxygen. The wafers were rinsed in DI water after completion of each cleaning step to remove any kind of residue.

4.1.3 Denuding

Each wafer was scribed on the back for identification. An oxide layer of approximate thickness of 800Å was grown by steam oxidation at 950°C for 40 minutes. This oxide layer was subsequently stripped using 6:1 BOE (buffered oxide etch). This step helped in the removal of impurities and contaminants from the wafer surface prior to actual processing.

Impurities can degrade the performance the circuit or even cause failure. This is even true for VLSI circuits, with extremely small devices operating at low voltages. For high yield and reliability, it is necessary to eliminate all possible sources of contamination.

4.1.4 Pad Oxidation

Wet oxide of thickness 400Å was first grown on the top of the SOI wafers at a temperature of 950°C with a flow rate of 3.5 SLM oxygen and 530 SCCM H_2O flow (bubbler). After removing the wafers from the furnace the thickness of each wafer was measured and found uniform thickness and good quality of the grown oxide.

4.1.5 PECVD Nitridation

A PECVD nitride of thickness 1250Å was then formed on the top of the pad oxide at 350°C with the SiH_4-NH_3 reaction. The process was carried out at a pressure of 900 mTorr.

4.1.6 Photolithography of Active Area

A process of photolithography was conducted to create the active area of the devices. In this process, first the wafers were coated with Shipley 1813 photo resist for 1 minute at 2000 r.p.m. After applying the resist the wafers were hard baked at 115°C for 1 minute and then soft baked for 1 more minute. The wafers were then exposed in the active mask for 22 second and developed.

In photolithography, a layer of polymeric photo resist (PR) was applied as a thin film to the substrate and subsequent exposed through a mask. The mask contains clear and opaque features that define the patterns to be created in the PR layer. The areas in the PR exposed to the light were soluble (positive photo resist) in a specific solvent known as developer. To start, the wafer was first coated with a pre-resist coating of a material designed for better photo resist adhesion. The wafers were then ready to be coated with

photoresist. Spin coating is the most widely used technique to apply a uniform and adherent film of desired thickness. This procedure was carried out by dispensing the resist solution on the wafer surface, and then rapidly spinning the wafer until the resist was essentially dry. After the wafers were coated with resist, they were subjected to a temperature step, called soft-bake. This step accomplished several important goal including improving adhesion of the resist. After the wafer had been coated with resist and suitably soft- baked, it was ready to be exposed in UV ray in order to create the patterns in it. The degree of exposure was adjusted by controlling the energy impinging on the resist. Following exposure, the resist film was made to undergo development in order to leave behind the image, which would serve as the mask for etching. The wafer was then spin dried and transported to the post- bake module. Following development, an inspection was performed to insure that the steps of the PR process up to this point had been performed correctly and within specified tolerance. Post-baking was then performed just prior to etching. Its major reason was to confirm that the residuals of the solvents and developer had been totally removed.

4.1.7 RIE of Nitride

Reactive Ion Etching of nitride was performed by Drytek Phantom etch station. The main objective of this process was to remove the unwanted nitride layer from the surface, more specifically from those places, which were not covered by the photo resist.

It was performed with 50 sccm Sulfur hexafluoride (SF_6) with RF power of 300W and pressure of 200mTorr for few minutes. The wafers were then checked in the DEKTAK and ellipsometer to ensure the total nitride removal.

After removal of nitride the photo resists were removed by mpyrol cleaning and P-cleaning.

4.1.8 LOCOS Formation

The oxide was formed to those areas of the wafer, where there were no nitride layers. Here, nitride was used as a mask to protect certain regions on the wafer from the formation of unwanted oxide.

The LOCOS was formed by steam oxidation process at a temperature of 1050°C with a flow rate of 3.5 SLM oxygen flow and 530 SCCM H_2O flow (bubbler) to obtain a 2500Å thick oxide.

4.1.9 Silicon Nitride Stripe

After formation of the oxide, it was found that a thin layer of silicon oxy-nitride had formed on the top of the nitride region, which was then removed by a combination of wet etching with 100:1 H_2O/HF for few seconds and RIE for of oxide for very few seconds. These two processes were able to remove the oxy-nitride layer completely from the top of the nitride.

Finally, silicon nitride was removed from the wafers by using hot phosphoric (H_3PO_4) acid at a temperature of 170°C.

4.1.10 Photolithography of n-well

The same process of photolithography was followed for n-well region as used in case of Active region formation. In this process, first the wafers were coated with Shipley 1813

photo resist for 1 minute at 2000 r.p.m. After applying the resist the wafers were hard baked at 115°C for 1 minute and then soft baked for 1 more minute. The wafers were then exposed in the active mask for 22 second and developed. After developing and inspecting the wafers, the wafers were hard baked at a temperature of 120°C for 5 min in the oven to make them ready for sending for implantation.

4.1.11 Implantation of n-well Region

The wafers were sent to the company to implant phosphorus to create the n-well region. The implantation condition for n-well region is shown in Table 4.1.

Table 4.1 n-well Implantation Conditions.

I/I	Species	Energy	Dose	Annealing
N-Well	Phosphorus	170 KeV	$7x10^{12}$	None

4.1.12 Formation of p-well, n^+ and p^+ Regions

The formation steps for p-well, n^+ and p^+ regions are same as the n-well region. It consists of Photolithography and implantation. The implantation conditions and annealing temperatures for various regions are given below in Table 4.2. First annealing was done at 1100°C for 30 minutes just after p-well implantation to drive both n-well and p-well regions up to 1μ depth. The next annealing was held after p^+ implantation at a temperature of 950°C for 5 minutes to drive both n+ and p+ regions to a depth of 0.5 μ.

Table 4.2 Implantation Conditions for Various Regions

I/I	Species	Energy	Dose	Annealing
p-well	Boron	70 KeV	$1x10^{13}$	1100°C for 30 min
n^+	Phosphorus	45 KeV	$2x10^{14}$	None
p^+	Boron	30 KeV	$2x10^{14}$	950°C for 5 min

4.1.13 LTO Deposition

A 2000Å thick layer of Low Temperature Oxide (LTO) was deposited on the top of the wafer by using PECVD process. The process was carried out by using 400 sccm of SiH_4 and 900 sccm of NO_2 at an elevated temperature of 150°C with a pressure of 900 mTorr.

4.1.14 Photolithography of Contact Areas

After doing the LTO, the photolithography was performed on the wafers (by using CONTACT mask) in the same way as performed in case of Active region formation. In this process, first the wafers were coated with Shipley 1813 photo resist for 1 minute at 2000 r.p.m. After applying the resist the wafers were hard baked at 115°C for 1 minute and then soft baked for 1 more minute. The wafers were then exposed in the contact mask for 22 second and developed. After developing and inspecting the wafers, the wafers were ready for etching.

4.1.15 Etching the Oxides from Contact Areas

The oxide was etched by using Drytek Phantom etch station. The etching was performed at a temperature of 25°C (room temperature) in presence of 50 sccm CF_4, with a pressure of 50 mTorr and a RF power of 100 watts.

4.1.16 Photo Resist Strip

After etching and inspecting the wafers, the photo resists were removed by using m-pyrol cleaning and P-cleaning.

4.1.17 Deposition of Aluminium

After following the several steps, the aluminium of thickness, 3000Å was finally deposited on the top of the wafer by sputtering process to make contacts with the active regions and also to form metal lines. The deposition of the metal was held using sputtering process.

4.1.18 Photolithography of Metal

After depositing the metal, the photolithography was performed on the wafers (by using METAL mask) in the same way as performed in case of active region formation. In this process, first the wafers were coated with Shipley 1813 photo resist for 1 minute at 2000 r.p.m. After applying the resist the wafers were hard baked at 115°C for 1 minute and then soft baked for 1 more minute. The wafers were then exposed in the contact mask for

22 second and developed. After developing and inspecting the wafers, the wafers were ready for etching.

4.1.19 Etching of Metal

After photolithography was done, metal etching was done using aluminium etchant (phosphoric acid, nitric acid, acetic acid and de-ionized water) at 45°C. After metal etching, photo resist was removed using m-pyrol cleaning (methyl pyrolidine – an acidic mixture). The processing temperature was maintained at 95°C.

4.1.20 Removal of Photoresist and D_2 Annealing

After etching and inspecting the wafers, the photo resists were removed by using m-pyrol cleaning and P-cleaning. In the next step, a deuterium (D_2) annealing (50 % D_2 and 50 N_2) was done at a temperature of 400°C for 20 minutes.

4.1.21 Passivation Layer Formation

After removing the photo resist, a 2000Å thick PECVD nitride was formed on the top of the wafer as a passivation layer. The process was carried out in 400 sccm of SiH_4 and 40 sccm of NH_3 with a pressure of 900 mTorr at a temperature of 300°C. After forming the layer, the wafer was observed in DEKTAK to insure the required thickness.

4.1.22 Photolithography

The same process of photolithography was followed for pad opening as used in case of Active region formation. In this process, first the wafers were coated with Shipley 1813

photo resist for 1 minute at 2000 r.p.m. After applying the resist the wafers were hard baked at 115°C for 1 minute and then soft baked for 1 more minute. The wafers were then exposed in the PAD mask for 22 second and developed. After developing and inspecting the wafers, the wafers were hard baked at a temperature of 120°C for 2 min in the oven to make the wafers ready for etching.

4.1.23 Silicon Nitride Etching (Pad Opening)

Reactive Ion Etching of nitride was performed by Drytek Phantom etch station. The main objective of this process was to remove the unwanted nitride regions from the surface for pad opening, more specifically from those places, which were not covered by the photo resist.

It was performed in hot H_3PO_4 at 170°C for few minutes. The wafers were then cleaned in hot and cold DI water for 10 minutes each. Finally the wafers were checked in the DEKTAK and ellipsometer to ensure the total nitride removal.

4.1.24 Stripping of Photoresist

After removal of nitride the photo resists were removed by m-pyrol cleaning and P-cleaning.

4.1.25 Attaching Dummy Wafer on the Front side of the Wafer

By using a removable glue, OP-19, a Dummy wafer will be temporarily attached on the front side of the Si wafer in UV ray environment with a cure speed of 0.25-inch bead/ 20

sec. The dummy wafer will be attached to the front –end of the wafer to protect it from the DRIE.

4.1.26 Back-End Thinning by DRIE and Wet Etching

The process of deep reactive ion etching (DRIE) will be performed at a temperature of 20°C for few hours in an environment of 70 sccm silicon hexafluoride with pressures of 100W and 800W. Helium is generally used there to keep the temperature near to room temperature. By using DRIE and wet etching processes it is expected to remove a very thick (600μ) Si layer from the back end- of the wafer. Finally, a very thin layer of device will remained on the top of silicon oxide.

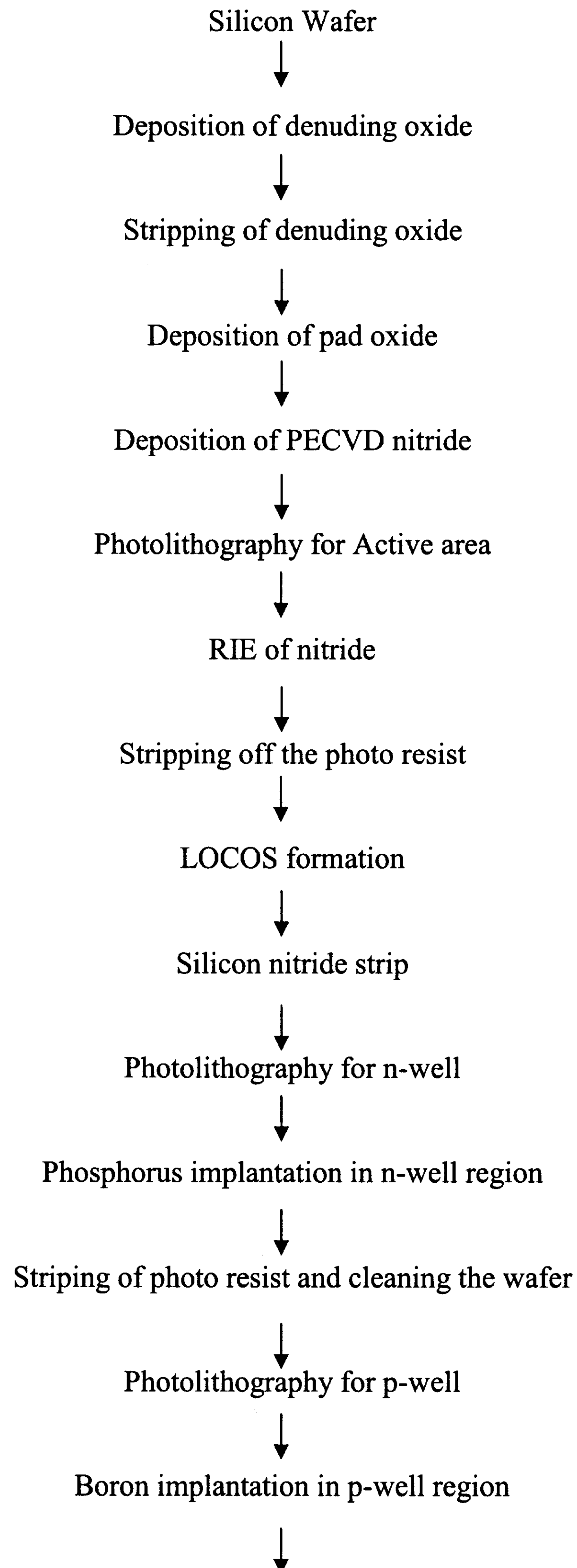
4.1.27 Attaching Glass Wafer on the Back-End by Using Adhesive

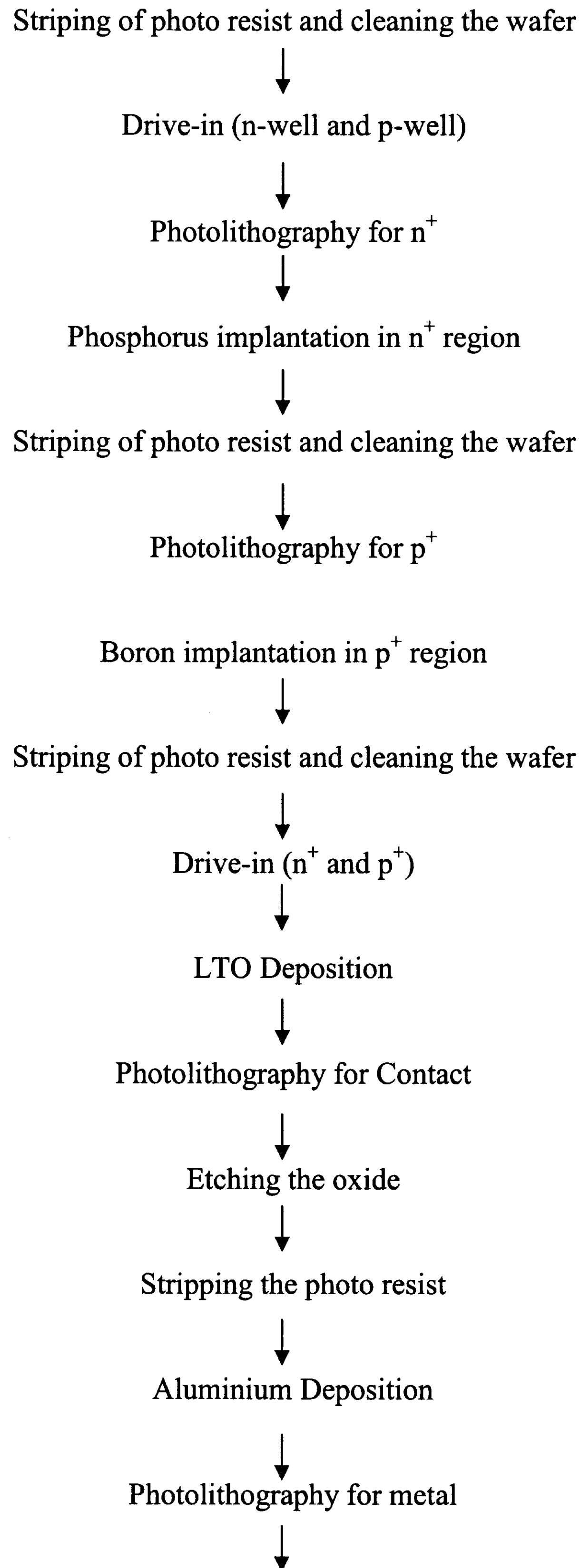
The glass wafer will be attached with the backside of the wafer by using optical glue-OP-30 Curing Description: 5 sec in UV ray with wavelength of 350 nm.

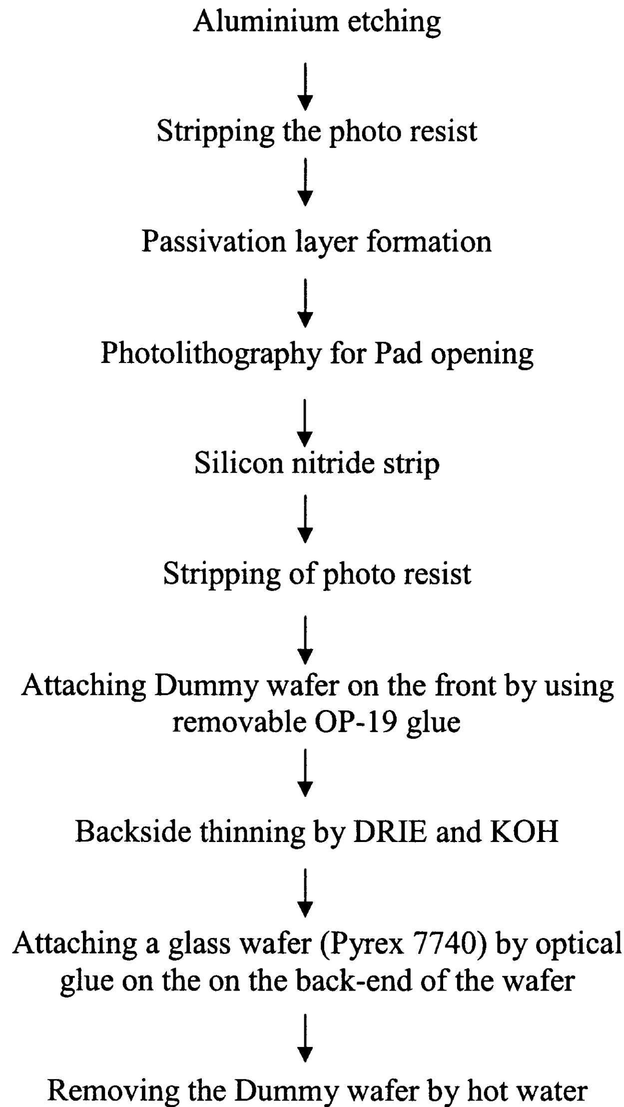
4.1.28 Removal of Dummy Wafer from the Front-End

The OP- 19 is water-soluble adhesive, dissolves completely in hot water. Removal of the dummy wafer will be done at 150°F in DI water.

4.2 Flow Chart for Fabrication of Photodiodes




Striping of photo resist and cleaning the wafer
Drive-in (n-well and p-well)
Photolithography for n+
Phosphorus implantation in n+ region
Striping of photo resist and cleaning the wafer
Photolithography for p+
Boron implantation in p+ region
Striping of photo resist and cleaning the wafer
Drive-in (n+ and p+)
LTO Deposition
Photolithography for Contact
Etching the oxide
Stripping the photo resist
Aluminium Deposition
Photolithography for metal



4.3 Schematic Representation of the Device Fabrication Steps

The cross sections of the wafers at different processing steps are shown schematically, in Appendix A, by means of cut-away profiles of a photodiode, along with a brief explanation of the step(s) involved. The description of all the cross sections were discussed on the previous sections from section 4.1.1 to section 4.1.28 and also the section numbers are given along with the figures below as references.

4.4 I-V Characteristics

After device fabrication, current-voltage (I-V) characterization was carried out. To observe the electrical diode characteristics and the leakage current, we first performed the I-V measurements. The I-V setup consisted of a Hewlett Packard 4145B semiconductor parametric analyzer instrument, micromanipulator probe station. The current was measured as various voltages were applied to the device.

When reverse bias voltage was applied to the p-n junction diode, virtually no current was observed initially. As the reverse bias was increased, the current started to increase and at a certain value of reverse bias the current suddenly increases to a high value. Bellow, Fig.4.1 shows the current characteristics measured after metallization at function of applied voltages. The photodiode achieved a dark current of about 15 pA at -3 V. Fig. 4.2 shows the enlarged view of the reverse bias characteristics to estimate the dark current.

Two main relationships were observed from the I-V characteristics: (a) V=0, and V= -ve, when current becomes the reverse saturation current. (b) V= +ve, when the current increases exponentially when a bias was applied to the photodiode. One of the main objectives of this work is to obtain low dark current. According to the about data, it is clear that the obtained reverse bias current is quite low and comparable to reported results.

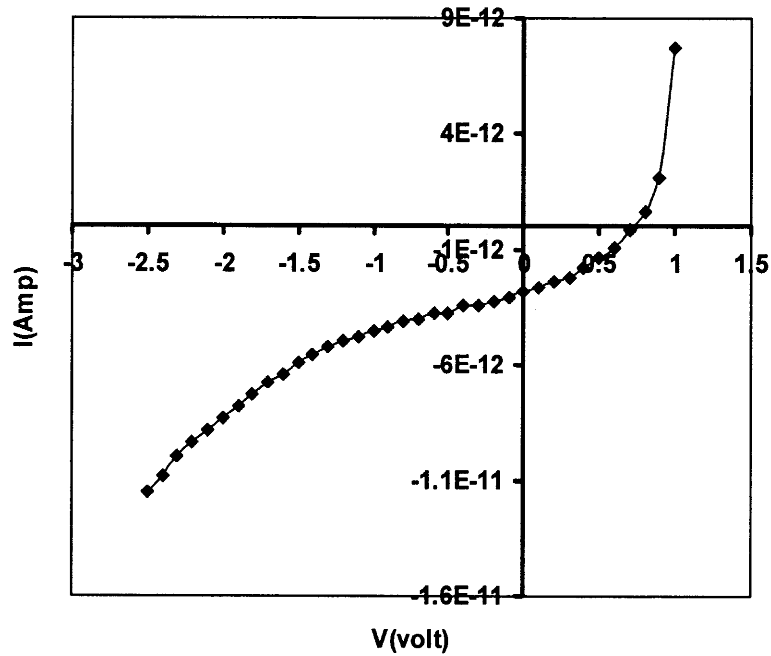


Figure 4.1 Current as a function of an applied voltage range of 1V to -2.5V.

Dark Current as a Function of Bias Voltage

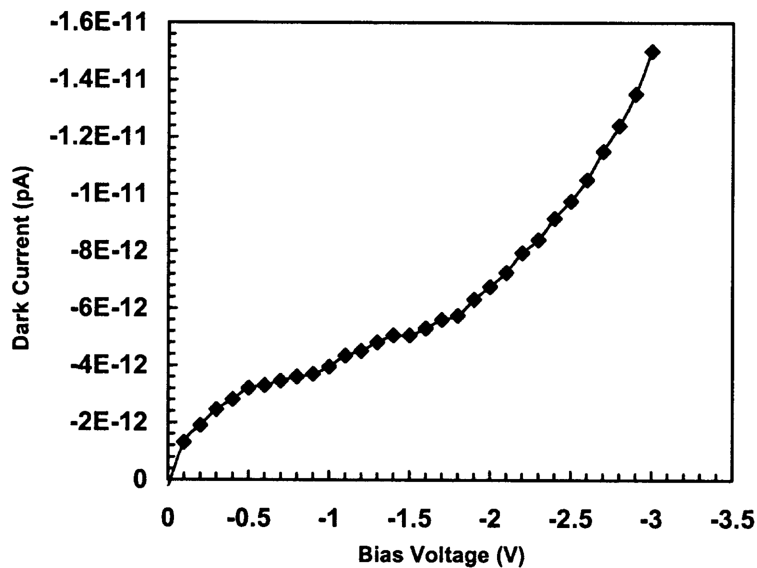


Figure 4.2 Reverse current characteristics with a reverse bias of -3V.

CHAPTER 5

CONCLUSION

5.1 Conclusion

An array of back-illuminated CMOS p-n junction photodiode has been designed, simulated and fabricated by a simple and low cost fabrication process to obtain high quantum efficiency and fill factor. A novel process was developed and used for back thinning of standard CMOS monolithic pixel sensors down to the epitaxial radiation sensitive layer.

Different test structures were fabricated along with the heart design to ensure consistency of each step. Measured sheet resistance values of different layers were reasonably agreed with the calculated values. Different doping concentrations for different regions were also simulated by using SRIM, TSUPREM and MEDICI softwares. SRIM results helped to obserb the damage that occurred during the implantations. The doping profiles from TSUPREM, were used to optimize the junction depths (where, for n-well and p-well regions the required depth is 1 micron and for n^+ and p^+ regions it's less than 0.5 micron). The leakage current simulation showed that the photodiode has dark current of 1.95pA at a bias voltage of -3V, whereas the measured value shows that the amount of dark current is 15pA at that reverse bias voltage.

5.2 Future Work

The photodiode array was fabricated to contribute in the field of CMOS imagers. Some work is being continued on the back-thinned CMOS imagers. The process of back-thinning was novel in this project and an optimum performance is expected from these devices. The back thinning of the devices needs to be completed to measure the reverse bias current during back-illumination. Measurement of electrical as well as optical characteristics is required to insure the device performance. Main area of concentration needs to be quantum efficiency, noise, image lag and linearity of the fabricated devices.

APPENDIX

SCHEMATIC REPRESENTATION OF DEVICE FABRICATION STEPS

The cross sections of the wafers at different processing steps are shown schematically by means of cut-away profiles of a photodiode, along with a brief explanation of the step(s) involved. The description of all the cross sections were discussed on the previous sections from Sub-section 4.1.1 to Sub-section 4.1.28 and also the Sub-section numbers are given along with the figures below as references.

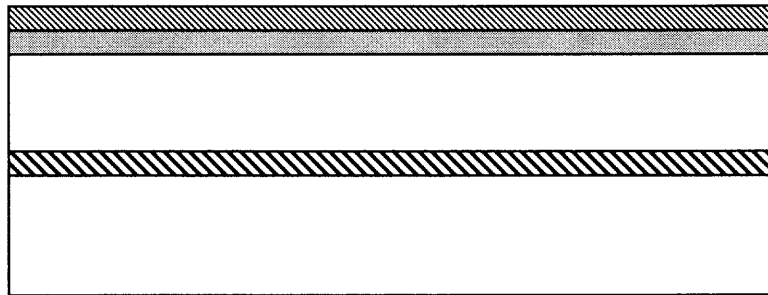


Figure A.1 <100> p-type Si wafer deposited with 400Å pad oxide and 1250Å silicon nitride [4.1.4, 4.1.5].

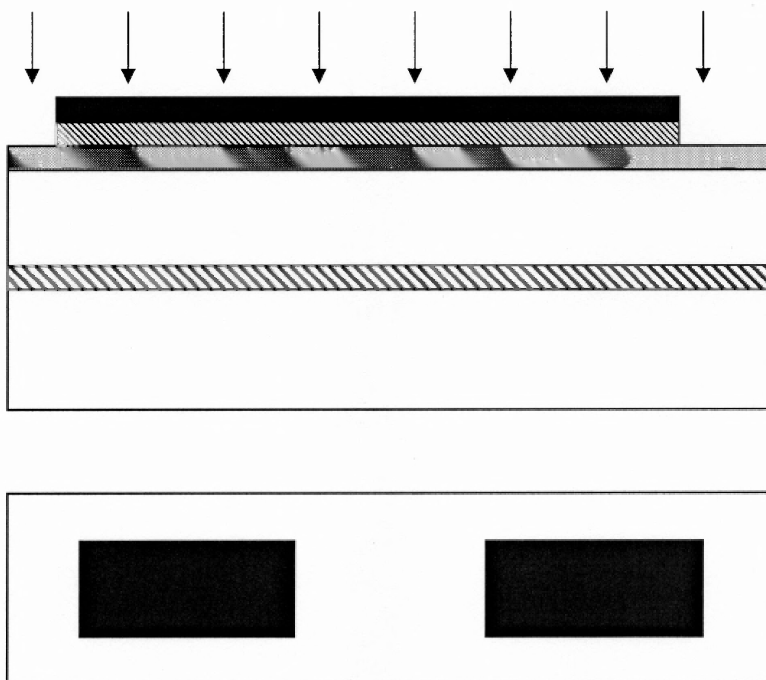


Figure A.2 Patterning of nitride to create window for oxide growth [4.1.7].

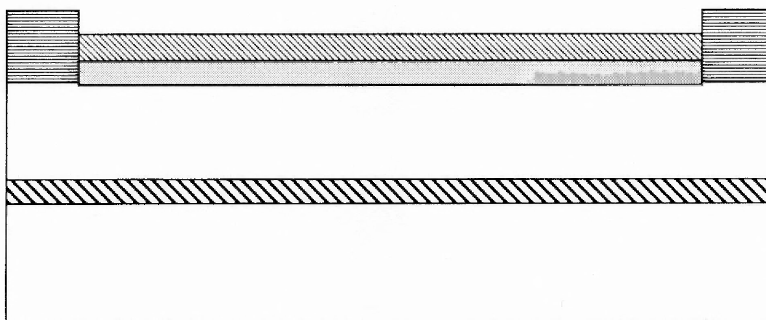


Figure A.3 Field oxide growth on top of the pad oxide [4.1.8].

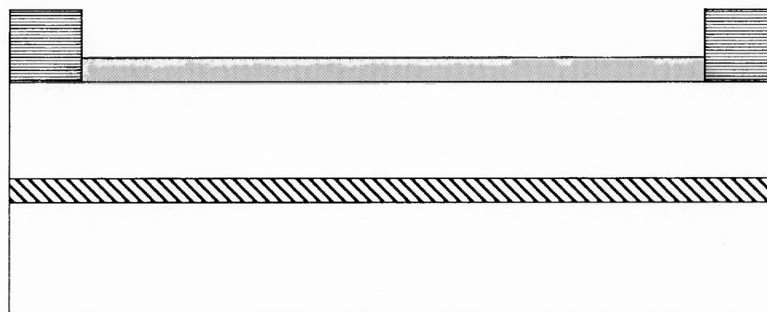


Figure A.4 Wet etching of nitride [4.1.9].

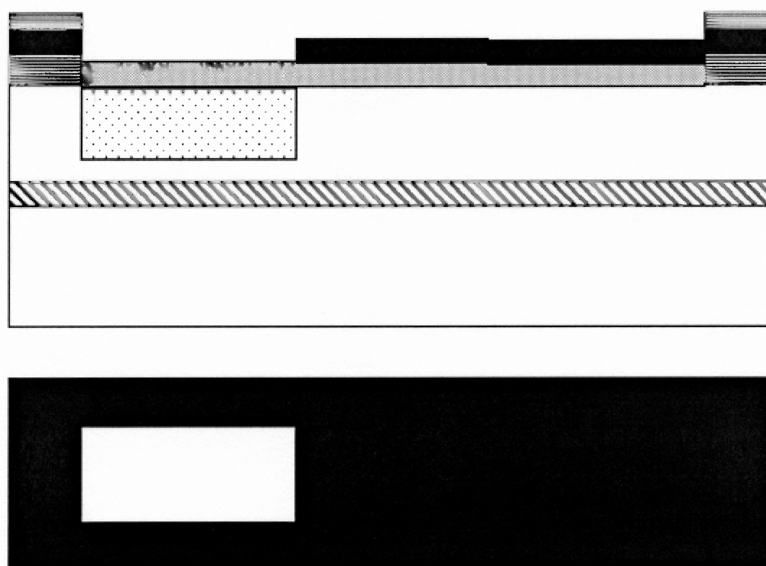


Figure A.5 Pattering the photoresist and n-well implantation [4.1.10, 4.1.11].

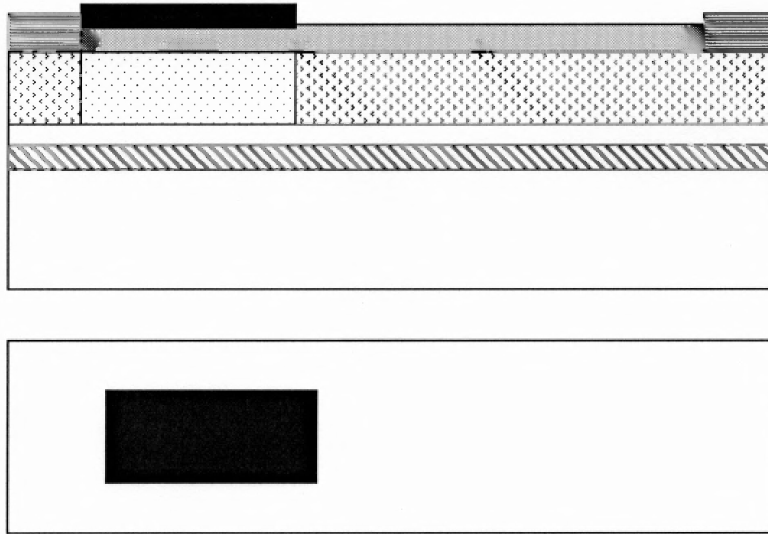


Figure A.6 Patterning of photoresist and p-well implantation [4.1.12].

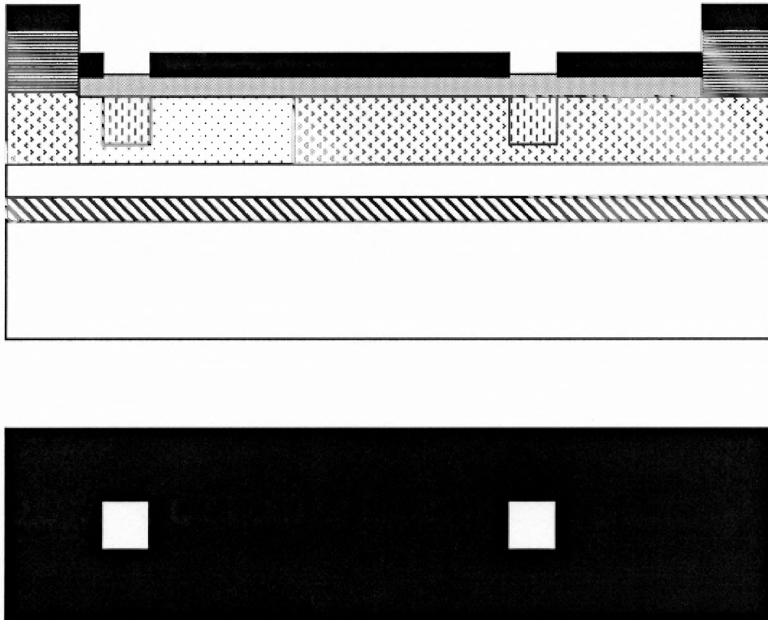


Figure A.7 Pattering the photoresist and n^+ implantation [4.1.12].

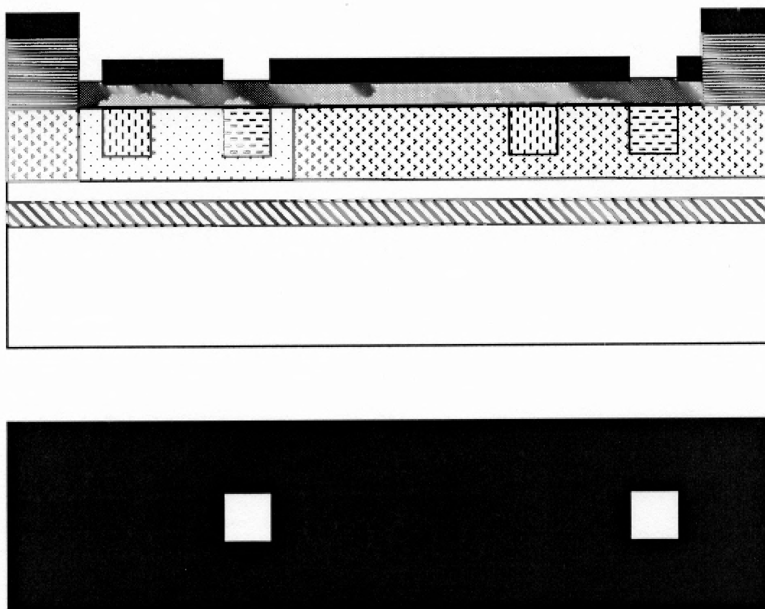


Figure A.8 Patterning the photoresist and p^+ implantation [4.1.12].

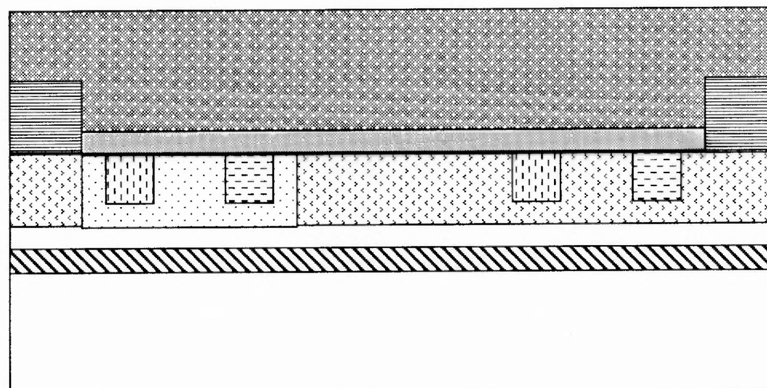


Figure A.9 Low temperature oxide growth [4.1.13].

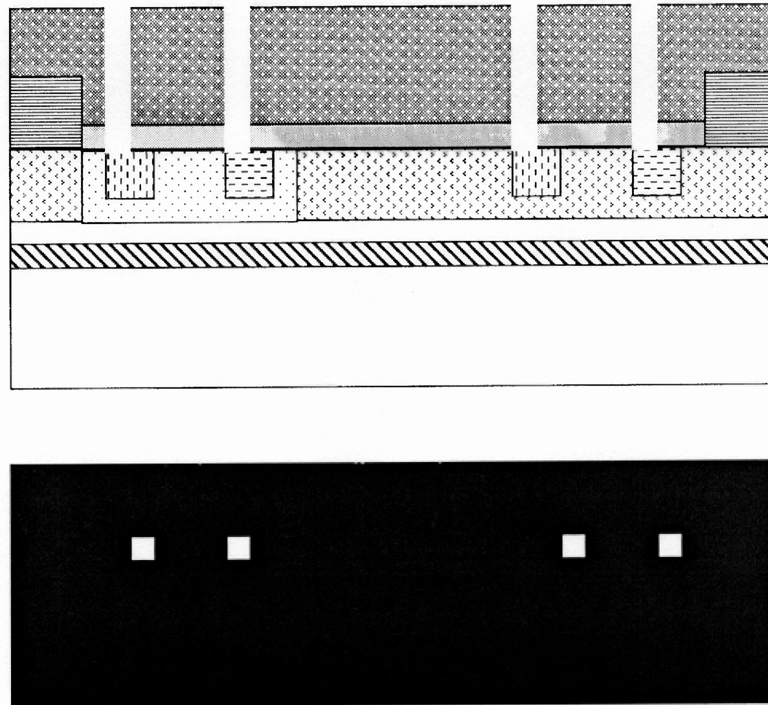


Figure A.10 RIE of LTO for contact formation [4.1.15].

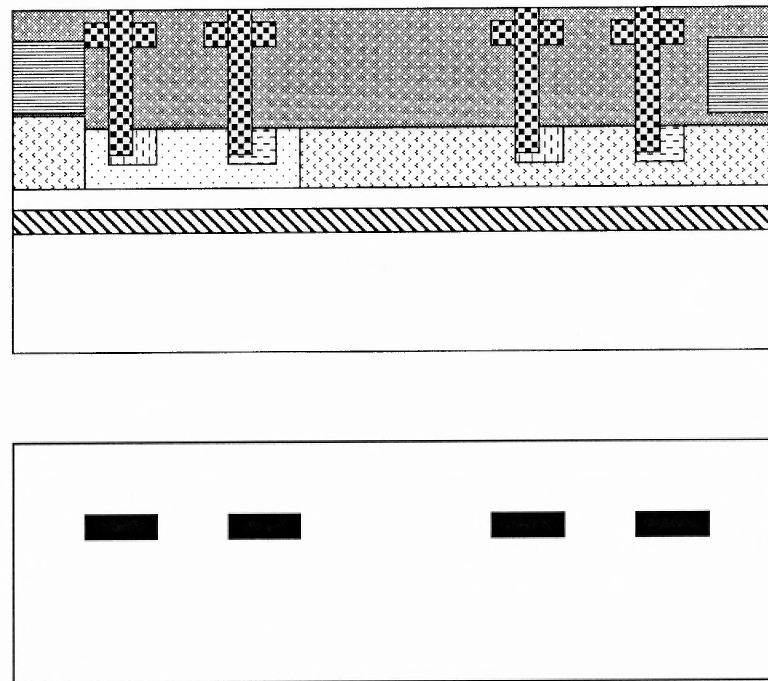


Figure A.11 Metallization and patterning [4.1.19].

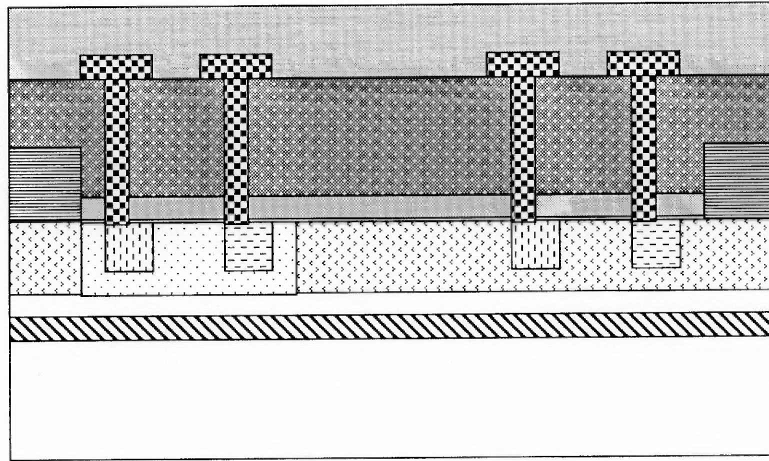


Figure A.12 Passivation layer formation [4.1.21].

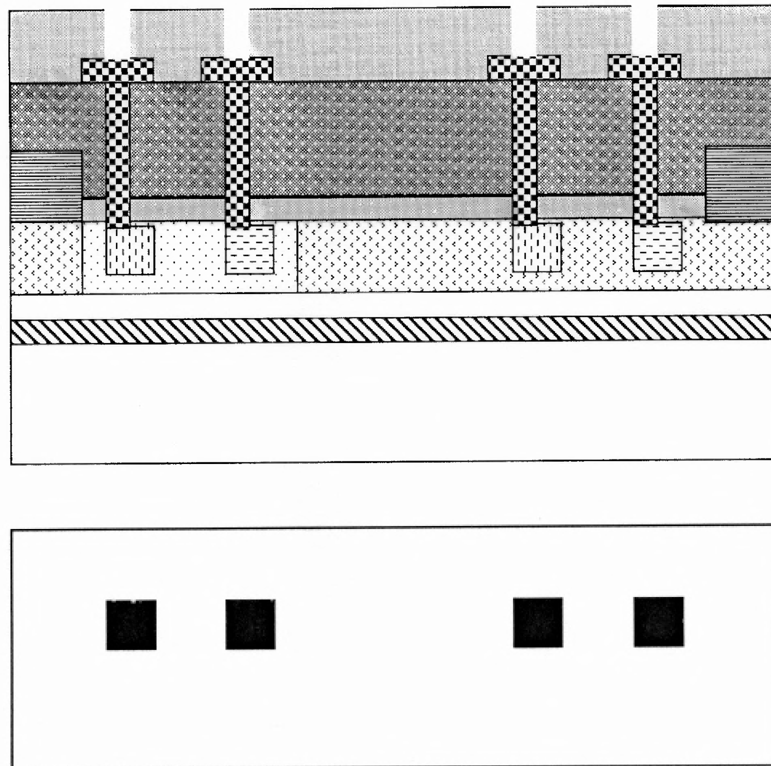


Figure A.13 Passivation layer formation and pad opening [4.1.23].

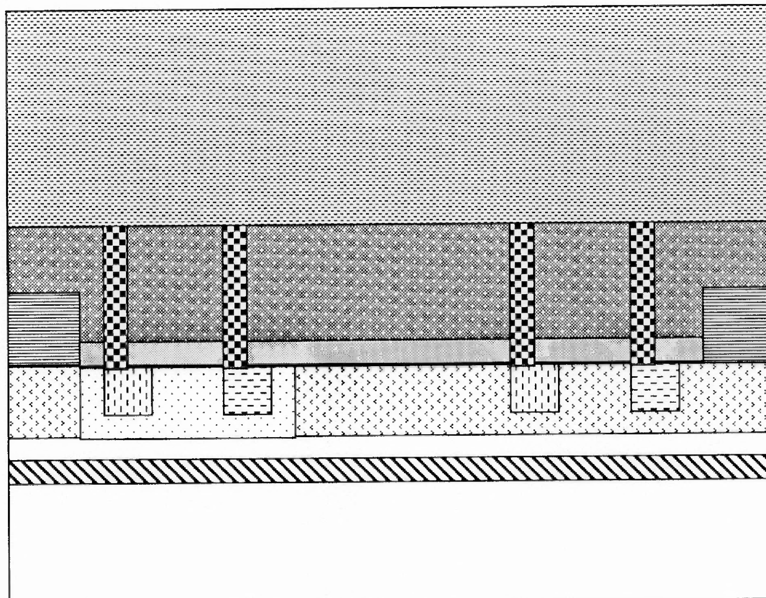


Figure A.14 Attaching a dummy wafer on the front side of the wafer [4.1.25].

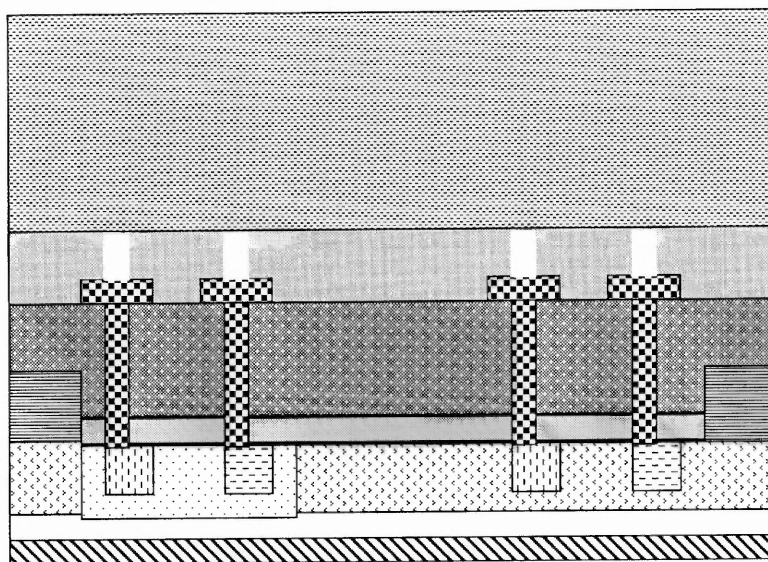


Figure A.15 Back-end thinning [4.1.26].

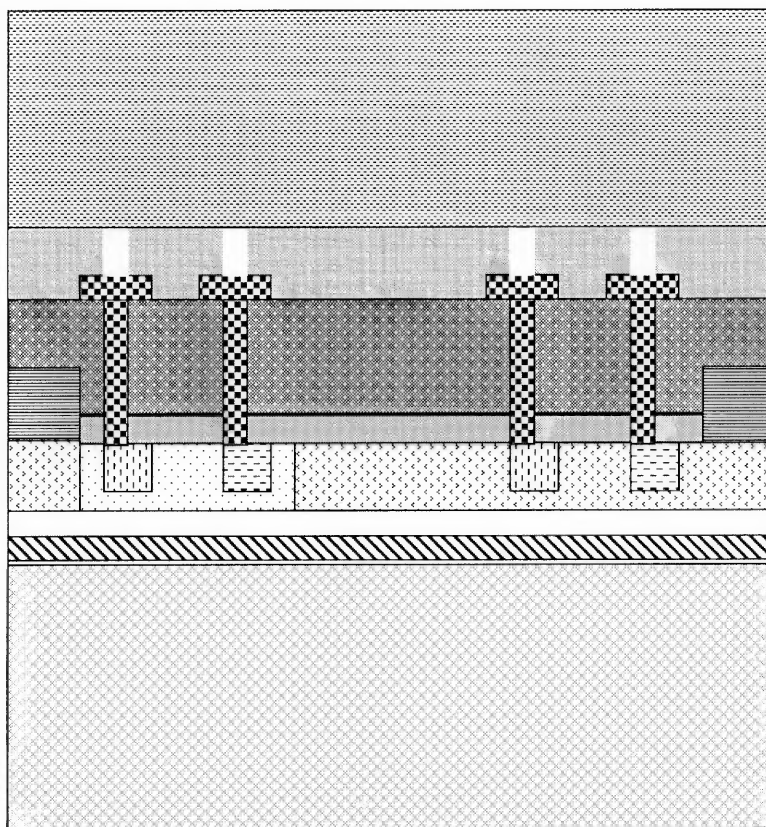


Figure A.16 Attaching a glass wafer at the back end [4.1.27].

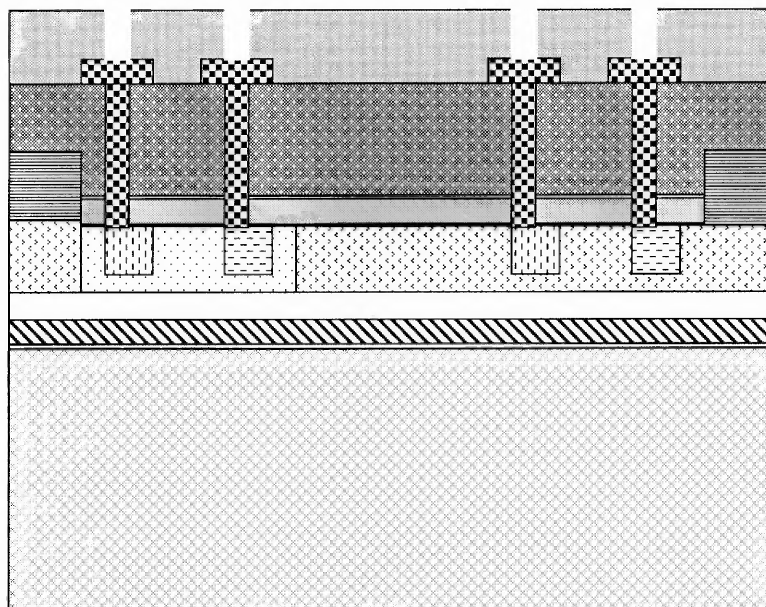


Figure A.17 Removing the dummy wafer from the front-end [4.1.28].

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