ABSTRACT

HfO_2 AS GATE DIELETRIC ON Si AND Ge SUBSTRATE

by
Reenu Garg

Hafnium oxide (HfO_2) has been considered as an alternative to silicon dioxide (SiO_2) in future nano-scale complementary metal-oxide-semiconductor (CMOS) devices since it provides the required capacitance at the reduced device size because of its high dielectric constant. HfO_2 films are currently deposited by various techniques. Many of them require high temperature annealing that can impact device performance and reliability.

In this research, electrical characteristics of capacitors with HfO_2 as gate dielectric deposited by standard thermal evaporation and e-beam evaporation on Si and Ge substrates were investigated. The dielectric constant of HfO_2 deposited by thermal evaporation on Si is in the range of 18-25. Al/HfO_2/Si MOS capacitors annealed at 450°C show low hysteresis, leakage current density and bulk oxide charges. Interface state density and low temperature charge trapping behavior of these structures were also investigated.

Degradation in surface carrier mobility has been reported in Si field-effect-transistors with HfO_2 as gate dielectric. To explore the possibility of alleviating this problem we have used germanium (Ge) substrate as this semiconductor has higher carrier mobility than Si. Devices fabricated by depositing HfO_2 directly on Ge by standard thermal evaporation were found to be too leaky and show significant hysteresis and large shift in flatband voltage. This deterioration in electrical performance is mainly due to the formation of unstable interfacial layer of GeO_2 during the HfO_2 deposition. To minimize this effect, Ge surface was treated with the beam of atomic nitrogen prior to the dielectric

deposition. The effect of surface nitridation, on interface as well as on bulk oxide, trap energy levels were investigated using low temperature C-V measurements. They revealed additional defect levels in the nitrided devices indicating diffusion of nitrogen from interface into the bulk oxide. Impact of surface nitridation on the reliability of $Ge/HfO_2/Al$ MOS capacitors has been investigated by application of constant voltage stress at different voltage levels for various time periods. It was observed that deeper trap levels in nitrided devices, found from low frequency and low temperature measurements, trap the charge carrier immediately after stress but with time these carriers detrap and create more traps inside the bulk oxide resulting in further devices deterioration. It is inferred that though nitrogen is effective in reducing interfacial layer growth it incorporates more defects at interface as well as in bulk oxide. Therefore, it is important to look into alternative methods of surface passivation to limit the growth of GeO_2 at the interface.

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by
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To my family

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CHAPTER 1

INTRODUCTION

To fulfill the need of modern information technology i.e. to increase the circuit functionality and performance at lower cost, semiconductor industry has been dramatically decreasing the minimum feature size used to fabricate integrated circuits to the nanometer range. This downscaling of metal-oxide-semiconductor field effect transistors (MOSFETs) implies, among others, the continuous decrease in the thickness of silicon dioxide (SiO_2) used as the gate oxide film. With this scaling in device dimensions to minimum of 40nm, SiO_2 thickness has to be reduced to keep sufficient current driving capability, as thinner dielectrics improve short channel characteristics.

According to International Technology Roadmap for Semiconductors (ITRS), by the year 2006 electrical equivalent oxide thickness, t_{eq}, will reach to 1.8nm and gate leakage currents less than $2mA/cm^2$ will be required for MOSFET devices for low standby power applications [1]. The microprocessor unit (MPU) applications will further require aggressive scaling of t_{eq} to 1nm. Amorphous SiO_2, the natural oxide of Si technology, is only 3-4 monolayers when it reaches the physical thickness of 1.5 - 2 nm. But when the thickness of SiO_2 goes down to 2nm or below, direct tunneling current increases 100 times for every 0.4 – 0.5 nm decrease of thickness [2].

Fig 1.1 shows measured and simulated $I_G - V_G$ characteristics under inversion conditions of SiO_2 nMOSFETs [3]. As it can be observed at a gate bias of 1V leakage current density increases from $\sim 10^{-7} A/cm^2$ to $\sim 10 A/cm^2$, when SiO_2 thickness is decreased from 3.2nm to 1.5nm. Although this leakage current at 1.5nm SiO_2 is still

tolerable for MPU applications with increased failure probabilities, it is simply unacceptable for low standby power applications.

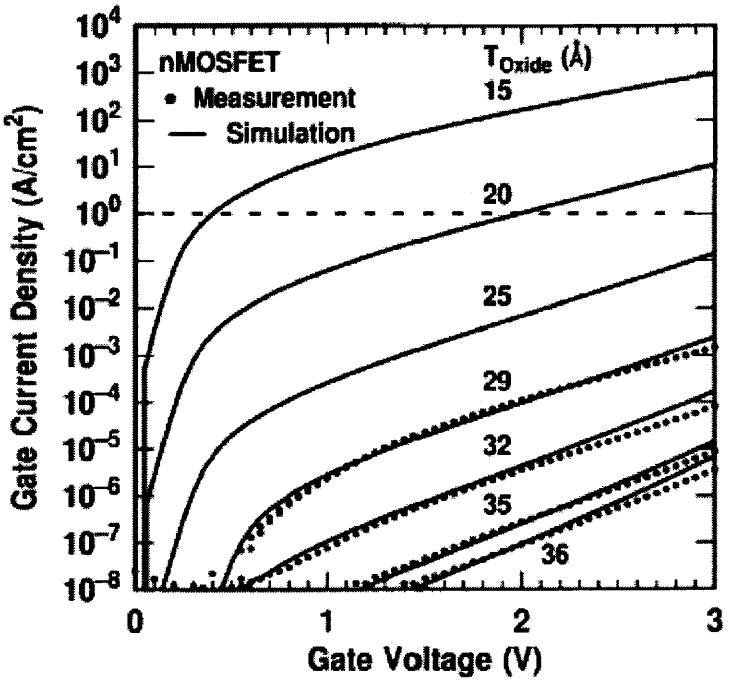

Fig. 1.1 Measured and simulated Ig-Vg characteristics under inversion conditions of SiO2 N- MOSFET devices [3].

Therefore, it has become quite evident that for continuous downscaling of Si CMOS devices, 40 years old SiO_2 technology is leading towards a physical roadblock due to high gate oxide leakage. This increased leakage current in SiO_2 has raised considerable attention on high-κ dielectrics as a suitable replacement of SiO_2, since they provide the required capacitance at a larger physical thickness than SiO_2 and allow reduction of gate leakage current by suppression of direct tunneling. The ITRS indicates that for CMOS applications, high-κ dielectrics will be needed by the end of year 2005.

Various high-κ dielectrics such as Tantalum Oxide (Ta_2O_5), Titanium Oxide (TiO_2), Aluminum Oxide (Al_2O_3), Yttrium Oxide (Y_2O_3), Zirconium Oxide (ZrO_2),

Hafnium Oxide (HfO_2) [4-6] etc. have been proposed to replace SiO_2. Among these high-κ dielectrics, HfO_2 has emerged as a strong contender because 1) high dielectric constant of ~25-30 (~6-7 times that of SiO_2), 2) energy band gap of 5.68eV, though much lower than SiO_2 but with band offsets greater than 1eV (1.5eV for electron and 3.4eV for holes), 3) free energy of reaction with Si is about 47.6Kcal/mol at 727°C making it more stable material on Si substrate in comparison to other high- κ dielectrics, 4) unlike other silicides, silicide of Hf can be easily oxidized [7] to form HfO_2. All these properties of HfO_2 make it an attractive alternative for SiO_2.

The properties of grown film and interface show a pronounced dependence upon the deposition process and the precise deposition parameters chosen. Each technique has their own set of advantages and disadvantages. However, most of the techniques show some or other kind of interface damage. Sputtering and e-beam assisted depositions create radiation induced surface damage during film growth. All these techniques, therefore, require high temperature annealing which further results in the deterioration of device performance and reliability. Since HfO_2-Si interface is critical for excellent device characteristics it is important to investigate other reliable deposition techniques for high quality interface.

Another critical drawback is the degradation of carrier mobility in FET channel. In fact, this mobility degradation is so severe that it can be reduced by a factor of 2 [8] in Si MOS devices with HfO_2 as gate dielectric. Many research groups are exploring different ways to enhance carrier mobility, such as the use of strained silicon germanium, SiGe on Si [9] or strained Si on relaxed buffer SiGe layers [10]. Changing the substrate from silicon to germanium could be a possible solution to surface carrier mobility

degradation as Ge has higher carrier mobility (2X for electrons and 4X for holes) in comparison to Si. Originally transistors were fabricated on Ge substrate but lack of stable Ge native oxide has been an obstacle in CMOS device realization in Ge. But recently devices using high-κ gate dielectrics deposited directly on Ge substrate have shown some promise.

The main objective of this research is to evaluate and characterize the MOS devices with HfO_2 as gate dielectrics, deposited by standard thermal evaporation (at Sarnoff Corporation) on Si and Ge substrate as thermal evaporation doesn't produce much damage to the interface and it doesn't require high temperature processing in comparison to other techniques. Second major objective of this research is to study the effect of Ge surface treatment prior to HfO_2 deposition on the reliability of $Al/HfO_2/Ge$ MOS capacitors using low temperature and stress measurements.

In this dissertation, the second chapter describes the basic properties of high-κ dielectrics and what makes them an attractive alternative of SiO_2. After a short review of the advantages of high-κ dielectrics, this chapter reviews the work done by different scientific groups on both silicon and germanium substrate. This chapter analyzes the technical challenges put forth for integration of high-κ materials in CMOS technology.

The third chapter gives an overview of the device fabrication and characterization used in this work. It describes each processing step used in fabricating the MOS capacitors. Then, the physical and electrical characterization techniques used in this research have been discussed

Fourth chapter presents the electrical characterization of HfO_2 films deposited by thermal evaporation on Si substrate. Measurements were taken before annealing and after

annealing to see the effect of annealing in these films. It also presents the analysis of experimental data and summarize the performance of MOS capacitors at room temperature as well as at low temperature.

Fifth chapter describes the physical and electrical properties of thermally evaporated HfO_2 films on Ge substrate. Physical characterization of these films has been done using scanning electron microscopy and X-ray photoelectron spectroscopy, while electrical characterization was performed similar to MOS capacitors on Si substrate.

Chapter six compares the HfO_2 films deposited by thermal evaporation and e-beam evaporation with reactive atomic O beam on Ge substrate. Effect of surface treatment prior to gate dielectric deposition has been described. It analyzes the trap energy levels using low temperature measurements and tests the reliability of $Al/HfO_2/Ge$ MOS capacitors using constant voltage stress measurements.

Finally, chapter seven presents the conclusions of this dissertation and suggestions for further research.

CHAPTER 2

HIGH-κ DIELECTRICS

2.1 Background

The continuous scaling of Si CMOS devices has led to the need of increased capacitances per unit area in CMOS conducting channel, which resulted in high gate leakage current. Capacitance can be increased by increasing κ (dielectric constant) or by decreasing the thickness of oxide, shown in eq. (2.1)

$$C_{ox} = \frac{k_{SiO_2}\varepsilon_0}{t_{SiO_2}} = \frac{k_{high-\kappa}\varepsilon_0}{t_{high-\kappa}} \qquad (2.1)$$

Where C_{ox} is capacitance per unit area, k_{SiO2} and $k_{high-\kappa}$ are the dielectric constant of SiO_2 and high-κ dielectrics respectively, ε_o is the vacuum permittivity, and t_{SiO2} and $t_{high-\kappa}$ are the physical thickness of gate dielectric. As t_{SiO2} can't be reduced below certain limit, the only alternative left is to increase the κ so that a thicker film can be employed compared to SiO_2 while maintaining equivalent C_{ox}.

Different gate stacks of silicon oxynitride and nitride/oxide films have been studied, showing improved characteristics in terms of leakage current and reliability [11-14]. Fig. 2.1 shows a reduction of ~10^3A/cm^2 in leakage current density of silicon nitride films grown by different techniques with respect to SiO_2 at t_{eq} = 2.1nm. However, due to relatively low dielectric constants, they can't be scaled down lower than 1 nm. This understanding has raised lot of attention to high-κ materials to replace SiO_2.

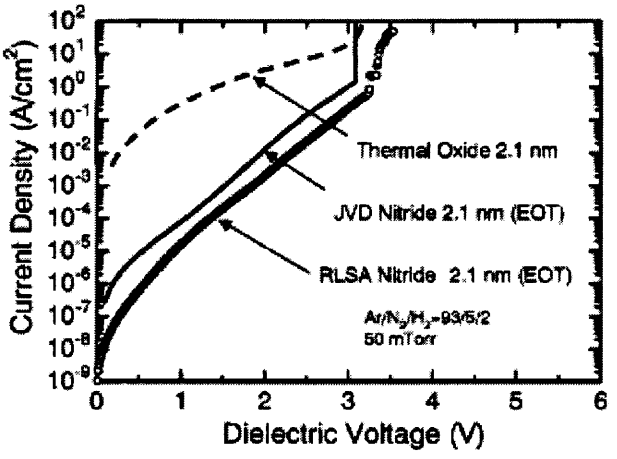

Fig. 2.1 Current density of various silicon nitride films with EOT of 2.1 nm. [15]

2.2 Selection Criteria

There are various aspects that need to be taken into consideration before selecting any dielectric material. Obviously the first consideration is the dielectric constant; it should be significantly higher than that of SiO_2. The replacement dielectric should be thermodynamically stable in contact with Si channel, able to withstand annealing temperatures up to 1050°C and is compatible with CMOS processing. As hot carrier emission into the gate insulator and gate direct-tunneling current is dependent on the barrier height [16, 17], it is desirable that silicon-to-gate oxide barrier height should be sufficiently large for both electrons and holes. In addition, interface trap densities should be close to that of SiO_2 in the silicon bandgap because performance of MOSFETs fundamentally relies on the quality of oxide-Si interface as current flows in Si channel

next to interface. Charge trapping in oxide and reliability of the gate dielectrics are also important in selecting the appropriate material.

Various alternatives have been proposed to replace SiO_2 such as TiO_2 [5,19], ZrO_2 [20], HfO_2 [21], Y_2O_3 [22], Al_2O_3 [23, 24], Ta_2O_5 [25, 26], and La_2O_3 [27] as well as their silicates and aluminates. Many of the materials initially chosen were inspired by memory capacitor application [28] such as Ta_2O_5 [29], $SrTiO_3$ [30] and Al_2O_3 [31], which have dielectric constants ranging from 10 to 80, and have been employed mainly due to their maturity in memory capacitor applications. However, except Al_2O_3, these materials are not thermodynamically stable in direct contact with Si (thermodynamic stability is not a requirement for memory capacitors, since the dielectric is in contact with the electrodes, which are typically nitrided poly-Si or metal). Also, as band gap tends to vary inversely with dielectric constant, one or both of their band offsets are under 1eV leaving them unacceptable for transistor application, shown in Fig. 2.2.

Table 2.1 lists some potential dielectric materials along with their properties to replace silicon dioxide. Though TiO_2 has high permittivity of ~80-100 depending upon the method of deposition, but it has been proved to be thermodynamically unstable with Si [34]. Also, it forms a reaction layer both at channel interface and metal electrodes. Among group III candidate dielectrics, Al_2O_3 is robust and stable with Si, has a larger bandgap of 8.8eV but its relatively low dielectric constant (κ~8-13) renders it to be short-term solution for industry needs. Various integration issues such as high fixed charge density and boron penetration have also been reported [23, 24].

Dielectric	*Dielectric Constant*	*Bandgap (eV)*	*Leakage current reduction w.r.t. SiO_2*	*Thermal stability w.r.t. Si*
SiO_2	3.9	9	N/A	>1050°C
Si_3N_4	7	5.3	$10^3 - 10^4$ X	>1050°C
Ta_2O_5	25	4.4		Not thermodynamically stable
TiO_2	~80	3.5		
ZrO_2	~23	5.8	$10^4 - 10^5$ X	~900°C
HfO_2	~25	6	$10^4 - 10^5$ X	~950°C
Y_2O_3	~15	6	$10^4 - 10^5$ X	Silicate formation
Al_2O_3	~10	8.8	$10^2 - 10^3$ X	~1000°C RTA
La_2O_3	~21	6		

Table 2.1 Various dielectric materials and their properties with respect to Silicon [32, 33].

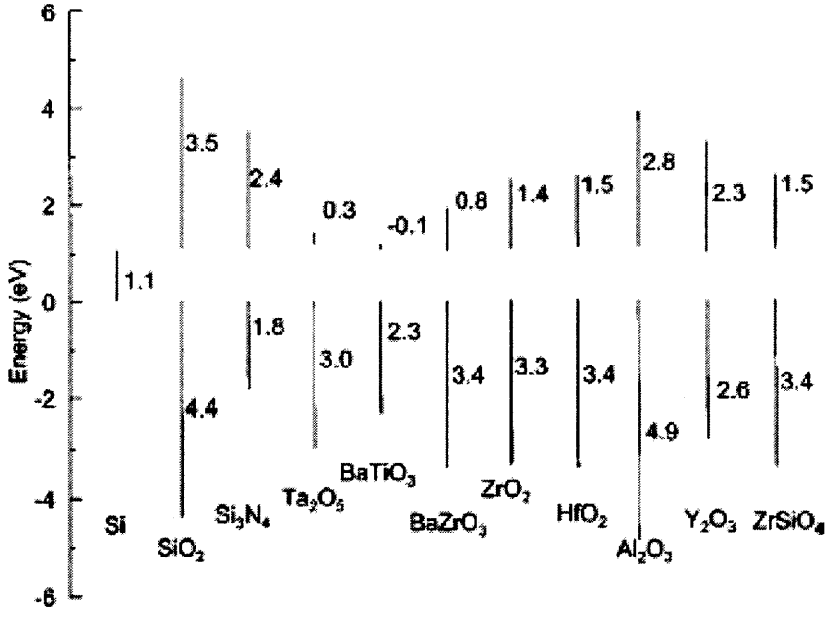

Fig. 2.2 Band offsets of various high-k dielectrics with respect to silicon [33].

HfO_2 and ZrO_2 have high dielectric constants (20~25), high stability on Si, sufficient band offsets to act as barrier for electrons and holes (shown in Fig. 2.2) and can withstand high annealing temperature up to 900°C. However, ZrO_2 reacts with poly-Si and Si substrate [35, 36], which leaves HfO_2 as an only but attractive replacement for SiO_2.

HfO_2 being a leading candidate has many advantageous qualities including high dielectric constant (~25), large heat of formation (-271 kcal/mol), and band offsets of 1.5eV and 3.4eV for electrons and holes, respectively. It's compatibility with poly-Si and CMOS processing add more support to its suitability.

2.3 Different Deposition Techniques

Since these high-κ materials need to be deposited on substrate, different research groups have been trying different techniques to get the optimum performance. Films are deposited in a unique way in each technique depending upon the deposition process and the deposition parameters chosen. Atomic layer deposition (ALD) is the most popular technique because of the controllable thickness and good step coverage of HfO_2 [37, 38]. However, in ALD, growth of the film is inversely proportional to temperature [39] that mean substrate temperature has to be 300°C [38, 40] to have controlled growth of film. This high temperature growth induces of degree of crystallanity in the oxide film, highly undesirable for CMOS technology. Another problem with chemical vapor deposition techniques is choosing the right precursor to form HfO_2, as it is directly related to impurities in the film [41]. Another popular technique is metal-organic chemical vapor deposition because of good film conformality and control on deposition rates. However,

choice of precursor, deposition temperature and incorporation of carbon impurities are major concern in this technique [8].

There are other alternative techniques that people have tried such as ultraviolet ozone oxidation [42], sputtering [43, 44], reactive atomic beam deposition [45], evaporation with ion-assisted beam deposition [46], etc. However, most of these techniques show some or other kind of interface damage, for example sputtering and e-beam assisted depositions create radiation induced surface damage during film growth. Also these techniques require high temperature annealing which further results in the deterioration of device performance and reliability. Since HfO_2-Si interface in important for excellent device characteristics it is important to investigate other reliable deposition techniques for high quality interface.

2.4 Integration Issues

In spite of having all the desirable qualities, still it's a challenge to bring HfO_2 in mainstream CMOS processing. Firstly, MOS capacitors fabricated with HfO_2 as gate oxide show large hysteresis and shift in flatband voltage (V_{FB}) [47, 48]. This is mainly because of trapped charge in the oxide layer as well as at the interface. Defects at interface are generated due to lattice mismatch of HfO_2 and Si, which can be reduced by growing a thin interfacial layer of SiO_2. However, it will lower the effective oxide thickness (EOT) of the gate stacks. Another factor that affects the V_T instability is the electron trapping and de-trapping taking place in HfO_2 bulk defects [49, 50]. Charge trapping also creates threshold voltage (V_T) instabilities by continuing the shift under device stress.

Another challenge with high-κ dielectrics is oxygen diffusivity and boron penetration during high-temperature annealing for source/drain activation. This lack of stopping power against O_2 leads to significant interfacial layer under low partial pressures of oxygen at low (400°C – 600°C) temperatures [51], ultimately bringing down the EOT. Boron penetration through HfO_2 films after annealing, at temperatures as low as 950°C, has been observed [52] resulting in interface degradation and V_T shifts. Nitridation of the Si surface using prior to a deposition of a high-κ dielectric has been shown to be effective in achieving low EOT and preventing boron penetration [52, 53]. However, it results in higher positive interface charges [54], which leads to higher hysteresis and reduced channel mobility.

Major concern in high-κ dielectrics is the degradation of surface carrier mobility in MOSFET channel. Fig. 2.3 shows the electron mobility of high-κ material with respect to SiO_2.

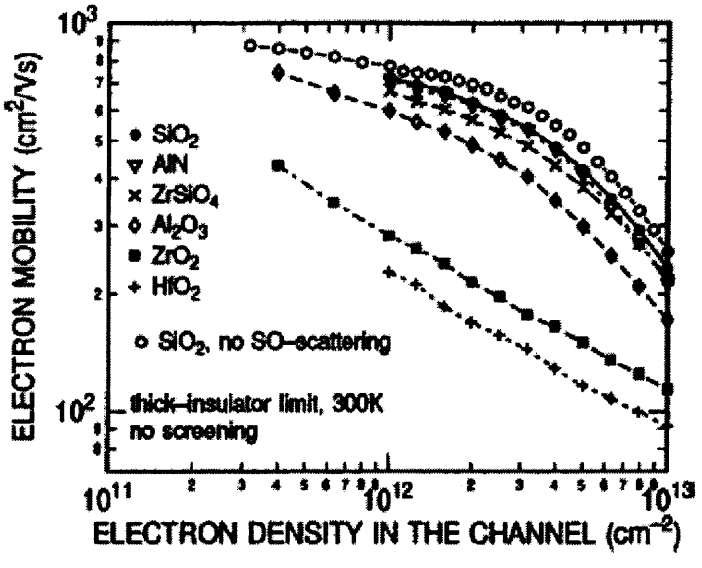

Fig. 2.3 Electron mobility of various high-k materials with respect to silicon [55].

Fischetti *et al* [55] explained that the reduced channel carrier mobility of high-κ material is actually related to their dielectric constant. The static dielectric constant of an insulator results from the combination of the ionic and the electronic polarization. Due to the larger bandgap of insulators, there is little electronic polarization. Therefore a higher dielectric constant can only originate from a larger ionic polarization of "soft" metal–oxygen bonds. These soft bonds are associated with low-energy phonons, which are optical in nature because of the ionic character of the atomic bonds in most insulators. This suggests that the higher the dielectric constant, lower the surface-optical-phonon-limited mobility. Another reason for lower mobility could be the Coulomb scattering due to fixed and trapped charges in the high–κ films [56].

2.5 Ge as a Substrate

Low surface carrier mobility in the inversion channel of high-κ Si MOSFETs has brought back the long forgotten Ge into CMOS technology. Ge has large hole mobility of 1900cm^2/Vs (4X of Si) in comparison to any other common semiconductors and electron mobility of 3900cm^2/Vs (2X of Si). These high motilities of Ge can provide drive current enhancement for both p- and n-MOSFETs. Furthermore, Ge has direct bandgap of 0.66eV, giving it an added advantage of being suitable for fiber-optical communication device applications.

The very first point contact transistor (by Brattain and Bardeen, 1947) and first integrated circuit (by Jack Kilby, 1958) both were fabricated on Ge. However, photoelectron spectroscopy studies have shown that annealing of GeO_2 transforms it into GeO on the surface, subsequently thermally desorbs from the surface [57]. The unstable

nature of GeO_2 and the fact it's water soluble, were the one of the biggest obstruction in the realization of very large-scale integration of CMOS devices in Ge.

Scientists have tried various procedures of depositing gate dielectrics involving plasma, pyrolytic and sputter deposition of different oxides and nitrides [58-60]. Most successful effort involved covering the GeO_2 with an insulator Al_2O_3 using molecular beam deposition resulted in interface state densities as low as 1×10^{11} $eV^{-1}cm^{-2}$ [61]. To obtain more stable oxide different gate stacks of Ge oxynitride (GeO_xN_y) using either thermal or plasma anodic nitridation [62, 63] or GeON with low temperature gate oxide were used to form Ge MOSFETs [64]. SiO_2 has also been explored as a non-native insulator on Ge [65]. However, its use on Ge has been far less effective in comparison to Si because of the poor interface between Ge and SiO_2. Most of the historical work has been done with the idea of depositing dielectrics on Ge to obtain films with good interface and bulk characteristics, but these gate stacks are very thick ranging from 5nm to 50nm unable to offer a t_{eq} of less than 1nm for sub-20nm regime.

2.6 High-κ Dielectrics on Ge

Advancements in thin films deposition techniques allowed the deposition of high-κ films in nanometer range on Si. Recently, these techniques have been adapted to deposit thin high-κ dielectrics (t_{eq} <1 nm) on Ge as well. Promising results have been reported showing increase hole mobility over Si p-MOSFET's with the same thin high-κ dielectrics. Chui et al [66] reported ultra-thin ZrO_2 (0.6–1nm) on Ge p-MOSFETS with twice the low-field hole mobility of Si MOSFETs, while Ritenour et al [67] have reported

HfO_2 on Ge p-MOSFETs showing 40% hole mobility enhancement over a Si control with an identical HfO_2 dielectric.

In spite of Ge p-MOSFETs showing improvement in terms of hole mobility, devices made by depositing HfO_2 directly on Ge are too leaky or show significant hysteresis. This deterioration in electrical performance is mainly due to the formation of interfacial layer during the HfO_2 deposition. Ge surface treatment prior to gate dielectrics deposition found to be an effective way in improving the MOS device quality. Different kind of Ge surface passivation has been done by forming thin Ge oxynitride [68, 69], by NH_3 annealing [70] or by SiH_4 annealing [71]. Recently, it has been demonstrated that initial treatment of Ge surface by atomic N beam seems to improve the physical and electrical characteristics of MOS capacitors [72]. Though incorporation of nitrogen at interface introduce positive traps in the films. Still, role of nitrogen on interfacial and bulk characteristics of the films is not well understood.

In this research, we are depositing HfO_2 films on silicon and germanium substrate by thermal evaporation as thermal evaporation, unlike other physical vapor deposition techniques, doesn't damage the substrate surface and it doesn't require high temperature processing. Films deposited by thermal evaporation on Ge substrate are compared to films deposited by e-beam evaporation with reactive atomic O beam. Also, effect of Ge surface treatment prior to gate oxide deposition was studied using low temperature measurements and stress measurements.

CHAPTER – 3

DEVICE FABRICATION AND CHARACTERIZATION

3.1 Device Fabrication

Three sets of MOS capacitors were fabricated with: - 1) thermally evaporated HfO_2 on Silicon substrate, 2) thermally evaporated HfO_2 on Germanium substrate, 3) HfO_2 deposited by e-beam evaporation with reactive atomic O beam on Germanium substrate. Thermal evaporation of hafnium was done at Sarnoff Corporation, while e-beam evaporation of hafnium was carried out at IBM. After gate oxide deposition, MOS capacitor fabrication has been performed in the Microelectronics Fabrication Center at NJIT. A detailed description of the individual process steps is presented below in section 3.1.1 through 3.1.8.

3.1.1 Starting Materials

For silicon-based devices, the starting material was 3" n-type (boron doped), <100> oriented CMOS grade silicon wafers with a sheet resistivity of 10-20 Ω-cm. For germanium-based devices, 2" n-type (antimony doped) <100> germanium wafers with sheet resistivity of 0.4 and 0.1 Ω-cm were used.

3.1.2 Cleaning

In thermal evaporation process, both Ge and Si wafers were cleaned by standard RCA clean (RCA-1 and RCA-2) followed by 50:1 HF dip for 15 minutes immediately before the deposition of the HfO_2 films.

In e-beam evaporation of HfO_2, Ge wafers were first cleaned by standard solvent cleaning and a de-ionized water (DI) water rinse. Then a cyclical rinse of H_2O_2, HCl/H_2O and DI water was done to further clean the wafer surface.

3.1.3 Surface Nitridation

For some device, *in-situ* surface-nitridation of the Ge substrates took place at 350°C–600°C by exposure to an atomic N beam from a remote RF source at 350 W for 30 s, prior to HfO_2 deposition.

3.1.4 HfO_2 Deposition

HfO_2 films of different thickness (50 & 60nm on Si substrate and 5 & 10nm on Ge substrate) were deposited on Si and Ge wafers by standard thermal evaporation. Oxygen was added at constant partial pressure during evaporation. The base pressure was maintained at 10^{-6} Torr before oxygen was added. As oxygen was added during evaporation, the pressure in the chamber increased to 10^{-4} Torr. Tungsten boats were used in evaporating hafnium. Films were deposited at room temperatures, but the measured substrate temperature was around 30-35°C due to source-induced substrate heating. No residual gas analysis was performed during evaporation.

In e-beam evaporation of HfO_2 on Ge, first a protective layer of Ge oxide was formed by immersion in a solution of $NH_4OH/H_2O_2/H_2O$. The protective oxide was then removed in ultrahigh vacuum by thermal adsorption. Following oxide adsorption, hafnium oxide was grown at 50°C to 300°C using a reactive atomic O beam from RF discharge source and Hf evaporated from an electron-beam source. HfO_2 films were then further subjected to UV-ozone oxidation at 600 Torr for 60 min., without breaking vacuum, to produce good-quality oxide film.

3.1.5 Annealing

After oxide deposition wafers were annealed at different temperatures in different ambience shown in table 3.1. In silicon devices annealing was performed after metal gate deposition.

Substrate	Annealing Temperatures (°C)		Annealing Environment
Silicon	350	450	FGA (N_2/H_2: 5%)
Germanium	500	550	N_2
	450		FGA (N_2/H_2: 5%)

Table 3.1 Various annealing temperature with annealing environments.

3.1.6 Metal Deposition

After having undergone the various conditions of annealing the wafers were deposited with metal (Al) using sputtering technique.

3.1.7 Photolithography

Photolithography was conducted to to produce devices with diameters 50um 100um, 200um, 250um, 300um, 400um, and 500um.

3.1.8 Etching

After photolithography was done, metal etching was done using aluminum etchant (phosphoric, nitric acid, acetic acid and de-ionized water) at 45°C. After metal etching,

photoresist was removed using m-pyrol cleaning (methyl pyrolidine - an acidic mixture). The processing temperature is maintained at 95°C.

The two fabrication processes are summarized in table 3.2 and 3.3.

S. No.	Process	Details
1.	Cleaning	RCA clean → 50:1 HF dip, 15 minutes
2.	HfO_2 deposition	Thermal evaporation
3.	Annealing	FGA, 20min, 350°C & 450°C (Si) N_2, 20min, 500°C, 550°C (Ge)
4.	Metal Deposition	Al, Sputtering
5.	Patterning	Photolithography
6.	Metal Etching	Phosphoric acid, nitric acid, acetic acid and DI water, 45°C
7.	Photoresist Removal	Methyl pyrolidine, 95°C
8.	Backside Metal Deposition and Anneal	Al, Sputtering → 350°C FGA

Table 3.2: Process flow of Si and Ge MOS capacitors with thermally evaporated HfO_2 as gate dielectric.

S. No.	Process	Details
1.	Cleaning	Standard solvent and DI water rinse, Cyclical rinse of H_2O_2, DI, HCl,
2.	HfO_2 formation and desorption	Dip in $NH_4OH/H_2O_2/H_2O$ $\longrightarrow$ 650°C, 30min.
3.	Surface Nitridation	N: 500°C, 30s, RF 350W
4.	HfO_2 Deposition	E-beam evaporation $\longrightarrow$ UHV Ozone oxidation
5.	Annealing	FGA, 20min, 450°C
6.	Metal Deposition	Al, Sputtering
7.	Patterning	Photolithography
8.	Metal Etching	Phosphoric acid, nitric acid, acetic acid and DI water, 45°C
9.	Photoresist Removal	Methyl pyrolidine, 95°C
10.	Backside Metal Deposition and Anneal	Al, Sputtering $\longrightarrow$ 350°C FGA

Table 3.3 Process flow of Ge MOS capacitors with HfO_2, deposited by e-beam evaporation with reactive atomic O beam as gate dielectric.

3.2 Physical Characterization

It is increasingly difficult to characterize ultra-thin gate dielectric films (typically 0.1 nm to 3.0 nm) used in MOS devices. Input from various physical characterization techniques is needed to improve the knowledge of structure and composition of these thin films. Scanning electron microscopy evaluates the surface structure of film in terms roughness and non-uniformity, while X-ray photoelectron spectroscopy characterize the elemental and molecular nature of thin films. It can determine the nature of bonds present between different elements in the film depending upon their binding energy.

3.2.1 Scanning Electron Microscopy

Field emission scanning electron microscopy (FESEM) [72] was used to study the surface of films after and before annealing. The main advantage of FESEM is that high quality images of insulating surfaces can be taken with nanometer resolution and negligible electrical charging of samples, without the need of conductive coating.

3.2.2 X-ray Photoelectron Spectroscopy

X-ray photoelectron spectroscopy, XPS is primarily used for identifying chemical composition of the films. Electrons can be emitted from any orbital with photoemission occurring for X-ray energies exceeding the binding energy. This is illustrated with the energy band diagram in Fig. 4.2 and the schematic in Fig. 4.3. Primary X-rays of 1-2 keV energy eject photoelectrons from the sample. The measured energy of the ejected electrons at the spectrometer E_{sp} is related to the binding energy E_b, referenced to the Fermi energy E_F by

$$E_b = h\nu - E_{sp} - q\phi_{sp} \qquad (3.1)$$

where $h\nu$ is the energy of primary X-ray and ϕ_{sp} is the work function of the spectrometer (3 to 4 eV).

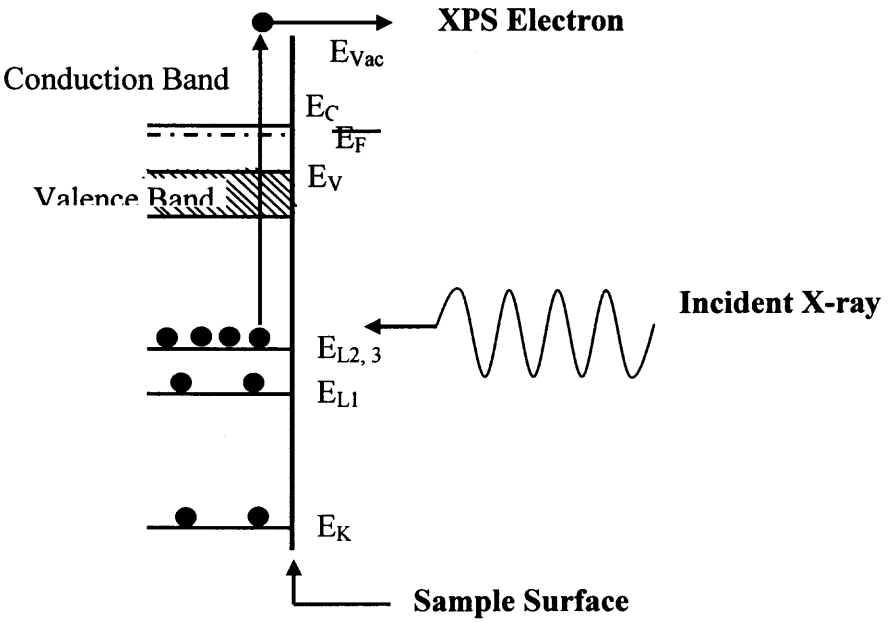

Fig. 3.1 Electronic processes in X-ray photoelectron Spectroscopy [72].

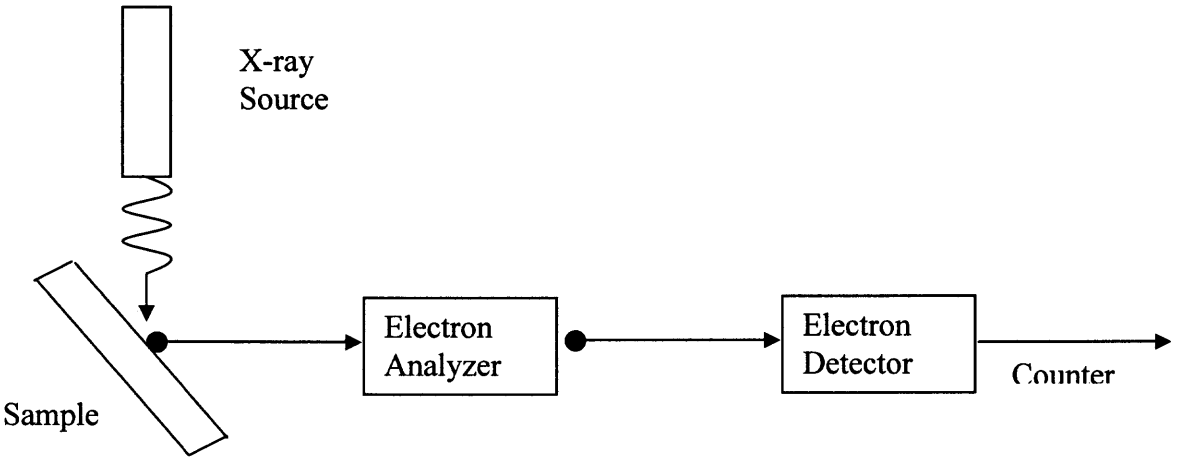

Fig. 3.2 XPS measurement schematic

The electron binding energy is influenced by its chemical surroundings making it suitable for determining chemical states. Though X-rays possess no charge, electron emission from the sample may cause positive sample charging, especially for insulators.

3.3 Electrical Characterization

Measurements of the electrical properties, parameters extracted from these measurements and control over these parameters lead to stable and high performance MOS devices. Bulk oxide and oxide-substrate interface are two major regions of the MOS system. Charges in these two regions are undesirable because they adversely affect the device performance and stability. The MOS capacitor is being used to study the electrical characteristics as it has the advantage of simplicity of fabrication and analysis. Following measurements techniques have been employed in characterizing the charges present in MOS capacitors using HfO_2 as gate dielectric.

3.3.1 High Frequency and Low Frequency C-V Measurements

The high frequency (HF) and low frequency (LF) measurements were carried out using Boonton Capacitance meter and HP 4284A. Measurements were carried out from high frequency of 1Mz to low frequency of 1kHz. The devices were probed using cascade microtech probe station. From the low frequency curve and the high frequency curve we can get information of the interface states. Interface states or "fast states" can be detected as a stretch out of the high frequency C-V curve of a MOS capacitor or a distortion in the

LF C-V curve. Oxide charge on the other hand causes a rigid shift along the voltage axis of the high frequency CV curve, and is detected as a change in the flat band voltage of the device [49]. A shift in the HF curve indicates the effect of the annealing effect. A post deposition anneal can reduce the oxide charges.

3.3.2 Conductance Measurement

The conductance measurements were carried out at various frequencies using HP 4284A. The frequencies were 1 KHz, 10kHz, 100 KHz, 1 MHz. This was used to measure the interface state density (D_{it}) which was computed using equation (3.4) and (3.5) [73].

$$\frac{G_P}{\omega} = \frac{\omega G_m C^2_{ox}}{G^2_m + \omega^2 (C_{ox} - C_m)^2} \qquad (3.2)$$

$$D_{it} = \frac{2.5}{q} \left(\frac{G_P}{\omega}\right)_{max} \qquad (3.3)$$

Where G_P is interface trap conductance, G_m is the conductance measured, C_{ox} is the accumulation capacitance, ω is the frequency, C_m is the measured capacitance at the particular frequency and gate voltage.

3.3.3 Estimation of Interface State Density by Terman Method

3.3.3.1 Plotting the Ideal C-V Curve. Ideal C-V curve can be plotted by calculating gate bias voltage V_g for different surface potential ψ_s and calculating the corresponding differential capacitance. Gate bias voltage is given by

$$V_g = V^o_{FB} + \frac{Q_S}{C_{ox}} + \psi_S \qquad (3.4)$$

here V^o_{FB} is ideal flatband voltage, C_{ox} isgate oxide capacitance, and Q_s is the charge in semiconductor given by,

$$Q_S = \sqrt{2\left(\frac{kT}{qL_D}\right)}\left\{\left[\frac{q\psi_s}{kT} + \exp\left(\frac{-q\psi_s}{kT}\right) - 1\right] + \left(\frac{n_i}{N_d}\right)^2\left[\exp\left(\frac{q\psi_s}{kT}\right) - 1\right]\right\}^{\frac{1}{2}} \quad (3.5)$$

here k is Boltzman's constant, T is temperature, n_i is intrinsic carrier concentration and L_D is Debye length calculated as,

$$L_D = \sqrt{\frac{\varepsilon_{Si} kT}{q^2 N_d}} \quad (3.6)$$

here ε_{Si} is dielectric constant of silicon, and N_d is doping concentration.

Putting all the constant terms in eq. (3.6) at room temperature

$$Q_s = 9.282\times10^{-17}\sqrt{N_d}\left[\frac{-q\psi_s}{kT} + \exp\left(\frac{q\psi_s}{kT}\right) - 1\right]^{\frac{1}{2}} \quad (3.7)$$

Differential capacitance, C_{diff}, can be calculated as

$$C_{diff} = \frac{C_{ox} \times C_S}{C_{ox} + C_S} \quad (3.8)$$

where C_s is semiconductor capacitance, given by

$$C_S = \frac{\in_{Si}}{\sqrt{2}L_D} \times \left| \frac{\left[1 - \exp\left(\frac{-q\psi_S}{kT}\right) + \left(\frac{n_i}{N_d}\right)^2 \exp\left(\frac{q\psi_S}{kT}\right)\right]}{\left\{\left[\frac{q\psi_S}{kT} + \exp\left(\frac{-q\psi_S}{kT}\right) - 1\right] + \left(\frac{n_i}{N_d}\right)^2\left[\exp\left(\frac{q\psi_S}{kT}\right) - 1\right]^{\frac{1}{2}}\right\}} \right| \quad (3.9)$$

Again Putting all the constant terms we get

$$C_s = 1.785\times10^{-15}\sqrt{N_d}\left|\frac{\left[\exp\left(\frac{q\psi_S}{kT}\right)-1\right]}{\left[\frac{-q\psi_s}{kT}+\exp\left(\frac{q\psi_s}{kT}\right)-1\right]^{\frac{1}{2}}}\right| \qquad (3.10)$$

Assuming different values of surface potential ψ_s ranging from depletion region to limited accumulation, corresponding differential capacitance is calculated to plot the ideal C-V curve.

3.3.3.2 Extraction of Interface State Density. In a MOS capacitor without interface traps, overall charge neutrality requires the change in gate charge (δQ_g) to be balanced by a change in silicon surface charge (δQ_s) i.e.

$$\delta Q_g + \delta Q_s = 0 \qquad (3.11)$$

Therefore, band bending changes to bring about this balance. However, in a MOS capacitor with interface traps, a change in interface charge density (δQ_{it}) also occurs with any change in band bending. Therefore charge balances satisfies

$$\delta Q_g + \delta Q_{it} + \delta Q_s = 0 \qquad (3.12)$$

This interface state Density D_{it} can be calculated as:

$$D_{it} = \frac{C_{ox}}{q}\frac{d(\Delta V_G)}{d\psi_s} \qquad (3.13)$$

Where $\Delta V_g = V_g - V_g(Ideal)$ is the voltage shift of the experimental from the ideal curve with V_g being the experimental gate voltage.

3.3.4 Stress Measurement

High field stress in ultra thin gate oxides of MOS devices is known to degrade the oxide quality and eventually lead to oxide breakdown. Charge trapping in the oxide is used to

monitor the degradation of the oxide. We have used constant voltage stress (CVS) to analyze the reliability of HfO_2 on Ge substrate. HP 4145 was used to for CVS. The initial characteristics of the device- leakage current and the high frequency (HF) and low frequency (LF) C-V were measured. Following this the devices were stressed for a different period of time and leakage current and HF and LF C-V measurements were conducted to study the effect of the stress at the interface of Ge/HfO_2 and the bulk oxide.

3.3.5 Low Temperature Measurements

Low temperature characterization is useful in understanding the bulk oxide traps and interface traps behavior. It provides detailed description of the type of trapping taking place in the bulk oxide as well as at the interface. Furthermore, activation energy (E_T) of traps from the conduction band edge can be calculated from flatband voltage shift (ΔV_{FB}) at different temperatures. A temperature range of 300°K to 130°K has been used for measurements. CTI Cryogenics M22 closed loop helium cooled refrigeration system and Palm Beach Cryophysics model 4075 temperature controller were used for low temperature measurements.

CHAPTER 4

ELECTRICAL CHARACTERISTICS OF THERMALLY EVAPORATED HfO_2 ON Si SUBSTRATE

This chapter discusses electrical characterization of the thermally evaporated HfO_2 on silicon substrate. HfO_2 film deposition was done at Sarnoff Corporation. Devices were fabricated using the process flow described in table 3.2. Characterization was performed using techniques mentioned in section 3.3.

4.1 C-V Characteristics

Fig. 4.1 shows the normalized C-V characteristics of 50nm HfO_2 film at various annealing temperatures along with an ideal C-V curve, plotted by calculating the differential capacitance across the MOS gate stack between the experimentally measured accumulation capacitance and the silicon depletion capacitance as a function of gate voltage [80]. For these measurements, Al gate MOS capacitors with an area of 1.26×10^{-3} cm^2 were used. Measurements were taken before annealing as well as after 350°C and 450°C forming gas (FGA) annealing. Comparison of experimental C-V curves with that of the ideal C-V curve (no oxide charge) shows that experimental C-V curve has moved closer to ideal curve indicating a reduction in bulk oxide charge from $6.97\times10^{11}/cm^2$ before annealing to $1.61\times10^{11}/cm^2$ after 450°C annealing. The high value of oxide charge ($\sim10^{11}/cm^2$) indicates significant contribution from the interface-trapped charge. The fact that the C-V curves stretch out near inversion region after 450°C annealing also supports the presence of high density of interface states.

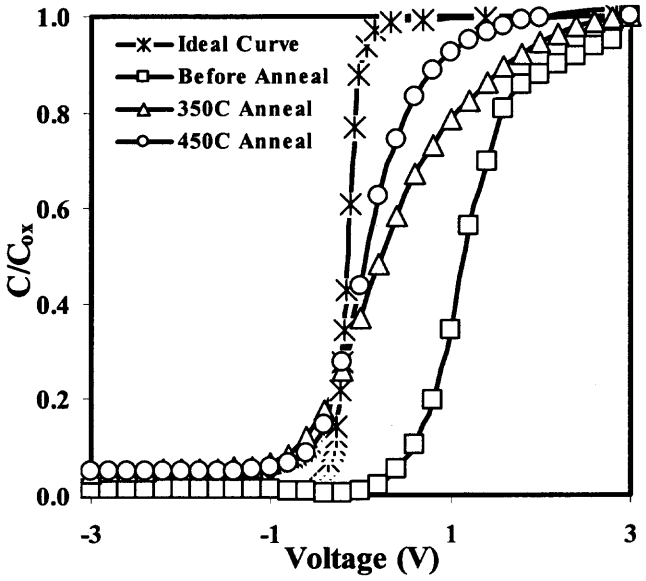

Fig. 4.1 Normalized C-V curves of MOS capacitors with 50nm HfO_2 film compared with ideal C-V curve. Bulk oxide charges were reduced to $1.61 \times 10^{11}/cm^2$ and interface state density was found to be $1.75 \times 10^{12}/cm^2eV$ after samples were annealed at 450°C.

The C-V curves show a reduction in hysteresis from 2.3V to 0.03V after 350°C anneals in comparison to as deposited film, shown in Fig. 4.2. No significant improvement was seen in hysteresis characteristics after 450°C anneal, though left shift in C-V curve indicates the reduction in bulk trap with high temperature annealing. The reduction in hysteresis indicates the reduced charge trapping under negative gate bias. Partial passivation of interface states is also observed as a result of FGA. No reduction in oxide capacitance was observed after 450°C annealing. However, it is believed that an Al_2O_3 layer or SiO_2 layer could have formed at the aluminum-HfO_2 interface and silicon-HfO_2 interface, respectively, during post metal annealing. Densification of HfO_2 is also

possible because of annealing. Thus, the observed combined effect shows an increase in net capacitance suggesting minimum impact of interfacial layer.

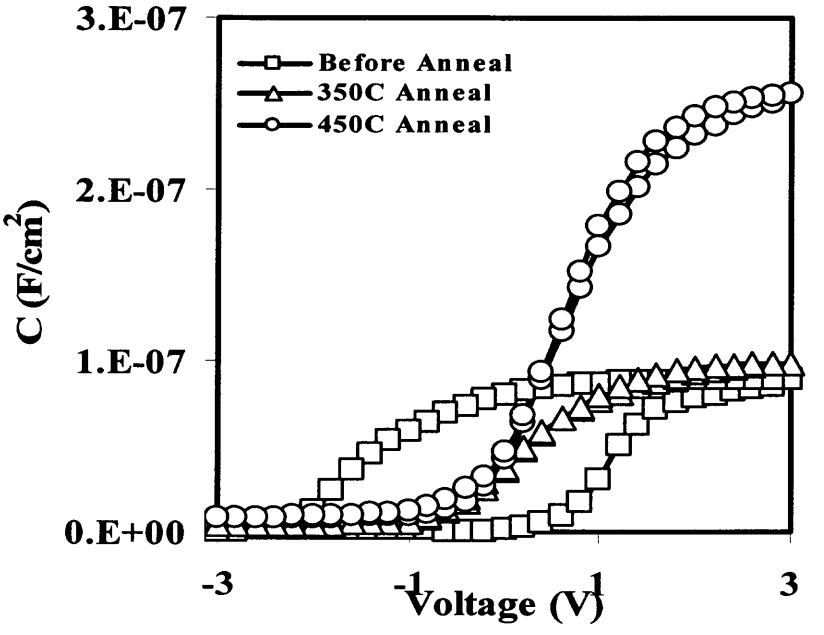

Fig. 4.2 Normalized C-V curves of MOS capacitors with 50nm HfO_2 film at different annealing temperatures. Hysteresis reduced to 30mV after 450°C FGA.

When experimental C-V curves of 60nm HfO_2 films were compared with that of the ideal C-V curves, shown in Fig. 4.3, an increase in bulk oxide charges from 8.72 × $10^{11}/cm^2$ before annealing to 1.15 × $10^{12}/cm^2$ after 450°C annealing is noticed. This increase in oxide charge in 60nm HfO_2 could be due to stoichiometric defects or extensive interface defects as the C-V curves in Fig. 4.3 have moved farther away from ideal curve after 450°C annealing.

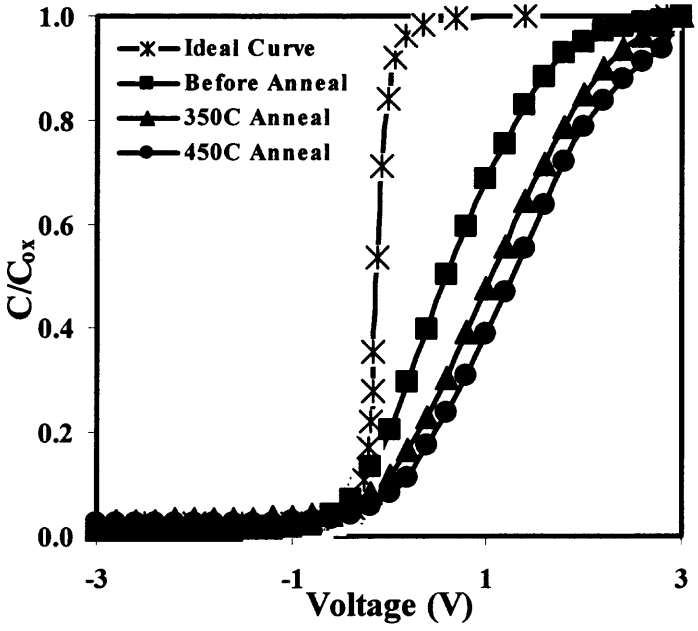

Fig. 4.3 Normalized C-V curves of MOS capacitors with 60nm HfO_2 film compared with ideal C-V curve. Bulk oxide charges were increased up to 1.15 × $10^{12}/cm^2$ and interface state density was increased to $6.47\times10^{12}/cm^2eV$ after a 450°C anneal.

After 350°C anneal, hysteresis was reduced compared to as deposited films but the stretch out near inversion capacitance (C_{min}) indicates that there is significant charge trapping remains at interfacial region near the Si substrate, shown in Fig. 4.4. After 450°C annealing, C-V curves are more symmetric for voltage sweep indicating a partial passivation of interface states. Increase in accumulation capacitance after 450°C annealing suggests that some densification of HfO_2 has also occurred for 60nm films. Hysteresis was reduced to less than 175mV but still it's significantly higher than the 50nm HfO_2 film (Fig. 4.2). The C-V characteristics, therefore, show better electrical performance for 50 nm HfO_2 films than 60 nm thermally evaporated HfO_2 films.

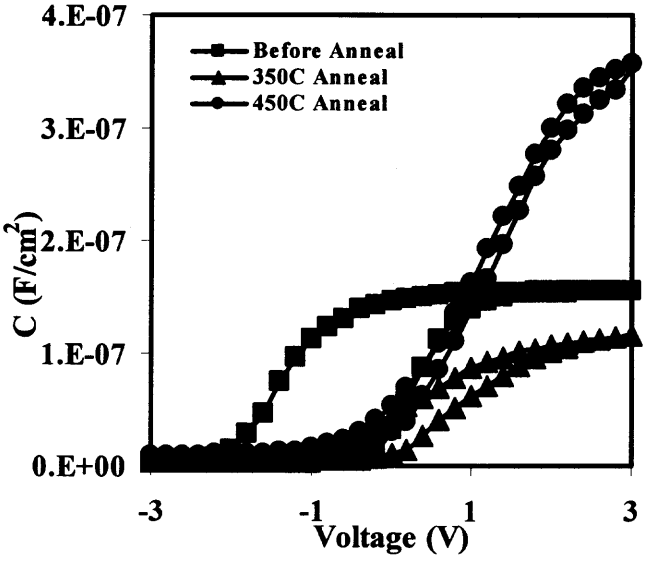

Fig. 4.4 Normalized C-V curves of MOS capacitors with 60nm HfO_2 film at different annealing temperatures. Hysteresis reduced to 175mV after 450°C FGA.

4.2 Dielectric Constant

Dielectric constant estimated from effective capacitance is found to be in the range of 18-25. Table 4.1 shows the dielectric constant obtained by thermal evaporation and is being compared with the dielectric constants obtained for HfO_2 films by other techniques. The dielectric constant of thermally evaporated films obtained in this work is somewhat in a higher range. Lower value of effective dielectric constants of HfO_2 gate stack formed by other techniques is attributed to the interfacial layer thickness between silicon substrate and HfO_2 after post deposition anneal (PDA) [74, 79]. If there is a growth of thin SiO_2 layer at the HfO_2 and silicon interface then a noticeable reduction in effective capacitance will be observed. Because the effective oxide thickness is estimated from the two

capacitances (interfacial layer and high-κ layer) in series. The high dielectric constant of our thermally evaporated HfO_2 films could be attributed to lack of interfacial SiO_2 layer as our samples were not subjected to high temperature anneal.

Film Deposition Techniques	Lowest Dielectric Constant	Highest Dielectric Constant
Thermal Evaporation	18	25
Electron beam Evaporation [74]	18	22
Sputtering [75]	18	21
Atomic Layer Deposition [76]	16	23
Remote Plasma Oxidation [77]	19	19
Plasma Enhanced CVD [78]	14	16

Table 4.1 Dielectric constant comparison with other current techniques.

4.3 Trapped Charge

To further investigate the oxide charge, flatband voltage shift (ΔV_{FB}) was plotted as a function of annealing as shown in Fig. 4.5. For 50nm HfO_2 film, ΔV_{FB} has decreased from 1.1V before annealing to 0.01V after 450°C annealing; while for 60nm thick hafnium oxide ΔV_{FB} has increased from 0.04V before annealing to 0.8V after 450°C annealing. One of the possible reasons for this behavior in 60 nm HfO_2 films could be due to higher built-in stress during the deposition of HfO_2 films, in comparison to 50nm film. Built-in stress generates bulk oxide defects as well as interface defects after the annealing of the films.

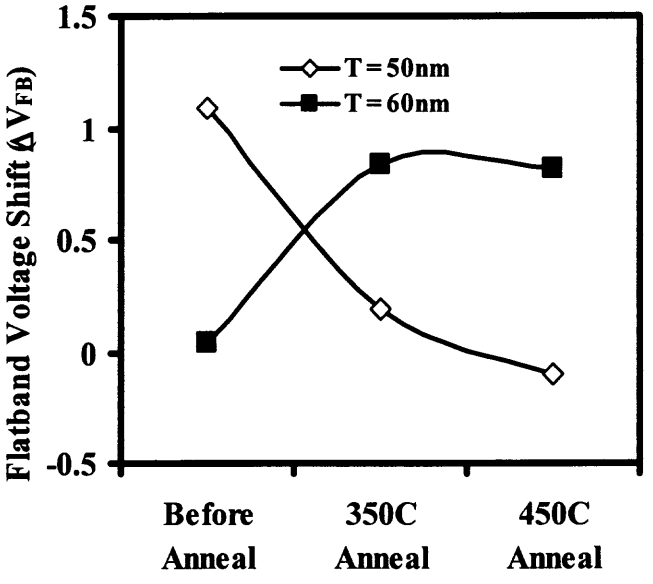

Fig. 4.5 Effect of annealing on flatband voltage shift (ΔV_{FB}). In 50nm HfO_2 films, ΔV_{FB} has reduced from 1.1V to 0.01V, while in 60nm HfO_2 films it has increased from 0.04V to 0.8V.

Effect of annealing on interface state density of these MOS capacitors is shown in Fig. 4.6. Terman method was employed to estimate interface trap density. Even though Terman method has limited accuracy it provides a quick estimate of interface trap density. Increase in interface state density was observed in both the cases as a result of annealing. In case of 50nm HfO_2, it has increased from $0.706\times10^{12}/cm^2eV$ before annealing to $1.75\times10^{12}/cm^2eV$ after 450°C annealing, while in case of 60nm it has increased from $2.2\times10^{12}/cm^2eV$ before annealing to $6.47\times10^{12}/cm^2eV$ after 450°C annealing. The significant degradation of interface quality in 60 nm HfO_2 films could be due to the relaxation of the stress after annealing.

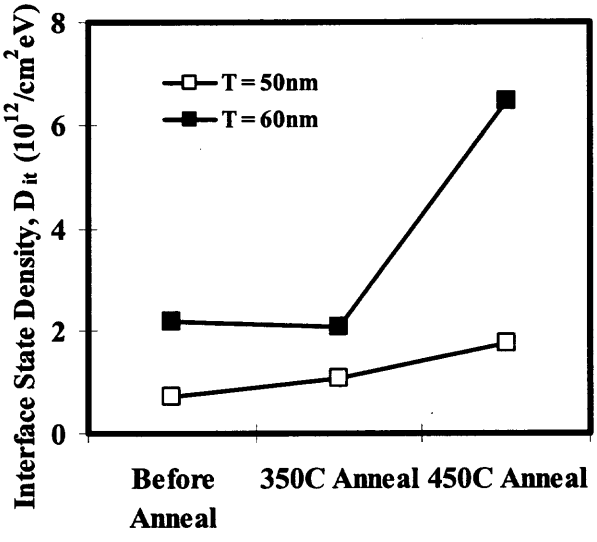

Fig. 4.6 In 50nm HfO_2 films, interface state density (D_{it}) has increased from 0.706×10^{12}/cm^{2}eV before annealing to 1.75×10^{12}/cm^{2}eV after 450°C annealing, while in 60nm HfO_2 films it has increased from 2.2×10^{12}/cm^{2}eV before annealing to 6.47×10^{12}/cm^{2}eV after 450°C annealing.

4.4 Leakage Current

Effect of annealing on leakage current density of 50 nm and 60 nm HfO_2 films is shown in Fig. 4.7. Leakage current density was decreased by more than two orders of magnitude after 450°C annealing in comparison to 350°C annealing in both of the HfO_2 films. Leakage current density of 50nm HfO_2 films was reduced to $<10^{-7}$amp/cm^2 at 1V after 450°C annealing. Though the leakage current density of 60nm HfO_2 was reduced after 450°C annealing but it is lower in 50nm films in comparison to 60nm. The observed improvement in leakage current in 50 nm film is possibly due the partial passivation of dangling bonds at the Si-HfO_2 interface as noticed from the C-V characteristics. In 60 nm films, however, the leakage current becomes resistive around 1V indicating a large increase of interface states after 450°C annealing.

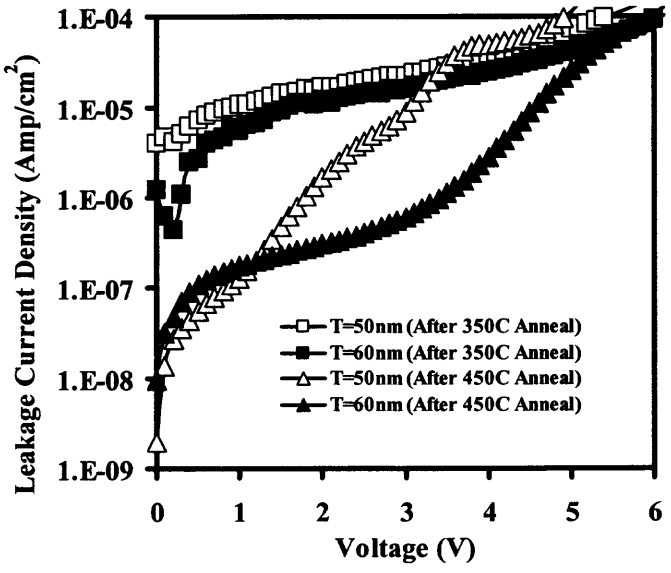

Fig. 4.7 Leakage current density in 50nm and 60nm HfO_2 film MOS capacitor after 350°C and 450°C annealing.

4.5 Traps Behavior at Low Temperatures

Since 50 nm HfO_2 films have shown better device performance in comparison to 60nm HfO_2 films, we have investigated the charge trapping characteristics of 50 nm films at various temperatures. MOS capacitors with 50 nm HfO_2 films of area size 1.96×10^{-3} cm^2 were studied. Temperature was gradually decreased from 290 to 130K and high frequency C-V measurements were taken once the sample attained a stable temperature.

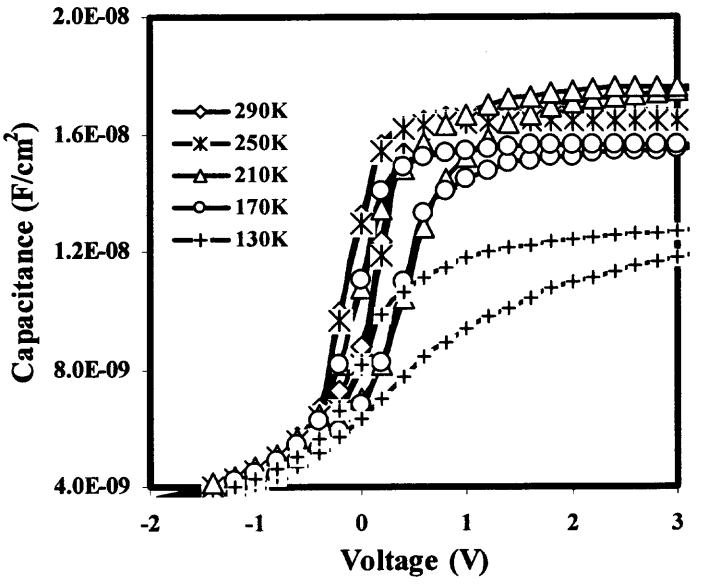

Fig. 4.8 Low temperature C-V curves for 50nm HfO_2 MOS capacitor.

C-V curves, at different temperatures in Fig. 4.8, demonstrated both parallel shift and stretch out along the bias axis as temperature was decreased. This verifies the presence of higher number of both shallow bulk oxide and interface trapped charges at low temperatures. Electron trapping seems to be dominant because higher barrier of holes in HfO_2 (3.4eV) compared to electrons (1.5eV) enhances the electron trapping probability [91]. The electron traps, especially shallow bulk oxide ones with energy levels close to conduction band of HfO_2 became more effective as temperature went down and this contributed to the shift of the C-V curves at low temperatures [87]. Moreover, we can observe hysteresis above midgap voltage in the C-V curves at low temperature (Fig. 4.8).

Flatband voltage shift (ΔV_{FB}) was calculated for the devices under test at different temperatures. Fig. 4.9 shows the ΔV_{FB} for some samples at temperatures ranging from

290K to 130K. A turn around effect was observed in ΔV_{FB} as it increased initially when temperature was decreased to 210K, and then it stared to decrease when the temperature was decreased further to 130K.

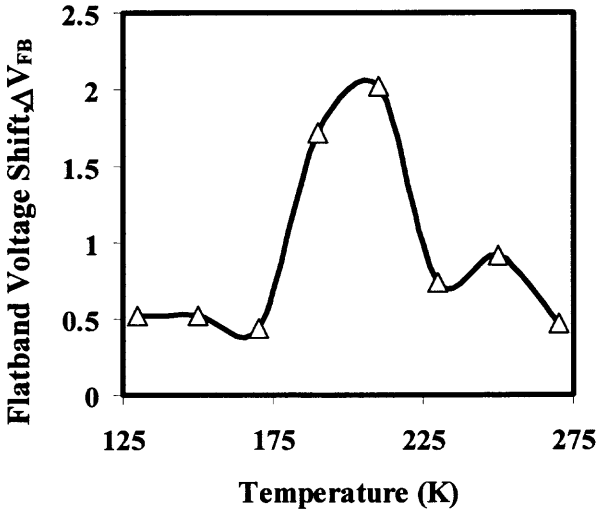

Fig. 4.9 Flatband voltage shift as a function of temperature for 50nm HfO_2 MOS capacitor.

To explain this turn around effect in $\Delta V_{FB,}$ concept of trapped charge centroid was used [91]. In these devices oxide charge is the only variable observed when the temperature was reduced. Considering the one-dimensional distribution of trapped charges along the oxide thickness, the oxide charge centroid can be defined as [92],

$$q \int_0^{t_{ox}} x\rho(x)dx = qN_{t-equiv} \bullet x_t \qquad (4.1)$$

where $\rho(x)$ is the trapped charge distribution function, t_{ox} is the oxide thickness, and $N_{t\text{-}equiv}$ is the equivalent trapped charge per unit area having centroid at x_t. Here, trapped charges consist of both interface and oxide trapped charges, and $x_t = 0$ at the gate and $x_t = t_{ox}$ at the substrate (Fig. 4.10).

It is obvious from eq. (4.1) that density, location and polarity (positively charged/negatively charged) of individual traps affect the location of centroid. Considering only the contribution of trapped charges in ΔV_{FB} [92] we get,

$$\Delta V_{FB} = -q \frac{\Delta N_{t-equiv}}{C_{ox}} \bullet \frac{x_t}{t_{ox}} \qquad (4.2)$$

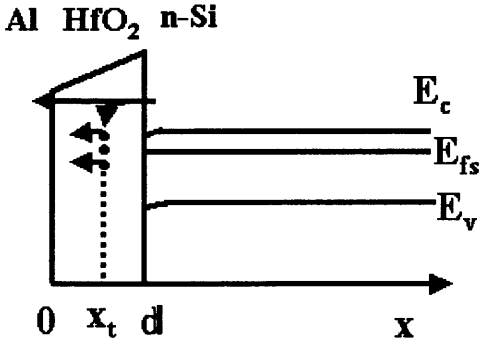

Fig. 4.10 Energy diagram for Al–HfO_2 –n-Si showing centroid shifting towards the gate electrode.

Cox is the oxide capacitance, q is the charge of an electron and $\Delta N_{t-equiv}$ is the change in equivalent trapped charge. If negatively charged bulk oxide traps dominate and electron trapping mostly occurs near the substrate, location of centroid shifts towards the substrate and positive shift in flat band voltage takes place. On the other hand, if electron trapping near the gate dominates centroid will move towards the gate as shown in the Fig.4.10 and this result in less positive shift in flatband voltage compared to the former case. It is obvious from the Fig. 4.9 and eq. (4.2) that charge centroid due to electron trapping was located near the substrate in 290-210K range as ΔV_{FB} steadily increased, but located near the gate as ΔV_{FB} decreased in 210-130K range.

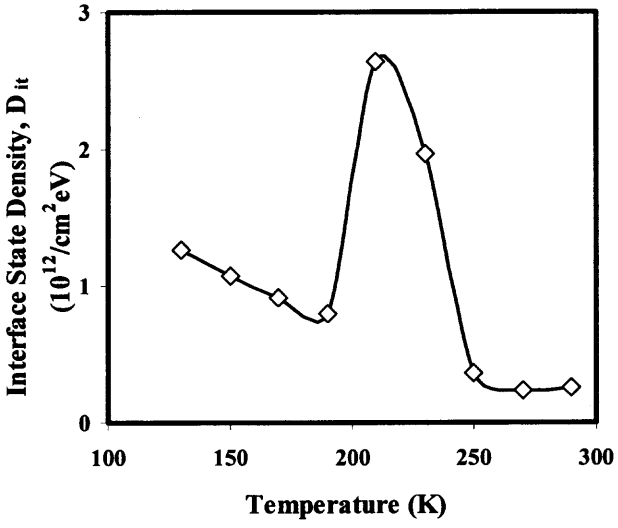

Fig. 4.11 Interface state density, D_{it}, as a function of temperature for various Al/HfO_2/n-Si MOS samples.

As stated earlier, both interface traps and bulk oxide traps contribute to the location of charge centroid. To investigate interface trap characteristics in details, D_{it} values for different temperatures are shown in Fig. 4.11. Since the D_{it} shows a similar turnaround effect and D_{it} is directly related to amount of interface-trapped charge, it suggests that interface states strongly contribute to the low temperature charge trapping characteristics. We may assume that at the Si/HfO_2 interface all interface states above intrinsic level E_i are acceptor type and below E_i are donor type [93] and acceptor type traps are negatively charged when filled and neutral when empty, whereas donor type traps are neutral when filled and positively charged when empty. At the flat band condition Fermi level E_{fn} is higher than E_i at the Si/HfO_2 interface for n-type substrate, and interface states above E_{fn} and below E_i are neutral [93]. Only the acceptor type

interface traps having energy levels in between E_{fn} and E_i capture electrons and get negatively charged and thus contribute to the positive shift of the flatband voltage. The concentration of interface states is, therefore, highest within the energy levels in between E_{fn} and E_i at the HfO_2/Si interface. It further confirms that the domination of electron trapping by shallow interface traps near the substrate in 290K - 210K range and near the gate in 210K - 130K range, which subsequently shifted the trapped charge centroid towards the substrate and gate respectively, may be the principal cause behind the turn around effect in ΔV_{FB}.

4.6 Effect of Aging

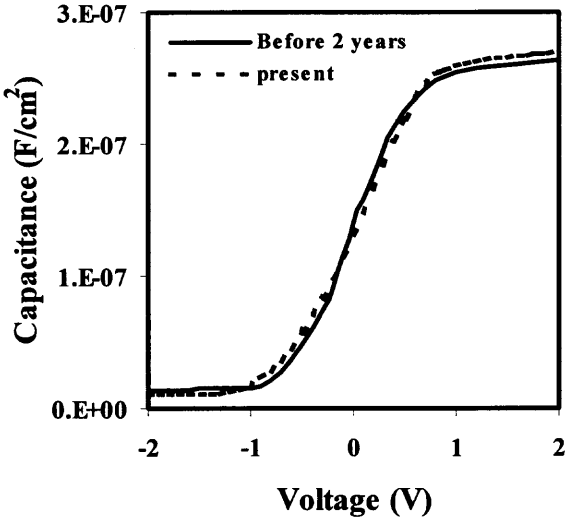

Fig. 4.12 Comparison of C-V characteristics of 50nm HfO_2 films before and after 2 years.

C-V measurements were taken for 70 MOS capacitors of various diameters ranging from 50μm to 500μm after 2 years to see the effect of environment on the device

characteristics. Fig. 4.12 compares the C-V characteristics of one of these devices before and after 2 years. Maximum variation in device characteristics after 2 years, from before, is within 5%. If the films were deposited with low packing density or with excessive background pressure they may exhibit change in its composition with time. Our films seem to be of good quality since no changes were observed.

Fig. 4.13 Interface state density and Flatband voltage of 50nm HfO_2 films before and after 2 years.

Fig. 4.13 shows the flatband voltage and interface state density distribution of these devices before and after 2 years. Minimal variation of V_{FB} and D_{it} distribution was observed, indicating excellent quality of these HfO_2 films.

4.7 Comparison with E-Beam Evaporation

Another physical vapor deposition technique, e-beam evaporation, has also been used in depositing HfO_2 films as gate dielectrics by Harris *et al* [74]. Annealing of these films at 400°C for 45 min. in H_2 reduced the large hysteresis of 500mV observed in unannealed films to 20mV. Leakage current also reduced to $<10^{-7}A/cm^2$ after annealing. Similar

phenomenon was observed in thermally evaporated films when annealed in FGA at 450°C. This indicates that annealing helps in passivating large number of trapping sites present in as deposited films. However, films deposited by e-beam evaporation exhibits large bulk oxide traps of ~10^{12}/cm^2 after annealing, one order of magnitude higher than thermally evaporated HfO_2 films. Though interface state density is in same order of magnitude in both deposition techniques (~10^{12}/cm^{2}eV), but after annealing it seems to be reducing in e-beam evaporated films (from 6.5×10^{12} /cm^{2}eV to 0.6×10^{12} /cm^{2}eV) while increasing in thermally evaporated HfO_2 (from 0.7×10^{12} /cm^{2}eV to 1.8×10^{12} /cm^{2}eV). Less oxide defects observed in thermally evaporated films makes thermal evaporation a preferable technique for HfO_2 deposition on silicon substrate.

4.8 Summary

Electrical characteristics of MOS capacitors with thermally evaporated HfO_2 films have been investigated. Characteristics such as hysteresis, leakage current density and flatband voltage shift have significantly reduced after 450°C FG anneal in 50 nm HfO_2 films. Bulk oxide charges have decreased after annealing in 50nm HfO_2 films whereas it increased for 60 nm films. Interface state density is found to be slightly higher as compared to other techniques and moderately increased with annealing. C-V characteristics taken even after 2 years didn't show major variations, indicating that enhanced quality of films.

Furthermore, shifts in C-V curves and turn around effect in flat band voltage shifts were observed in 290-130K temperature range giving the charge trapping characteristics of HfO_2 films. Even though the films studied in this work is higher than

the thickness required for nano-scale device application, the electrical properties investigated here suggest that thermally evaporated HfO_2 films can be suitable for metal-oxide-semiconductor device applications with enhanced process optimization.

CHAPTER 5

CHARATERISTICS OF THERMALLY EVAPORATED HfO_2 ON Ge SUBSTRATE

HfO_2 films deposited by the thermal evaporation on Si substrate has shown promising performance, therefore, deposition of HfO_2 film on Ge have also been explored. In this chapter, physical and electrical characteristics of ultra-thin HfO_2 films deposited by thermal evaporation on Ge substrate are presented. MOS capacitors were fabricated using the process described in table 3.2.

5.1 Physical Characterization

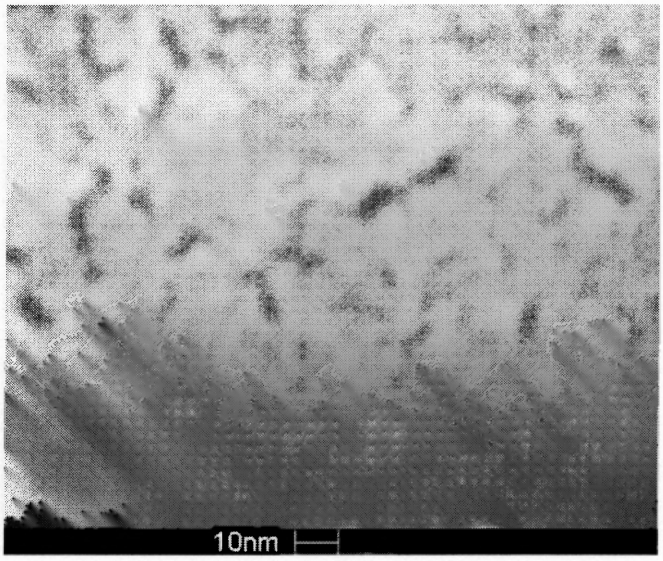

Fig. 5.1(a) Top Down scanning electron microscopy image of as deposited thermally evaporated HfO_2 on top of Ge substrate.

Fig.5.1a shows the SEM image of as deposited HfO_2 film on the Ge substrate. The surface of the HfO_2 film shows island-like morphology. The film appears to have a rough

surface and is not uniform. Similar type of surface structure has been reported for as deposited HfO_2 film on germanium substrates by Wu *et al* [81] using atomic force microscopy, where surface roughness was attributed to the presence of GeO_2 interfacial layer. After 500°C anneal in N_2 environment film surface seems to be smooth without any significant surface roughness as shown in Fig. 1b. This suggests that the film went through structural transformation during annealing.

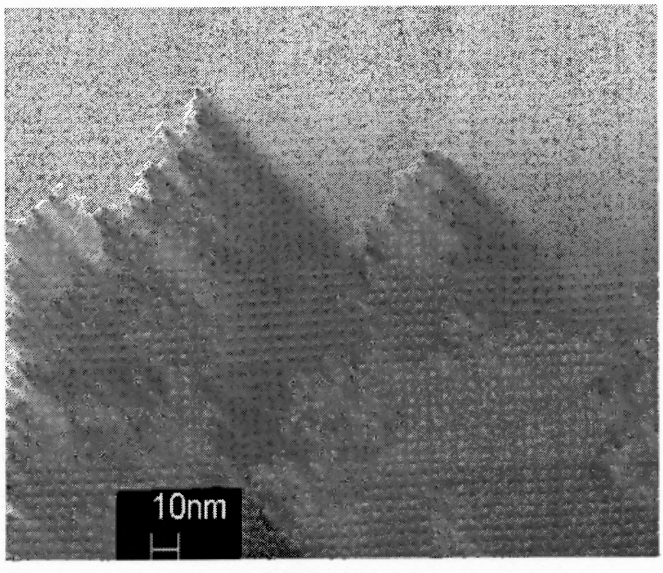

Fig. 5.1(b) Top Down scanning electron microscopy image of 500°C annealed HfO_2 films .on top of Ge substrate.

The as deposited HfO_2 film was analyzed by X-ray diffraction for structural analysis. Fig. 5.2 shows the XRD spectra of as deposited HfO_2 Film. A peak was observed at an angle of 66.7° corresponding to GeO_2. No other peaks were detected indicating the desired amorphous nature of the dielectric film. Presence of crystalline GeO_2 has also been detected at the interface [70] of the film deposited by metal-organic chemical vapor deposition (MOCVD) as GeO_2 induced by gaseous O_2 is found to be

polycrystalline [82]. It is possible that even after cleaning the surface, some formation of GeO_2 could have taken place prior to thermal evaporation of HfO_2. Therefore, due to the non-uniformity of GeO_2 induced by the oxidation of Ge [82], hafnium oxide films deposited on top of this non-uniform interfacial layer also exhibited non-uniform characteristics as seen in SEM image (Fig. 5.1a).

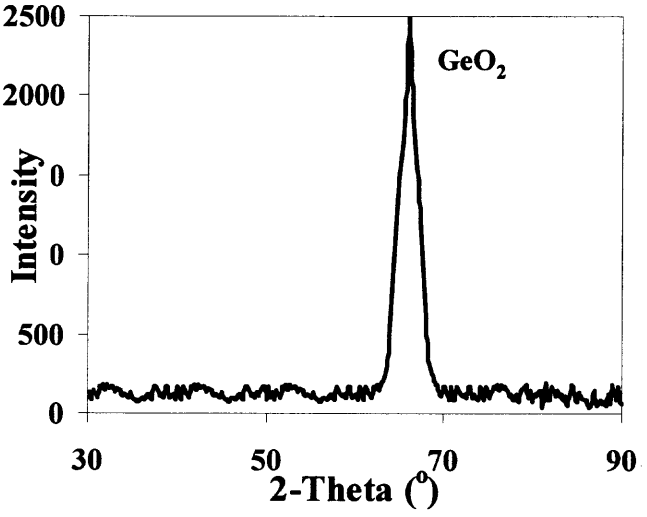

Fig. 5.2 X-Ray Diffraction spectra of the as deposited films. Peak indicates the presence of crystalline GeO_2.

As the SEM images after the 500°C annealing show the significant improvement on the uniformity of the dielectric film, XPS was done to study the effect of annealing on the composition of gate dielectric. Fig. 5.3a shows the XPS spectrum of Hf 4f peak for HfO_2. Also, Ge 2p3 peaks were detected at 1220.9 eV and identified for GeO_2, which shows the possible incorporation of Ge into HfO_2 (Fig. 5.3b). Since no signal was observed for Ge or Ge-Hf bond, it indicates that the dielectric film is composed of both GeO_2 and HfO_2. Similar film composition has been observed for the HfO_2 films deposited by other techniques [70] on Ge substrate without any surface treatment.

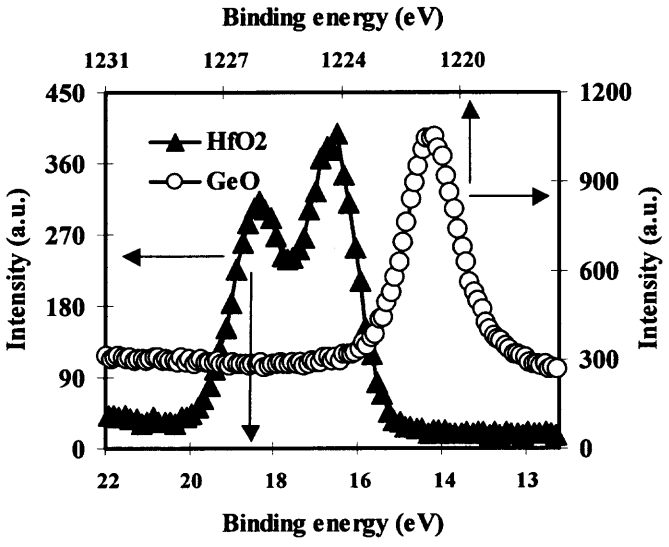

Fig. 5.3 X-Ray Photoelectron Spectroscopy spectra of Hf4f and Ge2p3 for HfO_2 films after 500°C annealing.

5.2 Electrical Characterization

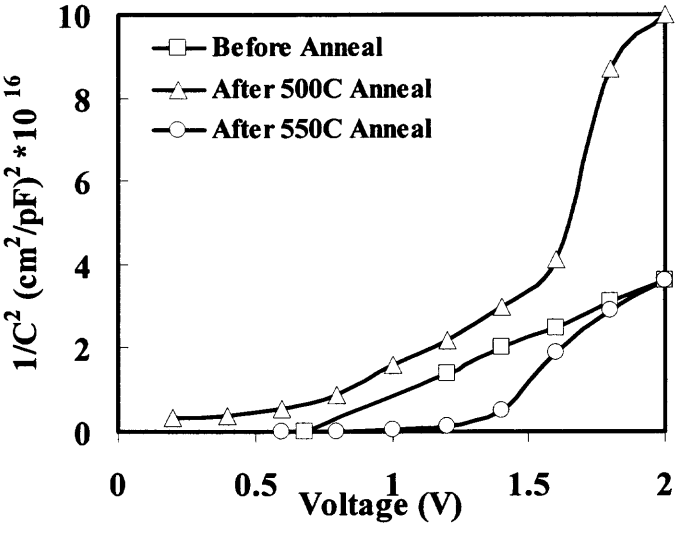

Fig. 5.4 $1/C^2$ vs. applied gate voltage for MOS capacitors with 5nm HfO_2 films before anneal and after anneal. Barrier height, calculated from the intercept on voltage axis is in the range of 0.38V to 0.68V.

C-V characteristics of the devices with as deposited 5nm HfO_2 films don't demonstrate a typical MOS capacitor behavior. A linear dependence is observed for $1/C^2$ vs. applied gate voltage (V) as shown in Fig 5.4. This suggests a rectifying behavior for as deposited devices. It implies that the as deposited films were either hafnium rich at the Ge/HfO_2 interface or they were rather non-uniform. The barrier height calculated from $1/C^2$-V plot of devices with as deposited HfO_2 film was in the range of 0.38V to 0.68V.

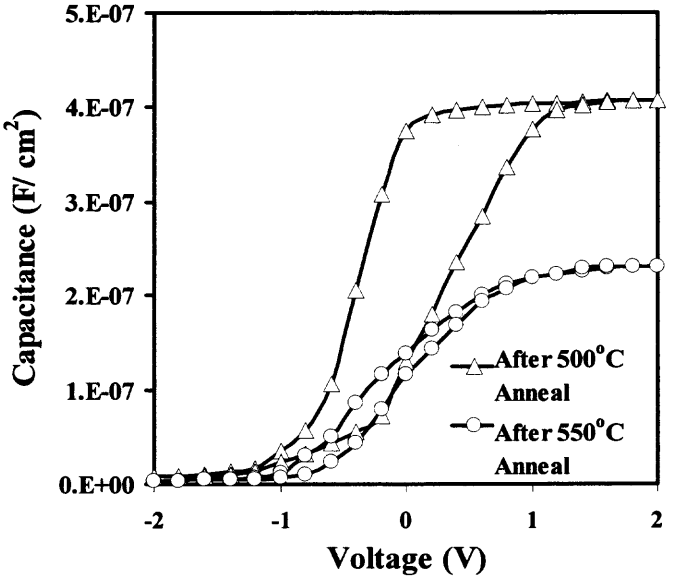

Fig. 5.5 Capacitance–Voltage characteristics of devices with 5nm HfO_2 films after annealing at 500°C and 550°C in N_2 environment. Hysteresis reduced to 0.2V while EOT and V_{FB} increased to 10.5nm and 1.23V, respectively, after 550°C annealing.

After annealing of these films at 500°C and 550°C in N_2 ambience transformation of gate dielectric could be observed, as non-linear dependence was seen for$1/C^2$ on the applied gate voltage (V) (Fig 5.4). It could be due to stiochiometric changes occurring in the films during the annealing. After 500°C annealing, 0.7V of hysteresis is observed

which reduced to 0.2V for films annealed at 550°C, shown in Fig. 5.5. This is comparable to the hysteresis obtained in HfO_2 films deposited by other techniques such as atomic layer deposition [68] and reactive atomic beam deposition [83] with no surface treatment.

This significant reduction in hysteresis in our case shows an improvement in gate dielectric but at the same time a reduction in accumulation capacitance is also observed at 550°C annealing as compared to 500°C annealing. Since GeO_2 had been detected by XRD analysis, it is possible that during high temperature annealing GeO_2 interacted with HfO_2 and formed an interfacial layer of hafnium germinate [70]. XPS results also show that dielectric film is combination of HfO_2 and GeO_2. The dielectric constant of good GeO_2 is ~3, implying that a significant interfacial layer of GeO_2 will have much lower capacitance in comparison to HfO_2 film. This low capacitance in series with high capacitance of HfO_2 film will bring down effective accumulation capacitance of the gate stack. As EOT has been calculated from the accumulation capacitance of total gate stack, it will result in higher EOT. As EOT further increased to 10.5nm with 550°C annealing it confirms the interaction of interfacial layer with the gate dielectric. After 500°C annealing, the flatband voltage (V_{FB}) shift observed in these devices was 0.36V, which further shifted to 1.23V after 550°C annealing. This positive shift in V_{FB} indicates the induction of negative charge in the film at high temperature annealing.

Capacitance-voltage curves for devices with 10nm as deposited HfO_2 films showed a rather large hysteresis of 2.3V and an EOT of 6.6nm as shown in Fig. 5.6. After annealing the films at 500°C, a small decrease in hysteresis (2.1V) was observed but EOT was increased to 7.5nm. Annealing at 550°C reduced the hysteresis significantly to 0.9V but increased the EOT further to 9.3nm. This reduction in hysteresis indicates the

improvement in gate dielectric characteristics but increase in EOT indicates formation of thicker interfacial layer with increase in annealing temperature. Chen *et al* [83] observed the identical behavior where EOT was increased and hysteresis was decreased with 550°C annealing

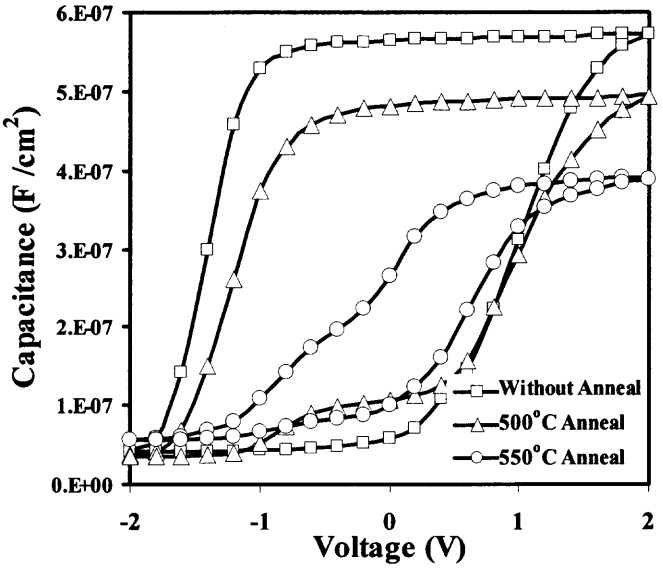

Fig. 5.6 Capacitance–Voltage characteristics of devices with 10nm HfO_2 films. Hysteresis reduced from 2.8V to 0.9V, while EOT increased from 6.6nm to 9.3nm and V_{FB} increased from –0.77Vto 0.73V after 550°C annealing.

5nm devices exhibited similar behavior was due to possible interaction of interfacial GeO_2 with the HfO_2 film at higher temperature annealing, which is confirmed by the XPS results shown in Fig. 5.3a & 5.3b. In 10nm HfO_2 film, flatband voltage shifts (ΔV_{FB}) from –0.77V before annealing to –0.35V after 500°C annealing indicates that the positive charge present in as deposited HfO_2 films is getting compensated during the annealing, hence pushing the V_{FB} towards ideal value. After 550°C annealing ΔV_{FB} further increased to 0.73V indicating the generation of more negative charge in the gate dielectric.

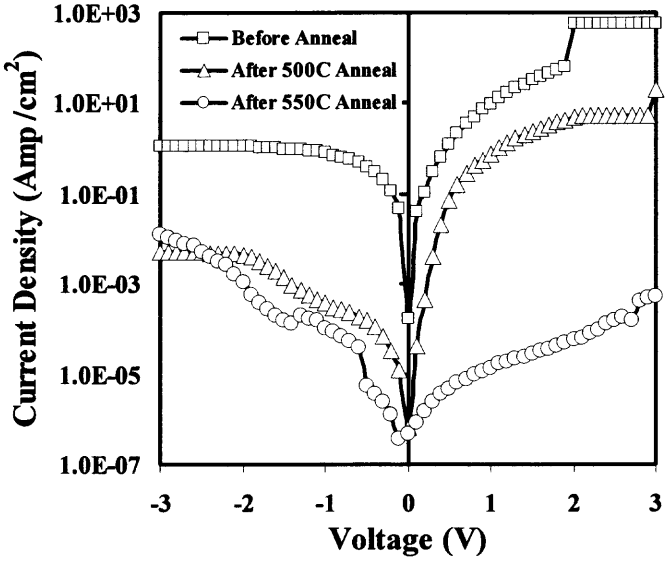

Fig. 5.7 Leakage current density of the MOS capacitors with 5nm HfO_2 films. After 550°C annealing leakage current reduced to ~10^{-5} A/cm^2.

The leakage current density in devices with 5nm HfO_2 films is shown in Fig 5.7. The leakage current density of devices with as deposited HfO_2 film is 10A/cm^2, which is slightly higher than the reported values [70][83] for as deposited HfO_2. This high leakage current indicates the presence of large density of oxide traps in the film, which resulted in trap-assisted tunneling [84]. After the annealing of these HfO_2 films at 500°C leakage current reduced to 1 A/cm^2 at 1V but annealing at 550°C resulted in further reduction of leakage current by five orders of magnitude which is lower than the leakage current obtained in HfO_2 films deposited on Ge substrate by other techniques such as MOCVD, reactive atomic beam deposition etc. [70][83]. As higher temperature (>600°C) annealing makes the HfO_2 films crystalline, 550°C anneal seems to be a good annealing temperature to bring the oxide trap density to its lowest possible inherent level for 5 nm devices but

an increase in EOT due to the interaction of interfacial layer as observed from C-V characteristics remains to be a problem.

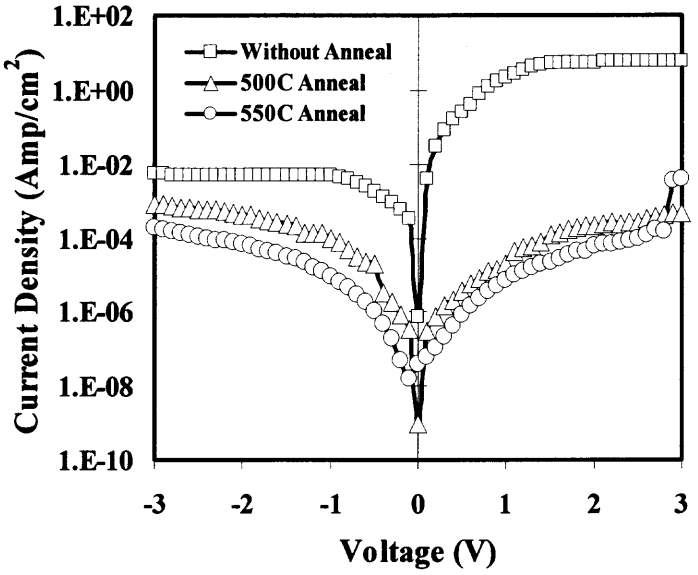

Fig. 5.8 Leakage current density of the MOS capacitors with 10nm HfO_2 films. After 550°C annealing leakage current reduced to ~10^{-5} A/cm^2.

Fig. 5.8 shows the leakage current density of MOS capacitors with 10nm HfO_2 films. The leakage current obtained for as deposited HfO_2 films was lower by two orders of magnitude as compared to the 5nm HfO_2 films, which is expected due to higher thickness of the gate dielectric. After annealing these films at 500°C and 550°C in N_2 environment leakage current reduced significantly to ~10^{-5}A/cm^2 for both annealing conditions. Even though significant improvement can be noticed between 500°C and 550°C annealing for 5 nm devices (Fig. 5.7), not much improvement was observed for the two annealing temperatures used for 10 nm devices (Fig. 5.8). Almost identical leakage

current was obtained for both 5nm and 10nm HfO_2 films after 550°C annealing, implying the higher concentration of oxide traps in 10nm HfO_2 films.

An increase in EOT was observed for both 5nm and 10nm HfO_2 films after the annealing, but for 5nm films EOT was found to be thicker than physical thickness while in case of 10nm it was lower than actual thickness of the film. As the growth of interfacial layer would be more in thinner films as compared to thicker films due to oxygen diffusion through the films, 5nm films will have thicker interfacial layer as compared as 10nm films. Therefore, this thicker interfacial layer will contribute more towards the increase in EOT than thinner interfacial layer in 10nm film. With the further growth of interfacial layer during the annealing, its fraction in total gate dielectric thickness will also increase in 5nm films than 10nm films, consequently reducing the fraction of HfO_2.

5.3 Interface Characteristics

We have investigated the effect of HfO_2/Ge interface on device performance using conductance measurements. C-V characteristics of MOS capacitors with 5nm HfO_2 film were taken at different frequencies, as shown in Fig. 5.9. The dispersion observed in accumulation region is due to the substrate series resistance, R_s, which mainly affects the high frequency C-V curve. Kinks seen in the inversion region at high frequency imply the existence of fast surface states near the valence band E_v. The difference between 10 kHz and 100 kHz C-V curves in the same region indicates the presence of slow interface states as well [85].

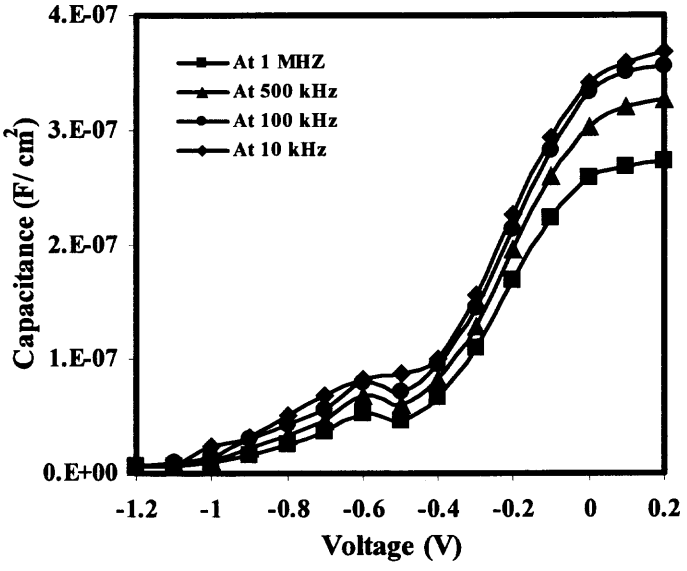

Fig. 5.9 C-V characteristics of Ge/HfO_2 (5nm)/Al MOSCAPs at different frequencies after 550°C annealing.

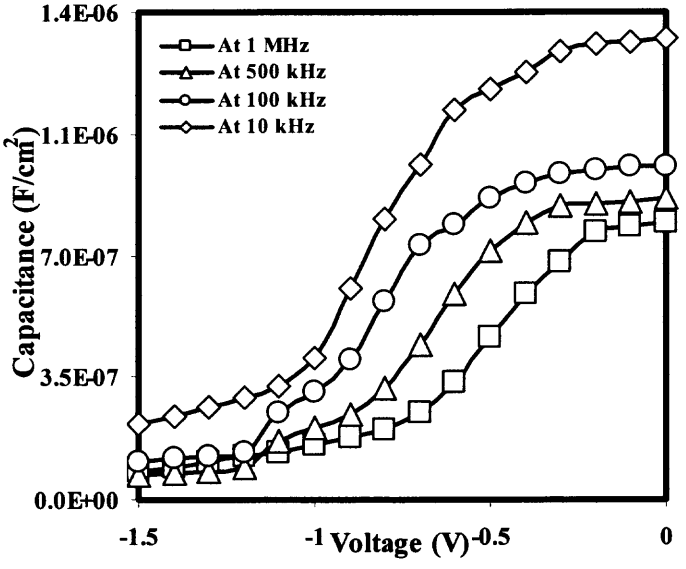

Fig. 5.10 C-V characteristics of Ge/HfO_2 (10nm)/Al MOSCAPs at different frequencies after 550°C annealing.

In contrast to C-V characteristics of 5nm HfO_2 films, significant dispersion can be observed in flatband regime for 10nm HfO_2 films, shown in Fig. 5.10. Combined with hysteresis (Fig. 5.6) and leakage current (Fig. 5.8) observed in these films, this dispersion suggests that more bulk oxide traps are present in these films. With the reduction in frequency, kinks start appearing in inversion region, indicating the presence of slow interface states near the valence band [85]. Higher level of peaks in G-V plots of 5nm films (Fig. 5.11) indicates larger concentration of interface statesas compared to 10nm films (Fig. 5.12). Though peaks observed in these films (Fig. 5.12) are broader compared to 5nm HfO_2 films (Fig. 5.11), indicating a large distribution of the energy levels of interface states in the germanium bandgap [86].

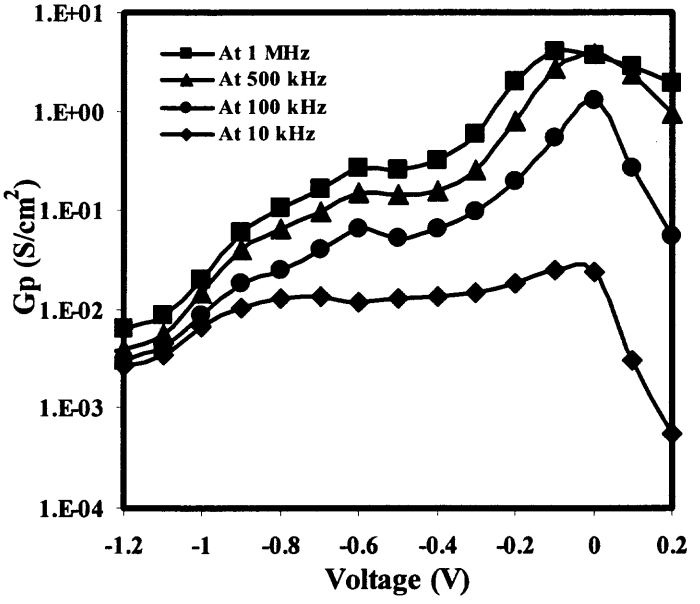

Fig. 5.11 G-V characteristics of Ge/HfO_2 (5nm)/Al MOSCAPs at different frequencies after 550°C annealing.

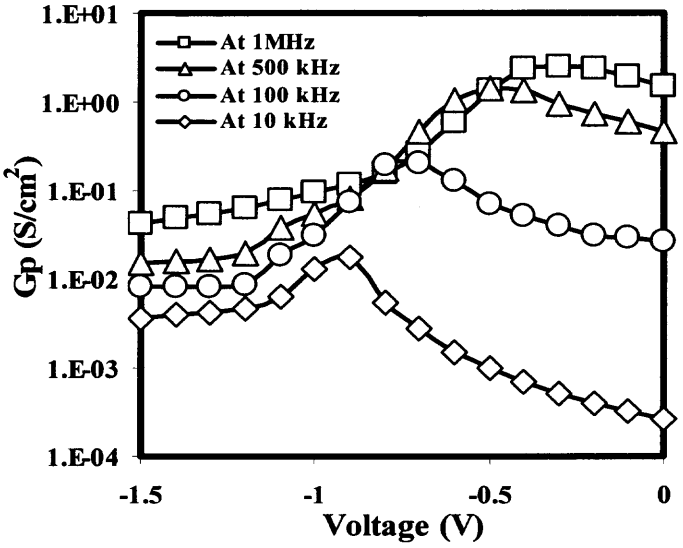

Fig. 5.12 G-V characteristics of Ge/HfO_2 (10nm) /Al MOSCAPs at different frequencies after 550°C annealing.

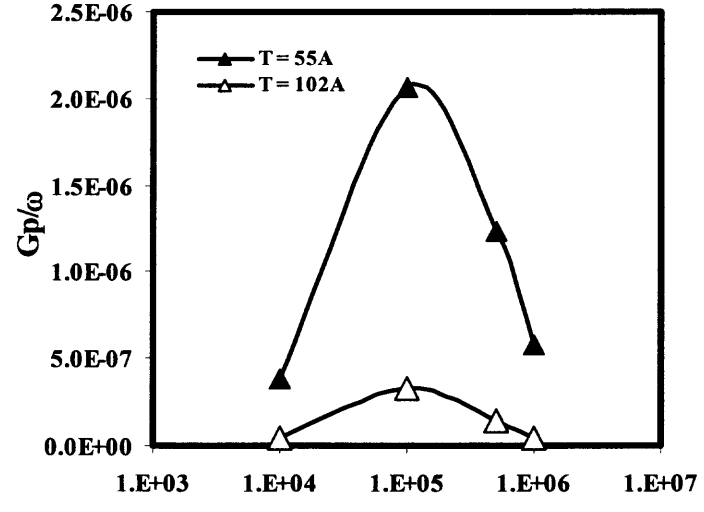

Fig. 13 Gp/ω vs. ω for both 5nm and 10nm HfO_2 films after 550°C annealing. Interface state densities (D_{it}) calculated from the peak of Gp/ω are, $3.1\times10^{13}cm^{-2}eV^{-1}$ and $5.1\times10^{12}cm^{-2}eV^{-1}$ for 5nm and 10nm HfO_2 films,

Interface state densities (D_{it}) extracted from the peak of Gp/ω vs. frequency plot (Fig. 5.13) are 3.1 $\times 10^{13}$ $cm^{-2}eV^{-1}$ and 5.1 $\times 10^{12}$ $cm^{-2}eV^{-1}$ for 5nm and 10nm HfO_2 films respectively, comparable to the D_{it} values obtained in HfO_2 films deposited by other techniques [83][69] on Ge. As interface state density is higher with a reduced bulk oxide trap concentration in 5nm HfO_2 film suggests that quality of gate dielectric film has improved after 550°C annealing in N_2 environment whereas the GeO_2/HfO_2 interface degraded. This suggests that GeO_2 type interfacial layer has increased further.

Different groups have reported similar characteristics of HfO_2 films, deposited on Ge substrate. Films deposited directly on Ge without any surface preparation show low hysteresis along with high leakage current [83] after post-deposition anneal. EOT also increased after annealing of films due to growth of interfacial layer. Surface nitridation prior to HfO_2 deposition is being suggested to reduce interface layer thickness. Ref. [70] and ref. [83] reported thinner interfacial layer with nitrided Ge surface, but a negative shift in flatband voltage indicates the presence of more positive oxide charge. Significant frequency dispersion was observed in inversion region for thinner films in comparison to thicker films [69] after surface nitridation, indicating the higher interface states being present in thinner oxides.

5.4 Summary

The physical and electrical properties of Ge MOS capacitors using thermally evaporated HfO_2 have been studied. SEM analysis showed the non-uniformity and island-like morphology of as deposited HfO_2 films on the Ge substrate but after 500°C annealing the films show smooth and uniform surface. XRD analysis showed the presence of

crystalline GeO_2. Electrical characterization showed the large hysteresis of 2.3V and high leakage current of $10A/cm^2$ at 1V in 10nm as deposited films. Hysteresis was significantly reduced to 0.9V and leakage current also reduced by six orders of magnitude after annealing of these films at 550°C in N_2 ambience. 5nm HfO_2 films showed the reduced hysteresis of 0.2V and leakage current of $\sim 10^{-5} A/cm^2$ after 550°C annealing. Interface trap density was found to be in the range of 10^{12}–10^{13} $cm^{-2}eV^{-1}$ after 550°C annealing. An increase in EOT was observed in both films at different annealing temperatures, which indicates possible interaction of interfacial layer with the gate dielectric. XPS results also confirm the interaction of GeO_2 with HfO_2 after 500°C annealing.

Since we have deposited HfO_2 directly on Ge substrate without any surface treatment, interfacial layer formation was possible for both 5nm and 10nm HfO_2 films. Reduced hysteresis and leakage current in 5nm HfO_2 film and lower interface state density and EOT in 10nm film further confirms that impact of interfacial layer is significant in 5nm film.

CHAPTER 6

CHARACTERISTICS OF E-BEAM EVAPORATED HfO_2 ON Ge SUBSTRATE

The large EOT of thermally evaporated HfO_2 on Ge substrate leave it impractical for future nano-scale CMOS devices. Therefore, another physical vapor deposition technique, e-beam evaporation with reactive atomic O beam has been used to deposit HfO_2 on Ge substrate with different cleaning process. Deposition of the HfO_2 film has been done at IBM Corporation and remaining fabrication of MOS capacitors is carried out at NJIT Microelectronics Fabrication Center. The complete process flow is given in table 3.3.

6.1 C-V Characteristic

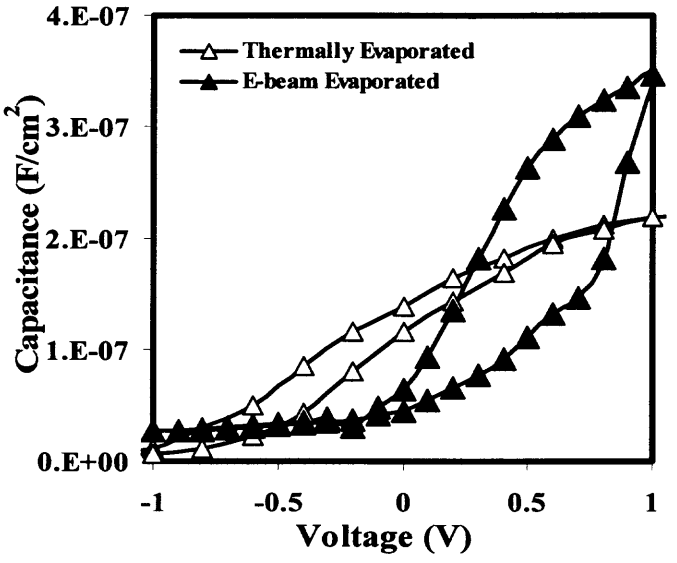

Fig. 6.1 C-V characteristics of HfO_2 deposited by thermally evaporation and e-beam evaporation with reactive atomic O beam.

Fig. 6.1 compares the C-V characteristics of HfO_2 films deposited by both techniques. The EOT decreased almost by a factor of two in e-beam evaporation for the same physical thickness of HfO_2 implying that the films deposited by e-beam evaporation demonstrates better characteristics. But hysteresis is higher in e-beam evaporated devices as compared to thermally evaporated films.

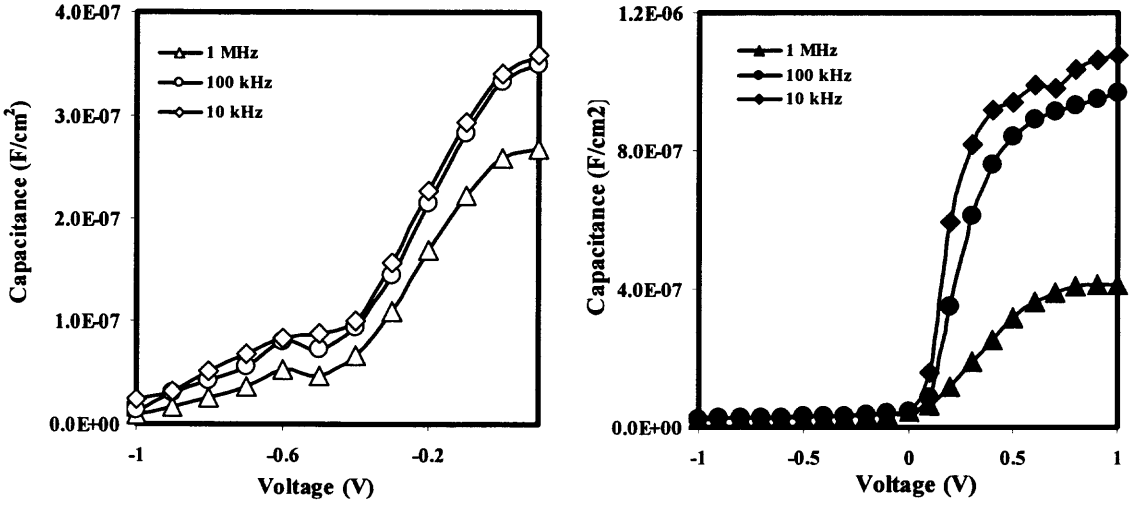

Fig. 6.2 C-V characteristics at different frequencies ranging from 1 MHz to 10 kHz for **a)** thermally evaporated HfO_2, and **b)** e-beam evaporated HfO_2 with reactive atomic O beam.

Fig. 6.2(a) and (b) shows the C-V characteristics of both the films at different frequencies. In Fig. 6.2(a), kinks seen in the inversion region at high frequency imply the existence of fast surface states near the valence band E_v. The difference between 10 kHz and 100 kHz C-V curves in the same region indicates the presence of slow interface states as well. No dispersion is visible in inversion region at any frequency in Fig. 6.2 (b) of e-beam evaporated HfO_2. However, dispersion started in weak inversion and extends in the accumulation region. It is because of slow acceptor interface trap levels near the

conduction band, E_c. They start responding with the reduction in frequency by emitting holes (capturing electrons), which results in the increase of accumulation capacitance. Similar effect is observed in Fig. 6.2(a), but its more pronounced in e-beam evaporated HfO_2 films.

Interface state density (D_{it}), extracted from the peak of Gp/ω vs. frequency plot (Fig. 6.3), is $4.55\times10^{12}cm^{-2}eV^{-1}$ for e-beam evaporated films while for thermally evaporated films is $3.1\times10^{13}cm^{-2}eV^{-1}$. It clearly shows that HfO_2 films deposited on Ge substrate by e-beam evaporation are better than thermally evaporated HfO_2.

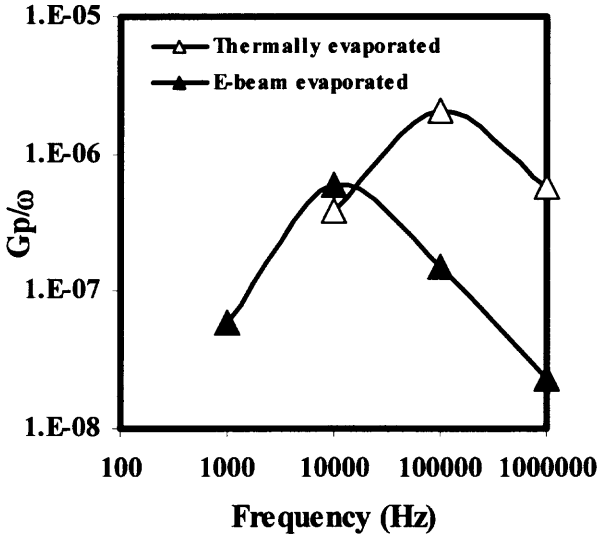

Fig. 6.3 Gp/ω vs. frequency for thermally evaporated and e-beam evaporated HfO_2. D_{it} is $4.55\times10^{12}cm^{-2}eV^{-1}$ for e-beam evaporated films while for thermally evaporated films it is $3.1\times10^{13}cm^{-2}eV^{-1}$.

6.2 Effect of Ge Surface Nitridation

Devices made by depositing HfO_2 directly on Ge show significant hysteresis or high EOT, as observed in section 6.1. This deterioration in electrical performance is mainly

due to the formation of unstable interfacial layer of GeO_2 during the HfO_2 deposition. It has been found that Ge surface treatment prior to gate dielectrics deposition is effective in improving the MOS device quality. Different kind of Ge surface passivation has been done by forming thin Ge oxynitride [68] [69], by NH_3 annealing [70] or by SiH_4 annealing [71]. Recently, it has been demonstrated that initial treatment of Ge surface by atomic N beam seems to improve the physical and electrical characteristics of MOS capacitors [83].

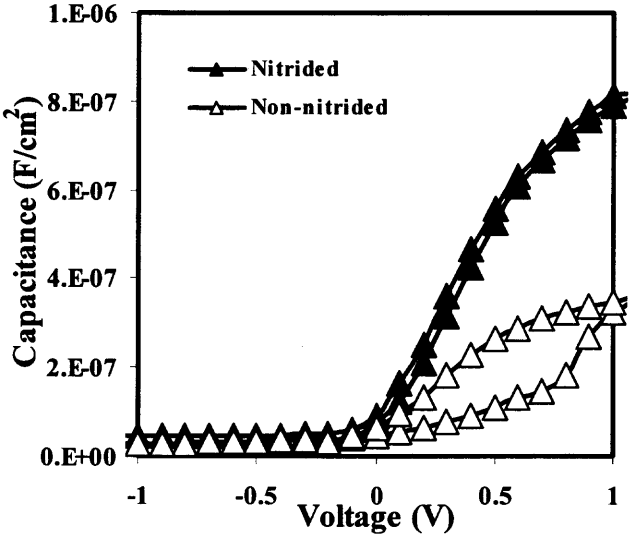

Fig. 6.4 C-V characteristics of nitrided and non-nitrided Ge/HfO_2/Al MOS capacitors. Nitrided and non-nitrided devices show hysteresis of 0.03V and 0.5V, respectively.

Fig. 6.4 shows the C-V characteristics of nitrided and non-nitrided Ge MOS capacitors at 1MHz. Significant reduction in hysteresis (0.03V) of surface nitrided capacitors imply the improvement in device performance after surface nitridation. The equivalent oxide thickness (EOT) decreased by a factor of 3 as accumulation capacitance

increased after surface nitridation. The reduction in interfacial layer after surface treatment has contributed to the increase in accumulation capacitance and possibly reduction in the hysteresis. This behavior was also observed by Chui *et al* [85] and Wu *et al* [71] for nitrogen treated interfaces.

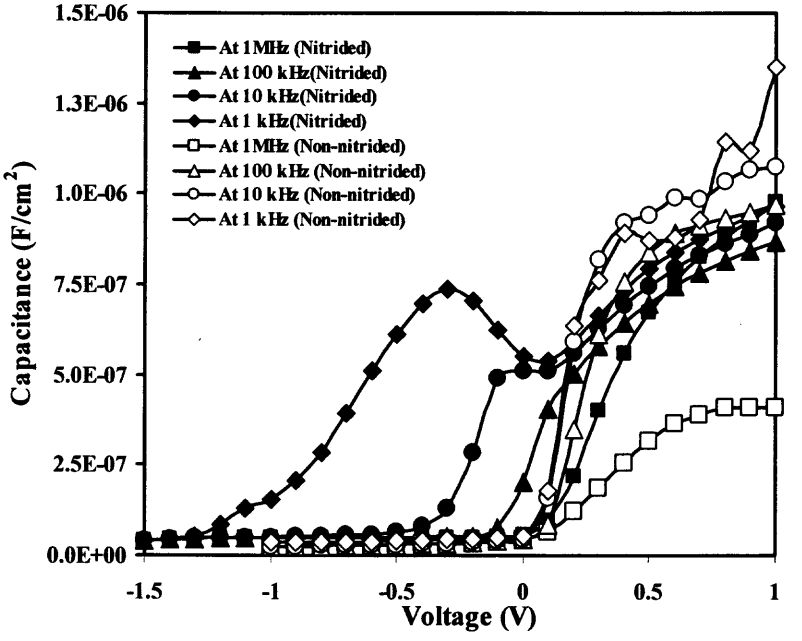

Fig. 6.5 C-V characteristics of nitrided and non-nitrided Ge/HfO_2/Al MOS capacitors at different frequencies ranging from 1kHz to 1MHz.

To analyze the effect of surface nitridation, C-V characteristics of nitrided vs. non-nitrided Ge MOS capacitors were taken at frequencies ranging from 1MHz to 1 kHz, shown in Fig. 6.5. Nitrided samples show significant dispersion in inversion region, indicating the presence of slow interface states. Dimoulas et al [69] had observed similar dispersion in inversion region on p-type substrate after Ge surface was treated with O and N beams. No dispersion was observed in the inversion region of non-nitrided devices. It

is possible that surface nitridation is creating new slow interface traps deep in the bandgap that were non-existent in non-nitrided samples. On the other hand, non-nitrided samples showed dispersion in accumulation region as a function of frequency that is mainly because of series resistance effect. This behavior is observed when conductance of gate oxide becomes comparable with the conductance associated with series resistance. Absence of this effect in nitrided devices suggests an improvement in gate dielectric, which was also observed in hysteresis measurements and EOT estimation of these devices (Fig. 6.4).

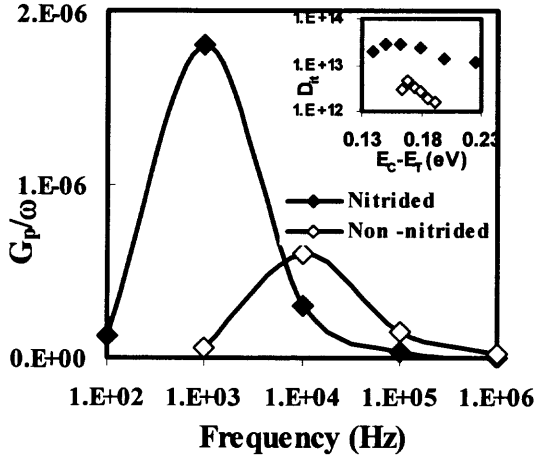

Fig. 6.6 Gp/ω vs. frequency for nitrided and non-nitrided devices. Interface state density (D_{it}) is 2.9×10^{13} $cm^{-2}eV^{-1}$ and 4.55×10^{12} $cm^{-2}eV^{-1}$ for nitrided and non-nitrided Ge MOS capacitors, respectively.

To estimate interface state density (D_{it}), G_P/ω was calculated from measured capacitance and conductance at the gate bias of –1V to 1V in the frequency range of 1MHZ to 1 kHz and then plotted as a function of frequency. Energy levels pertaining to gate biases from depletion to inversion region (as conductance method is reliable in this

region) were calculated from ideal C-V curve using oxide capacitance from experimental measurements [18]. Maximum D_{it} extracted from the peak of Gp/ω vs. frequency plot (Fig. 6.6) is 2.9×10^{13} $cm^{-2}eV^{-1}$ and 4.55×10^{12} $cm^{-2}eV^{-1}$ in nitrided and non-nitrided devices, respectively.

D_{it} in nitrided devices seems to be more widely distributed in Ge bandgap as compared to non-nitrided devices, shown in inset of Fig. 6.6. Also, interface states in nitrided devices are located deeper in Ge bandgap than non-nitrided devices. The concentration of deep interface states in nitrided devices in the bandgap is higher than that of the maximum D_{it} estimated for non-nitrided devices. This suggests the presence of slower interface traps in nitrided devices.

6.3 Low Temperature Characterization

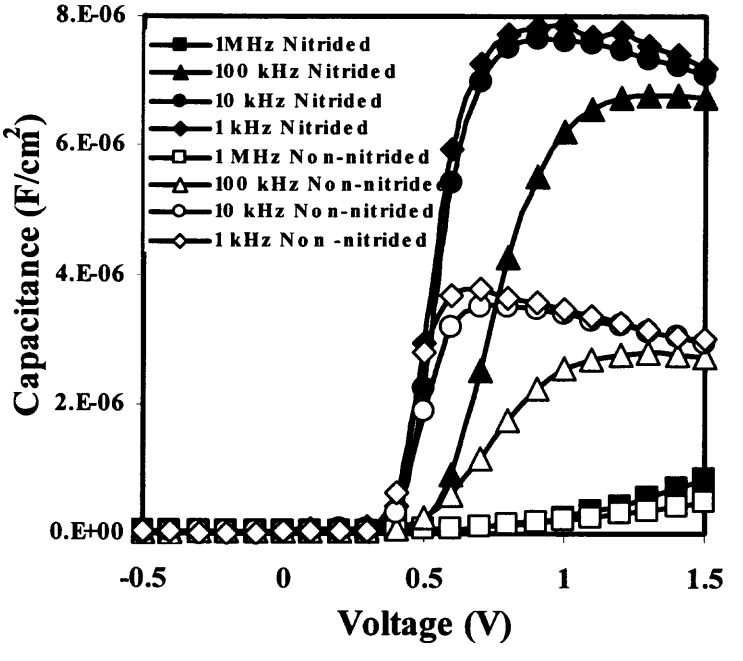

Fig. 6.7 C-V characteristics of nitrided and non-nitrided $Ge/HfO_2/Al$ MOS capacitors at different frequencies ranging from 1kHz to 1MHz at 140K.

Fig. 6.7 shows C-V characteristics of nitrided and non-nitrided devices at 140K as function of frequency. At low temperature, no dispersion is observed in inversion region of both devices. Dispersion in accumulation region can be attributed to series resistance effect, which was not visible in nitrided devices at room temperature. However, significant dispersion can be seen flatband region, which implies the dominance of bulk oxide traps at low temperature.

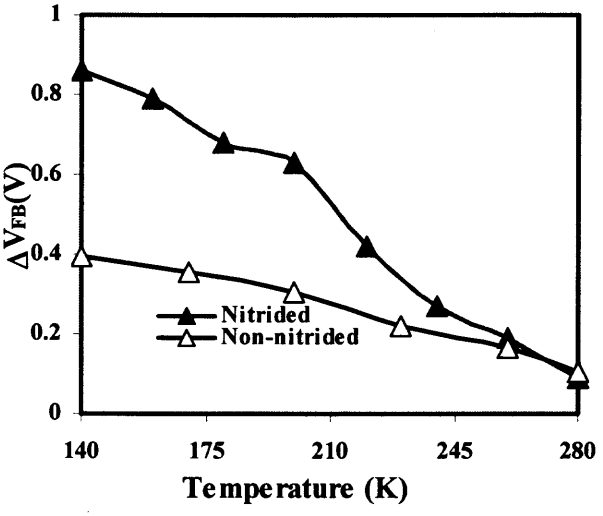

Fig. 6.8 Shift in flatband voltage, V_{FB}, as a function of temperature for nitrided and non-nitrided Ge MOS capacitors.

Recent studies have shown that HfO_2 has electrically active ionic defects [95] that traps and de-traps rapidly based on Shockley, Read, Hall theory (SRH model) [96]. However, this de-trapping process is thermally activated. Hence, detrapping decreases as temperature is lowered; this results in an increase in ΔV_{FB}. Therefore, to further investigate the nature of traps, in gate oxide as well as at interface, in nitrided and non-

nitrided MOS capacitors low temperature conductance and capacitance measurements were taken. Fig. 6.8 shows flatband voltage shift (ΔV_{FB}) with respect to room temperature after considering the appropriate flatband temperature correction. Positive increase in ΔV_{FB} with the reduction in temperature shows electron trapping in both nitrided and non-nitrided samples. Though almost linear dependence can be seen in both devices, nitrided devices have steeper slope in comparison to non-nitrided devices. This suggests bulk trapping in nitrided devices increases rapidly as temperature reduces, compared to non-nitrided devices. Nitrogen, therefore, is believed to be contributing to the additional defects in dielectric that are being revealed at low temperature.

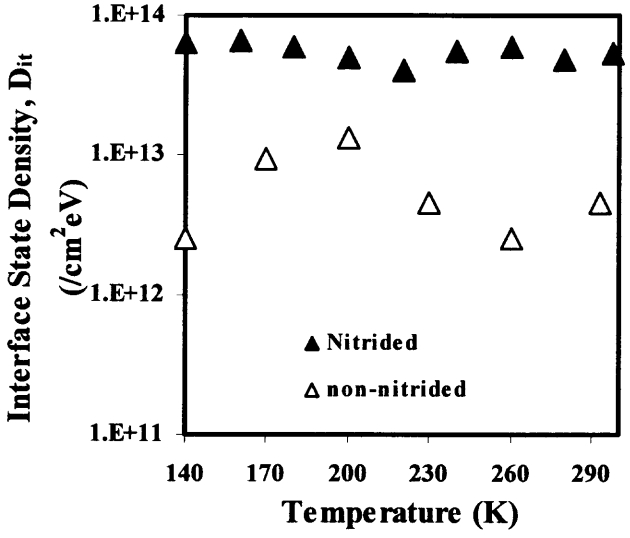

Fig. 6.9 Interface state density (D_{it}) as a function of temperature for both nitrided and non-nitrided samples.

In non-nitrided devices, there is a difference of almost one order of magnitude in D_{it} at room temperature and 200K as shown in Fig. 6.9. Since both interface traps and bulk oxide traps contribute to charge centroid [88], absence of any contribution of

interface traps on ΔV_{FB} implies that bulk oxide traps are dominant. No considerable variation was observed in interface state density (D_{it}) of nitrided devices as a function of temperature. This is in contrast to ΔV_{FB} where significant electron trapping was observed as a function of temperature. It shows that even though D_{it} is higher in nitrided samples, interface trap distribution is rather stable with temperature. On the other hand, the interface trap distribution fluctuates for non-nitrided devices. It is well known that HfO_2 has active intrinsic defects. Diffusion of nitrogen from interface into bulk oxide seems to modify the nature of these intrinsic defects in nitrided devices.

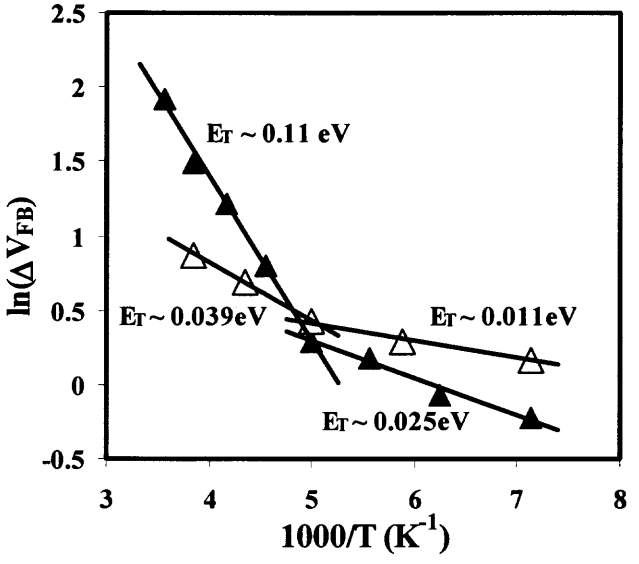

Fig. 6.10 Ionization energy levels (E_T) calculated from ΔV_{FB} with respect to 1000/K. E_T for nitrided devices is 110meV and 25meV (solid triangles) while non-nitrided it's 39meV and 11 meV (empty triangles).

As the flatband voltage varies with temperature due to change in traps behavior, trap activation energies (E_T) were estimated for both nitrided and non-nitrided devices [97]. As shown in Fig. 6.10, the estimated E_Ts from slope of the curve for nitrided sample

are ~ 110meV and 25meV, while for non-nitrided samples they are 39meV and 11meV from the Ge conduction band edge. The observed shallow traps in both devices are rather similar except the observed deeper trap energy level in nitrided devices. Presence of this additional trap energy level confirms that presence of nitrogen is indeed responsible for new trap levels in bulk oxide.

6.4 Charge Trapping Under Constant Voltage Stress

Charge trapping in the oxide has been used to monitor the degradation of the oxide. To better understand the trapped charge characteristics, constant voltage stress was done. Fig. 6.11 shows the schematic band diagrams for gate and substrate injection using conduction band offset, valence band offset, and aluminum work functions given in Table 6.1. As it can be seen in Fig. 6.11, two different tunneling distances are obtained for different polarity. For substrate injection injected current will be limited by interfacial layer at higher voltages, as tunneling will occur from single layer instead of double dielectric layers. For gate injection, tunneling through the bulk oxide would be more dominant.

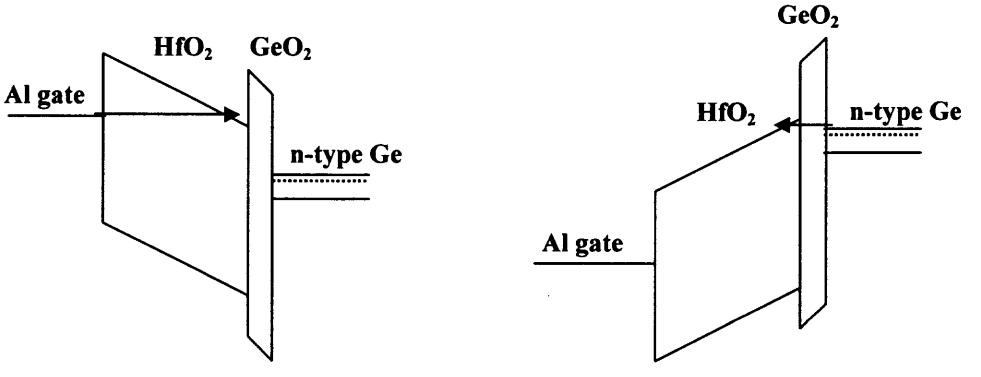

Fig. 6.11 Schematic band diagrams of a) gate injection, b) substrate injection using numbers given in Table 6.1.

	GeO_2	HfO_2	Ge	Al
E_{CB} (eV)	**1.32-4.99**	**2.0**		
E_{VB} (eV)	**2.0**	**3.0**		
ϕ_{ms} (eV)			**4.0**	**4.1**

Table 6.1 Conduction and valence band offset of GeO_2 and HfO_2 with respect to Ge [94] and work function values for Ge and Al.

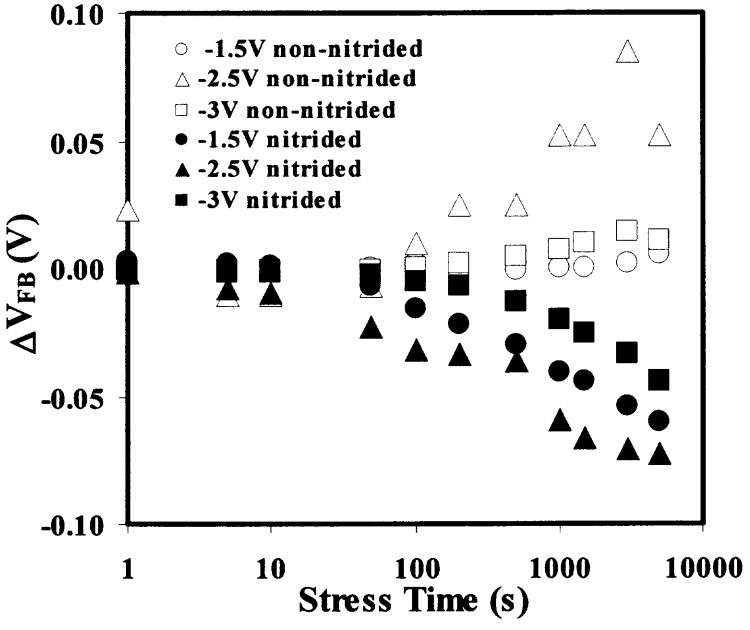

Fig. 6.12 Shift in flatband voltage, ΔV_{FB}, after constant voltage stress, under gate injection, of various time periods, for nitrided and non-nitrided Ge MOS capacitors.

Fig. 6.12 shows positive shift in V_{FB} as a function of stress time in non-nitrided devices, implying electron trapping. It is consistent with different gate dielectric on silicon substrate [89] for stress voltages less than -3V. Interestingly, nitrided devices

show totally opposite trend with negative shift in V_{FB} implying hole trapping as a function of stress time. It is probably due to the nature of defects introduced by surface nitridation in bulk oxide as observed in low temperature measurements. On the other hand, possible stress-induced N+ ion diffusion in the gate dielectric from interface can explain the opposite trend.

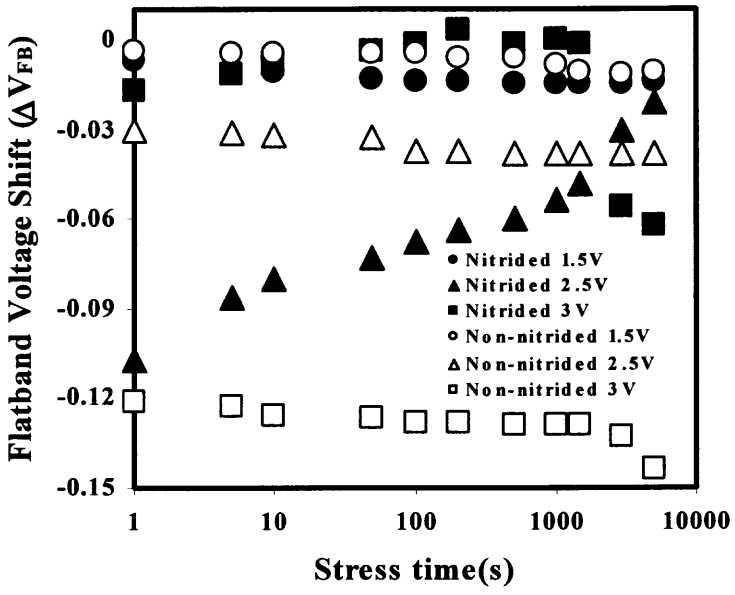

Fig. 6.13 Shift in flatband voltage, ΔV_{FB}, after constant voltage stress, under substrate injection, of various time periods, for nitrided and non-nitrided Ge MOS capacitors.

To further clarify the mechanism the devices were subjected to substrate injection as shown in Fig. 6.13. In nitrided devices it was observed that initially V_{FB} shifts negatively but at higher stress level (i.e. at 2.5 and 3V) as the stress time increases, it starts shifting positively thus reducing the shift in V_{FB}. While in non-nitrided case negative shift keeps on increasing with stress voltage and time. Therefore, it can be concluded that possible diffusion of N+ ions in the dielectric could be the main reason of

opposite flatband voltage shift observed during gate injection. However, Maximum shift in ΔV_{FB} at –2.5V, in comparison to –3V, of both nitrided and non-nitrided devices imply that two different trapping mechanisms may be taking place at the same time. Though mixed degradation in HfO_2 has been reported earlier [90][95], it still requires further analysis to clearly differentiate between these two types of trapping mechanisms.

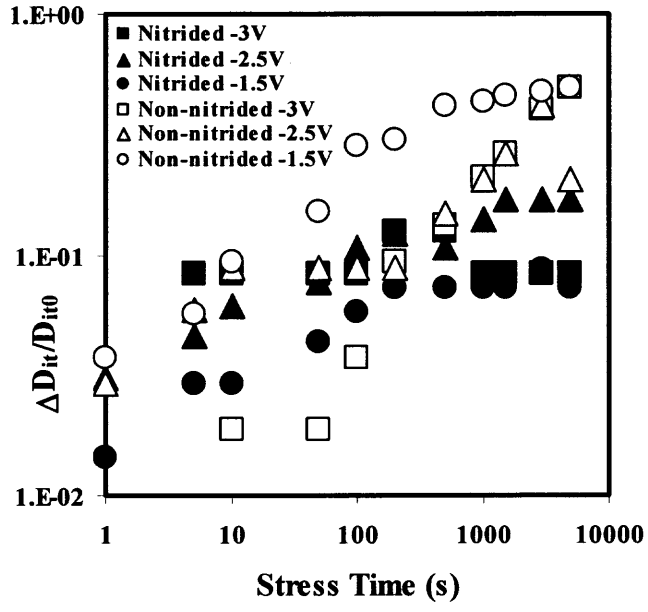

Fig. 6.14 Increase in interface state density (D_{it}), after stress under gate injection for various time periods, for both nitrided and non-nitrided Ge MOS capacitors.

Stress induced D_{it} under gate injection in non-nitrided devices increased by almost one order of magnitude while in nitrided devices there is minimal increase in D_{it}., shown in Fig. 6.14. During substrate injection at 1.5V both nitrided and non-nitrided devices showed little increase in D_{it}, shown in Fig. 6. 15. But at higher stress D_{it} increase in non-nitrided devices was more than one order of magnitude than n-nitrided devices, similar to gate injection. This implies that surface nitridation help in stabilizing the

interface but create defects in bulk oxide, observed from the shift in flatband voltage. Another factor could be that D_{it} is already higher in nitrided devices, therefore effect of charge injection may not be visible.

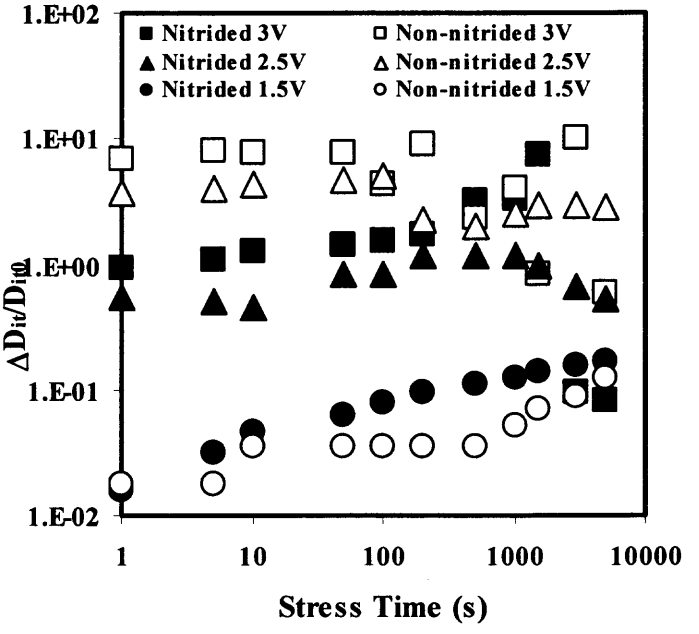

Fig. 6.15 Increase in interface state density (D_{it}), after stress under substrate injection for various time periods, for both nitrided and non-nitrided Ge MOS capacitors.

Fig. 6.16(a) and (b) shows the transient-current characteristics of both nitrided and non-nitrided devices as a function of stress time. Almost constant increase in current with stress time shows trap assisted tunneling being taking place in non-nitrided devices. While in nitrided devices, current is almost constant at –1.5V implying hole trapping, also seen in flatband voltage shift (Fig.6.13). At higher voltage levels, increase in current as a function of stress time suggests trap assisted tunneling as well. This also confirms the presence of two trapping mechanisms in these devices.

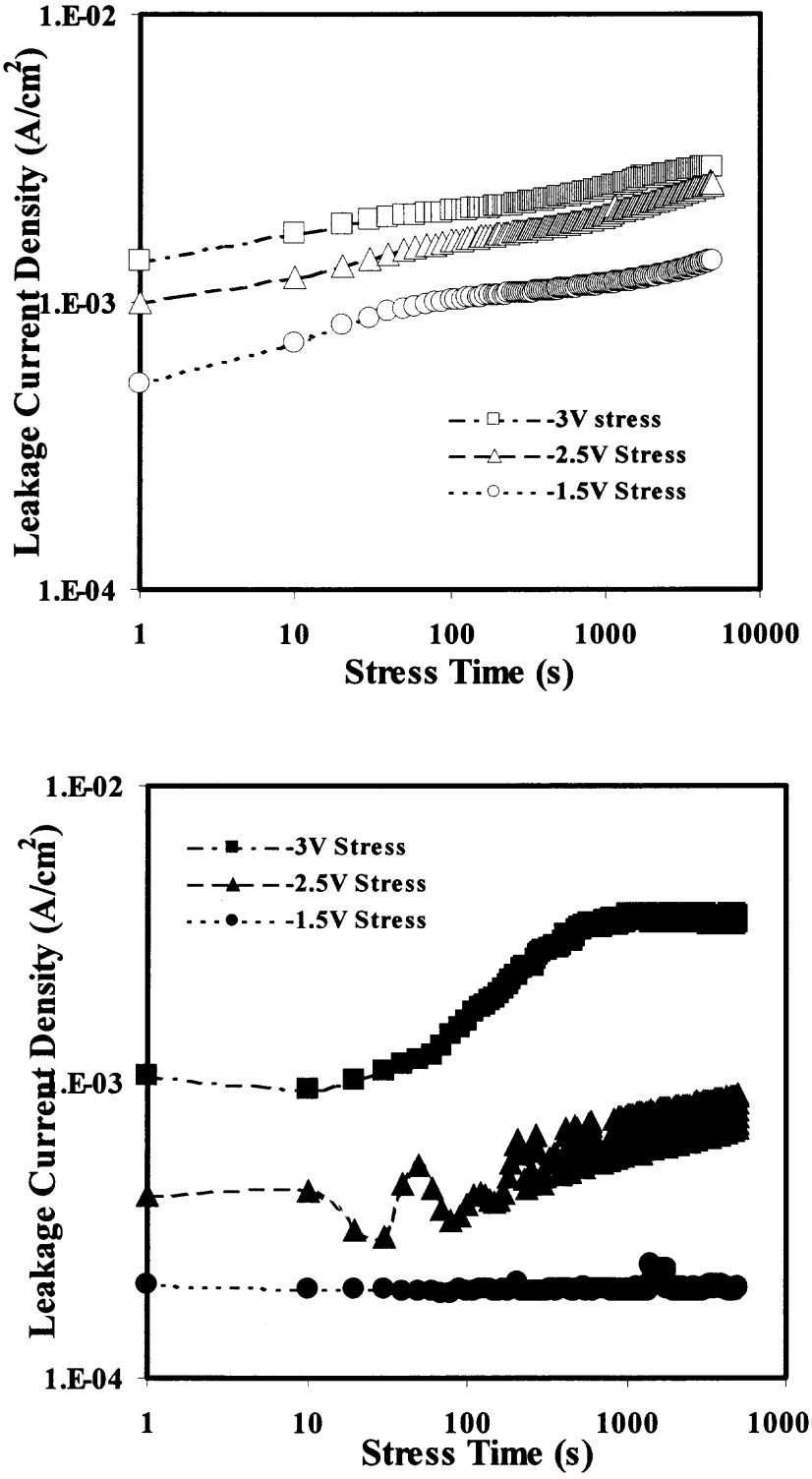

Fig. 6.16 Gate current as a function of time for **a)** non-nitrided and **b)** Ge MOS capacitors for three stress voltage of –1.5V, -2.5V and –3V.

6.5 De-trapping Phenomena

C-V and I-V measurements were taken after 3 days on the stressed devices. Fig. 17 show the V_{FB} of both nitrided and non-nitrided devices before stress, after 5000s stress and after a period of 72 hours. Non-nitrided devices show a recovery from the charge trapping damage after the relaxation period as flatband voltage almost comes back to their original value. For nitrided samples, on the other hand, flatband voltage remained slightly negative after 72 hours at –3V and –2.5V stress voltages but at –1.5V device deterioration is worse. This further confirms that relaxation was not possible due to the presence of slow traps deep in the bandgap. These traps were possibly intrinsic to nitrided devices or were created during stress due to nitrogen diffusion as discussed earlier.

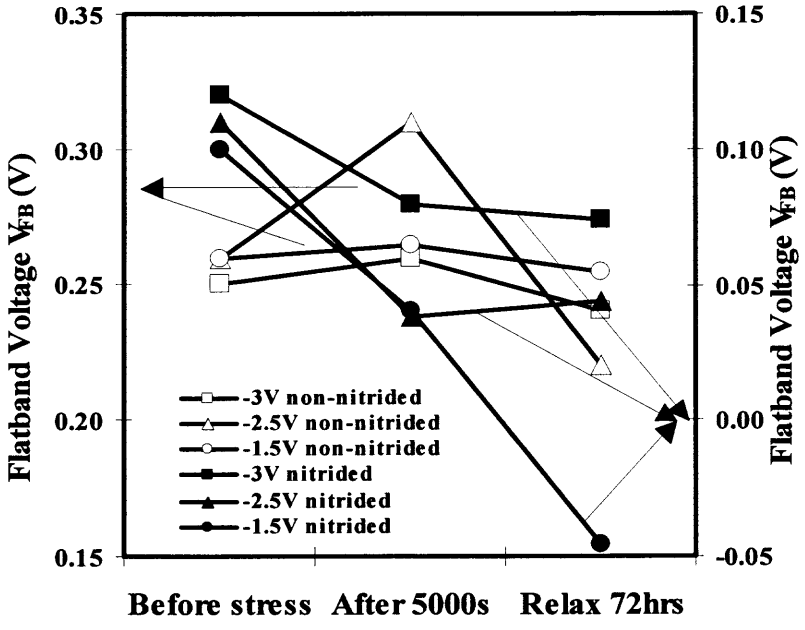

Fig. 6.17 Flatband voltage before stress, after 5000s stress and after 72 hours relaxation, for nitrided and non-nitrided Ge MOS capacitors.

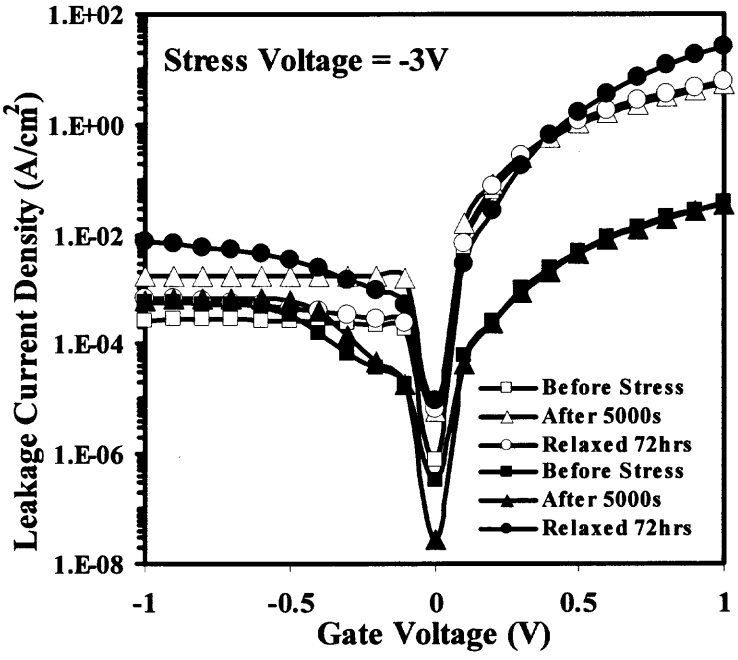

Fig. 6.18 Leakage current density before stress, after 5000s stress at –3V and after 72 hours relaxation, for nitrided and non-nitrided Ge MOS capacitors.

Leakage current in non-nitrided devices also showed recovery after the relaxation period, shown in Fig. 6.18. In nitrided devices, almost no change in leakage current was observed immediately after –3V stress. But after relaxation it increased up to 3 orders of magnitude in positive regime. It suggests that deeper trap levels, found from low frequency and low temperature measurements, trap the charge carrier immediately after stress but with time these carriers detrap and create more traps inside the bulk oxide.

6.6 Summary

E-beam evaporated HfO_2 films were characterized and compared with thermally evaporated films. Though hysteresis and flatband voltage shift was less in thermally

evaporated films but interface was superior in e-beam evaporated films. This improvement in interface is attributed to different cleaning process employed in e-beam evaporation. Ge surface treatment with atomic N beam improved hysteresis and EOT but introduced more interface states in these devices. $Ge/HfO_2/Al$ MOS capacitors with nitrided and non-nitrided Ge surface were also characterized using low temperature measurements with temperature ranging from 140k to 300K. Electron trapping was found to be dominant in both nitrided and non-nitrided devices as temperature was decreased from 300K to 140K. The activation energies of trap levels responsible for electron trapping in nitrided devices are estimated to be ~110meV and ~25meV, while for non-nitrided devices are ~39meV and ~11meV. Interface state density in non-nitrided devices show variation of one order of magnitude with respect to temperature but nitrided device does not show major fluctuations in D_{it}. Though electron trapping is dominant in non-nitrided devices and hole trapping in nitrided devices, both devices shows mixed degradation at higher stress voltages. Non-nitrided seem to recover after relaxation but slow deterioration seems to be taking place in nitrided devices with time.

CHAPTER 7

CONCLUSIONS AND FUTURE WORK

7.1 Conclusions

With device dimensions reaching to nano-scale in CMOS technology, electrical properties of HfO_2 are being investigated to assess its feasibility as a replacement of conventional SiO_2. Electrical performance of HfO_2 films and HfO_2/substrate interface depend on the deposition. In this research, we have investigated the electrical characteristics of HfO_2 films on two different platforms i.e. silicon and germanium substrates. The benefits of standard thermal evaporation deposition process on these two substrates and e-beam evaporation of HfO_2 on germanium were evaluated. Characteristics such as hysteresis, leakage current density, interface state density and flatband voltage shift of a MOS capacitor with HfO_2 were studied. Furthermore, the results of nitridation of HfO_2/Ge interface was evaluated for e-beam evaporated HfO_2.

For silicon substrates, the parameters such as hysteresis, leakage current density, and flatband voltage shift showed significant improvements after 450°C FGA anneal. Slight increase in interface state density was observed due to defects induced by the stress relieved during annealing. Shifts in C-V curves and turn around effect in flat band voltage shifts and interface state density were observed when measured in 290-130K temperature range indicating a variation of charge trapping characteristics of HfO_2 films with temperature.

To explore the possibility of improving mobility , we have deposited HfO_2 films on Ge substrate, as Ge offers higher mobility as compared to Si. Films deposited on Ge

substrate showed smooth and uniform surface after 500°C annealing. Significant improvement in hysteresis and leakage current was observed after 550°C annealing. Annealing increased the equivalent oxide thickness, which indicates the growth of interfacial layer at high annealing temperatures. XPS analysis confirmed that after annealing gate dielectric was composed of both HfO_2 and GeO_2. Since HfO_2 was deposited directly on Ge substrate without any surface treatment, interfacial layer formation was possible. Interface trap density was found to be high, in the range of 10^{12}–10^{13} $cm^{-2}eV^{-1}$, even after 550°C annealing.

To evaluate the performance of thermally evaporated films, properties of these films on Ge substrate were compared with another physical vapor deposition technique, e-beam evaporation. Though hysteresis and flatband voltage shift is better in thermally evaporated films HfO_2/Ge, interface was found to be superior in e-beam evaporated films. This could be attributed to different cleaning process used in e-beam evaporated films before depositing HfO_2. However, effect of interfacial layer was observed (large hysteresis and EOT) in films deposited by both techniques, indicating that Ge surface treatment is required prior to the deposition of HfO_2.

Ge/HfO_2/Al MOS capacitors with nitrided and non-nitrided Ge surface were characterized using low frequency measurements. Surface nitrided devices showed major dispersion in inversion region as compared to non-nitrided devices. Distribution of interface states in Ge bandgap showed that surface nitridation is creating new deeper interface traps. To further analyze the nature of traps in bulk oxide and interface, low temperature C-V measurements were taken with temperature ranging from 140k to 300K. Electron trapping was found to be dominant in both nitrided and non-nitrided

devices as temperature was decreased from 300K to 140K. Estimated trap activation energies also showed additional trap levels being created in bulk oxide of surface nitrided devices due to possible nitrogen diffusion during deposition process. Even though interface state density is higher in nitrided samples, interface trap distribution was rather stable with temperature.

Effect of nitridation on reliability of Ge/HfO_2/Al MOS capacitors was evaluated by applying a constant voltage stress in gate injection mode. Electron trapping was found to be dominant in non-nitrided devices under gate injection but nitrided devices show combined effect of hole and electron trapping. After relaxation, detrapping was observed as devices recovered to their original state while further device deterioration was observed in nitrided devices. From above observations, it is clear that even though nitridation reduced the hysteresis and growth of interfacial layer it introduced new defects at interface as well as in bulk oxide leading to further degradation in device performance.

In summary, this dissertation has reported the physical and electrical characteristics of thermally evaporated HfO_2 films on both Si and Ge substrates and compared with e-beam evaporated. The effect of Ge surface treatment on interface and bulk oxide was also studied in detail and provided useful information to industry and research area.

7.2 Recommendations for Future Work

It is clear from this research that thermally evaporated HfO_2 films can work with silicon substrate, but with Ge substrate e-beam evaporated films offer better interface

characteristics. However, many obstacles need to be overcome before successful integration of Ge with e-beam evaporated HfO_2 as gate dielectric in mainstream CMOS technology. Among them, first and foremost is the unstable interface Ge/HfO_2 interface. Though surface treatment by N beam prior to HfO_2 deposition reduces growth of interfacial layer but increases interface state density. Also reliability of devices is affected by surface nitridation, as surface nitridation seems to be incorporating defects in bulk oxide and at interface. Therefore, it is important to look into alternative methods for surface passivation to limit the growth of GeO_2 at the interface. Another major issue is mobility degradation observed in high-κ devices. Mobility degradation mechanisms need to be studied in detail by MOSFET characterization to achieve better mobility in nano-scale dimensions for future technologies.

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