ABSTRACT

ULTRA WIDEBAND COMMUNICATION LINK

by
Preeti Singh

Ultra-wideband communication (UWB) has been a topic of extensive research in recent years especially for its short-range communication and indoor applications. The preliminary objective of the project was to develop a description and understanding of the basic components of the communication link at microwave frequencies in order to achieve the primary objective of establishing a communication setup at a bandwidth of 2.5 GHz for testing Ultra Wideband (UWB) antennas. This was achieved with the aid of commercially available optical system which was modified for the purpose. Beginning with the generation of baseband narrow pulses with energy spanning over a broad frequency range, through multiplexing of different parallel channels carrying these pulses into a single stream, to finally capturing the received signal to understand the effect of the communication link formed; all provided basis for identifying the issues and possible solutions to establishing a reliable communication link at UWB frequency.

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by
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A Thesis
Submitted to the Faculty of
New Jersey Institute of Technology
in Partial Fulfillment of the Requirements for the Degree of
Master of Science in Telecommunications

Department of Electrical and Computer Engineering

August 2004

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ULTRA WIDEBAND COMMUNICATION LINK

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This thesis is dedicated to my Mom, my Dad, my elder Brother and my younger Brother, whose constant love and encouragement helped me throughout my education.

ACKNOWLEDGMENT

I convey my sincere thanks to my thesis advisor, Dr. Haim Grebel, whose constant guidance, helpful suggestions and reassurance helped me, carry out the thesis work satisfactorily. I would also like to thank Dr. Alex Haimovich for providing the necessary resources to carry out the work and also for being an integral part of the committee. Special thanks to Dr. Ali Abdi, for actively participating in the committee.

I want to take this opportunity to acknowledge the immense help, encouragement and support I have received from my family, my mother, my father, my elder brother and my younger brother. I am thankful to every little piece of advice and concern they have spoken over the years.

Words are inadequate to express my thanks to all my friends whose names have not been mentioned but have helped me directly or indirectly in my endeavor.

TABLE OF CONTENTS

TABLE OF CONTENTS
(Continued)

Chapter **Page**

LIST OF TABLES

LIST OF FIGURES

Figure **Page**

Figure **Page**

CHAPTER 1

INTRODUCTION

Wireless connectivity has enabled a new mobile life style filled with conveniences for mobile computing users ushering us into a new computing era. 3G wireless technologies are increasingly moving into the spotlight with telecom operators worldwide. 3G technologies such as Wideband Code Division Multiplex Access (WCDMA) and Ultra Wideband (UWB) could revolutionize communication communications. Built on open standards, WCDMA is currently the dominant 3G technology as it has tremendous potential in terms of providing wide ranging mobile multimedia features and economies of scale. Using a new spectrum with a 5MHz carrier, WCDMA provides data rates that are 50 times higher than Global System for Mobile Communication (GSM) networks. And UWB technology would enable wireless connectivity with consistent data rates for short range communication.

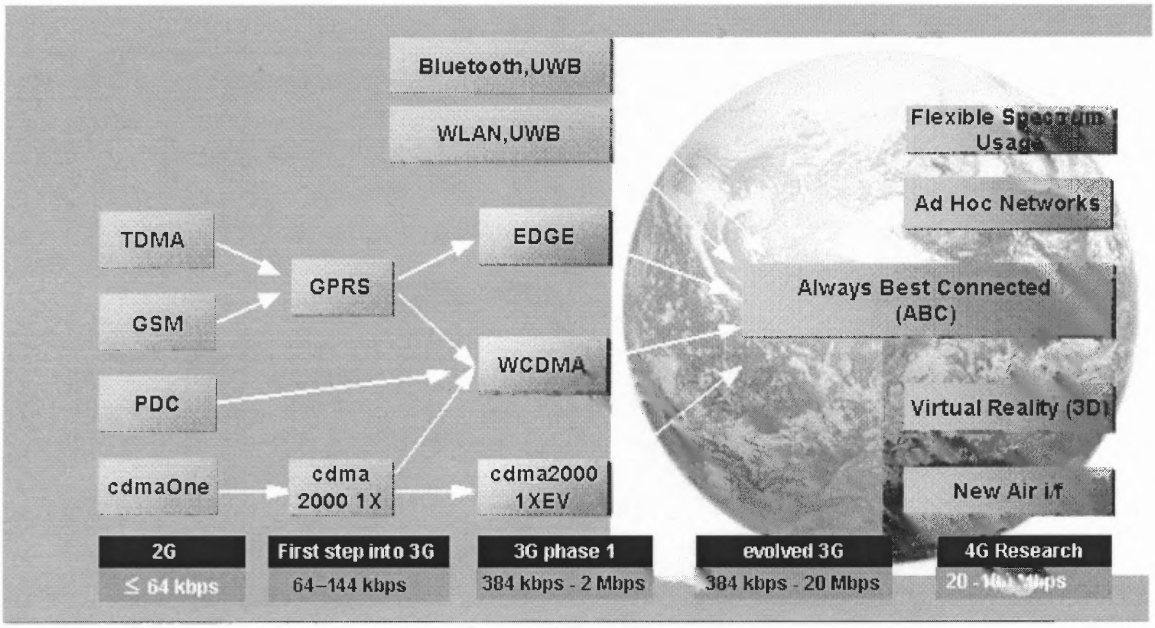

Figure 1.1 Existing and future wireless protocols.

1.1 UWB Technology and the Radio Spectrum

Ultra-wideband (UWB) transmission is a widely used technology and has recently received great attention in both academia and industry for applications in wireless communications [3, 9, 10, and 11]. A UWB system is defined as any radio system that has a 10-dB bandwidth larger than 25 percent of its center frequency, or has a 10-dB bandwidth equal to or larger than 1.5 GHz if the center frequency is greater than 6 GHz [7]. The motivation behind R&D activities carried out for UWB transmission for commercial communication applications include:

(a) Increasing demand for low-cost portable devices providing high-rate transmission capability at lower power than currently available.

(b) Lack of available frequencies, and crowding in currently assigned unlicensed frequency bands.

(c) Increasing availability of wire-line high-speed Internet access in enterprises, homes and public places.

(d) Decreasing semiconductor cost and power consumption for signal processing.

The Federal Communications Commission (FCC) of the United States declassified UWB for commercial use by reserving the frequency band between 3.1 and 10.6 GHz for indoor UWB communication systems [7]. In general, UWB technology has many benefits due to its ultra-wideband nature, which include the following:

1. High data rate - UWB technology is likely to provide high data rates in short- and medium-range (such as 20m, 50m) wireless communications [14].

2. Less path loss and better immunity to Multipath propagation - As UWB spans over a very wide frequency range (from very low to very high); it has relatively low material penetration losses. Because of its very large bandwidth, UWB provides high multipath resolution and hence better mitigation.

3. Availability of low-cost transceivers- The absence of modulation and hence a carrier promises low cost transceiver design. The techniques for generating UWB signals have existed for more than three decades [17]. Recent advances in silicon process and switching speeds make commercial low-cost UWB systems possible [8, 10 and 12].

4. Low transmit power and low interference - For a short-range operation, the average transmit power of pulses of duration of the order of one nanosecond.

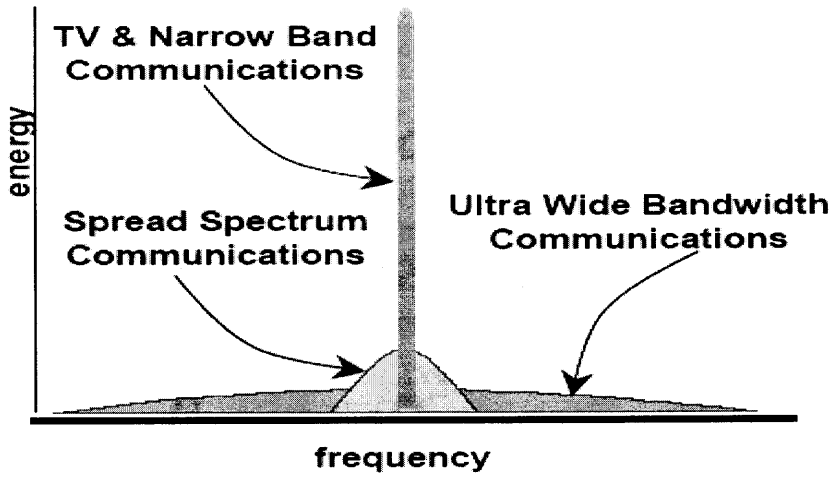

Figure 1.2 Spectrum of UWB signal compared with other standards.

1.2 IEEE 802.15.3a Standard for Wireless Personal Area Networks

Ultra Wideband (UWB) wireless networks are in their rudimentary stage, but are poised to become a valuable component of consumer electronics and computer equipment. The IEEE 802.15.3a task group is currently developing a UWB standard that involves most of the major chip manufacturers, including Texas Instruments, Intel, Motorola, and Xtreme Spectrum. The purpose of this task group is to provide a specification for a low complexity, low cost, low-power consumption and high data rate wireless connectivity among devices within or entering the Personal Operating Space. The data rate must be high enough (greater than 110 Mbps) to satisfy a set of consumer multimedia industry

needs for WPAN (Wireless Personal Area Networks) communications. The standard also addresses the Quality of Service (QoS) capabilities required to support multimedia data types. Products compliant with this standard will complement, not compete with, products compliant with IEEE 802.11, because 802.11 is a standard for Local Area Networks (LAN), and 802.15.3a will be a standard for Personal Area Networks. The difference is similar to that in the wired world of Ethernet and USB or Firewire which provide for connectivity to the network and to peripheral devices respectively. Devices included in the definition of Personal Area Networks are those that are carried, worn, or located near the body. Specific examples of devices include those that are thought of as traditionally being networked, such as computers, Personal Digital Assistants (PDAs), Handheld Personal Computers (HPCs), and printers. Also included are other devices such as digital imaging systems, microphones, speakers, headsets, bar code readers, sensors, displays, pagers, and cellular & Personal Communications Service (PCS) phones.

The 802.15.3 protocol specification requires one of the stations to act as a coordinator; providing the basic timing to the network and managing Quality of Service (QoS) requirements. The standard also defines a portal as a logical point that integrates the WPAN to a wired or a wireless LAN. Study group 15.3a has been working for the past year with strong involvement of leading UWB companies. Most of the presentations and discussions have been around UWB technology and it is likely that a UWB design will be selected as the basis for the new standard. Strong support from Consumer Electronics companies in 15.3 will ensure the standard results in products delivered to the market. There are two modes of operation: 110 and 200Mbps, and higher bit rates, such as 480Mbps, are desirable. The desired range is 30ft for 110Mbps and can be reduced for

higher bit rates. The system must be able to operate effectively in the presence of other 802.15.3a systems and in presence of other IEEE systems such as 802.11a. It is also important that the power consumption be low, to enable wireless connectivity on battery operated portable devices.

1.3 General Organization of IEEE 802.15

IEEE 802.15 is responsible for creating a variety of WPAN standards, and is divided into four major task groups which are described in the figure below:

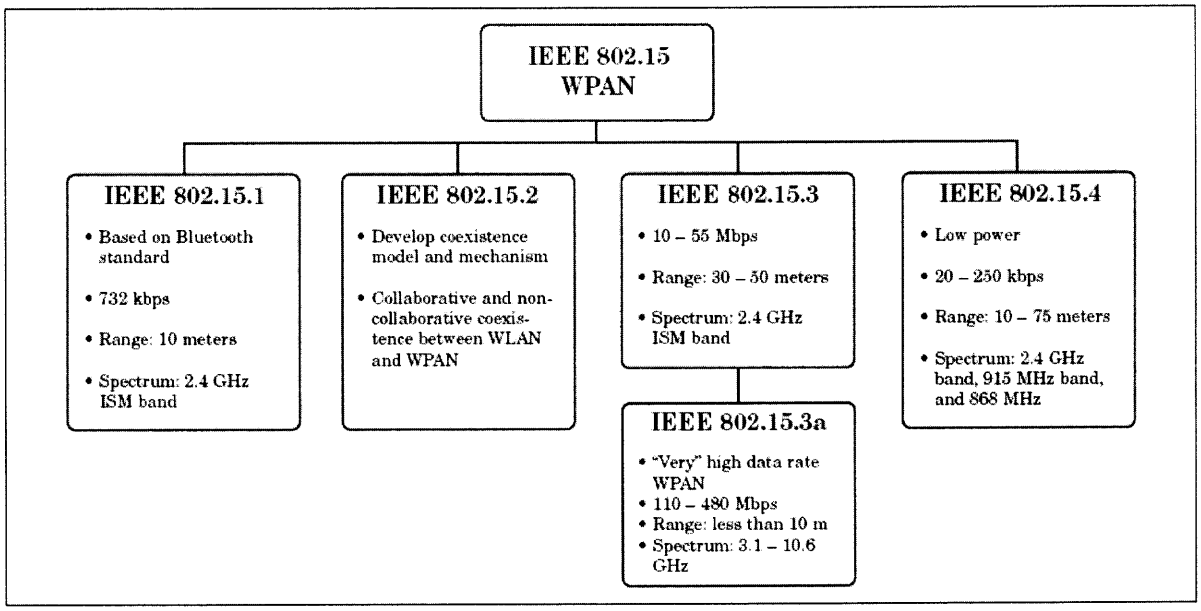

Figure 1.3 Organization of IEEE 802.15 WPAN.

The IEEE 802.15.1 task group was responsible for forging the standard based on Bluetooth [1], which uses a short-range radio link (up to a few meters) to transmit data between personal devices, forming an ad-hoc network in the unlicensed 2.4 GHz band. The 802.15.1 standard includes an adaptation of the Bluetooth Media Access Control

(MAC) and Physical (PHY) layers as well as a Logical Link Control (LLC/MAC) interface. This standard will eventually allow data transfers between a WPAN device and an 802.11 device.

The IEEE 802.15.2 is concerned with coexistence issues that arise when two wireless systems share an environment of operation [2]. The two principal goals of this standard are to quantify the effects of mutual interference between WPAN and WLAN devices, and to establish mechanisms for coexistence of WPAN and WLAN at both the MAC and PHY layer.

The IEEE 802.15.3 standard operates on five 15 MHz channels in the 2.4 GHz ISM band, though two of which interfere with IEEE 802.11b traffic [3]. The MAC layer described by this standard allows for the coordination of WPAN devices to form piconets. The MAC layer also allows for multimedia quality of service (QoS), power management, and ad-hoc networking support. The IEEE 802.15.3.a that focuses on UWB is seen as a separate task group discussed later.

The IEEE 802.15.4 task group is focused on low data rate WPAN solutions with a battery life ranging from months to several years and a very low complexity. This standard is intended to operate in unlicensed and international frequency bands. The range is 10 to 75 meters nominally, depending on the application. The spectrum allocation for this standard is as follows: 1 channel at 868 MHz, 10 channels in the 915 MHz band, and 16 channels in the 2.4 GHz band [4]. And using either MSK or BPSK (depending on the data rate), this standard transmits a spread spectrum signal. The range is 10 to 75 meters nominally, depending on the application again. The MAC layer

included in this standard supports various ad-hoc topologies and guaranteed packet delivery.

The IEEE 802.15.3a task group (also called "TG3a") for UWB focuses on low power consumption and low cost to ensure that the Wireless Personal Area Network (WPAN) standard is amenable to implementation in CMOS technology. These requirements will ensure that the high data rate physical layer drafted by 802.15.3a can be easily integrated into WPAN devices which have Medium Access Control (MAC) and network layers already implemented in CMOS technology [5]. IEEE 802.15.3a saw a new phase where in all the major companies merged to support a multiband approach which employs pulsed modulation. Then there was a new approach that employs multiple bands and uses Orthogonal Frequency Division Multiplexing (OFDM) modulation.

For instance we have a channelized UWB system preferred by Texas Instruments. There are three "Group A" bands, which are used for standard operation. Then the four "Group C" bands allocated for optional use in areas where simultaneous piconets are in close proximity. "Group B" and "Group D" bands are reserved for future expansion. . Each band uses frequency hopping orthogonal frequency division multiplexing (OFDM), which allows for each UWB band to be divided into a set of orthogonal narrowband channels. As the length of the symbol period of OFDM is increased, the modulation method can successfully reduce the effects of Inter Symbol Interference (ISI). However, this robust Multipath tolerance comes at the price of increased transceiver complexity, the need to combat Inter-Carrier Interference (ICI), and tighter linear constraint on amplifying circuit elements [6].

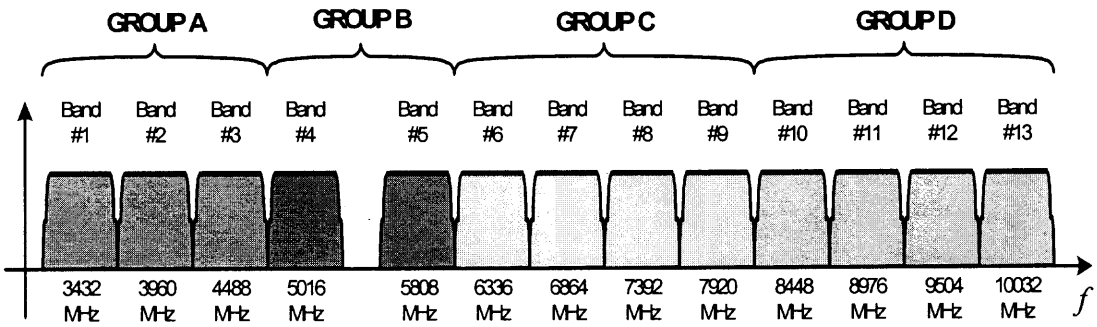

Figure 1.4 OFDM combined with multiband.

1.4 Comparison of Impulse Radio and Multibanded UWB

The two major approaches; the Impulse radio and the multibanded UWB being considered by IEEE 802.15.3a differ with regard to their allocation of UWB spectrum. The earliest approach to UWB communication was Impulse Radio (IR), here very short-duration pulses occupy a single band of several GHz. Data modulation used here is Pulse Position Modulation (PPM); and multiple users are supported using a time hopping scheme. This technology has been successfully used in radar applications. Whereas in the multibanded spectrum allocation system, UWB frequency band from 3.1-10.6 GHz is divided into several smaller bands. And to comply with FCC definitions of UWB each of these bands has to have a bandwidth greater than 500 MHz. Frequency hopping between these bands is used for multiple accesses. This approach is supported by most of the companies for its flexibility in adapting to the spectral regulation of different countries.

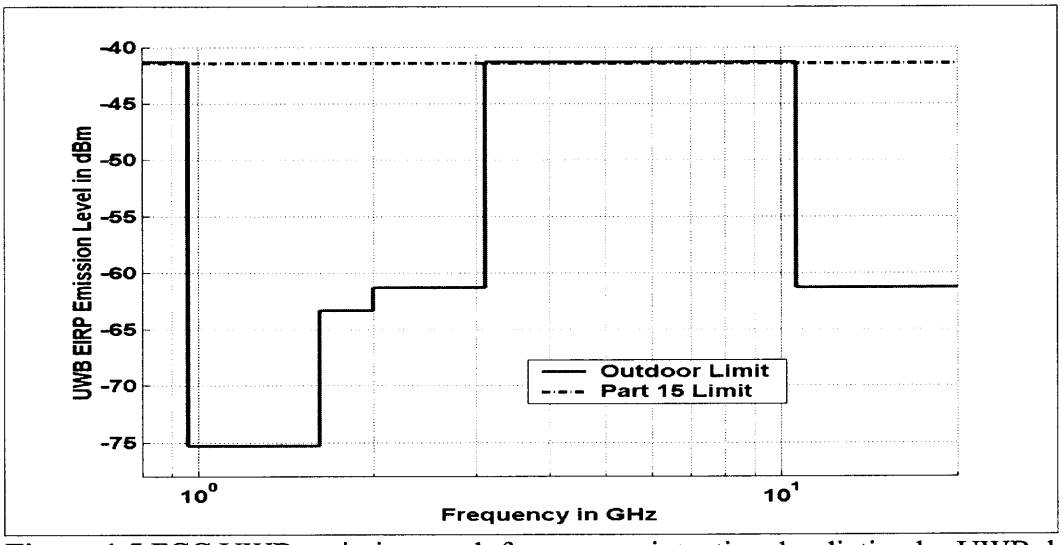

Figure 1.5 FCC UWB emission mask for average intentional radiation by UWB devices.

UWB (Ultra Wideband) has potential for interference to existing signals, especially spectral line interference, there has been a resistance to changing radio emission regulations to allow the development and use of proposed UWB waveforms. With any radio coexistence situation, the assessment task is much of concern with the scenario in which transmitters and receivers in proximity with the technical possibility of interference in the form of raising the noise floor in the receiver or more serious effects such as cancellation. Thus, the FCC issued rules. The emission restrictions established by these rules are primarily for protection of Global Positioning System (GPS) and other Government systems operating in the 690-1610 MHz band. As shown in the figure above, the band is excluded for UWB devices, while emissions in the allowable bands have a limit of -41.3dBm/MHz, equivalent to non-UWB systems. The mask also reflects the protection of various other systems in the 1610-3100 MHz band and satellite systems above 10600MHz. Other additions are restriction of handheld UWB devices to the 3100-10600 bands, determined by their 10dB bandwidths. Also there are limits on peak levels of emissions above 1GHz and on quasi-peak levels below 1GHz. The table below

summarizes the advantages, disadvantages and the applications of Ultra Wideband Communications.

The system being discussed in this report is based on Impulse Radio, as discussed above it uses a short pulse in the order of nanoseconds, and occupies a larger bandwidth. As there is no carrier involved in the transmission, it makes the design simpler.

Table 1.1 Advantages, Disadvantages and Applications of Ultra Wideband

UWB Property	Advantages	Disadvantages	Applications
Very wide fractional and absolute RF bandwidth	• High data rate communications • Potential for processing gain • Low frequencies penetrate walls.	• Potential interference to existing systems • Potential interference from existing systems	• High-rate WPAN • Low Power, stealthy communicat ion • Indoor Localization • Multiple Access
Very short pulses	• Direct resolvability of discrete Multipath components • Diversity gain	• Large number of multipaths • Long synchronizations times	Low power combined communication s and localization
Persistence of Multipath reflections	• Low fade margins • Low power	• Scatter in angle of arrival	• NLOS communicat ions indoor and on ships
Carrierless transmission	• Hardware simplicity • Small hardware	• Inapplicability of super-resolution beam forming	• Smart sensor networks

CHAPTER 2

THE COMMUNICATION SYSTEM

Communication occurs when information is transmitted or sent between an information source and the recipient of that information. For information, to be faithfully transmitted there must be a transmission medium or channel between the source and receptor (information sink). The three parts, source, channel, and sink (as shown in Figure) represent the entire information system.

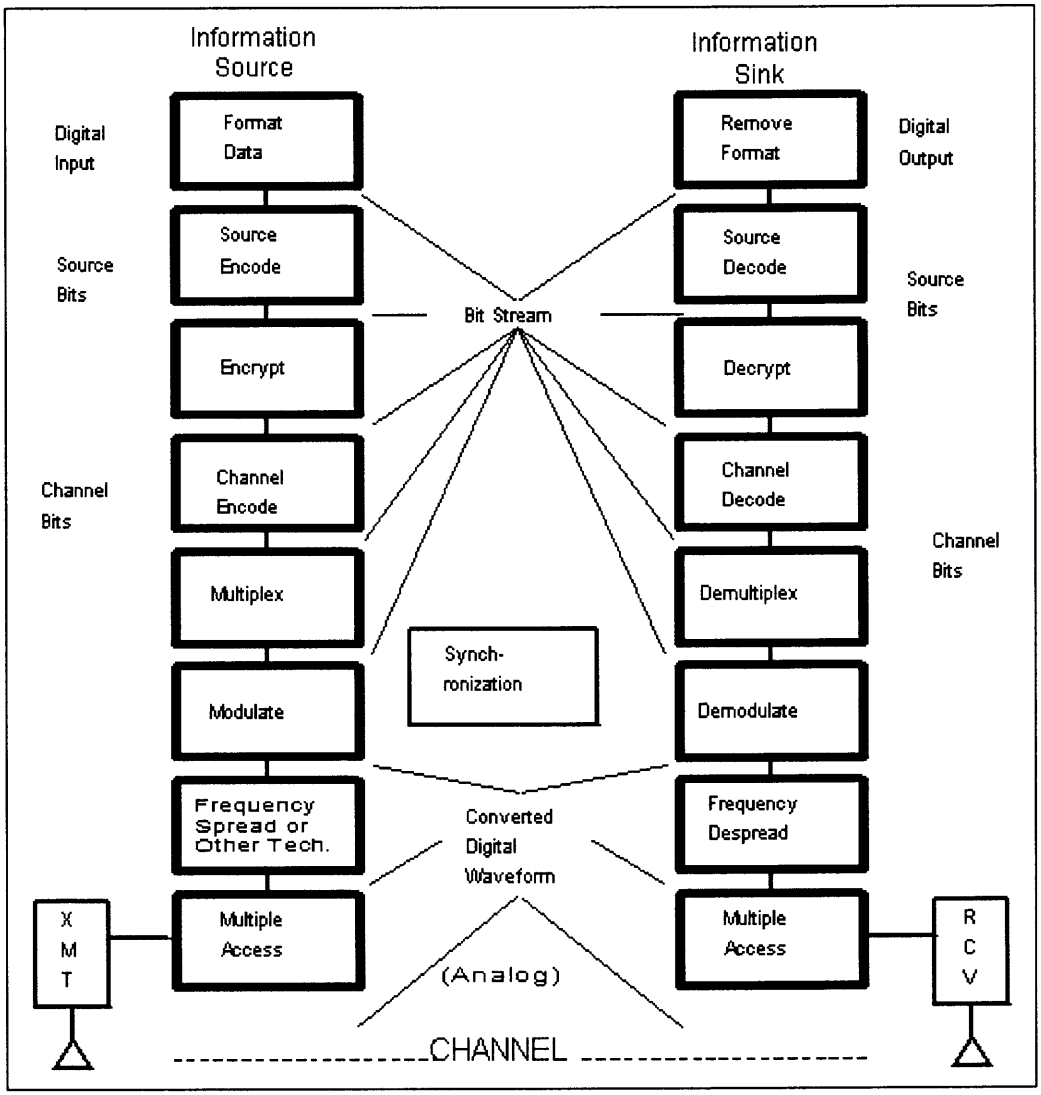

Figure 2.1 Basic communication system.

When information is put into a language understood by machines it becomes data. Data transmission occurs when data is moved electronically between two points. The resulting electronic information system can be a telemetry system, computer/digital system, or telecommunications system.

A similar basic communication system is being designed for Ultra Wideband Communication. This communication system in subject can be conveniently divided into three parts as well; Transmitter, Receiver and the RF channel.

2.1 Introduction to the System

A broader picture of our specific communication system is as shown in figure 2.2. It has the Data Generation block, followed by Maxim 3890(Evaluation kit): Serializer, Maxim 3867(Evaluation kit): Preamplifier, the amplifier and the antenna. On the receiving end it contains Maxim 3866(Evaluation kit): Post Amplifier, Maxim 3880(Evaluation kit): Deserializer, and then the Display unit to view the output; An Oscilloscope and a Spectrum Analyzer.

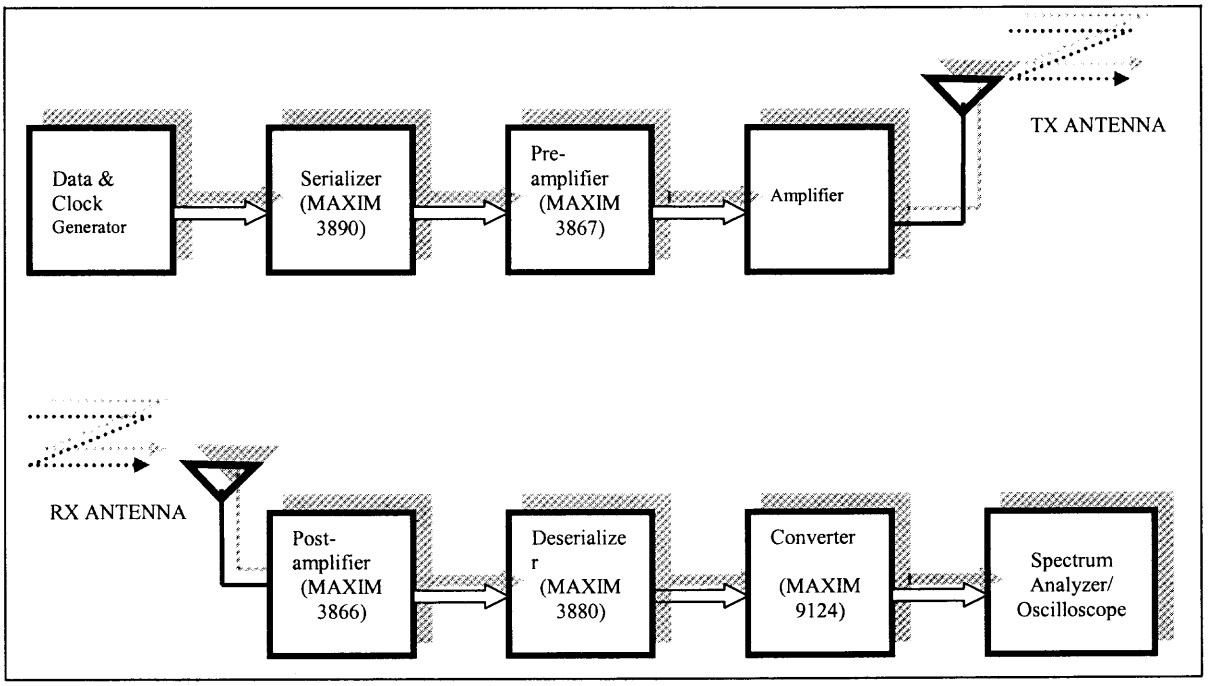

Figure 2.2 Block diagram of the system.

A Peripheral Component Interconnect (PCI) card CG400 used for data generation generates a differential pseudorandom data and clock signal at the rate of 155.52 MHz. As these Maxim boards are designed for Synchronous Optical Network (SONET) and Synchronous Digital Hierarchy (SDH) applications which are standards for optical communications. The signals; data and clock generated by PCI card are differential square pulses. These differential signals are in Low Voltage Differential Signal (LVDS) format (explained in chapter 4) as it is one of the principal requirements of the Maxim boards. LVDS; as these signals support high data rate, have low voltage swing and are immune to Electromagnetic Interference (EMI). Now we need sixteen such data channels of pseudorandom differential signals at the rate of 155.52 MHz are required for a total of 2.5GHz bandwidth, so we use power dividers to divide the single channel generated by

the PCI card into sixteen channels taking care that the power level does not fall below the acceptable level of 100mV differential voltage for each input channel.

Table 1.2 Hierarchy of SONET/SDH Data Rates

Optical Level	Electrical Level	Line Rate (Mbps)	Payload Rate (Mbps)	Overhead Rate (Mbps)	SDH Equivalent
OC-1	STS-1	51.840	50.112	1.728	-
OC-3	STS-3	155.52	150.336	5.184	STM-1
OC-12	STS-12	622.080	601.344	20.736	STM-4
OC-48	STS-48	2488.320	2405.376	82.944	STM-16
OC-192	STS-192	9953.280	9621.504	331.776	STM-64
OC-768	STS-768	39813.120	38486.016	1327.104	STM-256

Sixteen identical channels are fed to Maxim 3890 Evaluation kit; a serializer that converts 16 bit wide 155MHz parallel data to 2.5 GHz serial data. The retiming and serialization function requires a transmission clock, which must be synthesized. The clock synthesizer integrated with the serializer incorporates a Phase Lock Loop (PLL) and ensures data transmission with the lowest possible jitter. Thus, the synthesizer plays a key role in the transmitter of a transmission system. This data stream at the output of the serializer at 2.5 GHz in LVDS format is then fed to Maxim 3867 Evaluation kit. Maxim 3867 acts as a preamplifier to the system and also converts the LVDS signal to Positive Emitter Coupled Logic (PECL) output. An additional amplifier is required to boast the signal before feeding it to the antennas. Presently the antennas used are omni directional and a simple broadband antenna built in house to test the viability and reliability of the system, but the system is being designed with in house Ultra Wideband (UWB) antennas in mind.

The signal travels through air at the range of few meters and is captured by the receiver antennas. The receiver antenna then feeds the signal to the Maxim 3866 evaluation kit; this is a transimpedance amplifier that converts the single ended current to

a singe ended voltage, which is then amplified and converted to a differential signal. A DC-cancellation circuit helps in delivering differential output voltages with low pulse-width distortion over a wide range of input-current levels. Power dissipation is less than 85mW at +3.3V. The limiting amplifier delivers a certain output voltage swing whose maximum is independent of the input signal strength. There is a Loss Of Power (LOP) indicator that warns when the incoming signal falls below a user defined threshold. As a system parameter, this threshold must be adjusted externally. A comparator with the hysteresis ensures chatter-free operation for the LOP flag when the signal is close to the threshold level.

The differential signal from the output of the post amplifier is then fed to Maxim 3880 Evaluation kit; Deserializer with data and clock recovery. The main function of the clock and data recovery is to recover the clock signal from the received data stream and to regenerate the data's timing and amplitude characteristics. The Phase Lock Loop (PLL) necessary for clock recovery is fully integrated and does not require an external reference clock. It consists of a phase/frequency detector, a loop filter amplifier with external RC network, and a voltage controlled oscillator. The Phase Lock Loop (PLL) provides a Loss of Lock (LOL) signal that flags when the Phase Lock Loop (PLL) looses lock to frequency. Finally, a decision circuit supported by the recovered clock signal (from the PLL) regenerates timing and amplitude characteristics for the incoming data stream.

The differential signal at the output of each channel of the Deserializer is converted back to a single ended signal with the aid of another Maxim 9124 Evaluation

kit. The kit supports four channels at a time. The single ended signal at the rate of 155.52 MHz is monitored by an oscilloscope and Vector Signal Analyzer (VSA).

For synchronization a series of characters are send across the information channel under a timing control sequence initiated at the transmitter. This clock must be in synchronization at both ends to avoid the loss of any data bits.

In some communication channels, such as Ethernet, a clock stream is first sent over the channel in order to lock the receiver, while in radio communication system, generally a phase locked loop circuit is used to synchronize the receiver to the transmitted signal during data transmission.

CHAPTER 3

EXPERIMENTAL SETUP

The communication system is composed of commercially available boards for the purpose of optical communication and the system has been modified for wireless communication needs.

3.1 Data Generation

The toughest portion in the design of this system was the handling of data generation. Several means and components were considered for the generation of clock and data. Firstly a crystal Voltage Controlled Crystal Oscillator (VCXO) was considered. One for generating data and the other for clock at the rate of 155.52 MHz. Ecliptek EH13 VCXO, a 14 pin Dual In-line Package (DIP) integrated circuit was chosen for our purpose. Operating at 3.3V power supply it generated a square wave at 155.52 MHz with a duty cycle of 50%. But the output level of this board was incompatible for with the requirement of the single-ended signal to Low Voltage Differential Signal (LVDS) converter board to obtain a valid level of LVDS outputs: the output of the VCXO had to be converted into a LVDS before being fed into the next stage. In addition, the board used for this conversion MAX 9124 (explained later in the chapter). The component was rejected as it failed to provide signal for the necessary sixteen channels. A custom made PCI card was used that would generate LVDS data and clock signals at the rate of 155.52 MHz. This plug-n-play PCI card has female SMA connectors for output signals.

3.1.1 Peripheral Component Interconnect (PCI) Card

This CG400 arbitrary wave generator PCI card is capable of generating square waves in the megahertz frequency range, generates pseudorandom data and clock signals. Clock rates are programmable from 1Hz to 400 MHz with 0.23 Hz resolution through a graphic user interface provided. Standard output configurations being LVDS and complementary 3.3V Positive referenced Emitter Coupled Logic (PECL). It has four SMA connectors at the output, two for LVDS data and the other two for LVDS clock signals. These LVDS signals are further fed to the Maxim boards through RJ58 coaxial cables.

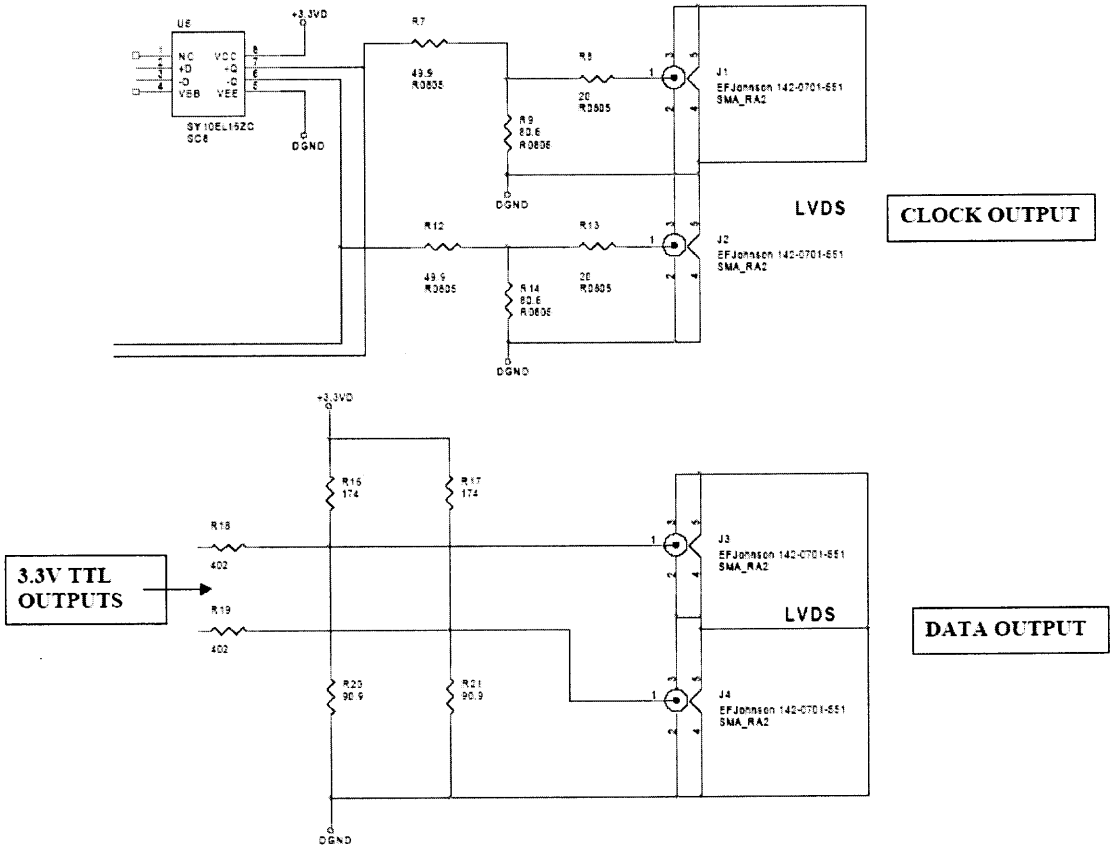

Figure 3.1 Schematic diagram of CG400 PCI card.

The values of Resistors R18 and R19 were varied to obtain the desired output data level. The value of the resistor was brought down from 400ohms to 75 ohms to boost the output signal amplitude.

3.1.2 Software Drivers

The software driver is written as a 32-bit Windows Dynamic Link Library (DLL) and is compatible with all C language compilers. A simple debug Graphic User Interface (GUI) interface is also provided so that the customers can determine if the kernel drivers are installed properly. The GUI also allows the user to set the frequency of the CG400, chirp parameters, and Input/Output controls without any programming. Source code is also available upon request.

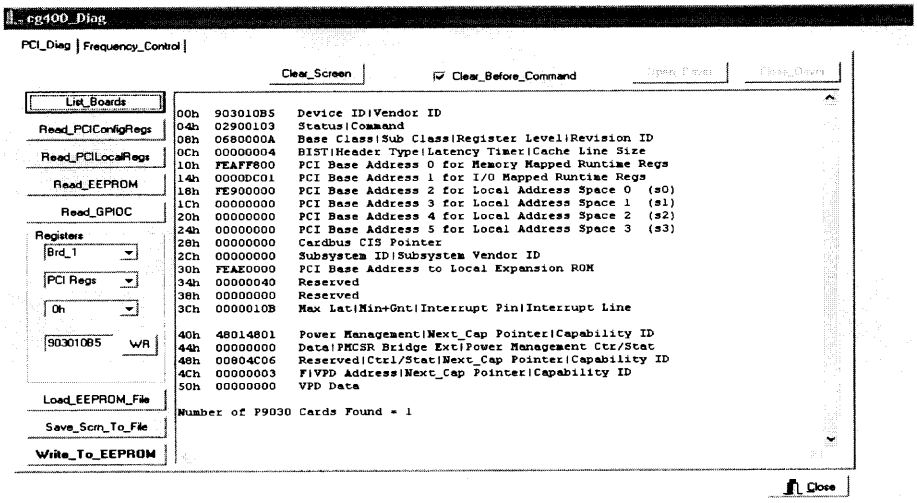

Figure 3.2 Snapshot of graphic user interface.

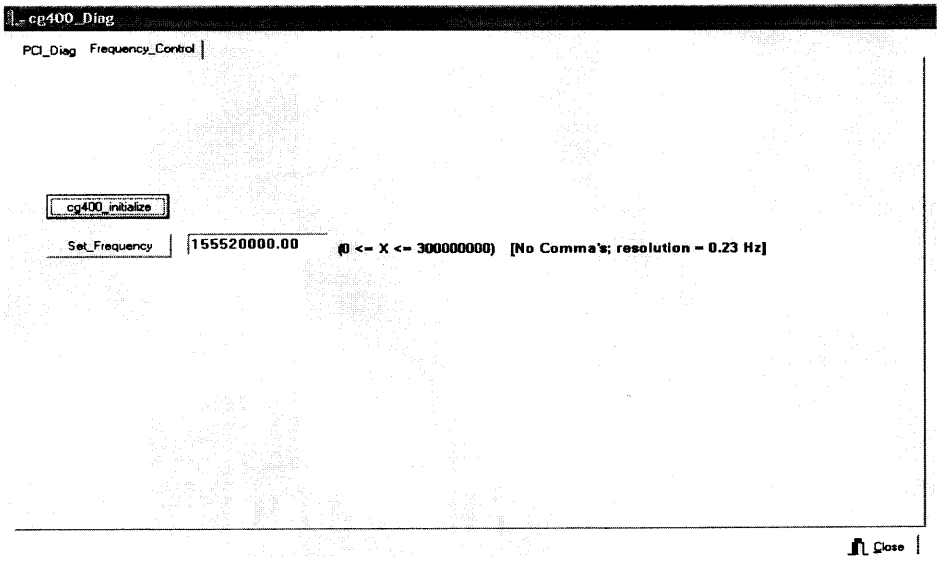

Figure 3.3 Snapshot of graphic user interface (frequency control).

The communication system requires sixteen LVDS input data channels and a single LVDS clock channel at the rate of 155.52 MHz. Thus power dividers were used to divide the pseudorandom data signal into sixteen channels taking care that the output amplitude does not fall below the acceptable limit. Two sets of power dividers were used; one for the positive differential signal and the other for the negative differential signal. Each set consisted of a 1:2 and a 1:8 power divider as shown in Figure 3.4.

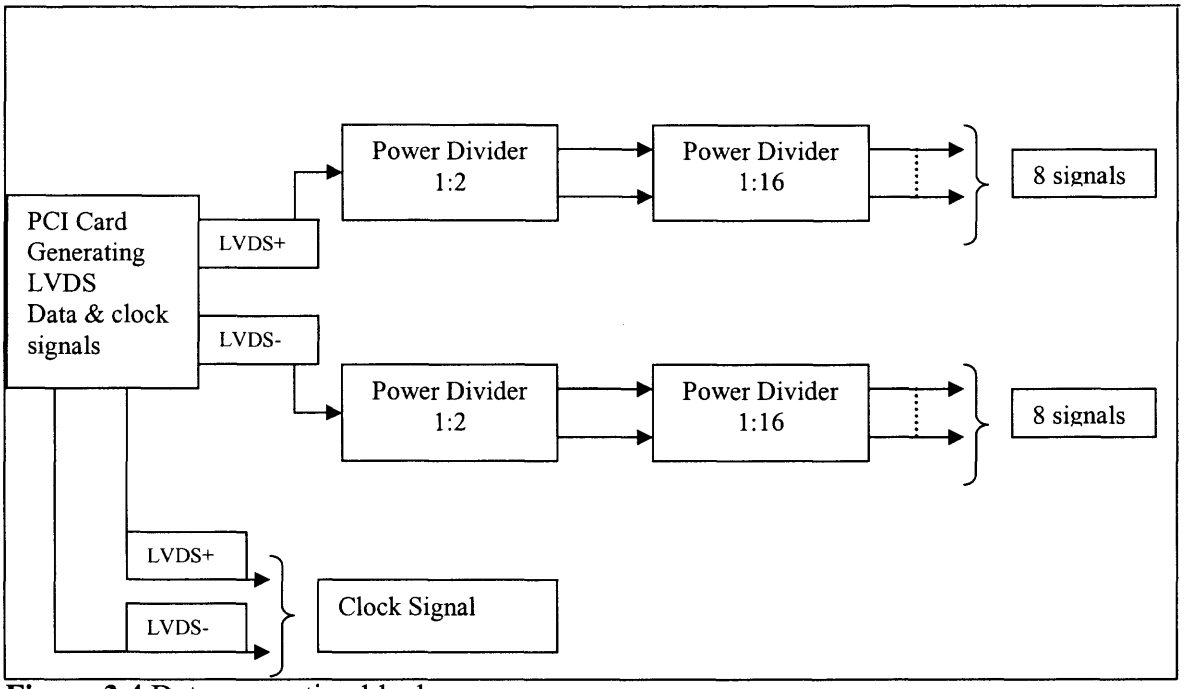

Figure 3.4 Data generation block.

3.2 Serializer

Max 3890: +3.3V, 2.5Gbps, SDH/SONET 16:1 Serializer with clock Synthesis and LVDS Inputs (referred as serializer through out the discussion)

3.2.1 Board Description

The Max 3890 serializer converts sixteen-bit-wide 155Mbps parallel data to 2.5Gbps serial data in Asynchronous Transfer Mode (ATM), Synchronous Digital Hierarchy/ Synchronous Optical Network (SDH/SONET) applications. This board operating with +3.3V supply, accepts Low-Voltage Differential Signal (LVDS) clock and data inputs for interfacing with high speed digital circuitry, and delivers Positive-referenced Emitter-Coupled Logic (PECL) serial data and clock outputs. Built into the system is a fully integrated Phase-Locked Loop (PLL) that synthesizes an internal 2.5GHz serial clock from a 155.52MHz, 77.76MHz, 51.84MHz, or 38.88MHz reference clock.

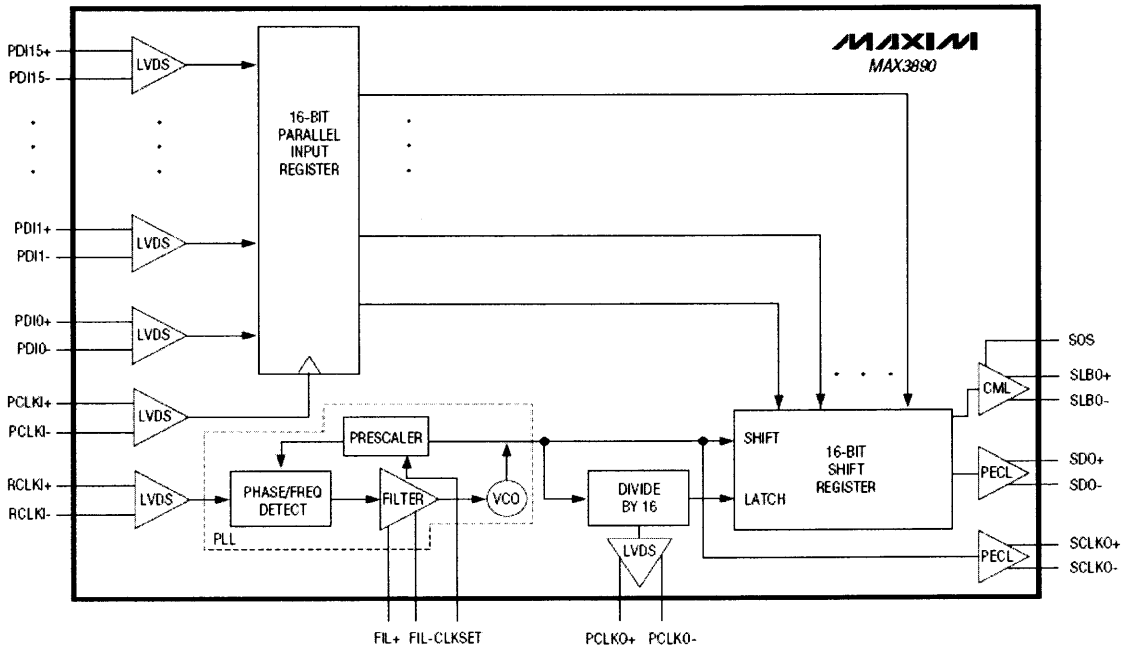

Figure 3.5 Functional block diagram of Max 3890 (Serializer).

The serializer is composed of a sixteen-bit shift register, control and timing logic, PECL output buffers, LVDS input/output buffers, and a frequency-synthesizing Phase Lock Loop (PLL; consisting of Phase/Frequency Detector, Loop Filter/Amplifier, Voltage Controlled Oscillator (VCO), and prescaler).

An internal 2.5 GHz reference clock is synthesized by the PLL to clock the output shift register. This clock is generated by locking onto the external 155.52MHz reference-clock signal (RCLK) provided to the board.

The incoming parallel data is clocked into the Max3890 on the rising transition of the parallel-clock-input signal (PCLKI). Proper operation is ensured if the parallel input register is latched within a window of time (t_{SKEW}) that is defined with respect to the parallel-clock-output signal (PCLKO). PCLKO is the synthesized 2.5Gbps internal serial-

clock signal divided by 16. The allowable PCLKO-to-PCLKI skew is 0 to +4 ns. The timing diagram below illustrates the above explanation.

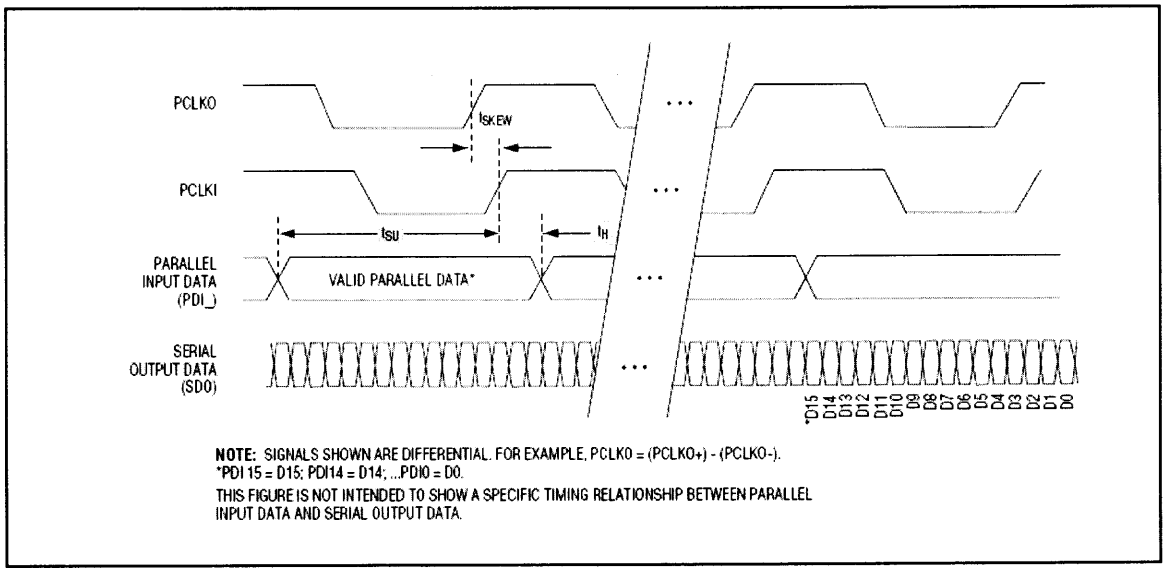

Figure 3.6 Timing Diagram.

3.2.2 System Loopback

The serializer allows us to test the system with the aid of system loopback testing. The loopback output pins (SLBO+, SLBO-) of the Max3890 are directly applied Max3880 for system diagnostics (Results in chapter 5). To enable these SLBO output, Transistor-Transistor Logic (TTL) logic high is applied to the System Loopback output select (SOS) input. There is a jumper setting on the Evaluation Kit (EV) kit to make these selections. SOS short means SLBO outputs is disabled and the board is operating on the regular mode. SOS open, means SLBO outputs enabled and the board is on the diagnostic mode.

All the data and parallel clock LVDS inputs (PDI+, PDI-, PCLK+, PCLK-, RCLK+, and RCLK-) are internally terminated with 100Ω differential input resistance. The serial PECL outputs (SDO+, SDO-, SCLKO+, SCLKO-) are 50Ω internally terminated. These outputs are then fed to the next stage that consists of MAX 3867.

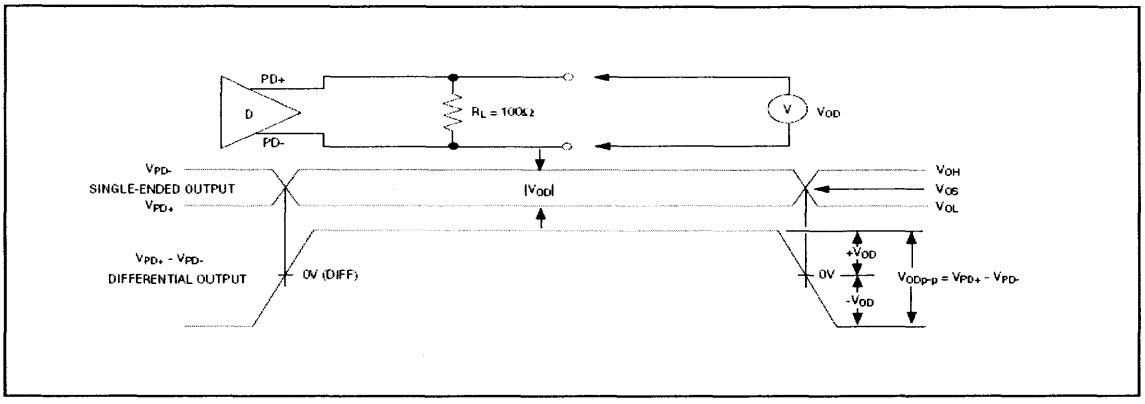

Figure 3.7 Driver output levels.

Table 1.3 Detailed Descriptions

PIN	NAME	FUNCTION
1, 17, 33, 48, 49, 63	GND	Ground
2, 5, 7, 10, 13, 14, 32, 56, 60, 64	VCC	+3.3V Supply Voltage
3	SLBO-	System Loopback Inverting Output. Enabled when SOS is high.
4	SLBO+	System Loopback Noninverting Output. Enabled when SOS is high.
6	SOS	System Loopback Output Select. System loopback disabled when low.
8	SCLKO-	Inverting PECL Serial Clock Output
9	SCLKO+	Noninverting PECL Serial Clock Output
11	SDO-	Inverting PECL Serial-Data Output
12	SDO+	Noninverting PECL Serial-Data Output
15	PCLKI+	Noninverting LVDS Parallel Clock Input. Connect the incoming parallel-clock signal to the PCLKI inputs. Note that data is updated on the positive transition of the PCLKI signal.
16	PCLKI-	Inverting LVDS Parallel Clock Input. Connect

		the incoming parallel-clock signal to the PCLKI inputs. Note that data is updated on the positive transition of the PCLKI signal.
18, 20, 22, 24, 26,28, 30, 34, 36, 38,40, 42, 44, 46, 50, 52	PDI15+ to PDI0+	Noninverting LVDS Parallel Data Inputs. Data is clocked on the PCLKI positive transition.
19, 21, 23, 25, 27,29, 31, 35, 37, 39,41, 43, 45, 47, 51, 53	PDI15- to PDI0-	Inverting LVDS Parallel Data Inputs. Data is clocked on the PCLKI positive transition.
54	PCLKO+	Noninverting LVDS Parallel Clock Output. Use positive transition of PCLKO to clock the overhead management circuit.
55	PCLKO-	Inverting LVDS Parallel Clock Output. Use positive transition of PCLKO to clock the overhead management circuit.
57	RCLK+	Noninverting LVDS Reference Clock Input. Connect an LVDS-compatible crystal reference clock to the RCLK inputs.
58	RCLK-	Inverting LVDS Reference Clock Input. Connect an LVDS-compatible crystal reference clock to the RCLK inputs.
59	CLKSET	Reference Clock Rate Programming Pin: CLKSET = VCC: Reference Clock Rate = 155.52MHz CLKSET = Open: Reference Clock Rate = 77.76MHz CLKSET = 20kΩ to GND: Reference Clock Rate = 51.84MHz CLKSET = GND: Reference Clock Rate = 38.88MHz
61	FIL-	Filter Capacitor Input. Connect a 330nF capacitor between FIL+ and FIL-.
62	FIL+	Filter Capacitor Input. Connect a 330nF capacitor between FIL+ and FIL-.

EP	Exposed Pad	Ground. This must be soldered to a circuit board for proper thermal performance (see *Package Information*).

3.3 Pre-Amplifier

Max 3867: + 3.3V, 2.5Gbps SDH/SONET Laser driver with Automatic Power Control.

(referred as pre-amplifier through out the discussion)

Max 3867 accepts differential PECL data and clock inputs and provides bias and modulation currents. An Automatic Power Control (APC) feedback loop is incorporated to maintain a constant average power over temperature and lifetime. The wide modulation current range of 5mA and 60mA and bias current of 1mA to 100mA are easy to adjust making this product ideal for use in various SDH/SONET applications.

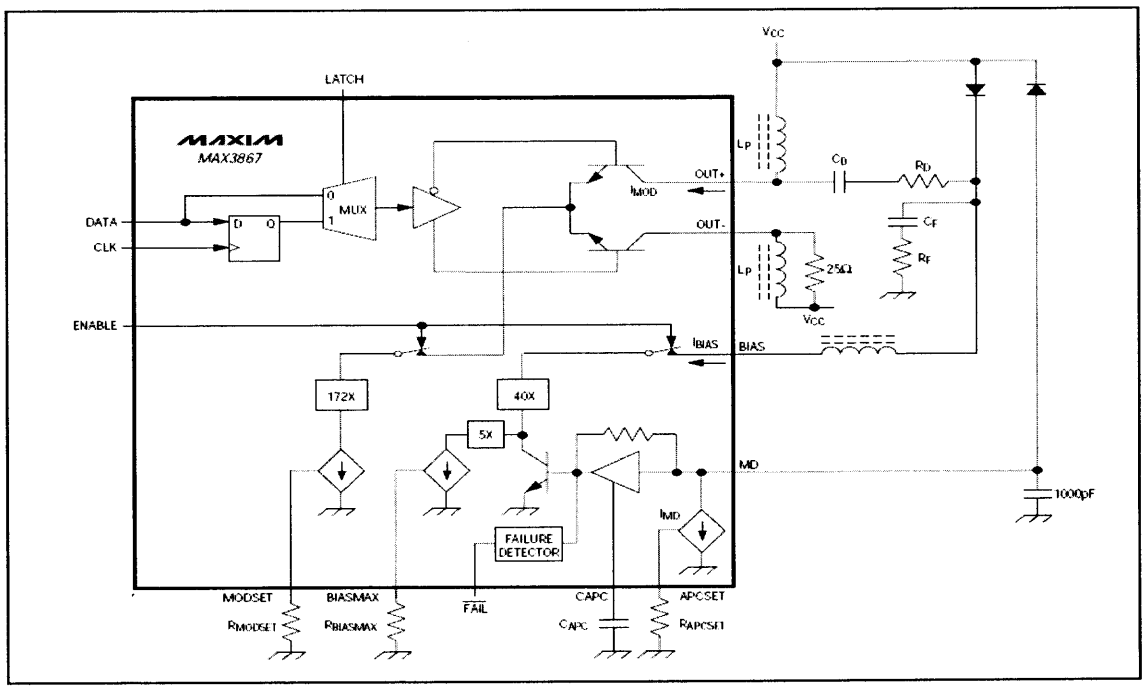

Figure 3.8 Functional block diagram.

Max 3867 consists of two main parts: an optical and an electrical part with Automatic Power Control (APC).This project deals only with the electrical part. When APC loop is functioning, the maximum allowable bias current is set by an external resistor, $R_{BIASMAX}$. An APC failure flag (FAIL) is set low when the bias current can no longer be adjusted to achieve the desired level. APC closed-loop operation requires the user to set three currents with external resistors connected between grounds BIASMAX, MODSET, and APCSET.

Table 1.4 Detailed Descriptions

PIN	NAME	FUNCTION
1, 42, 45	GND2	Ground for internal reference
2, 7, 12, 15, 16	GND1	Ground for digital circuits
3, 6, 8, 11, 18	VCC1	Power supply for digital circuits
4	DATA+	Positive PECL Data Input
5	DATA-	Negative PECL Data Input
9	CLK+	Positive PECL Clock Input. Connect to VCC if latch function is not used.
10	CLK-	Negative PECL Clock Input. Leave unconnected if latch function is not used.
13	LATCH	TTL/CMOS Latch Input. High for latched data, low for direct data.
14	ENABLE	TTL/CMOS Enable Input. High for normal operation, low to disable laser bias and modulation currents
17	SLWSTRT	A capacitor from this pad to ground delays the turn-on time of laser bias and modulation currents.
19	**FAIL**	TTL/CMOS output. Indicates APC failure when low.
21, 26, 28, 31, 39, 41, 43	N.C.	No Connection. Leave unconnected.
22	APCFILT	Connect a capacitor (CAPCFILT = 0.1μF) from this pad to ground to filter the APC noise.
20, 23, 33	GND4	Ground for output circuitry
24, 27, 32	VCC4	Power Supply for output circuitry
25	BIAS	Laser Bias Current Output
29	OUT+	Positive Modulation-Current Output. IMOD flows through this pad when input data is high.

30	OUT-	Negative Modulation-Current Output. IMOD flows through this pad when input data is low.
35	MD	Monitor Diode Input. Connect this pad to a monitor photodiode anode. A capacitor to ground is required to filter high-speed AC monitor photocurrent.
34,36,40	GND3	Ground for APC
37	VCC3	Power Supply for APC
38	CAPC	A capacitor connected from this pad to ground controls the dominant pole of the APC feedback loop. (CAPC = 0.1μF)
44	APCSET	A capacitor connected from this pad to ground controls the dominant pole of the APC feedback loop. (CAPC = 0.1μF) Connect 100k½ from this pad to ground if APC is not used.
46	MODSET	A resistor connected from this pad to ground sets the desired modulation current.
47	BIASMAX	A resistor connected from this pad to ground sets the maximum bias current. The APC function can subtract from this maximum value, but can not add to it.
48	VCC2	Power Supply for internal reference

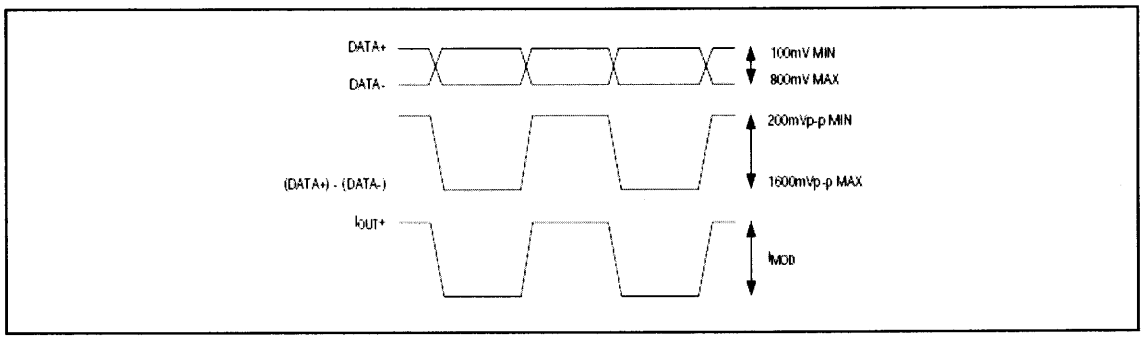

Figure 3.9 Required input signal and output polarity.

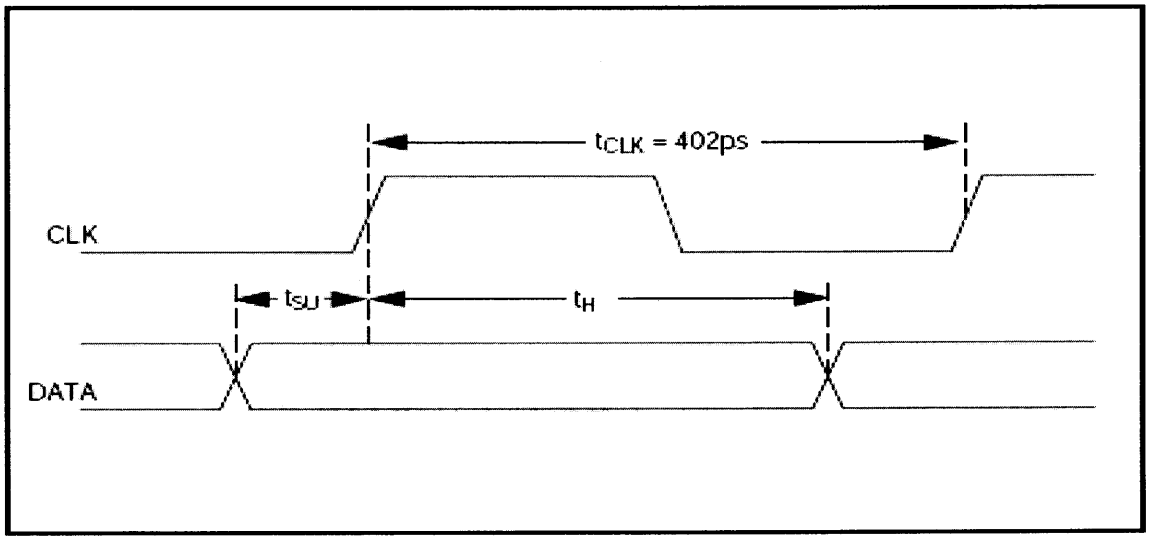

Figure 3.10 Setup/hold time definition.

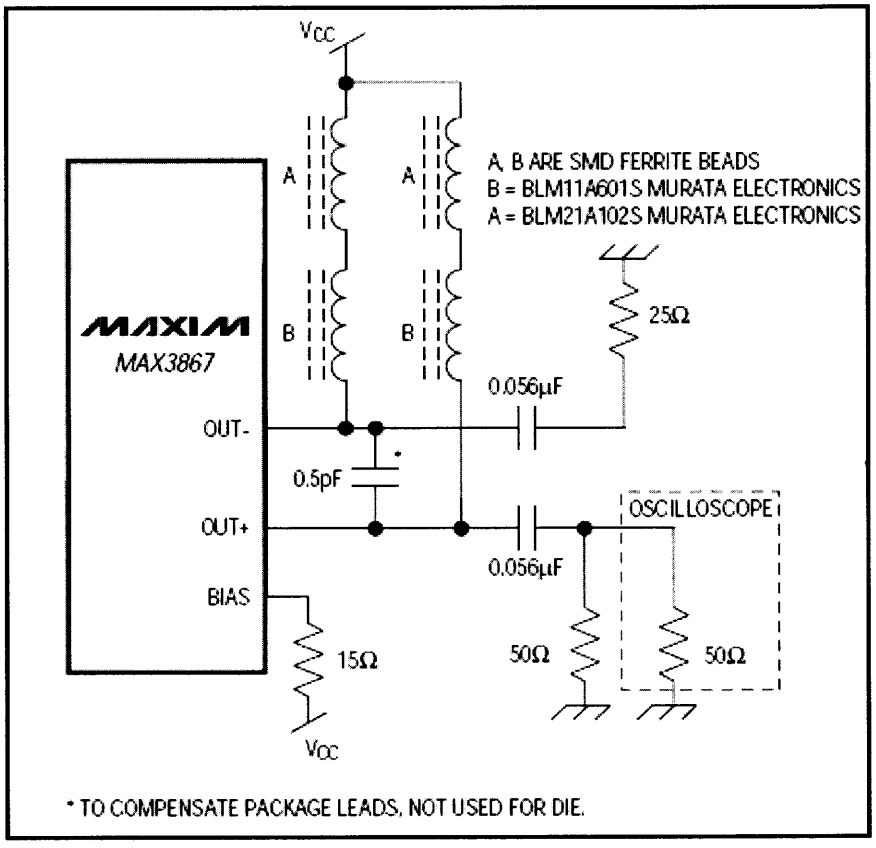

Figure 3.11 Output termination for characterization.

3.4 Post-Amplifier

Max 3866: +3.3V, 2.5Gbps Combined Transimpedance/ Limiting Amplifier (referred as post-amplifier through out the discussion)

A combination of transimpedance preamplifier and limiting postamplifier intended for applications in SDH/SONET systems operating at 2.488Gbps. This board also operates from a single +3.3V or +5V supply and provides a differential output signal. The differential outputs here also are 50Ω reverse terminated (100Ω differential termination) for low noise and high speed signal performance. Equipped with a power detect circuit, it consists of an adjustable gain amplifier and combined rectifier with a low pass filter.

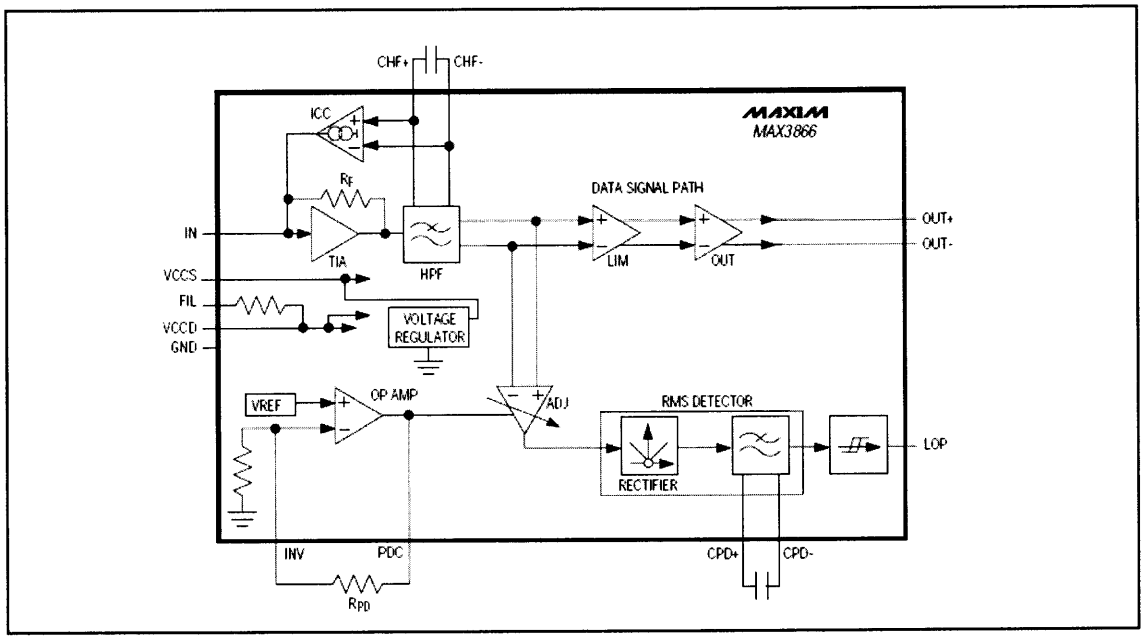

Figure 3.12 Functional block diagram.

The board accepts an input current from the antenna attached to the input pad IN+. The transimpedance input amplifier stage converts the input current to an output voltage. The second stage of the data path is an active high-pass filter. This filter converts the single-ended input signal to a differential signal, eliminating the DC component and adding approximately 16dB of gain. This output of the highpass filter drives the power

detector and limiting amplifier circuitry. The third stage that is the limiting amplifier stage amplifies and limits the differential input signal. The output voltage is typically limited to 145mVp-p.

The adjustable gain amplifier in the power detector circuit mentioned above is controlled by an op amp. The gain is adjusted by means of an external resistor connected between the PDC and INV pins. This output voltage of the adjustable gain amplifier drives the combined rectifier and lowpass filter circuitry. The resulting DC voltage is fed to a Schmitt trigger, which generates a high-level output signal if the DC input signal is below the Loss of Power (LOP) assert level, thus causing an LOP condition on the LOP output. The LOP function can be adjusted by setting R_{PD} = 510Ω, if the function is desired or else R_{PD} could be set to 0Ω. This Evaluation kit is supplied by 3.3V, supply voltage and is applied to VCCS pin.

Table1.5 Detailed Descriptions

PIN	FUNCTION
VCCS	Positive Supply Voltage of Input Stage. Apply +3.3V if VCCD = +3.3V. If VCCD > +3.47V, disconnect from supply and decouple to GND.
CHF+	External Filter Capacitor. A capacitor connected between CHF+ and CHF- is used for setting the low-frequency cutoff
CHF-	External Filter Capacitor. A capacitor connected between CHF+ and CHF- is used for setting the low-frequency cutoff
FIL	On-Chip Resistor for Filtering Photodiode Supply Voltage (connected to VCCD on chip)
GND	Electrical Ground
IN+	Signal Input
IN-	No Connect
PDC	The voltage at this node programs the gain of the power detector.

	Connect a resistor between PDC and INV to adjust the LOP threshold.
INV	Used for programming the gain of the power detector. Connect a resistor between PDC and INV to adjust the LOP threshold.
CPD-	Filter Node for Power Detector. A capacitor connected between CPD+ and CPD- will provide additional filtering to the rectifier output within the power detector.
CPD+	Filter Node for Power Detector. A capacitor connected between CPD+ and CPD- will provide additional filtering to the rectifier output within the power detector.
OUT-	Inverted Data-Signal Output
OUT+	Noninverted Data-Signal Output
LOP	TTL Output, Loss-of-Power, active high
VCCD	Power-Supply Voltage

3.5 Deserializer

Max 3880: +3.3V, 2.488Gbps, SDH/SONET 1:16 Deserializer with clock recovery (referred as deserializer through out the discussion)

The Max 3880 deserializer with clock recovery converts 2.488GBPS serial data to 16-bit-wide 155Mbps parallel data for SDH/SONET applications. Operating at +3.3V supply, this device accepts high-speed serial-data inputs and delivers low-voltage differential-signal (LVDS) parallel clock and data outputs for interfacing with digital circuitry.

The MAX 3880 includes a low-power clock recovery and data retiming function for 2.488Gbps applications as mentioned earlier. And the fully integrated phase-

locked loop (PLL) recovers a synchronous clock signal from the serial Non Return to Zero (NRZ) data input and the signal is then retimed by the recovered clock.

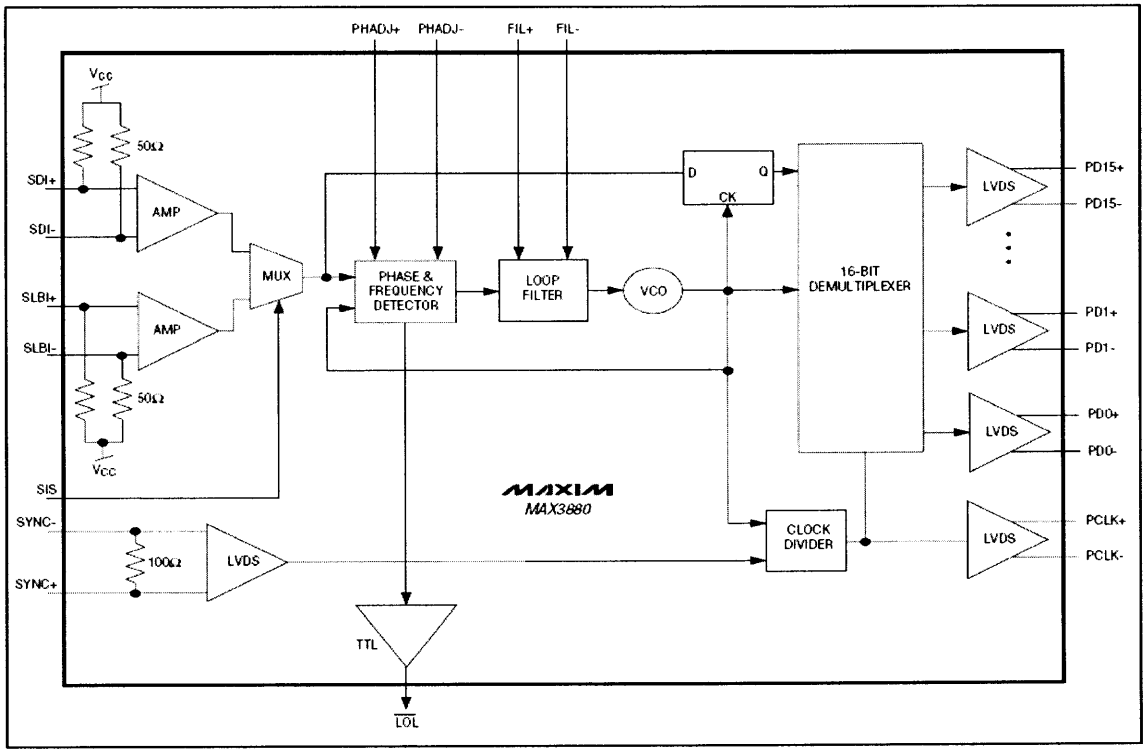

Figure 3.13 Functional block diagram.

The device combines a fully integrated phase-locked loop (PLL), input amplifier, data retiming block, 16-bit demultiplexer, clock divider, and LVDS output buffer as shown in Figure 3.13. The Phase-Locked Loop consists of a Phase/Frequency Detector (PFD), a loop filter, and a Voltage-Controlled Oscillator (VCO). The Max3880 is designed to deliver the best combination of jitter performance and power dissipation .As the PLL recovers the serial clock from the serial input data stream and the demultiplexer generates a 16-bit-wide 155Mbps parallel data output.

As indicated in the previous chapter; Synchronization being the main key of communication, we have synchronization inputs to realign the output data word.

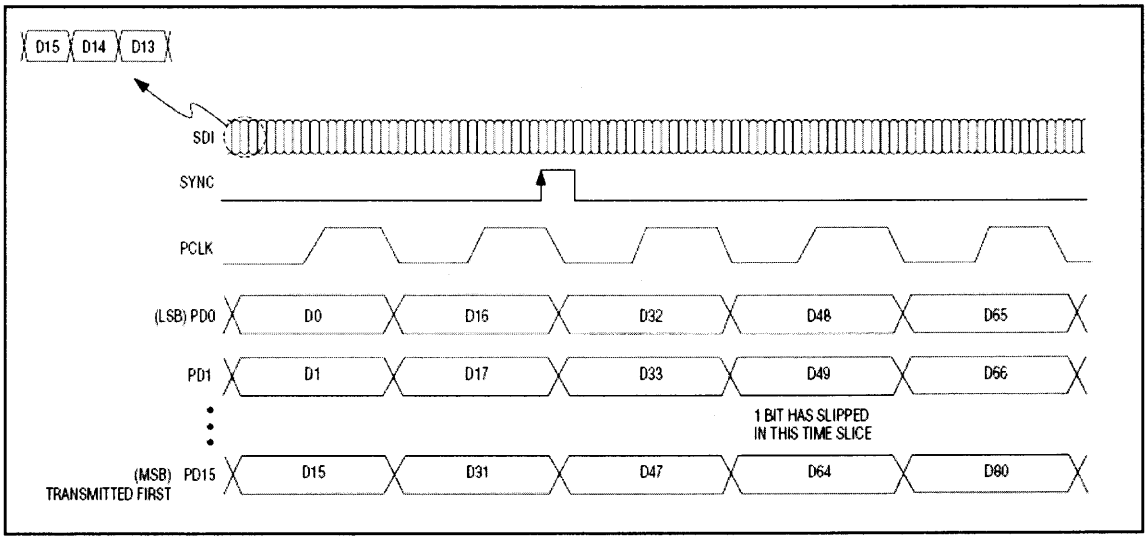

Figure 3.14 Timing diagram.

The input amplifiers on both the main data and system loopback accept differential input amplitude from 50mVp-p to 800mVp-p. The digital Frequency Detector (FD) aids frequency acquisition during startup conditions. The frequency difference between the received data and the VCO clock is derived by sampling the in-phase and quadrature VCO outputs on both edges of the data input signal. Depending on the polarity of the frequency difference, the FD drives the VCO until the frequency difference is reduced to zero. Frequency detector returns to zero once frequency acquisition is over. Thus, this digital frequency detector completely eliminates the false locking.

The phase detector and frequency detector outputs are summed into the loop filter. This loop filter output controls the on-chip LC VCO running at 2.488GHz. The VCO provides low phase noise and is trimmed to the correct frequency.

A Loss of Lock monitor is included in the Max3880 frequency detector that signals a Loss of Lock condition immediately with a TTL low. When the PLL is

frequency-locked, Loss of Lock switches to TTL high in approximately 800ns. An important fact about this indicator is that Loss of Lock is only valid when a data stream is present on the inputs to the board. Thus indicating that does not detect loss-of-power condition resulting from a loss of the incoming signal.

Table 1.6 Detailed Descriptions

PIN	NAME	FUNCTION
1, 17, 25, 33, 41, 49, 56, 62, 64	GND	Ground
2	FIL+	Positive Filter Input. PLL loop filter connection. Connect a 1.0μF capacitor between FIL+ and FIL-.
3	FIL-	Negative Filter Input. PLL loop filter connection. Connect a 1.0μF capacitor between FIL+ and FIL-.
4, 7, 10, 13, 24, 32, 40, 48, 57	VCC	+3.3V Supply Voltage
5	PHADJ+	Positive Phase-Adjust Input. Used to optimally align internal PLL phase. Connect to VCC if not used.
6	PHADJ-	Negative Phase-Adjust Input. Used to optimally align internal PLL phase. Connect to VCC if not used.
8	SDI+	Positive Serial Data Input. 2.488Gbps data stream.
9	SDI-	Negative Serial Data Input. 2.488Gbps data stream.
11	SLBI+	Positive System Loopback Input. 2.488Gbps data stream.
12	SLBI-	Negative System Loopback Input. 2.488Gbps data stream.

14	SIS	Signal Input Selection. TTL low for normal data input (SDI). TTL high for system loopback input (SLBI).
15	SYNC-	Negative Synchronizing Pulse LVDS Input. Pulse the SYNC signal high for at least four serial-data bit periods (1.6ns) to shift the data alignment by dropping 1 bit.
16	SYNC+	Positive Synchronizing Pulse LVDS Input. Pulse the SYNC signal high for at least four serial-data bit periods (1.6ns) to shift the data alignment by dropping 1 bit.
18	PCLK-	Negative Parallel Clock LVDS Output
19	PCLK+	Positive Parallel Clock LVDS Output
20, 22, 26, 28, 30, 34, 36, 38, 42, 44, 46, 50, 52, 54, 58, 60	PDO- to PD15-	Negative Parallel Data LVDS Outputs. Data is updated on the negative transition of the PCLK signal.
21, 23, 27, 29, 31, 35, 37, 39, 43, 45, 47, 51, 53, 55, 59, 61	PDO+ to PD15+	Positive Parallel Data LVDS Outputs. Data is updated on the negative transition of the PCLK signal.
63	LOL	Loss-of-Lock Output. PLL loss-of-lock monitor, TTL active low (internal 10kΩ pull-up resistor). The LOL monitor is valid only when a data stream is present on the inputs to the MAX3880.
EP	Exposed Pad	Ground. This must be soldered to a circuit board for proper thermal performance.

3.6 LVDS to single ended converter

Max 9124: Quad LVDS Line Driver (referred as LVDS to single ended converter throughout the discussion)

The Max 9124 quad low-voltage differential signaling (LVDS) line driver is ideal for applications requiring high data rates, low power, and low noise. It accepts four LVTTL/LVCMOS input levels and translates them to LVDS output signals. Max 9124 is capable of setting all four outputs to a high impedance state through two enable inputs, thus dropping the device to an ultra-low-power state of 16mW (typical) during high impedance. The enables are common to all four transmitters. This board operates from a single +3.3V supply. The Max 9124 contains a low voltage differential signaling quad line driver (Max9124) and receiver (Max9125). The differential line driver accepts LVTTL or LVCMOS inputs and translates them to LVDS output signals. The receiver accepts LVDS inputs and translates them to single-ended LVCMOS outputs. Both these circuitry operate with high data rates and low power dissipation.

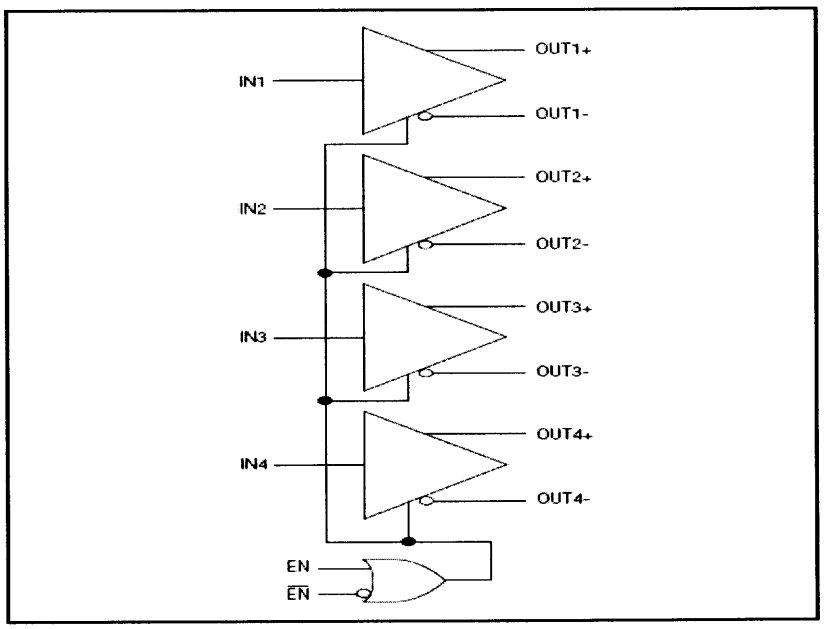

Figure 3.15 Functional block diagram.

This is an 800Mbps quad differential LVDS driver that is designed for high-speed, point-to-point, and low power applications. This board generates a 2.5mA to 4.0mA output current using a current steering configuration. This current steering approach induces less ground bounce and no shoot-through current, enhancing noise margin and system speed performance. The drivers outputs are short circuit current limited and enter a high-impedance state when the device is not powered or is disabled. The signal from the deserializer is fed to the channels of Max 9124 and the single ended signal is then viewed on the Vector Signal Analyzer in the frequency domain. Its IFFT can be found out to trace the signal in the time domain.

Table 1.7 Detailed Descriptions

PIN	NAME	FUNCTION
1, 7, 9, 15	IN_	LVTTL/LVCMOS Driver Inputs
2, 6, 10, 14	OUT_+	Noninverting LVDS Driver Outputs
3, 5, 11, 13	OUT_-	Inverting LVDS Driver Outputs
4, 12	EN, **EN**	Driver Enable Inputs. The driver is disabled and in high impedance when EN is low and EN is high. For other combinations of EN and EN, the outputs are active.
8	GND	Ground
16	VCC	Power-Supply Input. Bypass VCC to GND with 0.1μF and 0.001μF ceramic capacitors.

CHAPTER 4

LVDS SIGNALS

LVDS stands for Low Voltage Differential Signal and is a standard defined by IEEE (IEEE Std. 1596) TIA/EIA-644. LVDS is a low noise, low power, and low amplitude method using high speed analog circuit techniques to provide multi gigabit data transfers on copper interconnect.

4.1 Introduction

The need for data transfers is increasing dramatically in all areas of communications and in addition, data streams are requiring higher and higher bandwidth. The digital communications deluge is the driving force for high-speed interconnects between chips, functional boards, and systems. The data may be digital, but it is LVDS that designers are choosing to drive these high-speed transmission lines. LVDS's proven speed, low power, noise control, and cost advantages are popular in point-to-point applications for telecommunications, data communications, and displays. LVDS offers high speed data transfer at the rate of 100 Mbps and higher.

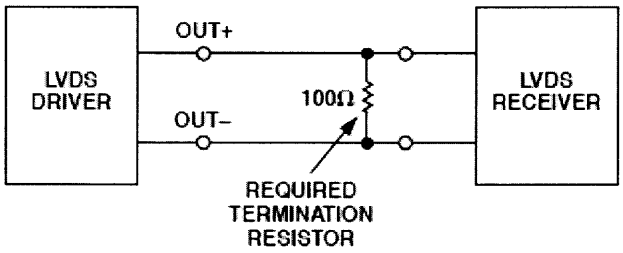

Figure 4.1 LVDS requires far end termination.

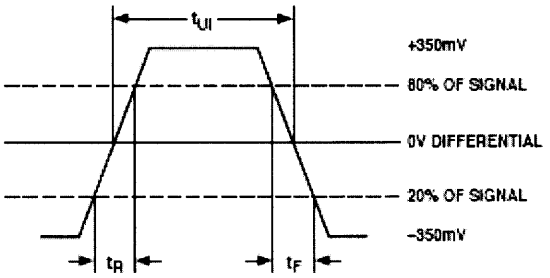

Figure 4.2 Timing diagram.

4.2 LVDS Input and Output Structure

The LVDS input signal, shown in Figure 4.3, has on-chip 100Ω differential impedance between IN+ and IN-. To accommodate a wide common-mode voltage range, an adaptive level-shifting circuit sets the common-mode voltage to a constant value at the input of a Schmitt trigger. The Schmitt trigger provides hysteresis relative to the input threshold. This signal is then applied to the following differential amplifier stage.

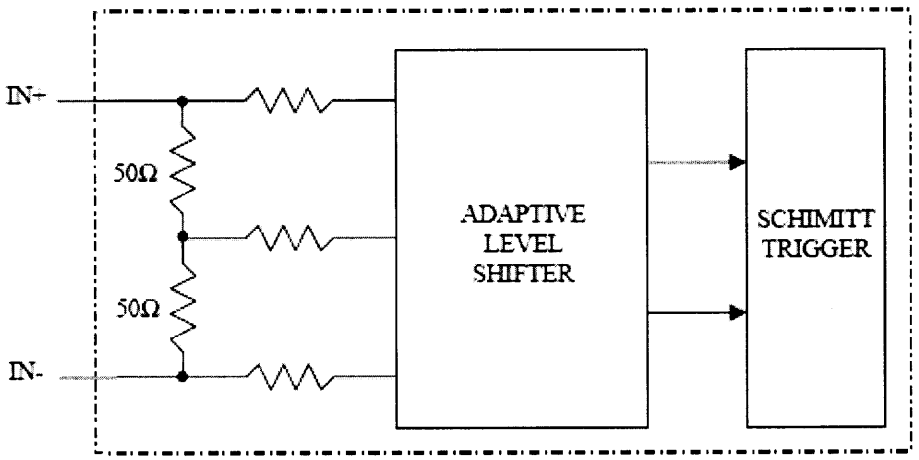

Figure 4.3 LVDS input structure.

Maxim's LVDS output structures are optimized for low-power and high-speed operation. The circuit configuration is shown in Figure 4.4. The differential output impedance is typically 100Ω.

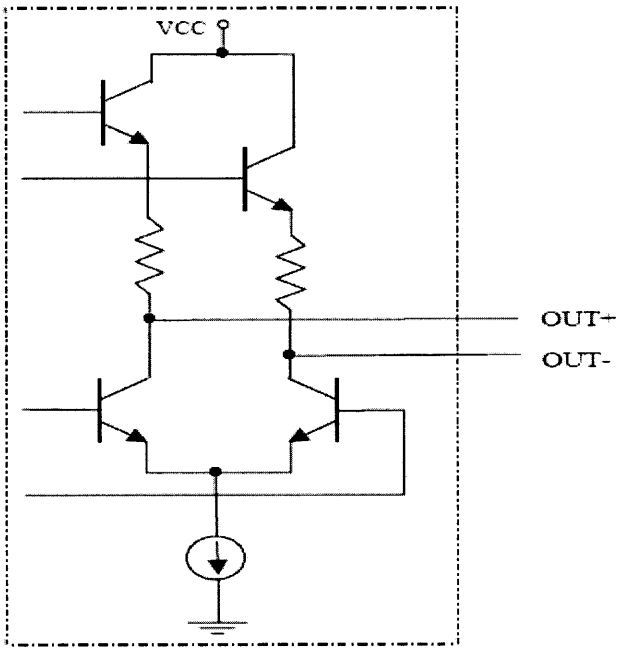

Figure 4.4 LVDS output structure.

The current returns within the wire pair, so the current loop area is small and therefore generates the lowest amount of electromagnetic interference (EMI). The current source limits any spike current that could occur during transitions. Because there are no spike currents, data rates as high as 1.5 Gbps are possible without a substantial increase in power dissipation.

4.3 Multiple Technologies and Supply Voltages

When choosing the signal-level voltages for drivers and receivers, the standards committee considered LVDS implementation in technologies such as bipolar, complementary metal oxide semiconductor (BiCMOS), and even GaAs. In addition, the

working group targeted a wide range of power supplies (such as 5 V, 3.3 V, and 2.5 V) for implementing LVDS to ensure that LVDS would be the interface of choice for future generations of products.

Low-voltage signals have many advantages, including fast bit rates, lower power, and better noise performance. Design engineers have previously used full-swing CMOS and low-voltage, transistor-transistor logic (LVTTL), but as bit rates increase, these solutions become unattractive. More recently, designers have turned to reduced-swing technologies such as stub series terminated logic (SSTL) and gunning transceiver logic (GTL) to gain speed, save power, and reduce noise. LVDS increases these advantages by lowering voltage swings to about 300 mV. To increase noise immunity and noise margins even further, LVDS uses differential data transmission. Differential signals are immune to common-mode noise, the primary source of system noise. An LVDS signal also changes voltage levels without a fast slew rate. Slowing the transition rate decreases the radiated field strength. Slower transitions reduce the problem of reflections from transmission-path impedance discontinuities, decreasing emissions and crosstalk problems. Low-voltage swing reduces power consumption because it lowers the voltage across the termination resistors and lowers the overall power dissipation.

For example, when the signal level changes 300 mV in 333 ps, the slew rate is only 0.9 V/ns, which is less than the 1 V/ns benchmark slew rate commonly acceptable for minimizing signal distortion and crosstalk. If we use the old benchmark that rise and fall times should be no more than two-thirds of the bit width, then signals with 333-ps transitions can operate as high as 1 Gbps with plenty of margin.

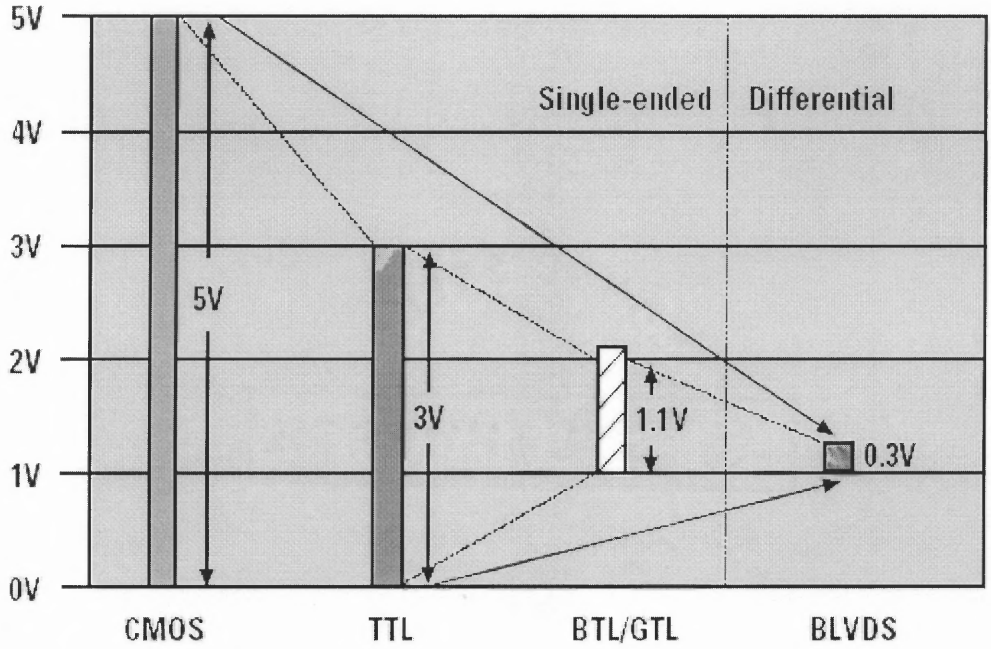

Figure 4.5 Comparison of voltage swings of various backplane technologies (Ref: Courtesy National).

4.4 Advantages of LVDS Signals

LVDS system features, such as serializing data, encoding the clock, and low skew, all work together for higher performance. Skew is a big problem for sending parallel data and its clock across cables or PCB traces. The problem is that the phase relation of the data and clock can be lost as a result of different travel times through the link. However, the ability to serialize parallel data into a high-speed signal with embedded clock eliminates the skew problem. The problem disappears because the clock travels with the data over the same differential pair of wires. The receiver uses clock and data recovery to extract the embedded clock, which is phase-aligned to the data.

4.4.1 Low Power Requirement

A significant advantage of LVDS technology is the lower power requirement. LVDS's supply current remains flat as the operating frequency increases, whereas the supply current for CMOS and GTL technology increases exponentially as frequency increases. LVDS benefits because it uses a constant-current line driver rather than a voltage-mode driver. The load power calculation (3.3 mA times the 330-mV drop across the 100-W termination resistor) means LVDS has only 1.1–mW load power consumption. Furthermore, the low power consumption inherent in LVDS technology eliminates the need for either heat sinks or special packaging. This benefit also reduces the system cost of Gigabit data transfers.

4.4.2 Low Electromagnetic Interference

Another advantage of LVDS is its low electromagnetic-interference generation. The reasons LVDS generates low emissions are its low voltage swing, slow edge rates, the odd-mode differential signals, and the minimal I_{cc} spikes from constant current drivers. High-frequency signal transitions flowing through a transmission path create electromagnetic fields that radiate emissions. The field's strength is proportional to the energy carried by the signal. By reducing the voltage swing and the current energy, LVDS minimizes these fields. However, even the reduced electromagnetic fields can cause radiation problems. Differential signal paths reduce the harmful effects of these fields to minimize these radiation problems further. Balanced differential lines have equal but opposite currents, called odd-mode signals. When the fields created by these odd-mode signals are closely coupled, they tend to tie each other up and thus cannot escape to

cause harm. Therefore, it is important to maintain a balanced and closely coupled differential transmission path to reduce the emission of electromagnetic interference. Differential signals also have the advantage of tolerating interference from outside sources such as inductive radiation from electric motors or crosstalk from neighboring transmission lines. When the differential transmission lines are closely coupled, the induced signal is common-mode noise that appears as a common-mode voltage at the receiver input. The differential receiver responds only to the difference between the plus and the minus inputs, so when the noise appears commonly to both inputs, the input differential signal amplitude is undisturbed. This common-mode noise rejection also applies to noise sources such as power supply variations, substrate noise, and ground bounce.

4.4.3 High Noise Immunity

These signals tolerate high levels of switching noise, so they can be reliably integrated with large-scale digital circuits. In addition, LVDS generates very little noise as a result of the constant-current nature of the output structures.

4.4.4 Many channels per chip

Because LVDS is capable of handling the high-speed data that results from serializing many parallel bits into a single data stream, LVDS chips commonly integrate serializers and deserializers. This saves about 50 percent of the cabling, connector, and PCB costs when compared to a parallel interconnect. The final LVDS system benefit is its integration capability. Because it is possible to implement high-speed LVDS in a standard CMOS process, integrating complex digital functions with LVDS's analog

circuits is very beneficial. Integrating serializers and deserializers is only the beginning to mixed-signal LVDS chips. LVDS's low power consumption enables integrating many channels per chip

4.4.5 Cost Benefit

All of the LVDS advantages discussed so far also benefit system cost. There are even more system cost savings from using LVDS. The first is LVDS's ability to tolerate minor impedance mismatches in transmission paths. As long as the differential signal passes through balanced discontinuities in closely coupled transmission paths, the signal can maintain integrity. The effect of non-impedance-controlled connectors, PCB via's, and chip packaging is not as detrimental to differential signals as it is to single-ended signals. In addition, it is possible to use fewer circuit board layers because of the relative immunity to crosstalk that is inherent in differential signals.

4.5 Disadvantage of LVDS Signal

However, LVDS does have a disadvantage in power dissipation compared to CMOS. LVDS power dissipation is constant and does not scale linearly with clock rates as in CMOS; at low sample rates CMOS can dissipate less power than LVDS. As sample rates increase, CMOS power dissipation will increase linearly with sample rate, eventually requiring more power than LVDS. At sample rates equal to 200 MSamples/s, LVDS and CMOS power dissipation are comparable.

CHAPTER 5

RESULTS AND CONCLUSIONS

5.1 Pseudorandom Bit Sequence (PRBS)

When testing high speed communication systems or components the test signals should be as similar as possible to the actual data transmitted the system is deployed. Real life signals are completely random: in frequency domain this translates to a continuous spectrum within a finite bandwidth. As a measurement should be reproducible, the test signals have to be standardized. The solution to this is to transmit Pseudo Random Bit Sequences (PRBS). PRBS signals have a very long periodicity (very dense discrete spectral components) and are therefore very similar to completely random signals. On the other hand, PRBS signals can be reproduced without any ambiguity. These signals have spectral components distributed over the entire transmission bandwidth.

Pseudo Random Bit Sequences (PRBS) are generated by shift registers: Some outputs of the registers are fed back via an XOR to the input. Depending upon the length of the shift register and the outputs back fed, different output patterns are generated. For some possible combinations a pattern is obtained with a maximum period before it repeats. The maximum period is 2n-1, where n is the amount of registers. The reason for the value of –1 is because a pattern consisting of n zeros is not feasible. The PRBS output may or may not be inverted.

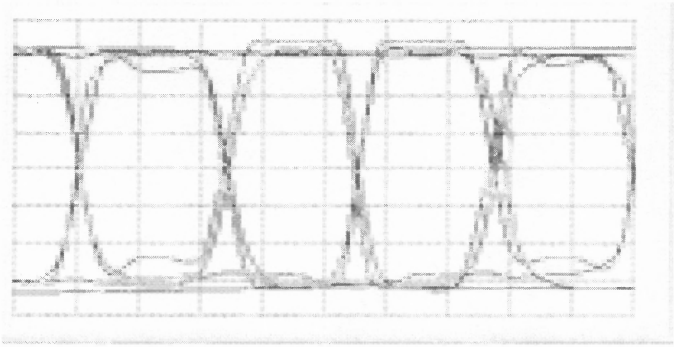

Figure 5.1 Typical pseudorandom bit sequence observed on an oscilloscope. (Both '0'and '1' are present and a good system delivers an 'open eye diagram', namely the system can resolve both bits, faithfully)

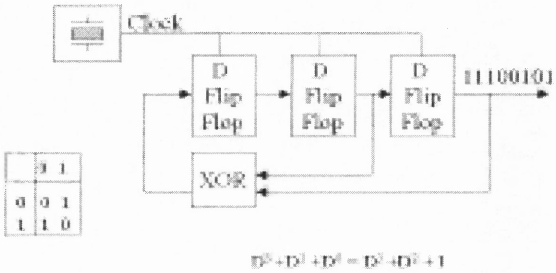

Figure 5.2 Circuitry showing pseudorandom bit sequence generation.

A PRBS- Signal in the frequency domain has a sinc output. The first zero occurs at the clock frequency and the temporal spacing of the individual spectral lines is the reciprocal of the period of the PRBS sequence. To obtain higher bit rates PRBS Generator has to be provided with a clock and also the signals have to be multiplexed. The PRBS characteristic of the input pattern is maintained by multiplexing.

To observe the pseudorandom signal on the oscilloscope, the clock or a synchronizing signal is used to trigger the oscilloscope. Many recordings are superimposed on each other to generate an "eye diagram". An eye diagram is an alternative way of displaying a digital signal on the oscilloscope. Figures (5.3, 5.4, 5.5) shows the pseudorandom data

signal observed on the oscilloscope at the output of the PCI card. On an eye diagram effects like droop, overshoot, ringing, noise, jitter and pattern dependencies can be seen.

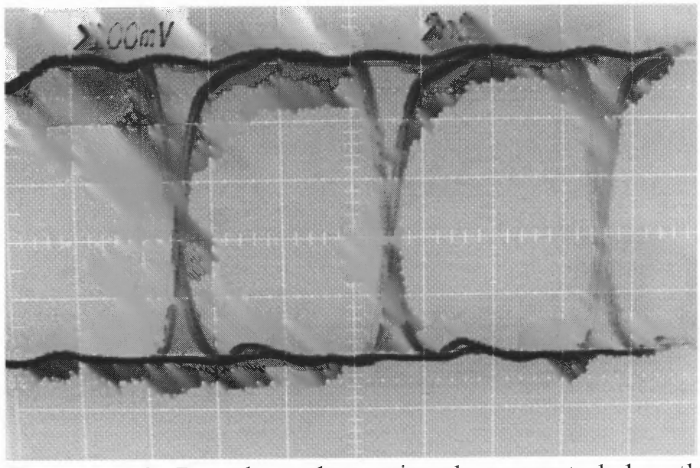

Figure 5.3 Pseudorandom signal generated by the PCI card, as observed on an oscilloscope.

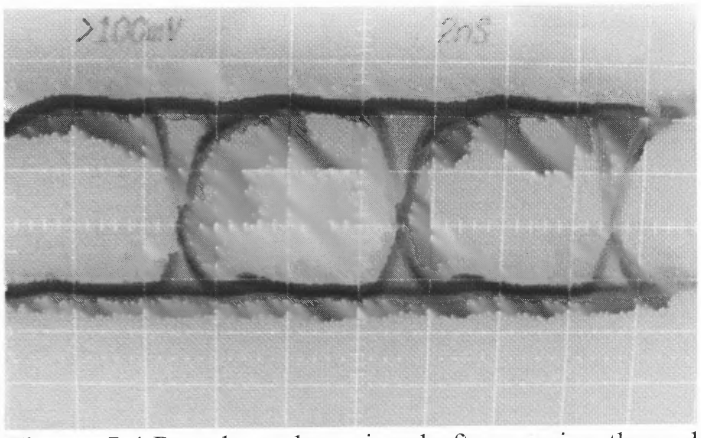

Figure 5.4 Pseudorandom signal after passing through 1:2 power divider, as observed on an oscilloscope.

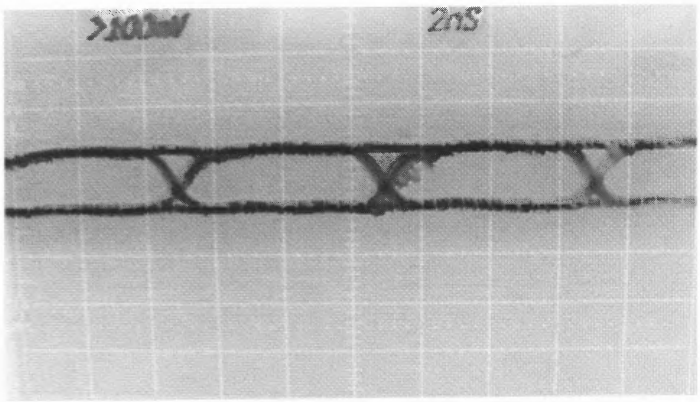

Figure 5.5 Pseudorandom signal after passing through 1:8 power divider alone, as observed on an oscilloscope.

As expected the signal amplitude decreased after being divided by the power dividers. The signal had already reached 100 mV thresholds after being divided into eight; hence no further divisions were advisable. Another technique known as "DC biasing" was used for the rest of the channels.

5.2 DC Biasing

As explained in chapter 3, the serializer Max3890 converts sixteen parallel input channels at the rate of 155.52 MHz each to an overall bandwidth of 2.5 GHz. Each of these sixteen Low Voltage Differential Signal (LVDS) data channels needs a 100mV differential voltage to function. DC biasing technique results in a predetermined pattern of "1" and "0".

On a single channel the positive LVDS connected to the positive terminal of the power supply and the negative connected to the ground of the power supply and the output voltage adjusted to 100mV would generate a binary one on that particular channel. On the other hand, when the negative LVDS of a channel is connected to positive terminal of the power supply and the positive LVDS connected to the ground with the voltage level adjusted to 100mV would generate a binary zero on that particular channel. The channels are connected to terminals of the power supply via a 50ohm resistor in order to protect the input circuitry. This DC biasing technique is used to generate a desired pattern of ones and zeros for each of the channels. A differential clock signal at the rate of 155.52 MHz is also provided to the serializer and thus the sixteen channels are combined to form 2.5 GHz bandwidth communication system.

5.3 Antennas

Antennas were used to transmit and receive the RF signals over the channel in the gigahertz range. First, commercially available omni directional antennas were used, designed to work in the range of 1-18 GHz these antennas were not able to pick the signals in the megahertz range, where these signals were predominantly present. Spiral broadband antennas, designed in-house (though not specifically for UWB application) were used. This antenna could pick up signals ranging from megahertz to gigahertz. An amplifier (100-4500 MHz range) was used to further boost the signals before being fed to the transmitting antenna. One ought to emphasize that ordinary "wideband" antennas do not transmit fast transients owing to large dispersion. Both frequency and spatial dispersions should be taken into consideration while building the UWB antennas. Frequency dispersion can be overcome by Transverse Electromagnetic (TEM) horn or biconical antennas. Both structures minimize frequency dispersion and spatial dispersion can be reduced by using lenses and reflectors [15].

5.4 Results

UWB employs baseband pulses of very short duration, typically in nanoseconds, and spreads the signal energy through the entire spectrum. Due to the low energy spectrum, probabilities of intercept and detection are low.

In this project, tests were performed over the communication link in order to assess the viability of the UWB system. The main objective of the test was to compare input signal at 155.52 MHz to output of the link for each of the channels.

As mentioned earlier, a diagnostic test link provided between the two boards; the serializer (Max 3890) and the deserializer (Max 3880) were used as reference to the results of the designed communication link. Three cases were assessed:

1. All channels were fed with the same pseudorandom signal.
2. Half of the channels were dc biased and the remaining channels were fed with pseudorandom signals.
3. All the channels were dc biased.

Signals were measured at the output of pre-amplifier (Max 3867) on transmitter side as it gave a single ended PECL output, and at the end of deserializer (Max 3880), since this provides LVDS output, the signal is converted into a single ended output with the help of Converter board (Max 9124).

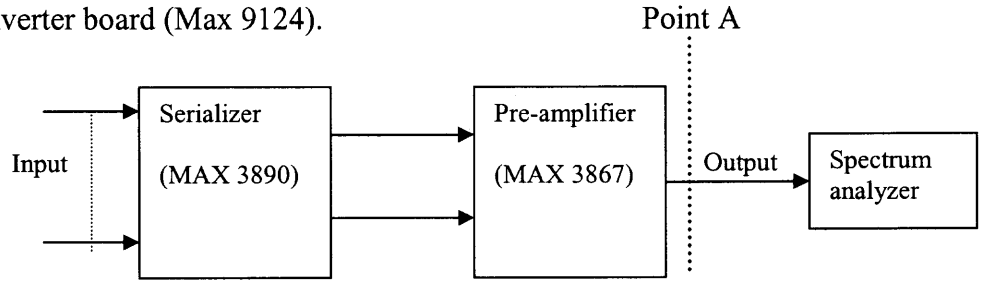

Figure 5.6 Showing the first point of measurement on the link.

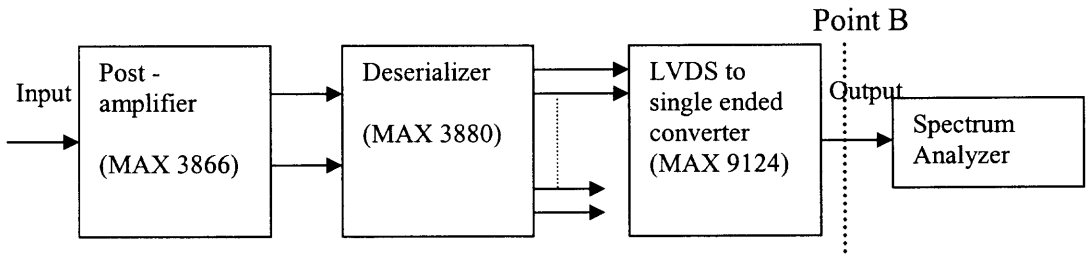

Figure 5.7 Showing the second point of measurement on the link.

1. All channels were fed with pseudorandom signal.

a) Signal measured at point A (Refer Fig 5.6).

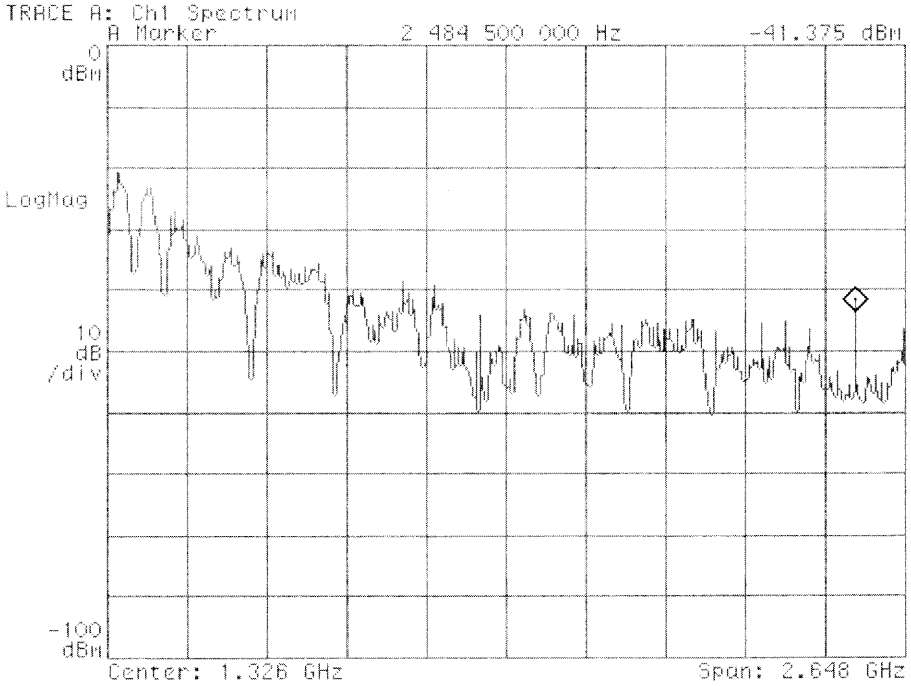

Figure 5.8 All channels were fed with pseudorandom signal, measured at point A.

The spectrum of the signal observed at the end of preamplifier is expected to show discrete frequency components at multiple frequencies of 155 MHz present over a spectrum of 2.5 GHz. In this case when all the channels were fed with the same pseudorandom signals, the absence of these discrete components implies that the signals at the input do not have sufficient differential voltage. Thus, in the next case only half the channels were fed with pseudorandom signal and the rest half were dc biased.

b) Signal measured at point B (Refer Fig 5.7).

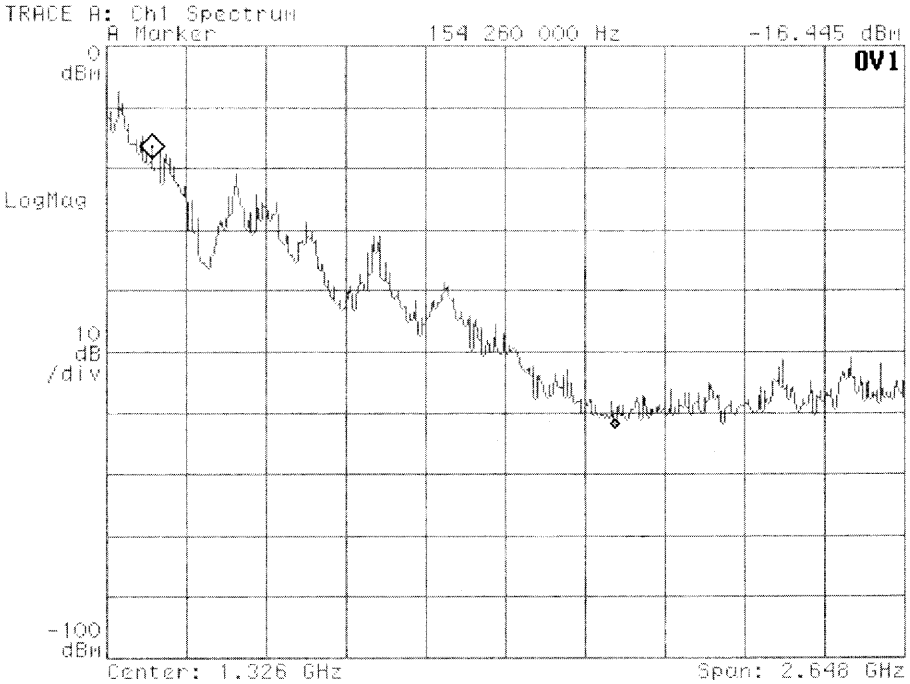

Figure 5.9 All channels were fed with pseudorandom signal, measured at point B.

The above figure shows the signal measured at the end of the link. The LVDS signal converted into a single ended signal is presented and no frequency component is observed at 155.52 MHz because of the improper transmission of the signal.

2. Half the channels were fed with pseudorandom signal and the rest half were dc biased.

a) Signal measured at point A (Refer Fig 5.6).

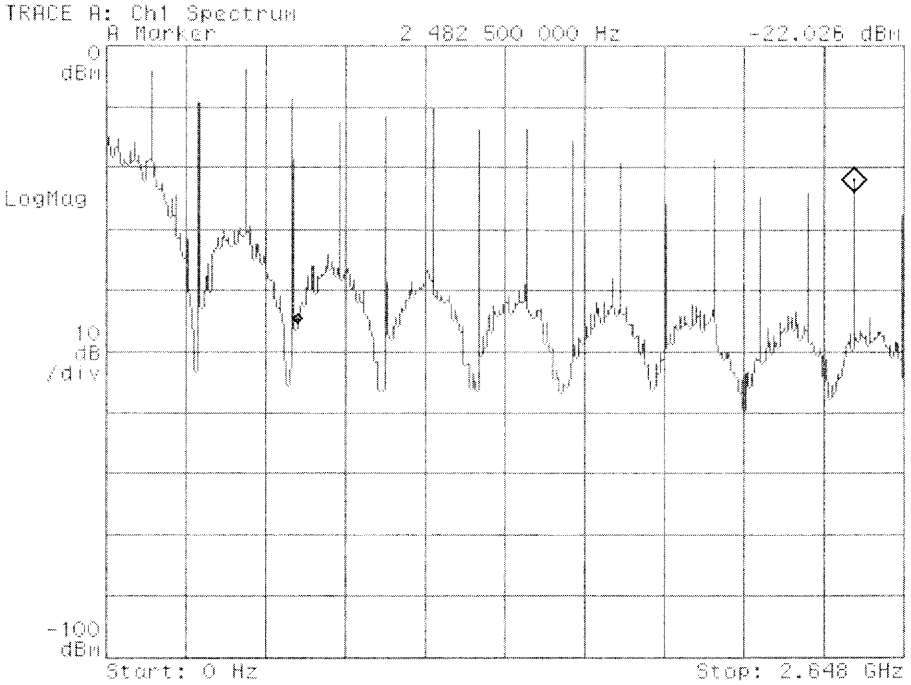

Figure 5.10 Half the channels were fed with pseudorandom signal and the other half are dc biased, measured at point A.

When all the channels were appropriately supplied with a 100mV differential signal; the discrete components of the signals spaced at 155.52 MHz from each other were observed spreading over the entire spectrum ranging from 155.52 MHz to 2.488 GHz. The presence of the pseudorandom signals launched into half of the channels is also evident. (the sinc like spectra between the 155MHz spikes)

b) Signal measured at point B (Refer Fig 5.7).

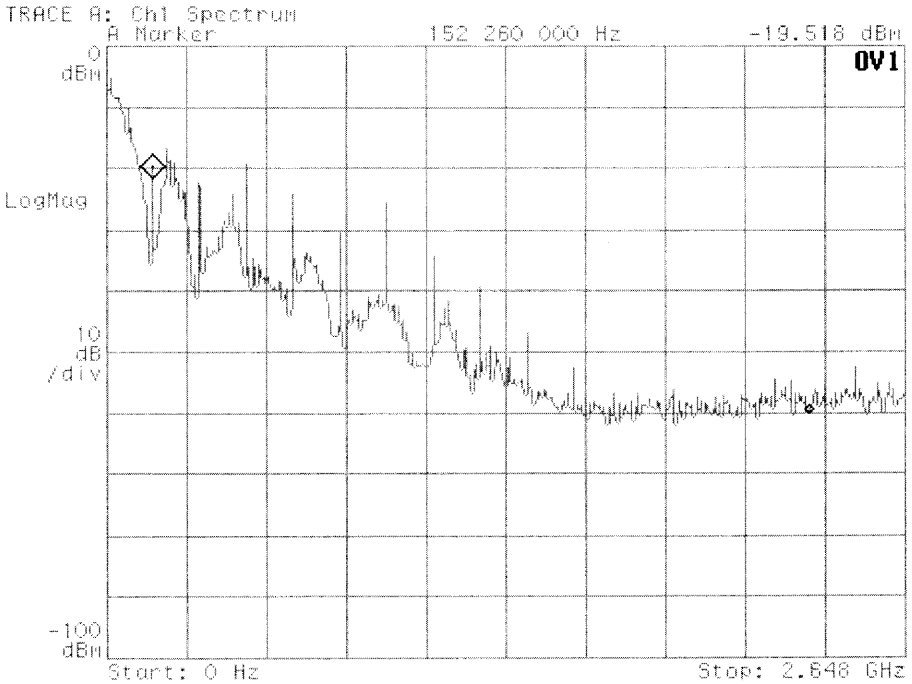

Figure 5.11 Half the channels were fed with pseudorandom signal and the other half are dc biased, measured at point B.

This signal measured at the end of the link has discrete frequency components present marking the presence of signals at the channel. A spike around 155.52 MHz along with a few harmonics is also observed: this indicates the presence of the pseudorandom signal at the particular channel. All the sixteen channels were tested individually to exhibit this pattern. This is point is still under investigation.

3. All channels dc biased.

a) Signal measured at point A (Refer Fig 5.6)

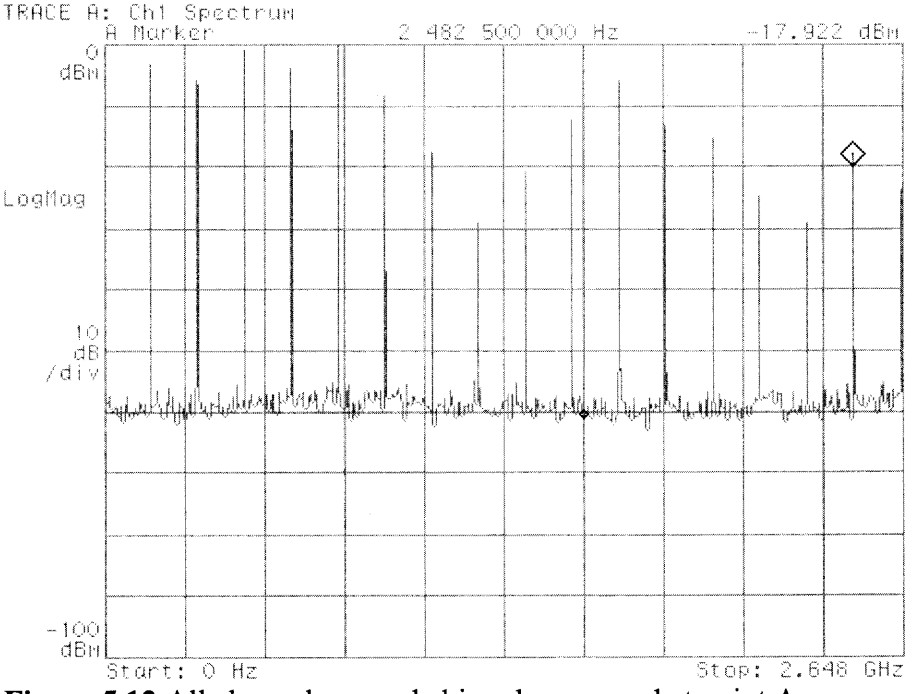

Figure 5.12 All channels were dc biased, measured at point A.

When all the signals were dc biased, there is a significant increase in the signal strength. The absence of pseudorandom signals is marked by the flat spectrum floor. All the frequency components observed in the above figure are spaced at 155.52MHz apart from each other. This spacing of 155.52 MHz is monitored only when a differential clock signal of 155.52 MHz provided to the board.

b) Signal measured at point B (Refer Fig 5.7).

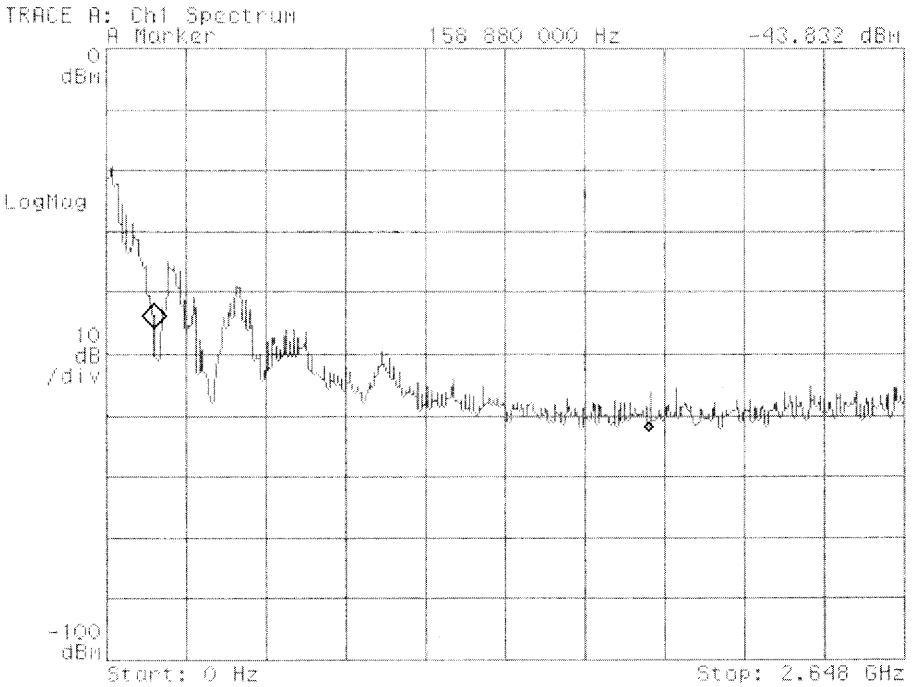

Figure 5.13 All channels were dc biased, measured at point B.

The above figure exhibits a dip at 155.52 MHz which explains that only dc biasing the signals is not enough, there has to be the presence of real differential data for the system to function properly. In the absence of amplification, the transmission was not proper. Therefore, it was concluded that, at this point biasing half the signals and feeding the remaining half with pseudo random signals provided the best results.

While measuring signals through the test link, the same sets of cases were assessed namely all pseudorandom, half biased and half pseudorandom and all DC biased channels. The results of these measurements were compared with the results from previous measurements on the communication link.

1. All channels fed with pseudorandom signal.

a) Signal measured at point A (Refer Fig 5.6).

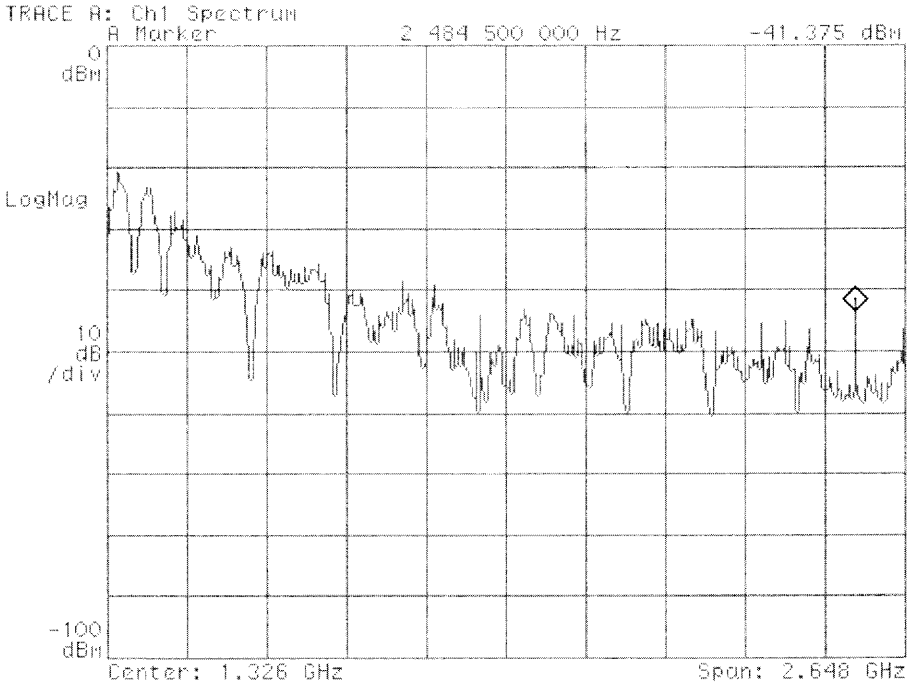

Figure 5.14 All channels were fed with pseudorandom signals, measured at point A.

The spectrum of the signal observed at the end of preamplifier exhibits the absence of discrete frequency components indicating insufficient differential voltage on the input channels.

b) Signal measured at the second point of measurement (Refer Fig 5.7).

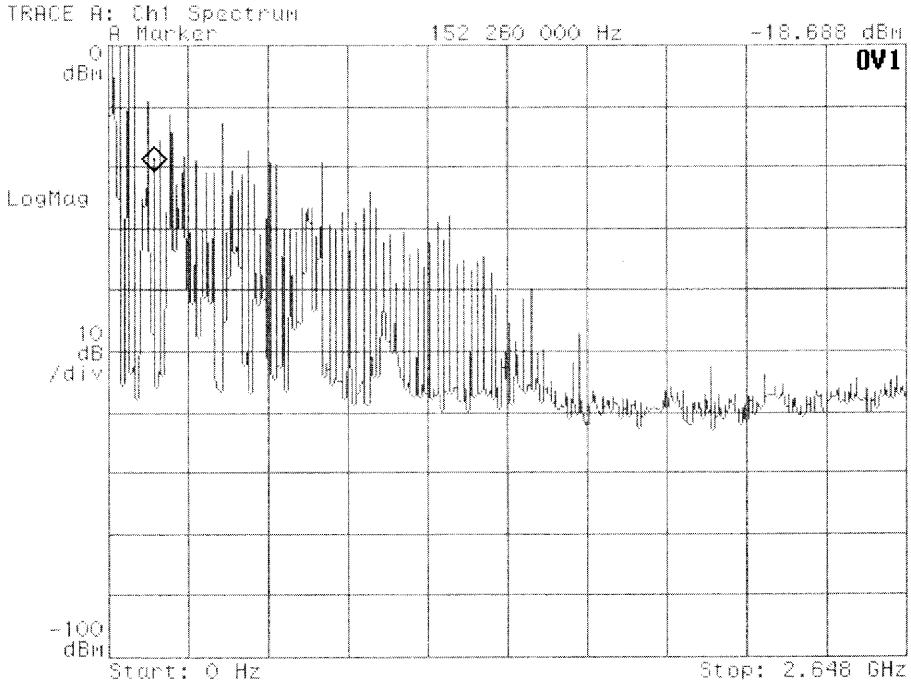

Figure 5.15 All channels were fed with pseudorandom signals, measured at point B.

This signal is measured at the end of the communication link comprising of the transmitter board, receiver board and the LVDS signal to single-ended converter board. The presence of other frequency components is explained by the amplifier present on the link (100-4500 MHz).

2. Half the channels fed with pseudorandom signal and the other half was dc biased.

a) Signal measured at point A (Refer Fig 5.6)

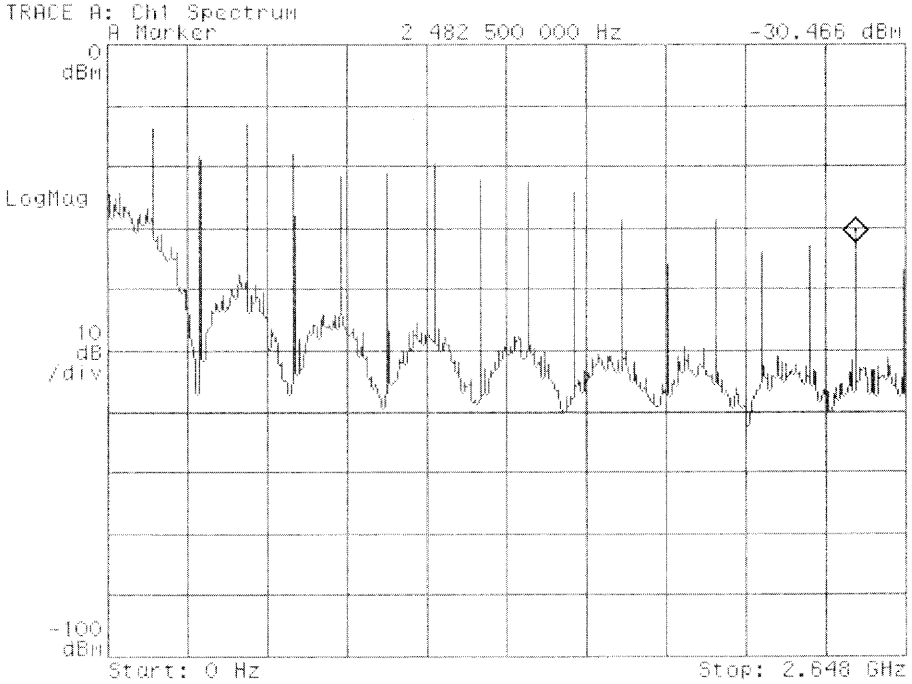

Figure 5.16 Half the channels were fed with pseudorandom signal and the other half are dc biased, measured at point A.

Here all the channels were supplied with a differential voltage of 100mV; half the channels were fed with the pseudorandom signal and the remaining half were dc biased. The spectrum shows the presence of pseudorandom signals.

b) Signal measured at the second point of measurement (Refer Fig 5.7).

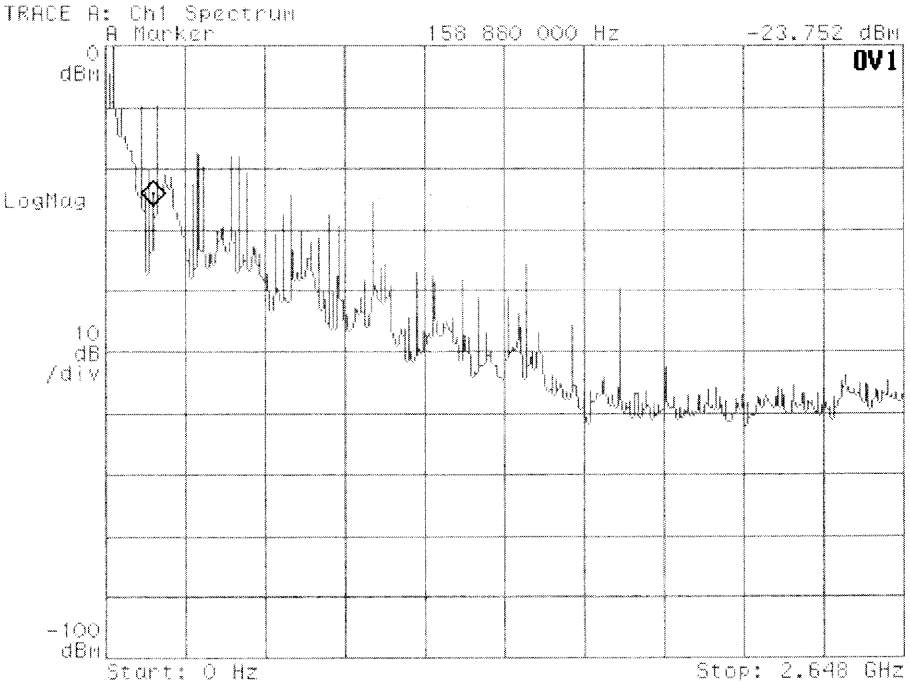

Figure 5.17 Half the channels were fed with pseudorandom signal and the other half are dc biased, measured at point B.

Signal was present around the 155.52 MHz range, when the channels were measured at the end of the communication link. Other frequency components are also seen along with the harmonics of the main signal because of the amplification of the signal before being received by the receiving antenna.

3. All the channels are biased.

a) Signal measured at the first point (Refer Fig 5.6)

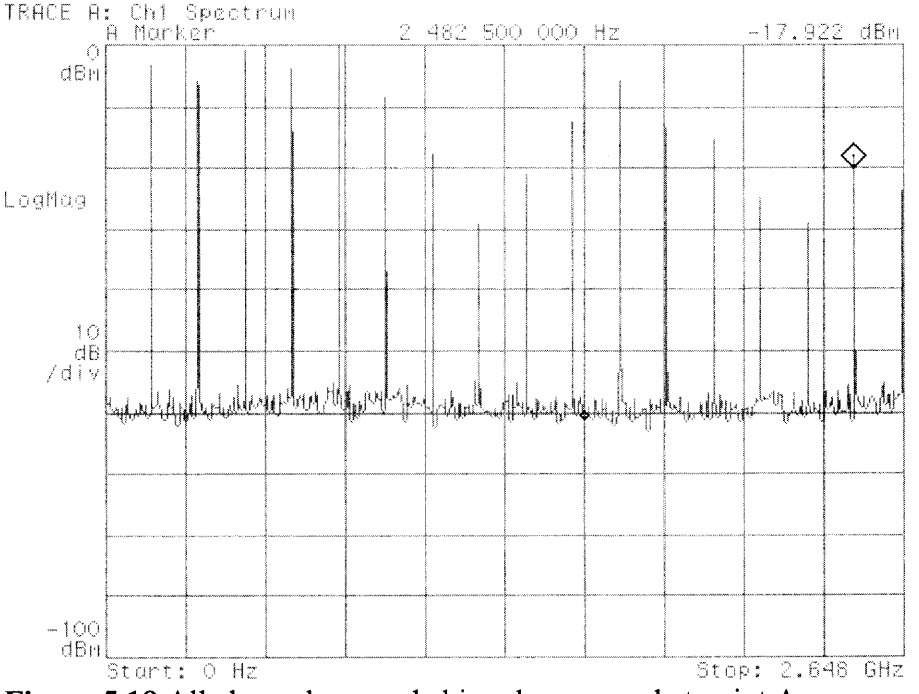

Figure 5.18 All channels were dc biased, measured at point A.

When all the signals were dc biased, there is a significant increase in the signal strength. And the absence of pseudorandom signals is marked by the flat spectrum. All the frequency components observed in the above figure are spaced at 155.52MHz apart from each other. This spacing of 155.52 MHz is monitored by the differential clock signal of 155.52 MHz provided to the board.

b) Signal measured at the second point of measurement (Refer Fig 5.7).

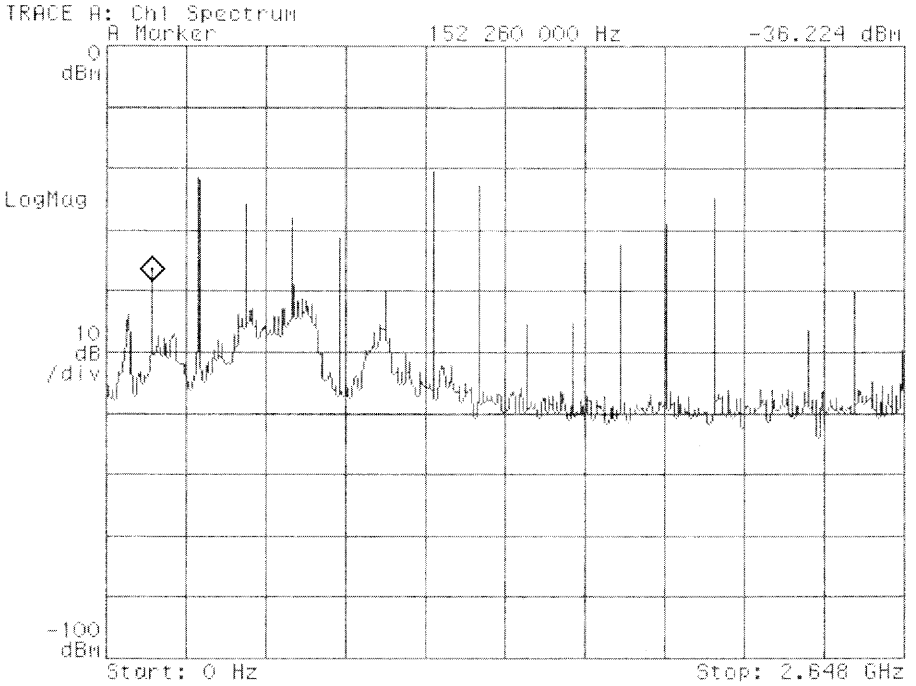

Figure 5.19 All channels were dc biased, measured at point B (Output obtained after amplifying the signal and then passing through the antennas).

Channels measured at the end of the communication link as shown in the figure above exhibits a significant signal present at 155.52 MHz. Some other undesirable frequency components were also present. Again, best results were obtained by feeding half the channels with pseudorandom signals and dc biasing the remaining half.

Verification of the Clock Recovery capability of the Deserializer was made by observing the recovered clock on an oscilloscope. It exhibits a pulse repetition rate of 6ns, corresponding to 155.52MHz.

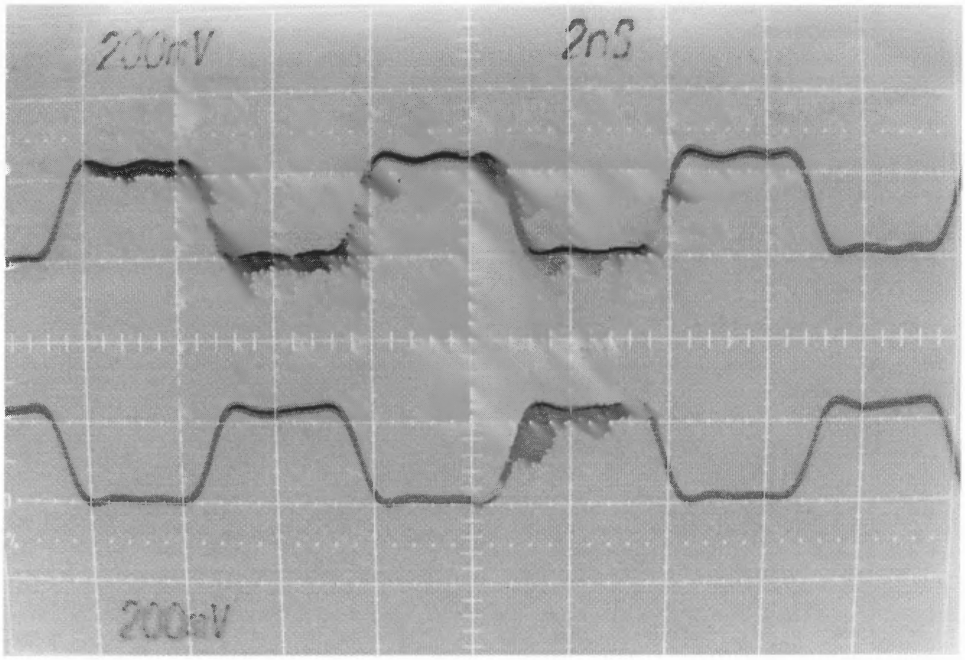

Figure 5.20 Differential clock signal fed to the serializer.

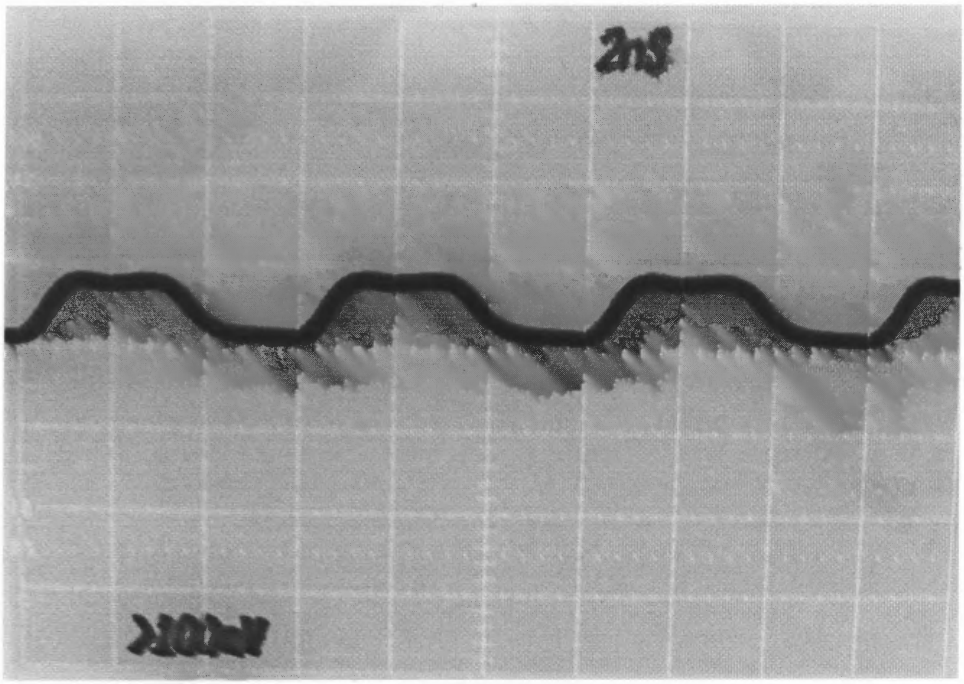

Figure 5.21 Recovered clock signal from deserializer.

When the measurement was taken at the end of the communication link at point B, and the signal viewed on an oscilloscope, following observations were made.

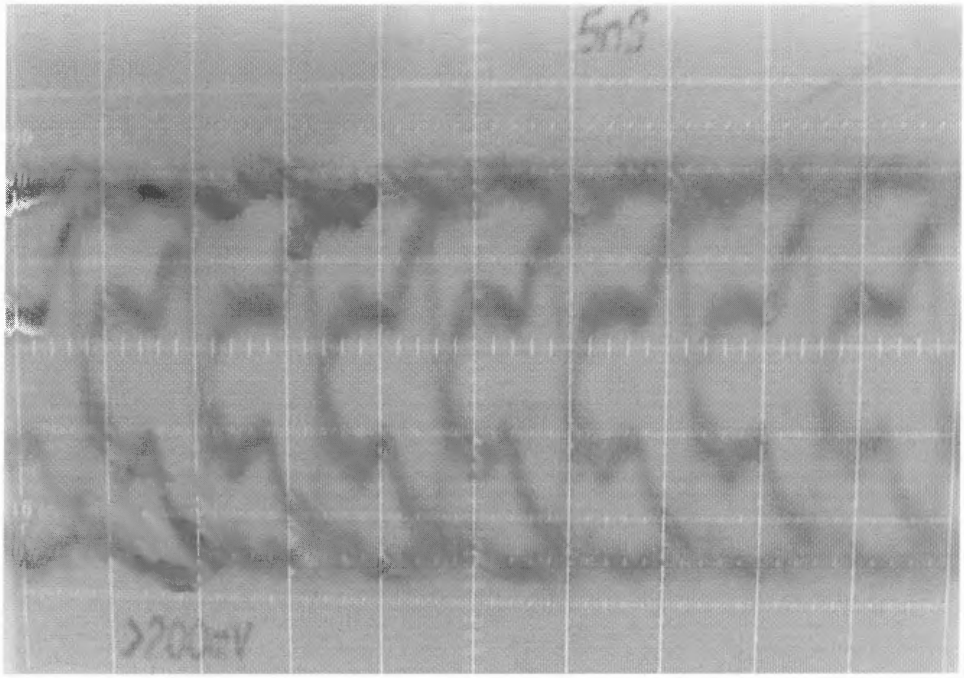

Figure 5.22 Signal observed on one of the receiver channels on the oscilloscope.

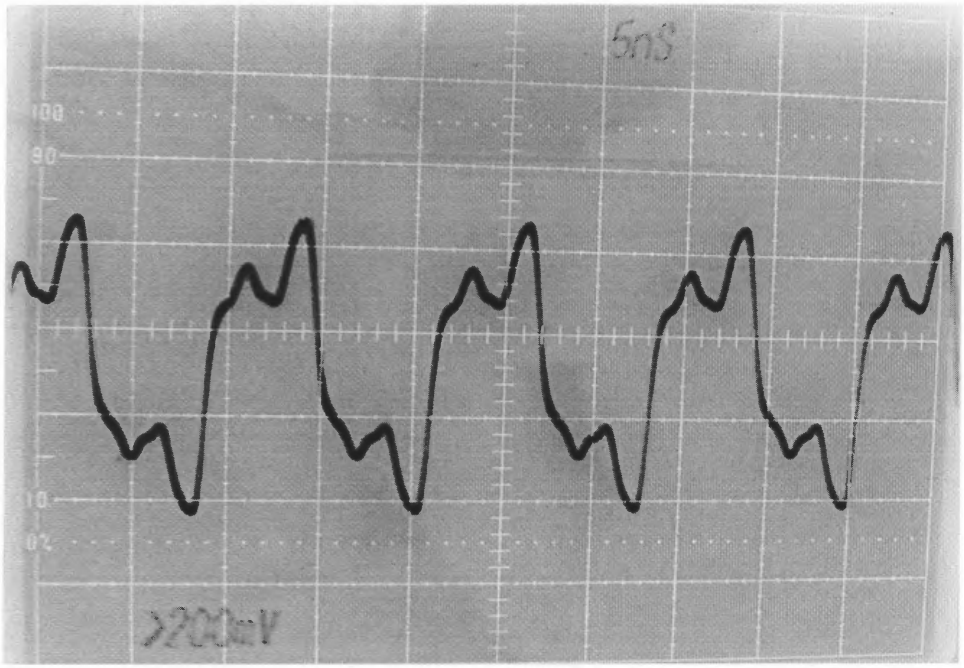

Figure 5.23 Signal observed on one of the receiver channels after disconnecting the transmitter portion. (This signal is present due to the internal clock recovery capability of the board).

5.5 Conclusion

In this experimental project, a communication link was assessed. The design of this link for Ultra Wideband required communication boards that could support high data rate and that could operate at a high frequency range. Maxim boards provided a practical solution with a wide range of options to choose from. The setting up of this link also required careful selection of components, connectors, and cables.

The goal of achieving a successful communication by supplying all the sixteen channels of the transmitter with a pseudorandom signal was not accomplished since after splitting the pseudorandom signals into sixteen, it was observed that the amplitude of the signals had reduced significantly below the 100mV threshold and hence an alternate method was chosen, here the pseudorandom signal was divided only into eight channels while the remaining channels were dc biased. Results were obtained by dc biasing all of the channels as well.

When all the channels were dc biased, a fixed pattern of zeros and ones were created on the channels. As there was no randomness in the input signals (as shown in Figures 5.12, 5.18), the power spectral density of the signals was discrete spectrum with frequency components spaced at 155.52 MHz. This spacing between the signals is because of the differential clock signal also at the rate of 155.52 MHz provided on the board.

When, half of the channels were dc biased and the remaining halves were fed with pseudorandom signals, its corresponding power spectral density exhibited a typical sinc-like distribution in addition to the discrete components observed at 155.52 MHz. The channels were fed with square waves, and the power spectral density of square waves is a

sinc function. This can clearly observed on first measurement point (Figures 5.10, 5.16) where the discrete components are present around the main lobes for each channel. It is also observed at the second measurement point (Figures 5.11, 5.17).

These results were compared to results from a direct serialized LVDS test link to find a complete agreement between the two cases. Thus, in principle the viability of such a communication link was proved.

The antennas used for the testing the communication link was not specifically designed for UWB system. Broadband antenna such as omni directional or log periodic antenna may possess the bandwidth yet lack the transient capability needed for the task. An antenna built in house did fulfill the requirements. A successful communication was achieved by receiving the signals at the same frequency at each of the receiver channels. The diagnostics test points provided on the Maxim boards were used to compare the results obtained through the link and analyze them.

CHAPTER 6

FUTURE WORK

This project can be extended by utilizing antennas that are specifically designed for Ultra Wideband technology. This would provide as a good testing bench for the antennas. Also a bit error generator can be employed to generate pseudorandom signals for the channels to test for actual bit errors.

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