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#### ABSTRACT

### CARRIER TRANSPORT IN Ge NANOWIRES AND ONE DIMENSIONAL SI/Ge HETEROJUNCTIONS

### by Eun Kyu Lee

Ge Nanowires (Ge NWs) on single crystal, (100) and (111) oriented *n*-type Si substrates were grown via the vapor-liquid-solid (VLS) mechanism and studied with respect to their electrical properties.

Using different contact geometries, direct current (DC) and alternating current (AC) electrical and photoelectrical measurements were carried out at room temperature to investigate electrical properties of Ge NWs and Ge NWs/Si substrate one-dimensional (1D) heterojunctions (HJs). A rectifying junction behavior is observed at NWs/substrate interface, but many orders of magnitude greater AC conductance than DC in Ge NW volume is measured at high frequencies. The obtained experimental data are consistent with the result of structural and optical studies and support the conclusion that the Ge NWs/Si substrate interface is nearly defect free while most of the structural defects in the form of twin dislocations are located within Ge NW volume. These defects control optical and carrier transport properties in the Ge NW volume. In addition, the frequency dependent AC conductance shows a power law behavior, suggesting that carrier transport in Ge NW volume is associated with hopping processes.

## CARRIER TRANSPORT IN Ge NANOWIRES AND ONE DIMENSIONAL SI/Ge HETEROJUNCTIONS

by Eun Kyu Lee

A Thesis Submitted to the Faculty of New Jersey Institute of Technology in Partial Fulfillment of the Requirements for the Degree of Master of Science in Electrical Engineering

**Department of Electrical and Computer Engineering** 

August 2004

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## **APPROVAL PAGE**

# CARRIER TRANSPORT IN Ge NANOWIRES AND ONE DIMENSIONAL SI/Ge HETEROJUNCTIONS

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This thesis is dedicated to my beloved parents, Sang-Hoon Lee and Young-Ok Choi.

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#### **CHAPTER 1**

### **INTRODUCTION**

High aspect ratio one-dimensional (1D) nanostructures or nanowires (NWs) are ideal systems for investigating the dependence of structural, electrical, optical and mechanical properties as a function of size and dimensionality. These NWs are expected to play an important role as both, interconnects (e.g., passive) and functional (e.g., active) components in nanoscale electronic and optoelectronic devices.

One of the key features in the NW properties is the quantum confinement effect. The effect of quantum confinement may play a crucial role transforming indirect band gap semiconductors such as Si and Ge into quasi-direct band gap materials, where optoelectronic applications no longer limited by an inefficient, phonon-assisted carrier recombination. The excitonic Bohr radius ( $R_B$ ) in bulk Ge is 24.3 nm, resulting in a more prominent quantum size effect compared to Si with  $R_B = 4.9$  nm [1]. In addition, there is a relatively small difference of ~ 200 meV between fundamental, indirect band gap and the first direct band gap in bulk Ge. Other interesting phenomena related to an increase in Ge NW carrier mobility due to band structure modifications are also very interesting for device applications [2].

In this thesis, I present detailed studies of Ge NWs fabricated on single crystal Si substrates produced by the method named vapor-liquid-solid (VLS) growth [3]. In the second chapter, I will discuss several possible fabrication procedures and NW structural, optical, electrical and mechanical properties using mostly the published data. The original part of this thesis is focused on electrical properties and carrier transport in a

one-dimensional heterostructure, e.g., a hetero-junction between a Si substrate and Ge NWs. I will present DC and AC electrical and photoelectrical measurements, and will discuss in details the admittance spectroscopy data in a wide range of frequencies from 10 to 10<sup>7</sup> Hz. I will show that these electrical measurements correlate with the optical measurements recently obtained in Prof. Tsybeskov's group. My data support the conclusion that Ge NWs/Si substrate interface is nearly defect free while most of the structural defects in the form of twin dislocations are located within a Ge NW volume. In the case of non-passivated NW surfaces, these defects control optical and carrier transport properties in Ge NWs.

#### **CHAPTER 2**

### BACKGROUND

### 2.1 Vapor-Liquid-Solid and Other Mechanisms of NW Growth

A critical issue in the study and application of NWs is how to assemble individual atoms into such a unique one-dimensional (1D) nanostructure in an effective and controllable way. A general requirement for any successful preparative methodology is to be able to achieve nanometer scale control in diameter during anisotropic crystal growth while maintaining a good overall crystallinity.

During the past decade, many methodologies have been developed to synthesize 1D nanostructures. Generally, they can be categorized into two major approaches based on the reaction media which were used during the preparation: solution and gas phase based processes. More detailed description includes several major techniques as the following:

- (a) Template-directed synthesis represents a convenient and versatile method for generating 1D nanostructures. In this technique, the template simply serves as a scaffold against which other kinds of materials with similar morphologies are synthesized. These templates could be nanoscale channels within mesoporous materials or porous alumina and polycarbonate membranes, etc. The produced NWs can then be released from the templates by selectively removing the host matrix.
- (b) Solution-liquid-solid (SLS) method has been used to obtain highly crystalline semiconductor NWs at low temperatures, e.g., for the growth of InP, InAs, and GaAs nanowhiskers. This approach uses simple, low-temperature (less than or

equal to 203 °C), solution phase reactions. The materials are produced as near-single-crystal whiskers having widths of 10 to 150 nanometers and lengths up to several micrometers.

- (c) Lately, solvothermal methodology has been extensively examined as one possible route to produce semiconductor NWs and nanorods. In these processes, a solvent was mixed with certain metal precursors and possibly a crystal growth regulating or templating agent such as amines. This solution mixture was then placed in an autoclave kept at relatively high temperature and pressure to carry out the crystal growth and assembly process. This methodology seems to be quite versatile and has been demonstrated to be able to produce many different crystalline semiconductor nanorods and NWs.
- (d) A well-accepted mechanism of NW growth via gas phase reaction is the so-called vapor-liquid-solid (VLS) process proposed by Wagner in 1960s during his studies of single-crystalline whisker growth [4]. According to this mechanism, the anisotropic crystal growth is promoted by the presence of liquid alloy/solid interface. This process is illustrated in Figure 2.1 for the growth of Ge NW using Au clusters as catalyst at high temperature.



**Figure 2.1** Au-Ge phase diagram showing three states along the isothermal line; (I) alloying, (II) nucleation and (III) axial growth [3].

In VLS, a metal particle is used as a catalytic nucleation site during the growth of semiconductor NWs. Various metals, such as Au, Fe, Ti, and Ga, catalytically enhance the growth of NWs. A phase diagram of these metal-semiconductor alloys determines the eutectic temperature, and the growth temperature is set in between the eutectic point and the melting point of the materials. However, the growth temperature can be lower than the eutectic temperature reported on the binary phase diagram; the equilibrium melting point of solid decreases with decrease in the size of its particle (Gibbs-Thomson effect).

For Au-Ge system, eutectic temperatures as low as ~360 °C (Figure 2.1) enable low temperature synthesis of Ge NWs, which is likely to give possible future advantage of easy incorporation with existing semiconductor electronic devices. It is already shown that Au-Ge chemical vapor deposition by Au-catalyzed decomposition of GeH<sub>4</sub> source gas is possible even below the eutectic temperature, 360 °C [5]. A temperature given, NWs grow passing three states as described in Figure 2.1 by the arrowed line from left to right through the phase diagram. The decomposition reaction can be expressed as below.

$$GeH_4 \xrightarrow{Au} Au-Ge(l) + 2H_2(g)$$

The mechanism of VLS growth mode for Au-catalyzed Ge NWs begins with a formation of a eutectic alloy between Au particle and Ge. Au particles are usually prepared by evaporating Au film onto Si wafer, which acts as catalytic sites for NWs growth. The catalytic reaction forms a very thin, Ge-rich layer on the surface of the Au-Ge alloy particle at the growing end of the wire. The excess Ge near the surface results in a concentration gradient that causes the excess Ge to diffuse to the Au-Ge island. The excess Ge is likely to precipitate (nucleate) usually at the alloy/solid interface.

According to the reference [6], this process can be explained with respect to energy conservation law as the following. In order to form macroscopic quantities of Ge on the free surface of the Au-Ge alloy, an additional interface must be formed, probably increasing the energy of the system. On the other hand, if the excess Ge diffuses to the underlying Au-Ge and Ge interface, it can attach to the Ge there without requiring an additional interface to form, and the energy of the system does not need to increase. As the Ge atoms precipitate on the underlying Ge, the Ge-Au island is pushed up, forming a wire. Transport of excess Ge from the alloy surface is accommodated by bulk diffusion through the alloy particle or surface diffusion around it on its surface, and Ge could reach the growing NW along the interface between the alloy particle and the NW. Figure 2.2 is the schematic representation of Ge NW growth mechanism.



Figure 2.2 Schematic representation of NW growth mechanism.

The supersaturation and following precipitation on the growth interface depends on the diameter of NW. The Gibbs-Thomson equation places a lower limit on the diameter of structures for thermal growth [7]. The growth rate of NWs is lower for smaller diameter and a critical diameter is found below which the growth stops completely [7]. However, the lower limit for the wire diameter decreases for increasing gas pressure, i.e., higher pressure increase the NW growth rate. An increased source gas pressure appears to enhance the catalytic growth process.

To allow wire growth, transport of Ge away from the surface must not be the slowest process. If neither bulk nor surface diffusion is adequately rapid, the Ge decomposing on the surface covers the catalyst particle. The incoming gas is then shielded from the particle so that the particle cannot continue catalyzing the decomposition, The growth rate then slows to the normal Ge growth rate on Ge, the surrounding Ge grows at the same rate as that of the Ge above the nanoparticle, and no wires form. As metal-containing liquid nanoparticles move along with the tip of the wire, Ge NWs grow.



**Figure 2.3** In situ high temperature TEM images during the growth of Ge NW. (a) Au nanoclusters in solid state at 500 °C, (b) alloying initiated at 800 °C, at this stage Au exists mostly in solid state, (c) liquid Au/Ge alloy, (d) the nucleation of Ge NW on the alloy surface, (e) Ge NW grows with further Ge condensation and eventually forms a wire (f) [8].

Figure 2.3 shows the real time sequential pictures of Ge NWs synthesis taken by in situ high temperature TEM performed by Wu et al. [8], which corroborate interpretation of NWs synthesis by VLS mechanism. Three stages mentioned before, (I) alloying , (II) nucleation and (III) axial growth, are well matched with the pictures (a) to (c), (d), and (e) to (f), respectively. Before Ge vapor applied, Au particles remain in solid state. Wu et al. observed that Au particles kept their state up to 900 °C. With increasing amount of Ge vapor on the surface of Au particle, Ge condenses, diffuses and forms an alloy with Au

particle and then liquefies as the Ge fraction increases in the alloy. In Figure 2.3 (a) to (c), the tendency of increase in size of the alloy droplet and decrease in elemental contrast indicate that, while the alloy composition changes with the increase of Ge fraction, the droplet undergoes the transition from a bi-phase region of solid Au and Au-Ge liquid alloy to a single phase region of Au-Ge liquid alloy. With further concentration of Ge in the Au-Ge alloy droplet, the precipitation of Ge after diffusion to the interface between the liquid alloy and the solid lead to the beginning of NW nucleation (Figure 2.3 (d)). After the Ge nanocrystal nucleates, further transport of the Ge vapor into the system increases the amount of Ge precipitation from the alloy (Figure 2.3 (e)). The interface is then pushed up to form NWs (Figure 2.3 (f)).

#### 2.2 Characterization of NWs

### 2.2.1 Structural Characterization

Mostly, structural characterization of NWs is performed by a combination of scanning electron microscopy (SEM), transmission electron microscopy (TEM), X-ray diffraction (XRD) and electron diffraction (ED). While TEM and SEM provide actual image of structure, XRD and ED helps quantitative analysis of it. Through structural characterization, it is also possible to investigate the growth mechanism.

Figure 2.4 (a) and (b) show a high resolution transmission electron microscopy (HRTEM) image of a Si NW and a SEM image of a Ge NW grown by VLS, respectively. Straight NWs shows high crystallinity. It is also seen that the outer layer of Si NW are surrounded with native amorphous  $SiO_2$ ; an oxide layer is characteristic of Si NWs and Ge NWs.



**Figure 2.4** (a) HRTEM image of a portion of Si NW [7] and (b) SEM image of a Ge NW [9].

Sometimes, amorphous worm-like NWs or 3D nanorods structure are formed at different growth conditions. When source gas decomposition and diffusive transport of it through or on the catalyst particle is so fast, then the transport supplies source material at a higher rate than the crystallization rate for a given diameter, resulting in amorphous NWs [7]. TEM image of an Au-catalyzed Si NW grown by plasma enhanced CVD shows that increased growth rate, which is accommodated by radio-frequency plasma, causes amorphous growth (Figure 2.5 (a)). However, 3D nanorods can form instead of NW when the decomposition is faster than transport as was already mentioned at section 2.1 or diffused material can not effectively surmount chemical potential barrier at the liquid eutectic-solid interface (the energy barrier for nucleation and for growth of NWs, in VLS this barrier provides rate limiting step for NW solidification), e.g., due to a low source gas pressure (Figure 2.5 (b)) [10].



**Figure 2.4** (a) HRTEM image of a portion of Si NW [7] and (b) SEM image of a Ge NW [9].

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Figure 2.5 (a) TEM image of a amorphous Si NW [7] and (b) SEM image of Ge nanorods [10].

Defects in the highly crystalline NW likely to create different crystal planes during growth, causing the shape of wire kinked [6, 9]. Kinks can be observed at sharp angles in NWs. These kinks are likely to be related especially to dislocation defect. Qiang Tang et al. [9] made an explanation of the origin of kinks by twin dislocation formation during the growth (Figure 2.6 (a) and (b)). In their theory, twin dislocation defect form due to lattice mismatch between catalyzing islands and NWs. Figure 2.6 (b) is TEM image of Si NW grown by molecular beam epitaxy using TiSi<sub>2</sub> catalyst and Si<sub>2</sub>H<sub>6</sub> gas source. The growth process can be explained by VLS except for the situation that the catalyzing islands remain in solid state during the growth different from VLS situation wherein they are in the liquid state, reducing the stress at the island-Si interface. The strain from the lattice mismatch of  $\sim 6$  % between Si NW and TiSi<sub>2</sub> island forms a twin crystal during the growth, which dominates the growth direction resulting in formation of kinks.



**Figure 2.6** TEM image of Si NWs containing twin crystals. (a) A short Si NW and (b) Si NW with a kink. In (b), the insets are the enlarged Si crystal image at position 1, 2, and 3. The white lines corresponds to (111) planes. Si lattice at 1 is twin to that at 2, which is twin to that at position 3 [9].

Figure 2.6 (a) shows a Si NW growing toward the right-hand side, in which a twin crystal is starting to develop at its lower edge and a highly defected Si crystal containing stacking faults is being formed at the upper edge. At initial stage, the lattice stress at the interface between TiSi<sub>2</sub> islands and Si causes the Shockley partial dislocation at the edge of TiSi<sub>2</sub> islands, where the stress is highest and the starting of dislocation is easiest, and then, it glides along Si {111} planes. As the partial dislocation glides through every parallel {111} plane, a twin crystal forms; otherwise, a highly defective crystal full of stacking faults forms. After the twin is formed, it grows along with the NW. When the twin is large enough to dominate the growth, the wire changes to a new growth direction dominated by

the twin crystal, resulting in a kink. The twinning process can happen several times during the NW growth. Therefore, the NW can change growth direction several times, leaving large amounts of twinned regions in the NWs.

Compared to electron microscopy, X-ray and electron diffraction can give complementary quantitative information about the structure. Diffraction technique is the method that permits the direct identification of any crystalline material based on their unique crystal structure.



**Figure 2.7** (a) SAED pattern of a single Si NW and (b) XRD spectrum of Si NW arrays [11].

In X-ray diffraction (XRD) technique, the intensity of the diffracted X-rays is measured as a function of the diffraction angle, and the material's orientation. Electron diffraction (ED) technique, since the diffracted electron beams have a high intensity and exposure times are in the order of a few seconds, enables the patterns to be directly observed on the viewing screen of the electron microscope. Furthermore, diffraction patterns can be obtained from very small crystals selected with a diffracted aperture (Selected Area Electron Diffraction or SAED) and by a focused electron beam even from nm-sized regions (Convergent Beam Electron Diffraction or CBED).

Figure 2.7 is SAED pattern and XRD spectrum of Si NWs arrays synthesized by CVD template method with an alumina template [11]. A single Si NW is taken for SAED. It can be seen that the diffraction spots are organized in a precise hexagon or parallelogram, indicating that the diamond lattice structure of bulk Si is preserved in the Si NWs. The pattern shows that each single Si NW is a single crystal. From the XRD results, the arrays of Si NWs show a polycrystalline structure and the result conflicts with the SAED data above. Considering statistical nature of XRD pattern and the diffraction pattern of different grains indicate different orientations, it can be proposed that these individual Si NW is essentially single crystal and Si NWs in an array has a different crystal orientation.

### **2.2.2 Optical Characterization**

Raman scattering and photoluminescence (PL) measurement are usually done for the optical characterization of NWs. Intensity and emission peaks in measured spectra gives direct information about the material properties. Raman peaks of well-defined phonons in single crystal semiconductor are very sharp. Raman spectroscopy is a suitable tool for investigating the phonon confinement effect of nanomaterials. The peak-position shift, broadening, and asymmetry of the Raman bands are characteristic of NWs.

The small physical dimension of the scattering crystalline NWs leads to a downshift and broadening of the first-order Raman line through a relaxation of size-dependent momentum vector selection rule [12]. Because the NWs are only

two-dimensionally confined crystals, there is a momentum k = 0 along their axis direction. Hence, the zone-center phonons allow for the Raman scattering to occur at the original peak position. However, in the direction perpendicular to the axis of NWs, nonzero k phonon dispersion may participate in Raman scattering and lead to both a peak broadening and an extension of the Raman peak towards low frequencies. Raman scattering is very sensitive to the lattice structure and crystal symmetry of microcrystalline materials. When the core diameter of a NW is small, the Raman peak width increases and becomes more asymmetric with an extended tail at low frequencies. Figure 2.8 (a) is Raman spectra of bulk Ge and Ge NWs measured by Y.F. Zhang et al [12]. The first-order Raman spectra in bulk Ge at 298.5 cm<sup>-1</sup> is symmetric with a full width at half maximum (FWHM) of 7 cm<sup>-1</sup>. Raman scattering from the Ge NW sample with diameters of 36~83 nm shows a peak at 298.5 cm<sup>-1</sup> that is slightly broadened (a FWHM of 10 cm<sup>-1</sup>) and asymmetric. Raman spectrum of Ge NWs with diameters ranging from 12 to 28 nm is peaked at 293 cm<sup>-1</sup>, asymmetric with a FWHM of 21cm<sup>-1</sup> and has an extended tail at low frequencies.

Figure 2.8 (b) shows Raman spectrum of Si NWs on Si substrates prepared by Mei Lu et al [11]. The peak located at ~513 cm<sup>-1</sup> is originated from the scattering of the first order optical phonon mode (TO) of Si, which corresponds to the TO mode peak of Si, 520 cm<sup>-1</sup> [13]. The full width at half maximum (FWHM) of the TO mode is broadened to ~18 cm<sup>-1</sup> from the typical value 3~5 cm<sup>-1</sup> of bulk Si [14]. They ascribed the downshift and larger FWHM to the quantum confinement effect caused by the small diameters, unique shapes and high surface-to-volume ratio of Si NWs. In addition, there are two broad peaks at ~286 cm<sup>-1</sup> and 920 cm<sup>-1</sup>, which are due to the scattering of the second order transverse acoustic phonon mode (2TA) and the second order optical phonon mode (2TO),

respectively. It is also found that the two broad peaks are down-shifted from the value  $\sim$ 300 cm<sup>-1</sup> and 970 cm<sup>-1</sup> and relative intensities increase as compared with those of 2TA and 2 TO mode of Si. These properties are typical of crystalline Si NWs [15].



Figure 2.8 Raman spectra of (a) (1) bulk Ge, and Ge NWs with diameters of (2) 36-83 nm and (3) 12-28 nm [14] and (b) Si NWs [11].

PL spectrum modification due to quantum confinement in undoped Si has been reported besides those due to phonon assisted excitonic recombination characteristic for bulk indirect bandgap Si (Figure 2.10 (a)) [16]. A typical low-temperature PL spectrum from a Si crystal containing low concentration of shallow phosphorus atoms is shown in Figure 2.9, which consists of the bound-exciton no-phonon (NP) transition and their phonon replicas, TA and TO, at lower energies [17]. Due to the indirect nature, the radiative recombination of electron-hole pairs in Si requires creation of a phonon with a certain k value to conserve momentum. On the other hand, in doped Si, it is possible for the bound electron-hole pair to recombine without phonon participation because impurity

itself transfers the momentum in NP transition. In general, the NP line is weak and even forbidden in intrinsic bulk silicon. The intensity ratio of the NP line to the phonon replicas depends strongly on the binding energy and the type of impurity and are different for materials In Si, coupling to TO phonon is strongest followed by the coupling to TA phonons. In Ge, LA and LO phonon replicas are favored.



**Figure 2.9** Low-temperature PL from Si crystal containing  $2 \times 10^{14}$  cm<sup>-3</sup> phosphorus atoms [17]. At the top of each peak, no-phonon transition (NP) and phonon-participating transition (TA and TO) are specified. 100  $\mu$ , 300  $\mu$ , 450  $\mu$  and 1000  $\mu$  indicate spectral resolution gain.

Z. G. Bai et al. observed three emission bands in the red, green and blue regions from the oxidized Si NWs and found out that as the core size of Si NWs decreases with additional oxidation time, especially the red peak intensity increases much faster than the other two (Figure 2.10). They proposed that the green and blue bands are attributed to recombination from the defects centers in oxidized layer and the quantum confinement results in both the blue shift of the energy gap and a transition from the indirect towards the direct gap, which in turn dramatically increase the efficiency and intensity of red PL and cause the blue shift of red PL.



Figure 2.10 (a) PL spectra of Si NWs [16] and (b) ball-milled Si nanocrystals [18]. In (a), oxidation conditions are (1) 900 °C, 30 min; (2) 700 °C, 15 min; (3) 700 °C, 10 min and (4) 700 °C, 5 min

Figure 2.10 (b) is PL spectra of ball-milled Si nanocrystals (average diameter d = 100 nm) and bulk Si at T = ~ 4 K obtained by B.J. Pawlak [18]. D1 in Figure 2.10 (b) is a band related to dislocations in Si nanocrystal due to fabrication process. There were some indications of confinement effect in the investigated silicon nanocrystals. First, the ratio between NP transition and its replica is significantly different from the ratio usually found for bulk material. Second, they also found from their experiments that this excitonic lines up-shifted with diminishing grain diameter, leading to conclusion that these were associated with band structure perturbation due to size-confinement.

### 2.2.3 Electrical Characterization

Much useful information about NWs such as doping status and transport mechanism can be obtained by studying the electrical characterization. However, little has been reported regarding electrical characterization compared with structural and optical properties. To date, most of electrical characterizations are performed through the investigation of single NW.



Figure 2.11 SEM image of three terminal Si single NW device, with the sorce (S), gate (G), and drain (D) labeled [19].

Figure 2.11 is an SEM image of a Si NW device produced via VLS growth with Au particles for the electrical measurement carried out by a group of Sung-Wook Chung et al. [19]. A gate electrode is used to vary the electrostatic potential of a NW while measuring current versus voltage of the NW. The change in conductance from I-V curves of Si NW as a function of gate voltage can be used to distinguish whether a given NW is *p*-type or *n*-type since the conductance will vary oppositely for increasing positive (negative) gate voltage.
They found out that the NWs were *p*-doped even before annealing and the comparison between the devices before and after thermal annealing (as indicated in figure 2.12 (a) and (b)) led them to the conclusion that thermal treatment of the device resulted in better electrical contacts. From the I-V curves in Figure 2.12 (c), metallic-like curve, which has shown no gate-voltage effect up to  $V_G = \pm 40$  V, indicates that diffusion of dopant atoms from Au contacts heavily doped the NWs during the thermal treatment; the diffusion coefficient of Au in Si at 750 °C is sufficient to heavily dope the entire wire with Au.



**Figure 2.12** (a) Three terminal transport measurement of Si NW device with Al contacts without annealing (a) and after annealing at 550 °C (b). (c) I-V characteristics of Si NW with Ti/Au contacts, before (solid line) and after (dashed line) annealing at 750 °C for 1h [19].

Because nonlinear I-V curve indicates that metal/NW contact is characterized by a non-ohmic Schottky barrier, this measurement could not directly give the intrinsic

resistance of the NW without the knowledge of the contact resistance due to the metal/NW junction.

The first demonstration of intended and controlled doping of Si NWs and the characterization of the electrical properties of these doped NWs was achieved by Yi Cui et al. [20]. They doped Si NW during the growth by incorporating dopants in the reactant flow and their estimates of the carrier mobility made from gate-dependent transport measurements were consistent with diffusive transport and showed an indication for reduced mobility in smaller diameter wires due to the enhanced scattering in the smaller diameter NWs.



**Figure 2.13** (a) I-V curves of Ge NWs at different temperatures and (b) Linear resistance dependence on the temperature, where diamonds are experimental data and the solid line is the fitting curve according to the thermal fluctuation-induced model [1].

Thermal scanning of resistance of individual NW also can be used for the study of transport mechanism. Figure 2.13 (a) and (b) are the I-V curves and temperature dependent

resistance curve measured on individual Ge NWs grown by Au-catalyst particle with Au contacts [1].

At temperatures higher than 100K, linear current dependence on voltage indicates ohmic contacts between Ge NW and Au contacts. From the temperature dependence of the linear resistance at small bias voltage (figure 2.13 (b)), G. Gu et al. found out that the resistance data could be fitted well with the fluctuation-induced tunneling model in heavily doped Ge NWs with Au atoms which could serve as both *p*-type and *n*-type dopants in Ge NWs.

### CHAPTER 3

### EXPERIMENTAL

Ge NWs/Si substrate HJ samples for this study were grown via the VLS technique using low pressure chemical vapor deposition by the collaborating group at Hewlett-Packard Research Laboratories [5]. The samples were prepared on (100) and (111) oriented Si substrates and found out to have different structural [5] and optical [21] properties, which will be described in the first section of this chapter.

Measurements were carried out by preparing contacts on the samples with different configurations for a comparison, and direct current-voltage (I-V) measurement and AC admittance spectroscopy were applied for the electrical characterization of Ge NWs/Si substrate HJs. All data were measured by KEITHLEY 6517A electrometer and HP 4192A impedance analyzer and recorded by a PC connected to them. Electrical measurements under illumination were also carried out. Detailed measurement setup regarding apparatus arrangement, experimental procedure and specifications are described below in this chapter. Especially, one section is devoted to a description of auto-balancing bridge circuit theory which is adopted in HP 4192A impedance analyzer.

### **3.1 Samples and Contacts**

#### 3.1.1 Ge NWs/Si Substrate HJ Samples

The description of the sample preparation entirely refers to the references [5, 21]; structural and optical characterization data of as-grown Ge NWs were obtained with the samples

fabricated in the same facilities. Particularly, the optical characterization was performed in Prof. Leonid Tsybeskov's group, and these results are subjects for the oncoming paper.

CVD by Au-catalyzed decomposition of GeH<sub>4</sub>, has been used to grow Ge NWs on single crystal silicon. First, 20-nm-diamter nanoparticles as catalyst were deposited by dispersion of Au aqueous suspension onto cleaned (100) and (111) Si substrates and subsequent drying. The density of nanoparticles in aqueous suspension was  $7 \times 10^{11}$ /mL. The suspension contained less than 0.01 % of HAuCl<sub>4</sub>. Substrate cleaning via 5% HF/H<sub>2</sub>O was performed before the deposition of Au particles to remove surface oxide layer and obtain H-termination accompanied by minimal deionized water rinsing; it is known that the NWs direction loses preferential orientation during the growth due to the high growth rate and the oxide layer screening the substrate orientation [7].

After inserting the substrates into the lamp-heated CVD reactor, they were annealed at ~650 °C in H<sub>2</sub> at a pressure of 12.6 kPa for 10 min to remove surface contamination from the nanoparticles and to enhance contact to the Si substrates, which would contribute to the NWs adopting the orientation of the substrates during the growth.

Then GeH<sub>4</sub> was introduced into the chamber after temperature was reduced to  $320^{\circ}$ C. The length of the grown Ge NWs increased approximately linearly with the deposition time. The typical diameter of the wires were 40 nm and the samples were prepared with different length of 360, 710, and 1400 nm, which depended on the deposition time 9, 18, and 36 minutes, respectively.

Finally, the samples were cooled in  $H_2$  and then  $N_2$  to < 200 °C to minimize oxidation of the wire surface.



**Figure 3.1** SEM image of Ge NWs (a) on (100) Si substrate and (b) on (111) Si substrate [5].

Figure 3.1 is an SEM image of the as-grown GeNWs, where both the Ge NWs on (100) and (111) oriented Si wafers have the same <111> preferential growing direction, i.e., on (100) Si substrate, most of NWs grow at an angle of  $\sim55^{\circ}$  to the substrate (Figure 3.1 is a view in a <110> direction which is perpendicular to Si substrate normal), which corresponds to <111> direction, and on (111) Si substrate, they grow in the direction perpendicular to the substrate, the same <111> direction. The preferential growth direction and structural investigation show that NWs are highly crystalline. However, in the SEM image, some twin dislocation related kinks are seen.

By optical characterization of the Ge NWs on Si substrate, additional information was obtained. Raman and low temperature PL spectra of Ge NWs on Si substrate are shown in Figure 3.2 (a) and (b), respectively.



**Figure 3.2** (a) Raman spectrum of the Ge NWs with an estimated NW length of 360 nm grown on a (111) Si substrate and (b) Low temperature PL spectra of c-Si, Ge NWs grown on (100) and (111) Si substrates [21].

In the Raman spectrum of Ge NWs on (100) Si substrate, there are only two clear Raman peaks originated from Si substrate and Ge NWs, respectively; Si-Si vibrations at ~520 cm<sup>-1</sup> and Ge-Ge vibrations at ~300 cm<sup>-1</sup>. Fully symmetric and narrow FWHM of ~6 cm<sup>-1</sup>, which is comparable with that of the bulk Ge, provides an additional proof that Ge NWs are unstrained and have high crystalline quality. Moreover, absence of Si-Ge vibration implies that Ge NWs/Si substrate interface region is very thin. With the Ge NWs samples grown on (111) Si substrate, very similar spectra were obtained.

The main PL spectrum peak, TO of Ge NWs on (111) Si substrate, which originates at the Ge NWs/Si substrate interface other than Ge NW volume or Si substrate [21], is red-shifted and broader compared to the PL spectrum from NWs grown on (100) substrates. This indicates that the intermixing at the base of NW is more efficient in samples grown on (111) substrate; B. V. Kamenev et al. attributed it to the difference of

initial stage of NW growth due to the crystallographic orientation and possible differences in strain resulting from the differently oriented substrates.

# **3.1.2 Contact Fabrication**

So far, the electrical measurements of NWs have been carried out after preparing single NW device by peeling off the NWs from the substrate and dispersing them parallel to the substrate surface followed by lithographical deposition of contacts on each NW. In this thesis, the electrical measurements were performed vertically through NWs to substrate including NWs/substrate HJ interface by placing one contact on the Ge NWs and the other on the bottom of Si substrate as shown in Figure 3.3.



**Figure 3.3** Schematic representation of the samples with contacts. (a) Metal contact and (b) graphite contact configuration.

As a back side contact, indium was pressed onto the bottom of Si substrate. The indium contact has the advantage of being chemically stable once placed and robust to attachment of wires for electrical measurement.

Top contacts were made with different configurations. A graphite or metal contact was used for each configuration. For the measurement of Ge NWs grown for 36 min on (100) Si substrate, two samples were prepared by fabricating different contacts on Ge NWs: one sample with metal contact which penetrates presumably toward to the Ge NWs/Si substrate HJ interface and the other with a graphite contact on the tips of Ge NWs (Figure 3.3).

The metal contact was made by soldering Wood's alloy on the Ge NWs at low temperature. Wood's alloy is composed of bismuth, lead, tin, and cadmium, and the melting point is about 70 °C. In addition, it was necessary to guarantee the wood's alloy not to make a direct contact on Si substrate. A reference contact was made with Wood's alloy on the top of substrate for this purpose. By observing quite a different I-V characteristic from the measurement with the reference contact, compared with that from the measurement with the Wood's alloy contact on top of Ge NWs, a successful contact fabrication was confirmed. The graphite contact was achieved by locating a graphite sharp tip on top of Ge NWs layer.

Two more samples were prepared with graphite contacts for the mesurements of the Ge NWs grown for 9 min on (111) Si substrate and the Ge NWs grown for 9 min on (100) Si substrate.

# 3.1.3 Ge/Si HJ Band Discontinuity

Band discontinuity at the interface of semiconductor HJ is one of crucial parameters which determine electrical carrier transport property and has been a central problem of lattice-mismatched HJ.

In an ideal case, the conduction band discontinuity  $\Delta E_c$  would be the difference in electron affinities  $q(\chi_2 - \chi_1)$ , and the valence band  $\Delta E_v$  would be found from  $\Delta E_g - \Delta E_c$ , which is known as the Anderson's affinity rule. However, no clear picture exists at present for the expected band alignments and band offsets for the real (Ge, Si) system, which can be changed from type I to type II [22, 23, 24]. Historically, the accepted band offsets values for semiconductor HJs are usually based on a consensus derived from the result of a number of different measurement techniques. The lattice constants of the pure elements Si and Ge are mismatched by 4.2 %. It has been possible to fabricate Ge/Si HJs with no misfit defect generation, but the mismatch is accommodated by lattice strain. Besides, it has been reported that the band lineups at the Si/Ge interfaces, even though essentially no misfit defect generation is found, is dependent on the interface orientation, and also upon the strain conditions in the materials [9]. Unfortunately, most of the experimental values for Ge/Si HJ band offsets that have been reported did not specify the exact structure of the interface, but it is accepted that the conduction band offset is negligibly small with a large valence band offset.

In case of self-assembled zero-dimensional Ge quantum dot embedded in Si matrix layer, the results are known to be very different from those in a biaxially strained 2 D layer HJ. Since the growth mode is strain induced and the dot formation is a result of elastic relaxation, the Si above and below the spherically strained islands exhibits tensional strain. It is known that in tensile strained Si, the two fold degenerate  $\Delta(2)$  valleys of the conduction band is downshifted, which result in a clear type-II band alignment with significant offset in both bands at the interface between the Ge dots and the surrounding Si [23, 25]. For 1 D NW system, because of a small NW diameter, the stress from the mismatch can relax without creating defects at the interface. This may introduce an additional benefit which is the advantageous condition for combining highly mismatched materials, achieved by the efficient strain relaxation through the open side surface in the NW geometry. However, to the best of my knowledge, there has been no experimental or theoretical report on the band lineup of Ge NW grown on Si substrate.

### **3.2 Experimental Techniques**

### **3.2.1 DC Measurements**

Carrier transport in ideal HJ can be explained only by diffusion of minority carriers over the potential barrier formed by the energy band discontinuities at the interface. One of unique property of HJ compared to homojunction is that if the barrier for hole is much higher than that for electrons, then the current will consist almost entirely of electrons and vice versa.

Realistically, the I-V characteristics of HJ are explained by various mechanisms. If the barrier width is very thin, the dominant current can be tunneling current through narrow nearly triangular barrier or thermionic emission current if the interface behaves like a Schottky barrier. As another source of current, thermal generation of carriers in the semiconductor bulk or via deep levels at the HJ interface can contributes to the current.

The I-V characterization of the samples in this thesis is quite attractive since they have complex and unique structure which has never been considered before, HJ comprised of n-doped 3D bulk and presumably intrinsic 1D NWs; Au can acts as dopant or carrier

scattering center in Ge and there is a possible incorporation of Au into the Ge NW during the growth.

### 3.2.2 AC Admittance Spectroscopy

Admittance spectroscopy is one of major techniques to diagnose semiconductor junction. Admittance signals can originate from deep level traps [26] and band offsets [27] in the junction. This technique has several modifications and the applications seem to be limited by device structure. Conventionally, most admittance spectroscopy has been performed for the investigation of Schottky barrier defect levels [26] and subsequently used to extract the band offsets in the HJ system such as Si/SiGe system [27]. During admittance spectroscopy the zero bias capacitance and AC conductance are both measured as a function of temperature at a number of different frequencies. These experiments give information about the temperature-dependent thermal relaxation times of the deep levels which are present in a semiconductor band gap [26] or can used to obtain the activation energy controlling the carrier transport in HJ related to band offsets [26]. For the latter application, the HJ is usually placed close to the depletion layer formed by a Schottky barrier, *p-n* junction or MOS capacitor. Frequency scanning of admittance is alternatively used as an admittance spectroscopy by measuring complex admittance of a junction as a function of frequency at several temperatures for the investigation of defect levels. Because in response to the testing AC electric potential, defects change their occupation numbers depending on their relaxation times, they have frequency dependent charge storing ability, thus, contributing to frequency dependent admittance.

As another modification of admittance spectroscopy, voltage-dependent capacitance data can be used to investigate the band offsets. Among electrical methods, Capacitance-voltage (C-V) profiling, especially known as C-V intercept method, is a commonly used technique to determine the band offsets in HJ structures [28, 29]. While frequency dependent admittance is generally attributed to defects, C-V profiling tests the spatial charge distribution.



Figure 3.4 Band diagram of *p*-*n* anisotype HJ.

The technique use the theory that the depletion region in a reverse biased semiconductor junction varies with applied bias. The band bending on either side of the junction contributes to the total built-in voltage  $V_b$ , with the relationship of  $V_b = V_{b1} + V_{b2}$ . From the band diagram of a HJ (Figure 3.4) consists of smaller band gap p type and larger band gap *n*-type semiconductor, the conduction band offset can be written as

$$\Delta E_c = qV_b + \delta_1 + \delta_2,$$

where  $\delta_1$  and  $\delta_2$  is the relative position of the Fermi levels from the valance band and the conduction band respectively. Applying Poisson's rule, we obtain

$$W_1^2 = \frac{2}{q} \frac{N_2 \varepsilon_1 \varepsilon_2 (V_b - V)}{N_1 (\varepsilon_1 N_1 + \varepsilon_2 N_2)} \text{, and } W_2^2 = \frac{2}{q} \frac{N_1 \varepsilon_1 \varepsilon_2 (V_b - V)}{N_2 (\varepsilon_1 N_1 + \varepsilon_2 N_2)}.$$

 $W_1$  and  $W_2$  are the depletion width in each side of the junction. Then, corresponding depletion capacitances for each region are  $C_1 = \frac{\varepsilon_1}{W_1}$ , and  $C_2 = \frac{\varepsilon_2}{W_2}$ .

The total capacitance of the junction is series capacitance of  $C_1$  and  $C_2$ ,

$$C_D^2 = \frac{qN_1N_2\varepsilon_1\varepsilon_2}{2(\varepsilon_1N_1 + \varepsilon_2N_2)(V_b - V)}$$

When plotting  $1/C_D^2$  versus V, the plot shows linear curve and, from the intercept value at V = 0, V<sub>b</sub> can be obtained. Doping concentration given, from the band offset equation, the conduction band offset  $\Delta E_c$  is calculated. As a matter of fact, this equation is applied only for the HJ comprised of two opposite types of semiconductors. For isotype HJs, because one side of junction has accumulation region, the depletion approximation can not be applied to get the equations. However, for both case, the linear relationship,  $1/C_D^2 \propto V$ , is valid in most cases [28].

Admittance spectroscopy in this thesis is different from the conventional junction admittance spectroscopy which is achieved by performing both frequency and temperature sweeping in order to extract quantitative information about deep states or band offsets. Instead, it is carried out by measuring sample admittance as a function of frequency and bias voltage at room temperature. The purpose is to understand and compare behavioral properties of the carrier transport associated with the defects in Ge NWs/Si substrate HJ interface and Ge NW volume. Also, the use of light provides information about defect-related transport mechanism of photo-generated carriers.

#### **3.3 Measurement Setup**

### **3.3.1 Apparatus for Measurement**

The entire arrangement of apparatus set up for the electrical measurements is shown in Figure 3.5. The samples were located in a sample holder with two side electrodes to which the cables of electrometer or impedance analyzer were connected.



Figure 3.5 Measurement apparatus setup.

KEITHLEY 6517A electrometer, which can generate DC source voltage in itself, was used for the I-V measurement. The admittance data were measured by HP 4192A impedance analyzer. The impedance analyzer can operate in self-scanning mode under the control of a personal computer. HP 4192A impedance analyzer provides a constant alternating voltage signal at the selected frequency to the sample. The magnitude and phase of the steady state current (after transient behavior has decayed) taken by the sample is recorded and converted into real and imaginary admittance or impedance. Thus, the impedance analyzer measures impedance by simultaneously measuring two independent,

complimentary admittance or impedance parameters in each measurement cycle. The frequency is then augmented to the next step and the process is repeated over the entire selected frequency range. The voltage sweeping measurement employs the same mechanism. Detailed description of the mechanism will be made in the next section.

An  $Ar^+$  laser was used in the measurement, and it can produce wavelengths of 514, 488, 457 nm and a multi-line as well. The laser beam was focused by lens and guided to the sample via several mirrors (Figure 3.5).

### 3.3.2 Auto-Balancing Bridge and Vector Ratio Detector

Traditionally, bridge method has been used with high accuracy and wide frequency coverage up to 300 MHz by using different types of bridges in order to measure impedance or admittance. These bridges are composed of certain combination of capacitors, inductors, and resistors with respect to the types of bridge which is suitable for measuring specific characteristic of impedance such as capacitance or inductance, and frequency range where the measurement is carried out.

These bridges are operated on the same principle of a dc bridge, Wheatstone bridge. A bridge consists of four arms, an AC source and a balance detector sensitive to small alternating potential differences respectively (Figure 3.6). When no current flows through the detector, the value of the unknown impedance  $Z_x$  can be obtained by the relationship of the other bridge elements. The general equations for bridge balance are;

$$Z_2 Z_X = Z_1 Z_3$$
, and  $\theta_2 + \theta_X = \theta_1 + \theta_3$ .



Figure 3.6 Schematic of the circuit for bridge method.

The disadvantage of bridge method is that manual balancing is needed for the measurement and different type of bridge is needed for each particular application.

There are many measurement method of impedance including bridge method described above such as I-V, RF I-V, Network analysis and auto-balancing bridge method. HP 4192A LF Impedance analyzer use Auto balancing bridge method to measure the impedance. Auto-balancing bridge method offers the best accuracy over a wide impedance measurement range.

The basic operation of the auto-balancing bridge method will be reviewed here using references [30, 31, 32]. In Figure 3.7, an AC signal is applied from the high/current terminal (Hc). The high/potential (Hp) terminal measures the voltage across  $Z_x$  with respect to a virtual ground maintained by the low/potential (Lp) terminal. The low/potential terminal is kept near the voltage level of ground by a feedback loop called a null loop. The null loop circuit pulls the current, which flow from Hc terminal to  $Z_x$ , to a range resister (R<sub>r</sub>). Impedance analyzer usually has several range resistors for high resolution measurement. The current flowing through  $Z_x$  can be measured by detecting the voltage of the range resistor. Since the range resistor value is known, measuring two voltages across  $Z_x$  (E<sub>x</sub>) and R<sub>r</sub> (E<sub>r</sub>) gives the impedance vector  $Z_x = R_r \times (E_x / E_r)$ .



Figure 3.7 Simplified block diagram of auto-balancing bridge method [30].

The balancing operation is performed in the null loop (shown with dashed line in Figure 3.7). When the bridge is unbalanced, the null detector detects current and the next phase detector separates it into  $0^{\circ}$  and  $90^{\circ}$  components. These signals go to the modulator passing through loop filter, and after modulated with Hc terminal source current, they are fed back through the amplifier and the range resistors to cancel out the current flowing through  $Z_x$ . This balancing operation is performed automatically through the frequency range which is limited by the performance of null loop circuit. In practice, the general LCR meters, which employ a simple operational amplifier in the null loop, has disadvantage in accuracy at high frequencies.

With the balancing maintained, the vector ratio detector measures two vector voltages across  $Z_x$  ( $E_x$ ) and  $R_r$  ( $E_r$ ). Selector S1 selects either one of these signals so that both the signals alternately flow the same path. Each vector voltage is sent to an A/D converter and separated into its 0° and 90° components by digital processing.

#### **3.3.3 Specifications and Procedure of Measurements**

A LabVIEW program developed for HP 4192A and KEITHLEY 6517A was used for all data acquisition and measurement control. Both I-V and admittance data were collected and recorded to PC and all the specifications of measurement, such as applied voltage and frequency range, sweeping interval during frequency and voltage scanning measurement, and oscillation level, was controlled by this program.

For I-V measurements, a voltage step was set to 5 mV from -1 V to 1 V and the electrical characterization was carried out with KEITHLEY 6517A electrometer before and after sample illumination with 40 mW red laser adjusted to multi-wavelength mode.

I-V measurements were followed by admittance scanning with HP 4192A impedance analyzer. During admittance measurement, parallel conductance and capacitance of the sample were measured by selecting corresponding circuit mode in the LabVIEW program window between series R and X (impedance) mode and parallel G and C (admittance) mode. For each sample, conductance and capacitance as a function of bias voltage (G-V and C-V) at a number of fixed frequencies were measured as well as conductance and capacitance as a function of frequency (G-f and C-f) at several fixed bias voltage. G-V and C-V scanning (In LabVIEW program, it is represented as voltage sweep mode) can be performed simultaneously at each selected fixed frequency and the same are

G-f and C-f at each bias voltage (frequency sweep mode). At each scanning, the same measurements with sample illumination were also carried out. During the voltage scanning, frequency was sweeping up with logarithmical intervals between 5 Hz to 1.3 MHz automatically, where 130 points were selected, and for frequency scanning, voltage step was set to 10 mV. Oscillation level of source voltage was set to 30 mV.

### **CHAPTER 4**

## **RESULTS AND DISCUSSIONS**

The results of I-V and admittance measurements on the samples described in chapter 3 are presented here as well as their discussion. During the measurements, it was possible to investigate Ge NW volume and Ge NWs/Si substrate interface separately by comparing data from the samples with different contact configurations. Different carrier transport properties observed in each region will be discussed.

A nomenclature for samples will be applied during the discussion. Each sample is assigned a name with respect to its substrate orientation and growth time as shown in Table 4.1 below. All the admittance data of the samples measured in this study are plotted in logarithmic scale in Appendix in the same order as the samples appear in the first column of the table.

Name	Substrate orientation	CVD growth time /Estimated length of Ge NWs
GeNW_9_100G	(100)	9 min/ 360 nm
GeNW_36_100G	(100)	36 min/ 1400 nm
GeNW_36_100M	(100)	36 min/ 1400 nm
GeNW_9_111G	(111)	9 min/ 360 nm

 Table 4.1 Sample nomenclature.

#### **4.1 DC Measurements**

Rectifying property typical of a diode is observed from Ge NWs/(100) Si substrate with metal contact (GeNW\_36\_100M) as shown in Figure 4.1. At large forward bias, the I-V curve saturates with increasing bias, which is probably due to series resistance of undepleted Si bulk and contacts. The estimated series resistance by measuring the I-V characteristic curve slope at high bias voltage is ~520  $\Omega$ .



GeNW\_36\_100M

**Figure 4.1** I-V characteristic curves of GeNW\_36\_100M in logarithmic scale. Red curve is I-V characteristic under illumination. In the inset, I-V characteristics of GeNW 36\_100G are plotted in linear scale.

On the other hand, during the measurement of samples with graphite contacts (GeNW\_36\_100G), no photosensitivity was observed. The I-V characteristic curves of the

sample follow nearly ohmic behavior. The corresponding resistance of  $\sim 0.6 \text{ T}\Omega$  is calculated from the slope of linear-plotted I-V characteristic in the inset of Figure 4.1.

Therefore, it is reasonable to conclude that the huge resistance of Ge NW volume dominates the I-V characteristic in the graphite contact sample whereas, in the metal contact sample, the contact reaches almost at the interface of Ge NWs and Si substrate, and hence the junction I-V characteristic of the interface can be measured without being shadowed by the resistance of Ge NW volume.

### 4.2 AC Admittance Spectroscopy

### 4.2.1 Voltage Independence in Admittance of Ge NW Volume

Significant differences are found between the admittance data from the sample with metal contact (GeNW\_36\_100M) and those with graphite contact (GeNW\_9\_100G and GeNW\_36\_100G). During voltage-sweep measurements, the conductance and capacitance of GeNW\_9\_G and GeNW\_36\_100G kept nearly constant value while those of GeNW\_36\_100M clearly showed a dependence on bias voltage. Figure 4.2 (a) and (b) are conductance characteristic curves of GeNW\_36\_100G and GeNW\_36\_100M plotted as a function of bias voltage, which clearly show difference in voltage dependence.

During frequency-sweep measurement of GeNW\_9\_111G, another sample containing Ge NW volume, even smaller admittance variation as a function of bias voltage was confirmed by examining C-f and G-f characteristics (Figure 4.10); hence, the voltage-sweep measurements were omitted for this sample.





The voltage independent property in admittance is well consistent with the I-V characteristics. When AC signal is applied, the Ge NW volume contributes to destructing voltage dependence of admittance at the junction interface by providing huge series resistance in the sample.

### 4.2.2 Carrier Transport in Ge NW Volume

In the admittance characteristic curves of the samples with graphite contacts as a function of frequency as shown in Figure 4.3, frequency dependence are observed. The observed behaviors are dominated by Ge NW volume hence they are considered as Ge NW volume properties. In particular, the G-f characteristic curves clearly show two regimes of one exhibiting a near power law behavior at high frequencies and the other with frequency independent response at low frequencies.

At low frequency range, some zeros and small negative values were obtained. The negative values were found only when a resonance-like curve existed in the characteristics, especially in illumination condition in the frequency range from  $\sim$ 1 kHz to  $\sim$ 10 kHz. The reason is believed that the small conductance of samples at low frequencies is out of measurable scope of measurement system and there is a resonant frequency caused by an introduction of a series inductance from the measurement system to the samples, which led to negative AC conductance. These resonance behaviors can be seen also in the C-f characteristic curves at the same frequency region as shown in Figure A.12 in appendix.



Figure 4.3 G-f characteristic curves of (a) GeNW\_9\_100G and (b) GeNW\_36\_100G.

On the whole, the G-f characteristic curves obtained from graphite contact samples are in accordance with conduction model based on hopping processes, where the localized centers are suggested to be associated with the defects in Ge NW volume. The AC conductivity due to electron hopping between localized centers at high frequency is known to have the form  $\sigma_{AC}(\omega) = A\omega^s$  [33], where A is constant dependent on temperature,  $\omega$  is the angular frequency of the signal and the exponent s is generally less than or equal to unity. Then the total conductivity is given by the equation  $\sigma_{tot} = \sigma_{DC} + A\omega^s$ . Here,  $\sigma_{DC}$  is frequency-independent conductivity due to excited electrons from localized states to the conduction band. The G-f characteristic curves of graphite contact samples are well fitted to this relationship.

The observed shift of G-f characteristic curves indicates that photo-generated electrons and holes are localized on defect states in Ge NW. When the Ge NW volume is illuminated, photo-generated electrons are immediately captured by defect states rather than excited to the conduction band, and then, they contribute to the conduction process by jumping between two states with the field variation (Figure 4.4).



Figure 4.4 Effect of illumination on hopping conduction in Ge NW volume.

### 4.2.3. Carrier Transport in Ge NWs/Si Substrate HJs Interface

During the admittance measurements with the sample with metal contact, significant frequency and voltage dependence were found, showing behaviors of a semiconductor junction as shown in Figure 4.2 (b) and Figure 4.5. The C-V characteristic curves (Figure 4.2 (b)) of GeNW\_36\_100M consist with the I-V characteristics. The curve slope well reflects the behavior of I-V characteristic curve at corresponding bias voltages. Additionally, a large difference between the conductance measured under illumination and dark condition at reverse bias indicates that valence band electrons are easily excited to the conduction band by the illumination and thus increased free carriers concentration improve AC differential conductivity. Also, the frequency dependence of the junction conductance will reduce as the photogenerated free carries dominate the carrier transport with increasing reverse bias (Figure 4.5).



Figure 4.5 G-f characteristic curves of GeNW 36 100M.

# **4.3 Electrical Equivalent Circuit Model**

From the discussion of I-V and admittance data, an electrical equivalent circuit model of GeNWs on Si substrate can be suggested as shown in Figure 4.6.

Ge NW volume can be modeled by a huge resistance  $R_B$  of the order of ~ 0.6 T $\Omega$  parallel with a capacitance  $C_B$  which values vary with signal frequency by hopping conduction mechanism. The conductance of Ge NW volume will gradually increase with increasing frequency as the polarization due to electron hopping between states inside the bulk has less and less chance to keep pace with the applied field without appreciable phase shift. The Ge NWs/Si substrate interface is represented as a Si/Ge HJ diode. Resistance  $R_s$  ~520  $\Omega$  is series combination of the undepleted Si bulk resistance and contacts.



Figure 4.6 Equivalent electrical circuit model of Ge NWs on Si substrate.

### CHAPTER 5

# **CONCLUSION AND FUTURE WORK**

In summary, my MS thesis present and discuss studies of electrical properties of Ge NWs grown on (001) and (111) n-type Si substrate by CVD through VLS mechanism. The carrier transport investigations are focused on DC conductivity (and photoconductivity) and AC admittance spectroscopy. The electrical measurements were carried out after preparing samples with metal or graphite contacts to Ge NWs with different configurations. Ge NWs/Si substrate one-dimensional HJs were fabricated by locating Wood metal contact into an interface region and a rectifying behavior is observed during DC conductivity measurements. The observed frequency and bias dependence in Ge NWs/Si substrate AC conductivity in samples with metal contact can also be explained using a simple rectifier model. The electrical properties of Ge NW volume were investigated by measurements of the samples with graphite contact, presumably contacting Au tips of Ge NWs. High DC resistance of ~0.6 T $\Omega$  and no voltage dependence from admittance measurements point on a very low conductivity, while the observed shift in conductivity as a function of frequency under illumination indicates that photo-generated electrons and holes are localized on defect states in Ge NWs. In particular, the admittance frequency dependence in the region of frequencies f > 10 kHz was associated with a carrier hopping process, and the localized centers are suggested to be associated with the twin dislocation defects in Ge NWs.

In conclusion, these results are in a good agreement with the data on structural [5] and optical [21] properties of Ge NWs, and they propose that the Ge NWs/Si substrate

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interface is nearly defect free.

We believe that future work in this direction can be focused on several critical issues:

- (a) Proper passivation of Ge NW surfaces, most likely by Si;
- (b) Formation of Ge NWs embedded into a Si matrix;
- (c) Temperature dependence of carrier transport in Ge NWs/Si substrate 1D
   HJ;
- (d) Spectral dependence of Ge NWs/Si substrate 1D HJ photoconductivity;
- (e) Time-resolved photoconductivity under pulsed laser excitation in all described samples.

# APPENDIX

### ADMITTANCE MEASUREMENTS RESULTS

All the measured admittance data are plotted as a function of bias voltage or frequency in logarithmic scale. Small negative values and zeros are not plotted in the characteristic curves except for the capacitance result of GeNW\_36\_100M, where the measured negative values are replaced with their absolute ones (Figure A.12).



Figure A.1 G-V characteristic curves of GeNW 9 100G.



Figure A.2 C-V characteristic curves of GeNW\_9\_100G.



Figure A.3 G-f characteristic curves of GeNW\_9\_100G.

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Figure A.4 G-f characteristic curves of GeNW\_9\_100G.



Figure A.5 G-V characteristic curves of GeNW\_36\_100G.



Figure A.6 C-V characteristic curves of GeNW\_36\_100G.



Figure A.7 G-f characteristic curves of GeNW\_36\_100G.



Figure A.8 C-f characteristic curves of GeNW\_36\_100G.



Figure A.9 G-V characteristic curves of GeNW\_36\_100M.


Figure A.10 C-V characteristic curves of GeNW\_36\_100M.



Figure A.11 G-f characteristic curves of GeNW\_36\_100M.



Figure A.12 C-f characteristic curves of GeNW\_36\_100M.



Figure A.13 G-f characteristic curves of GeNW\_9\_111G.



Figure A.14 C-f characteristic curves of GeNW\_9\_111G.

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