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ABSTRACT

TRANSPORT PROPERTIES OF NC-Si/A-SiO_2 SUPERLATTICES AND THEIR APPLICATIONS IN NON-VOLATILE MEMORY

by
Lakshmi Susmitha Koneru

The dc current-voltage characteristics, ac conductivity, equivalent capacitance, photocurrent transients of the n-Si/nanocrystalline-Si/amorphous-SiO_2/Al hetero-structure were measured in a wide range of illumination intensities for temperatures from 4.2 K to 300 K. Electrical transport properties of the nanocrystalline-Si/amorphous-SiO_2 superlattices were discussed. The observed domination of the electron component at negative bias and of the hole component at positive bias above 0.7 V in a dc current allows to separate transport features of electrons and holes in a nc-Si/a-SiO_2 superlattices. Transport of electrons is thermally activated if potential barrier at c-Si/SL interface of 70 meV is suppressed and several activation energies for different temperature regions were determined. Transport of holes is well described by the Fowler-Nordheim tunneling theory for a number of illumination intensities in the measured temperature region. Tunneling mechanism is additionally supported by an independence of the photocurrent decay on temperature. Two maxima in ac conductivity at 0 V and at 0.8 V were related to trap-assisted conductivity and to alignment of energy levels in the heterostructure (photoconductivity resonance), respectively. Time-dependent photocurrent measurements proved a decrease of the photoconductivity due to a decreasing mobility of holes and misalignment of the energy levels at bias above 0.8V. Density of traps of 3.5×10^{11} cm^{-2} and trapping time of 30 μs were found. An application of nanocrystalline Si/amporphous SiO_2 superlattices in non-volatile memory devices is discussed.

TRANSPORT PROPERTIES OF NC-Si/A-SiO_2 SUPERLATTICES AND THEIR APPLICATIONS IN NON-VOLATILE MEMORY

by
Lakshmi Susmitha Koneru

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APPROVAL PAGE

TRANSPORT PROPERTIES OF NC-Si/A-SiO_2 SUPERLATTICES AND THEIR APPLICATIONS IN NON-VOLATILE MEMORY

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To my dearest Grandmother

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CHAPTER 1

INTRODUCTION

1.1 Historic Overview

Modern computerized systems from simple appliances to complex networks contain many different parts - processors, displays, modems and information storage devices. Memory is that, which is capable of retaining information under certain conditions and uses the information later. A variety of different memory types exists at present as none of these types meet requirements for a universal memory cell. The main types of memory on the market are mask read only memory (Mask ROM), Random Access Memory (RAM), Read Only Memory (ROM) and Electrically-Alterable Non-Volatile Memory (E-NVM). The increase in the world memory market for different classes of memory for the last two decades is shown in Figure 1.1 [1]. There was a steady 10% market for the non-volatile memory during 1980's and the market increased steadily during 1990's. This increasing demand for non-volatility is stimulated by a fast growing market of mobile devices. An intense research and constant development of novel concepts for non-volatile memory devices show the possibility of using a non-volatile memory cell as an ideal cell. However, the ideal memory system must have an optimized density, fast access time and capability to retain data in a non-volatile condition (memory must not lose any data even without external power). Not all of these demands are satisfied by non-volatile memory at present. Further, the basic structure of memory cells including DRAM, SRAM and a non-volatile Memory cell will be discussed.

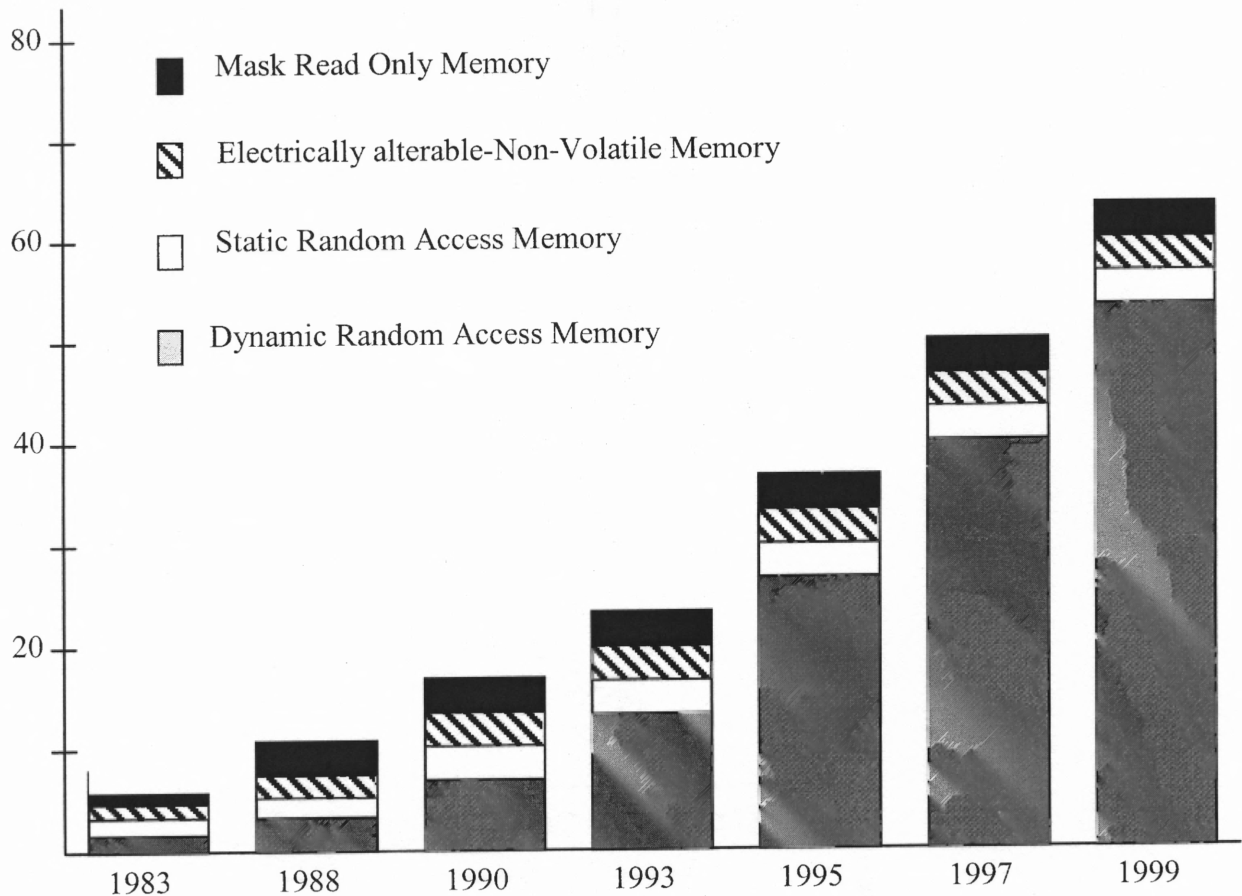


Figure 1.1 World memory market of the last decade and its share by the major classes of memory.

1.2 Random Access Memory (RAM)

Random Access Memory is the fastest memory type. That is why this memory is used in a computer where the operating system, application programs, and data in current use are kept and can be quickly accessed by the computer's process. Random Access Memory is a volatile memory. That means this cannot retain data when there is no power. The data is transferred to magnetic disk or other nonvolatile media for long-term storage purposes. There are two important classes of Random Access Memory- Static RAM (SRAM) and Dynamic RAM (DRAM).

1.2.1 Dynamic Random Access Memory (DRAM)

Currently, computers have DRAM as their main internal memory. The basic memory unit of DRAM is shown in Figure 1.2. It consists of a transistor and a storage capacitor. This simplicity of the basic unit stipulates several advantages of DRAM. It is very dense, simple to build, low cost memory.

Besides the advantages, there are disadvantages of DRAM. It has a shorter data life time about four milliseconds. This is due to the discharge of the capacitor and therefore, refreshment of the memory cell is necessary. Inspite of the fast access time of about 4ns, data is lost after each "read" step. Therefore, the "write" cycle after "read" step slows down the speed of its operation with a cycle time of about 60 ns.

There cannot be any further improvement for DRAM, as it has no more choice to improve the density with one transistor per bit. And there is no further improvement for its volatile nature because of its compromise with the density.

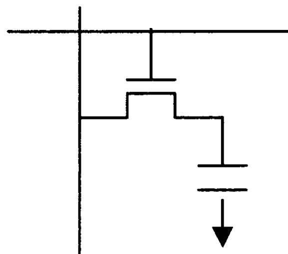


Figure 1.2 Basic DRAM cell.

1.2.2 Static Random Access Memory (SRAM)

Static Random Access Memory is used as cache for the computers as it has a faster access time of approximately two to four ns. SRAM is a volatile memory like DRAM as it can retain data only as long as the power is on. It does not need refreshing when it is powered. Bits are stored as on/off switches as digital flip-flops. The major disadvantage

of SRAM is its low density as it has a complex circuitry with 4-6 transistors per bit as shown in Figure 1.3. And so, it is expensive to build.

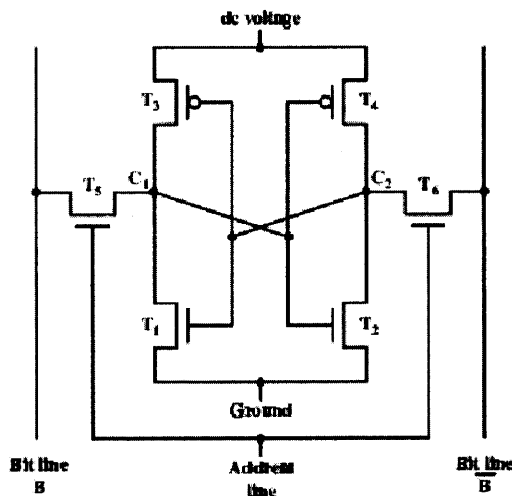


Figure 1.3 Basic SRAM cell.

1.3 Non-Volatile Memory

Non-volatile memory is a solid-state memory that need not have its memory contents periodically refreshed. That means the memory retains its data without loss even when there is no power. This memory combines the best features of DRAM, which is denser, and SRAM, which is faster. Characteristics of the ideal nonvolatile memory are: low power consumption, high speed, high reliability, high density, low cost, and the compatibility with any semiconductor circuit. Among potential applications are cellular phones, pagers, palm PCs, digital clocks, microwaves, VCRs, answering machines, calculators and integrated circuits in vehicles. A brief introduction to the basic operating principle and the concept of non-volatile memory devices are discussed below.

1.3.1 Operating Principle of Non-volatile Memory Device

The basic operating principle of the nonvolatile memory devices is the storage of the charges in the gate insulator of a MOSFET [1]. The structure of the basic cell is shown in Figure 1.4. The threshold voltage of the transistor can be changed between two different values, representing "0" (erased state) or "1" (programmed state) [1], as shown in Figure 1.5.

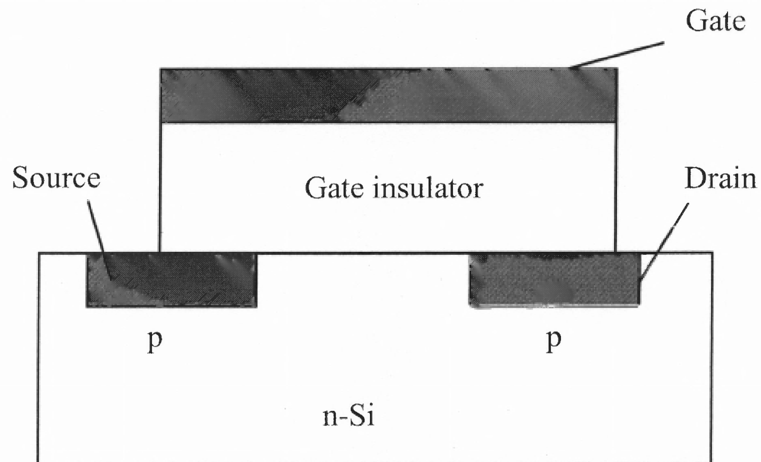


Figure 1.4 Basic MOSFET cell.

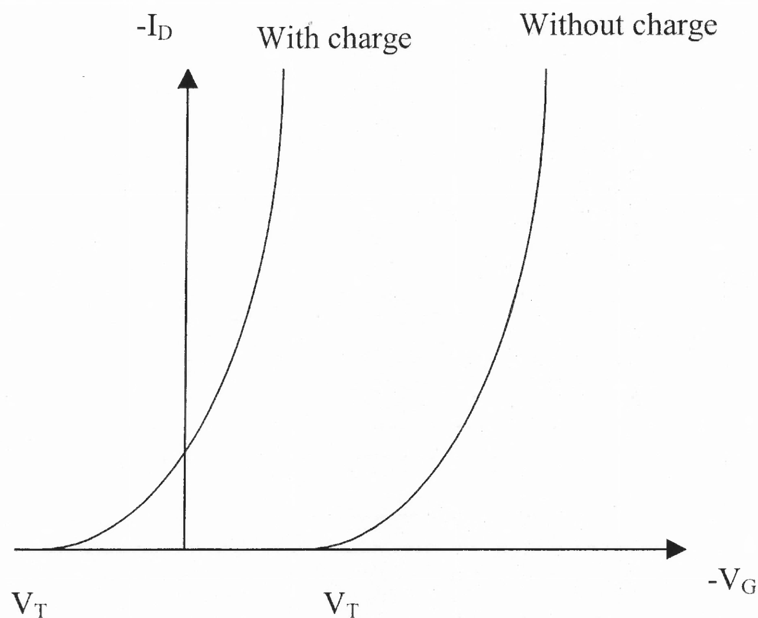


Figure 1.5 Transfer characteristics of non-volatile memory in two states representing "0" and "1".

1.3.2 Basic Types of Nonvolatile Memory Devices

Solid-state nonvolatile memory devices were introduced in the late sixties and commercial exploitation followed quickly [1]. The history of this device started with a basic MOSFET cell. The evolution of this cell led to the development of two devices - a charge trapping device and a floating gate device.

1.3.2.1 Charge Trapping Device. As seen in Figure 1.6(a), in the charge-trapping device called MNOS (Metal-Nitride-Oxide-Semiconductor), a thin dielectric layer Si_3N_4 (<10nm) is introduced between the gate insulator and the gate. The oxide-nitride layer interface contains a lot of traps, which can capture electrons and holes. These traps do not leak any charge, as the individual charges are isolated from each other by the nitride layer [1]. The energy band diagram of the MNOS cell is shown in Figure 1.6 (b). This class of memory cells is used only for military applications that must be resistant for radiation. The MNOS device has the intrinsic advantage that both programming and erasing can be achieved electrically. The chare transfer mechanism used is discussed in the subsequent section [1.4] of this chapter.

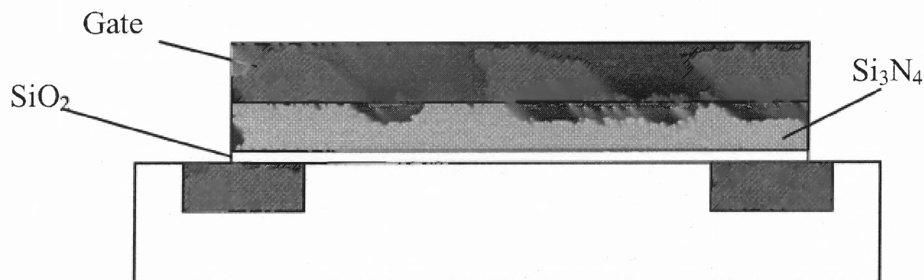


Figure 1.6(a) Charge trapping (MNOS) device structure.

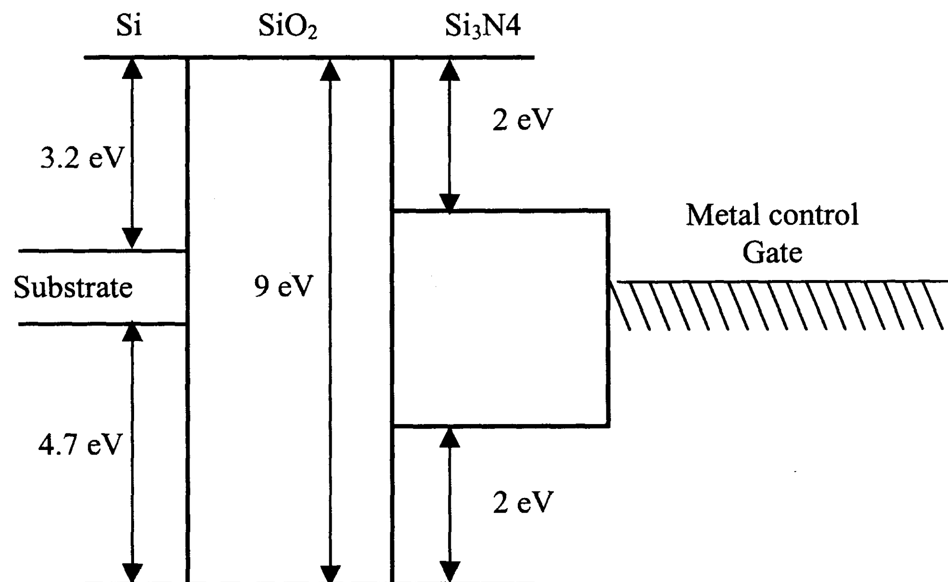


Figure 1.6(b) Energy Band Diagram of charge trapping device structure.

1.3.2.2 Floating Gate Device. The second device called floating gate (FG) or stacked gate device has emerged as a dominant design for the nonvolatile memory devices. Today, the stacked gate FG device structure continues to be the most prevailing nonvolatile memory implementation, and is widely used in both stand alone and embedded memories, and in both code and data storage applications [2].

In this floating gate device, there are two gates - the control gate and the floating gate. The control gate is the poly-silicon layer through which the voltage is applied and 'write' and 'erase' operations are performed. The floating gate is located between the control gate and the channel region and this gate is completely surrounded by the dielectrics as shown in Figure 1.7(a). The information is stored in the form of charge on the floating gate, and the charge is proportional to the threshold voltage of the FET.

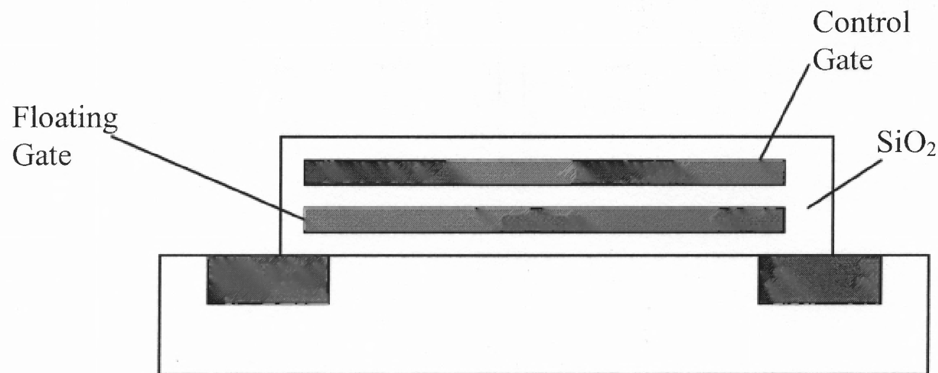


Figure 1.7 (a) Floating gate device.

This can be explained with the help of the energy band diagram of the floating gate transistor. A quantum well is formed with the floating gate surrounded by the dielectric layers as shown in figure 1.7(b). When a gate voltage is applied to program the memory cell by a certain programming mechanism, the charge is stored in the quantum well of the floating gate in the form of electrons. Tunneling describes the 'write' and 'erase' operations performed in the floating gate transistor either by increasing or reducing the charge stored in the floating gate as shown in Figure 1.7(c).

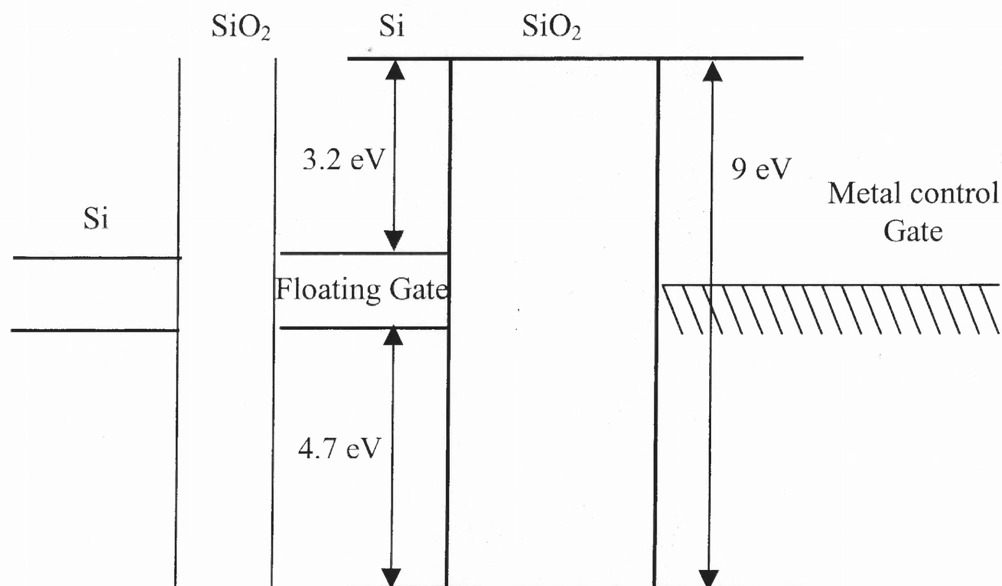


Figure 1.7(b) Energy band diagram of Floating Gate Transistor.

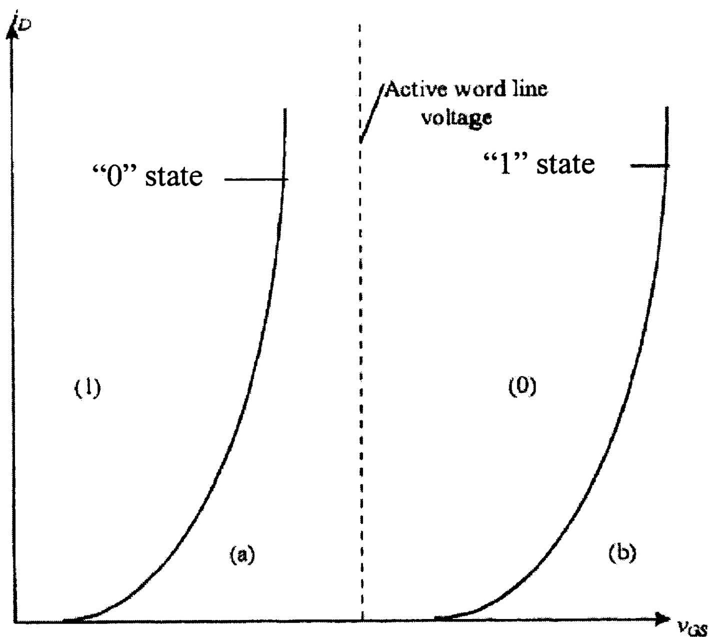


Figure 1.7(c) Transfer characteristics of the Floating Gate transistor.

1.3.2.3 Nano-crystalline Non-volatile Memory Devices. Although there has been a huge commercial success of the floating gate non-volatile memory devices, they have their limitations, which prevent them from further scaling beyond the 65 nm node. This scaling limitation comes from the extreme requirements on the tunnel oxide thickness [2]. On one hand, the oxide has to be thin enough to allow efficient charge transfer to and from the gate, under low injection conditions, in order to enable fast, low voltage and low power write and erase operations. On the other hand, the tunnel oxide must be thick enough to provide sufficient isolation under retention conditions. Hence, the industry standard compromise tunnel oxide thickness is of the order of 9-11 nm, which cannot be further reduced.

The solution of the non-volatility with allowed scaling is the concept of distributed charge storage instead of single element charge storage [4]. Nano-crystalline non-volatile memories, introduced in early nineties [3], are one particular implementation of this concept. As seen in the Figure 1.8, in the nano-crystalline non-volatile device, the charge is not stored on a continuous poly-Si layer, but instead on a layer of discrete, mutually isolated, nano-crystalline dots. Each dot stores a few number of electrons.

There are many advantages of nano-crystalline memories compared to conventional FG devices. The main one is the potential to use thinner oxide without sacrificing non-volatility. A weak spot or defect in the oxide in these devices does not create a fatal discharge path as in conventional devices, thereby maintaining good retention time. Also, the fabrication process for these devices is simpler as compared to the conventional FG devices reducing complex dual-poly processes. Further, it uses shorter channel length and therefore, smaller cell area.

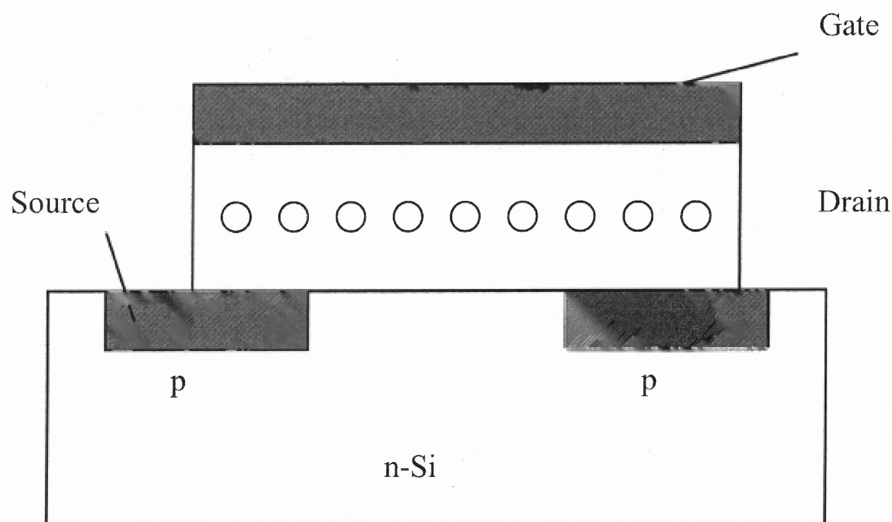


Figure 1.8 Nano-crystalline non-volatile memory cell.

1.3.3 nc-Si/a-SiO_2 Superlattices in Non-Volatile Memories

This kind of devices has nano-crystalline Si/SiO_2 superlattices embedded in the non-volatile memory devices. The nano-crystalline Silicon layers surrounded by Silicon-di-oxide superlattices are the floating gates embedded between the control gate and the source-drain conduction channel as shown in Figure 1.9(a).A similar structure was demonstrated in a publication[5]. The energy band diagram of the metal-Superlattice-Silicon structure is given in Figure 1.9(b). When a voltage is applied across the structure, there occurs resonant tunneling between the quantum wells formed within the superlattices and the charges tunnel through much thinner oxide into and off the superlattices by which the device threshold gets shifted. During the charge storage, the electrons are stored in the quantum well and there are no tunneling levels available for the electrons to escape. Also, the gate insulator is thick enough to prevent any leakage of the charge as shown in the band diagram in Figure 1.9(b). Hence, this makes the retention period of the memory device up to ten years. The carrier transport mechanism by which the conduction takes place is the objective of the thesis and is discussed in detail in the next chapter.

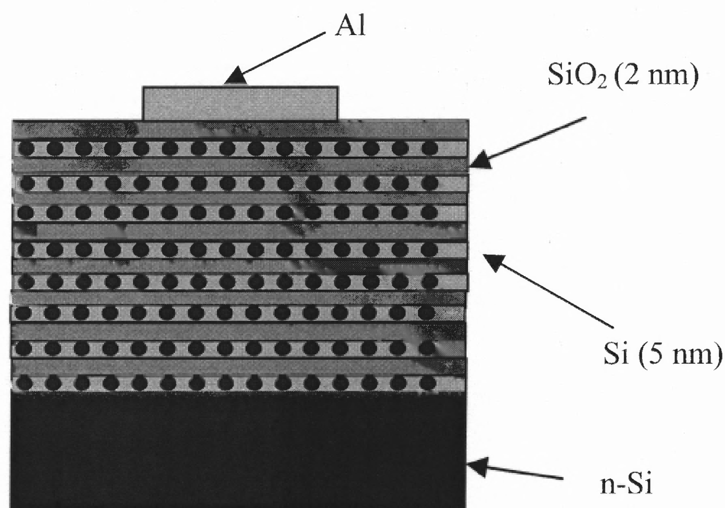


Figure 1.9(a) Superlattice Structure of multi-layered Si/SiO_2.

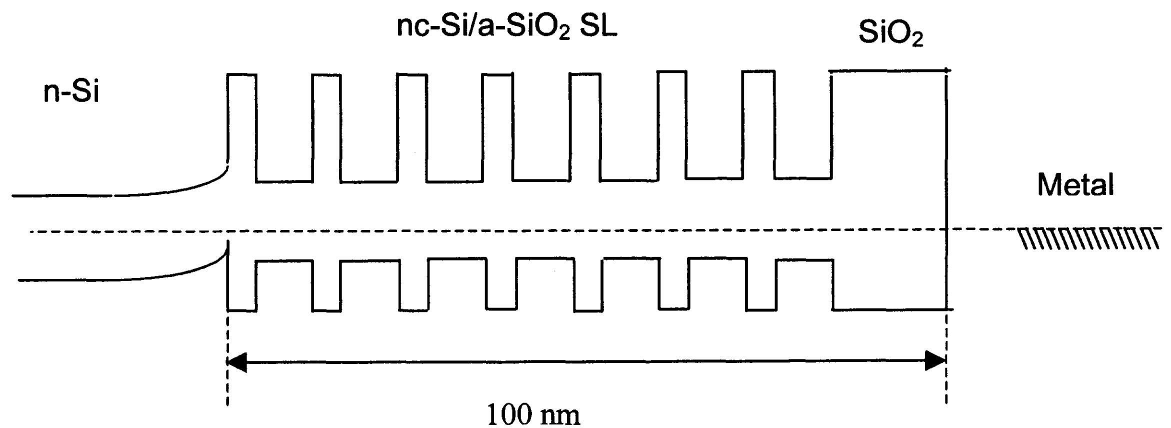


Figure 1.9(b) Si/SiO_2 superlattices embedded between the gate and the substrate.

1.4 Charge Transfer Mechanisms of Non-Volatile Memory

There are different mechanisms to change the charge content of the floating gate devices: Fowler-Nordheim tunneling, enhanced Fowler- Nordheim tunneling, channel hot electron injection and Frenkel-Poole emission.

1.4.1 Fowler-Nordheim Tunneling

Fowler-Nordheim tunneling is one of the most important mechanisms in the floating gate devices, which is a field assisted electron tunneling. The energy band diagram of the Si-SiO_2-Si structure is shown in the Figure 1.10. When a gate voltage is applied across the structure, electrons in the silicon conduction band tunnel through a triangular energy barrier of the insulator[1].

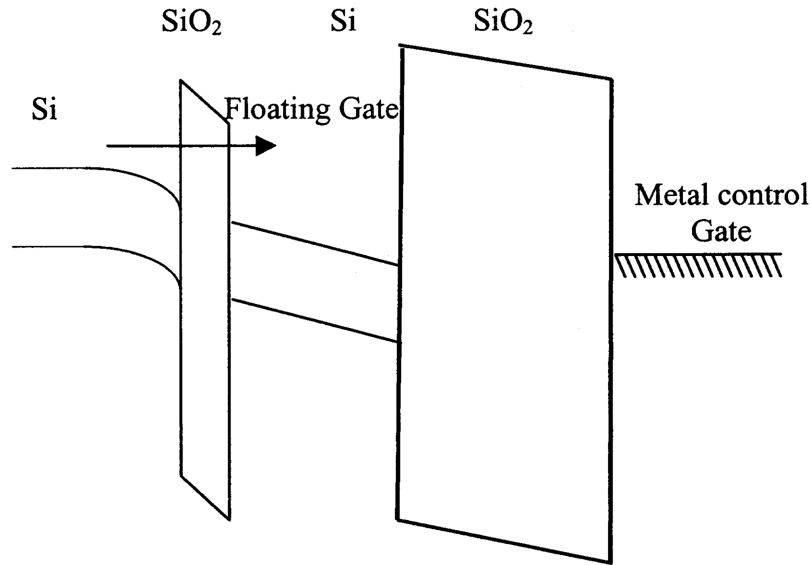


Figure 1.10 Energy band representation of Fowler-Nordheim tunneling.

The Fowler-Nordheim current density is given by [1]

$$J = \alpha E_{inj}^{2} \exp\left[\frac{-E_c}{E_{inj}}\right]$$

with

$$\alpha = \frac{q^3}{8\pi h \phi_b}\frac{m}{m^*}$$

and

$$E_c = 4\sqrt{2m^*}\frac{\phi_b^{3/2}}{3\hbar q}$$

Where h - Planck's Constant

ϕ_b - Energy Barrier at the injecting interface (3.2 eV for Si-SiO_2)

E_{inj} - Electric field at the injecting interface

q = Charge of a single electron (1.6×10^{-19} C)

m - mass of a free electron (9.1×10^{-31} kg)

m* - Effective mass of an electron in the band gap of SiO_2 (0.42 m)

$\hbar = h / 2\pi$

The Fowler-Nordheim current density is exponentially proportional to the applied electric field as shown in Figure 1.11[1].

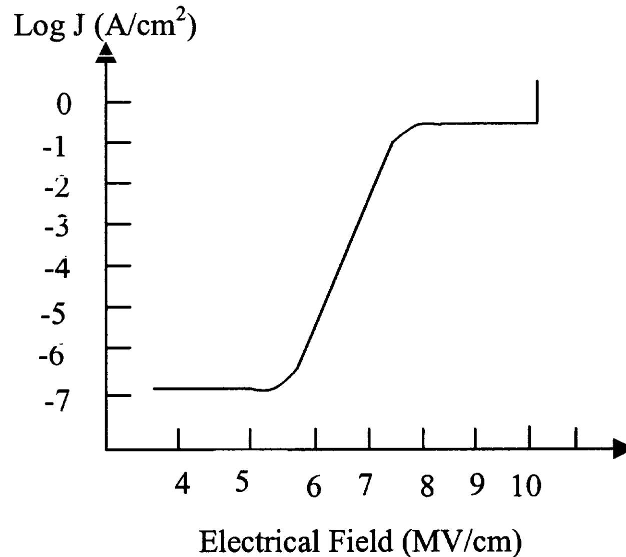


Figure 1.11 Fowler-Nordheim current as a function of applied field across the oxide.

1.4.2 Poly-oxide Conduction

This mechanism is also called enhanced Fowler-Nordheim tunneling as it enhances the conduction through the oxide barrier in the Si-SiO_2-Si structure with a lower applied field as compared to the Fowler-Nordheim tunneling [1]. Oxides thermally grown on the polysilicon show an interface covered with asperities due to the rough texture of the polysilicon. Enhanced tunneling of electrons is due to this local field enhancement at the interface. The energy band diagram of the poly oxide conduction is shown in the Figure 1.12.

As it can be seen from the band diagram, large injection fields at the interface can be obtained at moderate voltages even using relatively thick oxides.

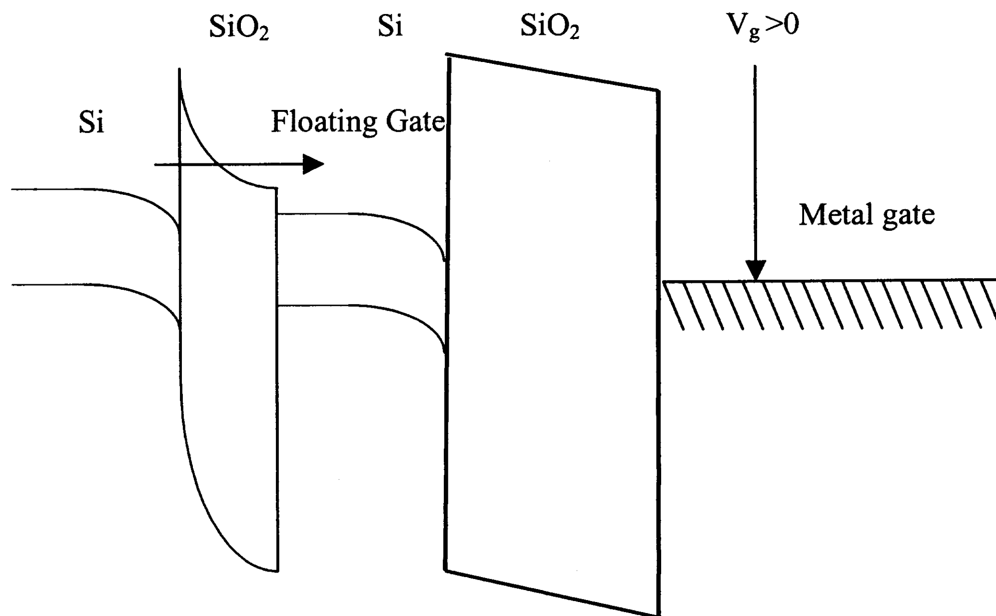


Figure 1.12 Energy band representation of enhanced Fowler-Nordheim tunneling.

1.4.3 Hot Electron Injection

Hot electron injection is the mechanism where the minority carriers (electrons in the p-type device) get heated and their energy distribution is shifted higher due to the large electric field at the drain surface. This causes impact ionization and electrons and holes are generated. The heated electrons in the channel get enough energy to overcome the insulator barrier into the gate. This current is called hot-carrier injection gate current as seen in Figure 1.13. It is only possible to inject the electrons onto the floating gate, but they cannot be erased wit the same mechanism.

The shape of the current-voltage characteristics is explained by both the drain and gate voltages as shown in Figure 1.14. For gate voltages greater than the drain voltage, the gate current is limited by the number of hot electrons that are injected. For $V_g>V_d$, the

gate current increases with decreasing gate voltage. For gate voltages smaller than the drain voltage, the oxide field becomes repulsive for the injected electrons. The gate current drops rapidly down with decreasing gate voltage.

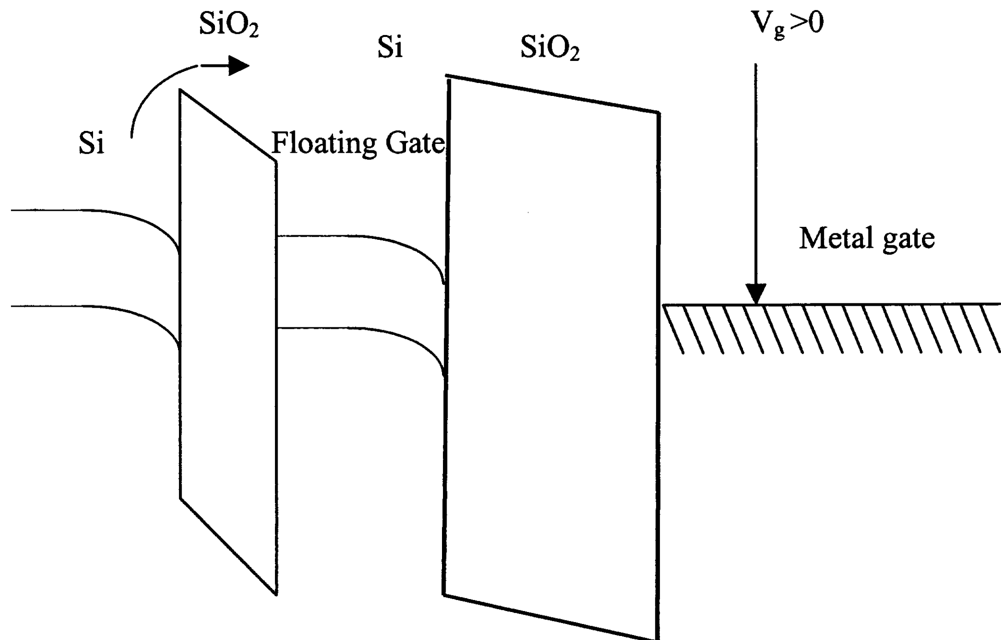


Figure 1.13 Energy band diagram of hot electron injection.

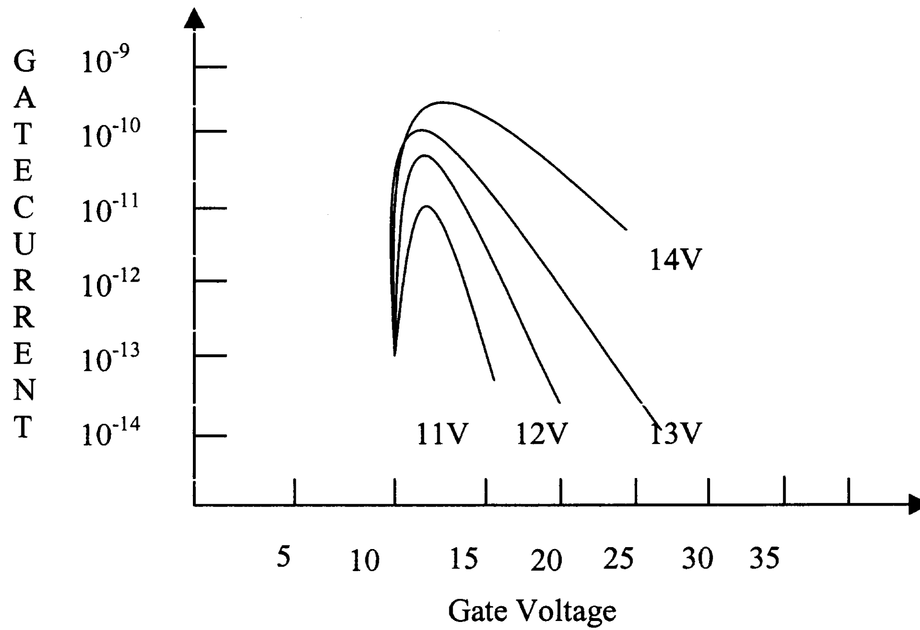


Figure 1.14 Hot electron injection current as a function of applied voltage.

1.4.4 Frenkel-Poole Emission

Frankel-Poole emission is the charge transfer mechanism used to write and erase the MNOS cell. Figure 1.15 shows the basic band diagram of this mechanism. The current J_0 is due to the Fowler-Nordheim tunneling current through the oxide layer. The current J through the silicon nitride is due to Frenkel-Poole emission given by [6]

$$J = C_2 E \exp\left[-q(\phi_B - \sqrt{qE / \pi\varepsilon_i}) / KT \right]$$

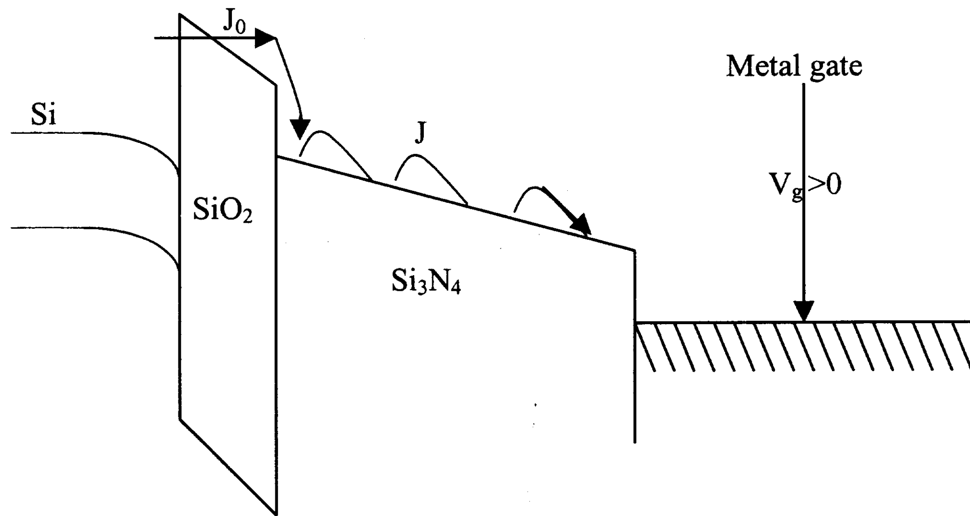


Figure 1.15 Band diagram of Frenkel-Poole emission.

1.5 Objective of the Thesis

The objective of the thesis was to find out the charge transport mechanism in the Si/SiO_2 Superlattice. The present non-volatile memory cell can have an improved performance by embedding a Si/SiO_2 superlattice between the gate and the substrate, instead of a floating gate layer surrounded by the insulator. Eight multi-layers of 2.5 nm thick Si and 5 nm thick SiO_2 were used as the superlatitice. The superlattice sandwiched between the Aluminium and the n-type Si substrate was the experimental hetero-structure used for characterization. LABVIEW and Microcal ORIGIN were used for data acquisition.

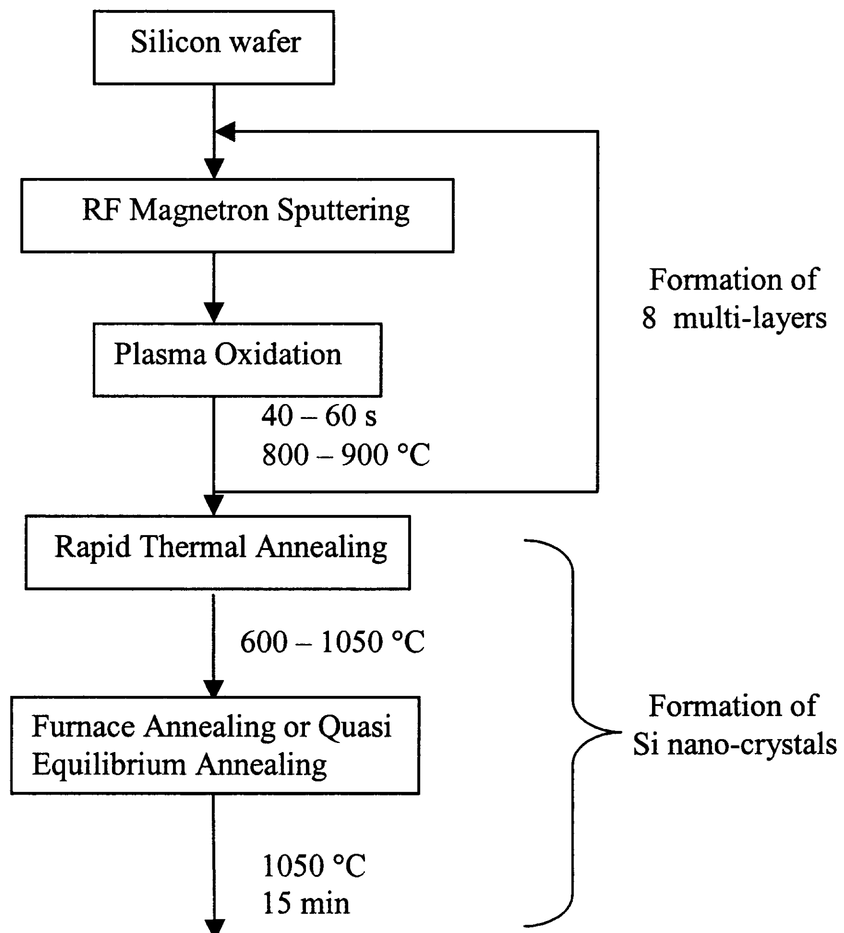
CHAPTER 2

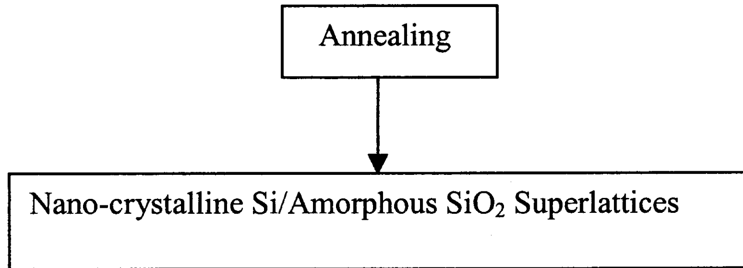
EXPERIMENTAL SETUP

This chapter details the fabrication of the samples in the first Section 2.1 and then the experimental setup for various measurements is detailed in the next Section 2.2. The fabrication of nano-crystalline multi-layers of Si/SiO_2 goes through several process steps. First, the outline of the process steps is shown in a flowchart and then the fabrication process is detailed.

2.1 Fabrication of nc-Si/a-SiO_2 Non-Volatile Superlattice

2.1.1 Flowchart for Fabrication Process





2.1.2 Starting Material

An n-type silicon wafer (Phosphorous doped with resistivity 10 Ω cm with crystallographic orientation (100) is taken. This material goes through several steps of magnetron sputtering and annealing to form 8 amorphous multi-layers of 50 Å thick Si / 25 Å thick SiO_2 layers [7,8].

2.1.3 Detailed Description of Fabrication

The step-by-step growth of amorphous Si / SiO_2 multi-layers is described here [7]. The amorphous silicon is prepared by passing the Silicon wafers initially through the first step of radio-frequency magnetron sputtering which is done in a Perkin-Elmer 2400 sputtering system. In the next step, the sputtered Silicon samples are oxidized using plasma oxidation to produce SiO_2 layers. The Si/SiO_2 multi-layers are thus formed by the repetition of successive steps of magnetron sputtering and plasma oxidation. There are eight layers with Silicon thickness of 50Å and with SiO_2 thickness of 25Å formed on the substrate.

Now, the growth of nano-crystalline superlattices is described through the remaining steps. This is performed by the recrystallization of amorphous Si/SiO_2 multi-layers formed. The thermal crystallization is performed in two steps [7]. First, the sputtered and oxidized multi-layered sample is subjected to Rapid Thermal Annealing at

800-900 °C. Nucleation starts in the amorphous-Si layers. And then in the second step, the sample is sent through furnace annealing or quasi-equilibrium annealing (QEA) with a slow increase of temperature from 600 to 1050 °C, which is done to improve surface passivation. This is followed by 15 minutes of annealing at 1050 °C in the next step. Also, strain in the multi-layers is released by QEA and slow Steam Oxidation. All these annealing steps are done in Nitrogen atmosphere.

By going through these successive steps of thermal recrystallization, 8 multi-layers of 50 Å nano-crystalline Si/ 25 Å SiO_2 are prepared and the shape of the nanocrystals is observed to be spherical which is due to the competition between surface and volume tensions of the crystals [8]. The size of the nanocrystals and the thickness of the insulator layer (~25 Å) is determined by the expected quantum confinement in Silicon nanocrystals and the relative transparency of the insulator layer that allows the charge carriers to tunnel through.

2.2 Experimental Setup for Hetero-Structure Characterization

Several types of experiments were carried out to characterize transport properties of the Al- $(nc\text{-}Si/a\text{-}SiO_2)_8$-n-Si hetero-structure. The experimental setup for dc conductivity measurements, impedance spectroscopy measurements and photocurrent transient measurements is detailed in this section. Also, parameters of the measurements using the equipment that was used in these experiments are also discussed.

2.2.1 DC Conductivity Measurements

Figure 2.1 describes the experimental setup for dc conductivity measurements. The current-voltage characteristics of the Al-(nc-Si/a-SiO_2)$_8$-n-Si hetero-structure were measured using KEITHLEY electrometer (Model 6517). The voltage was applied across the hetero-structure and the current was measured in the circuit. Photocurrent-voltage characteristics were measured by illuminating the hetero-structure sample from the side of the top Al contact with the CW He-Ne laser (wavelength 632.8 nm, maximal illumination intensity 5 mW).

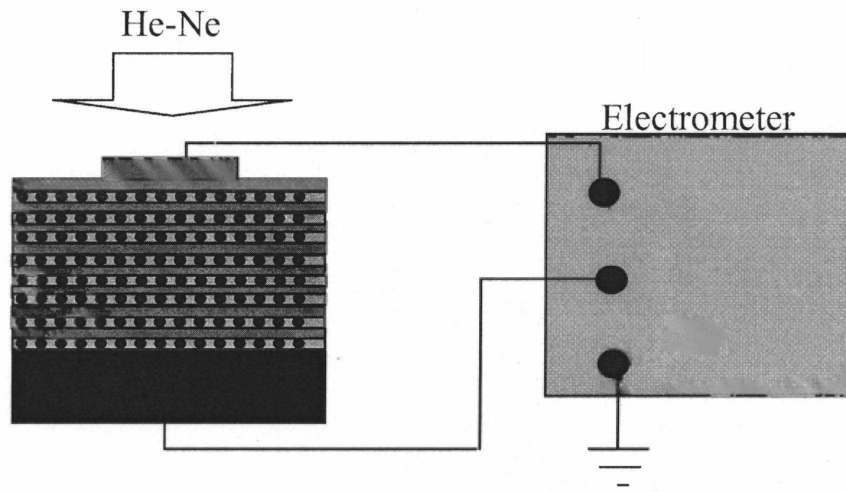


Figure 2.1 Experimental setup for dc conductivity measurements.

The voltage step applied varied for various measurements and was within –1.5 V to +2.5 V for all the dc measurements. The minimum voltage step was 5 mV. The delay time for the voltage pulse also varied for various measurements. The minimum delay time was given as 100 ms. The measurement of the current was done from 10pA to 0.1mA which was within the measurement capability of the electrometer (100aA to

21mA). Control of the measurements and the data acquisition was done using a PC with the IEEE 488 (GPIB) bus or the RS-232 interface.

2.2.2 Impedance Spectroscopy

2.2.2.1 Basics of Impedance Spectroscopy. Impedance is the response, in terms of the resultant ac voltage, of a circuit element to the application of an ac current. The ac voltage is the potential difference between two points, which reverses its sign for a given frequency as shown in Figure 2.2.

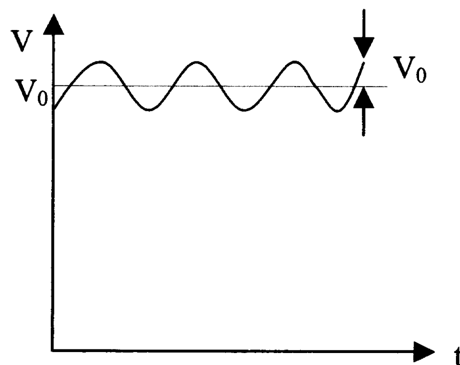


Figure 2.2 Applied ac voltage for a given frequency as a function of time.

The impedance for a parallel connection of a resistor and a capacitor is shown in Figure 2.3(a) and the phasor diagram is given in Figure 2.3(b).

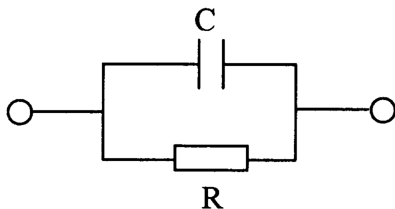


Figure 2.3(a) Parallel connection of a resistor and capacitor.

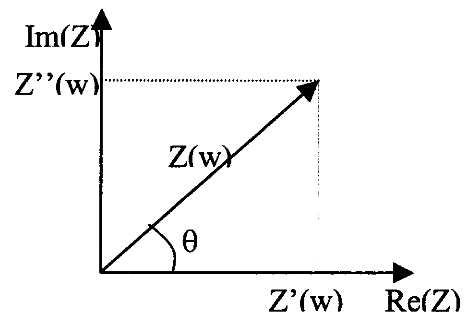


Figure 2.3(b) Phasor diagram of the impedance.

The impedance for the Figure 2.3(a) is given by the expression

$$Z^{-1}(\omega) = R^{-1} + j\omega C$$

where Z- impedance of the circuit

R- resistance

C- capacitance

The Figure 2.3(b) has the impedance Z(w) with a real part of Z'(w) and an imaginary part of Z''(w) and an angle of θ. The measurements for the conductance and the capacitance were done and presented in the next section 2.2.2.2.

2.2.2.2 Impedance Measurements. Figure 2.2 describes the experimental setup for the impedance spectroscopy measurements. AC photoconductivity and capacitance measurements were measured for the hetero-structure by using Hewlett Packard Low Frequency Impedance Analyzer (Model 4192A).

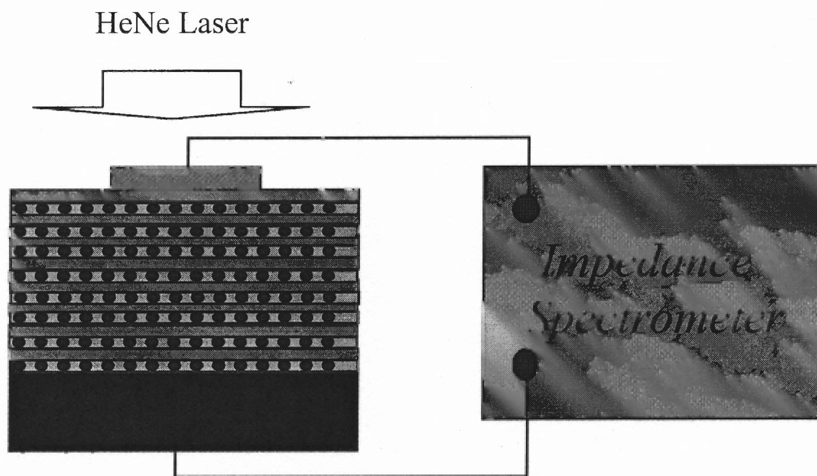


Figure 2.4 Experimental setup for impedance measurements.

The conductivity and the capacitance of the Si-SiO_2 superlattice were measured in the circuit by applying ac voltage of certain frequency across the Al -(nc-Si/a-SiO_2)$_8$- n-

Si hetero-structure. The ac voltage sweep in between –2 V and 2 V was applied for the frequencies of 400 Hz and 1 kHz. In another set of measurements, the conductivity was also measured as a function of frequency for several applied biases from 0 V to 1.5V. The frequency range for these measurements varied from 100 Hz to 1 MHZ, which is within the measurement range of the device (5 Hz-13 MHz). CW HeNe laser was used for the illumination of the sample for the photoconductivity measurements.

2.2.3 Photocurrent Transient Measurements

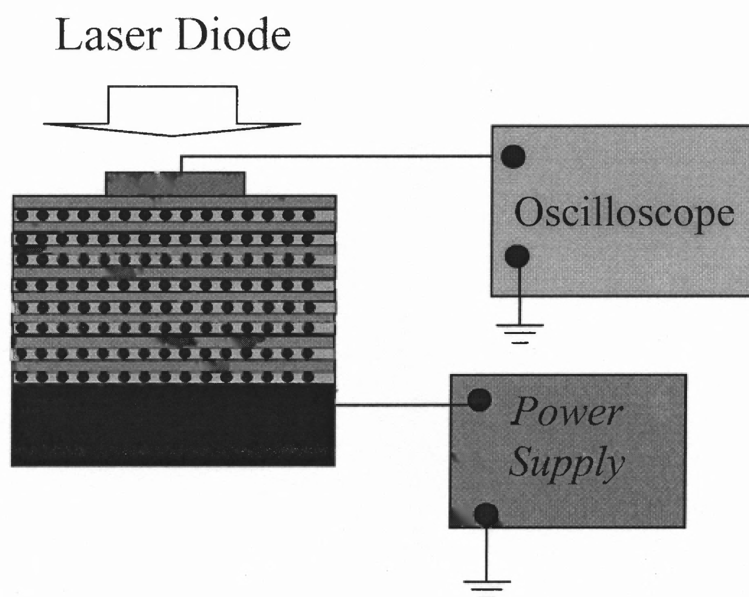


Figure 2.5 Experimental setup for photocurrent transient measurements.

Figure 2.3 describes the experimental setup for photocurrent transient measurements of the Al-(nc-Si/a-SiO_2)-n-Si hetero-structure. The excess charge carriers were excited by sequential pulses of the AlGaInP laser diode (wavelength 690 nm) with pulse duration of 100 ns or 430 ns and 10 ms delay between pulses. The voltage applied to the hetero-

structure was in the range of 0 V – 3 V (with the positive polarity applied to the c-Si substrate). Low noise batteries were used as the voltage source. The photocurrent transients were measured by the Hewlette-Packard digital oscilloscope (Model 54110D) with vertical scale resolution of 10 mV using self-made current amplifier with the input load resistance of 1 kΩ.

CHAPTER 3

EXPERIMENTAL RESULTS AND DISCUSSION

3.1 DC Dark and Photoconductivity at Room Temperature

Figure 3.1 shows dc current-voltage characteristics of (nc-Si/a-SiO_2)$_8$ superlattice at room temperature in dark (solid line) and under several intensities of a CW illumination. The polarity of the voltage is that of the substrate. The illumination was performed by a HeNe laser (wavelength 632.8 nm).

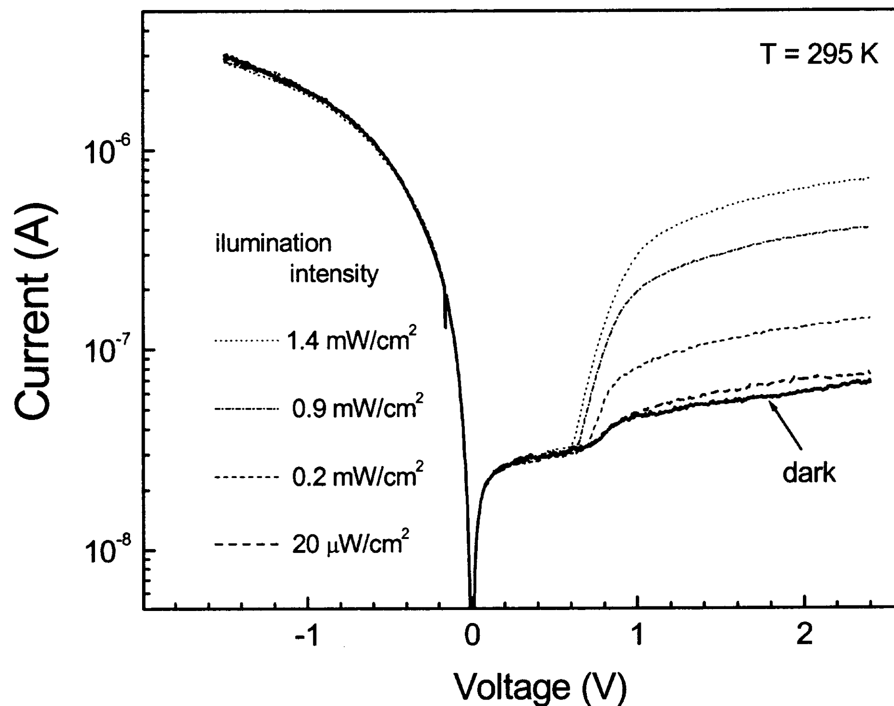


Figure 3.1 Dc current-voltage characteristics for 8 layer nc-Si/a-SiO_2 superlattice at room temperature in dark (solid line) and under several intensities of a CW illumination. Illumination was performed by a HeNe laser (wavelength 632.8 nm).

A steep increase of current at negative voltages up to 0.6V is observed and no difference exists between the curves in dark and under illumination. After the steep increase, the current increases linearly with the bias above 0.6V.

At positive bias, the current values are much smaller than those at negative voltages and there is no saturation at higher voltages. There is no difference for the dark current (solid line) and currents under different illuminations (dashed lines) until 0.6 – 0.8 V. This means the structure is sensitive to light only at positive bias higher than 0.6 V. As intensity of illumination increases from 20 $\mu W/cm^2$ to 1.4 mW/cm^2 the value of photocurrent increases from $5x10^{-8}$ A to $6x10^{-7}$ A. The increase is almost linear, which suggests that illumination is far from saturation.

Hence, there are some conclusions from the above current –voltage characteristics. At negative bias, the current is limited by the rate of supply of majority carriers (electrons) in the semiconductor [5]. And for different illuminations, photo excited charge carrier concentration is much smaller than the equilibrium or their separation is not effective (electric field drops over the whole substrate and there is no sufficient field in the region of excess electron-hole pairs generation). Hence, there is no change in the negative voltage characteristics for dark conditions and for illumination.

At positive bias, there exist two regions in the current curves under illumination-one sensitive to light and the other insensitive to light and remains the same part of the curve as in dark. The minority carrier (holes) transport is the leading charge carrier mechanism in the structure under positive bias. Excess holes are extracted from the substrate and transport through the superlattice to the top Aluminum contact. At a high positive bias: level of saturation current between dark curve and for different illumination

intensities increases with illumination: as c-Si substrate is an n-type crystalline Si which is 10 orders of magnitude smaller than the majority carrier concentration. Therefore, saturation level and its increase with illumination intensity (and, therefore, minority carrier concentration) are expected.

As the saturation value depends on the illumination intensity, an electron component of a current from the Al to substrate is negligible. A barrier of 0.7 eV is expected at the metal interface, therefore only 10^{22} cm-3 exp(-0.7eV/0.026eV)=$2x10^{10}$ cm^{-3} is negligible under illumination, but it can not be completely neglected in dark, and dark current before 0.6 V is more probably related to the flow of electrons.

Therefore, an analogy to a MIS diode with semitransparent insulator layer can be made. n-Si/SiO2 hetero-stucture may be treated in terms of standard MS or MIS theories depending on the relative input of insulator layer. Further, analysis of the theories of MIS capacitor structure for thick SiO_2 layers (not tunnel-transparent for charge carriers) and M/S theories (Schottky-barrier diode) for thin (tunnel transparent) will be applied with prior discussion of their applicability.

There is no photocurrent at zero applied bias. This means there is no built-in electric field. However, diffusion length of photo-excited charge carriers should be larger than the thickness of the superlattice (SL), in order to see any photocurrent. As conductivity of the superlattice is much less than that of the p-n junction, the same order of magnitude built-in potential as in the junction is hard to observe. Further more, a potential barrier for holes, which may exists at the nc-Si/a-SiO2 interface could also hinder movement of excess holes toward the Al contact.

Because of the qualitative difference between dc conductivity behavior at positive and negative bias at low temperatures, which is related to the respective transport of electrons and holes as was discussed above. DC conductivity at low temperatures for negative and positive biases will be discussed in the following section [3.2].

3.2 DC Conductivity at Low Temperature

3.2.1 Electron Current at Negative Bias

Figure 3.2 shows dc conductivity as a function of the applied negative bias for nc-Si/a-SiO_2 SL in a range of temperature from 15K to 300K. The starting point of the bias sweep was at the negative voltage of 1.5 V.

Several temperature ranges with qualitative difference in a dc current behavior could be selected. In the first region (I) from 299 K to 250 K, dc current decreases below 0.7 V and increases above 0.7 V with decreasing temperature. The experimental curves could be well – fitted by exponential laws (note semi-logarithmic scale). In the second temperature range (II) from 250 K to 190 K, dc current decreases with temperature below 1.0 V and remains constant above 1.0 V. As temperature decreases from 190 K to 125 K (third region, III), dc current decreases in the whole measured voltage range and becomes below our measurements capability of the electrometer below 125 K (forth region, IV). Surprisingly, an increase of the dc current (lines with symbols) is observed at temperatures below 30K (fifth region, V).

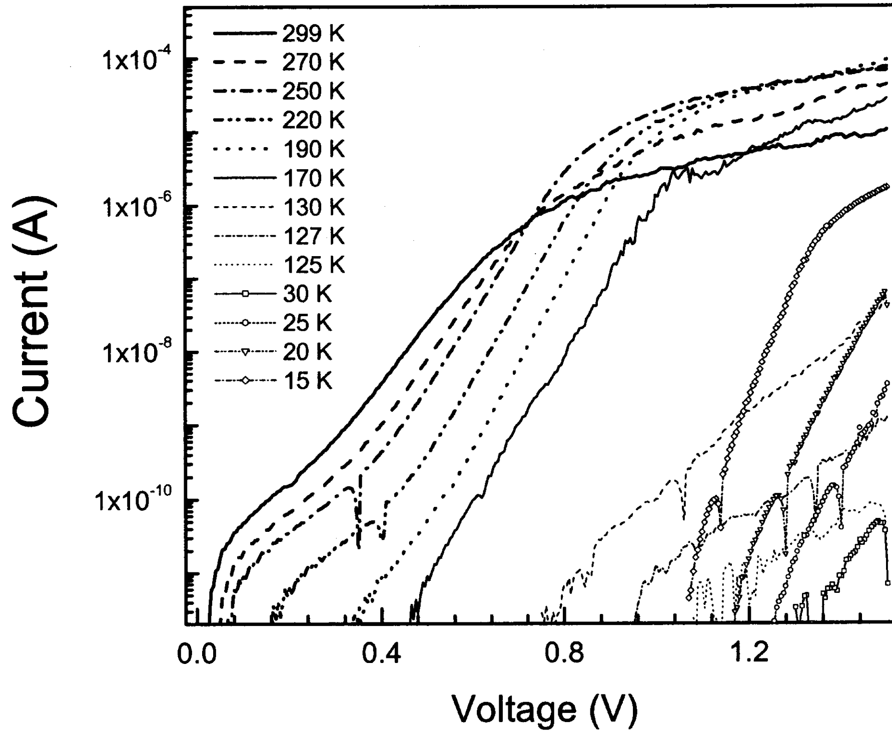


Figure 3.2 DC current – voltage characteristics of nc-Si/a-SiO_2 SL at different temperatures. The sweep of the applied bias was performed from –1.5 to zero.

The theoretical expression for the current density of a MIS tunnel diode is given by [10, 11]

$$J = A^{*}T^{2}e^{-\alpha_T \Phi_T^{1/2} d} e^{-\frac{q\Phi_B}{kT}} \left(e^{-\frac{qV}{kT}} - 1 \right) \qquad (3.1)$$

where A* - is the effective Richardson constant, α_T – depends on the effective mass of charge carrier in the insulator layer, Φ_T – tunneling barrier height, Φ_B – barrier height for Schottky emission.

As can be seen, this expression combines MS interface characteristic with tunneling factors. Independence of the tunneling component on temperature allows to use

temperature dependent measurements of dc current to determine the barrier height at V=0. And vice versa, for positive bias dependence on the electric field could be neglected (minority carrier transport in the surface space charge region, no barrier) and field dependence of the tunneling current may be separately considered. With the sweep of the applied bias change from -1.5 V to 0 V, the shift of the voltage value at which zero of current occur from 0V at room temperature to -1.3 V at 30 K, which shows strong charging effects at low temperatures. The trapped charge creates built-in electric field or interface dipoles that partially compensate an external electric field. It is observed that there are two extreme cases: near-zero bias at temperatures slightly below room temperature and at large negative bias (-1.5 V) in the whole measured temperature range. Charging effects do not change the interface potential significantly essentially at temperatures slightly below room temperature.

Figure 3.3 shows a plot of $\ln(J/T^2)$ vs. 1/T for determination of barrier height based on theory of Schottky barrier. A good approximation was obtained by a straight line which represents the Arrhenius behaviour. It is supposed that the potential barrier of 70 meV (derived from the plot) exists at the interface between the bottom of the conduction band in the n-Si and first nc-Si layer.

The dark dc current-voltage characteristics in Figure 3.1 and Figure 3.2 at 299K are different. No barrier for the experimental structure is observed in Figure 3.1. At high negative bias, the barrier at the n-Si/SL interface is straightened as well as there is no potential drop in the interface. Therefore, the properties of the hetero-structure at -1.5 V is related to the properties of the superlattice.

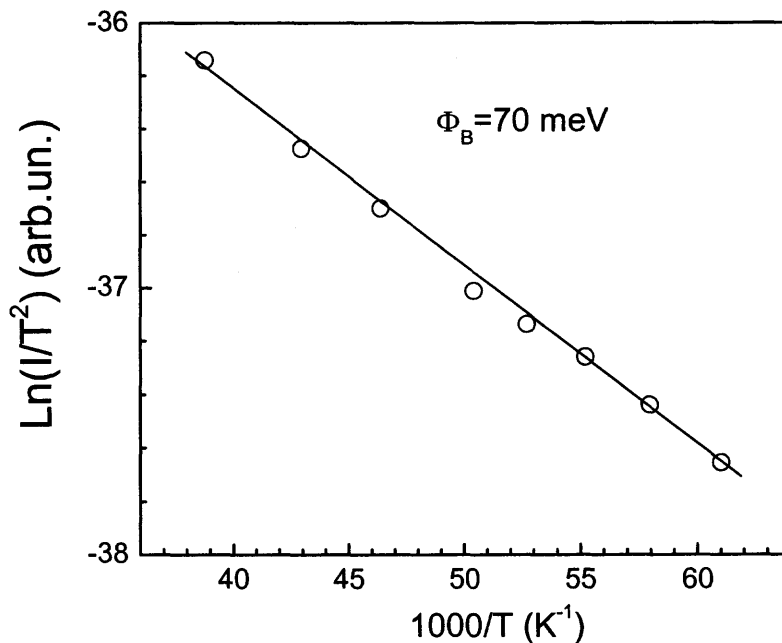


Figure 3.3 An Arrhenius plot of the dc current in the voltage range from 0 V to 0.4 V.

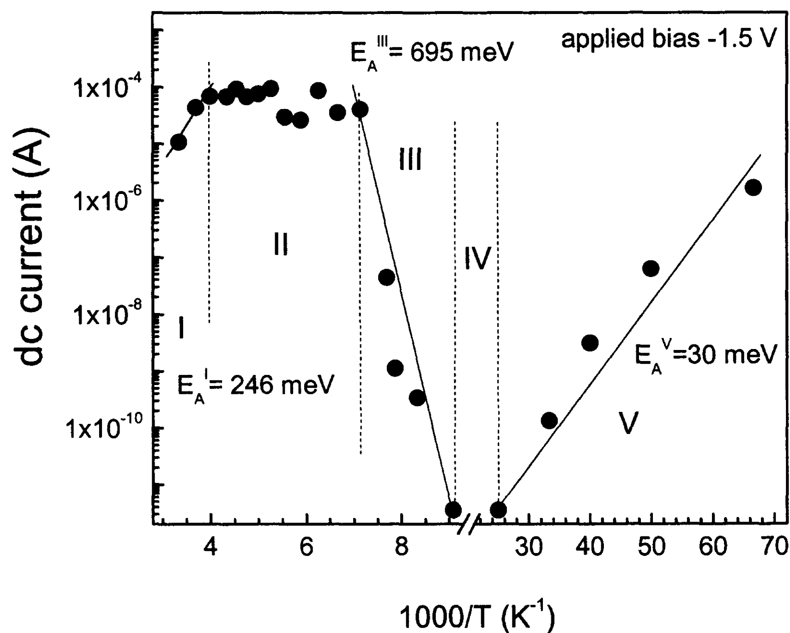


Figure 3.4 An Arrhenius plot of a dc current at the applied voltage of 1.5 V. The five temperature regions (see discussion to Fig.3.2) are marked.

Figure 3.4 shows an arrhenius plot of a dc current at applied voltage of 1.5 V. Five regions of temperature for the dc current are marked for discussion. In the region I, the dc current increases as the temperature decreases. The dc current is almost independent of temperaure in the region II. And the dc current decreases as the temperature decreases in the region III. And the current is so low that it is beyond the measurement capability in the region IV. In region V, the current increases linearly as the temperature decreases.

3.2.2 Separation of Electron and Hole Components at Positive Bias

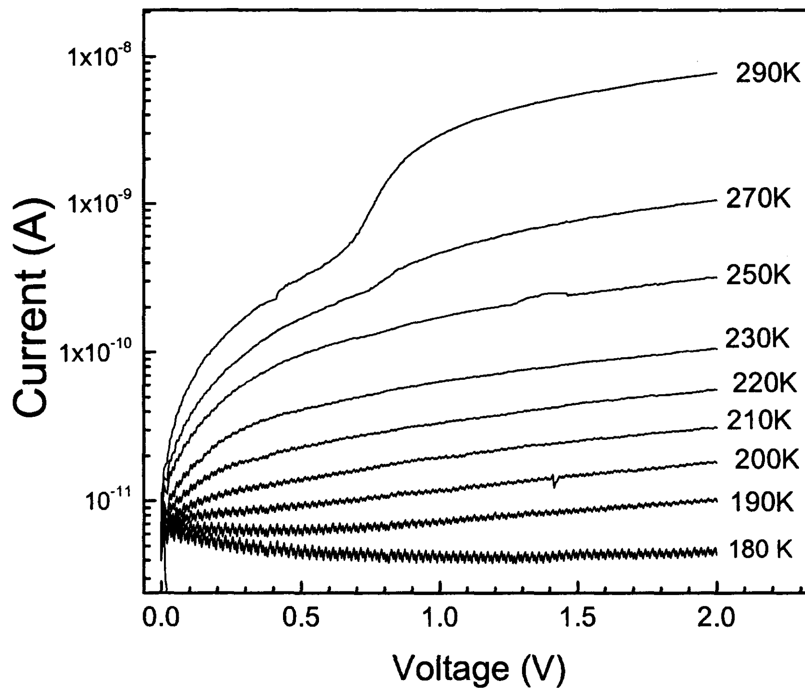


Figure 3.5 Dc current – voltage characteristics at positive bias for different temperatures.

Figure 3.5 describes the dc dark current measured for the voltage sweep from 0 to 2 V for different temperatures (180K-299K). Decrease of the dark current with decreasing temperature may be explained by the decrease in the electron carrier concentration in the metal and also due to the simultaneous decrease of the hole concentration in the semiconductor substrate. As it is difficult to determine the exact barrier height of the metal-superlattice interface due to the involvement of both the hole and electron transport, it cannot be known whether the decrease in the dc current is due to the decrease in hole concentration or electron concentration. Note that a dc current step exists at about 0.7 V at 270K and 290K. This increase of the current may be caused by an onset of the second current mechanism. In order to check this idea, activation energy is determined for the applied biases of 0.3V, 0.5 V, 1V, and 2 V.

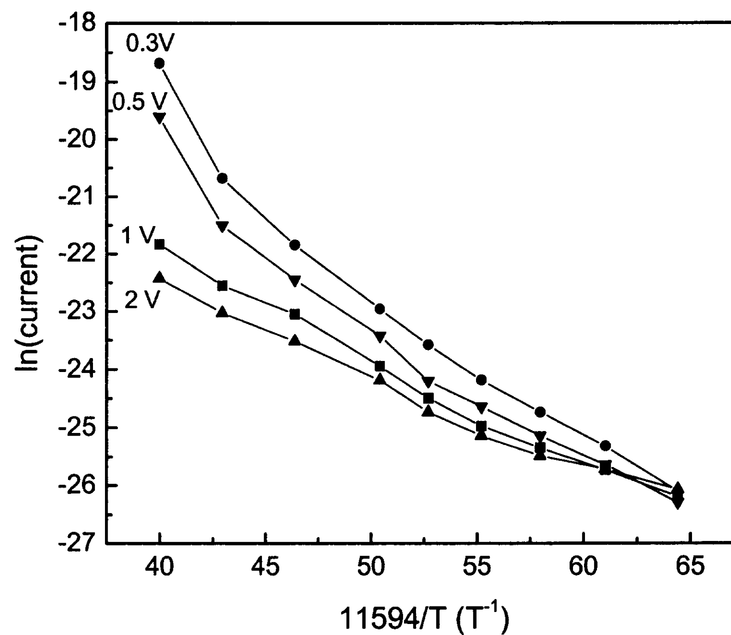


Figure 3.6 An Arrhenius plot of a dark dc current at positive applied bias of 0.3 V,0.5 V,1 V and 2 V.

An Arrhenius plot of the dark dc current for these voltages is shown in Fig.3.6. The logarithmic plot of current versus the inverse temperature for dc voltages of 0.3 V, 0.5V, 1V, 2V is graphed. The activation energy is the slope of the logarithmic scaled curves. The slope of the ln(I) vs 1/T gradually changes from 0.14eV at 0.3 V to 0.3eV for 2 V. This shows that the activation energies of the metal-superlattice-semiconductor structure changes gradually for varying dc voltages. And there is no difference in the activation energy variation for the bias voltage below and above 0.7 V where the step in current is observed in Figure 3.5.

3.2.3 Fowler-Nordheim Tunneling of Holes at Positive Bias

No difference between dark and photocurrent was observed for applied negative bias. Therefore, dc photocurrent will be discussed only for positive bias.

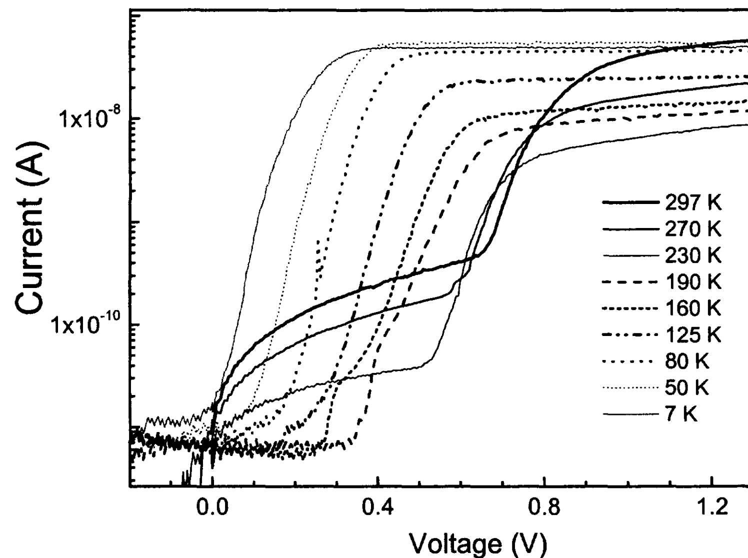


Figure 3.7 Dc photocurrent-voltage characteristics of nc-Si/a-SiO2 SL measured at different temperatures for positive bias on the substrate.

Figure 3.7 shows typical dc photocurrent-voltage characteristics of nc-Si/a-SiO_2 SL measured at different temperatures. Here, two regions of the characteristic current for bias voltage below and above 0.6v are observed. Below 0.6V, dc current is insensitive to light as discussed in section 3.1 and this dark current depends on the temperature in the way similar to that of dark current discussed before in section 3.2.1. The dc dark current decreases with decreasing temperature in the range from 300 K to 190 K and becomes impossible to measure for lower temperatures.

Above 0.6 V the behavior of the current is more complicated, as the current is the sum of dark component (equilibrium carriers) and photocurrent (photo-excited carriers). Dominating dark current is expected for temperatures close to room temperature. The current decreases in the temperature range from 300 K to 230 K. However, as temperature decreases further, an increase of the current is observed. With decreasing temperature, scattering of charge carriers on phonons decreases, increasing the mobility of charge carriers and therefore, the current. The increase of the photocurrent with further decrease of the temperature could be attributed to a reduced scattering of holes on the phonons.

A shift of the onset of photocurrent towards negative voltage with decreasing temperature can be observed. As starting point of the voltage sweep was at negative voltage, charging takes place. This is supported by the shift of zero-current point toward negative bias. Therefore, built-in potential due to the trapped charge at the interface shifts the voltage scale.

No decrease of the photocurrent with decreasing temperature shows that photocurrent is not thermally activated and tunneling of photo-excited charge carriers can be proposed as a transport mechanism.

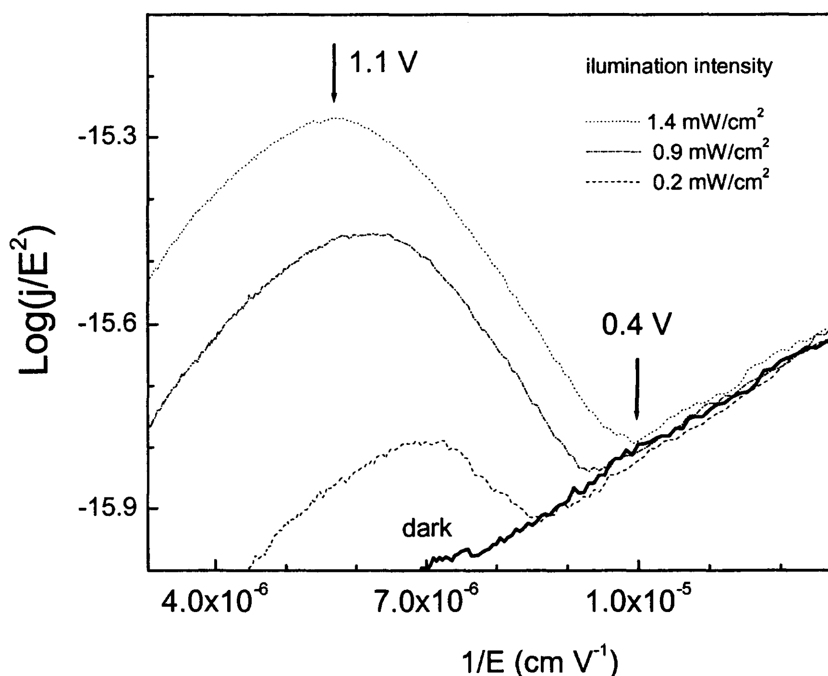


Figure 3.8 Fowler-Nordheim approximation of a photocurrent (Figure 3.1) for different illumination intensities.

A steep increase of the photocurrent above 0.6 V is suggested by transport of holes through a superlattice. The barriers of approximately 4 eV exist between Si nanoparticles. An expression of a theory for tunneling by Fowler and Nordheim is given in Section 1.3.1. Additional evidence for tunneling will be given in the dimensions of temperature dependent photocurrent transients (Section 3.5). The interception of the curves in Figure 3.8 with a vertical scale at 1/E would give a value of the potential

barrier. However, this procedure demands an exact knowledge of the current density, in this case the absolute current is used because the active area of the device is not really known. Assuming the active area of the device to be 0.02 cm^2 the non-realistically small value of 0.357 meV was obtained. If the area of the device was smaller, this would increase the value of the potential barrier. In order to get a more realistic value, the area for tunneling current should be much smaller than the contact one. This means, only certain chains of nano-particles constitute the transport chains [15].

Tunneling probability for triangular and parabolic barriers has been calculated [6]. Both the expressions contain reciprocal exponents of electric field, which could be considered as general (independent of a barrier shape). The exact expression for the constant in the exponent power strongly depends on the shape of the barrier. Therefore for the extraction of the barrier height the knowledge of the barrier shape is necessary, while to prove tunneling only field dependence may be enough.

In a wide range of the photocurrent in the voltage range from 0.4 to 1.1 V, the photocurrent divided by square of the electric field increases linearly, which suggests tunneling of excess holes through the superlattice.

3.3 Nature of the ac Photoconductivity Resonance

Figure 3.9 shows the ac differential conductivity of the Si/SiO_2 superlattice at modulation frequency of 400 Hz and illumination intensity of 0.43 mW/cm^2. There are three maxima observed in the curve at –0.71V, -0.029V and 0.81V successively. In these measurements a 400 Hz ac voltage with amplitude of X V was applied. The first two maxima at –0.71V and –0.029V are the same when measured in dark and under illumination. But the

third maximum 0.81V is observed only under illumination. The insert shows that the photoconductivity increases from 0.51μS to 1.75μS for an increase in the illumination from 0.1 to 1.13mW/cm^2 respectively. Measured ac conductivity vs. applied bias is in good agreement with the dc conductivity measurements (compared to Figure 3.1).

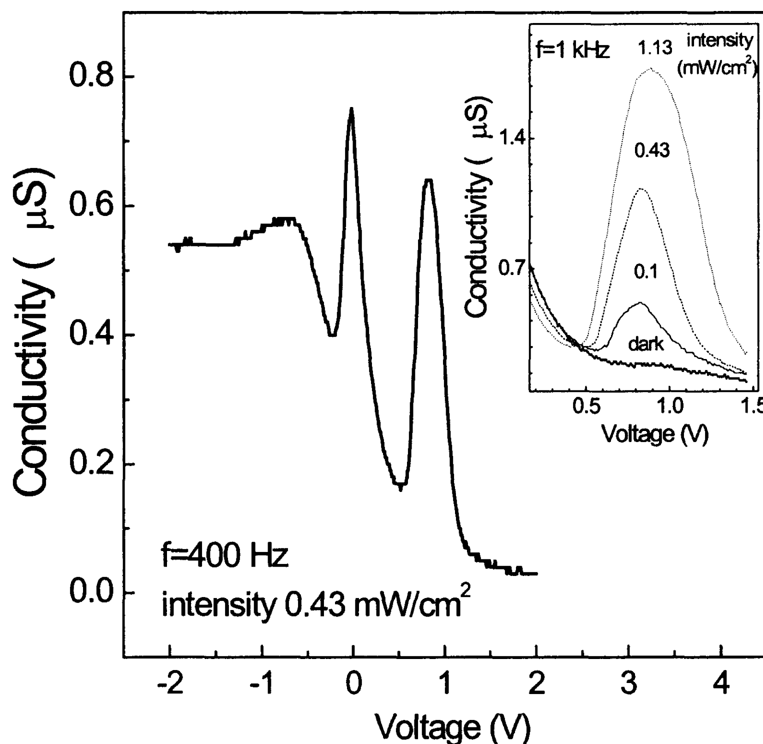


Figure 3.9 AC differential photoconductivity of Si/SiO2 superlattice at modulation frequency of 400 Hz and illumination intensity of .43 mW/cm^2. Insert shows ac photoconductivity for different illumination intensities at modulation frequency of 1 kHz. Dark ac conductivity is shown for comparison.

The first maximum in the Figure 3.9 can be explained like this. The potential barrier for the metal-superlattice contact decreases for the increasing negative voltage applied resulting in an increase in the conductivity of the structure. And further increase in the negative voltage leads to a saturation of the ac conductivity. The properties of the electron current in the SL were discussed for Figure 3.4. The appearance of the second

maximum is related to the loss of energy of applied ac voltage on interface traps between the silicon substrate and the Superlattice. Majority carriers (electrons) are captured and emitted changing the occupancy of the interface trap levels on the surface causing an energy loss at frequencies close to inverse value of their time constant. A Fermi level of semiconductor at the interface should cross the energy position of interface states. Therefore, a narrow maximum in ac conductivity vs. voltage shows narrow energy distribution of interface states. A frequency dependence of the ac conductivity can give time response constant of the traps and will be shown later. And the third maximum is due to the photoconductivity resonance caused by the alignment of the energy levels in c-Si, nc-Si/SiO2 SL and Fermi-level in Al contact.

An extraction of the density of interface states and time constant is possible from the frequency dependence of the second ac conductance peak. But prior behavior of the surface band bending and condition of the surface space charge region (accumulation, depletion or inversion) at a given applied bias should be understood. This information could be obtained from the complementary measurements of the capacitance as a function of the applied bias. These data are given in the following section.

3.3.1 Depletion of the Hetero-Structure at Positive Bias

Figure 3.10 describes the capacitance measured for the frequency of 1KHz as a function of the bias voltage applied to the Al-nc-Si/SiO2 SL –c-Si structure for different illumination intensities. There are several maxima observed for these curves.

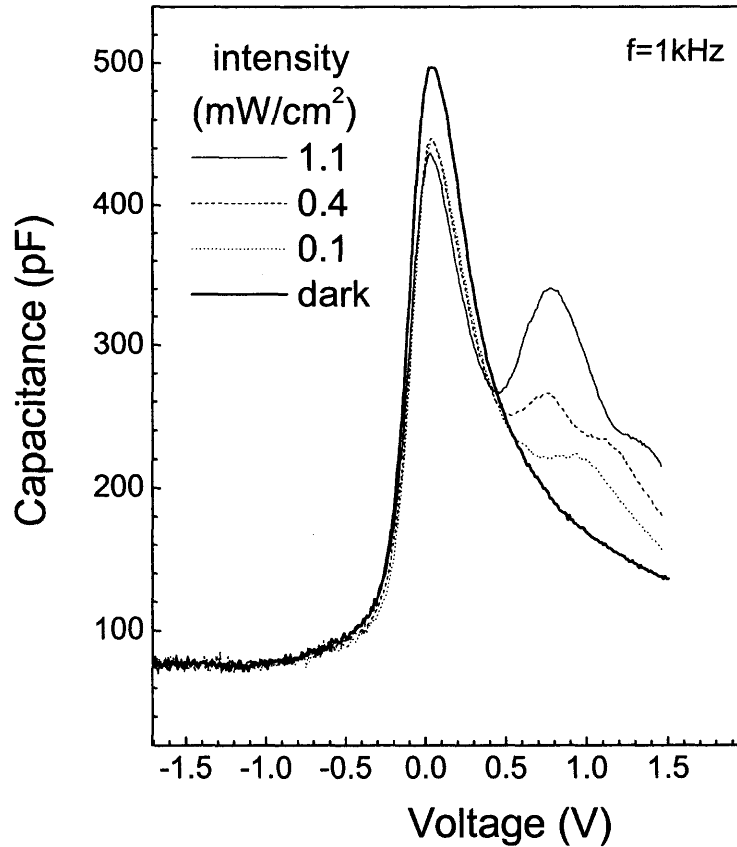


Figure 3.10 Capacitance-Voltage curves of the metal-superlattice-semiconductor for different illumination intensities measured for a frequency of 1 KHz.

The equivalent capacitance of the structure is a series of superlattice capacitance C_s and the capacitance of an interface space charge in depletion region C_d.

$$C_{eq} = \frac{C_s C_d}{C_s + C_d} \qquad (3.2)$$

The first maximum appears in all the curves for the dark and for the illumination. The curve for the dark has no other maximum but a shoulder at higher voltages. The first maximum is explained for these curves as follows. For small negative voltages, the depletion of interface space charge region (SCR) changes to accumulation extending the

width of the SCR and therefore, dramatically decreasing C_d. The total capacitance of the structure equals the depletion capacitance as C_s>>C_d. No injection of charge carriers from c-Si into SL was observed at small positive voltages. The capacitance of the SL can be considered as constant with voltage and for positive voltages, the equivalent capacitance is similar to that of the metal-insulator–semiconductor structure capacitance. As capacitance of SCR decreases with increasing positive bias, the equivalent capacitance also decreases. Saturation of the equivalent capacitance is expected at voltages where depletion is changed to inversion. No saturation at higher voltages for frequencies of 1 KHz was observed and interface SCR is in depletion region for the applied voltages up to 1.5 V. The redistribution of the applied voltage between SL and SCR is the reason for depletion of SCR at such a high voltage.

The domination of C_s and C_d in their respective regions can be justified from the following analysis. The capacitance of the interface space charge region of a metal-semiconductor interface is given

$$C = \sqrt{\frac{q \in_s N_D}{2\left(V_{bi} - V - kT/q\right)}} \qquad (3.3)$$

where q – electronic charge,

ε_s - permittivity of the semiconductor

N_D-donor concentration

V_{bi}-built in potential

V-applied voltage

kT-thermal voltage

Doping profile can be given from (3.3)

$$N_D = \frac{2}{q \in_s} \left[-\frac{1}{d(1/C^2)/dV} \right] \tag{3.4}$$

The doping profile of the semiconductor can be obtained by the differential capacitance method by plotting the differential of $1/C^2$ (C(V) curve is shown in Figure 3.10) as a function of voltage. Hence the doping profile (N_D) can be plotted as a function of bias voltage as shown in the Figure 3.11.

The doping profile (squares) measured under dark is clearly seen as a constant at $N_D = 1.1 \times 10^{15}$ through out the voltage range which is equal to the donor concentration of the n-type Si substrate. The deviation of $N_d(V)$ from the horizontal line (constant doping level) under illumination shows that the capacitance of the SL can not be neglected in this case and theory for the capacitance of metal-semiconductor interface is not applied. However, an increase of the equivalent capacitance at 0.5 V and 1.2 V (Figure 3.10) and respective increase in a charge carrier concentration (Figure 3.11) shows an injection of excess holes from the c-Si substrate into the SL in between these two maxima and above the second maximum.

The second and third maxima in the C(V) plot at higher voltages can be explained by the resonant tunneling of holes from the semiconductor through the superlattice in the structure in between the second and third maxima and at voltages above the third maximum. The capacitance of the total structure equals the superlattice capacitance as $C_d >> C_s$. The resonant tunneling is explained by the alignment of the energy levels in the quantum wells of the Si/SiO_2 superlattice. This phenomenon explains the successive second and third maxima in the capacitance–voltage curve in Figure 3.10. For positive

bias, the minimum in between the second and third is related to the alignment of the first energy

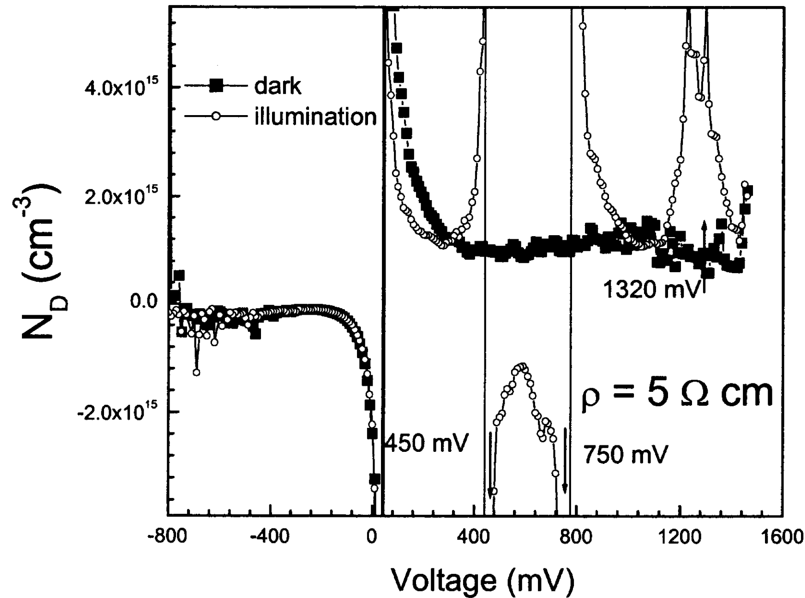


Figure 3.11 Doping profile of the n-Si-(Si/SiO_2) structure as a function of voltage.

levels of the quantum wells in the superlattice. Further increase in the positive bias leads to the misalignment of the first and second energy levels of the successive quantum wells, which explains the still decrease after the third maximum in the curve.

AC conductivity due to interface states strongly depends on the frequency of the applied ac signal.

3.3.2 Analysis of the Parameters for the Interface Traps

Figure 3.12 shows the ac conductance as a function of the frequency for nc-Si/a-SiO_2 SL. A maximum in ac conductance is clearly observed at frequency of 5200 Hz for applied bias of 1.5 V. The frequency at which the ac conductivity maximum appears decreases with decreasing bias and only a shoulder appears for 0.7 V and 0 V.

The change in the occupancy of the interface traps with frequency best explains the shape of the curves[12-15]. At low frequency (with respect to inverse trapping/detrapping time) interface traps change occupancy according to the applied ac gate voltage maintaining equilibrium. Therefore, there is no energy loss and ac conductance due to interface states is zero. As frequency increases, energy loss occurs as the interface traps lag behind the ac gate voltage and this causes an increase in the conductance. The conductance value goes on increasing until it reaches the maximum. As frequency increases further, the response of interface traps decreases thus decreasing the energy loss and the value of conductance.

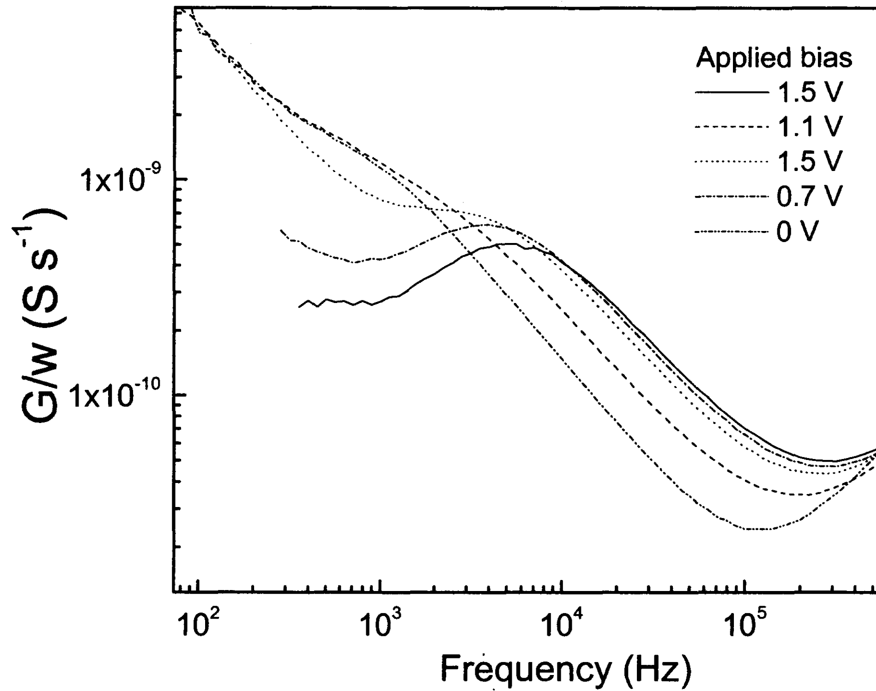
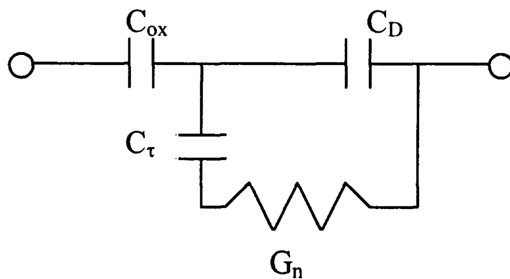
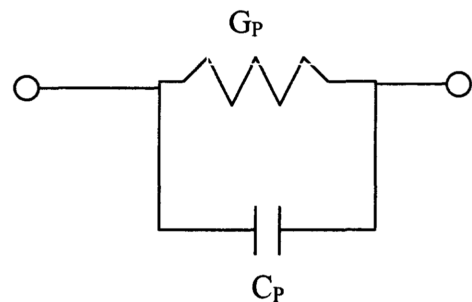


Figure 3.12 AC conductance over frequency as a function of frequency for several applied biases.

As referred to the discussion of Figure 3.10, the interface between c-Si and SL is in depletion. The equivalent circuit of the interface in depletion is shown in Figure 3.12(a).





(a) (b)

Figure 3.13(a) Equivalent circuit of the Al-Si/SiO_2-n-Si structure in depletion. (b) Parallel conductance and capacitance of the Al-Si/SiO_2-n-Si structure in depletion.

The admittance of the structure in Figure 3.12(a) becomes

$$Y_s = j\omega C_D + j\omega C_T G_n \left[G_n + j\omega C_T\right]^{-1}$$

Y_s consists of the depletion layer capacitance shunted by series combination of C_T and G_n The equivalent circuit given in Figure 3.13 (a) can be presented in terms of the equivalent parallel conductance G_p and capacitance Cp, given in Figure 3.13(b), that are related to the initial parameters as

$$\frac{G_p}{w} = C_T \frac{w\tau}{1+(w\tau)^2} \tag{3.5}$$

Figure 3.12 has a maximum at wτ=1 and the value of Gp/w at maximum is equal to $C_T/2$. The density of traps involved into ac conductivity [9] at applied voltage of 1.5V is given by

$$D_{it} = \frac{C_T}{qA} = 3.75\text{x}10^{11} \tag{3.6}$$

The trapping/de-trapping time of interface states near the Fermi-level at the applied voltage of 1.5V is given by

$$T=1/f=1/5170=3.1\text{x}10^{-5}\text{ s} \tag{3.7}$$

As the frequency at which the maximum appears decreases and the absolute value of maximum increases for decreasing bias, the trapping/de-trapping time and density of interface state increases.

3.3.3 Photocurrent Transients as a Measure of Transit Time

The conductivity of a semiconductor is a function of density and mobility of charge carriers

$$\sigma = qn\mu \qquad (3.8)$$

Where q - electronic charge, n – density of charge carriers, and μ - mobility of charge carriers

From the definition of mobility, it is the coefficient of the velocity of charge carriers V and the electric field E.

$$V = \mu E \qquad (3.9)$$

Also, the velocity of the charge is inversely proportional to the time if the distance is constant. Therefore, decay time of a photocurrent can serve as a characteristic time for a flight of photo-generated charge carriers through a SL.

Figure 3.14 describes the photocurrent as a function of time in nc-Si/a-SiO2 SL for several applied voltages at room temperature. The photocurrent is measured with the Al-Si/SiO_2/n-Si structure excited with a laser pulse (wavelength 690nm and duration 430 ns).

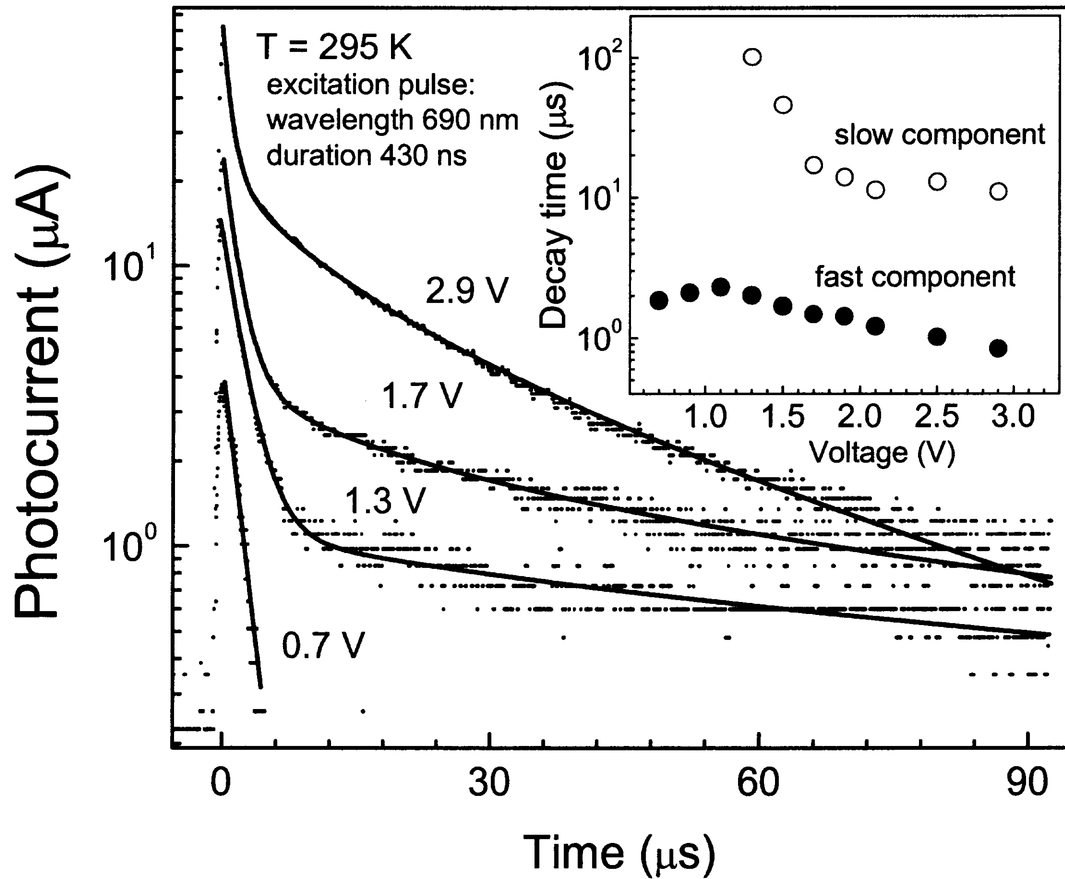


Figure 3.14 Measured photocurrent (symbols) and as a function of time in nc-Si/a-SiO2 SL for several applied bias and fit of the curves by expression (3.10).

The experimental curves are fitted by a sum of mono-exponential and stretched exponential decays

$$I_{ph} = A_1 e^{-\frac{t}{\tau_1}} + A_2 e^{-\left(\frac{t}{\tau_2}\right)^{\beta}} \tag{3.10}$$

where A1 and A2 are amplitudes and τ1 and τ2 time constants of the photocurrent.

Two components (with respect to decay time) are present in the photo current curves – slow component and fast component. The transient time for these components varies for different bias applied as shown in the insert to Figure 3.14. The decrease of conductivity from the third maximum toward positive bias (Figure 3.10) is justified by the increasing ratio between slow and fast components for increasing bias from 0.7 V to 2.9 V. The decrease of the slow component is much more pronounced than that of the fast components. This shows that the conditions for the photocurrent mechanism described by the slow component are more preferable at higher voltages.

Tunneling of holes was assumed as a transport mechanism of holes in nc-Si/a-SiO2 SL. The energy band diagram of the tunneling mechanism is given further in section 3.3.4. Temperature dependence of photocurrent decay can give information about transient time at different temperatures. Figure 3.15 describes the photocurrent as a function of time for temperatures of 90 K and 4.2 K at a fixed applied bias of 0.75V.

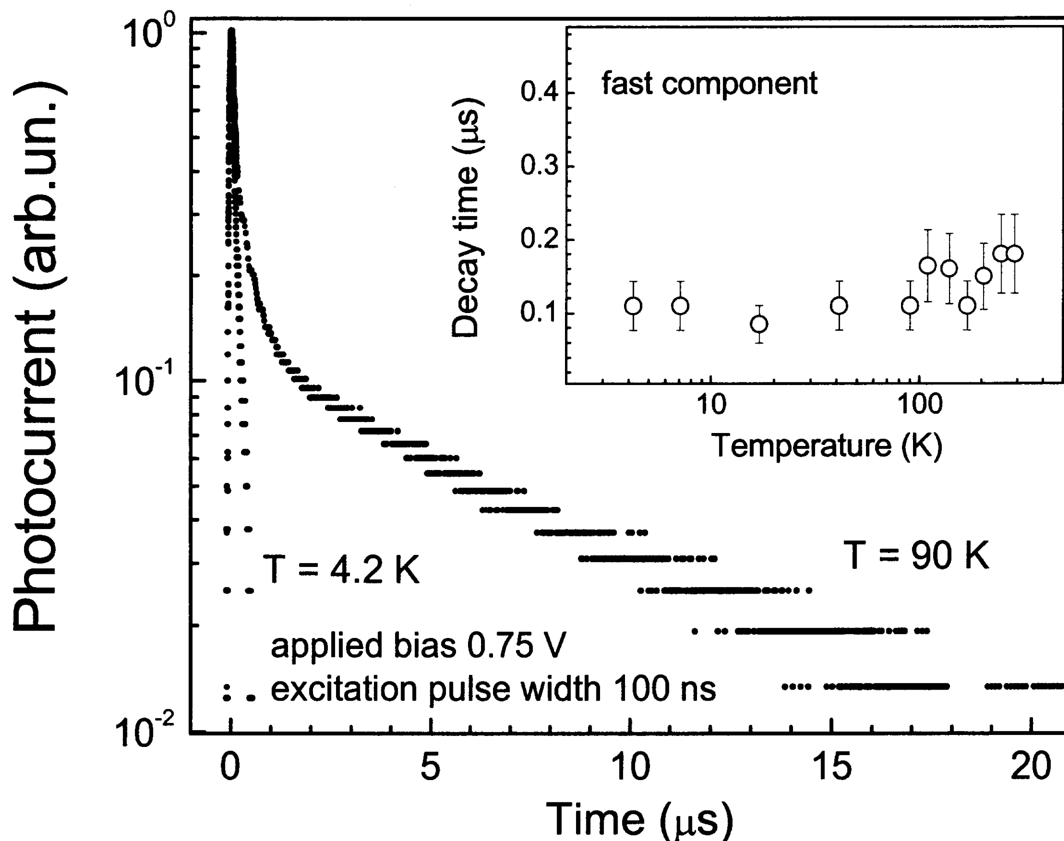


Figure 3.15 Photocurrent as a function of time for different temperatures.

The fast component in photocurrent decay as a function of temperature is given in the insert to Figure 3.15. This fast component is almost independent of temperature, and therefore can be associated with tunneling. Hence, it is concluded that resonance tunneling with fast time constant (100 ns) is the carrier transport process in the Al-Si/SiO_2-n-Si structure. The independence of the fast component with temperature proves that the main conduction mechanism is the resonant tunneling in the superlattice. The decay time of the slow component, on the other hand, is temperature dependent, its absolute value changes from 50 μs at 1.5 V to 10 μs at 2.9 V. The temperature

dependence of the slow component is not monotonical function of temperature. The decay time constant of the slow component is very close to the time constant of interface traps of 31 μs at 1.5 V and their voltage dependence (decrease with increasing bias). Therefore, slow component of photo-current can be related to the interface traps.

3.3.4 Resonance Tunneling of Holes in nc-Si/a-SiO_2 Superlattice

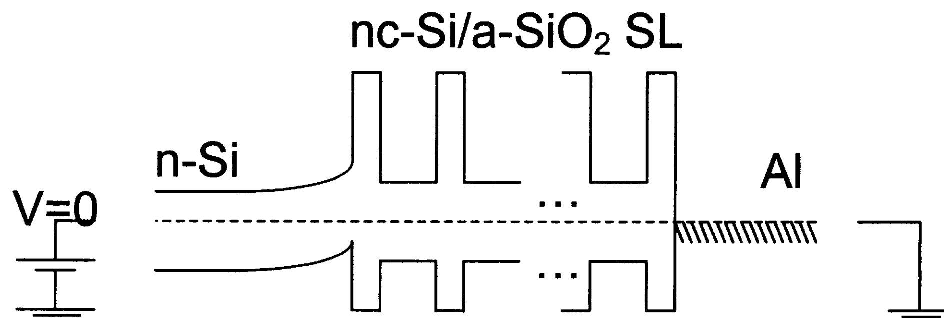


Figure 3.16 Energy band representation of the Al-(nc-Si/a-SiO_2 SL)-n-Si for no voltage applied to the substrate.

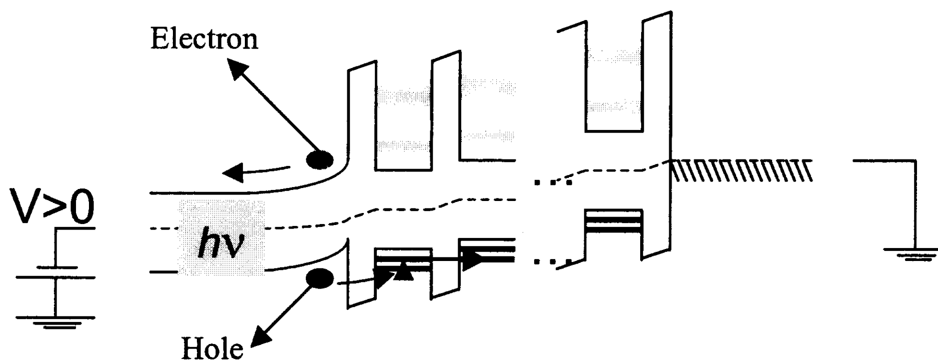


Figure 3.17 Energy band representation of the Al-(nc-Si/a-SiO_2 SL)-n-Si for a positive voltage applied to the substrate.

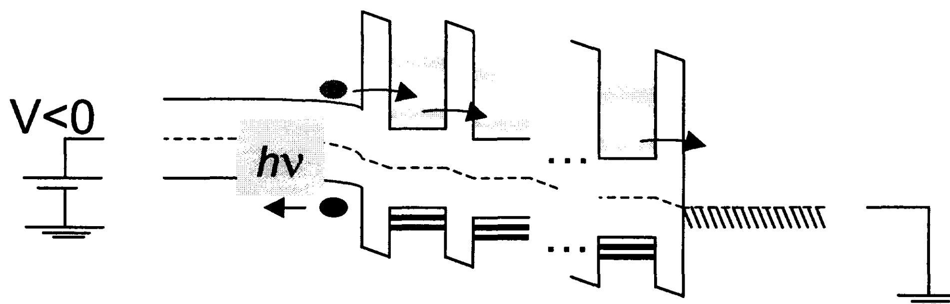


Figure 3.18 Energy band representation of the Al-(nc-Si/a-SiO_2 SL)-n-Si for a negative voltage applied to the substrate.

The energy band diagram of the heterostructure is shown in Figure 3.16 when there is no voltage applied to the substrate. When a positive voltage is applied to the substrate, the Fermi level of the substrate lowers with respect to the Fermi level of the Aluminum. The energy levels of the Si/SiO_2 superlattice align so that the electrons from the Aluminium tunnel through the energy levels to the substrate and holes from the substrate tunnel through the energy levels to the Aluminium. When a negative voltage is applied to the substrate, the energy levels of the Si/SiO_2 align themselves such that the holes from the substrate tunnel through the energy levels to the substrate and electrons from the substrate tunnel through the energy level to the Aluminium.

CHAPTER 4

CONCLUSIONS

The electron component at negative bias and hole component at positive bias above 0.6 V were found to be dominating in the current through nc-Si/a-Si superlattices with 8 bi-layers. A potential barrier of 70 meV exists at the interface of c-Si substrate and SL. Electron transport is thermally activated and several activation energies of dark dc current were determined. The tunneling mechanism is proved to be the leading hole current mechanism in the nc-Si/a-SiO_2 SL at positive bias. The unusual increase of the dc photocurrent at 0.6V and the maximum of the ac conductivity at 0.8 V suggest the onset of hole tunneling due to alignment of the energy levels in the c-Si/nc-Si/SiO_2/Al heterostructure. The time of photocurrent decay, which can be used as a measure of the operation speed of memory cell, can be varied in a range from 100 ns for aligned energy levels in resonance to 100 μs for the system out of resonance. The conductivity due to the interface traps with a density of 3.75×10^{11} cm^2 and trapping/detrapping time of 30μs was determined at the interfaces of the superlattice. This path is competing with the charge carriers tunneling through the heterostruture and should be blocked for proper operation of the memory cell.

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