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ABSTRACT

STUDY OF MOSFET DEGRADATION UNDER SUBSTRATE INJECTION AND HOT CARRIER DEGRADATION

By Bhawar Patel

With continued scaling of MOSFET's, the reliability of thin gate oxides is becoming increasingly important. Degradation issues due to fabrication technology may result in misinterpretation unless the actual physical situation arising at source, drain, gate and substrate of a transistor during processing is understood. This degradation is prominent in plasma processing due to wafer charging which occurs due to the reactive ions in the plasma. The voltages developed at source and drain junctions, depending upon polarity relative to the substrate cause the source and drain junctions to be forward biased or reverse biased. Keeping in view this type of physical situation arising at the source and drain junctions, this thesis reports the effects of reverse biased potential at source and drain junctions of a nMOSFET during high-field substrate injection and its impact on device parameters such as transconductance, threshold voltage and hot carrier degradation.

For the present study n-MOS transistors processed using 0.25 μm technology were used for study. Transistors were subjected to about 400mA/cm^2 constant current stress for three seconds using substrate injection mode, while applying potential at the source and drain to simulate reverse bias condition created by plasma charging. While applying potential at the source and drain, hot carrier lifetime based on 10% threshold voltage and transconductance degradation of the transistors were measured.

Experimentally it was observed that threshold voltage prior to stress was lower than threshold voltage after stress indicating dominant electron trapping. Since the device

is in strong inversion during stress, an increase in reverse biased voltage at the source and drain, will form the channel in the center of the device due to the depletion regions of source and drain junctions. Results show the hot carrier lifetime based on transconductance shift decreases after current stress. It shows an improvement when the reverse bias is at 1V and further degrades when reverse bias increases to 2V. These results clearly indicate that the source – drain depletion regions formed by reverse bias affect hot carrier lifetime.

STUDY OF MOSFET DEGRADATION UNDER SUBSTRATE INJECTION AND HOT CARRIER DEGRADATION

by
Bhawar S. Patel

A Thesis
Submitted to the Faculty of
New Jersey Institute of Technology
in Fulfillment of the Requirements for the Degree of
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Department of Electrical and Computer Engineering

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APROVAL PAGE

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Dedicated to my wife, Mittal.

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CHAPTER 1

INTRODUCTION

1.1 Overview

The study of Silicon-Silicon Oxide ($Si\text{-}SiO_2$) interface involves an understanding of semiconductor structure, doping, fabrication principles and their associated electrical properties. The $Si\text{-}SiO_2$ interface plays a vital role in all the MOSFET (Metal Oxide Semiconductor Field Effect Transistor) devices used in modern integrated circuit (IC) due to their characteristic behavior. A study in the interface properties leads us to these characteristics, some of which are explained in this thesis.

The trend in electronics is towards continuous scaling down of semiconductor devices into the sub micrometer range to reduce the physical size of IC's and power consumption. This in turn calls for the use of very thin gate oxides in these devices. For most MOS (Metal Oxide Semiconductor) applications, the primary dielectric is silicon dioxide. The reliability of very thin gate oxides thus becomes an important concern.

The performance and characteristics of MOSFET devices, containing an oxide layer as an integral part of the device, are intimately related to the nature of the silicon-silicon oxide interface. This interface represents the transition from the tetrahedral structure of silicon to the polyhedral structure of silicon dioxide. The interface is commonly characterized by a number of dangling bonds, because they represent positions in the silicon lattice where the silicon valencies are unfulfilled. These dangling bonds degrade the performance of the device. There also exist at the interface a number of charged states due to fixed and mobile charges. All of these result in undesirable behavior

of thin-gate oxides, particularly under conditions of high current, voltage or temperature stress.

Some of the modern VLSI (Very Large Scale Integration) processes also induce defects and charging effects that degrade the oxide quality. Charge retention is of key concern where non-volatile memories, such as EPROM's, are used to store information in microelectronic circuits. Non-volatile memories are programmed by storing electrons on a floating gate. These electrons must remain on the floating gate throughout the product life. Plasma induced damage and contamination in RIE processes have been studied extensively in VLSI processes. Most plasma-induced damage is done to gate oxides, resulting in transistor threshold voltage shifts [1].

Charging damage decreases when the gate oxide gets thin [3]. The thinner oxide has much larger charge to breakdown. Since the current supplied by the plasma is limited [4], the higher charge to breakdown helps thinner oxide to better withstand the charging current. Older plasma equipment fit the low ion current, high charging voltage category. Modern plasma systems usually have much higher plasma density and are much more uniform. High-density plasma can supply ion current up to $20 mA/cm^2$. Keeping the antenna ratio of 1000:1, the maximum charging current density can be as high as $20 A/cm^2$. At the same time, the voltage that the plasma can support is usually much lower. The high current and low voltage characteristic of modern plasma is the main reason for making thinner oxide more prone to charging damage [2].

1.2 Objective

This thesis seeks to investigate the MOSFET degradation under substrate injection and hot carrier degradation. The study takes the following approaches:

1. Characteristics of nMOSFET's under application of current stress and its relation to Hot Carrier Degradation (HCD) of the gate oxide.
2. Study the oxide degradation with substrate injection while drain and source are reverse biased and its impact on HCD.

This thesis deals with understanding of MOSFET degradation, origin of degradation and characteristics under plasma charging damage.

The second chapter in this thesis presents background of the MOS transistor and gate oxide. The third chapter discusses the various gate oxide degradation processes during device fabrication. The experimental setup is described in chapter four. The measurement results are outlined and discussed in chapter five. Finally, chapter 6 concludes this thesis.

CHAPTER 2

BACKGROUND

This chapter explains charges present in the oxide and at the interface. The effects of such stored charges on the operation of MOS capacitor and transistor. The different modes and capacitance associated during biasing the MOS capacitor operation are also explained. The degradation conditions that cause the maximum damage to the Si-SiO_2 interface is explained and used in the chapter 5 to perform experiments. Different methods to measure the threshold voltage are explained in Section 2.5.

2.1 Fixed Oxide Charge and Interface Traps

The gate oxide consists of a fixed amount of charge depending upon the thickness of the oxide. This charge affects the operation of the device. The flat band voltage shift due to this charge, Q_f is given by:

$$V_{FB,shift} = -Q_f / C_{ox} \tag{2.1}$$

Where Q_f is in coulombs per square centimeter and C_{ox} is the oxide capacitance in farads per square centimeter. The above equation is also applicable to any sheet-layer charge that exists right at the oxide-semiconductor interface. Since Q_f always a positive charge, the flatband shift caused by it is always negative. Typical values of the $V_{FB,shift}$ from Q_f are -0.5V.

Interface traps are electronic states that reside at the oxide-semiconductor interface. In fact, they are the results of dangling bonds. However, unlike Q_f, rather than

having a fixed charge, interface traps are charged or discharged (positive or negative, depending on whether the states are donor-like or acceptor-like) with changes in band bending. Interface traps are electronic states situated within the band gap. Of course it is very possible that they also exist within the conduction and valence bands but are indistinguishable by measurement from the large density of band states. Rather than being a single discrete energy level, interface traps are a continuum of energy levels; thus they are quantified as interface trap density D_{it} with a unit of number of states/(cm^2.eV). Good modern MOS processing can produce devices with a D_{it} of ~10^{10} cm^{-2} .eV.

To visualize the effect of interface traps on the CV plot, refer to Figure. 2.1, which shows p-type silicon with donor like states uniformly distributed at the surface. In Figure 2.1a with the device in accumulation, all the interface traps would be positively charged. This charge results from the fact that states below the fermi level are considered filled with electrons (donors remain neutral), while states above the fermi level are considered emptied of electrons (donors become charged). As the device moves toward inversion, the amount of positive charge at the surface reduces to a minimum.

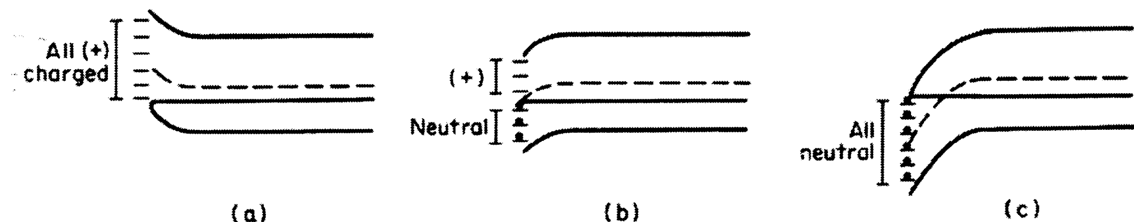

Figure 2.1 Effect of interface traps (Dewitt G. Ong [26]).

2.2 MOS Capacitor

The metal oxide semiconductor (MOS) capacitor is one of the basic structures to study the Si-SiO_2 interface properties. A very thin layer of SiO_2 is deposited by dry oxidation process (for good quality oxide layer) on the silicon substrate. On application of potential on the oxide layer we get capacitance across the structure. There are basically two types of capacitance associated with a junction:

1. Junction capacitance due to the dipole in the transition region
2. Charge storage capacitance arising from the lagging behind of voltage as current changes due to charge storage effects.

The MOS capacitor structure is shown in the Figure 2.2.

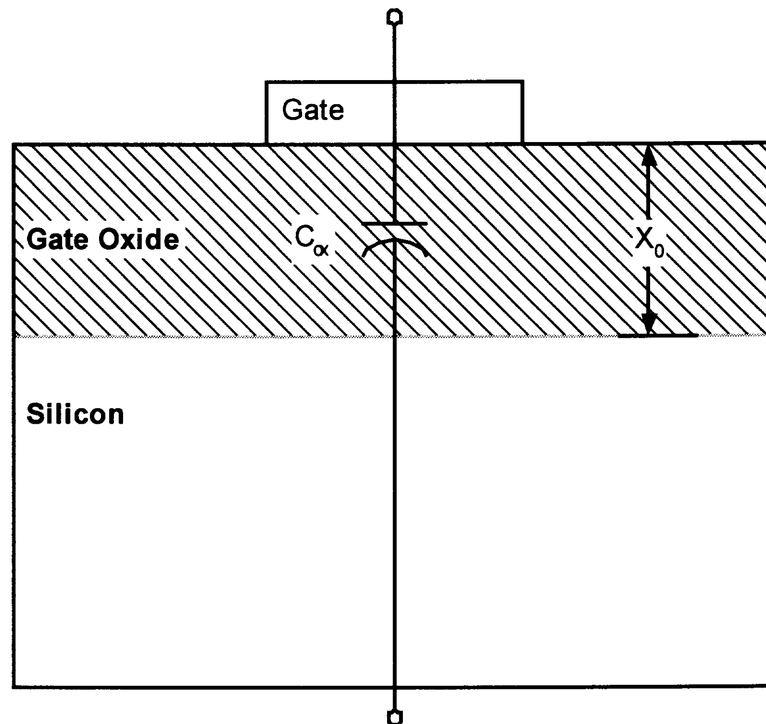

Figure 2.2 MOS Capacitor.

Where C_{ox} is the capacitance of the oxide given by the equation

$$C_{ox} = \frac{\varepsilon_{ox}}{X_0} \tag{2.2}$$

Where Xo is the oxide thickness

Substrate capacitance is given by C_s that is due to the applied potential. Operation of the MOS capacitance under different potential conditions is now described. The capacitances vs. applied potential curves are shown below which give behavior of MOS capacitor for different potentials. When negative charge is applied on the gate, equal positive charges accumulate at the Si-SiO_2 interface. When the p type substrate is used this occurs by hole accumulation at the Si-SiO_2 interface. Figure 2.3 shows the phenomenon.

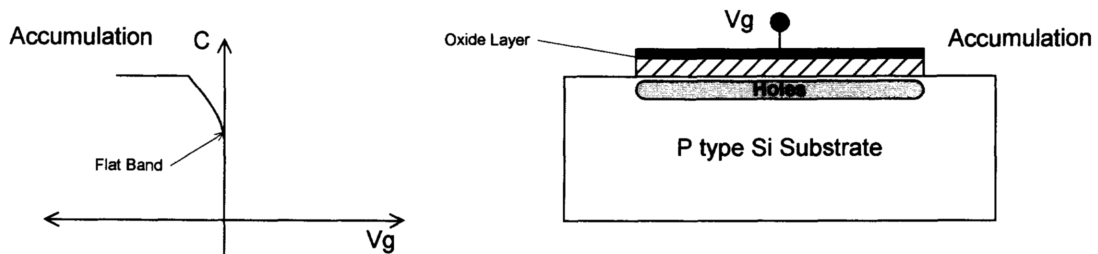

Figure 2.3 MOS capacitor in accumulation.

At this time, the capacitance across the structure is completely made up of the capacitance due to the oxide i.e. C_{ox}. As the potential is increased from negative to a value closer to zero, the holes accumulated near the interface start getting repelled. This

is caused as the field near the interface changes from being more negative to less negative. It therefore causes fewer holes to be attracted near the interface. However the holes that are repelled do not go back into the substrate in a uniform manner. As the potential changes from negative to positive, the polarity of the field near the interface changes and pushes all of the positive carriers i.e. holes away from the interface. The distance the holes are pushed away depends on the strength of the field near the interface due to the charge at the contact. As the field gets stronger, the holes are moved deeper into the substrate. Therefore the interface gets depleted of the holes due to the positive potential change. This stage is called depletion. The overall capacitance of the structure actually decreases due to the depletion layer capacitance added in series to the oxide capacitance. The depletion region is shown in the Figure 2.4 below:

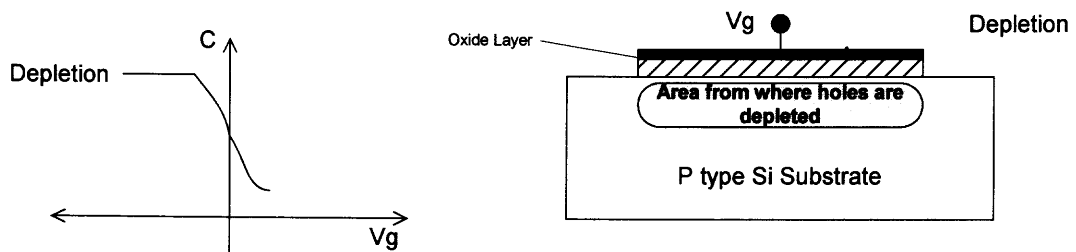

Figure 2.4 MOS capacitor in depletion.

The capacitance across the MOS structure decreases as the width of the depletion region increases until inversion is reached. As the field across the interface becomes stronger, it attracts more electrons near the interface. At sufficient potential, electrons

occupy the depleted region. That is why this stage is called inversion i.e. inversion of carriers occurs at the interface. The inversion stage is given in Figure 2.5.

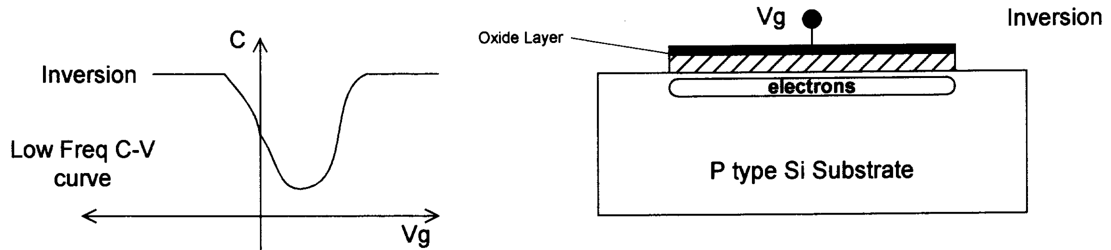

Figure 2.5 MOS capacitor in inversion.

The above figure shows the characteristics of capacitance vs. voltage for low frequency measurements. After inversion is reached, the small signal capacitance depends on whether the measurements are made in high frequencies i.e. 1 MHz or low frequency (1-100Hz) where high or low are with respect to the generation-recombination rate of the minority carriers in the inversion layer. If the gate voltage is varied rapidly i.e. riding on a high frequency signal, the charge in the inversion layer cannot change in response and thus does not contribute to small a-c signal capacitance. Hence the capacitance remains at:

$$C = C_{ox}.\, C_d \,/\, (C_{ox} + C_d) \tag{2.3}$$

Where: C_{ox} = Oxide capacitance

C_d = Depletion capacitance

However, at if the potential changes at low frequencies i.e. slowly, there is enough time for the minority carriers in this case electrons to be generated in the bulk

silicon substrate, drift across the depletion region to the inversion layer, or go back to the substrate and recombine. This eliminates the depletion capacitance and the overall capacitance across the structure returns to value of the oxide capacitance. The high and low frequency plots of C-V are given in Figure 2.6.

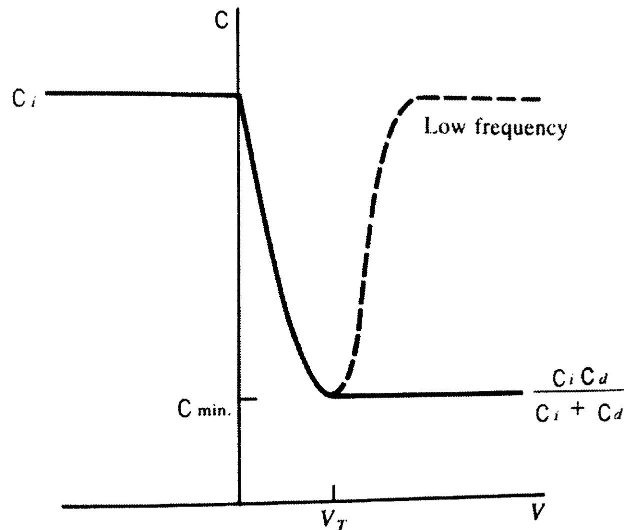

Figure 2.6 C-V plots under high and low frequency (B.G Streetman and S. Banerjee [23]).

The fast interface states can keep pace with low frequency variations of gate bias but not at high frequencies. Therefore the fast interface states contribute to low frequency capacitance C_{LF} but not the high frequency capacitance C_{HF} . The interface state density can be measured from the plot as shown in Figure 2.7 and from the Equation 2.4.

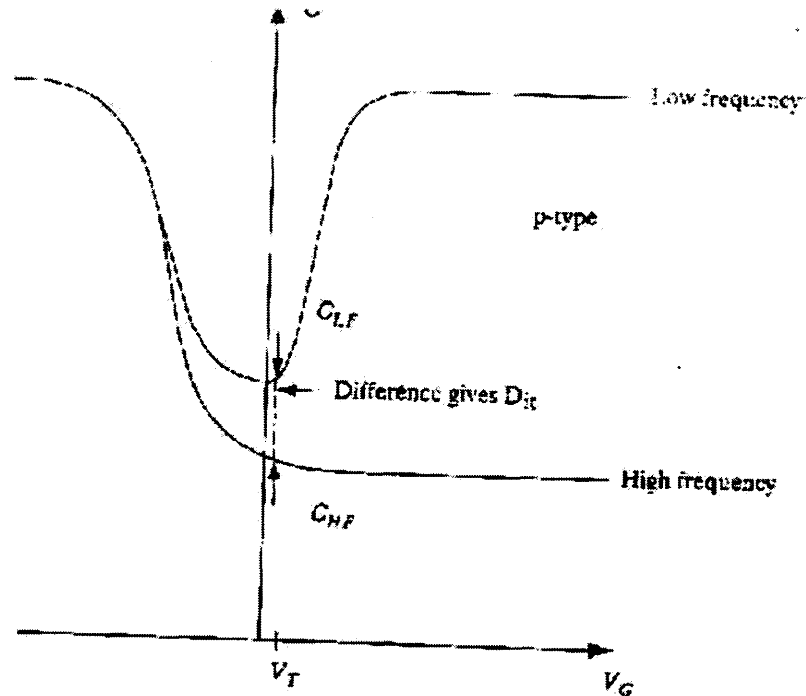

Figure 2.7 D_{it} measurement from C-V plots (B.G Streetman and S. Banerjee [23]).

$$D_{it} = \frac{1}{q}\left(\frac{C_i C_{LF}}{C_i - C_{LF}} - \frac{C_i C_{HF}}{C_i - C_{HF}}\right) cm^{-2} eV^{-1} \tag{2.4}$$

Where:

D_{it} = Interface state density
Ci = Capacitance of insulator i.e. oxide
C_{LF} = Low Frequency capacitance
C_{HF} = High Frequency capacitance
q = Charge

2.3 MOSFET Operation

The operating modes of MOS capacitor i.e. accumulation, depletion and inversion are observed in the operation of MOSFET (MOS Field Effect Transistor). The MOSFET operates as a closed switch in accumulation when the charge carriers form a channel between the source and the drain terminals. The threshold voltage measurements are performed when the MOSFET operates in saturation. The parameters of importance in saturation region for the study are drain current and transconductance. The drain current I_D in linear and saturation region is given by the following equations.

$$I_D = \frac{W}{L}\mu_n C_{ox}[V_G - V_T]V_D \tag{2.5}$$

$$I_{DSAT} \approx \frac{W}{2L}\mu_n \frac{\varepsilon_{ox}}{t_{ox}}(V_G - V_T)^2 \tag{2.6}$$

The transconductance g_m is given by the ratio of change in drain current to the change in gate voltage. Transconductance equations for linear and saturation region are given below.

$$g_m \approx \frac{\partial I_D}{\partial V_G}\bigg| V_D = \text{constant} \tag{2.7}$$

$$g_m \approx \frac{W}{2L}\mu_n \frac{\varepsilon_{ox}}{t_{ox}} V_D \qquad \text{For } V_D < V_{DSAT}\text{, Linear region} \tag{2.8}$$

$$g_m \approx \frac{W}{2L}\mu_n \frac{\varepsilon_{ox}}{t_{ox}}(V_G - V_T) \qquad \text{For } V_D > V_{DSAT}\text{, Saturation region} \tag{2.9}$$

The following factors affect the drain current (I_D) for fixed gate and drain voltage:

- Distance between source and drain.
- Channel width.
- Threshold voltage.
- Gate oxide thickness.
- Dielectric constant of gate oxide.
- Carrier mobility.

2.4 Degradation Condition

The worst degradation caused by the hot carriers can be determined by performing a substrate current vs. gate source voltage measurement. Figure 2.8a shows a typical I_{DB} vs. V_{GS} plot. It is seen from Figure 2.8b that the substrate current increases rapidly with the gate voltage at first, but it starts to decrease at high gate voltages after reaching a maximum value [24]. The increase in the substrate current is caused by the increase of electrons entering the depletion layer. The electrons are induced by the gate voltage, and they experience multiplication, giving rise to a large number of holes which exit through the substrate.

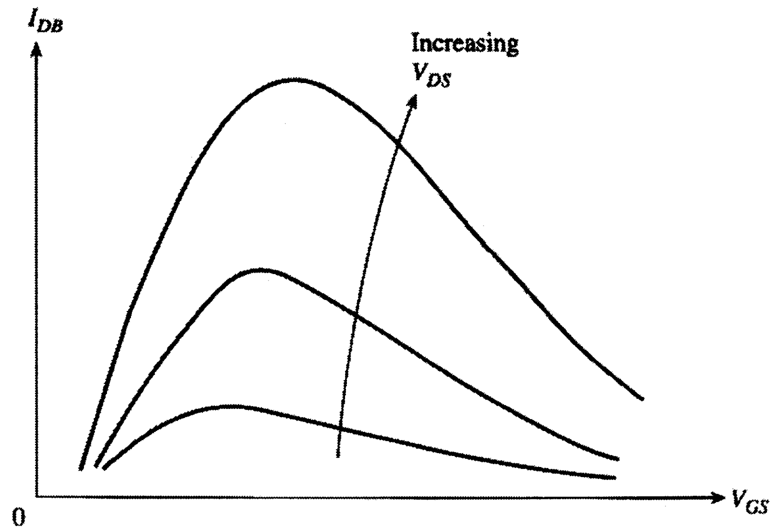

Figure 2.8 a Substrate current vs. gate source voltage (Edward S. Yang [24]).

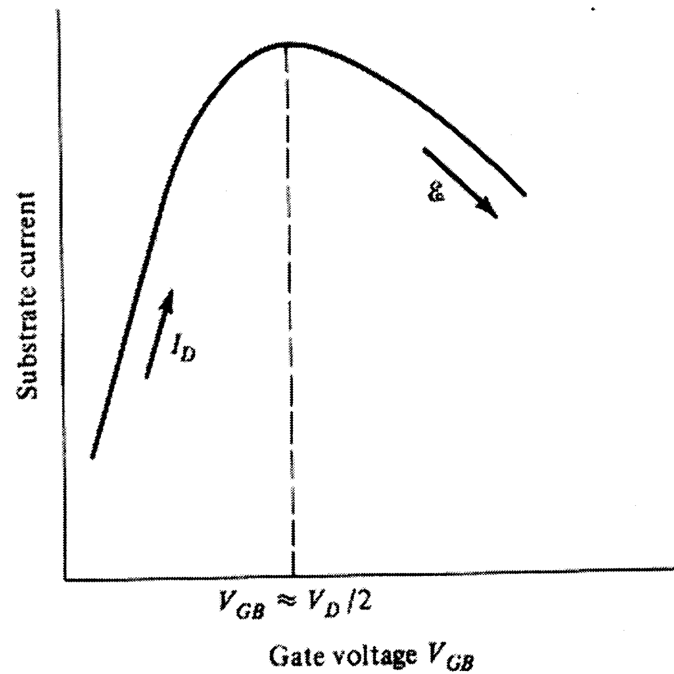

Figure 2.8 b Factors affecting substrate current vs. Gate Source voltage (Edward S. Yang [24]).

The surface electric field along the channel is shown in the Figure 2.9 where the pinch off point separates the high and low field regions. The high electric field is created by the bias voltage across the drain junction. When the gate voltage is increased, the pinch off point moves towards the drain for the same drain potential. The surface potential is lowered and the field pattern is shown by the broken line. The net voltage in the lateral direction from the drain to the pinch off location is decreased, and the avalanche multiplication and substrate current are reduced.

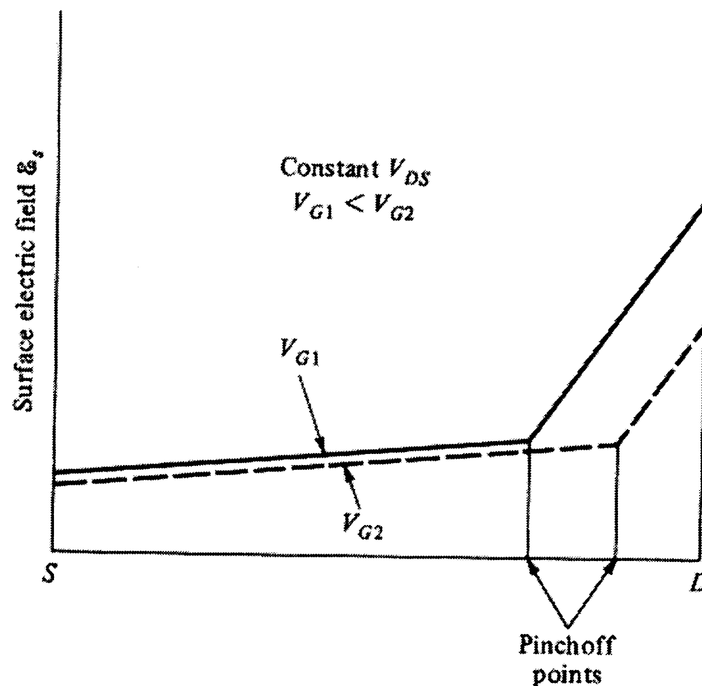

Figure 2.9 Electric field along the channel (Edward S. Yang [24]).

2.5 Threshold Voltage Measurement

The threshold voltage (V_T) is one of the most important parameters of the MOS transistor and can be described simply as the value of the gate voltage when current starts to flow between the source and drain. Yet there are many ways of measuring threshold that are in accepted usage that will yield slightly different values. The reason is that the device itself does not exhibit a well-defined cutoff. The different ways of measurement all give the same threshold to within 100 to 200 mV. But often when more precision is required, the V_T value quoted must be identified by the method by which it was measured. The threshold voltage value is measured with the device in saturation.

2.5.1 One Micron (1μA) Method

Threshold voltage V_T is arbitrarily defined as the gate voltage when 1μA of drain current flows. This method came into popular use in the early days of MOS work since it is straightforward. All it involves is to note down on a curve tracer the gate voltage at which the flat saturation drain current reaches 1μA. Its major drawback is that there is no way to take into account the size, i.e., the W/L ratio, of the device. Two different-sized devices side by side on the same wafer will yield different thresholds if this method is used. For this reason, the method is no longer recommended.

2.5.2 Square Root I_d vs. V_g Method

If the square root of the drain current is plotted as a function of gate voltage for a saturated device, a straight line will result as in Figure. 2.10, whose intercept with the X-axis is V_T. One way to ensure that the device is in saturation is to tie the gate to the drain.

The validity of this method is seen from taking the square root of both sides of the saturation current equation:

$$\sqrt{I_d} = \sqrt{\frac{Co\mu W(V_g - V_T)}{2L}} \tag{2.10}$$

$I_d = 0$ when $V_g = V_T$. The slope of the curve is

$$\frac{d\sqrt{I_d}}{dV_g} = \sqrt{\frac{Co\mu W}{2L}} \tag{2.11}$$

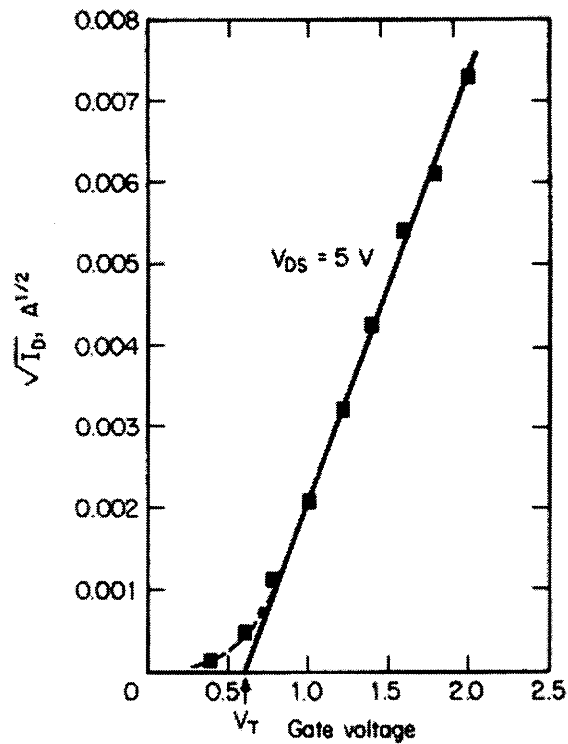

Figure 2.10 Square root I_d vs. V_g method (Dewitt G. Ong [26]).

This method will work for both enhancement and depletion-mode devices, although recall that forcing a device into saturation by tying its gate to the drain works only with enhancement devices. Actual devices will not exhibit the sharp intercept predicted by Equation. 2.10 because of weak inversion current; thus graphic extrapolation from the linear portion of the curve is needed. Different size devices adjacent to each other will produce lines that extrapolate to the same point when this method is used.

CHAPTER 3

OXIDE DEGRADATION IN A MOS DEVICE

In this chapter, the oxide degradation primarily in MOSFET is discussed which is one of the major concerns in MOS processes. For reliable operation of MOSFET's, maintaining *Gate Oxide Integrity* (GOI) is extremely important to process control. GOI is one of the trade-offs defining the gate oxide thickness in a new process, since thinner gate oxides are usually more sensitive to wear-out and damage for a given supply voltage. Hence, GOI requirements have an important role in defining the maximum supply voltage at which circuits designed in a given technology can be operated. These requirements support the reason behind a review of the Si-SiO_2 interface in the MOS structure.

3.1 Ionic Contamination

Mobile ions in semiconductor devices can result in changes in important device parameters such as the threshold voltages, off-state leakage currents and even the transistor drive currents. Over the years, the problem of ionic contamination has been steadily reduced as sources of contamination have been identified and removed. Screening tests, which identify and help correct for excessive mobile ion concentrations in the semiconductor during processing have contributed significantly to reducing this problem [6].

Ionic contamination is rated as both an fabrication process mortality and a wear-out mechanism in the bathtub curve. As a wear-out mechanism it does not seem likely

that an increasing failure rate will be observed, there being no fixed process by which ions move to the $Si0_2/Si$ interface.

The spectroscopic analysis has identified Na^+, Cl^- and K^+ to be the principal causes of failure. Na^+ is the most mobile due to its small radius, and is considered to be most suitable for transportation through the amorphous $Si0_2$. The main sources of mobile ions during the manufacturing process are:

1. Processing equipment and materials such as the furnaces, etchant's, and the solvents and cleaning materials.
2. Packaging materials such as the adhesives and the lead frames can be an important source of contamination.
3. The fabrication environment contains dust particles and water vapor, which can contaminate the semiconductor material if not controlled.
4. The human body is a major source of Na^+ contamination. Human contact during assembly, for instance, can result in serious contamination issues. The increased use of automated manufacturing has reduced the human interface problem greatly, but caution still needs to be exercised.

The effect of ionic contamination in MOS devices is shown in the Figure 3.1 below. A positive ion such as Na^+ would be driven to the SiO_2/Si interface by direction of the electric field in the gate oxide. The extra positive charge at the interface induces an extra negative charge in the n-channel inversion region. The result is that the threshold voltage, which is the gate voltage at which the transistor begins to turn on, goes down.

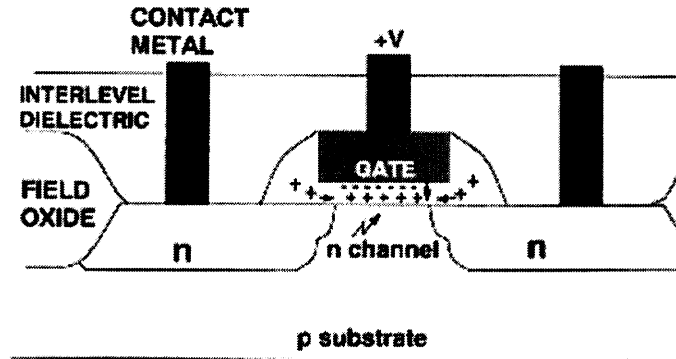

Figure 3.1 Effect of ionic contamination.

3.2 Charge Effects and I-V Instability

The quality of the silicon dioxides has a significant influence on the reliability of MOS devices. In particular, memory devices such as DRAMs and SRAMs are very dependent on the critical charge stored at the gate oxide capacitor. If charge leakage takes place through the gate oxide due to local defects or enhanced tunneling current then the memory cells will lose their stored data. The physical defects that directly alter the charge in the oxide, such as mobile ions, have already been discussed. In this section, the mechanisms of failure due to the injection of charge into the oxide are considered. Two types of charge effects are discussed: slow trapping or negative-bias temperature instability [6] [7], and hot carrier effects. Hot Carriers is one of the most important charge related failure mechanisms. A third mechanism, which is becoming more important with new process equipment, is that of plasma damage

3.2.1 Slow Trapping

Interstitial states at the Si-Si0_2 interface trap electrons and hold them in the oxide as shown in Figure 3.2, thereby permanently shifting the operational threshold of the device [8] [9]. Slow trapping occurs either during the read/erase cycles of programmable memories or when high electric fields in the silicon can provide electrons with sufficient energy to cross the Si-Si0_2 interface.

The presence of permanently trapped negative charge at the oxide interface raises the local threshold voltage, which makes it harder to turn on the device and affects the sensing of high and low voltage states in digital applications. In the case of pMOS transistors a decrease in threshold voltage and an increase in the off-state leakage current is likely. The presence of trapped charge in the oxide decreases the programming speed of programmable memories by creating fields that oppose the passage of electron current in the oxide.

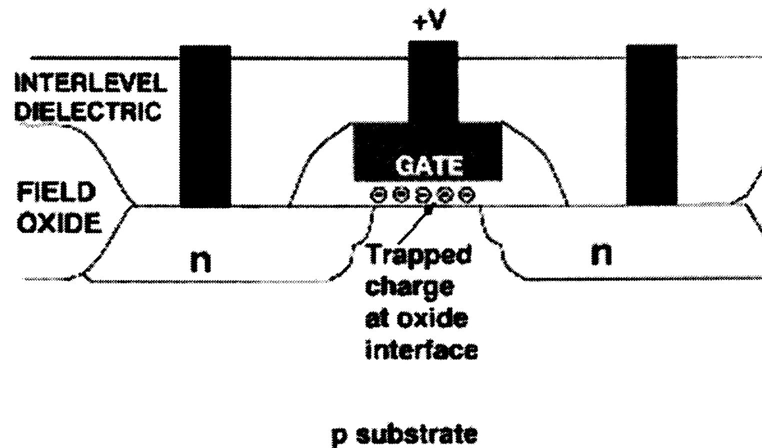

Figure 3.2 Slow Trapping.

3.2.2 Hot Carrier Degradation (HCD)

The MOS structure is widely used in MOSFET transistors where the oxide has two neighbors of the same doping to form either n channel (acceptor doping in source and drain) or p channel (donor doping in source and drain). In the reverse biased drain to substrate junction, the electric field may be quite high in short channel devices. Carriers that are injected into the depletion layer are accelerated by the high field, and some of them gain enough energy to cause impact ionization. These carriers have higher energy than thermal energy and are called hot carriers. As shown in the Figure 3.3, the holes are generated by multiplication can flow to the substrate, giving rise to a large substrate current.

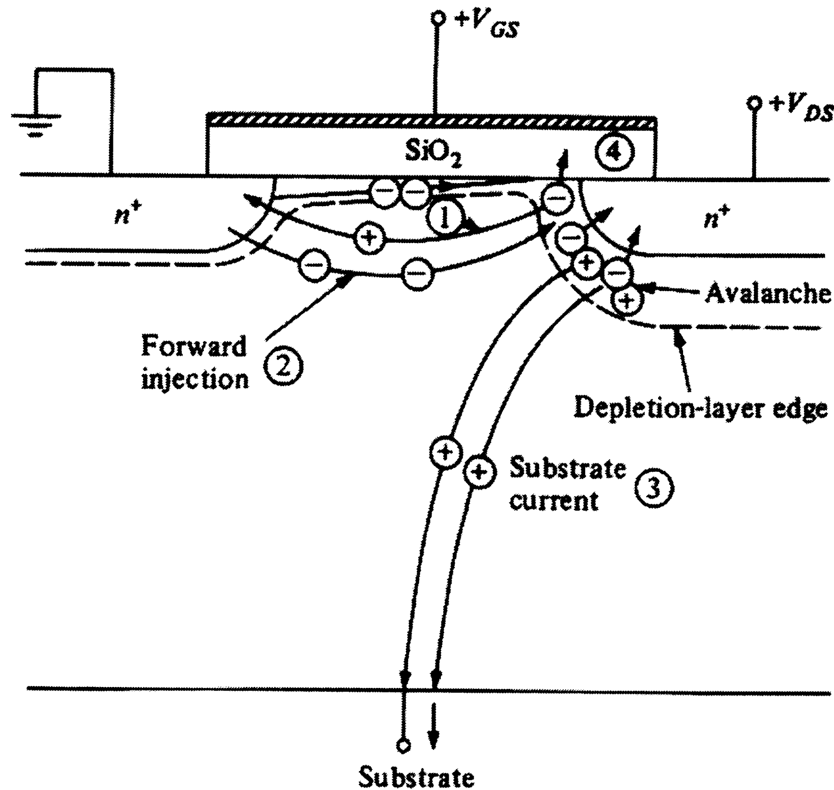

Figure 3.3 Hot Carrier Degradation (Edward S. Yang [24]).

Hot carrier generation and current components:

1) Holes reaching the source
2) Electron injection from the source
3) Substrate hole current
4) Electron injection into the oxide

Some of the holes may find their way to the source, effectively lowering the source barrier to induce electron injection. The drain channel source structure now acts as npn transistor with a floating base and with its collector under avalanche multiplication. Thus, the injected electrons from the source will reach the drain depletion layer, leading to more carrier multiplication.

The electrons generated in the drain depletion layer are attracted to the positive gate voltage, as show in the above Figure 3.3. If these electrons have energy greater than 1.5 eV, they may be able to tunnel into the oxide or to surmount the silicon oxide potential barrier to produce a gate current. Electrons can be trapped inside the gate oxide and can change the threshold voltage and the current voltage characteristics of the device. This is not desirable and should be avoided. The hot carrier effects can be minimized if the electric field of the junction can be reduced. As the reverse bias is increased, the substrate current increases rapidly with the gate voltage at first, but it starts to decrease at high gate voltages after peaking.

The increase in the substrate current is caused by the increase of the electrons entering the depletion layer. The electrons are induced by the gate voltage, and they experience multiplication, giving rise to a large number of electron hole pairs, which exit through the substrate. A high electric field is created by the bias voltage across the drain

junction. When the gate voltage is increased, the pinch off point moves towards the drain. The surface potential is lowered, and the field pattern in shown by the broken line in the Figure 3.3.

The injection of carriers into the oxide results in a change of the I-V characteristics. Figure 3.4 shows the drain current I_d of an nMOS transistor as a function of the drain voltage V_d for different gate voltages V_g, before and after stress [10] [11]. It is seen that a decrease in the drain current is observed both in the saturation region as well as in the linear regions of the I-V curve. An increase in threshold voltage V_t, is also commonly observed for $V_g \geq V_d/2$ and electron injection into the oxide is considered to be the mechanism of degradation. For low V_g, hole injection into the oxide is considered to be the cause of degradation, and the V_t shift is negative. Changes in V_t and I_d are used to monitor hot carrier degradation. The transconductance gm also gives an indication of damage [12]. Figure 3.5 shows the g_m as a function of V_g before stress and after stress. Decrease in g_m at low V_g indicates the change in V_t, a reduction in the peak g_m is related to the change in channel mobility, and at large V_g the g_m shows no change.

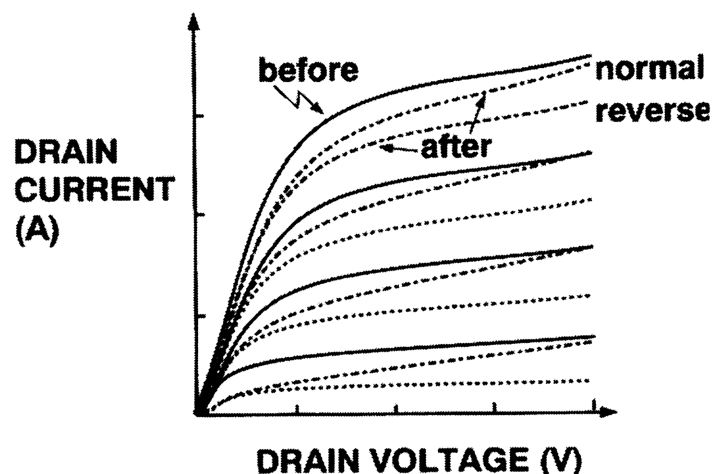

Figure 3.4 I_d vs. V_d characteristics: before and after stress.

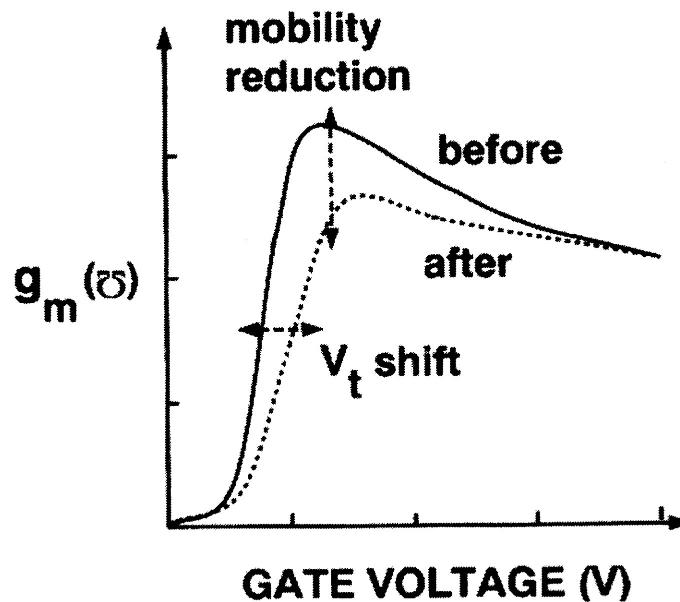

Figure 3.5 Transconductance vs. gate voltage: before and after Stress.

The effects of transistor degradation on circuit reliability have been studied both experimentally [13] and using circuit simulation techniques [14]. The impact on circuits is to show a degradation in propagation delay in inverter chains and changes in access times and data retention times. In analog circuits, the impact on differential amplifiers and current mirrors will be significant.

To limit hot electron effects, it is advantageous to have a lightly doped drain region. This is because, in such a case, part of the depletion region would be inside the drain, absorbing some of the potential that otherwise would exist in the pinch off region, and lowering the maximum electric field. However, a lightly doped drain in standard processes would mean a lightly doped source, since both regions are made simultaneously, in the same way. This would result in a large source resistance on which

a large voltage drop could develop, which is undesirable. This popular structure is referred to as Lightly Doped Drain (LDD) as shown in Figure 3.6. It makes possible to lower a maximum field and thus less severe hot electron effects, while keeping the series resistance relatively low. In addition, because the lightly doped part can be made shallow, the short channel effects related to the charge sharing are limited.

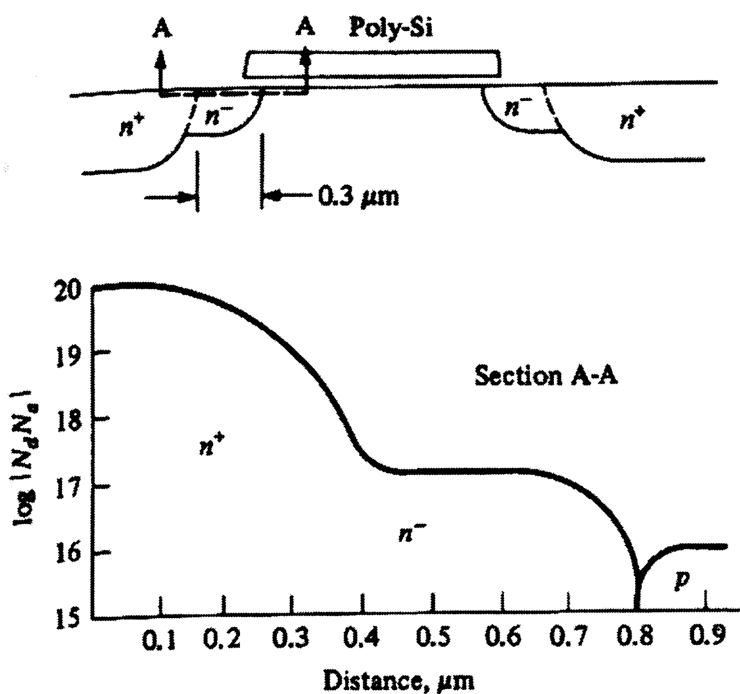

Figure 3.6 Lightly Doped Drain structure (Edward S. Yang [24]).

By introducing a lightly doped section between the drain and the channel, the depletion layers peak field is shifted toward the drain, and the field is lowered as shown in Figure 3.7.

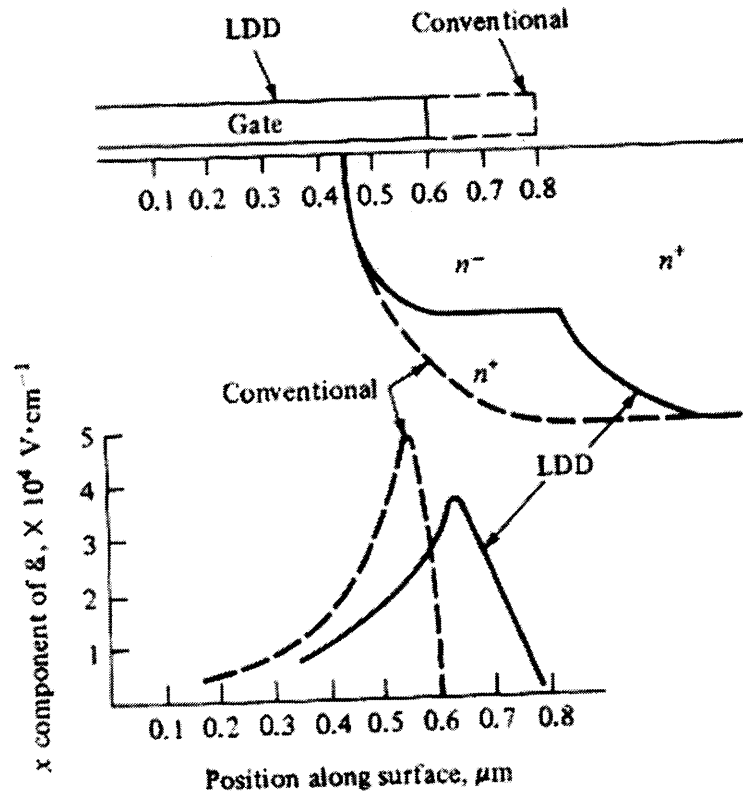

Figure 3.7 Shift of peak field in LDD structure (Edward S. Yang [24]).

The LDD structure is more complicated and takes more steps in fabrication, but few added processing steps produce significant improvements in performance. It has higher breakdown voltage, and substrate current is reduced by a factor of 30 [24]. The peak field is shifted away from the oxide, resulting in less hot electron injection into the oxide. The LDD means a thinner depletion layer, thus less charge sharing and less threshold reduction in short channel devices. There is also less overlapping capacitances, resulting in faster circuit.

3.2.3 Plasma Damage

Plasma processes such as etching, deposition, cleaning and ion implantation can all cause damage to the thin oxides in MOS devices. Hence, plasma damage has become a concern in submicron technologies. The incident plasma builds up charge on metal or polysilicon electrodes usually in the region where the area or periphery is large [15]. This charge is then transferred to the region of the same electrode where a high electric field enables some current flow to take place, such as across a thin gate oxide [16]. Oxide damage has been shown to be related to plasma processing steps such as etching, resist strip, and plasma chemical vapor deposition [17]. Charging is considered to be due to plasma non-uniformity, where the plasma and electron currents are not locally balanced. Hence, the surface (electrode) charges until the electron current is balanced by the local ion current [16]. Charging can be both positive and negative, with the peak voltages dependent on the thickness of the surface dielectrics.

The most commonly observed effect is that of increased oxide leakage current after plasma damage takes place. This is due to a reduction in the oxide breakdown voltage. In MOS devices, degradation of the I_d-V_g characteristics is also observed, usually in the form of an increase in the threshold voltage V_t and a decrease in the subthreshold slope [18]. The extent of the damage is a function of the antenna ratio, which defines the ratio of the size of the electrode to the size of oxide being damaged. The larger antennas are susceptible to attract more plasma charging during the process, thereby damaging the gate oxide to a greater extent. The Figure 3.8 shows that the yield of transistor testers with antenna as measured by gate leakage current at time zero. While

a clear antenna effect is evident, no different is seen between thickness splits [2]. The measurement results given later in this report support this phenomenon.

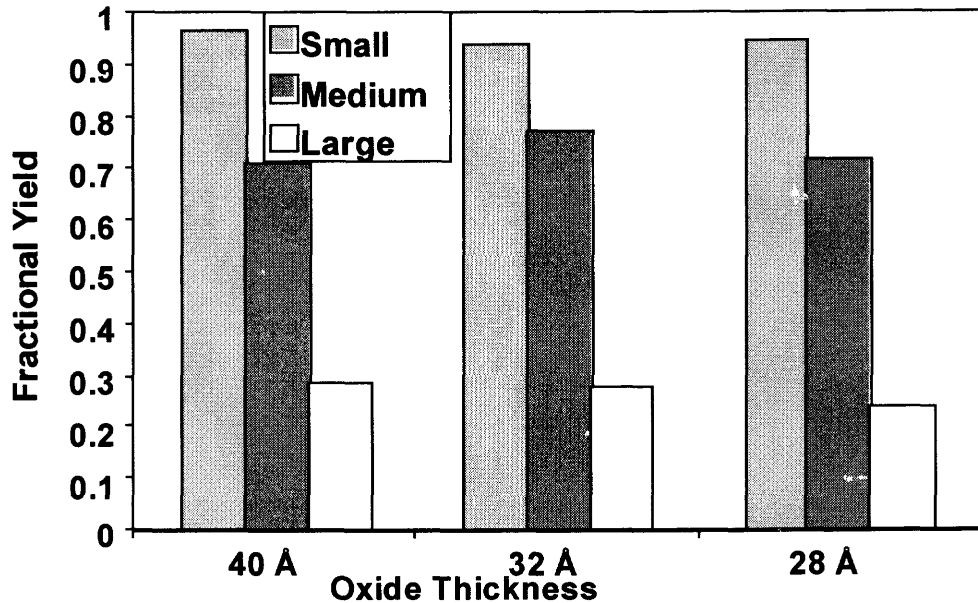

Figure 3.8 Yield based on antenna ratio for different oxide thickness (K. P. Cheung, et. Al [2]).

Plasma damage seriously reduces gate oxide integrity and is, therefore, considered to be a major yield limiter in processes where significant plasma damage is observed. Damage is most significant in MOS devices, although degradation in bipolar gain may be observed in bipolar processes.

3.2.4 Injection Modes

During plasma processes, for current to flow through a good quality oxide layer, a high field is needed. It is not sufficient just to show that there is a large amount of charges arriving to the gate electrode. It is the potential difference between the gate electrode and the substrate that determines the amount of current that flows through the gate-oxide [19].

Many factors affect the gate and substrate potential. At steady state, the dc behavior of both the gate and the substrate are determined by plasma potential as well as electron temperature. It is the nonuniformity of the plasma potential that causes the substrate potential to be different from the gate potential. Once oxides start to break down or once field enhanced tunneling starts to occur, both the gate potential and the substrate potential continuously adjust to maintain charge balance in the entire wafer. These complex adjustments are influenced by the asymmetry in electron-current flow from the plasma to the wafer, the ion-current saturation effect, and the nonlinear dependence of tunneling current on oxide-field.

In the stress measurements, MOSFET's are biased into either "substrate"- or "gate"- injection tunneling by applying positive or negative current to the floating gate. Figure 3.9 shows band diagram for gate injection (Figure 3.10) and substrate (Figure 3.11) injection.

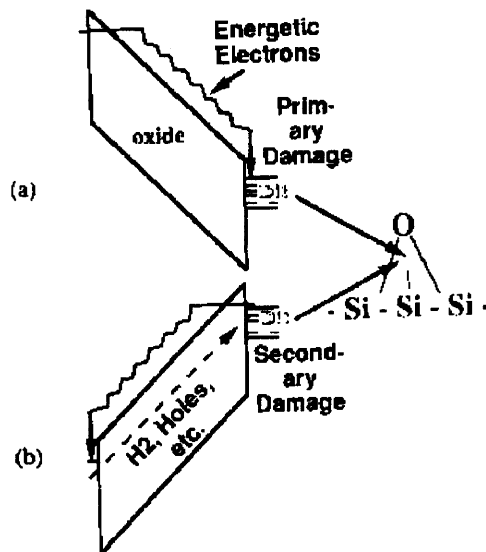

Figure 3.9 Band diagram for gate and substrate injection.

Depending upon the polarity of plasma potential relative to wafer the high-field electron injection process could be from gate or substrate. The difference in the potential between the substrate and gate causes electronic transport through the oxide. Energetic electrons directly release energy at the anode, in case of gate injection, causing primary damage and frees up species such as holes and H_2 etc that travel across the oxide/dielectric in the field and cause secondary damage at the cathode, which is the Si-SiO_2 interface.

Gate Injection:

When gate is at a lower potential than the substrate during plasma exposure, electrons inject from the gate into the substrate during charging damage [27]. The charge balance condition is such that the tunneling current equals the difference between electron current and ion current from the plasma as shown in Fig 3.10. Since plasma can respond to a positive floating potential change by supplying a electron current density many times higher than ion current density, the maximum stress current density for the gate injection polarity can be a couple of orders of magnitude higher than the substrate injection polarity. As a result, almost all gate injection charging damage is in the high current regime.

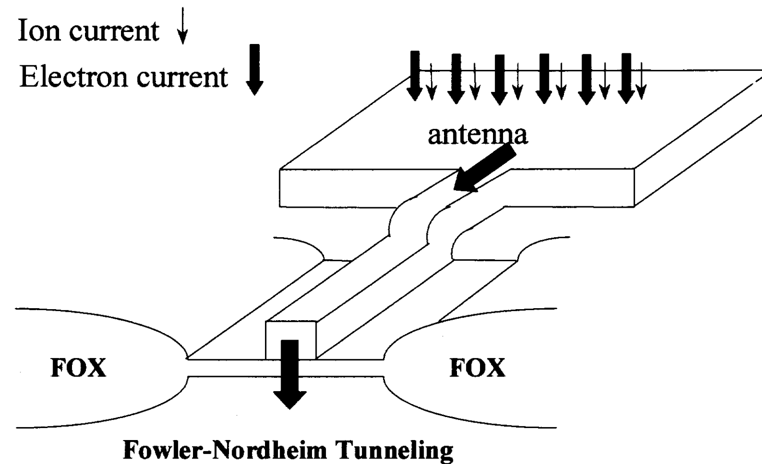

Figure 3.10 Gate injection.

Substrate Injection:

In the case of gate being at higher potential resulting in substrate injection of electrons [27] as shown in Figure 3.11, the charge balance condition is such that the tunneling current density is limited by the ion current density of the plasma multiplied by antenna ratio and antenna efficiency.

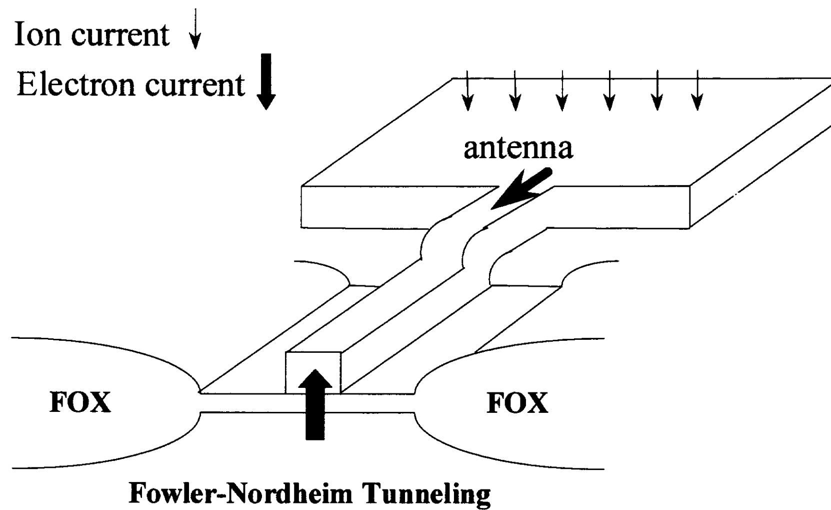

Figure 3.11 Substrate injection.

It has been shown that damage for substrate injection is more pronounced [22]. It is because when gate oxide is stressed defects are formed inside the bulk of the oxide as well as at the interface. The distribution of these defects is believed to be as a sheet near the cathode. For example, when electrons are injected from the gate, hot holes, generated form the Si/SiO_2 interface, create electron traps at the gate and oxide interface. For substrate injection, therefore, traps are formed at the Si/SiO_2 interface. Since transistor V_t is more sensitive to charge trapped near the Si/SiO_2 interface, substrate injection is, therefore, more damaging. We have used substrate injection in our experiments to simulate the maximum damage that could be caused by plasma charging. The following Figure 3.12 shows pictorial representation of gate and substrate injection.

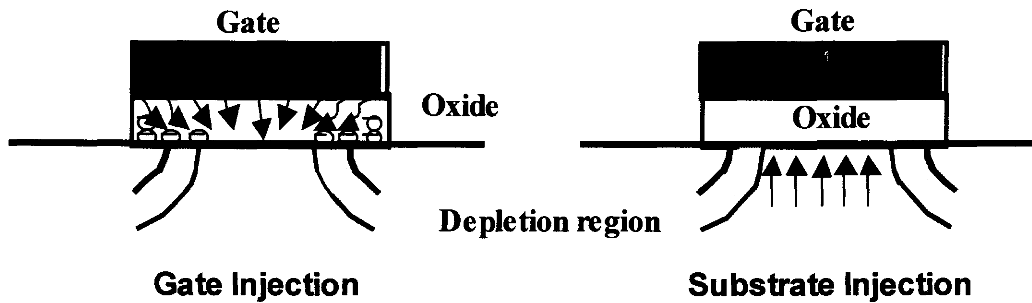

Figure. 3.12 Gate and substrate injection (D. Misra [21]).

CHAPTER 4

MOSFET DEGRADATION MEASUREMENTS

This chapter discusses the wafer used, the instrument setup and procedure for taking measurements for this study.

4.1 Experimental

The wafer was fabricated in 0.25μm technology at Lucent Technologies. The gate oxide thickness was 6nm with channel width and length of 600 nm and 250 nm respectively. The devices selected on the wafer consisted of both pMOSFET and nMOSFET with gate antenna ratios of 1:2009 (smallest antenna), 1:10066 (mid size antenna) and 1:50050 (largest antenna). The antennas were directly connected to the gate terminal of the respective transistor. A pictorial representation of the transistor layout is shown in the Figure 4.1. The source and substrate connections are common for all the transistors.

4.2 Measurement Setup

The HP 4156B Semiconductor Parameter Analyzer was used along with Cascade Probe Station to carry out the measurements for the above devices. The connections to HP 4156B to the transistor on the probe station were made as described in Table 4.1.

Table 4.1 HP4156B Parameter Setup and Connections

Source Monitor Unit	Voltage	Current	Mode	Set as	Connected to
SMU 1	V_d	I_d	VOLTAGE	CONSTANT	Drain
SMU 2	V_g	I_g	VOLTAGE	VAR1	Gate
SMU 3	V_s	I_s	COMMON	CONSTANT	Source
SMU 4	V_{sub}	I_{sub}	COMMON	CONSTANT	Substrate

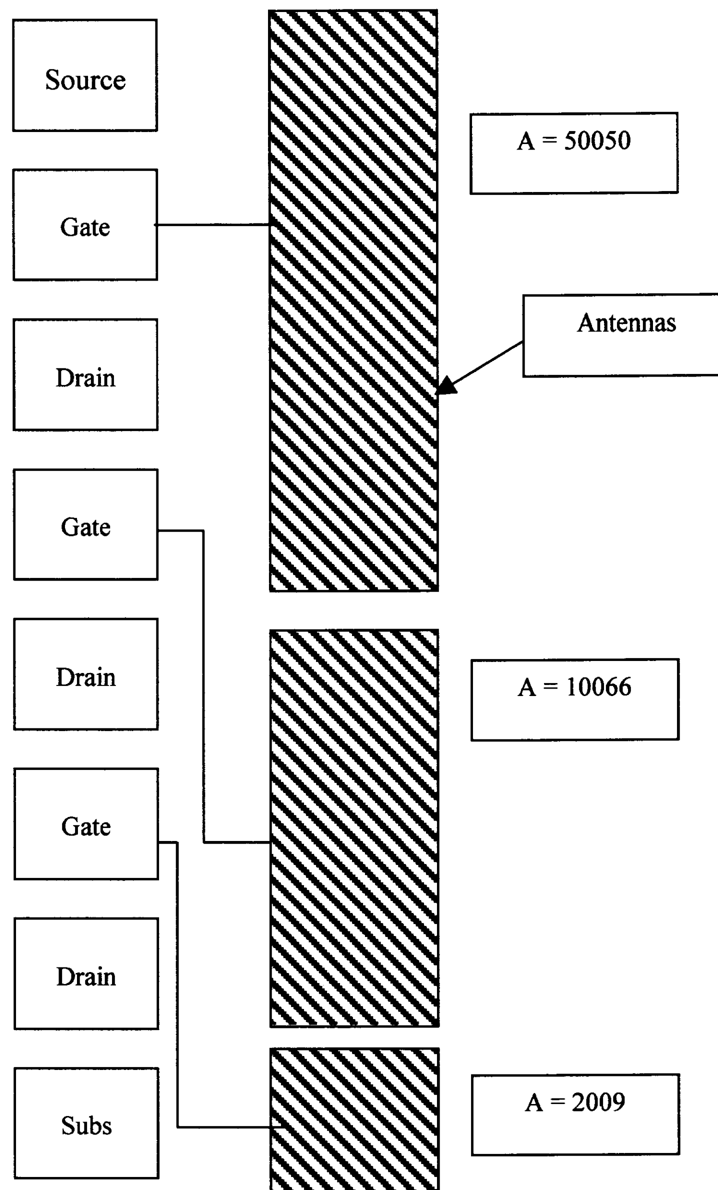

Figure 4.1 Transistor layout.

Each transistor measurement location co-ordinate was logged on for documentation purposes to apply similar stress conditions for achieving consistent results with all three antenna ratios. For the initial study, the measurements were made on the

devices with smallest antenna, since they are less prone to damage than the devices with larger antennas. The condition for maximum degradation caused by hot carriers was performed as per Section 2.4. The substrate current vs. gate source voltage measurement performed on the test transistor revealed the characteristics shown in Figure 4.2.

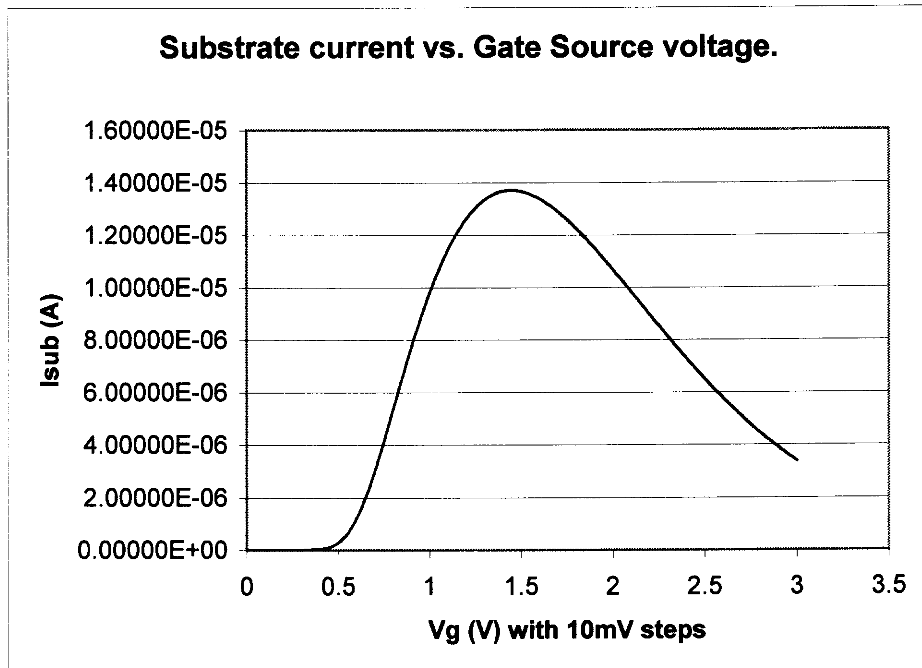

Figure 4.2 Measured substrate current vs. gate source voltage.

The value of gate potential, Vg where the substrate current reaches its maximum value was designated to be the Gate Stress potential, V_{gstr} for HCD measurement. The Drain voltage, V_d that was constant during the substrate current vs gate source voltage measurement is designated as Drain stress voltage (V_{dstr}).

The Square Root I_d Versus V_g Method was used in the measurement to determine the threshold voltage. The snapshot from the HP4156B showing the threshold voltage measurement is shown in Figure 4.3.

*** HP 4156B GRAPH PLOT *** Sep 28 5:01:56 1997 PAGE 1

Saturation Region Vth

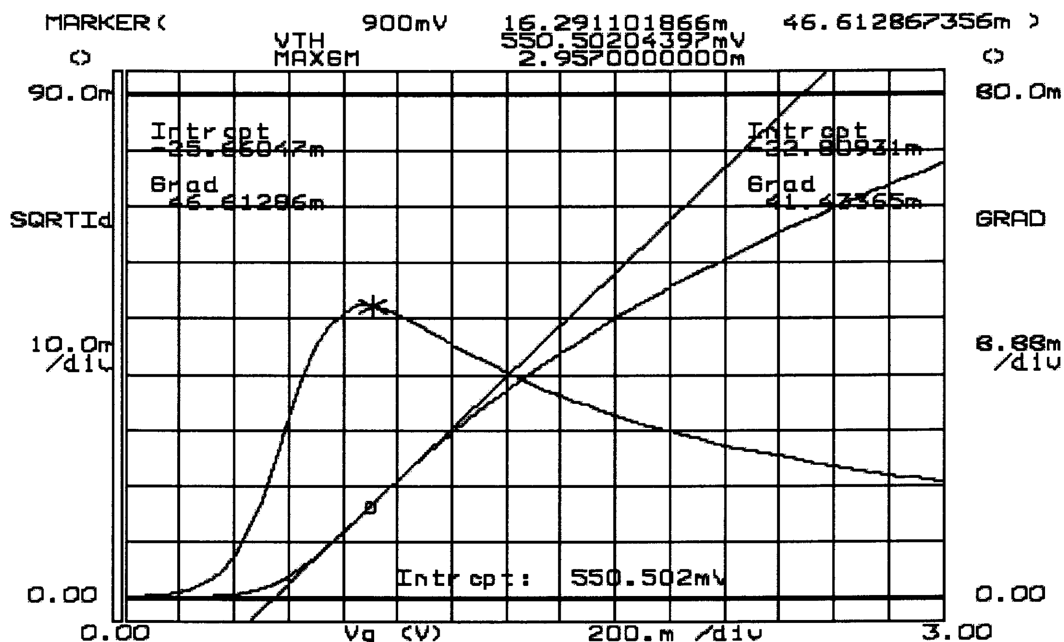

Figure 4.3 Threshold measurement on HP4156B.

4.3 Procedure

The stress application and measurement setup is shown in a pictorially in Figure 4.4 (a) and (b), the Figure 4.4. (a) is a typical injection mode used to evaluate the oxide integrity of a transistor, where source, drain and substrate terminals are connected together and grounded. In the present work, source and drain terminals were biased with a voltage from 0V to 2V shown in Figure 4.4 (b) keeping the substrate at measurement ground.

Two types of stress were applied to the test transistors, substrate injection and hot carrier injection by applying the Vgstr and Vdstr potentials at the gate and drain respectively, whose values are determined from the section 4.2.

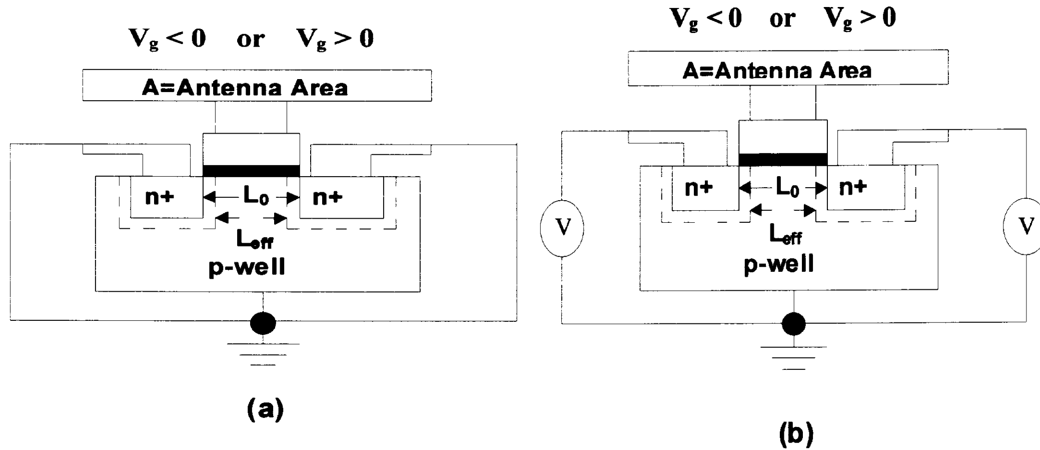

Figure 4.4 Stress application modes (Ref: D. Misra [21]).

The stress duration time was selected to provide proper measurements when plotted in a logarithmic scale. The duration for hot carrier stress was selected with the following values in seconds: 1, 3.16228, 10, 31.62278, 100, 316.227814, 615.9, 915.6, 1220. Which means that the hot carrier stress was carried out for 1 second and then threshold voltage and transconductance values were measured then the stress was applied for the next value of stress duration, which is 3.16 seconds followed by parameter measurements. These stress durations and condition were uniform over all the transistors selected for the measurement.

The substrate injection was carried out for three seconds only once on fresh transistor and then followed by HCD stress. In order to achieve consistent results a set of five transistors were selected and applied with the similar substrate injection condition and reverse bias potential at source and drain. These stress applications were automated

using a special LabView software program developed for the HP4156B. The values for the stress and time were entered into the fields of the graphical interface and the software program was initiated. The parameters were sent to the HP4156B and stress application was initiated thereby reducing time expensive manual entries through the HP4156B front console. The graphical interface for the LabView software program is given in Figure 4.5.

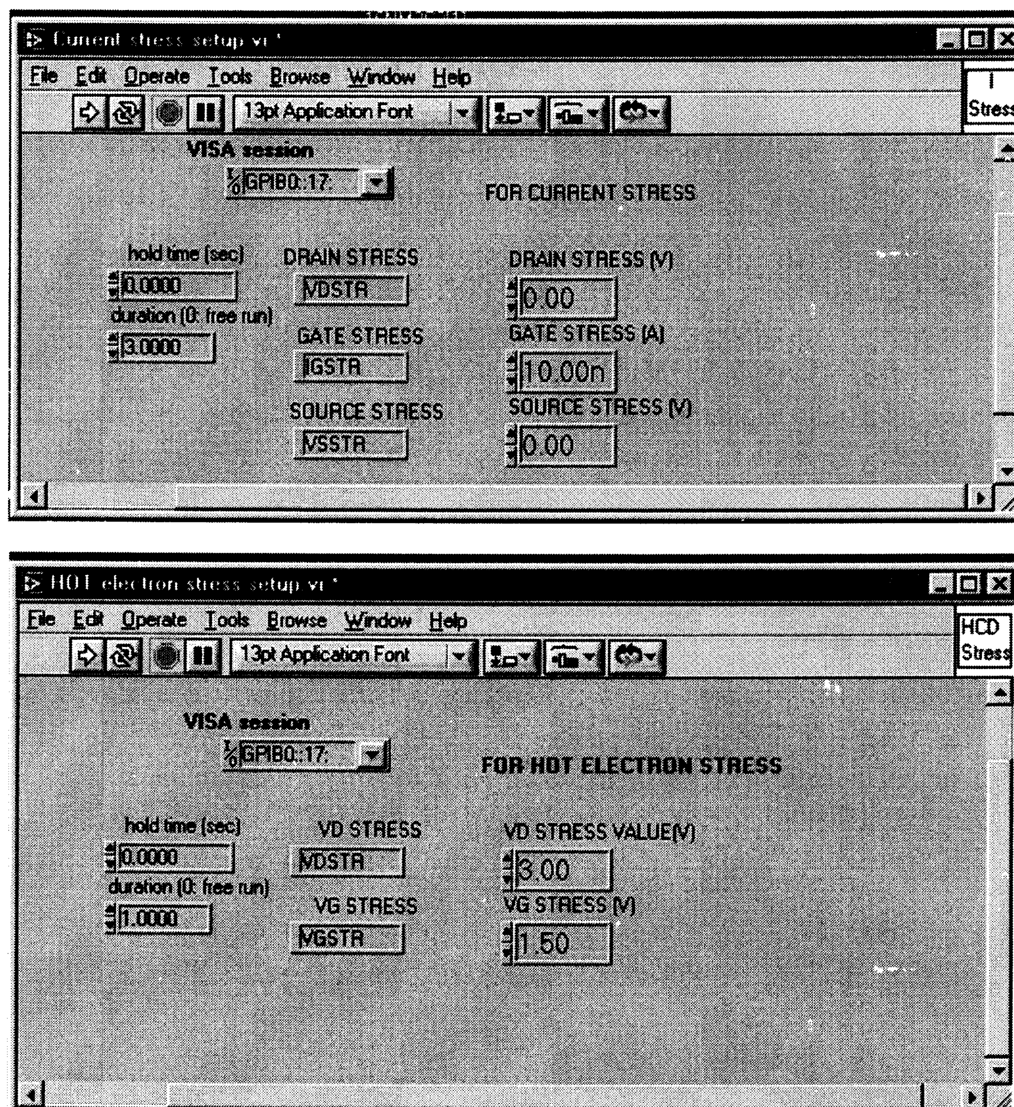

Figure 4.5 Graphical interface of LabView software for current stress and hot carrier stress.

The measurements were performed on transistors whose gate was linked to the smallest antenna located at co-ordinates as given in Table 4.2. The similar set of measurements were later carried out on the mid and large size antenna for comparison and verification purpose. The transistors were divided into the following stress conditions for the analysis:

1. HCD (Hot Carrier Degradation) Stress on 5 transistors.
2. Substrate Injection with the drain and source reverse biased at 0V on 5 transistors.
3. Substrate Injection with the drain and source reverse biased at 1V on 5 transistors.
4. Substrate Injection with the drain and source reverse biased at 2V on 5 transistors.

Table 4.2 Location Co- ordinates of Measured Transistors

X	Y
-42500	39000
-20500	39000
1500	39000
23500	39000
45500	39000
-42500	18500
-20500	18500
23500	18500
45500	18500
65500	18500
-48500	-3500
-28000	-3500
-4500	-3500
17500	-3500
39500	-3500
63000	-3500
-47000	-24000
-25000	-24000
-3000	-24000
19000	-24000
41000	-24000
63000	-24000
-25000	-45000
-3000	-45000
19000	-45000
41000	-45000

The measurements on transistors with smallest antenna were performed at the co-ordinates given in Table 4.3.

Table 4.3 Location Co-ordinates of Measured Transistors with Stress Conditions

X	Y	Transistor Name
-42500	39000	Used for Isub-Vg measurement
-20500	39000	WT1
1500	39000	WT2
23500	39000	WT3
45500	39000	WT4
-42500	18500	WT5
-20500	18500	C0T1
800	18500	C0T2
23500	18500	C0T3
45500	18500	C0T4
65500	18500	C0T5
-48500	-3500	C1T1
-28000	-3500	C1T2
-4500	-3500	C1T3
17500	-3500	C1T4
39500	-3500	C1T5
63000	-3500	C1T6
-47000	-24000	Bad
-25000	-24000	C2T1
-3000	-24000	C2T2
19000	-24000	C2T3
41000	-24000	C2T4
63000	-24000	C2T5
-25000	-45000	Bad
-3000	-45000	C2T5
19000	-45000	Bad
41000	-45000	C2T6

Table 4.3 shows which transistors were measured with procedure from Section 4.3. The nomenclature of transistor name WT stands for just HCD measurement, CxT stands for substrate injection with reverse bias on drain-source of x volts.

CHAPTER 5

RESULTS AND DISCUSSION

This chapter presents the results of measurements taken by the procedure in Section 4.3 along with the comparison and discussion. When the devices were subjected to substrate injection, a significant V_t shift was observed as shown in Figure 5.1. This indicates a significant electron trapping in the oxide.

5.1 Results for Transistors with Smallest Antenna Ratio

The transistors with gate connected to the smallest antennas were subjected to hot carrier and substrate injection stress. The results clearly indicate degradation in the threshold voltage and transconductance values. The time taken by the transistors to 10% degradation was considered as a benchmark for life time estimation. The Figure 5.1 and 5.2 show degradation of threshold voltage and transconductance for hot carrier stressed transistor in terms of logarithmic time scale. The time scale shows the aging of the device, due to reduction of device lifetime after stress application.

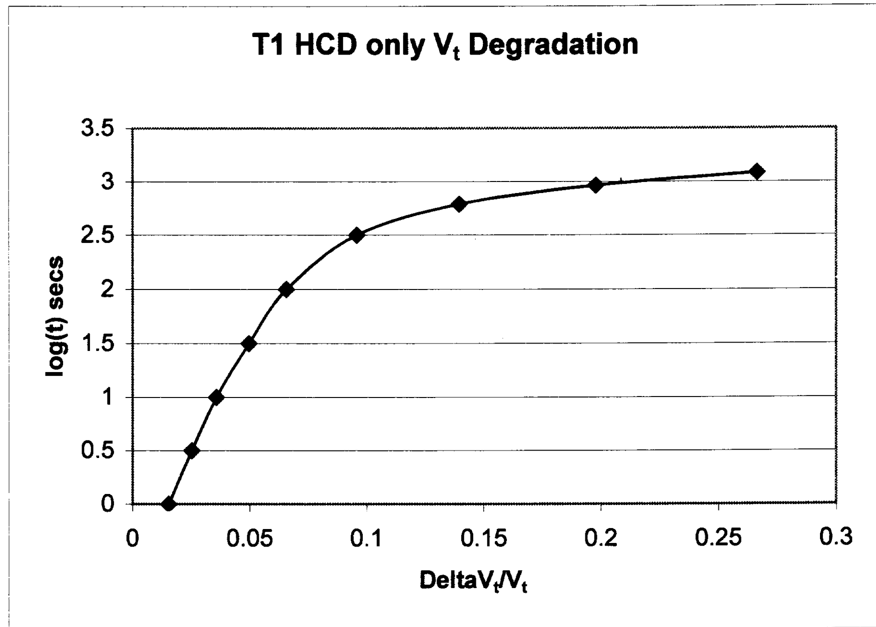

Figure 5.1 Threshold Voltage (V_t) Degradation for HCD stressed transistor.

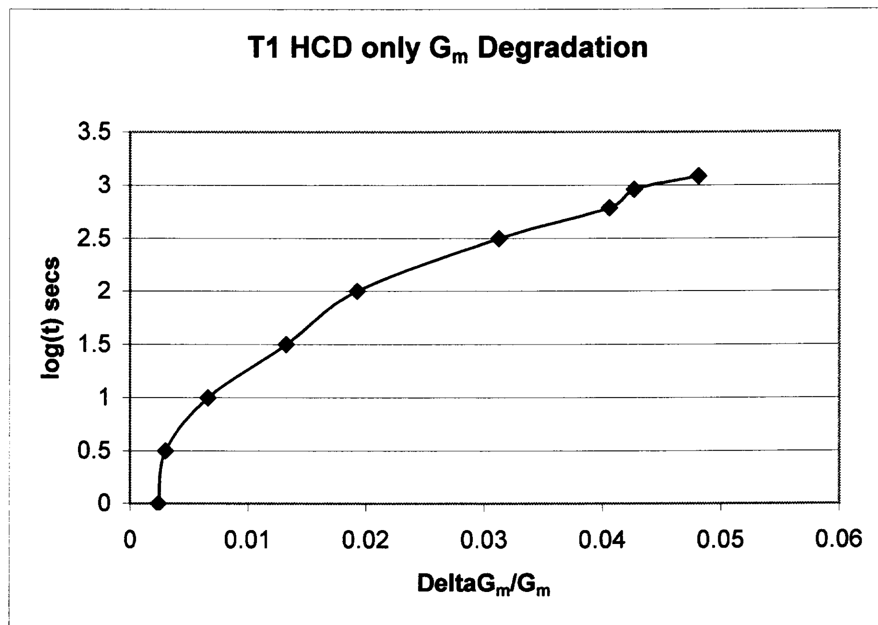

Figure 5.2 Transconductance (G_m) degradation for HCD stressed transistor.

Where:

T1 : Transistor number 1, on which HCD stress was applied.

DeltaV_t/V_t: (V_t measured after stress - Initial V_t value)/ Initial V_t value, which gives the variation from the initial value.

DeltaG_m/G_m: (G_m measured after stress - Initial G_m value)/ Initial G_m value, which gives the variation from the initial value.

As it can be observed in Figure 5.2, the time to achieve 10% degradation can be very long. In the results shown in Figure 5.2, the measurements were carried out for an hour and the transconductance value degraded 5% from its initial value.

This is one of the reason that channel hot-carrier stress is not often used in monitoring damage is that it is very time consuming. Conventional hot-carrier stress method to determine the lifetime of transistors under nominal operating condition involves aging the device under mildly accelerated conditions. It is appropriate to stop aging after a long enough time and the lifetime for that particular aging condition is obtained through extrapolation. Only after the degradation rate (slope of the curve) of Gm reaches the asymptotic value can one fit the data in the log-log plot to a straight line for lifetime extrapolation [25]. Figure 5.3 shows a plot where the transconductance value was extrapolated using slope and intercept formulas. The actual measurements and the extrapolated calculations are shown on the same chart and the value for 10% degradation is found by extrapolation. This value is saved for later comparisons to under stand effect of stress conditions on lifetime of device.

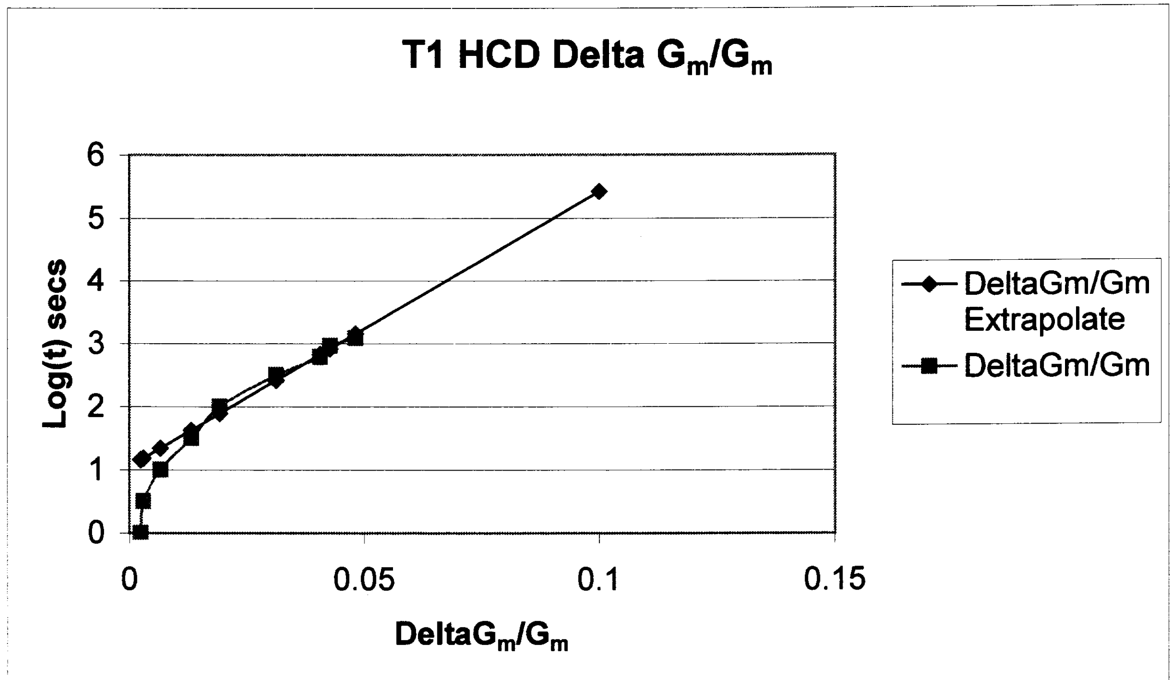

Figure 5.3 Extrapolated Transconductance(G_m) degradation of HCD stressed transistor.

5.1.1 Results for Hot Carrier Stressed Transistors

The following table shows lifetime values for transistors applied with hot carrier stress.

Lifetime (Log(t) seconds) Threshold voltage	Lifetime (Log(t) seconds) Transconductance
2.23886376	5.424932487
2.263443976	4.875159691
2.211129934	4.589294564
2.134139698	5.487499868
2.384469383	5.106704847

5.1.2 Results for Transistors with Substrate Injection

The following table shows lifetime values for transistors applied with substrate injection and reverse bias of 0V on the drain and source.

Lifetime (Log(t) seconds) Threshold voltage	Lifetime (Log(t) seconds) Transconductance
2.23886376	5.136558329
2.263443976	4.738869603
2.211129934	4.67124809
2.134139698	5.186374256
2.384469383	5.091886209

The following table shows lifetime values for transistors applied with substrate injection and reverse bias of 1V on the drain and source.

Lifetime (Log(t) seconds) Threshold voltage	Lifetime (Log(t) seconds) Transconductance
2.381819174	4.881529054
2.087902842	4.223994625
2.153408314	4.414548379
3.045876192	5.428681802
2.873110596	5.18923229

The following table shows lifetime values for transistors applied with substrate injection and reverse bias of 2V on the drain and source.

Lifetime (Log(t) seconds) Threshold voltage	Lifetime (Log(t) seconds) Transconductance
2.455082572	4.805970545
2.86893052	4.758310222
2.936841856	4.984441889
4.696085397	5.00183532
2.607850669	4.802075264

The mean values for each of the above measurements were taken and used for comparison. The Figure 5.4 and Figure 5.5 show comparison of all the lifetimes for 10%

degradation in transconductance and threshold voltage values under different stress conditions, respectively.

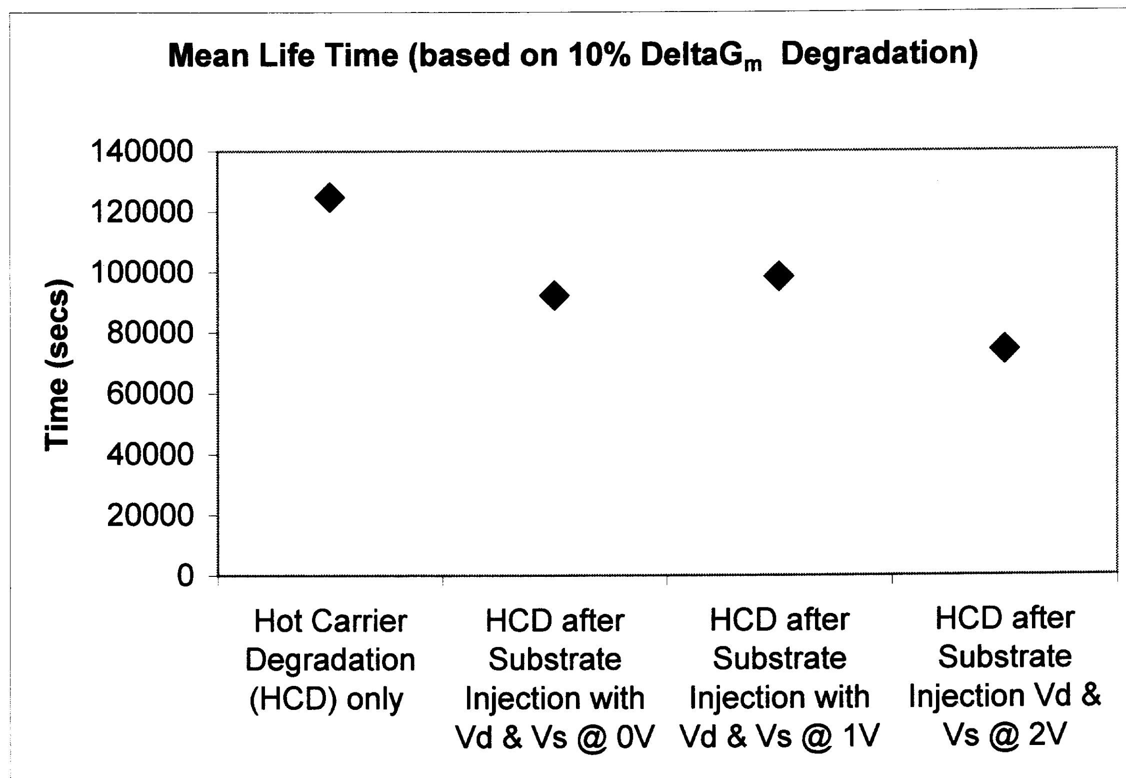

Figure 5.4 Lifetime for transistors with different stress condition (small antenna).

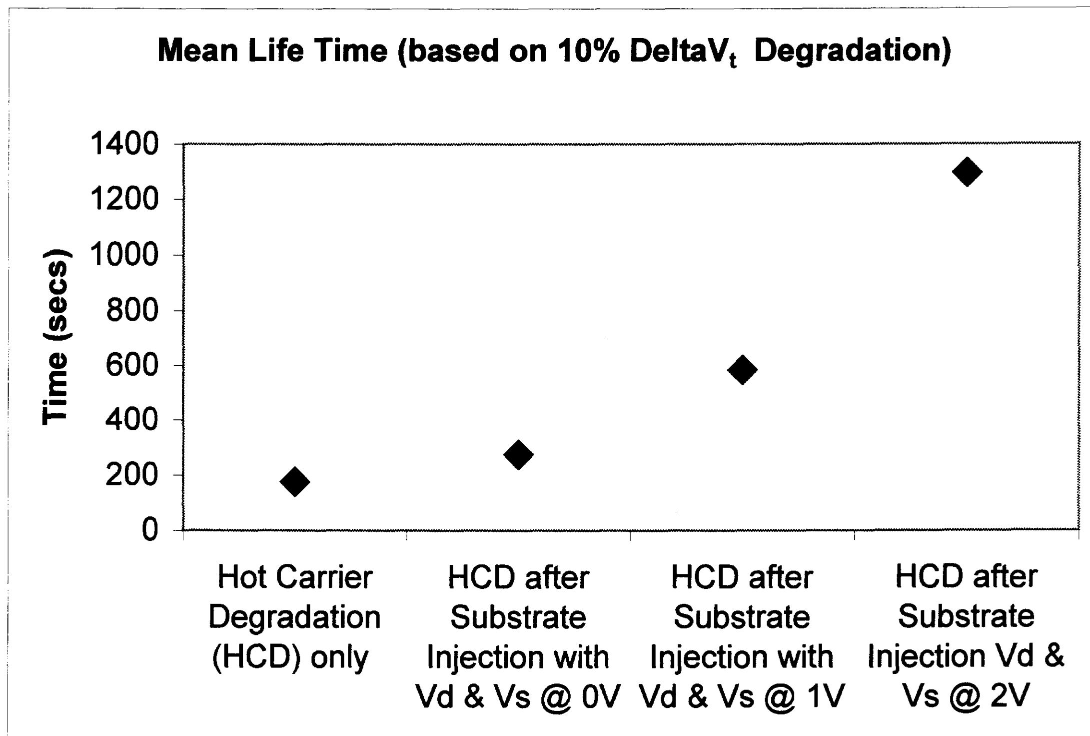

Figure 5.5 Lifetime for transistors with different stress condition (small antenna).

5.2 Results for Transistors with Midsize Antenna Ratio

The transistors with gates connected to antenna ratio of 10066 were put to similar set of stress conditions as per Section 4.3. The following sections present their results.

5.2.1 Results for Hot Carrier Stressed Transistors

The following table shows lifetime values for transistors applied with hot carrier stress.

Lifetime (Log(t) seconds) Threshold voltage	Lifetime (Log(t) seconds) Transconductance
2.272246186	4.975443404
2.243036144	4.963389238
2.276092589	4.995089267
2.489947634	5.759114187
2.537577483	5.406144717

5.2.2 Results for Transistors with Substrate Injection

The following table shows lifetime values for transistors applied with substrate injection and reverse bias of 0V on the drain and source.

Lifetime (Log(t) seconds) Threshold voltage	Lifetime (Log(t) seconds) Transconductance
2.351724449	5.317881306
2.422453871	5.408895283
2.351690853	4.532027382
2.098273561	5.336621791
2.681446063	4.360175603

The following table shows lifetime values for transistors applied with substrate injection and reverse bias of 1V on the drain and source.

Lifetime (Log(t) seconds) Threshold voltage	Lifetime (Log(t) seconds) Transconductance
2.446211839	4.657345837
2.835786618	5.950257511
2.399859496	4.622805374
2.710941894	4.955014014
2.570629127	4.700368347

The following table shows lifetime values for transistors applied with substrate injection and reverse bias of 2V on the drain and source.

Lifetime (Log(t) seconds) Threshold voltage	Lifetime (Log(t) seconds) Transconductance
1.702661741	4.368395477
1.679506594	1.843238632
2.579084697	4.808202937
2.461443104	4.299478034
1.702661741	4.368395477

The mean values for each of the above measurements were taken and used for comparison. The Figure 5.6 and Figure 5.7 show comparison of all the hot carrier

lifetimes for 10% degradation in transconductance and threshold voltage values under different stress conditions respectively.

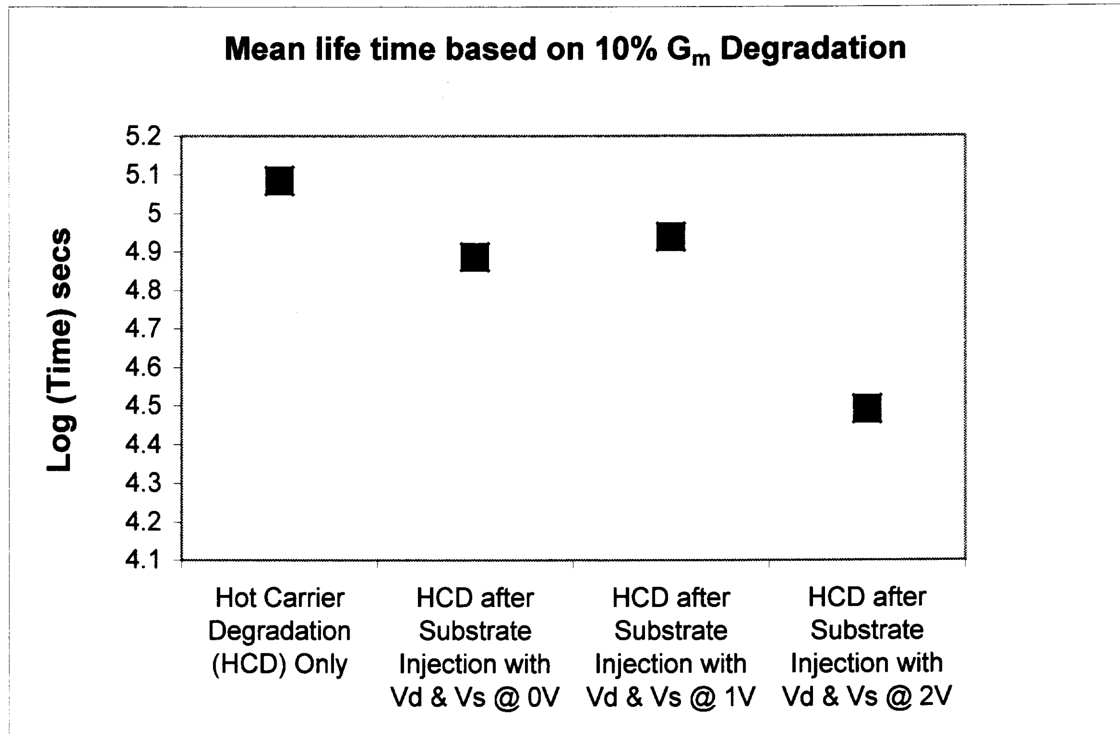

Figure 5.6 Lifetime for transistors with different stress condition (midsize antenna).

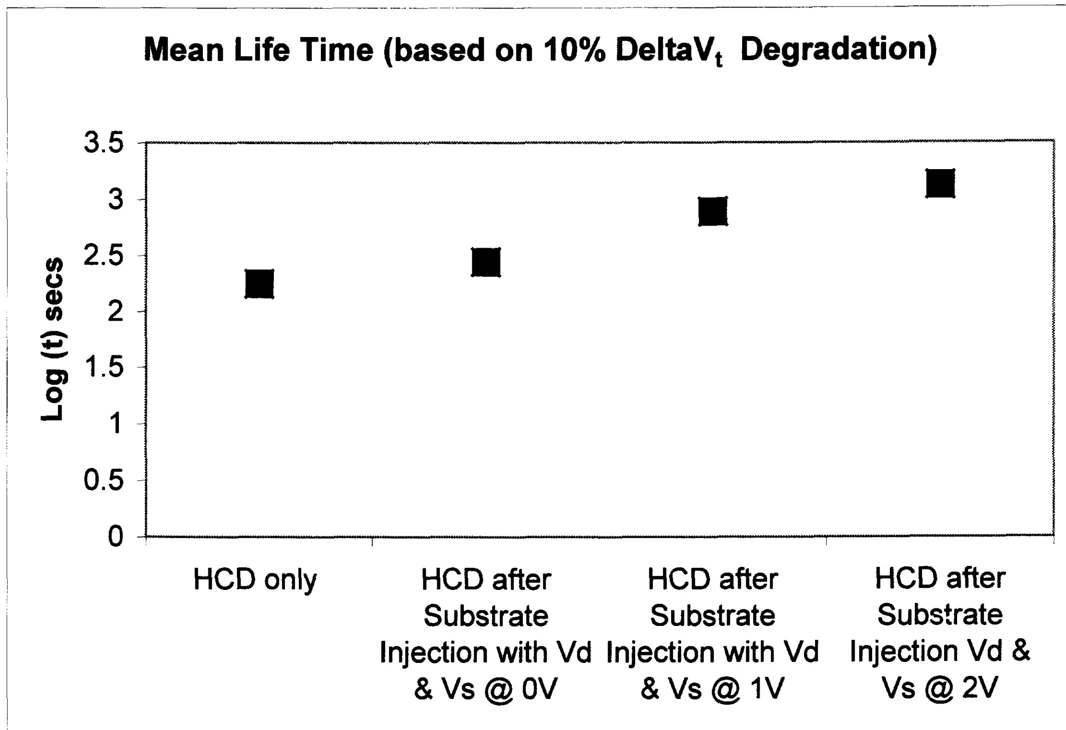

Figure 5.7 Lifetime for transistors with different stress condition (midsize antenna).

5.3 Results for Transistors with Largest Antenna Ratio

The transistors with gates connected to antenna ratio of 50050 were put to similar set of stress conditions as per Section 4.3. The following sections present their results.

5.3.1 Results for Hot Carrier Stressed Transistors

The following table shows lifetime values for transistors applied with hot carrier stress.

Lifetime (Log(t) seconds) Threshold voltage	Lifetime (Log(t) seconds) Transconductance
1.993717327	5.150011339
2.393445417	5.456863785
2.061684157	4.719056496
2.38982038	4.937731031
2.193400122	4.979401224

5.3.2 Results for Transistors with Substrate Injection

The following table shows lifetime values for transistors applied with substrate injection and reverse bias of 0V on the drain and source.

Lifetime (Log(t) seconds) Threshold voltage	Lifetime (Log(t) seconds) Transconductance
2.165441062	4.724200519
2.118732441	5.032830894
2.280795218	5.153455579
1.955221866	4.334935849
2.605102474	4.536067193

The following table shows lifetime values for transistors applied with substrate injection and reverse bias of 1V on the drain and source.

Lifetime (Log(t) seconds) Threshold voltage	Lifetime (Log(t) seconds) Transconductance
2.431718447	4.73510675
2.308473562	4.868143699
2.298694194	5.821134519
1.900320517	4.628406577
2.493786251	5.061647234

The following table shows lifetime values for transistors applied with substrate injection and reverse bias of 2V on the drain and source.

Lifetime (Log(t) seconds) Threshold voltage	Lifetime (Log(t) seconds) Transconductance
1.561676275	3.89992449
2.387227779	4.836774909
2.4566765	4.779236032
2.299539118	5.043845561
1.561676275	3.89992449

The mean values for each of the above measurements were taken and used for comparison. The Figure 5.8 and Figure 5.9 show comparison of all the hot carrier

lifetimes for 10% degradation in transconductance and threshold voltage values under different stress conditions, respectively.

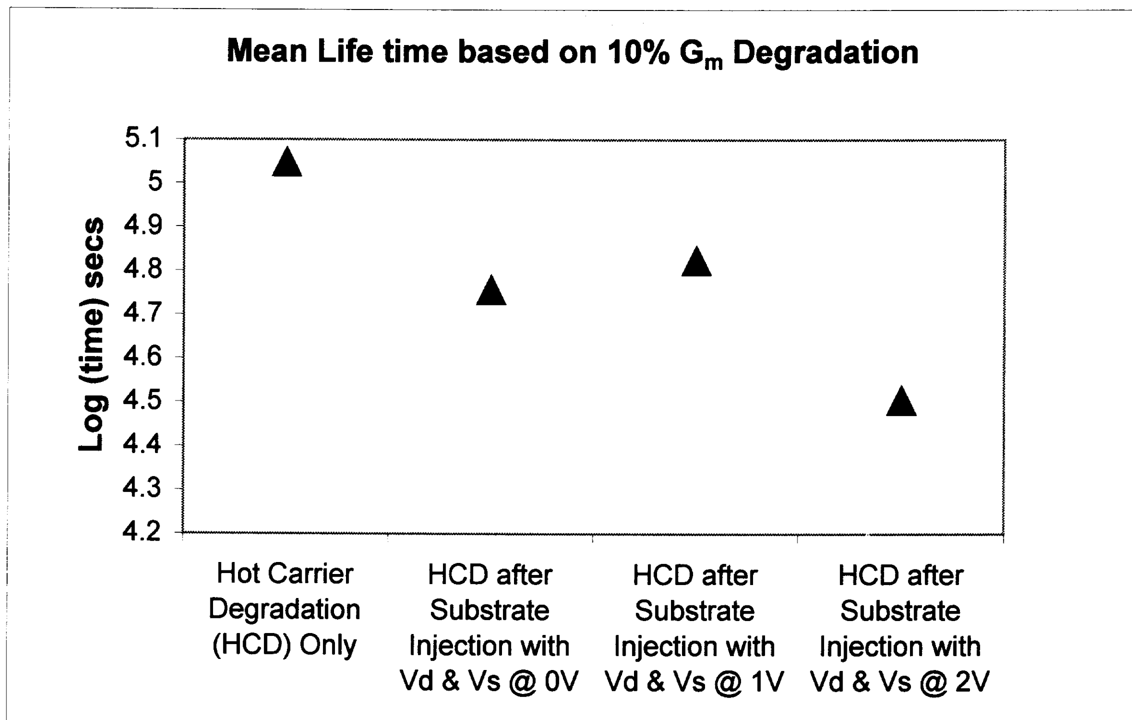

Figure 5.8 Lifetime for transistors with different stress condition (large antenna).

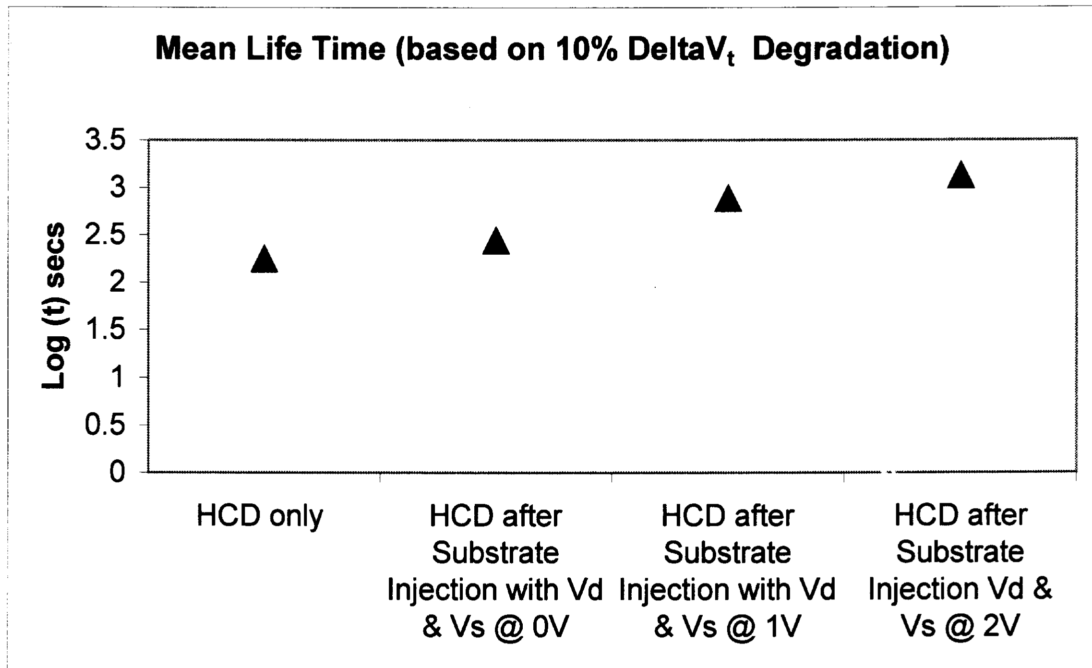

Figure 5.9 Lifetime for transistors with different stress condition (large antenna).

The plot giving a comparison of all measurements for three sizes of antenna is for transconductance degradation is given in Figure 5.10. It is observed that larger antenna acquire more plasma charge damage during the plasma processing thereby passing it to the gate oxide and damaging the oxide to a greater extent. The lifetime of such devices is reduced by the initial plasma damage, which is evident in the results when compared with devices with smaller antenna ratio. Also notable point is that transistors with different antenna ratio follow an identical lifetime characteristics for substrate injection with different reverse bias values.

The threshold voltage shifts after substrate injection. On comparison of the threshold voltage measured after substrate injection for devices with different antenna ratios, it is found that the devices with larger antenna ratios show the most shift in the

measured values of threshold voltage. The comparison with different conditions of reverse bias potentials on source and drain junctions is shown in the Figure 5.11.

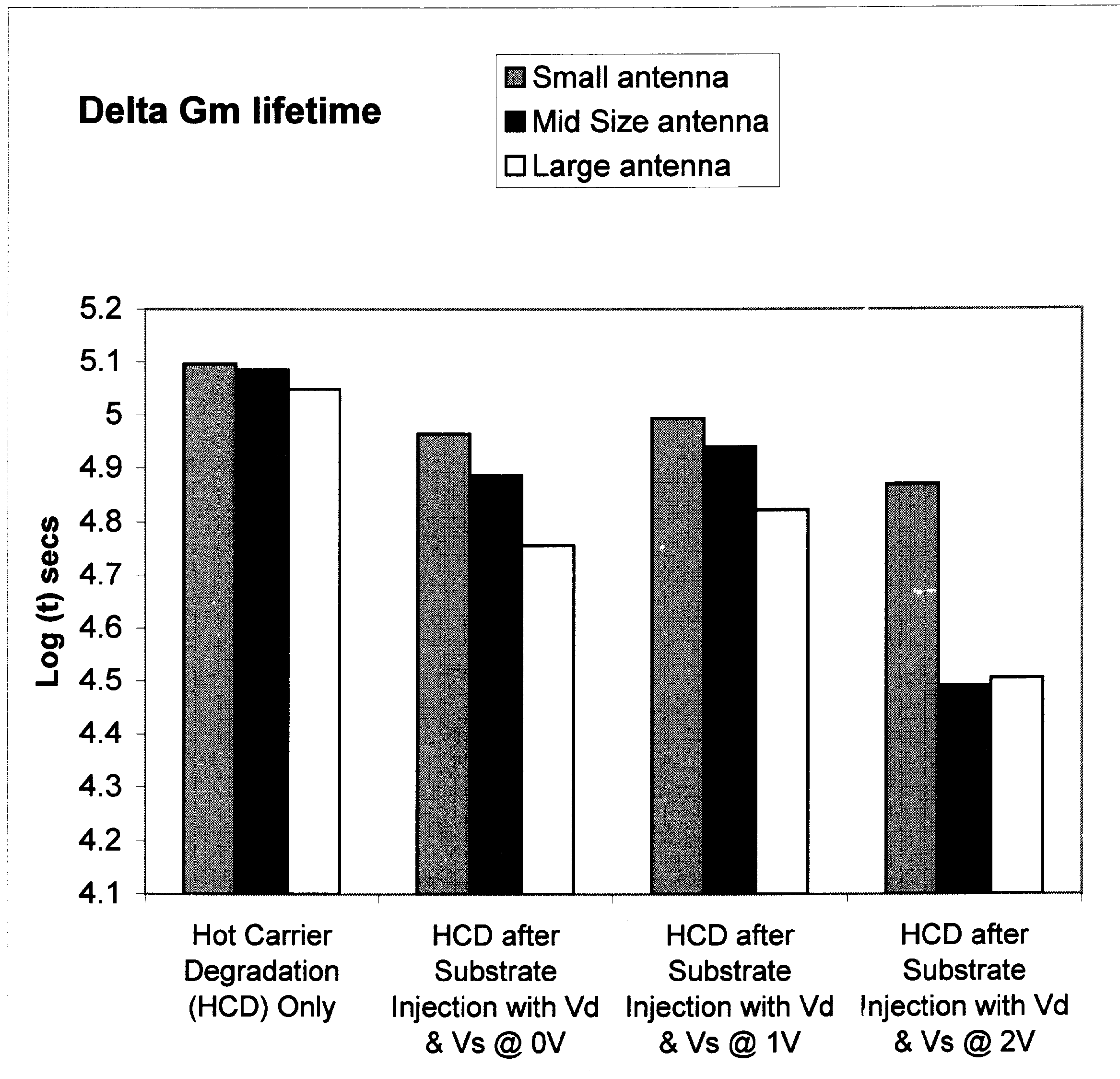

Figure 5.10 Comparison of lifetime for transistors with different antenna ratios.

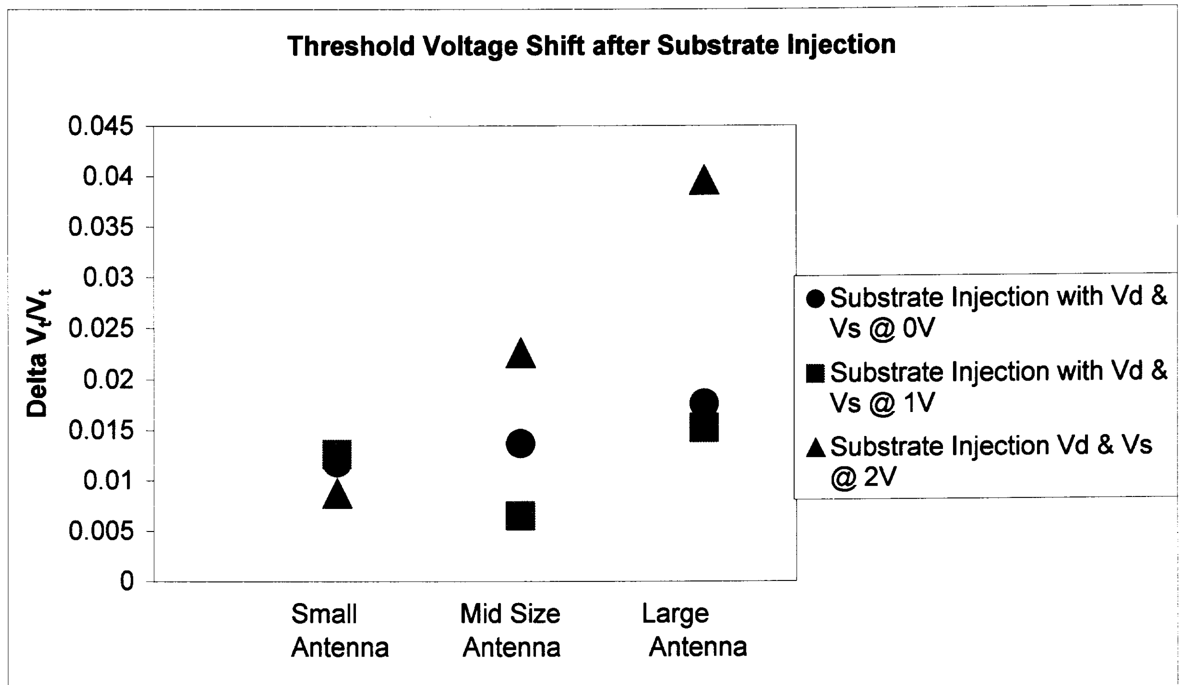

Figure 5.11 Comparison of threshold voltage shift for transistors with different antenna ratios.

5.4 Discussion

The lifetime results for HCD and substrate injection followed by HCD stress are shown in Sections 5.1, 5.2 and 5.3. The transconductance lifetime deteriorates with reverse bias of 0V but improves with 1V and gain deteriorates with 2V at drain-source terminals. The following sections discuss the results for different conditions applied during measurement.

5.4.1 Result Discussion for Hot Carrier Stress

During the hot carrier stress (HCD), the high field formed at the gate-drain junction. The free carriers passing through the high-field can gain sufficient energy to cause several

hot-carrier effects. This can cause many serious problems for the device operation. Hot carriers can have sufficient energy to overcome the oxide-Si barrier. They are injected from channel to the gate oxide and cause gate current to flow. Trapping of some of this charge can change threshold voltage permanently. Avalanching can take place producing electron-hole pairs. The measured threshold voltage and transconductance after stress on the transistors show deterioration. This is shown in Figure 5.1 and 5.2. There is a shift in the values of threshold voltage and transconductance on after measurement of each application of hot carrier stress. The shift in V_t shows electron trapping in the gate oxide. Figure 5.12 shows the LDD MOS transistor. The HCD stress degrades the gate-drain end of the oxide in the transistor, which is shown in pictorial form in Figure 5.13. The Figure 5.13 shows the electrons being injected from the channel to the gate-drain junction due to hot carrier stress condition.

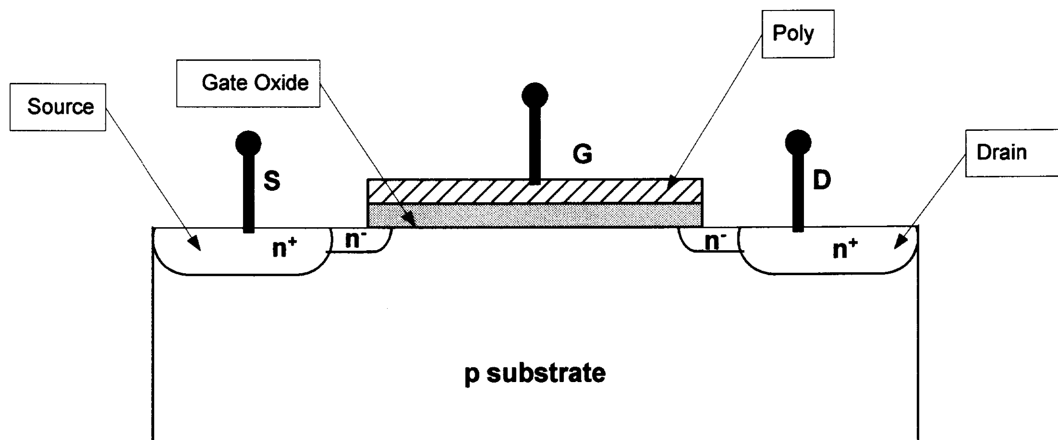

Figure 5.12 MOSFET with LDD structure.

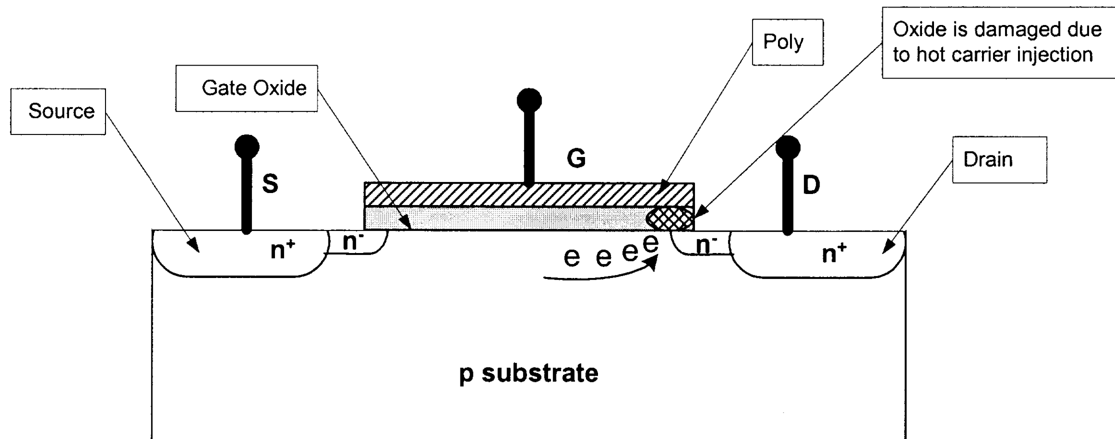

Figure 5.13 MOSFET under HCD stress.

5.4.2 Result Discussion for Substrate Injection and Reverse Bias of 0V

During this stress condition, since there is no reverse bias at the drain and source (0V) during substrate injection, on application of HCD stress, the lifetime results for transconductance are expected to be similar to that of section 5.4.1. However, that is not the case and the lifetime of measured parameters deteriorates. This is due to the fact that FN injection/stress or substrate injection as discussed in section 5.4 causes current to flow through the gate oxide that generates interface traps near the Si-SiO_2 interface. This phenomenon affects the drain current and therefore the transconductance. Since transconductance depends on oxide capacitance and mobility, the substrate injection condition degrades the oxide interface quality affecting the capacitance and generates the interface states that affects the mobility of channel carriers. The HCD stress application that follow the substrate injection cause electron hole pairs to be generated due to injected electrons, which cause further damage to integrity of the gate oxide. This results in degradation of lifetime for transconductance.

The Figure 5.14 shows the damage caused by the substrate injection and hot carrier stress in a pictorial form.

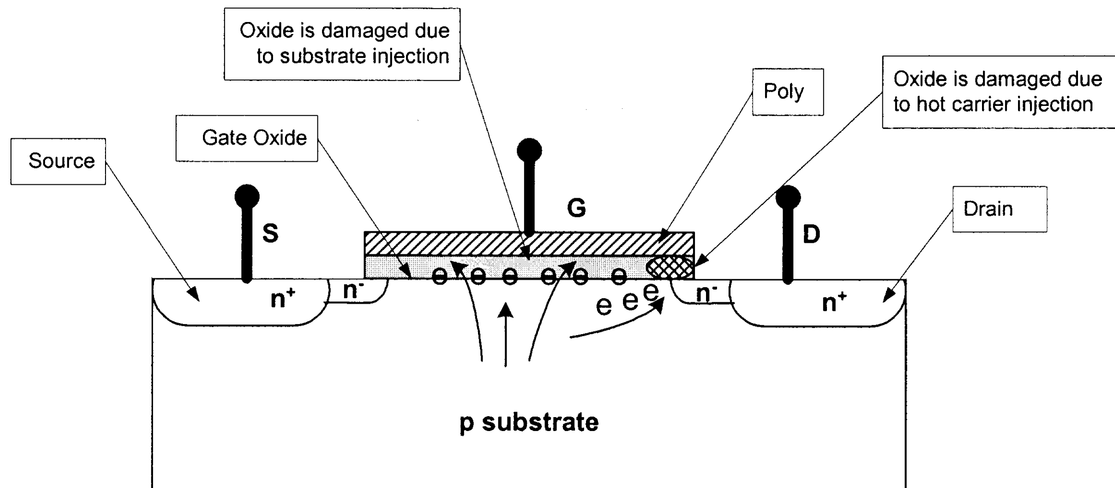

Figure 5.14 MOSFET during substrate injection with reverse bias of 0V.

5.4.3 Result Discussion for Substrate Injection and Reverse Bias of 1V

During this stress condition, since there is a reverse bias of 1V at the drain and source during substrate injection a depletion region is formed around the drain and source. This reduces the effective channel of the nMOSFET increasing the drain current. The substrate injection during the reverse bias does degrade the gate oxide quality. The reverse bias of 1V screens the drain end of the Si/SiO_2 interface during the substrate injection as compared to substrate injection and 0V reverse bias. The lifetime of transconductance improves in this case. This is supported by the measurements and shown in Figure 5.4. Figure 5.15 gives a pictorial view of the transistor under substrate injection with reverse bias at drain and source. The depletion layer is shown for understanding, which cause the carriers to be concentrated more towards the center of the gate oxide.

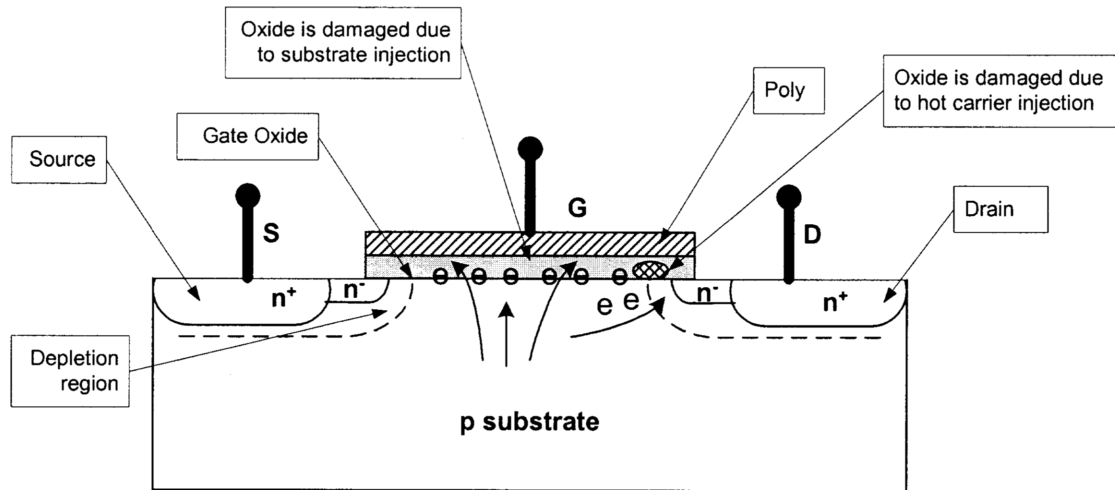

Figure 5.15 MOSFET during substrate injection with reverse bias of 1V.

5.4.4 Result Discussion for Substrate Injection and Reverse Bias of 2V

On application of substrate injection with reverse bias of 2V at drain-source terminals, the depletion region formed at drain and source widens, however this causes the current density to increase more in the gate oxide. The lifetime of transconductance degrade significantly due to the increased current density concentrated in the center of gate oxide caused by higher depletion widths on both gate-source and gate-drain junction edges. This is shown in a pictorial form in the following Figure 5.16. The results in Figure 5.4 prove the phenomenon. The depletion region formed during the substrate injection protects the gate-drain and gate-source junction edges, causing current density to increase in the gate oxide. This phenomenon damages the gate oxide in the region between the gate-source and gate-drain junction edges

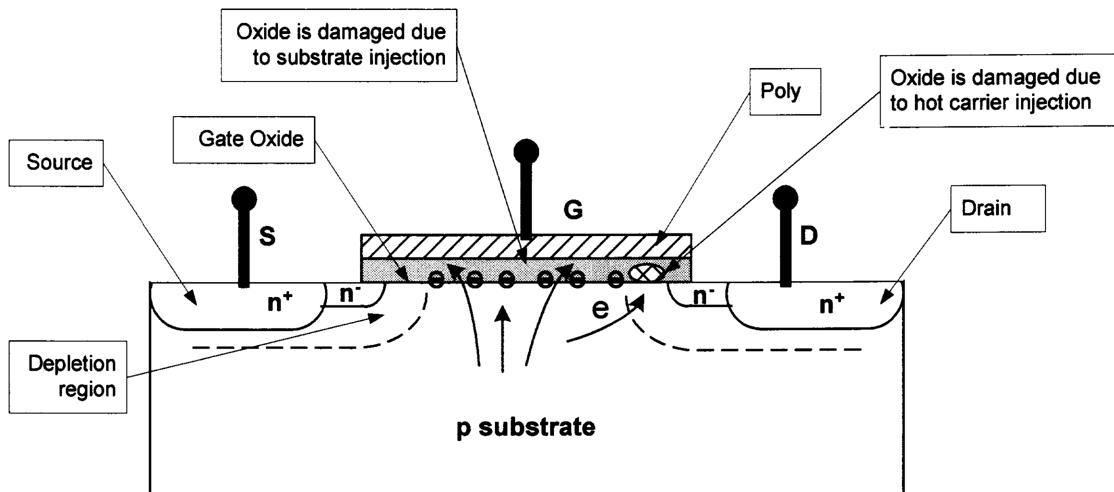

Figure 5.16 MOSFET during substrate injection with reverse bias of 2V.

The lifetime of device is affected by substrate injection along with reverse bias at the drain and source terminals. The transconductance lifetime improves with 1V at the drain-source, however, degrades when its increased to 2V, this is due to a higher reverse bias voltage of 2V increasing the field during the current stress and bringing them closer to breakdown. This condition adds additional trapping in the oxide.

5.5 Summary

The hot carrier lifetime charts shown in Figures 5.4, 5.6 and 5.8 show the lifetime degradation for substrate injection and reverse bias at the source and drain junctions for devices with different antenna ratios. The hot carrier lifetime improves somewhat for reverse bias of 1V at source and drain junction with current stress and it is not better than devices without substrate injection. The substrate injection causes electron trapping at the interface that degrades the transconductance of the device.

CHAPTER 6

CONCLUSIONS

The results given in Chapter 5 explain the dependence of hot carrier lifetime on reverse bias during substrate injection. During the current stress along with 0V reverse bias at the source and drain junctions, the channel length remains unaffected, as the depletion layer is not significant enough to protect the oxide at the drain edges. The substrate injection creates electron traps near the Si-SiO_2 interface causing shifts in threshold voltage. These traps also reduce the mobility of carriers from the source to drain during operation resulting in reduced transconductance, thereby reducing the device hot carrier lifetime.

In the case of 1V reverse bias at the source and drain, the lateral expansion of the depletion region at the drain edge prevents the damage to gate oxide near the drain edges. This is reflected in the hot carrier lifetime measurements.

On the other hand when the reverse bias becomes 2V, the device is degrade due to the increase in the field that brings the device near the breakdown condition. During this condition significant carrier trapping reduces the hot carrier lifetime of the device.

The experiments results support the notion that depletion layer formed by reverse bias during substrate injection affect the device reliability. Consideration of these results could help improve device reliability subjected to plasma processes in the chip fabrication. The results showing improvement in device hot carrier lifetime based on threshold voltage shifts are subjected to future work investigation.

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