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ABSTRACT

ELECTRICAL PROPERTIES OF ULTRA THIN Al_2O_3 AND HfO_2 FILMS AS GATE DIELECTRICS IN MOS TECHNOLOGY

by
Vishal R. Mehta

The rapidly evolving silicon industry demands devices with high-speed and low power consumption. This has led to aggressive scaling of the dimensions in metal oxide semiconductor field effect transistors (MOSFETs). The channel length has been reduced as a result of this scaling. The industry favorite, SiO_2, has reached limitations in the thickness regime of 1-1.5 nm as a gate dielectric. High-κ gate dielectrics such as Al_2O_3 and HfO_2 and their silicates are some of the materials that may, probably, replace SiO_2 as gate dielectric in the next four to five years. The present study is an attempt to understand the electrical characteristics of these exciting materials grown by atomic layer deposition (ALD) technique. The flat band voltages (V_{FB}) were determined from C-V measurements on circularly patterned MOS capacitors. For phosphorous doped polysilicon electrodes and Al-oxide based dielectrics, positive shifts in V_{FB} were observed, relative to a pure SiO_2 control, ranging from 0.2 to 0.8V. It is believed that this is caused by fixed charges. Rapid thermal annealing at 1000°C tends to decrease V_{FB} relative to a 800°C anneal. Changes in V_{FB} up to 0.35 V are observed for films deposited over SiO_2 underlayers, while smaller changes, up to 0.05 V, are observed for films deposited directly on Si. Spike annealing is also observed to reduce oxide leakage. HfO_2 showed large amount of leakage resulting in difficulty in performing capacitance measurements. ZrO_2 was found to be reacting with polycrystalline silicon and thus high leakage current was observed.

ELECTRICAL PROPERTIES OF ULTRA THIN Al_2O_3 AND HfO_2 FILMS AS GATE DIELECTRICS IN MOS TECHNOLOGY

by

Vishal R. Mehta

A Thesis
Submitted to the Faculty of
New Jersey Institute of Technology
In Partial Fulfillment of the Requirements for Degree of
Master of Science in Materials Science and Engineering

Interdisciplinary Program in Materials Science and Engineering

August 2002

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APPROVAL PAGE

ELECTRICAL PROPERTIES OF ULTRA THIN Al_2O_3 AND HfO_2 FILMS AS GATE DIELECTRICS IN MOS TECHNOLOGY

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Dedicated to my beloved family

ACKNOWLEDGEMENT

The author wishes to express his sincere gratitude to his co-advisors Dr. N. M. Ravindra and Dr. Anthony Fiory for their guidance and encouragement given throughout this research. The author would like to give special thanks to Dr. Dentcho Ivanov and Dr. Sufian Abedrabbo for serving as members of the thesis committee. The author is grateful to Professor N. M. Ravindra for helping with grants, to identify the research topic and also, for helping throughout the research.

The author appreciates the support of Dr. Glen Wilk (Agere Systems) and also of Ms. Mun Yee Ho (Agere System intern from Singapore State University) for helping with the materials and sharing their knowledge. The MOS devices were processed in the nanofabrication cleanroom of Bell Labs. The author is grateful to Tom Sorsch for giving helpful suggestions in his research activities.

The author is thankful to Mr. Henry McCloud and Mrs. Lorna Derilhomme Joasil for their continued support during his course of studies.

Finally, the author expresses words of gratitude to colleagues Aravind Balakrishnan, Sridhar Madishetty, Samrat Chawda and Anand Shenoy for their help and support throughout the course of this research.

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CHAPTER 1

INTRODUCTION

Since 1947, when the first bipolar transistor was constructed at Bell Labs [1], the semiconductor industry has come a long way. As scientists gain knowledge of the silicon material behavior at various voltages and temperature, progressively more useful devices are being introduced into the market. With rapid strides in the manufacturing technology, device sizes have also shrunk, thus demanding better material properties and characteristics. Millions of complimentary metal oxide semiconductor (CMOS) devices are fabricated on 300mm wafers. In CMOS, the Metal Oxide Field Effect Transistor (MOSFET) is the building block. The MOSFET is one of the many types of FETs, which is widely used in integrated circuits (ICs). FETs came into general use only in the late 1960s. In FETs, the current from source to drain is controlled by the application of potential (i.e., electric field) on the gate. Thus, the device is called field effect transistor. FET has a negative temperature coefficient at high current levels [2]. This behavior results in uniform distribution over the device area and prevents the FET from thermal runaway. FETs also offer high switching speeds and cutoff frequencies [1].

Field effect transistor is a unipolar device; that is, current is controlled by majority carriers only. It has three terminals which function as follows:

(1) Source: As the name suggests, it is one of the heavily doped regions of the FET from which carriers are transferred to the channel.

(2) Drain: This is also a heavily doped region of FET from where the carriers leave the transistor.

(3) Gate: This is the structure used to control the outgoing current. It is mainly made up of polysilicon. Historically, it used to be made up of metal (i.e. aluminum, platinum, etc).

The normally heavily doped source and drain regions are either diffused or implanted into a relatively lightly doped substrate. Ion implantation is a widely used commercial method for this purpose. A thin oxide layer either thermally grown or deposited separates the conducting gate from the Si surface.

Presently, several different types of FETs are available. When the junction is replaced by Schottky barrier, it is called Metal Semiconductor Field Effect Transistor (MESFET). The metal gate electrode can be separated from the semiconductor by an insulator; the device thus created is called a Metal Insulator Semiconductor Field Effect Transistor (MISFET). A more commonly used silicon device is Metal Oxide Semiconductor Field Effect Transistor (MOSFET), which uses SiO_2 or nitrided (N doped oxide) SiO_2 as the gate dielectric. The MOSFET is described in greater detail in Chapter 2.

In order to decrease the time constant of MOSFETs, the channel length is being continuously reduced. The state of the art in commercial production device has 130 nm-channel length and gate oxide of 1.5 nm thickness. However, the applied voltage has not been scaled at the same rate as the dimensions of the device. This situation creates problems. There are fringing field side effects. The reduction in thickness increases the capacitance. However, electrons can easily tunnel through the thin gate oxide. This causes decrease in input impedance and increase in leakage current. There is a concentrated effort to replace the gate oxide (i.e. SiO_2). If a high dielectric constant material is used, the same capacitance value can be obtained with increased thickness.

Thick films are known to reduce quantum mechanical tunneling of the oxide. Hafnium oxides, aluminum oxides and their silicates are the front-runners in this race to find a suitable gate dielectric in the next three to four years.

The second chapter in this study focuses on the fundamentals of p-n junction diodes and the effects of forward and reverse bias. It ends with brief description of the properties of MOSFETs. The third chapter explains the advantages and limitations of SiO_2 and the need to replace SiO_2. It ends with description of silicon nitride (Si_3N_4) and the importance of oxynitrides.

The fourth chapter describes the different physical as well as electrical properties of high-κ dielectrics and their benefits. Fifth chapter explains carrier behavior at low and high frequencies by utilizing Capacitance-Voltage (C-V) measurements. The C-V technique is used to find oxide thickness, fixed charges, interface traps and doping density. A short note about the current conduction mechanism in gate oxides is presented. The chapter concludes with discussion of several theories of time dependent dielectric breakdown (TDDB).

The sixth chapter presents results and discussion of electrical test experiments on capacitors prepared with various high-κ dielectrics. Various experimental observations are presented regarding shift in the flat band voltage (V_{FB}) and its possible interpretations.

CHAPTER 2

METAL OXIDE SEMICONDUCTOR DEVICE FUNDAMENTALS

2.1 The p-n Junction

When a p-type or an n-type semiconductor is diffused with n- or p-type impurities, a p-n junction is created. For simplicity, the formation of an abrupt p-n junction is shown in Figures 2.1 (a) and (b). There is a flow of electrons from the n-type to the p-type material and flow of holes from the p-type material to the n-type semiconductor. Thus, there is depletion of electrons near the junction in the n-type material and holes in the p- type region. This is called the depletion region of width W.

The resulting electric field ε is directed from the positive charge towards the negative charge. It is in the direction opposite to that of diffusion current for each type of carrier. Thus, the field creates a drift component of current from n to p opposing the diffusion current. At equilibrium, the drift and diffusion currents cancel each other (Figure 2.1(c)). Therefore, electric fields are built up to a point where the net current is zero at equilibrium, assuming the electric field is zero in the neutral region. Hence, a potential difference is generated at the p-n junction [2].

This potential difference is called contact potential V_0, which is also the built in potential barrier, in the transition region. It is necessary to maintain equilibrium at the junction. The contact potential separates the bands (E_c = Conduction band and E_v = Valence band, refer Figure 2.1 (b)). The energy bands on either side of the junction are separated by the contact potential V_o times the electronic charge q. Also, the Fermi level must be constant throughout the device in equilibrium.

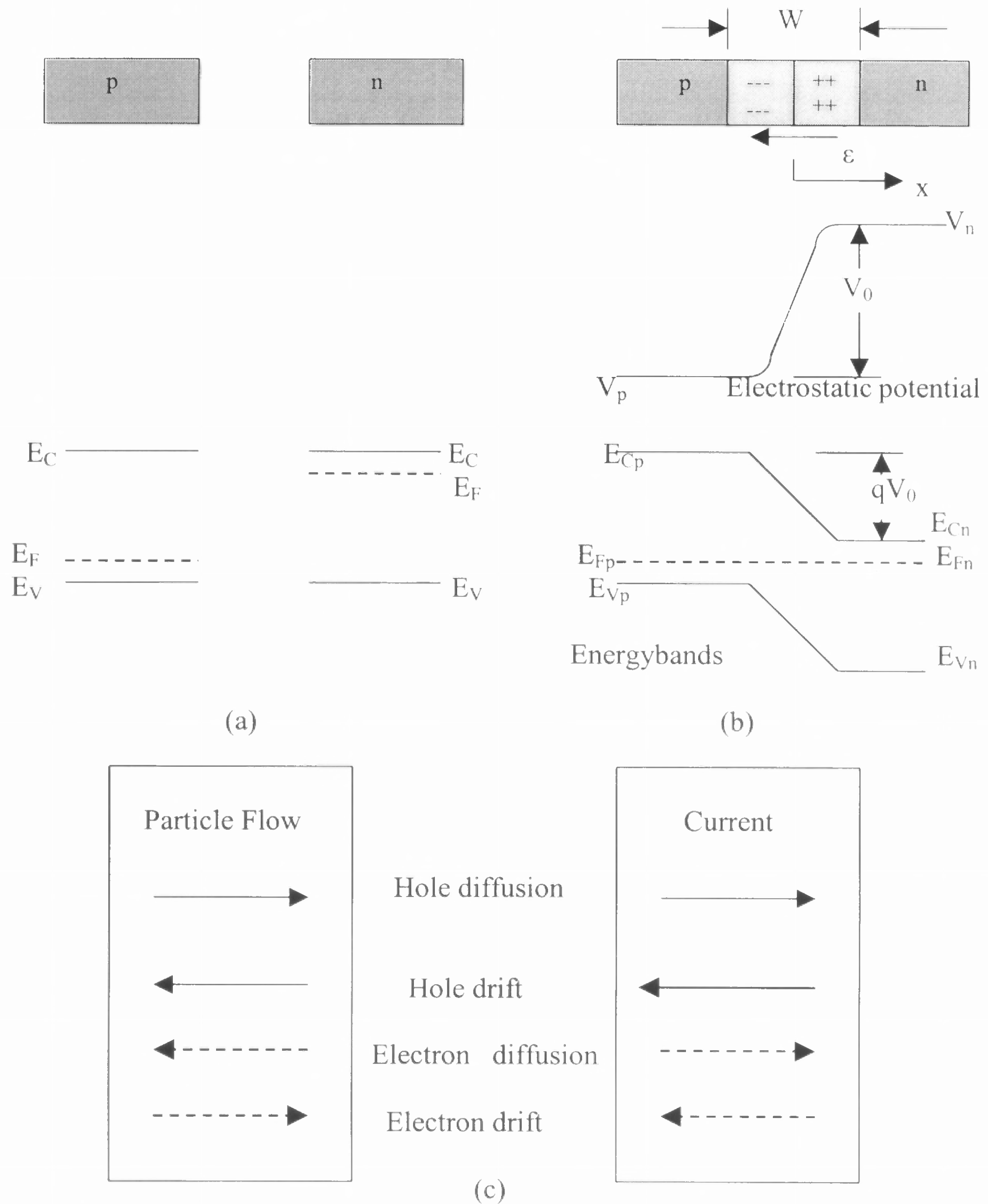


Figure 2.1 Energy Bands of p and n semiconductor (a) before contact, where E_C is the conduction band edge, E_V is the valence band edge and E_F is the Fermi level of the respective regions. (b) The electrostatic potential V_o after the regions are brought in contact, V_p is the voltage at the p region and V_n is the voltage at the n type region, E_{Cn} is the conduction band in the n region after contact, E_{Vn} is the valance band in the n region after joining, E_{Cp} is the conduction band in the p region, E_{Vp} is the valance band in the p region after contact, E_{Fp} and E_{Fn} are the Fermi levels in the respective regions after contact. (c) The direction of the particle flow and the current flow [2].

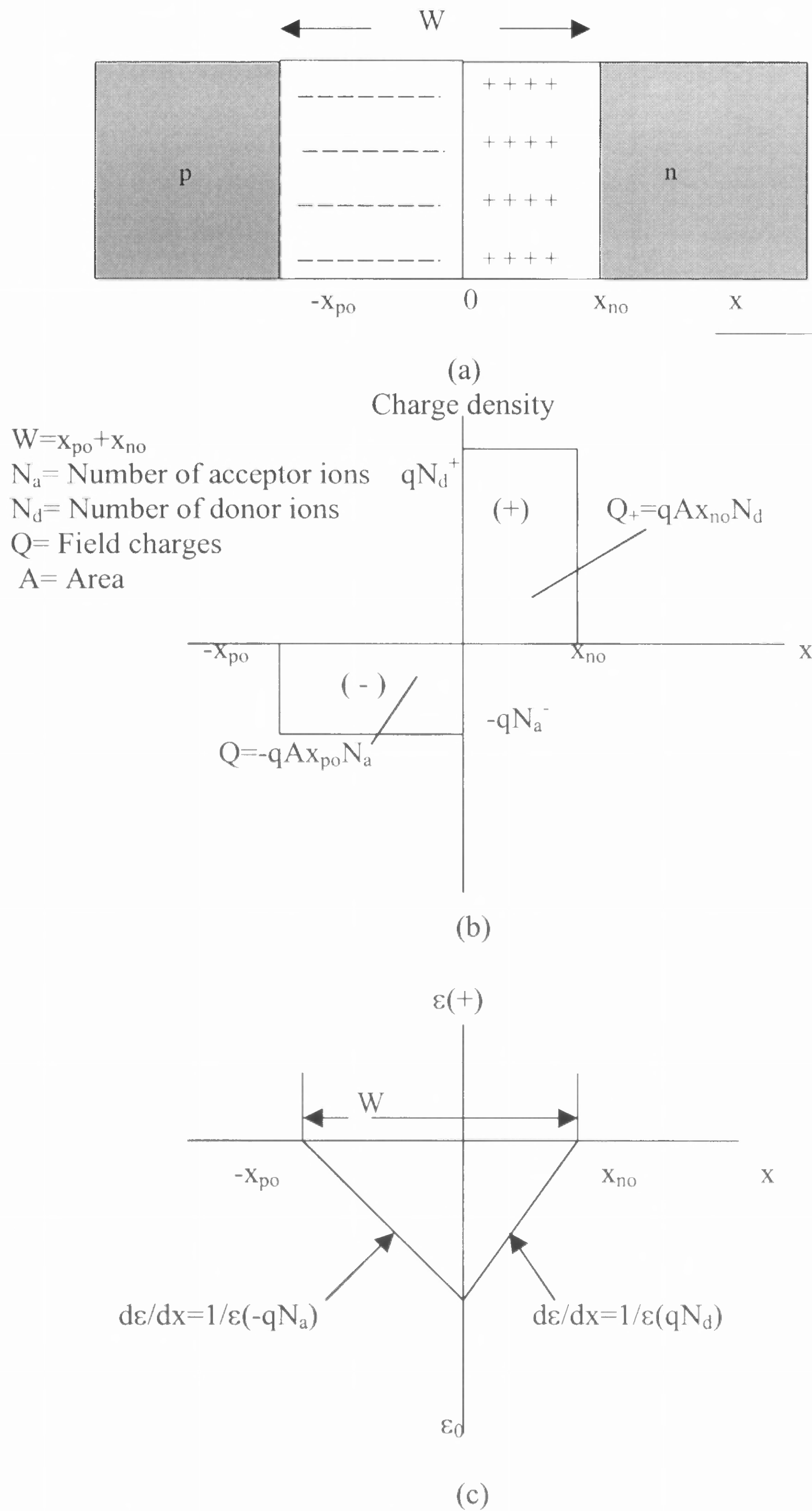


Figure 2.2 (a) The transition region with x=0 defined as metallurgical junction (b) Space charge density (c) electric field distribution [2].

The Fermi level [2] is given by the equation,

$$F(E_i) = \frac{1}{1 + e^{(Ec - EF)/kT}} \qquad (2.1)$$

where, E_i is the intrinsic Fermi level. The Fermi level is near the valence band in p-type material, while it is near the conduction band, in n type material. Figure 2.2 illustrates the electric field and charge distributions in the p-n junction area (i.e., depletion region).

2.2 Forward and Reverse Bias

An applied voltage changes the potential barrier and the electric field within the transition region. Thus, changes in the various current components are expected. The potential barrier is lowered when the junction is forward biased. The electrons have more energy and they can diffuse from n to p region. Similarly, holes can diffuse from p to n. Thus, electron diffusion current is greater in forward bias. In reverse bias, the barrier becomes so large that the diffusion current is negligible [2]. This is shown in Figure 2.3.

Two types of currents are mainly involved in the conduction process. These are diffusion current and drift current. The drift current is insensitive to the height of the potential barrier. The drift current arises because of the minority carrier in each region being swept down the potential barrier under the applied field. The number of minority carriers in turn depends on the generation of electron hole pairs. The total current is composed of the sum of both diffusion and drift currents.

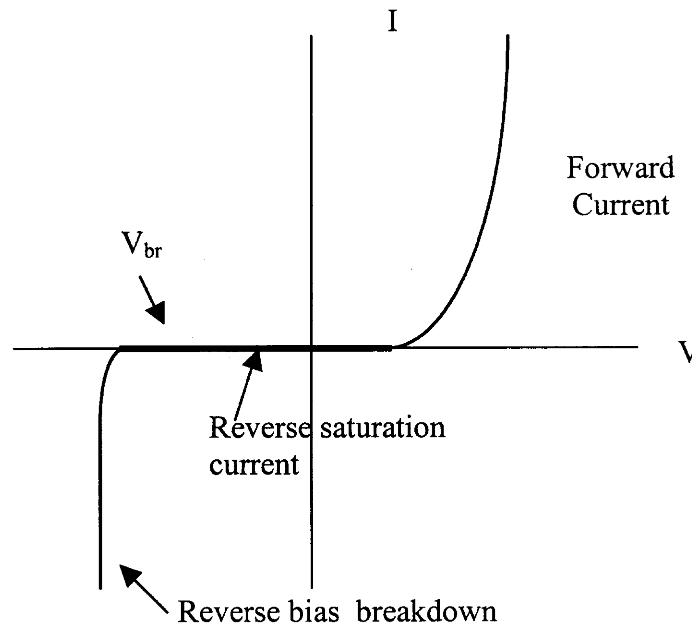


Figure 2.3 Current-voltage characteristics a p-n junction [2].

2.3 Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

The MOSFET is widely used in CMOS circuits where it is switched from the "off" state to "on" state. As the name suggests, the MOSFET has an oxide layer separating the gate electrode and the substrate. It is known as the gate oxide. Figure 2.4 is a schematic representation of an n-type MOSFET. The basic operation of the MOSFET is as follows.

The gate dielectric in between the gate and the substrate has a large band gap and a high dielectric constant. The gate electrode can either be of metal or highly doped polycrystalline silicon (polysilicon). Source and drain are doped in the substrate by ion implantation and then diffused by thermal diffusion. The morphology of the interface between the oxide and the substrate is very critical for the desired operation of the device. It should be smooth, as any roughness might scatter the electrons and reduce the carrier mobility. Since the Fermi level is near the different bands in the adjacent regions, there is

a barrier for the carriers due to the built in potential of the back-to-back p-n junctions between the source and drain. No current flows from drain to source without a conducting channel between them. Figure 2.5 explains the change in the number of carriers with the applied bias of an n-type MOSFET.

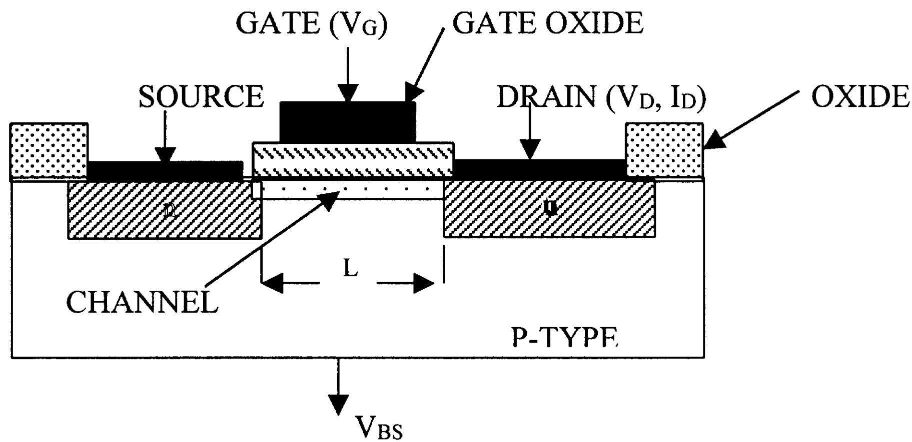


Figure 2.4 Schematic diagram of an n-type MOSFET.

With the application of the voltage at the gate (V_G), the outgoing current from the drain (I_D) can be controlled. This occurs because of the inversion of the semiconductor layer below the gate due to the dielectric effect of the high permittivity material (i.e., SiO_2). For a p type substrate, n channel will be created below the gate. Since electrons are electrostatically induced in the p-type channel region, the channel becomes less p-type. Therefore, the valence band moves down further away from the Fermi level [2]. This reduces the barrier for the electrons to move from source to drain. If this barrier is reduced sufficiently, by applying voltage in excess of threshold Voltage, V_T, there is significant current flow form source to drain. It is very important to have high quality, low leakage p-n junctions in order to ensure a low off-state leakage current in the

MOSFET. The threshold voltage (V_T) is the minimum gate voltage required to induce a conducting channel. This type of transistor is normally off with zero gate voltage and operates in the enhancement mode, by applying gate voltage large enough to induce a conducting channel.

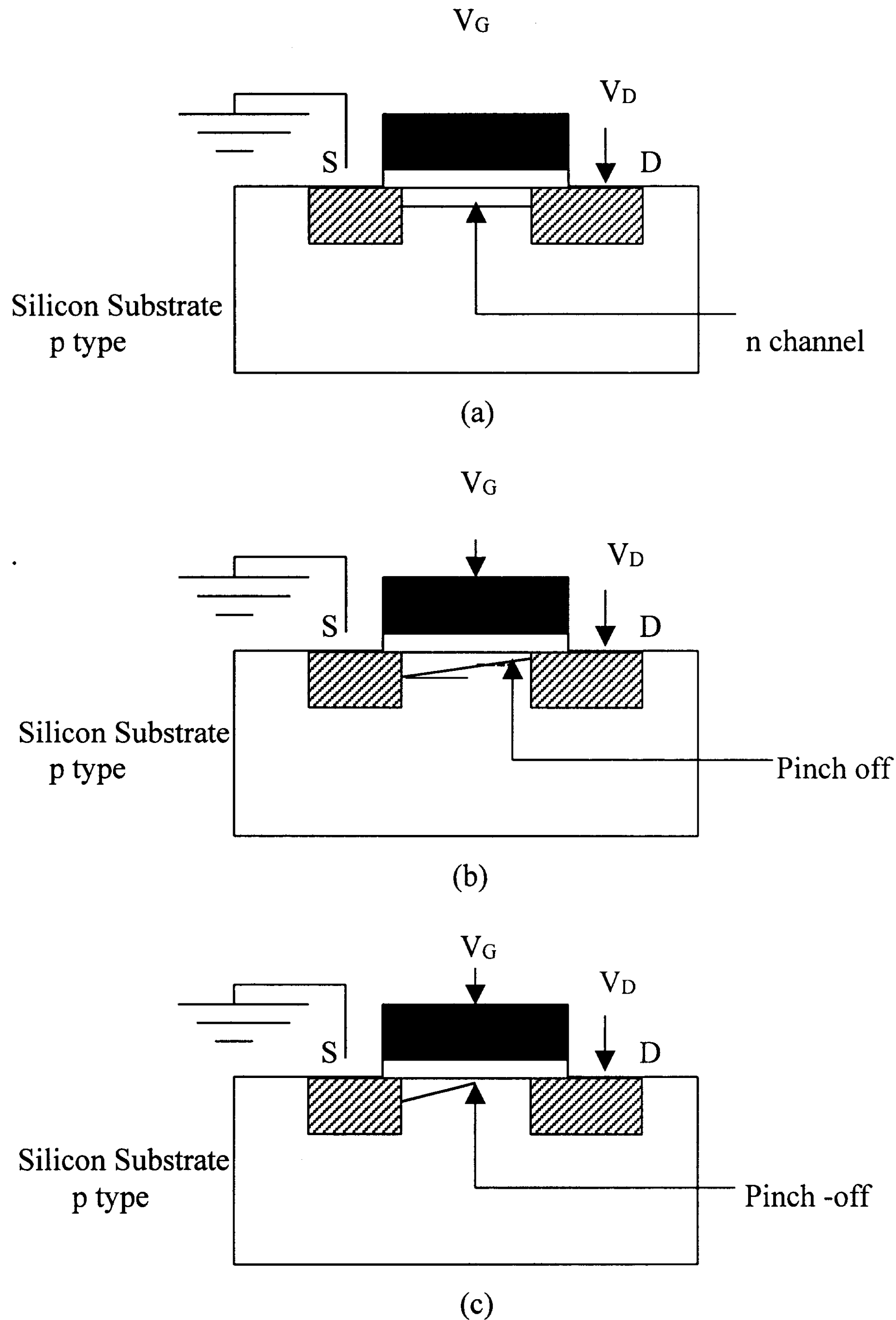


Figure 2.5 n channel MOSFET cross section under various operating conditions.

An increased positive voltage creates a more conducting n-channel. This increases the drain current flow in the channel (Figure 2.5a.). However, there is more Ohmic voltage drop along the channel such that the channel potential varies from zero near the grounded source to whatever the applied drain potential (V_D) is near the drain end of the channel [2].

Hence, the voltage difference between the gate and the channel reduces from V_G near the source to (V_G-V_D) near the drain end. Once the drain bias is increased to the point that (V_G-V_D) =V_T, threshold is barely maintained near the drain end, and the channel is said to be pinched off (Figure 2.5 b) [2].

Increasing the drain bias beyond this point (V_D (sat.)) causes the point at which the channel gets pinched off, to move more and more into the channel, closer to the source end (Figure 2.5 c). Electrons in the channel are pulled into the pinch-off region and travel at the saturation drift velocity because of the very high longitudinal electric field along the channel. Now, the drain current is said to be in the saturation region because it does not increase with drain bias significantly [2].

A MOS capacitor is used to study the properties of the gate dielectric that is used in the fabrication of the MOSFET. An MOS capacitor can be used to measure a large number of properties. Surface band bending and depletion layer width in the silicon as a function of gate bias can be measured. Doping profile in the silicon can be obtained from the MOS capacitor. Voltage and field at avalanche breakdown in the silicon can be determined. For many measurements, the n channel MOSFET is preferred because the mobility of electrons in silicon is higher than for holes. Electrical characterization of the MOS capacitor is described in Chapter 5.

CHAPTER 3

REPLACEMENT OF GATE DIELECTRIC

3.1 Limitation of Silicon Dioxide

Silicon dioxide has good interface properties with the underlying silicon substrate. In order to be used as an effective gate oxide, an alternative high-κ material should have a large band gap and an amorphous structure. If the dielectric has a polycrystalline structure, then the electrons can travel through the grain boundaries and cause leakage of the current, thus discharging the capacitor [3]. In Table 3.1 the various properties of gate dielectric materials are summarized. A good interface quality between the substrate and the dielectric is also desired so as to not to affect the mobility of the electrons by deflection of the surface atoms.

The gate oxide should also have low fixed charge so as not to affect the threshold voltage, which is required to switch on or off the device. In the present study, it has been shown that presence of the fixed oxide charge causes shift in the flatband voltage. SiO_2 has been ideal in all the above-mentioned properties. This explains why SiO_2 has enjoyed a limelight as a useful gate dielectric for many years.

The drive current I_d for the MOS device increases with respect to applied drain voltage V_d and then it saturates to a maximum at V_{dsat} [3]. It is given by,

$$I_{d,sat} = (W/L)\mu C_{inv} \{(V_{d,sat})^2/2\} \quad (3.1)$$

Where, W is the width of the transistor channel, L is the channel length, μ is the channel carrier mobility, and C_{inv} is the capacitance density associated with the gate dielectric. When the underlying channel is in the inverted state, $V_D = V_G - V_T$.

To increase drain current, either capacitance has to be increased or the channel length has to be decreased. V_d suffers from constraints on electric field, reliability and room temperature. SiO_2 has been widely used as a gate dielectric because of its physical and electrical properties. SiO_2 is resistant to dopant diffusion. The shrinkage of the MOSFET dimensions has led to the thinning of the gate dielectric. This causes leakage current in the device to increase.

If a high dielectric constant material is used, then thicker films can be utilized as the dielectric. The equivalent oxide thickness t_{eq}, is the thickness of any dielectric scaled by the ratio of its dielectric constant to that of silicon dioxide (where ε_{oxide}=3.9) such that

$$t_x = t_{eq} (\varepsilon_x / \varepsilon_{oxide}) \tag{3.2}$$

where t_{eq} and t_x are the equivalent oxide and physical thickness respectively and ε_{oxide} and ε_x are respectively the dielectric constant of silicon dioxide and that of the other dielectric. This equation implies that we can have a high dielectric constant material which is physically thicker then SiO_2. This prevents quantum mechanical tunneling of the carriers through the dielectric layer.

With the decrease in the thickness of SiO_2, there are problems like change in the dielectric thickness, penetration of the impurities from the gate into the gate dielectric, and the reliability and lifetime of devices made with ultra thin films.

In the study by Muller et al. [4] it was found that the density of states makes a transition from the substrate into the SiO_2 layer, indicating that the full band gap of SiO_2 is obtained after only about two monolayers of SiO_2. This implies that within two monolayers of the Si channel interface, silicon atoms do not have the full arrangement of oxygen neighbors and therefore cannot form the full band gap that exists within the bulk of the SiO_2 film. These results set an absolute physical thickness limit of SiO_2 of 7 Å.

Below this thickness, the silicon rich interfacial regions from the channel and polycrystalline Si gate interfaces used in MOSFETs overlap, causing an effective "short" through the dielectric, rendering it useless as an insulator [3]. When a thin oxide layer is biased electrically, electrons tunnel through the Si/SiO_2 barrier. As oxide thickness is decreased from 8 to 2 nm, the transition from Fowler-Nordheim tunneling to direct tunneling occurs as electron conduction mechanism through the oxide [1,2,5,6]. This is described in greater detail in chapter 5.

Table 3.1 Comparison of Relevant Properties of Various High-κ Materials [11]

Material	Dielectric Constant(κ)	Band gap E_G(eV)	ΔE_C(eV) to Si	Crystal Structure	Preparation Methods
SiO_2	3.9	8.9	3.2	Amorphous	Thermal
Si_3N_4	7.0	5.1	2.0	Amorphous	LPCVD, Thermal Nitride, JVD, MOCVD
Al_2O_3	9.0	8.7	2.8	Amorphous	Sputtering, ALCVD
Y_2O_3	15.0	5.6	2.3	Cubic	
La_2O_3	30.0	4.3	2.3	Hexagonal, cubic	
Ta_2O_5	26	4.5	1-1.5	Orthorhombic	MOCVD
TiO_2	80.0	3.5	1.2	Tetragonal	MOCVD
HfO_2	25	5.7	1.5	Mono, Tetra, cubic	Sputtering, ALCVD
$BaSrTiO_3$	190				MOCVD, PVD
ZrO_2	25	7.8	1.4	Mono, Tetra, cubic	ALCVD

Silicon dioxide is an amorphous material, and as such its atomic dimensions are not well defined. Average Si-O bond lengths [7] in SiO_2 are dependent upon the local structures assumed (α- or β-quartz, tridymite, cristobalite). In SiO_2, Si forms four directional covalent bonds to oxygen atoms. The oxygen atoms are two fold coordinated with a large bond angle and a weak bond-bending force constant. The low average coordination and the floppiness of the oxygen site gives amorphous structure to SiO_2.

As the SiO_2 thickness is reduced, the gate leakage current through the film increases. Leakage specifications are device design and application dependent. For silicon dioxide, at a gate bias of ~1 V, the leakage current changes from 1×10^{-12} A/cm^2 at ~35Å to 1x10 A/cm^2 at ~15 Å [17]. When a gate stack is used, i.e., an under-layer of thin SiO_2 and a high-κ dielectric as a gate oxide, then the conduction mechanism will differ in both the oxides and the exact mechanisms are not yet known [8].

The percolation model suggested by DeGraeve et al. [5] describes breakdown in ultra thin oxides (≥ 2.5 nm) as the buildup of many "defects" within the SiO_2 layer, where in after a certain amount of stress a complete path of defects form across the oxide thickness. This point defines breakdown or failure of the oxide.

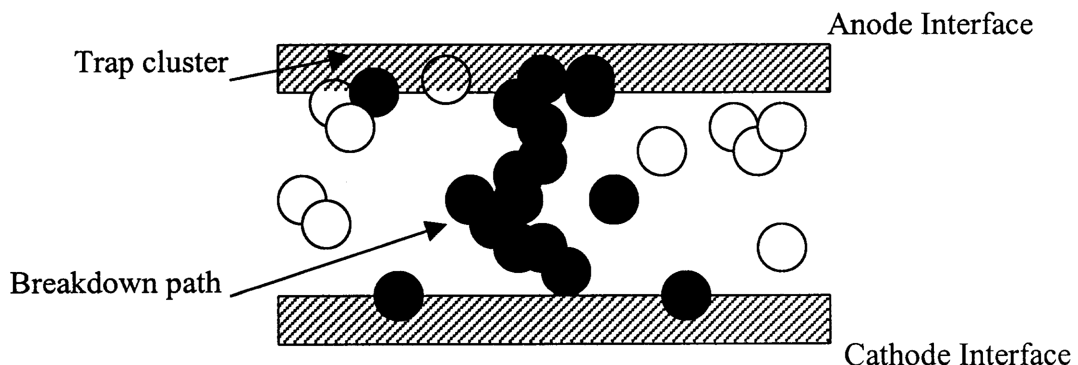


Figure 3.1 Percolation model. When trap clusters join together, breakdown occurs [6].

At this moment, the capacitor discharges through the breakdown path and thermal effects can cause further damage to the oxide locally, creating a highly conductive breakdown path. The mechanism, which leads to the creation of these defects, is however, under debate. Figure 3.1 shows the percolation model.

The speed of MOSFETs is defined by how fast conduction electrons/holes can travel in the (inverted) channel between the source and drain regions of the transistor [6]. In ultra small devices, the electrons in the channel are located very close to the very heavily doped gate, source and drain regions and as a result, the electrostatic potential in the gate and source/drain regions can extend into the channel. The long-range electrostatic interactions between these charges may have a negative impact on the performance of devices with thinner gate oxide [6]. It is likely that these electrostatic interactions will require devices with thicker high-κ dielectrics.

Table 3.2 2001 International Technology Roadmap for the Semicondutor Gate Stack. EOT is equivalent oxide thickness, I_g is gate leakage current density, T_{OX} is the oxide thickness [9]

Year of First Product Shipment Technology Node	2001 130nm	2004 90 nm	2007 65nm	2010 45nm	2013 32nm	2016 22nm
EOT for high performance T_{ox} (nm)	1.3-1.6	0.9-1.4	0.6-1.1	0.5-0.8	0.4-0.6	0.4-0.5
EOT for low operating power T_{ox} (nm)	2	1.4	1	0.9	0.8	0.7
EOT for low standby power T_{ox} (nm)	2.6	2	1.4	1	0.9	0.8
I_g at 100C (A/cm²) High Performance	$2X10^1$	$2X10^2$	$1X10^3$	$7X10^3$	$5X10^4$	$3X10^5$
I_g at 100C (A/cm²) Low operating power	0.11	0.19	0.31	0.33	0.4	0.56
Thickness control EOT (%)	<4	<4	<4	<4	<4	<4

3.2 Silicon Nitride (Si_3N_4)

Silicon Nitride has been researched for many years for its use in non-volatile memory devices. It has been known to be resistant to dopant diffusion. However, it causes threshold voltage shift. Also, its dielectric constant is not very high (Si_3N_4,$\kappa \sim 7.0$, SiO_2, $\kappa \sim 3.9$). It shows large amount of fixed charge as well as interface trap charges. Its interface properties are poor. Silicon has more affinity for O than for N. Incorporation of O is a method to improve the electrical properties of nitride layers [10].

The study of Si/Si_3N_4 interface by Lazar et al [11] showed that the presence of oxygen benefits the properties of the dielectric layer. Hydrogen, however, was found to be a defect precursor. This is due to N-H and Si-H bonds. The Si/Si_3N_4 interface is constrained. Bonding constraints arise due to differences between the average numbers of bonds per atom on each side of the interface. Studies show [12] that, when the average coordination is about 3.0, good quality interfaces are obtained. If it is more, then there is over coordination results, which increases the number of interface traps. If an oxide layer is grown prior to the nitridation, the properties of the interface improve as the coordination number reaches 3.0.

3.3 Oxynitrides

Dopant penetration through the gate dielectric causes change in threshold voltage [13]. The Si-O-N layer acts as a diffusion barrier to impurities [10]. One possible explanation is that the films are denser than SiO_2. Additionally, diffusivity of N_2O, NO, O_2 and N_2 is lower. However, the strong bond of N with the lattice may also be one of the reasons. The bonds are more constrained than that of SiO_2. Consequently, nitrided lattice resists the

diffusion of atoms and small molecules. A number of models have been proposed to explain diffusion resistance of oxynitrides. One particular model suggests that the N competes with boron for occupation of the defect sites [14]. Another model [15] explains that Si-N bond stops the substitution of Si atom with dopant atom. The silicon interstitial generated at the interface during oxynitridation are blocked from diffusing into the oxide [10]. This results in an enhanced flux of the interstitial into the silicon substrates. Chemical Vapor Deposition (CVD), Atomic Layer Deposition (ALD) and Metal Organic Chemical Vapor Deposition (MOCVD) are among the methods utilized for depositing oxynitrides.

CHAPTER 4

ALTERNATE GATE DIELECTRICS

4.1 Fundamentals of High Dielectric Constant Materials

As the feature sizes of complementary metal–oxide–semiconductor MOSFETs are scaled downward, the gate dielectric thickness must also decrease to maintain a value of capacitance, to reduce short channel effects and to keep device drive current at an acceptable level. The use of high-κ dielectric materials as gate oxides has been proposed since 70's [16]. They are extensively in use in Dynamic Random Access Memory (DRAM) circuits [3]. Thicker films can be employed, when high-κ materials are used as gate dielectrics. The high-κ dielectrics under consideration for CMOS applications are Ta_2O_5, $BaSrTiO_3$, TiO_2, La_2O_3, HfO_2, ZrO_2, Al_2O_3 and Y_2O_3. The aluminates and silicates are also of interest because they have higher crystallization temperatures than the pure oxides and show good interface properties.

Some gate dielectrics may form an interfacial layer during deposition even though they appear to be stable when in contact with silicon. Dielectrics such as HfO_2 and ZrO_2 are susceptible to oxygen diffusion, which can create interfacial layers during post-deposition annealing in oxygen atmosphere [3]. Such an interfacial layer may be a silicon oxide or silicate.

The incorporation of nitrogen into the silicon dioxide film reduces the defect generation rate. Defect generation rate is the density of defects produced per electron of a given energy that traverses the film, where the electron energy is determined by the applied potential or electric field [17]. Incorporation of a nitrogen-based interfacial layer

is found to be effective in suppressing the diffusion of oxygen and subsequent growth of silicon oxide. In some studies, it has been shown that a silicate interfacial layer can be beneficial in reducing interface trap density and improving reliability [18]. Figure 4.1 illustrates the importance of interfacial layer in controlling the shift of V_{FB} denoted as ΔV_{FB}.

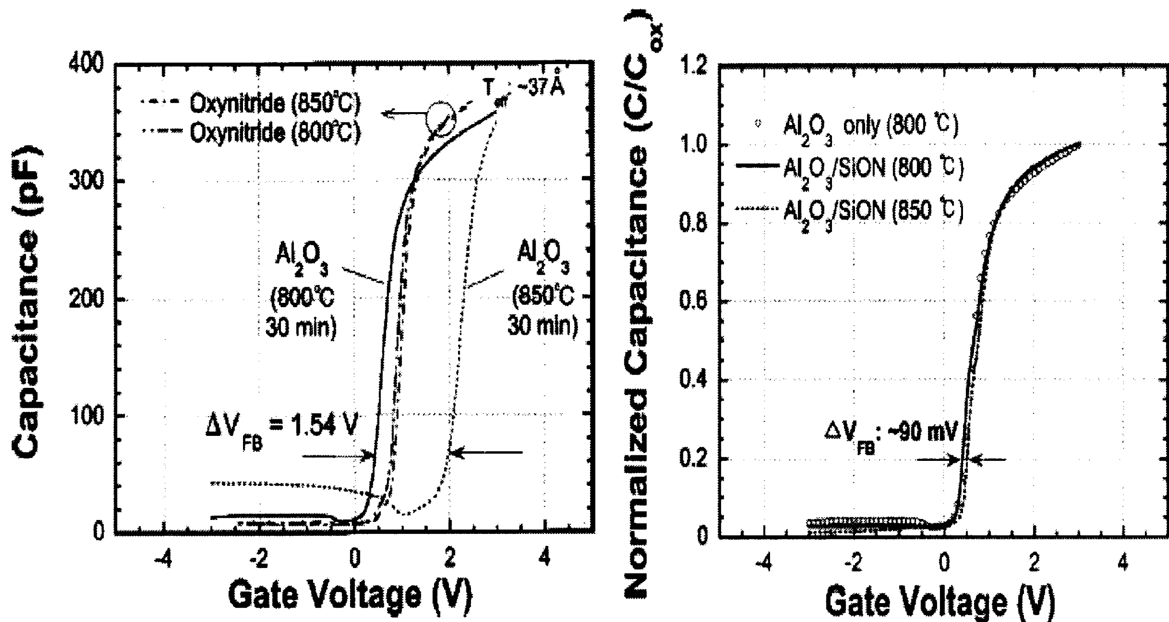


Figure 4.1 The effect of SiON underlayer in Poly-Si/Al_2O_3/SiON (~5Å)/In-Si MOS capacitor. The shift of the V_{FB} is reduced from 1.54 V to –90mV [13].

The rare earth oxides such as Lanthanides (i.e., La_2O_3, Y_2O_3, Gd_2O_3, etc.) are found to be hydroscopic which means that they react with water and create a low permittivity interface (hydroxide layer) with the underlying silicon [19]. The new high-k dielectric material must demonstrate thermodynamic stability on silicon with respect to formation of SiO_2 and silicides or silicates. The interface between Si and a high-κ dielectric is intrinsically heterovalent due to the large difference in average bond ionicity

between the two interfaces. There is a mismatch between the number of electrons available and the number required for covalent bonding leading to intrinsic charged atoms i.e., defects at the interface. Some high-κ dielectric films have a high amount of fixed charges. These charges modify the value of V_T [20]. The interface should show high breakdown strength and acceptable reliability. For metal oxides, breakdown strength is inversely related to permittivity. They should demonstrate low conduction for low power. Low leakage current implies large band-offsets for electrons and holes. The carrier mobility at the dielectric/Si interface should be high. Therefore, low D_{it} (e.g., $2E11/cm^2eV^{-1}$), low bulk charge or low effective fixed charge at the dielectric/Si interfaces are required. Figure 4.2 illustrates the conduction band offsets of the various high permittivity layers[21].

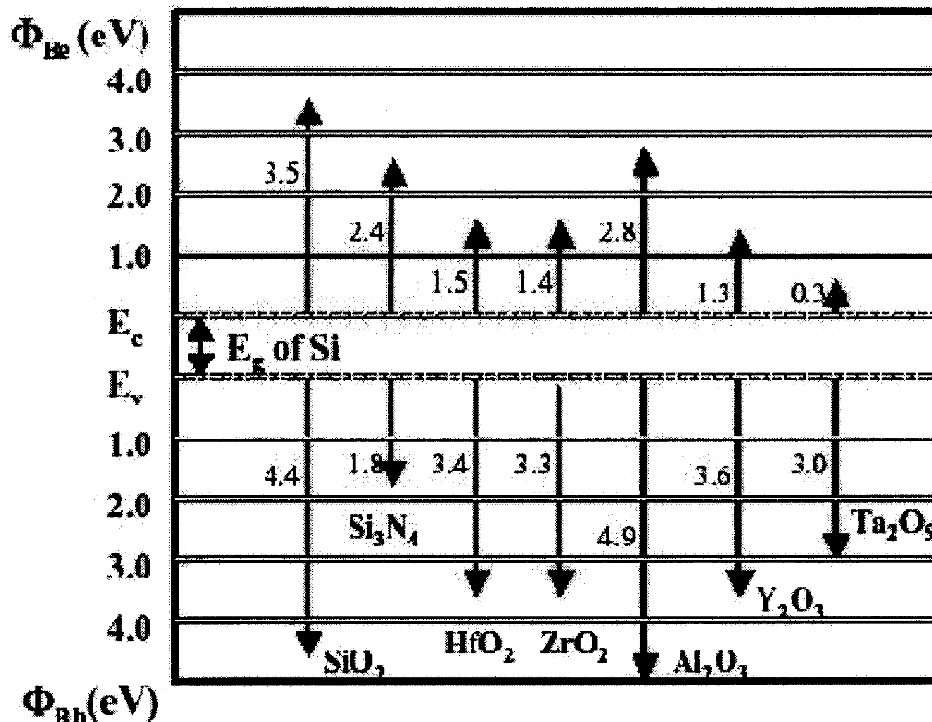


Figure 4.2 Conduction Band offset of SiO_2, Si_3N_4 and various high-κ materials with Silicon. Φ_{bh} and Φ_{be} are the hole and electron barrier heights respectively [21].

Researchers are now finding ways to replace the polysilicon as gate electrode [3]. This is because of its reactivity with high-κ materials e.g. ZrO_2. Polysilicon depletion effect is the other reason. The reduction of polysilicon activation temperature may cause incomplete activation of the dopants leading to voltage drops across the gate. This is called the polysilicon depletion effect. This occurs because more concentrated activated dopants will have high capacitance while a less dense diffused and inactivated dopant will result in low capacitance. A tunable work function of a Si-based electrode is also required. Therefore, by changing nitrogen concentration, it can be used in both pMOS and nMOS devices [3]. This changes the Fermi level. However, high-κ materials demand metal gate electrode. TiN and Pt are choice of metals that are currently being pursued. Metal electrode removes sheet resistance as well as dopant depletion effects.

Use of dual metal gate electrode requires extensive research, i.e., Al reacts with the gate dielectric. Platinum suffers from integration issues, i.e., it does not adhere and create good quality interface and it is costly, too [3]. Other disadvantage is that midgap materials require a threshold voltage of 0.5 V. However, due to scaling the applied voltage will be ~1.0 V. Thus, operation of the MOSFET might not be impossible at such a low voltage. Incorporating metal as gate electrode will require gate stack formation to be moved to the end of the process for reasons of thermal budget.

4.2 Alternative High-κ Gate Dielectrics

4.2.1 Introduction

High-k dielectric films are anticipated to be required by as early as 2005 for certain applications with low power and leakage current specifications [22]. Atomic coordination and bonding determine not just whether a solid can be amorphous or not, but also its electronic structure, because the electronic structure depends fundamentally on coordination, not on the presence of crystalline order.

Unlike SiO_2, most of the metal oxides have ionic bonding. Moreover, these high-κ metal oxides have localized metal-atom d states, which give rise to interface traps. The lowest conduction band offset energies of the high-κ oxides and alloys are determined by the d-state energies of the respective transition metal or rare earth atom. The d states generally give rise to states in the gap or near the conduction band, whereas oxygen 2p comprises the top of the valence band [23]. Following is the brief description of the some of the promising high-κ materials.

4.2.2 Deposition Techniques

Sputtering and electron beam evaporation are not advisable for depositing films of high permittivity materials because of potential radiation or ion-induced damage to the dielectrics. To deposit the thin high k layer, chemical vapor deposition (CVD) in one of its variations, such as metal-organic CVD (MOCVD), atomic layer deposition (ALD) or atomic layer CVD deposition (ALCVD), rapid-thermal CVD (RTCVD), plasma-enhanced CVD (PECVD), Jet Vapor Deposition (JVD) or remote plasma CVD (RPCVD) can be used. The CVD is a process by which a solid film can be formed on a substrate by

the reaction of vapor-phase chemicals that contain the required constituents [24]. Here, there is no consumption of substrate material. CVD thin films can be of high purity. However, a small contamination of carbon and hydrogen may be expected. They can be made of different compositions. Effective process control and good economy in operation can easily be achieved in CVD processes.

The energy for decomposition of the gases can be provided chemically, thermally or by plasma formation. The quality of the film is affected by substrate temperature, type of reactive species, their energy and rate of chemical supply [24]. CVD can be classified differently based upon the use of atmosphere, pressure and temperature.

In CVD systems, reactants are introduced into the reactor. The gas species are activated by mixing heat, plasma or by other means. This reactive species get adsorbed on the substrate surface. The adsorbed species undergo chemical reaction or react with other incoming species to form a solid film. The by-products of these reactions are desorbed from the substrate surface, which are then finally removed from the system [24]. CVD based techniques may find difficulty in yielding films with nucleation on a bare H-terminated silicon surface. Therefore, presence of interlayer of SiO_2 or nitrided SiO_2 is necessary, although, it means decreased permittivity.

Ultrahigh vacuum-physical vapor deposition (UHV-PVD) is attractive because it can be programmed easily for materials screening and studies, and provides very good chemical purity. However, it is still not commonly used for silicon device processing.

Plasma Enhanced Chemical Vapor Deposition (PECVD) uses energy in a plasma state to create more reactive radicals, allowing reactions to occur at lower temperatures. The film is dense. Lower amount of residue is found in the film because reactions occur

in the plasma region. However, if process control is not optimized, high impurity levels may occur. Plasma processing may damage devices under conditions of excessive ion bombardment. The film has high residual stress.

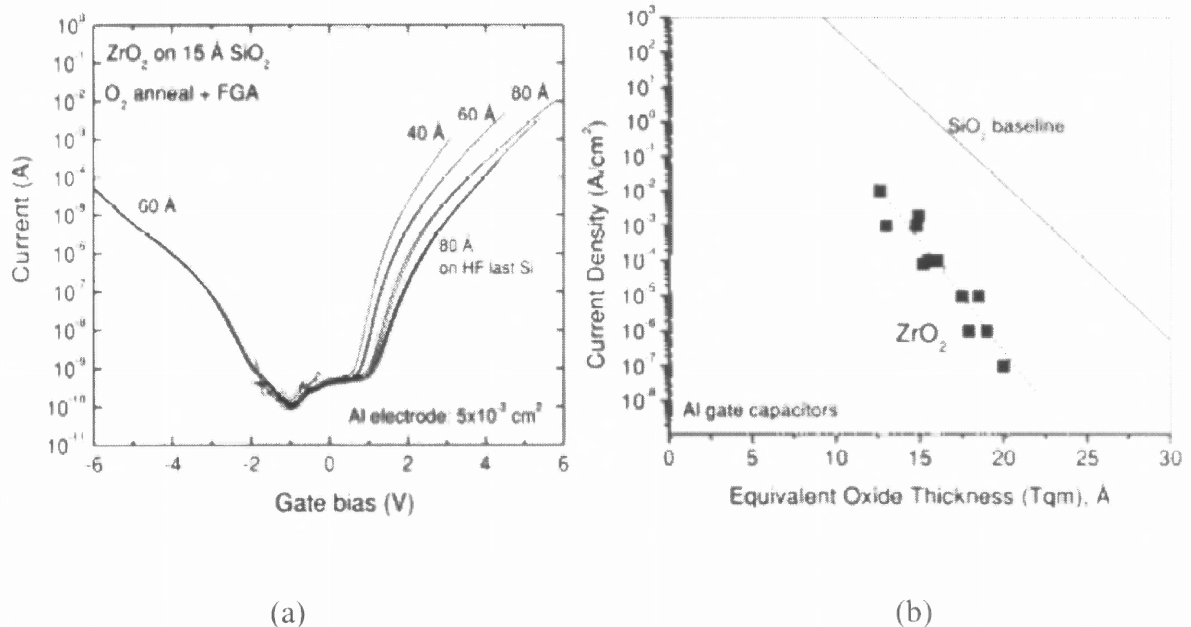
Low Pressure Chemical Vapor Deposition (LPCVD) is a high temperature process. It gives good step coverage and high quality films. However, deposition rates are low and can only be used before Al deposition due to high temperature of process (~900°C).

Molecular Beam Epitaxy (MBE) uses a substrate in high vacuum, while molecular or atomic beams of the constituents impinge upon its surface [2]. The components along with dopants are heated in separate chambers. Collimated beams of these components are directed on the surface of substrate. Good quality crystals can be grown by controlling the rate at which these beams impinge the substrate. Temperature of the substrate is lower than the components. By controlling the shutters, the doping level can be changed on lattice scale. MBE is comparatively costly because of the need for ultra-high vacuum and precise process control parameters.

Metal Organic Chemical Vapor Deposition (MOCVD) is also known as organo-metallic vapor phase epitaxy (OMVPE). It is widely used for deposition of epitaxial compound semiconductor films. MOCVD is distinguished by the chemical nature of the precursor gases. As the name implies, metal organic compound like Trimethylgallium (TMGa), Trimethyl-Indium (TMIn), etc. are employed. They are reacted with group V hydrides, and during pyrolysis the semiconductor compound is formed. This process can be used at moderately low temperatures. Deposition is efficient and reproducible. Carbon contamination may be one of its drawbacks [25].

4.2.3 Zirconium Oxide (ZrO_2)

ZrO_2 is considered to be one of the front-runners in the race for replacing SiO_2. It has dielectric constant of ~25. Its thermal stability is also considered to be very good up to 900°C. Barrier height and band offset with respect to silicon are also favorable. It has good interface quality with silicon. The electronic configuration of Zr is $5s^2 4d^2$ [21]. It donates its four valence electrons to two oxygens, to make Zr^{4+} and two O^{2-}, so that both ions have closed shells. The upper valence band consists of filled oxygen 2p sates and, higher up, empty 5s states [26]. The band gap of 5.8 eV is between the O 2p states and the Zr 4d states. It is given roughly by the difference of orbital energies in the free atom [27]. Figure 4.3 shows I-V measurements of the annealed ZrO_2/SiO_2 gate stacks on n-type and p-type wafers [6].



(a) (b)

Figure 4.3 (a) Current-Voltage measurements of annealed ZrO_2/SiO_2 gate stacks on n-type and p-type wafers, (b) Gate leakage current density of ZrO_2 gate stacks as a function of equivalent electrical thickness [6].

However, ZrO_2 suffers from some drawbacks also. When subjected to high temperature post deposition annealing, it crystallizes. This is a cause for concern, as it is believed that a crystallized phase may lead to heavy current leakage, although it has not yet been proved. This may occur because grain boundaries may serve as possible leakage paths [3,19]. It also causes problems of non-uniform dielectric properties.

Other studies [19] have shown that ZrO_2 is susceptible to diffusion of oxygen, which results in the formation of low dielectric interfacial film of SiO_2 or silicate layer. In other words, it decreases the dielectric constant. Also, it is observed that when deposited by Atomic Layer Chemical Vapor Deposition Technique (ALCVD), without an under layer of SiO_2, poor nucleation occurs. It is suggested [19] that during annealing, excess trapped oxygen in the ZrO_2 may be reacting with the silicon in the gate contact. This oxygen transport leads to interfacial SiO_2, which results in low overall dielectric constant of the gate dielectric.

Figure 4.4 shows High Resolution Transmission Electron Microscope (HRTEM) image of 20Å ZrO_2 on top of 15 Å SiO_2. Studies in the literature [3] have shown that using Zirconium silicate helps remove some of the above-mentioned problems. It has less interface charge, as it is believed to be closer to SiO_2.

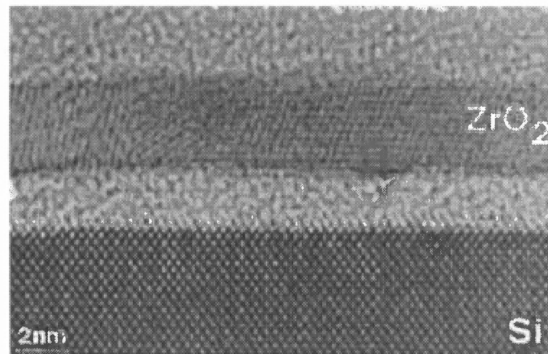


Figure 4.4 HRTEM image of ZrO_2 deposited on oxidized Silicon by ALCVD [3].

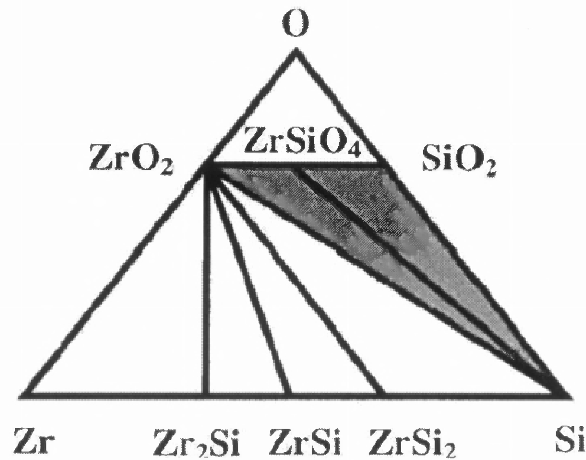


Figure 4.5 Zr-Si-O ternary system phase diagram [3].

In the present studies, it is speculated that ZrO_2 reacts with the polysilicon and forms Zirconium silicide, which causes current leakage in the device . Zirconium silicide is an electrical conductor which reduces overall dielectric thickness of the material. Figure 4.5 shows the Zr-Si-O ternary phase diagram [3]. It indicates that metal oxide ZrO_2 and the compound silicate will both be stable in direct contact with Si even at high temperatures [3].

4.2.4 Yttrium (Y_2O_3) and Gadolinium Oxides (Gd_2O_3)

The rare earth oxides of Yttrium and Gadolinium are thermodynamically stable and have moderate dielectric constants of ~18 and ~14 respectively [19]. Encouraging results [3] have been shown in cases, where Molecular Beam Epitaxy (MBE) deposited Gd_2O_3 films have been used. They are however; highly hygroscopic in nature meaning they react readily with water creating hydroxide layers. Moreover both are under constrained and may form very high defect densities. Trivalent compounds like Yttrium and Gadolinium generally form complex interfaces (i.e., hydroxides) [19].

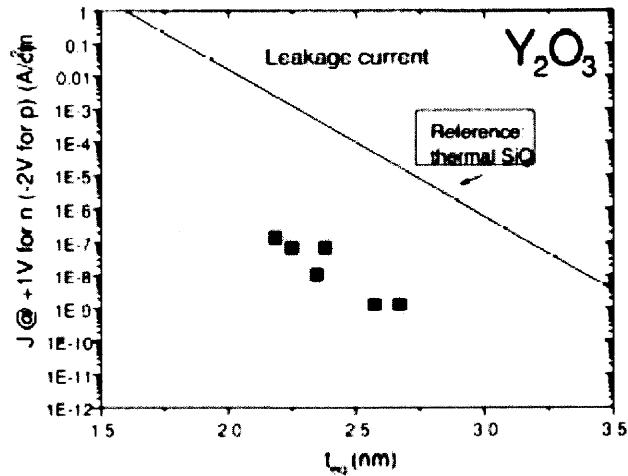


Figure 4.6 Electrical leakage current densities of Y_2O_3 films (thickness given in terms of equivalent SiO_2 thickness) and SiO_2 films [6].

Y_2O_3 has the cubic bixbyite (Mn_2O_3 defect spinel) structure, in which Y is sevenfold coordinated [21]. Y_2O_3 has a large conduction band offset, but it is a fast ionic conductor. Thus, the oxygen ion diffusivity is high. Figure 4.6 shows low leakage of ALD deposited Y_2O_3 compared to thermal SiO_2.

4.2.5 Titanium Oxide (TiO_2) and Tantalum Oxide (Ta_2O_5)

Titanium Oxide (TiO_2) and Tantalum Oxide (Ta_2O_5) have high dielectric constants but they are not thermally stable with silicon. They crystallize above 400-650°C [3,28]. They will react with silicon and create SiO_2. This layer will decrease the overall capacitance of the stack. Figure 4.7 shows ternary diagrams of Ta-Si-O and Ti-Si-O ternary systems at temperatures in the range of 700-900°C. It shows that Ta_2O_5 and TiO_2 are not stable when deposited on Si. Figure 4.7 shows that they will tend to separate into phases of SiO_2 and metal oxide (M_xO_y, M= metal) [3].

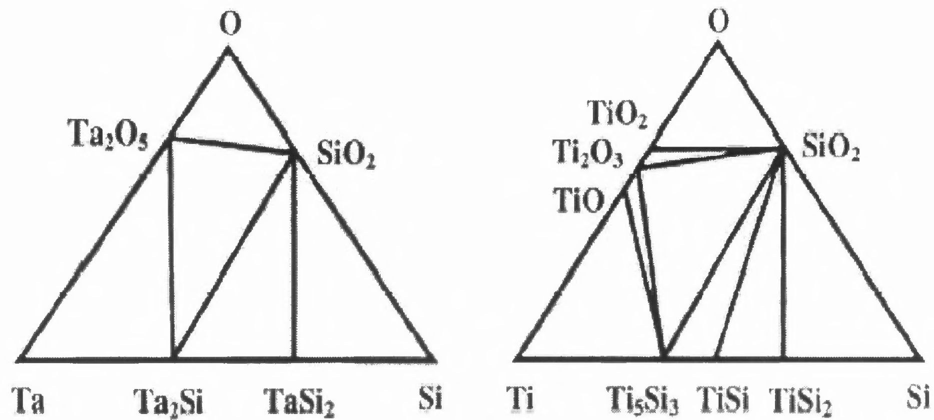


Figure 4.7 Gibbs free energy diagrams for Ta-Si-O and Ti-Si-O ternary systems [3].

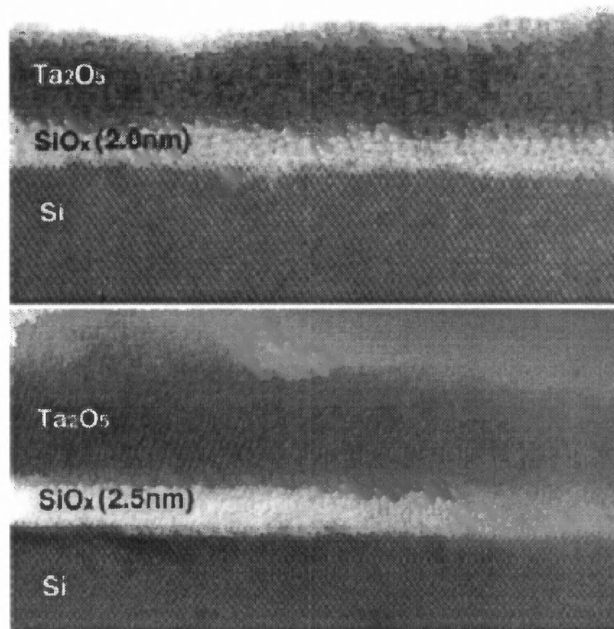


Figure 4.8 HRTEM micrographs of tantalum oxide and interface with Si. (a) After low-temperature plasma anneal, and (b) RTA at 800°C [29].

Figure 4.8 shows crystalline regions and growth of the interfacial region (2 nm.) after thermal annealing of Ta_2O_5 gate stack [29]. Figure 4.9 (a) shows the comparison between Ta_2O_5 and thermal oxide samples. The current leakage of Ta_2O_5 devices is 10^3x lower than that of thermal oxide at V_g= -1.0 V. Figure 4.9 (b) shows improved leakage

with the use of NO passivation layer [30]. If underlayer is not used, interfacial SiO_x is formed during deposition and post-deposition thermal treatments. At high temperature RTA, the interfacial oxide resembles SiO_2. Thus, a low temperature annealing is preferred.

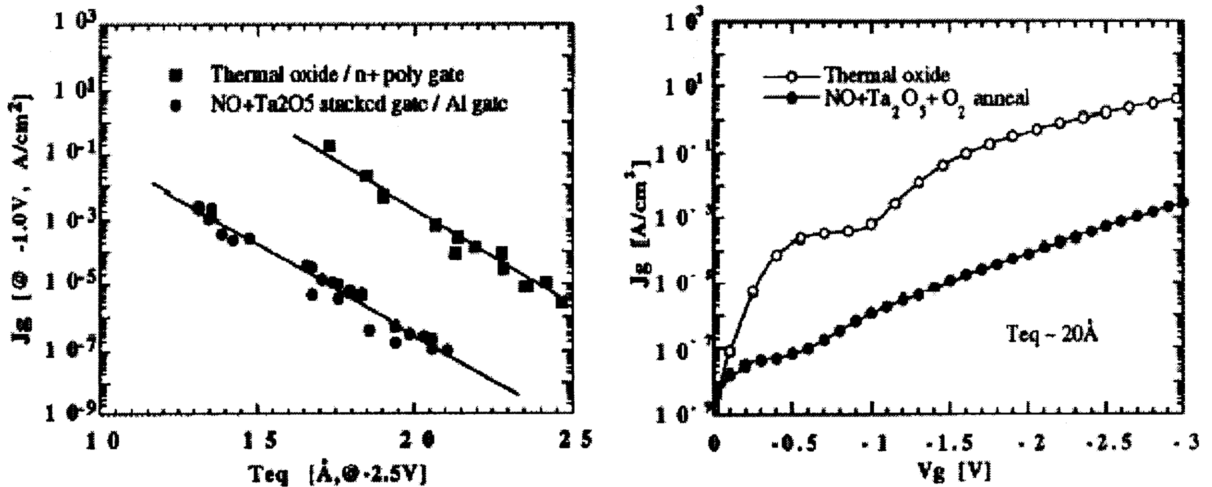


Figure 4.9 (a) leakage current density comparison of different layers, and (b) J_g-V_g characteristics of different dielectric films [30].

Ta_2O_5 can be deposited by thermal oxidation, rf magnetron sputtering, UV-photo CVD, LPCVD, PECVD techniques. The conduction mechanism is Schottky emission at low electric field and Frenkel-Poole emission at high electrical field [28]. The underlayer can be oxide or nitrided oxide (NO) layer. This not only improves the interface between the Ta_2O_5 and Si but also prevents further oxidation of Si due to the deposition process of Ta_2O_5. NO layer is stable compared to SiO_2 layer. Figure 4.10 shows the I-V characteristics of Ta_2O_5/SiO_2 gate insulator in nMOSFET with T_{eq} of 2.8 nm and L_g of 0.35μm [31].

Deposition of TiO_2 without an underlayer by CVD is extremely difficult but it can be deposited by Jet Vapor Deposition (JVD) process. Its high permittivity (~80-100) is due to a major contribution from soft phonons involving Ti ions. Ti has several stable oxidation states of Ti^{3+} and Ti^{4+}. This gives rise to reduced oxide. Reduced oxide has large number of oxygen vacancies, which act as carrier traps and high leakage paths [3].

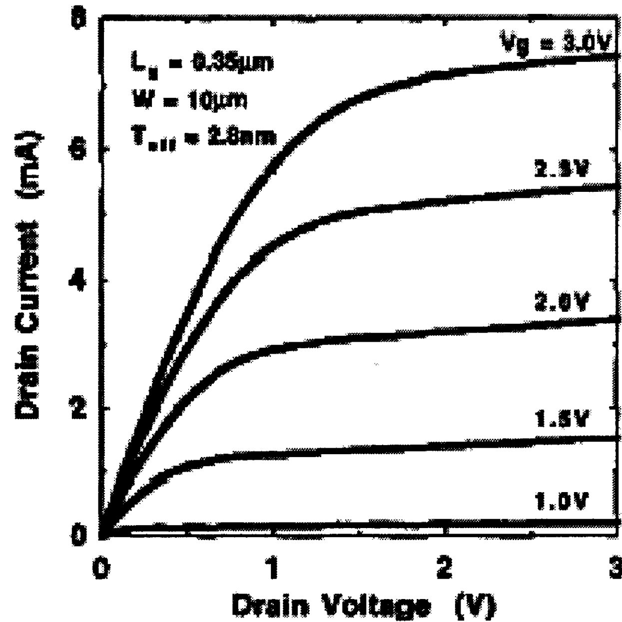


Figure 4.10 I_d-V_d characteristics of Ta_2O_5/SiO_2 nMOSFET [31].

4.3 Aluminum Oxide (Al_2O_3)

Alumina (Al_2O_3) is a group III-VI substance with useful properties for a gate dielectric. It has a large band gap, it is amorphous under conditions of interest and is thermodynamically stable with SiO_2. In Al_2O_3, the electronic structure of the metal atom is Al $3s^2 3p^1$ [21]. It donates its electrons to the oxygen to form Al^{3+} and O^{2-}. The upper valence states are filled O $2p$ states, while the conduction-minimum is the Al $3s$ state. The band gap is between the O $2p$ and the Al s states. Al forms more polar bonds to six

oxygen atoms in crystalline α-Al_2O_3 (sapphire) and four to six oxygen atoms in its amorphous phase. The Al-O bond is 60-70% ionic. It is not a good glass former like SiO_2. Al_2O_3 is believed to have a large amount of fixed charge. This may result in a substantial shift in the threshold voltage. ALCVD, MBE or MOCVD can be used to deposit Al_2O_3. Figure 4.11 is a HRTEM image of an Al_2O_3 gate stack [6].

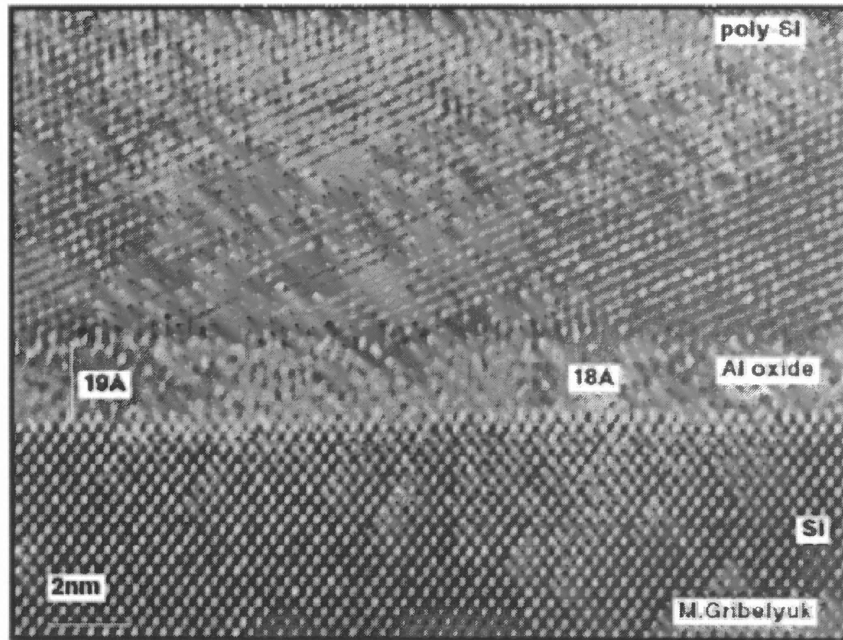


Figure 4.11 HRTEM image of deposited and processed ALCVD layers of poly-Si/ Al_2O_3/Si [6].

4.4 Hafnium Oxide (HfO_2)

HfO_2 appears promising due to its high dielectric constant (~25) as compared to SiO_2 and Al_2O_3. It has relatively high free energy of reaction with Si (47.6kcal/mole at 727ºC) as compared to TiO_2 and Ta_2O_5. HfO_2 becomes crystallized above 950ºC. It mainly

crystallizes in monoclinic phase and some tetragonal phases. At about 1000°C, HfO_2 has been found to interact with polysilicon [22].

The degradation of the mobility of the electrons up to 15% has been observed vis a vis SiO_2. Poor nucleation of HfO_2 is observed on H-terminated surface [6]. This may be due to the absence of dangling bonds. HfO_2 is extremely susceptible to O diffusion and reaction at the channel interface. Therefore, high interface trap levels may be the other reason for the decrease in mobility. Many researchers [32] have reported promising results when the HfO_2 is sputter deposited. However, as the channel length decreases and device dimensions shrink, sputtering is not advantageous. So the Chemical Vapor Deposition techniques are the preferred methods for depositing the oxide. ALCVD™ is foremost amongst them. Figure 4.12 is the HRTEM image of Poly-Si/HfO_2/SiO_2/Si [33].

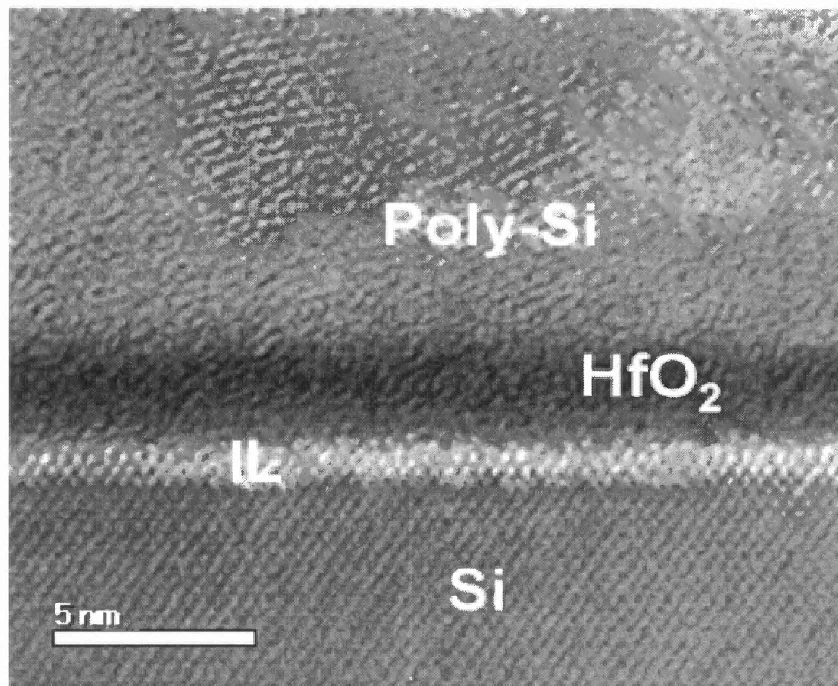


Figure 4.12 HRTEM image of Poly-Si/HfO_2/SiO_2/Si, where "IL" denotes the SiO_2 interfacial layer[33].

4.6 Rapid Thermal Annealing (RTA)

RTA has been used in the present study for post deposition annealing. RTA is used for spike activating implanted dopant particles in source and drain. It is also used to activate in-situ doped polysilicon. This is required since as-doped polysilicon is usually not activated and has high sheet resistance. Effect of spike annealing on high-κ materials has also been studied. Spike annealing is rapid thermal annealing at a short cycle time [36].

RTA is also used for single wafer forming gas annealing in this study. The Rapid thermal annealing is intended to diffuse dopant from the implanted region near the surface to the gate oxide interface, creating in the ideal case a high active carrier concentration in the polysilicon at the interface with negligible diffusion of dopant through the oxide to silicon channel [36].

In other words, RTA is a widely used technique: (a) to create high carrier concentration at the polysilicon /gate dielectric interface, (b) to minimize the depletion depth in the polysilicon, (c) to have negligible penetration of the dopant to the crystalline silicon channel and to maintain gate dielectric reliability with minimal threshold voltage variation [35].

In-situ doped polysilicon was selected over ion-implantation because of the uniformity of the dopant density throughout the layer. In-situ doped polysilicon is heavily doped (5E21). This is to ensure reasonable conductance of the polysilicon gate. In-situ doped polysilicon is electrically inactive as deposited. Consequently, spike annealing has been used to activate the layer.

Electrical activation of the source and drain regions at high temperature proceeds by dissociation of the clusters and diffusion of the dopant that increases junction depth. Heavy dose of the dopant by ion implantation causes damage and strain in the silicon lattice. RTA reduces this strain and anneals out defects. Rapid thermal annealing creates electrically active dopants and reduces the sheet resistance. It reduces defect densities formed by impurities in junctions. Deposition of high-κ layer results in a highly stressed film. RTA has some disadvantages. Ion implantation dose and screen oxide thickness variation can occur. It can create metrology problems as well as ambient gas combination variations [24].

Various methods are used to perform RTA. The furnace bell jar method is largely heated on one side, although there is underside heating as the wafer is raised. Other techniques with single side wafer heating may use an array of incandescent lamps (Applied Materials), an arc lamp or a hot plate (Mattson). Incandescent lamp systems with dual sided heating surround the wafer with maximum lamp exposure to achieve high heating rates. There are tradeoffs in heating and cooling rates, time at maximum temperature, and process uniformity among the methods [34]. Figure 4.8 shows a Metron RTA machine. A similar type of machine has been used in the present study. Generally, multiple lamp methods require more complex multiple-zone power control and wafer rotation to achieve reasonable heating uniformity, compared to systems with a high power lamp or stationary heat source [34].

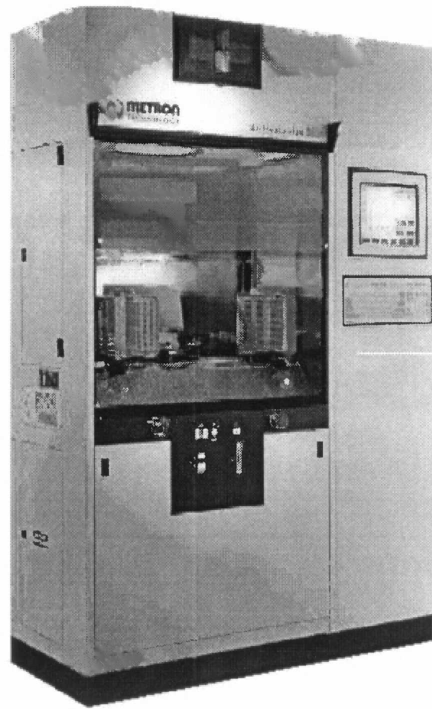


Figure 4.13 Metron AG HEATPULSE 8800 RTA machine [37].

CHAPTER 5

ELECTRICAL CHARACTERIZATION

5.1 Capacitance Voltage (C-V) Measurements

Two types of capacitances can be defined for the MOS capacitor. The static capacitance is defined as $C_{stat} = (Q_T/V_G)$, where Q_T is the total charge density on the capacitor and V_G is the bias applied to it. The differential capacitance is defined as $C = (dQ_T/dV_G)$. The differential capacitance is most important, because small signal measurements determine the rate of change of charge with voltage [3].

The C-V measurements can be used to measure a) barrier height, b) deep impurity levels, c) interface traps, d) oxide thickness, e) silicon bend bending, and f) fixed charges. Carrier concentrations in polysilicon and crystalline Si are determined from band bending. The method is convenient, unambiguous, can be nondestructive and effective even for intrinsic samples. The shape of the C-V curve depends upon the type of substrate doping.

To measure capacitance as a function of gate bias in the steady state, a small alternating component of voltage is superimposed on the gate bias. The small signal range is the range of applied signal amplitude producing a linear response of ac current to ac voltage. Interface traps and interfacial charge non-uniformities influence the small signal range because they alter the variation of admittance of the MOS capacitor varies with gate bias [38]. Figure 5.1 shows the cross section of a MOS capacitor with a simple equivalent circuit.

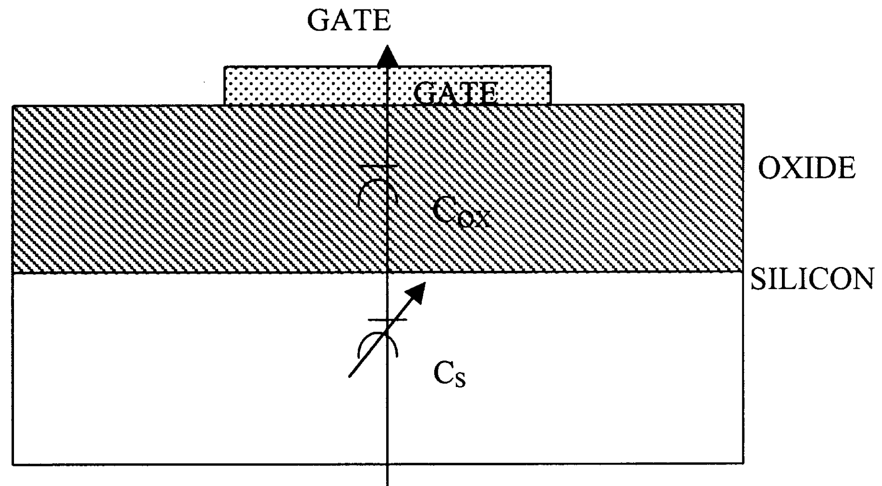


Figure 5.1 Cross-section of an MOS capacitor showing a simple equivalent circuit [38].

5.1.1 Low Frequency C-V Measurements

Minority carriers in silicon respond to low frequencies [38]. This behavior is observed because their response time is too slow at high frequency, where the cycle is very fast. Following is a discussion of the measurement of low frequency capacitance in a p-type MOS capacitor.

An application of bias across the MOS capacitor establishes the electric field in the oxide layer. For all values of gate bias below the oxide breakdown, no dc current flows when gate bias is applied. Consequently, the Fermi level is always flat as shown in Figure 5.2. When the voltage is increased more towards the negative side, the number of holes increases. At some point the number of holes is more than they are in the bulk. This increase in the number of holes contributes to a large differential capacitance. Thus, the capacitance of semiconductor exceeds that of oxide. When the gate bias is made less negative, there is a net decrease in the number of holes near the surface. Thus, the semiconductor capacitance decreases and the oxide capacitance dominates.

As the gate bias is completely removed, the flatband point is reached as shown in Figure 5.2. When the positive bias is applied to the gate, the holes move away from the silicon surface, thereby, creating a depletion region as seen in Figure 5.2. Bands move downwards. These causes a decrease in $c_{S,}$ therefore, overall capacitance decreases. Low frequency capacitance can be measured by the following equation [38]:

$$C_S = -Sin(u_B - u_S)\left(\frac{\varepsilon_S}{\lambda_i}\right)\frac{Sinhu_S - Sinhu_B}{F(u_S,u_B)} , \qquad (5.1)$$

where $_i$ = intrinsic Debye length, $_s$ = semiconductor dielectric constant, C_s= semiconductor capacitance, u_s and u_b are surface and bulk potential.

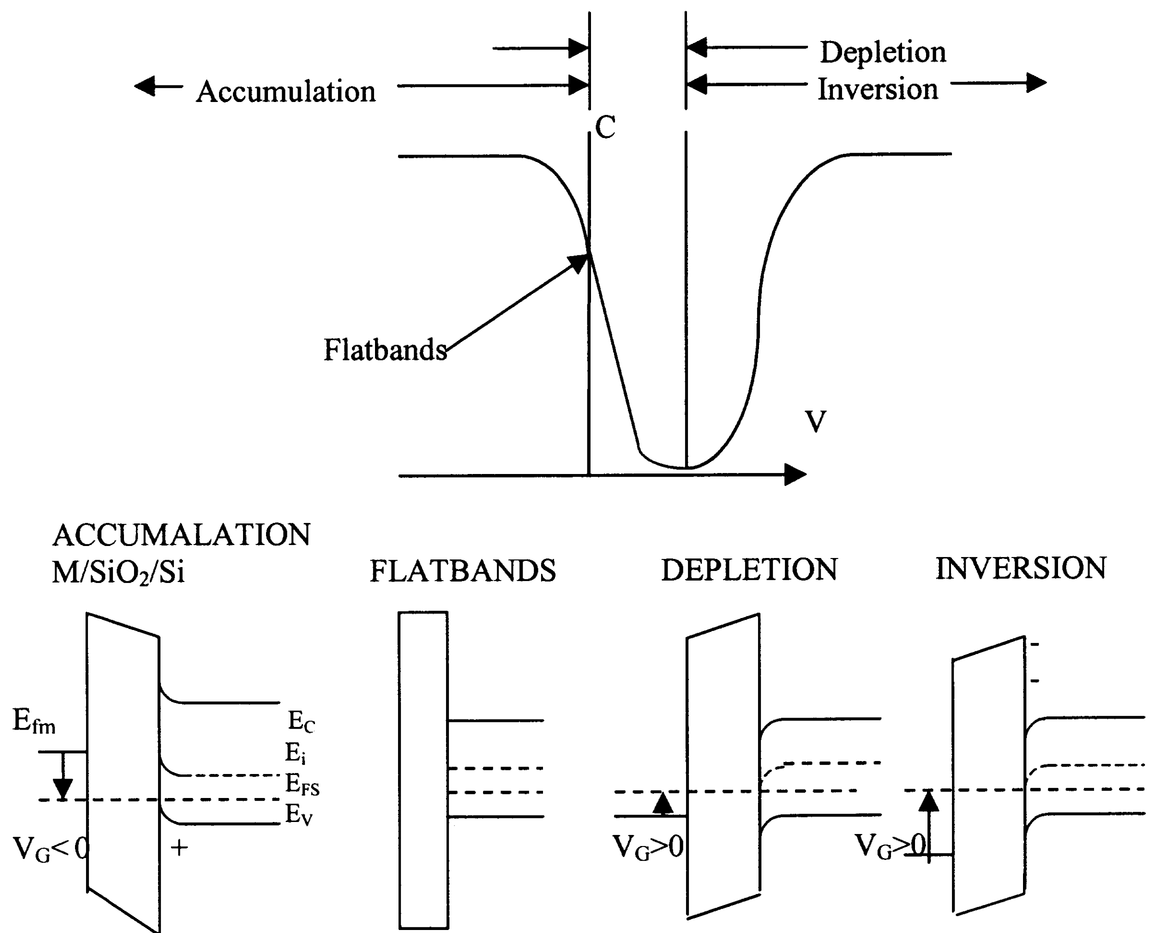


Figure 5.2 Capacitance as a function of bias and corresponding band diagrams for p-type MOS capacitor [3].

The intrinsic Debye length [38] is defined as $\lambda_i = (\varepsilon_s kT/2q^2 n_I)^2$ cm. The value of λ_i, at T= 290°K, is 2.84x10^{-3} cm using $n_i = 10^{10}$ cm^{-3}. As the positive gate bias is increased, the Fermi level crosses midgap and the electron and hole densities become equal. When more positive gate voltage is applied, the surface electron density increases compared to holes. This layer is called inversion layer. This inversion layer is also known as the channel.

5.1.2 High frequency C-V measurements

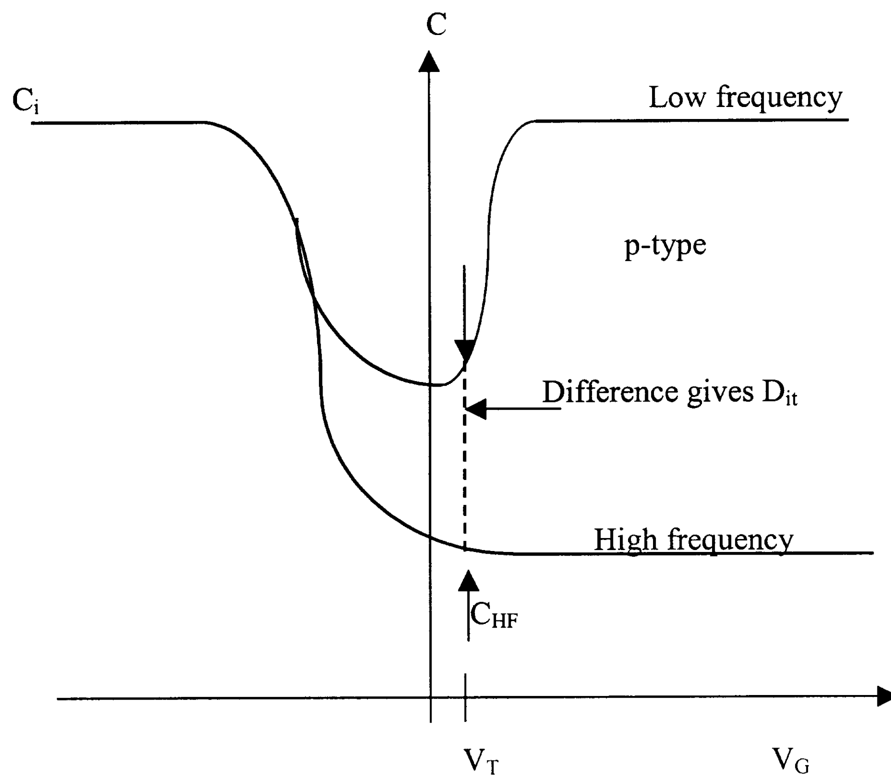


Figure 5.3 C-V measurements at various frequencies [2].

Figure 5.3 shows C-V curves at high and low frequencies. Here, C_{HF} is the high frequency capacitance, C_i is insulator capacitance and D_{it} is interface trap density. The capacitance C_i is inversely proportional to the thickness of the dielectric layer.

On comparing Figures 5.2 and 5.3 in the accumulation and depletion regions for $D_{it}= 0$, the high and low frequency capacitance are the same. However, they differ in the inversion region.

The steady state characteristics of a C-V curve are governed by the minority carrier response in the inversion region. In the accumulation and depletion region, the number of minority carriers is much less compared to the majority carriers. In the inversion layer, the number of minority carriers do not change and their contribution to the capacitance is negligible. The majority carriers maintain the charge balance as they can follow the high frequency. They move in and out of the depletion region, thus, causing it to expand. Table 5.1 gives the quantities determined by high frequency MOS C-V data analysis. Principally, these are oxide thickness, T_{ox}, Si doping, N_d, fixed charge density in the oxide Q_{ss}.

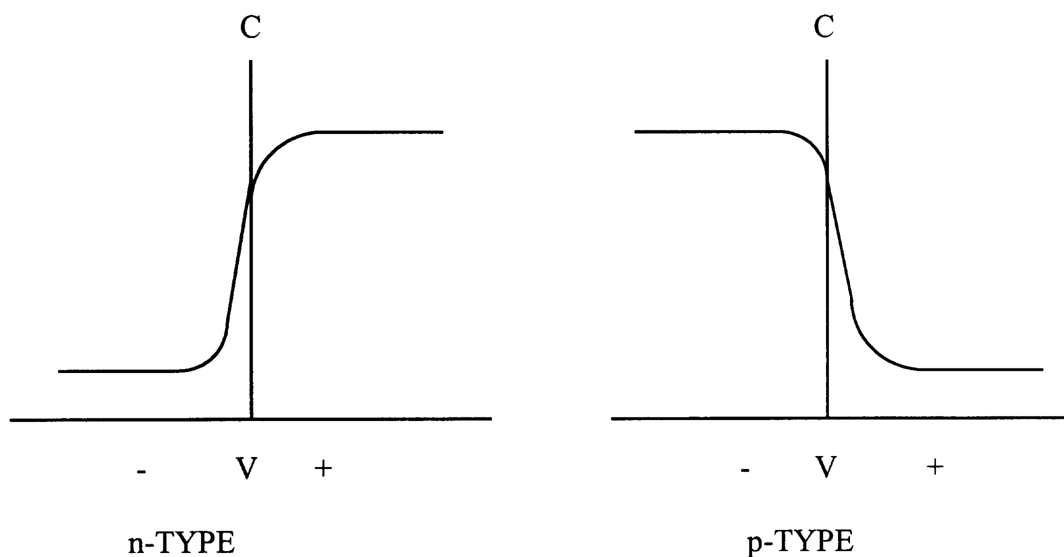


Figure 5.4 High frequency curves for two types of substrate dopings.

Table 5.1 Quantities Determined by High Frequency MOS C-V Data Analysis

FROM	USING	WE DETERMINE
• Measured Oxide Max Capacitance, C_{ox} ε_{ox} = 3.4 E-13 fd/cm • Area of Capacitor	$t_{ox} = (\varepsilon_{ox} A)/C_{ox}$	Oxide Thickness, t_{ox}
• High Frequency Min MOS Capacitance, C_{hfmin} • C_{ox}	$C_{hfmin} = (C_{ox} \times C_{min})/(C_{ox} - C_{min})$ $N_D = f(C_{hfmin})$	Doping Density of Silicon Substrate Surface Region, N_D
• N_D, C_{ox}	$C_{fbs} = \sqrt{(\varepsilon_s q^2 N_D/kT)}$ $C_{fb} = C_{fbs} C_{ox}/(C_{ox} + C_{fbs})$	Flat Band Capacitance, C_{fb}
• C_{fb}	The measured MOS C-V Curve	Flat Band Voltage, V_{fb}
• V_{fb} • C_{ox} • Φ_{ms} • N_D • ε_s	$Q_{ss} = C_{ox}(V_{fb} - \Phi_{ms})/q$ $W_{max} = \sqrt{(4 \varepsilon_s kT \ln(N_D/n_i) q^2 N_D)}$	Oxide-Silicon Interface Fixed Charge Density $Q_{ss}(N_{fb})$ Depletion Width. W_{max}

5.1.3. Analysis of the Capacitor Measurements

In this section, various useful definitions and equations for measuring electrical characteristics of the MOS capacitor [39] are presented:

A : calculated area in sq.cm.

V_{fb}: flatband voltage.

V_t: threshold voltage.

N_{fixed}: fixed oxide surface charges (ions/cm^2).

N_b: background concentration (acceptors or donors/cm^2).

N_d: No of dopant atoms.

χ : electron affinity.

Area: The area, A, enters into the expression for C_{max},

$$C_{max} = C_{ox} = \frac{\varepsilon_{ox}\,Area}{t_{ox}} \tag{5.2}$$

Semiconductor doping

The doping is assumed to be uniform. It is calculated from the measured C_{min} in inversion and C_{max}, the oxide capacitance in accumulation. The high frequency semiconductor capacitance C_{hfmin}, is given by:

$$\frac{1}{C_{hf\,min}} = \frac{1}{C_{min}} - \frac{1}{C_{max}} \tag{5.3}$$

From the strong inversion capacitance at high frequency, the doping concentration N_A is calculated by the equation,

$$\frac{N_A}{\ln(N_A/n_i)+\frac{1}{2}\ln(2\ln(N_A/n_i)-1)}=\frac{4kT{\varepsilon_{ox}}^2}{q^2\varepsilon_s {t_{ox}}^2}\left[\frac{C_{ox}}{C_{hf\min}}-1\right]^{-2} \quad (5.4)$$

Flatband Capacitance

The flatband voltage is the voltage at which the flatband capacitance occurs on the observed forward (depletion) C-V curve. The flatband capacitance of the semiconductor C_{fbs} is given by:

$$C_{fb}=A\sqrt{\varepsilon_s q^2 N_A/kT} \quad (5.5)$$

The measured capacitance at flatband, C_{fb}, has the oxide capacitance, C_{max} in series with $C_{fbs,}$. Therefore,

$$C_{fb}=\frac{1}{\frac{1}{C_{fbs}}+\frac{1}{C_{\max}}} \quad (5.6)$$

Flatband Voltage

The flatband voltage is the voltage at which the observed capacitance is equal to the theoretical flatband capacitance. This voltage is independent of area, the area being only a scaling factor for both the oxide and semiconductor capacitance. On the other hand, the observed capacitance at flatband voltage is dependent on the oxide thickness, its dielectric constant, semiconductor doping and dielectric constant.

Shifts in Flatband Voltage

The flatband voltage shifts may have one or more causes.

1) Mobile ions in the insulator, particularly sodium in silicon dioxide.
2) Ions, electrons, or holes in the insulator, possibly injected by application of excess voltage.
3) Mobile impurities other than sodium.

Threshold Voltage

The onset of inversion and the flow of current in an MOS transistor occur at the gate threshold or turn-on voltage,

$$V_t = V_{fb} + 2\Phi_B + \frac{t_{ox}}{\varepsilon_s}\sqrt{2\varepsilon_s q N_A * 2\Phi_B} \tag{5.7}$$

where, the barrier height is,

$$\Phi_B = \frac{kT}{q} * \ln\frac{N_A}{n_i} \tag{5.8}$$

Maximum Depletion Width

The maximum depletion width is given by:

$$W_{max} = \sqrt{\frac{2\varepsilon_s \Phi_m}{q N_A}} \tag{5.9}$$

where, the metal work function Φ_m is,

$$\Phi_m = 2\Phi_B + \frac{kT}{q} \ln \frac{2q\Phi_B}{kT} \tag{5.10}$$

Fixed Oxide Charges

The initial charge concentration affecting the flatband voltage is calculated by correcting the initial measured flatband voltage V_{fb} for the work-function difference,

$$N_f = \frac{\varepsilon_{ox}}{q t_{ox}} * \Phi_{ms} - V_{fb} \tag{5.11}$$

where, the metal-semiconductor workfunction Φ_{ms} is,

$$\Phi_{ms} = \Phi_m - (\chi + \Delta E - \Phi_B) \tag{5.12}$$

Deep depletion

The capacitance in deep depletion is given by the equation

$$C_{s,DD} = \frac{Cox}{\left[\sqrt{1 + 2(V_G - V_{FB})/V_0} - 1\right]} \tag{5.13}$$

where, V_G is the gate voltage and $V_0 = (qK_s\varepsilon_0 N_A)/C^2_{ox}$. When the dc bias voltage is changed rapidly with insufficient time for inversion charge generation, it results in deep depletion curve. This approach is used in this study to determine V_{FB}. It is described fully in section 6.2.

5.2 Current Transport in Thin Oxides

Thin film insulators at high temperature or electric field show carrier conduction. The electric field in an insulator can be found from following equation:

$$E_i = E_s \left(\frac{\varepsilon_s}{\varepsilon_i}\right) \quad (5.14)$$

where, ε_i and ε_s are the dielectric constants of the insulator and semiconductor respectively, and E_i and E_s are the electric fields across the insulator and the semiconductor, respectively. For the Si-SiO_2 system the breakdown field is about 3 x 10^5 V/cm. The field in the oxide is 10^6 V/cm [1]. The mobile sodium ions can move through the oxide and create instability and hysteresis effect. For ultrathin SiO_2 films, tunneling will occur [1]. The following is a description of several current transport mechanisms.

In Schottky emission, thermionic emission across the metal-oxide or the oxide-semiconductor interface is responsible for carrier transport. This is given by following equation [1]:

$$J=A^* T^2 \exp\left[\frac{-q(\Phi_B - \sqrt{qE/4\pi\varepsilon_i}}{kT}\right] \quad (5.15)$$

where Φ_B is the barrier height and E is the electric field. Insulator permittivity is expressed by ε_i and A^* is the effective Richardson constant.

The Frenkel-Poole emission, shown in Figure 5.5, is due to field–enhanced thermal excitation of trapped electrons into the conduction band. It occurs at high temperatures and high fields. Frenkel-Poole emission is given by [1]:

$$J \sim E \exp\left[\frac{-q(\Phi_B - \sqrt{qE/4\pi\varepsilon_i}}{kT}\right] \qquad (5.16)$$

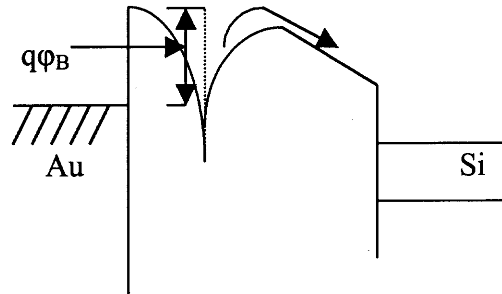


Figure 5.5 Frenkel-Poole emission [1].

Tunnel emission is due to the field ionization of electrons that are trapped in the conduction band or by tunneling of electrons from the metal Fermi energy to the insulator conduction band. The tunnel emission is not dependent on temperature. It is dependent on the applied voltage. It is given [1] by following equation,

$$J \sim E^2 \exp\left[-\frac{4\sqrt{2m^*}(q\Phi_B)^{3/2}}{3q\hbar E}\right], \qquad (5.17)$$

where, $\hbar$ is the Plank constant and m^* is the effective mass. Space charge limited current arises when a carrier travels inside the insulator and there is no compensating charge present. At high temperature and low voltage, current is carried by thermally excited electrons hopping from one isolated state to the next. The current density, (J), is proportional to the square of the applied voltage [1]. This is given in the following equation,

$$J = \frac{8\varepsilon_i \mu V^2}{9d^3} \tag{5.18}$$

where, d is the insulator thickness.

Ionic conduction is similar to a diffusion process. The ions cannot be readily injected into or extracted from the insulator. Therefore, the dc ionic conductivity decreases when the electric field is applied. The positive and negative space charges develop after some time has passed. These charges are at the gate-insulator and semiconductor-insulator interfaces. This situation creates imbalance in potential distribution. After the removal of applied field, large internal fields remain which causes a hysteresis effect [1]. This can further be explained by,

$$J \sim E \exp(-\Delta E_{ac} / kT) \tag{5.19}$$

and

$$J \sim \frac{E}{T} \exp(-\Delta E_{ac} / kT) \tag{5.20}$$

where, ΔE_{ac} is the electron field.

At different voltages and temperatures, various conduction process may dominate for a given insulator. For relatively thick film (t_{ox}>50Å) the characteristics of current density versus field are independent of the film thickness, area, electrode material and polarity of the applied bias at a given field and temperature [1].

For thin oxides, the tunneling mechanism depends on the thickness as well as the voltage drop across the oxide. Electrons quantum mechanically tunnel through a sufficiently thin

barrier even though the voltage is less than 3.0 V. The tunneling current increases exponentially with decreasing oxide thickness. The two prevalent conduction mechanisms are the Fowler-Nordheim and direct tunneling. When tunneling occurs at ~4.3 V, it is called Fowler-Nordheim (F-N) tunneling [40]. Refer to Table 5.2 where, KE_{ox} is the average kinetic energy of electron in oxide, V_{ox} is the oxide voltage [41].

Table 5.2 Tunneling Energies in Ultrathin Oxides [41]

Tunneling	qV_{ox}	$<KE_{ox}>$
	[eV]	[eV]
Direct	<3	0
Ballistic FN	3-9	0-6
Steady-State	>9	>6

Here the electrons tunnel from the cathode conduction band to the oxide conduction band through triangular barrier. F-N tunneling can be described by the following equation:

$$I_{FN} \, \alpha \, E^2 \exp\left(\frac{-B}{E_{ox}}\right) \tag{5.21}$$

where, B is related to the electron effective mass in the oxide conduction band and the Si/SiO_2 barrier height. When the gate oxide is made sufficiently thin, the electrons in the conduction band of Si can tunnel through a trapezoidal barrier directly through the gate oxide and emerge in the gate. This is called direct tunneling [2]. It occurs at low temperatures and high fields and when V< 3.0 V [40]. Figure 5.6 shows F-N tunneling as well as direct tunneling.

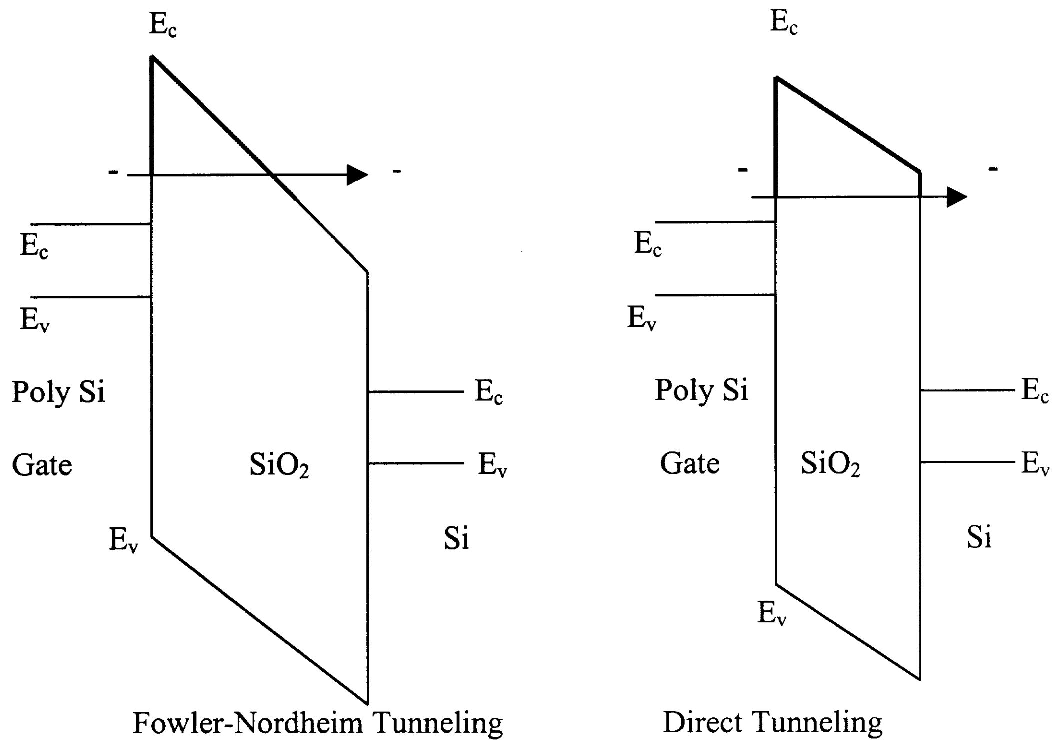


Figure 5.6 Leakage current mechanisms in thin oxides [2].

5.3 Time Dependent Dielectric Breakdown (TDDB)

When an electron current is passed through the gate dielectric (SiO_2) of a MOS capacitor or transistor, defects such as electron traps, interface states, positively charged donor like states, etc., gradually build up in the oxide until a point where the oxide suddenly and destructively breaks down. The exponentially increasing tunnel current with decreasing oxide thickness will cause the time to breakdown to decrease if the gate voltage is not simultaneously reduced sufficiently [42].

When charge conduction through the oxide continues for a long time, it can cause catastrophic breakdown of the oxides. This is known as Time Dependent Dielectric Breakdown (TDDB). Here, electrons tunnel from the conduction band of the gate and, under the influence of the electric field, become hot electrons in the oxide. They cause

impact ionization within the oxide and create electron hole pairs [2]. The holes move towards the gate oxide interface, while electrons drift towards the oxide semiconductor interface. However, the carrier mobility in the oxide is low and chances are that comparatively slow moving holes can get trapped in the oxide. This creates internal field. This lowers the barrier from gate to oxide. Consequently, more electrons tunnel into the oxide, and cause more impact ionization [2]. Two models for describing TDDB are prevalent within the scientific community. One is denoted by the E model and the other is the 1/E model. In the E model [40], t_{50} is defined as the median time to breakdown, and is given by:

$$t_{50} = A \exp(-\gamma E) \exp(E_a/kT), \qquad (5.22)$$

where A is a constant, γ is field acceleration parameter, E is the oxide field, E_a is thermal activation energy, k is the Boltzmann constant and T is absolute temperature. Researchers [43] showed that the free energy of activation for the breakdown reaction rate could be expressed as a series expansion in E. However, other researchers [44] state that the breakdown process is a current driven process. Thus t_{50} should be dependent on 1/E due to FN conduction. The 1/E model is good only at high voltages in thick oxides. The 1/E model [40] is given by:

$$t_{50} = \tau_0 \exp(G/E) \exp(E_a/kT), \qquad (5.23)$$

where τ_0 and G are constants, E is the oxide field and E_a is the activation energy. Figure 5.7 shows the TDDB of a thin oxide layer.

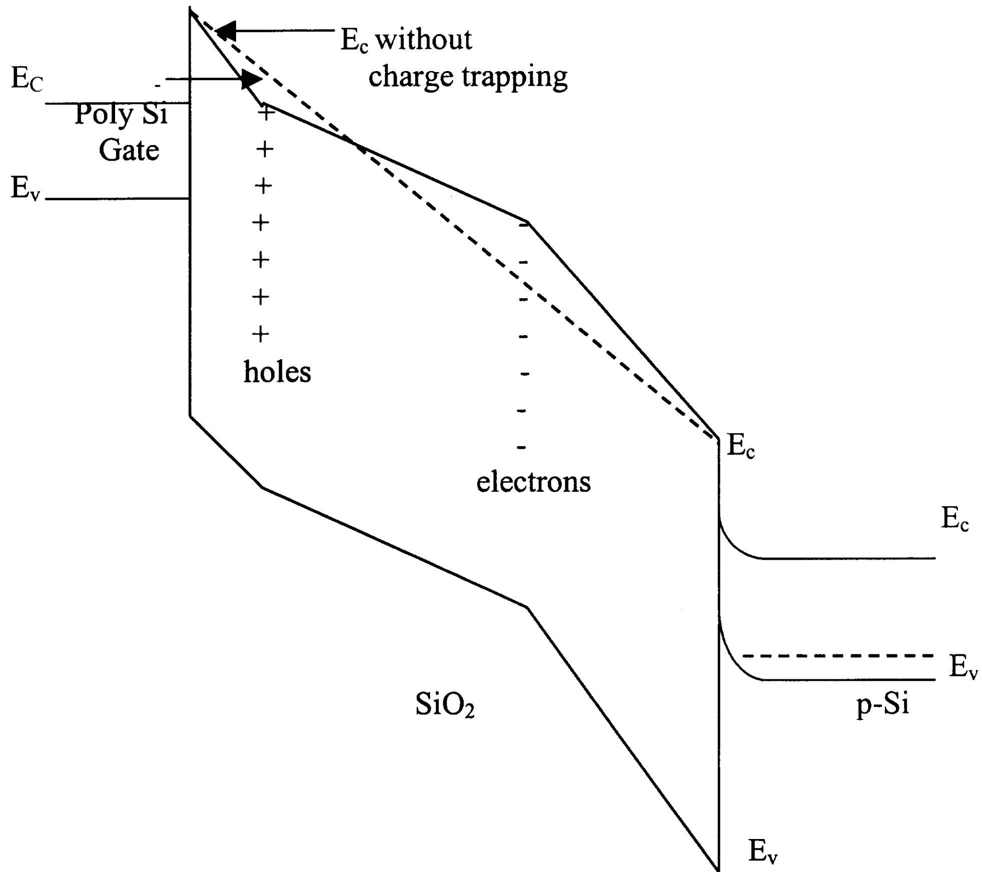


Figure 5.7 Time dependent dielectric breakdown of thin oxide layer [2].

CHAPTER 6

EXPERIMENTAL DETAILS

6.1 Sample Preparation

High-κ dielectrics, based on oxides of aluminum, hafnium and zirconium were prepared by atomic layer deposition (ALD) on 200-mm Si wafers in an ASM production reactor similar to the one shown in Figure 6.1. The samples for analysis were prepared from wafers received from Lucent Technologies and Agere Systems.

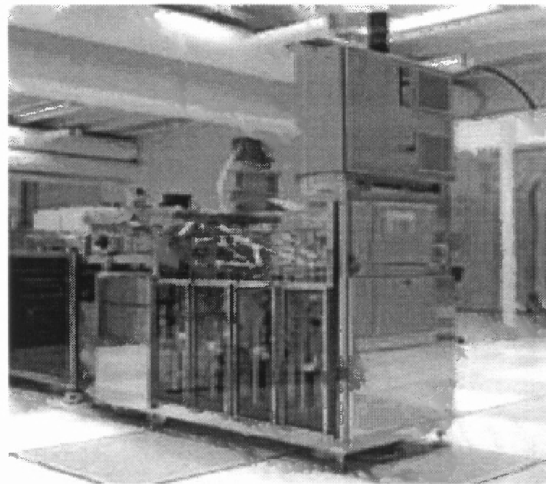


Figure 6.1 ASM PULSAR ALCVD system [45].

These ultra thin films were deposited directly on clean Si or on under-layers of various thin (~ 0.5 nm) oxides or oxynitrides of Si. The latter was grown in an ambient atmosphere of 60%NO and 40%O_2. The under layers were prepared both chemically as well as thermally. The purpose of the under layer films is to provide a barrier for charge penetration from the crystalline Si to the high-κ dielectric film. All cleaning steps were done in the same automated wet bench machine.

To prepare the chemical oxide, the first step was P-cleaning, using ozonated sulfuric acid solution as one of the constituents. The oxide was then stripped off, using dilute Hydrofluoric acid (HF). The wafers were then rinsed in ozonated deionized water. This reoxidizes the wafer. Such an oxide layer (5Å) is called a chemical oxide layer.

To prepare a thermal oxide underlayer, P-cleaning is the first step. Ozonated sulfuric acid solution was used as one of the constituents. The oxide was then stripped off, by using HF acid. Wafers were then reoxidized in Applied Material's Centura Rapid Thermal Oxidation system (RTO). Underlayers of various thin oxynitrides were thermally grown on Si (i.e., oxidation in pure O_2 or 60% NO and 40% O_2, respectively) in the RTO system. RTO oxide and oxynitrides were of 5Å thickness.

Al_2O_3 films were then deposited on the wafers, by passing precursors of tetramethyl aluminate $(CH_3)_3Al$ and water vapor, in cycles in the ALCVD machine. The deposition rate was estimated to be 0.87 Å/cycle. HfO_2 films were prepared by using precursors of $HfCl_4$ and water. The deposition rate was estimated to be 0.59 Å/cycle. Deposited Al-oxide films varied in thickness from 2 to 6 nm. The HfO_2 film thicknesses were of 4 and 6 nm.

Post deposition anneals (PDA) were used to stabilize the gate oxides. These were done at 600°C for 60s in N_2 atmosphere. This was carried out in RTA machine. PDA was performed to densify the film, remove the residual precursors and hydrogen. Equivalent oxide thickness (t_{ox}) measured by ellipsometer, varied from 1 to 3.5 nm. Pure thermal oxides were included in the study for reference.

Blanket in-situ heavily phosphorous-doped ($5x10^{21}$ cm^{-3}), polycrystalline silicon was deposited in Applied Material's Centura Rapid thermal CVD system. The deposited films were 160 nm thick. This process is required to prepare heavily doped gate electrodes in MOS structures. In the first study, both the Si wafer substrate and the gate electrode were p-type while for HfO_2, both p-type and n-type substrates were used.

MOS capacitor samples (of size 12mm x 12mm) were prepared from the wafers and suitably labeled. The samples were then placed on a dummy wafer as shown in Figure 6.2. Polysilicon was activated by annealing in the RTA system in N_2 ambient at 800˚C for 30s, or spike annealed at 950, 1000, and 1050˚C (nominally zero time at peak temperature). The RTA machine was programmed with 35˚C/s ramp up rate. The maximum available heating rate was about 150˚C/s. Power to the lamps was turned off at about 20˚C below the desired peak temperature for spike annealing.

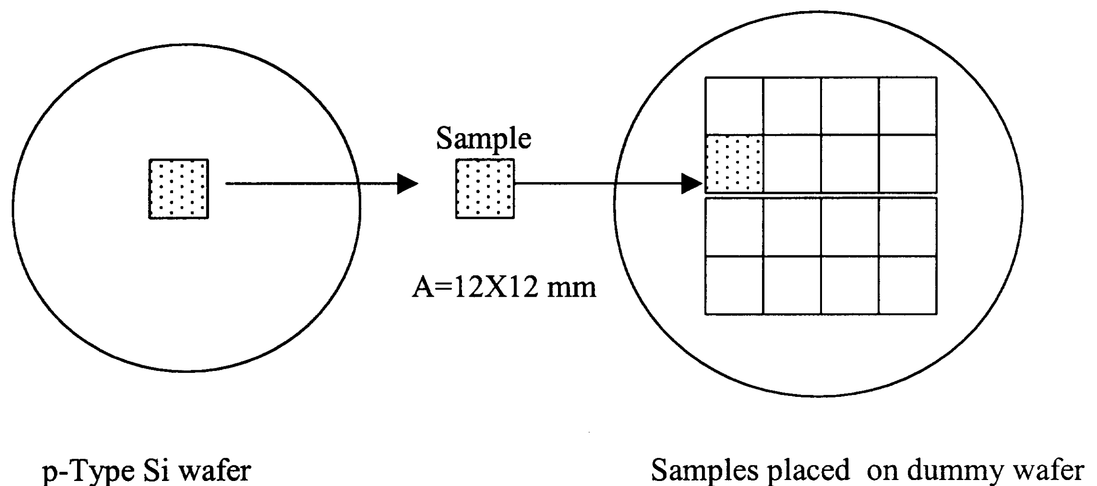


Figure 6.2 Sample preparation for the RTA activation.

Temperature was controlled by a ripple pyrometer calibrated against wafers with embedded type-K thermocouples [46]. Cooling at about 80˚C/s occurred by free radiation. Heating and cooling rates were approximately 50˚C/s.

The capacitors were prepared by applying black wax as dots onto the sample. The wax was used in place of photoresist. It was indirectly heated on hot plate. A wooden stick was used for their application onto the sample, which was also kept on the hot plate. Surface tension of the liquid wax caused it to form circular patterns. Care was taken not to over-heat the wax, as this may degrade the quality of the wax and cause it to polymerize. The prepared dots were allowed to cool for five minutes.

The Al_2O_3 gate dielectric samples were etched by wet chemical etching in a mixture of HF: HNO_3: H_2O (1:4:2) for 30 seconds. Each sample was taken out and cleaned with de-ionized (D.I.) water. The samples were dried by blowing nitrogen. The wax was then removed by dipping it sequentially for 30s in toluene, acetone, and propanol. The samples were purged with N_2 again.

Finally, the samples were dipped in HF: DI (1:10) solution to remove any residual products of etching and surface oxide. The samples were then cleaned in D.I. water and dried in N_2. This was done to remove the water from the sample surface.The HfO_2 samples were believed to be easily attacked by the HF: HNO_3: H_2O solution. High leakage current was observed in these samples.

Consequently, a 40% solution of Tetra Methyl Ammonium Hydroxide (TMAH) was used. It is considered to be a selective polysilicon etchant. The threshold temperature for etchant activation is 120°F. Therefore, it was indirectly heated in the temperature range of 138-145°F. Samples were dipped in TMAH for about six minutes. The samples

were stirred continuously, so that the reaction products got detached from them and a fresh surface was exposed in the solution all the time. The remaining cleaning steps were similar to those of Al_2O_3. The samples were tested immediately using the probe station.

6.2 Measurement Procedure

A probe station (Micromanipulator) was used for quasistatic C-V measurements. The probe station is basically a box type structure designed to isolate the sample from exposure to light. It is electrically grounded and has a facility for nitrogen purging. Nitrogen is used mainly to remove moisture from the sample. This is required so that the water in the sample does not become ionized and interfere with the measurements.

The sample was placed on the vacuum chuck in the probe station to measure electrical properties. The chuck can be electrically heated to make high temperature measurements (i.e., to study the transport of oxide charges from one interface to other). The chuck is connected to vacuum to hold the sample firmly to its place during the measurements. Three terminals were used for C-V measurements. The metal used for making contact with the sample was indium. It was chosen because of good adhesive properties and high conductivity. It is a malleable metal and application of indium on the sample was easy.

One terminal contact was made with the base (i.e., substrate) by scratching the sample with the help of diamond tip, until the substrate appears and then, applying a small piece of indium on it. Two contact pads were made on the capacitor gate electrode. The contact resistance was kept in the range of 100-150Ω. It was an indicator of a good metallic contact. Contact resistance was measured with a multimeter.

Hewlett Packard (HP) model 3310A function generator and Ithaco model 1211 current preamplifier were used to measure quasi-static frequency capacitance-voltage measurements. The function generator generates frequency from 50 to 5khz. It produces output voltage in triangular waveform of amplitude of ±3.0 V. The current preamplifier produces output voltage that is linear with input current (i.e., 10^{-6} Amp/Volt). The current preamplifier acts as a virtual ground sink for the circuit. A Tektronix TDS 340A, two-channel real time digital recording oscilloscope then displays the derived voltage in horizontal axis and the voltage from the preamplifier in the vertical axis. The scope records signals (i.e., voltage and output of the current preamplifier). Tektronix plots data vs time as well as channel 1 (ch1) vs channel 2 (ch2). Ch1 plots V (v) vs time (sec) on x-axis while ch2 plots I (amp) vs time (sec) on y-axis. The scope can plot either ch1 vs ch2 or both channels vs time. The data acquisition system collects the signal and saves them on a 1.44 MB floppy disc.

Figure 6.3 describes the set up schematically. The output voltage in the triangular form, from the function generator is supplied to one of the dots. The voltage from the scope is applied to the other dot. The input current from the sample is converted to voltage linearly and fed to the x-axis of the scope.

Figure 6.4 shows the equivalent electrical circuit. Here R_1, R_2 and R_3 are contact resistances arising because of the contacts being made on the sample surfaces. C is the capacitance of the MOS capacitor. The oscilloscope has high input impedance and the current preamplifier has low input impedance. Thus, the current passes through R_3 and it produces output voltage that is linear with input current. Figure 6.5 shows the time recording of the voltages on the x and y axis of the scope.

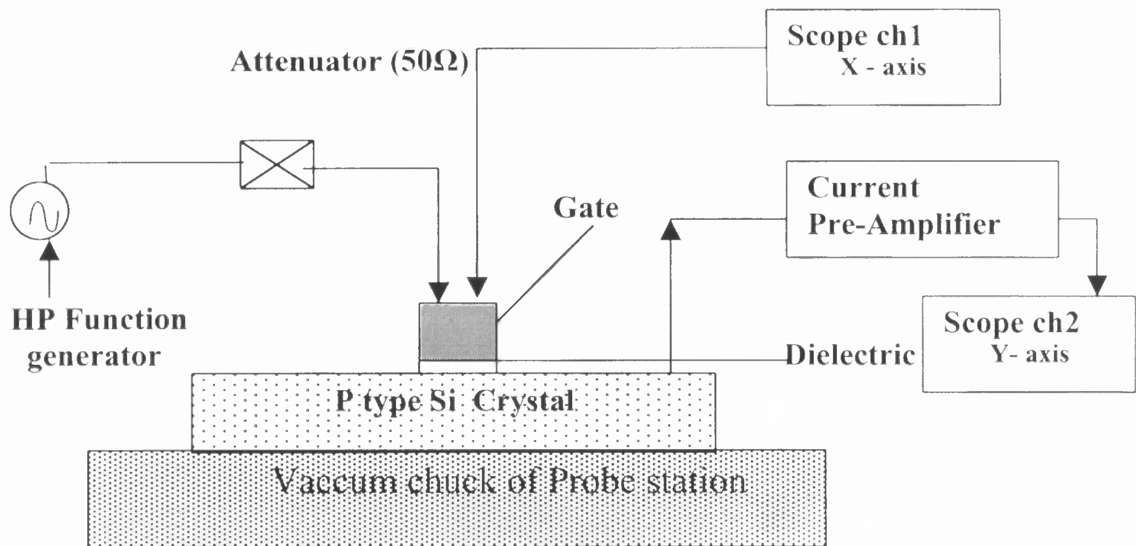


Figure 6.3 Schematic circuit of the experimental set-up for C-V measurements of MOS capacitors.

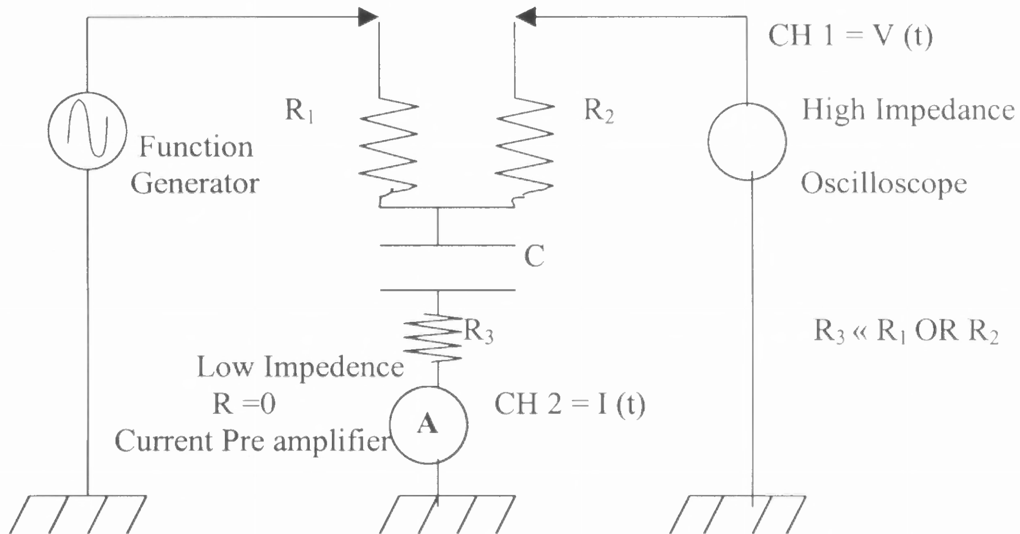


Figure 6.4 Equivalent electrical circuit of the experimental set-up where R_1, R_2 and R_3 are contact resistances.

From fundamentals it is well known that capacitance (C) is given by,

$$C(v, t) = dQ/dV \tag{6.1}$$

Equation 6.1 can also be written as,

$$C(v) = \{(dQ/dt)/(dV/dt)\} \tag{6.2}$$

writing $dQ/dt = I(t)$, we obtain

$$C(V) = I/(dV/dt) \quad (6.3)$$

An offline personal computer is used to analyze the signal according to Equation 6.3. Capacitance is found from the difference of current between one period of oscillation at the same voltage. The voltage points are found by interpolation of the data.

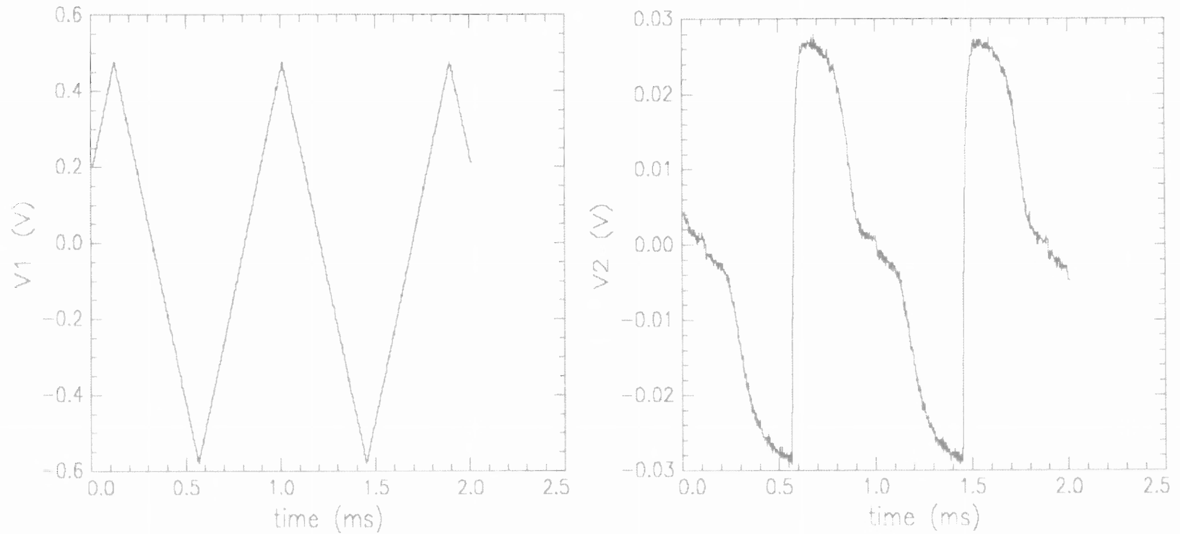
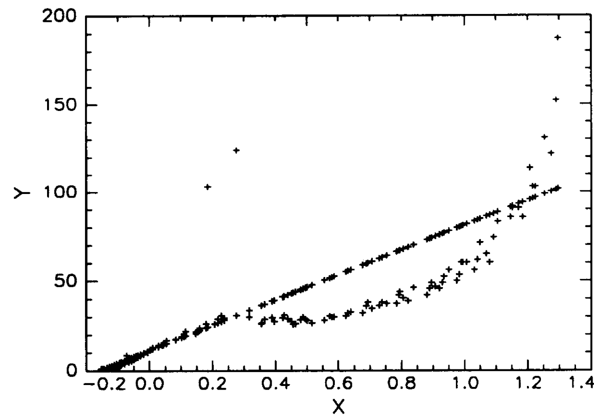


Figure 6.5 Voltage output of current preamplifier. It shows time recording of Voltage and current on y and x axis (i.e., Ch1 and Ch2).

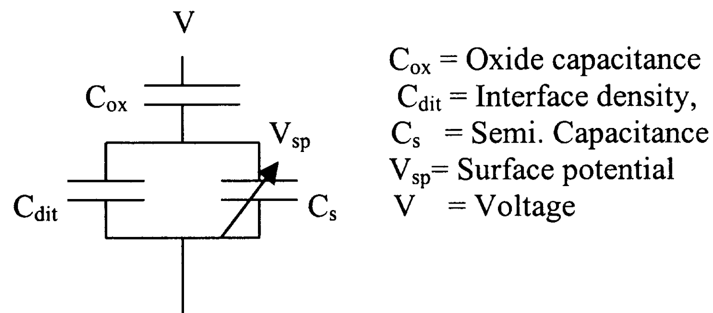
The generated C vs V data were analyzed using Equation 5.13 in deep depletion. The flatband gate voltage, V_{fb}, was determined by Berglund 's method i.e., fitting the Si surface potential from flat band into depletion [35]. See appendix A for the program.

Deep depletion is a non- equilibrium widening of the depletion layer width. In other words, during C-V measurements, if the gate bias is varied rapidly from accumulation to inversion, the depletion width can momentarily become greater than the theoretical maximum for gate bias beyond V_T.



X axis = Surface potential (V)

(a)



(b)

Figure 6.6 (a) The curve fit program plot of $1/C^2_s$(y-axis) v/s $V_{surface\ potential}$ (x-axis). (b) The equivalent circuit of the program.

The analysis program creates a plot of $1/C^2_s$ v/s $V_{surface\ potential}$, which is then fitted by Genplot program using a personal computer [47]. The program does a non-linear least squares fit. The result is shown in Figure 6.6 (a). Here, the linear line is the program fit while the data curve can be seen below line. It can be seen that the fixed charges are affecting the shape of the curve. The aim is to obtain as many points on the curve as possible. Figure 6.6 (b) shows the equivalent circuit used in the analysis. It requires the oxide thickness as input and fits D_{it} and V_{FB} as adjustable parameters. The capacitance for C_s in deep depletion is treated as in Equation 5.13.

The NCSU, CVC program, was also used for the analysis of the high frequency CV curves. This program uses a least-squares algorithm to fit the experimental data, where oxide thickness (t_{ox}), flatband voltage (V_{FB}) and substrate doping density (N_d) are used as fitting parameters.

These measurements and analysis techniques are applied to the high- problem in the next Chapter.

CHAPTER 7

RESULTS AND DISCUSSION

Flat band voltages (V_{FB}) were determined from C-V measurements with the use of equation 5.13 on circular MOS capacitor patterns. The shift in V_{FB} (ΔV_{FB}) is the measured V_{FB} relative to the theoretical V_{FB}. The samples were Post Deposition Annealed (PDA) at 600°C, in nitrogen atmosphere in the RTA machine. This was done to remove residual stress and to improve film densification. The influence of PDA on the MOS capacitor properties was examined. The 800°C, 30s anneals were used as a

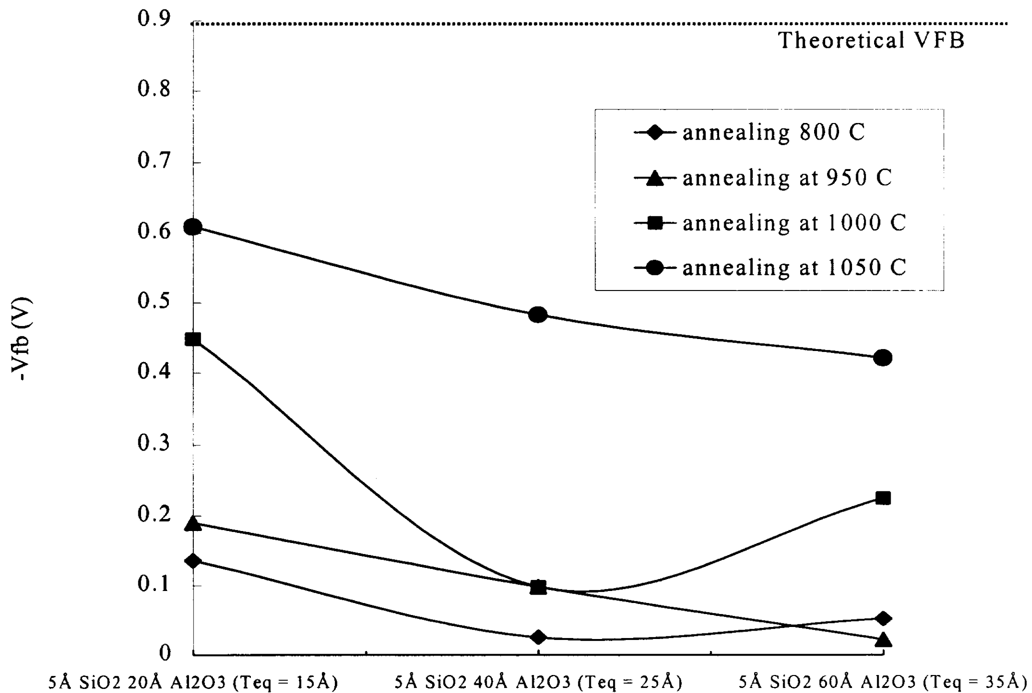


Figure 7.1 Plot of $-V_{FB}$ vs Al_2O_3 thickness and equivalent SiO_2 thickness (T_{eq}) for various annealing temperatures for p type substrates having 5Å SiO_2 underlayer.

baseline, at which the polycrystalline silicon electrodes are crystallized and acquire electrical activation while subjecting the high-κ dielectrics to low thermal budget anneals. Spike anneals at 900, 1000 and 1050°C were used to reduce the effect of fixed charges on V_{FB}. The spike anneals are similar to what could be used on MOSFETs to activate shallow junctions.

For P doped polysilicon electrodes and Al-oxide based dielectrics, positive shifts in V_{FB} ranging from 0.2 to 0.8 V were observed, relative to the theoretical V_{FB} value (i.e., -0.876 V). of pure SiO_2 control. The V_{FB} shifts are interpreted as evidence of fixed charges in the oxide film.

Figure 7.1 shows a plot of the negative V_{FB} for three high-κ film thicknesses annealed at four temperatures. The theoretical V_{FB} is denoted by dotted line. The Al_2O_3 films were deposited on a 5Å SiO_2 underlayer that was prepared chemically by rinsing the wafer in ozonated water after HF clean with no delay. The data shows that the baseline anneals at 800°C and the lowest temperature spike anneals have largest fixed charges. Trends indicate that spike annealing reduces the fixed charge in the oxide. This effect is greater in samples having 5Å SiO_2 /20Å Al_2O_3 gate-dielectric stack. The fixed charge density (N) can be found from the equation:

$$N = Q = (C_{ox}\Delta V_{FB})/q \qquad (7.1)$$

The data in Figure 7.1 indicates that N is of the order of 10^{13} cm^{-2} and varies by a factor of 2 with annealing. Figure 7.2 shows V_{FB} relative to anneal temperature for 5Å SiO_2/Al_2O_3 samples. The 5Å SiO_2 underlayer was prepared chemically by rinsing the wafer in ozonated water after HF clean with no delay. The trend of V_{FB} with anneal temperature for samples with various thicknesses of Al_2O_3 shows that, with increasing

anneal temperature, the fixed charges are reduced and there is decrease in V_{FB} towards the theoretical value. The decrease in V_{FB} is monotonic, with largest change occurring between 950 and 1050°C. The measured change in V_{FB} is ~ 0.5V. The 20Å Al_2O_3 sample shows less V_{FB} shift. This shows that the thin samples have less fixed charge. Samples exposed to base line anneal (800°C) show higher amount of fixed charges. Spike annealing is believed to be removing fixed charges and this is evident from the graphs. The change in V_{FB} is greater at higher temperatures than at base line anneals.

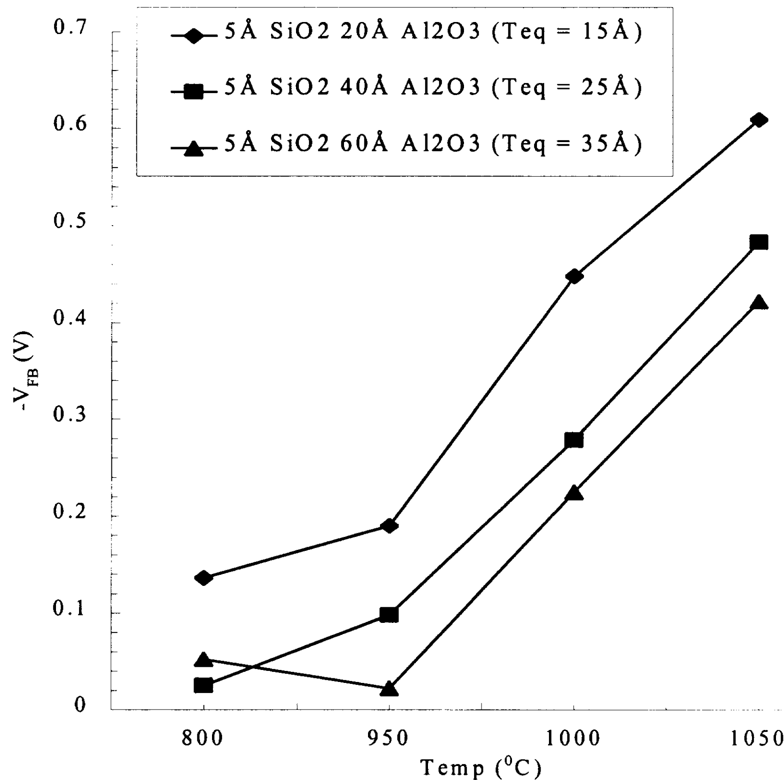


Figure 7.2 Plot of $-V_{FB}$ vs temperature for various thickness of Al_2O_3 with an underlayer of 5Å SiO_2.

In Figure 7.3, the change in V_{FB} relative to temperature for different thicknesses of RTO SiO_2 is presented. These SiO_2 films were grown on HF cleaned Si with no time delay in the RTO system. This experiment was done as a reference study. It clearly shows that, with decreasing oxide thickness, the V_{FB} value decreases. The shifts in the thinner films are believed to arise from leakage charge trapping in the dielectric. The spike annealing for thin samples shows detrimental effects. Results for base line annealing (800°C) and spike annealing show a steady decrease in V_{FB} with increasing film thickness. For the 106Å SiO_2 film, V_{FB} is equal to that of the theoretical value.

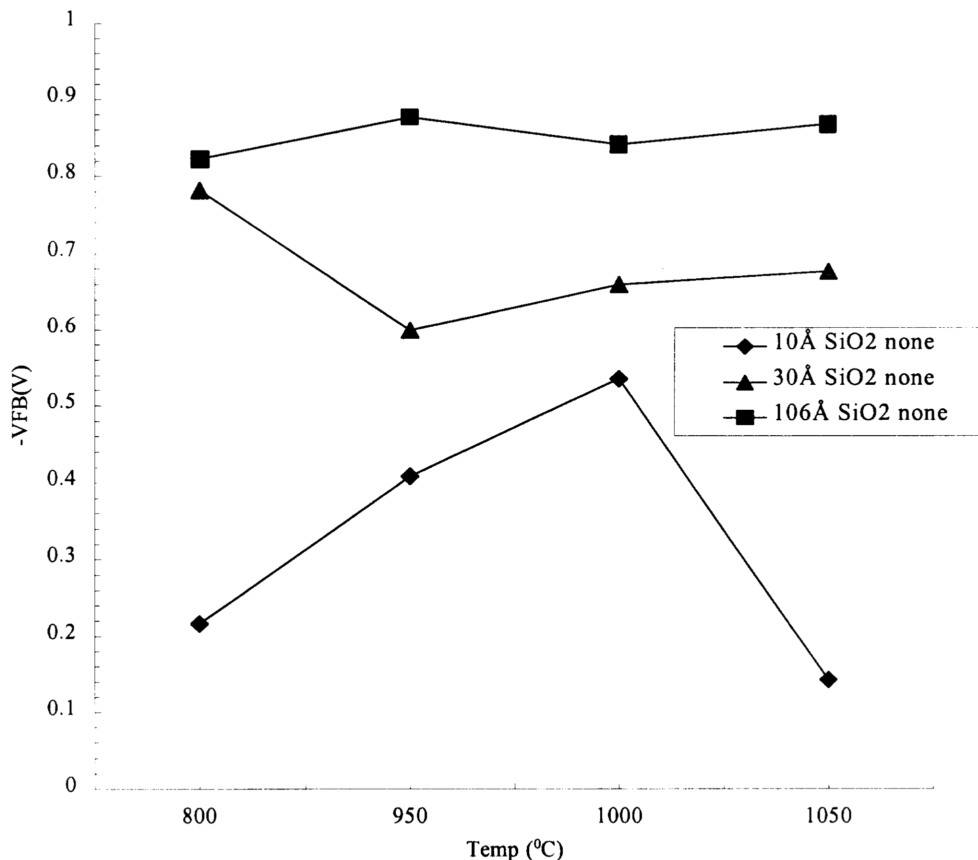


Figure 7.3 Plot of $-V_{FB}$ vs temperature for various RTO SiO_2 thickness with no underlayer or high-κ film. "none" indicates no underlayer.

Figure 7.4 shows V_{FB} relative to temperature for high-κ layers of varying thickness (i.e., 20-60 Å). The aim of this experiment was to study the characteristics of high-κ layer without the underlayer. The base line anneal is found to be effective in removing fixed charges. The thicker films show more fixed charges. The behavior at higher temperatures is irregular. Comparison with Figures 7.2 indicates that underlayer is helpful in reducing the amount of fixed charges. Moreover, the devices characteristics also improve when the underlayer is used. The layer is most likely to be amorphous. Thus, leakage current decreases, as the leakage path is more difficult to form in an amorphous phase.

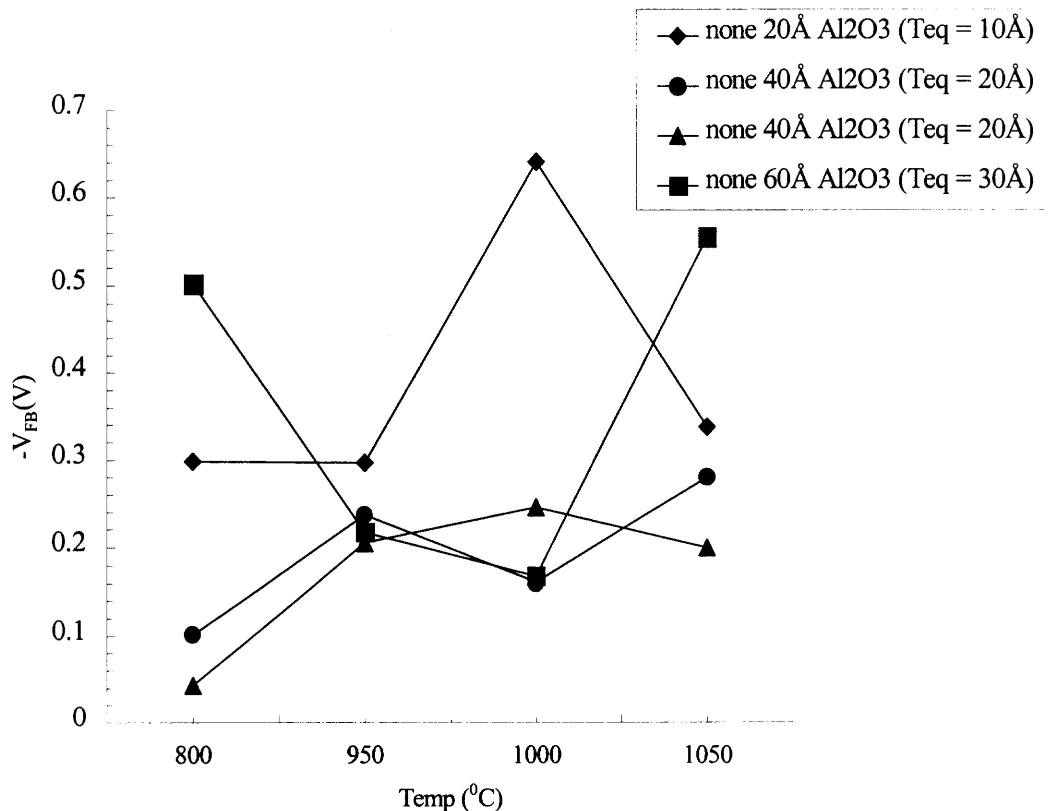


Figure 7.4 Plot of $-V_{FB}$ vs temperature for the ALCVD high-κ layer of various thickness. "none" denotes deposition of Al_2O_3 directly on cleaned Si surface. PDA omitted for the 40-Å film data plotted as circle symbols.

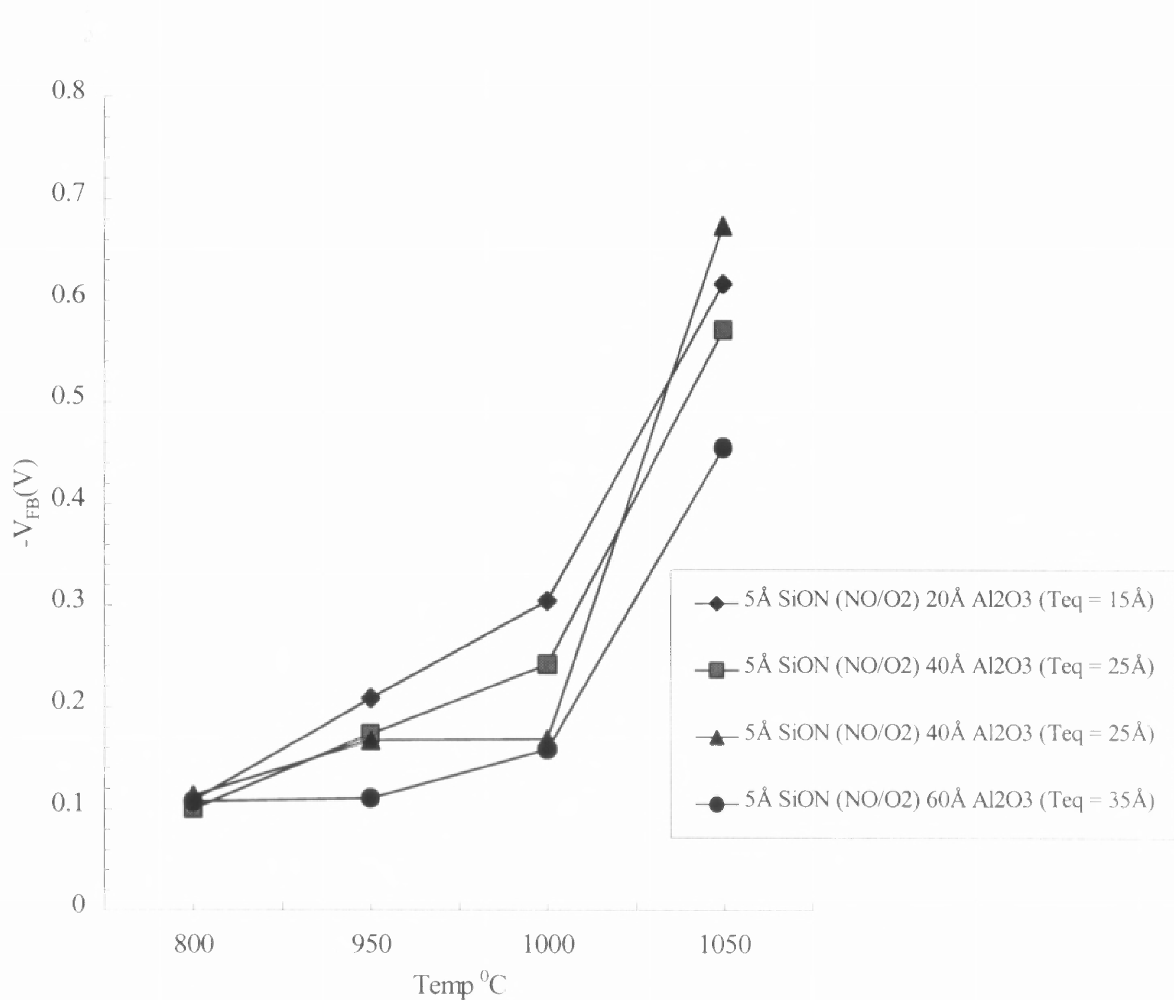


Figure 7.5 Plot of $-V_{FB}$ vs temperature for various thickness of high-κ layer of Al_2O_3 having underlayer of 5Å SiON (NO/O_2). PDA omitted for the (—■—) 40-Å film data.

Figure 7.5 displays graphs of $-V_{FB}$ relative to temperature for various thickness, of high-κ layer of Al_2O_3 having underlayer of 5Å SiON (NO/O_2), prepared by RT-NO (rapid thermal oxynitriding) on HF cleaned wafers. It shows the importance of the underlayer. SiON is known to be effective in neutralizing the fixed charges in the gate oxide. It is physically dense compared to SiO_2. Thus, a clear trend of decrease in $-V_{FB}$

with increasing annealing temperature is observed. Comparison of Figure 7.5 with Figure 7.2 shows that, with SiON as the underlayer, the change in V_{FB} with temperature is more rapid above 1000°C. It is believed that nitrogen bonding in SiON is stronger. Thus, movement of fixed charges is restricted at low temperatures. It is observed that spike annealing reduces the fixed charges more effectively than base line annealing. Also, a closer look reveals that thicker high-κ films have large amounts of fixed charges. The samples with SiON underlayer show more uniform behavior at base line anneals. Another experiment shown in Figure 7.4 and Figure 7.5, involves studying the effect of bypassing post deposition anneals. For 40Å Al_2O_3 films with underlayers (Figure 7.5) it is also observed that, for the same thickness, the PDA may be introducing more fixed charges. Results for films without underlayers are similar irrespective of whether there is a PDA step.

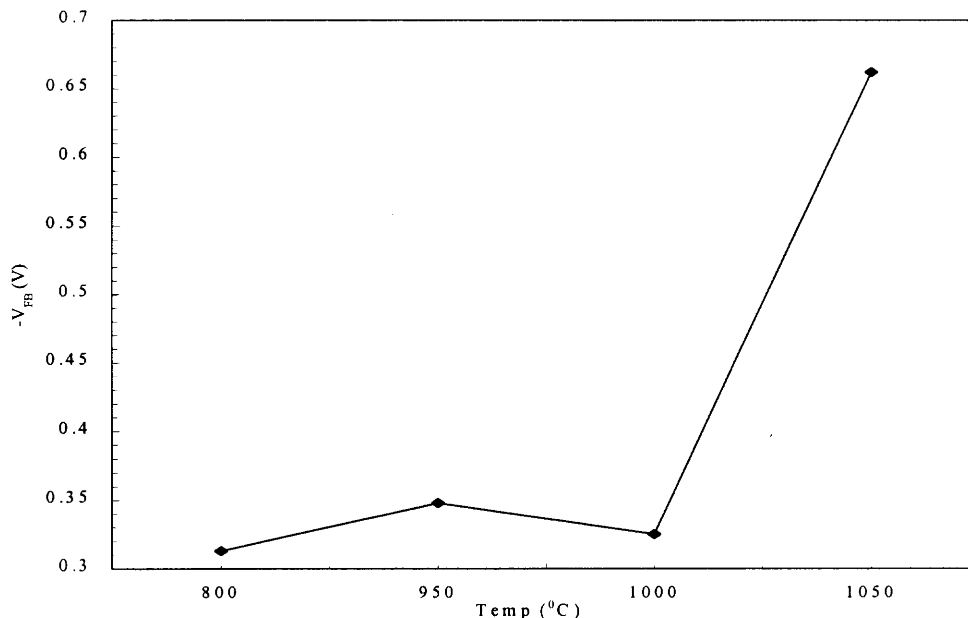


Figure 7.6 Plot of $-V_{FB}$ vs temperature for 20Å Al_2O_3 films over 5Å SiON underlayer grown in pure NO only.

Figure 7.6 shows $-V_{FB}$ relative to anneal temperature for 20Å Al_2O_3 with an underlayer of 5Å SiON RT-NO using pure NO ambient (NO only). Here $-V_{FB}$ is about 0.2 V lower than for samples with underlayers grown in ambients containing O_2, indicating an approximately 25% lower fixed charge for the NO-only growth ambient.

The plot also shows insensitivity of $-V_{FB}$ to annealing at or below 1000 °C. There is improvement in the characteristics of the high-κ dielectric when it is spike annealed at 1050 °C. Here again, spike annealing is more effective in reducing the amount of fixed charge than base line anneals. However, the annealing temperature dependence of the improvement is much more abrupt than for underlayers grown in ambients containing O_2. Tables 7.1 and 7.2 summarize the experimental data of $-V_{FB}$ for Al_2O_3 samples.

In summary, for the pure SiO_2 underlayer, high fixed charges are observed to be reduced by spike annealing with the most sensitivity to the annealing temperature. For underlayers grown in O_2/NO atmosphere, high fixed charges are observed which show intermediate response to high temperature anneals. Underlayers grown in pure NO-only atmosphere show less fixed charges and are less sensitive to anneals. In all cases, 1050°C is effective in minimizing fixed charges.

Table 7.1 Experimental Values of Al_2O_3 Gate Dielectric Sample, Where D_{it} is Interface State Density, N_d is Dopant Concentration and V_{FB} is the Flat Band Voltage

Anneal Temp (°C)	Wafer ID	$-V_{FB}$ Mean (V)	V_{FB} Error (V)	D_{IT} ($10^9 cm^{-2}/V$)	N_D ($10^{15} cm^{-3}$)	Underlayer & High-K Layer
800	111	0.108	0.01	0.104	0.025	5Å SiON (NO/O2) 20Å Al2O3 (Teq = 15Å)
950	111	0.208	0.00	1.182	0.003	5Å SiON (NO/O2) 20Å Al2O3 (Teq = 15Å)
1000	111	0.304	0.00	0.038	0.024	5Å SiON (NO/O2) 20Å Al2O3 (Teq = 15Å)
1050	111	0.616	0.00	0.148	0.023	5Å SiON (NO/O2) 20Å Al2O3 (Teq = 15Å)
800	112	0.136	0.00	2.230	0.903	5Å SiO2 20Å Al2O3 (Teq = 15Å)
950	112	0.190	0.00	0.715	0.004	5Å SiO2 20Å Al2O3 (Teq = 15Å)
1000	112	0.448	0.00	0.082	0.043	5Å SiO2 20Å Al2O3 (Teq = 15Å)
1050	112	0.609	0.01	0.085	0.018	5Å SiO2 20Å Al2O3 (Teq = 15Å)
800	113	0.313	0.01	0.006	0.004	5Å SiON (NO only) 20Å Al2O3 (Teq = 15Å)
950	113	0.348	0.00	0.015	0.006	5Å SiON (NO only) 20Å Al2O3 (Teq = 15Å)
1000	113	0.325	0.00	0.175	0.006	5Å SiON (NO only) 20Å Al2O3 (Teq = 15Å)
1050	113	0.662	0.02	0.465	0.026	5Å SiON (NO only) 20Å Al2O3 (Teq = 15Å)
800	114	0.100	0.01	0.004	0.012	5Å SiON (NO/O2) 40Å Al2O3 (Teq = 25Å)
950	114	0.173	0.00	0.028	0.012	5Å SiON (NO/O2) 40Å Al2O3 (Teq = 25Å)
1000	114	0.241	0.00	1.037	0.008	5Å SiON (NO/O2) 40Å Al2O3 (Teq = 25Å)
1050	114	0.57	0.00	0.267	0.039	5Å SiON (NO/O2) 40Å Al2O3 (Teq = 25Å)
800	115	0.113	0.02	0.016	0.010	5Å SiON (NO/O2) 40Å Al2O3 (Teq = 25Å)
950	115	0.167	0.01	0.470	0.013	5Å SiON (NO/O2) 40Å Al2O3 (Teq = 25Å)
1000	115	0.168	0.00	3.246	0.002	5Å SiON (NO/O2) 40Å Al2O3 (Teq = 25Å)
1050	115	0.673	0.00	0.030	0.018	5Å SiON (NO/O2) 40Å Al2O3 (Teq = 25Å)
800	116	0.025	0.01	0.028	0.002	5Å SiO2 40Å Al2O3 (Teq = 25Å)
950	116	0.098	0.01	0.001	0.003	5Å SiO2 40Å Al2O3 (Teq = 25Å)
1000	116	0.279	0.01	0.180	0.005	5Å SiO2 40Å Al2O3 (Teq = 25Å)
1050	116	0.483	0.02	0.008	0.084	5Å SiO2 40Å Al2O3 (Teq = 25Å)
800	117	0.107	0.00	0.003	0.005	5Å SiON (NO/O2) 60Å Al2O3 (Teq = 35Å)
950	117	0.110	0.01	0.001	0.026	5Å SiON (NO/O2) 60Å Al2O3 (Teq = 35Å)
1000	117	0.158	0.00	0.411	0.007	5Å SiON (NO/O2) 60Å Al2O3 (Teq = 35Å)
1050	117	0.454	0.00	0.001	0.043	5Å SiON (NO/O2) 60Å Al2O3 (Teq = 35Å)

Table 7.2 Experimental Values of Al_2O_3 Gate Dielectric Sample, Where D_{it} is Interface State Density, N_d is Dopants concentration and V_{FB} is the Flat Band Voltage, "none" indicates no underlayer

Anneal Temp (°C)	Wafer ID	$-V_{FB}$ Mean (V)	V_{FB} Error (V)	D_{IT} (10^9cm^{-2}/V)	N_D (10^{15}cm^{-3})	Underlayer & High-K Layer
800	118	0.052	0.00	1.820	0.003	5Å SiO2 60Å Al2O3 (Teq = 35Å)
950	118	0.022	0.00	0.297	0.002	5Å SiO2 60Å Al2O3 (Teq = 35Å)
1000	118	0.225	0.00	0.246	0.006	5Å SiO2 60Å Al2O3 (Teq = 35Å)
1050	118	0.422	0.00	1.387	0.016	5Å SiO2 60Å Al2O3 (Teq = 35Å)
800	120	0.101	0.00	0.005	0.564	none 40Å Al2O3 (Teq = 20Å)
950	120	0.237	0.00	0.026	0.037	none 40Å Al2O3 (Teq = 20Å)
1000	120	0.161	0.00	3.940	0.000	none 40Å Al2O3 (Teq = 20Å)
1050	120	0.280	0.01	0.002	0.074	none 40Å Al2O3 (Teq = 20Å)
800	121	0.043	0.00	0.014	0.011	none 40Å Al2O3 (Teq = 20Å)
950	121	0.205	0.00	0.026	0.006	none 40Å Al2O3 (Teq = 20Å)
1000	121	0.246	0.00	0.751	0.007	none 40Å Al2O3 (Teq = 20Å)
1050	121	0.200	0.01	0.007	0.071	none 40Å Al2O3 (Teq = 20Å)
800	122	0.502	0.00	0.345	0.152	none 60Å Al2O3 (Teq = 30Å)
950	122	0.217	0.00	0.253	0.016	none 60Å Al2O3 (Teq = 30Å)
1000	122	0.168	0.00	0.300	0.003	none 60Å Al2O3 (Teq = 30Å)
1050	122	0.555	0.00	0.198	0.032	none 60Å Al2O3 (Teq = 30Å)
800	123	0.216	0.02	0.034	0.006	10Å SiO2 none
950	123	0.408	0.02	0.004	0.012	10Å SiO2 none
1000	123	0.535	0.02	0.037	0.005	10Å SiO2 none
1050	123	0.142	0.01	0.001	0.087	10Å SiO2 none
800	124	0.782	0.02	0.005	0.017	30Å SiO2 none
950	124	0.599	0.02	0.007	0.033	30Å SiO2 none
1000	124	0.659	0.00	0.473	0.008	30Å SiO2 none
1050	124	0.676	0.00	0.000	0.090	30Å SiO2 none
800	189	0.298	0.01	0.025	0.003	none 20Å Al2O3 (Teq = 10Å)
950	189	0.297	0.00	0.001	0.005	none 20Å Al2O3 (Teq = 10Å)
1000	189	0.641	0.04	0.273	0.008	none 20Å Al2O3 (Teq = 10Å)
1050	189	0.338	0.00	0.000	0.091	none 20Å Al2O3 (Teq = 10Å)
800	X1	0.8223	0.01	0.002	0.041	106A SiO2 none
950	X2	0.876	0.01	0.048	0.006	- none
1000	X3	0.841	0.00	0.450	0.475	- none
1050	X4	0.867	0.01	0.000	0.081	- none

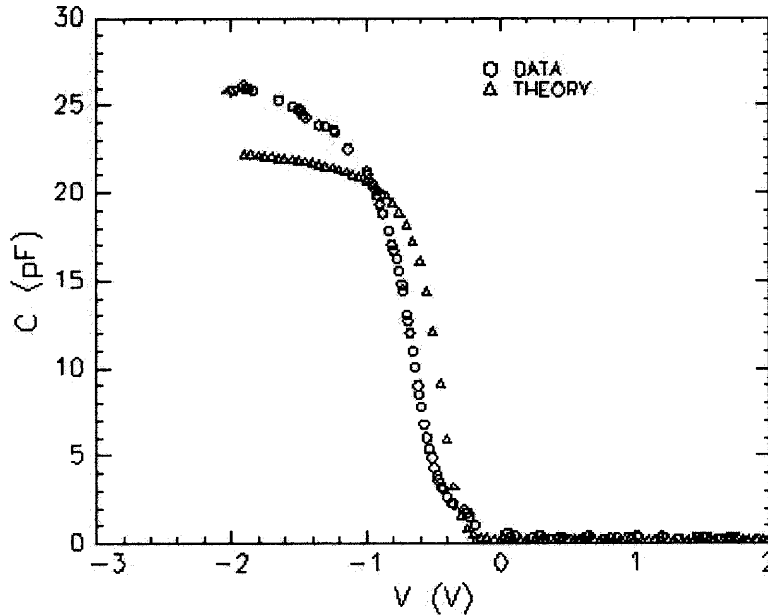


Figure 7.7 Comparison of measured C-V data with the theoretical C-V curve from NCSU CV3 program [48] for Al_2O_3 sample having 5Å SiON (NO/O_2) underlayer and high-κ layer of 40Å.

Figure 7.7 shows comparison of measured C-V data with the theoretical C-V curve using NCSU CV3 program [48] for Al_2O_3 sample having 5Å SiON (NO/O_2) underlayer and high-κ layer of 40 Å. The values for V_{FB} and N_d obtained from the depletion region of the curve, the experimentally determined T_{eq}, and polysilicon doping (~5E21 cm^{-3}) were fed into the program. The resulting capacitance values were plotted relative to applied voltage. The plot shows that, in the depletion region, both the theoretical and the experimental data overlap.

However, there is a shift in V_{FB}. Also, in the accumulation region, the capacitance does not approach saturation, as predicted by the model. These effects may be occurring due to charging of oxide and fixed charges. These charges distort the resulting C-V curve in the accumulation region.

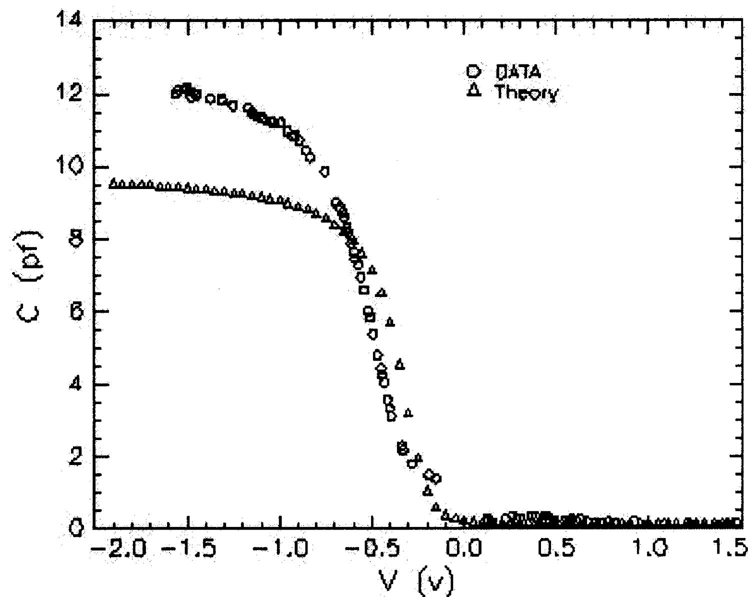


Figure 7.8 Comparison of measured C-V data with the theoretical C-V curve of NCSU program for Al_2O_3 5Å SiON (NO/O_2) underlayer and high-κ layer of 60 Å.

In Figure 7.8, a comparison is made of the measured C-V data with the theoretical C-V curve of NCSU program for Al_2O_3 5Å SiON (NO/O_2) underlayer and a high-κ layer of 60 Å. Again, there are differences in the V_{FB} region and accumulation region. There is also a decrease in the effective oxide thickness, since the measured capacitance is greater than the calculated capacitance.

Figure 7.9 gives a comparison of measured C-V data with the theoretical C-V curve of NCSU program for a sample with 5Å SiO_2 underlayer and a high-κ layer of Al_2O_3 of 60Å thickness. The effect of higher oxide capacitance is clearly visible.

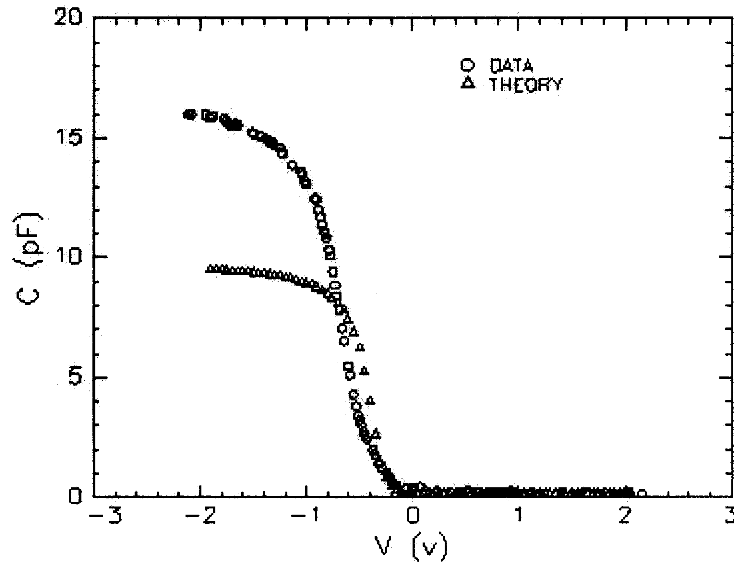


Figure 7.9 Comparison of measured C-V data with the theoretical C-V curve of NCSU program for Al_2O_3 5Å SiO_2 underlayer and high-κ layer of 60 Å

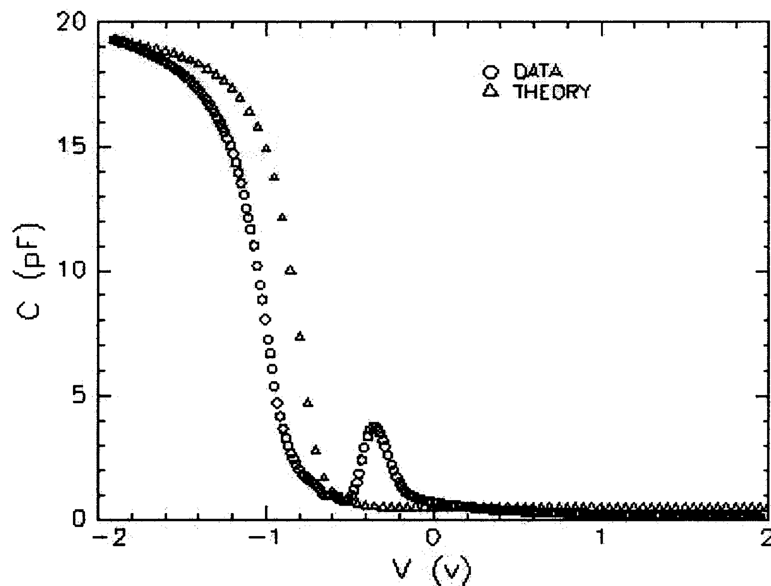


Figure 7.10 Comparison of measured C-V data with the theoretical C-V curve of NCSU program for 30Å SiO_2.

Figure 7.10 shows a comparison of measured C-V data with the theoretical C-V curve of NCSU program for 30Å SiO_2. Here, the presence of oxide charges is seen. An attempt was made to overlap the measured and calculated C-V curve by adjusting the oxide thickness in the program (17 Å). However, due to the presence of fixed charges and

interface traps, the curve is stretched in the accumulation region. This is visible in the plot, where the calculated curve and the data differ in the accumulation region. The feature observed at -0.35 V bias is believed to arise from minority carrier response and interface traps.

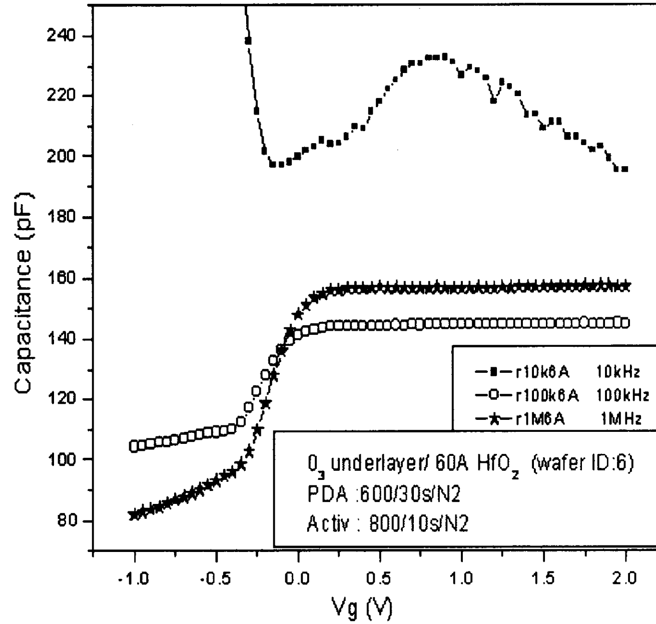
The HfO_2 films were deposited on n and p type wafers, respectively. The polysilicon was also doped n and p type, respectively. The wafers had an underlayer prepared either by ozonated deionized water or by RT-NO in the RTO machine. The underlayer films were 5.5 and 5.0 Å, respectively. The HfO_2 thickness was kept at 40 Å and 60Å. PDA was performed at 600°C for 30 s in nitrogen atmosphere. Table 7.3 shows the wafer preparations steps.

Table 7.3 Sample Preparation Chart for HfO_2 Gate Dielectric Samples; PCL = P clean step, HF is for HF Last Step

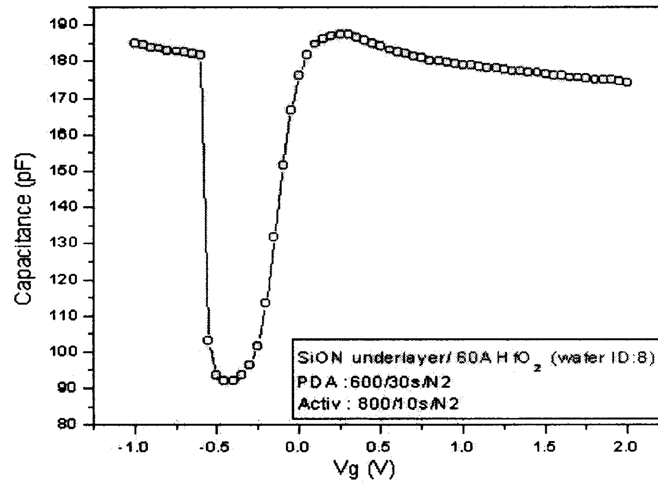
Scribe id	Final Clean	Underlay	ALD cyc. / Tphys (Å)	PDA (Heatpulse)	EOT (Å)
1	PCLO3/SC1/HF + 60sec O3	5.5 Å	68 cyc HfO2/40 Å	600 / 30s / N2	13 Å
2	PCLO3/SC1/HF + 60sec O3	5.5 Å	102 cyc HfO2/60 Å	600 / 30s / N2	17 Å
3	PCLO3/SC1/HF	5 Å SiON	68 cyc HfO2/40 Å	600 / 30s / N2	13 Å
4	PCLO3/SC1/HF	5 Å SiON	102 cyc HfO2/60 Å	600 / 30s / N2	17 Å
5	PCLO3/SC1/HF + 60sec O3	5.5 Å	68 cyc HfO2/40 Å	600 / 30s / N2	13 Å
6	PCLO3/SC1/HF + 60sec O3	5.5 Å	102 cyc HfO2/60 Å	600 / 30s / N2	17 Å
7	PCLO3/SC1/HF	5 Å SiON	68 cyc HfO2/40 Å	600 / 30s / N2	13 Å
8	PCLO3/SC1/HF	5 Å SiON	102 cyc HfO2/60 Å	600 / 30s / N2	17 Å

For HfO_2, the capacitance measurement was not possible because of high leakage current through the oxide layer. It was believed that the nitric-hydrofluoric acid etchant, which was used for Al_2O_3, might have been too strong for HfO_2 and may have laterally etched the gate dielectric. Consequently, the leakage currents were too large. Independent C-V measurement performed at Bell Laboratories, Murray Hill, NJ, also, showed similar results. C-V measurements were not interpretable because the leakage current was too high. This can be seen in Figures 7.11 and 7.12, which show high and low frequency C-V measurements using the methods described in Chapter 5, Sections 5.1.1 and 5.1.2. Therefore, the etchant was replaced by TMAH solution, as described in Chapter 6. TMAH is believed to be milder to HfO_2 compared to HF: HNO_3: H_2O solution. However, depletion and the accumulation curves were still not obtained because of high leakage. Crystallization of the HfO_2 during activation annealing may be causing the observed behavior.

ZrO_2 samples were tested and were also found to be leaky. Depletion curves were not obtained due to high leakage at the gate electrode. It is speculated that Zr silicide formation causes electrical weak spots or shorts.

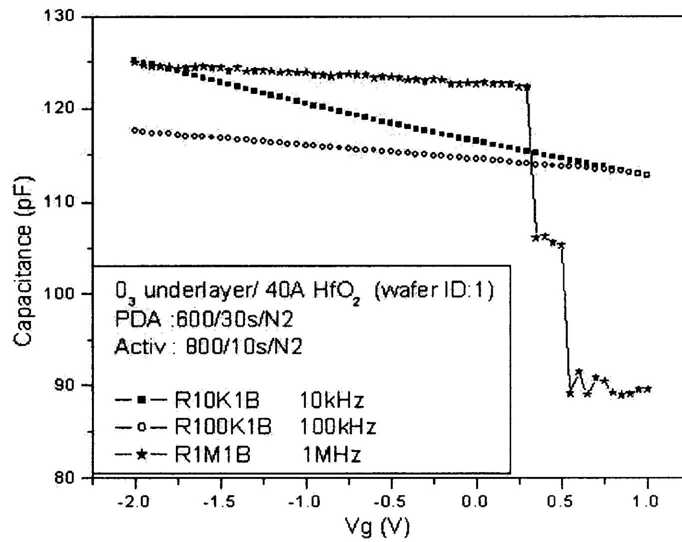


(a)

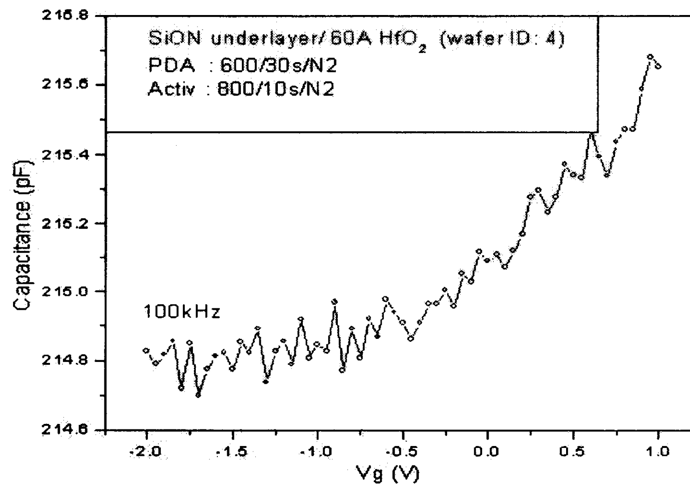


(b)

Figure 7.11 (a) The C-V measurements at low and high frequency for samples having SiO_2 as underlayer (b) Low frequency measurements of the sample having SiON as underlayer. The samples consisted of n-type polysilicon and substrates.



(a)



(b)

Figure 7.12 C-V measurements on HFO_2 samples on n-type Si. (a) With O_3 (Ozone) underlayer and (b) With SiON underlayer.

CHAPTER 8

CONCLUSION

For many years, the semiconductor industry has benefited from SiO_2, a native oxide of silicon, which has excellent physical, chemical, structural and electrical properties. As a result of vigorous scaling of device dimensions in VLSI technology, the gate oxide thickness has been reduced to ~2 nm or less. The gate leakage current, in the MOS device, increases drastically in this thickness regime causing high consumption of stand-by-power in integrated circuits. The replacement for SiO_2, as a gate dielectric, is required within the next three to four years. The new gate dielectric material should meet all the material properties (i.e., miminal gate leakage current, chemical and thermal stability, t_{ox}, mobility, diffusion barrier to the gate metal, etc.) in order to meet the stringent ITRS roadmap predictions.

In the present study, flat band voltage shifts were measured on MOS capacitors utilizing Al_2O_3, HfO_2 and ZrO_2 as gate dielectrics. It was observed that the fixed charges in Al_2O_3 caused the shift in measured V_{FB}. The effect of the mobile charges was observed in the accumulation region of the C-V curve. The back and forth movement of the mobile charges from the gate oxide to the substrate caused the shift in the measured capacitance and the C-V curve was distorted in the accumulation region. It is believed that interface traps also affect inversion layer formation in the depletion region in low frequency C-V measurements.The etching techniques applied for preparing HfO_2 was found to be satisfactory. Thus, the high leakage found in HfO_2 is due to inherent material properties. The ZrO_2 gate dielectric may have formed a conducting silicide by reacting with polysilicon, after annealing, resulting in high leakge current.

APPENDIX

PROGRAM FOR CALCULATION OF -V_{FB}

This program calculates V_{FB}, V_{FB}(error), D_{it}, N_D.

```
/* DIT in units of 1E9 /Vcm^2, ND is crystal Si doping in units of 1E15 /cm^3

hc on

declare fname = &QUERY -PROMPT 'CV data file'

setv tox = &QUERY -PROMPT 'tox in Angstroms'

setv pfb=1.

setv dit=.1

setv ss=1.e-16

/* change sign of x axis

read %fname% -col 1 2 let x=-x sort arch cc

setv cox=3.9*.0885e-12/(1.e-8*tox)

let y=y/cox transform integrate let y=x-y fit spline let y=y-fit(0) exch arch pv

let y=1./cc:y-1./cox let x=pv:x let y=y*y

setv nd=2.5

let nd=(@avg(x)/@avg(y))/9.18e-9**2 eval nd

let y=ss*y

define c=1.6e-10*sqrt(dit*dit)+9.18e-9*sqrt(sqrt(nd*nd)/vx)

define cfbs=1./(1./8.05e-8*sqrt(sqrt(nd*nd))+1./cox)

/* define dit1=sqrt(dit*dit+1.e-5)

define vx=max(x-.026-pfb,.013)
```

```
define f=ss/(c*c)

pl -pen 3 title 'Fit data inside cursor box' cull_data keep cur

let pfb=@min(x)

setv x1=@min(x)

setv x2=@max(x)

/* eval @min(x) eval @max(x)

/* eval @min(y) eval @max(y)

fit nlsfit

function f

vary dit /

vary nd /

vary pfb /

fit

return

/* pl ov -fit -pen 2  arch yc

/* let y=1./(1./cc:y-1./cox) let x=pv:x

/* fit spline

/* eval fit(0)-9.14e-9*sqrt(nd/.026)

retr pv fit spline

setv vfb=fit(pfb) eval vfb

retr cc fit spline eval fit(vfb) eval cfbs

let x=pv:x let y=1./cc:y-1./cox let y=ss*y*y pl title %fname%

let y=f ov -pen 2
```

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