ABSTRACT

FORMATION AND CHARACTERIZATION OF n/p SHALLOW JUNCTIONS IN SUB-MICRON MOSFETs

by
Sridhar Madishetty

Semiconductors are the burgeoning industries in today's information age. Silicon based microelectronic devices are shrinking day-by-day in accord with the scaling dimensions reported by the International Technology Roadmap for Semiconductors (ITRS). There have been many semiconductor models and simulation programs constantly keeping pace with the continuously evolving scaling dimensions, process technology, performance and cost. Electrical characterization plays a vital role in determining the electrical properties of materials and device structures. Silicon based Metal Oxide Semiconductor Field Effect Transistor (MOSFET) forms the basis of Complimentary Metal Oxide Semiconductor (CMOS) circuits. Today's aggressive scaling approaches in silicon Integrated Circuit (IC) technology require ultra shallow junctions in MOSFETs.

The objective of this thesis is to study the leakage current in n/p shallow junctions and to correlate them with process steps required for the formation of shallow junctions. The leakage current measurements were performed by utilizing three-point probe method, which is one of the popular techniques used in the semiconductor industry. Apart from n/p shallow junctions, experiments have been performed on p/n shallow junctions. Finally, comparison of the leakage current measurements has been made. The comparison takes into account the implant variables and post-implant annealing steps that have been deployed in the fabrication of shallow junctions.

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Sridhar Madishetty

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"Dedicated to my beloved family"

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CHAPTER 1

OVERVIEW

This thesis is divided into seven chapters prefaced by the contents. Each Chapter begins with an introduction to the chapter prior to the detailed explanation of the sub-topics inside the chapter and ends with a summary.

The second Chapter deals with the fundamentals of transistors. Various types of transistors and the principle of operation are explained in a lucid manner.

The third Chapter focuses on processing of formation of shallow junctions. Ion implantation, which is one of the dominant methods of introducing dopants, is explained in depth. The various ion implantation process parameters influencing the electronic properties of silicon are also discussed. Different types of rapid thermal processing, various types of annealing and thermal budget are some of the interesting topics covered.

The fourth Chapter focuses on the mathematical modeling of ion implantation. Some of the mathematical models like Stopping Range of Ions in Matter (SRIM), Transport of Ions in Matter (TRIM) and Rutherford Universal Manipulation Package (RUMP) have been discussed.

The fifth Chapter describes characterization techniques. There are many characterization techniques available to the semiconductor industry. Some of these techniques are discussed.

The experiments performed at NJIT, for this research, are discussed in the sixth Chapter. The electrical characterization technique using three point probe method is also discussed.

The seventh Chapter focuses on results and discussion based on our experiments. Conclusions and recommendations based on these studies are summarized in Chapter 8.

In the appendices, figures relevant to shallow junction device data are discussed in the thesis. Also, sample experimental data is presented in Appendix C. A simple program written in C++ for calculation of area and leakage current is included in Appendix D.

CHAPTER 2

TRANSISTOR FUNDAMENTALS

Transistors are the heart of the microelectronics industry. In day-to-day life, there are many applications of microelectronics in computers, televisions, mobile phones, automobiles, home appliances, aircrafts, medical appliances, space shuttles, et. In Integrated Circuit (IC) technology, transistors can execute some millions (with $>10^9$ frequency) of instructions per second, which is called flow of binary information. Historically, transistors replaced vacuum tubes. In its simple operation, transistor can act as an electronic switch with ON and OFF functions.

2.1 Principle of Operation of Transistors

The following are the different types of transistors:

- Bipolar Junction Transistor (BJT).
- Junction Field Effect Transistor (JFET).
- MEtal Semiconductor Field Effect Transistor (MESFET).
- Metal Oxide Semiconductor Field Effect Transistor (MOSFET).
- Metal Insulator Semiconductor Field Effect Transistor (MISFET).

Figure 2.1 shows a simple n-type (JFET) transistor with three terminals - emitter, base and collector or source, gate and drain. In Figure 2.1, it can be seen that for an n-type transistor, the substrate is p-type silicon and the source and drain are negatively charged. The gate is generally doped polysilicon on an insulating layer, such as SiO_2, which is grown or deposited on the substrate. When a positive voltage is applied to the

gate electrode, the electrons in the p-substrate get attracted towards the gate region thereby, forming a certain area or a region below the gate. This area indeed serves as the channel for the flow of electrons from the source and drain. During the ON state of a transistor, that is, when a positive voltage is applied to the drain, the electrons from the source is pulled towards the drain and similarly, during the OFF state of a transistor, there is no flow of electrons.

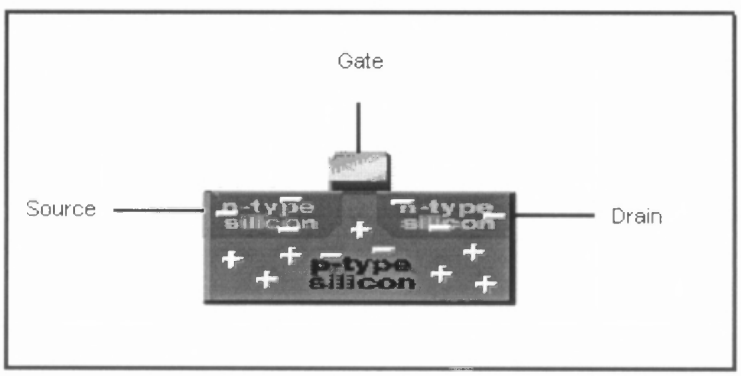

Figure 2.1 n- type JFET transistor.

2.2 Bipolar Transistors

Figure 2.2 represents an n-p-n bipolar junction transistor. The symbols I_E, I_B and I_C denote the emitter current, base current and collector current respectively. The direction of electron flow and hole flow is described in Figure 2.2. In the normal mode of operation, the emitter and base junction should be forward biased and the collector and base region should be reverse biased. Due to forward bias, the majority carriers i.e., electrons, will flow into the base region and the holes flow into the collector region. However, as the base region is very thin and due to the large positive collector - base voltage, these electrons are collected by the collector [1].

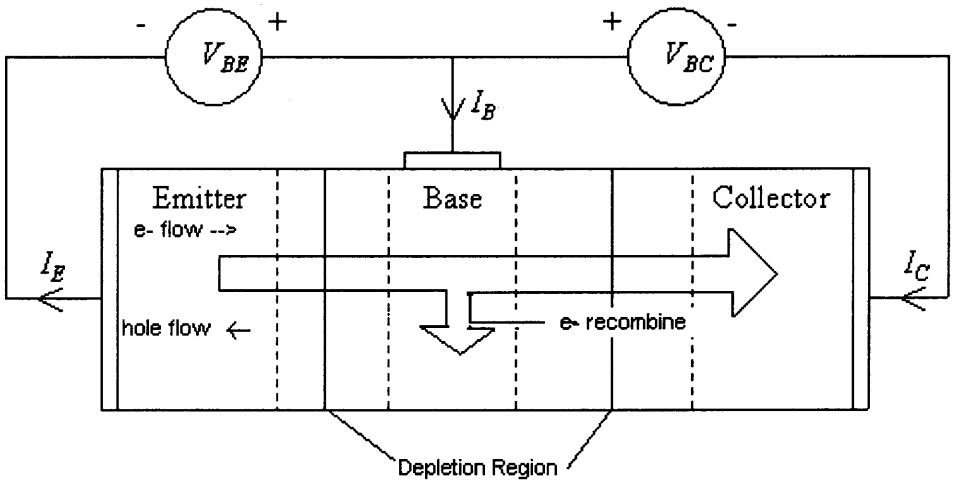

Figure 2.2 Schematic line diagram of an npn BJT.

2.3 Field Effect Transistor (FET)

One of the undesirable features of a bipolar transistor is low input impedance with the base-emitter junction that causes matching impedances between interstage amplifiers. The Field Effect Transistor (FET) has high input impedance combined with many other advantages. These devices are useful for controlled switching in digital circuits between conducting states and insulating states and are widely used in the (IC) industry. Bipolar transistors use bias current between base and emitter to control conductivity whereas, FET uses voltage to control an electrostatic field within the transistor. FETs can also be called as unipolar devices, as the operation of these devices depends on only one type of carrier i.e., majority carriers. BJT operates by the injection and collection of minority carriers (action of both electrons and holes). Hence, it is called as a bipolar device [2]. There are two basic types of FETs:

- Junction Field Effect Transistor (JFET or FET);
- Metal Insulator Semiconductor Field Effect Transistor (MISFET).

2.3.1 Junction Field Effect Transistor

In general, there are two types of JFETs: one is an n-channel JFET and the other is a p-channel JFET. In Figure 2.3, a pair of metallic contacts can be seen at each end of the channel. Current flows from one contact to the other when a voltage is applied. This Figure 2.3 represents a typical n-type channel JFET where the electrons drift from left to right, opposite to the current flow.

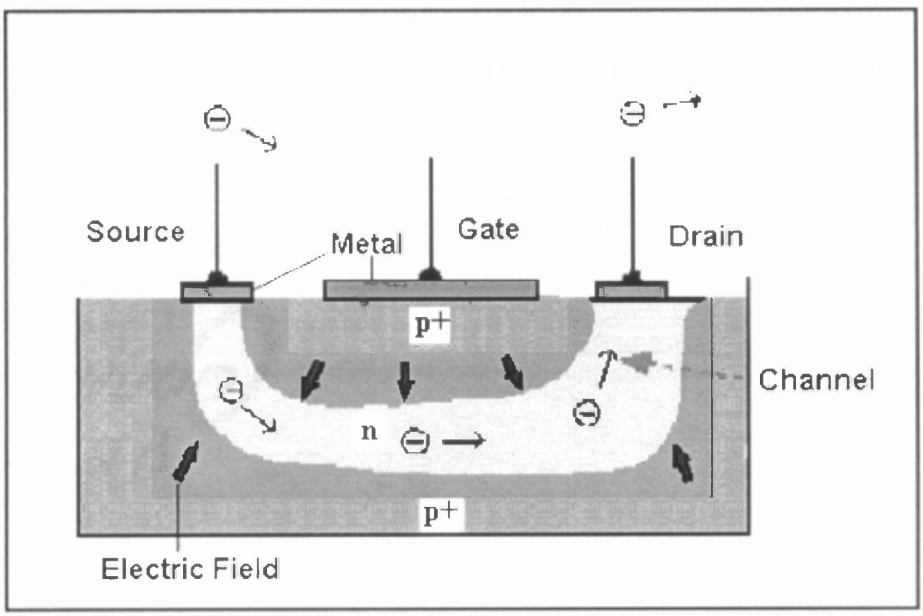

Figure 2.3 Typical JFET transistor.

The end of the channel from which flow of electrons takes place is called source and these electrons reach the other end called drain. Similarly, in the case of a p-channel JFET, there will be flow of holes from source to drain. It is to be noted that gate junction of a JFET is always reverse biased thereby, the gate current is essentially zero. This permits the use of JFET as a resistor in ICs at low voltages.

2.3.2 Metal Insulator Semiconductor Field Effect Transistor

These are widely used in the IC industry. In these types of devices, the gate voltage controls the channel current and the gate electrode is isolated from the conducting channel by an insulator. Generally, this insulator is silicon dioxide (SiO_2). Hence, these are commonly termed as MOSFETs.

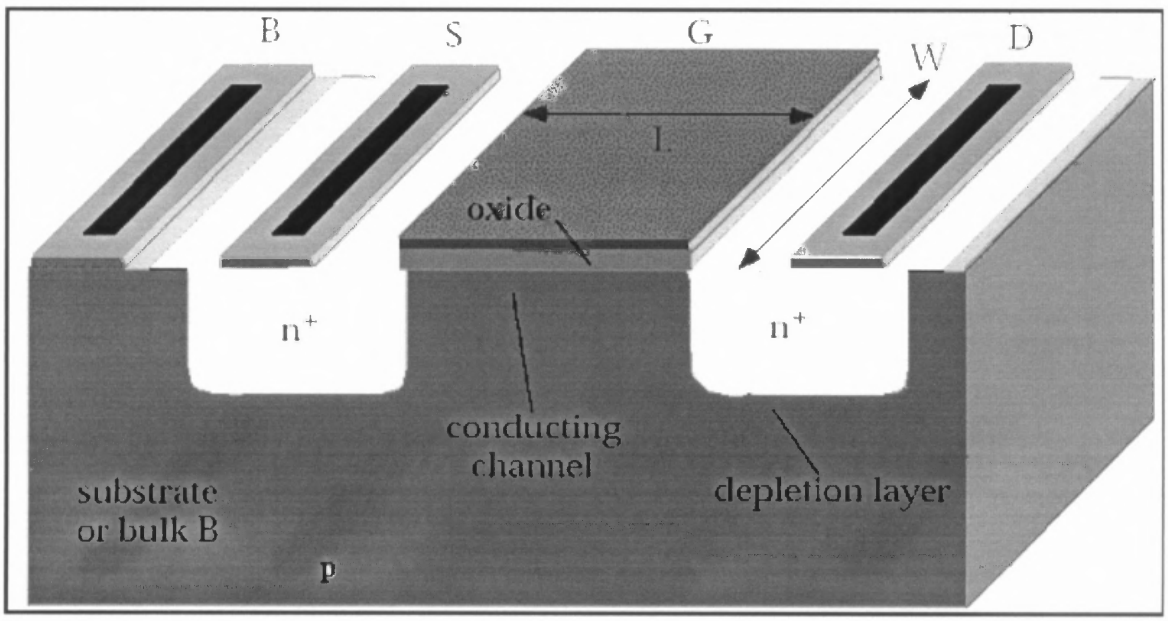

Figure 2.4 n- Channel MOSFET [3].

Figure 2.4 represents an n- Channel MOSFET [3]. It consists of a p-type substrate (bulk) and two n-type wells that are diffused into the substrate, which form source and drain of the device and these regions are separated by the conducting channel. The gate acts as the control valve of this device for the flow of current and is typically made of polycrystalline silicon (polysilicon) material. Polysilicon of the gate material acts as one plate of a capacitor and the substrate acts as the other plate of a capacitor with relatively low conductivity. During its operation, if a positive voltage is applied to the

gate with respect to the substrate, then, in order to maintain equilibrium condition, negative charges are induced in the substrate. A thin depletion region containing mobile electrons is formed and the current flows from drain to source. As these electrons continue to be induced electrostatically, the p-channel becomes less and less p-type. Due to this, the valence band droops down away from the Fermi level. Consequently, there will be no flow of current from source to drain until the electrons overcome the barrier (which is the threshold voltage V_T). The threshold voltage is defined as the minimum voltage required to form a channel and is controlled by the gate. Hence, the positive gate voltage must always be larger than the threshold voltage so as to form a conducting channel. This type of transistor that requires a positive voltage to turn on is called as enhancement mode transistor. Similarly, in some cases, a source to drain current will flow at zero gate bias and negative potential is required to turn off. These are known as depletion mode transistors [4].

2.4 Applications of Transistors

The applications of transistors are as follows:

1. Transistors are used in amplifiers, which amplify the ac signal.
2. Transistors are used in oscillators that convert dc into an ac signal.
3. Transistors can be used as variable resistors.
4. Transistors are non-linear devices and are used in microwave mixing, modulation and detection.
5. Transistors are used for impedance transformation for transforming the output impedance to a much-reduced value.

6. Transistors are used in switching.
7. Transistors are widely used in the formation of logical blocks in the microprocessor industry.

2.5 MOS Scaling

Device scaling technologies are improving at a drastic rate from time to time. The dimensions of the vital parts of the transistors in the chip industry are shrinking continuously and the circuits are becoming more and more complex, accompanied by increase in number of transistors per chip. The main objective of the scaling is to improve the performance of transistors consistently, increase the frequency of operation and to decrease the rate of power dissipation. The process or methods in which the dimensional downsizing is achieved is known as scaling theory [5,6]. According to Moore's law, the number of transistors doubles every eighteen months. This can be seen in Figure 2.5. Also, the entire scaling laws can be summarized with a factor called 'K' as shown in Figure 2.6.

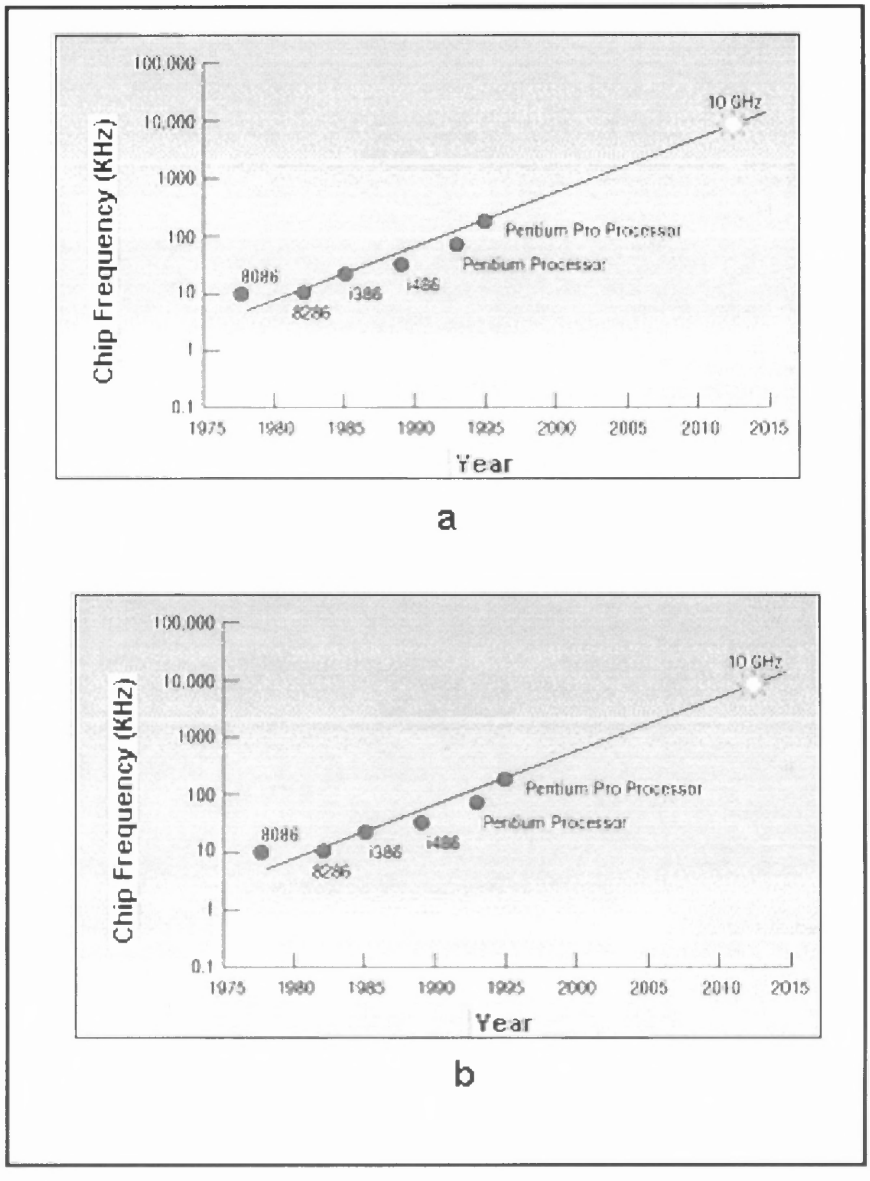

Figure 2.5 Moore's law projected out for 15 years a) Number of components per chip versus year and b) Chip frequency in KHz for transistors versus year [7].

The conventional scaling of MOS transistors includes junction depths, gate lengths, source/drain extensions and gate oxide thickness etc. However, there are many limitations associated with the above parameters. They are summarized in Table 2.1 along with the key scaling limits. In this chapter, some of the features are described in detail.

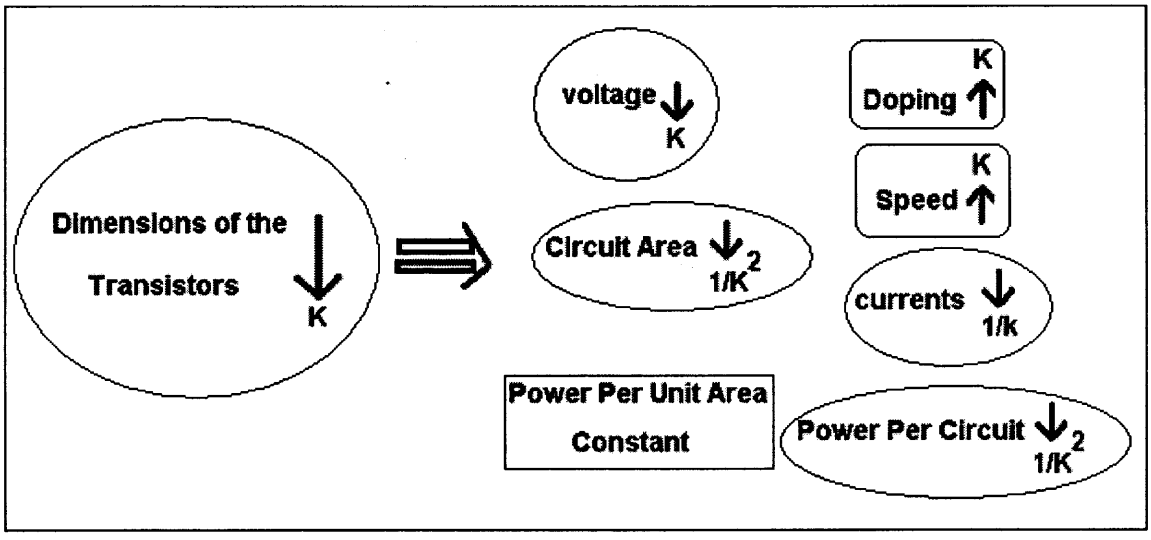

Figure 2.6 Scaling laws as a factor of 'K'.

Table 2.1 Key Scaling Limits [8]

Feature	Limit	Reason
Oxide Thickness	2.3 nm	Leakage (I_{GATE})
Junction Depth	30 nm	Resistance (R_{SDE})
Channel Doping	V_T = 0.25 V	Leakage (I_{OFF})
SDE under Diffusion	15 nm	Resistance (R_{INV})
Channel Length	0.06 μm	Leakage (I_{OFF})
Gate Length	0.10 μm	Leakage (I_{OFF})

2.5.1 Oxide Thickness

The gate oxide scaling plays an important role in controlling short channel effects. In order to maintain good gate control, the gate oxide thickness should be linear with respect to the channel length [8]. Figure 2.7 represents the plot between the channel length versus gate oxide thickness for Intel's process technology over the past 25 years and the points represent the technology development for every three years [8]. It is observed that the

channel length is 45 times the gate oxide thickness. The gate oxide thickness plays a vital role in tunneling of carriers. Direct tunneling occurs due to the decrease in the oxide thickness.

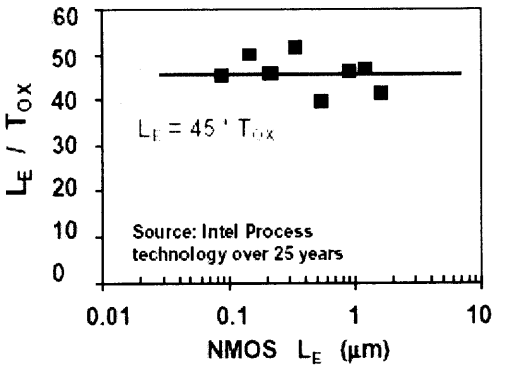

Figure 2.7 Channel length divided by gate oxide versus channel length [8].

2.5.2 Junction Depth

The following Table 2.2 gives the shallow Source Drain Extension (SDE) junction requirements based on the 2001 ITRS roadmap [9]. Shallow junctions are required while at the same time, the contact resistance should be low, sheet resistance should also be low and the junction depth should be deep enough for silicidation [10]. In Table 2.2, the blocks in white (no blocks) indicate that solutions exist, light gray blocks indicate that solutions are known and bold blocks indicate that solutions are not known. The sheet resistance (R_S), vertical junction depth (X_j) and lateral abruptness are given in Table 2.2 for each technology node. For the 45-65nm node, the sheet resistance is 760-830 Ω/□, the junction depth is around 7-15 nm and abruptness is 2.0-2.8 nm per decade. There are a number of results related to the junction depth and related parameters, which are explained in the 7th Chapter.

Table 2.2 ITRS Roadmap 2001 for Ultra Shallow Junctions [9]

Year of production	2001	2002	2003	2004	2005	2006	2007	2010	2013	2016
DRAM 1/2 pitch (nm)	130	115	100	90	80	70	65	45	32	22
MPU/ASIC 1/2 pitch (nm)	150	130	107	90	80	70	65	50	35	25
MPU gate length (nm)										
printed	90	75	65	53	45	40	35	25	18	13
physical	65	53	45	37	32	28	25	18	13	9
Equivalent physical oxide thickness for MPU/ASIC Tox (nm)	1.3-1.6	1.2-1.5	1.1-1.6	0.9-1.4	0.8-1.3	0.7-1.2	0.6-1.1	0.5-0.8	0.4-0.6	0.4-0.5
Gate electrode thickness (nm)	65-130	53-106	45-90	37-74	32-64	30-60	25-50	18-36	13-26	9-18
Profile control (side wall angle)	> 89	> 89	> 89	90	90	90	90	90	90	90
Drain exten. X_j (nm)	27-45	22-36	19-31	15-25				7-12	5-9	4-6
Max. drain extension R_s (PMOS) (Ω/sq)	400	460	550	660	770	830	760	830	940	1210
Extension lateral abruptness (nm/decade)	7.2	5.80	5.0	4.1	3.5	3.1	2.8	2.0	1.4	1.0

2.5.3 Threshold Voltage

Threshold voltage is one of the key parameters of a MOS transistor. It is symbolically represented as 'V_T'. The measure of threshold voltage is very important, as it serves as a valuable tool for monitoring the success of a fabrication process, due to its sensitivity to device geometry, doping and thickness of gate oxide. During the enhancement mode of a transistor, 'V_T' is very important as this is the minimum voltage that a device should be operated so that inversion layer is formed beneath the gate oxide [11]. Threshold voltage is also dependent on temperature, as many device applications require the device to operate at temperature other than the room temperature.

2.5.4 Contact Resistance

The contact resistance is given by Equation 2.1. Here, only metal-to-semiconductor contact resistance is defined [12].

$$R_c = \frac{\sqrt{\rho_c \rho_s}}{W} \coth\left| L_C \sqrt{\frac{\rho_s}{\rho_c}} \right| \tag{2.1}$$

where,

R_C = Contact resistance.

ρ_c = Contact resistivity.

ρ_s = Sheet resistance.

L_C = Length of metallization.

W = Width of the contact.

Summary

The Chapter above gives a basic introduction to transistors. The state of the art in process technology and MOS device scaling is dealt in a brief manner. The fundamental issues related to feature size, junction depth, gate oxide thickness etc., can be known for the present as well as for the future shrinking regime. The ITRS roadmap gives the overview of the scaling phenomena.

CHAPTER 3

SHALLOW JUNCTION PROCESS

The formation of shallow junctions has become an extremely critical step in the fabrication of MOSFETs. For a sub-micron CMOS transistor, there are two extreme features, one is the control of short channel effect (SCE) and the other is to have low sheet resistance. This can only be achieved by formation of shallow junctions in the MOSFET. Also, one of the important characteristic features of these devices is that they reduce junction leakage across the channel.

Shallow junctions or ultra shallow junctions are fabricated by many techniques such as, solid phase diffusion, epitaxial doping method, plasma doping method, laser annealing, thermal annealing etc. However, in shallow junction fabrication, ion implantation followed by rapid thermal annealing, are the conventional techniques used for better controllability, reproducibility and dopant uniformity. During implantation technique, the ions are bombarded onto the substrate with certain acceleration energies. To obtain lower or reduced projected distribution range, the energies should be low. In order to eschew thermal diffusion, sometimes, post annealing is done. High temperature annealing at a rapid rate i.e., rapid thermal annealing is preferred to achieve low sheet resistance [13].

3.1 Ion Implantation

This is one of the predominant methods used for introducing the dopant species into the semiconductor substrate, to a precise depth below the surface. The basic idea of doping

semiconductors by the bombardment of ions was first studied by William Shockley [14] in 1954 at Bell Laboratories. The basic concept in ion implantation is the bombardment of energetic species into the crystal lattice of the semiconductor surface. These energetic species have controllable concentrations of n-type and p-type dopants [15]. These energetic ions loose their energy by two processes, one is by undergoing elastic or nuclear collisions and the other by undergoing inelastic collisions or electronic collision processes [16].

Generally, semiconductors follow elastic collisions and cause lattice damage or disorder by direct displacement of atoms inside the crystal. In other words, whenever high energy ions enters into the crystal lattice, they knock off the target atoms located in the lattice position and thereby create a vacancies or interstitials or a combination of these defects also called Frenkel Pairs. These defects are mobile and are the cause for dynamic annealing and annihilation damage [17]. The damage caused depends on many parameters such as ion arrival rate, ion energies, target temperatures and collision details [18]. Finally, after ion implantation there can be substantial damage to the crystallinity due to collisions and is the cause for point defect formation. Also, the dopants introduced need to be electrically activated and transferred to substitutional sites during annealing treatment.

3.1.1 Merits and Demerits of Ion Implantation

Merits:

- Wide choice of Masking Materials.
- Doses can vary from short to long ranges ($10^{11} - 10^{16}$ /cm^2).

- Control of doses, profile depths and area uniformity is very accurate and precise.
- Effective for controlling the threshold voltage.
- Good reproducibility.
- Process cleanliness.

Demerits:

- Damage of crystallinity.
- Annealing of the damage created during implantation leads to transient enhanced diffusion (TED) [12]. Hence, difficulty in achieving shallow junctions.
- In some cases, the insulating layer also gets charged; in other words, this technique is prone to junction passivation.
- This technique needs very expensive and complicated equipment.

3.1.2 Typical Ion Implanter

A typical ion implanter is as shown in Figure 3.1 [19]. It consists of an ionization chamber, which is the source of ions to be implanted, an accelerator, for accelerating the ions electrostatically to higher energies, target compartment, where the material that desires implantation is placed for the impingement of ions. The amount of ions to be impinged onto the target is known as dose and is given as per the requirements. The amount of dose is controlled by the supply of current. Generally, this current is very small and is typically in microamperes. The depth profile of these ions relies on ion energies, ion species and also on the amount of dose. These ion energies may be from KeV to MeV ranges.

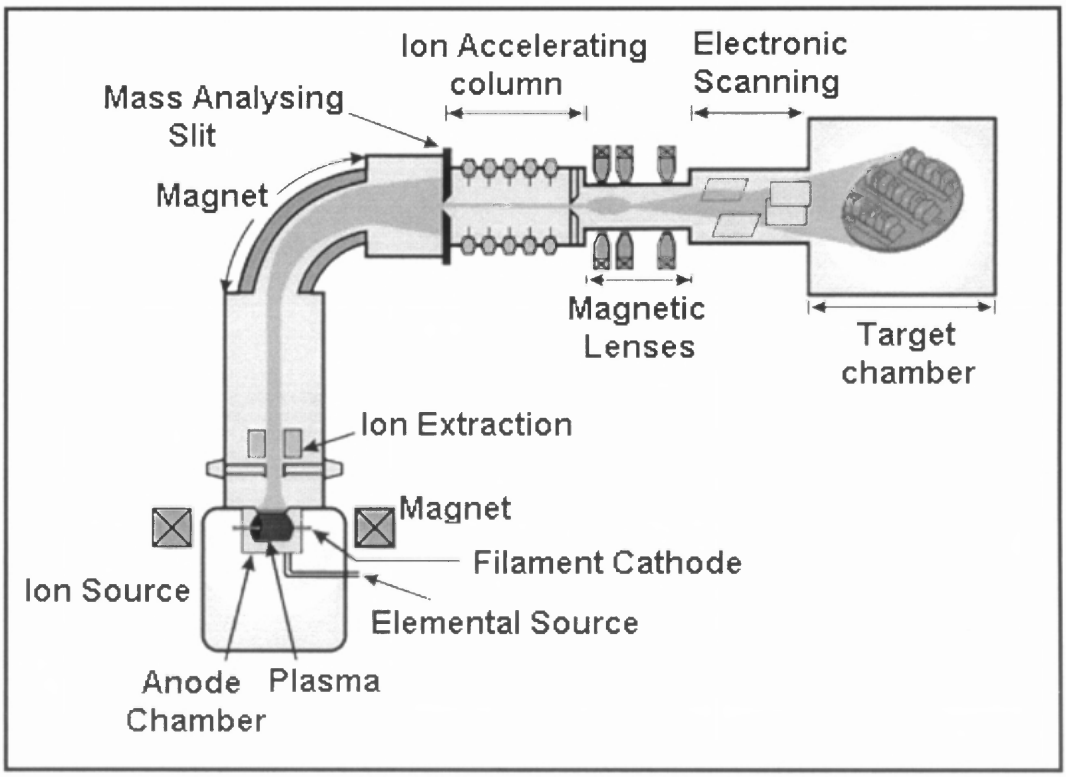

Figure 3.1 Typical ion implanter [19].

3.1.3 Process Parameters

Ion implantation parameters include the following:

- Range.
- Atomic mass of the dopant species.
- Implantation energies.
- Tilt and twist angle.

3.1.3.1 Range. The ion beam penetrates to a certain depth, depending upon the ion energies. Distance traveled by the ion in the solid is called range. The average penetration of the ions below the surface is called projected range [20]. Figure 3.2 shows the range and projected range of the ions.

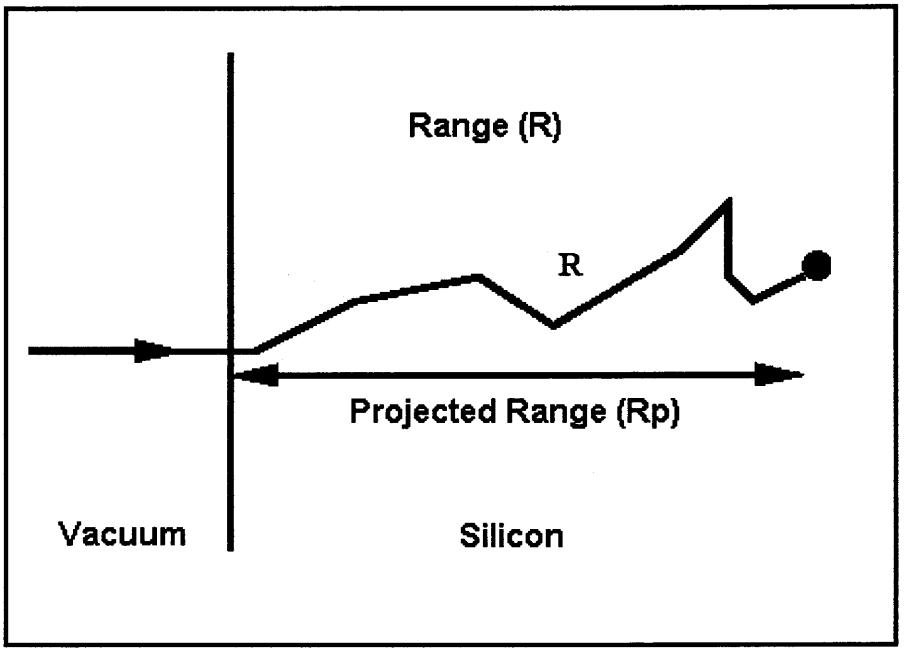

Figure 3.2 Schematic diagram of range and projected range of the ions [21].

Figure 3.3 shows the implant profiles of various dopant impurity species. Projected range (μm) is shown on the abscissa and concentration (cm^{-3}) is shown on the ordinate axis. These profiles are formed when the dopant ions are accelerated at 200 KeV implant energies. Out of antimony (Sb = 122amu), arsenic (As = 74amu), phosphorus (P = 31amu) and boron (B = 11amu), the heaviest is antimony and the lightest is boron. The peak of heavier ions is found to be much narrower than that compared to lighter ions. Antimony has the narrower peak and boron has the broader peak. Hence, much shallower depths can be obtained by implanting antimony ions. In generalized terms, it can be said that the heavier the ions, the shallower will be the depths obtained. It is also vital to mention that these ion profiles undergo approximately Gaussian distribution.

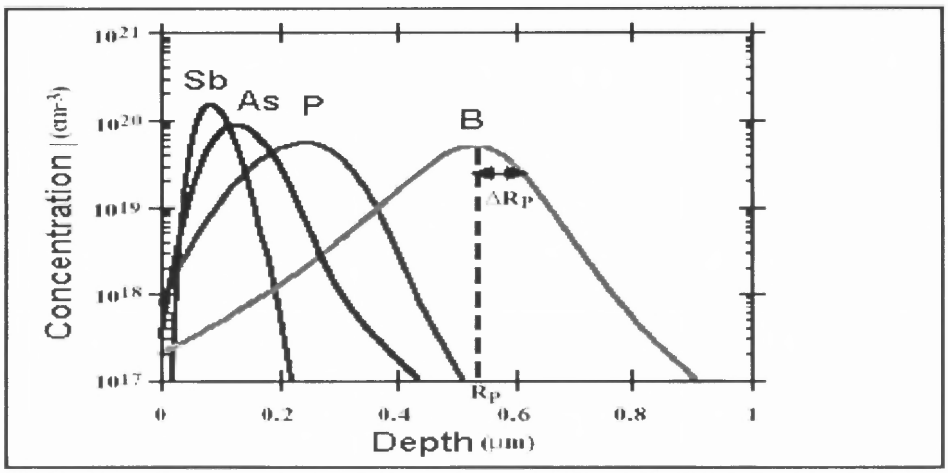

Figure 3.3 Concentration (cm^{-3}) vs. depth (μm) of various dopant species in Si [21].

3.1.3.2 Atomic Mass of the Dopant Species. In the current technology of semiconductors, many impurities can be doped based on the needs of applications in the industry. However, group III and group V elements are widely used, as the atomic radii of these atoms are closer to the group IV elements. The selection of the dopant elements also depends on the physical properties such as atomic mass and atomic number. If third group elements are used in the doping process, they are called p-type (positive) dopants, as there are insufficient number of electrons in the formation of bonding and thereby create holes in the bonding process. The most common p-type dopant species that are used are boron and indium. If the fifth group elements are introduced as dopants in silicon, then they are called n-type (negative) dopants. In this case, there is excess number of electrons available in the bonding process. The most common n-type dopants are phosphorus, arsenic and antimony. Also, sometimes for other applications, nitrogen implantation is done, as nitrogen influences the diffusion behavior of boron in polysilicon and SiO_2 [22].

3.1.3.3 Tilt and Twist Angles. Tilt and twist angles are very important, as they have direct effect on channeling. Channeling occurs when the ions are bombarded parallel to the crystallographic direction of the target material during ion implantation. Hence, in order to avoid the effect of channeling, the trajectory of the ions needs to be considered. The ions are therefore bombarded at an optimum angle to avoid channeling and twist of wafer is required to obtain uniform distribution of the ions. This optimum angle is also called the critical angle [23] of dopant (boron, phosphorus, arsenic) in silicon and is a function of energy. Typically, for large ions, the critical tilt angle is 7° off the wafer axis and the rotation or twist of the wafer is around 30° approximately [24].

3.1.3.4 Implant Energies. The implant energies mainly depend on the atomic species, dose and range needed to form a shallow junction. The typical energies include KeV to MeV range and most of the ion implanters use energies ranging from 30 KeV to 200 MeV range [21]. In some cases, the ion implantation can be done at lower energies by using doubly charged species. It is known that the higher the energies, the deeper will be the penetration of the ions. Figure 3.4 illustrates the dependence of the ion depth or trajectories on implantation energies. Also, lower depth profiles can be obtained with lower energies and high concentrations. In order to obtain higher depths, higher energies and low concentrations are required. This is illustrated in Fig 3.4. For example, for boron implantation into silicon, a depth of 0.6μm is obtained for implantation energy of 100 KeV.

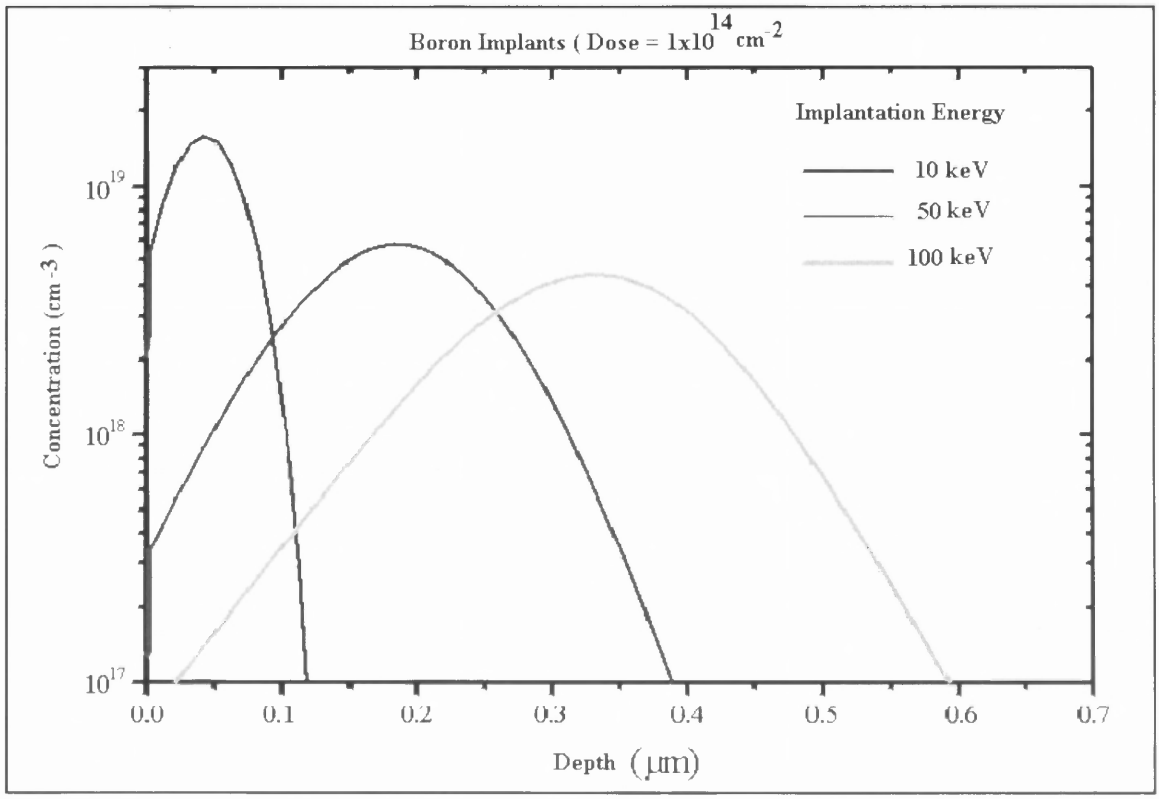

Figure 3.4 Concentration vs. depth for various implant energies of boron in Si [25].

3.2 Implantation Damage

Ion implantation induces lattice damage, i.e., loss of crystallinity of silicon. This is due to the collision effect of ions inside the substrate. These collisions can be of two types, nuclear and electronic. Only the nuclear collisions produce damage or disorder, as these collisions have enough energy to displace the silicon atoms from the lattice positions and the dopants introduced will not be present in the substitutional sites [26]. This energy is also called as displacement energy 'E_d' which forms a stable Frenkel pair. This energy is approximately equal to 15eV for a silicon atom [24]. Hence, in order to eliminate the residual damage and to electrically activate the dopant atoms into the substitutional sites, annealing is done. A typical annealing treatment, which reduces the damage and also

electrically activates the dopant atoms, includes heating to a temperature of 900 °C and for a time of 30 minutes. This simple method of heating to high temperature is also called Furnace Annealing. In order to meet the challenges for the formation of shallow junctions, diffusion of dopants should be controlled. Hence, other than the conventional form of annealing, the silicon samples after implantation are heated to a certain anneal temperature for a brief time period of ten seconds or may be less in some cases by a method called Rapid Thermal Processing (RTP) [2].

There are many types of annealing techniques such as, laser annealing, photo-assisted annealing and solid phase epitaxial annealing. It is important to note that in the 1960's, AT&T used horizontal annealing furnaces. A typical furnace of this kind consists of a furnace box, loading deck, heating elements, thermocouples etc. Today, these furnaces are rarely used by the silicon industry. Instead they are modified and replaced by vertical furnaces. The vertical furnace for rapid thermal processing is as shown in Figure 3.5 [27]. The wafer is placed inside the bell jar onto a horizontal base by means of an elevator. Then the wafer is heated in this bell jar with a vertical temperature gradient and the temperature is controlled by adjusting the elevator height [27]. For measuring the wafer radiance and temperature, pyrometers are used. These furnaces have better process control, particle performance and possess fully automated capabilities [26].

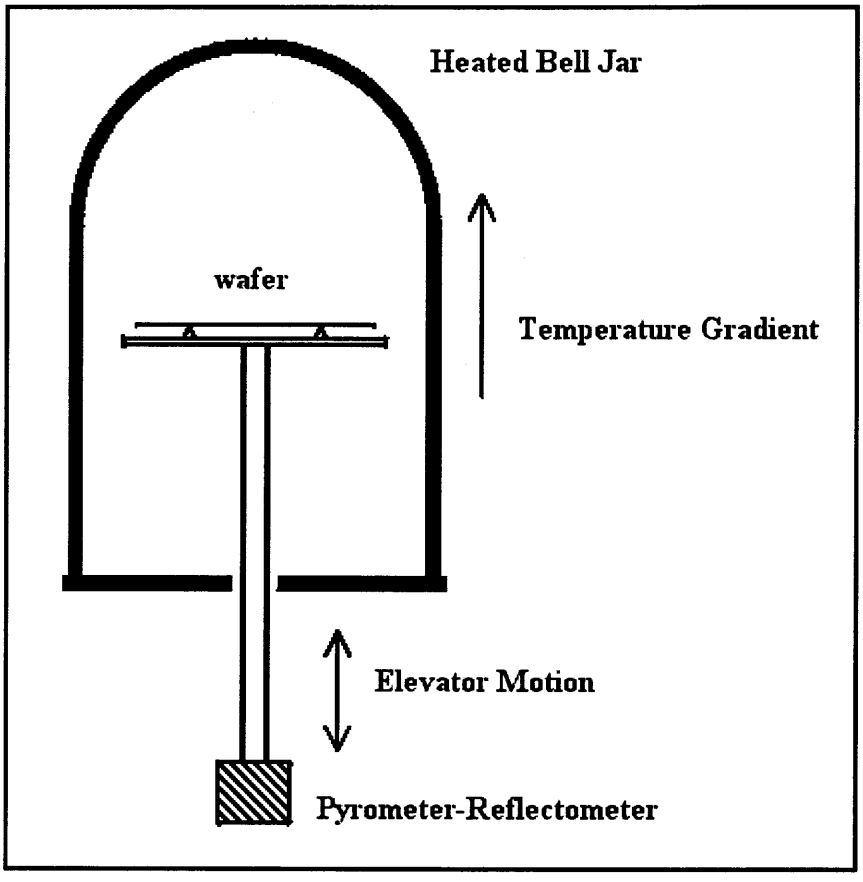

Figure 3.5 Typical Bell Jar furnace with vertical wafer movement [27].

3.3 Rapid Thermal Processing (RTP)

As the name suggests, Rapid Thermal Processing can be defined as fast heating and cooling of wafers. It can also be defined as cold wall and control ambient processing. An example of this type is shown in Figure 3.6. When compared to the conventional process, RTP is not done in thermal equilibrium with the surrounding environment [28]. Soak annealing, spike annealing, impulse annealing, flash annealing and laser annealing are the various types of RTP presently used in the industry. Soak annealing is the conventional RTP process where the samples are heated to a certain temperature and soaked for a period of time and then cooled.

3.3.1 Spike Annealing

In this type of annealing, the wafer is heated to a sudden high temperature and then cooled immediately. Heating of the wafers can be done by various methods i.e., by using arc lamps or by using incandescent lamps, etc., as shown in Figures 3.5 and 3.6. In case of heating by incandescent lamps, the lamps are arranged in the form of an array on both sides of the oven as shown in Figure 3.6(a). Pyrometers are used for measuring the temperature and emissivity of the wafers. As the wafer is surrounded by the heating filaments, the wafer gets heated uniformly by radiation [29,30]. The main aim of spike annealing is to avoid thermally activated diffusion while maintaining a certain temperature to achieve dopant activation.

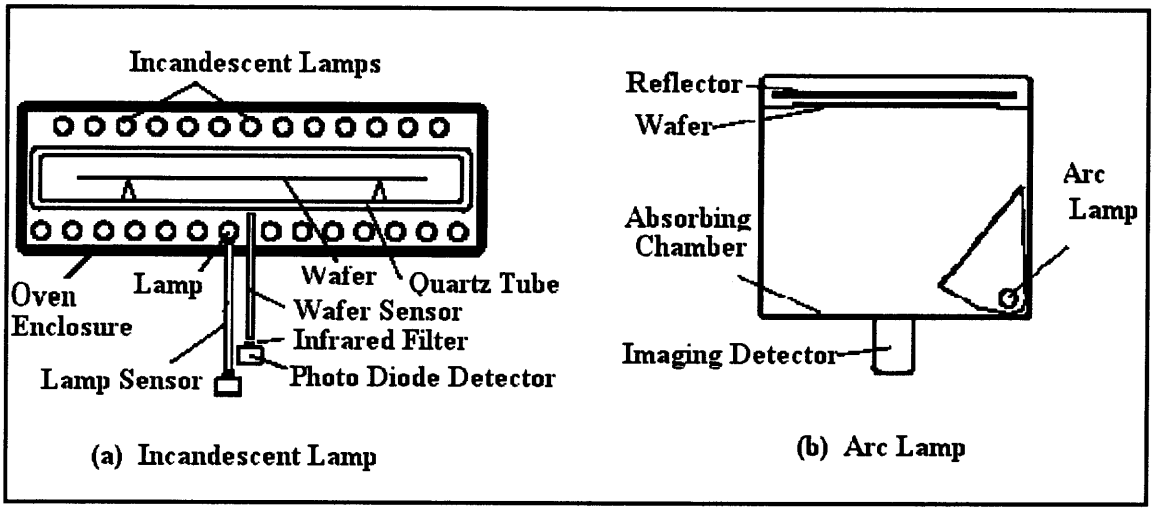

Figure 3.6 Spike annealing by (a) Incandescent lamps and (b) Arc lamp method [27].

During spike annealing, there should be minimal dwell time at peak temperature [31]. The effective annealing time and the sharpness of spike is illustrated in Figure 3.7. Figures 3.7(a) and (b) illustrate the actual time and the cumulative time at an activation

energy of 5eV for different spiking methods respectively. The effective annealing time taken by the arc lamp method is 0.27 sec, for dual incandescent method it is 0.86 sec, for furnace bell jar method it is 1.64 seconds and for the single incandescent method, the value is 1.75 seconds. The cumulative time for the arc lamp is very much less compared to the other spiking methods. Also the curves for the arc lamp spike annealing are sharp and narrow when compared with the other curves. Mathematical equations involved in spike annealing are as follows:

Activated process variable is given by,

$$r(t) = r_o \exp [-E_A / k\, T(t)] \tag{2.1}$$

Normalization prefactor is given by,

$$r_o = \exp [-E_A / k\, T_{MAX}] \tag{2.2}$$

Effective annealing time is given by,

$$t = \int dt' r_o \exp [-E_A / k\, T(t')] \tag{2.3}$$

where,

t' = Cumulative time in seconds,

E_A = Activation energy in electon-volts,

T = Temperature in °C,

T_{MAX} = Maximum temperature in °C.

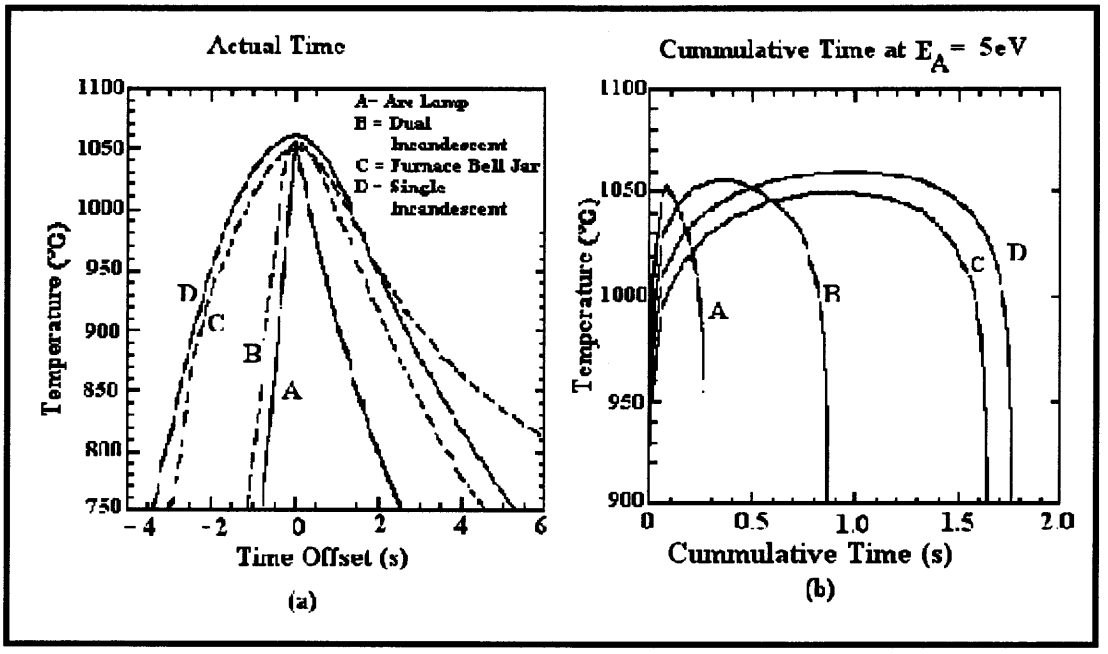

Figure 3.7 (a) Temperature versus actual time and (b) temperature versus cumulative time for various methods of spike annealing [32].

3.3.2 Impulse Annealing

This has been termed as a special case of conventional spike annealing using the arc lamp method [33]. In this method, the response time for heating is faster than the wafer [34]. When a graph is plotted between temperature and time for spike annealing and impulse annealing respectively, the peak of the impulse curve is pointed and the spike anneal curves are rounded as illustrated in Figure 3.8. Reduction in thermal budget is possible with this type of annealing. This process has been tested for its excellent repeatability and controllability of temperature.

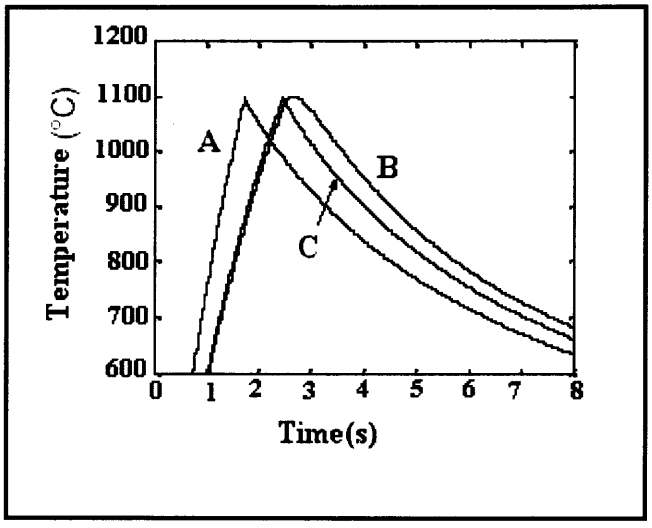

Figure 3.8 Temperature versus time (A and C are impulse annealed at 400 °C/sec and 250 °C/sec respectively and B is spike annealed) [34].

3.3.3 Flash Annealing

This is one of the most promising techniques for the formation of ultra shallow junctions. In this technique, the bulk of the wafer is heated to an intermediate temperature (T_i) and the device side of the wafer is heated to a higher temperature, by means of a flash or a pulse of intense light for a short time [35] as illustrated in Figure 3.9. Generally, this pulse of light will be of milliseconds duration [33]. The flash causes the thin layer to heat up to a high temperature. However, the bulk of the wafer is not at the same (high) temperature as that of the upper active layer. Thereby, it forms a heat sink. Thus, as soon as the flash lamp is turned off, the device layer starts cooling rapidly. The temperature of the bulk and the upper device layer are carefully selected so as to form a heat sink and will cause a rapid cooling of the device layer. Due to this, there will be a very high electrical activation with little or no dopant diffusion. The goal of the RTP is to increase the sharpness of the peak temperature profile and to decrease the effective time, and this can be achieved only by using lamps with low thermal mass. Thus, the technology of

using continuous arc lamps has been developed for heating the bulk of the wafer to a certain intermediate temperature. The radiation from the flash lamps are then incident on the thin layer of the device as an additional energy source. This is illustrated in Figure 3.9 [35]. Generally, the values of T_i are in the range of 600 – 800 °C and T_{MAX} are in the range of 1100 – 1350 °C.

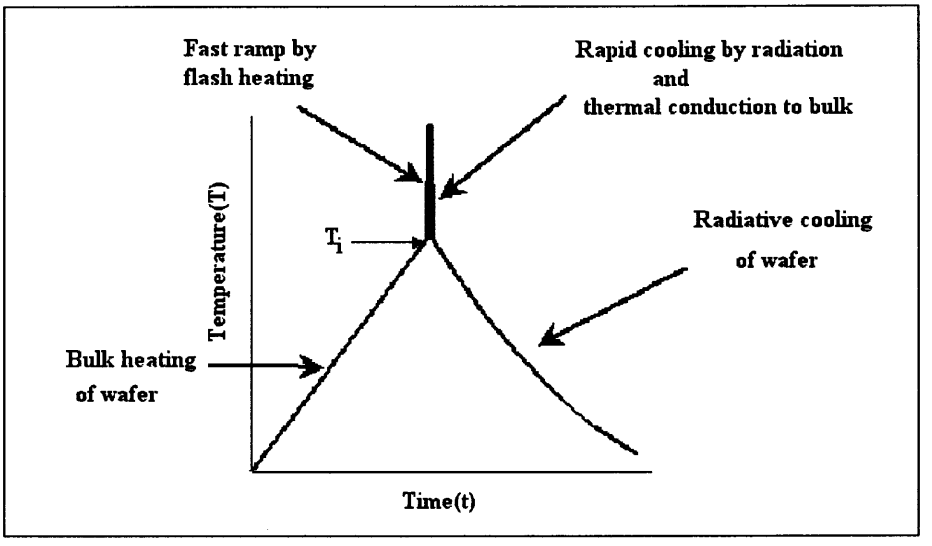

Figure 3.9 Illustration of the thermal profile during flash type of annealing for device layer formation [35].

3.3.4 Laser Annealing

Laser annealing, compared to that of conventional RTA techniques, offers much steeper profiles and high peak concentrations [36]. During this process, the surface layer of the wafer is heated, as the response time of heat source is faster than the wafer [33].

The comparison of all types of annealing is done in Figure 3.10. In the case of spike annealing, the thermal profile is more rounded and the wafer response is similar to the heat source. This type of annealing is currently used for production. The thermal profile is peaked in the case of impulse annealing and the heat source is faster than the

wafer and the bulk is at uniform temperature. The thermal profile is sharper in laser annealing when compared to all the other annealing techniques and the heat source has a higher response time than the wafer. The laser annealing method is considered to be an experimental technique for research purposes. In the case of flash assisted annealing, initially the bulk is heated and then after certain intermediate temperature, flash lamps are turned on so that the surface gets annealed. This technique is under development and many experiments are being done for improving this method.

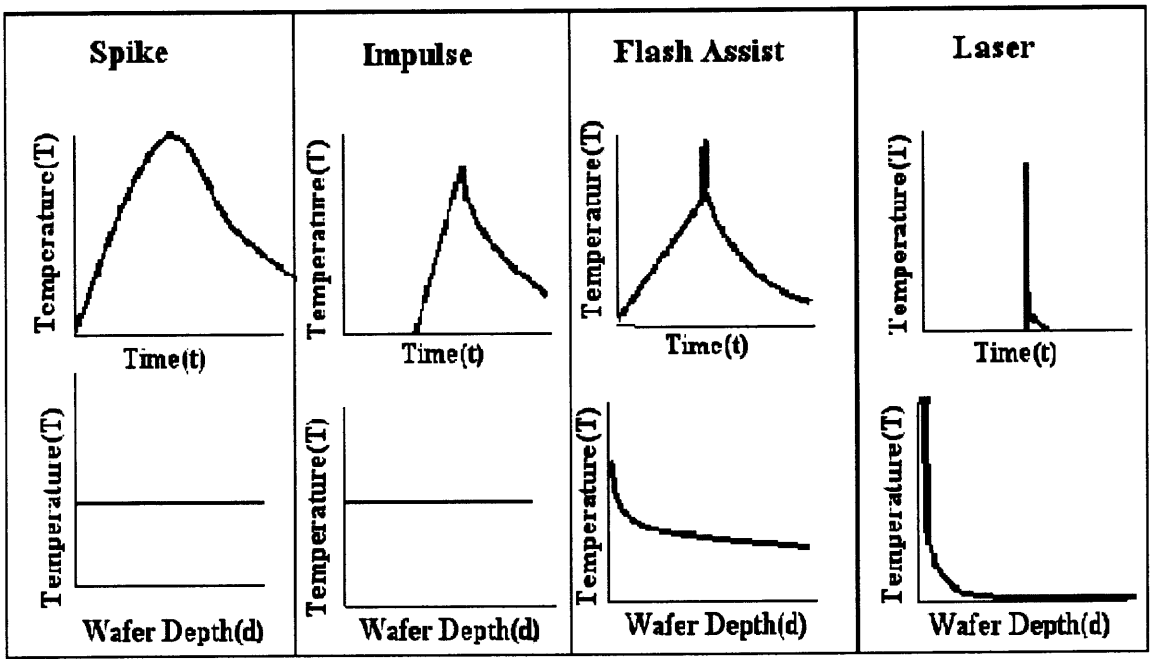

Figure 3.10 Illustration of the different temperature curves with respect to time and wafer depth for various annealing techniques[35].

3.3.5 Epitaxy

Epitaxy is the process of film growth over crystalline substrate in such a way that the atomic arrangement of the film bears a crystallographic relationship to the atomic arrangement of the substrate. Epitaxy is performed at temperatures below the melting

point of either the substrate or the film. Generally, the film thickness is approximately around 1-20μm thick [37]. Epitaxial growth is a successful approach for growing a wide range of materials, provided lattice constant and atomic spacing of the epitaxial layer and the substrate should be less than only few atomic percentage [38]. Epitaxial growth can be achieved by three techniques- vapor phase epitaxy, liquid phase epitaxy and solid phase epitaxy (SPE). As far as ion implantation and annealing are concerned, only SPE is discussed in the following section.

In this technique, regrowth of amorphous layers takes place at temperatures in the range of 500-600°C [26]. The regrowth process depends on several important parameters such as implanted species, orientation of the crystal and the annealing temperature. Figure 3.11 shows the regrowth processes occurring layer by layer and recrystallization continues until it reaches the surface. Usually, the process lasts only for a few minutes.

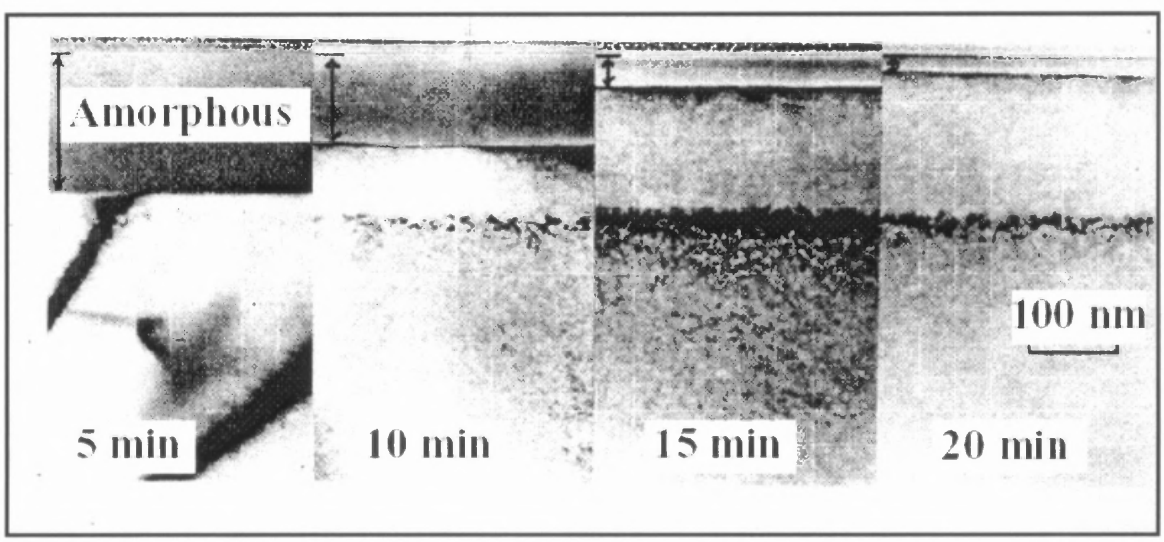

Figure 3.11 Transmission Electron Microscopy (TEM) micrograph, illustrating the solid phase regrowth at 525°C of a 200KeV, 6x 10^{15} / cm^2 antimony implantation [26].

Low temperatures are sufficient during SPE for electrical activation of amorphous layer, as the dopant impurities lie in substitutional sites. For regions that are beyond the

amorphous layer, they are subjected to higher temperatures for electrical activation. Hence, the optimum temperature must be chosen to be in between those corresponding to the formation of amorphous regions and crystalline damage region. Even though the crystalline defects beyond the amorphous layer can be eliminated during annealing, some of them form extended defects giving rise to defects such as dislocations and stacking faults.

3.4 Oxidation

In this process, silicon surface is made to react with oxygen to form a continuous layer of silicon dioxide (SiO_2). This layer of thin film of oxides can be used for many applications. These include:

(a) Isolation of devices from one another.

(b) Insulation between the metallization pattern interconnecting devices in the circuit.

(c) Use as a gate dielectric in MOS devices.

(d) Mask against implantation or diffusion.

(e) Passivation (passivation minimizes the electrical activity of the device surface and also serves as a protective layer against environmental contamination).

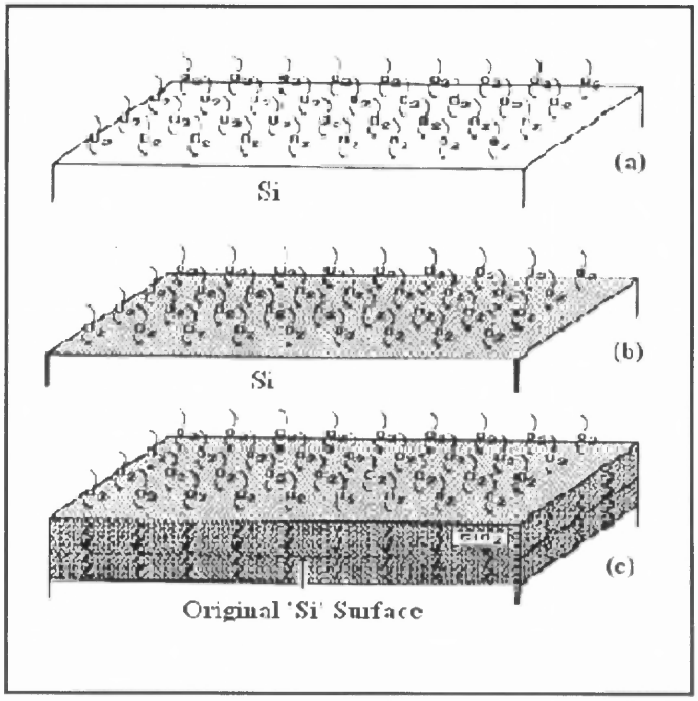

Figure 3.12 (a), (b) and (c) Indicates the step-by-step oxidation process [39].

The oxide films can be prepared at high temperatures under low or high pressures, in boiling water or in anodic solutions or by chemical vapor deposition method. Thermal oxides can be prepared by wet oxidation or dry oxidation method by utilizing a wide range of temperatures and pressures. Generally, the temperature ranges from 900 - 1000°C.

Figure 3.12 illustrates the thermal oxidation process. Initially, the silicon surface is exposed to the oxidizing atmosphere, as shown in Figure 3.12 (a). The oxidant diffuses through the silicon dioxide film to the silicon-silicon dioxide interface as shown in Figure 3.12 (b). Figure 3.12(c) represents the oxidant undergoing a chemical reaction between the surface of the silicon and the oxidant itself to form a silicon dioxide. In other words, oxidation occurs at the Si / SiO_2 interface, thereby, a new interface is formed constantly. During this step, part of the silicon substrate is consumed and hence, only inward diffusion of oxidant takes place rather than the outward diffusion of silicon [21].

Consequently, the oxidation part of the silicon surface is consumed. The oxidation rate can be controlled by the chemical reaction rate between the film of silicon dioxide and the underlying silicon substrate [39]. Sometimes, in IC manufacturing, only some part of the silicon surface may be needed to be oxidized rather than the entire wafer surface. For such applications, LOCOS (LOCal Oxidation of Silicon) is used.

3.5 Transient Enhanced Diffusion

During annealing, the dopants undergo enhanced diffusion because of excess silicon interstitials that exist in the silicon crystal. These interstitials are also formed due to residual implantation damage. This enhanced diffusion is present for a transient period until the damage is annealed out. Hence the name of this type of diffusion is called Transient Enhanced Diffusion (TED). This is also called as anomalous diffusion because of the diffusion behaviour of the profiles. In Figure 3.13, it is seen that the implant species of boron profiles that were annealed at low temperature diffuse more than the profiles that were annealed at high temperature. TED has become one of the dominant issues for producing shallow junctions. Essentially, reverse short channel effects can also be reduced by avoiding TED [21].

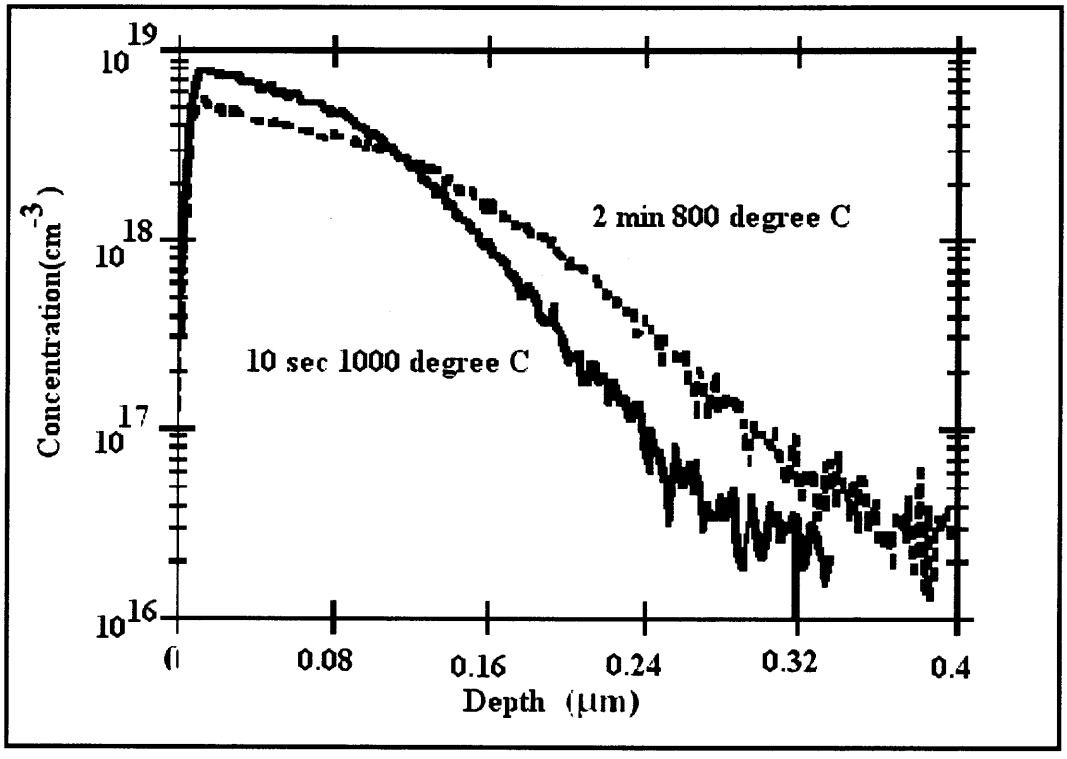

Figure 3.13 Diffusion profile of boron implants illustrating the TED effects [21].

TED depends on various process variables such as implant parameters (implant energies, dose, dose rate, annealing), evolution of point defects, annealing parameters (ramp up rates / thermal budget).

TED can thus be reduced or minimized by controlling the above factors. It is not possible here to describe in detail influence of all the process parameters on TED since it is beyond the scope of this thesis. Hence, only a few of them are considered. The role of annealing and implant variables is the principal consideration for reducing TED. Figure 3.14 illustrates the effect of ramp-up rates, time and temperature on the formation of shallow junctions by spike annealing. A Secondary Ion Mass Spectroscopy (SIMS) profile for 1 KeV boron implant spike annealed at a peak temperature of 1050°C with different ramp up rates of 75 / 150 / 230 °C/s and at a similar cooling rate is presented in

Fig. 3.14. The samples shown are pre-amorphized with germanium at a dose of 1 x 10^{15} /sq.cm and with an implant energy of 5 KeV.

From Figure 3.14, it can be inferred that the faster ramp-up rates will lead to the formation of ultra shallow junctions. For a concentration of 1 x 10^{18} cm^{-3} at a ramp up rate of 230°C/s, the junction depth is 400 Å. The junction depth for the same concentration and at a ramp-up rate of 75°C/s is found to be 500Å [40].

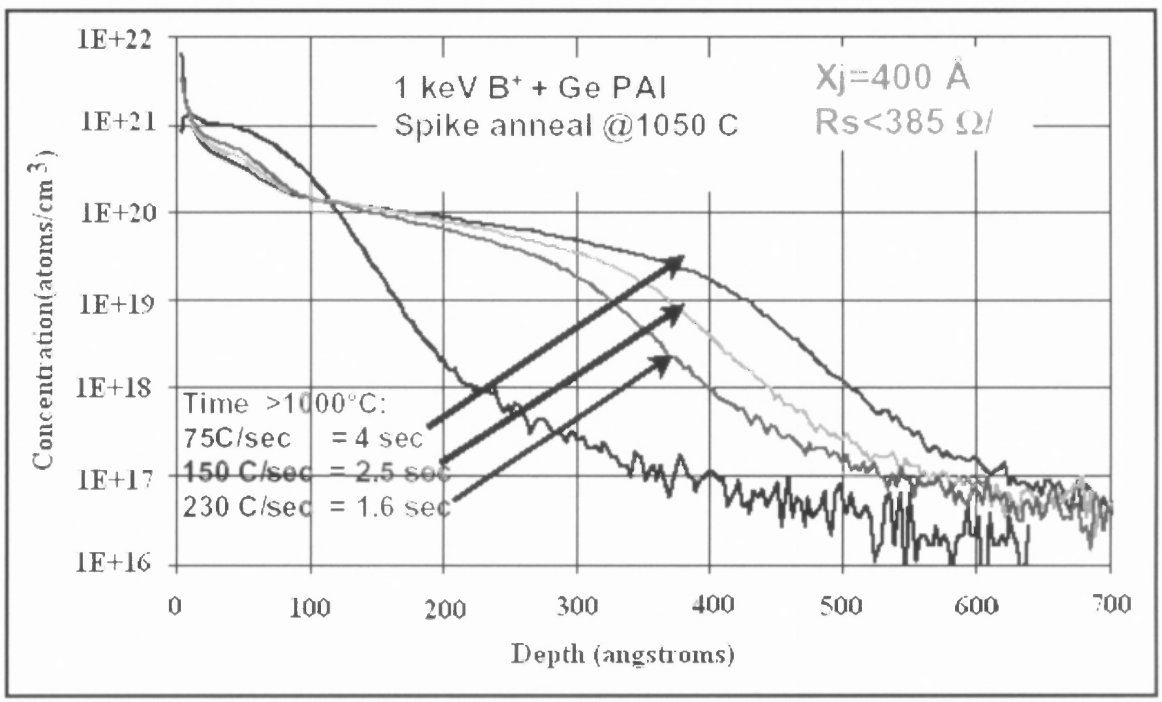

Figure 3.14 Impact of ramp-up rates on the formation of shallow junctions (PAI = pre amorphized implants, X_j = junction depth and R_S = sheet resistance) [40].

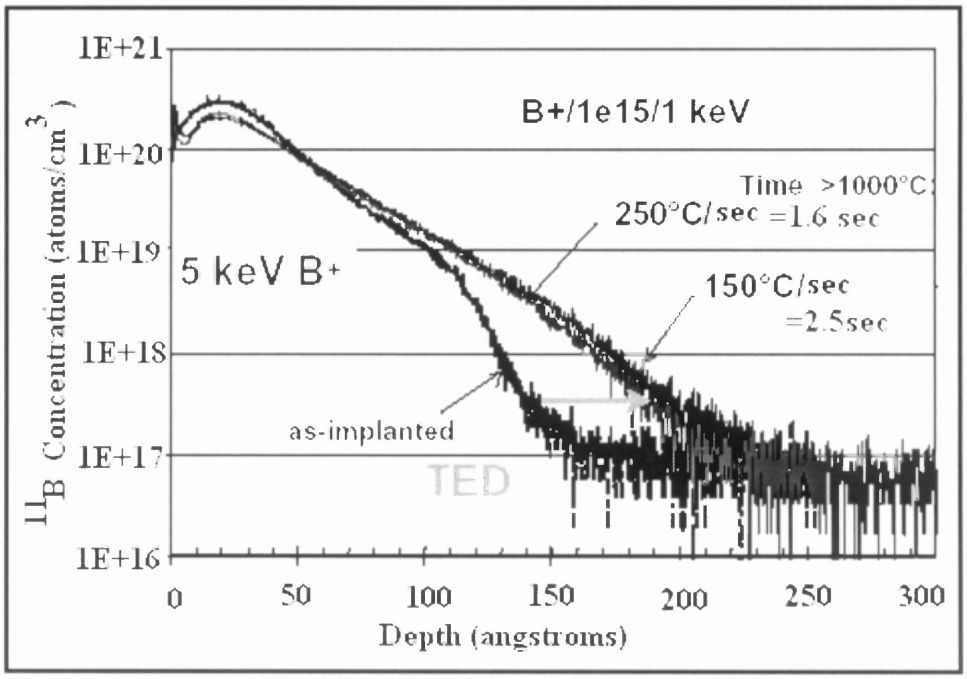

Figure 3.15 Diffusion profiles of high energy implants [40].

Figure 3.15 shows the effect of ramp-up rate and high-energy implants on junction depth. This is a SIMS profile of boron implants at a dose of 1 x 10^{15} /cm^2 at 5 KeV implant energy and annealed at two different ramp rates. These profiles were compared with that of the lower energy boron implants. The one with the faster ramp-up rate of 250°C/s had deeper junction depth compared to that of the 1 KeV profiles from Figure 3.14. This difference is due to the formation of TED at higher energies. This occurs due to the phenomena that, at higher energies, there are more interstitials and stable secondary defects. At lower energies, there are only few interstitials wherein, point defects suppress the occurrence of secondary defects during annealing and therefore, there is reduction in TED at lower energies [40].

3.6 Lattice Defects

Any deviation from an orderly array of lattice points can be termed as defect or imperfection. If the deviation lies in the localized vicinity of only few atoms, then it is called a point defect or point imperfection. The extension of this point defect through microscopic regions of the crystal leads to lattice imperfection [41].

3.6.1 Point Defects

Any non-silicon atom incorporated into the lattice at either a substitutional or interstitial site is called point defect. If only vacancies are present, then the defects are termed as Schottky defects and if there are vacancies and interstial sites, then these defects are called as Frenkel pairs or Frenkel defects.

Both vacancies and self-interstitials are present in crystalline silicon and these undergo self and impurity diffusion processes. This was studied by Seeger and Chikk in 1968 [26]. Furthermore, investigating the formation of these intrinsic point defects is done thermodynamically according to the Gibbs Free Energy (G_x) of the silicon material:

$$G_x = H_x - T.S_x \tag{3.1}$$

$$C_{I\,(eq)} = C_0.\ \mathrm{Exp}\ (-G_I / k.\ T) \tag{3.2}$$

$$C_{v\,(eq)} = C_o.\ \mathrm{Exp}\ (-G_v / k.\ T) \tag{3.3}$$

$$D_{self} = D_I + D_v = (\emptyset_I + 1).\ D_I.C_I/C_S + (\emptyset_v + 1).D_v.C_v / Cs \tag{3.4}$$

where,

x = I, V (I =interstitials and v= vaccancies),

D_{self} = Diffusivity of self interstitial mechanism,

D_I = Diffusivity of interstitials,

D_v = Diffisivity of vacancies and

$Ø_I$ and $Ø_v$ are the correlation factors of diffusion mechanisms involved in interstitial and vacancy mechanisms.

3.6.2 Extended Lattice Defects

These are also called as lattice imperfections and can be classified as follows:

- Line defects,
- Surface defects/Planar defects,
- Volume defects.

Line defects are two dimensional lattice imperfections where, the defect propagates in the form of lines in the crystallographic planes of a crystal. Line defects can also be called dislocations. Dislocations play a major role in the electrical and mechanical properties of semiconductors. The positive aspect of dislocation is that it acts as pores, absorbing the dopant atoms and through these pores, the dopants travel into the substrate. The disadvantage is that the dopants tend to segregate in these dislocations. Such impurity segregation leads to the formation of dangling bonds that severely affects the electrical activity of the devices [42]. The most common dislocations are edge dislocations and screw dislocations.

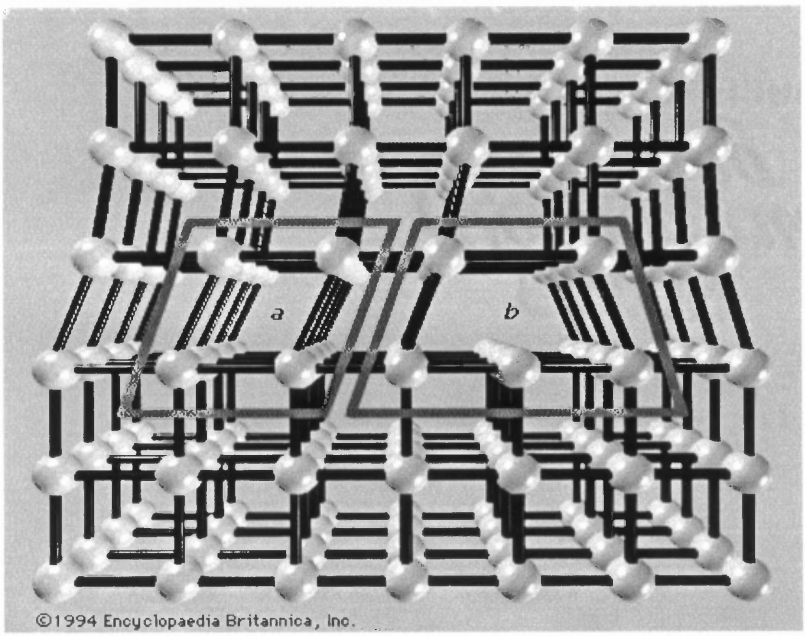

Figure 3.16 An example of an edge dislocation [43].

The presence of extra half plane of atoms either in the upper crystallographic plane or lower crystallographic plane is termed as edge dislocation. Figure 3.16 represents a negative edge dislocation as the extra half plane of atoms is in the lower plane. Similarly, if extra half planes of atoms are in the upper crystallographic plane, then it is termed as positive edge dislocation. These extra half plane of atoms form a dislocation line in 2-D. The movement of these dislocations takes place either by slip or by glide. Slip occurs in the direction of the dislocation meaning that the edge dislocation is parallel to the slip vector. In screw dislocations, the extra half plane of atoms is twisted by atomic spacing. There can also be positive and negative type of screw dislocations as in edge dislocations. The slip vector is perpendicular to the dislocation.

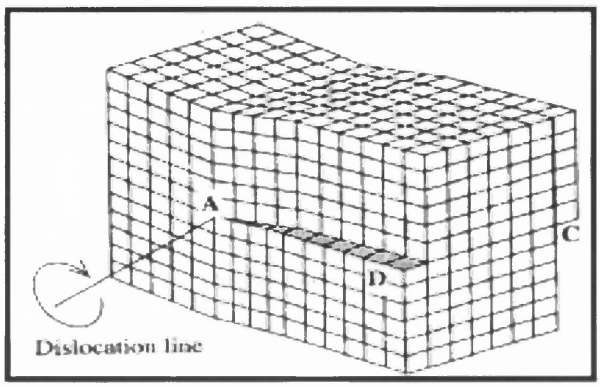

Figure 3.17 An example of a srew dslocation [44].

Planar defects include stacking faults and grain boundaries. Figure 3.18 illustrates the grain boundary defect and Figure 3.19 shows an example of a volume defect. Precipitates indicate the presence of volume defects. Vacancies, interstitials, stacking faults and dislocations in a crystal are also depicted in this figure.

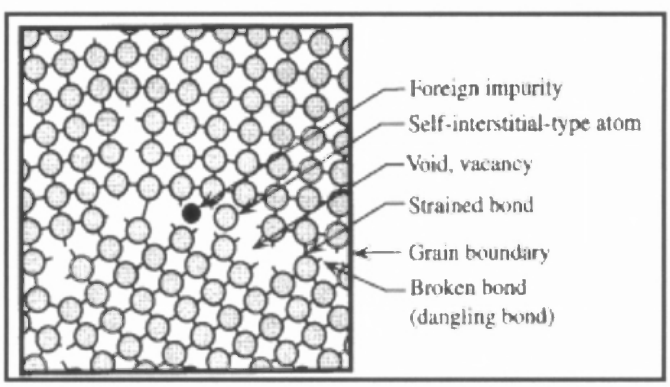

Figure 3.18 Illustration of grain boundary defects [44].

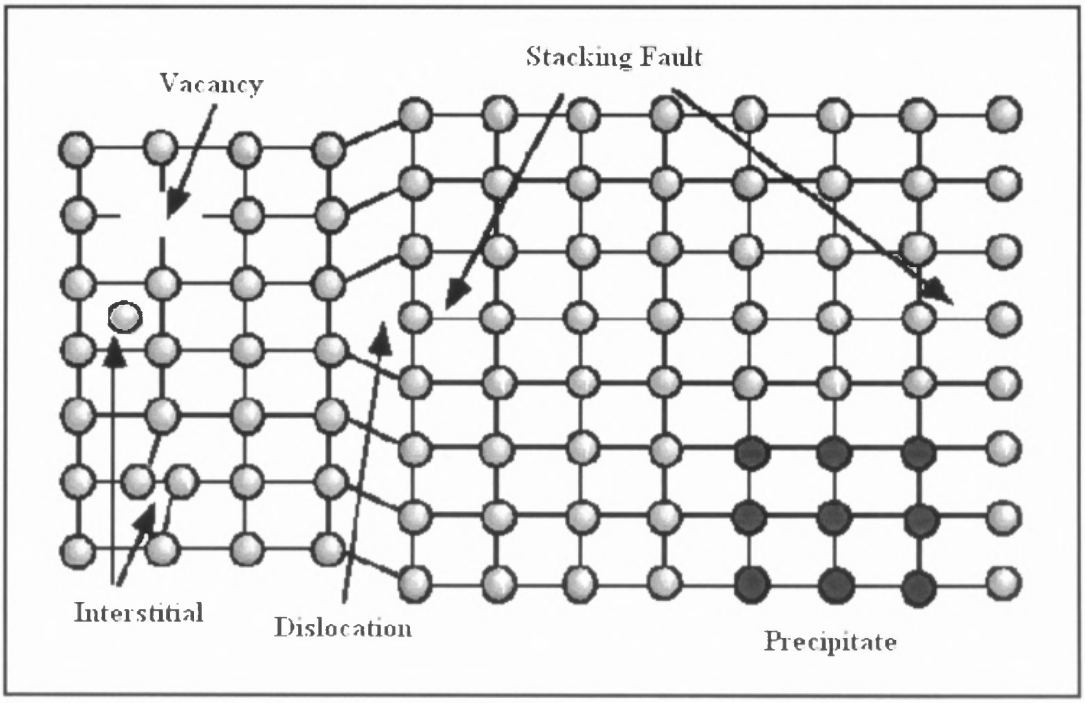

Figure 3.19 Various types of dislocations present in a crystal structure [21].

3.7 Diffusion

Diffusion is the oldest known method of introducing impurities in silicon. Basically, diffusion is the transport mechanism where the transport of mass or material takes place from one level to the next level because of the physical or chemical gradient existing between them. Alternately, diffusion is defined as the movement of dopant atoms in a semiconductor material because of the dopant gradient existing between the dopants and the semiconductor material [22]. There are mainly two kinds of defects that are associated with the diffusion mechanism. One is the native point defect and the other is the impurity related defect. Native point defects are present initially in pure silicon whereas, impurity related defects are created due to the introduction of third and fifth group elements into the crystal lattice of silicon [45].

Dopant diffusion may occur through a myriad number of mechanisms depending upon the atomic interactions between the dopant atoms and the silicon lattice. Among these mechanisms, the most important are interstitial mechanism and vacancy mechanism. Generally, diffusion takes place by interstitial mechanism for boron and phosphorous. For antimony, diffusion occurs by a vacancy mechanism and arsenic diffuses via both vacancy and interstitial mechanisms. These mechanisms are very much influenced by point defects.

Diffusivity of dopants is given by the following basic equation that is also known as Fick's Law:

$$D(T) = D_0 \exp(-E_a / k T) \tag{3.5}$$

where,

D_0 = Diffusion Constant,

E_a = Activation Energy,

k = Boltzmann Constant and

T = Temperature.

The activation energy is the energy in electron volts required to displace a crystalline atom by the impurity atom [46].

3.8 Thermal Budget

The amount of time, the wafer has been exposed to a particular temperature during the entire process is called as thermal budget. It can also be defined as the area under the time-temperature dependent curves or the time-diffusivity curves [47]. In order to meet the challenges of junction scaling, most of the silicon related industries are concentrating

on reduced thermal budget. For this, RTP of single wafers has taken over the lead from conventional batch type furnaces. The thermal budget processing is schematically shown in Figure 3.19. In this Figure, a comparison is made between the state-of-the-art RTP single wafer processing and conventional batch type furnace processing. In batch type furnaces, the wafers are exposed to high temperature for hours, while in single wafer processing, these wafers are subjected to very high temperatures only for seconds. It is very crucial to gain control of temperature across the wafers in the case of batch type furnaces, as subsequent thermal processing steps are required. Hence, for the formation of ultra shallow junctions, batch type furnaces do not match the thermal budget requirements and lead to poor device performance [48]. Thus, only using RTP, it has been possible to meet the challenges of forming ultra shallow junctions, with low leakage current, low power requirements and greater switching speeds [48].

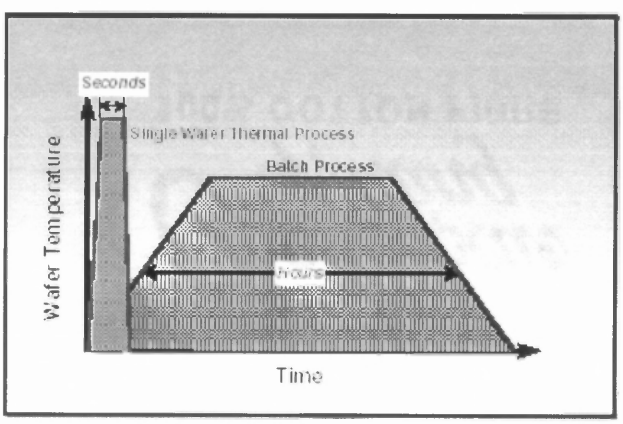

Figure 3.19 Thermal budget processing [48].

Mathematically, thermal budget can be expressed by referring to the following formula, where, the product 'Dt' is called the thermal budget [2]:

$$L = \sqrt{Dt} \tag{3.6}$$

D = diffusivity in the solid,

T = processing time and

L = diffusion length.

Summary

This chapter deals with processes for the formation of shallow junctions. Ion implantation, annealing, rapid thermal processing, transient enhanced diffusion, defects, diffusion and the reduction in thermal budget have been discussed. Thermal budget is one of the critical technical drivers for shallow junction performance.

CHAPTER 4

MATHEMATICAL MODELS OF ION IMPLANTATION

Implantation has become the primary process for introducing dopant atoms for formation of shallow junctions. Low implantation energies and low doses have been found to be practical for forming very shallow layers [49]. However, parameters such as implantation damage, annealing conditions or rapid thermal annealing and thermal budget need to be investigated. Process limitations and optimizations can be evaluated, for making the shallow junction fabrication more economical and viable. This will also lead to breakthroughs in models and simulation for shallow junction formation. The main objective of these models is to reduce the thermal budgets, the number of materials processing steps for process development and to bring down the manufacturing costs. Basically, models can be classified as low energy models, two and three-dimensional models and physically based models. Some of the current models include, Stopping Range of Ions in Matter (SRIM), Transport of Ions in Matter (TRIM) and Monte Carlo Simulation Models. These models are essentially function of implant parameters such as dose, energy, tilt and rotation angles. In this chapter, SRIM and TRIM has been discussed. These two models depend on the energy loss mechanisms [50] such as electronic and nuclear stopping powers.

4.1 Stopping Range of Ions in Matter (SRIM)

Basically, SRIM works on the principle of the theory of ion stopping using a quantum mechanical treatment of ion-atom collisions [51]. According to this theory, whenever an

ion collides with a solid target, it transfers its energy by two types of collisions. One is known as electronic collision and the other is known as nuclear collision. This also depends on the type of energetic ions used for implantation. If the mass of the ions are light (for example, H^+ and He^{++} and B^+) and when they are impinged on to the substrate with high energy ($\geq$ KeV range), then these ions will be stopped by means of electronic stopping. If the mass of the ions are heavier (for example, As^+) and are bombarded on to the target material at low energy ($\leq$ KeV range), then they undergo nuclear collisions or nuclear stopping. This is illustrated in the Figure 4.1 [21].

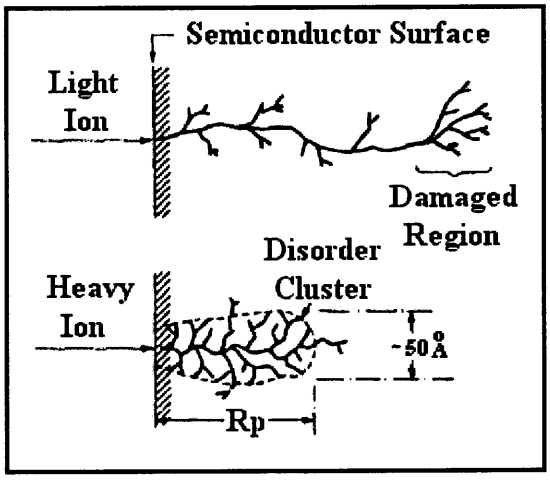

Figure 4.1 Implantation of ions into the semiconductor surface [21].

In the case of nuclear stopping, the ions collide with the lattice ions, thereby displacing the lattice ion and create either a vacancy or an interstitial. This is characterized by an energy loss per unit length and is mathematically represented as '$S_n(E)$'[21]. Similarly, the implanted ion also looses its energy due to the excitation (emission of electrons to a higher state) and this energy loss per unit length due to electronic stopping is mathematically represented as '$S_e(E)$'. These mechanisms of

collisions are as shown in Figure 4.2. As a matter of fact, only nuclear collisions tend to damage the crystallinity. The total energy loss per unit length, dE / dx, is given by the sum of the nuclear and electronic losses:

$$\frac{dE}{dx} = -N (S_n + S_e) \qquad (4.1)$$

where,

E = Energy of the ion at any point along the trajectory,

x = Length,

N = Density of the target atoms per unit volume,

S_n = Energy loss due to nuclear collision and

S_e = Energy loss due to electronic collision.

Range 'R' of the projectile is given by:

$$R = \int_0^R dx = 1/N \int_0^{E0} dE / Sn(E) + Se(E) \qquad (4.2)$$

The coulomb scattering potential 'V(r)' is given by the following formula for the nuclear stopping power [21]:

$$V(r) = \frac{Q^2 Z_1 Z_2}{4\pi\varepsilon r} \exp(-r / a) \qquad (4.3)$$

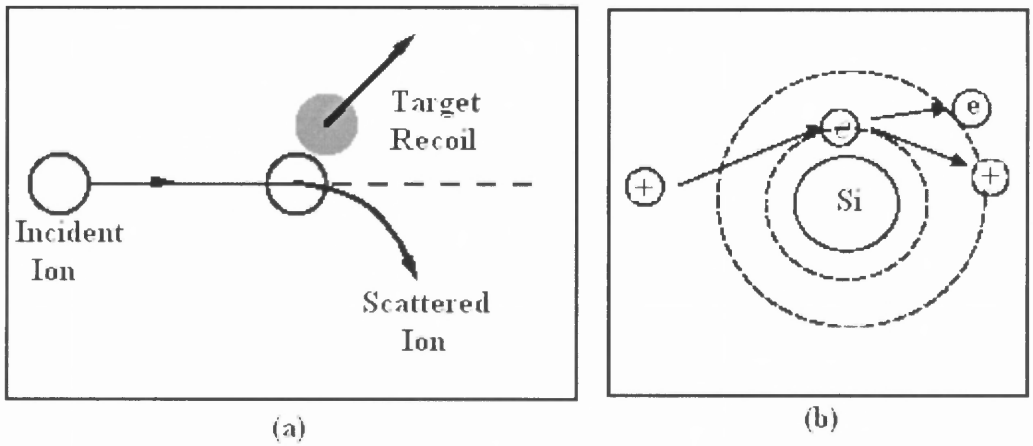

Figure 4.2 (a) Nuclear collisions of ions and (b) Electronic collision of ions [21].

From equation 4.2, the term Sn(E) can be approximated as:

$$S_n(E) = 2.8 \times 10^{-15} \frac{Z_1 Z_2}{(Z_1^{2/3} + Z_2^{2/3})^{1/2}} \frac{m}{(m_1+m_2)} \text{ eV} - \text{cm}^2 \qquad (4.4)$$

where,

Z_1, m_1 = atomic number and mass of the ion,

Z_2, m_2 = atomic number and mass of the substrate.

Similarly, the electronic stopping power is considered to be analogous to that of stopping a projectile in a viscous medium [27] and is directly proportional to the square root of energy.

$$S_e(E) = eV_{ion} = kE^{1/2} \qquad (4.5)$$

where,

k = proportionality constant and depends weakly on the atomic masses, number of ions and target atoms and is approximately equal to 0.2×10^{-15} $eV^{1/2}$ cm^2.

Table 4.1 Critical Energy Corresponding to Stopping Power of Various Ions [21]

Impurity atom	E_1 keV	E_2 keV
B into Si	3	17
P into Si	17	140
As into Si	73	800

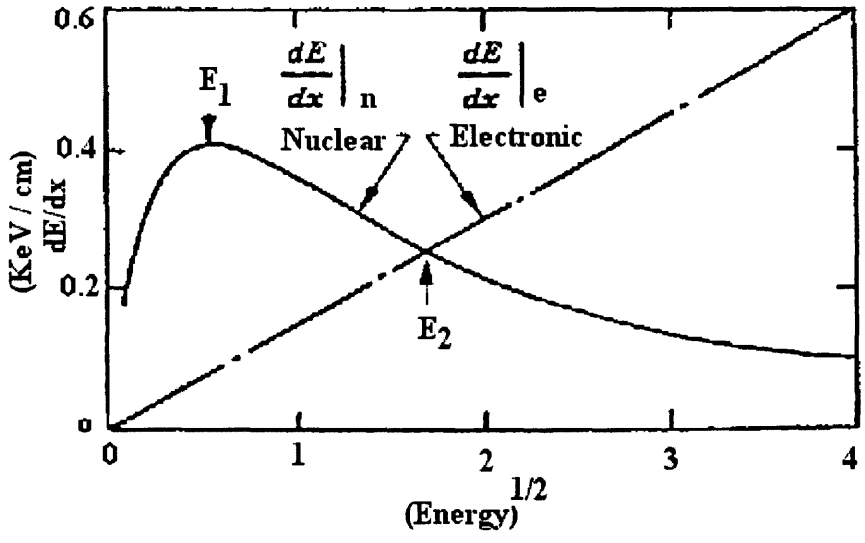

Figure 4.3 Rate of energy loss dE/dx vs. $(\text{Energy})^{1/2}$ [21].

The total stopping power of the various ions are given in the form of a graph in Figure 4.4. The critical energy where the nuclear and electronic stopping powers are equal is approximately known. For (a) boron, it is equal to 3 KeV, (b) phosphorus, it is equal to 140 KeV and (c) both arsenic and antimony, the critical energy should be more than 500 KeV approximately [21]. This is shown in Figure 4.3 and is summarized in Table 4.1.

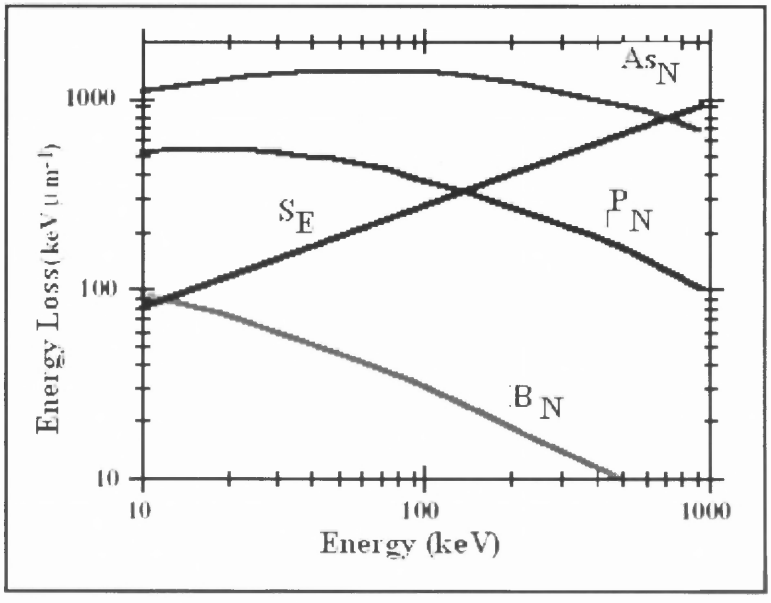

Figure 4.4 Total stopping powers of various ions vs. energy [21].

4.2 Transport of Ions in Matter (TRIM)

TRIM is an ion implant simulator and is also a part of the SRIM program software. This simulator can be used for any complex targets and is limited only for amorphous materials, as there is difficulty in predicting the channeling effects. The dose and angles for the implant profiles cannot be predicted accurately by this method [52]. An early version of TRIM used an interpolation approach by means of universal potential model. Currently, the latest version, SRIM 2000 and TRIM 2000, uses the pair-specific universal potential model [53]. With the advent of this approach, even though species change, the change in the interpolation process can be calculated progressively for that species [52].

4.3 Rutherford Universal Manipulation Package (RUMP)

This software is used for the analysis of Rutherford Back Scattering (RBS) and Electron Recoil Detection (ERD). Historically, RUMP was converted from FORTRAN into a 'C' language and thus, this package became one of the most powerful simulation packages [53] for calculating the stopping powers for all elements in a given energy range. The calculations used for the stopping powers are based on the polynomial representation and the principle of Bragg's Law. These polynomial fits are compared with those of the analytical models to get a fair optimization of the energy ranges. As these computation tools are expensive, the optimization is performed only once for each ion-target pair. Recently, Chu, Mayer and Nicolet implemented a sixth-order polynomial fit for representing the stopping power [53]. These calculations were simple and yet improved the fit precision by extending the energy range. For example, in the case of silicon, the tables for stopping power extended from 0.18MeV to 3.45MeV range and the maximum deviation decreased to a value of 0.24 percent [52]. It is an interesting phenomena that both RBS and ERD data analyses are to be performed separately with specific stopping power tables for each. The tables are automatically loaded during the simulation runs. The following Figure 4.5 shows a measured RBS spectrum (thick line) and the RUMP simulations are indicated by the dashed line. The sample is a silicon wafer which was first deposited with diamond like carbon (DLC) by using a CVD technique and then a thin amorphous silicon film was deposited by Molecular Beam Epitaxy (MBE) at room temperature [54]. The thickness of the DLC is 310Å or 1.55×10^{17} Si atoms/sq.cm. [54].

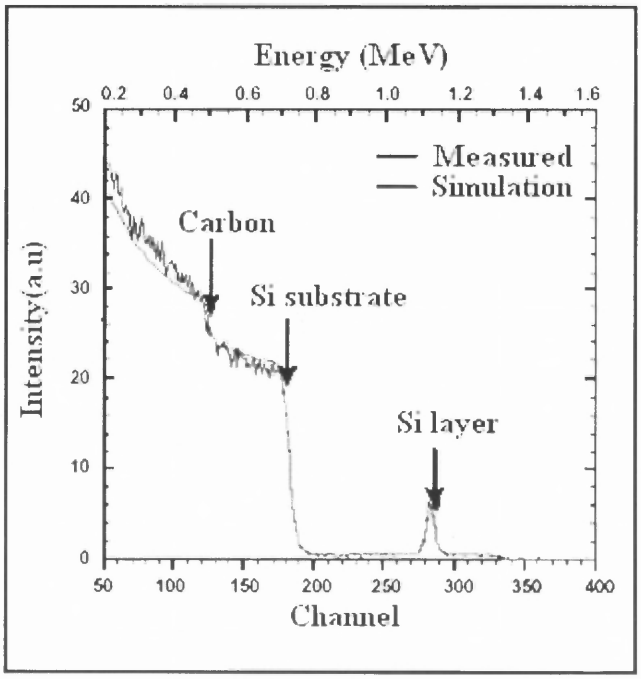

Figure 4.5 RUMP Simulation and the RBS spectra for Si/DLC/Si sample [54].

Summary

This chapter presents the current status of simulations used in the IC industry for range and stopping power of the ions during ion implantation. SRIM and TRIM have been discussed in detail and RUMP has been mentioned with a brief overview. It is also compared with RBS data for a typical sample that has been prepared with diamond and silicon layers.

CHAPTER 5

CHARACTERIZATION TECHNIQUES

Semiconductors form the backbone of today's microelectronic devices. Characterization is one of the key issues to be considered for the advancement of this technology. From the material characterization techniques, topographical properties, defects, structural properties, compositional properties and luminescent properties of the material can be known. There are several characterization techniques that are available depending upon the applications in manufacturing and process development. The detailed list of material and device characterization techniques can be mainly classified into three types namely, optical characterization, electrical characterization and physical/chemical characterization. These techniques have been summarized in Table 5.1. Physical/chemical characterization techniques provide visual and structural data, compositional and defect parameters etc. Some of these techniques also provide information in two as well as in three-dimension [55]. The main asset of this technique is that the impurities can be clearly discerned by the characteristic energies and wavelengths [55]. Optical characterization techniques are used for measuring layer thickness, physical dimensions, impurity concentrations, optical properties, defect identification etc. For device diagnostics, electrical characterization is the most widely used method. This method is used for measuring the resistivity, mobility, contact resistance, channel length, carrier concentration, barrier height, junction depth, leakage current, lifetime etc. Only a few of the techniques have been discussed in this chapter.

Table 5.1 Different Types of Characterization Techniques

Physical, Chemical and Compositional technique	**Optical Characterization**	**Electrical Characterization**
Scanning Tunneling Microscopy (STM).	Optical Microscopy.	Current- Voltage Technique.
Atomic Force Microscopy (AFM).	Ellipsometry.	Capacitance-Voltage Technique.
Ballistic Electron Emission Microscopy (BEEM).	Near Field Scanning Optical Microscopy (NSOM).	Spectral Responsivity.
Chemical Force Microscopy (CFM).	Optical Microscopy.	Hall Effect.
Scanning Chemical Potential Microscopy (SCPM).	Raman Spectroscopy.	Deep Level Transient Spectroscopy.
Interfacial force Microscopy (IFM).		Van der Pauw's Method
Magnetic Resonance Force Microscopy (MRFM).	Scanning Tunneling. Optical Microscopy.	Scanning Resistance Profilometry (SRP).
Nano Nuclear Magnetic Resonance (Nano-NMR).	Raman Spectroscopy.	Four-Point Probe Method.
Scanning Capacitance Microscopy (SCM).		Scanning Resistance Technique (SRT).
Scanning Ion Conductance Microscopy (SICM).	Fourier Transform Infrared (FTIR).	Reverse Bias Diode Leakage.
Scanning Thermal Microscopy (SThM).		Carrier Lifetime.
STOM: Scanning Tunneling Optical Microscopy		
Nano- Spreading Resistance Profilomety (Nano-SRP).		
Acoustic Microscopy.		
X-ray Photoelectric Spectroscopy (XPS).		
X-ray Diffractometry.		
Scanning Chemical Potential Microscopy (SCPM).		
Secondary Ion Mass Spectroscopy (SIMS).		
Rutherford Back Scattering (RBS).		

Some of the characterization techniques described are as follows:

- Four Point Probe Method.
- Van der Pauw Method.
- Hall Effect Measurements.
- Deep Level Transient Spectroscopy (DLTS).
- Secondary Ion Mass Spectroscopy (SIMS).
- Rutherford Back Scattering (RBS).
- Scanning Electron Microscopy (SEM).
- Spreading Resistance Profilometry.
- Capacitance – Voltage (C-V) Measurements.
- Reverse Bias Diode Leakage Measurements.

Before describing the above characterization techniques, it is necessary to show the device parameters that can be obtained to examine by these measurement techniques. Figure 5.1 shows a MOSFET with some of the important device parameters.

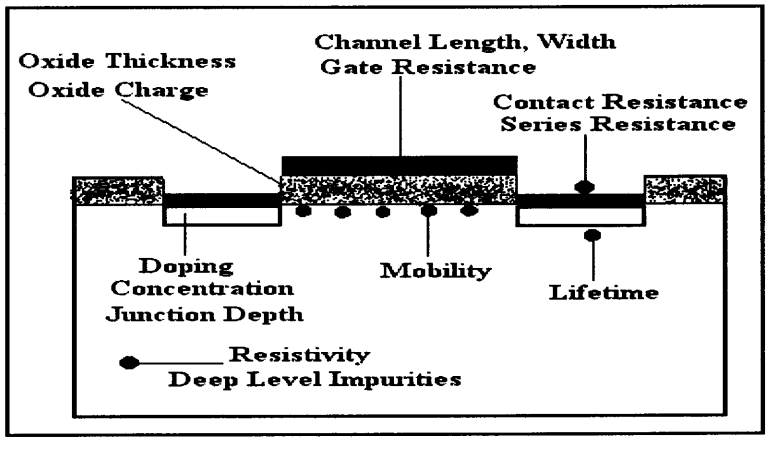

Figure 5.1 MOSFET with various device parameters [55].

5.1 Four-Point Probe Method

This is one of the most dominant methods for measuring the reisistivity of a semiconductor. A simple two-point probe method can be used for measuring the resistivity, where one probe acts as a current probe and the other acts as a voltage probe. Mathematically, the total resistance is given by:

$$R_T = V / I = 2 R_C + R_{SP} + R_S, \qquad 5.1$$

where,

R_C = Contact Resistance,

R_{SP} = Spreading Resistance,

And R_S = Semiconductor Sheet Resistance.

The main drawback of this method is that the 'R_C' and 'R_{SP}' cannot be measured accurately, hence R_S is also not accurate. Therefore, a four-point probe method is best suited for measuring the sheet resistance. Figure 5.2 shows the alignment of probes in a four-point probe method.

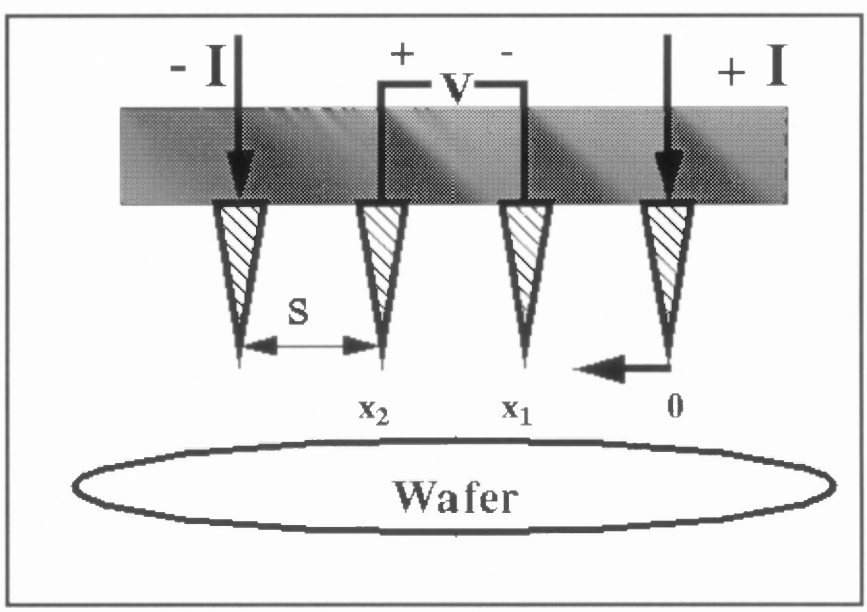

Figure 5.2 Arrangement of probes in a four-point probe method [56].

In the four-point probe method, the outermost electrodes are used for current injection and current collection. The innermost electrodes are used for measuring the voltage drop. One of the important aspects of four-point probe method is that measurement errors due to contact resistance between the electrodes and the surface can be eliminated [57]. Resistivity of any semiconductor material can be measured by this method. This method is also used for measuring the conductivity of the wafer by using the rectification principle. The mathematical expression for the resistivity is shown below.

For a bulk sample, (t >> s), the resitivity is given by the following formula:

$$\rho = \frac{2\pi s V}{I} \tag{5.2}$$

For a thin sheet, (t<<s), the resistivity is given by:

$$\rho = \frac{\pi t}{\ln 2} \times \frac{V}{I} \tag{5.3}$$

$$= 4.532\, t\, (V/I) \tag{5.4}$$

$$= 4.532\, (V/I)\ \text{Ohms}/\square \tag{5.5}$$

where,

t = sample thickness and s = probe spacing.

5.2 Van der Pauw Method

This method measures the sheet resistance (R_S) for the sheets of actual boundary shapes. As the samples may not always be square or rectangular, the probe arrangement, in Fig. 5.3, is the good option for measurements. The most common geometry is of the square

pattern and is illustrated in Figure 5.3 (a). Other patterns such as Greek Cross and Cloverleaf are illustrated in Figures 5.3 (b) and (c) respectively. One of the advantages of this technique is that the arbitrary shaped samples can be used and the contact of the probes should be present at the perimeter of the sample [58].

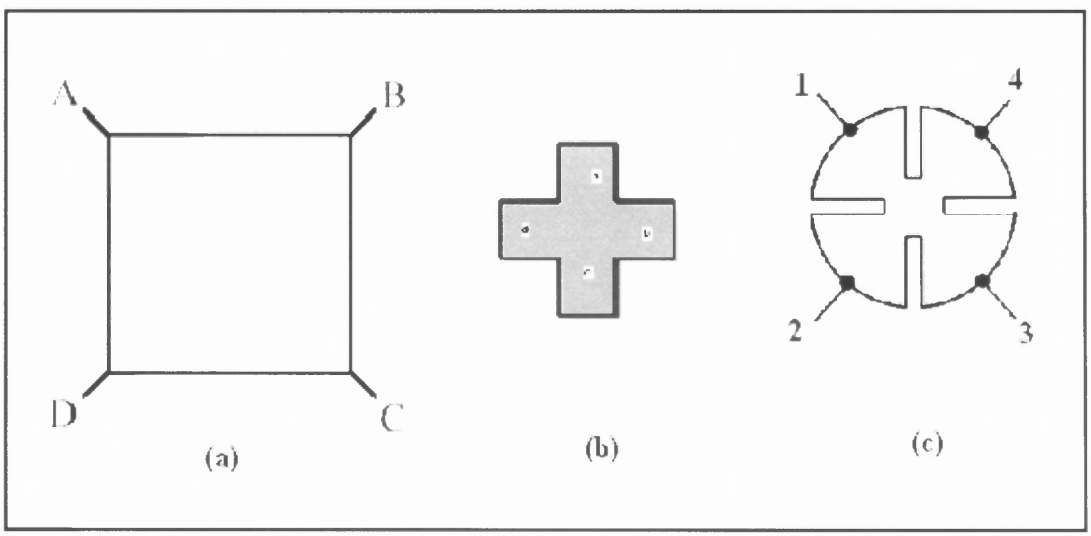

Figure 5.3 Van der Pauw's patterns (a)Square Pattern (b)Greek Cross (c)Cloverleaf [56].

According to van der Pauw, the following relation exists between the resistivity, voltage and thickness:

$$\exp(-\pi R_{AB,CD}\, d/\rho) + \exp(-\pi R_{BC,DA}\, d/\rho) = 1 \qquad (5.6)$$

where,

$R_{AB,CD}$ = potential difference $V_D - V_C$ / Current from A to B,

$R_{BC,DA}$ = potential difference $V_A - V_D$ / Current from B to C,

d = thickness of the sample and ρ = resistivity.

($R_S = \rho / d$), is obtained by solving the transcendental Equation 5.6.

5.3 Hall Effect Measurements

Hall Effect is the technique for deriving useful semiconductor properties like carrier type in p or n-type materials, majority carrier concentration, majority carrier mobility, Hall voltage and Hall coefficient. Hall effect works on the principle of Lorentz force. "When an electron moves in the direction perpendicular to the applied magnetic field, it experiences a force acting normal to both the directions and moves in the direction of the force."[59]. Figure 5.4 represents an n-type semiconductor with majority carriers, electrons, of bulk density 'n' and constant current 'I ' flowing from left to right and excess charge is created on the side of the sample thereby resulting in Hall voltage (V_H).

$$V_H = IB / q\, n\, d, \tag{5.7}$$

where,

I = Current,

B = Magnetic Field,

d = Sample thickness and

q = Free carrier charge

The sheet density is given by:

$$n_S = n\, d, \tag{5.8}$$

$$n_S = I\, B / q\, |V_H|, \tag{5.9}$$

The Hall mobility is given by:

$$\mu = |V_H| / R_S IB = 1 / (q\, n_S R_S), \tag{5.10}$$

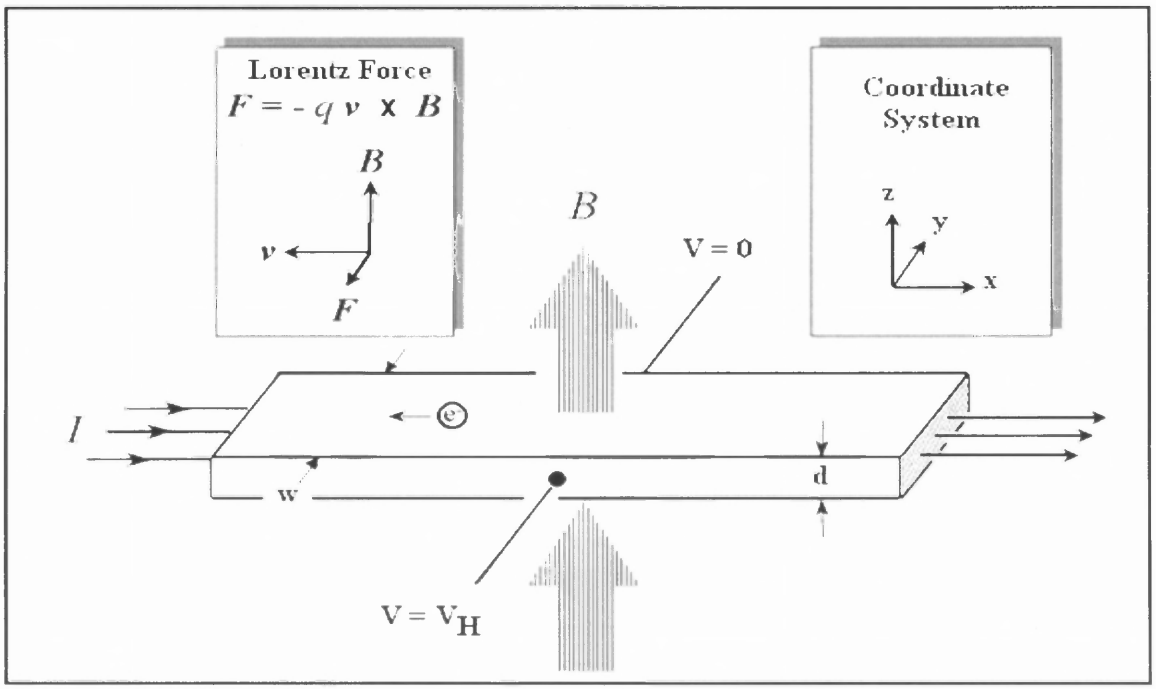

Figure 5.4 Schematic diagram of the Hall effect and Lorentz force [59].

5.4 Deep Level Transient Spectroscopy (DLTS)

This method is used for detecting electrically active defects in semiconductors. It serves as an important tool in the characterization of defects at deep levels. Impurities and defects of concentrations up to 10^{11} cm^{-3}[60] can be detected utilizing this technique. The principle of this method is that deep levels emit charge carriers during the forward bias pulse and the capacitance change is observed on reverse biasing. The emitted carriers are truly related to temperature and thus the activation energy of a deep level can be observed. Figure 5.5 represents the DLTS pulse scheme and voltage signal. DLTS is a non-destructive technique unlike SIMS and Auger Electron Spectroscopy. It is used in determining the energy levels, capture/emission rates and concentration of deep states [60].

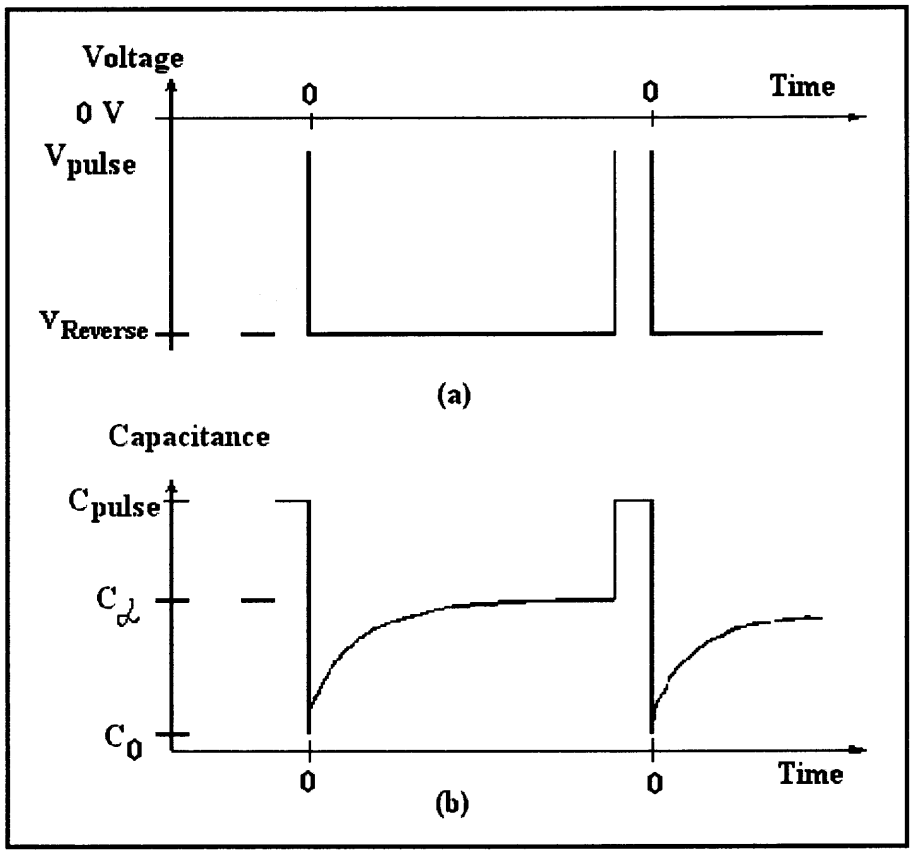

Figure 5.5 Standard DLTS (a) Pulse (b) Voltage signal [61].

5.5 Secondary Ion Mass Spectroscopy (SIMS)

SIMS is widely used in detecting dopants and impurities within a junction. This technique is used by ion implanters for determining the dose and shape of the dopant profile [57]. This technique is dependent on the application of sputtering phenomena. The incident ions with high energies are bombarded onto the surface, and thereby, transfer some of the energies into the lattice atoms. These incident ions are also called as primary ions and they interact with the sample or surface that is to be measured. Initially, the upper layer of the sample gets amorphized and some of the ions get implanted due to atomic collisions within the solid, thus releasing some of the secondary ions which can be analyzed mass spectrometrically. Figure 5.6 represents the basic principle of this

technique [62]. The secondary ions are characteristic functions of the composition of the surface. This method is a high sensitivity surface analytical technique and the typical detection limits range from 10^{14} to 10^{15} cm^{-3}. The lateral resolution range limits are from 1 μm to 100 μm and depth resolution ranges from 50 Å to 100 Å [57]. Figure 5.7 gives the detailed flowchart of SIMS operation.

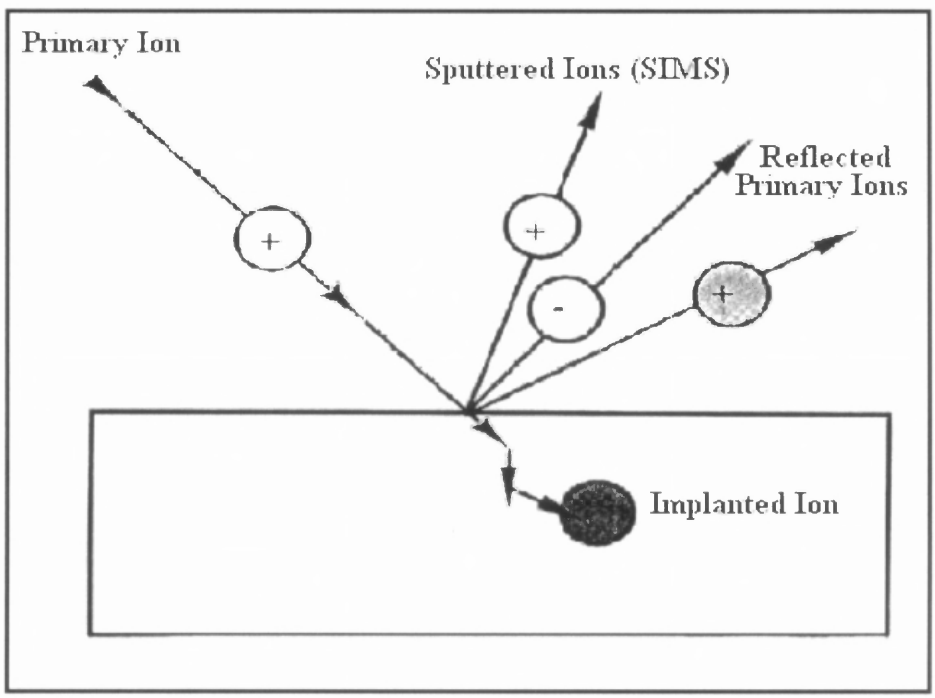

Figure 5.6 Principle of operation of SIMS [62].

SIMS can be used for almost any element in the periodic table except for noble gases because of the difficulty in ionization. One of the main advantages of SIMS is that it has high spatial resolution and can be used for all semiconductors. Also, as it measures the dopant profiles and not the carrier profile, it can be used for the implanted samples prior to activation anneals [57].

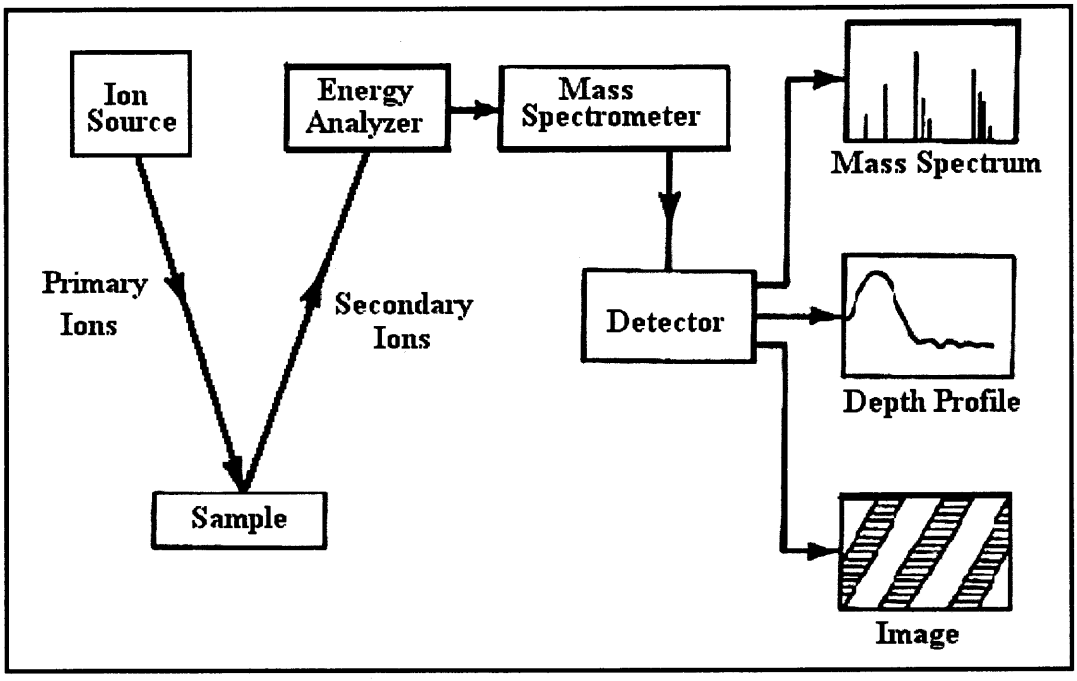

Figure 5.7 Flowchart explaining the SIMS technique [62].

5.5.1 Merits and Demerits of SIMS

Merits

- This can be used for wide range of materials including organic, inorganic compounds, ceramics, polymers, biological samples, solid state materials etc.
- The sensitivity of this analysis is very high and range from ppm to ppb.
- SIMS has the ability to distinguish isotopes.
- High spatial resolution.

Demerits

- This is a destructive technique.
- The equipment is highly complex.
- The sensitivity is more for boron in silicon than for the rest of the impurities.

5.6 Rutherford Back Scattering (RBS)

Lord Ernest Rutherford first introduced this technique in 1911. This is the most widely used technique in the semiconductor industry for surface analysis. This is because the scattered ions come out from the surface as well as from the inner or sub regions. This technique works on the simple principle of backscattering of ions from a solid surface. Beams of high energetic ions are incident on the solid surface and these energetic ions elastically collide with the lattice atoms. Some ions are absorbed and some of them are back scattered into a suitable detector, which measures the number of back-scattered particles and their energy [63]. Typically He+ or He++ monoenergetic ions is used as the incident beam (1-3MeV) as this passes very close to the nucleus of an atom in the solid and they are back-scattered through a large angle and leave the target [57].

The back scattering of the ions mainly depends on the mass of the target element. If the target atoms are heavy, then the back-scattering energy will be high almost close to the incident energy [64]. If the target atoms are light, then the energy back scattered is very low. Hence they need to be scattered in the forward direction. Typical examples include hydrogen. The thickness of RBS in terms of density is given by the following formula:

$$T_{RBS} \cdot D_{RBS} = (\text{atom} / \text{cm}^2) = T_{Real} \cdot D_{Real} \qquad (5.11)$$

where,

T_{RBS} = thickness obtained by RBS,

D_{RBS} = Density assumed during the calculation of RBS thickness,

T_{Real} = actual film thickness and D_{Real} = actual density.

This is useful when the density assumed is different from the actual density of the film [65]. The RBS spectrum for the Si/ DLC / Si is given in Figure 4.5 in chapter four.

5.6.1 Merits and Demerits of RBS

Merits

- This technique is widely used for measuring the thickness, nature, amount and distribution of impurities in thin films [57].
- RBS associated with channeling is used for locating the impurity atom position in a single crystal [63].
- The primary use of this technique is in the quantitative depth profiling of semiconductors, polymers, catalysts, superconductors etc.
- Good reproducibility.

Demerits

- It has limited sensitivity.
- Cost of equipment is high.

5.7 Scanning Electron Microscopy (SEM)

This is the primary tool used as an analytical technique. With the demand for increasing performance and for practical applications in the VLSI era, SEM has become the standard instrument because of its high resolution. In principle, a high-energy electron beam is focused on to the surface of a sample. This electron beam interacts with the surface of the sample and creates a variety of signals (secondary electrons, X-rays, photons, back-scattered electrons, internal currents, etc.). These signals are scanned so as to form an image on the screen. The image formed is highly magnified. The present state of the art

SEM has a magnification in the range of 20x – 650000x [66] and the resolution of the image is found to be in the order of 1-3nm [67]. Figure 5.8 represents a schematic drawing of a SEM. An electron gun is used for producing electrons, which pass through several lenses. The electrons are then accelerated so as to optimize the electro-optical performance of the lens and also to enhance the brightness of the electron source. Generally, the accelerating voltages are in the range of 15-30kV [68]. When the electron passes through the electrostatic lenses, it is focused like a spot on the surface of the specimen. As the electron strikes the sample, it undergoes multiple collisions and produces images from the signals such as cathode-luminescence, electron beam induced conductivity, specimen current, auger electrons, fluorescent X-rays, backscattered electrons, etc. [68].

Most of the SEM tools produce images based on the back-scattered electrons. These signals are detected by means of detectors and the characteristic of these detectors play a vital role in the contrast of the image. The distance traversed by some of the incident electrons that do not backscatter and come to rest is called Range (R). The electron range is a factor of the atomic number and incident beam energy. The range increases with decrease in atomic number and increase in the incident beam energy [69].

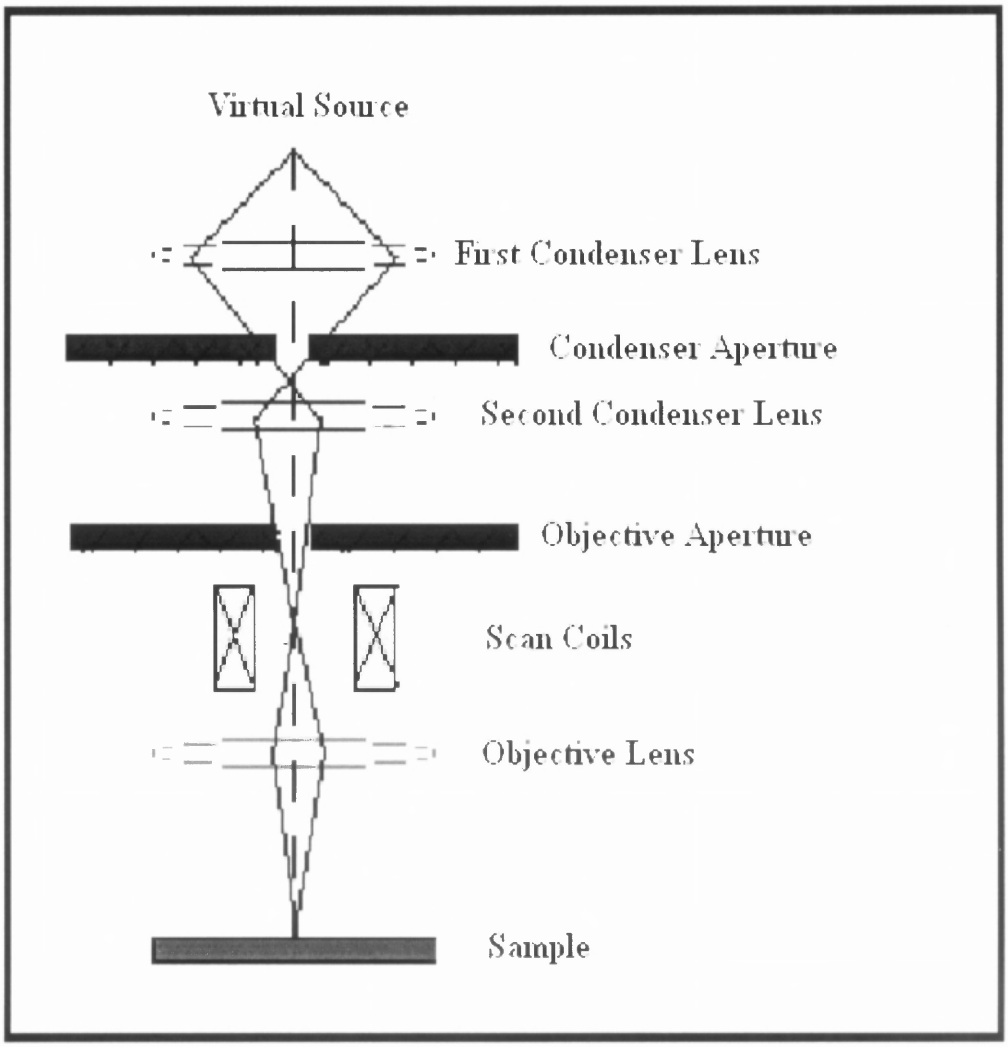

Figure 5.8 Schematic diagram of a SEM [70].

5.8 Spreading Resistance Profilometry (SRP)

This technique is used for measuring the dopant concentration and depth profiles of silicon. Figure 5.9 shows the schematic representation of the measurement setup of the alignment of probes used in SRP. The two probes are placed at a step along the semiconductor surface. Care is to be taken during the placement of probes. The probes are placed in such a way that it should make an electrical contact, while at the same time, the probes should not penetrate too much into the surface [21].

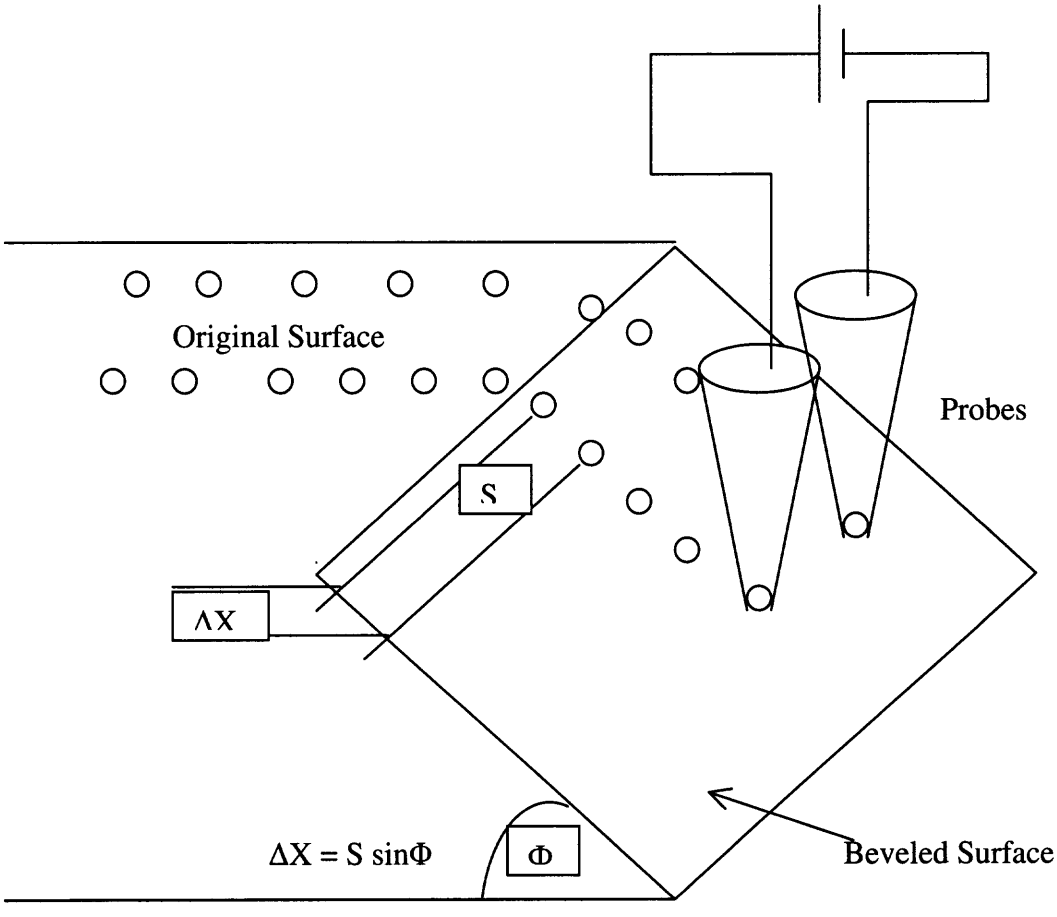

Figure 5.9 Schematic diagram of the alignment of probes using SRP [21].

The probes are generally made of osmium or tungsten alloy. The samples are beveled at a shallow angle (Φ) and this angle is approximately 1° for shallow layers [55]. When the probes are made to come in contact with the silicon, it appears that the probes tend to fracture whereas the probe / silicon interface deforms elastically. On supplying the voltage between the two probes the resistance can be measured and plotted [55]. Mathematically, the spreading resistance – resistivity relationship can be expressed as:

$$R_{SP} = \rho / 4r \tag{5.12}$$

where,

ρ = Resistivity

and r = Probe radius.

SRP cannot be performed with accuracy as it is dependent on the probe and the sample preparation. Hence it is necessary to use calibration procedures [71]. SRP is used for the study of epitaxial autodoping effects because of its wide carrier concentration sensitivity range [72]. It also finds application in verifying the models for arsenic dopant activation and autodoping phenomena [73].

5.9 Capacitance – Voltage (C-V) Measurements

This technique is the most dominant and widely used method as it provides detailed information about dielectrics and interfaces used in the semiconductor industry [21]. In this technique, the capacitance of a semiconductor device as a function of voltage is studied. C-V techniques are used in determining the semiconductor parameters such as dopant profiles, threshold voltage, density of interface states, carrier lifetime and oxide

charge. In the doping profiling method, a reverse biased space charge region is required to create a junction [55]. C-V profiling is used in the characterization of MOS capacitors, p-n junctions and Schottky barrier junctions, MOSFETs and junctions formed by electrochemical methods [55]. C-V measurements for a reverse bias capacitance of an n+/p or p+/n junction is given by the following formula:

$$C(V) = [q \varepsilon_{Si} C_A / 2]^{1/2} \times [V_{bi} \pm V_R - (2kT / q)]^{1/2} \qquad (5.13)$$

where,

$C(V)$ = Capacitance of a junction,

q = Free carrier Charge,

ε_{Si} = Permitivity of silicon,

C_A = Substrate doping concentration,

V_{bi} = Built in potential of the junction and

V_R = Applied reverse bias voltage.

The concentration of majority carriers can be determined by this technique by using a time varying voltage of variable frequency. Measurement of threshold voltage (V_T) plays a major role in characterizing the sub-micron MOSFETs. The measurement of ultra thin film oxides and V_T is done by using hard probe and also by using a high repeatability mercury probe.

5.10 Reverse Bias Diode Leakage Measurements

Reverse bias diode leakage is a diagnostic tool for the study of n/p junctions. Electron and hole recombination at defects in n/p junctions increases the reverse bias current. Theoretically, high quality n/p junctions should show leakage currents as low as 10^{-10} to 10^{-8} amp/cm^{-2} [74]. Increased leakage indicates the presence of defects. The typical defects produced by ion implantation and RTA are dislocations or dislocation loops, small clusters of silicon interstitials and vacancies, and impurity-defect clusters. Low leakage is required for ultra shallow junctions in MOSFET fabrication. In this thesis, a study of the leakage currents in n/p junctions, produced by ion implantation of phosphorus and arsenic into silicon, and diffusion by RTA, is presented. The experimental procedures are summarized in Chapter 6.

Summary

As characterization plays a vital role in determining the device parameters and also in failure analysis, it is critical to discuss them. In this chapter, various characterization techniques have been described. To name a few, the four-point probe method, DLTS, SIMS, RBS, SRP, SEM have been discussed in detail. Table 5.1, presented in this chapter, provides information on techniques that are being utilized in the semiconductor industry.

CHAPTER 6

EXPERIMENTAL TECHNIQUES DEPLOYED IN THIS STUDY

In this chapter, the experiments performed in this research are explained. Many experiments were carried during the study. Shallow junction samples were prepared by ion implantation followed by rapid thermal annealing. The wafers were 200 mm in diameter. In the first experiment, p-type silicon substrates were ion-implanted with phosphorus and arsenic. The wafers were then cut to a specific dimension of 1 cm^2. Then they are subjected to spike annealing. In the second experiment, the large wafers, after ion implantation, are subjected to rapid thermal annealing step. In this experiment, arsenic monomer and dimer were implanted at a constant dose with varying energies and the samples are cut to specific dimension of 1 cm^2. Major companies like Sematech International, Vortek Industries, Agere Systems and Axcelis Technologies provided the samples, which forms the building block of this research.

This research focuses on experimental study of the leakage currents in shallow junctions. This begins with the sample preparation at the laboratory at NJIT. Processing steps (RTP) were done at the collaborating companies and then finally, testing and measurements were done at NJIT. The results of leakage currents were analyzed using semiconductor theory. From the analyses of the experimental data, conclusions were drawn which are explained in the next chapter. The flowchart given in Figure 1.1 explains the formation of shallow junctions.

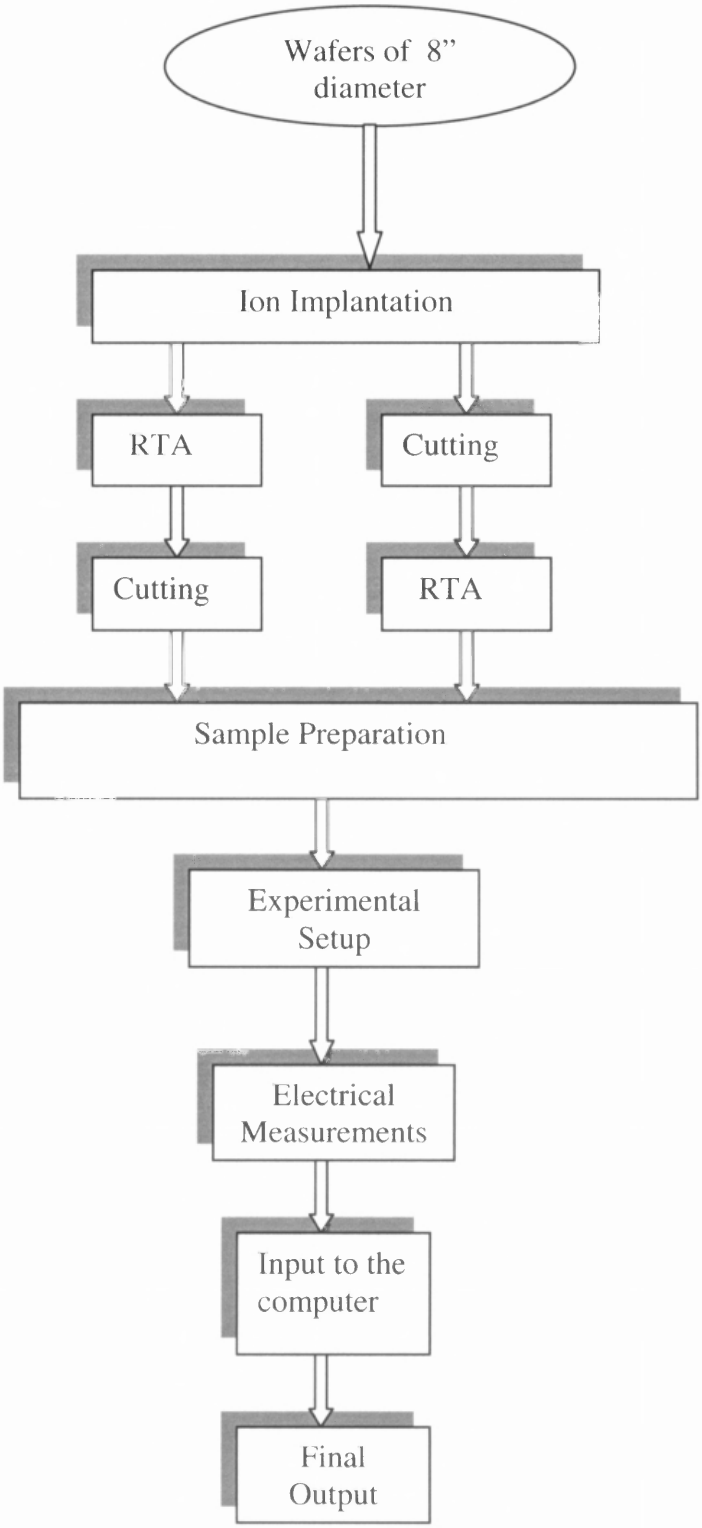

Figure 6.1 Flowchart describing the process carried out in this research.

6.1 Sample Preparation

The silicon wafers of 200 mm diameter were to be cut to a proper size for carrying out the experiments. The typical size of the cut sample (wafer) was 1cm x 1cm. The cutting of the large wafer was done in a special compartment with a hood and proper cutting tools. The samples from the collaborating industry were shipped in a special packing case, in order to avoid contamination and damage to the wafers. Then, they were cut to a shape of 1cm x 1cm with the help of cutting tools. Initially, a notch or groove was made in such a position that the wafer could be cut into two halves. The groove was made by means of a diamond indenter. As silicon is a very brittle material, the cleavage takes place in <110> direction, that is, a typical orientation followed during the single crystal growth of silicon. The notched wafer is first placed on the anvil, which is a raised flat board. The wafer is placed laterally in such a way that only the notched portion rests on the anvil. Slight pressure is applied on either side of the notch for the cleavage. This is as shown in Figure 6.2.

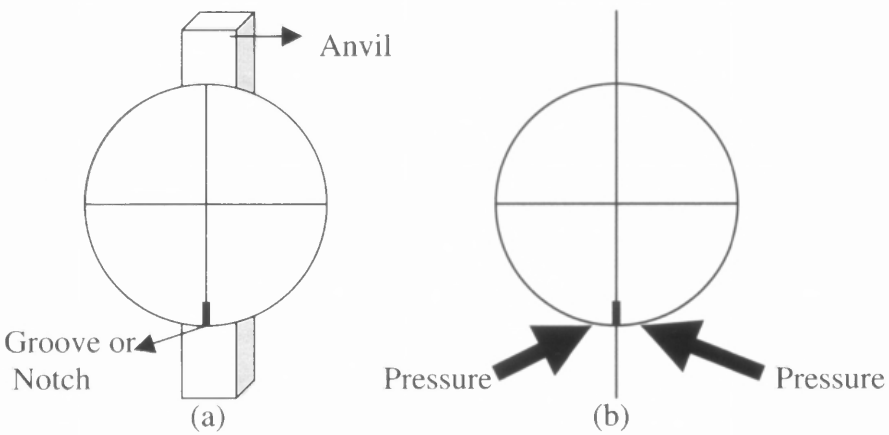

Figure 6.2 Schematic representation of the wafer before cutting.

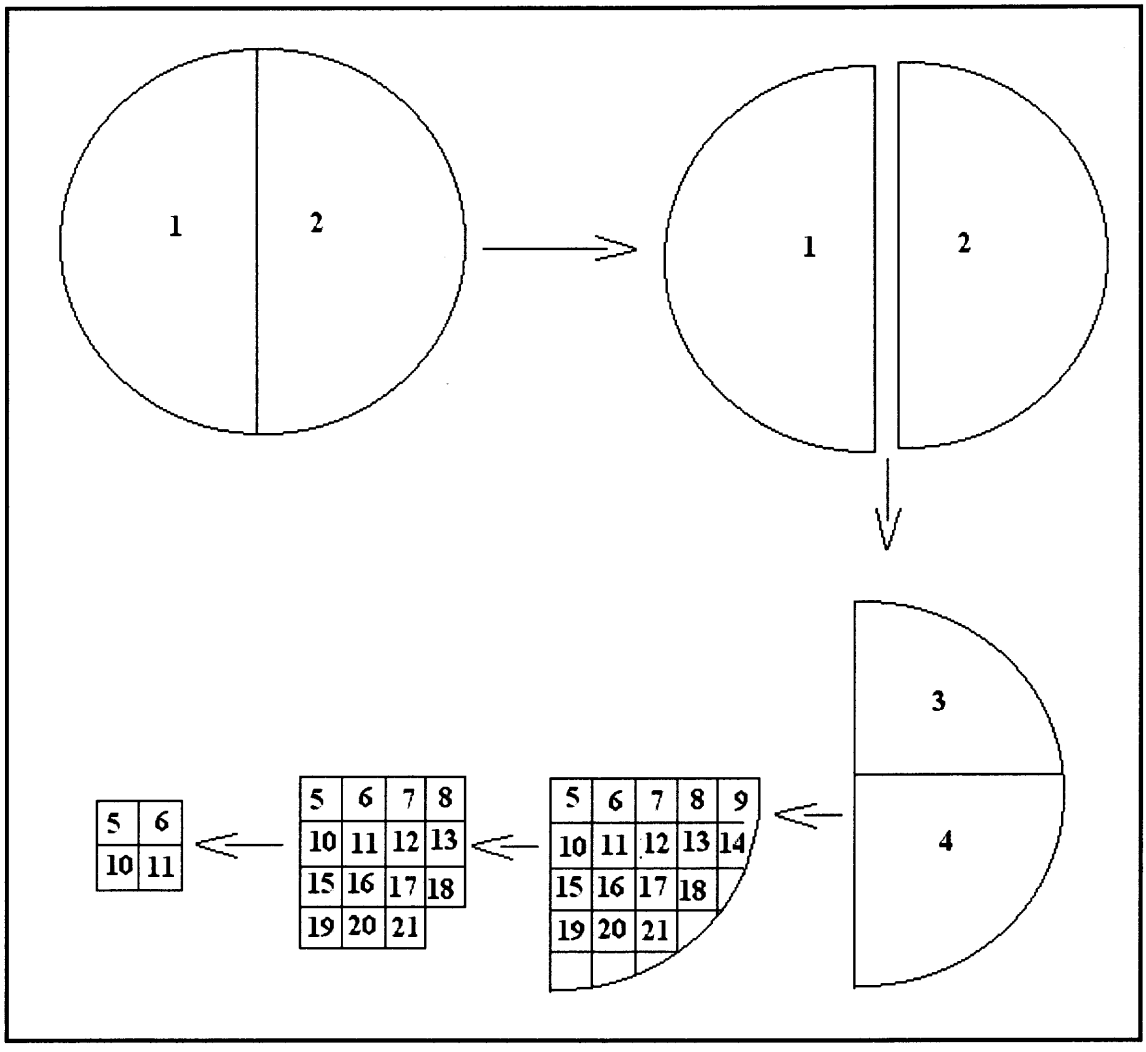

Figure 6.3 Schematic representation of cutting of wafers to a desired size.

The cutting of the samples is shown in Figure 6.2. After cutting, the final dimensions of the samples should be 1cm x 1cm and generally four samples were taken from each big wafer. The cut samples were marked with the help of a diamond indenter on the back for identification purposes. In the second step, the samples were again sent for processing, which is done by the collaborators. The four chips (5, 6, 10 and 11) from Figure 6.3 were annealed at different temperatures, which is the case for the first experiment.

6.2 Wax Patterning and Chemical Etching

The processed chips were patterned with the help of a wax (polymer) and 1mm diameter dots were created on the chips. Mesa diodes were formed as shown in Figure 6.4. This step is known as Wax Patterning.

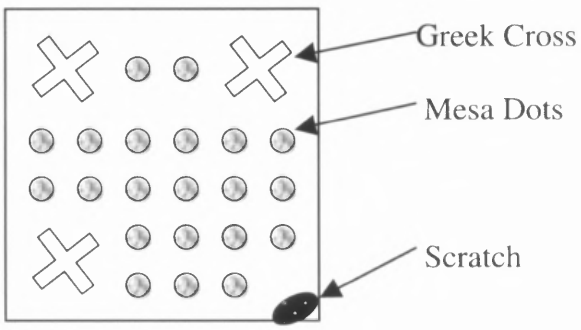

Figure 6.4 Wax patterning of the chip.

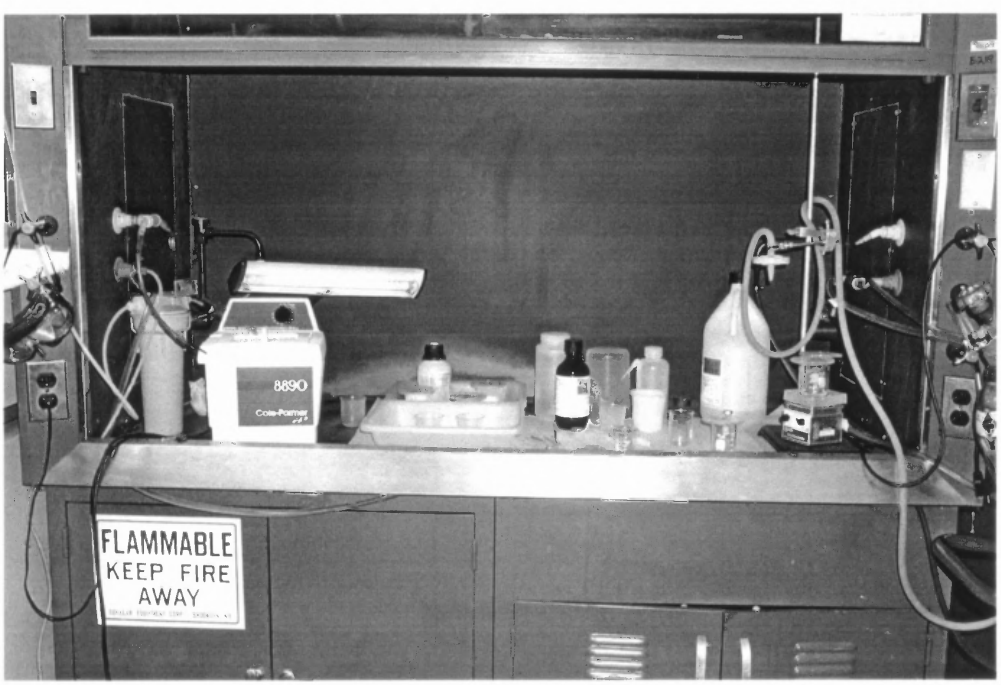

Figure 6.5 Chemical station for etching.

After wax patterning, the chips were etched by using CP4 etchant (fast, polishing or slow polishing) under a chemical station, which is shown in Figure 6.5. The etching time typically ranged from 20 – 30 seconds. The wax was removed after this step by dissolving it in solvents. Generally, first the chips were dipped in toluene, acetone, and propanol. Then they were immersed in distilled water and dried under nitrogen gas. Finally, the chips were dipped in hydrofluoric acid (HF) and then into acetic acid (CH_3COOH). The wax removal led to the creation of diodes in the form of circular dots. In reality, these dots were elliptical. During patterning of the dots, some space was left for scratching which formed the base of the sample and one of the probes was placed on this spot. The circular dots and the scratch on the base are illustrated in Figure 6.4.

6.3 Measurements

The sample after finishing the chemical step was ready for the measurement. A semiconductor probe station, shown in Figure 6.6, was used for the measurements. The probe station consists of a base platform or probe anvil. It has a chuck or a slot for mounting the sample. When the vacuum is turned on, the chuck secures the sample firmly. The sample can be moved longitudinally as well as laterally with the help of the knobs on the either side of the probe station. For making a good contact, indium was used. Indium is a very soft, adhesive and conductive material. The probe tips of the needles were also coated with indium by soldering.

The microscopic eye lens of the probe can be adjusted horizontally and vertically with the knobs. One of the knobs is shown in Figure 6.6. Out of the two eye-pieces, the left eye is used for making contacts and the right eye consists of a micrometer scale that

is used for measuring the diameter of the dots. The maximum number of divisions in the micrometer scale is 200 divisions. It is important that the number of divisions in the micrometer scale should be converted into the normal scale reading. For this, Vernier scale is used which converts number of divisions into inches. This is a multi-point probe station. In the present study, only three probes are used for the measurements. These probes typically have needles, which are attached to the micromanipulators. These micromanipulators are also associated with vacuum, in order to have a firm grip as well as to prevent the probe from moving. These manipulators can be moved up and down as well as forward and backward with the help of knobs.

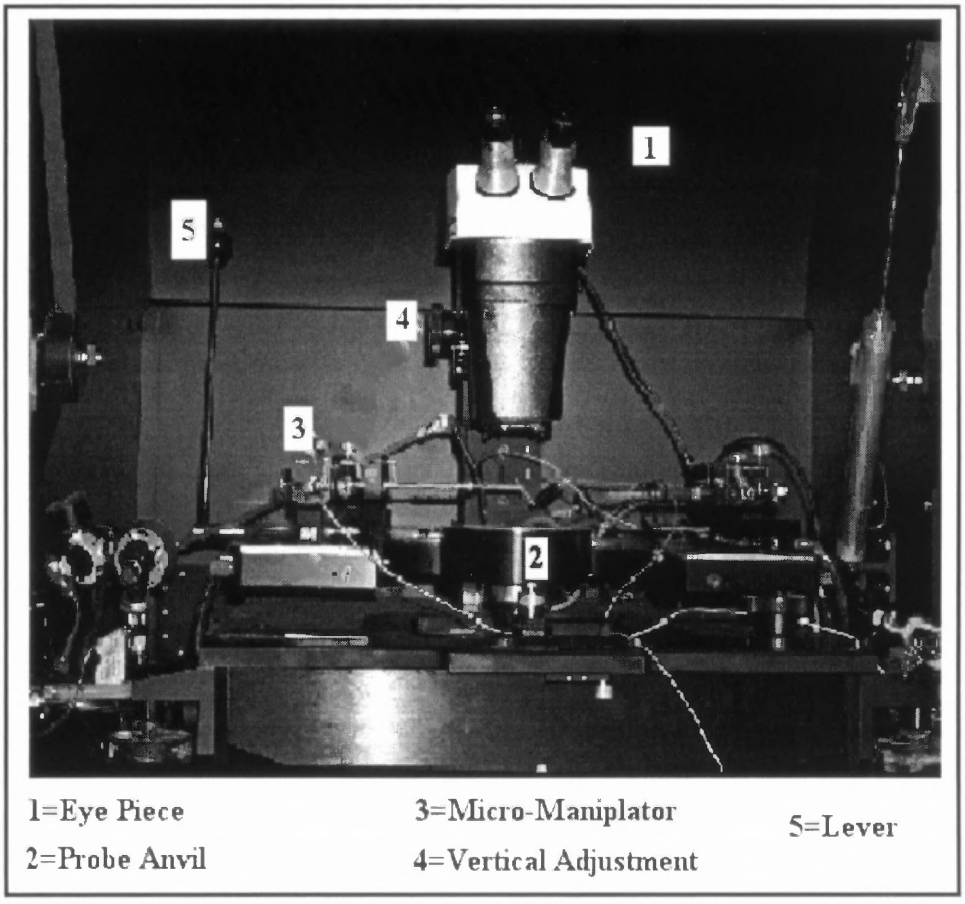

Figure 6.6 Detailed view of probe station with labeled parts.

One of the important steps is the circuit connection. Current amplifiers, digital multimeter, banana cables and connectors are required to complete the circuit. This is shown in the simple line diagram in Figure 6.7. The circuit connections should be checked before starting the experiments. There may be damage of the cables, improper functioning due to leakage or improper connections. Hence, it is always good to rectify them by double-checking and replacing the same.

There are a large number of mesa dots on the chip. For experimental purposes, the measurements were made only on four dots. The main aim of performing this experiment was to measure the +1V reverse biased leakage current of the diodes. Initially, a current reading is obtained. However, as time passes, there are fluctuations in the current readings and the value drops. These fluctuations cannot be completely eschewed. Consequently, the fluctuation in readings decreases as time passes. Hence, the readings are noted with increment of one minute for three minutes. The third reading of current after three minutes is the final value, as this is constant and there will be little or no fluctuations. In order to minimize fluctuations, the probe station enclosure, after making the electrical contacts is closed. The lamp of the microscope must also be turned off and the circuit should be properly grounded.

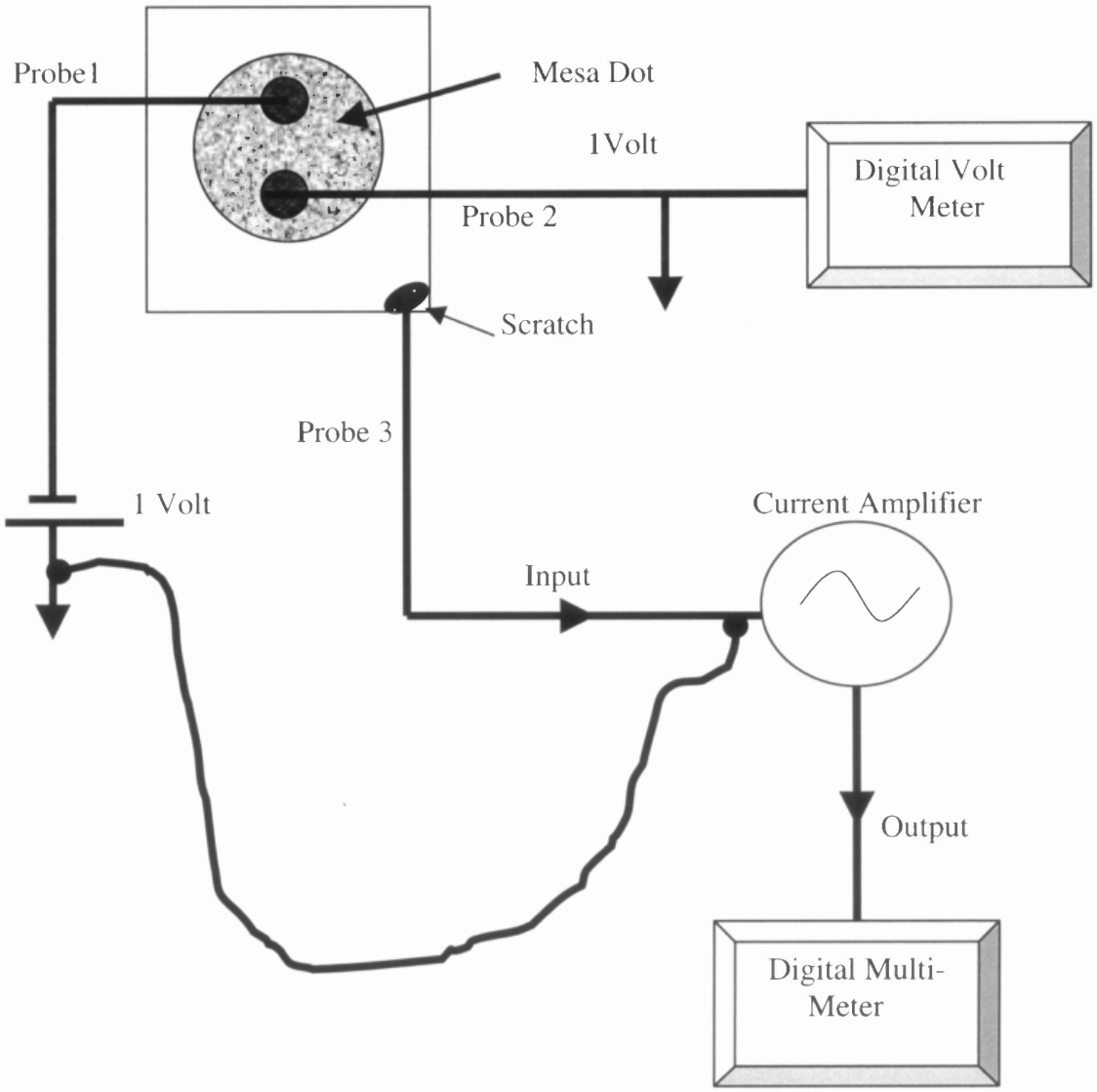

Figure 6.7 Schematic representation of the circuit diagram.

Before calculating the current density of the chip, the device area is to be determined by the following calculations. One of the important points to be noted, in this connection, is that the mesa dots formed by wax patterning are elliptical and not circular in geometry.

6.3.1 Calculations of Current Density

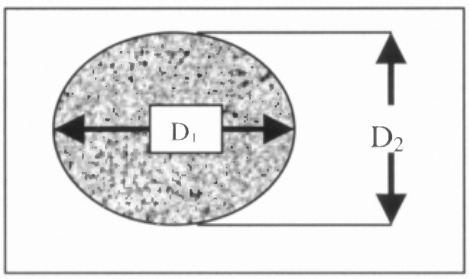

Figure 6.8 Representation of Mesa dot in elliptical form.

$$\text{Area} = \text{Area of Ellipse} \tag{6.1}$$

$$= \frac{\pi}{4} \times (D_1 \times D_2) \tag{6.2}$$

$$= \frac{\pi}{4} \times \frac{D_1 \times D_2 \times 0.01}{137 \times 137} \tag{6.3}$$

where,

D_1 = Diameter in vertical direction in divisions,

D_2 = Diameter in horizontal direction in divisions,

137 (1mm of vernier scale = 137 divisions of probe scale),

0.01 (Conversion factor from mm → cm),

$$\text{Current Density} = \frac{\text{Leakage Current}}{\text{Area}} \quad \frac{(\text{amp})}{(\text{cm}^2)} \tag{6.4}$$

The average of the two least current densities is taken and is formatted in Microsoft Excel for plotting graphs. From the interpretation of the data, conclusions have been made that are discussed in the next chapter.

Summary

This chapter explains the experimental procedures used in this research. Details of sample preparation and leakage current measurements have been presented. A simple program written in C++ (Appendix D) has been utilized for data formatting and calculations of area and current densities.

CHAPTER 7

DISCUSSION AND COMPARISON WITH RESULTS AND LITERATURE

The experiments that were carried out are listed here. The data sheets for each experiment are in the Microsoft Excel format. The summary sheet for each set of experiments is also presented.

In the first experiment, two different methods of spike annealing were done at Vortek Industries and Agere Systems. Vortek Industries performed the spike annealing (arc lamp) by heating the samples at a ramp-up rate of 400 °C / sec. Agere Systems utilized the other method of spike annealing (incandescent lamp), where the samples were heated at a ramp-up rate of 200 °C / sec. The results of the measured diode leakage current were plotted as function of annealing. These graphs also show the variation of diode leakage current with implant dose for the two types of annealing methods. The implant doses included 2 x 10^{14}, 4 x 10^{14}, 7 x 10^{14} and 1 x 10^{15} cm^{-2} of boron and phosphorus, and 1 x 10^{15} cm^{-2} of arsenic. The conclusions drawn from these plots are explained below. For the other device parameters such as junction depth, Hall carrier density, sheet resistance, etc., the graphs are presented in Appendix A.

In the second experiment, leakage current measurements for arsenic monomer and dimer implants were studied. These samples were rapid thermal annealed by Heatpulse method at two different temperatures: 850 °C, 900 °C, for 30 seconds. The dimer arsenic (As 2) species was implanted at double the energy (6 KeV) than the monomer (As), which is implanted at 3 KeV. Graphs were plotted for the variation of the leakage current with the implant dose for these samples. Results were also compared

with those obtained in the first experiment. RBS channeling spectra provided useful information about the implantation damage that occurred during the monomer and dimer arsenic implants.

7.1 Experiment 1

An example of an experimental data sheet is attached in Appendix C. Table 7.1 gives the summary of the samples studied in this experiment. It includes some of the ion implant parameters such as energy, dose, maximum temperature (T_{max}), sheet resistance (RS), Hall coefficient (RH), Hall carrier density (NH), junction leakage current ($J_{leakage}$), etc.

The first group of samples were prepared by boron ion implantation into n-type silicon wafers at an energy of 0.5 KeV and doses of 2 x 10^{14}, 4 x 10^{14}, 7 x 10^{14} and 1 x 10^{15} cm^{-2}. The first eight samples in this group were spike annealed at Agere Systems by the incandescent lamp method using a Heatpulse rapid thermal annealing system. The rest of the samples in this group were annealed at Vortek Industries using an arc lamp system.

The second group of samples were prepared by phosphorus ion implantation into p-type silicon wafer, at energy of 1.5 keV, and the same range of doses as for the boron group. In this group, the first 12 samples were spike annealed by incandescent lamp and the next set of samples in this group were spike annealed by arc lamp method.

shallow extension junctions

HP8108: 12mm sq chips on 8" aperture wafer.Ar +0.1% O2 spike anneals, ramp="200C/s"
Vortek: 25mm sq chips, Ar+0.1%O2 spike anneals,ramp 400C/s
Incandescent (Incand) and Arc Lamp Method (Arc Lamp.)

B implant, n-type wafer

CHIP ID	Energy	dose	recipe	Method	Tmax	Rs	RH	NH	NH/Dose	Xj	$J_{leakage}$ (A/cm^2)
D3-2	0.5	2.E+14	as1108.v00	Incand.	1111	1074.0	4.760	1.02E+14	0.5123	3.33E-06	1.34E-05
D3-3	0.5	2.E+14	as1125.v00	Incand.	1122	1045.3	4.604	1.06E+14	0.5291	3.33E-06	4.83E-04
F5-3	0.5	4.E+14	as1062.v00	Incand.	1058	819.1	3.384	1.42E+14	0.3559	3.22E-06	9.95E-04
F5-2	0.5	4.E+14	as1067.v00	Incand.	1075	665.3	2.690	1.78E+14	0.4462	3.58E-06	3.39E-06
A5-3	0.5	7.E+14	as1027.v00	Incand.	1026	822.4	3.299	1.45E+14	0.2076	2.79E-06	1.85E-06
A5-1	0.5	7.E+14	as1033.v00	Incand.	1037	722.5	2.824	1.69E+14	0.2417	2.79E-06	4.50E-07
D0-3	0.5	1.E+15	as1008.v00	Incand.	1009	761.1	2.948	1.62E+14	0.1619	2.54E-06	1.93E-06
D0-1	0.5	1.E+15	as1012.v00	Incand.	1017	729.4	2.826	1.69E+14	0.1689	2.65E-06	9.40E-07
D3A	0.5	2.E+14	1085	Arc Lamp.	1086	1797.0	8.280	6.02E+13	0.3008	2.20E-06	9.12E-07
D3B	0.5	2.E+14	1105	Arc Lamp.	1105	1500.0	6.627	7.45E+13	0.3727	2.25E-06	1.44E-06
D3C	0.5	2.E+14	1125	Arc Lamp.	1125	1369.0	6.099	8.11E+13	0.4057	2.55E-06	9.73E-07
D3D	0.5	2.E+14	1145	Arc Lamp.	1145	1265.0	5.630	8.79E+13	0.4394	2.74E-06	1.52E-06
F5A	0.5	4.E+14	1065	Arc Lamp.	1066	1248.0	5.265	9.30E+13	0.2326	2.24E-06	3.75E-06
F5B	0.5	4.E+14	1085	Arc Lamp.	1086	1006.8	4.157	1.17E+14	0.2934	2.53E-06	3.05E-06
F5C	0.5	4.E+14	1105	Arc Lamp.	1105	821.9	3.380	1.44E+14	0.3607	3.05E-06	1.14E-06
F5D	0.5	4.E+14	1125	Arc Lamp.	1125	688.7	2.839	1.72E+14	0.4296	3.68E-06	7.53E-07
A5A	0.5	7.E+14	1035	Arc Lamp.	1036	1261.0	5.180	9.41E+13	0.1345	1.98E-06	1.51E-06
A5B	0.5	7.E+14	1055	Arc Lamp.	1056	966.7	3.928	1.24E+14	0.1770	2.46E-06	8.76E-07
A5C	0.5	7.E+14	1075	Arc Lamp.	1075	752.8	3.000	1.62E+14	0.2311	2.90E-06	7.61E-07
A5D	0.5	7.E+14	1095	Arc Lamp.	1095	585.4	2.310	2.10E+14	0.2997	3.56E-06	9.84E-07
DOA	0.5	1.E+15	1005	Arc Lamp.	1006	1369.0	5.705	8.57E+13	0.0857	1.94E-06	1.29E-06
DOB	0.5	1.E+15	1025	Arc Lamp.	1026	1090.0	4.339	1.12E+14	0.1118	1.99E-06	2.20E-06
DOC	0.5	1.E+15	1045	Arc Lamp.	1046	879.0	3.470	1.40E+14	0.1397	2.38E-06	data missing
DOD	0.5	1.E+15	1065	Arc Lamp.	1065	693.4	2.694	1.80E+14	0.1796	2.81E-06	1.55E-06

Phos implant, p-type wafer

CHIP ID	Energy	dose	recipe		Tmax	Rs	RH	NH	NH/Dose	Xj	
A6-1	1.5	2.E+14	as1079.v00	Incand.	1077	1114.0	-15.670	4.88E+13	0.2281	4.68E-06	2.49E-05
A6-3	1.5	2.E+14	as1100.v00	Incand.	1097	1026.8	-14.380	5.32E+13	0.2484	5.04E-06	2.90E-05
A6-2	1.5	2.E+14	as1108.v00	Incand.	1115	873.2	-11.150	6.77E+13	0.3163	4.92E-06	2.36E-05
D1-3	1.5	4.E+14	as1000.v00	Incand.	1001	943.5	-12.740	5.97E+13	0.1396	5.10E-06	2.90E-06
D1-2	1.5	4.E+14	as1028.v00	Incand.	1031	731.2	-8.598	8.63E+13	0.2017	4.91E-06	7.20E-06
D1-1	1.5	4.E+14	as1060.v00	Incand.	1063	560.1	-6.036	1.20E+14	0.2813	5.21E-06	6.28E-05
F4-3	1.5	7.E+14	as970.v00	Incand.	971	565.1	-6.811	1.10E+14	0.1463	6.72E-06	2.17E-06
F4-2	1.5	7.E+14	as1000.v00	Incand.	1003	425.6	-3.933	1.78E+14	0.2371	4.53E-06	1.30E-06
F4-1	1.5	7.E+14	as1028.v00	Incand.	1032	335.6	-2.880	2.39E+14	0.3191	4.69E-06	sample not found
A4-3	1.5	1.E+15	as950.v00	Incand.	951	467.5	-4.114	1.68E+14	0.1571	3.60E-06	4.50E-06
A4-2	1.5	1.E+15	as970.v00	Incand.	972	367.9	-2.900	2.35E+14	0.2198	3.47E-06	5.97E-06
A4-1	1.5	1.E+15	as1000.v00	Incand.	999	303.2	-2.373	2.87E+14	0.2684	4.14E-06	4.91E-06
A6A	1.5	2.E+14	1090	Arc Lamp.	1090	1328.0	-18.640	4.27E+13	0.1994	3.55E-06	1.15E-06
A6B	1.5	2.E+14	1110	Arc Lamp.	1110	1173.0	-20.850	3.85E+13	0.1800	5.97E-06	4.66E-06
A6C	1.5	2.E+14	1130	Arc Lamp.	1131	1045.0	-13.700	5.74E+13	0.2682	3.95E-06	7.89E-06
A6D	1.5	2.E+14	1150	Arc Lamp.	1150	890.7	-11.880	6.64E+13	0.3103	4.81E-06	6.59E-06
D1A	1.5	4.E+14	1050	Arc Lamp.	1051	818.4	-9.917	7.80E+13	0.1821	4.27E-06	8.40E-07
D1B	1.5	4.E+14	1070	Arc Lamp.	1071	688.3	-7.637	9.90E+13	0.2313	4.13E-06	1.94E-06
D1C	1.5	4.E+14	1090	Arc Lamp.	1091	640.5	-6.470	1.14E+14	0.2665	3.52E-06	6.66E-06
D1D	1.5	4.E+14	1110	Arc Lamp.	1111	549.0	-5.377	1.36E+14	0.3184	3.80E-06	2.21E-06
F4A	1.5	7.E+14	1005	Arc Lamp.	1006	532.5	-4.966	1.46E+14	0.1950	3.46E-06	1.18E-06
F4B	1.5	7.E+14	1025	Arc Lamp.	1026	474.3	-4.247	1.70E+14	0.2266	3.52E-06	1.49E-06
F4C	1.5	7.E+14	1045	Arc Lamp.	1046	423.5	-3.697	1.94E+14	0.2595	3.72E-06	9.26E-07
F4D	1.5	7.E+14	1065	Arc Lamp.	1066	343.3	-2.782	2.57E+14	0.3437	3.90E-06	sample not found
A4A	1.5	1.E+15	985	Arc Lamp.	986.6	432.4	-3.457	2.07E+14	0.1936	3.02E-06	2.25E-06
A4B	1.5	1.E+15	1005	Arc Lamp.	1006	395.1	-3.200	2.24E+14	0.2091	3.39E-06	2.84E-06
A4C	1.5	1.E+15	1025	Arc Lamp.	1026	339.3	-2.575	2.79E+14	0.2610	3.50E-06	2.85E-06
A4D	1.5	1.E+15	1045	Arc Lamp.	1046	266.2	-1.838	3.98E+14	0.3722	3.86E-06	2.47E-06

Arsenic implant, p-type wafer

CF3-1	5	1.E+15	as950.v00	Arc Lamp.	948	371.9	-2.120	3.36E+14	0.3137	2.15E-06	1.72E-06
CF3-2	5	1.E+15	as980.v00	Arc Lamp.	981	365.5	-2.067	3.45E+14	0.3225	2.18E-06	1.01E-06
CF3-3	5	1.E+15	as1010.v00	Arc Lamp.	1009	341.9	-1.895	3.79E+14	0.3540	2.29E-06	1.68E-06
CF3-4	5	1.E+15	as1040.v00	Arc Lamp.	1036	315.3	-1.743	4.12E+14	0.3852	2.47E-06	7.14E-07
F3A	5	1.E+15	985	Arc Lamp.	985.7	352.5	-1.881	4.33E+14	0.4049	2.22E-06	9.39E-07
F3B	5	1.E+15	1005	Arc Lamp.	1006	362.0	-1.967	4.11E+14	0.3837	2.19E-06	6.39E-07
F3C	5	1.E+15	1025	Arc Lamp.	1026	350.8	-1.888	4.30E+14	0.4017	2.25E-06	7.08E-07
F3D	5	1.E+15	1045	Arc Lamp.	1046	336.7	-1.799	4.53E+14	0.4231	2.33E-06	8.69E-07

The third group of samples were prepared by implanting arsenic at one dose (1 x 10^{15} cm^{-2}) and energy (5 KeV). Half of the number of samples was annealed by incandescent lamp, and the other half was annealed by the arc lamp method.

There were 50 samples in number that were tested in this experiment. The process conditions of these samples are summarized in Table 7.1. Three to four anneal temperatures were studied for each dose. From this experiment, observations were drawn from three graphs of the leakage current data and sheet resistance as function of annealing temperature: Two graphs for the phosphorus implants and one for the arsenic implants.

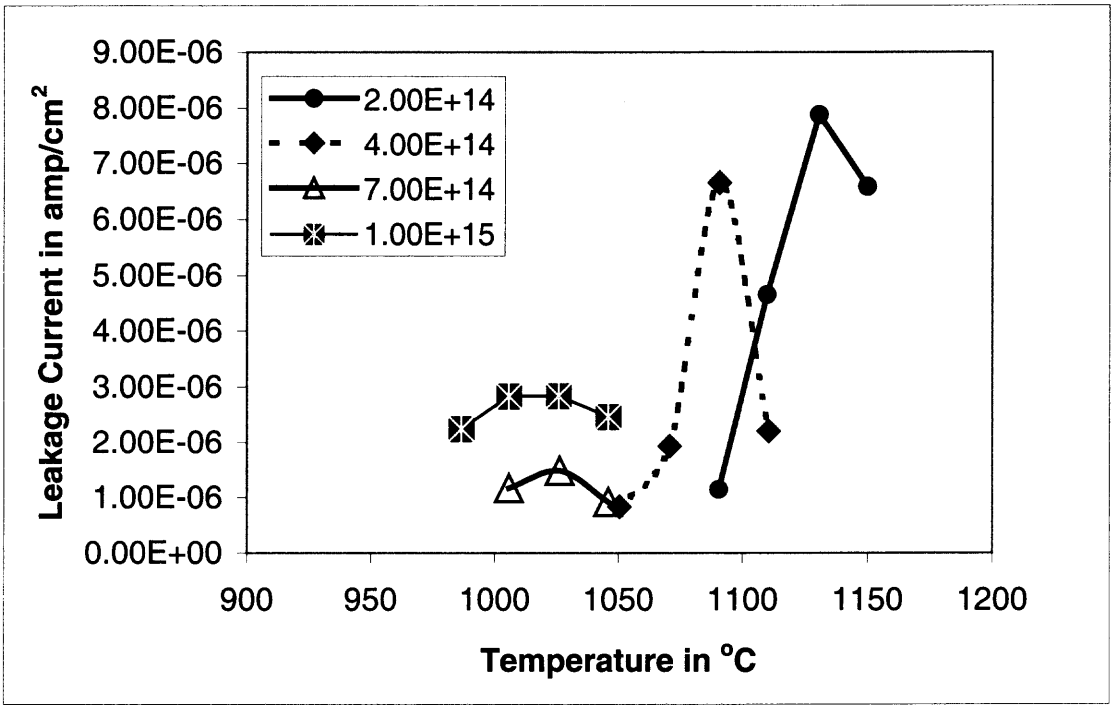

Figure 7.1 Leakage current versus temperature for phosphorus samples that were rapid thermal annealed by arc lamp method at a ramp-up rate of 400 °C / sec.

7.1.1 Observations - 1

Figure 7.1 illustrates the reverse bias diode leakage current density at +1Volt bias vs. arc lamp spike anneal temperature for 1.5 KeV phosphorus implants at four doses (cm^{-2} units). The leakage current density exhibits a maximum, as a function of the spike anneal temperature. This is seen in the data for all lower phosphorus doses. From the graphs, it is seen that for the two highest doses the leakage is low. The leakage current maximum is found to be 2.85×10^{-6} amp/cm^2 at a dose of 1×10^{15} cm^{-2} and the maximum is 7.89×10^{-6} amp/cm^2 at a dose of 2×10^{14} cm^{-2}. However, this trend is different for the lower two doses annealed at higher temperatures. It is found that at higher temperatures the leakage was high for a low dose, whereas theoretically, the leakage current might be expected to be low at higher temperatures. One of the reasons for this might be due to the transient enhanced diffusion of phosphorus, which causes defects. The data suggests that the defects, which are responsible for the leakage, may be annealed out at sufficiently high temperatures.

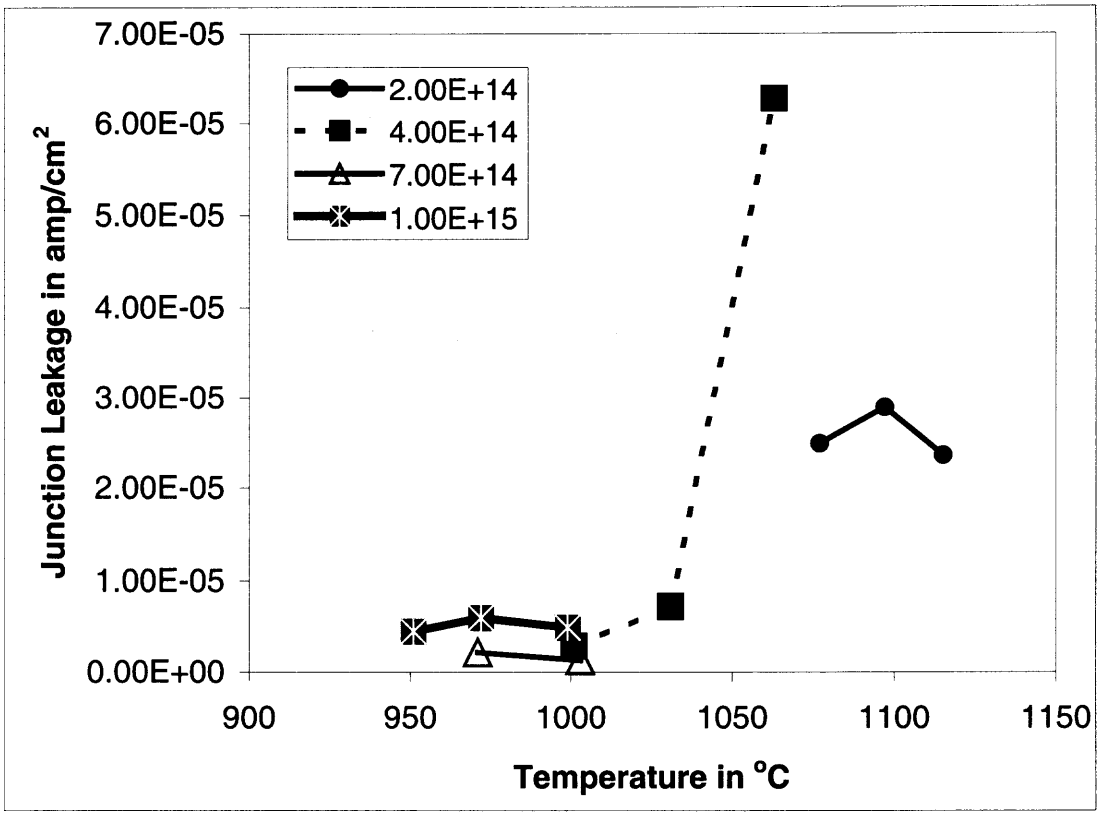

Figure 7.2 Leakage current versus temperature for phosphorus samples that were rapid thermal annealed by incandescent lamp method at a ramp-up rate of 200 °C / sec.

7.1.2 Observations - 2

Figure 7.2 illustrates the reverse bias diode leakage current densities at +1Volt bias vs. incandescent spike anneal temperature for 1.5 KeV phosphorus implants at four doses (cm^{-2} units). From the graph, it is observed that for the higher two doses the leakage is lower than the lowest two doses. This behavior is the same as was observed for the arc lamp annealing method as discussed in Observations - 1. This also gives a hint of the maximum temperature effect. However, there are too few data points to draw this as an independent conclusion. The leakage current maximum is found to be 5.97 x 10^{-6}

amp/cm^2 at a dose of 1 x 10^{15} cm^{-2} and the maxima is 6.28 x 10^{-5} amp/cm^2 at a dose of 4 x 10^{14} cm^{-2}. The highest leakage is observed for the 4 x 10^{14} cm $^{-2}$ dose.

From the comparison of two methods of spike annealing, it can be concluded that the leakage current for the incandescent lamp method is generally higher than the arc lamp method. The temperature ranges for the incandescent lamp anneals are lower than the arc lamp anneals. This is due to the fact that the goal of these experiments is to obtain films with comparable sheet resistance range in the two methods as shown in Figures 7.3 and 7.4 for the same samples.

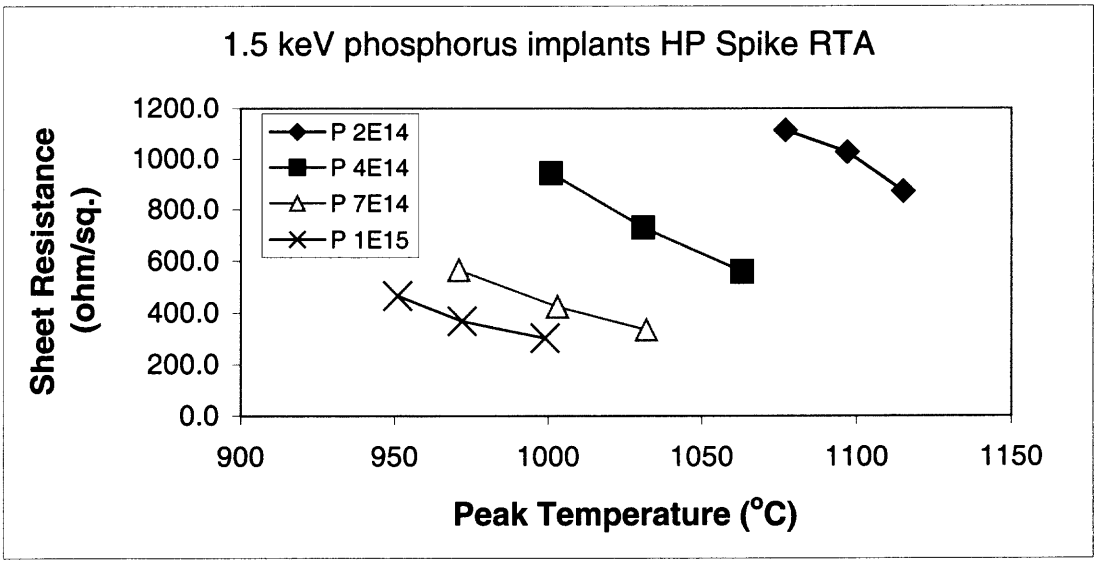

Figure 7.3 Sheet resistance versus peak temperature for 1.5 KeV phosphorus implants (Heatpulse by using incandescent lamps).

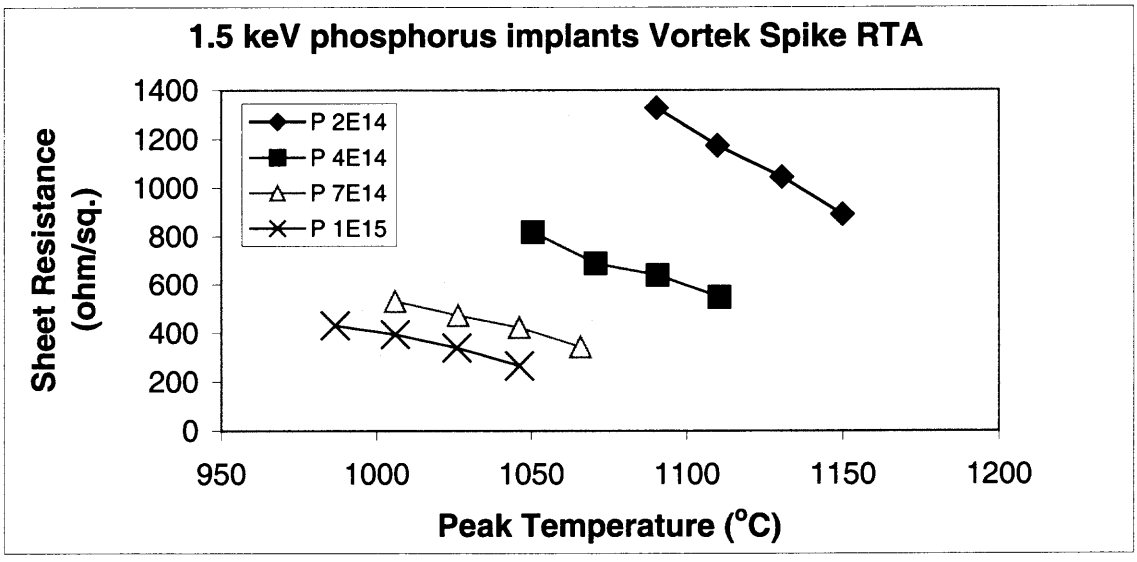

Figure 7.4 Sheet resistance versus peak temperature for 1.5KeV phosphorus implants (Vortek spike RTA by using arc lamp method).

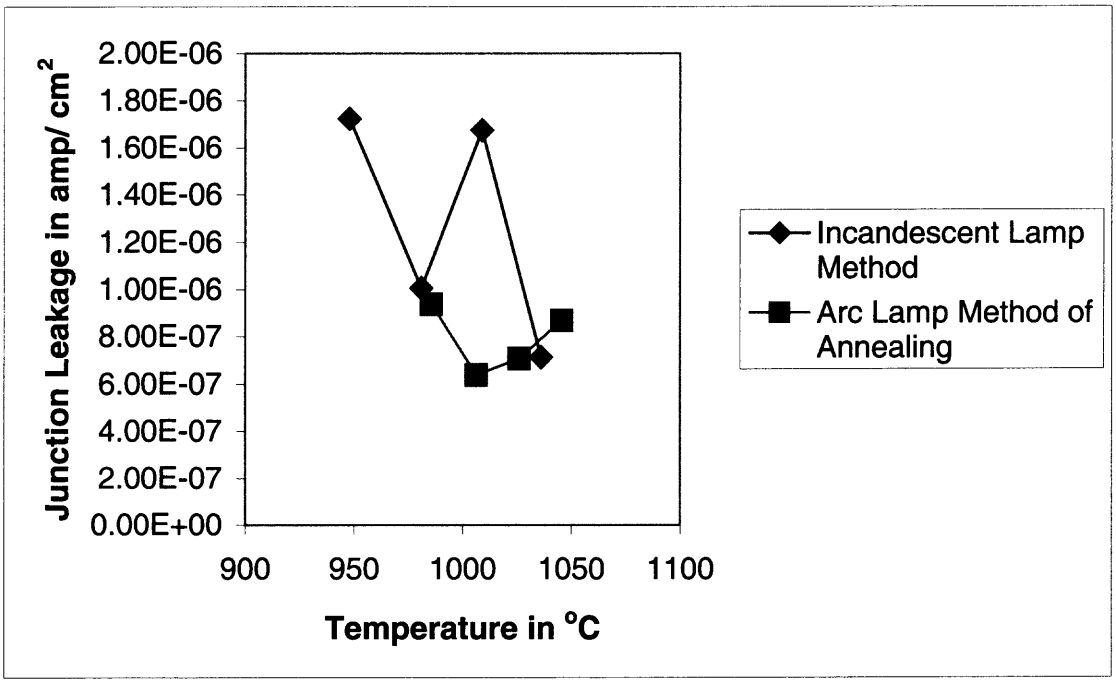

Figure 7.5 Leakage current density vs. temperature for arsenic implants (Comparison is made with the annealing procedures for incandescent lamps and arc lamp method of annealing).

7.1.3 Observations - 3

Figure 7.5 shows the variation of the leakage current density versus spike anneal temperature for arsenic implants, using the arc lamp and incandescent lamp methods. The variation of leakage current with temperature is not particularly systematic. The leakage current decreases with decrease in temperature. However, at an annealing temperature of 1009 °C, the leakage current was found to be high in the case of incandescent method of annealing. Also, the leakage current behavior is found to be similar for both types of annealing.

It is observed from Figure 7.5 that the average leakage current by the incandescent lamp method is higher than the average leakage current by the arc lamp method for the arsenic implants. This is also found to be true in the case of phosphorus implants (Observation-2). The overall leakage levels for the arsenic implants is lower than that of the phosphorus implants by a factor of 5.

From the observations of the above graphs, it can be summarized that the arsenic implants are favorable for shallow n/p junction formation because arsenic implants have negligible transient enhanced diffusion. Results of the leakage current density presented here show that there is an additional advantage of lower junction leakage for using arsenic in n/p junction.

Experiment 2

This experiment compares arsenic monomer (As) and dimer (As 2) implants at two implant energies chosen to yield the same range for both species. Moreover, the implant doses differ by a factor of 2 (dimer species has twice the implant energy than the

monomer arsenic species). Five implant doses were studied in this experiment. The samples were annealed by incandescent lamp rapid thermal annealing method for 30 seconds. Most of the samples were annealed at 850 °C. Several samples were annealed at 900°C in a test for possible variation of device properties with anneal temperature.

Table 7.2 Summary Sheet of Arsenic Monomer (75 arsenic) and Dimer (150 arsenic 2) Samples

Chip Id	Dose	Energy (KeV)	Species	Leakage Current (Amp/ cm^2)
H114 A	5.00E+13	3	75 Arsenic	6.36 E-9
H119 A	1.00E+14	3	75 Arsenic	3.35 E-9
H172A	2.00E+14	3	75 Arsenic	4.64 E-9
H132 A	4.00E+14	3	75 Arsenic	4.57 E-9
H020 A	8.00E+14	3	75 Arsenic	5.28 E -9
H020B	8.00E+14	3	75 Arsenic	5.09 E-9
H02A	5.00E+13	6	150 Arsenic2	8.07 E –9
H68 A	1.00E+14	6	150 Arsenic2	5.76 E-9
H01 A	2.00E+14	6	150 Arsenic2	5.95 E-9
H04A	2.50E+13	6	150 Arsenic2	6.05 E-9
H 67 B	4.00E+14	6	150 Arsenic2	6.58 E-9

The motivation for this study is the desirability of using higher implant energy for shallow junction formation. A higher energy allows a higher beam current in the implanter and this lowers the cost of production. Table 7.2 gives the summary of the arsenic samples. The wafers were 200 mm diameter highly doped p-type silicon. The sheet resistivity of the wafers was approximately 10 Ohm-cm. The reverse bias diode leakage measurements were carried out for arsenic monomer and dimer implants after soak RTA. The experiment was performed on 11 samples and the graphs were plotted.

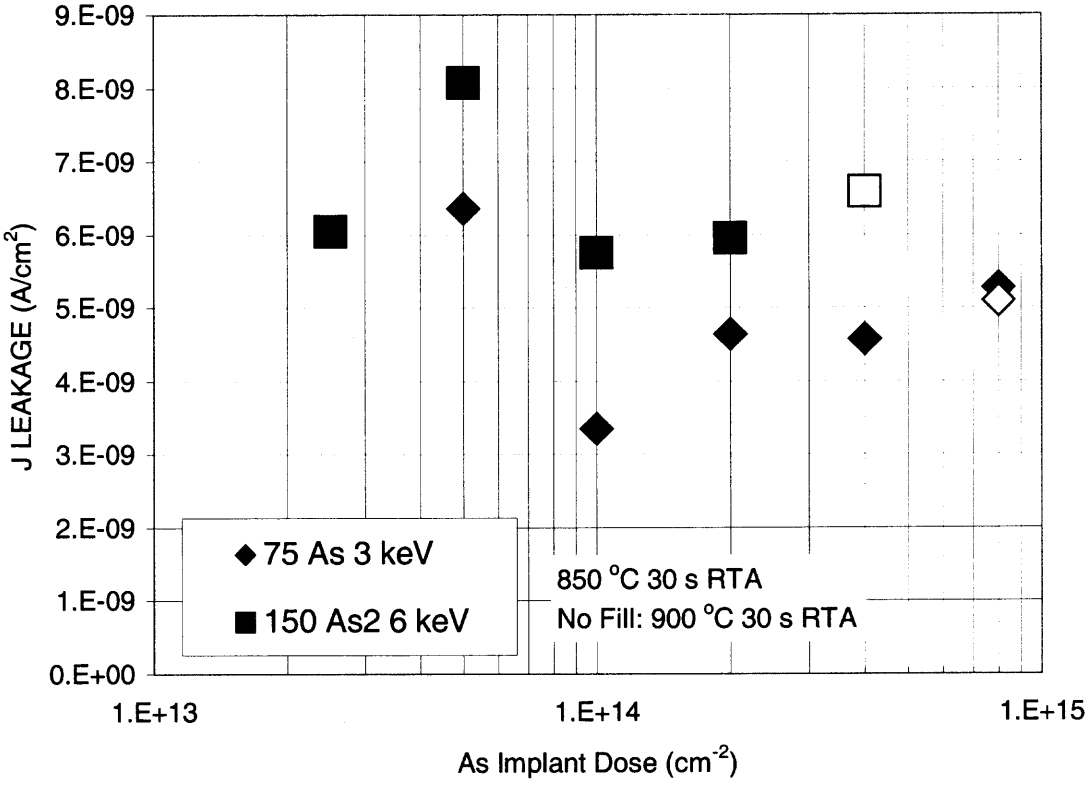

Figure 7.6 Leakage current density versus implant dose for arsenic samples that were rapid thermal annealed at 850 °C for 30 seconds or 900 °C for 30 seconds.

7.2.1 Observations - 4

Figure 7.6 shows the variation of leakage current density with arsenic implant dose for arsenic monomer and dimer species. The leakage current density is found to have a small (10 %) variation with dose. The largest variations are as follows: the 5 x 10^{13} cm^{-2} dimer implant shows the highest leakage and the 1 x 10^{14} cm^{-2} monomer implant shows the lowest leakage. Even though the dimers were implanted at double the implantation energy, i.e., 6 KeV, the leakage current density was found to be consistently larger than the monomer implanted at 3 KeV. These differences were found to be approximately up to 50 percent. However, the leakage current density values for both species are two

orders of magnitude lower than that obtained by spike annealing of arsenic implants in Experiment I (compare Figure 7.6 with Figure 7.5). It can be concluded that soak annealing is more effective for removing defects than spike annealing in n/p junctions.

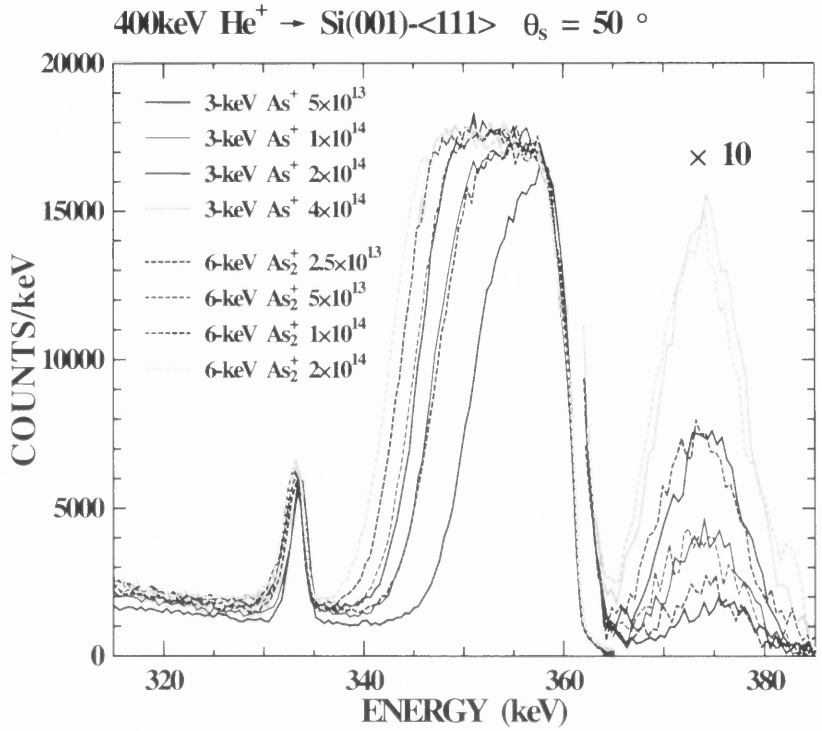

Figure 7.7 RBS channeling spectra for the implants shown in Table 7.2.

There are three peaks in the spectra in Fig. 7.7. The lowest energy peak (330-335KeV) is from a surface oxide. The middle peaks, from 340-360 KeV, represent the damage of amorphized silicon. In the middle peak, the dimer (dotted curves) creates greater and deeper damage than the monomer (solid curves) at the same equivalent arsenic dose. The amorphized silicon peak becomes broader i.e., it extends to lower energy with increasing dose. The highest energy peak from 365-380 KeV represents the monomer and the dimer arsenic profiles. The profiles for both species are almost the same for equivalent doses as shown by the broad peaks at 375 KeV (expanded 10 times).

Finally, from the above discussions of Experiment 2, it can be concluded that the dimer arsenic species creates more damage and the diode leakage indicates that more defects remain after annealing the dimer implant. The damage that remained after annealing thus correlates with the damage created by the implant.

CHAPTER 8

CONCLUSIONS

In this thesis, n/p shallow junction formation was studied with the influence of various parameters such as: implantation dose, energy conditions, rapid thermal annealing (RTA) methods, annealing temperatures and type of species (P^+, As^+, and As_2^+). Electrical characterization technique is used for measuring the reverse bias diode leakage current at +1Volt bias. The three-point probe method is used for performing the leakage current density.

It can be concluded that the leakage current densities for the incandescent lamp method RTA are generally higher than for the arc lamp RTA method. When comparing the leakage current densities of both phosphorus and arsenic, the overall leakage levels for the arsenic is lower than that of phosphorus implants by a factor of 5. Transient Enhanced Diffusion (TED) plays an important role in the leakage levels for arsenic and phosphorus. TED for arsenic is negligible. For the phosphorus, the higher leakage is attributed to defects caused by TED. Leakage in phosphorus-based n/p junctions show maxima in the temperature dependence, which indicate that these defects can be annealed out at sufficiently high temperatures.

These studies show that the arsenic implants are in general favorable for the formation of n/p shallow junctions. Comparison of monomer (As^+) and dimer (As_2^+) implants show that at equivalent doses and ranges, n/p junctions prepared with dimer implants have systematically higher leakage, which correlates with the relatively greater damage produced by dimer implants found by ion scattering measurements.

APPENDIX A

RESULTS OF BORON IMPLANTS

Electrical and junction depth data of n/p junctions formed by boron implantation and spike annealing are presented here.

In Figure A.1, the sheet resistance is plotted versus the junction depth for four different implant doses. The samples are spike annealed at a ramp rate of 400 °C/sec. In general, as the junction depth increases, the amount of dose required decreases. However, the sheet resistance is approximately constant with increase in the junction depth. The sheet resistance is highest for the energy dose of 2 x 10^{14} amp/cm^2 and is lowest for the energy dose of 7 x 10^{14} amp/cm^2.

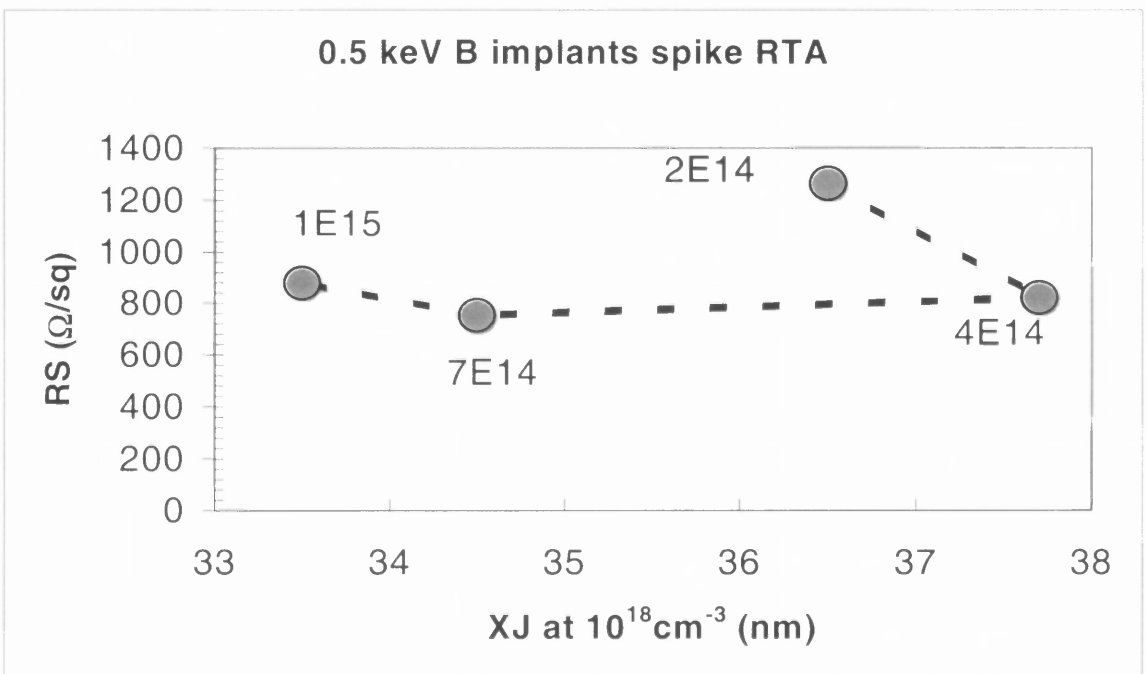

Figure A.1 Sheet resistance versus junction depth for 0.5 KeV boron implants (spike RTA).

The samples are spike annealed at a ramp rate of 200 °C/sec and this is done in a Heatpulse (HP) 8108 furnace in argon ambient. The sheet resistance decreases with decrease in temperature and decreases with increase in dose. The sheet resistance is in the range of 700-800 ohms/□ for the high energy dose of boron 1 x 10^{15} cm^{-2} and is in the range of 1000-1000 ohms/□ for the low energy dose of boron 2 x 10^{14} cm^{-2}.

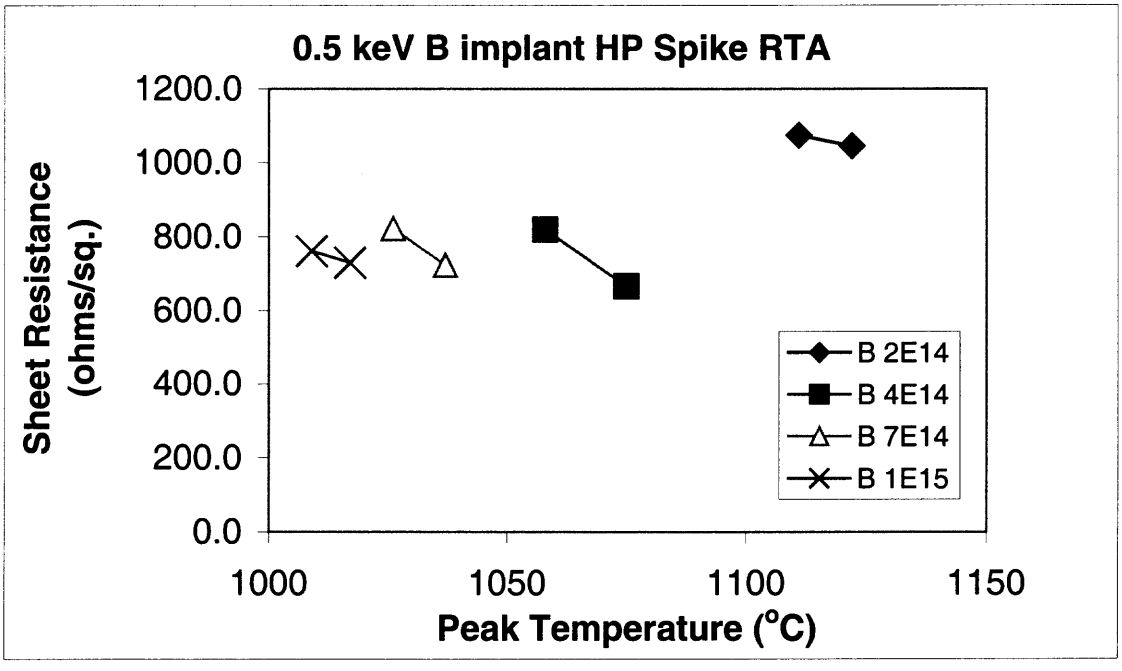

Figure A.2 Sheet resistance versus peak temperature for 0.5 KeV boron implants (HP spike RTA).

As the energy dose increases, the sheet resistance decreases. For a constant energy dose, the sheet resistance decreases with increase in annealing temperature. This is observed for all energy doses ranging from low energy dose of boron 1 x 10^{15} cm^{-2} to a high-energy dose of boron 1 x 10^{15} cm^{-2}. This shows that the sheet resistance depends on the energy dose as well as the peak annealing temperature. Also, flash lamp annealing at a rate of 400 °C/sec shows much steeper curves than the heat pulse annealing done at a ramp rate of 200 °C/sec

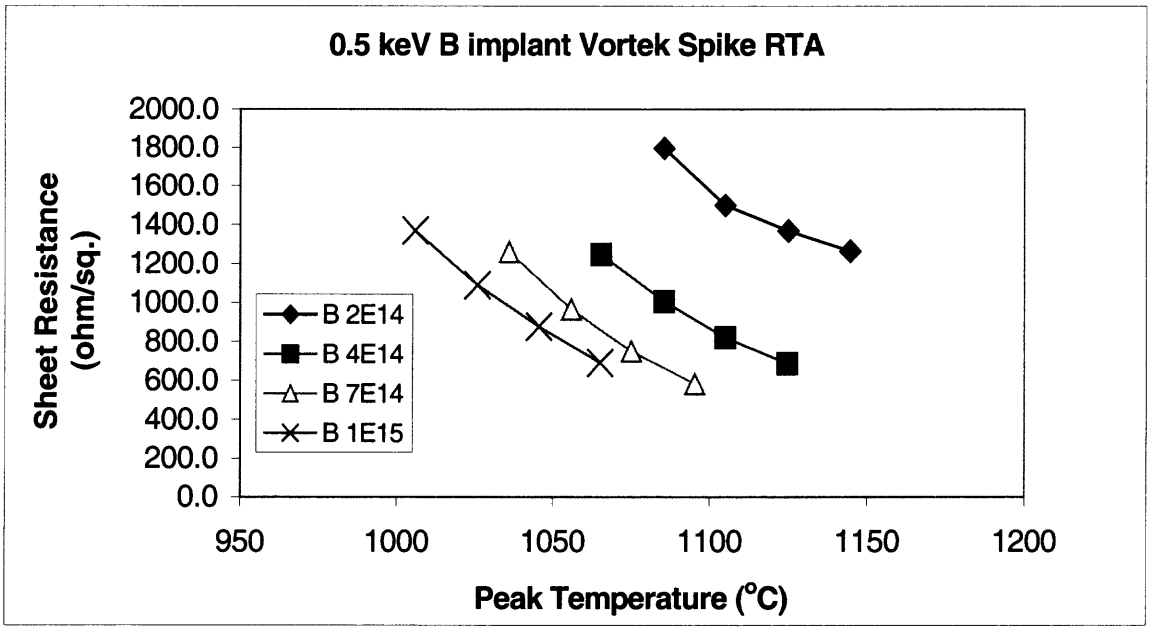

Figure A.3 Sheet resistance versus peak temperature for 0.5 KeV boron implants (Vortek spike RTA).

The Hall carrier density increases with implant dose. For a given dose, it tends to increase with annealing temperature.

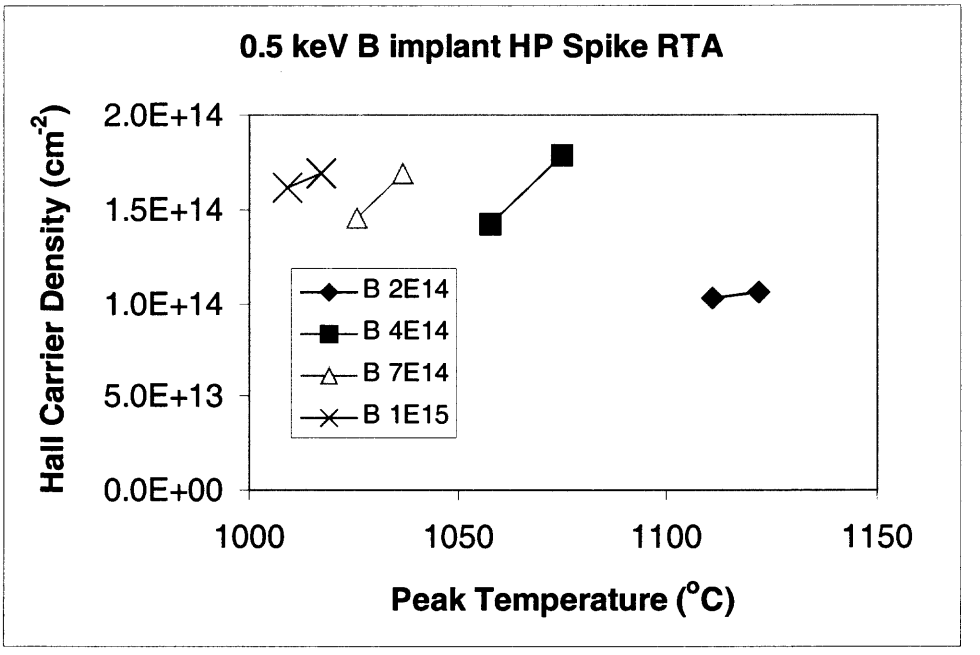

Figure A.4 Hall carrier density versus peak temperature for 0.5 KeV boron implants (HP spike RTA).

Hall carrier density is almost constant with increase in annealing temperature. However, as the implantation dose decreases, the Hall carrier density increases. For a constant dose, as the temperature increases, the Hall carrier density also increases. Similar results are observed for both ramp rates for the two spike annealing methods.

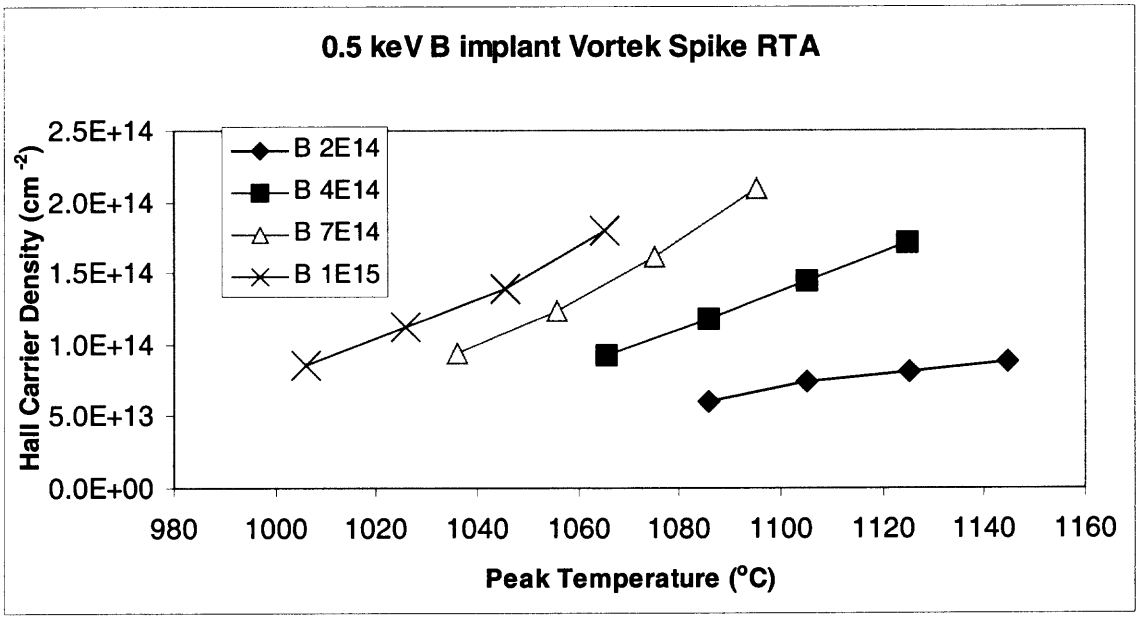

Figure A.5 Hall carrier density versus peak temperature for 0.5 KeV boron implants (Vortek spike RTA).

The activated fraction of boron increases with the increase in temperature and the activated fraction increases with the decrease in implantation dose. For a high implantation dose, the activation fraction is found to be in the range of 0.1 - 0.2 at low temperatures. For a low implantation dose of boron 2 x 10^{14} cm^{-2}, the activated fraction of boron is high, in the range of 0.5 - 0.6, approximately.

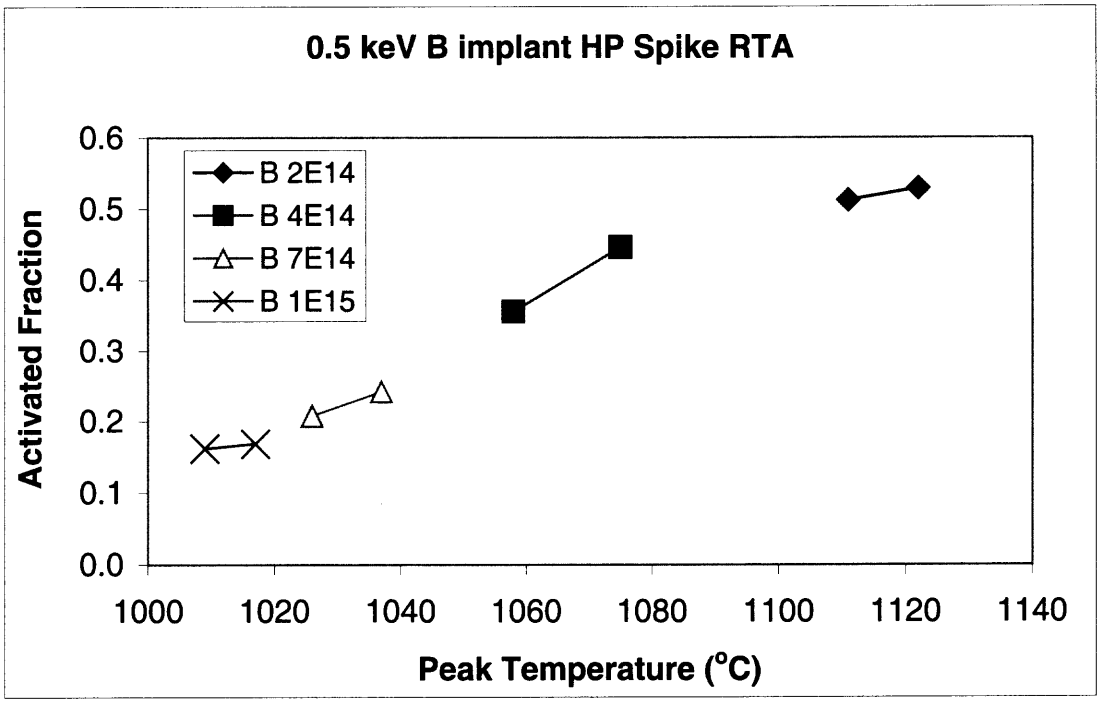

Figure A.6 Activated fraction versus peak temperature for 0.5 KeV boron implants (HP Spike RTA).

In Figure A.6, the activated fraction (Hall carrier density / Implant dose) is plotted as a function of the arc lamp spike anneal temperature for four doses (cm^{-2}) as indicated in the legend. It is conspicuous from the figure that, as the temperature increases, the activated fraction of boron increases, irrespective of the implant dose. The spike annealing is done at a ramp rate of 400 ^{o}C/sec. In general, the Boron Enhanced Diffusion (BED) increases with the implant dose. Further, it has been found that the diffusivity had very minimal influence on the electrical activated fraction.

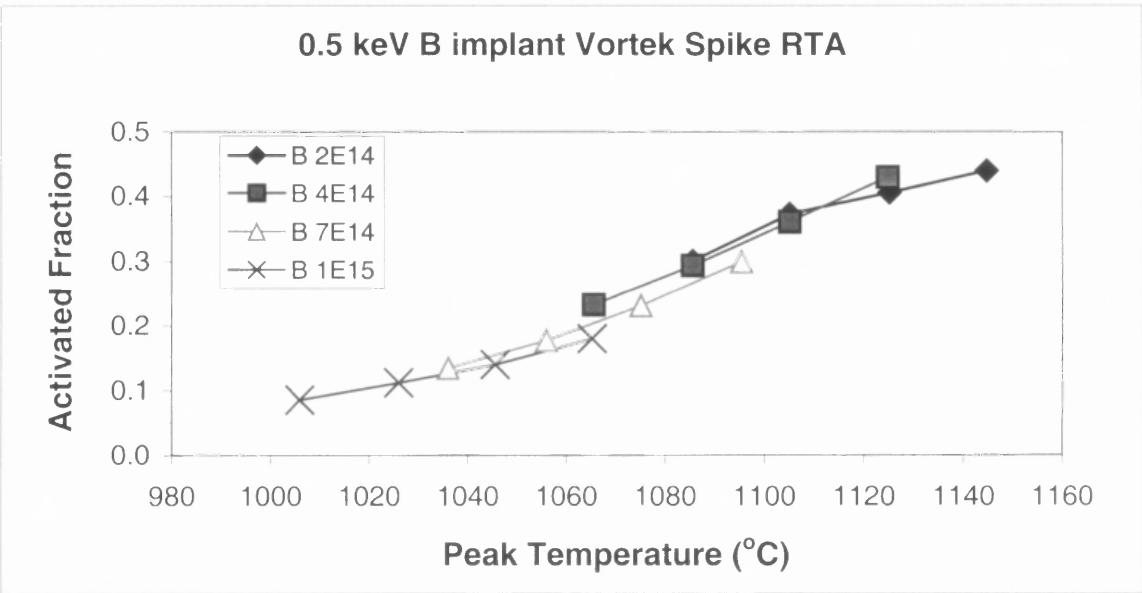

Figure A.7 Activated fraction versus peak temperature for 0.5 KeV boron implants (Vortek Spike RTA).

APPENDIX B

RESULTS OF PHOSPHORUS AND ARSENIC IMPLANTS

Electrical and junction depth data of n/p junctions formed by phosphorus implantation and spike annealing are presented here.

In Figure B.1, the sheet resistance decreases with increase in temperatures irrespective of the implanted dose. However, for high phosphorus implantation dose, the sheet resistance is found to be low at low temperatures. It is found to be high at low doses and at high temperatures. The sheet resistance is found to be almost constant for arsenic implants (independent of the dose) as the temperature is increased. It can also be seen from the figure that, even though the dose is high for arsenic, the sheet resistance is found to be low. The behavior of sheet resistance is almost similar in both spike annealing methods.

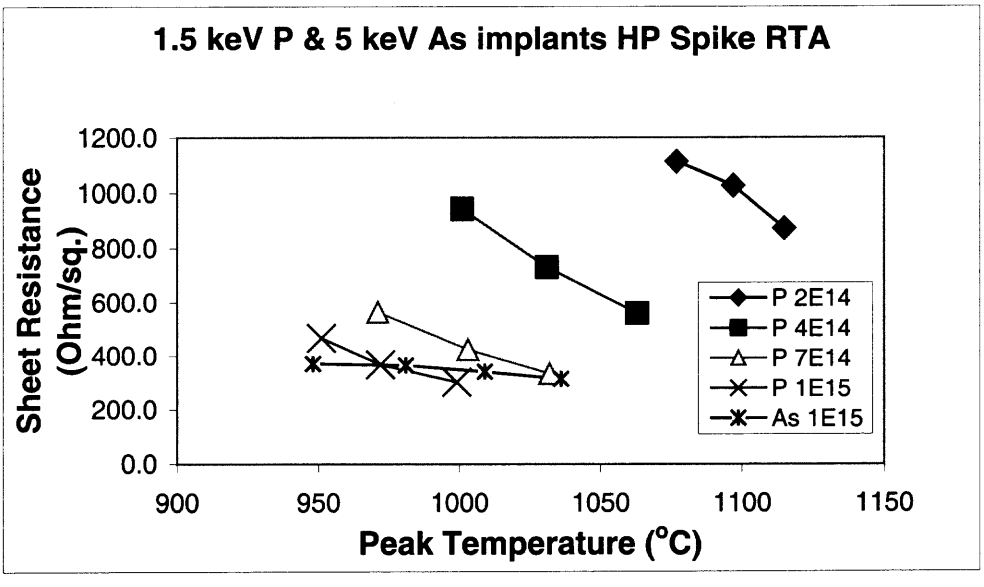

Figure B.1 Sheet resistance versus peak temperature for 1.5KeV phosphorus and 5 KeV arsenic implants (HP spike RTA).

Figure B.2 represents the same qualitative behavior as described in the Figure B.1. However, the temperatures tend to be lower for comparable R_s.

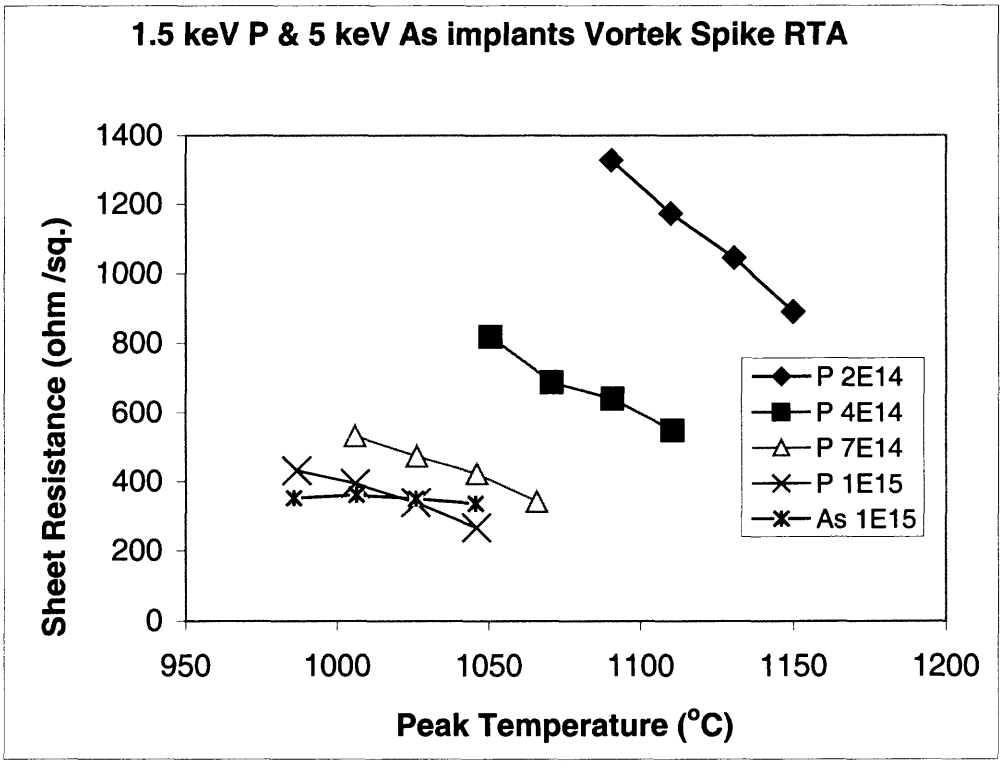

Figure B.2 Sheet resistance versus peak temperature for 1.5KeV phosphorus and arsenic implants (Vortek Spike RTA).

The activated fraction increases with the increase in temperature irrespective of the implant dose. However, arsenic showed higher activated fraction than phosphorus for the same implantation dose and at different energies.

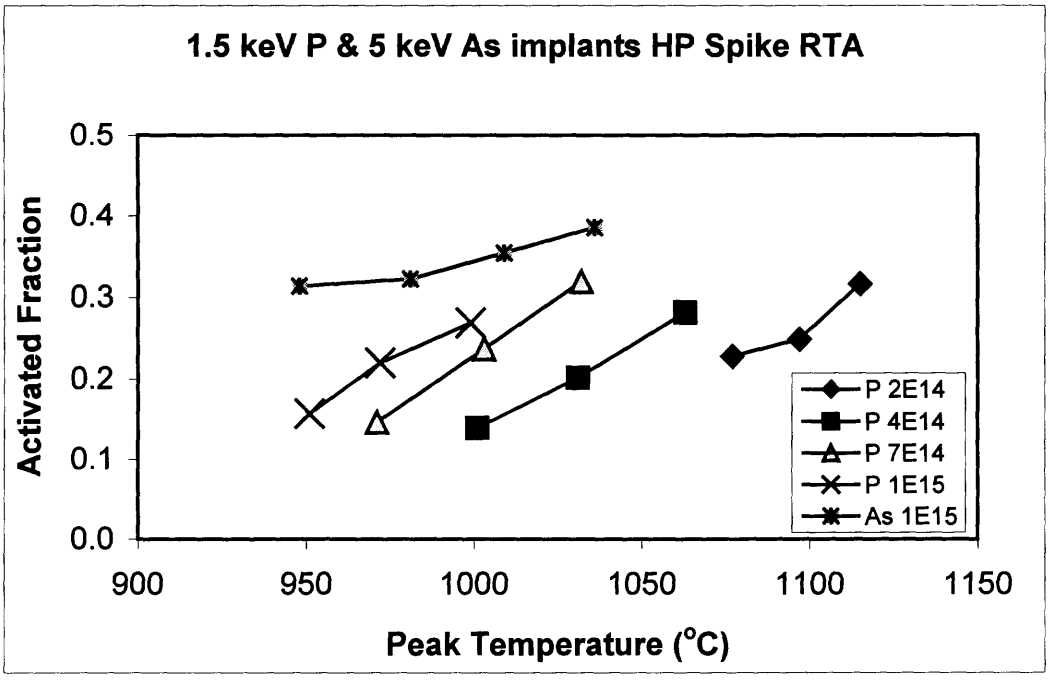

Figure B.3 Activated fraction versus peak temperature for 1.5KeV phosphorus and 5 KeV arsenic implants (HP spike RTA).

The activated fraction behavior is similar to that observed in Figure B.3. The activated fraction is almost constant even though there is a decrease in the implanted dose of phosphorus. In the case of arsenic, the activated fraction is high, and is almost constant with increase in temperature.

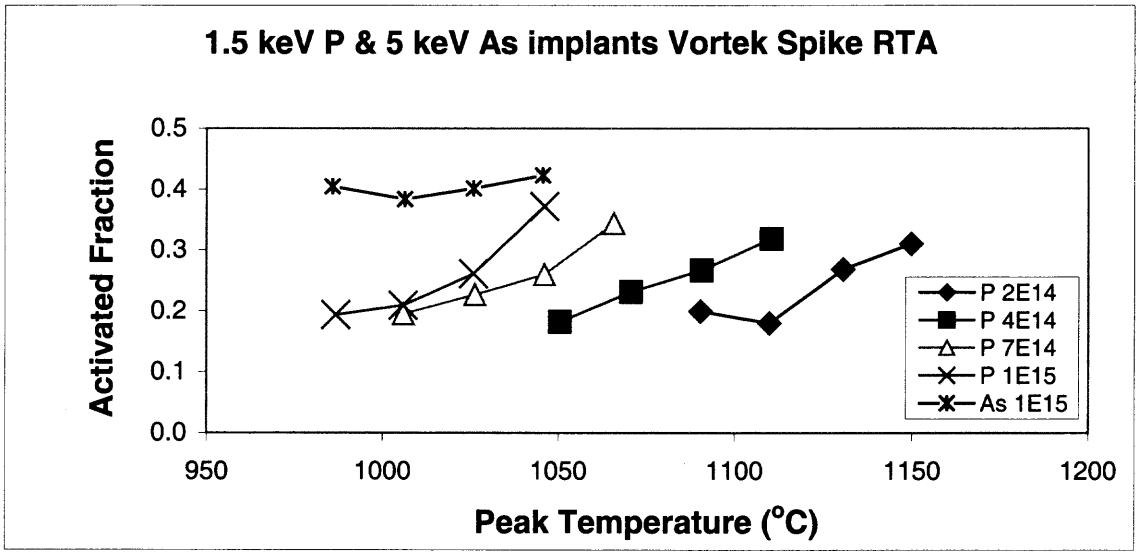

Figure B.4 Activated fraction versus peak temperature for 1.5KeV phosphorus and 5 KeV arsenic implants (Vortek spike RTA).

Hall carrier density decreases with the increase in temperature. For a high implant dose, the Hall carrier density is high and is low for a low implanted dose. Generally, the Hall carrier density increases with the increase in temperature for a constant dose. This behavior is observed for both the ramp rates.

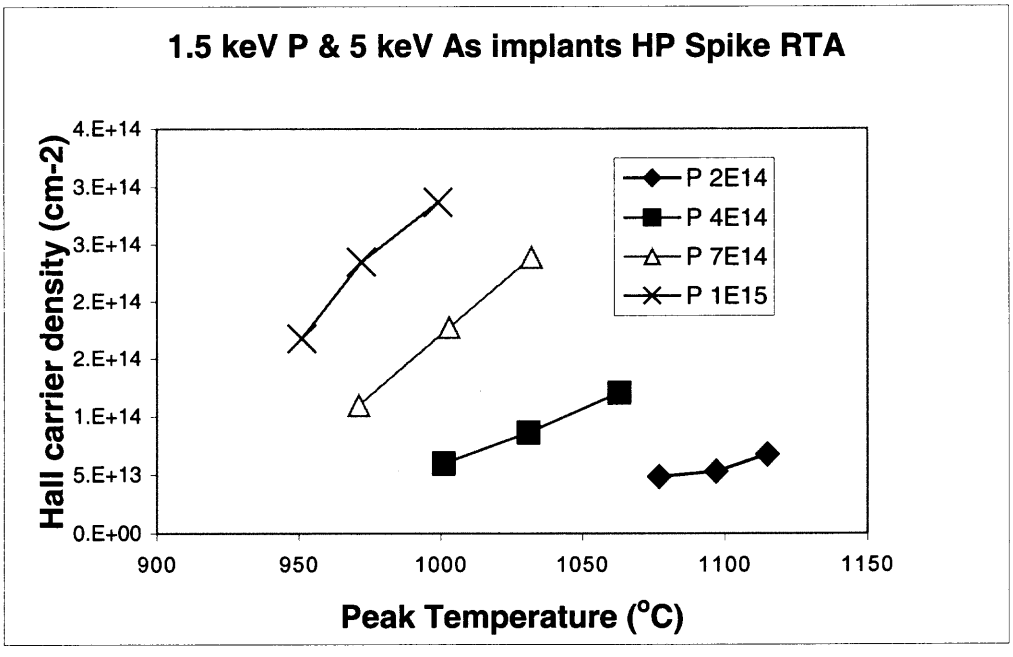

Figure B.5 Hall carrier density versus peak temperature for 1.5KeV phosphorus and 5 KeV arsenic implants (HP Spike RTA).

The Hall carrier density increases with implant dose. For a given dose, it tends to increase with annealing temperature.

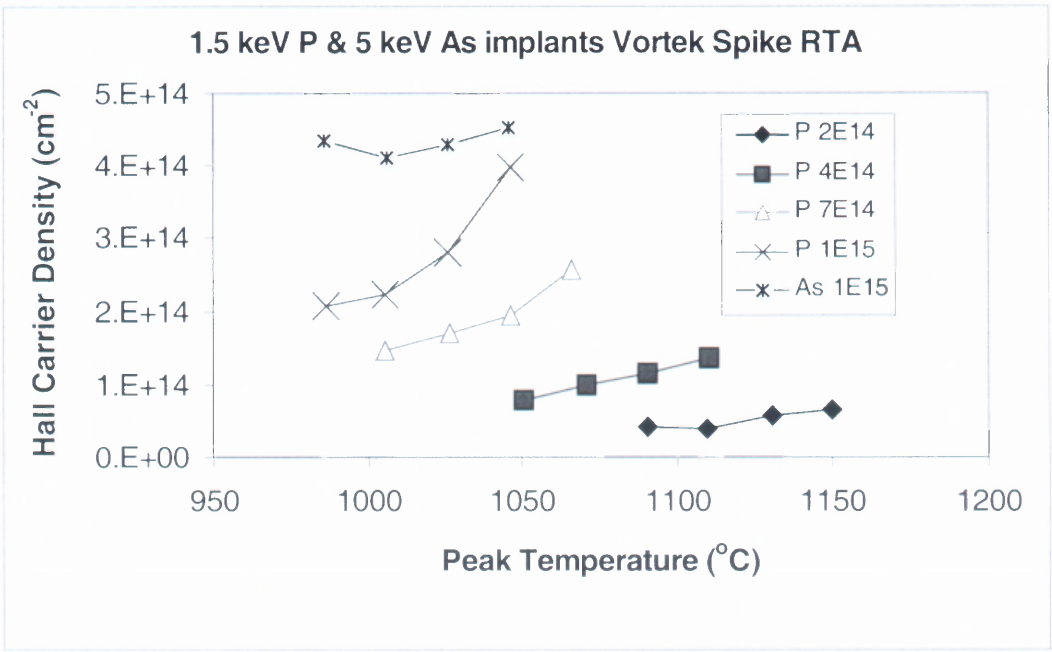

Figure B.6 Hall carrier density versus peak temperature for 1.5KeV phosphorus and 5 KeV arsenic implants (Vortek spike RTA).

The following table illustrates the sample data sheet of the experiments performed at NJIT.

Date Performed :				Notes and Comments :				
Name of the supplier :								
Annealing Details :								
Type of Implants :								
Dot	Dia 1	Dia 2	Area	(-)Voltmeter	Current	Current	**Avg. Current**	Two Lowest
No.	Divisions	Divisions	Sq.Cm	Reading (V)	Reading(Amp)	Density(dot)	**Density(chip)**	Avg. Dots
						(Amp/Sq.Cm)	**(Amp/Sq.Cm)**	
1	136	138	0.007853563	1	1.07E-08	1.36E-06		
2	161	154	0.010375173	1	2.60E-09	2.51E-07	**1.34E-05**	avg 3and4
3	124	123	0.006382275	1	9.40E-08	1.47E-05		
4	135	130	0.007343885	1	8.83E-08	1.20E-05		
1	111	113	0.005248681	1.002	4.32E-06	8.23E-04		
2	135	140	0.007908799	1.001	4.25E-06	5.37E-04	**4.83E-04**	avg2 and3
3	136	127	0.007227555	1.002	3.09E-06	4.28E-04		
4	118	124	0.006122833	1.001	3.15E-06	5.14E-04		
1	135	137	0.007739325	1.001	7.51E-06	9.70E-04	**9.95E-04**	avg1and2
2	135	136	0.007682834	1.001	7.86E-06	1.02E-03		
3	126	124	0.006537941	1.002	4.12E-05	6.30E-03		
4	109	125	0.005701449	1.001	2.33E-05	4.09E-03		
1	179	171	0.012808489	1	3.39E-08	2.64E-06		
2	135	127	0.007174411	1	4.77E-08	6.65E-06	**3.39E-06**	avg1and4
3	119	120	0.005975537	1	3.50E-08	5.86E-06		
4	114	117	0.005581353	1	2.31E-08	4.14E-06		
1	122	125	0.006381439	1.001	3.63E-08	5.69E-06		
2	146	138	0.008431031	1.001	2.80E-09	3.32E-07	**1.85E-06**	avg2and4
3	124	126	0.006537941	1.005	2.77E-08	4.24E-06		
4	138	147	0.008488778	1.001	2.86E-08	3.37E-06		
						(Amp/Sq.Cm)	**(Amp/Sq.Cm)**	
1	125	126	0.006590666	1.001	3.01E-09	4.57E-07		
2	131	133	0.007290741	1.001	3.39E-09	4.65E-07	**4.50E-07**	avg1and4
3	124	126	0.006537941	1.001	3.29E-09	5.03E-07		
4	134	124	0.006953048	1.001	3.08E-09	4.43E-07		
1	120	131	0.006578112	1.001	1.51E-08	2.29E-06		
2	132	126	0.006959743	1.001	1.10E-08	1.57E-06	**1.93E-06**	avg1and2
3	100	100	0.00418455	1.001	1.25E-04	2.99E-02		
4	116	120	0.005824893	1.001	1.94E-08	3.33E-06		
1	138	140	0.00808455	1.001	6.46E-09	7.99E-07		
2	129	127	0.006855548	1.001	2.20E-04	3.21E-02	**9.40E-07**	avg1and4
3	120	118	0.005925323	1.001	9.45E-09	1.59E-06		
4	131	133	0.007290741	1.001	7.90E-09	1.08E-06		
1	161	164	0.011048885	1	3.28E-08	2.97E-06		
2	158	155	0.010247963	1	9.50E-09	9.27E-07	**9.12E-07**	avg2and3
3	162	157	0.010642984	1.001	9.55E-09	8.97E-07		
4	150	155	0.009729078	1.001	1.02E-08	1.05E-06		
1	144	145	0.00873734	1.001	9.63E-09	1.10E-06	**1.44E-06**	avg1and2
2	174	172	0.012523521	1.001	2.23E-08	1.78E-06		
3	152	159	0.01011322	1.001	2.77E-08	2.74E-06		
4	151	146	0.009225259	1.001	2.65E-08	2.87E-06		
1	144	138	0.008315537	1	5.87E-09	7.06E-07		
2	162	165	0.011185302	1.001	1.39E-08	1.24E-06	**9.73E-07**	avg1and2
3	173	155	0.01122087	1.001	1.39E-08	1.24E-06		
4	168	160	0.01124807	1.002	2.33E-08	2.07E-06		

APPENDIX D

C++ PROGRAM FOR LEAKAGE CURRENT DENSITY

The following program evaluates leakage current density of shallow junctions.

```
#include<iostream.h>
#include<math.h>
#include<stdio.h>

double dia1[4], dia2[4], area[4], Vr[4],Curr[4],CurrDens[4], AvgCurrDens;

int chipid;
int i=0;

void bubblesort(double* ptr, int lmt)
{
        void order(double* , double*);
        int j,k;
        for(j=0;j<(lmt-1);j++)
                for(k=j+1;k<lmt;k++)
                        order(ptr+j,ptr+k);
}

void order (double * numb1, double* numb2)
{
        if(*numb1>*numb2)
        {
                double temp=*numb1;
                *numb1=*numb2;
                *numb2=temp;
        }
}

void main()
{
        cout<<"Enter the chipid"<<endl;
                cin>>chipid;


        for(i=0;i<4;i++)
        {
                cout<<"Enter the dia1 of the dot"<<endl;
                cin>>dia1[i];
```

```
            cout<<"Enter the dia2 of the dot"<<endl;
            cin>>dia2[i];


        area[i]=(3.14285714285714285714285571*dia1[i]*dia2[i]*0.01)/(137*137*4);

            cout<<"Enter the reading from the voltmeter"<<endl;
            cin>>Vr[i];

            cout<<"Enter the reading for the current"<<endl;
            cin>>Curr[i];

            CurrDens[i]=Curr[i]/area[i];

            cout<<endl;
        }

        bubblesort(CurrDens,4);

        AvgCurrDens=(CurrDens[0]+CurrDens[1])/2;


        for(i=0;i<4;i++)
                {
                        cout<<"The dia1 of the dot:\t"<<dia1[i]<<endl;

                        cout<<"The dia2 of the dot:\t"<<dia2[i]<<endl;


                        cout<<"The area of the dot:\t"<<area[i]<<endl;


                        cout<<"The reading from the voltmeter:\t"<<Vr[i]<<endl;

                        cout<<"The reading for the current:\t"<<Curr[i]<<endl;

                        cout<<"The Current Density is :\t"<<CurrDens[i]<<endl;
                }

        cout<<"The Average Current Density for the "<< chipid<<"
is:\t"<<AvgCurrDens;

        cout<<endl;
}
```

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