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ABSTRACT

FORMATION & CHARACTERIZATION OF p/n SHALLOW JUNCTIONS IN SUB-MICRON MOSFETs

by
Samrat G. Chawda

The formation of shallow junctions in the source and drain regions is a major challenge to the continued success of scaling of complementary metal oxide semiconductors (CMOS) circuits. The formation of these device structures requires low-energy ion implantation and rapid thermal annealing (RTA). One of the processes which has been shown to be advantageous is spike annealing, with fast ramping and short dwell time at maximum temperature. This work is a study of the effects of implant energy, implant dose and annealing cycles on the reverse-bias leakage current in the diode junction. The reverse-bias leakage is the study of junction quality. Low leakage is ideal, but for some experimental processes, leakage is found to be high. Experiments have been performed on p/n diode samples, which were annealed by various methods. The methods of annealing include spike anneals by (a) arc lamp, (b) incandescent lamp and (c) flash annealing. Implant conditions were typically ultra-low energy B implants (0.5 keV & 5 keV), which also included Ge pre-amorphization implants (PAI).

A general observation is that the junctions with least leakage are obtained for B implants without PAI. When the PAI step is included, the best shallow junctions are obtained if the PAI depth is greater than the junction depth, because of the damage produced by PAI. Flash annealing of B implants with PAI showed very high leakage, when compared to conventional spike annealing, apparently because it does not sufficiently anneal out the implant damage.

FORMATION & CHARACTERIZATION OF p/n SHALLOW JUNCTIONS IN SUB-MICRON MOSFETs

by
Samrat G. Chawda

A Thesis
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New Jersey Institute of Technology
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"To my Parents who are a constant source of support and encouragement, and who have taught me a few priceless treasures of sincerity, faith, hope and love."

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CHAPTER 1

INTRODUCTION

1.1 Overview of Shallow Junctions

Silicon based integrated circuits (ICs) have revolutionized the world for many years. ICs built up of many silicon devices (such as transistors and diodes), on a single chip are used everywhere from computer memory chips to cars to telephones.

The main growth of semiconductor IC industry has been the shrinking of transistors to smaller dimensions. This growth is well described by Moore's law [1]. Gordon Moore predicted in 1965 that for each new generation of memory chip and microprocessor unit on the market, the device size would reduce by 33%, the chip size would increase by 50%, and the number of components on a chip would quadruple every three years. So far, the trend continues to obey the law.

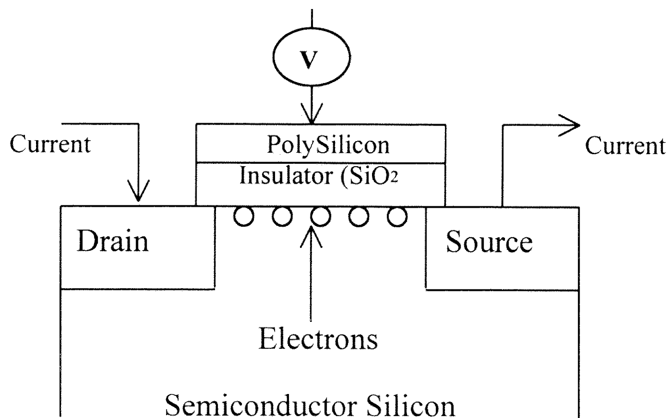

Figure 1.1 Schematic of a simple MOSFET.

The success of the metal oxide semiconductor field effect transistor (MOSFET) is due to the fact that it can be scaled to increasingly smaller dimensions, which results in improved performance.

MOSFET is a remarkably simple device. An n-channel MOSFET is shown schematically in Figure 1.1. It mainly consists of source and drain channel contacts, and a polysilicon gate electrode separated from the silicon by the gate insulator SiO_2. Considering a case where in voltage on the gate is positive and the current is flowing as shown, there is an accumulation of electrons. These electrons accumulate as shown in the figure making the channel between the source and drain conducting. This turns the transistor from off to on state.

In the ideal case, a MOSFET should behave like a switch, i.e. the device current drive should be high when the device is ON, and there should be minimal leakage current in the device when the device is OFF.

The growth of the semiconductor IC industry has been mainly through the shrinking of the transistor. Hence, work is in progress to increase the transistor packing density, to increase the circuit speed and lower the power dissipation. Most of the problems that arise during the front end process (FEP) of silicon device includes ultra shallow junction formation, leakage current with decreasing channel lengths and the need for inter-well isolation as packing density increases.

As the semiconductor device technology expands, there is a thrust for shallow junction depth (X_j) and lower sheet resistance (R_s). Figure 1.2 shows the International Technology Roadmap for Semiconductors (ITRS) requirements for junction depth and sheet resistance with the technology and the year of introduction [2]. It can be clearly

seen that there is a decrease in R_S and X_j along with the technology, which is the most essential challenge for researchers today.

The most challenging part of the front-end process development is the source-drain contact module. Source-drain junction extensions needs to be shallower. However, this need leads to high series resistance, which negatively impacts drive current and circuit performance. Metallization choices such as silicidation can achieve low contact resistance, but may increase the junction leakage current that results in increased off current and stand-by power.

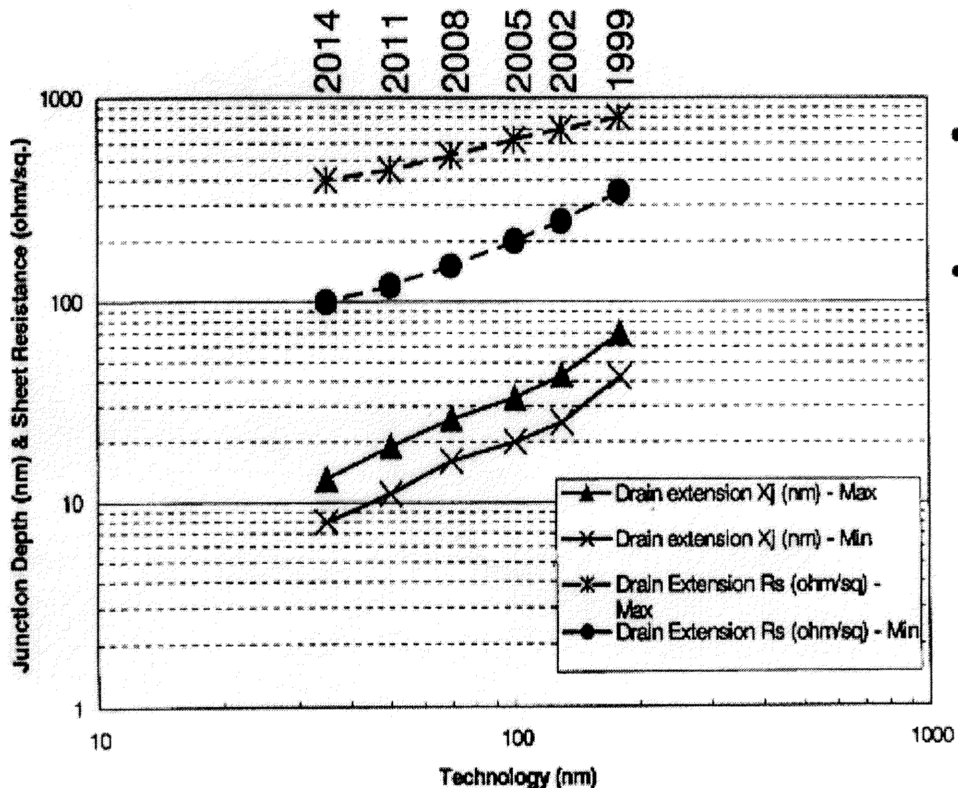

Figure 1.2 Required Junction depth and Sheet Resistance according to the 1999 ITRS scaled with technology and the year of introduction [2].

In this thesis, the main goal was to compare the junction leakage current with its implant temperature, the implant dose and implant energy. Considering the current leakage from the junction of MOSFET, discussion about the formation of MOSFET, its characterization techniques and the different models that are commonly used for ion implantation and diffusion are discussed here.

The experimental part focuses on patterning the p-n junction diodes and etching the samples to obtain desired patterns on wafers. The next part is the usage of semiconductor probe station to measure leakage current in the samples prepared by various methods. The discussion mainly considers the leakage current along with the implant energy, the implant dose, and comparison with the results from the literature.

CHAPTER 2

SHALLOW JUNCTION PROCESS FUNDAMENTALS

2.1 Ion Implantation

Ion implantation can be described as the introduction of ionized-projectile atoms (dopant ions) into targets with enough energy to penetrate beyond the surface regions. The incident ions come to rest in the substrate material via electronic and nuclear stopping. In the case of electronic stopping, the energy loss occurs through the excitation and ionization of target electrons, where as, in the case of nuclear stopping, there is a transfer of kinetic energy to the target atoms. In the second case, often, there is displacement of atoms from their positions and this causes point defects such as Frenkel pair vacancies and interstitials. Figure 2.1 shows the schematics of this process.

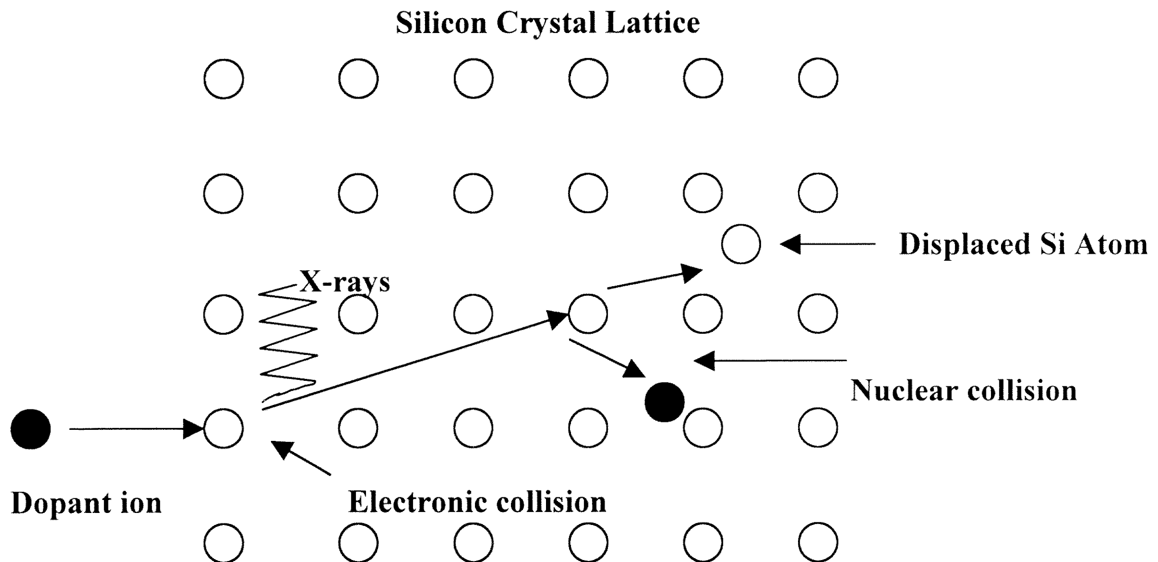

Figure 2.1 A schematic of the energy loss mechanisms and displacements of lattice atoms [3].

Advances in ion implantation have made it the most preferred method to introduce impurities into silicon to achieve reproducible concentration and depth profiles. Currently the most promising option for shallow junctions formation is the low energy ion implantation. For many reasons such as uniformity, reproducibility, and cleanliness, ion implantation is presently the method of choice for the formation of source/drain junctions and the channel.

During implantation, when the dopants enter the crystal, the dopants give up their energy to the lattice due to collisions, and finally come to rest at some average penetration depth called projected range (R_p). This range may vary from one semiconductor to another, depending upon the type of impurity and its implantation energy. Figure 2.2 shows the even distribution of ions about the projected range that occurs during implantation.

The following Gaussian formula shows the distribution of the implanted dose, Φ ions/cm^2 [4]:

$$N(x) = \frac{\phi}{\sqrt{2\pi}\Delta R_P} \exp\left[\frac{-1}{2}\left(\frac{x - R_P}{\Delta R_P}\right)^2\right] \tag{2.1}$$

where, ΔR_p = straggle, measures the half-width of the distribution at $e^{-1/2}$ of the peak, as in Figure 2.2. Both R_p and ΔR_p increase with increasing implantation energy. These parameters are shown as a function of energy for various implant species into silicon in Figure 2.3 and Figure 2.4.

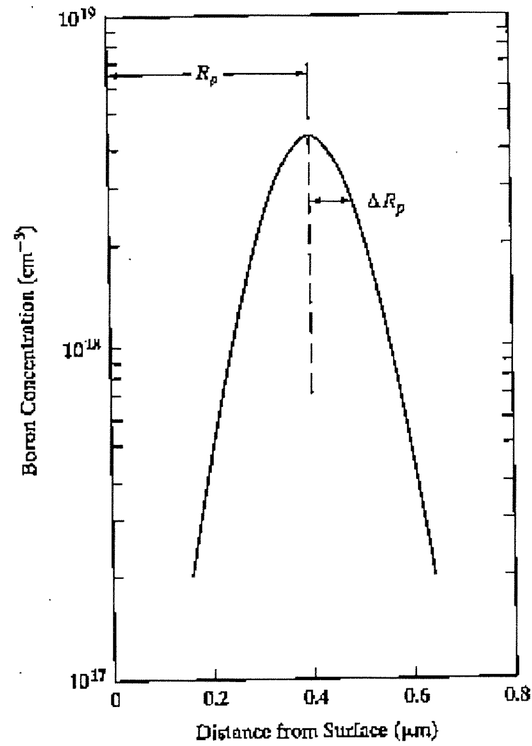

Figure 2.2 Gaussian distribution of impurities of boron atoms about a projected range R_p [4].

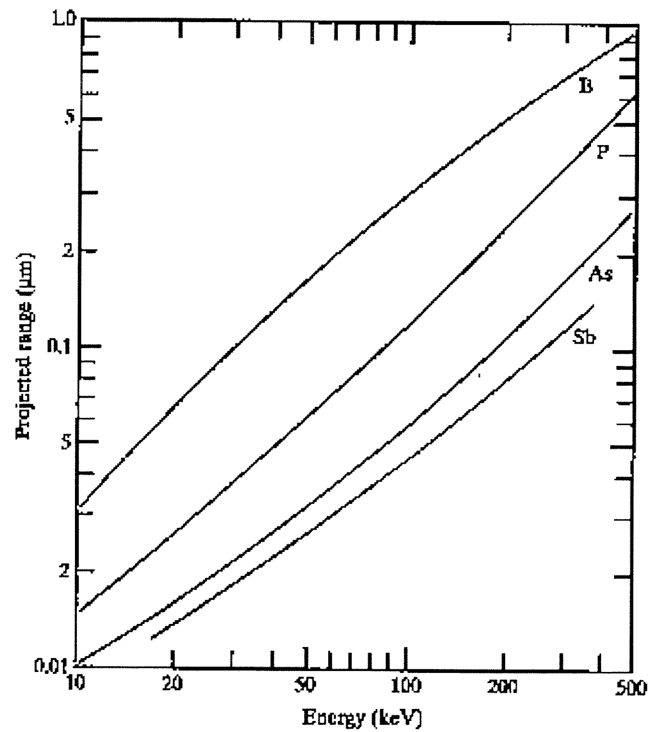

Figure 2.3 Projected Range as a function of implant energy in Si [4].

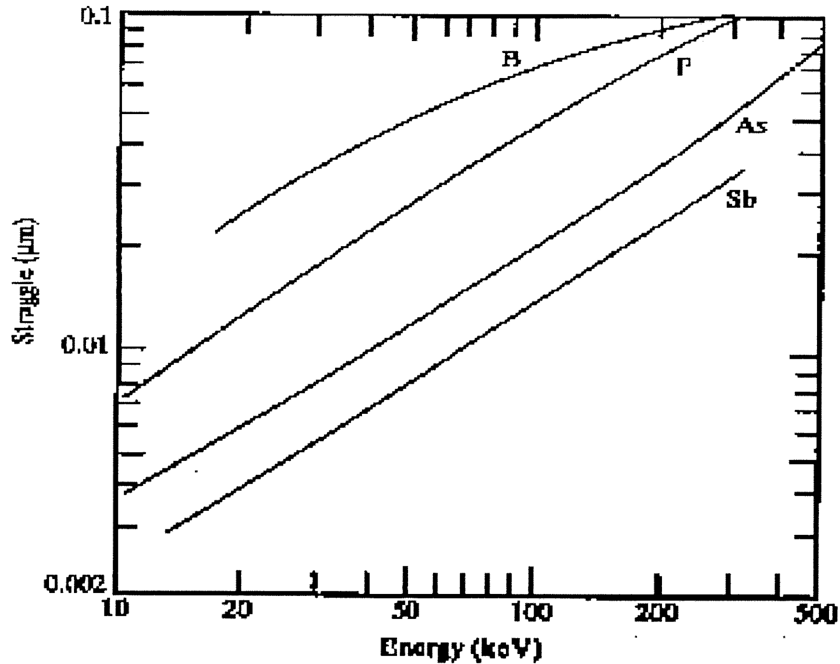

Figure 2.4 Straggle as a function of implant energy in Si [4].

One of the most pertinent issues associated with ion implantation is the inherent introduction of excess point defects. During thermal processing subsequent to ion implantation, excess point defects, namely interstitials, precipitate into extended defects in order to reduce the free energy of the system [5]. These point defects are of higher magnitude than the dopant concentration. However, these excess point defects quickly recombine and lead to roughly a net damage "+1" [6]. This has been found to be a reasonable approximation for modeling the extent of transient enhanced diffusion at higher temperatures. However, the validity of using a "+1" model for parameter extraction at lower temperature is not clear [6].

2.1.1 Implant Damage

The knowledge of implant damage is necessary since it is closely related to the electrical properties of the implanted region. To build functional devices, the damaged lattice structure must be repaired, and the implanted dopant atoms must be electrically activated.

2.1.2 Channeling

The crystallinity of a silicon wafer has quite dramatic effects on their implant profile. There are planar and axial channels present in crystalline silicon [7]. In the case of amorphous silicon, the atoms are assumed to be randomly distributed in a way, which conforms to over all packing density, local atomic co-ordination and atomic size constraint [8].

These types of symmetry explain that crystals have openings through which ions can travel long distances without encountering a target atom on its way. An ion beam can either be directly aligned along such channel directions or will allow the incident ions to be scattered into a channel. This allows the dopant atom to travel far deep into the crystal, before coming to rest. This is known as channeling.

It is clearly undesirable to allow channeling to occur if an accurately tailored impurity profile is required in a crystal. In semiconductor production, the ions do tend to be small and the substrate material into which implantation is done are extremely high quality crystals. The unwanted doping at depths beyond R_P degrades the dopant profile [9]. Either tilting the crystal axes, of the substrate material, to about 7° or to use a large dose of self-ions to amorphize the target [9] can reduce channeling. After implanting the impurities, the material is rapidly annealed. This is done in order to regenerate the crystalline structure.

Some of the uses of ion implantation are:

- Wide range of dopants with no masking complications.
- Profile control independent of temperature.
- Precise control of ion dose.
- Fine control (to the limit of photolithography) of lateral dimensions.
- High degree of uniformity of impurity concentration for each wafer and from wafer to wafer.

2.2 Annealing Techniques

The doping of silicon crystal by ion implantation will result in collisions between the ions and the lattice atoms. This will in turn create lattice damage. This damage can be removed by heating the silicon crystal after implantation. This process is termed annealing.

Continued device scaling requires the formation of ever-shallower, low-resistivity junctions [9]. The major trends in conventional ion implantation and rapid thermal annealing (RTA) in recent years have been the use of ultra low energy implants and spike anneals for the formation of ultra shallow junctions [10]. RTA with a short dwell time at maximum temperature is used with ion implantation to form shallow junctions and polycrystalline silicon gate electrodes in complementary metal oxide semiconductor (CMOS) circuits [11]. During annealing, the main problem, which arises, is that of Transient Enhanced Diffusion (TED). To reduce the undesirable effects of TED and thermal de-activation of dopants, fast thermal cycles such as spike annealing/soak annealing are required.

Rapid thermal processing methods are also used to form, anneal, or reoxidize gate dielectrics such as nitrided SiO_2 and metal oxides with high dielectric constants [12,13]. Temperature control and uniformity is critical for thin gate oxide films grown by thermal oxidation.

2.2.1 Rapid Thermal Annealing (RTA) Procedures

Most of the RTA techniques fall in two broad categories: (1) rapid wafer transfer between a steady heat source and a heat sink. (2) a fixed or rotating wafer heated by rapid modulation of heat source [11].

Various methods or procedures that are used for thermal annealing are:

- Furnace and hot plate heating
- Lamp based heating

Basically, in the above processes, heat is exchanged by radiation, gas convection and gas thermal conduction. Spike annealing techniques have been introduced to control dopant diffusion in shallow junction formation [14] and it is integrated with contact junction and gate electrode activation [15].

Figure 2.5 shows a typical temperature vs time graph for spike anneals with an arc and incandescent lamp. Spike annealing is done by abruptly turning off the lamp power at or near peak temperature. Heating rates are in the range of 100 to 400 °C/s. The wafers cool by chamber absorption of the emitted radiation at rates upto 150 °C/s [11]. The peaks are different for both the types of annealing. The arc lamp method produces a sharper temperature peak because an arc lamp can turn off more rapidly than incandescent lamps. In this thesis, a set of wafers annealed by arc and incandescent lamps

have been evaluated utilizing the leakage current method. Comparisons of spike annealing and soak annealing is discussed in the next section.

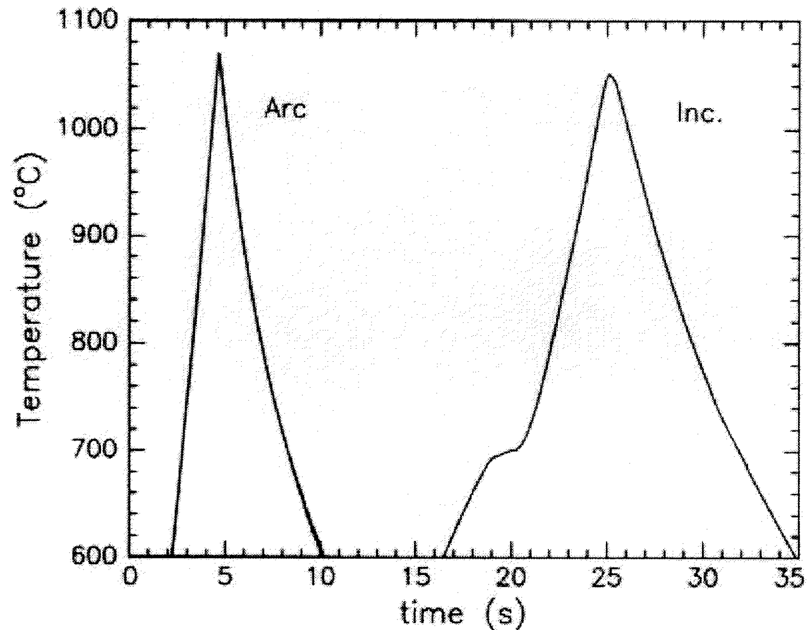

Figure 2.5 Temperature v*s* time for spike anneals with an arc and incandescent lamp system.

2.2.2 Soak Annealing and Spike Annealing

2.2.2.1 Soak Annealing. A typical annealing profile using rapid thermal processing involves ramping up to a target temperature, (e.g., 1000 °C), a soak time at this target temperature, (10 s) and then ramping down to ~200 °C at a rate of ~50 °C/sec [16].

This type of annealing is termed as soak annealing. Here, generally high ramp rates are favored, which reduces the total residence time at the high temperature regime, which in turn reduces the TED and intrinsic boron diffusion.

2.2.2.2 Spike Annealing. In spike annealing, the soak time has been reduced to ~1sec or even lesser time. The approach, here, is to minimize the diffusion of boron, by minimizing the soak time and also adopting relatively high ramp rates [16]. A typical graph of soak and spike annealing is shown in Figure 2.5.

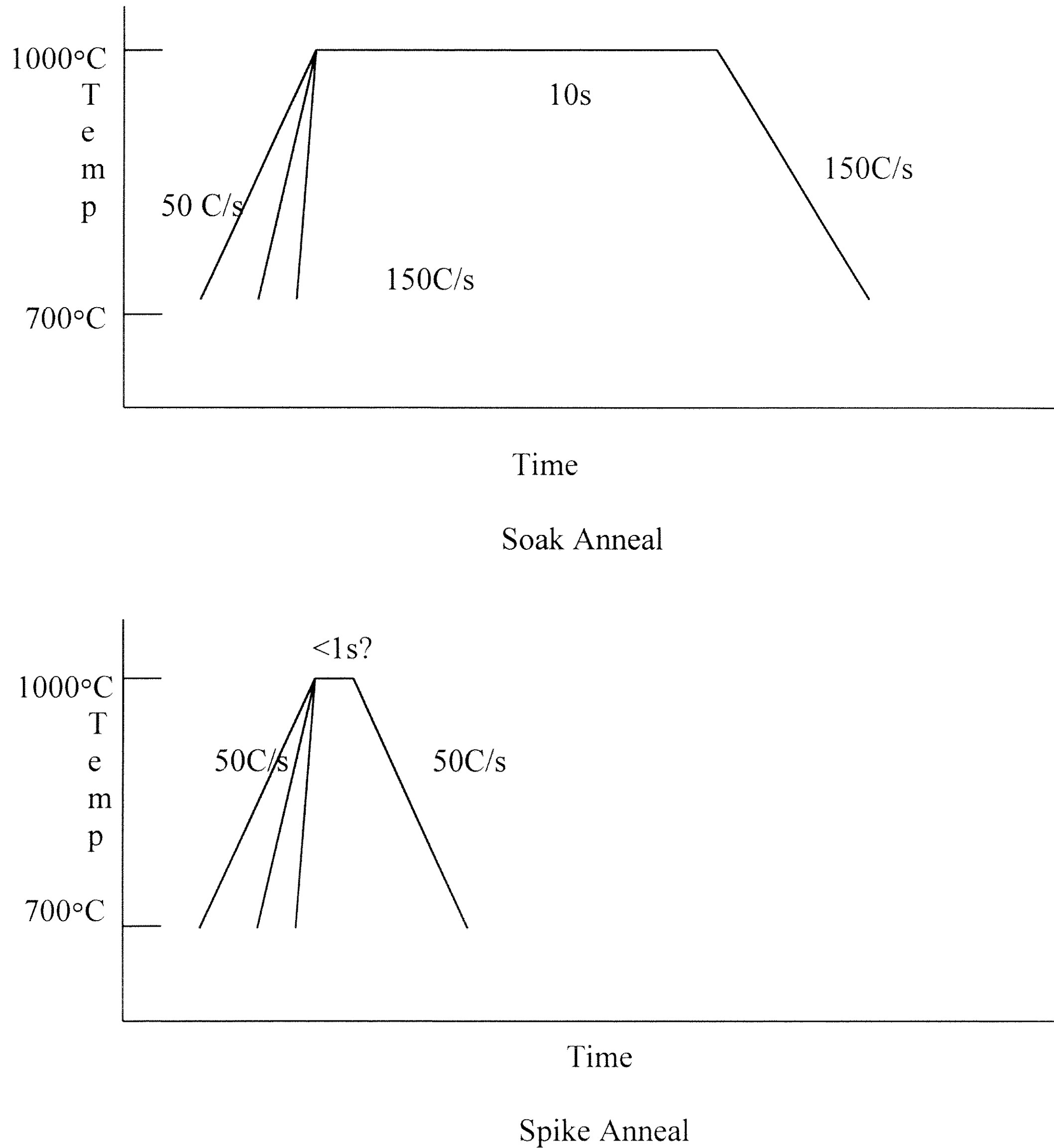

Figure 2.6 Soak Vs Spike anneal [17].

Spike annealing techniques were introduced to control dopant diffusion in shallow junction formation [14]. Current spike annealing methods use infrared heating characterized by near thermal equilibrium across the thickness of the wafer [11].

2.2.3 Importance of Spike Annealing

The formation of junction depth requires annealing at the highest temperature possible while limiting the total thermal budget for diffusion [18]. Spike annealing meets the above requirements. Spike annealing has been deployed to control dopant diffusion [11].

2.3 Diffusion

Diffusion is a phenomenon by which one chemical constituent moves within another as a result of the presence of chemical potential gradient [19]. The ion implantation technique for doping advanced silicon devices induces a huge super-saturation of point defects in the silicon crystal. This super-saturation leads to anomalous broadening of dopant profile during the high temperature activation anneal [20]. This phenomenon is known as the Transient Enhanced Diffusion (TED). TED is particularly noticeable and problematic for controlling boron diffusion.

During implantation of boron into silicon, high concentration peak of the implanted boron profile, which is electrically inactive, does not diffuse. TED makes it difficult to fabricate modern silicon based devices.

The enhanced diffusion of dopants such as boron and phosphorous can be as large as the implanted depth [21]. Some other TED trends include a larger displacement at lower temperature [22] and an increase in duration of anneal resulting from increased

implant dose and energy [23]. This poses a challenge to the formation of ultra shallow junctions and research is needed to elucidate optimum conditions for TED reduction.

2.3.1 Mechanisms of Diffusion

The possible mechanisms of diffusion of an impurity atom, A, in silicon is shown in Figure 2.6 [24]. In Figure 2.6, V and I denote vacancies and interstitials. Subscript I and s indicate interstitial and substitutional positions of the foreign atoms. AV is the pair of A and V and AI the pair of A and I.

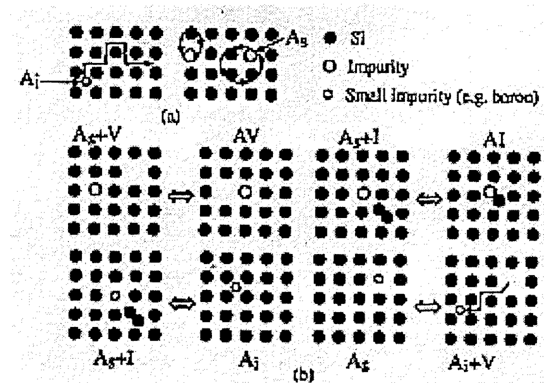

Figure 2.7 Schematic representation of (a) direct and (b) indirect diffusion mechanisms of an impurity atom A (open circle) in a solid [24].

Figure 2.7 and Figure 2.8 show the profile of boron concentration vs depth which were obtained in an experiment to study the effect of Si-implant damage on the diffusion of B in a delta-doped layer.

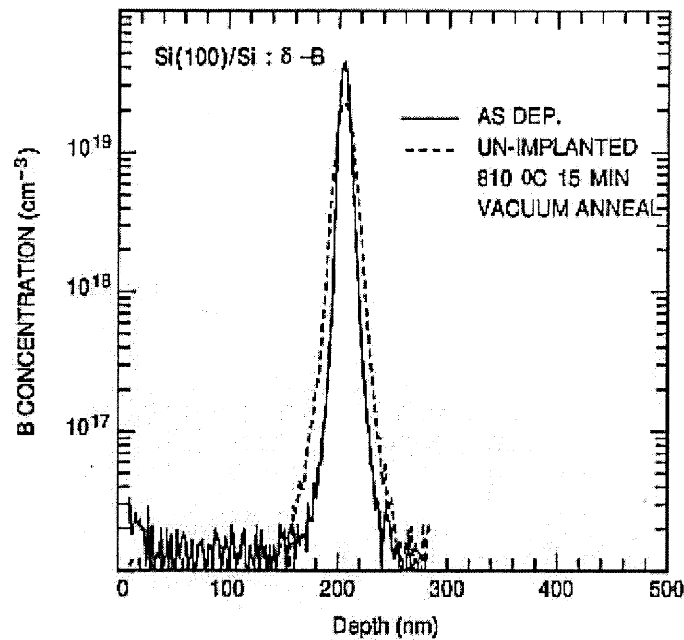

Figure 2.8 Boron concentration vs depth at equilibrium.

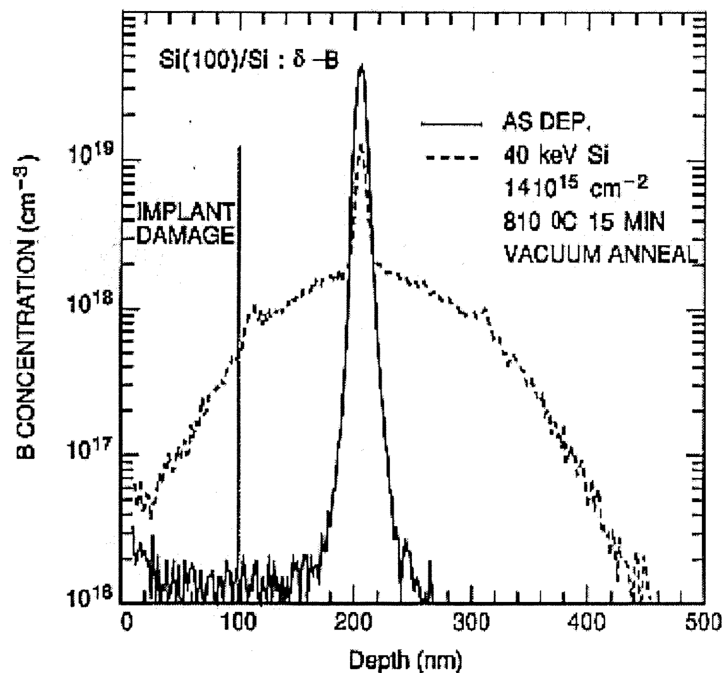

Figure 2.9 Boron concentration vs depth before after implantation.

The conclusions drawn by comparing Figure 2.7 and Figure 2.8 is that the TED from the Si implant damage greatly increases the diffusion broadening of the delta-doped B layer. Also the dopant atoms are more uniformly distributed after annealing and there is a noticeable amount of displacement of the dopant species (boron) during annealing.

It was found that the boron junction depth after annealing is shallower in BF^{2+} implant than in equivalent B^+ implant [26,27]. However, it is still unclear whether this behavior originates from physical damage or from the chemical effect of fluorine.

2.3.2 Preamorphization with Germanium

Traditional ion-implantation and RTP achieve the X_j/R_S values necessary because B^+ implants have limited enhanced activation and non-equilibrium enhanced diffusion [28]. Low energy implants confine defects close to surface, minimizing the effects of defect enhanced diffusion [29]. Germanium pre-amorphization can prevent channeling and activation.

Germanium is considered more useful than Si for implanting as a pre-amorphizing agent, as it is the heavier of the two. Low energy germanium implant pre-amorphization alone has not been very effective in preventing the diffusion of excess Si interstitials under certain conditions [30], thereby inducing TED upon dopant activation.

CHAPTER 3

MODELS OF ION IMPLANTATION AND DIFFUSION

There is an increasing need to understand in detail the dependence of implanted impurity profiles and implant-induced damage profiles in silicon on all key implant profiles. This need is for both technology and manufacturing equipment development. There are many reasons for the need to understand the above stated points. Some of them include largely reduced thermal budgets in IC processing, with heavy emphasis on control of equipment and process costs, and the need for rigid manufacturing control [31]. This shows a way to compute efficient models. These models greatly facilitate technology development and implementation in manufacturing, improved manufacturing process control and the development of new tools that can be executed more efficiently.

The models are mainly used to predict and know the theory of distribution of implanted ions in a crystal. In this chapter, a general explanation of models that predict the direction of ions into a crystal after implantation and diffusion is presented. The ion implantation models are used to predict the initial ion distribution and the diffusion models are used to understand the final distribution of dopant species.

3.1 Ion Implantation Models

Ion implantation is a key process in the Si integrated circuit technology. B^+ ion implantation is one of the most useful p-type doping processes in Si. It is vital to determine as-implanted and post-anneal impurity distributions with high accuracy.

Presently, there are many models used to understand the theory of ion implantation and to predict the final ion distribution. The Monte Carlo model for ion implantation is called TRIM (Transport of Ions in Matter). In the Monte Carlo approach, ion implantation is simulated by following the history of an energetic ion through successive collisions with the target atoms using binary collision approximation [19]. Here many individual ion histories are simulated, so that by summing up over all the ion histories, it is possible to obtain a representation of the ion distribution.

Following are some theoretical models that are developed for determining implantation profiles:

3.1.1 LSS Theory

Lindhard, Scharff and Schiott culminated this theory in 1963. This theory mainly explains or allows the stopping powers to be calculated for any arbitrary atomic species and elemental targets within a factor of two [7]. This theory mainly predicts the range R and the projected range R_P [19]. Here the range can be termed as the total distance that an ion travels in the target atom before coming to rest. R_P is the penetration depth of the implanted ions along the implantation direction.

3.1.2 Gaussian Distribution

The total number of ions that are distributed after implantation can be explained with the help of Gaussian distribution, which is given by equation 3.1 [7]:

$$C(x) = C_P \exp\left(-\frac{(x - R_P)^2}{2\Delta R_P^{\;2}} \right) \tag{3.1}$$

where, R_P is the average projected range normal to the surface, ΔR_P is the standard deviation about the range and C_P is the peak concentration where the Gaussian is centered. The total number of ions implanted is defined as the dose and is given by equation 3.2 [7].

$$Q = \int_{-\infty}^{\infty} C(x)dx \tag{3.2}$$

3.1.3 Pearson's Equations

These equations give good agreement between predicted and experimental profiles in all amorphous materials. The integral representation of the moments is not particularly convenient, so in practice the equivalent moments are described by coefficients in a functional form known as Pearson's equations. These are characterized by four moments R_P, ΔR_P, skewness, and kurtosis. These moments can be explained by the following equations [7]:

First Moment is the projected range,

$$R_P = \frac{1}{Q} \int_{-\infty}^{\infty} xC(x)dx \tag{3.3}$$

The second moment is the straggle or standard deviation,

$$\Delta R_P = \sqrt{\frac{1}{Q} \int_{-\infty}^{\infty} (x - R_P)^2 C(x)dx} \tag{3.4}$$

The third moment describes the skewness (γ) and is given by,

$$\gamma = \frac{\int_{-\infty}^{\infty} (x - R_P)^3 c(x)dx}{Q \Delta R_P{}^4} \tag{3.5}$$

and the fourth moment is the kurtosis,

$$\beta = \frac{\int_{-\infty}^{\infty}(x - R_p)^4 C(x)dx}{Q\Delta R_p^{\ 4}} \tag{3.6}$$

These four moments can be used to obtain a more accurate description of a wide range of implanted species in silicon [7]. The above set of equations represents some theoretical models for ion implantation. The most widely used model these days is the simulation model TRIM. This is a PC based Monte Carlo range and damage simulation program. TRIM assumes that the target material is amorphous and consequently provides a very useful first-approximation to the atomic range and damage distribution in multi-element and multi-layer materials [19]. TRIM is one of the main simulation programs of a group of programs in SRIM (Stopping and Range of Ions in Matter). SRIM is a group of programs which calculate the stopping and range of ions (upto 2 GeV/amu) into matter using a quantum mechanical treatment of ion-atom collisions [32].

3.2 Diffusion Modeling

One of the important physical processes during thermal processing is the prediction of the movement of dopant atoms in Si. Mathematical simulations are usually capable of predicting the movement of dopants. The main reason for this prediction to be made is to facilitate the process engineers to minimize the number of process steps required during technology development [19]. There are several simulation programs, which are being used today. The most common of them is SUPREM (Stanford University Process Engineering Model). SUPREM III covers the modeling of diffusion in one-dimensional scheme while SUPREM IV covers two-dimensional modeling.

3.2.1 SUPREM Models for Boron

Fair and Tsai proposed several models, which are used in SUPREM III and which are based on the vacancy model under non-oxidizing conditions [19]. Since diffusion is related to both dopant/interstitial and dopant/vacancy interactions, these models do not accurately reflect physical processes that are occurring on an atomic scale [19]. But the Fair and Tsai models are useful, since they provide an accurate representation of the diffusion profile for the common dopants.

These models assume that the diffusivity of an ionized dopant atom is based on the sum of the diffusivities of neutral vacancies and ionized vacancies, weighted by the probability of their existence [19]. These models further predict that there are four possible states of vacancy-the-neutral-vacancy V^o, the single-negatively-charged-vacancy V^{-1}, the double-negatively-charged-vacancy V^{-2} and the single-positively-charged-vacancy V^{+1}. During extrinsic diffusion, each contribution must be modified by the ratio of the doping level to the intrinsic carrier concentration raised to the power of the charge state. Thus, the effective diffusion coefficient, D, under non-oxidizing conditions can be calculated from the sum of all the individual vacancy components. The effective D is given by Equation 3.7 [19]:

$$D = D^o + D^-(\frac{n}{n_i}) + D^{2-}(\frac{n}{n_i})^2 + D^+(\frac{n_i}{n}) \quad (3.7)$$

where, n is the carrier concentration resulting from dopant ionization and n_i is the intrinsic carrier concentration at the diffusion temperature. In Equation 6.7, the individual diffusivities on the right hand side of the equation correspond to the interaction between dopant atoms and neutral or charged vacancies.

CHAPTER 4

CHARACTERIZATION TECNHIQUES

4.1 Analytical Techniques

4.1.1 Secondary Ion Mass Spectroscopy (SIMS)

SIMS provides a direct method for measuring the depth profile of an impurity in a diffused layer. It is considered to be one of the most versatile analytical techniques for semiconductor characterization. A growing number of books, conferences and workshops specializing in SIMS [8] address the wide range of applications and technique improvements.

The basis of SIMS is to destructively remove the material from the sample by primary ion sputtering as shown in Figure 4.1. These incident ions (primary) loose their energy mainly by momentum transfer as they come to rest within the solid. These primary ions in turn displace atoms within the solid. The displaced atoms (secondary) are detected by mass spectrometer and the profiling is done. This interaction between the primary and the secondary ions introduces a issue of atomic mixing which makes it difficult to measure the area closer to the surface. When the primary atoms knock the sample, they replace atoms from the sample. These atoms can leave their sites with enough energy to knock out other atoms which, inturn, knocks out others. This effect is called cascade effect [19]. In order to over come the cascade effect, the use of primary ion beam with low energy is preferred. The main use of SIMS is to measure the dopant concentration versus depth. It is also used to determine the diffusion depths and can be used for measurements of implanted samples before and after annealing [33].

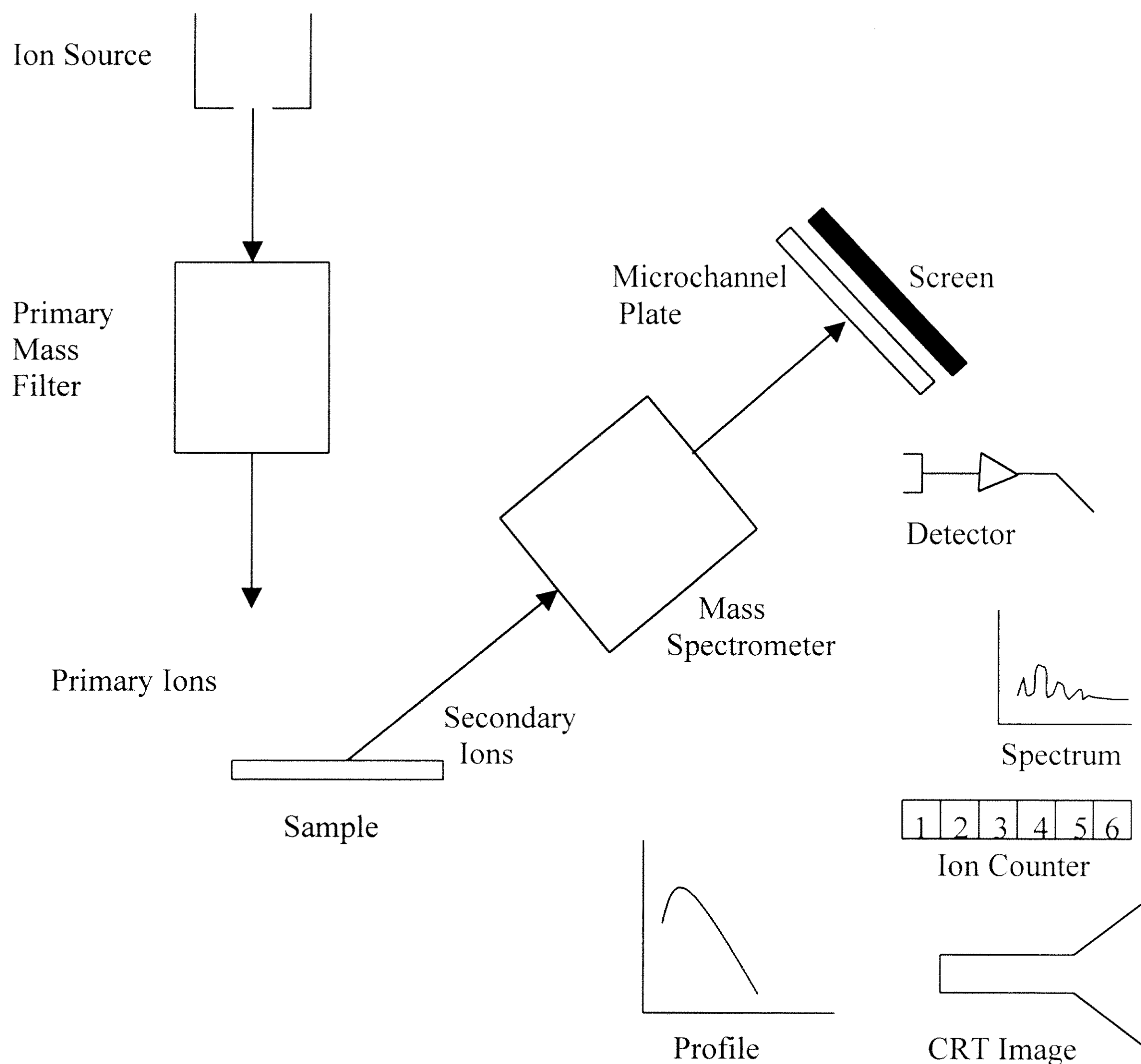

Figure 4.1 SIMS schematic. Also shown are the analysis components such as spectrum acquisition system, ion counter, CRT image & profile [33].

4.1.2 Transmission Electron Microscopy (TEM)

TEM was originally used to see highly magnified sample images. Later, analytical capabilities such as electron energy loss detectors and light X-ray detectors were added to the instrument, and the technique is now known as analytical transmission electron spectroscopy (AEM) [33].

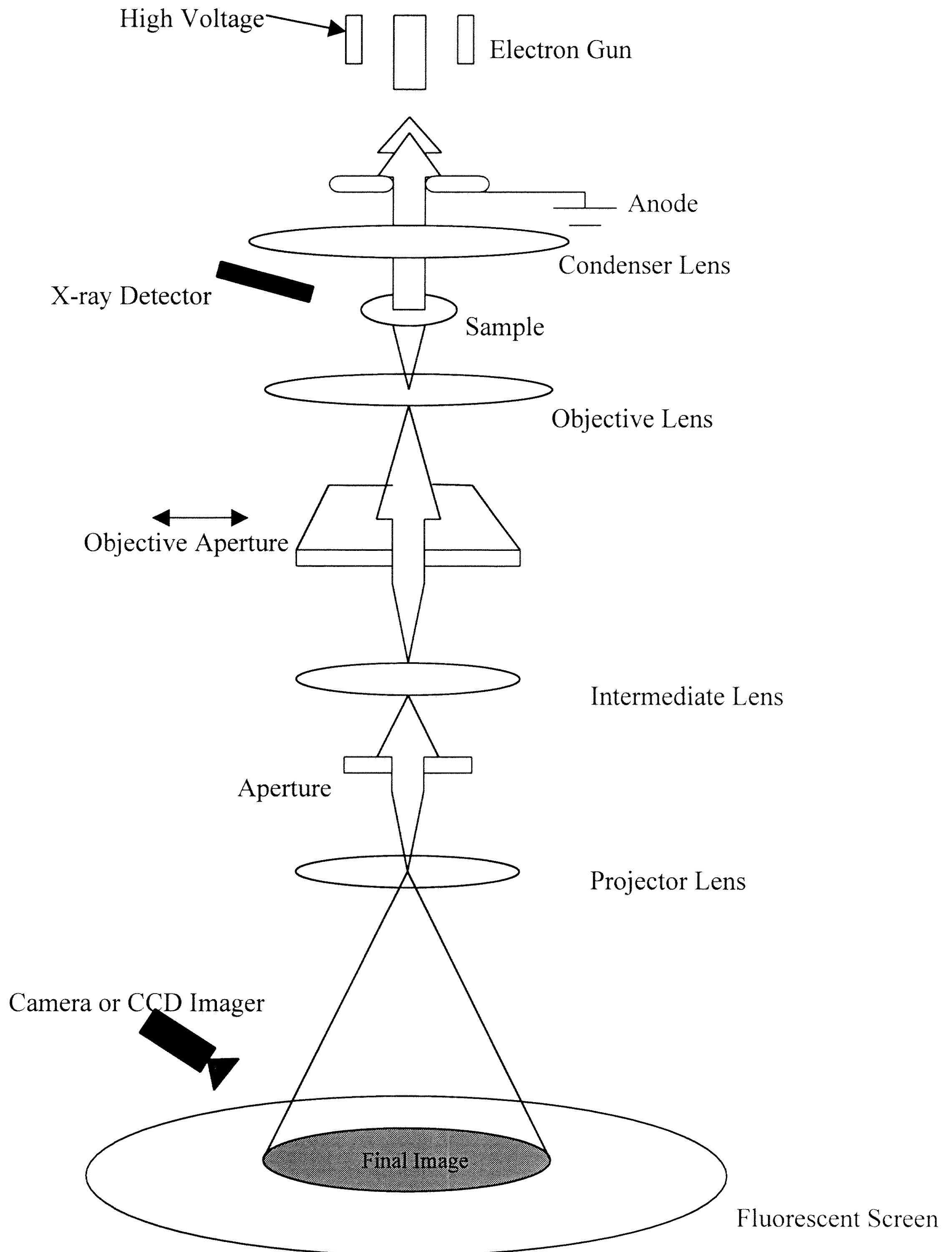

Figure 4.2 Schematic of a TEM [8].

TEM achieves atomic resolution for both crystalline and non-crystalline materials. It is virtually the only tool capable of imaging point defects related to thermal, mechanical and implant processing [8]. Some of the uses of TEM are measuring the grain size distribution with high accuracy, thickness of gate oxides and capacitor composite dielectrics and interface morphology. The typical configuration of a TEM is shown in Figure 4.2. Electrons from the electron source are accelerated to high voltage. Condenser lens shapes the beam from electron gun to focus on the sample. In TEM, the samples must be sufficiently thin for electrons to transmit through it.

4.1.3 Rutherford Backscattering Spectroscopy (RBS)

RBS is a method to determine depth profile. The technique involves directing an ion beam onto the surface of the sample. This results in elastic collisions between the incident ion and a target atom, which causes the ion to loose energy. Energy-dispersive silicon barrier detector detects the scattered ions, and the signal is fed into a multi-channel analyzer [34] as shown in Figure 4.3.

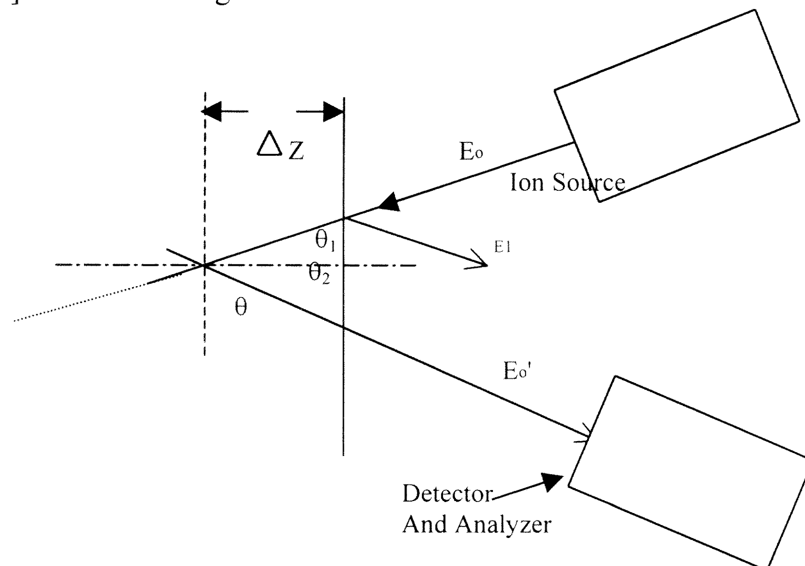

Figure 4.3 Schematics of Rutherford Backscattering Spectrometer [34].

The relation between the ion energy E_o and the energy of ion after backscattering E_o' is given by equation 4.1.

$$E_o' = k\, E_o \tag{4.1}$$

where, k is the kinematic factor.

In the scattering process, there is loss of energy. The incident ions suffer energy loss as they penetrate and scatter into the sample. These ions normally penetrate, scatter and collide with the sample atoms, until a certain depth ΔZ and then will return through the same path before they can escape and be detected. Energy is lost in this trip [34]. The total energy difference between ions scattered at the surface and ions emerging from the sample after scattering at a depth ΔZ is given by Equation 4.2.

$$\Delta E = kE_o - E_1 = [\varepsilon]\, N\, \Delta Z \tag{4.2}$$

where, $[\varepsilon]$ = stopping cross-section factor, N = atomic density of sample.

A depth profile is obtained by monitoring the number of backscattered ions as a function of back scattered ion energy E_1.

4.2 Electrical Techniques

4.2.1 Capacitance-Voltage (C-V) Technique

The C-V technique relies on the fact that the width of a reverse-bias space charged region (scr) of a semiconductor junction depends on the applied voltage. The C-V profiling method has been used with Schottky barrier diodes using metal and liquid electrolyte contacts, p/n junctions, MOS capacitors, and MOSFETs [33].

From p/n junction theory, the space charge capacitance is a function of the reverse-bias voltage. Considering the n^+/p or p^+/n junction, where the impurity

concentration is very high on one side of the junction and decreases to a lower value abruptly on the other side, the following Equation 4.3 explains the impurity concentration at the surface-charge layer edge (C_x) [34] :

$$C_x = \frac{C^3(V)}{q\varepsilon_s} \frac{1}{\frac{dC}{dV}} \tag{4.3}$$

where, C(V) is the junction reverse-bias capacitance per unit area at a reverse voltage V, and ε_s is the permittivity of silicon and q is the elementary charge. The depth x is given by Equation 4.4:

$$x = \frac{\varepsilon_s}{C(V)} \tag{4.4}$$

The reverse voltage (V) is given by,

$$V = V_R + V_{bi} \tag{4.5}$$

where, V_R is the applied reverse-bias and V_{bi} is the built-in potential of the p/n junction, given by,

$$V_{bi} \cong \frac{kT}{q} \ln \frac{C_A C_D}{n_i^2} \tag{4.6}$$

Here, C_A is the acceptor concentration and C_D is the donor concentration. Thus,

$$C(V) = \frac{\varepsilon_s}{\sqrt{2}L_D} (\beta V_{bi} \pm \beta V - 2)^{\frac{-1}{2}} \tag{4.7}$$

and

$$L_D = \left[\frac{\varepsilon_s}{qC_B} \frac{kT}{q} \right]^{\frac{1}{2}} \tag{4.8}$$

Here, $\beta = q/kT$, and L_D is the Debye length. C_B is the substrate doping concentration.

Thus, the built-in potential of the p/n junction can be determined from the junction capacitance at zero reverse bias using Equation 4.6. The impurity profile can be determined by measuring the reverse-bias capacitance as a function of the applied voltage from Equation 4.3 and Equation 4.4.

4.2.2 Diode Current-Voltage Characteristics

When considering a p/n junction, its most resistive portion is the space charge (depletion) region [35]. Increasing the width of the depletion region can increase the resistance of this junction. This width can be increased by applying a negative voltage to the p-region with respect to the n-region. This helps the electrons and the holes to draw away from the junction increasing the depletion width. This situation corresponds to a reverse bias. If a positive voltage is applied to the p-region, the electrons and holes are pushed towards the junction, which decreases the width of the depletion region and the device resistance.

Figure 4.4 indicates that the electron and hole diffusion currents are being directed from p to n (although the charge flow directions are opposite to each other), and the drift currents are from n to p. It also shows the effects of bias on a p/n junction. At equilibrium, the net current crossing the junction is zero. Under the reverse bias condition, both diffusion components are negligible because of the large barrier at the junction, and the current is small. This current is basically voltage independent. Figure 4.5 shows the I-V characteristics of a p/n junction diode.

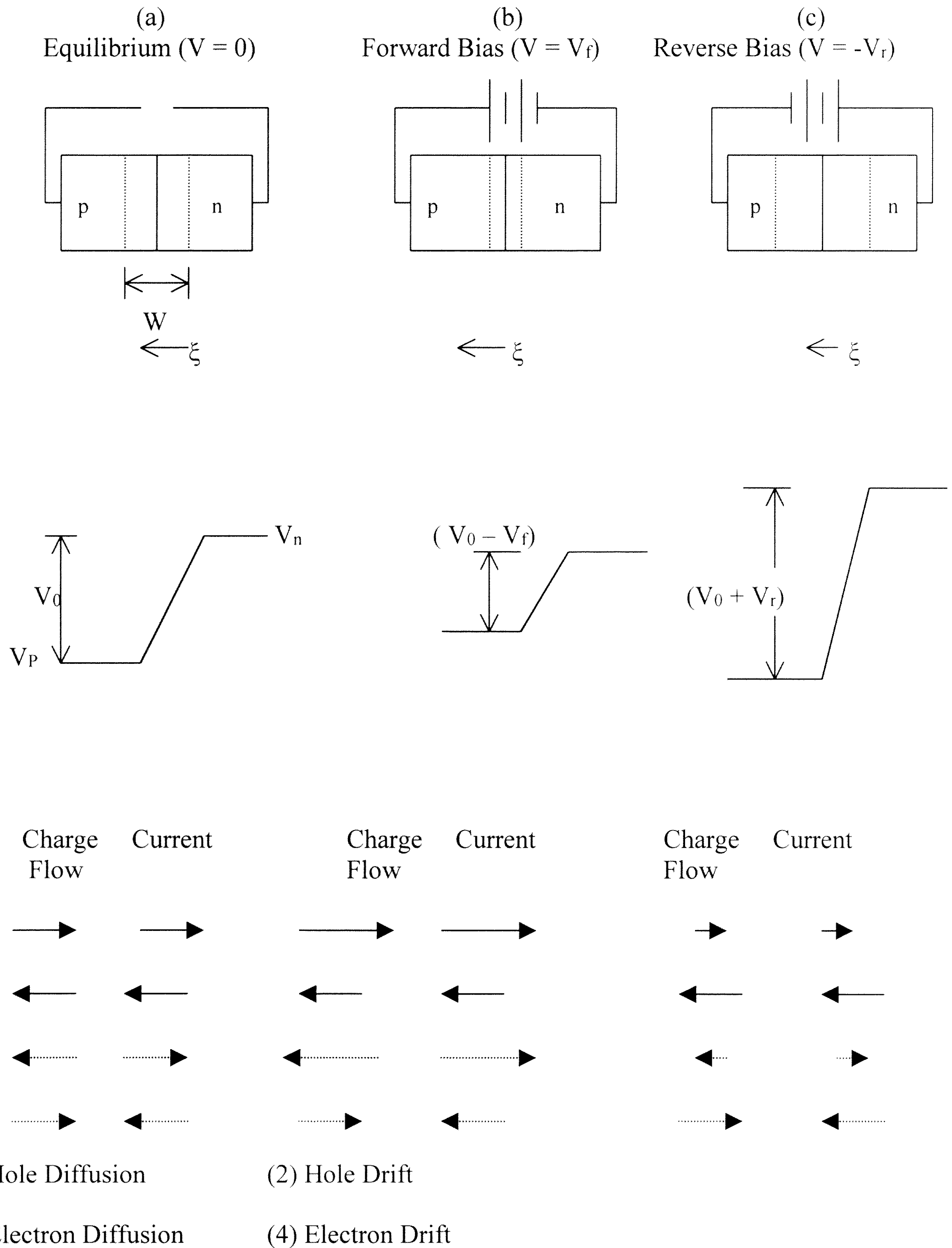

Figure 4.4 Effects of bias on a p-n junction; Transition region width and electric field, electrostatic potential and charge flow and current direction within W, under (a) equilibrium, (b) forward bias and (c) reverse bias [4].

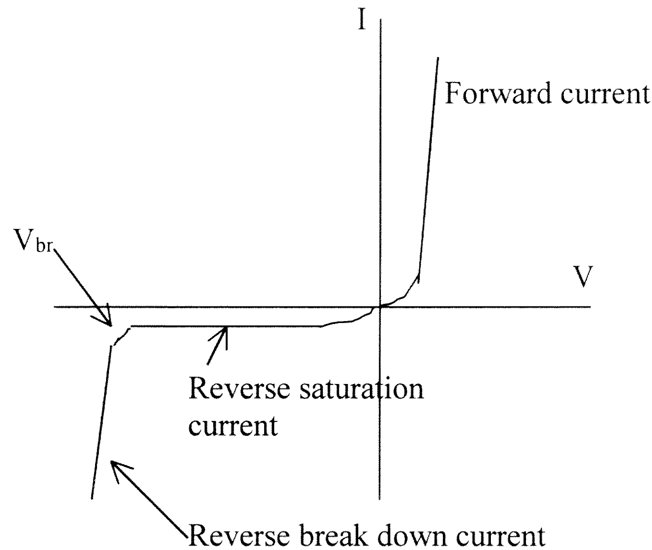

Figure 4.5 I-V characteristics of a p-n junction and reverse breakdown in the junction [4].

There is a very little amount of current flowing under reverse bias as seen from Figure 4.5. This is typical for an ideal junction. The reverse breakdown current occurs at a voltage termed as critical voltage (V_{br}). At this voltage, the reverse current increases sharply, and a large amount of current can flow with a small increase in voltage. Considering the device part, the defects in the junction region can greatly increase the reverse bias current flow and is denoted as leakage current. It is considered that the active defects are the recombination centers, an example of which is dislocation loops that remain even after the annealing implant damage.

4.2.3 Spreading Resistance Probe Technique (SRPT)

Spreading resistance is the resistance associated with the divergence of the current lines emanating from a small tipped electrical probe that is placed on silicon [19]. Spreading resistance measurements provide an electrical measurement of the active concentration using a pair of fine metal probes to step down the beveled surface of a sample. By

knowing the resistivity and comparing it against resistivity standards, the doping concentration can be obtained.

The first step in analyzing a sample is to bevel the sample at a shallow angle as shown in Figure 4.6 [7]. The sample is then polished using diamond slurry and a rotating wheel. The beveling is done by gluing a small sample to a precision-machined holder with typical bevel angles between 8° and 34°. The metal probes are then made to contact with the beveled surface. As the current flows between the point contacts, the raw spreading resistance data is obtained. This is then converted to resistivity and the active dopant concentration is obtained by comparing with resistivity standards.

The most important aspect is that the probes make a good electrical contact with the silicon surface. The tips of the probes are generally roughened by stepping them on a diamond abrasive paste. If the tip is smooth, then the smoothness on the tip will not be able to fracture any native oxide layer. This will not give good results because of poor contact resistance. If the tip is rough, it penetrates into the silicon which is not desirable. Also, the consideration of probe pressure, probe conditioning and sample polishing is important in the carrier profile data.

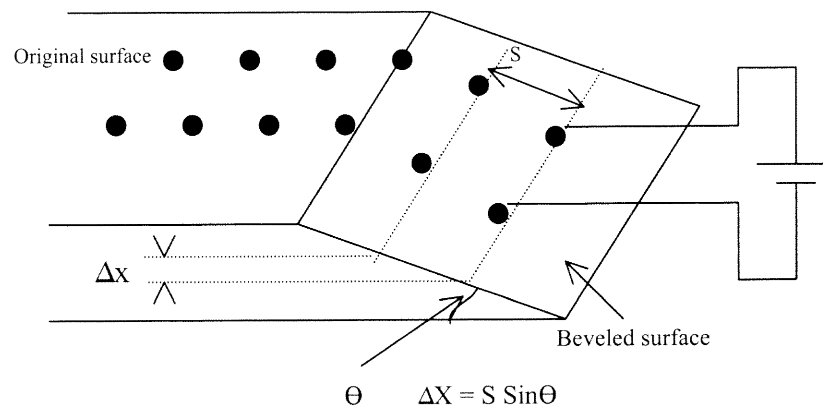

Figure 4.6 Schematic of a spreading resistance measurement [7].

4.2.4 Four-Probe Technique

Four-probe technique is usually used to measure the sheet resistance R_S. Sheet resistance of a diffused layer is the resistance exhibited in a square of that layer, which has a thickness X_J. Figure 4.7 [19] shows a schematic of a four-point probe arrangement. In this technique, current I is applied between the two outer probes and the voltage drop V is measured between the two inner probes. When, all of the probes are equally spaced the resistivity is given by Equation 4.9.

$$R_S = 2\pi sF\ (V/I) \tag{4.9}$$

where, s is the probe spacing, and F is a function of the ratio V/I.

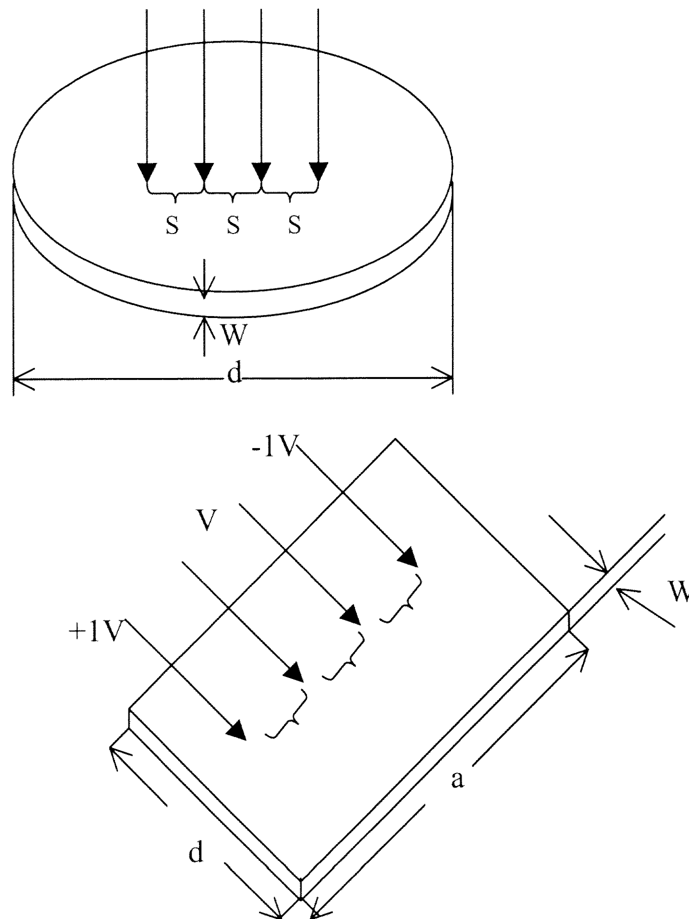

Figure 4.7 Co-linear four-point probe arrangement for the measurement of resistivity [19].

This measurement is performed when the current is in forward direction and then in the reverse direction. This is done in order to minimize errors due to thermo-electric heating and cooling effects [19]. The two V/I readings are then averaged.

4.2.5 Hall Effect

Hall effect is widely used to measure the carrier concentration, resistivity, and the mobility at a given temperature. Occasionally, one needs to measure the spatially varying carrier concentration profiles. Mainly due to simplicity, low-cost and fast turn around time, it is widely used as a characterizing technique in the semiconductor industry and research laboratories. Figure 4.8 shows an n type bar shaped semiconductor. The carriers here are predominantly electrons. When an electron moves along a direction perpendicular to an applied magnetic field, it experiences a force acting normal to both direction and moves in response to this force. This force is affected by the initial electric field [36]. This force is called the Lorentz force.

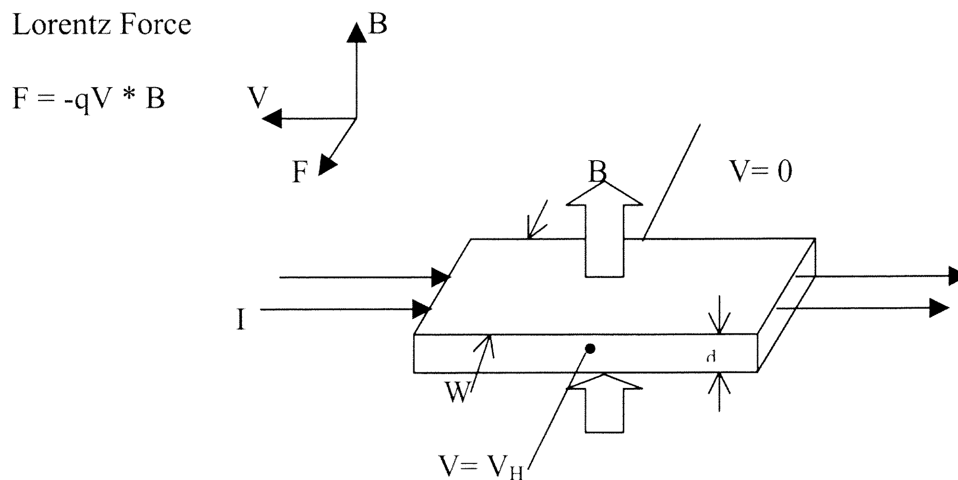

Figure 4.8 Details of Hall effect [36].

When a constant current 'I' flows along the x-axis, the magnetic field is in the z-direction. Electrons subject to Lorentz force initially drift away from the current line towards the negative y-axis, resulting in an excess surface electrical charge on the side of the surface. This results in a potential drop across the two sides of the sample. This is the Hall voltage (V_H) and is given by Equation 4.11:

$$V_H = \frac{IB}{qnd} \tag{4.11}$$

where, I = current, B = magnetic field, d = sample thickness, q = 1.602 x 10^{-19} C, is the elementary charge. In some cases, it is convenient to use layer or sheet density ($n_s = n_d$) instead of bulk density [36]. This leads to Equation 4.12:

$$n_s = \frac{IB}{q|V_H|} \tag{4.12}$$

Thus, by means of Hall Voltage V_H and from the known values of I, B, and q, one can determine the sheet density n_s of charge carriers in semiconductors.

Of the analytical techniques describe above, the main ones used for this thesis are sheet resistance, SIMS, and the measurement of reverse bias leakage in p/n diodes for characterizing defects in shallow p/n junctions.

CHAPTER 5

EXPERIMENTAL PROCEDURE

The experiments focussed on the measurement of electrical leakage in ultra shallow p/n junctions for the extension region of PMOS transistors. The junctions were prepared by ultra-low energy boron ion implantation into n-type 200 mm wafers followed by rapid thermal annealing. The purpose of the experiment is to use the method of leakage current in p/n diodes to evaluate the junction quality and process viability for shallow p-type dopants. Results of the reverse bias current leakage were compared for various boron implant doses and implant energies.

5.1 Sample Preparation

The samples, which are studied, were divided into three groups. This was based on the sample implant, the implant dose, and the sample annealing conditions. Reverse bias currents are measured and compared with the processing conditions of the sample. Following three sections describe the work on samples that were studied. The details of the experiments and their results are explained in Chapter 6.

5.1.1 Experiment A

In this experiment, the study was done on samples that are processed by two different spike-annealing methods. The effect of varying B implant dose was also studied. The spike annealing methods applied are the incandescent lamp spike annealing with a Heatpulse model 8108 and the arc lamp Vortek spike annealing. The boron implant energy is 0.5 keV and the dose is varied from $2x10^{14}$ cm^{-2} to 10^{15} cm^{-2}.

5.1.2 Experiment B

In this experiment, the use of Ge for pre-amorphization implants (PAI) to reduce the boron implant depth is studied. The Ge PAI energy for this set of samples was 10 keV and 80 keV. The B implant energy at 10^{15} cm^{-2} dose was varied from 0.5 keV – 5 keV. The samples were prepared at Sematech International. Details of spike annealing were kept as Sematech proprietary and were not made available.

5.1.3 Experiment C

The study of flash annealing method and its effects on reverse bias leakage current is the main aim in this experiment. For this set of samples, the B implant dose was not varied and all samples received Ge PAI. The flash annealing method in this experiment consisted of varied intermediate temperature, T_i, ranging from 700 - 1000°C. Samples annealed without the flash annealing step were also included.

5.2 Annealing Techniques Used for Sample Processing

Shallow junctions were formed by implantation of ultra low energy B implants. Annealing was done mainly to activate the implants. The samples were subjected to three different methods of annealing treatment, arc lamp spike annealing, incandescent lamp spike annealing and flash lamp annealing. The first two processes are conventional spike annealing processes whereas the flash annealing cycles are a recent innovation used for shallow junction formation.

5.2.1 Arc Lamp Spike Annealing

In the arc lamp spike annealing, a high power arc lamp is used for rapid thermal processing. An arc lamp annealing furnace is shown in Figure 5.1.

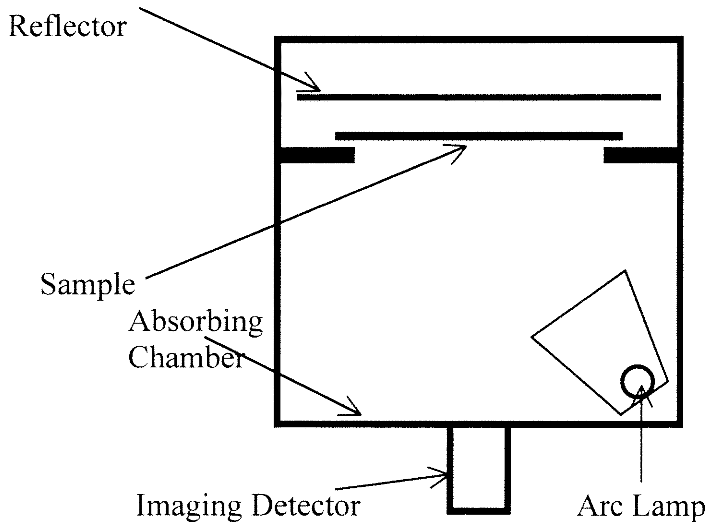

Figure 5.1 Schematic of a chamber with a single arc lamp in a reflector housing for heating wafer in absorbing chamber [11].

This type of lamp is used particularly for spike annealing. Here, a single lamp is used to heat the sample. The chamber is designed in such a way that the reflector shown helps to uniformly heat the sample. The imaging detector creates the images of sample reflectivity and temperature by modulating the arc lamp on and off [37]. The ramp rate for samples was 400 °C/s and the peak temperature was in the range of 1000 - 1550°C.

5.2.2 Incandescent Lamp Spike Annealing

The incandescent lamp based annealing chamber basically surrounds the wafer with heating lamps. Here the lamps are arranged in rows with the filaments parallel to the

wafer and include a quartz isolation tube to control the gas ambient as seen in Figure 5.2. The power distribution among the lamps is adjusted to produce uniform process results or temperature [11].

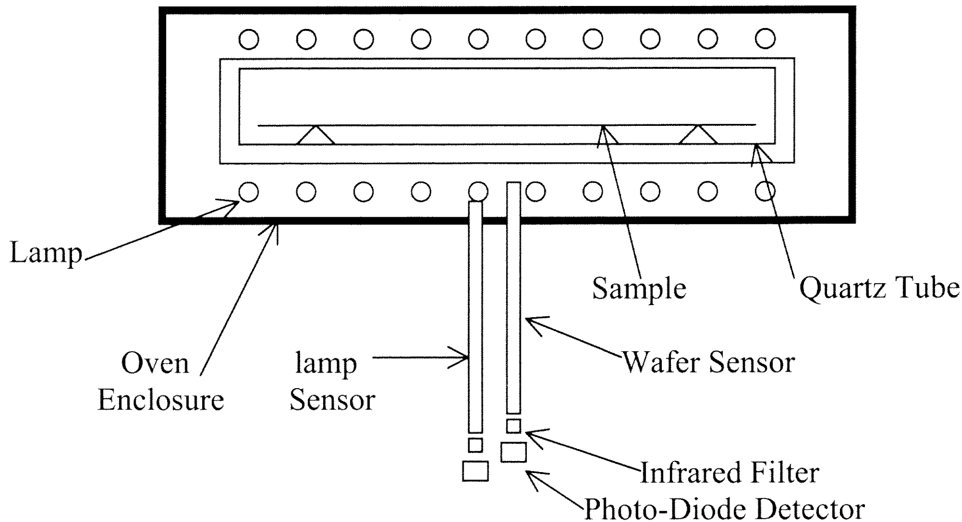

Figure 5.2 Cross-sectional view of annealing chamber with dual-side heating with linear incandescent lamps [11].

Here the spike annealing temperature varies from 1000 - 1150˚C, the ramp rate is about 150 ˚C/s, and the cooling rate is about 80 ˚C/s.

5.2.3 Flash Annealing

In this type of annealing the sample is introduced to a sudden flash from a lamp source. The lamp is used to first heat the sample to a pre-determined intermediate temperature (T_i). Then, a flash of much higher power from a lamp is given to the sample. The flash duration is about 10-20 ms. Flash annealing is done on the device or implant topside of the sample. Final temperature on the topside of the wafer is much greater than T_i, typically 300 to 500 ˚C higher than T_i.

5.3 Sample Preparation for Reverse-Bias Diode Leakage Measurements

Reverse-bias leakage current was studied utilizing three sets of samples. Of these, two sets were prepared from n-type wafers with low energy boron implants with Ge PAI. Leakage current measurements were performed on these sets of samples. Wet chemical etching was done in order to obtain a desired geometry on the sample to produce diode and Van der Pauw measurement patterns on the samples. Measurements of leakage current were made by supplying a constant reverse bias voltage of ~1V.

5.3.1 Wet Chemical Etching Process

The samples were heated to about 50-60°C. Patterning was done by masking the sample, which was one square inch, using hot wax (Apiezon W40) as shown in Figure 5.3. The sample was then etched to define electrical test patterns.

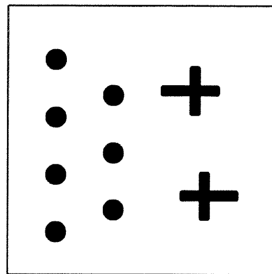

Figure 5.3 Sample with wax patterns.

An etching solution, chemical polish number 4 (CP4), was made with 1:4:2 ratio of $HF:HNO_3:CH_3OOH$. The sample was stirred in this solution for about 15s. The time used for the first few samples was 30s. In case of some samples, it showed high etching of the sample surface and formation of grooves around the patterned portion. By reducing the time of sample stirring to 15s, good results were obtained. After etching, the samples

were then rinsed in de-ionized (DI) water and dried under a flow of N_2 gas. Main reason for this etching was to isolate a mesa diode structure.

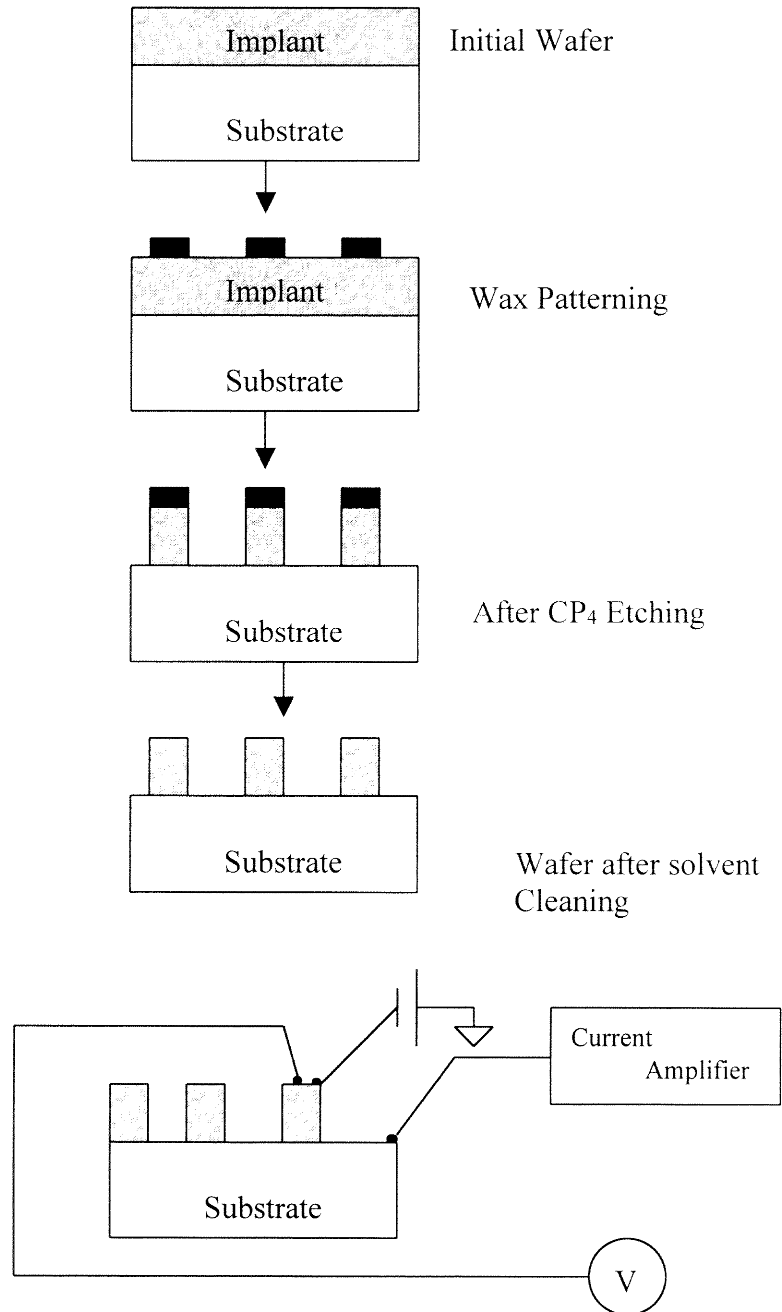

Figure 5.4 Schematic of process steps for sample preparation and test.

The next step was cleaning the sample to remove wax in a series of solvents (toluene, acetone, and propanol). Cleaning time in each of these solvents was kept to about 15s. After cleaning the samples, they were again rinsed in DI water and dried under N_2 gas. The last and final step was the etching of the sample in a solution of 1:25 ratio of $HF:H_2O$ for about 15s and again rinsing with DI water and drying under N_2 gas. This etching process flow is illustrated in Figure 5.4, which also shows the connections for electrical measurements.

5.3.2 I-V Measurements

The sample was mounted on a probe station (Micromanipulator) and a scratch was made on one of the corners of the sample using a diamond tipped pen, to make the connection with the current amplifier. The probes were spaced on the dot such that they did not touch each other. Indium was soldered at the tip of these probes in order to obtain good electrical contact. The contact resistance between the two probes on the diode dot was measured and they ranged from 100-1000 Ohms. Two probes were used to make contacts to a circular diode pattern as shown in Figure 5.5. A third contact was made to the base of the silicon sample. BNC cables were used to make the necessary circuit connections. After making the connections as shown in Figure 5.3, the probe station was closed in a light tight enclosure and a constant reverse bias voltage was applied.

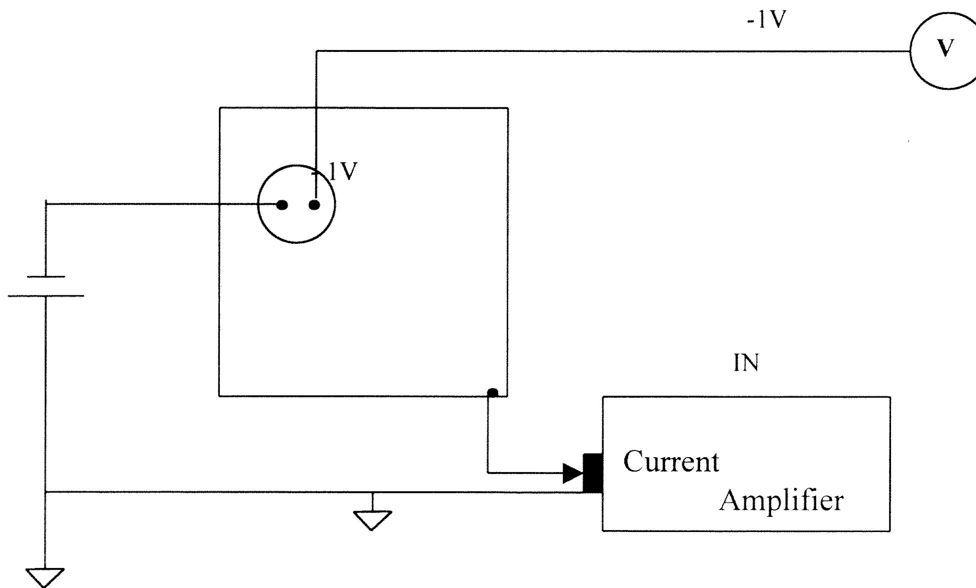

Figure 5.5 The basic connections for reverse-bias diode leakage measurements. The circle shows the diode area.

The equivalent circuit of the connections is as shown in Figure 5.6. R_1 and R_2 represent the contact resistances. The current I flows from the power supply V_0. The power supply is a digital source, Power Designs model 2005A. When the current I_D is applied through R_1, V_0 is adjusted such that the voltage across the meter V shows close to –1V. A Keithley model 177 digital voltmeter was used to measure voltage. The current amplifier has a digital display, and the zero check is done before taking the readings. The instrument used here for the current measurement was a Keithley model 617 programmable electrometer.

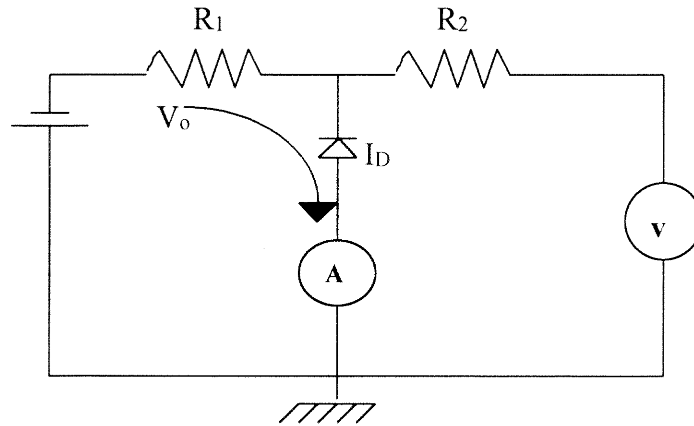

Figure 5.6 The equivalent circuit diagram for reverse-bias diode leakage measurement.

The measurements for leakage current were taken immediately and at one minute and two minutes intervals, after the reverse bias voltage was adjusted to ~1V ± 0.003 V. This procedure was done for four diode dots at different positions on each sample and the readings of current were taken. Calculations were done to calculate the area of dots and the average current density.

Calculations

Area of the dot is determined by equation 5.1,

$$\text{Area} = \frac{\pi}{4} D_1 D_2 \frac{0.01}{(137)^2} \text{ cm}^2 \qquad (5.1)$$

Here the area calculated is approximated as an ellipse.

The factor, D_1 is the number of divisions in vertical direction and D_2 is the number of divisions in horizontal direction. The quantity '137' is the number of divisions of the microscope reading in the probe station and is equivalent to 1mm. The number 0.01 is the conversion from mm^2 to cm^2. Measurements of D_1 and D_2 are made using the reticule in the eyepiece of a microscope.

The average current density for each sample was calculated in the following manner. After calculating the area for each sample, the average of the three leakage current readings was taken for each dot in the sample. This gave four current readings for a dot. The current density was calculated from these readings by taking the ratio of average current reading to the area of that particular dot. This gave four current densities for each of the samples. The final current reading was then obtained by taking the average of the least two of the four current readings. An example of the calculated data sets is shown in Table 5.1.

Table 5.1 Example Data for a B Implant with Ge PAI from Experiment B

Sample 1

Dot	Voltmeter reading	D1	D2	Area (Sq. cm)	current reading (A)	Avg. current Reading (A)	Leakage Current amp/sq.cm	Average current density amp/sq.cm
1	1.001	130	127	0.0198	1.66E-05	1.66E-05	8.39E-04	
					1.67E-05			
					1.67E-05			
2	0.986	130	130	0.0207	1.07E-05	1.07E-05	5.17E-04	
					1.08E-05			
					1.09E-05			
3	0.999	132	130	0.0213	1.59E-05	1.55E-05	7.25E-04	6.21E-04
					1.55E-05			
					1.58E-05			
4	0.999	110	108	0.0102	6.40E-05	6.40E-05	6.25E-03	
					6.40E-05			
					6.50E-05			

Sample 2

1	1.002	120	147	0.0226	4.90E-07	1.80E-07	7.97E-06	
					3.10E-07			
					1.80E-07			
2	1	118	117	0.0138	5.90E-07	5.80E-07	4.19E-05	
					6.00E-07			
					5.80E-07			
3	1	130	130	0.0207	1.90E-07	1.40E-07	6.76E-06	2.24E-05
					1.50E-07			
					1.40E-07			
4	1.002	144	152	0.0348	2.50E-07	1.00E-07	2.88E-06	
					1.30E-07			
					1.00E-07			

CHAPTER 6

EXPERIMENTAL RESULTS

There were four sets of samples, which were tested for leakage current measurements. Basically, three experiments were done and these are explained by considering the shallow boron implants and spike annealing conditions.

6.1 Experiment A

The first experiment discussed here has two sets of samples with different annealing methods. The samples tested in this section have a boron implant of 0.5 keV with variations in dose from $2x10^{14}$ cm^{-2} to $1x10^{15}$ cm^{-2}. These samples were annealed by two methods, the incandescent lamp spike annealing with a Heatpulse model 8108 and the arc lamp spike annealing with a Vortek system. The spike anneal temperature is also a major variable when the results are considered. The samples are annealed at a higher temperature for lower doses of implant. The sheet resistances of samples are also considered as a function of anneal temperature. The leakage current in diodes fabricated on the same samples is also considered as a function of temperature.

Table 6.1 shows the results obtained for the leakage measurement of samples that were spike annealed by the incandescent lamp method. The columns show the boron implant dose, the maximum temperature at which the annealing was done, the sheet resistance, the corresponding junction depths, which were measured by SIMS, and the average reverse-bias diode leakage current.

The SIMS data and the sheet resistance value of the samples were received from the work performed at Agere Systems, from where this set of samples also came. Figure

6.1 shows the sheet resistance plotted against maximum temperature. Although there are only two samples at each implant dose, the graph shows a trend where the sheet resistance is decreasing as the maximum anneal temperature is increased.

Table 6.1 Experimental Data for 0.5 keV Boron Implants Annealed by Incandescent Lamp Method, where T_{max} is the Maximum Anneal Temperature

Boron dose (cm^{-2})	T_{max} (°C)	Sheet Resistance R_S (Ω/sq.)	Junction depth X_J at $10^{18}cm^{-3}$ (cm)	Average leakage Current (A/cm^2) (at –1V reverse bias)
2E14	1111	1074.0	3.33E-06	1.55 E-06
2E14	1122	1045.3	3.33E-06	1.54E-04
4E14	1058	819.1	3.22E-06	3.12E-04
4E14	1075	665.3	3.58E-06	9.90E-06
7E14	1026	822.4	2.79E-06	3.10E-06
7E14	1037	722.5	2.79E-06	1.29E-06
1E15	1009	761.1	2.54E-06	6.52E-06
1E15	1017	729.4	2.65E-06	2.21E-06

It can be explained from Figure 6.1 that, to get about same range of sheet resistance, one must anneal to a higher temperature as the implant dose is varied. From the graph it can be seen clearly that the sample with the $2x10^{14}$ cm^{-2} implant is an exception as it shows high sheet resistance at higher peak temperature.

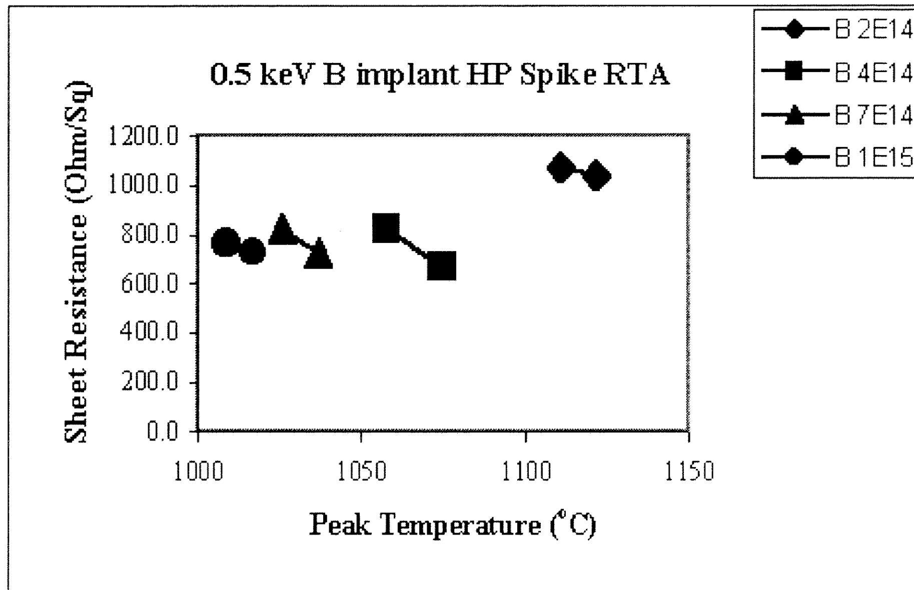

Figure 6.1 Sheet resistance vs junction depth for incandescent lamp spike annealed 0.5 keV B^+ implants at four doses (cm^{-2} units).

Figure 6.2 shows the leakage current compared against the maximum anneal temperature. Except for the lowest temperature point, the leakage current is weakly dependent on annealing temperature and implant dose. The set of samples with the highest implant dose ($1x10^{15}$ cm^{-2}) showed different values for leakage. The leakage for one sample was more than twice the amount as for the other samples.

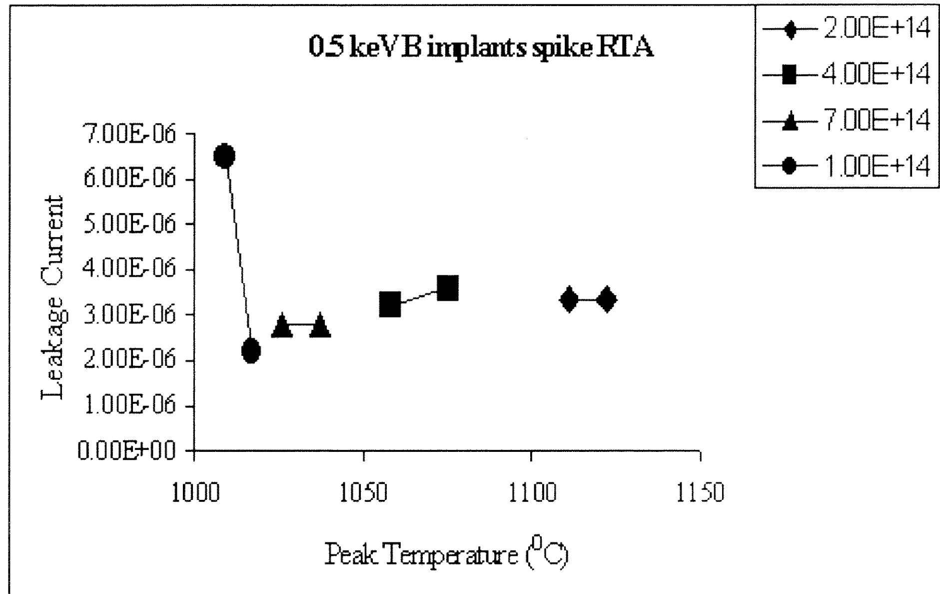

Figure 6.2 Diode **l**eakage current density vs maximum temperature of incandescent-lamp spike annealed 0.5 keV B^+ implants at four doses (cm^{-2} units).

Table 6.2 gives the data for samples annealed with the arc lamp spike annealing method. The sheet resistance and junction depth vs temperature graphs were plotted for the same parameters as the case earlier. In this case the number of samples is sufficient to make a good judgement of the trends shown by the data. Figure 6.3 shows a plot of sheet resistance as a function of maximum temperature. This graph shows a trend where in it can be said that the sheet resistance tends to decrease as the maximum temperature for annealing is increased. The leakage currents measured are shown in Figure 6.4. The leakage current densities vary from 10^{-6} to 4 x 10^{-6} A/cm^2. The trend of the data for the 4 x 10^{14} cm^{-2} dose shows the leakage decreasing with increasing annealing temperature towards a low value comparable to the leakage found for the other doses, 10^{-6} to 2 x 10^{-6} A /cm^2.

Table 6.2 Experimental Data for 0.5 keV B Implants Annealed by Arc Lamp Method

Boron dose (cm^{-2})	T_{max} (°C)	Sheet Resistance R_S (Ω/sq.)	Junction depth X_J at $10^{18}cm^{-3}$ (cm)	Average leakage Current (A/cm^2) (at –1V reverse bias)
2E14	1086	1797.0	2.20E-06	8.20E-07
2E14	1105	1500.0	2.25E-06	1.31E-06
2E14	1125	1369.0	2.55E-06	9.01E-07
2E14	1145	1265.0	2.74E-06	1.61E-06
4E14	1066	1248.0	2.24E-06	4.04E-06
4E14	1086	1006.8	2.53E-06	4.86E-06
4E14	1105	821.9	3.05E-06	1.20E-06
4E14	1125	688.7	3.68E-06	1.88E-06
7E14	1036	1261.0	1.98E-06	1.96E-06
7E14	1056	966.7	2.46E-06	1.15E-06
7E14	1075	752.8	2.90E-06	2.43E-06
7E14	1095	585.4	3.56E-06	9.12E-07
1E15	1006	1369.0	1.94E-06	1.68E-06
1E15	1026	1090.0	1.99E-06	3.88E-06
1E15	1046	879.0	2.38E-06	-
1E15	1065	693.4	2.81E-06	1.30E-06

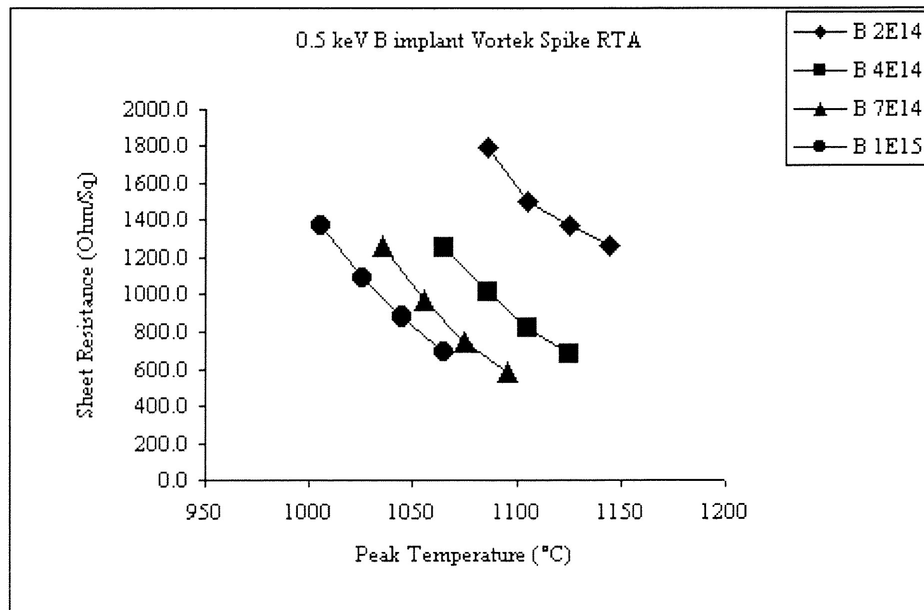

Figure 6.3 Sheet resistance vs peak temperature of arc lamp spike anneal for 0.5 keV B^+ implants at four doses (cm^{-2} units).

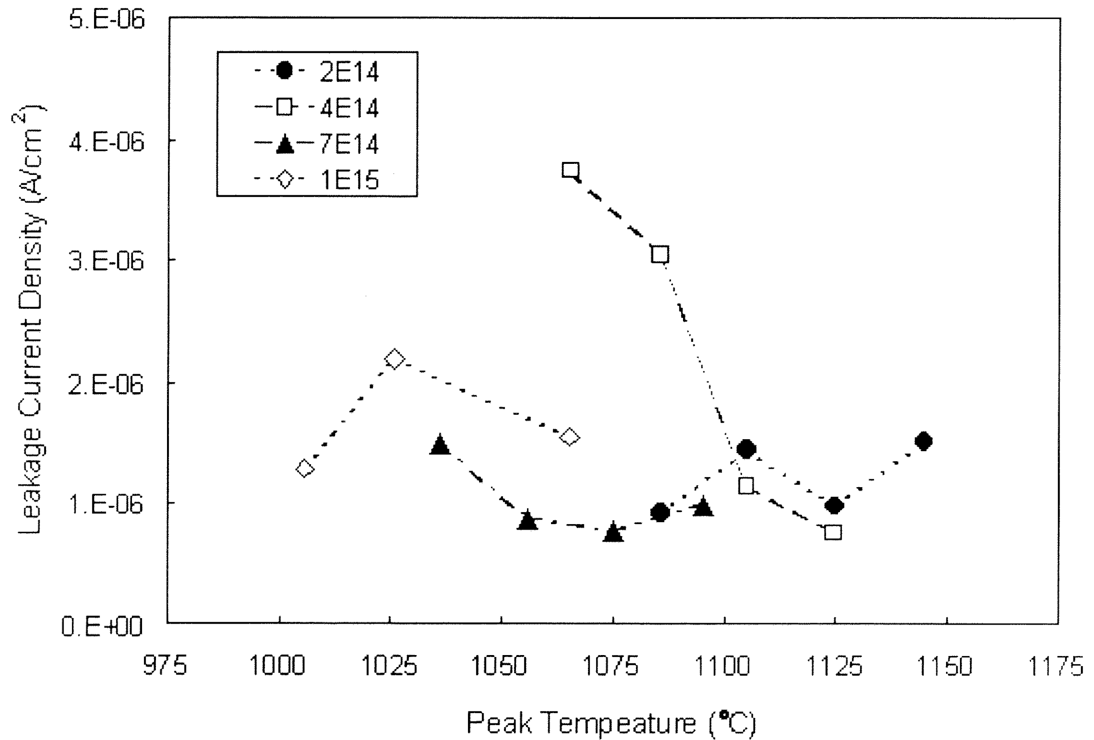

Figure 6.4 Reverse bias diode leakage current density (at –1V bias) vs. arc-lamp spike anneal temperature for 0.5 keV B^+ implants at four doses (cm^{-2} units).

On comparing Figure 6.1 and Figure 6.3, the arc lamp annealing requires a higher temperature than incandescent lamp annealing to yield a comparable result for the sheet resistance. This is explained by the shorter time at peak temperature for the arc lamp method, when compared to the incandescent lamp method. This is shown in Figure 2.5 in Chapter 2.

On comparing Figure 6.2 and Figure 6.4, the leakage current densities tend to be lower for the arc lamp method, with few exceptions, when compared to the incandescent lamp method. The leakage current densities are in the (1-7) x 10^{-6} A/cm^2 range for this boron implant experiment and the two spike annealing methods.

6.2 Experiment B

Sematech International (Austin, Texas) provided the samples for this experiment. The samples had B implants at 10^{15} cm^{-2} dose and energies from 0.5 keV to 5 keV and were Ge pre-amorphized. The purpose of this experiment was to relate the effects of B implant and Ge PAI energies to diode leakage and junction formation. The motivation for the PAI is that it allows the B to be shallower. The range of damage by Ge PAI and the range of B implant are both varied and the effects were studied. The results obtained from this experiment reveal that PAI introduces more damage and diode leakage, which may be detrimental when shallow junction properties are considered.

Table 6.3 gives the data for the implants and leakage current measurements. The boron implant energy at 10^{15} cm^{-2} dose was varied along with the energy of the Ge PAI. Figure 6.5 shows the leakage current density versus boron implantation energy. Note that the samples with the higher Ge PAI energy of 80 keV show noticeably larger leakage current density when compared to the samples with the lower Ge PAI energy of 10 keV. The diffusion depths are discussed qualitatively and were not independently determined.

Table 6.3 Reverse Bias Current Readings for Ge Pre-Amorphized Samples at Different Implant Dose

Sample number	Boron Implant energy at 10^{15} cm^{-2} dose (keV)	Ge Post Anneal Implant at 10^{15} cm^{-2} dose (keV)	Average leakage Current (A/cm^2) (at –1V reverse bias)
1	0.5	10	6.21E-04
2	1	10	4.95E-05
3	2	10	2.24E-05
4	5	10	2.60E-09
5	0.5	80	1.46E-04
6	1	80	3.39E-04
7	2	80	1.48E-04
8	5	80	4.97E-04
9	0.5	80	2.31E-04
10	1	80	2.25E-04
11	2	80	4.23E-04
12	5	80	6.83E-04

It can be further concluded from Figure 6.5 that the Ge PAI plays an important role in the junction depth formation with low energy boron implants. The PAI allows boron to be much shallower, but it also introduces defects in the junction, which is not desirable. Figure 6.6 describes further the damage caused by the Ge PAI.

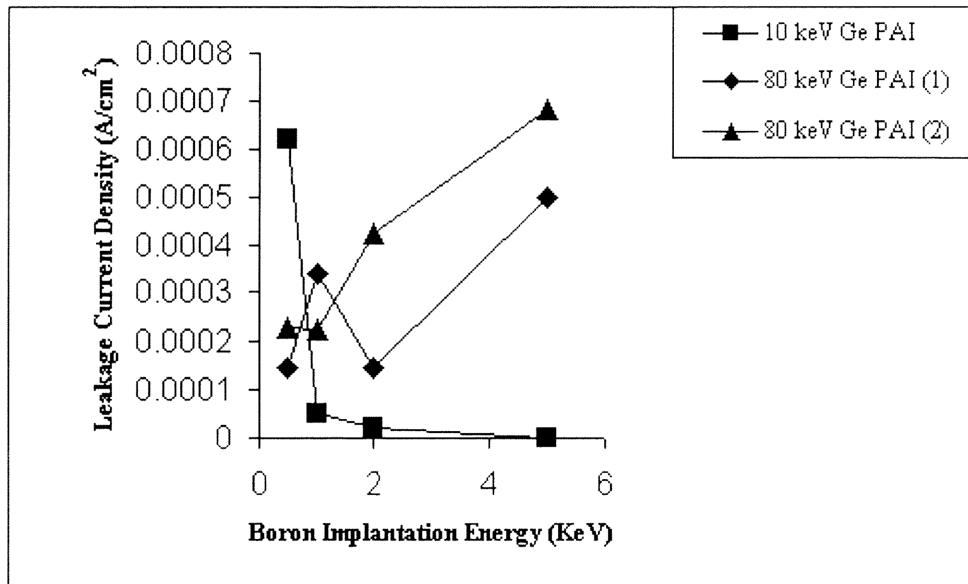

Figure 6.5 Leakage current density vs boron implant energy.

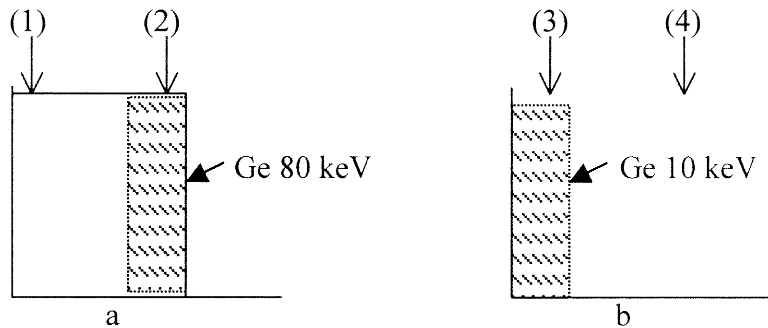

Figure 6.6 a) Ge implant range for 80 keV; b) Ge implant range for 10 keV.

Qualitatively, Figure 6.6 shows by shaded areas that the Ge depths for the two implant energies (10 keV and 80 keV) vary. The B implant ranges are indicated by numbered arrows. Defects from 80 keV Ge PAI implants are much deeper when compared with Ge implant for 10 keV. From Figure 6.6, B implant ranges indicated by the arrows marked by (1) and (4) are expected to show lower leakage because the B and

PAI implants ranges do not overlap. The B implant ranges indicated by the arrows marked by (2) and (3) do overlap and are expected to show higher leakage.

When this quantitative picture is compared to the data in Figure 6.5, it is seen that the combination of low B implant energy and high Ge PAI energy (i.e., like case (1) in Figure 6.6a) does indeed lead to lower diode leakage, for example, 0.5 keV B and 80 keV Ge PAI. Similarly (like case (4) in Figure 6.6b), high B implant and low Ge PAI give low leakage, for example, $B \geq 1$ keV, 10 keV Ge PAI. On the other hand, B implants analogous to case (2) in Figure 6.6a and case (3) in Figure 6.6b, do indeed show higher leakage, for example 0.5 keV B and 10 keV Ge PAI (both energies low) and > 1 keV B and 80 keV Ge PAI (both energies high).

It can be also concluded that of the two sets of 80 keV Ge PAI samples, one set received more aggressive annealing than the other. Some samples from these two sets showed significantly higher leakage. It can be summarized from Figure 6.5 that the set of 80 keV Ge PAI samples denoted by the diamond symbols (case 1) received a larger thermal budget than the other set denoted by triangle symbols (case 2).

The lower Ge PAI has higher leakage for the 0.5 keV B implants. The explanation can be given that the defects produced by the 10 keV Ge PAI are closer to the junction formed with 0.5 keV B implant. This is an important observation because low energy B implants are needed for ultra shallow junction formation. Thus, higher energy Ge PAI, such as 80 keV, is more suitable for ultra shallow junction. This is denoted as case (1) in Figure 6.6a.

6.3 Experiment C

The set of samples for this experiment were provided by Vortek Industries, which were Ge pre-amorphized with PAI of 30 keV for all the samples. The Boron implant energy was 500eV and the dose was $1x10^{15}$ cm^{-2}. The implants were done at Varian Semiconductor Equipment Associates and the annealing was done in an arc lamp system at Vortek. The annealing conditions for this set of samples were different from the previous case. These samples were flash annealed with several annealing conditions as shown in Table 6.4. The B implant conditions for this set of samples was not varied. The Ge PAI was reduced to 10 keV for one sample. The flash annealing method in this experiment is varied with the intermediate temperature (T_i) ranging from 700 - 1000 °C, and the final temperature from 1086 - 1325 °C. The approach to the intermediate temperature is similar to spike annealing without flash annealing. The ramp rate was 400 °C/s for most of the samples but a few samples received ramp rates of 50 °C/s.

During the etch process, the samples showed deeper etching of the exposed Si, and even the wax residue was seen at the edges of the patterned area. The etching time for subsequent samples was then reduced to 15s, which reduced the residue seen earlier. The faster etching of the annealed B implant is an important observation and it can be predicted that a high concentration of B at the surface is present. The flash-annealed doped layers etch faster than conventionally spike annealed and diffused layers. They also show higher leakage than the diffused layers in addition to lower junction depth.

Generally, the leakage current densities found in this experiment are higher than for experiment B. As seen in Table 6.4 leakage densities are in the range of 10^{-3}-10^{1} A/cm^2 for flash annealing. This is in contrast with experiment B, where the

leakage was at most 10^{-4} A/cm^2 for PAI with conventional annealing. Graphs were plotted to display the correlation of junction leakage with the base temperature and the maximum temperature. The samples which did not receive flash annealing also showed high leakage.

Table 6.4 Reverse-Bias Current Leakage Measurements for Ge Pre-Amorphized samples with several Annealing conditions and Different Ramp Rates

Boron implant conditions Dose (cm^{-2})	Intermediate temperature (°C)	Ramp rate (°C)	Final temperature	PAI	Average leakage Current (A/cm^2) (1V reverse bias)
B^+,500eV,1E15	700	400	1307	Ge+,30keV	3.9550E-03
B^+,500eV,1E15	900	400	1311	Ge+,30keV	9.5225E-02
B^+,500eV,1E15	1000	400	1325	Ge+,30keV	8.3550E-02
B^+,500eV,1E15	760	50	1307	Ge+,30keV	8.935E-02
B^+,500eV,1E15	900	50	1316	Ge+,30keV	7.20E-02
B^+,500eV,1E15	760	400	1086	Ge+,30keV	4.835E-01
B^+,500eV,1E15	760	400	1196	Ge+,30keV	8.50E-01
B^+,500eV,1E15	900	400	1101	Ge+,30keV	1.085E-01
B^+,500eV,1E15	900	400	1206	Ge+,30keV	3.81E-01
B^+,500eV,1E15	760	400	-	Ge+,30keV	3.060E-02
B^+,500eV,1E15	900	400	-	Ge+,30keV	1.64E-01
B^+,500eV,1E15	1000	400	-	Ge+,30keV	6.125E-01
B^+,500eV,1E15	760	50	-	Ge+,30keV	8.54E-01
B^+,500eV,1E15	900	50	-	Ge+,30keV	9.75E-01
B^+,500eV,1E15	820	400	1200	Ge+,10keV	1.655

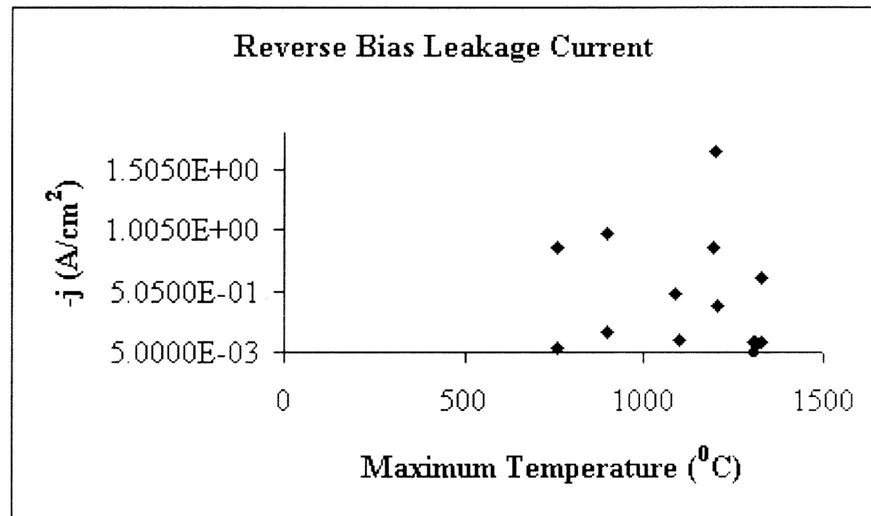

Figure 6.7 Leakage current density vs maximum temperature.

Figure 6.7 shows the leakage current density versus maximum temperature. This set of samples had a higher Ge PAI than in the previous Experiment B and also they were flash annealed. This appears to have an effect on the defects in the junction. The samples show a considerably higher amount of leakage when compared to Experiment B. Figure 6.8 shows the leakage current density as a function of the intermediate temperature.

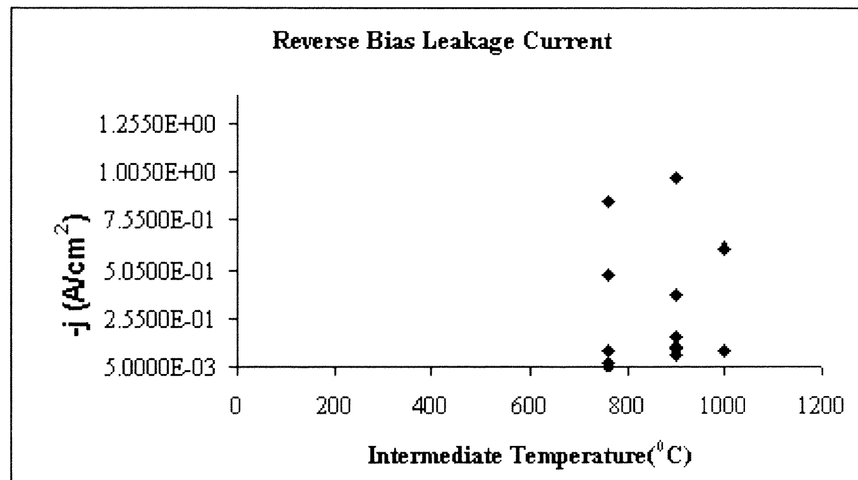

Figure 6.8 Leakage current vs intermediate temperature.

The results shown in Figure 6.7 and Figure 6.8 show that there is no obvious general correlation with T_i or final temperature. A noticeably high leakage is observed for the low energy 10 keV PAI, which is similar to the observation of high leakage found in experiment B (0.5 keV B, 10 keV Ge PAI). Another perhaps noticeable result in the data is that the combination of low T_i and high final temperature may exhibit lower leakage. The general conclusion is that the optimum concentration of PAI, T_i and final flash temperature remains to be found, since the leakage for flash annealing is much higher than for conventional spike annealing.

CHAPTER 7

CONCLUSIONS AND REMARKS

Reverse bias voltage was applied to p-n junction diodes made from B implanted Si and the leakage currents were measured. This leakage current was then compared with shallow junction process parameters such as implant dose, implant energy and annealing conditions.

In Experiment A the arc lamp annealed samples showed less leakage than the incandescent lamp spike annealed samples. The sheet resistance for both these cases of annealing decreased with increase in maximum temperature. From this experiment, the results showed that the leakage current densities tend to be lower for the arc lamp spike annealing method when compared with the incandescent lamp spike annealing.

Experiment B showed less leakage current density for both 10 keV and 80 keV Ge pre-amorphization followed by boron implants. The PAI helps to reduce the range of the boron implants, but it also allows defects to be formed in the junctions. It was also observed that low B implant energy with high energy Ge PAI leads to low diode leakage. Also, from the same experiment it is concluded that the annealing conditions can be predicted by the results observed. The annealing conditions in this experiment were not divulged but, from the experimental results obtained in this work, it is seen that one set of samples with 80 keV Ge PAI received a larger thermal budget than the other set. Low leakage for Ge PAI is observed for low PAI energy and high B implant energy, and vice versa. This is explained by the need to separate the residual damage caused by the PAI from the junction region.

Experiment C leads us to believe that the junction depths were much shallower for samples that are flash annealed. This result is concluded from the fact that the wet chemical etching of samples at normal time of 30s was much faster and showed formation of grooves at the edges of the diodes. Flash annealing was also a major factor in the consideration of the leakage current density of the samples. Flash annealing of B implants with Ge PAI showed up to 10^4 higher leakage than similar implants with conventional spike annealing, as in Experiment B. A lower intermediate temperature and a higher final temperature for flash annealing were found to exhibit the least leakage.

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