ABSTRACT

GATED MULTI-CYCLE INTEGRATION (GMCI) FOR FOCAL PLANE ARRAY (FPA) APPLICATIONS

by
Haijiang Ou

In this thesis, the model and the theory of gated multi-cycle integration (GMCI) were first developed specifically for focal plane array dealing with repetitive or modulated image. The operational modes of GMCI include gated integration (GI), phase sensitive integration (PSI), multi-point summation, multi-point subtraction, multi-sample averaging and some of their combinations. Thus, the analytic theory of GMCI somehow unifies the theories of gated integration, phase sensitive detection, multiple summation and average. PSI works with background and/or dark current subtraction. As a result, the storage well of a pixel is mainly used for signal integration even if there exists a strong background. Thus, the signal-to-noise ratio, the dynamic range, the sensitivity of the detection and the noise equivalent temperature are greatly improved. For a storage well of 10^6 electrons, the sensitivity of the FPA operated at PSI mode could be improved by 3 orders. In addition, the transmission windows of PSI peak at odd harmonics of the modulation frequency, and therefore, the detector's 1/f and other low frequency noise can be attenuated.

A switched capacitor integrator was designed and fabricated with HP-0.5μm CMOS processing to demonstrate the feasibility of GMCI. The primary experimental results showed that the minimum detectable signal could be 5 orders less than the background, which is impossible for the conventional readout methods employed by current staring FPAs. The fixed patterns associated with switching charge injection,

feedthrough, offset voltage of operational amplifier were addressed and suppressed by taking the differentia of two sampled voltages that correspond to signal integrations with 180^{o} phase difference while keeping the same fixed pattern. GMCI, operated at PSI with multiple averages, is expected to become a powerful method in dealing with repetitive weak image swamped by strong background.

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To my family

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CHAPTER 1

RESEARCH BACKGROUND

1.1 Introduction

The term ***Focal Plane Array*** (FPA) is used to refer to an imaging system having its optical focal plane placed with a large number of detectors simultaneously integrating signals from an image projected onto the array. Visible and infrared FPAs have found a variety of rapidly growing industrial, commercial, military, and scientific applications. Current trends of solid-state focal plane array are pursuing high pixel density for high resolution, much more on-chip processing for more function and high efficiency, low power consumption for space application, room temperature IR operating for hand-held use, new detector materials for covering more spectral bands, and multi-color imaging for more information. Widely used imaging systems such as Si CCD (charge coupled device), CMOS APS (complementary metal-oxide field effect transistor active pixel sensor), Schottky-barrier detector (SBD), InGaAs, InSb, and HgCdTe FPAs are all based on the concept of current integration to accumulate signal in the purpose of improving signal-to-noise ratio, dynamic range and sensitivity. Small unit area but high performance integrators such as detector direct integration (DDI) or source- follower per detector (SPD), direct injection (DI), buffered direct injection (BDI), gate modulation input (GMI), and capacitive transimpedance amplifier (CTIA) are well known in the FPA community. They are very successful in the applications with low to high backgrounds given the signal is not far lower than background. The integration, however, includes both the signal-induced and background-associated (including detector's dark current)

currents at same time. Consequently, present single integration FPA technology encounters intrinsic difficulty when dealing with repetitive images and weak images buried in strong backgrounds. Examples are pulse laser-induced fluorescence or Raman imaging in biosciences [1,2], solar magnetography where signal is four orders less than background [3], and very long wavelength IR FPA [4] where the detector's dark current is significant.

Alternate integrators such as current memory [4,5], dynamic current mirror buffered direct injection (DCM-BDI) [6], and correlated capacitive transimpedance amplifier (CCTIA) [7] were proposed to solve the difficulty. However, the requirement of a calibration phase made the CM and DCM-BDI impracticable. CCTIA will not properly work since it requires the detector forwardly biased. Nevertheless, the concept is worth for further consideration.

Current technologies for pulse laser-induced imaging are confocal laser scanning microscopy [8] and gated intensifier CCD [9]. The former takes an image point by point by using a photomultiplier tube. The later uses CCD to form the second image from the primary image captured by the gated intensifier, thus, the resolution is limited by the primary image of the intensifier. In both cases, the image signal from each pixel is acquired through a single integration.

It is well known that boxcar averaging, lock-in amplifier and photon counting are powerful technologies used to detect weak repetitive signals. They have played very important roles in developing modern sciences. However, their applications are limited to a single detector due to the complexity of the systems.

In dealing with the weak repetitive image (if the image is not repetitive, it can be modulated) buried in strong background, the theory of an alternate integration method, called gated multi-cycle integration [10-12], is developed. It unifies the basic concepts of phase sensitive detection, gated integration, multiple summation and averaging. Before presenting the theory of multi-cycle integration, the basic concepts of FPA and some related background information are briefly reviewed.

1.2 Structure of FPA

A FPA usually refers to a solid-state imaging system with array detectors placed on the optical focal plane where an object is imaged. A FPA could be scanning or staring. To take an image, a scanning FPA uses a linear array detector, which scans in the direction perpendicular to the array. The advantage of scanning array is its relative simple configuration and low cost. The disadvantage is that it needs an additional scanning system. Therefore most scanning FPAs are used on satellites or airplanes for mapping clouds, ground, or resources on the ground while the scanning is automatically carried out by the flight of the satellites or airplanes. A staring FPA uses an area array. Its advantage is its efficiency to take images, since it does not need scanning, and is therefore more compact.

A complete digital FPA system usually includes a photon-sensing array, signal preamplifiers or input unit cells, multiplexer, correlated double sampling (CDS) circuit, output or video amplifiers, analog-to-digital converter (ADC), post readout processing circuit, bias and pulse generator, optical lens, display, and sometimes cryogenic set for cooling detectors. CDS circuit may be put in the unit cell or after multiplexing or just

calculated in the post readout processing. Fig.1.1 shows the block diagram of a FPA system.

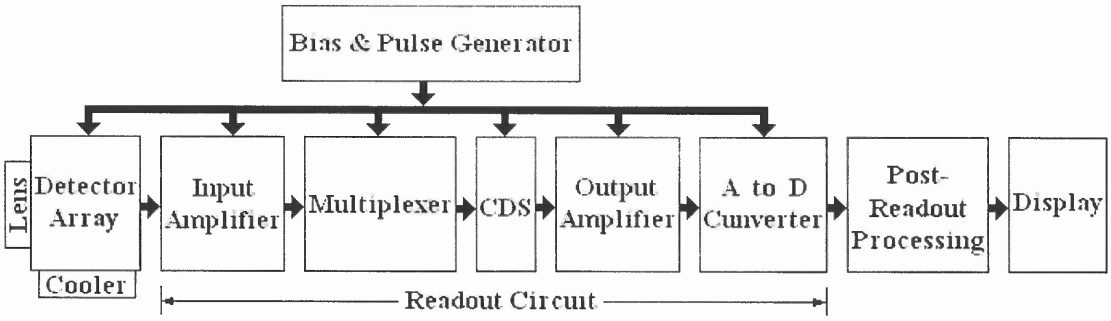


Figure 1.1 Block diagram of a FPA

A chip that at least includes the input unit cells and multiplexer is called readout circuit. The most important two components in a FPA are the detector array and the readout circuit. FPAs can be fabricated in two basic configurations, monolithic and hybrid. For a monolithic FPA, the detector array and the readout circuit are integrated in the same chip. Because they are fully integrated, they are potentially inexpensive. For a hybrid FPA, the two are fabricated on separate substrates and are connected together by certain bonding technique such as In-bump bonding. Readout circuit is almost always fabricated on Si substrate in order to take the advantages of the well-developed Si technologies. Silicon is highly sensitive to visible but insensitive to infrared light. Si monolithic FPAs are dominant in visible range. Two well-known visible FPAs are Si CCD and CMOS APS. By contrast, narrow-band-gap materials are highly sensitive to infrared wavelengths. Hence infrared FPA usually is hybrid, except PtSi SBD FPA, to take advantages of both detector material and Si. Commercial IR FPAs with high performance are InGaAs photovoltaic (PV) FPA operating at 1.3~1.7μm, InSb PV FPA

working at 3~5μm, GaAs/AlGaAs MQW photoconductor (PC) FPA functioning at 8~20μm, and HgCdTe PV FPA performing at 1~14μm. They are all hybrid.

1.3 A Brief History of FPAs

The development of FPA is a history of finding and improving both detector materials and readout methods. People used thermal and photon detectors for a long time. However detector array and readout circuit were not available until micro-electronic technologies were developed. In fact, FPA actually is an integrated circuit. It started with the invention of Si integrated circuit.

As early as in 1800, Sir Frederick William Herschel first found infrared radiation when he used a thermometer to measure the spectrum of the sun. More sensitive photon infrared detectors were not developed until 1940's, mainly due to their military applications. The first practical IR detector was PbS, which can detect IR radiation with wavelength up to 3μm. Intrinsic Si and Ge covered the visible and near infrared (NIR). Beginning in the late 1940's and continuing into 1950's, PbSe, PbTe, and InSb extended the spectral range beyond that of PbS, providing sensitivity in the 3-5 μm medium wavelength infrared (MWIR) atmospheric window. The important HgCdTe detector was introduced in late 1950's with high sensitivity up to 14 μm long wavelength infrared (LWIR) spectral window. At the same time extrinsic impurity doped Ge and Si conductive detectors extended the wavelength to very long wavelength (VLWIR) of 14-30 μm.

Linear detector arrays were first demonstrated with PbS, PbSe, and InSb in the early 1960's when photolithography became available. Photovoltaic (PV) detector

development began with the availability of single crystal InSb material. The discovery in the early 1960's of extrinsic Hg-doped germanium led to the first forward looking imaging radiometer (FLIR) system operating in the LWIR spectral window using linear array. However it required a two-stage cooler to operate at 25K because it was an extrinsic detector. Later on intrinsic HgCdTe photoconductor linear array were developed in the late 1960's and early 1970's. These allowed LWIR FLIR systems to operate at 80K in a dewar with liquid nitrogen.

First generation IR imaging systems used liner arrays coupled with room temperature preamplifiers. Consequently, each detector element in the array had an individual conductive signal lead, which had to feed through the cryogenic vacuum dewar wall. This approach limited first generation linear arrays to less than two hundred elements.

The important concept of signal integration, suggested by Weckler [13] in 1967, began the second generation of scanning FPAs. In his approach, photon flux induced photocurrent was integrated on a reverse-biased junction capacitance. Integrated charges were read out through pMOS switches. Thus, multi-pixels can be read out one by one through a multiplexer. The advantages of this approach were revolutionary. First, it increases the signal-to-noise ratio by accumulating more photons through increasing integration time. Previous instant signal voltages were usually less than 0.1 μV, which were quite susceptible to noise. Second, it reduced tremendously the complexity of the signal readout. One pixel one lead was replaced by a single integrated multiplexer. Third, integrated readout circuit can be directly coupled to sensor array, making the imaging system more compact and more resistant to the interference from electronic and magnetic

fields nearby. Following the integration concept are different basic integration methods such as direct integration (DI), source-follower per detector (SFD), buffered direct injection (BDI), gated modulation input (GMI), and capacitive transimpedance amplifier (CTIA). However, at that time, MOS switch readout circuits suffered from fixed pattern noise (FPN) [14].

In 1970, charge-coupled device (CCD) [15] was first reported with attractive features of freedom of FPN and small pixel pitch. Since then CCD has dominated the visible FPA for 40 years. Array size of 5120×5120 [16] has been demonstrated with dynamic noise level of 3 to 5 electrons and a dynamic range of over 80dB. CMOS imaging, beginning in early 1970's and rapidly re-growing after early of 1990's, shows its urgent ambitious trying to take over the visible market due to its much lower power consumption [17]. Camera on a single chip is only realized by CMOS technology. However, today's scientific instruments are still embracing CCD because of its better overall performance.

In IR region, early hybrid FPAs used conventional CCD as readout circuits. This has all the advantages of low noise, high storage capacity and linear response. This approach showed that photovoltaic (PV) detectors such as InSb, PtSi, and HgCdTe detectors or high impedance photoconductors such as PbSe, PbS, and extrinsic silicon detectors were promising candidates because they had impedances suitable for interfacing with readout multiplexers. Monolithic extrinsic silicon detectors were demonstrated first in the middle of 1970's. Later on it was set aside because the process of integrated circuit fabrication degraded the detector quality. Monolithic PtSi Schottky detectors, however, in

which the detector can be formed after the readout is processed, are now widely available.

Since the invention of the CCD, it had taken nearly two decades to develop the technology of integration of IR detectors and electronic readout circuits. A milestone in the development of readout history is the correlated double sampling (CDS) method [18], which can effectively reduce kTC noise of reset, low-frequency noise of detectors and FPN due to switching. By using CDS, CMOS readout circuit has gradually replaced CCD multiplexer for hybrid FPA system, because CMOS readout has better performance at low temperature and can integrate more functional circuitries such as self scanning address and analog-to-digital converter (ADC) in the same chip.

The first high performance second-generation hybrid array was demonstrated in 1978 using InSb PV detectors in a 32×32 array format. Second generation devices have now been demonstrated with many detector materials and devices types. These materials and devices include PbS, PbSe, InSb, extrinsic Si bulk devices, PtSi Schottky, HgCdTe PV and GaAs/AlGaAs MQW PC detectors with array size up to 2048×2048.

In late 1980's, with advance molecular beam epitaxy (MBE) and metal-organic chemical vapor deposition (MOCVD) epitaxial growth techniques available, tailored InGaAs/InP PV and AlGaAs/GaAs QWIP materials became the new members in the infrared community covered the wavelength in the NIR and LWIR, respectively. With maturated material and processing technologies of GaAs/AlGaAs, plus the high performance of the Sterling cryostat, hand-held GaAs/AlGaAs QWIP FPA camera become dominate in commercial LWIR market. With advanced micro electro-mechanical system (MEMS) and submicron technologies becoming available, uncooled thermal

detector FPA made great progress in 1990's. NEΔT of 20 mK^{o} was reported in a recent SPIE conference [19].

Before 1990, the development of infrared sensors had mainly centered on the growth, fabrication, measurement, and optimization of IR materials and detectors. The signal readout of the detector had been given less attention since IR sensor performance was limited by materials at that time. With rapid advancement in material growth and in micro-chip processing, detector arrays became well suited. In addition, with sub-micron technology available in 1990s, readout methodologies started to gather attention. That is reflected in four specific conference proceedings on the readout circuit [20-23] organized by the International Society for Optical Engineering (SPIE) during 1990s. Recent pursuit of readout tends to build more functional circuitries, such as for A/D converter, edge enhancement, non-uniformity correction, towards the third generation of "smart" FPA. Now FPA technology seems quite mature from visible to LWIR, except in the case of weak image signal buried in strong background. With background several orders stronger than image signal, it is the readout electronics rather than the detectors that limit FPA performance.

1.4 Performance of FPA

The general feature of a FPA falls into broad categories of array format, pixel size, storage capacity, input interface, signal conversion gain, minimum readout noise, dynamic range, integration time, noise equivalent temperature difference, maximum frame rate, maximum data rate, operating temperature and power dissipation.

1.4.1 Array Format

Array size usually follows the format of $2^n \times 2^n$, such as 128×128, 256×256,···, 2048×2048 or VGA format, such as 640H×480V, ···, 1600H×1200V. Larger array provides better spatial resolution at cost of lower yield and higher price. Commercial FPAs usually have array sizes from 128×128 to 1024×1024.

1.4.2 Pixel Size

Pixel pitches are around 15 to 50 μm for hybrid FPAs and 5 to 15 μm for monolithic FPAs. With array size becoming larger, the pixel pitch tends to shrink smaller. However, the minimum pixel size is limited either by input unit circuit or optical diffraction. For hybrid FPAs, it may also be limited by the interconnection between the sensor array and the readout chip.

1.4.3 Storage Capacity

Charge storage capacity is determined by the capacitance of the integrator circuit, which is limited by the real estate of a chip, as well as the saturation voltage of the readout circuit. It varies from 10^5 to 10^7 electrons. Large storage capacity means large pixel pitch and higher kTC noise (see 1.4.5). Here k is the Boltzman constant, T the temperature, C the capacitance of the integrator. Large capacity is only necessary for high dynamic range or strong background applications. Most FPAs have capacities in the order of 10^6 electrons.

1.4.4 Signal Conversion Gain

The signal conversion gain is defined as the integrated voltage per input charge. It is dependent on the quantum efficiency of the detector and the capacitance of the integrator.

Higher quantum efficiency and lower integrating capacitance result in a higher signal conversion gain. The gain can vary from 0.1 to 20 $\mu V/e^-$.

1.4.5 Noise

General noise in a FPA system includes fluctuations related to photon flux (both signal and background), detector, readout electronic circuitry and its nonuniformity. Photon related noise is called photon shot noise measured as the square root of the number of integrated photo-induced electrons. Thermal, dark current shot, and 1/f noises are the main detector associated noise sources [24]. Electronics noise includes the unit cell integrator noise, as well as the downstream multiplexer, driver amplifier and analog-to-digital converter noises. The unit cell electronics is the main electronics noise source, which includes the transistor white noise, 1/f noise and reset noise. Reset noise is also called kTC noise, since the resetting of an integrator through a transistor switch has an uncertain residual charge, the rms (root mean square) value of which is equal to $(kTC)^{1/2}$. 1/f and kTC noises can be reduced through the well-known correlated double sampling (CDS) methodology. Readout noise is directly related to the readout method. A normal FPA system has readout noise from tens to hundreds of electrons. Carefully designed FPA may have minimum readout noise less than 10 electrons by using CDS. CCD readout has minimum readout noise around a few electrons. However, CCD readout has been abandoned by the hybrid infrared FPA due to its performance degradation at low temperature and its process incompatibility with CMOS technology. Finally, the fixed pattern noise (FPN) is associated with randomly distributed, time- invariant offsets in unit cell circuits. Generally, it is feasible to control readout noise at a level lower than detector

noise or photon shot noise. Hence, readout noise will become critically important when signal photon flux is extremely low.

1.4.6 Dynamic Range

Dynamic range is defined as $20\log_{10}(SNR_{max})$, where the maximum signal-to-noise ratio $(SNR)_{max}$ is defined as the ratio of the maximum signal that can be integrated to the noise floor. SNR_{max} can be understood as the ratio between the brightest feature to be observed and the weakest detectable one. The dynamic range of a normal FPA is usually limited by the charge storage capacity, typically 60-70 dB for consumer products and 70-80 dB for scientific applications.

1.4.7 Integration Time

Integration time is one of the most important parameters for the application of a FPA. The longer the integration time, the better the signal-to-noise ratio. Consequently, the higher the dynamic range and the better the sensitivity. Integration time is not only determined by the capacity of the FPA, it is also determined by the photon flux of the application. When the background or dark current is dominant compared to the signal, current readout methods will fail to obtain meaningful SNR. A good FPA has an integration time close to the frame time.

1.4.8 Noise Equivalent Temperature Difference (NEΔT)

In IR thermal imaging, NEΔT represents the temperature variation from incident radiation source, which gives an output signal equal to the rms noise level. System NEΔT usually is inferior compared to that of a single detector because there the exists system

loss and the nonuniformity of pixels. Another more preferred figure of merit for IR FPAs is the minimum resolvable temperature (MRT). MRT is a function of spatial resolution and is defined as the signal-to-noise ratio required for an observer to resolve a series of standard four-bar targets. It includes the effect of human eye's response.

1.4.9 Maximum Frame Rate

Frame rate is usually inversely proportional to the integration time. Maximum frame rate gives the shortest integration time an FPA can provide. When the scene is bright, the integration time needs to be short. The integration time could be as short as 0.1 μs and as long as tens of hours.

1.4.10 Maximum Data Rate

Maximum data rate is the maximum output data transfer rate and is usually determined by the main clock rate and may be limited by the speed of ADC. For a large FPA, e.x., 2048×2048, output data must be quite fast. With multi-video-output architecture, maximum data rate of 800 MHz is commercially available for CMOS camera.

1.4.11 Operating Temperature

Visible and thermal IR detector FPAs usually operate at room temperature, while photon detector FPAs usually need a cooler to suppress detector dark current to increase the integration time. The operating temperature of IR FPAs is set by the detector cutoff wavelength. The longer the cutoff wavelength of the detector is, the larger the thermally generated dark current, resulting in a mandatory colder operating temperature.

1.4.12 Power Dissipation

Low power dissipation is always preferred for hand-held cameras and for IR imaging systems operating at low temperature. In a FPA, most power is consumed by the readout circuit. This is one of the main reasons why CMOS readout circuits become the predominant player for hybrid FPAs, and why CMOS APS camera becomes a strong competitor to CCD camera.

The performance requirements vary with applications. For example, astronomical observation usually requires low noise, long integration time and high bit ADC due to low background flux. High background or LWIR needs precise control of detector bias, large charge capacity and snap shot function. Digital camera for family use pursues high resolution, low power, and large memory at low price. The performance of a FPA also varies with the type of detectors and the input readout method.

1.5 Commonly Used Input Unit Cell Readout Circuits

In a FPA construction, readout circuit is a signal processing circuit that accumulates signals from every detector in the array and transfers the integrated signals to the video output. First generation FPAs used the same number of AC amplifiers as the number of pixels, as well as the number of leads that connect detectors to the amplifier. This approach has been replaced by second-generation FPA technology, which uses unit cell readout circuit plus one or a few multiplexer to process signals. For photon detector FPAs, a unit cell readout circuit or a unit cell input amplifier circuit becomes a unit cell integrator, which integrates the signal current as well as the background and dark currents. Thus, the unit cell integrator is an important topic in the FPA community. The

requirements for the unit cell integrator are: 1. The layout of the unit integrator must be limited within the pixel area. This means that the integrator cannot be composed of more than a few transistors, say less than 5 transistors for a large 2D array. 2. The noise of the integrator should be less than that from the detector. 3. The integrator must be matched with the detector at the operating temperature: the integrator should have good linearity and responsibility, and can effectively integrate the signal with the given background and impedance of the detector. 4. The power consumption should be low. Since the first proposal of the signal integration in late 1960s, integrator has been sufficiently studied and practiced. There are only a few matured integrators that satisfy the above requirements and represent the state-of-the-art FPA readout technology. These input unit cell integrators are direct detector integration (DDI) [25] (also called source follower per detector), direct injection (DI) [26], buffered direct injection (BDI) [27], gate modulation input (GMI) [28] (also called current mirror integration), and capacitive transimpedance amplifier (CTIA) [29]. They will be briefly reviewed in this section.

1.5.1 Direct Detector Integration (DDI)

A readout integrator must have at lease one capacitor to collect signal-induced charges. The most simplified integrator is the direct detector integration, which utilizes the junction capacitance of the detector. Fig. 1-2 illustrates the schematic of DDI. At the starting time of a frame, the reset switch pre-charges the junction at certain voltage level. The current (includes the signal-induced current) passes through the detector will then discharge the capacitor. By the end of the frame, the buffered voltage signal will be sensed to the output amplifier by enabling the selecting switch. DDI is an RC discharging circuit. In order to get a good linearity of a RC circuit, the RC time constant must be

much larger than the integration time. Thus, DDI is only suited for high impendence of detector and low background application. In DDI, the detector must be heavily reversely biased in order to obtain adequate dynamic range. The noise sources of DDI are the reset kTC noise and the input MOSFET's 1/f and channel thermal noises. The advantage of DDI lies in its simplicity. In fact DDI construction uses a minimum number of transistors among all the input integrators. This is why the DDI is widely employed in today's large format FPAs from visible to MWIR range.

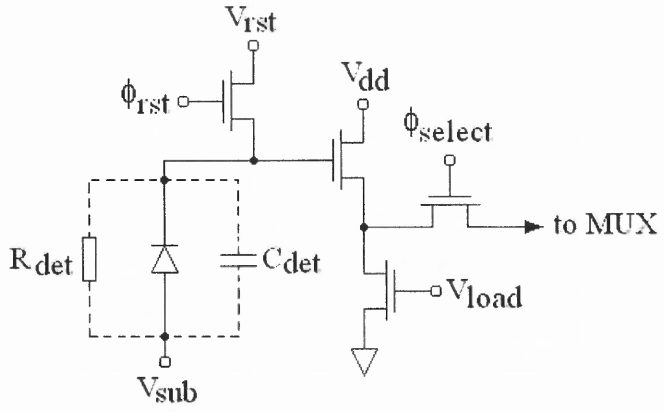


Figure 1.2 Schematic of a direct-detector integration

1.5.2 Direct Injection (DI)

Instead of using the detector junction capacitor as the integrator, direct injection scheme uses a separate integration capacitor C_{int} as shown in Fig. 1.3. The unit cell consists of an active injection transistor, a reset transistor, an output selection transistor, and an integration capacitor. The photon current from detector is injected, via the active injection transistor, onto the integration capacitor that has been reset prior to the beginning of integration. After integration, the charges accumulated on the capacitor is either dumped

on to the column selection line or is buffered by a source follower to provide voltage mode output.

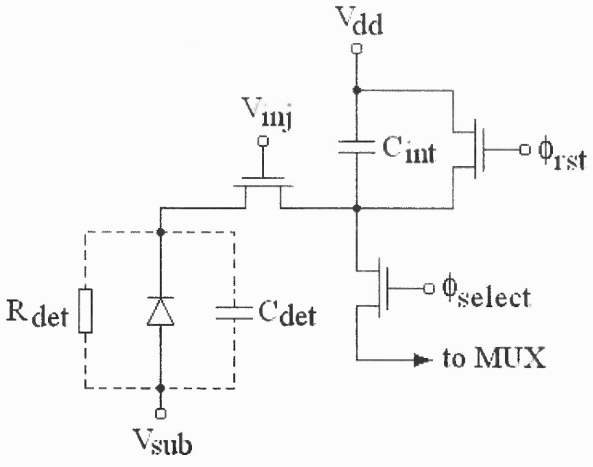


Figure 1.3 Schematic of a direct injection unit

Since the photocurrent is input through the injection transistor, the DI scheme yields somewhat better bias control during integration compared to DDI. However, the nonuniformity of the threshold voltage of the injection transistor will cause FPN directly. Since the detector is not directly reset, residual charges from one frame can be integrated into the next frame, resulting in frame-to-frame crosstalk.

The input of the DI should provide a low impendence to the detector. This provides a stable detector bias and a high photocurrent injection efficiency. If the input impendence is too high, a fraction of photocurrent will be bypassed across the detector and not injected to the capacitor, resulting in a loss of SNR. This injection efficiency, which represents the percentage of detector current that can be stored, is

$$\eta_{inj,DI} = \frac{g_m R_{\det}}{1 + g_m R_{\det}} \tag{1.1}$$

where R_{det} is the detectors' dynamic resistance, g_m the transconductance of the injection transistor.

g_m is a strong function of the drain current of the MOSFET, which is typically very low since it directly comes from the detector. In many injection applications, the injection transistor operates in weak inversion. The transconductance is given by

$$g_m = \frac{qI_D}{mkT} \tag{1.2}$$

where I_D is the drain current of the input transistor, q the charge of an electron, m the sub-threshold ideality of the input transistor. It is clear that g_m and R_{det} must be large in order to get high injection efficiency. This limits the DI applications to medium and high photon flux and detectors with cutoff wavelength not beyond MWIR. This in turn means that the integration capacitance should not be made too small. The overall advantage of DI is its small unit area. Comparing to DDI, DI extends the photon flux to medium and high.

1.5.3 Buffered Direct Injection (BDI)

The poor injection efficiency of DI can be overcome by buffered direct injection (BDI) configuration as shown in Fig. 1.4. The injection transistor is controlled by an inverting amplifier with open-loop gain $-A_v$. The effective g_m is increased by a factor of $(1+A_v)$. Consequently, the injection efficiency and the minimum photon flux are improved by a factor of $(1+A_v)$. Another benefit from BDI is that the inverted gain provides feedback to yield a better control over the detector bias at different photocurrent levels. BDI is not suited for extreme low photon flux.

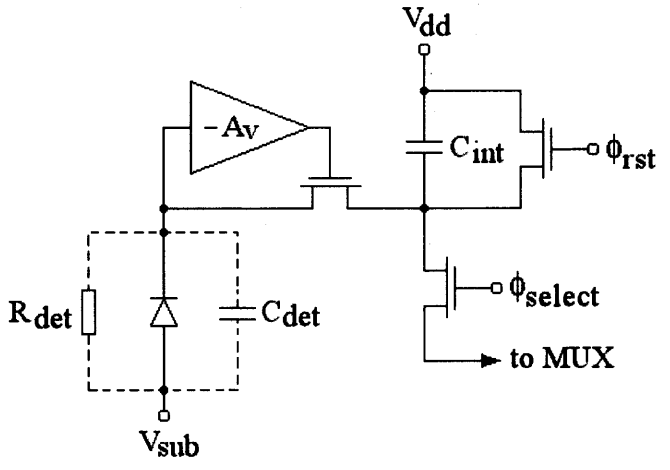


Figure 1.4 Schematic of a buffered direct injection unit

1.5.4 Gate Modulation Input (GMI)

In a gate modulation input scheme as shown in Fig.1.5, the detector is connected in series with a load, either a passive resistor load or an active transistor load. The voltage across the load is used to modulate the gate voltage of an input MOSFET. The output current of the input transistor is then to discharge a capacitor previously reset to a reference level. When the load is a transistor, the configuration of the GMI actually is a current mirror (CM).

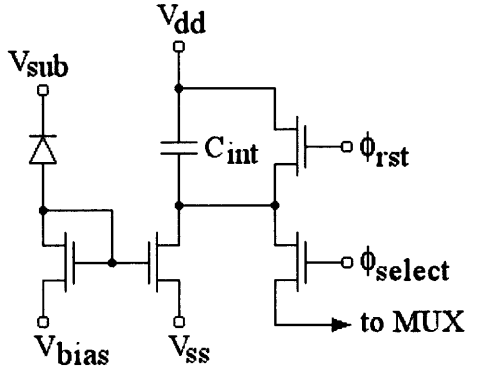


Figure 1.5 Schematic of a gate modulation input

The main advantage of the GMI is the current gain that can be set through adjusting the detector bias V_{bias}, the source voltage of the input transistor V_{ss}. For active load the current gain is given by

$$A_I = (\eta + I_{det} / I_p)\frac{(W/L)_{Input}}{(W/L)_{Load}}\exp[\frac{q}{mkT}(V_{bias} - V_{ss})] \quad (1.3)$$

where I_{det} is the dark current of the detector, I_p the photon-induced current. Thus, the integration current can be scaled up or down several orders by adjusting biases and the dimensions of the transistors. A large current gain lead to higher charge detection sensitivity and reduced input-referred noise levels. A fraction gain is useful for the application of strong background. However, the signal is also scaled down. For this reason, the capability of the background suppression is susceptible.

The nonuniformity of detector's dark current as well as the threshold voltage variation in the input transistor causes the current gain to vary from one cell to another, resulting in big FPN. The detector as the input of the GMI must have a high impendence in order to keep high injection efficiency. CM has been used for low background application of InGaAs FPAs and for LWIR of GaAs/AlGaAs QWIP FPAs.

1.5.5 Capacitive Transimpedance Amplifier (CTIA)

Figure 1.6 shows the configuration of CTIA. It consists of an inverting amplifier, an integration capacitor C_{int} placed in a feedback loop, and a reset transistor in parallel with the integration capacitor. The amplifier could be a simple CMOS inverter, a simple cascade amplifier or a more elaborate differential amplifier. The choice of the amplifier is considerably upon with the respect to open-loop voltage gain, bandwidth, power dissipation, linearity, and unit cell real estate.

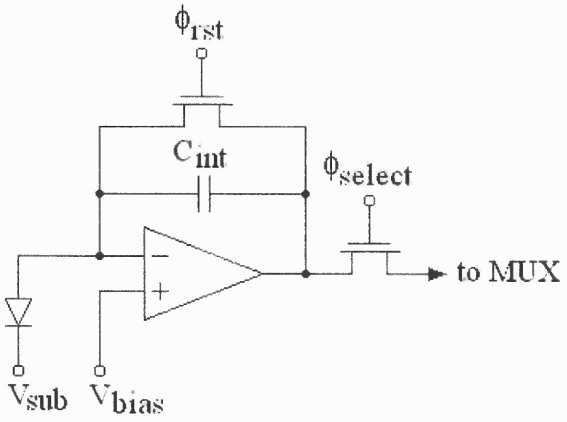


Figure 1.6 Schematic of a CTIA.

Due to the high open-loop gain of the amplifier, the voltage at input node of the CTIA is virtually fixed, resulting in a tight control on the detector's bias. It also maintains an almost 100% collection of the photocurrent to the feedback capacitor, yielding a high injection efficiency. A good linearity is another advantage of CTIA. Since the capacitance can be made very small, say a few fF, the transimpendence of the CTIA can be extremely high, yielding a higher detector sensitivity and excellent low noise performance. CTIA has overall best performance characteristics [29] among the conventional input integrators and is an ideal readout circuit embraced with many circumstances.

1.6 Researches on Background Subtraction

Conventional input integrators, as discussed in previous subsections, integrate both signal-induced current and background (including detector dark current). In this thesis, background is used to indicate both the current due to background radiation and the

detector dark current. It is difficult for these integrators to deal with weak image buried in strong background. There are special applications that need to recover weak images swamped by strong background. There are cases when the integrator is saturated by the background while the accumulated signal level is still less than the background related noise. Pedestal removal in FPA readout has been studied for many years. From the earlier "skimming", "partitioning" to recent "dynamic current mirror buffered direct injection", "current memory" and "correlated readout", yet there is still no convincing approach that is widely accepted. The remaining useful technology to deal with weak image swamped by strong background is the post-readout averaging. However, the accuracy of multi-frame averaging is limited by the least step of ADC and it also suffers from the background drift and low frequency noise.

1.6.1 Skimming and Partitioning

Skimming and Partitioning [30] were fulfilled in a CCD readout circuit. The principles of skimming and partitioning are illustrated in Fig. 1.7. Photo-generated charge is integrated in a potential well formed under gates V_{store} and V_{part}. Charge skimming is a process of setting the V_{skim} potential barrier at an appropriate level and skimming only the overflowing charge into the integrating ϕ_{CCD} well. Charge partitioning is a process of dividing the input charge into two packets by raising the V_{part} potential. The small charge packet is passed to the transport CCD, with or without skimming. The large packet is dumped through the drain diode V_{drain}. In this way, a gain reduction is realized.

Skimming and partitioning requires integrating the complete signal prior to background suppression and would not alleviate the recovery of weak image.

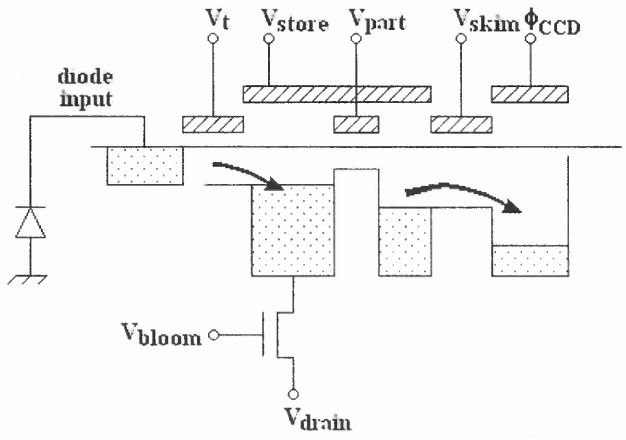


Figure 1.7 Schematic of skimming and partitioning

1.6.2 Dynamic Current Mirror Buffered Direct Injection (DCM-BDI)

Figure 1.8 shows the schematic of DCM-BDI [6]. It operates in two phases, calibration phase and integration phase. During the calibration phase, signal flux is blocked and switch S is on. The gate voltage of M2 is maintained at a level necessary to sink the reference current through the readout M1 and the photodiode. At same time the integration capacitor is reset. This is possible if the detector substrate is held at the level slightly above the threshold of the active M3. At integration cycle, only the signal-induced current is integrated through the way of BDI because the detector current is compensated during calibration.

There are several drawbacks of this approach. First, detector dark current is forced to be the reference current. It is dangerous to the diode if the dark current is lower than the reference current. Second, the reference current can hardly keep constant if the M1's drain voltage is going down due to integration. A transistor biased at a reference voltage

usually provides the reference current source of this scheme. The lowering voltage at this node will increase the reference current, yielding the loss of signal.

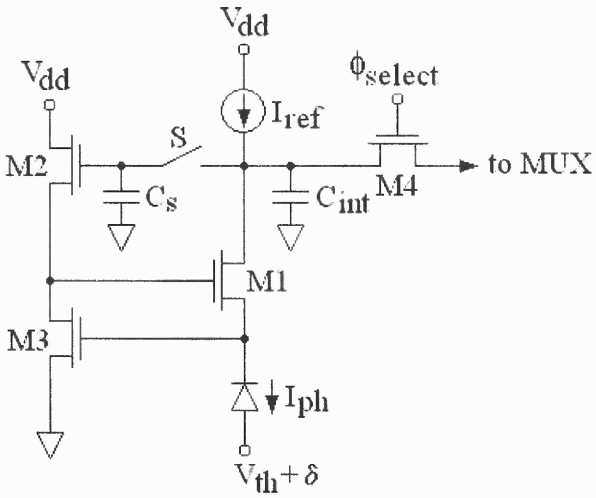


Figure 1.8 Schematic of a DCM-BDI

There are several drawbacks of this approach. First, detector dark current is forced to be the reference current. It is dangerous to the diode if the dark current is lower than the reference current. Second, the reference current can hardly keep constant if the M1's drain voltage is going down due to integration. A transistor biased at a reference voltage usually provides the reference current source of this scheme. The lowering voltage at this node will increase the reference current, yielding the loss of signal.

1.6.3 Current Memory

Current memory also operates in two phases, calibration phase and imaging phase. During calibration, signal flux is blocked and background related current is led to an analog current memory circuit. During imaging, the background is sunk to the current memory circuit except for a small error current $I_{res}= I_b-I_{mem}$ that flows into the integration node. Thus, the signal current plus the error current are fed to the integrator. In order to

eliminate the error current, the error current is also integrated on the integration capacitor after the current memorization is finished at calibration phase. By using correlated double sampling one can virtually eliminate the background. Fig.1.9 shows the schematic of current mode background subtraction (CMBS) [4].

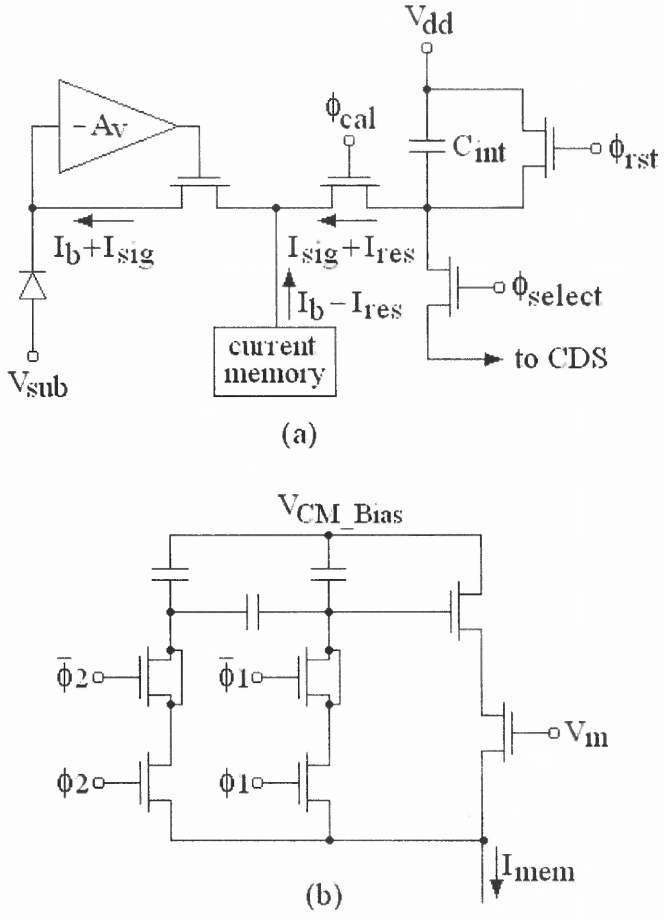


Figure 1.9 Schematic of current mode background subtraction (a) Circuit implementation of CMBS and (b) Circuit schematic of current memory with feedback suppression.

However, the sources of error current are the losing of the memory current due to using an analog memory and the current injection at the time of turning on the calibration switch (initial voltages are different at the integration node and the input node of the memory circuit). The worst feature of the method is that the error current could be a

function of the integration node voltage. In this case, the error current cannot be eliminated completely even CDS is employed lately, resulting in a FPN in the image.

1.6.4 Correlated Readout (CR)

Correlated readout [7,10-12] has been studied since 1996 when Prof. Ken K. Chin and Prof. Haiming Wang at NJIT discussed about the solar magnetography where the signal due to Zeeman splitting is four orders less than background. CR integrates modulated signal by using a correlated integrator while rejecting unmodulated background. The principle of CR is shown in Fig.1.10. Photon flux is chopped by a modulator. Signal current plus background current will charge the integrator in one phase (when the modulator is on). Then background current will discharge the integrator in another phase (signal is blocked) with same duration time. Through charging and discharging the integrator many times, the background is cancelled out while the small signal can be gradually accumulated. Due to the increased integration time, the signal-to-noise ratio and dynamic range can be improved. An additional benefit is its capability of attenuating low frequency noise. In fact, correlated readout is the extension of phase sensitive detection (lock-in amplifier) to FPA area.

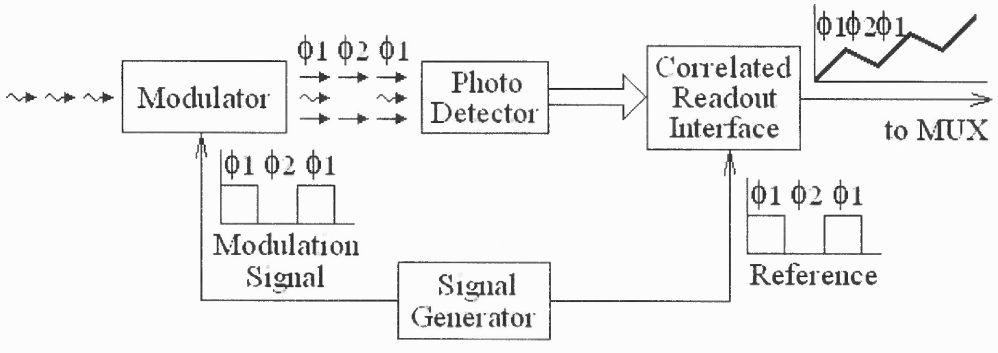


Figure 1.10 The principle of correlated readout

Figure 11 shows the correlated capacitive transimpedance amplifier (CCTIA) initially proposed to fulfill the function of CR. When $\phi 1$ is enabled and $\phi 2$ is disenabled, M1 and M3 turn on while M2 and M4 stay off. The detector is responding to the source signal as well as background so that all the current will be integrated in the integration capacitor. When $\phi 2$ is enabled and $\phi 1$ is disenabled, M2 and M4 turn on while M1 and M3 become off, and the capacitor will be discharged by the background related current only. This process can be repeated until significant signal charges are accumulated. However, this scheme has fetal drawback. The detector is not symmetrically biased in the two phases. In fact a detector is slightly reversely biased in one phase while it is slightly forward biased in another phase. For LWIR applications, it is not allowed to bias a detector forwardly. Another drawback of this approach is it cannot be used for array detectors since array detectors usually have a common subtraction node while the two terminals of a detector in CCTIA case are independent.

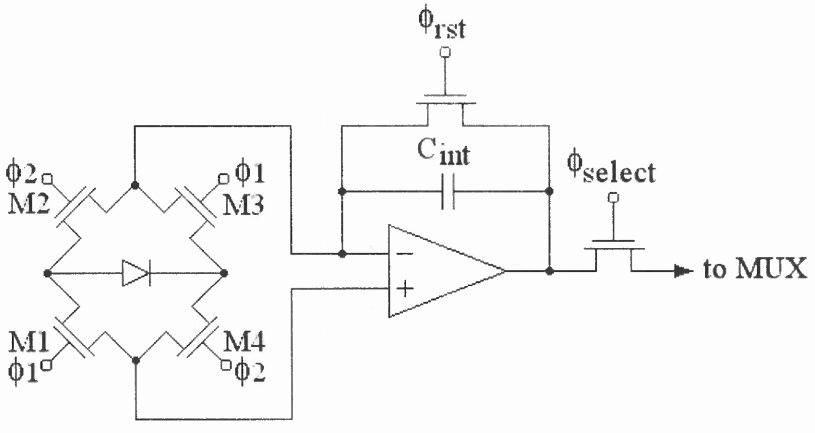


Figure 1.11 Correlated capacitive transimpedance amplifier

Correlated readout reads modulated AC signal and rejects DC and unrelated AC background. This is a preferred way for the measurement of single detector. Since AC

measurement needs to modulate the image source, this is what the second generation FPA tries to avoid because most natural scenes are unmodulated. For the special case of weak image under strong background, however, AC measurement will be the most effective method because the modulated weak image can be separated from the strong background. Furthermore, there are urgent growing requirements of capturing laser-induced weak repetitive images in bioscience.

The readout circuits have been briefly reviewed. More discussion about readout circuitries can be found in some review papers [31-33]. This thesis will focus to construct the general model and the theory of gated multi-cycle integration (GMCI) FPA for repetitive images and to demonstrate the functions of GMCI with a switched capacitor integrator.

1.7 Demands for Repetitive Imaging

Pulsed laser-induced fluorescence or Raman imaging plays an important role in the studies of biology, biochemical and biomedicine samples. Issues such as cancer-related tumors or lesions, spectra of a single molecule, the sequence of DNA are needed to trace. Current technologies of spectroscopic imaging are confocal laser scanning microscopy and gated intensifier CCD. The former takes image point by point through a photo-multiplier tube (PMT), lacks of efficiency, although it has the great advantage of imaging with fine depth resolution. The latter uses a CCD to form the second image from the primary image captured by the intensifier, losing the resolution that the CCD can provide. The wavelength in both cases is limited by the responses of PMT and intensifier. Their cutoff wavelength could be up to 1.1 μm. Since the image signal is usually weak and

repetitive, current high performance FPA systems cannot directly take image due to the way of readout.

1.8 Outline of this Dissertation

In the next chapter, the general model and the theory of gated multi-cycle integration is presented for FPA taking repetitive image with any duty of cycle. The general model includes multi-point summation, multi-point subtraction and multi-sample averaging. The analytic theory of (GMCI) unifies the theories of gated integration, phase-sensitive detection, multiple summations and averaging. In Chapter 3, a version of GMCI–a switched capacitor integrator (SCI)–is proposed to fulfill the function of GMCI. Chapter 4 deals with the design issue of SCI. Experimental results are presented in Chapter 5. Extremely weak signal 5 orders less than background is measured through multi-cycle integration. Conclusions, including proposed further work are discussed in Chapter 6.

CHAPTER 2

THEORY OF GATED MUTI- CYCLE INTEGRATION (GMCI)

2.1 Introduction

The signal or imaging source may be modulated or unmodulated. When an unmodulated source is measured, the signal must compete with the total low-frequency noise sources. However, when the source is modulated, the signal may be measured at the modulation frequency, far away from those large noise sources. Thus, the ratio of signal to noise (S/N) can be greatly improved by using modulated sources.

The lock-in amplifier [34-36], invented by Dicke [34] in 1946, is a powerful technique for the recovery of modulated weak signal, which may be swamped by the interference of noise that is much larger than the signal of interest. The invention of the lock-in amplifier has had a huge impact in modern science and technology. The core of lock-in amplification is the concept of phase sensitive synchronous detection or phase sensitive detection (PSD).

In order to recover the modulated signal, a demodulator must be used in the measurement system. The demodulator recovers the modulated signal and suppresses background and interference. In the case of the lock-in, the demodulator opens half window for signal and half window for background subtraction.

The repetitive signal, however, may appear briefly during each cycle, as in the measurement of the spin-lattice relaxation time (T_1) in nuclear magnetic resonance imaging (MRI) [37]. The boxcar averaging [37-40], also called gated integration (GI), is employed to deal with the recovery of repetitive signal with low cycle duty. A typical

application of boxcar integration is the measurement of fluorescence induced by laser pulses. It becomes a powerful tool in the research fields of biology, biophysics, biochemistry and biomedicine.

Photon counting [41] is another technique used to record very low signal intensities with very high sensitivity and a large dynamic range. It can detect a single incident photon or particle with energy not less than visible light by using a high-gain photo-multiplier tube (PMT) and a discriminator. The discriminator is used to reject most low-level noise by setting a threshold.

However, the lock-in amplifier, gated integrator and photon counting are developed for a single detector. Modulated images have never been directly taken by solid-state camera so far. It is virtually impossible to put the quite sophisticated lock-in amplifier, boxcar averaging, or photon counting circuitry into a pitch of around 50×50 μm^2.

In practice, the need for taking the modulated or repetitive image is becoming urgent in the fields of biotechnology. The well-developed FPA is hardly involved due to its single-cycle integration. With the advanced microelectronic technologies in hand, it is time to develop gated multi-cycle integrator for signal modulated FPAs.

By introducing a general model of gated multi-cycle integration (GMCI), a concept containing PSD and GI, the theory of GMCI will be developed specifically for FPA dealing with pulsed or modulated image sources in this chapter. Before this is done, a brief review of the lock-in and the gated boxcar-averaging techniques of measuring modulated signals is given for the purpose of a better understanding GMCI technology.

In the next chapter, a simple switched capacitor integrator circuit, which can be operated in modes of PSD and GI, will be employed to fulfill the functions of GMCI.

2.2 Basic Concepts of Lock-in Amplifier

A lock-in amplifier uses phase-sensitive detection to improve the signal-to-noise ratio. The analytical signal to be measured is modulated at some reference frequency. The lock-in-amplifier then amplifies only the component of the input signal at the reference frequency, and filters out all other frequencies, i.e., noise.

The diagram of a basic lock-in amplifier is shown in Fig. 2.1. The basic requirements for look-in amplifier are the pre-amplifier followed by a band-pass filter, then the phase sensitive detector. A pre-amplifier is necessary to bring the small signal to a level sufficient to overcome the noise induced by the amplifier, band-pass filter and PSD. The band-pass filter rejects unnecessary noise and interference from higher odd harmonics of reference frequency.

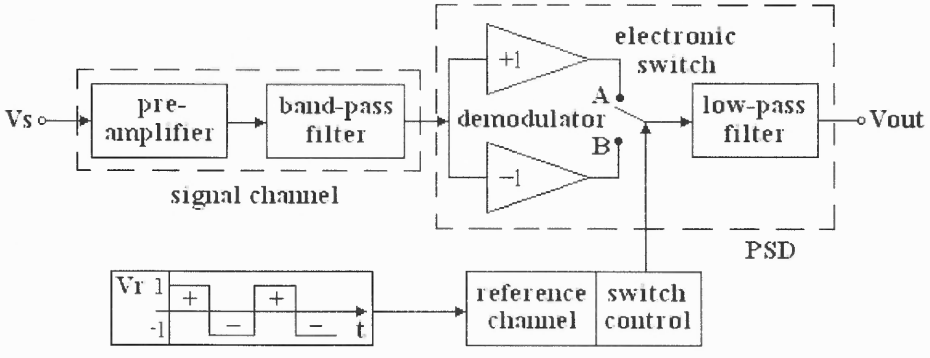


Figure 2.1 Block diagram of a basic lock-in amplifier

The main components of PSD are the demodulator and the low pass filter as shown in Fig. 2.1. The key to the operation of the demodulator is the two-state switch,

which is controlled electronically from a reference voltage. The switch changes position between points A and B as the reference changes polarity. This action gives a systematic change of gain between +1 and -1 in the signal path, resulting in demodulation of the signal at the reference frequency to a DC component. The low pass filter recovers the dc component. The PSD passes only the signal at the reference frequency if all the higher harmonic frequencies are filtered before they go through it.

An intuitive way to understand the operation of lock-in amplifier can be found in reference [36]. Here the mathematical language is presented to describe the system. Assume that the frequency-response functions for the pre-amplifier plus band-pass filter and low-pass filter are $H_P(j\omega)$ and $H_L(j\omega)$, respectively. From symmetry $H_P(j\omega)= H_P(-j\omega)$, and $H_L(j\omega)= H_L(-j\omega)$. The reference angular frequency is ω_r. Moreover, consider the reference waveform with equal time in its two phases. By using Fourier series representation, the functioning of the demodulator can be expressed by:

$$V_r(t) = \frac{2}{\pi j}\sum_{k=-\infty}^{\infty}\frac{1}{2k+1}e^{j(2k+1)\omega_r t} \tag{2.1}$$

Now if the input signal is

$$V_i(t) = e^{j\omega t} \tag{2.2}$$

Then, the voltage at the output of the band-pass filter can be written as

$$V_{po}(t) = H_p(j\omega)e^{j\omega t} \tag{2.3}$$

Therefore, the voltage input at the low-pass filter is

$$V_{Li}(t) = \frac{2}{\pi j}H_P(j\omega)\sum_{k=-\infty}^{\infty}\frac{1}{2k+1}e^{j[(2k+1)\omega_r+\omega]t} \tag{2.4}$$

The Fourier transform of $V_{Li}(t)$ is found by

$$F_{Li}(j\varpi) = \frac{2}{\pi j} H_P(j\omega) \sum_{k=-\infty}^{\infty} \frac{1}{2k+1} \delta[\varpi - \omega - (2k+1)\omega_r] \tag{2.5}$$

The Fourier transform at output is

$$F_{Lo}(j\varpi) = \frac{2}{\pi j} H_P(j\omega) \sum_{k=-\infty}^{\infty} \frac{1}{2k+1} \delta[\varpi - \omega - (2k+1)\omega_r] H_L(j\varpi) \tag{2.6}$$

The output voltage of the lock-in is obtained by the inverse Fourier transform of (2.6)

$$v_o(t) = \frac{2}{\pi j} H_P(j\omega) \left\{ \sum_{k=-\infty}^{\infty} \frac{1}{2k+1} H_L\{j[\omega + (2k+1)\omega_r]\} e^{j(2k+1)\omega_r t} \right\} e^{j\omega t} \tag{2.7}$$

In this thesis, a base gain function of a system is defined by its output corresponding to the base input of $e^{j\omega t}$. A base gain function differs from a transfer function by that it is a function of both frequency and time in general case. Hence, the base gain function of the lock-in is

$$G_{Lock-in}(j\omega, t) = H_P(j\omega) \left\{ \frac{2}{\pi j} \sum_{k=-\infty}^{\infty} \frac{1}{2k+1} H_L\{j[\omega + (2k+1)\omega_r]\} e^{j(2k+1)\omega_r t} \right\} e^{j\omega t} \tag{2.8}$$

Obviously, the base gain function of the PSD is in the form of

$$G_{PSD}(j\omega, t) = \frac{2}{\pi j} \sum_{k=-\infty}^{\infty} \frac{1}{2k+1} H_L\{j[\omega + (2k+1)\omega_r]\} e^{j[(2k+1)\omega_r + \omega]t} \tag{2.9}$$

Now, for any input $V_{in}(t)$, the output will be given by

$$V_o(t) = \int_{-\infty}^{\infty} F_{in}(j\omega) G_{Lock-in}(j\omega, t) d\omega \tag{2.10}$$

where, $F_{in}(\omega)$ is the Fourier transform of $V_{in}(t)$, which is given by

$$F_{in}(j\omega) = \frac{1}{2\pi} \int_{-\infty}^{\infty} V_{in}(t) e^{-j\omega t} dt \tag{2.11}$$

A typical example of input is

$$V_{in}(t) = \sin(\omega_r t + \varphi) \tag{2.12}$$

From (2.11), (2.10) and (2.8), it can be found

$$F_{in}^{*}(j\omega)=\frac{1}{2j}[(\delta(\omega-\omega_r)e^{j\varphi}-\delta(\omega+\omega_r)e^{-j\varphi}] \tag{2.13}$$

$$V_{o,\sin}^{Lock-in}(t)=\frac{2}{\pi}\left|H_p(j\omega_r,t)\right|\left|H_L(0)\right|\cos(\varphi) \tag{2.14}$$

For a lock-in system, the equivalent bandwidth is determined by the bandwidth of the low-pass filter, which usually is much narrower than ω_r. Therefore, the following approximation is always satisfied

$$\left|H_L\{j[\omega+(2k+1)\omega_r]\}\right|\left|H_L\{j[\omega+(2k'+1)\omega_r]\}\right|\approx 0 \quad if \quad k\neq k' \tag{2.15}$$

In this thesis, the transmission windows or the transmission function of a system is defined by $\sqrt{G_x G_x^{*}}$. For the lock-in system and the PSD, they are given by

$$T_{PSD}(\omega)=\sum_{k'=0}^{\infty}\frac{2}{(2k'+1)\pi}\left|H_L\{j[\omega-(2k'+1)\omega_r]\}\right| \tag{2.16}$$

$$T_{Lock-in}(\omega)=\sum_{k'=0}^{\infty}\frac{2}{(2k'+1)\pi}\left|H_L\{j[\omega-(2k'+1)\omega_r]\}\right|\left|H_P(j\omega)\right| \tag{2.17}$$

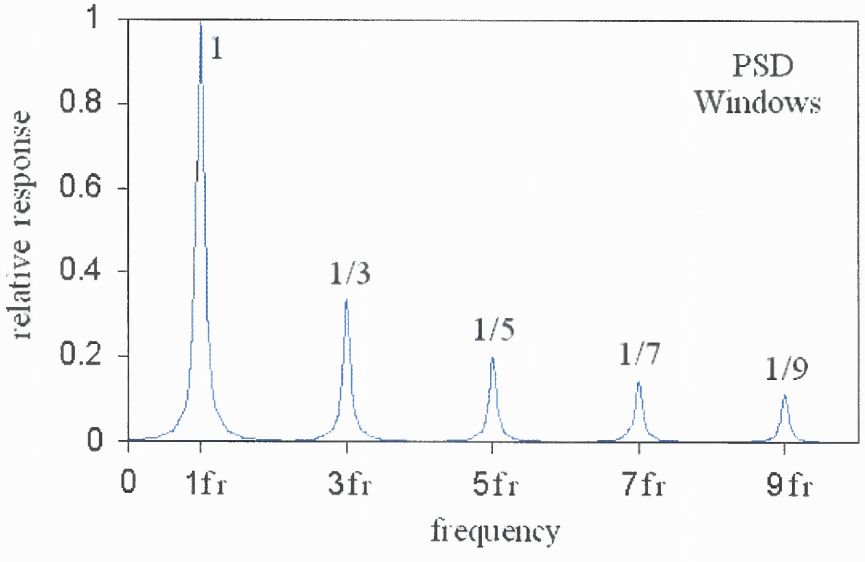


Figure 2.2 Transmission windows of a switching PSD

Figures 2.2 and 2.3 depict these windows. Obviously, PSD is not only sensitive to the signal at the reference frequency, but is also susceptible to interference from higher odd harmonic frequencies. For this reason, the band-pass filter is put before the PSD in order to suppress these windows.

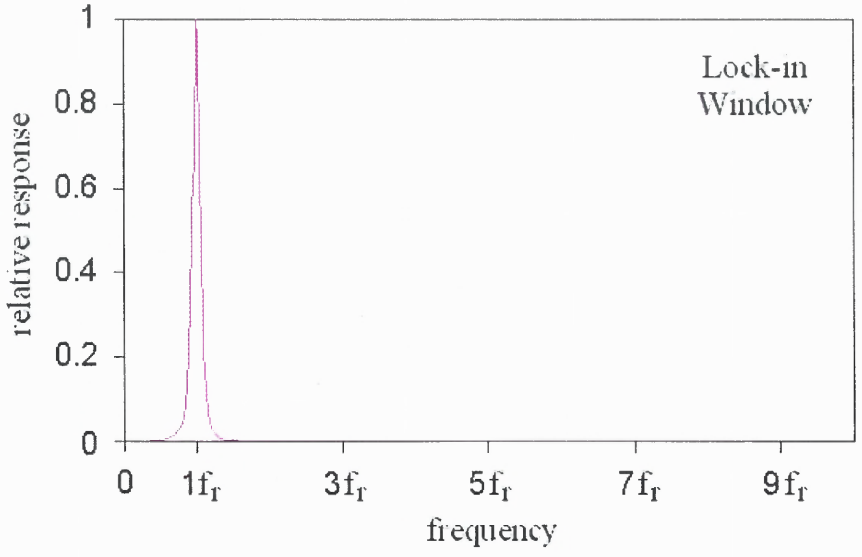


Figure 2.3 The transmission window of Lock-in

2.3 Gated Integration

A gated integrator or a boxcar averager is designed to recover fast, repetitive, analog signals with time scales ranging from 10^{-11} to 10^{-4} seconds. Fig. 2.4 shows a gated integrator with exponential averaging. In a typical application, a time window within a certain width is "gated" after a set delay from an internal or external trigger. A gated integrator amplifies and integrates the signal that is present during the time the gate is open, excluding noise and interference that may be present at other times. Shot by shot data from a gated integrator may be averaged by a boxcar to improve the SNR. Commercial boxcar averagers provide linear or exponential averaging. Since any signal

present while thee gate is open will add linearly, while noise will add in a "random walk" fashion as the square root of the number of shots, averaging *n* shots will improve the SNR by a factor of square root of *n*. A gated integrator is typically used in a boxcar pulsed laser instrument such as to measure laser-induced fluorescence.

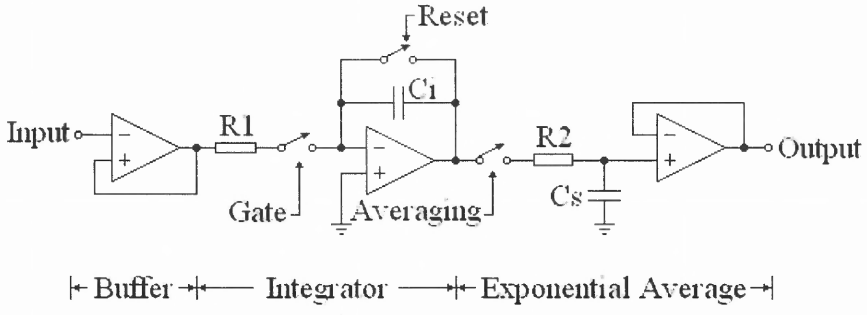


Figure 2.4 Schematic of a gated integrator

The gated integrator is actually a capacitive transimpedance amplifier (CTIA) except the gated switch, so it also performs as a low pass filter. Since the gated time is quite short, the signal must be significant for integration. The boxcar averager works as a sample/hold (S/H) circuit, but in a different mode. The main difference is the sampling times. The boxcar samples in a shot time which is much less than the time constant of the circuit, while, the sample time of a S/H circuit must be much larger than the time constant.

2.4 Theory of the Gated Multi-Cycle Integration

In order to deal with a weak repetitive image buried in strong background, the gated multi-cycle integration is proposed, which unifies the basic concepts of phase sensitive detection, gated integration, multiple summation and averaging. GMCI is a general model

of input integrator developed for multi-cycle integration focal plane array (MIFPA). In this thesis, the previous integrators are called single-cycle integrators employed for single-cycle integration focal plane array (SIFPA). The detail model and the theory of GMCI will be presented in this subsection.

2.4.1 General Model of GMCI

The basic concept of GMCI is to integrate signal as well as background when the image appears, to block or subtract the background when there is no image signal. Such procedures are executed numerous times for summation and averaging. Fig. 2.5 shows the block diagram of GMCI for one pixel.

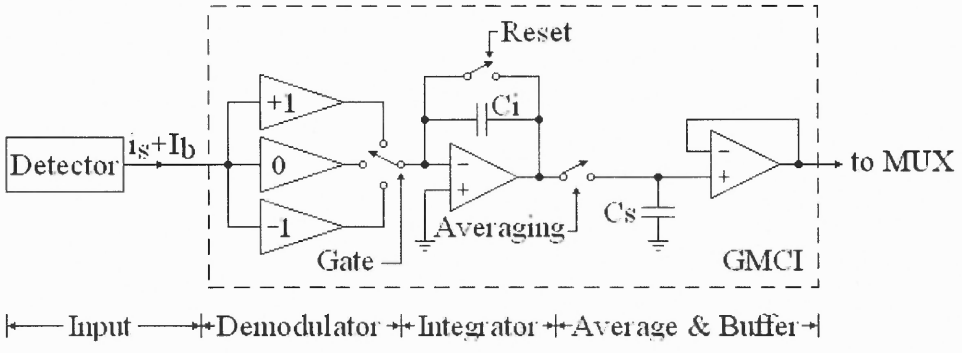


Figure 2.5 Block diagram of gated multi-cycle integration

The general operation is described as following. The total integration includes *n* sweeps with *n* samples for averaging. In each sweep there are *m* cycles of integration for summation. In every cycle of integration, the input signal and/or background may be either added or subtracted or blocked to the integrator according to a reference signal. In each cycle, the integration begins after some time delay t_d. The phase-sensitive gated switches, controlled by a reference channel, first guide the input current to discharge the

integrator within time interval of τ_1, followed by some dead time τ_2, then lead the input current to charge the integrator within time interval of τ_3, succeeded by another dead time τ_4 before the next cycle of integration. After a sweep, i.e., *m* cycles of integration, the output of the integrator is sampled out to a storage memory within time t_s, followed by resetting the integrator within time t_r, then, the integrator begins to integrate again. Such a sweep repeats *n* times so that the memory gets *n* samples for average in the purpose of improving signal-to-noise ratio. The averaging may be performed off-chip by using image-processing software. For GMCI the averaging is performed by either hardware or software, and therefore included in this discussion.

2.4.2 Demodulation Function and its Fourier Transform

In order to derive the transfer function of GMCI, first, it is needed to formulate the demodulation function, D(t)

$$D(t) = \sum_{j=1}^{n} D_j(t) \tag{2.18}$$

where $D_j(t)$ represents the demodulation function corresponding to the jth sweep of multi-cycle integration, which is depicted in Fig. 2.6.

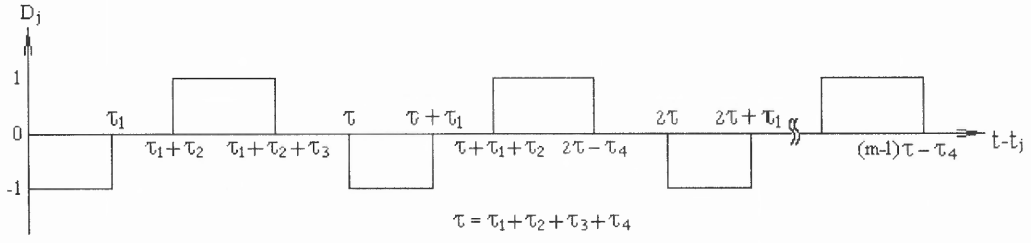


Figure 2.6 The jth demodulation function

According to the model and Fig. 2.6, the demodulation corresponding to jth swipe is

$$D_j(t)=\begin{cases} -1 & if\ \ (i\text{-}1)\tau < t - t_j \le (i-1)\tau + \tau_1 \\ 1 & if\ \ (i-1)\tau + \tau_1 + \tau_2 < t - t_j \le (i-1)\tau + \tau_1 + \tau_2 + \tau_3 \\ 0 & \text{otherwise} \end{cases} \quad \begin{matrix} i = 1,2,\cdots,m \\ j = 1,2,\cdots,n \end{matrix} \tag{2.19}$$

where τ is the period of the cycle of discharging and charging, and the delay time corresponding to the *jth* sweep, t_j is determined by

$$t_j = (j-1)T_p + t_d \tag{2.20}$$

Here, T_p denotes the total process time for one sweep, which is given by

$$T_p = m\tau + t_d + t_s + t_r \tag{2.21}$$

Let T_i denote the total integration time of a single sweep,

$$T_i = m(\tau_1 + \tau_3) \tag{2.22}$$

Let T and T^i denote the total process time, the total integration time of the n sweeps, respectively. They are easily found to be

$$T = nT_p \tag{2.23}$$

$$T^i = nT_i \tag{2.24}$$

The Fourier transform of the demodulation function is

$$\begin{aligned} F_D(j\omega) &= \frac{1}{2\pi}\int_{-\infty}^{\infty} D(t)e^{-j\omega t}dt \\ &= \frac{j}{2\pi\omega}\frac{\sin(\frac{m\omega\tau}{2})}{\sin(\frac{\omega\tau}{2})}\frac{\sin(\frac{n\omega T_p}{2})}{\sin(\frac{\omega T_p}{2})}e^{-j\omega[\frac{(m-1)\tau+(n-1)T_p}{2}+t_d]} \\ &\quad \times\left[1 + e^{-j\omega(\tau_1+\tau_2+\tau_3)} - e^{-j\omega\tau_1} - e^{-j\omega(\tau_1+\tau_2)}\right] \end{aligned} \tag{2.25}$$

2.4.3 General Output of GMCI

For any input $i_{in}(t)$, the general output of a normal average of n samples after time T is

$$V_o(T) = -\frac{1}{nC}\int_0^T i_{in}(t)D(t)dt = \int_{-\infty}^{\infty} F_{i_{in}}(j\omega)G_{GMCI}(j\omega)d\omega \tag{2.26}$$

where, linear average is taken, C is the capacitance of the integrator, a coefficient of transforming of voltage-to-current may be included if the initial signal is voltage. The Fourier transform of the input current is

$$F_{i_{in}}(j\omega) = \frac{1}{2\pi}\int_{-\infty}^{\infty} i_{in}(t)e^{-j\omega t}dt \tag{2.27}$$

Furthermore,

$$G_{GMCI}(j\omega) = -\frac{1}{nC}\int_0^T D(t)e^{j\omega t}dt = -\frac{2\pi}{nC}F_D(-j\omega) \tag{2.28}$$

is the base gain function of the gated multi-cycle integrator, which is the output of GMCI corresponding to the input of $e^{j\omega t}$. In equations of (2.26) and (2.28), the average of n linear samples is taken as the output. The average may be carried out by off-chip memory calculation without considering the accuracy of analog-to-digital converter (ADC). In above expression, the characteristics of D(t) is also used, in the time rang beyond [0,T], which is zero.

It is worth mentioning some outputs corresponding to special inputs. If the input current is a sinusoidal wave, that is, $i_{in} = \sin(\omega_o t + \varphi)$, then, the output will be

$$v_{o,\sin} = \frac{1}{2j}[e^{j\varphi}G_{GMCI}(j\omega_0) - e^{-j\varphi}G_{GMCI}(-j\omega_0)] \tag{2.29}$$

If the input is similar to the demodulate function with some time delay, that is, $i_{in} = i_0 D(t + t_0)$, then, the output will be

$$v_{o,D} = \frac{i_0}{nC}\int_0^T D(t)D(t + t_0)dt \tag{2.30}$$

Specially, if t_0=0, i.e., the input is in phase with reference signal, then the output will be

$$v_{o,D} = \frac{i_0 m}{C}(\tau_1 + \tau_3) = \frac{i_0 T_i}{C} \tag{2.31}$$

2.4.4 Base Gain Function of GMCI

According to equation (2.28), the base gain function of GMCI is derived by

$$\begin{aligned} G_{GMCI}(j\omega) &= -\frac{2\pi}{nC} F_D(-j\omega) \\ &= \frac{j}{n\omega C} \frac{\sin(\frac{m\omega\tau}{2})}{\sin(\frac{\omega\tau}{2})} \frac{\sin(\frac{n\omega T_p}{2})}{\sin(\frac{\omega T_p}{2})} e^{j\omega[\frac{(m-1)\tau+(n-1)T_p}{2}+t_d]} \left[1 + e^{j\omega(\tau_1+\tau_2+\tau_3)} - e^{j\omega\tau_1} - e^{j\omega(\tau_1+\tau_2)}\right] \\ &= e^{j\omega t_d} G_C(j\omega) H_S(j\omega) H_A(j\omega) \end{aligned} \tag{2.32}$$

where

$$G_C(j\omega) = \frac{j}{\omega C}[1 + e^{j\omega(\tau_1+\tau_2+\tau_3)} - e^{j\omega\tau_1} - e^{j\omega(\tau_1+\tau_2)}] \tag{2.33}$$

is the base gain function of a single cycle integration, including the two phases of adding input current to and subtracting input current from the integrator,

$$H_S(j\omega) = \frac{\sin(\frac{m\omega\tau}{2})}{\sin(\frac{\omega\tau}{2})} e^{j\omega\frac{(m-1)\tau}{2}} \tag{2.34}$$

is the transfer function of the multi-point summation, and

$$H_A(j\omega) = \frac{\sin(\frac{n\omega T_p}{2})}{n\sin(\frac{\omega T_p}{2})} e^{j\omega\frac{(n-1)T_p}{2}} \tag{2.35}$$

denotes to the averaging of n samples.

2.4.5 Transmission Window of GMCI

The transmission window, or the magnitude-response function, can be described by

$$T_{GMCI}(\omega) = \frac{1}{n\omega C}\left|\frac{\sin(\frac{m\omega\tau}{2})\sin(\frac{n\omega T_p}{2})}{\sin(\frac{\omega\tau}{2})\sin(\frac{\omega T_p}{2})}\right|\left|1 + e^{j\omega(\tau_1+\tau_2+\tau_3)} - e^{j\omega\tau_1} - e^{j\omega(\tau_1+\tau_2)}\right| \quad (2.36)$$
$$= T_C T_S T_A$$

where

$$T_C(\omega) = |G_C(j\omega)| = \frac{1}{\omega C}\left|1 + e^{j\omega(\tau_1+\tau_2+\tau_3)} - e^{j\omega\tau_1} - e^{j\omega(\tau_1+\tau_2)}\right|$$
$$= \frac{1}{\omega C}\{4 + 2\cos(\omega\tau_2) + 2\cos[\omega(\tau_1+\tau_2+\tau_3)] - 2\cos(\omega\tau_1) \quad (2.37)$$
$$- 2\cos(\omega\tau_3) - 2\cos[\omega(\tau_1+\tau_2)] - 2\cos[\omega(\tau_2+\tau_3)]\}^{1/2}$$

$$T_S(\omega) = |H_S(j\omega)| = \left|\frac{\sin(\frac{m\omega\tau}{2})}{\sin(\frac{\omega\tau}{2})}\right| \quad (2.38)$$

$$T_A(\omega) = |H_A(j\omega)| = \left|\frac{\sin(\frac{n\omega T_p}{2})}{n\sin(\frac{\omega T_p}{2})}\right| \quad (2.39)$$

are the transmission functions corresponding to a single cycle integration, m point summation and n sample averaging, respectively. Notice that $T_s(\omega)=m$ whenever $\omega\tau$ is an integral multiple of 2π. Fig. 2.7 shows the comb filter response of equations of (2.38) and (2.39) for several values of m and n.

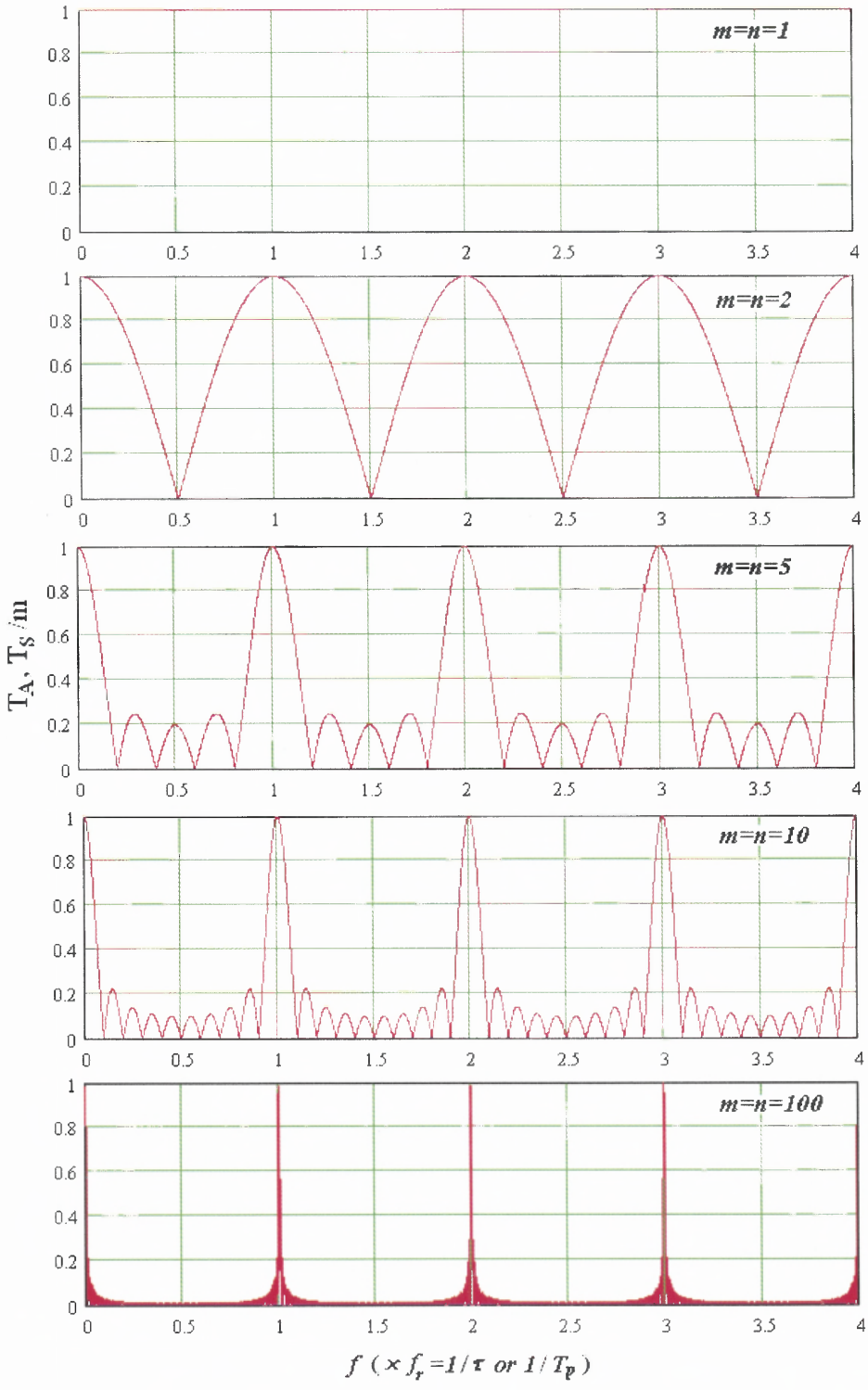


Figure 2.7 Transmission windows of multipoint summation or average

Note each band-pass response is centered at a harmonic (k/τ or k/T_p) of the sweep/trigger rate. Since the relative peak transmission of each band-pass response is 1, the –3dB points must occur at $1/\sqrt{2}$, so that

$$\frac{T_S(\omega)}{m} = \left|\frac{\sin(m\omega\tau/2)}{m\sin(\omega\tau/2)}\right| = \frac{1}{\sqrt{2}} \tag{2.40}$$

or

$$T_A(\omega) = \left|\frac{\sin(n\omega T_p/2)}{n\sin(\omega T_p/2)}\right| = \frac{1}{\sqrt{2}} \tag{2.41}$$

from which the –3dB bandwidth B for large values of m or n, is found to be

$$B_S = 0.886/(m\tau) \tag{2.42}$$

or

$$B_A = 0.886/(nT_p) \tag{2.43}$$

From the derivation of (2.36), it can be seen that the shape of the transmission windows is totally determined by the demodulation function (only a difference of a constant). It seems that these windows have nothing to do with the integrator. As a matter of fact, the demodulation function is defined within the total integrating time. It is this very total integrating time that determined the bandwidth of the GMCI. To see this, it is needed to find the power noise at the output. It will be discussed later on.

2.4.6 Average Signal under the Synchronized Integration

The purpose of demodulating integration is to recover the repetitive imaging by synchronized integration. The general input current is the sum of pure repetitive signal

induced current i_s, the background radiation induced current i_b, and the leakage current of detector i_d.

$$i_{in} = i_s + i_b + i_d \tag{2.44}$$

Let

$$I_b = i_b + i_d \tag{2.45}$$

For simplification without losing generality, the background related currents are consider as DC constants for a given detector and a background radiation in the rest of the derivation. The average of pure repetitive signal induced current is define as

$$i_p = \frac{1}{\tau_1 + \tau_3}\left| \int_{t_j+(i-1)\tau}^{t_j+(i-1)\tau+\tau_1} i_s(t)dt - \int_{t_j+(i-1)\tau+\tau_1+\tau_2}^{t_j+(i-1)\tau+\tau_1+\tau_2+\tau_3} i_s(t)dt \right| \quad \begin{matrix} i = 1,2,\cdots,m \\ j = 1,2,\cdots,n \end{matrix} \tag{2.46}$$

Noise associated average current due to pure signal radiation is

$$i_p^* = \frac{1}{\tau_1 + \tau_3}\left| \int_{t_j+(i-1)\tau}^{t_j+(i-1)\tau+\tau_1} |i_s(t)|dt + \int_{t_j+(i-1)\tau+\tau_1+\tau_2}^{t_j+(i-1)\tau+\tau_1+\tau_2+\tau_3} |i_s(t)|dt \right| \quad \begin{matrix} i = 1,2,\cdots,m \\ j = 1,2,\cdots,n \end{matrix} \tag{2.47}$$

Under synchronizing detection, i_p, i_p^* are independent of i and j. Furthermore, they are equal when the gates are in phase with the signal. Therefore, the signal at output is

$$v_s = \frac{i_p T_i^i}{nC} = \frac{i_p T_i}{C} \tag{2.48}$$

which is proportional to the total integration time of a sweep.

2.4.7 Power Noise and the Equivalent Bandwidth

If the readout noise caused by GMCI circuit can be ignored, then the output noise due to the input current can be found by

$$\overline{v_n^2} = \int_{-\infty}^{\infty} T_{GMCI}^2(2\pi f)\frac{w(f)}{2}df \tag{2.49}$$

Where

$$f = \frac{\omega}{2\pi} \tag{2.50}$$

is the linear frequency, w(f) the power density of current noise at the input of the demodulator. w(f) is usually defined in the frequency range of 0 to ∞. Here it is extended to negative infinite. In case of shot noise, it is a constant and is given by

$$w = 2e(i_p^* + I_b) \tag{2.51}$$

Here, e is the charge of an electron and (2.49) becomes

$$\overline{v_n^2} = \frac{m(\tau_1 + \tau_3)w}{2nC^2} = \frac{wT_i}{2nC^2} = w\left(\frac{1}{2T_i^i}\right)\left(\frac{T_i}{C}\right)^2 \tag{2.52}$$

The equivalence bandwidth of GMCI, converting to the input, is given by

$$B_{GMCI} = \frac{1}{2T^i} \tag{2.53}$$

which is only determined by the total integration time.

2.4.8 Signal-to-Noise Ratio

From equations of (2.48) and (2.52), the signal-to-noise ratio at output is found by

$$SNR_o = \frac{v_s}{\sqrt{\overline{v_n^2}}} = \frac{i_p}{\sqrt{w}}\sqrt{2T_i^i} = \frac{i_p}{\sqrt{2e(i_p^* + I_b)}}\sqrt{2T_i^i} \tag{2.54}$$

which is proportional to the square root of the total integration time. An important conclusion is that whatever technologies, either multi-cycle summation or multi-sample averaging, weather performed on chip or off chip, the purpose of the technologies is

same–to increase the total effective integration time, thereby, to improve the signal-to-noise ratio.

2.4.9 Maximum Integration Time

Maximum integration time is dependent on the storage capacity of the integrator as well as the magnitudes of signal and/or background related current. Let N_{sat} denote the maximum number of electrons the integrator can handle, which is determined by the capacitance of integrator and the saturation voltage of the circuit. The maximum integration time T_i is approximately determined by

$$eN_{sat} = i_p T_{i,\max} + m|\tau_1 - \tau_3| I_b = [i_p + (2\gamma - 1) I_b] T_{i,\max} \tag{2.55}$$

where

$$\gamma = \begin{cases} \delta & if\ \tau_1 \geq \tau_3 \\ 1 - \delta & if\ \tau_3 \geq \tau_1 \end{cases} \tag{2.56}$$

And

$$\delta = \frac{\tau_1}{\tau_1 + \tau_3} \tag{2.57}$$

From (2.55), the maximum integration time of one sweep is

$$T_{i,\max} = \frac{eN_{sat}}{i_p + (2\gamma - 1) I_b} \tag{2.58}$$

which is dependent on the ratio of background related current to the signal current and the ratio of gated lengths of the two phases; charge and discharge time of the integrator. Fig. 2.8 depicts the relationship of these variables. When δ=0 or 1, the integration time is minimum for a given current ratio. When δ=0.5, the maximum integration time goes to its maximum value corresponding to the whole storage well of the integrator being used

for signal integration. In order to keep at least half storage well for the signal, δ has to be held on a bandwidth of i_p/I_b at the center of 0.5. When the ratio of $I_b/\ i_p$ is large, this is quite a strict condition.

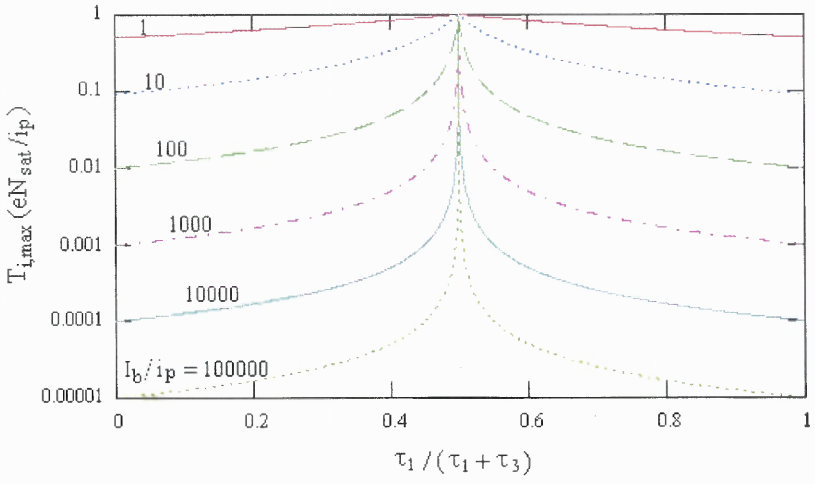


Figure 2.8 Maximum integration time versus the ratio of two window lengths of charging and discharging.

2.4.10 Maximum SNR_o and Dynamic Range

If the shot noise associated with background related current is dominant among whole noises, then the maximum signal-to-noise ratio $SNR_{o,max}$ can be found by substituting (2.58) into (2.54)

$$SNR_{o,\max} = \frac{i_p\sqrt{nN_{sat}}}{\sqrt{(i_p + I_b)[i_p + (2\gamma - 1)I_b]}} \tag{2.59}$$

In above equation, it is already assumed that the measurement is in phase with the signal. Therefore, the dynamic range is found by

$$DR = 20\log_{10} SNR_{o,\max} = 10\log_{10}\left\{\frac{ni_p^2 N_{sat}}{(i_p + I_b)[i_p + (2\gamma - 1)I_b]}\right\} \tag{2.60}$$

Equations of (2.57) and (2.58) are pictured in Fig. 2.9. The maximum SNR and DR occur when $\tau_1=\tau_2$.

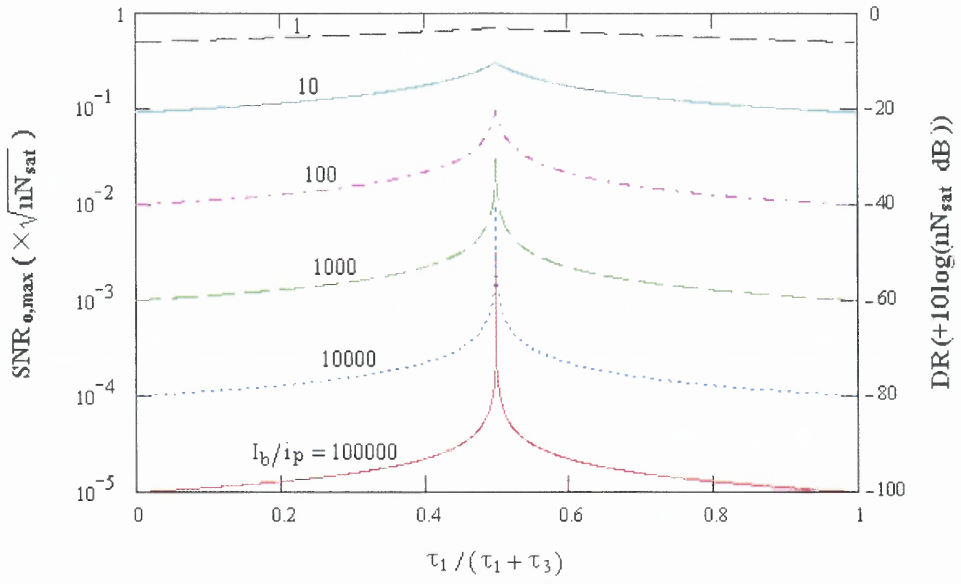


Figure 2.9 Maximum SNR and DR as a function of the ratio of two gated lengths of charging and discharging.

2.4.11 Optimum Sensitivity

Assume $SNR_{o,max}$=1. From (2.59), the minimum signal that can be measurable satisfies

$$i_{p,\min} = \frac{\gamma + \sqrt{\gamma^2 + (2\gamma - 1)(nN_{sat} - 1)}}{nN_{sat} - 1} I_b \tag{2.61}$$

Thus, the minimum photon flux that a pixel can detect is

$$\Phi_{\min} = \frac{i_{p,\min}}{e\eta A} = \frac{I_b}{e\eta A} \frac{\gamma + \sqrt{\gamma^2 + (2\gamma - 1)(nN_{sat} - 1)}}{nN_{sat} - 1} \tag{2.62}$$

where, η is the quantum efficiency, and A is the sensitive area of a detector. With the δ from 0 or 1 to 0.5, $i_{p,\min}$ decreases from the maximum value of $I_b / \sqrt{nN_{sat}}$ to the

minimum value of I_b / nN_{sat} .Fig 2.10 illustrates their relationship. Obviously, only when the two gates open exactly same length in time can the GMCI effectively suppress the background.

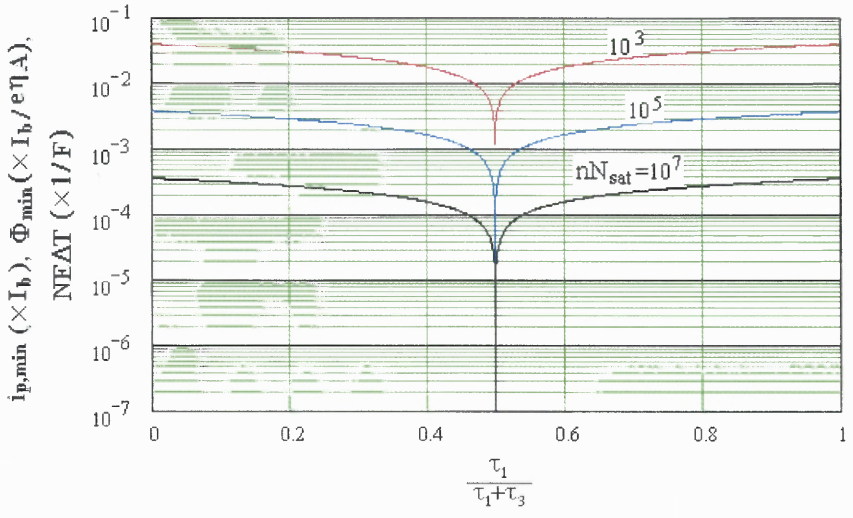


Figure 2.10 Background-limited optimum sensitivity vs. the ratio of two gated lengths of charge and discharge.

The noise equivalent temperature, *NEΔT*, representing the total output (or pixel) noise at a given background temperature converted into an equivalent temperature difference at the background scene, is a very effective figure of merit for a thermal imager. The noise equivalent temperature for an FPA is normally measured as:

$$NE\Delta T = \frac{N_{noise}}{\Delta N_b / \Delta T} = \frac{i_{p,\min}}{\frac{di_b}{dT}} = \frac{i_{p,\min}}{\frac{e\eta N_b}{N_b}\frac{dN_b}{dT}} = \frac{i_{p,\min}}{i_b \frac{1}{N_b}\frac{dN_b}{dT}} = \frac{\kappa}{\varepsilon}\frac{I_b}{i_b} \tag{2.63}$$

where

$$\kappa = \frac{i_{p,\min}}{I_b} = \frac{\gamma + \sqrt{\gamma^2 + (2\gamma - 1)(nN_{sat} - 1)}}{nN_{sat} - 1} \tag{2.64}$$

N_{noise} : the measured pixel noise in rms value of the number of electrons/pixel

$\Delta N_b/\Delta T$: the measured FPA's responsivity in electrons/pixel/K for a background signal N_b in electrons/pixel.

η : the quantum efficiency of the incident photons converted to electrons

N_b : the flux of photon collected by a pixel in photons/pixel/s

And the contrast ε is given by [42]

$$\varepsilon = \frac{1}{N_b}\frac{dN_b}{dT} \tag{2.65}$$

For thermal imaging of an FPA operating at background scene (that is $I_b=i_b$, a shot noise limited performance), the noise equivalence temperature can be expressed as

$$NE\Delta T_{\min} = \frac{\kappa}{\varepsilon} \tag{2.66}$$

Its relationship of gate rate to well capacity is also illustrated in Fig. 2.10. With the small window for the ratio of δ centered at 0.5 and the bandwidth around i_p/I_b, the noise equivalent temperature reduces dramatically inside this window.

Equations of (2.58) to (2.62) and (2.66) describe the optimized performance of GMCI. An obvious conclusion can be drawn about the performance of the average. That is, average operation is equivalently enhancing the limited capacity of the integrator by a factor of the number of samples.

The performance of the multi-point summation is not clear in these optimized equations. However, it is clear that by using multi-summation, it can be done to modify a single integration that is not optimized, to optimum multiple integrations. If the total integration time is extended by a factor of *m*, then from (2.54), the SNR will be increased by a factor of the square root of *m*.

The optimized performance takes two extreme values: δ=0 or 1 and δ=0.5. When δ=0 or 1, either τ_1 or τ_3 must be zero. There is no background subtraction. When δ=0.5, $\tau_1=\tau_3$, background is completely cancelled out in one single cycle. It is named the operation as a gated integration (GI) when there is no background subtraction, and a phase-sensitive integration (PSI) when the background is completely cancelled out.

2.4.12 Special Integration Modes

So far, the general performance of GMCI has been derived. There are several special cases according to the method of source signal modulation. They correspond to different operating modes of GMCI.

2.4.12.1 Gated Integration (GI) There is no background subtraction for gated integration. Either τ_3=0 or τ_1=0, and γ=1. Thus, from (2.36), the transmission window of GI is

$$T_{GI}(\omega)=\frac{2}{n\omega C}\cdot\left|\sin(\frac{\omega T_i}{2m})\frac{\sin(\frac{m\omega\tau}{2})}{\sin(\frac{\omega\tau}{2})}\frac{\sin(\frac{n\omega T_p}{2})}{\sin(\frac{\omega T_p}{2})}\right| \tag{2.67}$$

This is the transmission function of a single integration modulated by multi-summation and averaging. It takes its maximum value of T_i /C at ω=0. An ideal case for this expression is when all the dead, reset, and sample time approach zero, then a simple expression for the transmission function can be found

$$T_{GI}(\omega) = \frac{T_i}{C}\left|\frac{\sin(\frac{\omega T'}{2})}{\frac{\omega T'}{2}}\right| \tag{2.68}$$

which returns to a transmission window of the single integration, and is a sinc function performing as a low-pass filter as depicted in Fig. 2.11.

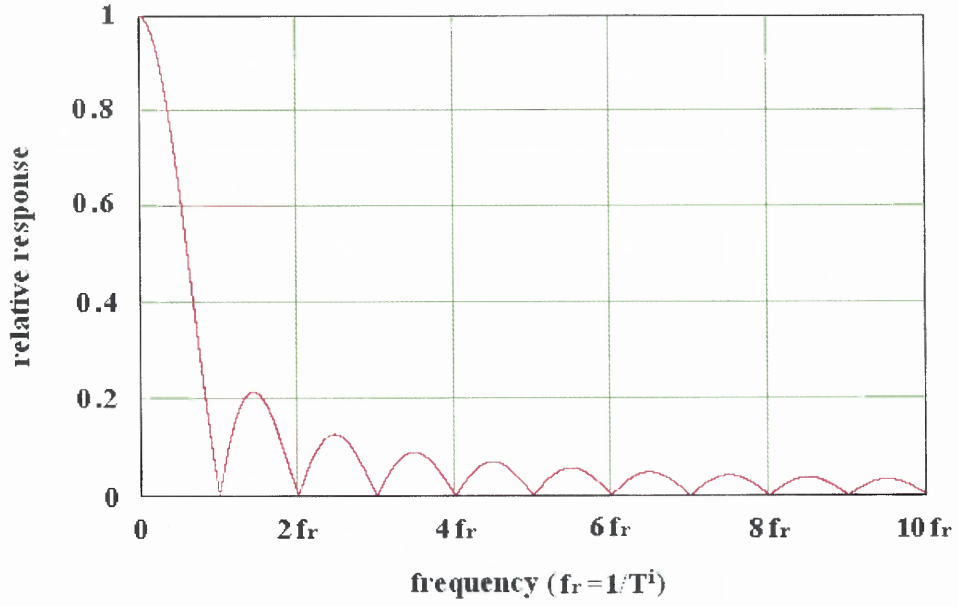


Figure 2.11 The transmission function of GI

Now from (2.58) to (2.59), it can be found

$$T_{GI}^{i,\max} = nT_{i,\max}^{GI} = \frac{enN_{sat}}{i_p + I_b} \tag{2.69}$$

$$SNR_{o,\max}^{GI} = \frac{i_p\sqrt{nN_{sat}}}{i_p + I_b} \tag{2.70}$$

$$DR^{GI} = 10\log_{10}\left[\frac{i_p^2 nN_{sat}}{(i_p + I_b)^2}\right] \tag{2.71}$$

$$i_{p,\min}^{GI} = \frac{I_b}{\sqrt{nN_{sat}}} \tag{2.72}$$

$$\Phi_{\min}^{GI} = \frac{I_b}{e\eta A\sqrt{nN_{sat}}} \tag{2.73}$$

$$NE\Delta T_{\min}^{GI} = \frac{1}{F\sqrt{nN_{sat}}} \tag{2.74}$$

The maximum integration time is inversely proportional to the total input current. When the background is much stronger than the signal, it is the background that limits the maximum integration time of a single cycle as well as the signal-to-noise ratio. Both the minima of detectable signal and the NEΔT are inversely proportional to the square root of the electron number that an integrator can handle during imaging. When m=n=1, equations of (2.68) to (2.74) describe the behavior of the capacitive transimpedance amplifier, which renders the best performance of conventional integrating methods for an FPA [29].

According to (2.29), the output due to an input of $i_0\sin(\omega_0 t+\varphi)$ will be

$$v_{o,\sin}^{GI} = \frac{i_o T_i}{C}\sin(\omega_o t_d + \varphi + \frac{\omega_o T^i}{2})\frac{\sin(\frac{\omega_o T^i}{2})}{\frac{\omega_o T^i}{2}} \tag{2.75}$$

The phase shift and the reduction of amplitude are obvious as in the same case of boxcar averager [38].

2.4.12.2 Phase Sensitive Integration (PSI) In this mode, τ_1=τ_3 and γ=0.5. The background is cancelled out for any two successive single integrations within one cycle. From (2.36), the transmission window of PSI is found

$$T_{PSI}(\omega)=\frac{4}{n\omega C}\left|\sin(\omega\frac{\tau_1+\tau_2}{2})\right|\left|\sin(\frac{\omega T_i}{4m})\frac{\sin(\frac{m\omega\tau}{2})}{\sin(\frac{\omega\tau}{2})}\frac{\sin(\frac{n\omega T_p}{2})}{\sin(\frac{\omega T_p}{2})}\right| \tag{2.76}$$

Compared to the case of GI, the transmission function of PSI is further modulated by a sine function. The importance of this modulation is that it shifts the maximum peak window from dc to ac and totally blocks any dc part. Again, it is worth considering the transmission function with background subtraction but without taking into account any delay, dead, reset and sample time. Therefore

$$T_p = T_i = m\tau = 2m\tau_1 = 2m\tau_3 \tag{2.78}$$

Equation (2.76) becomes

$$T_{PSI}(\omega)=\frac{T^i}{nC}\left|\frac{\sin(\frac{\omega T^i}{2})}{\frac{\omega T^i}{2}}\right|\left|\tan(\frac{\omega T^i}{4mn})\right| \tag{2.79}$$

The tangent function can be viewed as a modulation function due to background subtraction, which has a modulation frequency to be addressed by

$$f_m=\frac{mn}{T^i}=\frac{1}{\tau} \tag{2.80}$$

Figure 2.12 illustrates the transmission function with the same τ but different *mn*. The center of the main window peaks near the modulation frequency f_m, accompanied with satellite windows centered at the odd harmonics of f_m with reduced amplitude. These windows are similar to those of PSD shown in Fig 2.2. When *mn* and the time constant of the low-pass filter go to infinite, the windows of PSD and PSI tend to same discrete distribution. The similarity is due to similar switched demodulators being used in both cases. The difference is due to a finite processing time being used by the demodulation

function of the PSI while infinite processing time being employed by the demodulation function of PSD. With the same modulation frequency, the more the integration cycle number is, the longer the total integration time, rendering a narrower bandwidth.

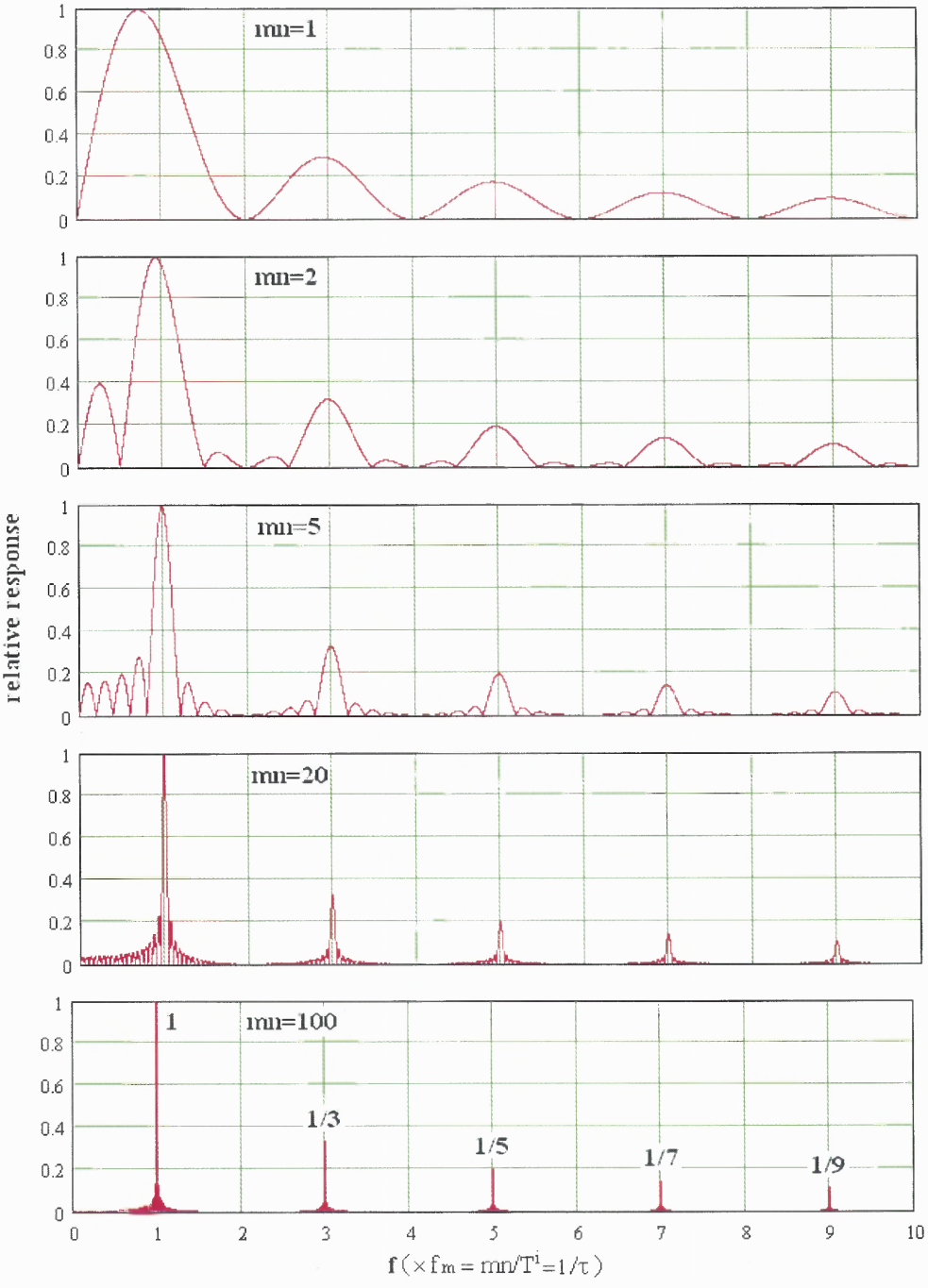


Figure 2.12 Transmission windows of PSI with different mn but same τ

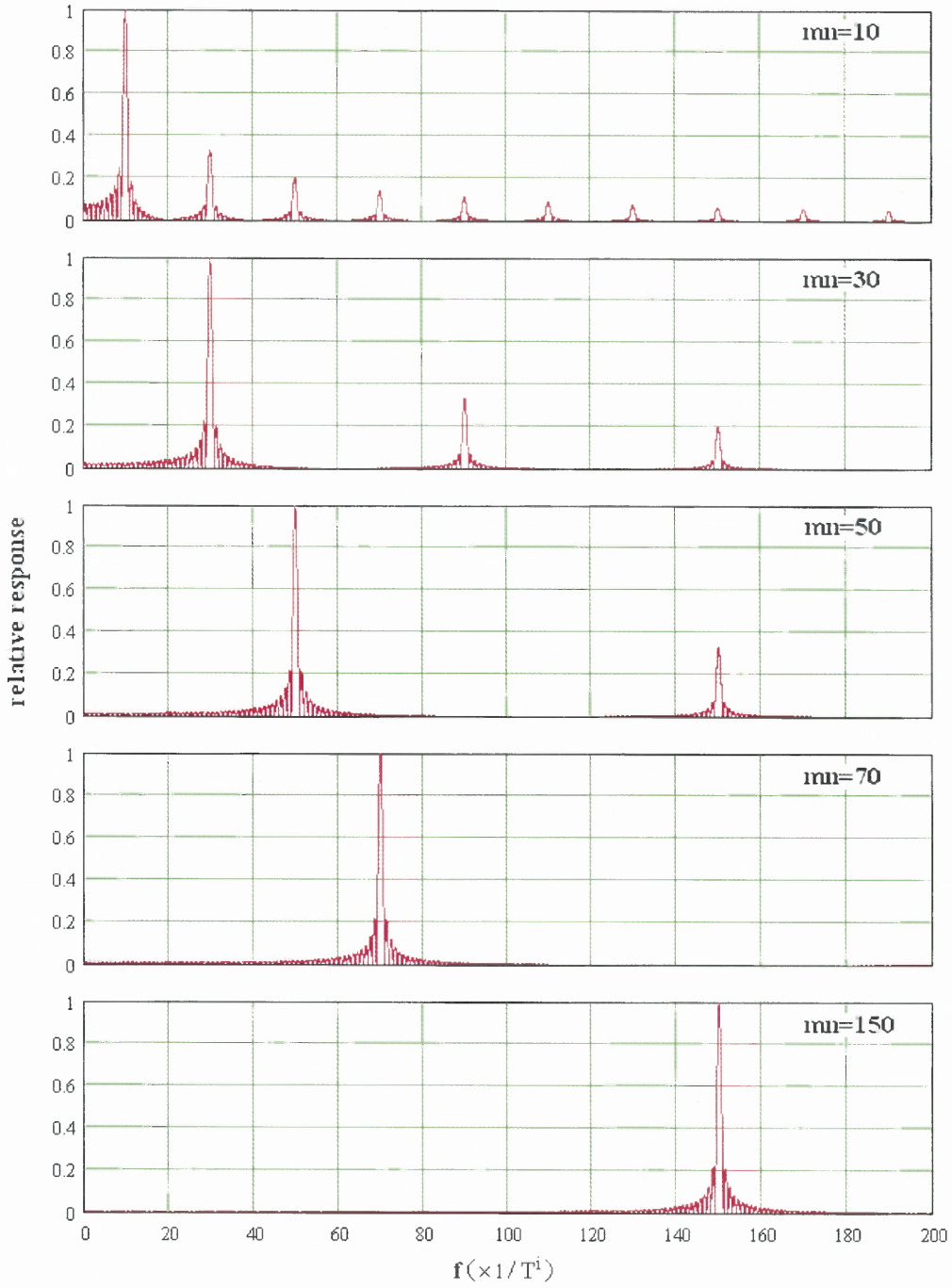


Figure 2.13 Transmission windows of PSI with different mn but same T^i

Figure 2.13 shows the transmission windows of PSI with same total integration time T^i but with different *mn*. While keeping the total integration time unchanged, the

more the cycle number, the higher the modulation frequency. However, the bandwidths do not change due to the total integration times being same.

For large *mn* (>5), the maximums of the transmission function of the PSI occur at the harmonic modulation frequency with magnitude determined by

$$T_{PSI}[(2k+1)f_m] = \frac{0.637T'}{(2k+1)nC} \qquad \text{k} = 0,1,2,\cdots \tag{2.81}$$

The -3dB bandwidth B for each band-pass is determined by the bandwidth of the transmission windows of summation and average. Therefore, B is given by

$$B = 0.886/(mn\tau) = 0.886/T' \tag{2.82}$$

With background subtraction plus multi-sample averaging, the total integration time could be quite long. Thus, it narrows the transmission window and improves the SNR. However, the bandwidth of PSI is still determined by (2.56).

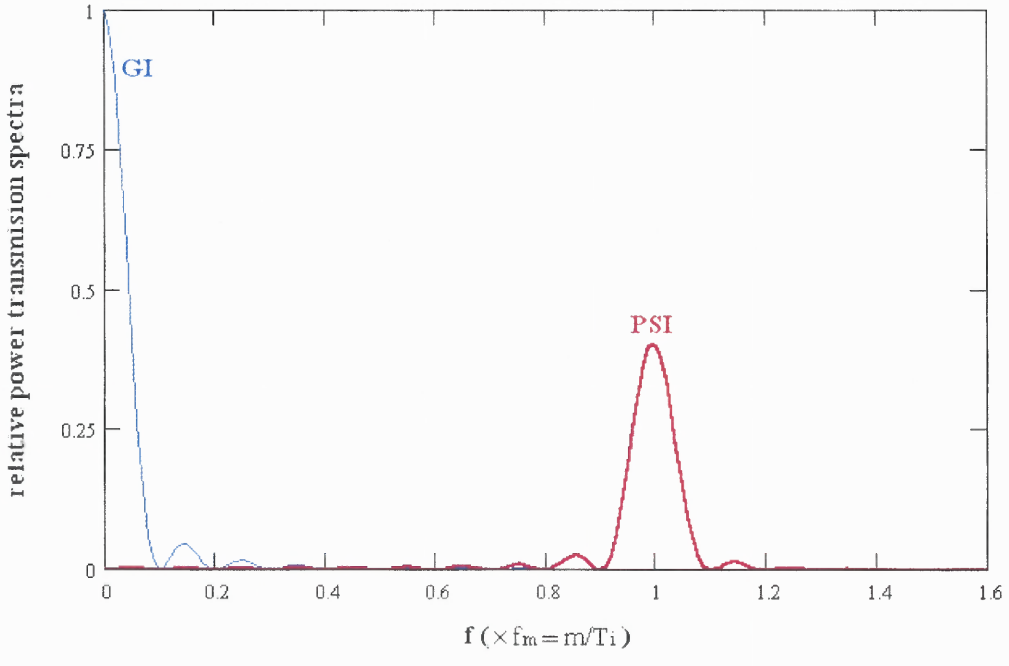


Figure 2.14 Comparison of power transmission windows of PSI and GI

A significant feature of the transmission function of the PSI, as shown in Fig. 2.12, is its capability of attenuating the low frequency noise. Fig. 2.14 emphasizes this point by comparing the power transmission spectra of PSI and GI with same integration time

Given $\tau_1=\tau_3$, from equations of (2.58) to (2.62) and (2.66), it can be found

$$T_{PSI}^{i,\max} = nT_{i,\max}^{PSI} = \frac{enN_{sat}}{i_p} \tag{2.83}$$

$$SNR_{o,\max}^{PSI} = \sqrt{\frac{i_p nN_{sat}}{i_p + I_b}} \tag{2.84}$$

$$DR^{PSI} = 10\log_{10}\left(\frac{i_p nN_{sat}}{i_p + I_b}\right) \tag{2.85}$$

$$i_{p,\min}^{PSI} = \frac{I_b}{nN_{sat}} \tag{2.86}$$

$$\Phi_{\min}^{PSI} = \frac{I_b}{e\eta AnN_{sat}} \tag{2.87}$$

$$NE\Delta T_{\min}^{PSI} = \frac{1}{\varepsilon nN_{sat}} \tag{2.88}$$

The storage well of a pixel could almost be saved for signal integration under the condition of the background being totally subtracted. Fig. 2.15 illustrates the difference between (2.83) and (2.69). Clearly, without background subtraction, the strong background mostly limits the integration time.

With background subtraction, the maximum SNR, so as the dynamic ranges, is improved due to the increased integration time. The increased SNR will, in turn, improve the minimum detectable signal induced current so as the sensitivity of an FPA. Figures 2.16 and 2.17 illustrate these improvements.

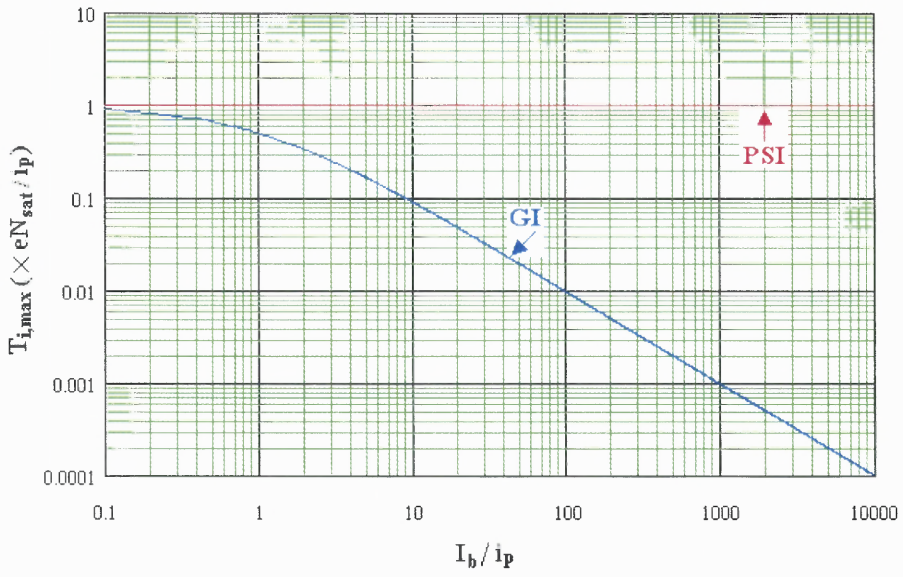


Figure 2.15 Maximum integration times with and without background subtraction

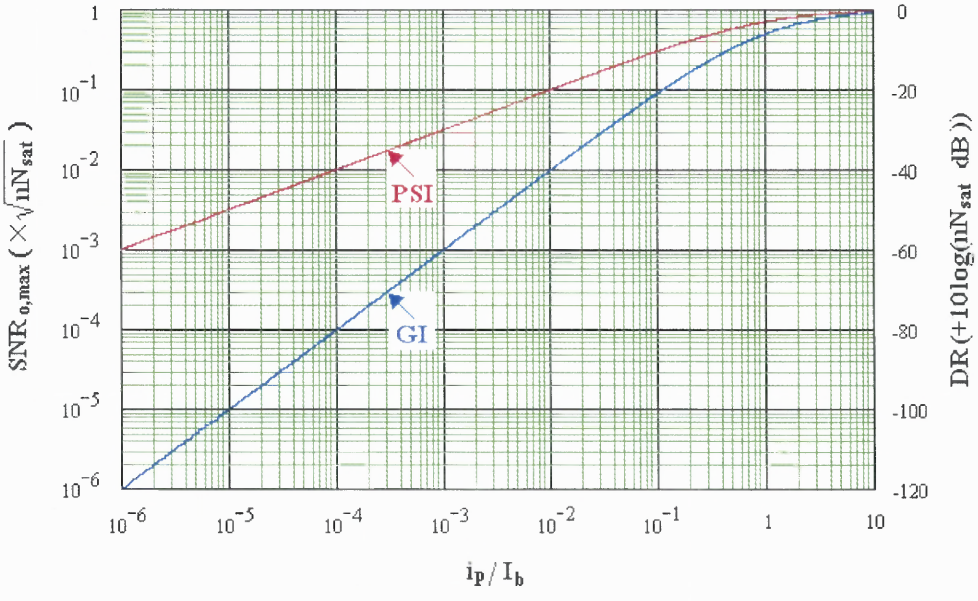


Figure 2.16 Maximum SNRs and DRs in cases of PSI and GI

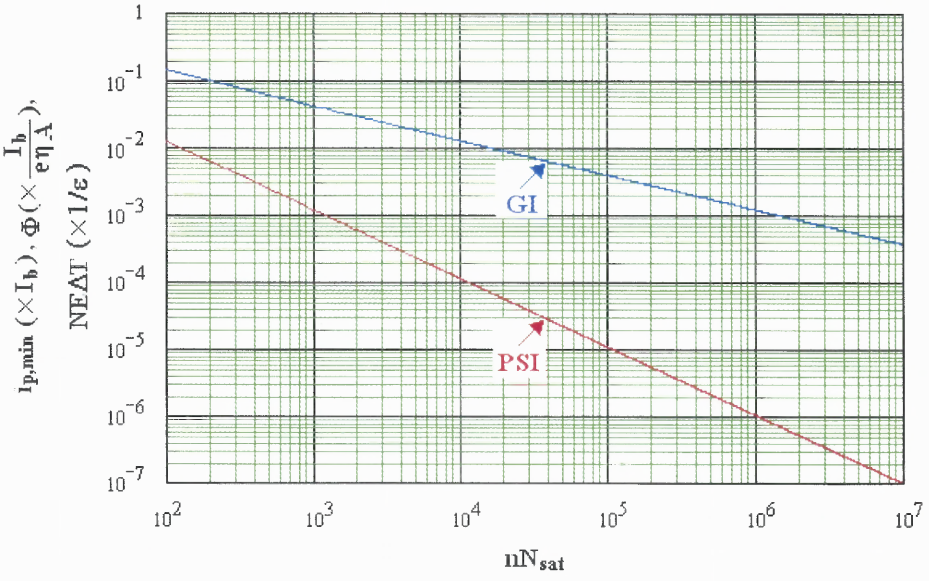


Figure 17 Sensitivities as a function of storage capacity in cases of GI and PSI

If the signal current i_s is integrated in one phase and blocked in another phase, according to (2.46), the average signal induced current i_p in (2.83) to (2.85) is need to be replaced with half i_s, and the sensitivities of (2.86) to (2.88) will be multiplied by 2.

$$T_{PSI^*}^{i,\max} = nT_{i,\max}^{PSI^*} = \frac{2enN_{sat}}{i_s} \tag{2.89}$$

$$SNR_{o,\max}^{PSI^*} = \sqrt{\frac{i_s nN_{sat}}{i_s + 2I_b}} \tag{2.90}$$

$$DR^{PSI^*} = 10\log_{10}\left(\frac{i_s nN_{sat}}{i_s + 2I_b}\right) \tag{2.91}$$

$$i_{p,\min}^{PSI^*} = \frac{2I_b}{nN_{sat}} \tag{2.92}$$

$$\Phi_{\min}^{PSI^*} = \frac{2I_b}{e\eta AnN_{sat}} \tag{2.93}$$

$$NE\Delta T_{\min}^{PSI^*} = \frac{2}{\varepsilon n N_{sat}} \tag{2.94}$$

In order to get expected performance of PSI, the two pulse widths associated with charge and discharge of the integrator must be stringently equal. The difference of these widths must be within the range of the ratio of the signal current to background current. Besides the pulse widths, the gap between these two pulses should be as small as possible in order to make sure that the main transmission window is centered at the modulation frequency and also to avoid unnecessary additional transmission windows.

Comparing to GI without background subtraction, improvement of the performance of PSI is clearly illustrated by the following equations

$$\frac{T_{i,\max}^{PSI}}{T_{i,\max}^{GI}} = \frac{i_p + I_b}{i_p} \tag{2.95}$$

$$\frac{SNR_{o,\max}^{PSI}}{SNR_{o,\max}^{GI}} = \sqrt{\frac{i_p + I_b}{i_p}} \tag{2.96}$$

$$DR^{PSI} - DR^{GI} = 10\log_{10}\left(\frac{i_p + I_b}{i_p}\right) \tag{2.97}$$

$$\frac{i_{p,\min}^{PSI}}{i_{p,\min}^{GI}} = \frac{1}{\sqrt{nN_{sat}}} \tag{2.98}$$

$$\frac{\Phi_{\min}^{PSI}}{\Phi_{\min}^{GI}} = \frac{1}{\sqrt{nN_{sat}}} \tag{2.99}$$

$$\frac{NE\Delta T_{\min}^{PSI}}{NE\Delta T_{\min}^{GI}} \frac{1}{\sqrt{nN_{sat}}} \tag{2.100}$$

Equations of (2.95) to (2.97) indicate that PSI is especially efficient when signal is much less than background. These comparisons are graphed at Fig. 2.18

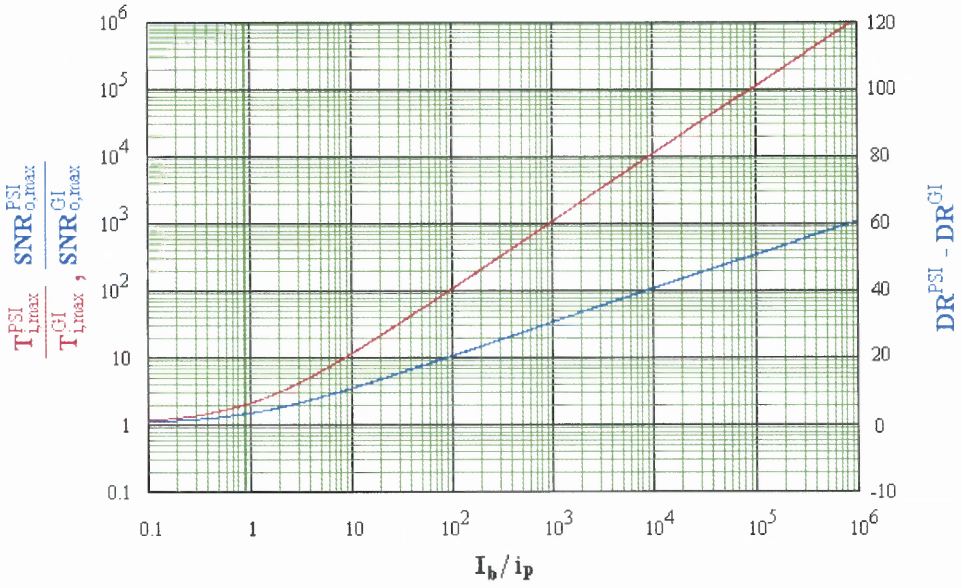


Figure 2.18 Comparisons of the maximum integration time and dynamic range with and without DC subtraction as a function of the current ratio of background over signal

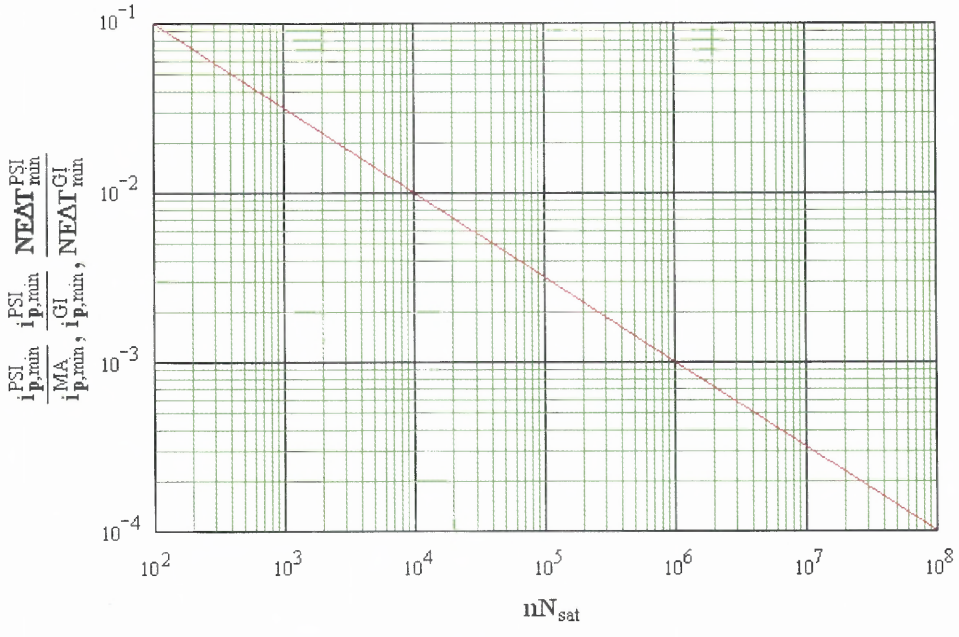


Figure 2.19 Comparison of sensitivities with and without dc subtraction

With background subtraction, the most significant improvement is the sensitivity of the FPA as shown by (2.98) to (2.100). The improvement is a factor of the square root of the total electron number an integrator can handle during imaging. These comparisons are graphed at Fig. 2.19.

The mode with background subtraction is called as the phase-sensitive integration due to the fact that the concepts of the PSI and PSD are similar. They not only have similar transmission windows, but also share similar phase relationships in terms of the output corresponding to the input of $i_0 \sin(\omega_m t + \varphi)$. From (2.29), combined with the conditions of the PSI and assuming t_d=0, the output will be

$$v_{o,\sin}^{PSI} = \frac{2i_0 T_i}{\pi C} \cos(\varphi) \tag{2.101}$$

The same phase relationship of PSD can be found in reference [36].

2.4.12.3 Mode List The operation modes of GMCI have been discussed with and without background subtraction. A complete list of its operation modes is the following:

(1) Single Integration (SI), which is equivalent to CTIA.

(2) Gated Integration with Multi-Point Summation (MGI).

(3) Gated Integration with Multi-Sample Averaging (AGI), which is gated integration boxcar averaging.

(4) Gated Integration with background subtraction (BSGI). This is a special case of PSI. There exists significant dead time between two cycles.

(5) Gated Integration with Multi-Point Summation and Multi-Sample Averaging (MAGI).

(6) BSGI with averaging (ABSGI).

(7) Phase-Sensitive detection (PSD). This is a special case of PSI. There is no significant dead time between two cycles.

(8) Phase-Sensitive Detection With Multi-Sample Averaging (APSD).

2.5. Summation

In this chapter, the model and the theory of gated multi-cycle integration have been successfully developed. The analytic theory unifies the concepts of gated integration, phase-sensitive detection, multi-point summation, and multi-sample averaging. GMCI is specifically developed for pulse or repetitive imaging of FPA with capability of picking extremely weak images buried in strong backgrounds.

CHAPTER 3

A SWITCHED-CAPACITOR INTEGRATOR (SCI); ONE VERSION OF GMCI

3.1 Introduction

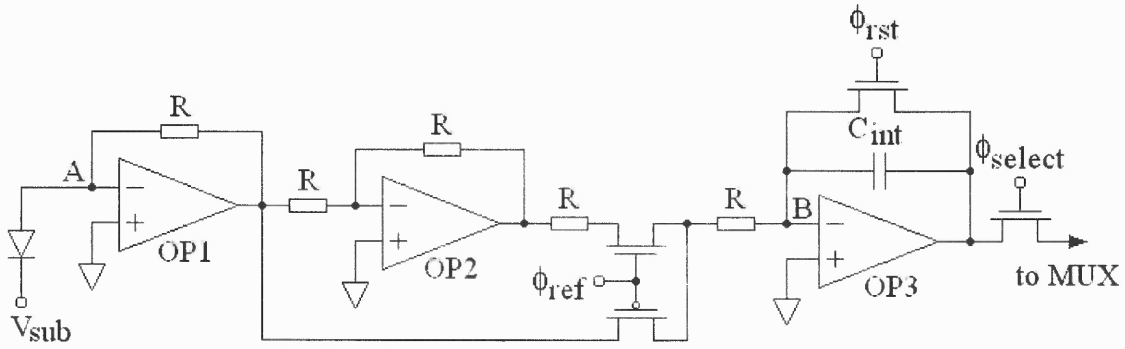
As mentioned in Chapter2, multi-cycle integration focal plane array (MIFPA) is a special FPA dealing with recovering modulated weak image signal from broadband noisy background. Like all the conventional readout circuits of FPAs, a readout circuit of a MIFPA must have the function of integrating of currents from detectors. Besides, it also should have the performance of demodulating the modulated signals as pointed out in Chapter 2. These two functions determine that the readout circuit of MIFPA is usually more complex than conventional readout circuits. Fortunately, modern microelectronic technologies have scaled down the dimensions of devices nearly to their physics limits. Feature size of 0.1 μm was already executed in industry. Therefore, the design and fabrication of relatively more complicated circuits to perform more functions of signal readout are feasible.

In previous chapter, the general model of the readout circuit for MIFPA was developed, which is the gated multi-cycle integrator (GMCI). In this chapter, a version of GMCI, a switched-capacitor integrator (SCI) is presented. The SCI is still a simple circuit, yet it may perform all the modes described in Chapter 3 except the averaging. That is, it may run either as a single integration (CTIA), or a gated integration with multi-point summation (MGI), or a gated integration with background-subtraction (BSGI) or a phase sensitive detection (PSD).

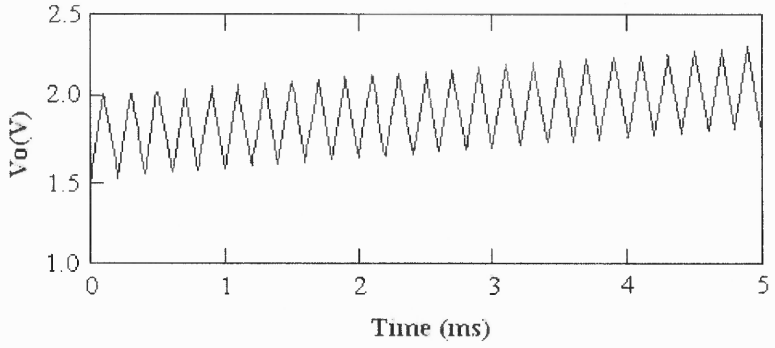
3.2 Circuitries of GMCI

Most lock-in amplifiers deal with voltage signals. Most solid-state cameras deal with current signals. An easy way to design the demodulator of current is to convert current to voltage, followed by a demodulator of voltage as depicted in Fig. 3.1. In this schematic diagram, the circuitry between node A and B is a demodulator. The first operational amplifier is used to convert the input current to voltage, and the second operational amplifier is a voltage inverter. In order to convert the small input current to a measurable voltage, the trans-resistor R must be large enough. By using two MOS switches controlled by the reference signal, either the voltage or the inverted voltage is selected as the input of the third operational amplifier, which also serves as the multi-cycle integrator. The input resistor of this stage brings its input voltages back to currents, with opposite directions in any two successive phases. Hence, the background related current I_b or the DC part of the input current is cancelled out in each of two successive phases, while the signal current i_s, or the AC part with reference frequency, will be gradually integrated. If the two switches are controlled by two separated clocks, then, the circuit can also perform the function of blocking the input by disenable the two switches at same time.

The operational principle of the circuit is straightforward and can be easily understood. This was the original circuit proposed for this study. However, the three operational amplifiers and four high impedance resistors for each pixel take too much real estate of a FPA chip. It may be suitable for linear arrays, not for two-dimension arrays.



(a) Schematic diagram of a GMCI circuit



(b) Output voltage of the integrator

Figure 3.1 Schematic diagram of a GMCI circuit and its output

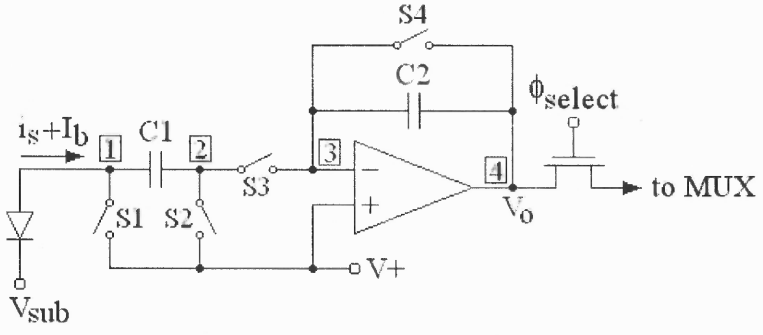


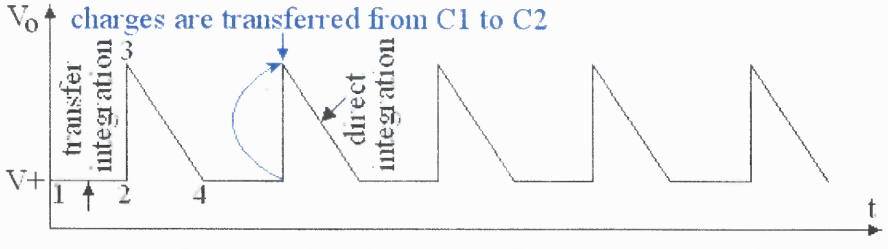
Figure 3.2 The switched-capacitor-gated integrator

An alternate way was later adopted to replace the previous circuit, which is a switched-capacitor integrator as shown in Fig. 3.2. In this circuit, C2 is the main integrator. S4 is the reset switch for the main integrator. C2, S4 and the operational

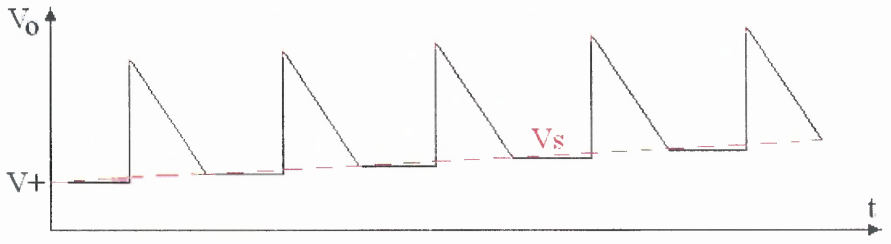
amplifier construct a CTIA integrator. C1 is a temporal integrator. S1, S2, and S3 are the gates of the integrators. S1, S2, S3, and C1 form the demodulator.

Generally, when switch S1 is on, the input current will be bypassed to the voltage source of V+ through S1. This fulfills the blocking function. When S1, S3 are off and S2 is on, the input current will be integrated on C1 first. At the end of this period of integration, the charges stored on C1 will be transferred to C2 by turning off S2 followed by turning on S1 and S3. Assume the input current flows into the integrator. the right terminal of C1 will collect negative charges during this integration. During the charge transfer, the input node 1 almost has a same voltage level as that of node 2. Hence, the negative charges stored on the right side of C1 must be transferred to the left side of C2, yielding a rise of the output voltage at node 4. This performs one phase of integration. This period of integration is named as transfer integration. When S1, S2 are off and S3 is on, the input current will be integrated directly on both C1 and C2. During this period of integration, positive charges are collected on the left side of C2 (nearly equivalent negative charges are collected on the right side of C1) if the input current is flows into the integrator, resulting in a fall of the output voltage at node 4. This completes the reverse integration. This period of integration is named as direct integration. Hence, direct integration performs the subtraction (or addition) of input charges from the main integrator if the transfer integration performs addition (or subtraction) of input charges to the main integrator. Thus, it explained that the proposed switched-capacitor integrator can perform the main functions of GMCI; that is, it can block or integrate or integrate reversely the input current.

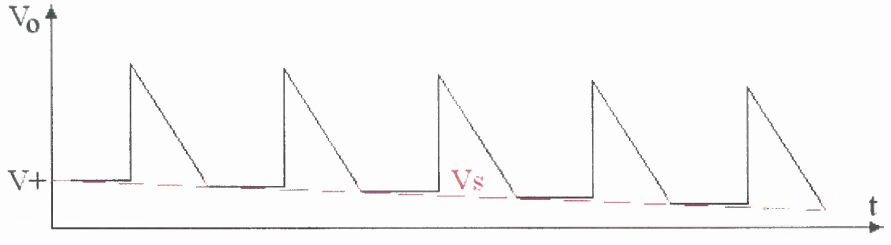
Figure 3.3 shows the zigzag output of SCI corresponding to the transfer and the direct integrations under several different situations. Fig. 3.3 (a) shows the output of SCI vs. time when there is no AC signal presented. Route 1 to 2 represents the period of transfer integration while the output does not change with time. Route 2 to 3 corresponds to the instant charge transfer from C1 to C2, yielding a jump of the output level. Followed is the route 3 to 4 associated with the discharging period of direct integration. With equal durations of both integrations, Any DC input is cancelled out in any two successive transfer and direct integration phases. Fig. 3.3 (b) and (c) indicates how the small correlated AC signal is gradually accumulated while the DC input is suppressed under multi-cycle integration (5 cycle integrations are pictured in the figures). In Fig3.3 (b), the small correlated signal is input in the period of transfer integration. The short vertical red line drawn on the top of transfer line shows the comparison of accumulation of the small signal integration with that of background accumulation during the entire period of transfer integration phase. The red dashed line represents the signal accumulation through multi-cycle integration. In Fig. 3.3 (c), the small correlated signal is input in the period of direct integration. Fig. 3.3 (d) to (e) show the same outputs of SCI as Fig. 3.3 (a) to (c) except that the large DC input is negative. Multi-cycle integration is not necessary starting from the transfer integration. It can start from either the direct integration or the transfer integration or even start from the blocking phase.



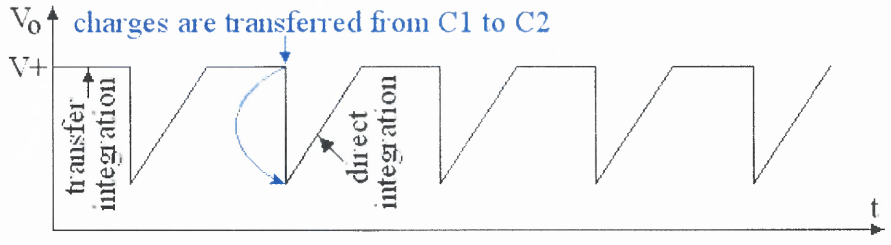
(a) positive DC input current without AC signal



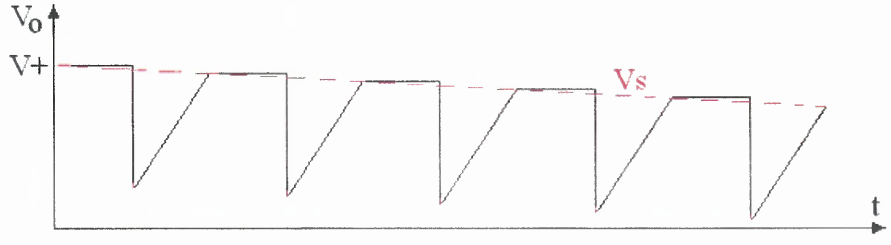
(b) positive DC input with small AC input during transfer integration phase



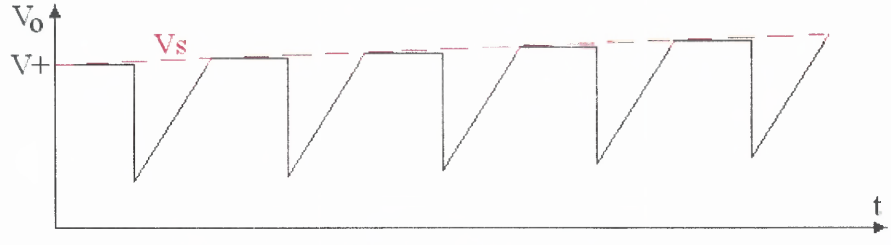
(c) positive DC input with small AC input during direct integration phase



(d) negative DC input current without AC signal



(e) negative DC input with small AC input during transfer integration phase



(f) negative DC input with small AC input during direct integration phase

Figure 3.3 Outputs of SCI under different situations

It is easy to see that the equivalent circuits in both the transfer and direct integrations are RC charging or discharging circuits. However, it is not straightforward what is the output of SCI during both the integration phases. In next section the calculation of SCI based on the equivalent circuits will be addressed.

3.3 Injection Efficiency and the Output of SCI

3.3.1 Injection Efficiency

In the readout circuit, the injection efficiency is the ratio of injecting signal charges collected by the integrator to the total signal charges of injection. In the SCI circuit, the main source that reduces the injection efficiency is the stray capacitance at input node 1. The injection efficiency can be calculated by using the equivalent injection circuit as shown in Fig. 3.4. In this circuit, C_p is the parasitic capacitance at input node, which includes the pad, the bonding wire capacitances. It is obvious that the injection efficiency, η, is given by

$$\eta = \frac{C1}{C1 + C_{\text{det}} + C_p} \tag{3.1}$$

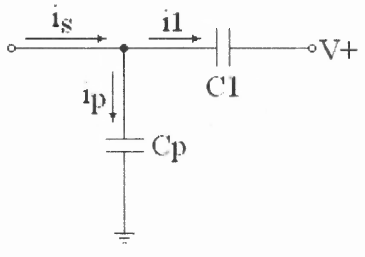
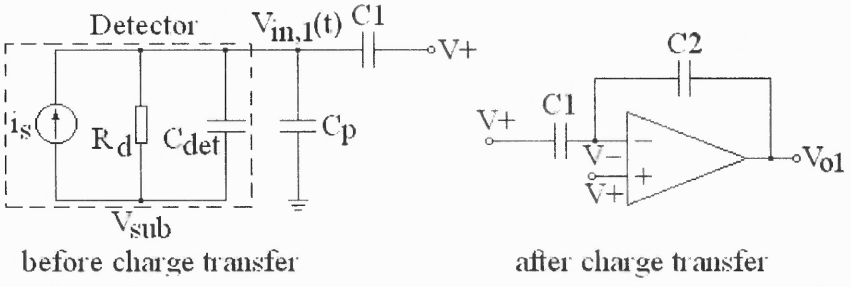


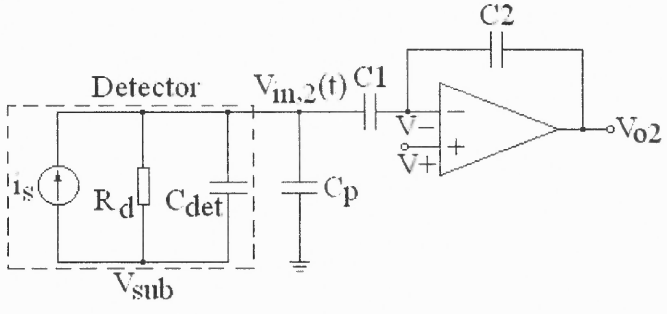
Figure 3.4 The equivalent circuit used for calculation of injection efficiency

3.2.2 Output of SCI

For a real operational amplifier (op-amp), its open-loop gain A_o is a finite number, which will cause a small voltage difference at its two differential input nodes, yielding an offset voltage at the two nodes. Here by offset voltage it means the voltage difference between the two differential input nodes of the op-amp. It may also be caused by the asymmetry of the real differential stage. Let $V_{offset}=V_+-V_-$. This voltage will make the charge collection asymmetric, and keep some residual charges on C1 when the integrated charges on C1 are transferred to C2. The maximum V_{offset} is $(V_{dd}-V_{ss})/2A_o$, here V_{dd} is the maximum voltage source and V_{ss} is the minimum voltage source of the circuit. It changes with the change of the output since the open-loop gain is finite. In order to evaluate the effect of the offset voltage, the equivalent circuits will be checked related to the two phases of transfer and direct integrations, which are shown in Fig. 3.5.



(a) equivalent circuit during transfer integration phase



(b) equivalent circuit during direct integration phase

Figure 3.5 Equivalent circuits of SCI at two different phases

In Fig. 3.5, a detector, which is biased with V_{sub}, is replaced by its equivalent circuit, which is composed of a current source, a leakage resistor and a junction capacitor. In transfer integration phase, the current is first integrated on C1, and then transferred to C2. In direct integration phase, the input current is directly accumulated on C1 and C2.

During direct integration phase, the voltage at input node, $V_{in,2}$, satisfies

$$i_{s2} + \frac{V_{sub} - V_{in,2}}{R_d} = (C_{det} + C_p + C1)\frac{dV_{in,2}}{dt} - C1\frac{dV_-}{dt} \tag{3.2}$$

The additional equations that can be used to solve (3.2) are

$$(V_+ - V_-)A_o = V_{o2} \tag{3.3}$$

$$C1\frac{d(V_{in,2} - V_-)}{dt} = C2\frac{d(V_- - V_{o2})}{dt} \tag{3.4}$$

$$V_{in,2}(0) = V_+ \tag{3.5}$$

Assume i_s and R_d do not change with time, the solution of (3.2) can be easily found

$$V_{in,2}(t) = V_+ e^{-\frac{t}{t_{RC,2}}} + (i_{s2}R_d + V_{sub})(1 - e^{-\frac{t}{t_{RC,2}}}) \qquad 0 \le t \le \tau_2 \tag{3.6}$$

where t_{RC} is the RC time constant given by

$$t_{RC,2} = R_d[C_d + C_p + C1 - \frac{C1^2}{C1 + C2(1 + A_o)}] \tag{3.7}$$

At the end of the integration, or at time τ_2, the voltage change at output is found by

$$\Delta V_{o2} = -\frac{C1A_o[V_{in}(\tau_2) - V_+]}{C1 + (1 + A_o)C2} \tag{3.8}$$

when A_o»1 and A_oC2»C1, the voltage change at output becomes

$$\Delta V_{o2} = -\frac{C1}{C2}[V_{in}(\tau_2) - V_+] \tag{3.9}$$

In the transfer integration phase, the voltage at input node during charge accumulation can be found by setting dV./dt=0 in (3.2). The result is

$$V_{in,1}(t) = V_+ e^{-\frac{t}{t_{RC,1}}} + (i_{s1}R_d + V_{sub})(1 - e^{-\frac{t}{t_{RC,1}}}) \qquad 0 \le t \le \tau_1 \tag{3.10}$$

the RC time constant now is found by

$$t_{RC,1} = R_d(C_d + C_p + C1) \tag{3.11}$$

By the end of accumulation or at time τ_1, the charges in C1 and C2 are

$$Q_{1i} = [V_{in,1}(\tau_1) - V_+]C1 \tag{3.12}$$

$$Q_{2i} = (V_{o1}^i - V_-^i)C2 \tag{3.13}$$

After the charge transferred, the charges in C1 and C2 become

$$Q_{1f} = (V_+ - V_-)C1 \tag{3.14}$$

$$Q_{2f} = (V_{o1} - V_-)C2 \tag{3.15}$$

From $Q_{1i}+Q_{2i}=Q_{1f}+Q_{2f}$ at node V-, it can be found

$$\Delta V_{o1} = V_{o1} - V_{o1}^i = \frac{C1A_o[V_{in,1}(\tau_1) - V_+ - V_{o1}^i / A_o]}{C1 + (1 + A_o)C2} \tag{3.16}$$

Normally, $A_o \gg 1$, and $A_oC2 \gg C1$. (3.16) becomes

$$\Delta V_{o1} = \frac{C1}{C2}[V_{in,1}(\tau_1) - V_+ - V_{o1}^i / A_o] \tag{3.17}$$

Now from (3.9) and (3.17), the change of voltage at output is

$$\Delta V_{o1} + \Delta V_{o2} \approx \frac{C1}{C2}[V_{in,1}(\tau_1) - V_{in,2}(\tau_2) - V_{o1}^i / A_o] \tag{3.18}$$

Let

$$\tau_1 = \tau_2 = \tau / 2 \tag{3.19a}$$

$$i_{s1} = i_s + I_b \tag{3.19b}$$

$$i_{s2} = -i_s + I_b \tag{3.19c}$$

where i_s is the modulated signal input current, I_b the background related current. Now (3.18) becomes

$$\Delta V_{o1} + \Delta V_{o2} \approx \frac{C1}{C2}[\frac{i_s \tau}{2(C_{\text{det}} + C_p + C1)} - V_{o1}^i / A_o] \tag{3.20}$$

(3.20) represents the voltage change at output after one cycle of charging and discharging. The first term in the bracket corresponds to the signal contribution. The second term, however, put a fixed pattern in the readout. This fixed pattern will increase with the increase of the number of cycles. Now the offset voltage for every cycle will be checked. Let $V_{os,k}^i$ denotes the initial offset voltage of the k'th cycle and $V_{os,1}^i = V_{offset}$. Let

$$V_s = i_s \tau / 2(C_{\text{det}} + C_p + C1) = \frac{\eta i_s \tau}{2C1} \tag{3.21}$$

Then

$$\begin{aligned} V_{os,k}^i = V_{o,k-1} / A_o &= [V_{os,k-1}^i A_o + \frac{C1}{C2}(V_s - V_{os,k-1}^i)] / A_o \\ &= \frac{C1}{A_o C2} V_s + V_{os,k-1}^i (1 - \frac{C1}{A_o C2}) \\ &= \cdots \\ &= V_s - (V_s - V_{offset})(1 - \frac{C1}{A_o C2})^{m-1} \end{aligned} \tag{3.22}$$

After *m* cycle, the output will be

$$V_{os1} = A_o V_{os,m+1}^i = A_o \left[V_s - (V_s - V_{offset})(1 - \frac{C1}{A_o C2})^m \right] \tag{3.23a}$$

or

$$V_{os1} = A_o V_s \left[1 - (1 - \frac{C1}{A_o C2})^m \right] + V_{offset}(1 - \frac{C1}{A_o C2})^m \tag{3.23b}$$

The second term at the right side of (3.23b) represents the fixed pattern noise due to offset voltage of the op-amp and is a function of the cycle number. The output voltage after multi-cycle integration usually has no linear relationship with the cycle number m. However, it has linear relationship with the intensity of the image signal.

Usually, $A_oC2 \gg C1$, (3.23a) become

$$\begin{aligned} V_{os1} &= mV_s C1/C2 + V_{offset}(1 - \frac{C1}{A_o C2})^m \\ &= \frac{\eta i_s m \tau}{C2} + V_{offset}(1 - \frac{C1}{A_o})^m \end{aligned} \tag{3.24}$$

Now if let

$$i_{s1} = -i_s + I_b \tag{3.25a}$$

$$i_{s2} = i_s + I_b \tag{3.25b}$$

i.e., the phase of the modulated signal is changed by 180°, then the output will be

$$V_{os2} = A_o V^i_{os,m+1} = -A_o V_s \left[1 - (1 - \frac{C1}{A_o C2})^m \right] + V_{offset}(1 - \frac{C1}{A_o C2})^m \tag{3.26}$$

From (3.23b) and (3.26), the differential output is

$$\begin{aligned} V_{os} = V_{os1} - V_{os2} &= 2A_o V_s [1 - (1 - \frac{C1}{A_o C2})^m] \\ &\approx \frac{C1}{C2} \frac{m\tau i_s}{C_{\text{det}} + C_p + C1} \\ &= \frac{\eta i_s m \tau}{C2} \end{aligned} \tag{3.27}$$

The result is independent of the initial offset voltage of the op-amp. Any fixed pattern due to charge injection and clock feedthrough can also be subtracted by this method.

The operation modes of the switched-capacitor integrator are dependent on the timing of the switches, which will be addressed in the following section.

3.4 Operational Modes of the SCI

Since the SCI can perform the basic functions of GMCI, multi-mode operation can be found by using these functions.

3.4.1 Single Cycle Integration (Equivalent to CTIA)

In this mode, S1, and S2 are off, and S3 is on. The process begins with the reset of integrator by switch S4. Followed are the first sample and the signal integration. At the end of integration, the integrated signal is sampled again. The residual charge due to the reset will be subtracted by the first sample, which only includes residual charges. This correlated-double sampling (CDS) can be finished by a differential amplifier after multiplexing (see next chapter). Fig. 3.6 illustrates the timing forms and the output of the integrator.

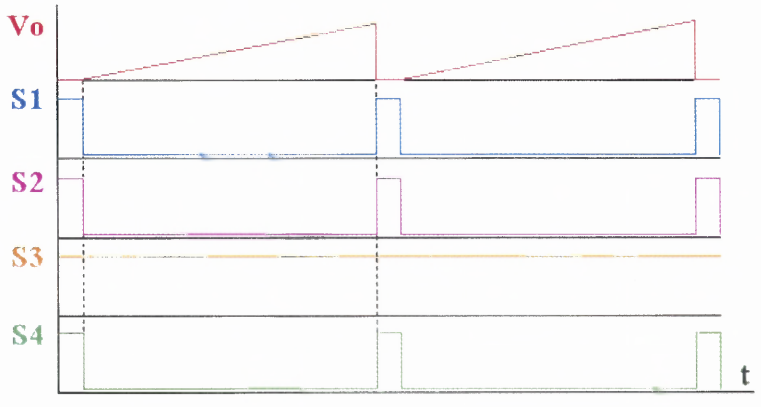


Figure 3.6 Waveforms of the switches and the output of integrator for CTIA mode

The relationship between the input current i_{in} and the change of voltage at output of the integrator is given by

$$\Delta V_o = \frac{\eta \int_0^{T_i} i_{in} dt}{C_2} \tag{3.28}$$

This mode is equivalent to CTIA operation. According to Equation (2.72), the minimum achievable signal is

$$i_{s,\min} = \frac{I_b}{\eta \sqrt{N_{sat}}} \tag{3.29}$$

3.4.2 Gated Integration with Multi-Point Summation (MGI)

This mode is similar to that of CTIA except the reset switch will not be enabled until a number of cycle integrations are summed together in the integrator since the last reset. Fig. 3.7 pictures the timing form and the output of an integrator. Small signal with negative large background-related current is fed in the direct integration phase. When signal is absent, the switched-capacitor integrator just rejects the background related input current. In this figure, five gated signals are summed together in the integrator. According to Chapter 3, the performances of MGI are similar to those of the average of multi-sample CTIA if the impact of ADC is ignored. However, MGI is suited when gated integration signal is too small for ADC to acquire. The improvement of signal-to-noise ratio is also proportional to the square root of the number of cycles. The minimum measurable signal is also given by (3.29). The output voltage is

$$\Delta V_o = \frac{m\eta \int_0^{T_i} i_{in} dt}{C_2} \tag{3.30}$$

When SCI is operating in MGI mode, the input signal can also be fed in the transfer integration phase.

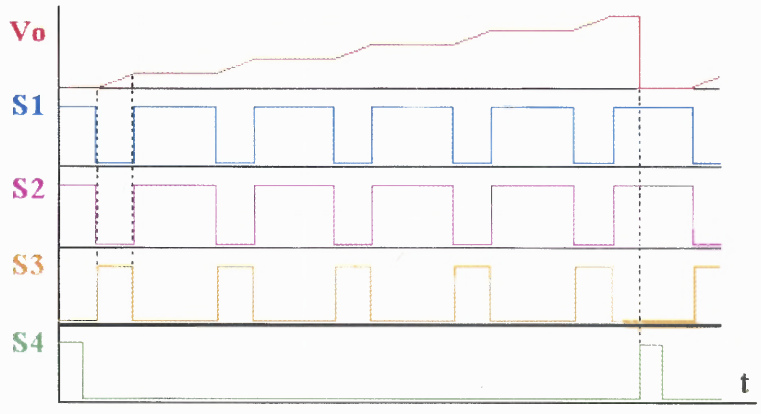


Figure 3.7 Waveforms of the switches and the output of integrator for MGI mode

3.4.3 Gated Integration with Background Subtraction (BSGI)

In some situations, the gated signal may suffer from large background drift [40]. The multi-cycle background-subtraction gated integration may be employed to cancel out the low-frequency drift. The SCI can also be operated in this mode. The timing of the switches is shown in Fig. 3.8. In this figure, three cycles of integration with background subtraction are illustrated. The brown dashed line represents the weak signal integration. There are three phases for integration, reverse integration and blockage. The operation begins by resetting the circuit by turning S1, S3, and S4. When S1 and S2 are off and S3 on, the integrator is on its direct integration. At the end of this integration, the C1 is discharged by first turning off S3 followed by turning on S1 and S2. In the transfer integration phase, S1 and S3 are off and S2 is on. The input current will be integrated to C1 first. At the end of this integration, the charges stored in C1 will be transferred to C2 by first turning off S2 followed by turning on S1 and S3. For any two successive direct

and transfer integration phases, the net charges stored in C2 is the difference of the charges associated with the two integrations. In this way, the DC part will be cancelled out and the AC part with modulation frequency and phase will be gradually integrated. Besides the transfer and direct integration phases, there is another blocking phase when S1 and S2 are on, and S3 is off. In blocking phase, all the background is blocked, and the integrator is in a holding status. The output voltage, in this case, is given by (3.23b). According to Equation (2.86), the minimum measurable signal is

$$i_{s,\min} = \frac{I_b}{\eta N_{sat}} \tag{3.31}$$

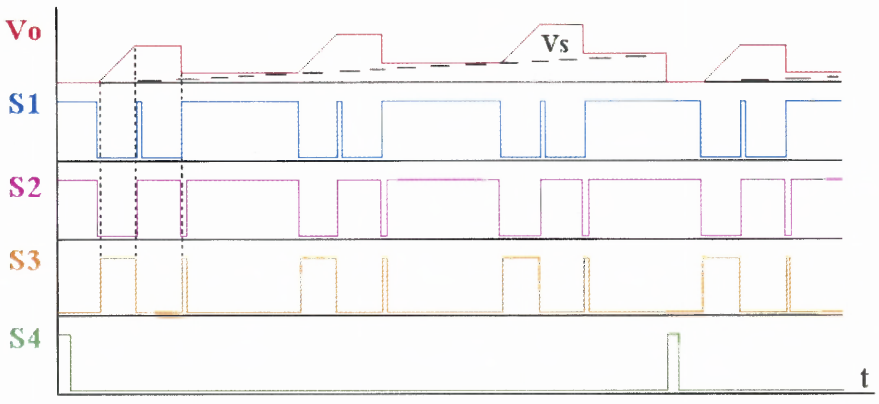


Figure 3.8 Waveforms of the switches and the output of integrator for BSGI mode

3.4.4 Phase-Sensitive Detection (PSD)

There is some dead time between the cycles in BSGI operation. If the dead time goes to zero, then BSGI becomes operating in phase-sensitive detection mode. The reason to distinguish PSI from BSGI is similar to that of Lock-in amplifier differing from Gated boxcar averager. The waveforms of the switches are illustrated in Fig. 3.9.

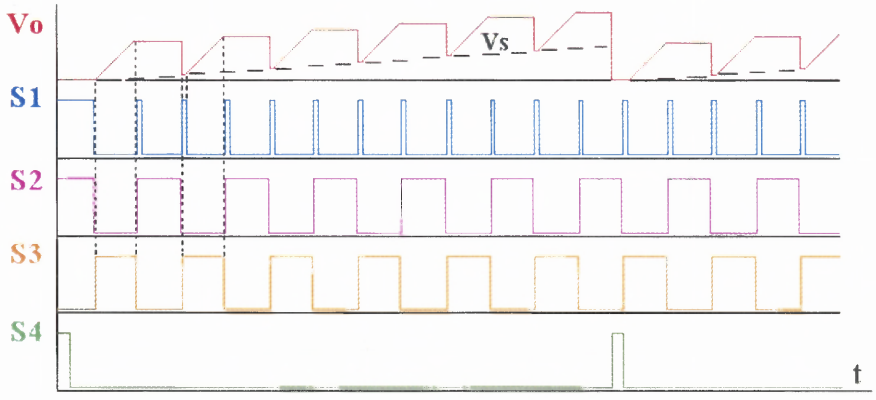


Figure 3.9 Waveforms of the switches and the output of integrator for PSD mode

3.5 Summation

The proposed switched-capacitor integrator has all the basic functions of gated multi-cycle integration. It can operate in one of the following modes, CTIA, MGI, BSGI, and PSD. If a boxcar averager is connected to the output of SCI, then it will perform all the functions of GMCI. In next chapter, the design of the SCI circuit will be addressed by using HP-0.5μm processing foundry via MOSIS service.

CHAPTER 4

DESIGN OF SWITCHED-CAPACITOR INTEGRATOR

4.1 Introduction

General design of FPA begins from the requirements of application system. Such requirements concerning FPA include the resolution (i.e. the number of pixels), the operating temperature, the dynamic range or sensitivity, the wavelengths or target temperature, the frame rate and the maximum power permitted for consuming. According to the wavelengths and operating temperature, the kind of detector array can be determined. Sometimes the wavelengths, the operating temperature and the detector array must be traded off due to limited resources. Then referring to the photon flux, frame rate and the specific detector array, one can design the mechanical system, optical system, and readout circuit. The design of readout includes finding suited schematic circuit, making performance simulation based on processing parameters, drawing layout and finding the parasitic components for further simulation. Only the simulation with parasitic components passes the requirements of performance can one finish this step.

Readout circuit includes the input amplifier or the integration stage, the multiplexer for pixel selection and signal transfer, CDS circuit, the output amplifier, testing cells, clock and pulse generators, and possible ADC. Early readout circuits were based on n- or p-MOS. Later on they are almost always based on CMOS technology due to its popularity, low power, and reliability at low temperature.

In this paper, however, the feasibility of GMCI is focused for demonstration. It is not necessary to restrict the circuit to any specific application in this primary stage. In this chapter, the design of the switched-capacitor integrator (SCI) proposed in the previous

chapter, a shift register as a linear multiplexer, and an output amplifier based on HP 0.5μm CMOS foundry organized by MOSIS, are presented. The processing and SPICE BSIM3 model parameters are appended on appendix A. All the device and circuit simulations are based on these parameters. All the circuit simulations are done by Top-Spice

4.2 Characteristics of MOSFET

The readout circuit is based on MOSFETs. A quick review of the performance of MOSFETs will be helpful for the designing of circuits.

4.2.1 DC Characteristics

A MOSFET is a four terminal voltage-current device as depicted in Fig. 4.1. The behavior of drain-source DC current is described as follows:

i) Cutoff Region, $V_{GS} \leq V_{th}$ (threshold voltage of the MOSFET)

$$I_{DS} = 0 \tag{4.1}$$

ii) Linear Region, $V_{DS} < V_{GS} - V_{th}$

$$I_D = \beta(1 + \lambda V_{DS})(V_{GS} - V_{th} - \frac{V_{DS}}{2})V_{DSs} \tag{4.2}$$

where λ is channel-length modulation factor, and

$$\beta = KP\frac{W}{L} = \mu_0 C_{ox}\frac{W}{L} \tag{4.3}$$

Here μ_0 is the carrier mobility, C_{ox} the oxide capacitance per unit gate area.

The resistance of the channel, R_{DS}, is given by

$$R_{DS} = \frac{V_{DS}}{I_D} = \frac{1}{\beta(1+\lambda V_{DS})(V_{GS} - V_{th} - V_{DS}/2)} \approx \frac{1}{\beta(V_{GS} - V_{th})} \tag{4.4}$$

iii) Saturation Region, $V_{DS} \geq V_{GS} - V_{th}$

$$I_{D,sat} = \frac{\beta}{2}(1+\lambda V_{DS})(V_{GS} - V_{th})^2 \tag{4.5}$$

where the threshold voltage, V_{th} is determined by

$$V_{th} = V_{bi} + \gamma(\phi_s - V_{BS})^{1/2} \tag{4.6}$$

Here γ is the body effect factor, ϕ_s the surface inversion potential, and the build-in voltage is defined as:

$$V_{bi} = V_{th0} - \gamma\sqrt{\phi_s} \tag{4.7}$$

where V_{th0} is the zero-bias threshold voltage.

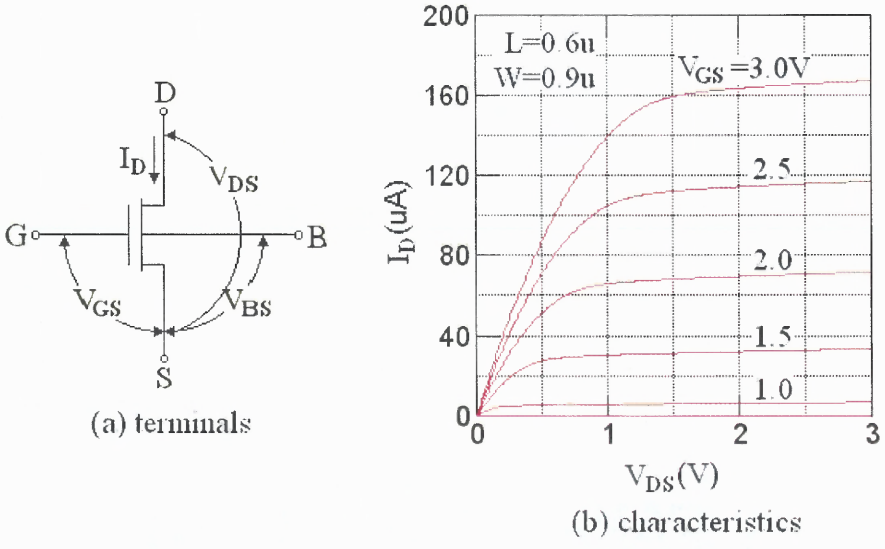


Figure 4.1 A MOSFET's four terminals and its characteristics

4.2.2 Small AC Model

Equivalent small AC circuit for a MOSFET is shown in Fig. 4.2. In this circuit, the transconductance g_m, in region of saturation, is given by

$$g_m = \left(\frac{\partial I_{D,sat}}{\partial V_{GS}}\right)_{V_{BS},V_{DS}} = KP\frac{W}{L}(1+\lambda V_{DS})(V_{GS}-V_{th})$$
$$= \sqrt{2KP\frac{W}{L}(1+\lambda V_{DS})I_{D,sat}} \qquad (4.8)$$
$$= \frac{2I_{D,sat}}{V_{GS}-V_{th}}$$

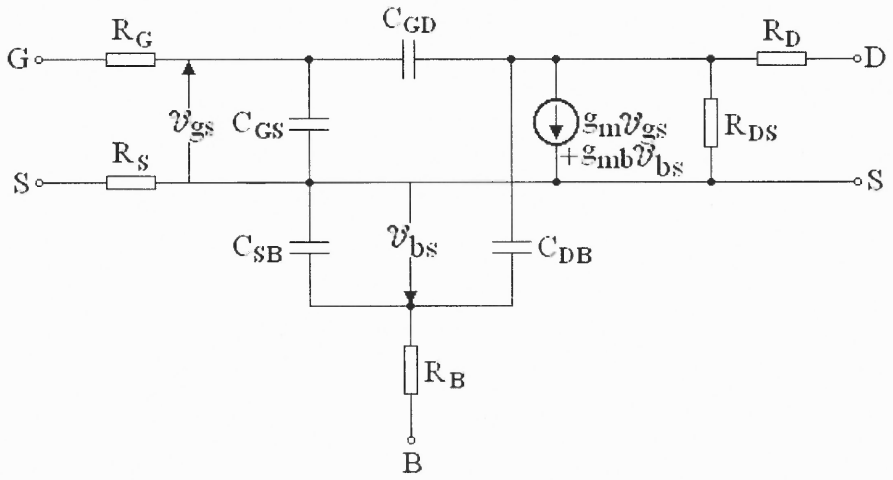


Figure 4.2 A small ac model for a MOSFET

The bulk transconductance g_{mb} is defined as

$$g_{mb} = \left(\frac{\partial I_{D,sat}}{\partial V_{BS}}\right)_{V_{GS},V_{DS}} = \frac{\gamma}{2\sqrt{2\phi_s - V_{BS}}} \qquad (4.9)$$

The output conductance g_o, is the slope of I_{ds} at saturation region

$$g_o = \frac{1}{R_o} = \left(\frac{\partial I_{D,sat}}{\partial V_{DS}}\right)_{V_{GS},V_{BS}} \approx \lambda I_{D,sat} \qquad (4.10)$$

The parasitic capacitances are listed in table 4.1

Table 4.1 MOSFET Capacitances

In Saturation		In Linear Region	
$C_{GS} = C_{GS0} + 2/3C_{oxt}$	$C_{SB} = C_{JSBt} + 2/3C_{BCt}$	$C_{GS} = C_{GS0} + 1/2C_{oxt}$	$C_{SB} = C_{JSBt} + 1/2C_{BCt}$
$C_{GD} = C_{GD0}$	$C_{DB} = C_{JBDt}$	$C_{GD} = C_{GD0} + 1/2C_{oxt}$	$C_{DB} = C_{JBDt} + 1/2C_{BCt}$

$C_{oxt} = WLC_{ox}$ $\quad C_{ox} = \varepsilon_{ox} / t_{ox}$

$C_{BCt} = WLC_{JBC}$ $\quad C_{JBC} = C_J / (1 - V_{BC} / \phi_j)^{mj}$

$C_{JBSt} = A_S C_{JSB} + P_S C_{JSWSB}$ $\quad C_{JSB} = C_J / (1 - V_{BS} / \phi_j)^{mj}$ $\quad C_{JSWSB} = C_{JSW} / (1 - V_{BS} / \phi_j)^{mjsw}$

$C_{JDBt} = A_D C_{JDB} + P_{JSWDB}$ $\quad C_{JDB} = C_J / (1 - V_{BD} / \phi_j)^{mj}$ $\quad C_{JSWDB} = C_{JSW} / (1 - V_{bd} / \phi_j)^{mjsw}$

$C_{J(SW)} = \sqrt{q\varepsilon_{Si} N_b / 2\phi_{j(sw)}}$ $\quad mj = 1/3, \ldots, 1/2$

ϕ_j is the build-in junction potential $\quad$ A_S is the source area

P_S is the source perimeter $\quad$ A_D is the drain area

C_{GX0} is the overlap capacitance between G and X $\quad$ P_D is the drain perimeter

4.2.3 Noise Sources of MOSFET

The noise generators in a MOSFET are due to thermal and flicker ($1/f$ noise) noises. The r.m.s thermal or Johnson noise currents in a MOSFET are generated by the effective channel resistance and by the parasitic drain, source, gate, and substrate resistances. The noise currents due to parasitic resistances are given by

$$\sqrt{\overline{i_{RX}^2}} = \sqrt{\frac{4kT}{R_X}} \tag{4.11}$$

where X indicates D (drain), S (source), G (gate) or B (substrate) terminals.

The thermal noise due to the channel resistance depends on its operating mode. If the MOSFET is in its linear region, the thermal noise would be simply given by

$$\sqrt{\overline{I_d^2}} = \sqrt{\frac{4kT}{R_{DS}}} \tag{4.12}$$

where R_{DS} is given by Eq. (4.4). When the MOSFET is in its saturation region, the channel is not homogeneous. And the resistance is modeled as $3/2g_m$. Thus, its thermal noise will be

$$\sqrt{\overline{I_{D,sat}^2}} = \sqrt{\frac{8}{3}kTg_m} \tag{4.13}$$

The flicker or 1/f noise results from trapping of charges at the oxide/semiconductor interface in the inverted channel. This trapping gives rise to a change in the drain current caused by the carrier recombination and/or generation taking place via the traps. Since the carrier lifetime in silicon is on the order of tens of microseconds the resulting current fluctuations are concentrated at lower frequencies. The flicker noise can be modeled as a voltage source in series with the gate of value

$$\sqrt{\overline{v_{1/f}^2}} = \sqrt{\frac{K}{WLC_{ox}^2 f}} \tag{4.14}$$

where K is a constant dependent on the device characteristics and is around 10^{-32} C^2/cm^2 for P-MOSFET and 4×10^{-31} C^2/cm^2 for N-MOSFET. An important point to note here is that the $1/f$ noise is inversely proportional to the channel area of the transistor WL.

For hand calculations the thermal noise due to the parasitic resistances will be neglected. In this case, the total input-referred noise is given by

$$\overline{v_{ieq}^2} = \frac{8kT}{3g_m} + \frac{K}{WLC_{ox}f} \tag{4.15}$$

And the simplified noise model is shown in Fig. 4.3

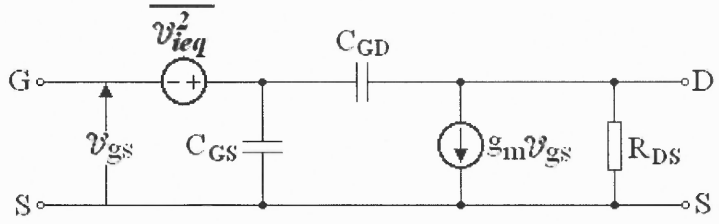


Figure 4.3 A simplified noise model of a MOSFET

4.3 Design of the Switched Capacitor Integrator

The SCI circuitry is composed of switches, operational amplifier and capacitors. The non-ideal switch and amplifier will introduce additional noise and fixed pattern. The goal of the design is trying to understand the issues and take appropriate strategies to limit them such that the performance of the circuitry is not overshadowed.

4.3.1 Characteristics of MOS Switch

The main features of a MOS switch are switch speed, charge injection, and clock feedthrough. The rise and fall times of a submicron gate switch is usually less than 0.1 ns. This can impose a problem only in readout circuit of extremely high speed FPAs. The charge injection and clock feedthrough, however, are the main sources of noises in a MOS switch.

4.3.1.1 General Issue of MOS Switch A switch is used to pass voltage or current. An ideal switch has the characteristics of zero resistance when it is on, infinite resistance when it is off and no delay when it is turned on or off. A real MOSFET switch however, has turn-on non-zero channel resistance, turn-off leakage current, threshold voltage, and parasitic capacitances.

The turn-on channel resistance will induce some time delay when voltages or charges pass through the switch. Furthermore, this resistance corresponds to charges in the channel, which are accumulated and injected through terminals. Thus, charge injection must be dealt carefully when charge integration is involved. The charge injection will be discussed in more detail later on. The turn-off leakage current will cause some signal loss in the integrator or sample/hold circuitry. The leakage basically resulted from the subthreshold current and the inverse current of the pn junction between the channel and the source or drain. This leakage now is extremely low and can be ignored. The threshold voltage raises several issues. Firstly the gate-source voltage must be larger than the threshold in order to keep the switch on, which will force the voltage to drop across the switch when the input voltage is high for N-MOSFET and low for P-MOSFET. Thus, it will introduce some voltage offset in the switch at some special cases. Secondly, when the gate-source voltage is lower than the threshold, some charges will feed through terminals via parasitic capacitors, which will induce some fixed patterns if the switch is somehow related to the integrator. This so-called capacitive feedthrough will be studied in more detail later in this chapter. In addition, the parasitic capacitances will also cause some time delay. The driver of the switch must be sort of capability of driving current. A simple MOSFET switch model is illustrated in Fig. 4.4.

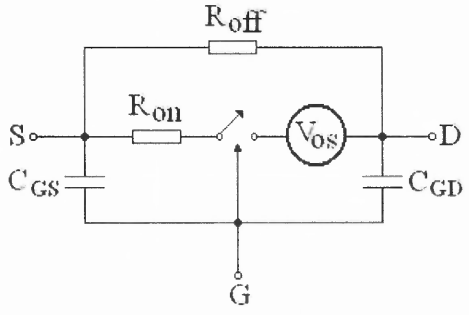


Figure 4.4 A model of a MOS switch

The noise sources of a switch are mainly the thermal and flicker noises as discussed in section 4.2.3. When a switch is used for reset, the kTC noise arises.

4.3.1.2 Charge Injection Figure 4.5 shows the basic charge injection effect. When the MOSFET is on, some charges are present under the gate oxide resulting from the inverted channel. When the switch turns off, part of these charges will be injected into the capacitor C_{int}. For a nMOSFET the charge under the gate can be estimated by

$$Q_{IN} = -C_{ox} \cdot W \cdot L \cdot (V_{GSN} - V_{THN}), \tag{4.16a}$$

and for a pMOSFET the channel charge is

$$Q_{IP} = -C_{ox} \cdot W \cdot L \cdot (V_{GSP} - V_{THP}), \tag{4.16b}$$

For the HP-0.5μm process, the number of injected electrons can be estimated for a minimum size transistor. According to Table A, $C_{ox} = 3.4 \times 10^{-3} (F/m^2)$, then $N_{IN} = Q_{IN}/e = -3.4 \times 10^{-3} \times 0.6 \times 0.9 \times 10^{-12} \times (3.3 - 0.73)/(1.6 \times 10^{-19}) = -2.9 \times 10^4$, and $N_{IP} = Q_{IP}/e = -3.4 \times 10^{-3} \times 0.6 \times 0.9 \times 10^{-12} \times (-3.3 + 0.86)/(1.6 \times 10^{-19}) = 2.8 \times 10^4$. The number of these charges varies with the areas of gates. They are shown in Fig. 4.6. It is noteed that the injection charges are negative for nMOSFET and positive for pMOSFET.

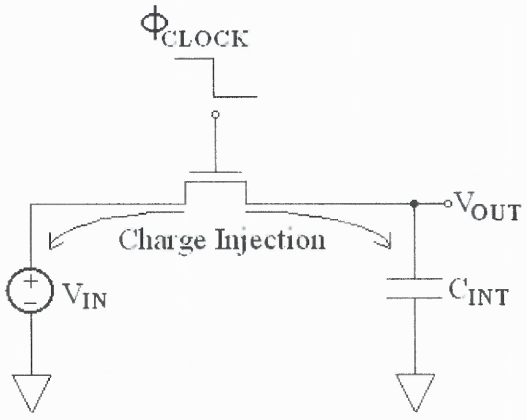


Figure 4.5 The illustration for charge injection.

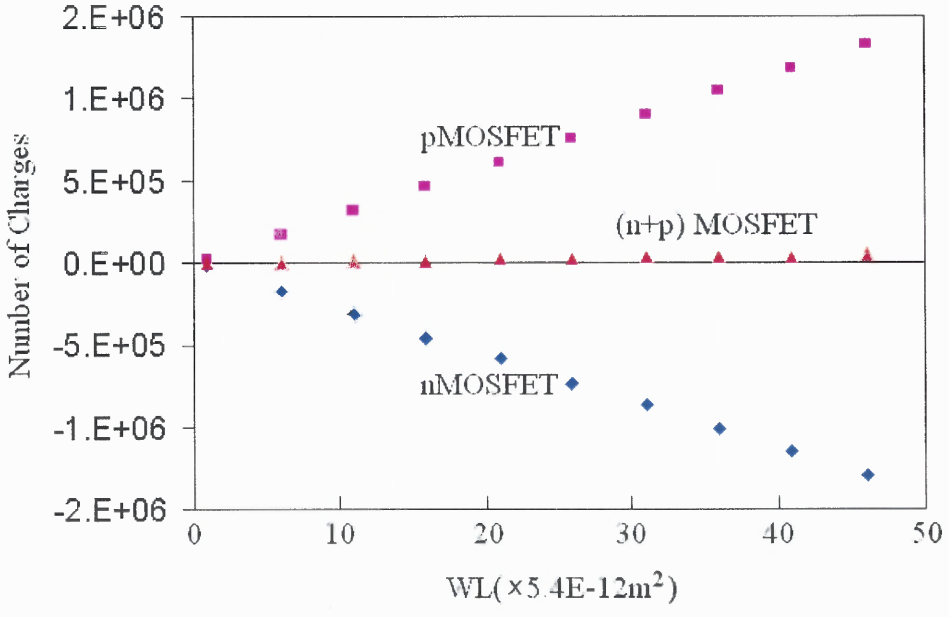


Figure. 4.6 The number of charges in channel versus the area of gate

The charge injection induces two effects for the integrator. First it takes part of the storage well; the integrator must have a capacity that is much larger than the number of injected carrier. Second, the injected charge induces fixed pattern noise that is in the order of $\sqrt{N_{IN}}$, which will limit the minimum detectable signal. The first problem can be

resolved by using a CMOS transmission gated switch that is composed of a NMOSFET and a PMOSFET connected in parallel controlled by complementary signals (Fig. 4.7). Since the signs of the charges in an n-channel and in a p-channel are opposite, the charges injected from the n-channel and the p-channel will cancel out each other if their areas of gates are carefully designed (see Fig. 4.7). The second problem can be sort of suppressed if a slow change clock is used to turn off the switch [43]. When the signal of the clock is slow, the charges in the channel will mostly injected into the substrate.

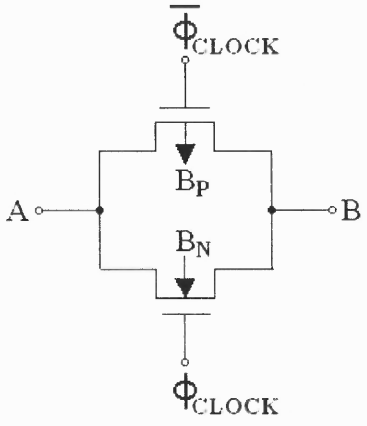


Figure. 4.7 A transmission gated switch

In contrast to charge injection when the switch is turned from on to off, there is charge absorption when the switch is turned from off to on. Hence, when the switch keeps turning on and off, there should no charge accumulation due to multiple switching.

4.3.1.3 Capacitive Feedthrough Capacitive feedthrough occurs when a voltage is applied to the terminal of a capacitor that its other terminal is floated and is connected to at least one other capacitor. Fig. 4.8 illustrates the effect of feedthrough related to a NMOS switch. During the rising edge of $\phi 1$ phase, the gate starts at 0 volts and increases

toward 3.3 volts. In the transition from 0 to $V_{in}+V_{th}$, M is off. Consequently, this part of the clock waveform can couple to C_{int} via C_{GS}. As a result, a portion of the clock signal, ϕ, appears across C_{int} as indicated by (4.17)

$$\Delta Q_{\text{int}} = (\frac{C_{GS}C_{\text{int}}}{C_{\text{int}}+C_{GS}})(V_{in}+V_{th}) \approx C_{GS}(V_{in}+V_{th}). \tag{4.17}$$

These charge change are also proportional to the area of the gate according to table 4.1, and are in the same order as those of charge injection. The remainder of the rising clock waveform is not coupled to C_{int} because M turns on and connects C_{int} to the low-impedance voltage source.

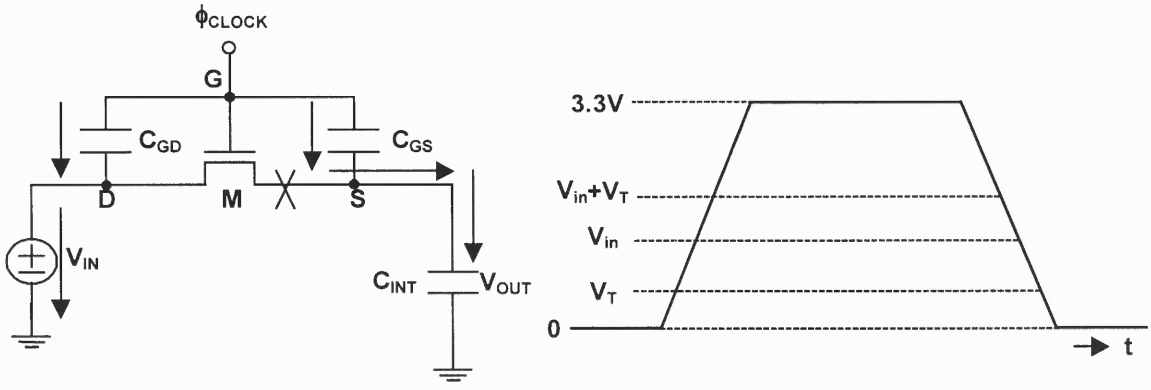


Figure 4.8 The illustration of capacitive feedthrough and the clock waveform

When M turns off, the feedthrough occurs once again as the clock goes from $V_{in}+V_T$ to zero volts. If the voltage change due to the on transition still remains on the integrator, ideally the feedthrough due to the off transition will cancel it out if the switching process is completely symmetric. Again the capacitive feedthroughs are complementary for n-channel and p-channel switches.

4.3.1.4 Methods to Suppressing the Charge Injection and Feedthrough Charge injection and feedthrough are all induced via capacitor coupling. The main capacitance is related to the gate oxide capacitance, C_{ox}. Therefore, the area of the gate switch should be as small as possible given that the time constant is still suited for circuit performance. However, the minimum area of a gate is limited by the feature size of the specified technology. For instance, HP-0.5μm has feature size of 0.5μm with λ of 0.3μm, which gives a minimum gate area of 0.54μm^2, resulting in a number of charge difference of around 3×10^4. If the integration capacitance is 0.5pF, it will put a fixed pattern of around 10mV at output.

There are several ways to suppress charge injection and feedthrough [43-44], among which the transmission gated switch is a wise choice since it plays a role in improving charge injection, feedthrough and offset voltage due to threshold voltage mentioned before. However the areas of the n-channel and p-channel gates must be carefully matched to reduce the additional charge level. The disadvantage of using transmission gate is that it actually takes four transistors with two used for producing an invert signal. Fig. 4.9 shows the layout of a transmission gate used in this research. In the figure, an inverter is put on the left side. Its output is used to control the p-gate. Its input is connected to the n-gate. The transmission gates are put on the right side of the layout.

In order to show the benefit of using transmission gate switch, a comparison is taken by TopSPICE simulations with and without transmission gate. Fig. 4.10 (a) gives the Schematic diagram of a CTIA circuit modified by an input switch. By using a minimum size of n-channel transistor as the input switch, the fixed pattern due to charge injection and clock feedthrough is around 15 mV indicated by the simulation shown in

Fig. 4.10 (b). Fortunately, the charge effects do not accumulated with multi-cycle switching. By using a transmission gate, the fixed pattern is reduced around one order as shown by Fig. 4.10(c).

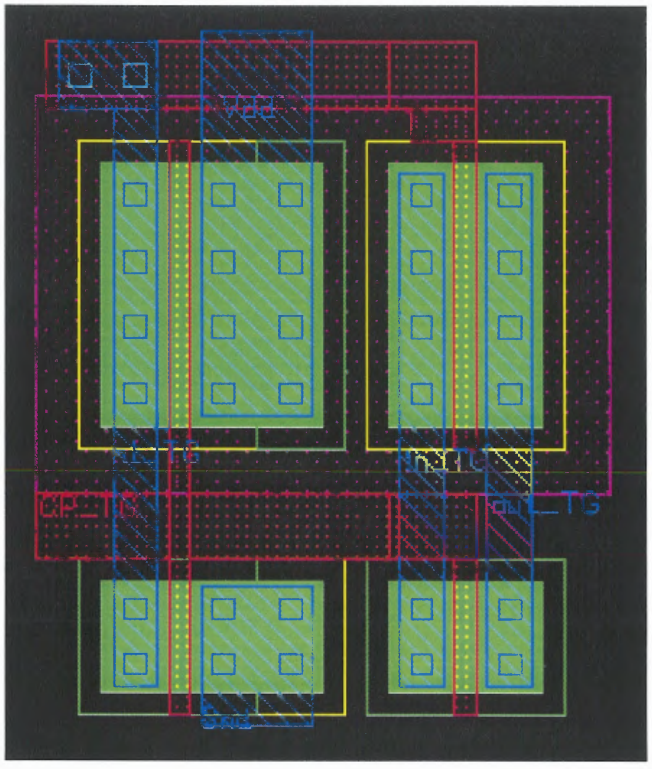
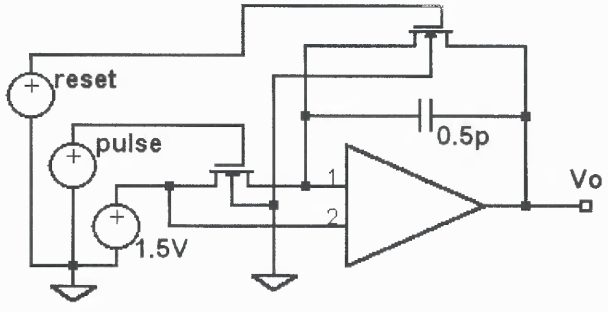
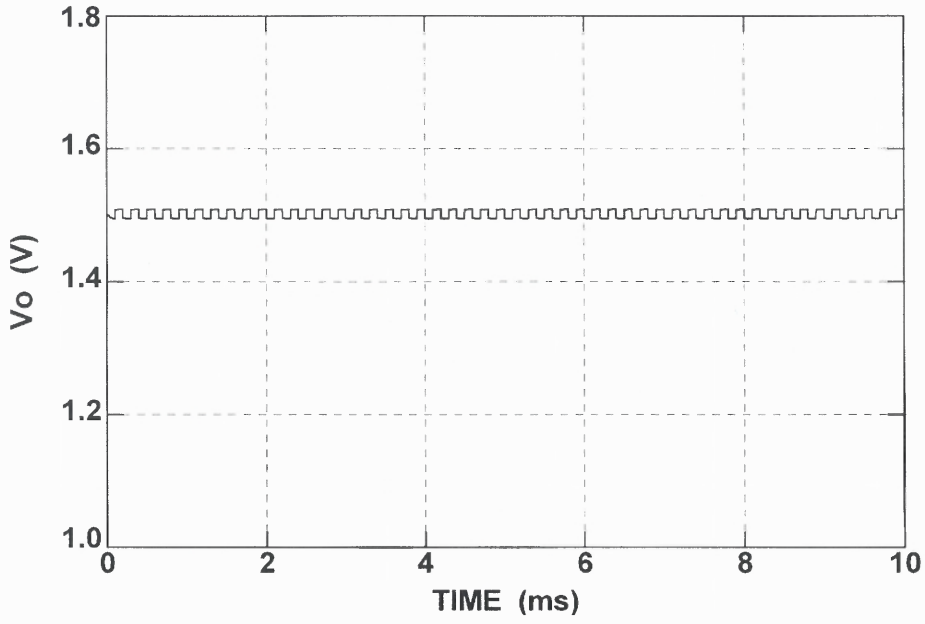


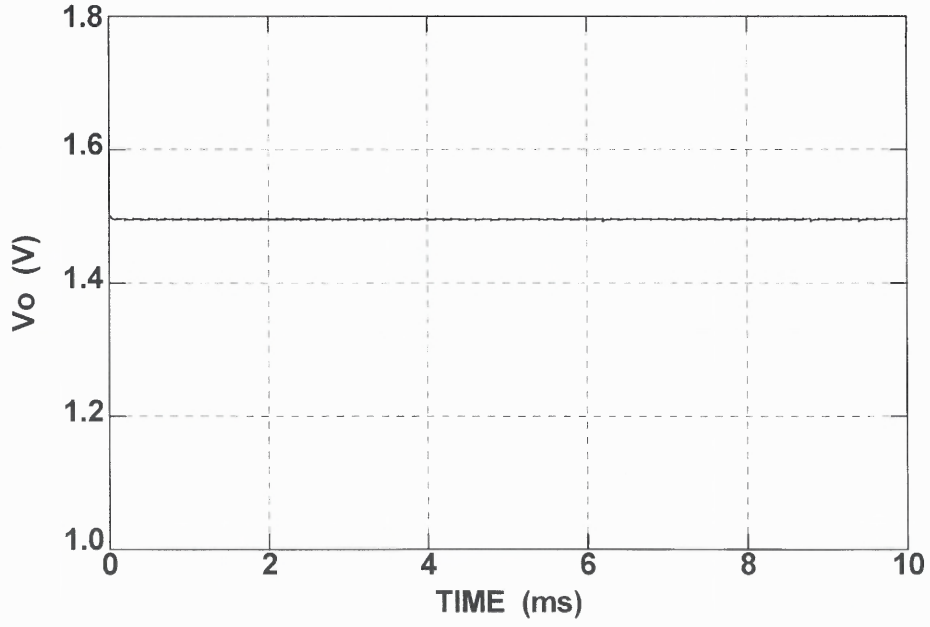
Figure 4.9 Layout of a transmission-gated switch



(a) The Schematic diagram of a circuit used for demonstrating the charge injection and feedthrough



(b) By using a minimum n-channel switch



(c) By using a transmission gate switch

Figure. 10 Charge injection and feedthrough due to switching

4.3.2 Operational Amplifier

The operational amplifier (op-amp) is a fundamental building block in analog integrated circuit design [44-47]. An op-amp usually includes several stages. The basic stages include an input differential amplifier, followed by another gain stage, and an output buffer stage. A block diagram of this construction is shown in Fig. 4.11. In this figure, a compensation capacitance C_c is used to increase the phase margin of the op-amp for stability purpose at high frequency [48].

If the load of the op-amp is a small capacitance as in the cases of CTIA and switched capacitor integrator, the output buffer is not necessary. If the op-amp is used to drive a resistive load or a large capacitive load, then the output buffer is required to have a strong current driving capability.

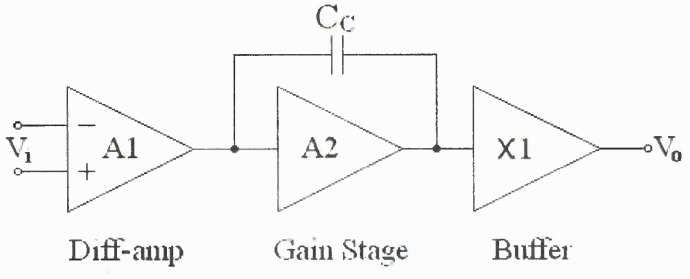


Figure 4.11 Block diagram of basic op-amp

The open-loop gain (A_o), gain-bandwidth (GBW), phase margin (PM), slew rate (SR), common-mode input range (CMR), common mode rejection ratio (CMRR), power supply rejection ratio (PSRR), power dissipation, output voltage swing, output impedance, offset, noise, and layout area are specification parameters involved in op-amp design. However, in readout circuit design, the most important considerations are the layout area, the power dissipation and the noise. For current integration amplifiers, the overwhelming consideration is the real estate. A simple op-amp without output buffer is

still too extravagant for two-dimensional array even with submicron technology. In this case, a single inverter or a cascade amplifier is usually used to replace the normal op-amp. However, in order to satisfy the specific requirements of the switched capacitor gated integrator for GMCI purpose, a two stage, without output buffer, op-amp and a three stage, with output buffer are adopted in the design.

4.3.2.1 A Simple Two-Stage Op-Amp (Miller CMOS OTA) Design The basic two-stage op-amp by using N-well CMOS process is shown in Fig. 4.12. The first stage is a differential stage. It has two p-channel MOSFET input devices M1 and M2. M3 and M4 are the active loads. The second stage is a simple CMOS inverter with M6 as driver and M7 as active load. The compensation capacitor C_c is a feedback capacitance that connects the input and output of the second stage for the purpose of stability at high frequency. Since the op-amp is an operational transconductance amplifier (OTA) and C_c acts as Miller capacitance, the simple two-stage amp is also called the Miller OTA.

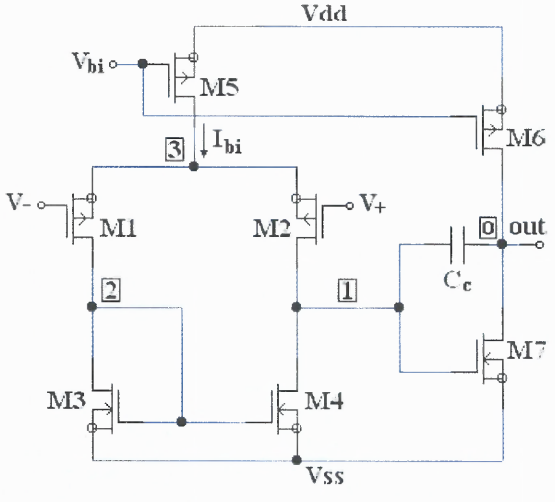


Figure 4.12 Schematic diagram of the two-stage op-amp

The small-signal equivalent circuit of the above op-amp is shown in Fig. 4.13. Where the input is the differential input voltage of the op-amp. $g_{o2//4}=g_{o2}+g_{o4}$ is the load conductance of the first stage. $g_o=g_{o6}+g_{o7}$ is the total load conductance of the last stage. The stray capacitance at node 1 is $C_{n1}=C_{gd2}+C_{db2}+C_{gd4}+C_{db4}+C_{gs7}$.

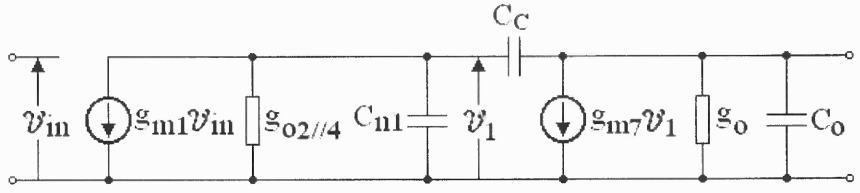


Figure 4.13 An equivalent circuit of the two-stage op-amp

The open-loop gain of the op-amp at low frequency is given by

$$A_o = -\frac{g_{m1}}{g_{o2}+g_{o4}}\frac{g_{m7}}{g_{o6}+g_{go7}} = -\frac{4}{(\lambda_2+\lambda_4)(\lambda_6+\lambda_7)(V_{gs1}-V_{th1})(V_{gs7}-V_{th7})} \tag{4.18}$$

The dominant pole is a result of the Miller effect of the feedback capacitance C_c. Therefore, the bandwidth (BW) is approximately given by

$$BW \approx \frac{g_{02}+g_{o4}}{2\pi A_2 C_c} \tag{4.19}$$

Thus, the gain-bandwidth product (GBW) is obtained by the product of BW and the open-loop gain.

$$GBW \approx \frac{g_{m1}}{2\pi C_c} \tag{4.20}$$

The slew rate (SR) is the maximum rate that the output voltage can change. This is an important parameter for the switched capacitor integrator, which determines the charge

transfer time from C_1 to C_2. In this two-stage op-amp, SR is limited by the compensate capacitance, which is given by

$$SR = \frac{I_{bi}}{C_c} \tag{4.21}$$

The non-dominant pole occurs at the output node and is given by

$$f_{nd} \approx \frac{g_{m7}}{2\pi C_o} \tag{4.22}$$

where

$$C_o = C_L + C_{gd6} + C_{db6} + C_{db7} \tag{4.23}$$

The phase-margin (PM) is now given by

$$PM = 90^o - \tan^{-1}(\frac{GBW}{f_{nd}}) \tag{4.24}$$

The equivalent input noise voltage associated with this op-amp is given by

$$\overline{dv_{nie}^2} = \sum_{i=1}^{7} \overline{dv_{ni}^2}(\frac{A_{ni}}{A_0})^2 \tag{4.25}$$

in which $\overline{dv_{ni}^2}$ is the equivalent input noise voltage of transistor T_i expressed by (4.15) and A_{ni} is the gain from the noise source to the output. Usually the noise of the input stage is the dominant noise source because its gain is largest.

To design an op-amp, means to determine the sizes of transistors and compensation capacitance to satisfy the requirements such as GBW, PM, CMRR, SR et al. in a specified application. For readout circuits, the most important parameters are the area of layout, the power dissipation, the readout noise and GBW. A design may begin from the choice of power dissipation P_s, which is given by $(V_{dd}-V_{ss})(I_{bi}+I_{s7})$. For HP-0.5μm Technology, $V_{dd}-V_{ss} \leq 3.3V$. Simply take $V_{dd}-V_{ss}=3V$, $I_{bi}=1\mu A$ and $I_{bi}=10\mu A$,

which gives P_s=33μW for one pixel. Then V_{gs}-V_{th} for varies transistors and C_c are set to obtain the desired open-loop gain, GBW and PM (>70°). Finally the node voltages and sizes of transistors can be calculated. However, the hand calculation is only the first step for rough estimation, since the model used for hand calculation is a rough model for submicron transistor. Several runs to adjust the parameters through SPICE simulation need be taken in order to obtain the final parameters of an op-amp. One such op-amp's parameters are listed in table 4.2 and their simulation features are shown in Fig. 4.14.

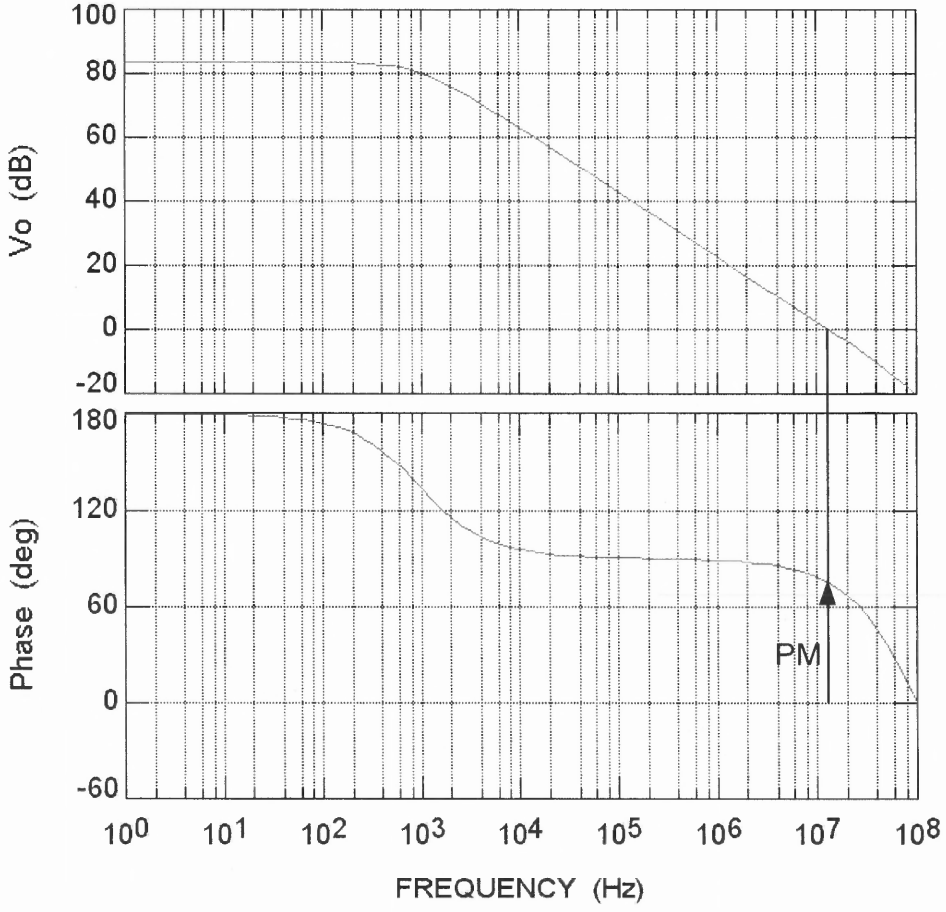


Figure 4.14 The amplitude and phase response of a two-stage op-amp

Table 4.2 Transistor sizes and the characteristics of the Miller CMOS OTA

MOST	P/N	W/L	G_m (μS)	G_o (μS)	I_{ds} (μA)	V_{gs}-V_{th} (V)	V_{sat} (V)	V_{gs} (V)	V_{th} (V)	C_c: 0.1 pF
M1	P	2.4/2.4	8.86	0.04	1.2	0.2440	0.2357	1.1216	0.8776	**Characteristics:**
M2	P	2.4/2.4	8.86	0.04	1.2	0.2440	0.2357	1.1216	0.8776	PM: 75°
M3	N	2.4/3.0	12.6	0.04	1.2	0.1579	0.1480	0.8756	0.7177	A_o: 14.6 k
M4	N	2.4/3.0	12.6	0.04	1.2	0.1579	0.1480	0.8756	0.7177	f_{3dB}: 930 Hz
M5	P	3.3/2.4	14.8	0.28	2.4	0.2952	0.2798	1.1682	0.8730	SR: 24 MV/s
M6	P	11.7/2.4	69.3	0.38	12	0.3134	0.3096	1.1682	0.8548	GBW: 12 MHz
M7	N	4.7/1.2	113	0.49	12	0.1732	0.1634	0.8756	0.7024	

4.3.2.2 A Symmetrical Miller CMOS OTA with High Speed Previous Miller CMOS OAT has a high open-loop gain but a low driving capability of current and limited setting time due to the low bias current. An alternative op-amp with higher driving capability is shown in Fig. 4.15, which is a three-stage symmetrical Miller CMOS OTA [49]. The design strategy can be found in reference [49]. Table 4.3 give the transistor sizes and the performance of the op-amp used by this thesis. The unity-gain frequency response is given in Fig. 4.16. This op-amp may also be used as an output amplifier.

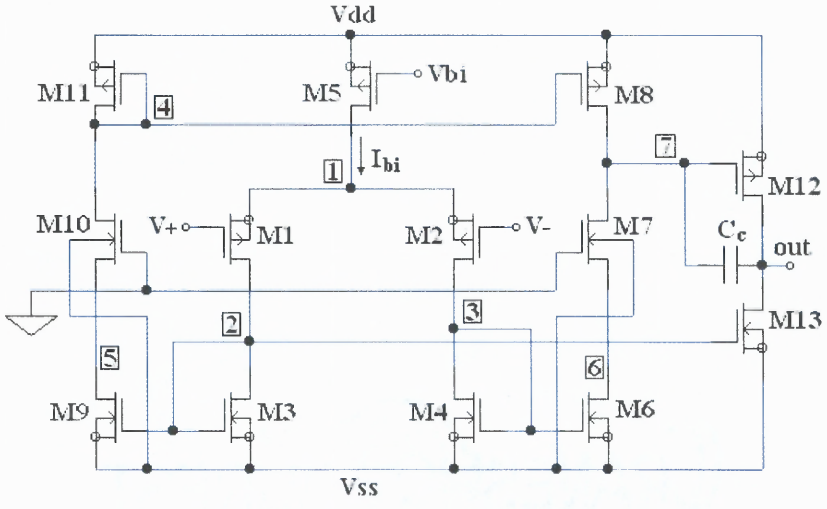


Figure 4.15 Schematic diagram of the symmetric Miller CMOS OTA

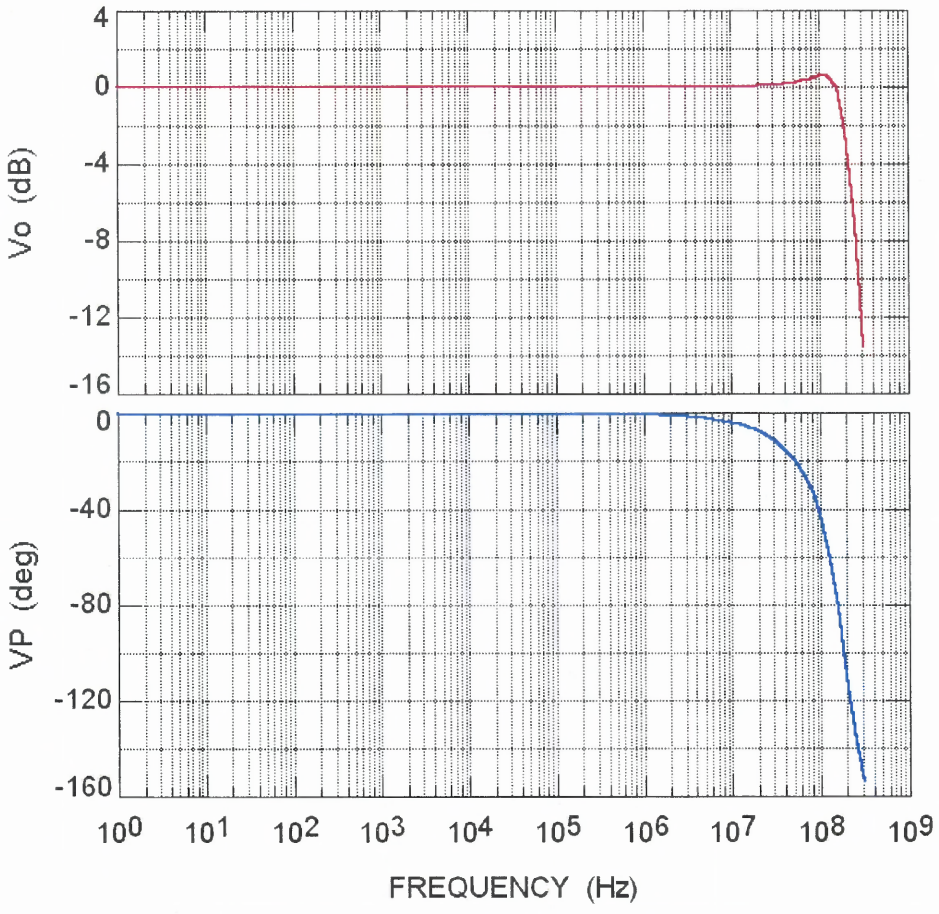


Figure 4.16 The frequency response of the unity-gain of the op-amp buffer

Table 4.3 Transistor sizes and the characteristics of the symmetric Miller CMOS OTA

MOST	P/N	W/L	g_m (μS)	g_o (μS)	I_{ds} (μA)	V_{gs}-V_{th} (V)	V_{sat} (V)	V_{gs} (V)	V_{th} (V)	C_c=0.5pF
M1	P	23.4/1.2	278	2.51	42.5	0.271	0.280	1.117	0.845	
M2	P	23.4/1.2	278	2.51	42.5	0.271	0.280	1.117	0.845	**Characteristics:**
M3	N	8.40/1.2	267	1.54	42.5	0.284	0.244	0.979	0.695	
M4	N	8.40/1.2	267	1.54	42.5	0.284	0.244	0.979	0.695	PM=56°
M5	P	11.1/0.6	325	49.7	84.0	0.423	0.401	1.230	0.807	A_o=2.1k
M6	N	11.1/0.9	495	20.6	84.0	0.296	0.254	0.979	0.683	f_{3dB}=65 kHz
M7	N	8.10/0.9	432	3.39	84.0	0.339	0.294	1.148	0.808	SR=170 MV/s
M8	P	19.8/0.9	409	6.61	84.0	0.369	0.363	1.208	0.839	GBW=130 MHz
M9	N	11.1/0.9	495	20.6	84.0	0.296	0.254	0.979	0.683	
M10	N	8.10/0.9	432	3.39	84.0	0.339	0.294	1.148	0.808	
M11	P	19.8/0.9	409	6.61	84.0	0.369	0.363	1.208	0.839	
M12	P	19.8/0.6	738	17.9	173	0.407	0.394	1.208	0.801	
M13	N	19.2/0.9	986	7.23	173	0.305	0.263	0.979	0.674	

4.3.3 SCI Circuit

The primary SCI circuit fabricated by the HP-0.5μm process technology is shown in Fig. 4.17. In this circuit, single n-channel MOSFETs are used as switches. The principle of the circuit was already described in Chapter 3. The effects of some non-ideal factors such as input node parasitic capacitance, the clock feedthrough, charge injection, the offset voltage, and the finite open-loop gain of the op-amp were also discussed in Chapter 3.

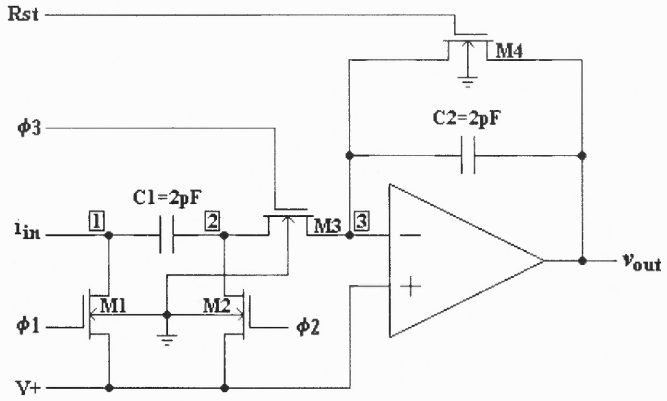


Figure 4.17 Schematic diagram of the SCI circuit

As discussed in Chapter 3, this SCI circuit can operate in several modes. Fig. 4.18 shows the simulation result of the SCI operating in PSI mode. In this simulation, the small signal is modulated and initially input to SCI in transfer integration phase and blocked in direct integration phase until 25 cycles are finished. After 25 cycles (5 ms in the figure) of integration, the signal was re-guided to SCI in the direct integration phase and blocked in the transfer integration phase. Thus, the signal is integrated in two opposite directions and can be isolated from fixed pattern by using a differential method. If single cycle integration were used for the readout, the integrator would have been saturated in 0.3 ms.

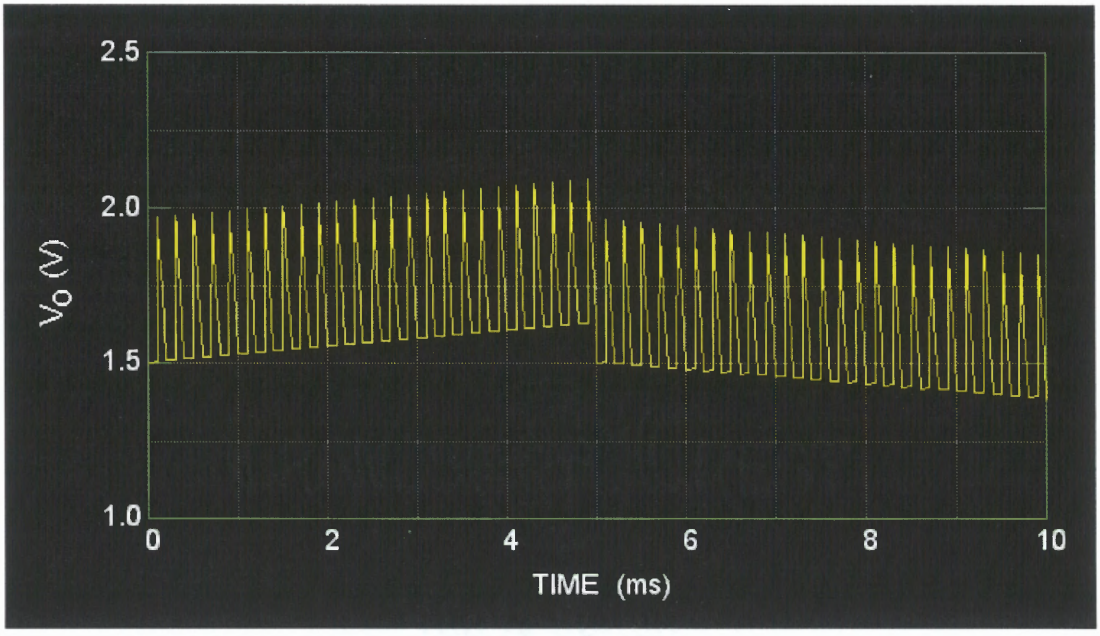
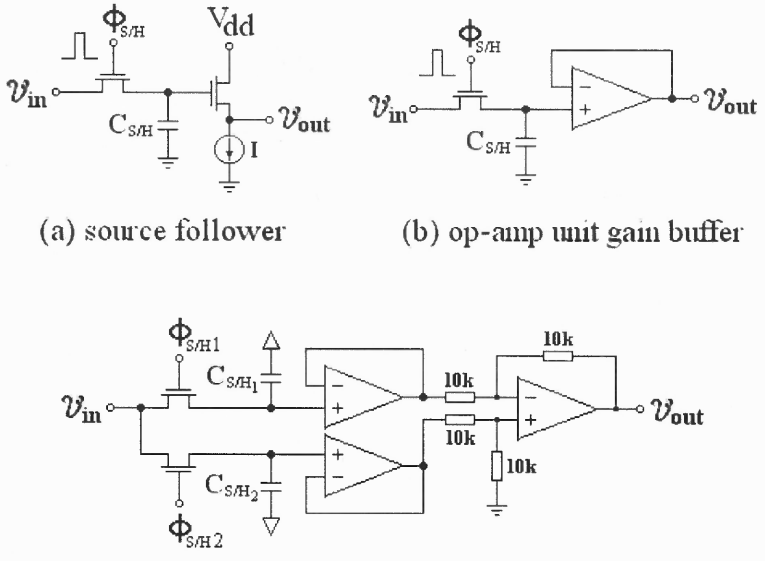


Figure 4.18 Simulation result of SCI

4.4 Sample & Hold or Averaging Circuit

In FPA, the signal from every pixel needs to be transferred to the output video cable. It is impossible for all the signals sampled to the video cable at same time. It is the sample & hold circuit that sample and keep the signals for later on transferring to the video cable one by one. A simplest S/H circuit could be composed of one sampling switch and a hold capacitor connected to a source follower (Fig. 4.19a) or a unit gain op-amp buffer (Fig. 4.19b) as show at Fig. 4.19. A narrow pulse is applied to the gate of the MOSFET, enabling the input gate to charge the capacitance $C_{S/H}$. The width of the narrow pulse should allow the capacitor to be fully charged before the switch is turned off. If the pulse is too narrow that the input voltage is just partially sampled, then this circuit becomes an exponential averager. Fig. 4.19(c) is a double sample and hold circuit with a differential amplifier as its output. These S/H circuits suffer from the clock feedthrough, charge

injection and the well-known kTC noise problems. However, due to its simplicity, it is still widely adopted in current FPAs. More complex design of S/H circuits dealing with charge injection and feedthrough can be found in reference [50,51].



(a) source follower (b) op-amp unit gain buffer

(c) double sample and hold circuit

Figure 4.19 Basic sample-and-hold circuitries

4.5 Shift Register

Shift registers are used in FPA's as a decoder to select each pixel's signal one by one and to feed it to the bus of output video. In this thesis, a shift register is designed for the 16×1 linear array. The Schematic diagram of the shift register is shown in Fig. 4.20. The shift register is composed of D flip flops which reset through a reset transistor per stage. A nor buffer gate is set in every stage to enhance the driving capability. The shift register starts by cleaning the output of multiplexer lines of S1 to S16, then triggered by the rising of a start pulse, followed is the logical high shifted from S1 to S2 per clock cycle then gradually to S16. Finally the end of shift (EOS) shows when S16 is reached. The

Synchronous pulse is designed to modify the width of S1 to S16, which will make the shift register suit for some applications, where both left and right shift registers are need on both side of a linear array.

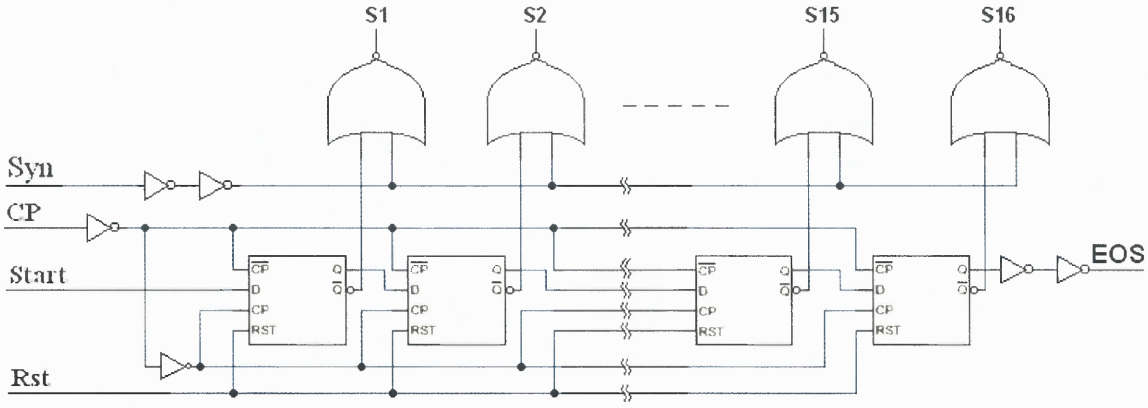


Figure 4.20 Schematic diagram of the shift register

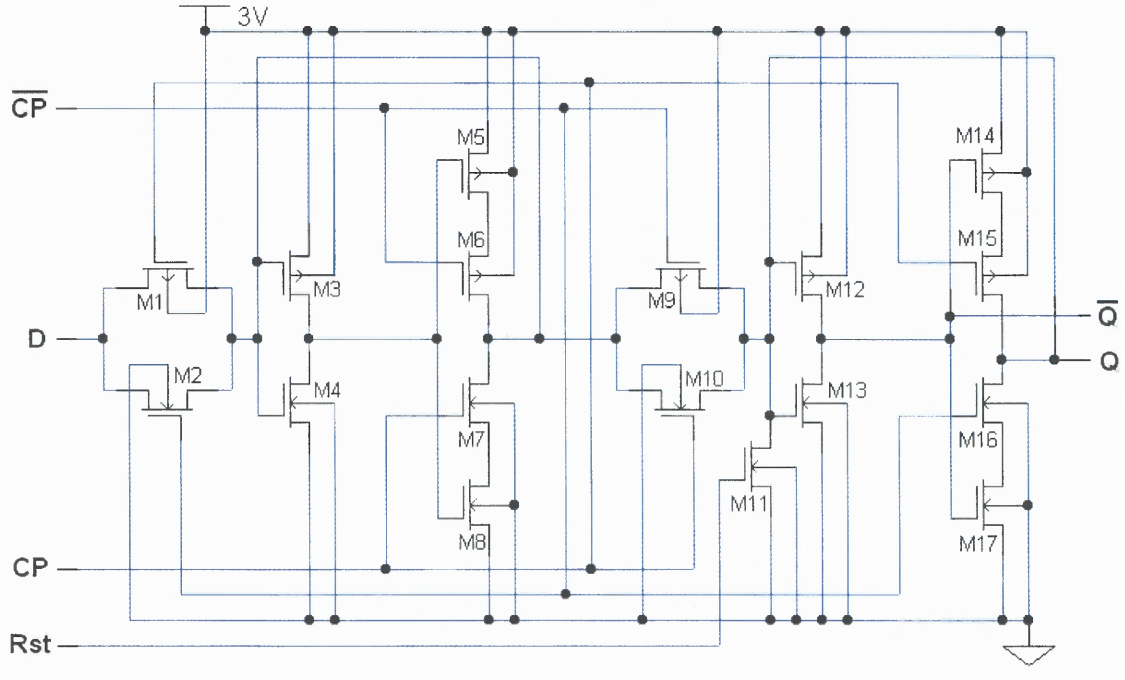


Figure 4.21 Schematic diagram of the D flip-flop

The Schematic diagram of a D flip flop is shown in Fig. 4.21. The circuit is composed of two dual inverters. The dual inverter stages provide a positive feedback signal to preserve the state of the input. The signal is passed from input to output with each change of the clock polarity. M13 is used for pre-cleaning.

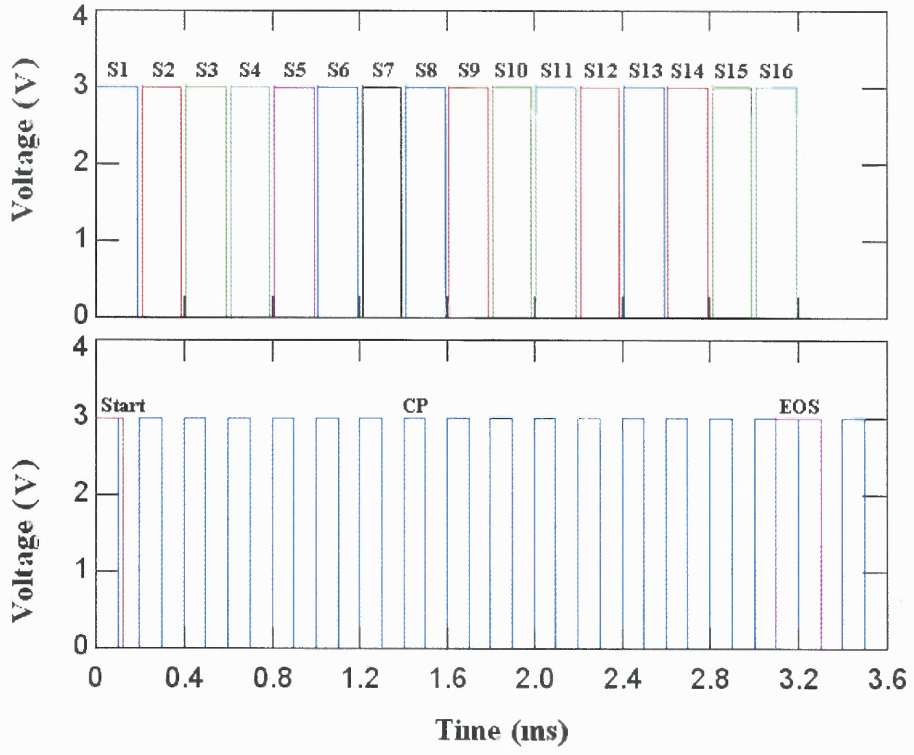


Figure 4.22 Simulation results of the shift register

The timing relationship among CP, Start, S1 to S16 and EOS are demonstrated in Fig. 4.22. The results of S1 to S16 should not be overlapped.

4.6 Linear Array of SCI

The linear array is composed of multiple SCIs, S/Hs, a column shift register and an output differential amplifier as shown in Fig. 4.23. In this linear array, the detector diode

array is bonded to the pads of the readout circuit. The signal induced current and/or the currents due to background or detector leakage are selectively integrated on the switched capacitor integrator according to the reference pulses of $\phi 1$, $\phi 2$ and $\phi 3$ in the purpose of performing background and leakage subtraction. The final multi-cycle integration signals are sampled to the sample/hold or average circuits controlled by pulses of S/H_1 and S/H_2. For every element, there are two sampled voltages that correspond to signal integrations with 180^{o} phase difference but keep same fixed pattern due to charge injection, feedthrough of switching or the offset of the op-amp. These two voltages will be passed to the output differential amplifier at the time that the element is selected by the shift register. Thus, the output video signals will only include the signals related to the modulated image.

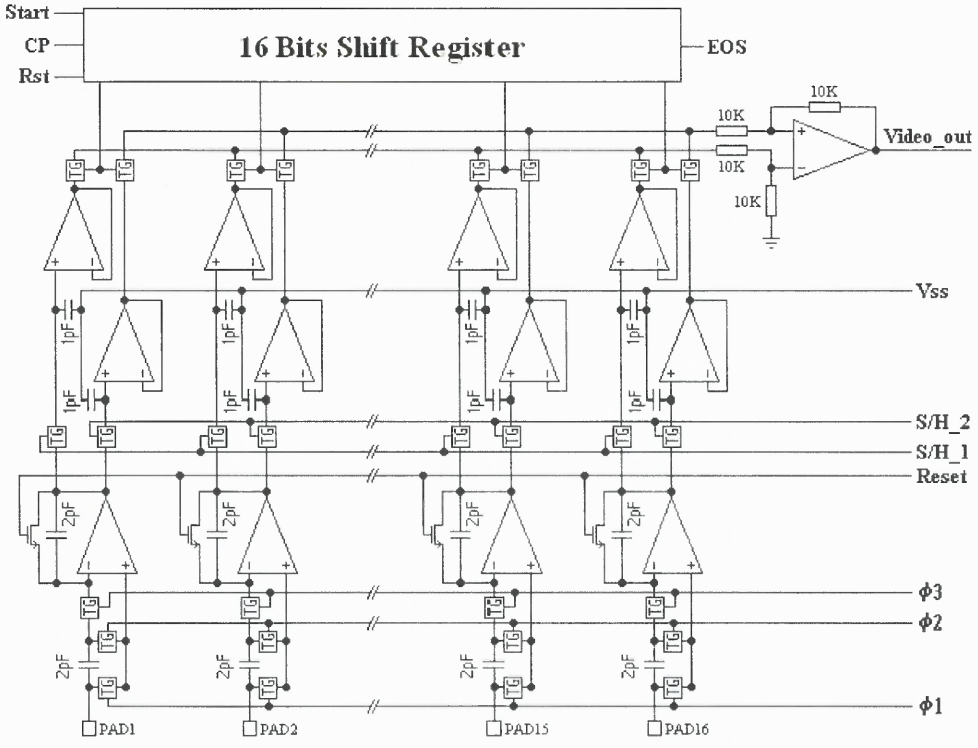


Figure 4.23 Block diagram of a linear array

4.7 Layout

Layout is the geometries of all the layers of masks representing the devices and circuits. The general rules to draw a layout is to try to get minimum layout area while following the design rules. A good way to construct a layout is to draw all the basic elements as different unit cells stored in a library with design rule and net-list checked (DRC & NLC). Then the layout of the functional circuits are constructed by using basic cells and also stored as unit functional cells in the library with DRC and NLC passed. Finally, the whole layout can be constructed step by step by using all the cells in the library.

Figure 4.24 shows the top layout of the chip designed by the author of this dissertation based on HP-0.5μm CMOS Technology. In this layout there are several circuits. At the bottom is the SCI unit, which can be seen in detail in Fig. 4.25. In the middle is a 16 element linear array with S/H, shift register and correlated readout circuitries (CCTIA). In the middle of the top is a 21-stage oscillator used to test the speed of the transistor. There are other test circuits that are not discussed in this thesis. Besides the circuits, the pad construction satisfies the tiny PIN 40 package provided by MOSIS. The center-to-center distance between two successive pads is 70 μm and every input pad is designed with a simplified electrostatic discharge (ESD) protection by appending two pn diodes in the input with other terminals connected to the highest and lowest power sources.

Figure 4.25 shows the layout of a single SCI circuit, which takes a total area of around 100×100 μm^2. On the left and right bottom corners are the two capacitors. Between the two capacitors are N-MOSFET switches. Above them is the high-speed op-amp discussed in section 4.3.2.2.

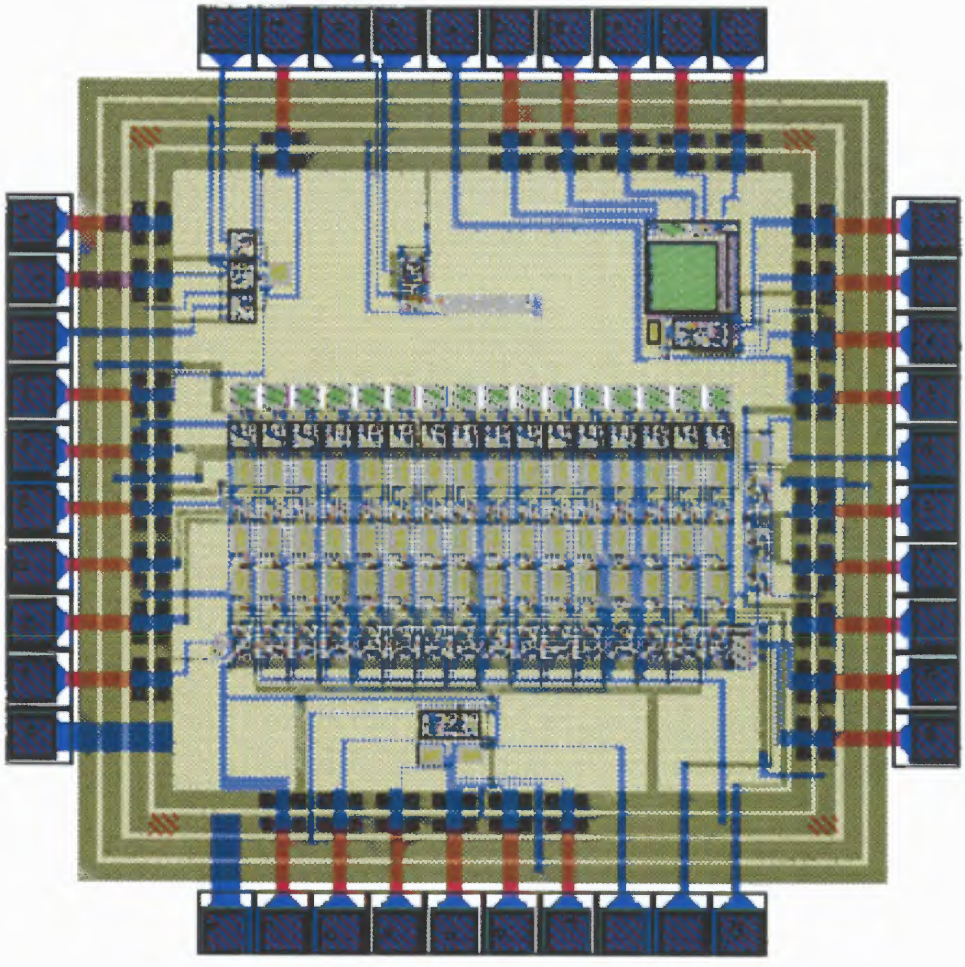


Figure 4.24 The layout of the chip

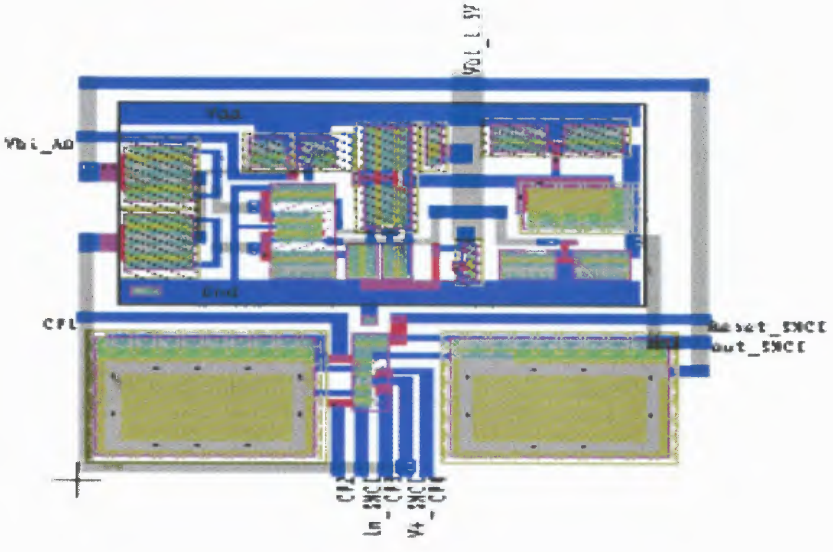


Figure 4.25 The layout of a SCI unit

The layout was designed in the early of 1999. At that time, the linear array was constructed with CCTIA interface. Hence, the design of the linear array with SCI interface is put in this thesis as a reference for further work.

4.8 Summation

In this chapter, some basic design issues associated with analog and digital CMOS readout circuits are addressed. A unit of SCI as a representative key component of GMCI and a linear array of SCI is presented. The fixed pattern due to charge injection, clock feedthrough and the offset voltage of a non-ideal op-amp is also emphasized. The simulations based on processing parameters seem encouraging.

CHAPTER 5

EXPERIMENTAL RESULTS

5.1 Introduction

Several criteria must be satisfied to measure the readout circuit. They are the appropriate biases and pulses for operating the chip, the generation of modulated signal, and the acquirement of the input data. Fortunately, there are standard bias and pulse generator systems specifically designed for FPA measurements. In this research, a Pulse Instrument Product, the 4000 Series Low Noise Focal Plane Array Test System, was used to generate biases and pulses for chip operation, controller of the modulated signal, and data acquisition. An oscilloscope was used to monitor the output of SCI. Both modulated electrical injection and optical injection under strong background were used as signal sources to test the chip. The primary results showed that the SCI can detector signal that was five orders less than background. The linearity of output signal versus the number of cycles m and the relationship between the output signal and its phase were also measured.

5.2 Experimental System

Figure 5.1 shows the block diagram of the test system based on the PI-4000. It consists of a PI-5800A Data Generator, a PI-4001 Control Mainframe, two PI-4002 Instrument Mainframe, one can generate a maximum of 16 channel pulses with voltage within ±20V, and one can provide a maximum of 16 channel DC biases with voltage within ±20V, one PI-4007 Preamplifier and one PI-4005 Acquisition Mainframe. The PI-5800A and PI-4001 are controlled through an IEEE-488 bus and the PI-4005 is controlled through an

EISA/VME bus for increased system speed. The other components are controlled through an internal bus among the various components of the instrument. This system can be operated by programming in a computer or by the soft key on the instrument panel. An Oscilloscope can monitor the pulses, biases and the video output from the readout circuit. The output of SCI can be the output of the integrator or the output of the differential amplifier.

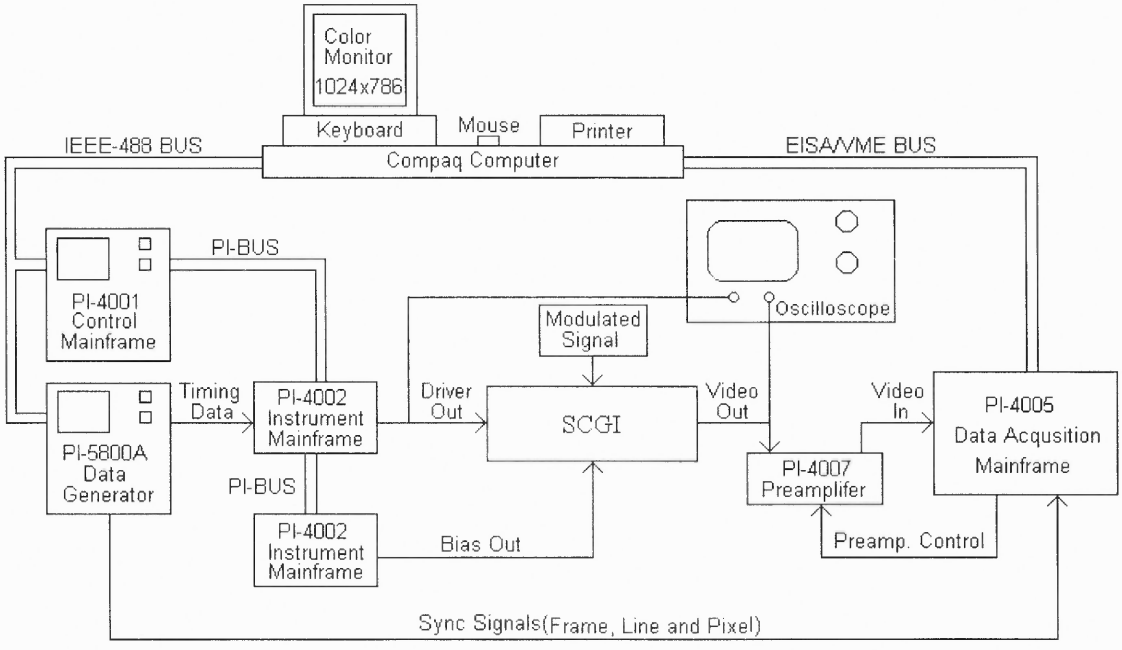


Figure 5.1 The PI-4001 measurement system

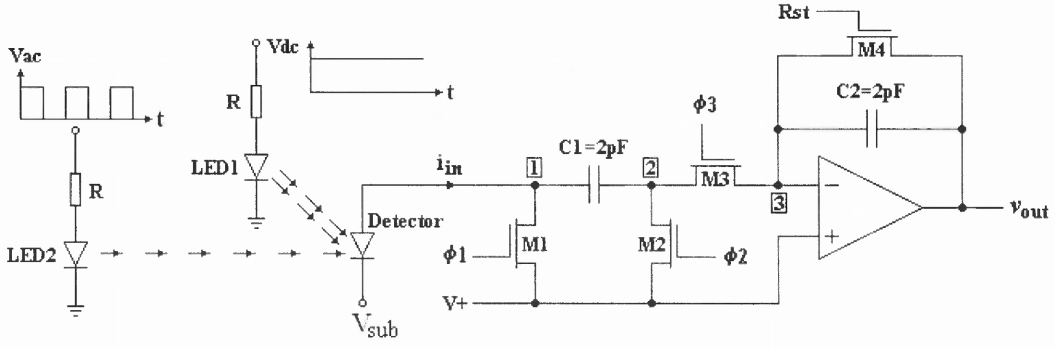
5.3 Signal Injection

The input of a readout circuit is the injecting current from the connected detector. When readout circuit is tested, the injecting current could be from a detector induced by a light source or a resistor biased with a voltage source. For the SCI circuit, two current sources

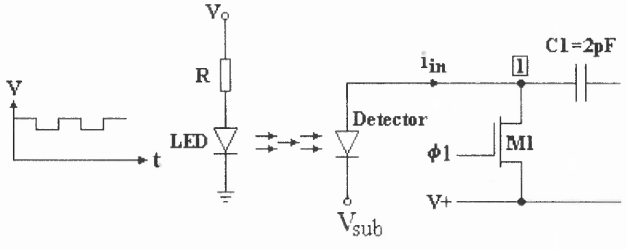
are needed in testing, one acting as the weak signal that is modulated, the other as the strong background that does not change with time.

5.3.1 Optical Injection

In the case of optical injection, a photodiode is reversely biased and connected to the readout circuit. The background radiation was created by a LED with DC forward bias. The modulated signal could be generated either by the same LED or another LED of the same characteristics. Part of the radiation from LED was received by the photodiode. The modulator of optical signal could be mechanically, optically, or electrically controlled. In this experiment, the signal LED was pulsed to generate repetitive signal by using the same PI-5800A. Fig. 5.2 illustrates the block diagram of the optical injection used by this experiment.



(a) Using two LEDs to generate modulated and unmodulated radiations



(b) Using same LED to generate modulated and unmodulated radiations

Figure 5.2 Optical injection

In the case of using the same LED, a small pulse is added to the DC bias of the LED. Assume the photo-induced current across the photodiode is proportional to the current passing through the LED. The forward current of the LED is given by

$$I = I_o \exp(\frac{V_{LED} - IR_{LED}}{nkT}) \tag{5.1}$$

where I_o is the reversed saturation current, V_{LED} is the voltage across the LED, R_{LED} is the parasitic resistance of the LED, n the pn junction ideality, k the Boltzmann's constant. With the current limit protection of resistor R, the current change due to the change of voltage is approximately given by

$$\Delta I = \frac{1}{R_{LED} + R} \Delta V \tag{5.2}$$

Hence, the signal to background radio can be estimated

$$\frac{i_s}{I_b} \approx \frac{\Delta I}{I} = \frac{\Delta V}{I(R_{LED} + R)} = \frac{\Delta VR}{(V - V_{LED})(R_{LED} + R)} \approx \frac{\Delta V}{V} \tag{5.3}$$

This method was first used to show the operation of the SCI circuit. It is hard, however, to get a big ratio of I_b/I_s.

By choosing two similar LED biased with same current, they are assumed to have similar radiation. The photon flux a diode receives from the two LEDs depends on the distances of the two LEDs away from the receiver. If the LEDs can be thought as point radiation sources, then the ratio of the photo-induced currents is given by

$$\frac{i_{s1}}{i_{s2}} = \left(\frac{r_2}{r_1}\right)^2 \tag{5.4}$$

If LED 2 is DC biased as a background and LED 1 is square wave pulsed with same amplitude and a duty of 0.5, then the ratio of signal current to background related current is

$$\frac{i_s}{I_b} = \frac{1}{2}\left(\frac{r_2}{r_1}\right)^2 \tag{5.5}$$

where the factor of two is from the modulation duty.

5.3.2 Electric Injection

Figure 5.3 illustrates the Schematic diagram of electric injection. In this structure, R3>R2»R1. From Appendix B, the background current is determined by

$$I_b = \frac{V_1 - V_+}{R_3} \tag{5.6}$$

And the signal current is

$$i_p = \frac{\Delta V_2 R_1}{(V_1 - V_+)R_2} I_b = \frac{\Delta V_2 R_1}{R_2 R_3} \tag{5.7}$$

By taking R_1=1K, R_2=10M, R_3=50M, V_1=3V, and V_+=1.5V, then

$$\frac{i_p}{I_b} = 6.7 \times 10^{-5} \Delta V_2 \tag{5.8}$$

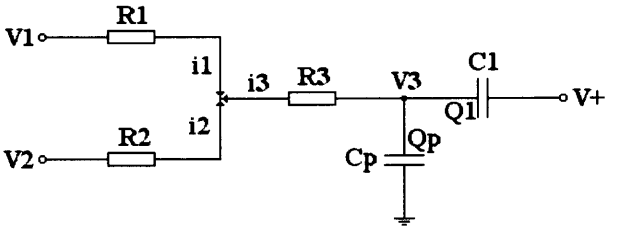


Figure 5.3 Electric injection

5.4 Output of Differential Signal with 180° Phase Difference

In order to get rid of fixed pattern noise due to multi-switching associated charge injection and feedthrough, the SCI circuit of Fig. 4.17 is connected to a CDS circuit of Fig. 4.19c, yielding the schematic diagram for the measurement of differential signals with 180° phase difference as depicted in Fig. 5.4. Both optical and electrical inputs are used for the measurement.

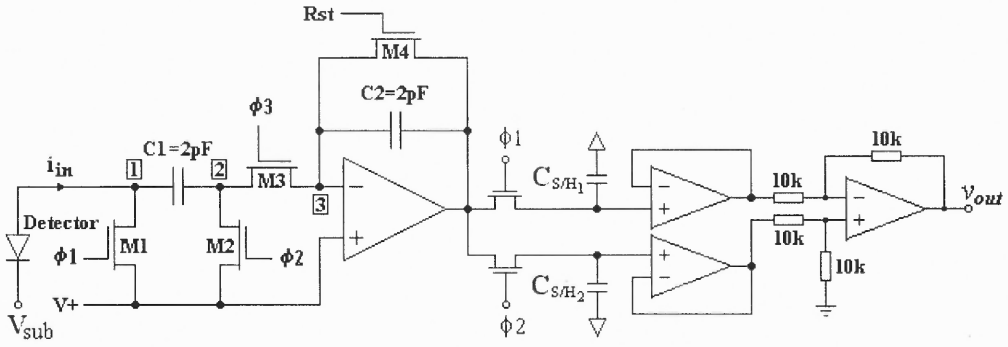


Figure 5.4 The schematic diagram used for measuring differential signals

As discussed in Chapter 3, the normal output of SCI usually includes two terms; one is related to the modulated image signal, and the other is a fixed pattern associated with the offset voltage of the operational amplifier. Generally, the fixed pattern may include other sources such as charge injection and clock feedthrough due to switching. Hence, when the correlated image signal is fed through the transfer integration phase, (3.23b) can be rewrite to a general form

$$V_{os1} = A_o V_s \left[1 - (1 - \frac{C1}{A_o C2})^m \right] + V_{FPN} \tag{5.9}$$

where V_{FPN} is a voltage related to fixed pattern noise. It is a function of the number of cycles, m. V_s is a voltage related to signal i_s and is given by (3.21). When the signal is fed through direct integration phase, then the output is

$$V_{os2} = -A_o V_s \left[1 - (1 - \frac{C1}{A_o C2})^m \right] + V_{FPN} \tag{5.10}$$

By subtracting (5.10) from (5.9), again, the differential output is

$$V_{os} = A_o V_s \left[1 - (1 - \frac{C1}{A_o C2})^m \right] \tag{5.11}$$

which virtually eliminates all the fixed pattern noise. However, this differential output usually does not have a linear relationship with m. When $A_oC_2 \gg C_1$, (5.11) becomes

$$V_{os} = \eta \frac{i_s \tau m}{C2} \tag{5.12}$$

which is proportional to the total integration time. Obviously, a high open-loop gain of the op-amp is required to obtain a better linear relationship between the differential output of the SCI and the cycle number.

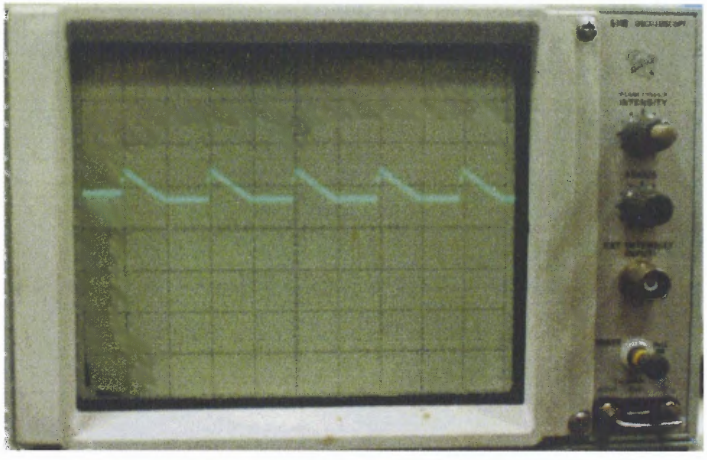
5.5 Experimental Results

Both optical and electric injections are used to generate small signal under strong background. All the pulses and biases are obtained from the 4000 series low noise focal plane array test system.

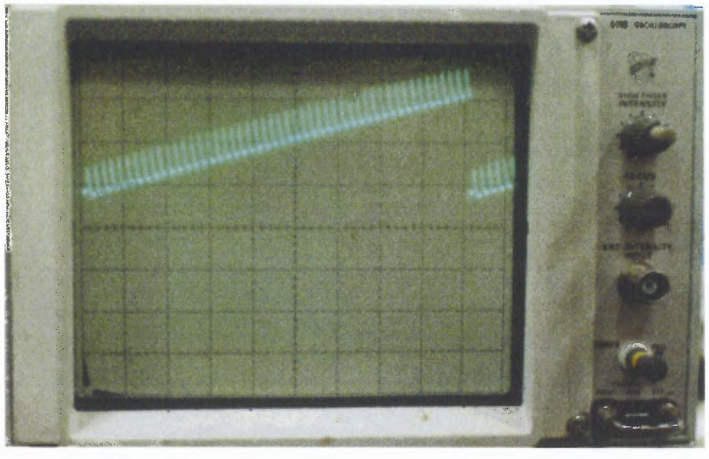
5.5.1 Zigzag Output of SCI

Figure 5.5 shows the zigzag outputs of the SCI measured from a fabricated chip traced by an oscilloscope. In Fig. 5.5a, the transfer integration is corresponding to the horizontal line ended by the jump to a higher level. Followed by the direct integration with a slope

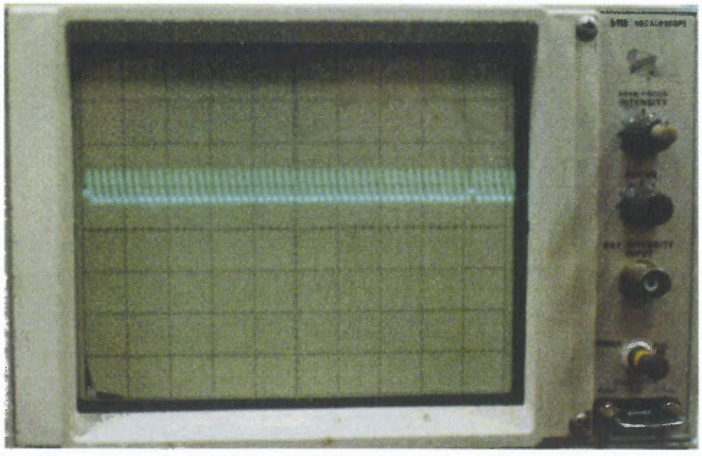
going down. Then it comes the transfer integration again. Fig. 5.5b to Fig. 5.5d indicates a 50 cycles of integration with background subtraction. The small signal is integrated during transfer integration phase in Fig. 5.5b, during direct integration phase in Fig. 5.5d. There is no signal but background input in Fig. 5.5c. The larger background related current in all the cases in Fig. 5.5 is positively fed to the input of the switched-capacitor integrator.



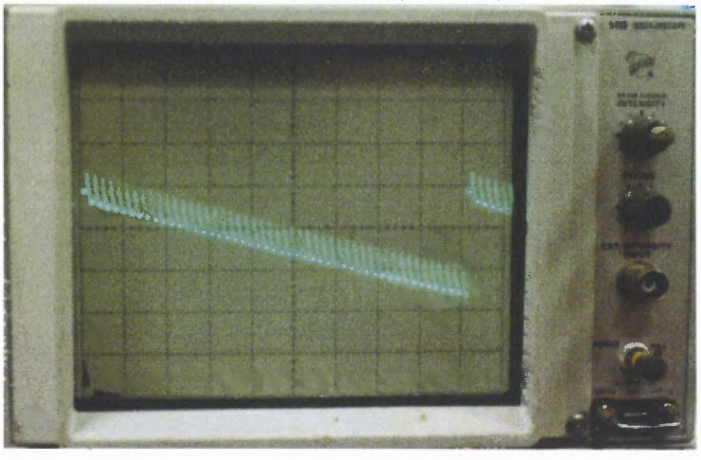
(a) Transfer and direct integrations under positive DC input (x:10μs/div, y:0.5V/div)



(b) Small signal is captured in transfer integration (x:50μs/div, y:0.5V/div)



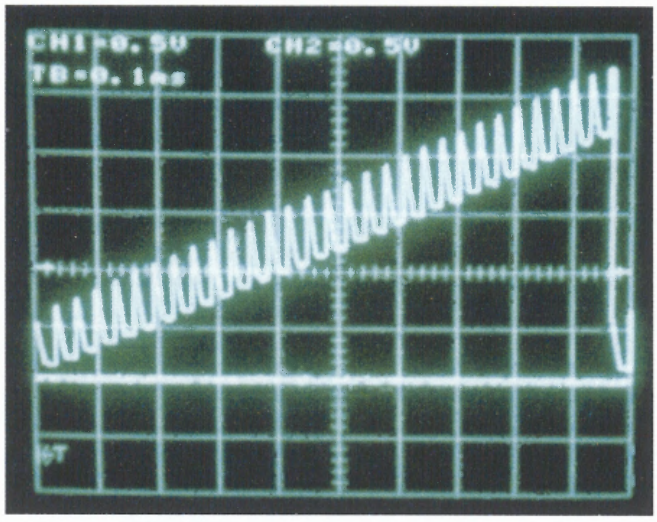
(c) No signal is input (x:50μs/div, y:0.5V/div)



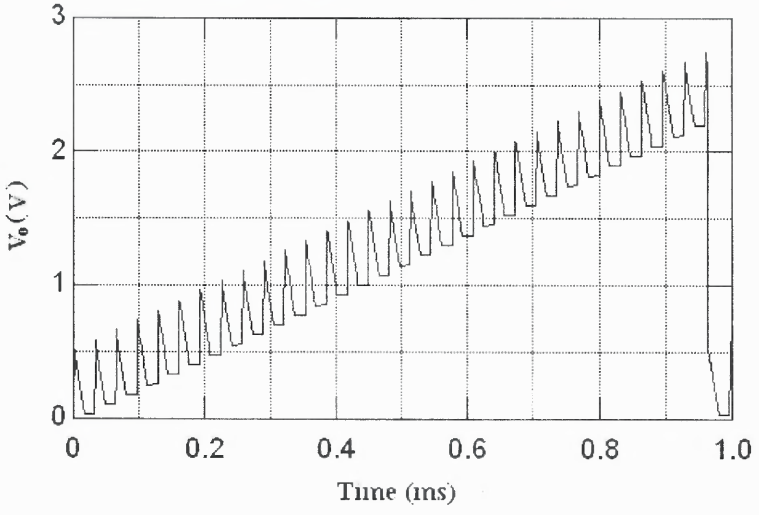
(d) Small signal is captured in the direct integration (x:50μs/div, y:0.5V/div)

Figure 5.5 Zigzag outputs of SCI with background subtraction

Figure 5.6 compares the experiment result with computer simulation. The small signal is captured in transfer integration phase. The background is cancelled out in two successive integration phases, otherwise, it will saturate the circuit in 0.1 ms. With 30 cycles, a total time of 0.96 ms is used for integration. Fig. 5.6a is the zigzag outputs of the experimental record while Fig. 5.6b is the simulated result computed by TopSPICE. They match very well.



(a) Measured (x: 0.1ms/div, y: 0.5V/div)



(b) Simulated

Figure 5.6 Experiment and simulation results of the zigzag outputs of the SCI

Figure 5.7 shows the zigzag output under input signals with 180° phase difference. The signal is input in transfer integration phase for the first 30 cycles. Followed 30 cycles is the signal fed in direct integration phase. By sample and hold circuit followed by the differential amplifier as shown in Fig. 5.4, the differential output can be obtained, which virtually eliminate the fixed pattern noise due to switching and the finite gain of the op-amp.

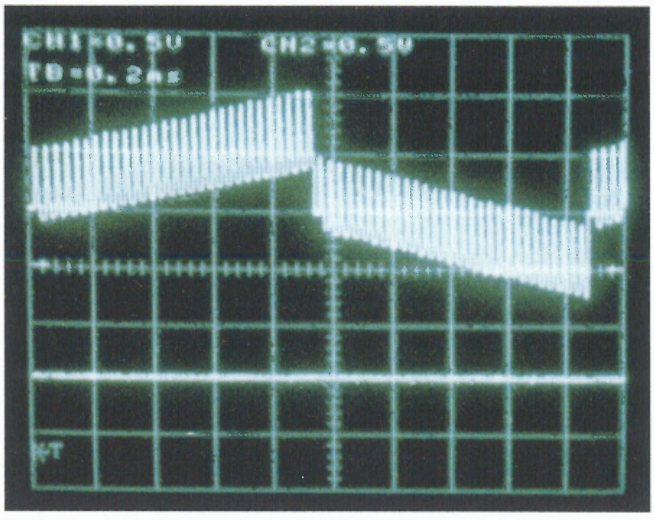


Figure 5.7 The output of SCI under input signals with 180° phase difference

5.5.2 Linearity

Figure 5.8 shows the differential output as a function of the number of the cycles. The squares represent measured data. The solid line is described by (5.11). The linearity is mainly determined by the open-loop gain of the op-amp. The higher the open-loop gain, the better the linearity between the differential output and the cycle number. However, for a fixed cycle number, the linearity of the differential output with the strength of signal is quite good as demonstrated by Fig. 5.9. In the figure, 2000 total cycles were used to accumulate the extremely weak signal buried in strong background. Signal that was 5 orders less than background were measured in both optical and electric injections.

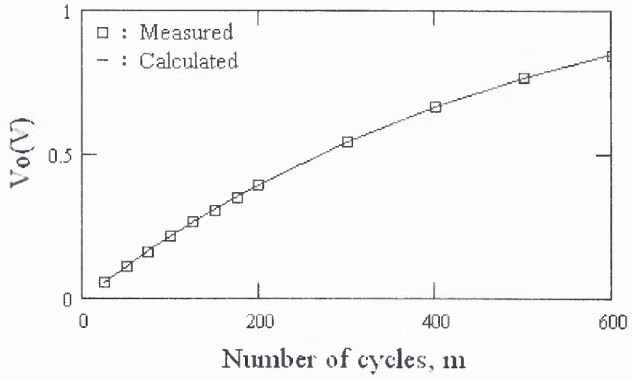


Figure 5.8 The differential output as a function of cycle number

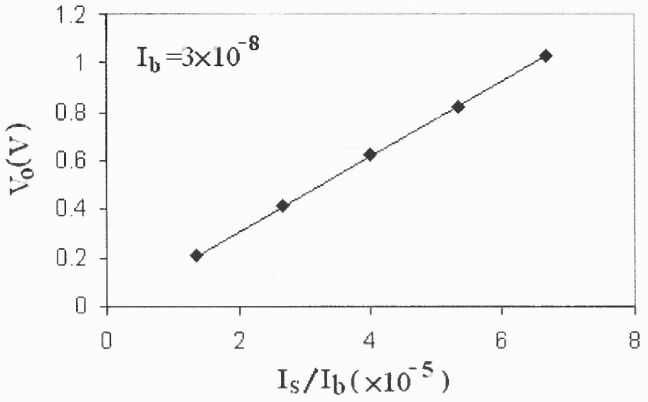


Figure 5.9 Measured differential output vs. input signal

5.6 Conclusions

In this chapter, the experimental results were presented and compared with simulation results. The quite fitted results between experiment and simulation shows the calculation is reasonable. It demonstrated the feasibility of the switched-capacitor integrator (SCI) as a readout circuit to perform the function of the gated multi-cycle integration (GMCI) of a MIFPA.

CHAPTER 6

CONCLUSIONS AND FURTHER WORK

6.1 Summation

To develop a new focal plane array for pulse-induced or repetitive images is a new attempt to find the potential application of FPA in the fields of biosciences. The general model and theory of GMCI have been successfully developed. It consists of basically a demodulator, an integrator, and possibly an averager. It can integrate the signal as well as background when signal is presented, and block or integrate reversely when signal is absented or reversed. GMCI can operate either with background subtraction (that is the phase-sensitive integration) or without background subtraction (that is the gated integration). It can also perform multi-point summation and multi-sample averaging. GMCI is specifically developed for FPA dealing with extremely weak repetitive or modulated images buried in strong backgrounds.

The theory of GMCI is successfully developed in terms of the merits of FPA based on the given model. Several operational modes of GMCI are analyzed and compared. The main features of GMCI are summarized as following.

GMCI can perform multiple integration modes; these modes include conventional single integration such as CTIA, gated integration with multipoint summation and/or multi-sample averaging, and phase sensitive integration, which intrinsically has background subtraction with or without multi-sample averaging.

Although the theory of GMCI is specifically developed for FPA of array detectors dealing with modulated images, it is also suited for single detector measurement. Thus,

the analytic theory of GMCI somehow unifies the theories of gated integration, multi-point summation, multi-sample averaging, and phase sensitive detection (lock-in amplifier). This will be much helpful to build instrument with multiple operational modes towards the "smart" generation of FPA.

Universally, improvement in measurement, imaging sensitivity or dynamic range is resulting from increased total measurement or total integration time, as in the GMCI. The purpose of the multi-point summation and averaging is to increase the total integration time, yielding an improvement in the performance of the measurement or image. Any other processing time should be as short as possible or as parallel to the integration time as possible for the purpose of efficiency.

The transmission functions of GI FPAs and all other conventional FPAs, whether with or without off-chip summation or averaging, is analogous to a low- pass filter. An FPA operated in PSI mode is analogous to a band-pass filter centered mainly at the modulation frequency. An apparent advantage of PSI lies in its capability of suppressing the flicker or 1/f noise, which, among all the noise sources, is usually important, and even dominant for many detectors, such as HgCdTe IR photodetectors. Besides 1/f noise, other low frequency noises may also play important roles.

The input-referred bandwidth of GMCI is determined by the total integration time, which is$1/2T^{i}$. The multiple summation and/or averaging and/or combination with background subtraction, are used to increase the total integration time, thus, to narrow the bandwidth, and subsequently to improve the sensitivity of the measurement or image.

The multiple summation is used to increase the integration time, however, the total integration time is still limited by the capacity of the storage well of the integrator,

thus, the total number of summation is limited. Nevertheless, by using multi-point summation, a single integration that is not optimized can be optimized to multiple-integration. The multi-point summation increases the signal by a factor of *m* (the number of points for summation), while it increases the noise only by a factor of the square root of *m*. Thus, it improves the SNR by a factor of the square root of *m*. Multi-point summation is meaningful when dealing with a short lived, small repetitive signal that otherwise would be swamped out by the least significant bit (LSB) of the A-to-D converter.

The multi-sample averaging technique keeps the signal unchanged, but reduces the noise by a factor of square root of *n* (the number of samples for averaging). The performance of multi-sample averaging appears to enhance the storage capacity by a factor of the number of samples. Thus, the merits of the FPA are improved by the square root of the sample number. And this number is not limited by the FPA itself but by the maximum frame rate the circuit can provide and by the maximum measurement time you can endure. Thus, multi-sample averaging can be used to extend the storage capacity of the integrators. Consequently, multi-frame averaging can breakthrough the limit performance of a camera based on one frame image, given that the source of image does not change with time and the image signal is above the LSB of the ADC.

Strong background and/or a large dark current will reduce the performance of conventional FPAs. With background subtraction, PSI can dramatically improve the performance of FPAs. First, the storage well is almost exclusively used for signal integration. The optimal integration time is improved by a factor of the ratio of background current to signal current. Second, the SNR is improved by a factor of the

square root of the ratio of background current to signal current. Third, sensitivity, such as the minimum detectable signal and the optimal noise equivalent temperature difference, is improved by a factor of the square root of total electron numbers that a pixel handles in imaging. Thus, FPA operated in SPI mode is specifically useful in dealing with a repetitive weak image buried in a strong background.

As a version of GMCI, the switched-capacitor integrator (SCI) was successfully proposed, designed, fabricated, and measured. Theoretical analysis and experimental result shows the feasibility of SCI as a candidate of GMCI detecting an extremely weak image signal buried in a strong background.

6.2 Further Researches

It has been successfully demonstrated the feasibility of the gated multi-cycle integration for repetitive imaging both in theory and experiment. A better understanding should be done before a staring MIFPA is fabricated. The suggested further research topics are

1. The noise feature of the SCI circuitry
2. The fabrication of linear array of SCIs and its application in biosciences
3. A simplified version of GMCI for 2-dimentional staring arrays
4. The application of GMCI for gated camera

6.3 Conclusions

The contributions of this dissertation are:

1. Development of the concept of multi-cycle integration focal plane array
2. Successful construction of the general model of GMCI and its theory

3. Presentation of a unified analytic theory that enhances the behaviors of gated integration, phase-sensitive detection, multiple summation and averaging
4. Proposition, analysis, design, and experimental demonstration of a version of GMCI, the switched-capacitor integrator that can perform multi-cycle integration with or without background subtraction
5. Experimental demonstration of the main feature of GMCI–its capability of handling strong background

APPENDIX A

PROCESSING PARAMETERS FROM HP-0.5μm TECHNIQUE

Mosis Parametric Test Results

RUN: N91X VENDOR: HP-NID
TECHNOLOGY: SCN05H FEATURE SIZE: 0.5 microns
INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.
COMMENTS: SMN3MLC06

TRANSISTOR PARAMETERS:	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM:	0.9/0.60			
Vth:	0.73	-0.86		Volts
SHORT:	15/0.60			
Idss:		344	-173	uA/um
Vth:		0.64	-0.88	Volts
Vpt:		10.0	-10.0	Volts
WIDE:	15/0.60		-10.0	Volts
Ids0:		0.6	-0.1	pA/um
LARGE:	5.4/5.4			
Vth:		0.70	-0.89	Volts
Vjbkd:		11.5	-9.8	Volts
Ijlk:		-28.8	-5.3	pA
Gamma:		0.66	0.45	V^0.5
K' (Uo*Cox/2):		76.3	-25.4	uA/V^2

COMMENTS: Poly bias varies with design technology. To account for mask and etch bias use the appropriate value for the parameter XL in your

SPICE model card.

Design Technology	XL
---	---
SCN_SUBM (lambda=0.30), CMOSH,	
HP_CMOS14TB	-0.10
SCN (lambda=0.35)	-0.20

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth:	Poly	>15.0	<-15.0	Volts

PROCESS PARAMETERS	N+ACTV	P+ACTV	POLY	MTL1	MTL2	MTL3	UNITs
Sheet Resistance:	2.9	2.4	2.4	0.07	0.07	0.05	ohms/sq
Width Variation:			-0.05	0.17	0.11	-0.36	microns

				(measured - drawn)		
Contact Resistance:	2.3	2.0	1.8	0.55	0.53	ohms
Gate Oxide Thickness:	95	angstroms				

CAPACITANCE PARAMETERS	N+ACTV	P+ACTV	POLY	MTL1	MTL2	MTL3	N_WELL	UNITS
Area (substrate)	464	924	93	27	11	9	90	aF/um^2
Area (N+active)			3618					aF/um^2
Area (P+active)			3452					aF/um^2
Area (poly)				58	18	11		aF/um^2
Area (metal1)					44	16		aF/um^2
Area (metal2)						47		aF/um^2
Area (cap well)			2215					aF/um^2
Fringe (substrate)	350	210						aF/um
Overlap (N+active)			246					aF/um
Overlap (P+active)			257					aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	1.32	Volts
Vinv	1.5	1.46	Volts
Vol (100 uA)	2.0	0.25	Volts
Voh (100 uA)	2.0	2.99	Volts
Vinv	2.0	1.55	Volts
Gain	2.0	-19.71	

	Ring Oscillator Freq.
DIV4 (31-stage, 3.3V)	131.13 MHz
	Ring Oscillator Power
DIV4 (31-stage, 3.3V)	7.10 uW/MHz/g

COMMENTS: SUBMICRON

N91X SPICE BSIM3 VERSION 3.1 (HSPICE Level 49) PARAMETERS
* DATE: Mar 22/99
* LOT: n91x WAF: 803
* Temperature_parameters=Default

.MODEL CMOSN NMOS (				LEVEL	= 49
+VERSION	= 3.1	TNOM	= 27	TOX	= 9.5E-9
+XJ	= 1.5E-7	NCH	= 1.7E17	VTH0	= 0.6627693
+K1	= 0.7615468	K2	= -0.0209294	K3	= 25.5980319
+K3B	= 4.1033147	W0	= 7.55976E-6	NLX	= 1E-9
+DVT0W	= 0	DVT1W	= 5.3E6	DVT2W	= -0.032
+DVT0	= 16.7040008	DVT1	= 0.7965223	DVT2	= -0.0532065
+U0	= 448.996411	UA	= 8.1904E-11	UB	=2.10990E-18
+UC	= 6.9605E-11	VSAT	= 1.581766E5	A0	= 0.9324122
+AGS	= 0.2267987	B0	= 1.22110E-6	B1	= 5E-6
+KETA	= -0.0125031	A1	= 0	A2	= 1
+RDSW	= 1.017989E3	PRWG	= 0.1061268	PRWB	= -9.56082E-4

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+WR      = 1            WINT     = 2.32171E-7  LINT     = 4.04090E-8
+XL      = -1E-7        XW       = 0           DWG      = -1.55575E-8
+DWB     = 8.83151E-9   VOFF     = -0.1082101  NFACTOR  = 2
+CIT     = 0            CDSC     = 1.21650E-4  CDSCD    = 0
+CDSCB   = 0            ETA0     = 5.80931E-5  ETAB     = -0.0698897
+DSUB    = 0.5269133    PCLM     = 0.586676    PDIBLC1  = 0.3656155
+PDIBLC2 = 8.29059E-4   PDIBLCB  = 0           DROUT    = 0.6493508
+PSCBE1  = 1.72996E10   PSCBE2   = 5.64974E-9  PVAG     = 0.3536189
+DELTA   = 0.01         MOBMOD   = 1           PRT      = 0
+UTE     = -1.5         KT1      = -0.11       KT1L     = 0
+KT2     = 0.022        UA1      = 4.31E-9     UB1      = -7.61E-18
+UC1     = -5.6E-11     AT       = 3.3E4       WL       = 0
+WLN     = 1            WW       = 0           WWN      = 1
+WWL     = 0            LL       = 0           LLN      = 1
+LW      = 0            LWN      = 1           LWL      = 0
+CAPMOD  = 2            XPART    = 0.4         CGDO     = 2.46E-10
+CGSO    = 2.46E-10     CGBO     = 0           CJ       = 5.00305E-4
+PB      = 0.99         MJ       = 0.8         CJSW     =4.39353E-10
+PBSW    = 0.99         MJSW     = 0.1         PVTH0    = 0.0146926
+PRDSW   = -90.261466   PK2      = 0.013714    WKETA    =-4.03674E-3
+LKETA   = 4.175605E-3  )

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.MODEL CMOSP PMOS                             LEVEL    = 49
+VERSION = 3.1         TNOM     = 27          TOX      = 9.5E-9
+XJ      = 1.5E-7      NCH      = 1.7E17      VTH0     = -0.8679312
+K1      = 0.3900362   K2       = 0.0171845   K3       = 33.1854557
+K3B     = -4.2227409  W0       = 6.91098E-6  NLX      = 2.35748E-8
+DVT0W   = 0           DVT1W    = 5.3E6       DVT2W    = -0.032
+DVT0    = 7.837227    DVT1     = 0.6993988   DVT2     = -0.0605442
+U0      = 172.453906  UA       = 6.9282E-10  UB       =1.96028E-18
+UC      = -3.644E-11  VSAT     = 1.556441E5  A0       = 0.8988824
+AGS     = 0.2602425   B0       = 3.54822E-6  B1       = 5E-6
+KETA    = -1.4924E-3  A1       = 0           A2       = 1
+RDSW    = 2.397929E3  PRWG     = -0.0268945  PRWB     = -0.0163463
+WR      = 1           WINT     = 2.14012E-7  LINT     = 1.12927E-9
+XL      = -1E-7       XW       = 0           DWG      = -2.31994E-8
+DWB     = 1.38930E-9  VOFF     = -0.119076   NFACTOR  = 2
+CIT     = 0           CDSC     = 1.41332E-4  CDSCD    = 0
+CDSCB   = 0           ETA0     = 0.9076168   ETAB     = -2.57421E-3
+DSUB    = 0.6489225   PCLM     = 6.0319793   PDIBLC1  = 0.0370098
+PDIBLC2 = 5.58821E-3  PDIBLCB  = 0           DROUT    = 9.98073E-4
+PSCBE1  = 1.59698E10  PSCBE2   = 1.03760E-8  PVAG     = 7.2923297
+DELTA   = 0.01        MOBMOD   = 1           PRT      = 0
+UTE     = -1.5        KT1      = -0.11       KT1L     = 0
```

```
+KT2      = 0.022          UA1      = 4.31E-9        UB1      = -7.61E-18
+UC1      = -5.6E-11       AT       = 3.3E4          WL       = 0
+WLN      = 1              WW       = 0              WWN      = 1
+WWL      = 0              LL       = 0              LLN      = 1
+LW       = 0              LWN      = 1              LWL      = 0
+CAPMOD   = 2              XPART    = 0.4            CGDO     = 2.57E-10
+CGSO     = 2.57E-10       CGBO     = 0              CJ       = 9.34151E-4
+PB       = 0.9393556      MJ       = 0.4775952      CJSW     =1.79232E-10
+PBSW     = 0.3006888      MJSW     = 0.1089545      PVTH0    = 4.43363E-3
+PRDSW    = -195.22559     PK2      = 3.89918E-3     WKETA    = 3.24787E-4
+LKETA    = -1.436449E-3   )
```

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APPENDIX B

ELECTRICAL INJECTION

The circuit employed to generate weak modulation current in the presence of large current is given in Fig.B1.

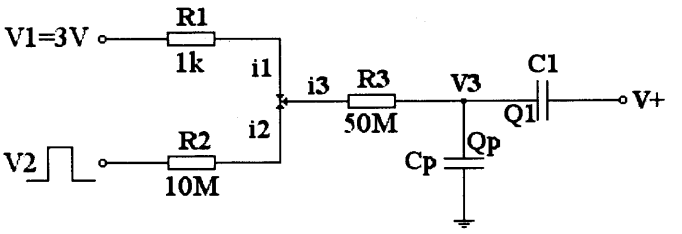

Figure B1 Schematic diagram of the circuitry for electrical injection

At t=0, V_3=V+. In node A, the following equation is satisfied

$$i_1 + i_2 + i_3 = 0 \tag{B.1}$$

or

$$\frac{V_1 - V_A}{R_1} + \frac{V_2 - V_A}{R_2} + \frac{V_3 - V_A}{R_3} = 0 \tag{B.2}$$

Therefore,

$$V_A = \frac{V_1 R_2 R_3 + V_2 R_3 R_1 + V_3 R_1 R_2}{R_1 R_2 + R_2 R_3 + R_3 R_1} \tag{B.3}$$

Let

$$Q = Q_i + Q_p \tag{B.4}$$

$$C = C_i + C_p \tag{B.5}$$

$$i_3 = -\frac{dQ}{dt} = \frac{V_3 - V_A}{R_3} = \frac{(V_3 - V_1)R_2 + (V_3 - V_2)R_1}{R_1 R_2 + R_2 R_3 + R_3 R_1} \tag{B.6}$$

From

$$Q = C_p V_3 + C_i (V_3 - V_+) \tag{B.7}$$

it is found

$$V_3 = \frac{Q}{C} + \frac{C_i}{C} V_+ \tag{B.8}$$

Substitute (B.8) into (B.6). The relationship between Q and t can be found, which is given by

$$\frac{dQ}{dt} + \frac{Q}{\tau} - i_0 = 0 \tag{B.9}$$

where

$$\tau = \frac{(R_1R_2 + R_2R_3 + R_3R_1)C}{R_1 + R_2} \tag{B.10}$$

$$i_0 = \frac{R_1V_2 + R_2V_1}{R_1R_2 + R_2R_3 + R_3R_1} - \frac{C_iV_+}{\tau} = \frac{CV_3^f - C_iV_+}{\tau} \tag{B.11}$$

where

$$V_3^f = \frac{R_1V_2 + R_2V_1}{R_1 + R_2} \tag{B.12}$$

which is the final stable voltage at node V_3. The solution of Q is given by

$$\begin{aligned} Q(t) &= i_0\tau(1 - e^{-\frac{t}{\tau}}) + C_pV_+e^{-\frac{t}{\tau}} \\ &= Q^f(1 - e^{-\frac{t}{\tau}}) + C_pV_+e^{-\frac{t}{\tau}} \\ &= C_pV_+ + C(V_3^f - V_+)(1 - e^{-\frac{t}{\tau}}) \end{aligned} \tag{B.13}$$

where

$$Q^f = i_0\tau = CV_3^f - C_iV_+ = C_pV_3^f + C_i(V_3^f - V_+) \tag{B.14}$$

which is the final charges stored at node 3. Substitute (B.13) into (B.8), then

$$V_3(t) = V_+ e^{-\frac{t}{\tau}} + V_3^f (1 - e^{-\frac{t}{\tau}}) = V_+ + (V_3^f - V_+)(1 - e^{-\frac{t}{\tau}}) \tag{B.15}$$

and

$$Q_i(t) = C_i(V_3 - V_+) = C_i(V_3^f - V_+)(1 - e^{-\frac{t}{\tau}}) \tag{B.16}$$

$$i_3(t) = -\frac{dQ}{dt} = \frac{C(V_+ - V_3^f)}{\tau} e^{-\frac{t}{\tau}} \tag{B.17}$$

$$i_{C_i}(t) = \frac{dQ_i}{dt} = \frac{C_i(V_3^f - V_+)}{\tau} e^{-\frac{t}{\tau}} \tag{B.18}$$

$$i_{C_p}(t) = \frac{dQ_p}{dt} = \frac{C_p(V_3^f - V_+)}{\tau} e^{-\frac{t}{\tau}} \tag{B.19}$$

The efficiency of the injection is given by

$$\eta = \frac{Q_i}{Q - C_p V_+} = \frac{i_{C_i}}{i_{C_i} + i_{C_p}} = \frac{C_i}{C_i + C_p} \tag{B.20}$$

and the average currents from t=0 to μ will be

$$\overline{i_3(\mu)} = \frac{1}{\mu}\int_0^{\mu} i_3(t)dt = \frac{C(V_+ - V_3^f)}{\mu}(1 - e^{-\frac{\mu}{\tau}}) \tag{B.21}$$

$$\overline{i_{C_i}(\mu)} = \frac{1}{\mu}\int_0^{\mu} i_{C_i}(t)dt = \frac{C_i(V_3^f - V_+)}{\mu}(1 - e^{-\frac{\mu}{\tau}}) \tag{B.22}$$

$$\overline{i_{C_p}(\mu)} = \frac{1}{\mu}\int_0^{\mu} i_{C_p}(t)dt = \frac{C_p(V_3^f - V_+)}{\mu}(1 - e^{-\frac{\mu}{\tau}}) \tag{B.23}$$

The change of output voltage due to Q_i is given by

$$\Delta V_0 = -\frac{Q_i(t)}{C_f} = \frac{C_i}{C_f}(V_+ - V_3^f)(1 - e^{-\frac{t}{\tau}}) \tag{B.24}$$

ΔV_o can be got from measurement. Thus, C and the parasitic capacitance can be found in the input port.

$$\tau = \frac{t}{\ln \frac{C_i(V_+ - V_3^f)}{C_i(V_+ - V_3^f) - C_f \Delta V_o}} \tag{B.25}$$

It is important to find the impact of the change of V_2 against other variables. First,

$$\frac{\partial V_3^f}{\partial V_2} = \frac{R_1}{R_1 + R_2} \tag{B.26}$$

Then,

$$\frac{\partial V_o}{\partial V_2} = -\frac{R_1 C_i}{(R_1 + R_2)C_f}(1 - e^{-\frac{t}{\tau}}) \tag{B.27}$$

$$\frac{\partial i_3}{\partial V_2} = -\frac{R_1 C}{\tau(R_1 + R_2)} e^{-\frac{t}{\tau}} = -\frac{R_1}{R_1 R_2 + R_2 R_3 + R_3 R_1} e^{-\frac{t}{\tau}} \tag{B.28}$$

$$\frac{\partial i_{C_i}}{\partial V_2} = -\frac{R_1 C_i}{\tau(R_1 + R_2)} e^{-\frac{t}{\tau}} = -\frac{R_1 C_i}{(R_1 R_2 + R_2 R_3 + R_3 R_1)C} e^{-\frac{t}{\tau}} \tag{B.29}$$

$$\frac{\partial Q_i}{\partial V_2} = -\frac{R_1 C_i}{(R_1 + R_2)}(1 - e^{-\frac{t}{\tau}}) \tag{B.30}$$

The ratios of the difference of the injected currents due to the change of V_2 and the currents are derived as

$$\frac{\Delta i_3}{i_3}\Big|_{\Delta V_2} = -\frac{\Delta i_{C_i}}{i_3}\Big|_{\Delta V_2} = \frac{R_1 \Delta V_2}{(R_1 + R_2)(V_+ - V_3^f)} \tag{B.31}$$

Special case: $R_1 << R_2 < R_3$. In this case

$$\tau \approx R_3 C \tag{B.32}$$

$$i_0 \approx \frac{V_+ - V_1}{R_3} \tag{B.33}$$

$$V_3^f \approx V_1 \tag{B.34}$$

$$\tau = \frac{\mu}{\ln \frac{C_i(V_+ - V_3^f)}{C_i(V_+ - V_3^f) - C_f \Delta V_o}} \tag{B.35}$$

$$\frac{\Delta i_3}{i_3}\Big|_{\Delta V_2} = \frac{\Delta V_2 R_1}{(V_+ - V_1)R_2} \tag{B.36}$$

$$V_s = N\frac{\partial V_o}{\partial V_2}\Delta V_2 = N\Delta V_2 \frac{R_1}{R_2}(1 - e^{-\frac{\mu}{\tau}}) \tag{37}$$

From the experiment, R_1=1kΩ, R_2=10MΩ, R_3=50MΩ, V_1=3V, V_2=3V, ΔV_2=-0.2V, V_+=1.5V, $\Delta V_o(\mu)$=-0.6V, μ=0.1ms. ΔV_s=0.16V, C_f=C_i=2pF, μ_s=38ms. Hence

$$\frac{\Delta i_3}{i_3}\Big|_{\Delta V_2} = \frac{\Delta V_2 R_1}{(V_+ - V_1)R_2} = 1.3\times 10^{-5}$$

$$i_0 = -3\times 10^{-8} A$$

$$\tau = 2\times 10^{-4} s$$

$$C_p = 2pF$$

$$\bar{i}_3 = 2.4\times 10^{-8} A$$

$$\bar{i}_{C_i} = 1.2\times 10^{-8} A$$

$$\eta = 0.5$$

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