ABSTRACT

BROADBAND WHOLE PACKAGE FDTD SIMULATION

by

Shenjun (Peter) Li

Whole package analysis is becoming more and more important with the rapid expansion of high frequency electronics. The motivation of this thesis is to find and implement a new method for broadband whole package simulation. 3-dimension (3-D) whole package Finite Difference Time Domain (FDTD) simulation result was first reported in detail in this thesis.

The FDTD method is a widely used full-wave time-domain simulation method used in the design and analysis for electromagnetic (EM) systems, such as antennas, wave propagating, and microwave circuits. Absorbing boundary condition (ABC), such as the perfect matched layer (PML) method, makes it possible to accurately analyze an EM structure involving complicated wave propagation in three-dimensional domain. Instead of running simulation at each frequency, time-domain solution gives complete frequency-domain response including coupling and dispersion effects. Chapter2 introduces the principle of FDTD and two important boundary condition methods. It also discusses the nonuniform grid numerical error, and gives the FDTD simulation and theoretical result.

Flip chip package is one of the most important package types. Chapter 3 presents a wide band approach for characterizing multiple flip chip interconnects by the FDTD method. Detailed analysis for electrical performance for frequencies up to 40 GHz has been performed with variations of interconnect bumps (ball cross section and via cross section). Flip chips of three sizes are studied using FDTD method in detail. The relationship between reflection loss, via pad length, ball cross-section and via cross

section is tabulated for future packaging design. Based on the simulation results, some design approaches are proposed for packaging structure operating at near 40 GHz.

FDTD whole package simulation method is introduced at the beginning of Chapter 4, followed by discussion how to implement this method to specific packages. The packages used to host circuit in chapter 4 are microstrip line and flip chip interconnects. The embedded circuits are ideal transmission line and an HP amplifier. Transient effects are observed when an amplifier is hosted in a package. Most of the simulations are processed under three-dimensional environment; two-dimensional simulation is used for reference standard. All these results were first reported by the author of this thesis and his collaborators.

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To my daughter Denice, my wife and my parents

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CHAPTER 1

OVERVIEW OF FDTD AND BROAD BAND PACKAGE SIMULATION

1.1 Introduction of Numerical Electromagnetic Modeling Techniques

Modeling of planar microwave structure has developed at an outstanding speed in the past decade. Current computer hardware and software technology makes it possible to implement algorithms based closer to the governing Maxwell equations of the EM system of interest. These algorithms have found widespread application in the areas of microwave devices and guiding structures, such as waveguides, resonators, junctions, microstrip, vias, interconnects, and transmission lines.

Computer methods for analyzing problems in EM generally fall into one of three categories, analytical techniques, numerical techniques, and expert systems. Their detailed definitions are as follows by Hubing [22].

Numerical techniques are the most accurate and important methods. They analyze the entire geometry which encloses the simulation domain as input. These numerical techniques can be broadly classified as frequency and time domain methods. The FDTD technique is a major time domain method. The FDTD method discretizes Maxwell's equations in space and time in a straightforward manner. FDTD results lend themselves well to scientific visualization methods since they tracks the time-varying fields throughout a volume of space. The FDTD method is a widely used full-wave time-domain simulation method used in the design and analysis for EM systems, such as antennas, wave propagating, and microwave circuits [50]. Berenger's PML method [5] makes it possible to accurately analyze an EM structure involving complicated wave propagation in three-dimensional domain. Instead of running simulation at each designs

frequency like a frequency-domain EM method, a time-domain solution gives full frequency-domain response up to the frequency of $1/(2\Delta t)$, where Δt is the minimum time difference. The response includes coupling and dispersion effects [49].

Finite difference frequency domain (FDFD) method and Method of Moments are frequency domain numerical techniques. FDFD technique results from a finite difference approximation of Maxwell's curl equations. In this case the time-harmonic versions of these equations are employed. Method of Moments uses basis and testing functions to discretize integral equations of electromagnetics. This numerical technique is based on weighted residuals method. It is not well-suited to the analysis of complex inhomogeneous geometries. The shortcoming for the frequency domain method is that one simulation can only obtain the system performance at one frequency. It should be run for numerous times if the system performance at different frequencies needs to be obtained.

Analytical techniques and expert systems are the other two computer methods for analyzing EM problems. Analytical techniques make simplifying assumptions about the geometry of a problem in order to apply a closed-form (or table look-up) solution. Expert systems estimate values for the parameters of interest based on a rules database. As system design and board layout procedures become more automated, analytical technique and expert system EM software will become more and more important.

1.2 Finite Difference Time Domain Technique

1.2.1 The Origin of FDTD

The Finite-Difference Time-Domain method, first proposed by Yee [57], is a simple and elegant way to discretize the differential form of Maxwell's equations. Maxwell (differential form) equations are simply modified to central-difference equations, discretized, and implemented in software. The equations are solved in a leap-frog manner; that is, the electric field is solved at a given instant in time, then the magnetic field are solved at the next instant in time, and the process is repeated over and over again. Although FDTD was simple, elegant and can be easily implemented, it did not gain much attention immediately after its publication. One reason was its high computational cost, and the others were the inherent limitations at that time, such as boundary conditions and numerical error.

1.2.2 The Development of FDTD

FDTD was initially used to solve the EM scattering problem by Taflove [49] in 1975, which is the first break-through in FDTD history. Taflove was among the first to rigorously analyze FDTD numerical errors [49]. Taflove was also the first to present the correct stability criteria for the original orthogonal-grid Yee algorithm [49]. In his papers, some critical problems were solved or improved. The correct derivation of the stability criterion was demonstrated; the lattice truncation conditions were proposed to handle the unbounded boundary.

ABC is often used to truncate the computational domain in space since the tangential components of the electric field along the outer boundary of the computational domain

cannot be updated using the basic Yee algorithm. The early ABC technique is radiation

conditions [2]. ABC's can be grouped into those that are derived from differential

equation based or material absorber. Mur [32] first applied an ABC technique of acoustic

wave equations used by Engquist and Majda [13] in time domain electromagnetic field

equations. Microstrip line was modeled with Mur's ABCs by Sheen [39]. Mur's ABCs

and Berenger's PML [5] are differential and materials ABCs respectively, which

essentially solved the problems of boundary conditions in FDTD.

PML gained attention immediately after Berenger's publication in 1993 [5].

Waveguide and multilayered planar circuit structure were studied with PML technique by

Bahr [1], Reuter [38] and Verdu [55]. Berenger [4] used PML to solve interaction

problems. Afterwards, he also reported evanescent waves in PML's [6] [3]. Katz [25]

extended 2-D PML to 3-D PML, gave 3-D PML expression. Li [29] reported microstrip

modeling by PML in non-uniform FDTD grid. Veihl [54], Fang [14] , Sullivan [47] and

Zhao [60] worked to improve PML performance by various formulations. PML makes it

possible for high accuracy simulation and therefore has a major impact upon the FDTD

modeling community.

Lumped elements were modeled into the FDTD formulation by adding an

additional current term, named lumped current, in the Ampere's Law [44]. Dumey [12]

and Picket-May [37] have extended Sui's 2D analysis to model full wave propagation in

3D circuits containing both active and passive elements. Based on Sui and Picket-May's

work, SPICE-like circuit simulator can interface with FDTD simulation in time domain

seamlessly, yielding stable and accurate result for nonlinear and active circuit [29,30].

Zheng [61] and Namiki [33] reported new algorithms that overcame the time step

restriction in FDTD calculation, thus further enhancing the incorporation of FDTD with SPICE-like simulator. Kuo [28] reported another lumped elements method, which was named as lumped voltage approach. This approach employs voltage sources to represent the lumped devices and generate electromagnetic fields based on Faraday's Law.

1.3 Planar Package Simulation

1.3.1 Flip chip interconnect and FDTD method

Flip-chip interconnect is a popular surface mount packaging technique because it does not have lateral leads or pins and has advantages, such as low electrical parasitic and low-cost, easy assembly through self-alignment, the smallest footprint, and the thinnest profile and weight [17][34][35].

One important topic for flip-chip package is how to enhance the transition performance at operating frequency range. There are many parameters which affect the performance, such as the interconnect bump length and width, the conductor on the board below the chip, the feeding line width of coplanar waveguide (CPW), and the ground to ground distance of CPW. Various methods have been applied to tune these parameters for optimal packaging performance [15][19][20][34], but they were limited to few structural variations. Solution of electromagnetic (EM) field is required for most of the packaging analyses, preferably broadband technique for high-speed circuitry. Flip-chip interconnect was studied by Sonnet simulation in comparison with experimental measurements [34]. The simulation result was quite different from measured results, probably because incomplete modeling of the contributing factors to the transition performance, such as via pad size, via cross section and height, and dielectric layer. Two CPW lines with one

interconnect was analyzed recently [15]. They also gave broadband solutions. However, the structure with three CPW layers connected by two sets of interconnects (via and ball), which is more complicated and close to actual design, has not been studied in detail.

This thesis presents a wideband approach for characterizing multiple flip-chip interconnects by the FDTD method. Three different flip chip interconnects are studied in chapter 3. Detailed analysis for electrical performance for frequency up to 40 GHz has been performed with variations of interconnect bumps (ball cross section and via cross section). A three-layer CPW connected by two sets of interconnects (via and ball) is studied using FDTD method in detail. The relationship between reflection loss, via pad length, ball cross-section and via cross section is tabulated for future packaging design. Based on the simulation results, some design approaches are proposed for packaging structures operating at near 40 GHz.

1.3.2 Whole Package Simulation

Whole package simulation is the most import part of this thesis. Circuit designers are faced with the problem of devising packages with sufficient electrical properties for mounting circuits that perform at high speed. The accurate prediction of the electrical performance prior to fabrication has been difficult because of its fully three dimensional structure. The FDTD whole package simulation is strongly expected to aid in designing the packages more efficiently.

From the point of view of electromagnetic modeling a microwave package is not only a considerably complex structure. There are different simulation segments. The first is the simulation of the embedded circuit. To deal with package simulation it needs not to

go into details of the circuit. The chip is treated as an n-port whereby its global interaction with the surrounding package is considered. A current flow from one port of the circuit to another leads to a global EM coupling to the environment. There is no need to register the local current distribution due to the internal circuitry as long as the chips are small compared to the package. The second is the package itself containing the carrier, sealing, feedthrough, and interconnects. Optimization of interconnects is another important question that is also concerned with different connecting techniques inside and outside the package. Chapter 3 focuses on how to optimize interconnects by adjusting some package parameters. Chapter 4 concentrates on whole package simulation.

Circuit simulation was reported by Shibata [39], but he focused more on circuit than whole package. Pereda [36] also reported linear RLC lumped network FDTD simulation. A break through of whole package simulation was reported by Sui [45]. A general method to integrate s-parameter and behavioral block, along with lumped circuit components, into standard FDTD simulation, was presented by Sui. The convolution algorithm for s-parameter block requires inverse Fourier series calculation for impulse response function. The concept of absorbing cube is introduced, in addition to the induced current to Maxwell's equations, to clearly define the interface between distributed and lumped circuit. It also revolves the uncertainty of the size and location of the added subcircuits, either s-parameter block or other lumped components. Since the s-parameter and behavioral model integration approach follows the same paradigm for modeling lumped elements, it greatly extended FDTD capability to include both lumped components and s-parameter block into full-wave time-domain simulation. Accuracy and stability of the method are verified by excellent comparisons for some two-dimensional

test circuits. The formulation is derived for three dimensions and its implementation is straightforward. This method includes industrial standard s-parameter circuit representation and behavioral module in FDTD simulation and it should find its application in full-wave solution for RF integrated circuits, chip packaging and many other high-frequency system designs.

CHAPTER 2

PRINCIPLES OF THE FDTD METHOD AND

NON-UNIFORM GRID NUMERICAL ERROR

2.1 Introduction

The first part of this chapter introduces the principles of the FDTD method. The FDTD equations for the field components are presented, and the locations of the electric and magnetic field components on Yee cells are illustrated. The stability condition and relationship among the spatial and temporal discretization are also discussed.

The second part of this chapter demonstrates the relationship between the non-uniform grid and numerical error. The non-uniform grid can be used to describe accurately the complicated geometrical shape of the electromagnetic system. The non-uniform FDTD grid provides us with flexibility to improve its accuracy. The characteristics of a plane wave on the boundary of two adjacent media with non-uniform FDTD rectangular grids are analyzed. The reflection and refraction characteristics of the wave propagation at the boundary or two adjacent media due to the numerical dispersion of The FDTD method are demonstrated. In the FDTD simulation, these characteristics are different from the theoretical solution and cause numerical errors. The magnitude of numerical errors depends on the FDTD simulation parameters. Knowing these characteristics would help us manipulate the FDTD cell size distribution in order to achieve the desired simulation accuracy within the requirement.

Li [29] derived non-uniform numerical error equations in the TE mode when electrical field is in parallel to the plane of incidence. In this chapter, the non-uniform numerical error equations when the electrical field is perpendicular to the plane of

incidence were derived. The FDTD simulation results are also given in comparison with the theoretical ones.

2.2 The Yee FDTD

Kane Yee reported a set of finite difference equations for the time dependent Maxwell's curl equations system [57]. The Yee algorithm solves for both electric and magnetic fields in time and space using the coupled Maxwell's curl equations rather than solving for the electric field alone or magnetic field alone with a wave equation. This is analogous to the combined-field integral equation formulation of Maxwell, where both E and H boundary conditions are enforced on the surface of a material structure.

Using information of both E and H, the solution is more liable than using either alone. Both electric and magnetic material properties can be modeled in a straightforward manner. This is especially important when modeling radar cross-section migration. Features unique to each field such as tangential H singularities near edges and corners, azimuthal (looping) H singularities near thin wires, and radial E singularities near points, edges and thin wires can be individually modeled if both electric and magnetic fields are available.

The original Maxwell's curl equations:

$$\frac{\partial D}{\partial t} - \nabla \times H = -J \qquad (2.1)$$

$$\frac{\partial B}{\partial t} + \nabla \times E = 0 \qquad (2.2)$$

In linear, isotropic, time invariant, non dispersive media, the Maxwell's curl equations can be written as

$$\varepsilon \frac{\partial \mathrm{E}}{\partial t} = \nabla \times \mathrm{H} - J \tag{2.3}$$

$$\mu \frac{\partial \mathrm{H}}{\partial t} = -\nabla \times \mathrm{E} \tag{2.4}$$

In Cartesian coordinates, equations (2.3-2.4) can be rewritten as a system of equations for all the electromagnetic field components

$$\varepsilon \frac{\partial E_x}{\partial t} = \frac{\partial H_z}{\partial y} - \frac{\partial H_y}{\partial z} - J_x \tag{2.5}$$

$$\varepsilon \frac{\partial E_y}{\partial t} = \frac{\partial H_x}{\partial z} - \frac{\partial H_z}{\partial x} - J_y \tag{2.6}$$

$$\varepsilon \frac{\partial E_z}{\partial t} = \frac{\partial H_y}{\partial x} - \frac{\partial H_x}{\partial y} - J_z \tag{2.7}$$

$$-\mu \frac{\partial H_x}{\partial t} = \frac{\partial E_z}{\partial y} - \frac{\partial E_y}{\partial z} \tag{2.8}$$

$$-\mu \frac{\partial H_y}{\partial t} = \frac{\partial E_x}{\partial z} - \frac{\partial E_z}{\partial x} \tag{2.9}$$

$$-\mu \frac{\partial H_z}{\partial t} = \frac{\partial E_y}{\partial x} - \frac{\partial E_x}{\partial y} \tag{2.10}$$

As illustrated in Figure 2.1, a special spatial discretization scheme named Yee cell, is used in The FDTD method to discretize the equations (2.5-2.10). The Yee algorithm centers its E and H components in 3-D space so that every E component is surrounded by four circulating H components, and every H component is surrounded by four circulating E components. The placements of the electromagnetic field components are off the grid nodes of one half cell size. The arrangement of the positions of E and H components is for the purpose to locate the electrical media more conveniently. In order to locate the magnetic media conveniently, the positions of E and H components can be exchanged.
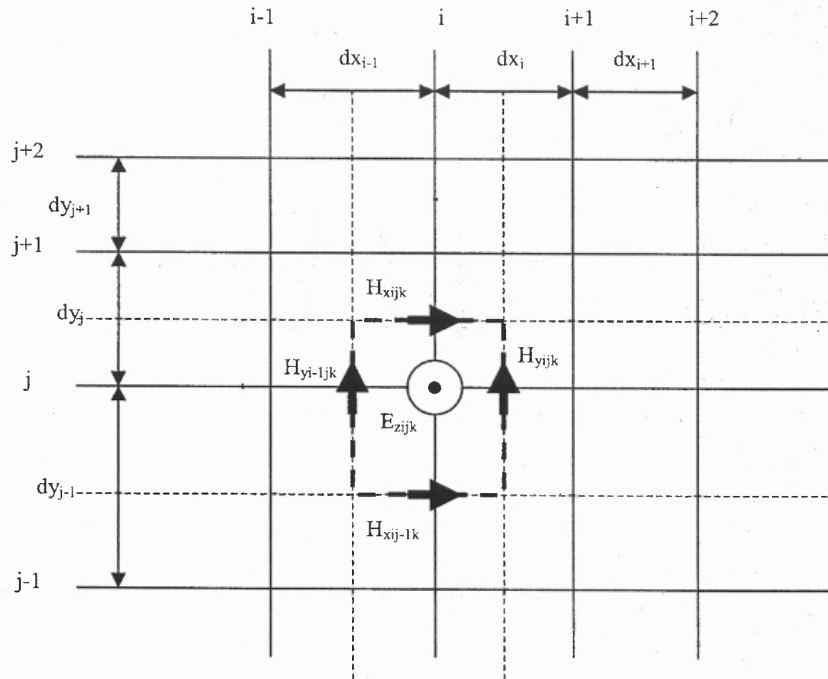
Figure2.1 Non-uniform FDTD grid

This does not change the FDTD equations at all. In time domain, the E and H components are also defined at different time instants. Specifically, the E field is defined at the ndt and the H field is defined at (n+1/2)dt, n is a non-negative integer and dt is the temporal increment.

E and H field component expressions can be obtained with uniform cell size and only conduction current from equations (2.5-2.10)

$$E_{xijk}^{n+1} = \frac{\frac{\Delta t}{\varepsilon} - \frac{\sigma}{2}}{\frac{\Delta t}{\varepsilon} + \frac{\sigma}{2}} E_{xijk}^{n} + \frac{1}{\frac{\Delta t}{\varepsilon} + \frac{\sigma}{2}} \left(\frac{H_{zijk}^{n+1/2} - H_{zij-1k}^{n+1/2}}{\Delta y} - \frac{H_{yijk}^{n+1/2} - H_{yijk-1}^{n+1/2}}{\Delta z} \right) \tag{2.11}$$

$$E_{yijk}^{n+1} = \frac{\frac{\Delta t}{\varepsilon} - \frac{\sigma}{2}}{\frac{\Delta t}{\varepsilon} + \frac{\sigma}{2}} E_{yijk}^{n} + \frac{1}{\frac{\Delta t}{\varepsilon} + \frac{\sigma}{2}} \left(\frac{H_{xijk}^{n+1/2} - H_{xijk-1}^{n+1/2}}{\Delta z} - \frac{H_{zijk}^{n+1/2} - H_{zi-1jk}^{n+1/2}}{\Delta x} \right) \tag{2.12}$$

$$E_{zijk}^{n+1} = \frac{\frac{\Delta t}{\varepsilon} - \frac{\sigma}{2}}{\frac{\Delta t}{\varepsilon} + \frac{\sigma}{2}} E_{zijk}^{n} + \frac{1}{\frac{\Delta t}{\varepsilon} + \frac{\sigma}{2}} \left(\frac{H_{yijk}^{n+1/2} - H_{yi-1jk}^{n+1/2}}{\Delta x} - \frac{H_{xijk}^{n+1/2} - H_{xij-1k}^{n+1/2}}{\Delta y} \right) \tag{2.13}$$

$$H_{xijk}^{n+1/2} = H_{xijk}^{n-1/2} - \frac{\Delta t}{\mu} \left(\frac{E_{zij+1k}^{n} - E_{zijk}^{n}}{\Delta y} - \frac{E_{yijk+1}^{n} - E_{yijk}^{n}}{\Delta z} \right) \tag{2.14}$$

$$H_{yijk}^{n+1/2} = H_{yijk}^{n-1/2} - \frac{\Delta t}{\mu} \left(\frac{E_{xijk+1}^{n} - E_{xijk}^{n}}{\Delta z} - \frac{E_{zi+1jk}^{n} - E_{zijk}^{n}}{\Delta x} \right) \tag{2.15}$$

$$H_{zijk}^{n+1/2} = H_{zijk}^{n-1/2} - \frac{\Delta t}{\mu} \left(\frac{E_{yi+1jk}^{n} - E_{yijk}^{n}}{\Delta x} - \frac{E_{xij+1k}^{n} - E_{xijk}^{n}}{\Delta y} \right) \tag{2.16}$$

where the conduction current is evaluated as forward time average $J^{n} = \sigma(E^{n} + E^{n+1})/2$.

The new value of a field vector component at any space lattice point depends on its previous value and the previous values of the components of the other field at adjacent points [50, 51]. In another word, every E components can be calculated based on its

value at its previous time step and H field values around it at a half time step before. Every H field component can also be computed according to its value in previous time step and the E field values around it at a half time step before. Thus, this scheme is also called leap frog scheme.

The FDTD method is necessary to avoid numerical instability. The stability criteria of the FDTD method are [51]

$$c\Delta t \leq \Delta x \tag{2.17}$$

$$c\Delta t \leq \frac{1}{(\frac{1}{\Delta x^2} + \frac{1}{\Delta y^2})^{1/2}} \tag{2.18}$$

$$c\Delta t \leq \frac{1}{(\frac{1}{\Delta x^2} + \frac{1}{\Delta y^2} + \frac{1}{\Delta z^2})^{1/2}} \tag{2.19}$$

Equations (2.16-2.18) are for 1-D, 2-D and 3-D methods respectively. They are also known as Courant-Eriedrichs-Lewy(CFL) stability criterion.

2.3 Boundary Condition Techniques

The field computation domain must be limited in size because the computer can not store an unlimited amount of data. The computation domain must be large enough to enclose the structure of interest, and a suitable boundary condition on the outer perimeter of the domain must be used to simulate its extension to infinity. The outer boundary condition must suppress spurious reflections of the outgoing numerical wave analogs to an acceptable level, permitting the FDTD solution to remain valid for all time steps, especially after the reflected wave analogs return to the vicinity of the modeled structure.

These conditions are called absorbing boundary conditions (ABCs). Two ABCs are used in this thesis, one is Mur's ABC, the other is Berenger's PML.

2.3.1 Mur's ABCs

Mur's ABCs are based on defactoring the second order wave equation into two first order wave equations, each of which represents the wave in opposite directions. Each component of the electric field independently satisfies the three-dimensional wave equation:

$$(\frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} + \frac{\partial^2}{\partial z^2} - c^{-2}\frac{\partial^2}{\partial t^2})W = 0 \qquad (2.20)$$

where W is any E or H component.

Define three inverse velocity components Sx, Sy and Sz

$$Sx = \frac{\partial t}{\partial x} \qquad (2.21)$$

$$Sy = \frac{\partial t}{\partial y} \qquad (2.22)$$

$$Sz = \frac{\partial t}{\partial z} \qquad (2.23)$$

which satisfy

$$Sx^2 + Sy^2 + Sz^2 = c^{-2} \qquad (2.24)$$

It is assumed that the mesh is located in the region 0≤x, and give boundary conditions for the plane x=0. The differential equation that describes the outgoing wave is

$$\frac{\partial W}{\partial x} \pm c^{-1}(1 - (cSy)^2 - (cSz)^2)^{1/2}\frac{\partial W}{\partial t} = 0 \qquad (2.25)$$

The first order Mur ABCs can be obtained by first order Taylor's series from Equation (2.25):

$$\frac{\partial W}{\partial x} = \frac{\partial W}{c\partial t} \tag{2.26}$$

From the second order Taylor's series:

$$(1 - (cSy)^2 - (cSz)^2)^{1/2} = 1 - \frac{1}{2}((cSy)^2 + (cSz)^2) \tag{2.27}$$

Second order Mur ABCs can be obtained:

$$(\frac{\partial^2}{c\partial x\partial t} + \frac{\partial^2}{2\partial y^2} + \frac{\partial^2}{2\partial z^2} - c^{-2}\frac{\partial^2}{\partial t^2})W = 0 \tag{2.28}$$

Mur's ABCs can keep the reflection coefficient as low as 20dB. But Mur's ABC is not faultless. A wave is absorbed without reflection only when it is a plane wave propagating perpendicularly to the boundary. Although the Mur's boundary condition can be extended to higher order if higher Taylor's series is used, it does not help much on the reflection and can cause a stability problem.

2.3.2 Perfect Matched Layer (PML)

Berenger [5] published a novel ABC for FDTD meshes in two dimensions with orders of magnitude of improved performance relative to any earlier technique. For a 2-D problem, with only E_x, E_y and H_z field components. If there is a medium, with property $\frac{\sigma}{\varepsilon_0} = \frac{\sigma^*}{\mu_0}$, where ε_0 and μ_0 are the free space permittivity and permeability, and σ and σ^* denote electric conductivity and magnetic loss respectively. Then the impedance of the media equals that of vacuum and no reflection occurs. A plane wave is perfectly matched (zero reflection) when normally incident on a half space of this media.

But the absorbing medium described above fails perfect match for the EM waves that are not normally incident on the absorbing layer. The PML approach based upon a

splitting of electric or magnetic field components in the absorbing boundary region with the possibility of assigning losses to the individual split field components, can absorb EM waves when oblique incident. The net effect of this is to create a non-physical absorbing medium adjacent to the outer FDTD mesh boundary that has a wave impedance independent of the angle of incidence and frequency of outgoing scattered waves. PML effective reflection coefficient is 1/3000th of standard second and third order analytical Mur's ABCs [5,49].

Using PML to terminate 2-D electrical structure having E_x, E_y and H_z components [5]. Hz is split into two subcomponents: Hzx and Hzy.

$$\varepsilon \frac{\partial E_x}{\partial t} + \sigma_y E_x = \frac{\partial (H_{zx} + H_{zy})}{\partial y} \tag{2.29}$$

$$\varepsilon \frac{\partial E_y}{\partial t} + \sigma_x E_y = -\frac{\partial (H_{zx} + H_{zy})}{\partial x} \tag{2.30}$$

$$\mu \frac{\partial H_{zx}}{\partial t} + \sigma^*_x H_{zx} = -\frac{\partial E_y}{\partial x} \tag{2.31}$$

$$\mu \frac{\partial H_{zy}}{\partial t} + \sigma^*_y H_{zy} = \frac{\partial E_x}{\partial y} \tag{2.32}$$

If PML region is set according to following rules:

$$\frac{\sigma_x}{\varepsilon} = \frac{\sigma^*_x}{\mu} \tag{2.33}$$

$$\frac{\sigma_y}{\varepsilon} = \frac{\sigma^*_y}{\mu} \tag{2.34}$$

when electrical wave propagates in the +x direction, at maximum x, the electrical wave meet with PML that has σ_x and σ^*_x matched with $\sigma_y = \sigma^*_y = 0$. The PML permits transmission across the vacuum-PML interface without reflection, as shown in Figure

2.2. It is assumed that the loss in PML region increases quadratically with depth d. The loss σ will reach to its maximum value when d=δ. The loss in PML can be chosen to bound the reflection coefficient [47]

$$R = e^{-\frac{2\sigma_{max}\delta}{3\varepsilon c}}$$
(2.35)

So reflection coefficient can be kept to some desired level.

In three dimensional cases, all six Cartesian field vector components are split. The resulting PML modification of Maxwell's equations yields 12 equations [25], as follows:

$$\varepsilon\frac{\partial E_{xy}}{\partial t} + \sigma_y E_{xy} = \frac{\partial H_z}{\partial y}$$
(2.36)

$$\varepsilon\frac{\partial E_{xz}}{\partial t} + \sigma_y E_{xz} = -\frac{\partial H_y}{\partial z}$$
(2.37)

$$\mu\frac{\partial H_{xy}}{\partial t} + \sigma^*_y H_{xy} = -\frac{\partial E_z}{\partial y}$$
(2.38)

$$\mu\frac{\partial H_{xz}}{\partial t} + \sigma_y^* H_{xz} = -\frac{\partial E_y}{\partial z}$$
(2.39)

$$\varepsilon\frac{\partial E_{yx}}{\partial t} + \sigma_x E_{yx} = -\frac{\partial H_z}{\partial x}$$
(2.40)

$$\varepsilon\frac{\partial E_{yz}}{\partial t} + \sigma_z E_{yz} = \frac{\partial H_x}{\partial z}$$
(2.41)

$$\mu\frac{\partial H_{yx}}{\partial t} + \sigma^*_x H_{yx} = -\frac{\partial E_z}{\partial x}$$
(2.42)

$$\mu\frac{\partial H_{yz}}{\partial t} + \sigma^*_z H_{yz} = -\frac{\partial E_x}{\partial z}$$
(2.43)

Figure 2.2 Three layers: vacuum, PML, conducting wall.

$$\varepsilon \frac{\partial E_{zx}}{\partial t} + \sigma_x E_{zx} = \frac{\partial H_y}{\partial x} \qquad (2.44)$$

$$\varepsilon \frac{\partial E_{zy}}{\partial t} + \sigma_y E_{zy} = -\frac{\partial H_x}{\partial y} \qquad (2.45)$$

$$\mu \frac{\partial H_{zx}}{\partial t} + \sigma^*_x H_{zx} = -\frac{\partial E_y}{\partial x} \qquad (2.46)$$

$$\mu \frac{\partial H_{zy}}{\partial t} + \sigma^*_y H_{zy} = \frac{\partial E_x}{\partial y} \qquad (2.47)$$
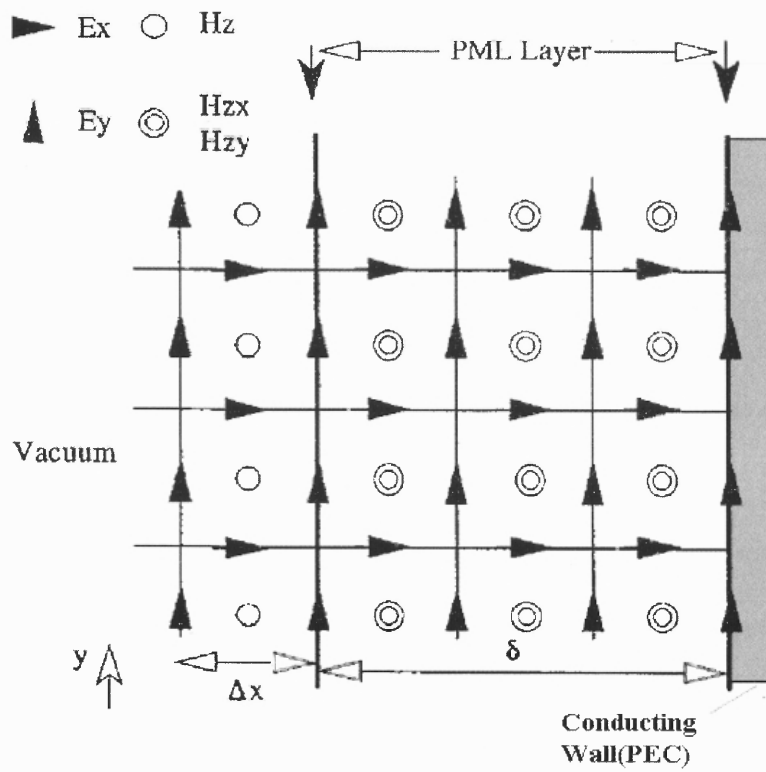
Since the electromagnetic field changes rapidly in a PML medium in space but not in time, the exponential scheme in time does not improve stability. Thus, the central discretization scheme to discretize the time derivative is also used.

The electric and magnetic conductivity profile in a PML layer is also an important factor to influence the performance of the PML. Constant, linear, parabolic, and geometric profiles are all used to define the conductivity profile from the interface between PML and Yee cell to the outer boundary, normally perfect electrical conductor (PEC) wall. The parabolic profile is much better than the linear and constant profile, but for the simulation with a large number of iterations, the parabolic profile causes a significant error. The geometric profile can avoid this problem, but a more careful design must be made to define the PML boundary laryers.

Generally, the performance of PML is much better than Mur's ABCs. According to Berenger's work [5], the reflection coefficient of PML is 20 dB less than that of Mur's ABCs. The shortcoming of PML is its higher computational cost because of the splitting of the electromagnetic field components and additional layers in the FDTD grid. In the microwave and high frequency circuit analysis, involving complicated electromagnetic phenomena, such as near field phenomena and high order modes, PML is

generally accepted as the main approach to handle boundary conditions in FDTD simulation.

2.4 PEC cell type

FDTD simulation sometimes needs to treat very thin conductor layer with zero thickness. So an artificial property, which is called PEC type is created to stand for zero thickness conductor. The PEC property fixes some of the E components in a Yee cell to zero during all the computational time. There are 7 PEC types [29],

PEC Type	Description
0	No Components are fixed to 0
1	Ex=0
2	Ey=0
3	Ez=0
4	Ex=Ey=0
5	Ex=Ez=0
6	Ey=Ez=0
7	Ey=Ez=Ez=0

Table 2.1 PEC type

Figure 2.3 is thin conductor rectangle that is expressed by PEC cell types. The four thin conductor cells are PEC type 4, which keep Ex and Ey to zero. Its boundary PEC cells are type 1 and 2; type 1 keeps Ex to zero, and type 2 keep Ey to zero. PEC is a very
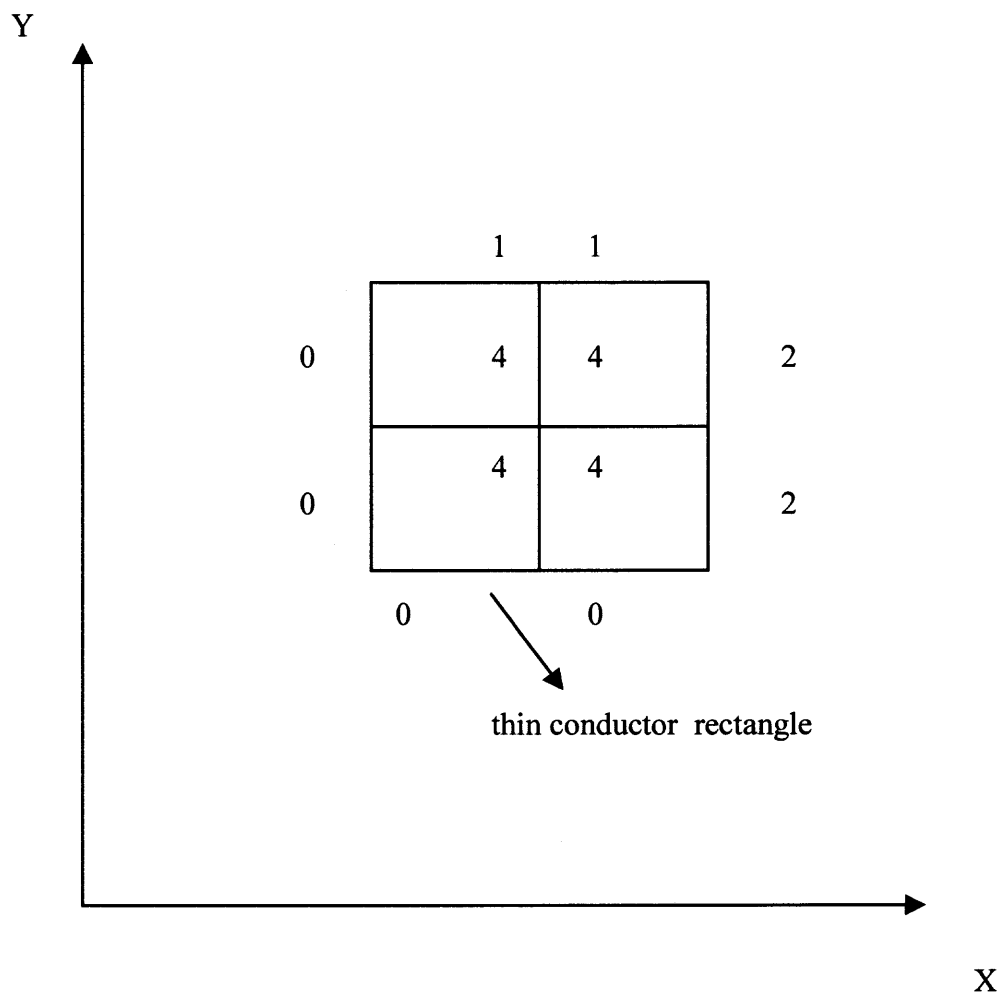
Figure 2.3 Thin conductor rectangle's PEC type

useful property for FDTD. With its help, lumped elements can be added in between one or two cells. PEC is used default in this thesis. Non-PEC type is stated when it is used.

2.5 Numerical Error for Non-uniform Grid of Electromagnetic System

The non-uniform FDTD grid provides us flexibility to improve accuracy of simulation. It is often desirable to have a refined lattice in localized regions such as near sharp edges or corners to accurately model the local field phenomena. This section analyzes the characteristics of a plane wave on the boundary of two adjacent media with non-uniform FDTD rectangular grids. The reflection and refraction equations of the wave propagation at the boundary or two adjacent media due to the numerical dispersion of The FDTD method are derived. In the FDTD simulation, these equations are different from the theoretical solution due to numerical errors. The magnitude of numerical errors depends on the FDTD simulation parameters.

There are two regions for non-uniform grid reflection, as it is shown in Figure 2.4:

Region One: incident wave and reflected wave

$$E_{z1} = \xi_1 A(e^{j(\omega ndt - (k_{xi} id_{x1} + k_{yi} jd_{yi}))} + R \cdot e^{j(\omega ndt + (k_{xr} id_{x1} + k_{yr} jd_{yi}))}) \tag{2.48}$$

$$H_{x1} = A(\sin\theta_i e^{j(\omega ndt - (k_{xi} id_{x1} + k_{yi} jd_{yi}))} + R \cdot \sin\theta_r e^{j(\omega ndt + (k_{xr} id_{x1} + k_{yr} jd_{yi}))}) \tag{2.49}$$

$$H_{y1} = A(\cos\theta_i e^{j(\omega ndt - (k_{xi} id_{x1} + k_{yi} jd_{yi}))} - R \cdot \cos\theta_r e^{j(\omega ndt + (k_{xr} id_{x1} + k_{yr} jd_{yi}))}) \tag{2.50}$$

Region Two: transmitted wave

$$E_{z2} = \xi_2 Be^{j(\omega ndt - (k_{xt} id_{x2} + k_{yt} jd_{y2}))} \tag{2.51}$$

$$H_{x1} = B\sin\theta_t e^{j(\omega ndt - (k_{xt} id_{x2} + k_{yt} jd_{y2}))} \tag{2.52}$$
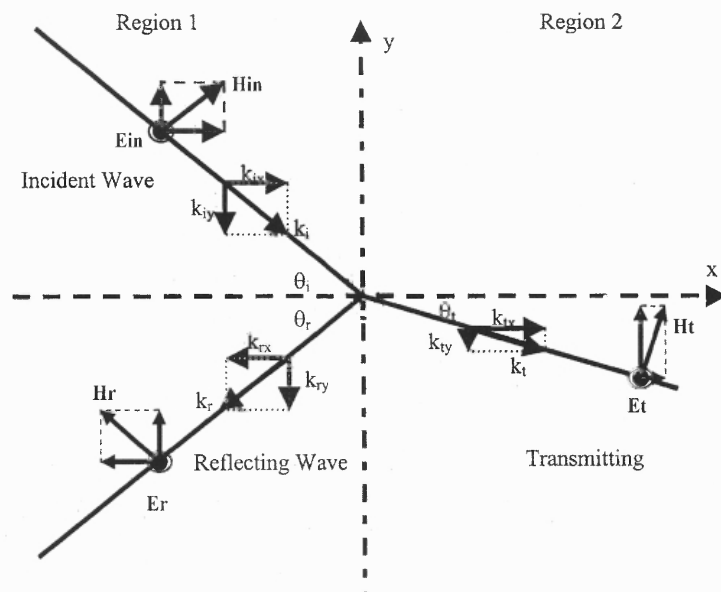
Figure 2.4 TM mode wave propagates in the interface of two different media

$$H_{y1} = B\cos\theta_t e^{j(\omega n dt - (k_{xi}idx2 + k_{yi}jd_{y2}))}$$
(2.53)

where characteristic impedance $\xi = \sqrt{\dfrac{\mu}{\varepsilon}}$

using Ampere's Law near the interface

$$\iint_S (\varepsilon \frac{\partial E_z}{\partial t} + \sigma E_z)ds = \oint_C H \cdot dl$$
(2.54)

from equation (2.54),

$$\frac{(H_{yij+1/2}^{n+1} - H_{yij+1/2}^n)}{dt} \cdot \frac{\mu_1 dx_1 + \mu_2 dx_2}{2} = -E_{zi+1/2j+1/2}^{n+1/2} + E_{zi+1/2j+1/2}^{n+1/2}$$
(2.55)

Substituting (2.48)—(2.53) into (2.55), the numerical reflection coefficient can be obtained as follows

$$R = \frac{\cos\theta_i \cdot i \cdot \sin(\dfrac{\omega dt}{2}) \cdot \dfrac{\mu_1 dx_1 + \mu_2 dx_2}{dt} + \xi_1 e^{jk\frac{1}{2}dx_1} - \xi_2 e^{-jk\frac{1}{2}dx_2}}{\cos\theta_t \cdot i \cdot \sin(\dfrac{\omega dt}{2}) \cdot \dfrac{\mu_1 dx_1 + \mu_2 dx_2}{dt} - \xi_1 e^{-jk\frac{1}{2}dx_1} - \xi_2 e^{-jk\frac{1}{2}dx_2}}$$
(2.56)

By using the same procedure as above, the reflection coefficient for E in the incident plane can also be attained [29]:

$$R = \frac{-i \cdot \sin(\dfrac{\omega dt}{2}) \cdot \dfrac{\varepsilon_1 dx_1 + \varepsilon_2 dx_2}{dt} + \dfrac{\xi_1^{-1} e^{-jk\frac{1}{2}dx_1}}{\cos\theta_t} - \dfrac{\xi_2^{-1} e^{-jk\frac{1}{2}dx_2}}{\cos\theta_i}}{i \cdot \sin(\dfrac{\omega dt}{2}) \cdot \dfrac{\varepsilon_1 dx_1 + \varepsilon_2 dx_2}{dt} + \dfrac{\xi_1^{-1} e^{jk\frac{1}{2}dx_1}}{\cos\theta_t} + \dfrac{\xi_2^{-1} e^{-jk\frac{1}{2}dx_2}}{\cos\theta_i}}$$
(2.57)

Two FDTD simulations are run to verify the reflection coefficient equation. The simulation area is 100X18 cells, with minimum grid size of 1mm.

Case One: the whole simulation area is divided by two, the first half has uniform grid size 1mmX 1mm, the second half has uniform grid 10mmX 1mm, the monitor point is in the middle of the interface of the two areas. Figure 2.5 is the FDTD simulation and theoretical result, directly calculated from the equations derived above.

Case Two: the first half has uniform grid size 1mm X 1mm, and the second has uniform grid 20mm X 1mm. The monitor point is the same as case one. Figure 2.6 is the FDTD simulation as well as the theoretical result.

Efforts at deciding nonuniform cell size can be very time consuming. Our work shows that the nonuniform numerical error can be kept at very low level by varying the size of the grid intervals slowly and monotonically. It can be concluded that the difference between two adjacent non-uniform cells should not be more than 10 times, otherwise it will cause great numerical reflection, which can be proved by Figure 2.5 and 2.6. The reflection also increases as the simulation frequency increases.
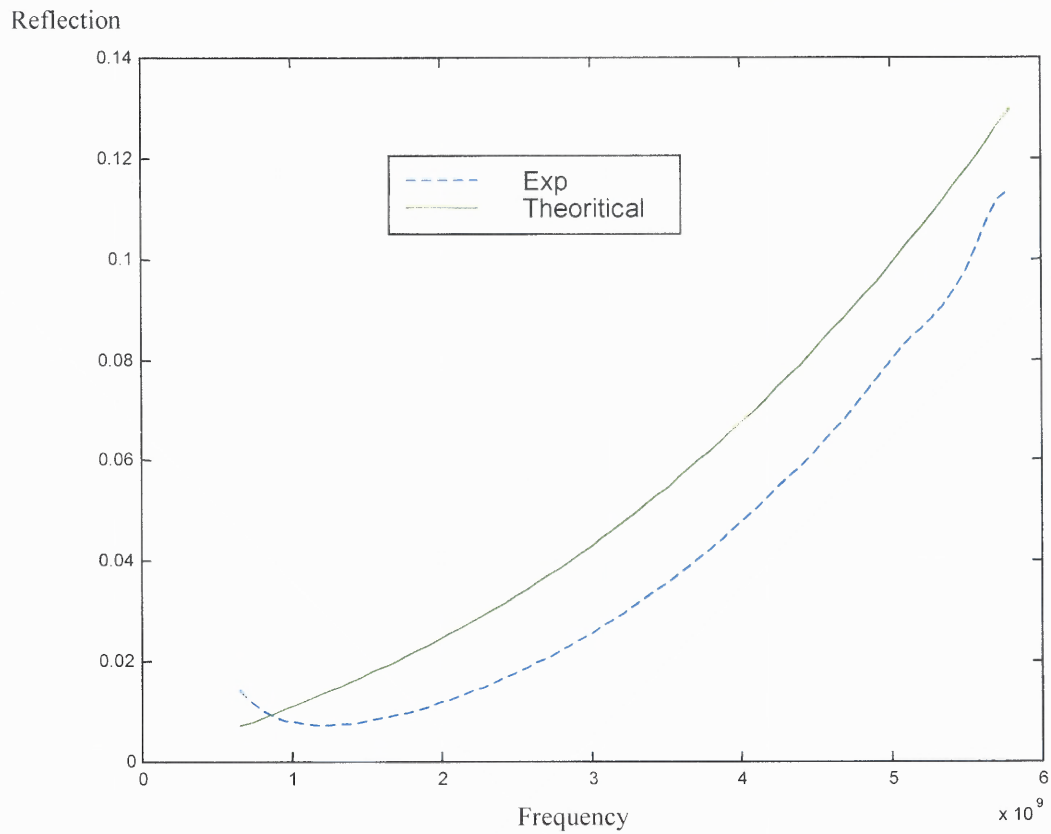
Figure 2.5 FDTD simulation result against theoretical result for non-uniform grid 1mm to 10mm

Reflection
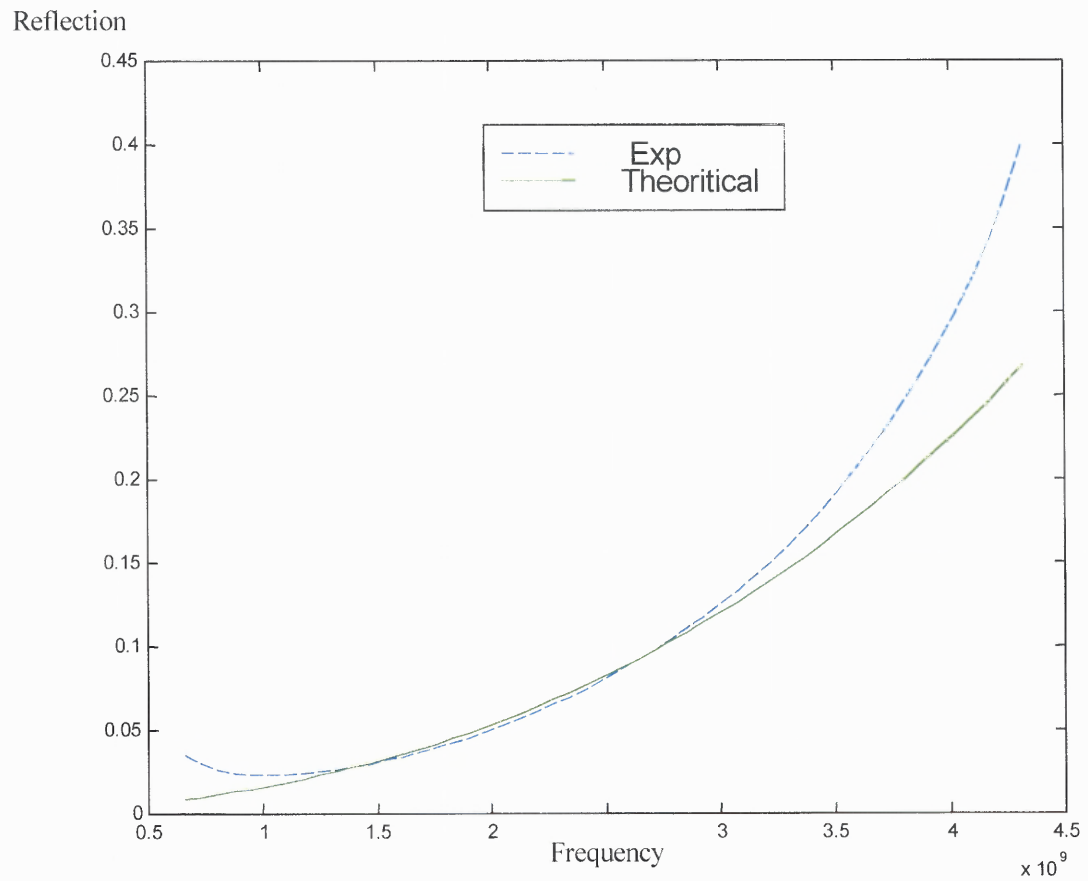
Figure 2.6 FDTD simulation result against theoretical result for non-uniform grid 1mm to 20mm

CHAPTER 3

BROADBAND TIME-DOMAIN CHARACTERIZATION

OF MULTIPLE FLIP CHIP INTERCONNECTS

3.1 Introduction

This chapter presents a comprehensive approach for the characterization of multiple flip-chip interconnects by 3-D FDTD method. The behaviors of transition discontinuities in CPW layers and flip-chip bump interconnects are investigated for optimal packaging performance. The relationship between the reflection loss, the via pad length and the cross-section of bumps is discussed in detail. Three types of flip-chip interconnects, which are quite different in size and structure, are simulated. Results in this chapter shows that FDTD is a reliable simulation method, which may be used as a design tool for complicated packaging structures.

3.2 Using FDTD Method on the Flip Chip Simulation

Maxwell's equations are the starting point for solving electromagnetic field distribution.

$$\oint_C E \cdot dl = -\int_S \mu \frac{\partial H}{\partial t} \cdot dS \tag{3.1a}$$

$$\oint_C H \cdot dl = \int_S (\sigma E + \varepsilon \frac{\partial E}{\partial t}) \cdot dS \tag{3.1b}$$

Since the general three-dimensional finite-difference expressions are well known [51], for reference purpose only the equations for z-components in Cartesian coordinate system are listed here.

$$H_{zijk}^{n+1/2} = H_{zijk}^{n-1/2} + \frac{\delta t}{\mu}(\frac{E_{xij+1k}^n - E_{xijk}^n}{\delta y_{ijk}} + \frac{E_{yijk}^n - E_{yi+1jk}^n}{\delta x_{ijk}}) \tag{3.2a}$$

$$E_{zijk}^{n+1} = \frac{\frac{\varepsilon_{ijk}}{\delta t} - \frac{\sigma_{ijk}}{2}}{\frac{\varepsilon_{ijk}}{\delta t} + \frac{\sigma_{ijk}}{2}} E_{zijk}^n + \frac{1}{\frac{\varepsilon_{ijk}}{\delta t} + \frac{\delta \sigma_{ijk}}{2}}(\frac{H_{yijk}^{n+1/2} - H_{yi-1jk}^{n+1/2}}{\delta x_{ijk}} + \frac{H_{xijk}^{n+1/2} - H_{xij-1k}^{n+1/2}}{\delta y_{ijk}}) \tag{3.2b}$$

During FDTD simulation, the voltage between the feeding line and ground is recorded at every FDTD iterations. The voltage is the integral of the electrical field from the ground to the feeding line. The observation point is between the discontinuity and the source. This position should be set to match the simulation results to the measurement ones.

Scattering (S) parameters of a given structure can be obtained by FDTD simulation. S parameters for a two port network are defined as:

$$\begin{bmatrix} v_r^1 \\ v_r^2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} v_i^1 \\ v_i^2 \end{bmatrix} \tag{3.3}$$

where v is a component of the EM field, superscripts 1 and 2 are port indices, and subscripts i and r refer to incident and reflected signals, respectively .

In order to obtain the S parameters at port 1, namely S_{11} and S_{12}, FDTD simulation should be run twice. First, the input signal v_i^1 is obtained for the distributed structure that has only the feeding CPW. Second, the total signal v_t^1 is calculated, which is the summation of the input and reflected signals with the effects of interconnects and other discontinuities in the system. Then the reflected signal can be calculated from the total

signal and input signal. The reflection parameter can then be obtained by Fourier transform [29].

$$S_{11} = \frac{fft(v_r^1)}{fft(v_i^1)}$$

(3.4)

where fft is the fast Fourier transform.

3.3 Simulation and Discussion

3.3.1 Small size flip chip

Small size flip chip is referred to the structure with which CPW ground to ground spacing is 120 μm in this thesis. Heinrich [20,21] reported 3-D the FDFD simulation results first. Then Jentzsch [24] reported the different possibilities to improve the return loss of the small size flip chip with FDFD method. The dielectric layer they used is GaAs. FDTD was used to simulate this structure in this chapter for the first time, and different dielectric fillers (GaAs, Sapphire) were used in simulation. Wide range frequency performance is evaluated from DC to 100 Ghz in this chapter.

Structure parameters: ground to ground distance is 120μm , feeding line width 50 μm , gap between feeding line and ground 35 μm , air above the layer is 200 μm , dielectric layer below the layer is 100 μm with dielectric constant =12.3, as the structure is shown is Figure 3.1. Reflection loss and insertion loss are displayed in Figure 3.2 and 3.3. By using FDTD S_{11} can be obtained with different dielectric fillers. When dielectric constant is changed from 12.3 to 9.6, other parameter is kept the same as above, the reflection loss is as shown in Figure 3.4.
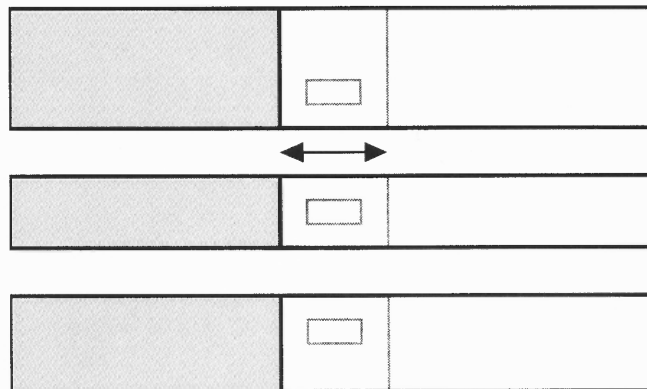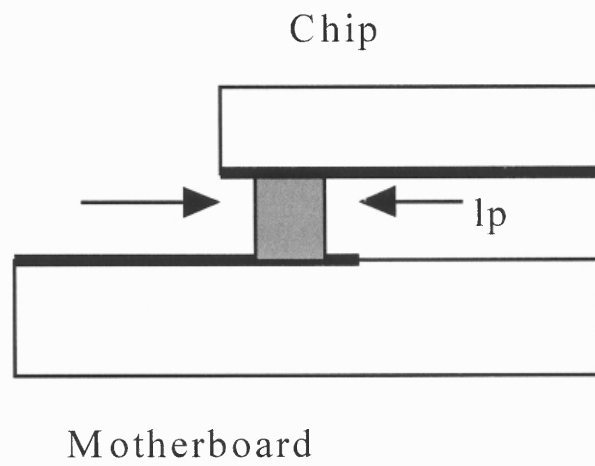
Figure 3.1 Flip chip interconnect structure side view and top view.
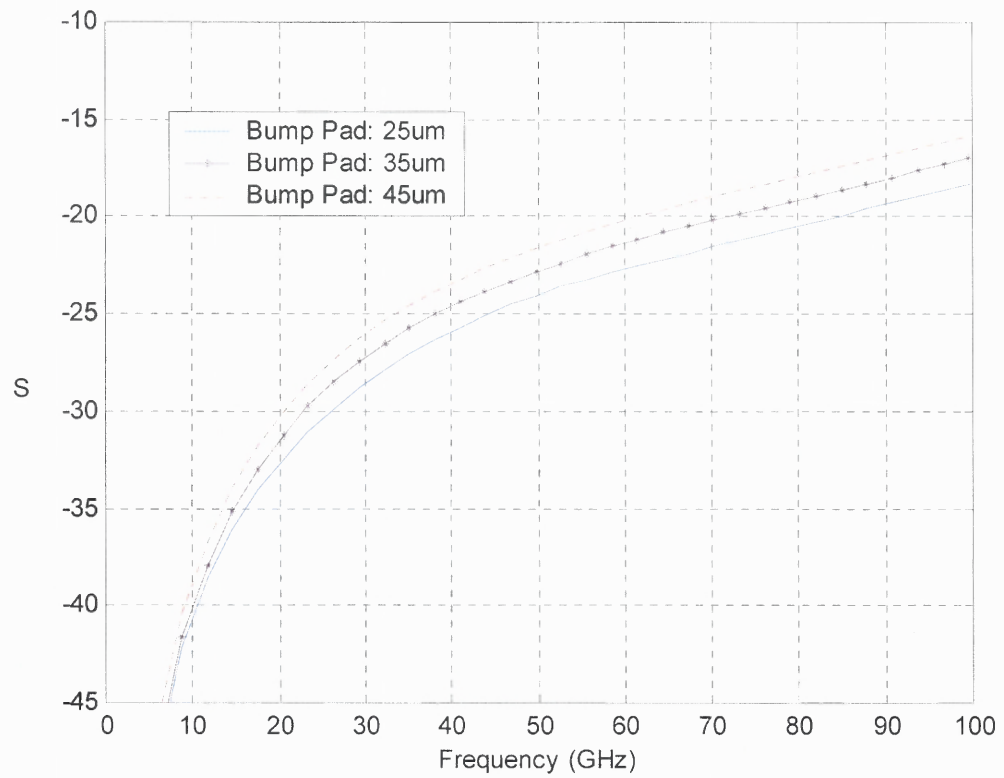
Figure 3.2 Return loss of small size CPW with dielectric constant=12.3, bump pad=25μm, 35μm, 45μm.

Figure 3.3 Insertion Loss of Small size CPW
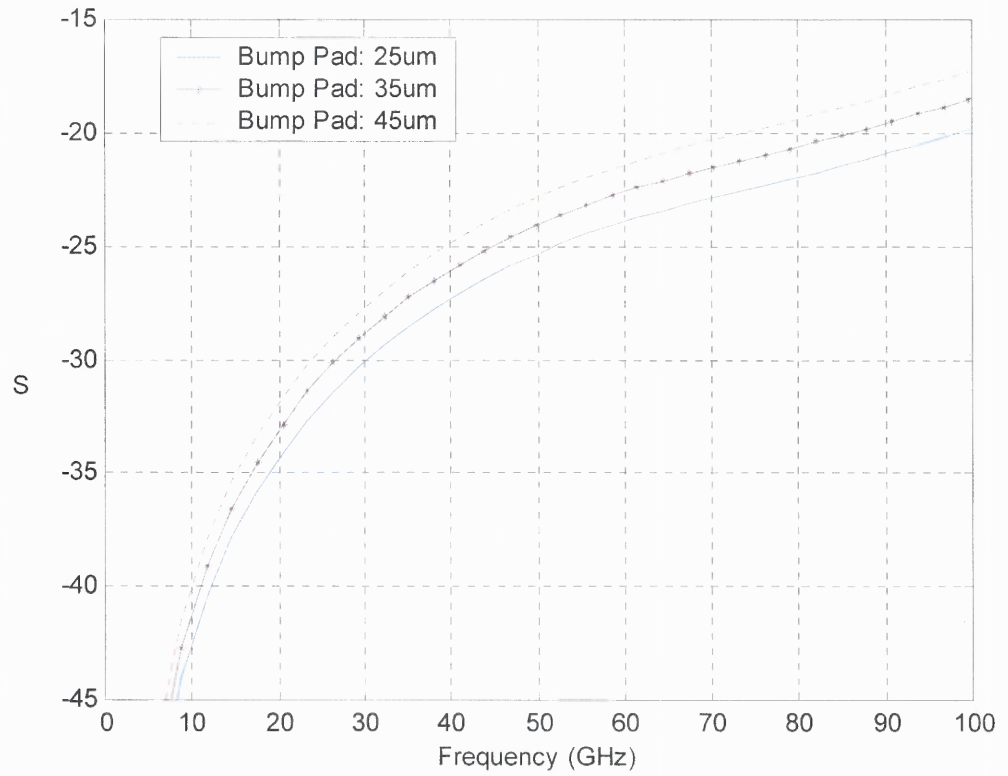
Figure 3.4 Small size CPW with dielectric filler, ε=9.6

From our simulation result, it can be concluded that the bump-pad length (lp) is one of the most important parameters in the mm-wave frequency range. The return loss and insertion loss given above are excellent and demonstrate the potential of this type of flip-chip for mm-wave applications. Sapphire filler has better reflection performance than GaAs as shown by our simulation results.
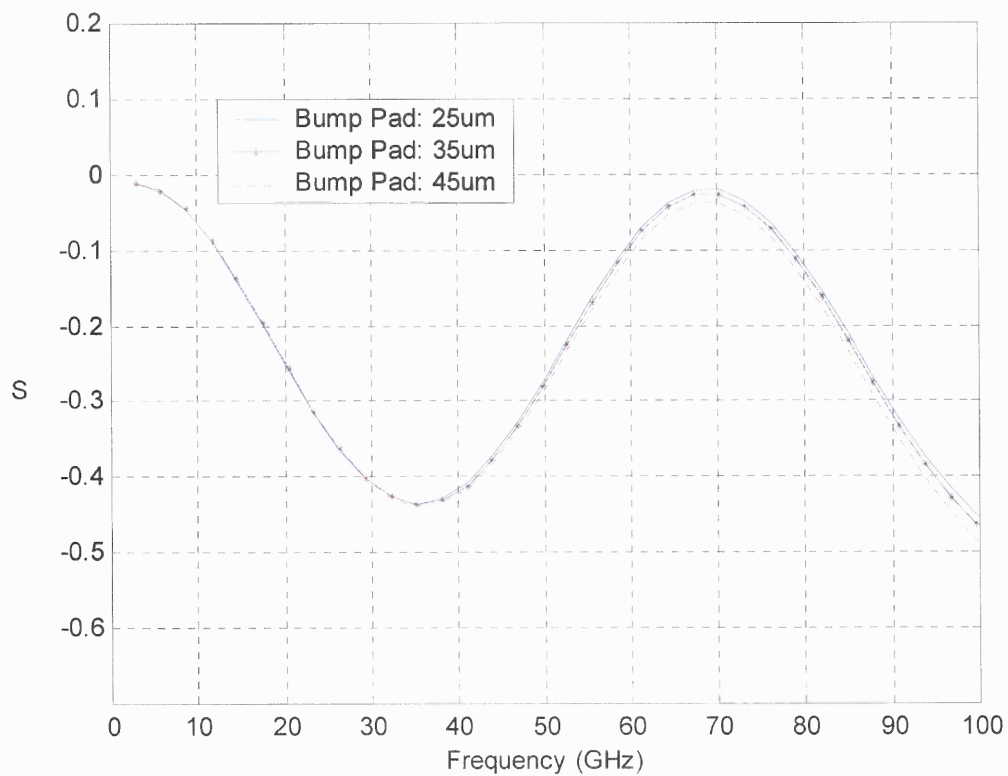
3.3.2 Middle size flip chip

For a middle size flip chip the CPW ground to ground spacing is about 0.36mm in this thesis. Ghouz [15] reported FDTD simulation for this structure, followed by the work of wang [56], who tried to optimize some parameters such as the bump numbers, and the bump to bump distance to find structure with less reflection at high frequency range. Wang [56] continued his FDTD work combined with PML and found some good transition structure.

The grid size used in this section is about 0.06mm, 8 PML cells are used to truncate the out boundary of the simulation domain. The original middle size flip chip structure is show on Figure 3.5, which is also called flat structure. Figure 3.6 is our simulation result. Ghouz' result [15] and our simulation are in excellent agreement with each other.

A new design named Single Resonance Design was reported by Wang [56]. The top view of the structure is shown on Figure 3.7 . Two vias are placed along the feeding line in this structure. The scattering from the two via will interfere with each other and optimum transition may be achieved when two vias are in suitable resonant separation, which is the original purpose of this design. Figure 3.8 is our FDTD simulation result

chip

motherboard

Side View
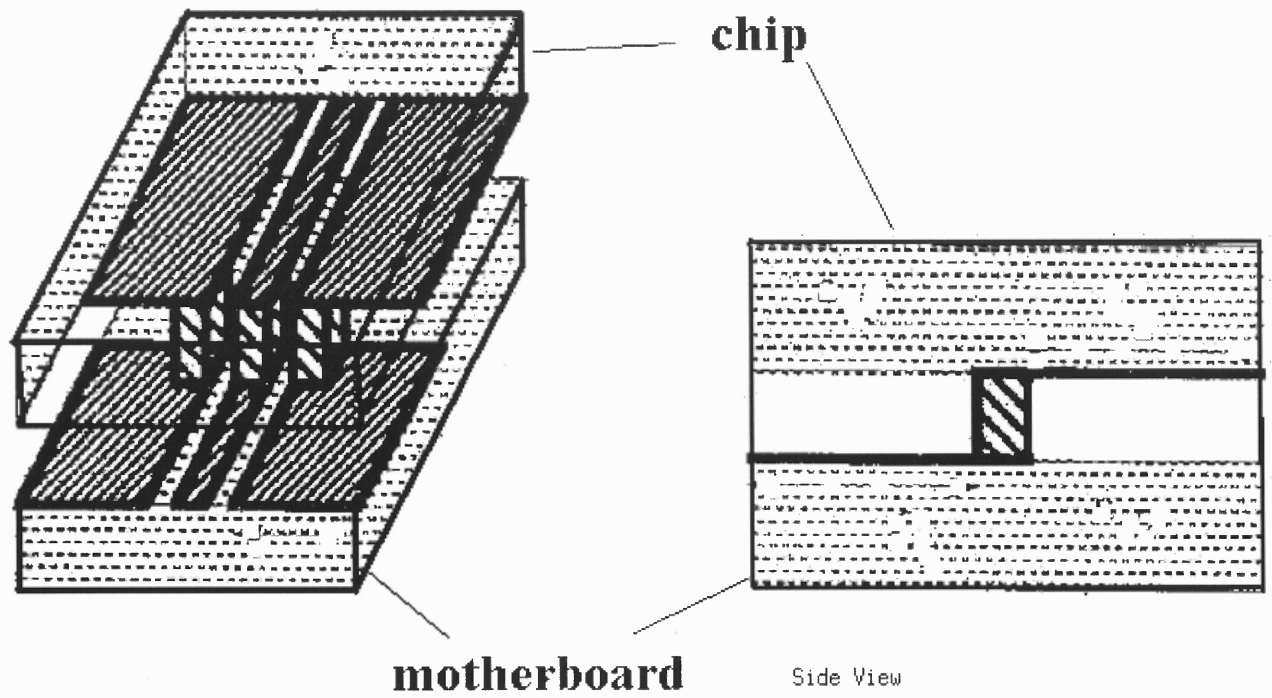
Figure 3.5 Flat flip chip structure
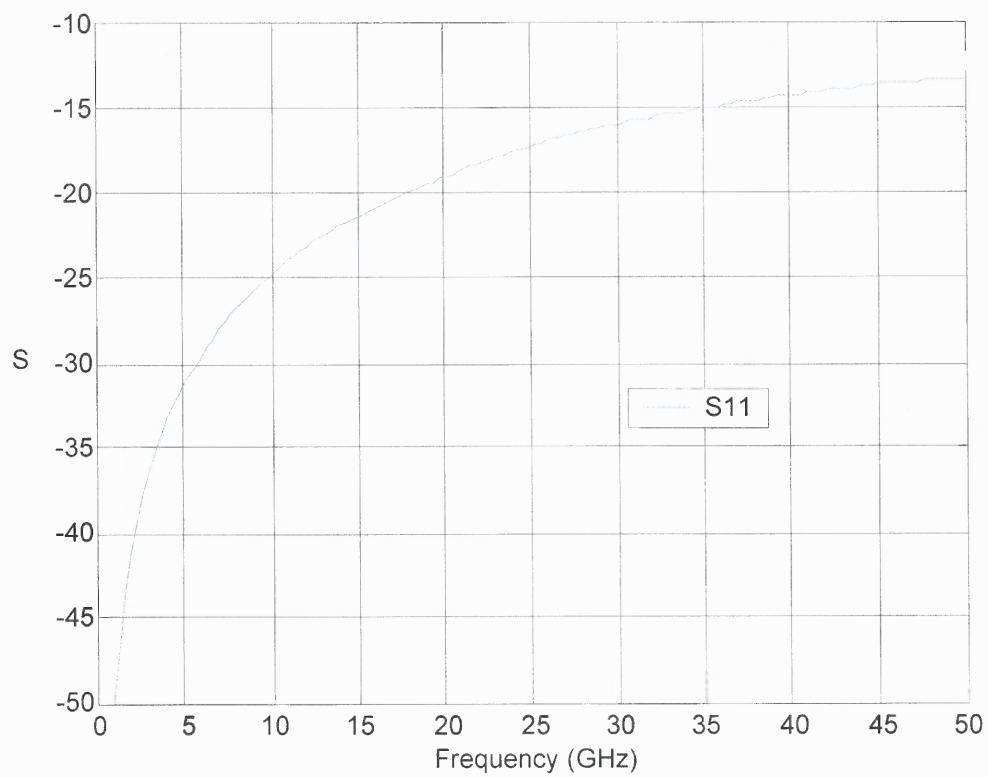
Figure 3.6 Flap structure simulation result
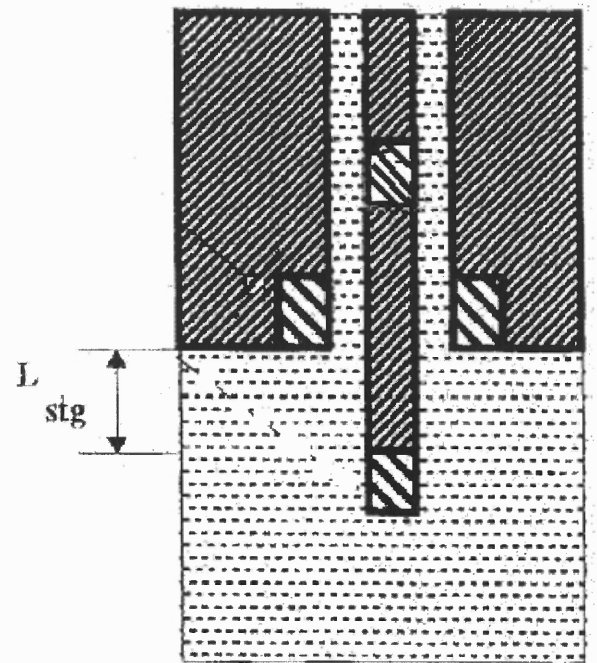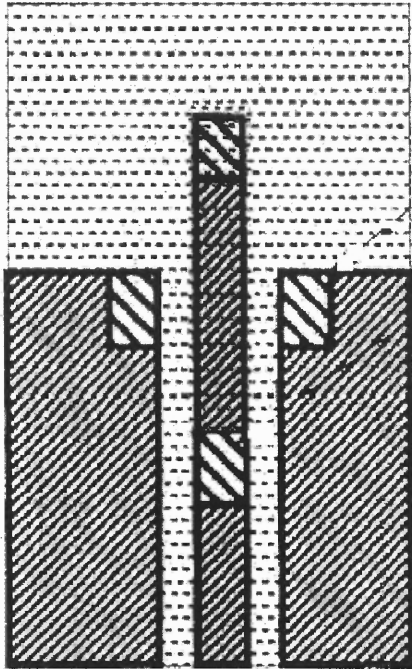
Figure 3.7 Top view of Single Resonant Structure
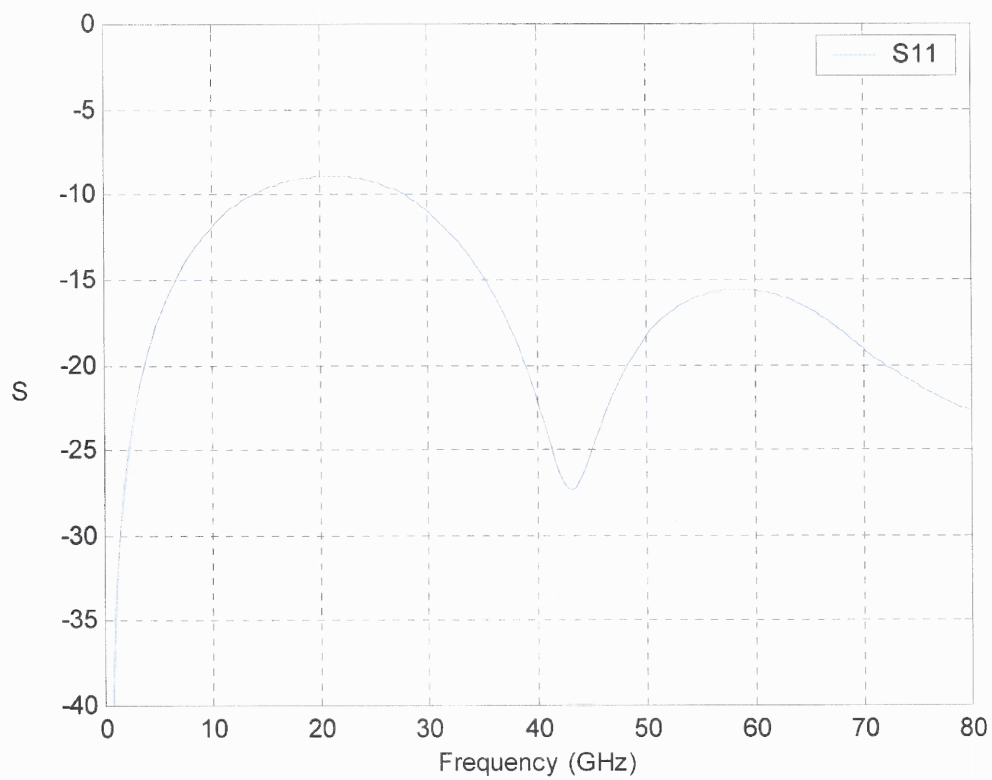
Figure 3.8 Single resonance flip-chip transition design

when Lstg=0.48mm. The reflection loss becomes bigger than flat flip chip when operating frequency is near 20 Ghz. However, this structure has better transition at the frequency range of 35 to 80 Ghz.

Another design to overcome the high reflection in high frequency range is the staggered structure, as shown in Figure 3.9. Figure 3.10 is the FDTD simulation result for Lstg=0.24 and 0.48mm. It seems that reflection loss can not be lower at low frequency and high frequency at the same time. 40Ghz is a turning point for this structure. Lstg should be kept short if the transition frequency is at DC to 40 Ghz range. But it should be kept long if 40 to 70 Ghz is the frequency range.

Although a great amount of FDTD simulation results are displayed in this section, it is hard to get a concise rule for the choice of optimized structure parameters at an arbitrary desired frequency band. The reason is parasitic resonance phenomenon in these structures. Detailed discussion of this phenomenon will be pursued in our future work.

3.3.3 Large size flip chip

The multiple flip-chip interconnect structure used in this section is based on thin film ceramic ball grid array (BGA) package [33]. The original structure has 3 RF and 5 DC I/O's. Figure 3.10 shows the side and top views of the simplified structure used for this study. There are three 50Ω CPWs and three associated dielectric layers. Layer substrates are alumina for the top and bottom layers, and air for the middle one, with heights of H1, H2 and H3, respectively. The dielectric constant for alumina is 9.6. Both input and output ports are on the bottom CPW lines as shown in Figure 3.11 and 12. The metal layers
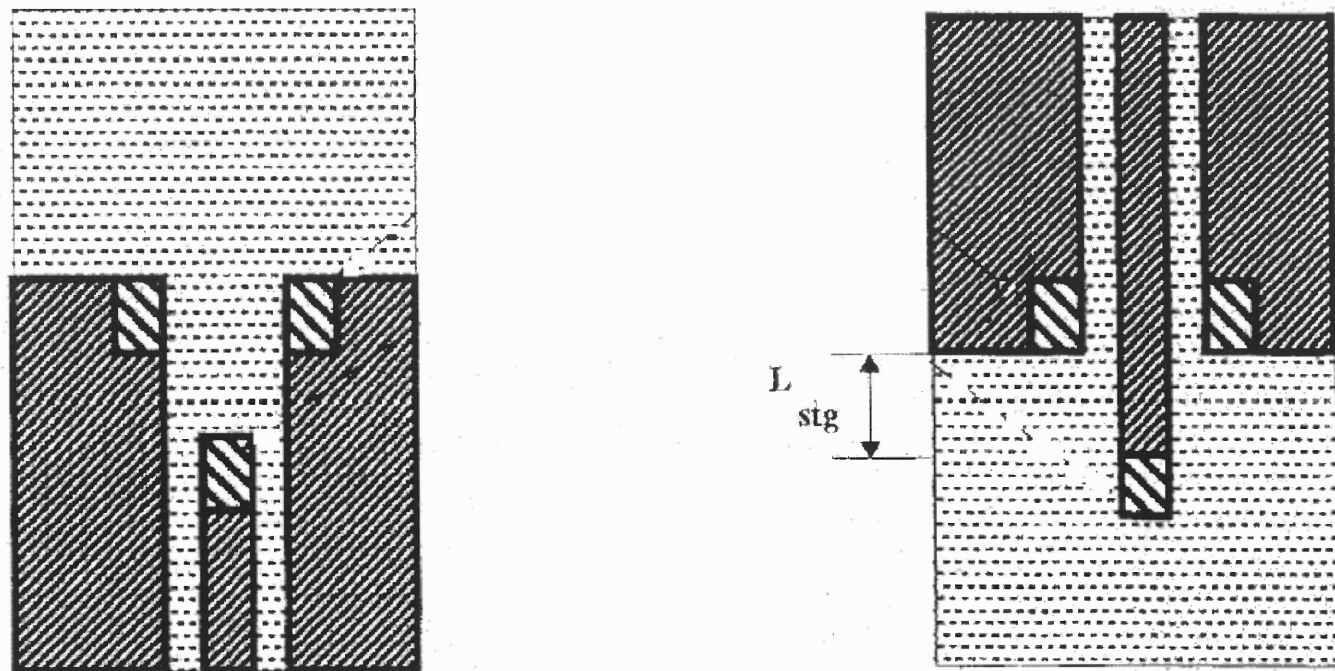
Figure 3.9 Staggered flip chip structure
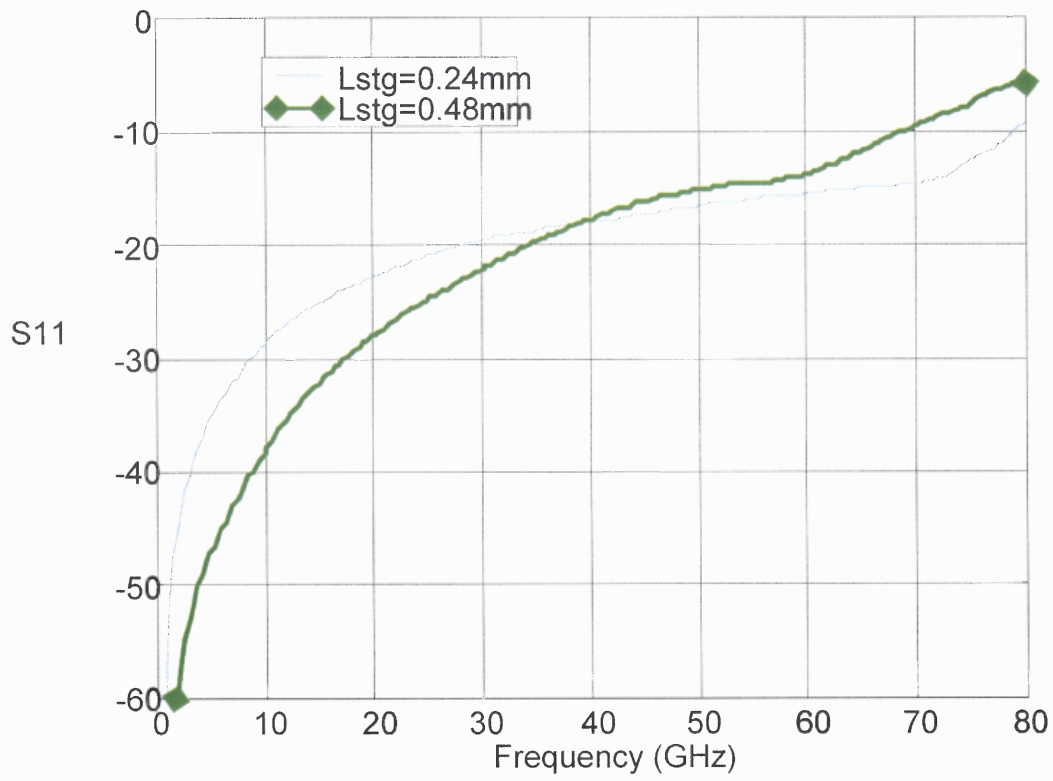
Figure 3.10 FDTD simulation of staggered structure with staggered distance 0.24,

0.48mm
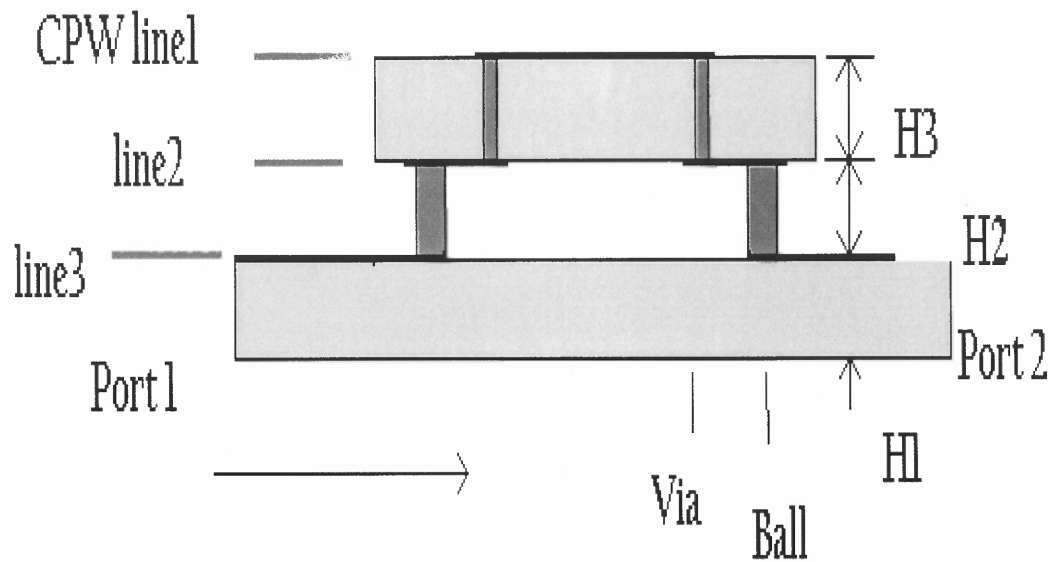
Figure 3.11 Side view of the three-layer structure. H1, H2, and H3 are 15 mils. The single arrow stands for the signal feeding direction.

are assumed perfect conductors (PEC) and of negligible thickness. There are two types of interconnect bumps: ball connecting CPW line 1 and line 2, and via connecting CPW line 2 and line 3. The round ball geometry is approximated as square and the RF via is also simplified as having a rectangular cross section. PML boundary condition in a non-uniform FDTD grid, 160x54x31 with average grid size of 50.8 mils, follows algorithm described in [30,31]. The workstation used for simulation is a Sun E5500 server; the average simulation time is 6-8 hours.

Figure 3.13 shows a comparison of reflection loss S_{11} between FDTD simulation and measurement, as well as reported Sonnet simulation [34]. The close match between FDTD result and measured data demonstrates the accuracy of the FDTD method. It proves that FDTD is an effective package simulation method. In the following we will use FDTD to optimize some interconnect bump packaging structures.

Ball and via interconnects can be described as an equivalent circuit of capacitance and inductance [19,20]. Changing ball cross section will change capacitance and inductance in the system, therefore causing reflection loss change at certain frequency range. FDTD simulation results demonstrated this behavior, as shown in Figure 3.14, where S_{11} is plotted versus different ball cross sections when via cross section is set at 4×4 mil. The reflection coefficient becomes smaller as the ball cross-area increases from 4×4 to 16×16 mil. The reflection coefficient increases with the increase of the cross section area when it is larger than 16×16 mil. This suggests that the package in this
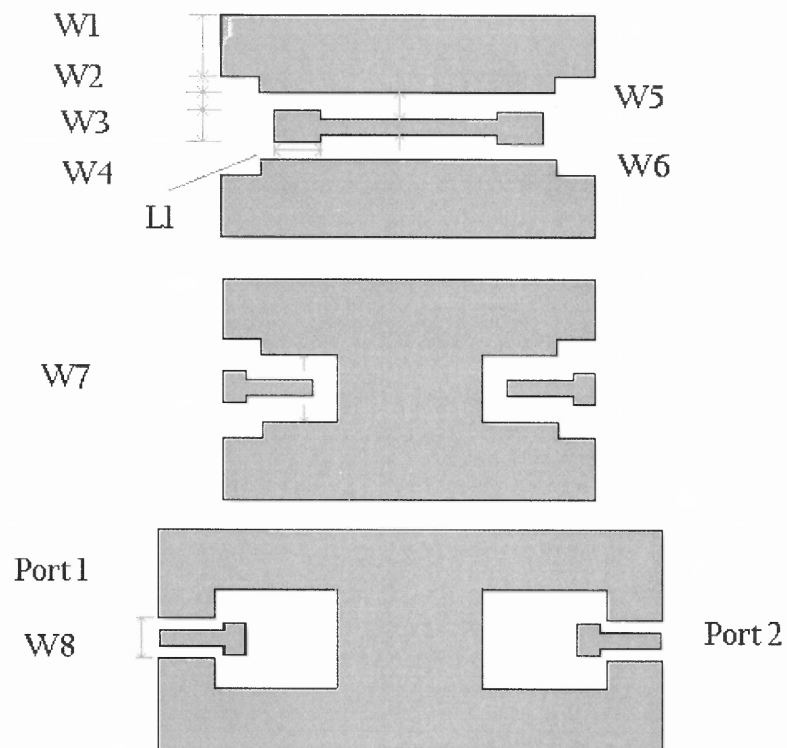
Figure 3.12 Top view of three CPW layers. W1, W2, W3 and W4 are 30, 10, 6, and 16 mils, respectively.
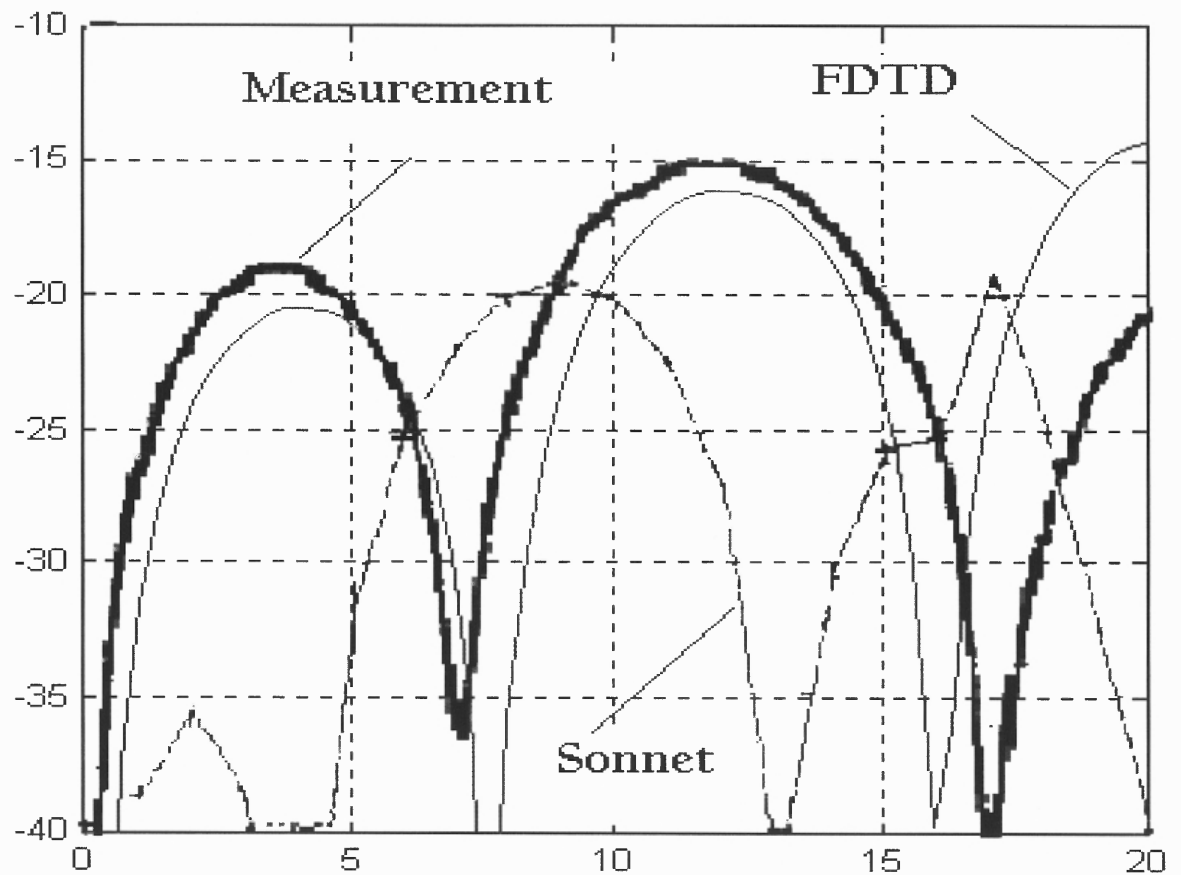
Figure 3.13 Comparison of S11, in dB vs. frequency in unit of GHz, from measurement and Sonnet simulation with FDTD result. W5, W6, W7, W8 and L1 are 4, 8, 24, 16 and 40 mils, respectively.

S11
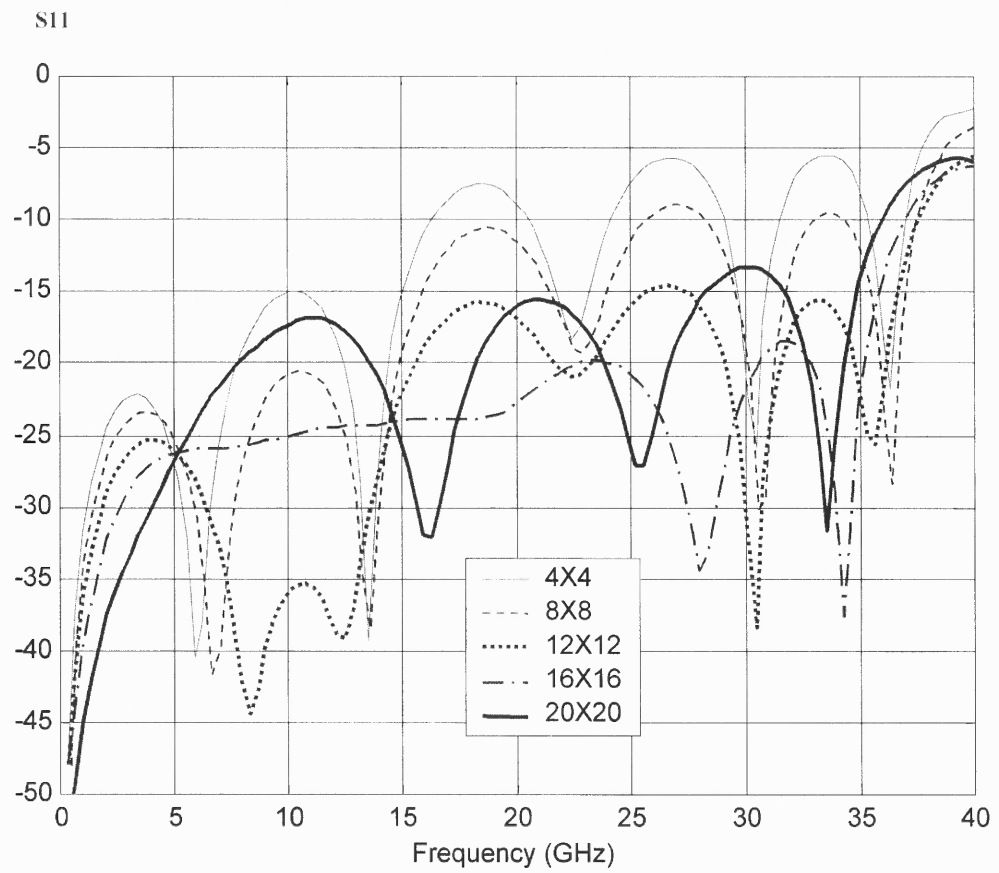
Figure 3.14 Reflection Loss for Different ball cross section

BGA format is useable in the frequency range of DC to 36 GHz if appropriate ball cross-section is chosen.

As shown in Figure 3.11, the via bump connects CPW line 2 and line 3. In order to study its effects to the packaging performance, its cross section is changed in parallel and perpendicular to feeding direction respectively. The effective inductance becomes larger when via size is increased along the signal propagating direction. The larger inductance degrades signal transition for flip chip. This is in agreement with FDTD simulation result as shown in Figure 3.15 where S_{11} changes with via length along propagating direction. The structure with via size 8×4 mil has better transition at higher frequency near 30 GHz. However, the structure with 4×4 mil has an overall better performance near lower frequency range.

Tuning effective via capacitance can improve flip chip interconnect transition, the parameters which can contribute to via capacitance are via pad length [19,20] and via width perpendicular to feeding direction. Figure 3.16 shows that S_{11} changes with via width perpendicular to the propagating direction. Structure with via size of 4x12mil has the lowest reflection near 30 GHz, but 4x8mil structure has the best performance from 0-40 GHz.

It is reported by Kim that the cross-section area of bump or via does not affect S parameter significantly [26]. In their structure, there was only one via along the feeding line that connects two CPW lines and it was only half of the structure studied here along the feeding direction. There are two sets of balls and vias which vertically connect three CPW in this thesis. Ball to ball, via to via and ball to via resonance affect S parameter
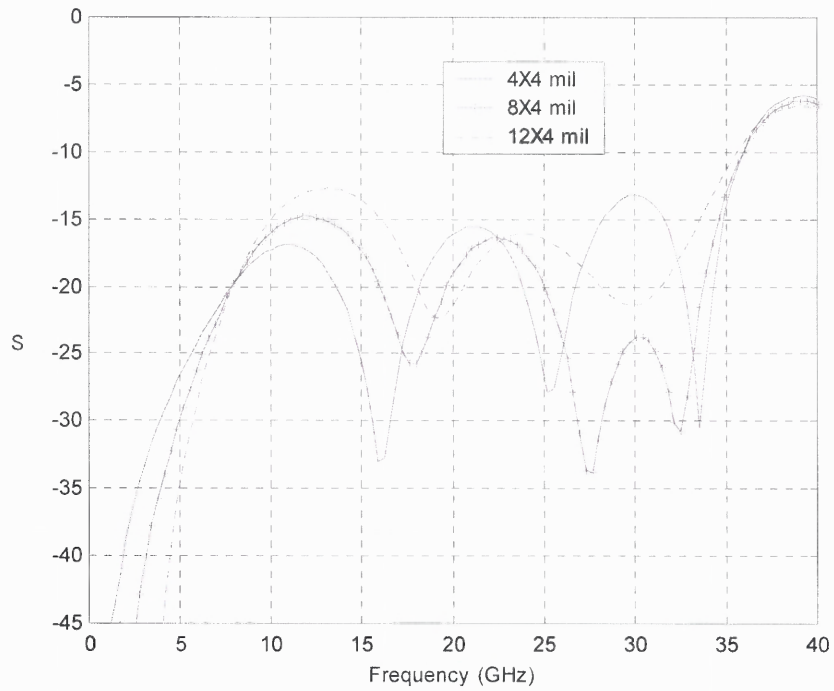
Figure 3.15 S_{11} for different via size along propagating direction. Via sizes are 4x4, 8x4 and 12x4 mil.
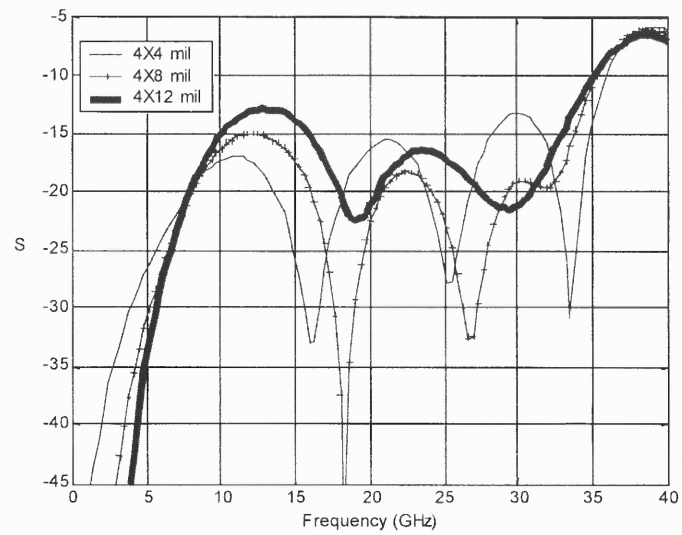
Figure 3.16 S_{11} for different via size perpendicular to propagating direction. Via sizes are 4x4, 4x8 and 4x12 mil.

significantly. Simulation results presented here indicate that S_{11} parameter is sensitive to ball and via cross section and they illustrate that several flip-chip structures can achieve a good transition design of 80% bandwidth over which the return loss is smaller than -20DB.

3.4 Conclusions

FDTD simulation results show that via and ball effects can change the designed packaging structure performance significantly. S_{11} can be optimized for certain frequency by changing the size and shape of the ball and via. However, it is difficult to obtain a precise rule for choosing the optimized via or ball cross section at an arbitrary desired frequency band; FDTD method, nevertheless, provides an accurate and efficient approach to study the performance of the interested structure.

CHAPTER 4

WHOLE PACKAGE SIMULATION WITH LUMPED ELEMENT METHOD

4.1 Introduction

The rapid expansion of high-frequency electronics demands more powerful analysis tool that can include both mixed signals from lumped elements and field effects in circuit design. Sui [44] extended FDTD method to include distributed electromagnetic systems with lumped elements (a hybrid system) as well as voltage and current sources in 2-D system. FDTD equations that include nonlinear elements such as diodes and transmitters are derived. Calculation of driving-point impedance is described. The extended FDTD method should prove useful in the design and analysis of complicated distributed systems with various active, passive, linear and nonlinear lumped electrical components.

Sui [45] also first reported an effective method for whole package simulation. The whole package includes the package interconnects and embedded circuits. It presents a generalized formulation for incorporating a lumped sub circuit, described by its current-voltage (I-V) relation, an n-port scattering parameters (S-parameters) or a behavioral model, into full-wave time-domain field simulator, FDTD method. The concept of absorbing cube is introduced for including any sub circuit in the FDTD grid. For a sub circuit described by S-parameters, the convolution formulae are based on its physical interpretation, and its numerical implementation requires additional computation and storage.

In this chapter lumped current algorithm and 3-D whole package simulation

53

algorithm are introduced. How to implement the whole package algorithm is the next topic for this chapter. Embedded circuit is modeled as a lumped block. 3-D simulation results from some test circuits can illustrate the accuracy and stability of the algorithm. This method provides a general approach for integrating n-port s-parameter and behavioral model representation into time-domain FDTD simulation.

4.2 Lumped Current Algorithm

Maxwell's equations are the fundamental equations for any field calculation and their FDTD solution can be found in many references [51]. Additional current term has been added to the total current integration, as shown in Eq (4.2), in order to take into account the contribution of any "alias system", as previously introduced in [43]. The current due to a lumped block can be added to the integration in Equation (4.2) to account for the current contribution to the total electromagnetic field.

$$\oint_C E \cdot dl = -\int_S \mu \frac{\partial H}{\partial t} \cdot dS \qquad (4.1)$$

$$\oint_C H \cdot dl = I_a + \int_S (\sigma E + \varepsilon \frac{\partial E}{\partial t}) \cdot dS \qquad (4.2)$$

Additional current term I_a in Equation (4.2) contributed by an alien system and it usually is related to other variables by a mathematical equation.

$$I_a(t) = f(\mathbf{i}, \mathbf{v}, \mathbf{E}, t) \qquad (4.3)$$

Since the general finite-difference expressions for Equation (4.1) are well known [43, 51], only the equations for z-component in Cartesian coordinate system are listed here for reference purpose. Field components in other directions can be written in similar equations.

$$H_{zijk}^{k+1/2} = H_{zijk}^{k-1/2} + \frac{\delta t}{\mu}\left(\frac{E_{xij+1k}^{k} - E_{xijk}^{k}}{\delta y} + \frac{E_{yijk}^{k} - E_{yi+1jk}^{k}}{\delta x}\right) \tag{4.4}$$

$$E_{zijk}^{k+1} = \frac{\dfrac{\varepsilon_{ijk}}{\delta t} - \dfrac{\sigma_{ijk}}{2}}{\dfrac{\varepsilon_{ijk}}{\delta t} + \dfrac{\sigma_{ijk}}{2}} E_{zijk}^{k} + \frac{1}{\dfrac{\varepsilon_{ijk}}{\delta t} + \dfrac{\delta t \sigma_{ijk}}{2}}\left(\frac{H_{yijk}^{k+1/2} - H_{yi-1jk}^{k+1/2}}{\delta x} + \frac{H_{xijk}^{k+1/2} - H_{xij-1k}^{k+1/2}}{\delta y} - \frac{I_{zijk}^{k+1/2}}{\delta x \delta y}\right) \tag{4.5}$$

The lumped resistor, inductor or capacitor can be modeled easily by substituting in to the above equations for each component. In finite-difference terms, these relations take the following forms for the resistor, inductor, and capacitor, respectively [37]:

$$I_{zi+1,j,k}^{n+1/2} = \frac{\delta l (E_{zi,j,k}^{n+1} + E_{zi,j,k}^{n})}{2R} \tag{4.6}$$

$$I_{zi,j,k}^{n+1/2} = \frac{(\delta l)(\delta t)}{L}\left(\sum_{k=1}^{n} E_{zi,j,k}^{k}\right) \tag{4.7}$$

$$I_{zi,j,k}^{n+1/2} = \frac{C \delta l}{\delta t}(E_{zi,j,k}^{n+1} - E_{zi,j,k}^{n}) \tag{4.8}$$

where R, L and C are given per unit length, and zero values are assumed for both inductor current and capacitor voltage at time zero.

Forward time averages have been taken in the above equations to be consistent with the treatment of the conductance. However, the forward difference form of the difference equations will lead to instabilities for certain values of R if no time averaging is used for the currents [44].

4.3 Broad Band Package with Lumped Elements

4.3.1 S parameter of embedded circuit

The electromagnetic behavior of the embedded circuit is described by its port behavior. S-parameter is used in this section. S-parameter is one of the most commonly used descriptive methods in frequency domain for high-frequency electric system and component. S, Y and Z parameters and other equivalent representations for linear system can be inter-transformed to each other. It is desirable to model the circuitry on chip as lumped sub-circuit with its S-parameter. S-parameter was transferred into Y-parameter and incorporated into FDTD simulation in [58] and [44]. The S-parameter modeling approach can be obtained with the relation between port voltage/current and incident and reflected ones at each port of an n-port system. The conversion of the frequency domain S- parameter to time domain is necessary for whole package simulation, so the embedded circuit can be processed as a lumped element by lumped algorithm. Figure 4.1 is the illustration of voltage and current at each port of an n-port system, where subscript + and − represent incident and reflected signal, respectively.
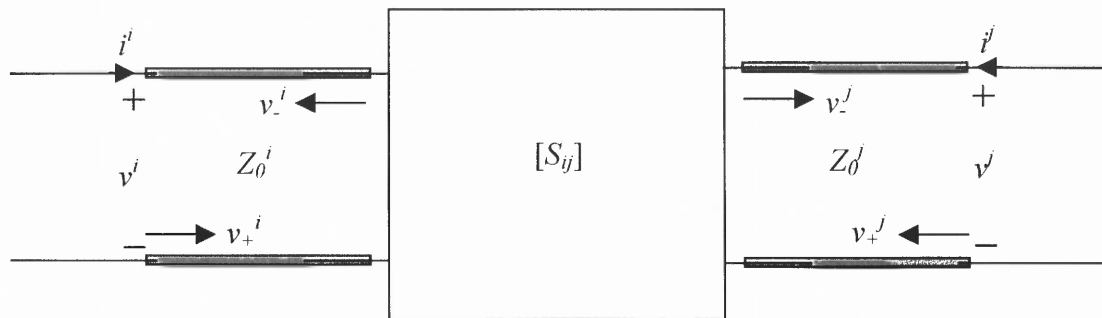
Figure 4.1. Illustration of voltage and current at each port of an n-port system, where subscript + and – represent incident and reflected signal, respectively.

4.3.2 Absorbing cube

The concept of absorbing cube is implemented in whole package simulation [45]. The absorbing cub is connected to the distributed circuit through a section of matching transmission line. It can trap any incident EM wave so the embedded circuit can be expressed by its mathematical representation at the interfaces with the distributed system. Each port of an n-port embedded circuit system is terminated with an absorbing cube through a section of lossless transmission line. The absorbing box can be approximated with many existing absorbing boundary conditions. Mur's 1st ABC is used by this section. Artificially high impedance is realized by assigning low permittivity and high permeability to the media that fill the space between the conductors, waveguide or substrate so that an open circuit effect at each port can be obtained. Since absorbing cube has high impedance property, its position and size will affect simulation result very much. The ideal position and size of this absorbing cube should be the same as the physical embedded circuit. The other determining factor would be the interactions between different portions of the distributed system. The absorbing cube can be shown in Figure 4.2.

4.3.3 Equation derivation of whole package simulation

When an n-port system is emerged in a distributed system, each port of the system is connected at its closest grid point inside the FDTD grid. An interface between distributed and the n-port system is then defined at these port points. At the interface, voltage and current are the connecting variables between the two electronic realms. So voltage and
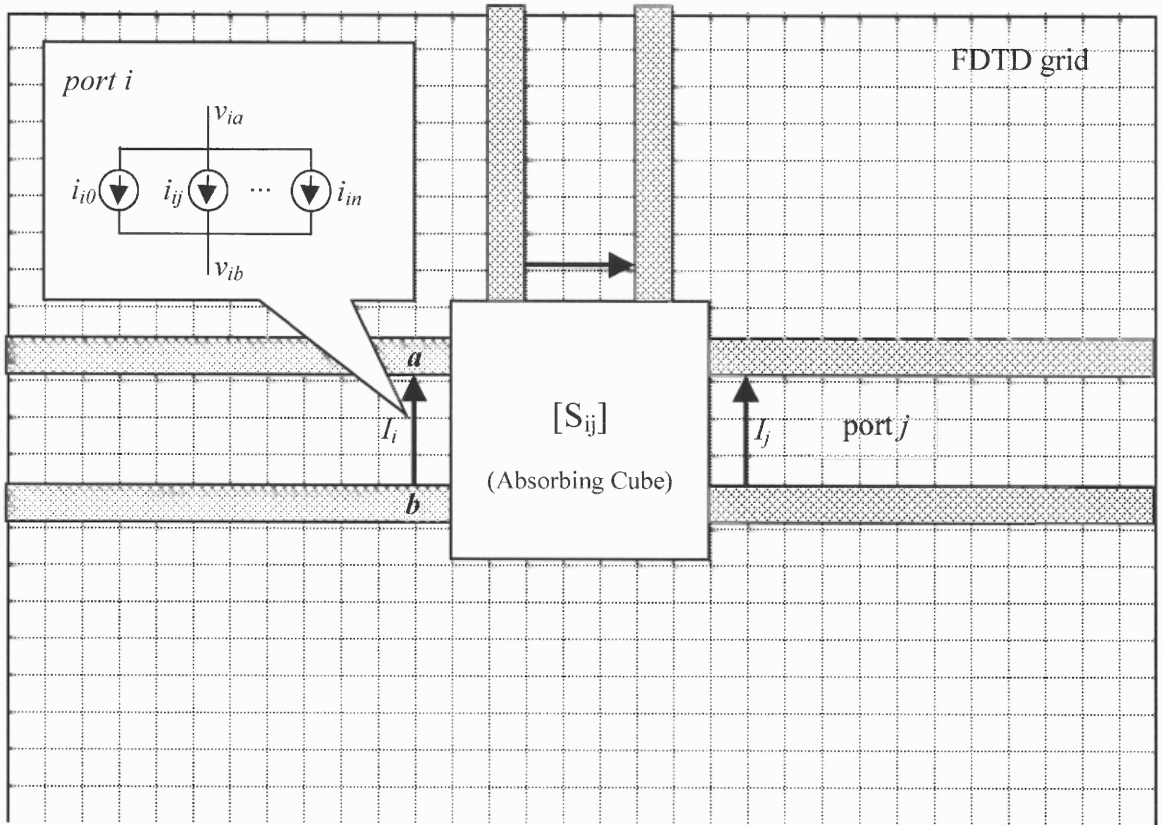
Figure 4.2. An n-port system is connected within a FDTD grid through sections of transmission line. Nodes a and b are the connecting points for port i. Electric field components along path ab are updated using Equation (4.9). The inlet shows the sum of current at this port where i_{ij} is current contribution from port j.

current are, in general, related to the electric and magnetic field, port voltage can be calculated by the following static equation

$$v_{ba} = -\int_a^b E \cdot dl \tag{4.9}$$

or in FDTD approximation

$$v_{ba}^i(t^k) = \sum_{j=j_b}^{j=j_a} E_{zijk}^{t^k}(\delta z_j) \tag{4.10}$$

where integral path is assumed along z direction for electric field E_{zijk} across point a and point b. Current can also be related to magnetic field, but it is usually calculated by the current/voltage relation of the modeling system.

By definition, frequency-domain scattering parameters of an n-port are defined as

$$
\begin{bmatrix}
v_-^1 \\
v_-^2 \\
\vdots \\
v_-^{n-1} \\
v_-^n
\end{bmatrix}
=
\begin{bmatrix}
s_{11} & s_{12} & \cdots & s_{1n-1} & s_{1n} \\
s_{21} & s_{22} & \cdots & s_{2n-1} & s_{2n} \\
\vdots & \vdots & \vdots & \vdots & \vdots \\
s_{n-11} & s_{n-12} & \cdots & s_{n-1n-1} & s_{n-1n} \\
s_{n1} & s_{n2} & \cdots & s_{nn-1} & s_{nn}
\end{bmatrix}
\begin{bmatrix}
v_+^1 \\
v_+^2 \\
\vdots \\
v_+^{n-1} \\
v_+^n
\end{bmatrix}
\tag{4.11}
$$

or

$$V_- = SV_+ \tag{4.12}$$

where superscript i is the index for each port, and subscripts - and + refer to reflected and incident signals, respectively.

Assuming a system represented by matrix S in Equation (4.11) is connected through a lossless transmission line to the distributed system, it can be shown that the incident and reflected voltage and current at each port are related to port voltage and current by the following equations

$$v_-^i = v^i - Z_0^i i^i \tag{4.13}$$

$$v_+^i = v^i + Z_0^i i^i \tag{4.14}$$

where Z_0^i is the characteristic impedance of the connecting lossless transmission, voltage and current without subscript stand for their corresponding variables at each port [11]. Equations (4.13, 4.14) are illustrated in Figure 4.1 where relationship between port voltage and incident and reflected ones is shown.

Eliminating variables v_+^i and v_-^i by combining Equations (4.11, 4.12) and (4.13, 4.14), voltage at each port is therefore the sum of the contributing factors from all the ports.

$$v^i = Z_0^i i^i + \sum_{j=1}^n s_{ij}(v^j + Z_0^j i^j) \tag{4.15}$$

These equations can be easily converted to time-domain as convolution equations

$$v^i(t) = Z_0^i i^i(t) + \sum_{j=1}^n h_{ij}(t) \otimes (v^j(t) + Z_0^j i^j(t))$$

$$= Z_0^i i^i(t) + \sum_{j=1}^n \int_{-\infty}^t h_{ij}(\lambda)(v^j(\lambda) + Z_0^j i^j(\lambda))d\lambda \tag{4.16}$$

or

$$i^i(t) = y_0^i v^i(t) - \sum_{j=1}^{n} \int_{-\infty} h_{ij}(\lambda - t)(y_0^j v^j(\lambda) + \frac{y_0^i}{y_0^j} i^j(\lambda)) d\lambda$$

$$\equiv y_0^i v^i(t) - \sum_{j=1}^{n} i_{ij}(t) \tag{4.17}$$

$$= y_0^i v^i(t) - I_i(t)$$

where $y_0{}^i$ is the characteristic admittance of port i, and the time-domain impulse response $h_{ij}(t)$ is the inverse Fourier transform of its frequency-domain counterpart $s_{ij}(f)$.

$$h_{ij}(t) = FFT^{-1}[s_{ij}(f)] \tag{4.18}$$

and

$$i_{ij}(t) = \int_{-\infty} h_{ij}(\lambda - t)(y_0^i v^j(\lambda) + \frac{y_0^i}{y_0^j} i^j(\lambda)) d\lambda \tag{4.19}$$

$$I_i(t) = \sum_{j=1}^{n} i_{ij}(t) \tag{4.20}$$

The total current $I_i(t)$ in Equation (4.20) is the algebraic sum of contributions from each of all the ports $(j=1,...,n)$ to port i and they can be modeled as n number of current sources in parallel, as shown in the inlet in Figure 4.2. The induced current $I_i(t)$ is the additional current I_a that should be included in the extended Maxwell's Equation (4.2). Interactions between the distributed system and the s-parameter system are reflected by the discontinuity caused by the additional current located at the port, as illustrated in Figure 4.2.

Direct convolution method requires the complete history of voltage or current at each port, therefore it requires significant amount of computer resources. For most of the physical systems, the impulse responses have finite duration T, implying $h_{ij}(t) \approx 0$ for $t > T$.

Also different kind of extrapolation schemes must be used to expand frequency range and data point for Fourier transformation since most of the measured s-parameter data has limited points at a certain frequency range. These limitations and their effects on simulation result will be discussed in more details in the latter session.

Implementing finite-difference technique to calculate current at each port from Equation (4.19), port current flow at current time step $k+1$ can be determined by the history of voltage and current.

$$
\begin{aligned}
i^i(t^{k+1}) &= y_0^i v^i(t^k) - \sum_{j=1}^{n} \int_{-\infty}^{t^k} h_{ij}(\lambda - t)(y_0^i v^j(\lambda) + i^j(\lambda))d\lambda \\
&\equiv y_0^i v^i(t^k) - \sum_{j=1}^{n} i_{ij}(t^k) \\
&= y_0^i v^i(t^k) - I_i(t^k)
\end{aligned}
\tag{4.21}
$$

where again the induced current $I_i(t^k)$ in Equation (4.21) accounts for contributions from all the contributing ports.

As shown in Figure 4.2, each port of the n-port system is connected to FDTD cells, where an integral path between the two connecting points defines a voltage, as shown in Equations (4.9, 4.10). Current flow is defined inside the loop for electric field integration. At each port interface, input and output variables for a behavioral model are represented by Equation (4.9). Giving the derivation for s-parameter modeling in FDTD described earlier in this section, any n-port behavioral model can be handled in the same manner. more detailed discussion can be found in [43].

FDTD solution for the electromagnetic field inside the distributed system is stepped through all the time steps for complete time simulation. Voltage and current are therefore updated in every time step along with field variables. These additional calculations can be executed at the end of standard FDTD iteration for electric-magnetic field. To avoid unphysical effects of numerically adding an abstract object inside the discrete grid, or equivalently to make sure the inserted alias object is only described by its mathematical representation, concept of an absorbing cube (square in 2D) is described at the beginning of this section.

4.4 3-D Multi-Port Circuit Modeling in FDTD Field Simulation

To verify the simulation results from the newly developed algorithm, the availability of the other numerical simulation is vital. However, there is no commercial 3-D simulation for whole package to be compared with. A few examples of hybrid circuits, such as 2-port ideal transmission line and amplifier, are simulated to verify the accuracy and stability of the algorithm described earlier in this thesis. All example circuits are modeled in three-dimensional uniform grid, with a cell size of 1mm and time step of 1.667ps for mircrostrip line structure, and with a cell size of 50um for flipchip. The absorbing square is made of four surfaces with Mur's 1st order absorbing boundary condition with the dimensions matching those of the waveguide. S-parameter descriptions used in simulations are obtained either from scanning the modeled device in ADS or from the manufacturer of the device.
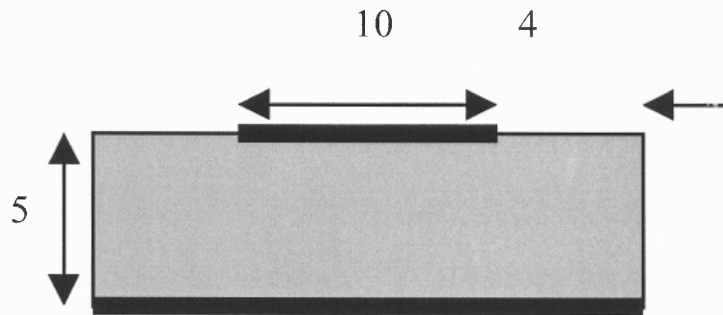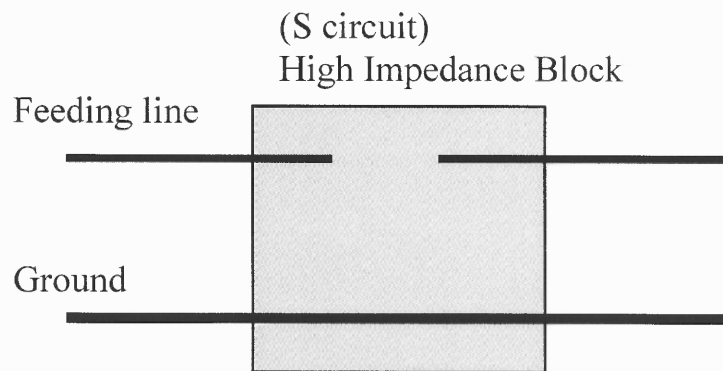
4.4.1 Microstrip line 3D simulation

Microstrip is an important planar microwave component. There is an extensive literature about microstrip. Zhang [59] has studied the dispersive characteristics of microstrip by FDTD method. Sheen also used FDTD to analyze microstrip rectangle antenna [39]. Shorthouse and Railton [41] incorporated static field solutions into the FDTD method for microstrip discontinuities. None of them, however, can give a general method for whole package simulation with microstrip.

This section will use the method described at the beginning of this chapter to study 3-D whole package simulation. 2-port ideal transmission line is used for embedded circuit. Microstrip line is used as host package. The cross section of this package is shown in Figure 4.3. The side view of this package is shown as Figure 4.4, the shadowed square standing for absorbing cube and embedded circuit block. The simulation signal is a gauss pulse, with half width 2×10^{-10} sec. The simulation result is shown in Figure 4.5, V1 and V2 are the voltage behavior at port one and port two. There is no commercial 3-D simulation result for this 2-port ideal transmission line.

The other embedded circuit used for whole package simulation is an HP amplifier. 2-D simulation is obtained, as shown in Figure 4.6. The exciting source is lumped sine wave source, with period 0.4×10^{-9} sec. The 3-D microstrip line simulation is shown in Figure 4.7, hard source is used in this simulation with period 0.4×10^{-9} sec. The relative volume and phase difference for Figure 4.6 and 4.7 are almost the same.

Figure 4.3 the cross section of microstrip structure, top metal layer is feeding line, bottom metal is ground layer, unit is cell size, one cell = 0.001m, dielectric constant =14.3

Figure 4.4 Side view of microstrip line whole circuit simulation structure
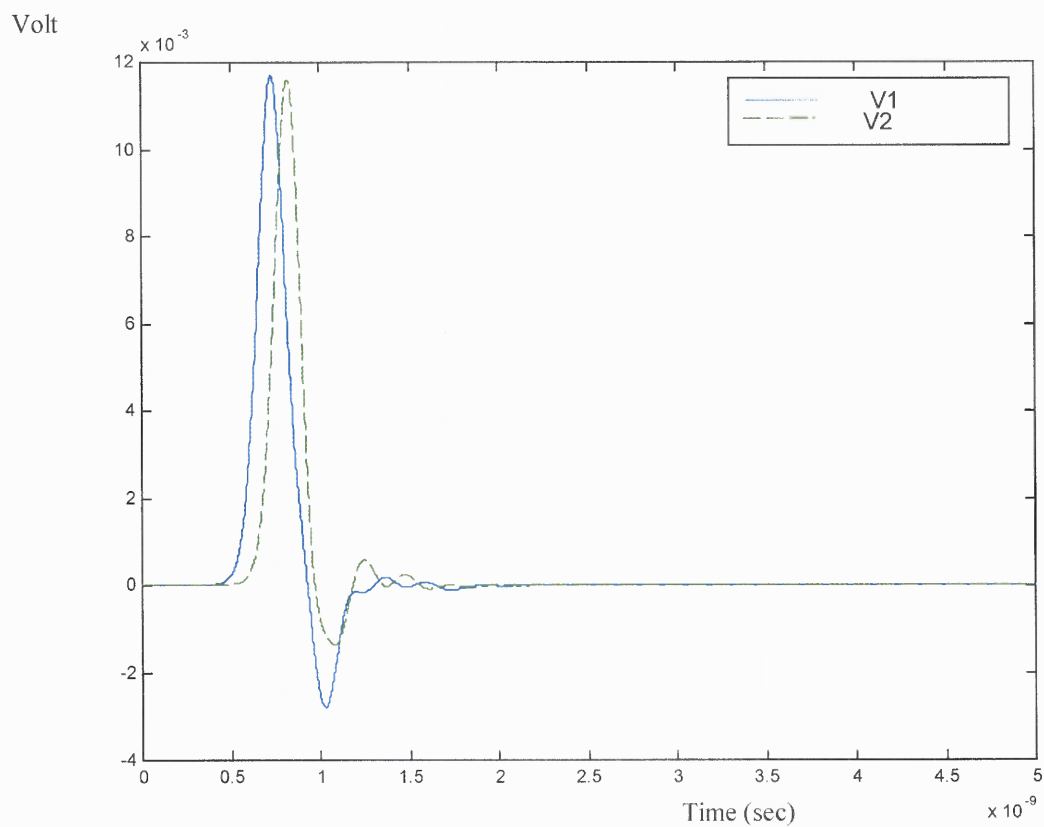
Volt

Figure 4.5 Voltage at two circuit ports of the microstrip line with ideal transmission line
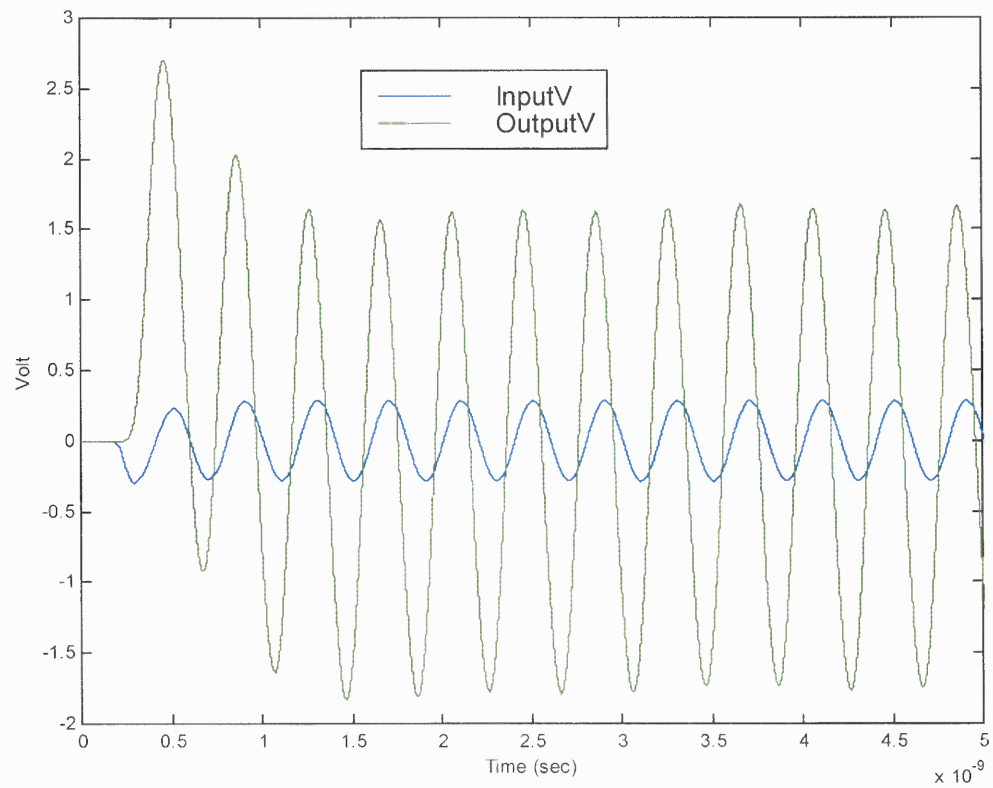
Figure 4.6 Two dimension simulation for two ports with Amplifier Circuit

Figure 4.7 Microstrip line with sine wave hard source, 0.4X10-9, S circuit is a HP

amplifier

4.4.2 Flip Chip 3D simulation

Flip chip package structure is discussed in Chapter 3. The big size flip chip interconnect

is used in this chapter. The ball cross section is 16 X 16 cell. The via size is 4 X 4 cell.

Figure 3.14 has the reflection information for this empty package. An absorbing cube is

added for whole package simulation, as shown in Figure 4.8 and 4.9. The size of this

absorbing cube is about 29 X 54 X 7 cell, which should be the same as the actual circuit.

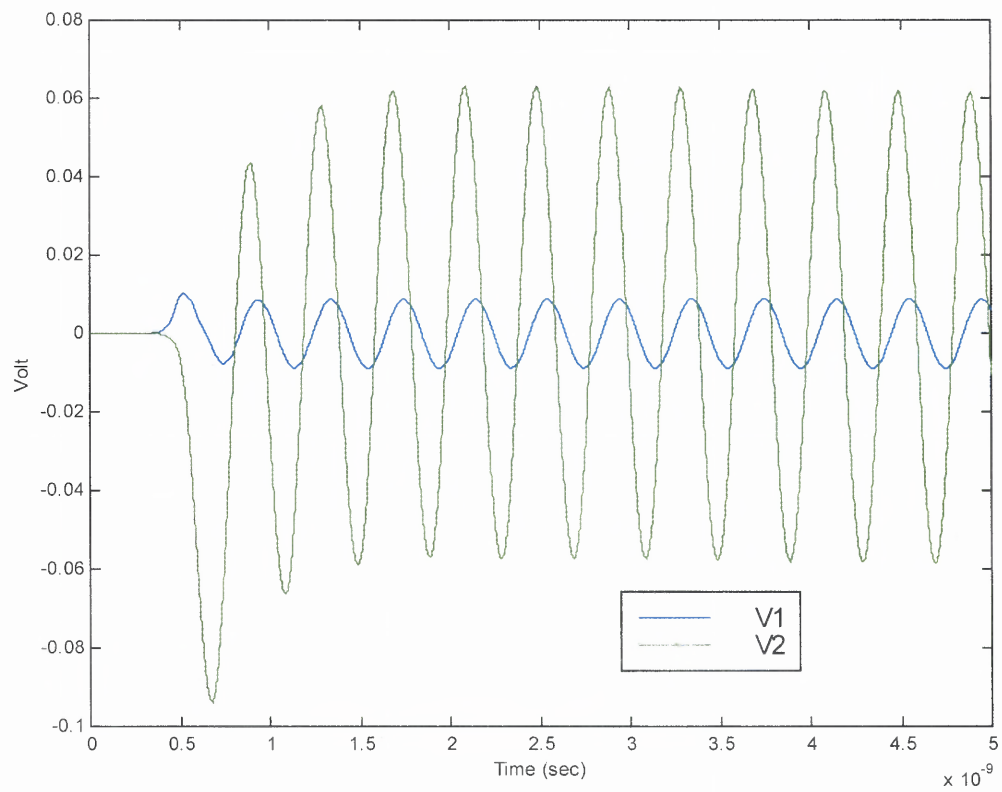The flip chip package modeling is much more difficult than microstrip line because one

flip chip port has two path to ground. The port current consists of two parts that share

different directions. It makes field simulation complicated, as shown in Figure 4.10.

Figure 4.11, which is one curve in Figure 3.14, is the reflection against frequency

for the flip chip used for this section without embedded circuit. The package has good

transition performance from DC to 30GHz. The average reflection loss is below 20dB.

The flip chip interconnects and embedded circuit should be processed at the same time

when whole package simulation is started. In another word, the whole package simulation

result should have both flip chip interconnect information and embedded circuit

information. The voltage distributions for embedded circuit ports and input and output of

whole package have all the necessary information according to whole package simulation

principle.

The first frequency of input signal source is 2.5 GHz. The embedded circuit is a HP

amplifier. The flip chip interconnect has a very good transition at 2.5GHz, which is 30dB

according to Figure 4.11. The voltages at circuit ports are shown in Figure 4.12.
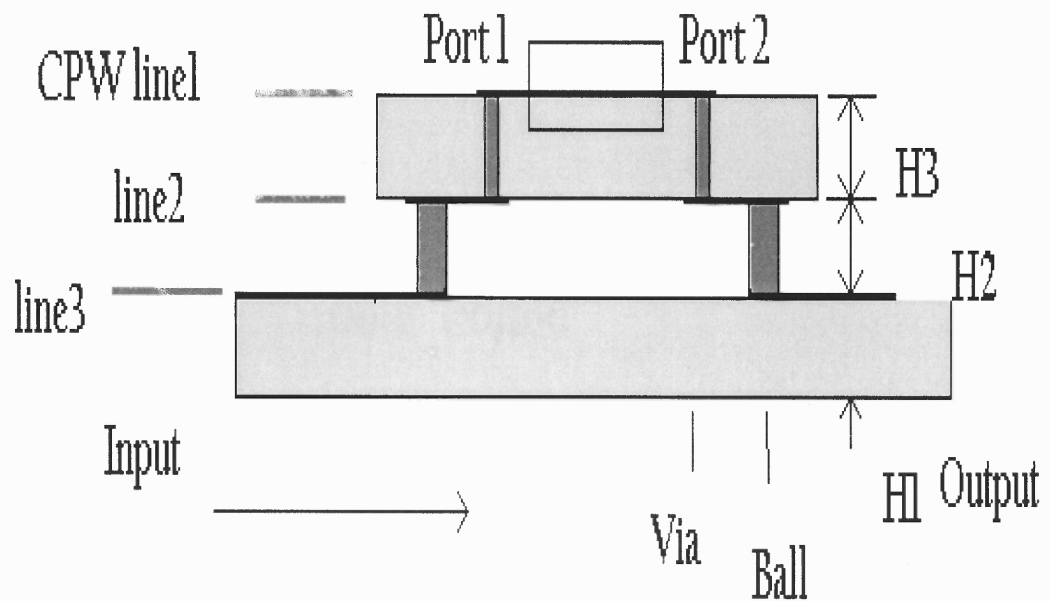
Figure 4.8 Side view of the three-layer structure. H1, H2, and H3 are 15 mils. The single arrow stands for the signal feeding direction, while the upper cube is the absorbing cube and S circuit for whole package simulation
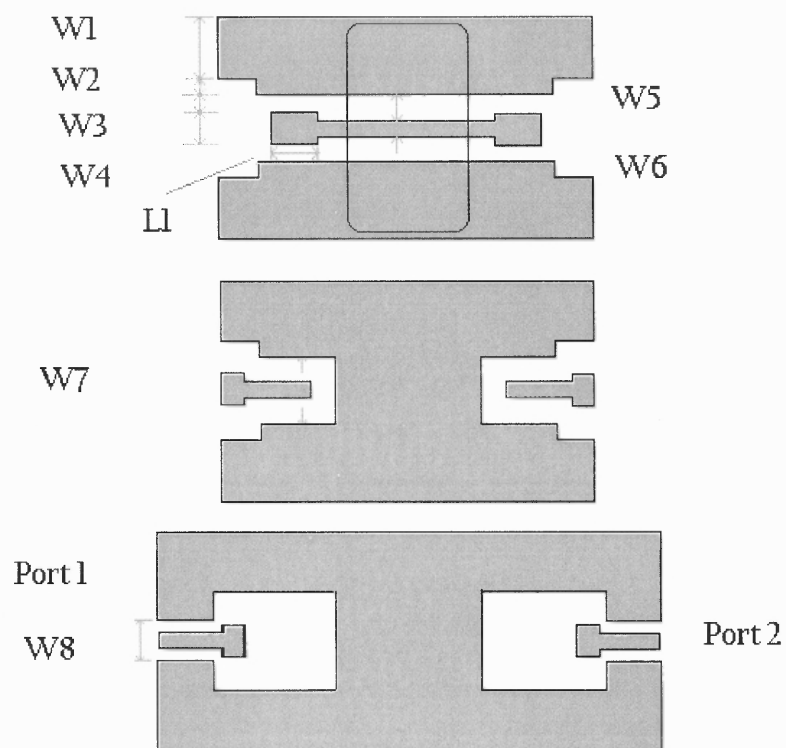
Figure 4.9 Top view of three CPW layers. W1, W2, W3 and W4 are 30, 10, 6, and 16 mils, respectively. The upper cube is the absorbing cube.
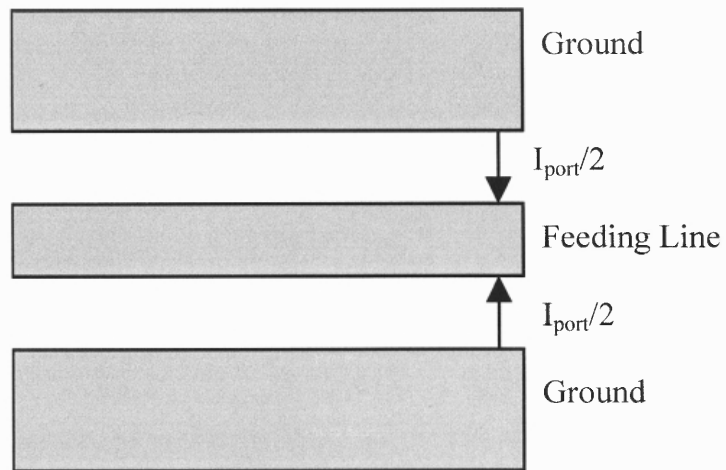
Figure 4.10 The circuit port on flip chip interconnect. I_{port} is the port current.

S11

Figure 4.11 FDTD simulation of flip chip package without embedded circuit.

Figure 4.12 Voltage distribution on the two ports of embedded amplifier circuit mounted on flip chip package.

The voltages at whole package input and out put ports are shown in Figure 4.13. These two figures are almost the same except a small phase difference at the beginning, which cause by transmission line. The loss for this package is very small at 2.5 GHz working frequency.

The second frequency of input signal source is 36GHz. The embedded circuit is ideal transmission line with 2×10^{-11} sec delay. The flip chip interconnect has 15dB transition at 36GHz according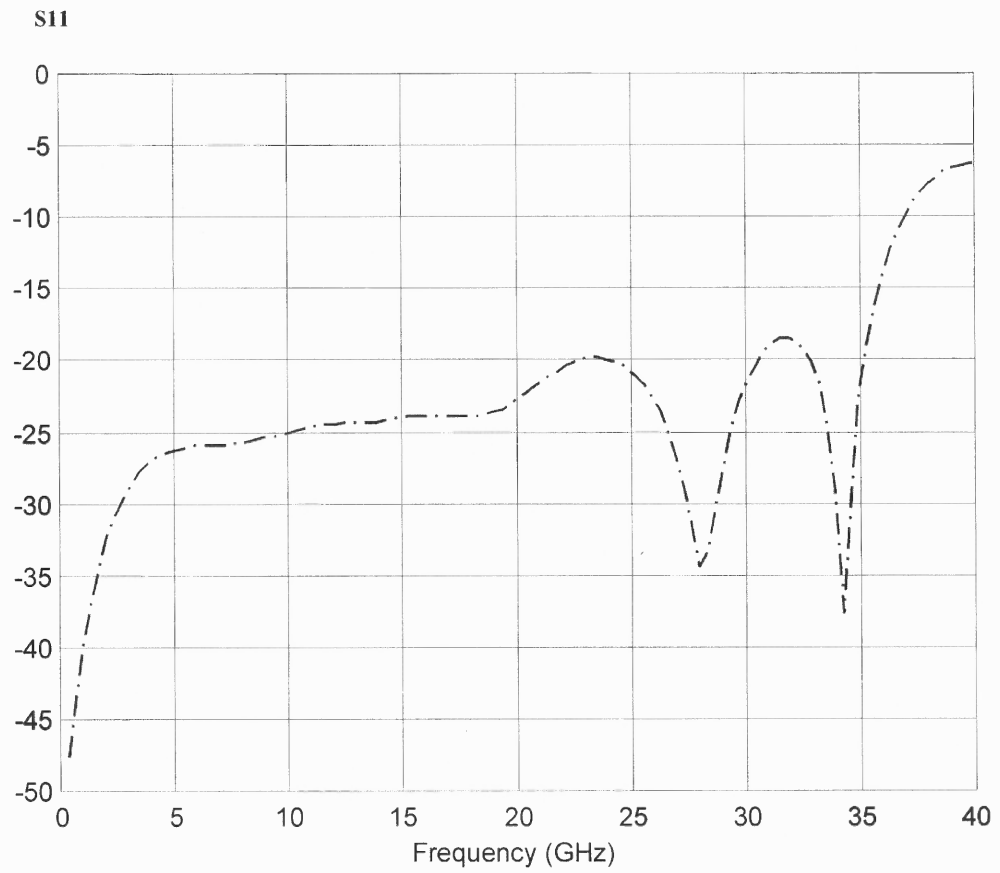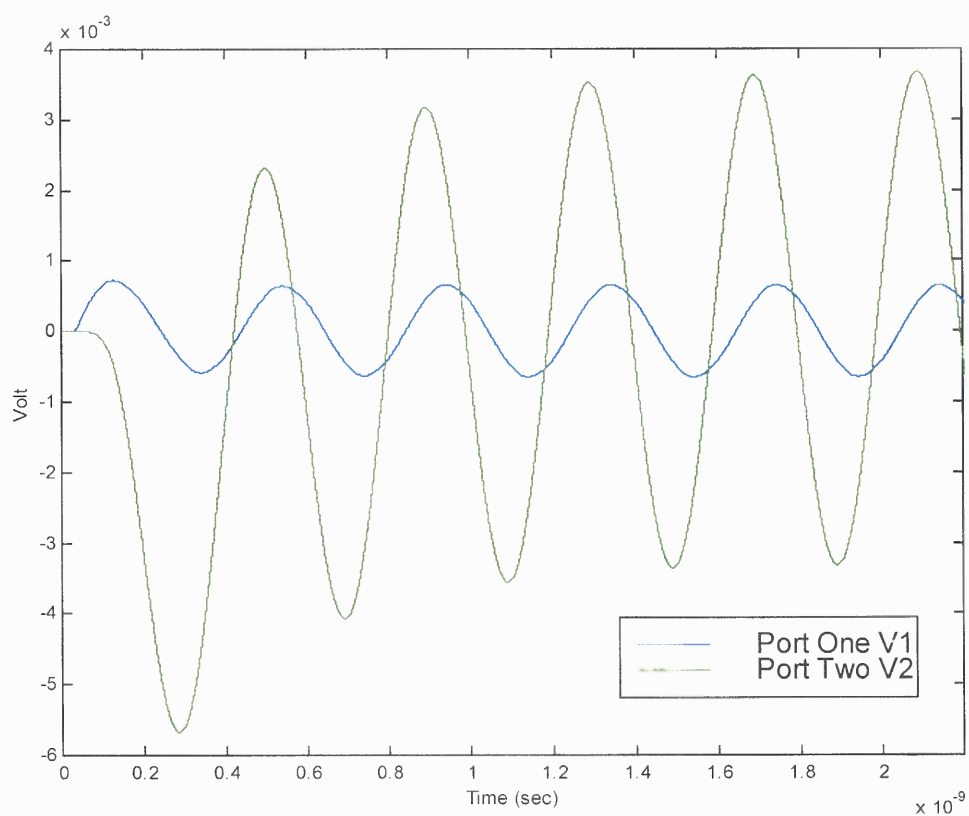 to Figure 4.11. The voltages at circuit ports, package input and output ports, are shown in Figure 4.14 and 4.15. The outstanding phase difference can be found as the signal frequency become higher. The package input voltage are stronger than output. It means this package can cause the big loss for the 36 Ghz signal, which can be also proved by Figure 4.11.

The third simulation uses 28 GHz sine wave source, and a shifted HP amplifier. The flip chip interconnect has 33 dB transition at 28 GHz. Figure 4.16 and 4.17 are the voltage distribution of embedded amplifier ports and whole package input and output ports. There is also outstanding phase difference as the case with ideal transmission line at 36 GHz, but its transient time is much longer that the other case, about 5×10^{-10} sec, which is still a small time value for amplifier.

4.5 Conclusions

3-D whole package FDTD simulation is first implemented in this chapter. 2-D simulation is used as the reference standard because there is no 3-D whole package simulation to
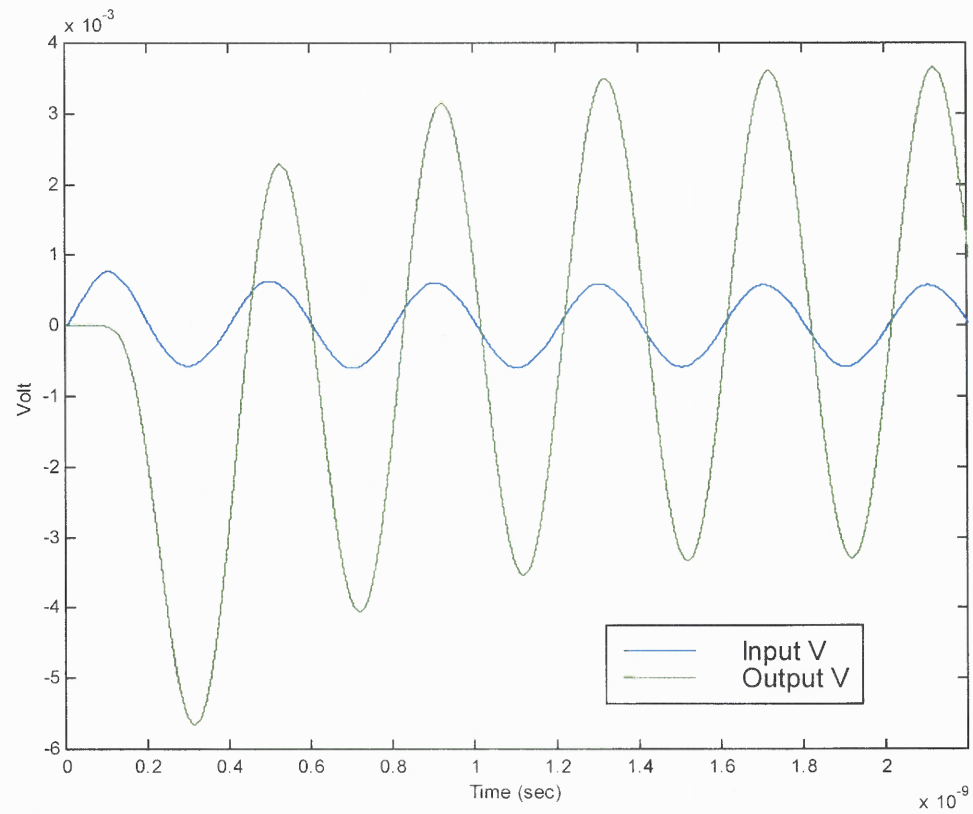
Figure 4.13 Input and output simulation of whole flip chip package with mounted amplifier
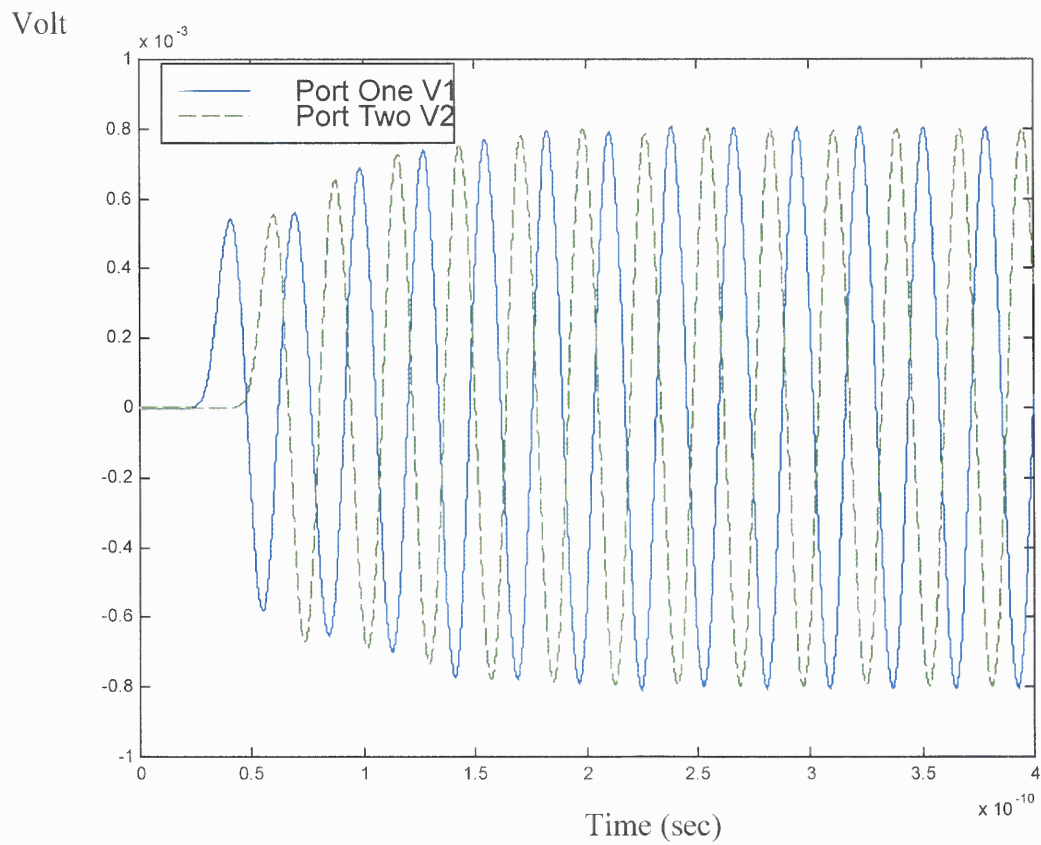
Figure 4.14 Voltage distribution at port one and two of ideal transmission line embedded in flip chip package with sine wave source, frequency=36GHz
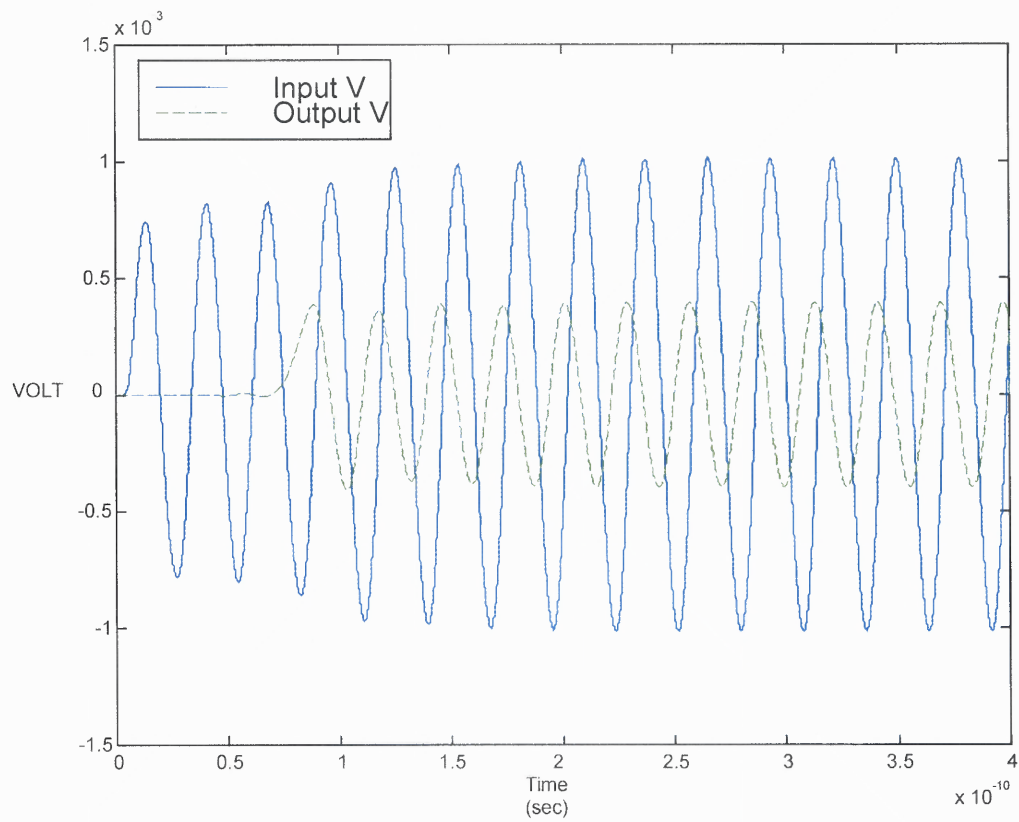
Figure 4.15 Voltage distribution at package input and output ports of flip chip package with embedded ideal transmission line, the frequency of sine wave form =36GHz
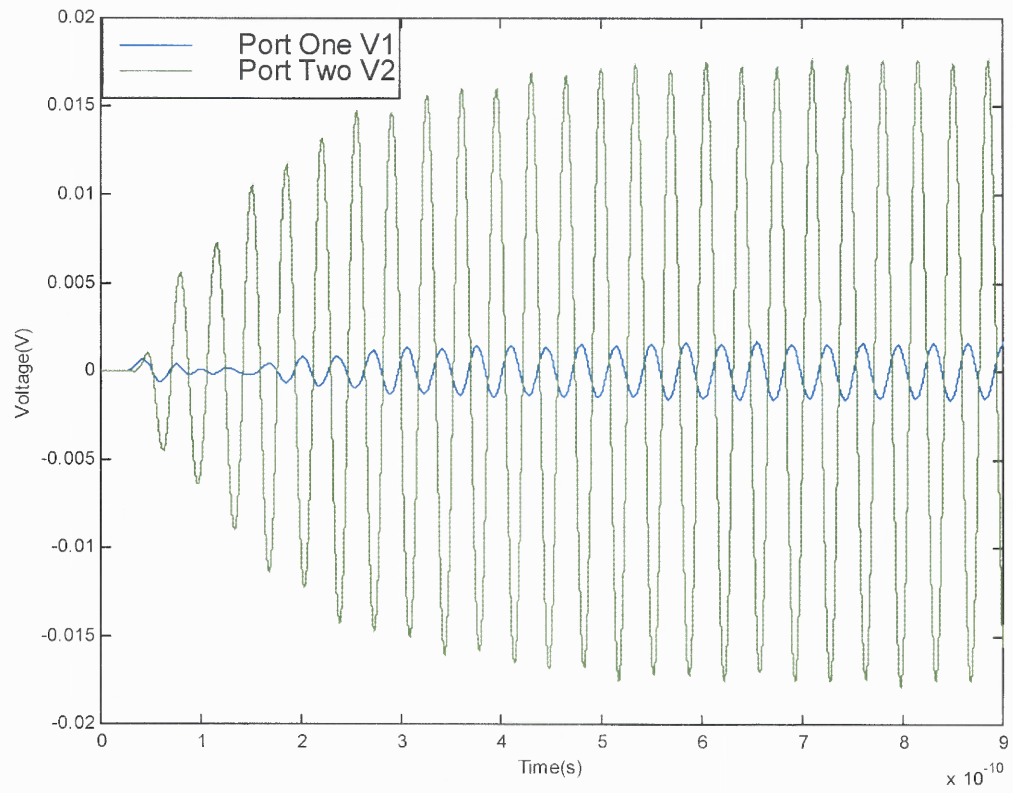
Figure 4.16 Port voltage of HP amplifier embedded in flip chip package with 28GHz sine wave source
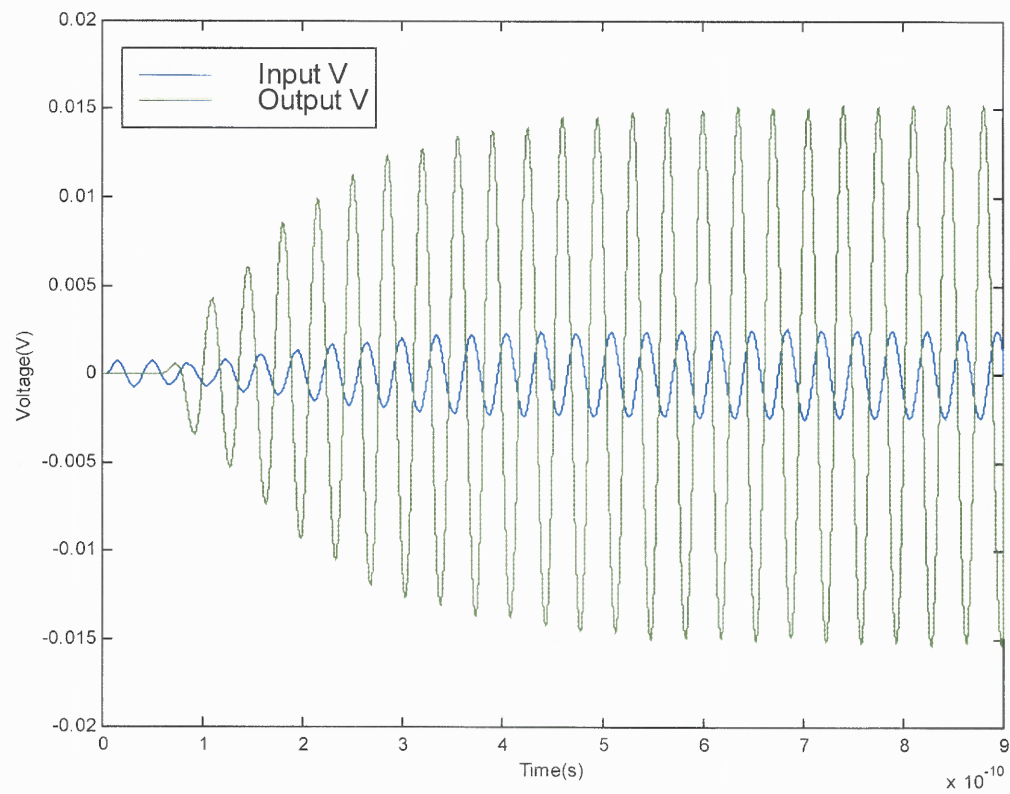
Figure 4.17 Input and output voltage of whole flip chip package with embedded HP amplifier, sine wave source frequency is 28GHz

compare with at present time. The excellent results indicate the concept of the absorbing cube is suitable and effective. It solved the previous uncertainty about the size of the added lumped system and it actually agrees with the definition of a lumped element. The absorbing cube can be applied to general modeling of any system that possesses "lumped" feature.

Microstrip and flip chip planar packages with on-chip circuit are first studied by FDTD whole package simulation. The embedded circuit port has two grounds for flip chip, so special processing is need during FDTD simulation. Chapter 3 is also part of 3-D whole package FDTD simulation. Package interconnect is very import to whole package simulation. Interconnect simulation can be used to find what the working frequency range is available so appropriate circuit will be chosen. Whole package with on-chip circuit FDTD simulation is used to simulate in a wideband, which is from DC to 40 GHz. All these show that whole package with on-chip circuit FDTD simulation is an emerging technique. Single on-chip circuit is used in this thesis, but there could be as many as the real design need according to the basic theory introduced at the beginning of this chapter.

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