ABSTRACT

CURRENT-VOLTAGE CHARACTERISTICS OF $TaSi_2$/Si AND MOS DEVICES USING LABVIEW™

Analyses of current-voltage (I-V) characteristics of Schottky Barrier Diodes (Tantalum Silicide) and Metal Oxide Semiconductor (MOS) Devices, using LabVIEW™, has been presented here. LabVIEW™, a graphical program development application, has been used to program a computer-driven Keithley Source Measure Unit (SMU) for device characterization. The SMU, which can be used as a Source Voltage – Measure Current as well as Source Current – Measure Voltage instrument, is used in the Source Voltage – Measure Current mode in this study. A General Purpose Interface Bus (GPIB) IEEE 488.2 has been used to interface the SMU with LabVIEW™. LabVIEW™ has been successfully implemented to obtain the current-voltage characteristics of semiconductor devices, such as $TaSi_2$ /Si and MOS structures. Based on this characterization, factors such as the barrier height for $TaSi_2$ /Si and current conduction mechanisms in MOS device structures have been evaluated.

CURRENT-VOLTAGE CHARACTERISTICS OF $TaSi_2$/Si AND MOS DEVICES USING LABVIEW™

by
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APPROVAL PAGE

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To My Parents

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CHAPTER 1

INTRODUCTION

The primary thrust of this study is on the I-V characteristics of devices such as Metal Semiconductor Contacts and MOS capacitors. The current-voltage technique has been used to determine the properties of these devices such as their barrier height and current conduction mechanism. In Chapter 2, an introduction is given to energy-band diagrams of the ideal Metal Semiconductor Contact and the MOS capacitor. This is followed by their properties and an overview of their characteristics along with the important methods for electrical characterization. These include the four-point probe method, capacitance-voltage method, deep-level transient spectroscopy and the current-voltage method. Since the last named method has been used for characterization in this study, it is discussed in more detail.

Chapter 3 introduces the concept of graphical programming with LabVIEW^{TM}, which has been used as the software programming tool for obtaining the I-V characteristics. The application of LabVIEW^{TM} to device characterization in general is also presented here. The Source Measure Unit (SMU) communicates with the Device Under Test (DUT) and is the principal instrument used for obtaining the I-V characteristics. The working of the instrument and its modes of operation are presented in Chapter 4.

Chapter 5 deals with the results and discussion of the I-V characteristics. The conclusions of this study are presented in Chapter 6. The conclusions of this study are presented in Chapter 6. Appendix A contains the LabVIEW^{TM} program, Appendix B lists the device-dependent commands of the Source Measure Unit and Appendix C shows the

GPIB IEEE 488.2 common commands, queries, and compliance requirements. Appendix D summarizes the programming and the simulation of I-V characteristics of Metal Semiconductor Contacts.

CHAPTER 2

OVERVIEW OF METAL-SEMICONDUCTOR CONTACTS AND MOS TECHNOLOGY

2.1 Metal-Semiconductor Contacts

Metal-semiconductor contacts are an integral part of every semiconductor device. The rectifying metal-semiconductor junction or Schottky barrier has numerous uses as a high-speed switching device, while the special case of the Ohmic contact is used to interface semiconductor devices to the outside world.

2.1.1 Energy-Band Relation

If a metal and an n-type semiconductor are brought into intimate contact, electrons will flow from the side of the higher energy level (metal) to the other side (semiconductor) since both Fermi energies must be equal. This phenomenon is illustrated as two limiting cases in Figure 2.1.

Fig 2.1(a) shows the electronic energy relations at an ideal contact between a metal and an n-type semiconductor in the absence of surface states. At the far left, the metal and semiconductor are not in contact, and the system is not in thermal equilibrium. If the metal and the semiconductor are brought in contact, charges will flow between them and thermal equilibrium is established, and the Fermi levels line up on both sides. Relative to the Fermi level in the metal, the Fermi level in the semiconductor is lowered by an amount equal to the difference between the two work functions. The second limiting case is shown in Fig. 2.1 (b), where a large density of surface states is present on the semiconductor surface.

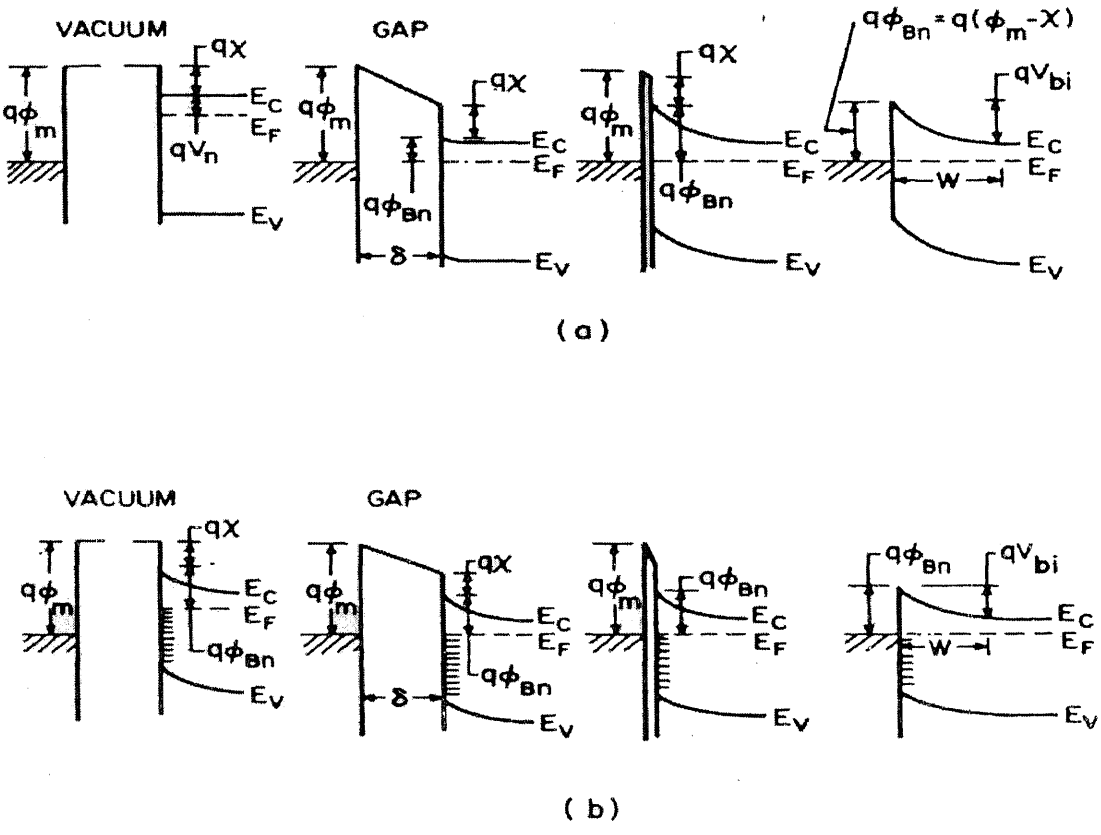


Fig. 2.1 Energy-band diagrams of metal-semiconductor contacts[1]

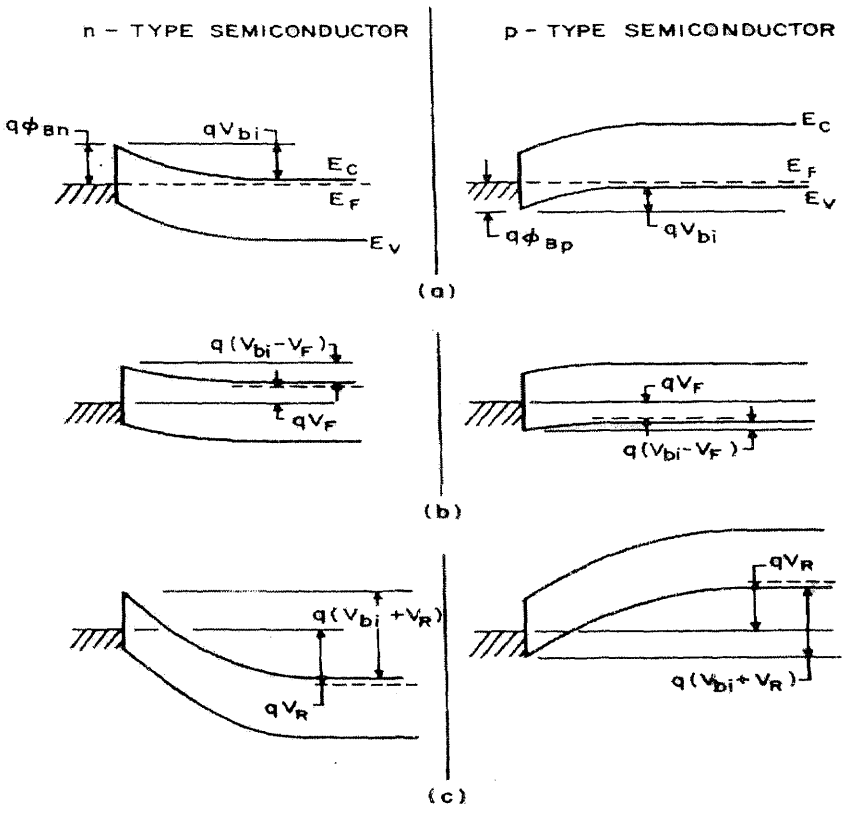


Fig. 2.2 Energy-band diagram of metal/n-type and metal/p-type semiconductors under different biasing conditions (a) Thermal equilibrium. b) Forward bias. (c) Reverse bias [2].

At the far left, the figure shows equilibrium between the surface states and the bulk of the semiconductor but non-equilibrium between the metal and the semiconductor. In this case, the states are occupied to the Fermi level E_F. When the metal-semiconductor system is in equilibrium, the Fermi level of the semiconductor relative to that of the metal must fall by an amount equal to the contact potential and, as a result, an electric field is produced in the gap δ. The energy-band diagrams for metals on both n-type and p-type semiconductor materials, for different biasing conditions are shown in Fig. 2.2. Fig. 2.2 (a) shows the thermal equilibrium state, Fig. 2.2 (b) shows the forward bias state and Fig.2.2 (c) shows the reverse bias state.

2.1.2 The Schottky Barrier

As described in Fig. 2.1 above, when a metal is in contact with a semiconductor, the Fermi levels in the two materials must be coincident at thermal equilibrium. Thus, relative to the Fermi level in the metal, the Fermi level in the semiconductor is lowered by an amount equal to the two work functions. This potential difference or contact potential is given by[3] :

$$q\phi_m - q(\chi + V_n)$$

Where q is the electronic charge, ϕ_m is the metal work function, χ is the electron affinity of the semiconductor measured from the bottom of the conduction band and V_n is the Fermi potential relative to the conduction band edge.

As the metal is brought closer to the semiconductor, an increasing charge is built up at the metal surface and an equal and opposite positive charge must exist in the semiconductor. When the gap between the metal and the semiconductor decreases to interatomic distances, the metal-semiconductor contact is formed. The limiting barrier (neglecting image effects) is given by:

$$q\phi_{Bn} = q(\phi_m - \chi)$$

Similarly, for a p-type semiconductor, the barrier height is given by:

$$q\phi_{Bp} = E_g - q(\phi_m - \chi)$$

The sum of the barrier heights of a metal contact on a given semiconductor material is equal to the bandgap. In the above equations, ϕ_{bn} is the Schottky barrier height on an n-

type semiconductor, ϕ_{bp} is the Schottky barrier height on a p-type semiconductor and E_g is the energy-gap of the semiconductor.

$$q(\varphi_{Bn} + \varphi_{Bp}) = E_g$$

The difference in Fermi levels before contact is the contact potential difference; this difference in reference to the semiconductor energy gap is theoretically the height of the barrier between the two materials. In practice, there is little correlation between measured and theoretical barrier heights: this is due to a permanent layer of trapped charge at the semiconductor surface, which affects the barrier height.

2.1.3 Properties of the Schottky Barrier

The carrier flow across a metal-semiconductor interface can be affected by the application of a voltage, which decreases or increases the Fermi level depending upon its polarity[4]. A metal-semiconductor contact can also be utilized as an optical detector (photo absorption) where photons are absorbed by band-to-band transitions and the resulting electron-hole pairs are collected. Another important property of the Schottky barrier is photoemission from metal. In this case, photons are transmitted through the semiconductor and are absorbed in the metal adjacent to the barrier. A fraction of the excited electrons will surmount the barrier, flow into the semiconductor, and be collected. The spectral response is bound by two limiting photon energies – a lower threshold given by the barrier height ($h\nu_{min} = q\varphi_{MS}$) and an upper threshold determined by transmission through the semiconductor ($h\nu_{min} = E_g$). The characteristic features of a Schottky barrier diode can be summarized as:

- It has nearly ideal characteristics in all respects, including capacitive, transport, and optical properties.
- Minority carrier injection and charge storage effects can essentially be eliminated. For a given semiconductor, the barrier height can be varied over a wide range by proper choice of the metal.

2.2 MOS Technology

The MOS Capacitor is the most basic device in the study of semiconductor surfaces and in the production of semiconductor circuits. The reliability and stability of key semiconductor devices such as Very Large Scale Integrated Circuits (VLSI), are sensitive to MOS surface conditions. An understanding of the various physical mechanisms in MOS capacitors is of great importance to device operations. In the ideal MOS structure shown in Fig.2.3, voltage V is applied on the metal field plate and the thickness of the insulator is given by *d*. Conventionally, the voltage V is positive when the metal plate is positively biased with respect to the Ohmic contact, and negative when the metal plate is negatively biased with respect to the Ohmic contact.

2.2.1 The Ideal MOS Capacitor

The energy band diagrams of an ideal MOS structure of a semiconductor for V = 0 are shown in Figure 2.4. For an ideal MOS diode, the energy difference between the metal work function ϕ_m and the semiconductor work function is zero, or the work-function difference ϕ_{ms} is zero[2]:

$$\phi_{ms} = \phi_m - (\chi + \frac{E_g}{2q} - \psi_B) = 0 \qquad \text{for n-type}$$

$$\phi_{ms} = \phi_m - (\chi + \frac{E_g}{2q} + \psi_B) = 0 \qquad \text{for p-type}$$

where ϕ_m is the metal work function, χ the semiconductor electron affinity, χ_i the insulator electron affinity, E_g the bandgap, ϕ_B the potential barrier between the metal and the insulator, and ψ_B the potential difference between the Fermi level E_F and the intrinsic Fermi level E_i.

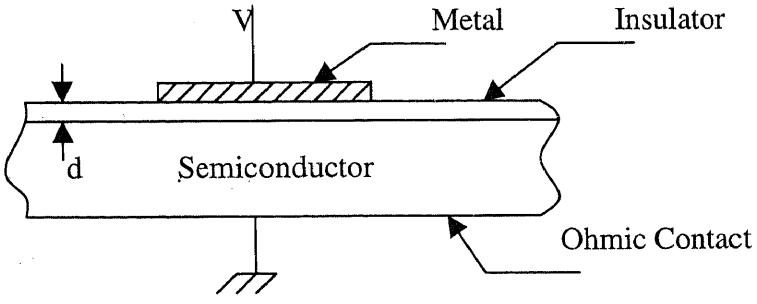


Fig.2.3 Metal-oxide-semiconductor (MOS) diode

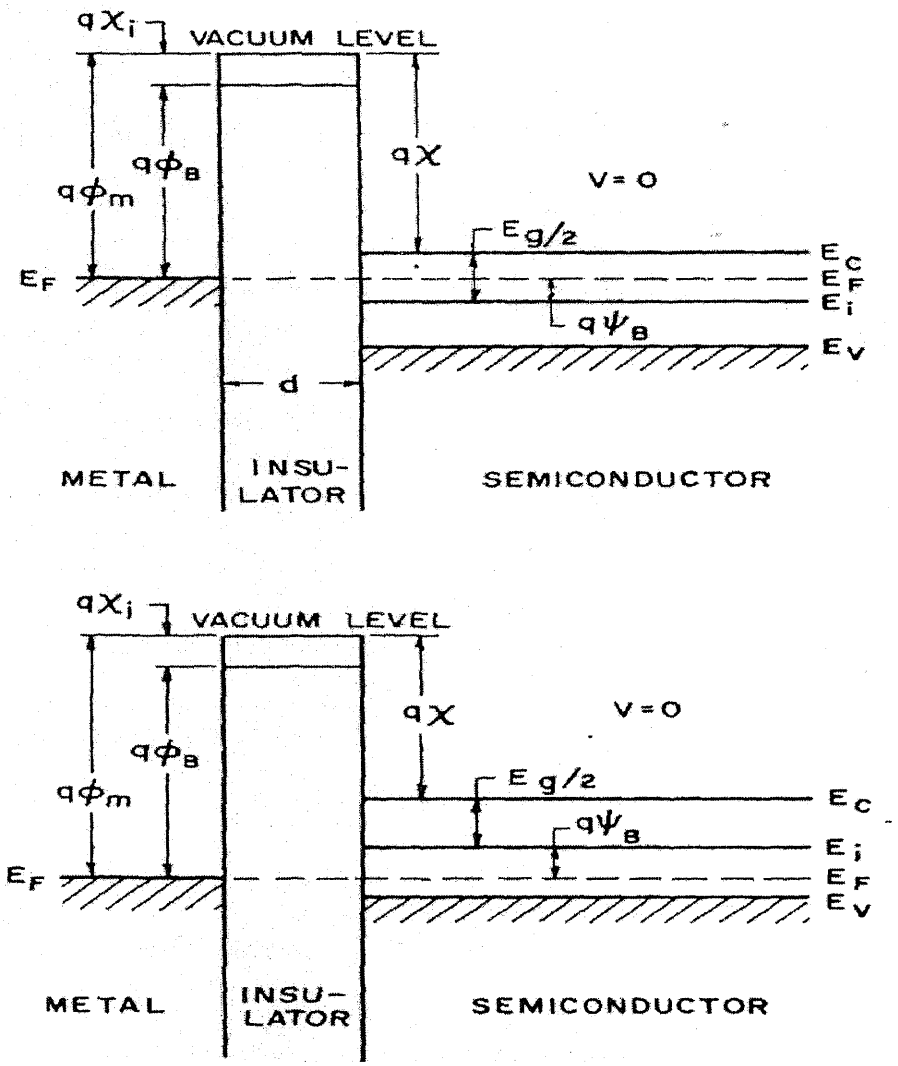


Fig. 2.4 Energy-band diagrams of ideal MOS diodes at V = 0. (a) n - type semiconductor (b) p - type semiconductor.

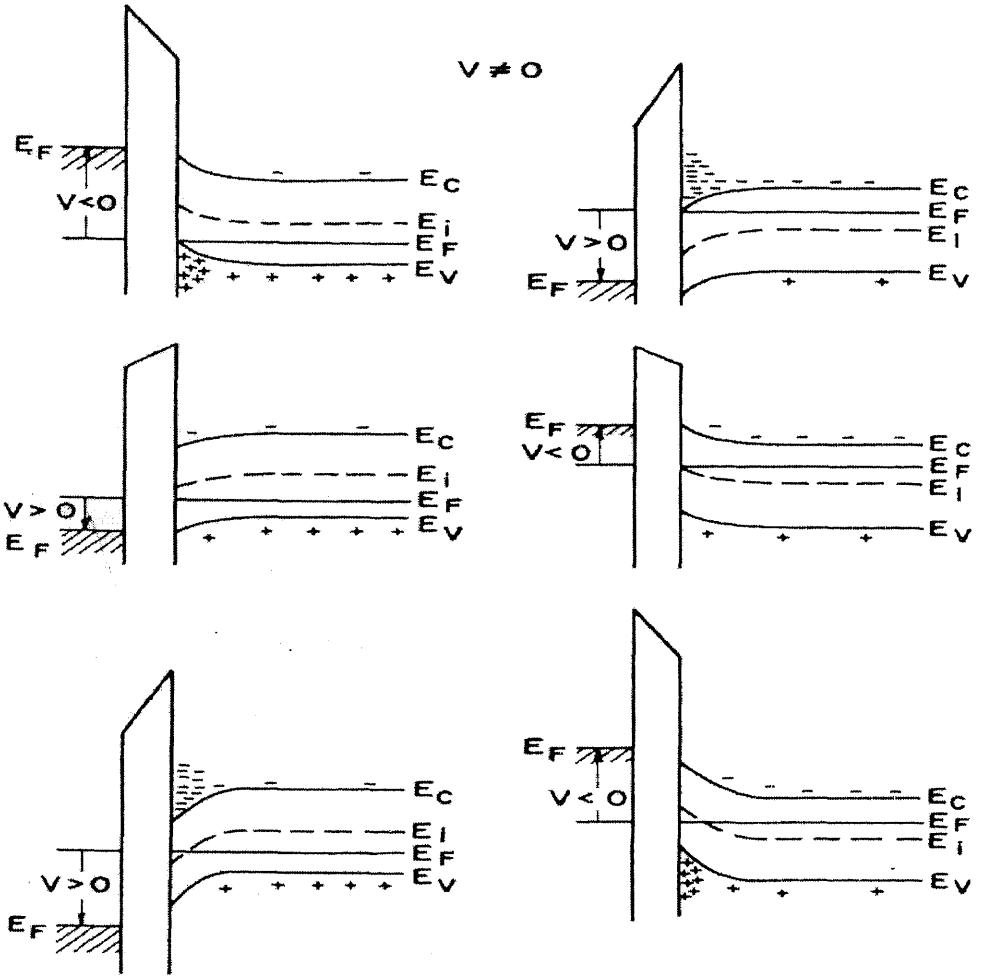


Fig. 2.5 Energy-band diagrams for ideal MOS diodes when V ≠ 0, for the following cases: (a) accumulation (b) depletion (c) inversion[1].

Thus, when there is no applied voltage, a flat-band condition exists, and the only charges that are present in the structure are those in the semiconductor and those with equal and opposite sign on the metal surface adjacent to the insulator. Under dc biasing conditions, there is no carrier transport through the insulator. In other words, the resistivity of the insulator is infinity.

When the ideal MOS diode is biased with positive or negative voltages, basically three cases may exist at the semiconductor surface as shown in Figures 2.5.

When a negative voltage ($V < 0$) is applied to the metal plate, the top of the valence band bends upward and is closer to the Fermi level (Fig.2.5(a)). For an ideal MOS diode, no current flows in the structure, so the Fermi level remains constant in the semiconductor. Since the carrier density depends exponentially on the energy difference, ($E_F - E_V$), this band bending causes an accumulation of the majority carriers (holes) near the semiconductor surface. This is the accumulation phase. When a small positive voltage ($V > 0$) is applied, the bands bend downward, and the majority carriers are depleted (Fig.2.5(b)). This is the depletion case. When a larger positive voltage is applied, the bands bend even more downward so that the intrinsic level E_i at the surface crosses over the Fermi level E_F. At this point the number of electrons (minority carriers) at the surface is larger than that of the holes, the surface is thus inverted, and this is the inversion case (Fig.2.5(c)).

2.3 Electrical Characterization Methods

Electrical characterization involves determining device parameters such as resistivity, barrier height, sheet resistance, etc. Basically, four techniques are used to determine these parameters: the Four-point Probe, Capacitance-Voltage, Current-Voltage, and the Deep-Level Transient Spectroscopy methods. Each one of them is examined here.

2.3.1 The Four-Point Probe

The four-point probe technique is one of the most common methods for measuring the semiconductor resistivity. In this method, the two outer probes carry the current and the inner two probes are used for voltage sensing. The probes are generally arranged in-line

with equal probe spacing. But other probe configurations are possible. The use of four probes has important advantages over two probes. Although the two current-carrying probes still have contact and spreading resistance associated with them, that is not true for the two voltage probes because the voltage is measured either with a potentiometer which draws no current at all or with a high impedance voltmeter which draws very little current.

The potential V at a distance r from an electrode carrying a current I in a material of resistivity ρ is given by the relationship[5] :

$$V = \frac{\rho I}{2\pi r}$$

For a four-probe system with current entering probe 1 and leaving probe 4, the voltage V becomes:

$$V = \left(\frac{\rho I}{2\pi}\right)\left(\frac{1}{r_1} - \frac{1}{r_2}\right)$$

Where r_1 and r_2 are the distances between the probes.

Therefore, the resistivity ρ is given by:

$$\rho = 2\pi s\left(\frac{V}{I}\right)$$

Where s is the equal distance between the probes.

Sheet resistance

Thin layers are characterized by their sheet resistance ρ_s expressed in units of Ohms per square. The sheet resistance is given by[5]:

$$\rho_s = \frac{\rho}{t} = \left[\frac{\pi}{\ln(2)}\right]\left(\frac{V}{I}\right) = 4.532\left(\frac{V}{I}\right)$$

Subject to the thickness t ≤ s/2. The sheet resistance is frequently used to characterize thin semiconductor sheets or layers, such as diffused ion-implanted layers, polycrystalline silicon, and metallic conductors.

2.3.2 Capacitance – Voltage Measurements

The Capacitance – Voltage (C-V) technique relies on the fact that the width of a reverse-biased space-charge region (scr) of a semiconductor device depends on the applied voltage. This scr width dependence voltage is the basis of the C-V technique. The C-V profiling method has been used with the Schottky barrier diodes using metal and liquid electrotype contacts, pn junctions, MOS capacitors, and MOSFETs[5]. Consider a Schottky barrier diode with p-type semiconductor with doping concentration N_A as shown in Fig. 2.6. If a dc bias V is applied to the metal contact, the reverse bias produces a space-charge region of width W. Then the capacitance is defined by[5]:

$$C = \frac{-dQ_S}{dV} \tag{2.1}$$

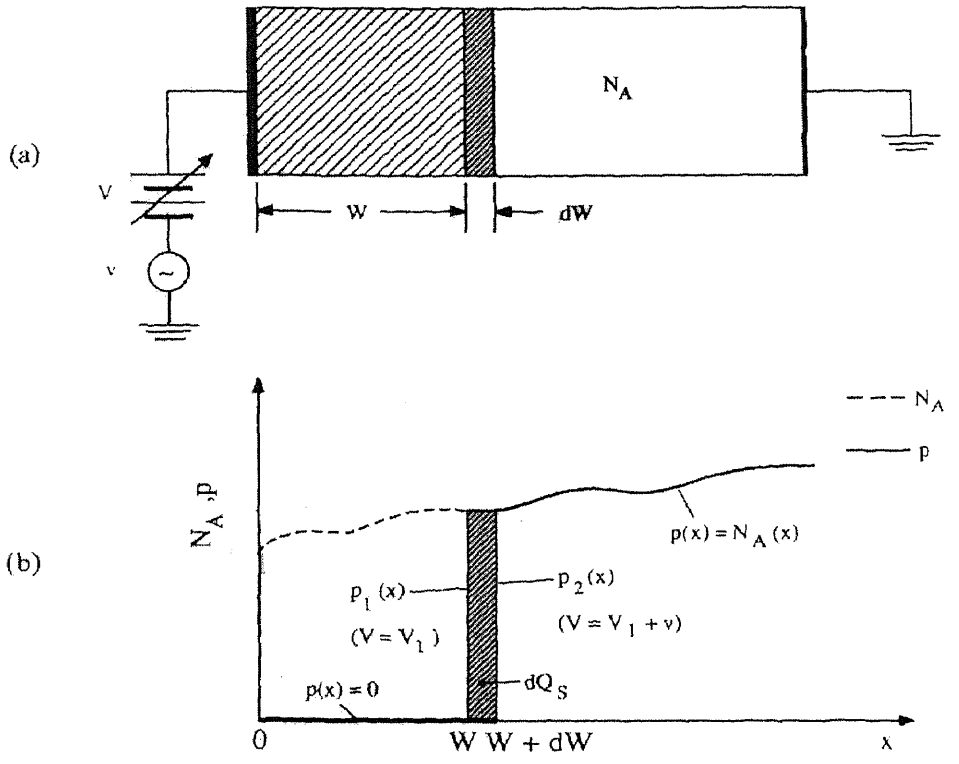


Fig. 2.6 (a) A reverse-biased Schottky diode and (b) the doping concentration and majority carrier profiles in the depletion approximations.

Where Q_S is the semiconductor charge. The negative sign accounts for enhanced negative charge in the semiconductor scr (negatively charged ionized acceptors) for increased positive voltages on the metal. The capacitance is determined by superimposing a small-amplitude ac voltage v on the dc voltage V. The ac voltage typically varies at a frequency of 1 MHz with an amplitude of 10 to 20 mV. The diode is biased to dc voltage V plus a sinusoidal ac voltage. The ac voltage is now increased from zero to a small positive voltage adding a charge increment dQ_m to the metal contact. The charge increment dQ_m must be balanced by an equal semiconductor charge increment dQ_s for overall charge neutrality. dQ_s is given by:

$$dQ_S = -qAN_A(W)dW \tag{2.2}$$

The charge increment, shown in Fig. 2.4 (b), comes about through a slight increase in the scr width. From equations (2.1) and (2.2) the following relation is obtained:

$$C = \frac{-dQ_S}{dV} = qAN_A(W)\frac{dW}{dV} \tag{2.3}$$

The capacitance of a reverse-biased junction, when considered as a parallel plate capacitor, is expressed as:

$$C = \frac{K_S \varepsilon_0 A}{W} \tag{2.4}$$

Differentiating equation (2.4) with respect to voltage and substituting dW/dV into equation (2.3) gives:

$$N_A(W) = \frac{-C^3}{qK_S\varepsilon_0 A^2\left(\frac{dC}{dV}\right)}$$

which can be written as:

$$N_A(W) = \frac{2}{qK_S\varepsilon_0 A^2\left[\frac{d\left(\frac{1}{C^2}\right)}{dV}\right]}$$

Using the identity:

$$\frac{d\left(\frac{1}{C^2}\right)}{dV} = -\left(\frac{2}{C^3}\right)\frac{dC}{dV}.$$

The doping concentration is obtained from the C-V curve by taking the slope dC/dV or by plotting $1/C^2$ versus V and taking the slope $d(1/C^2)/dV$. The depth at which the doping concentration is evaluated is obtained from the following equation[5]:

$$W = \frac{K_S \varepsilon_0 A}{C}$$

2.3.3 Deep-Level Transient Spectroscopy (DLTS)

Conventional DLTS

If the Capacitance-time (C-t) curve from a transient capacitance experiment is processed so that a selected rate produces a maximum output, then a signal whose decay time changes monotonically with time reaches a peak when the rate passes through the rate window of boxcar averager or the frequency of a lock-in amplifier. When observing a repetitive C-t transient through such a rate window while varying the decay time by varying the sample temperature, a peak appears in the temperature versus output plot. Such a plot is known as the DLTS spectrum. The technique, being merely a method to extract a maximum in a decaying waveform, applies to capacitance, current, and charge transients.

2.3.4 Current-Voltage Measurement Techniques

Theory

For moderately doped semiconductors, the I-V characteristics in the forward direction with V>3kT/q is given by the equation[6]:

$$J = A^{**}T^2 \exp\left(\frac{-q\phi_{B0}}{kT}\right)\exp\left[\frac{q(\Delta\phi + V)}{kT}\right] \qquad (2.5)$$

Where ϕ_{BO} is the zero-field asymptotic barrier height, as shown in Fig.2.7. A** is the effective Richardson constant, and $\Delta\phi$ is the Schottky Barrier lowering. Since both A** and $\Delta\phi$ are functions of the applied voltage, the forward J-V characteristics (for V>3kT/q) is represented by:

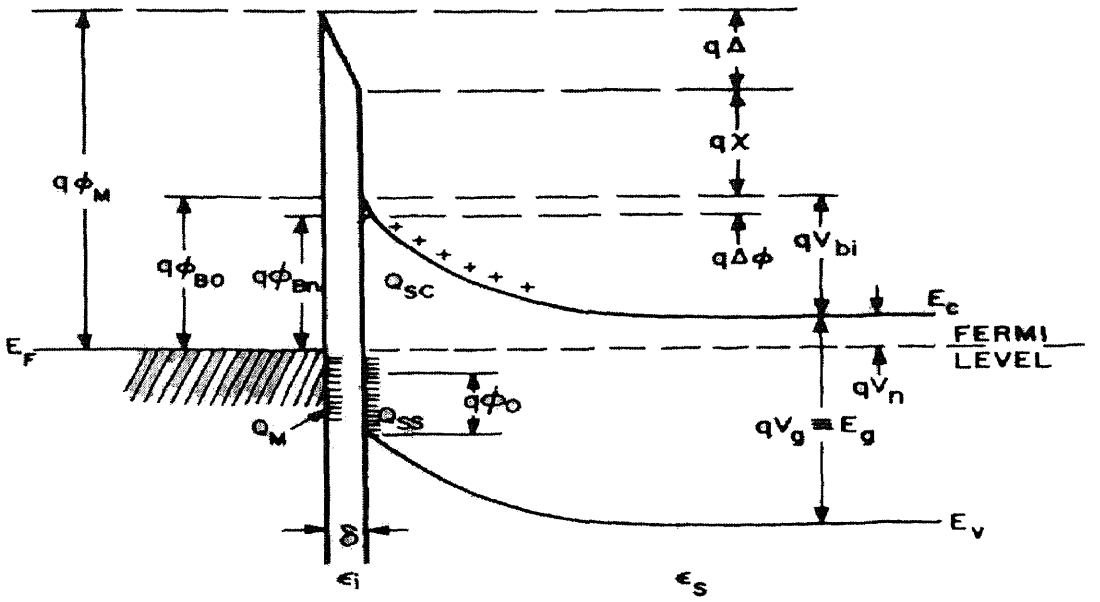
$$J = \exp\left(\frac{qV}{nkT}\right)$$

Where n is the ideality factor, given by:

$$n = \frac{q}{kT}\frac{\partial V}{\partial(\ln J)} = \left[1 + \frac{\partial\Delta\phi}{\partial V} + \frac{kT}{q}\frac{\partial(\ln A^{**})}{\partial V}\right]^{-1}$$

Ideal curves are shown in Fig. 2.8, where n = 1.02 for the W-Si diode and n = 1.04 for the W-GaAs diode[7]. The extrapolated value of current density at zero voltage is the saturation current J_S, and the barrier height can be obtained from the equation:

$$\phi_{Bn} = \frac{kT}{q}\ln\left(\frac{A^{**}T^2}{J_S}\right)$$



ϕ_M = WORK FUNCTION OF METAL
ϕ_{Bn} = BARRIER HEIGHT OF METAL–SEMICONDUCTOR BARRIER
ϕ_{BO} = ASYMPTOTIC VALUE OF ϕ_{Bn} AT ZERO ELECTRIC FIELD
ϕ_o = ENERGY LEVEL AT SURFACE
$\Delta\phi$ = IMAGE FORCE BARRIER LOWERING
Δ = POTENTIAL ACROSS INTERFACIAL LAYER
χ = ELECTRON AFFINITY OF SEMICONDUCTOR
V_{bi} = BUILT-IN POTENTIAL
ϵ_s = PERMITTIVITY OF SEMICONDUCTOR
ϵ_i = PERMITTIVITY OF INTERFACIAL LAYER
δ = THICKNESS OF INTERFACIAL LAYER
Q_{SC} = SPACE-CHARGE DENSITY IN SEMICONDUCTOR
Q_{SS} = SURFACE-STATE DENSITY ON SEMICONDUCTOR
Q_M = SURFACE-CHARGE DENSITY ON METAL

Fig. 2.7 Detailed energy-band diagram of a metal n-type semiconductor contact with an interfacial layer of the order of interatomic distance.[8]

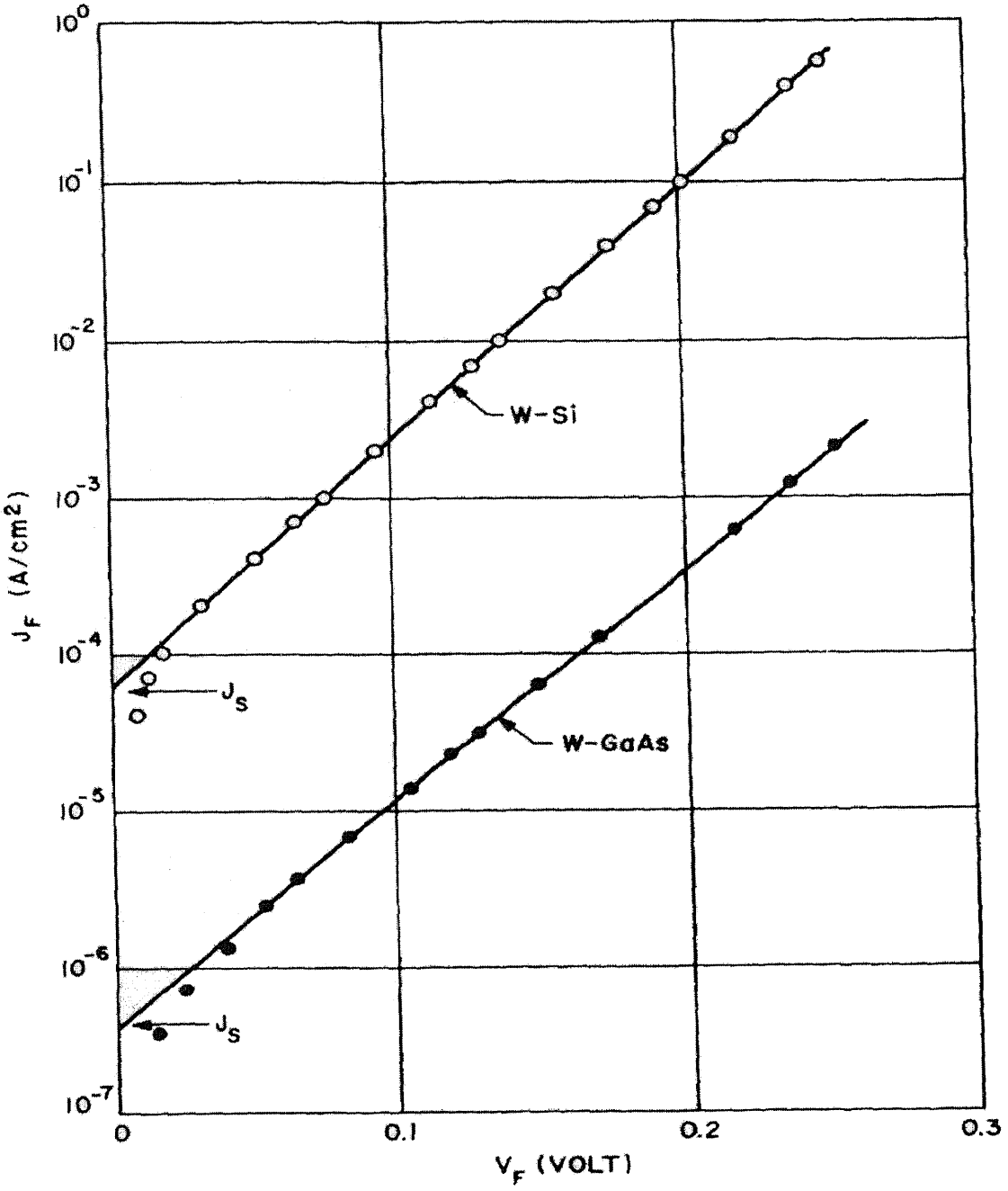


Fig. 2.8 Forward current density versus applied voltage of W/Si and W/GaAs diodes[18].

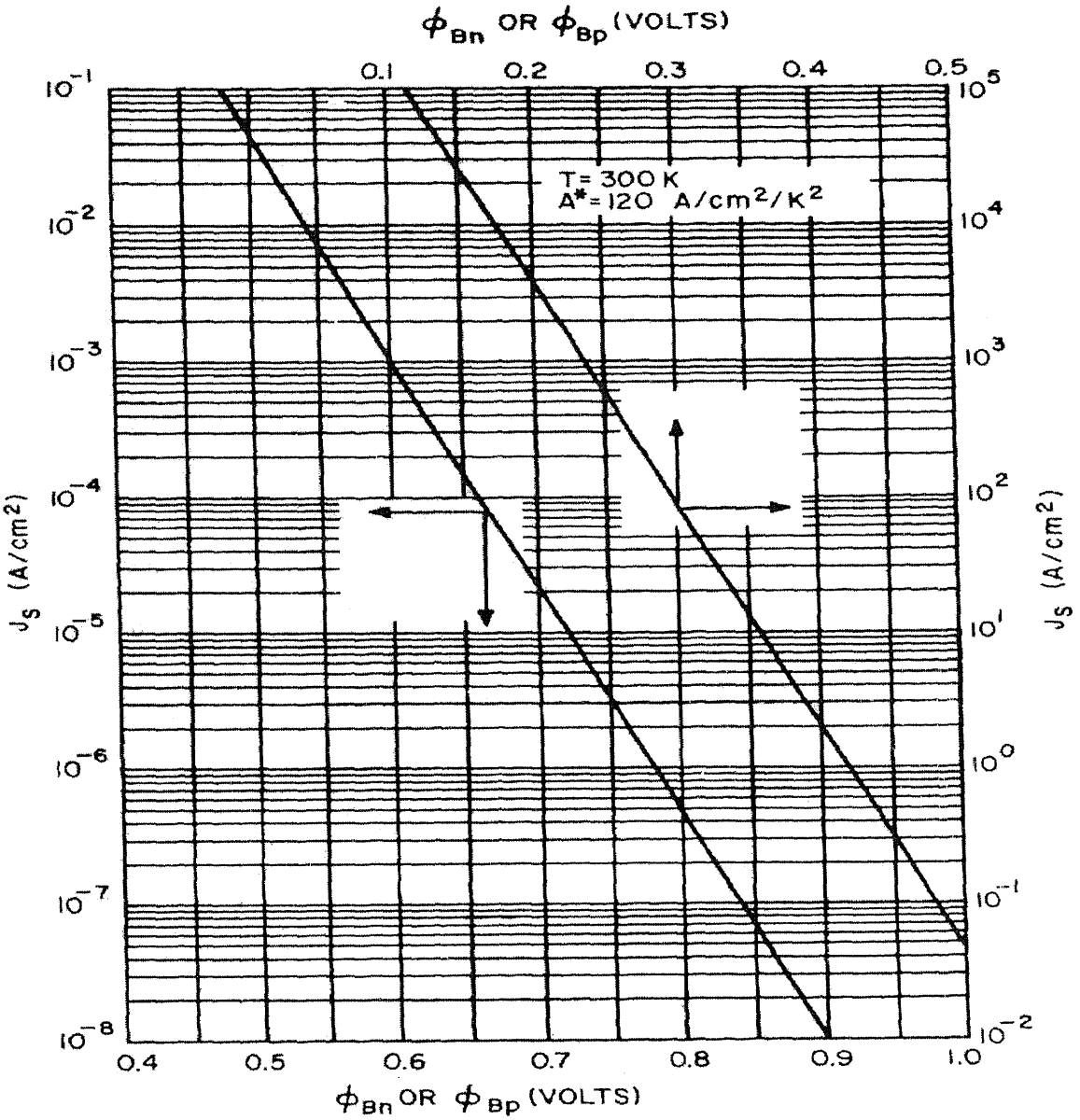


Fig. 2.9 Theoretical saturation current density at 300 K versus barrier height for a Richardson constant of 120 A/cm^2/K^2[2].

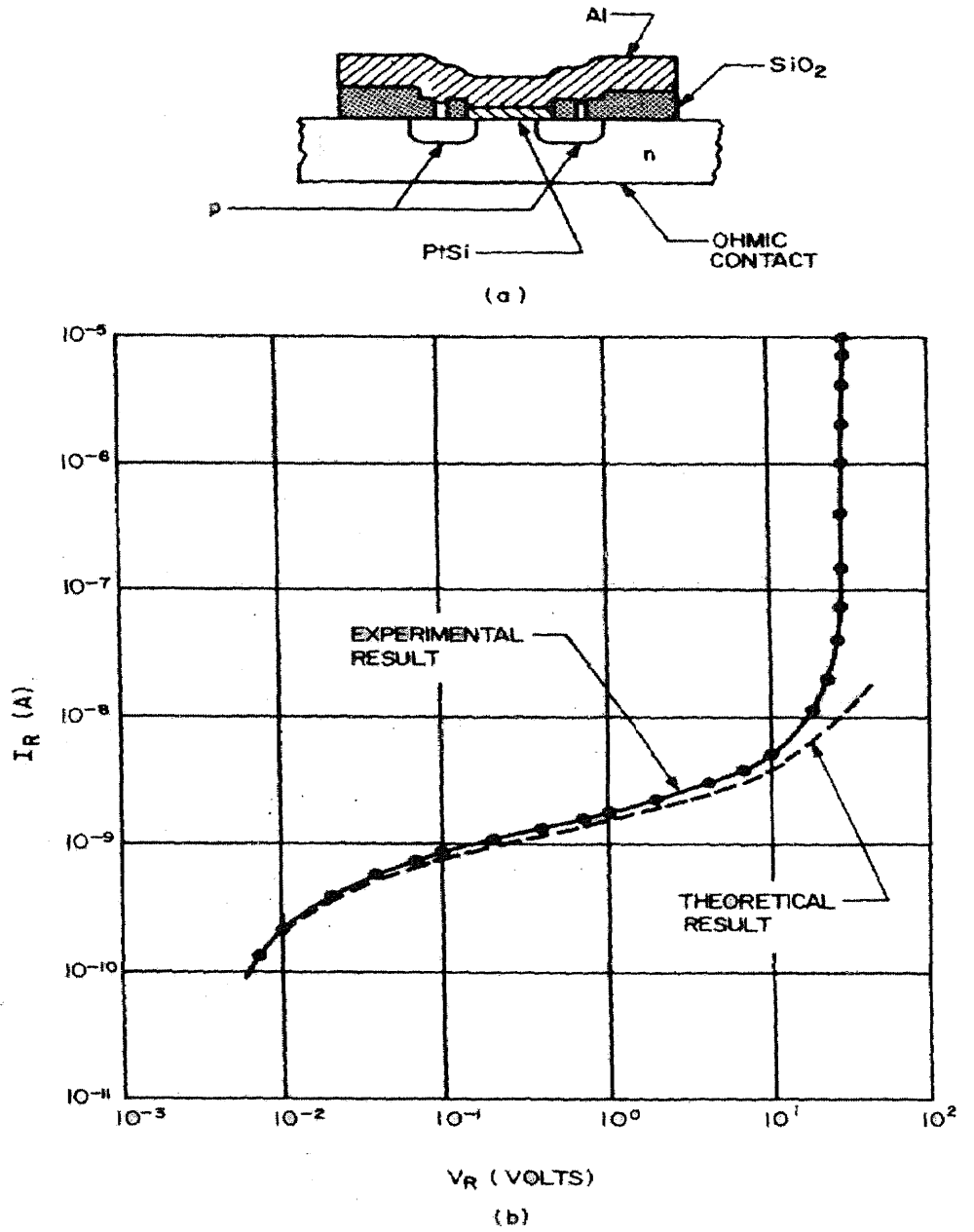


Fig. 2.10 (a) PtSi/Si diode with a diffused guard ring. (b) Comparison of experimental with theoretical prediction of the equation for J_R for a PtSi/Si diode[2].

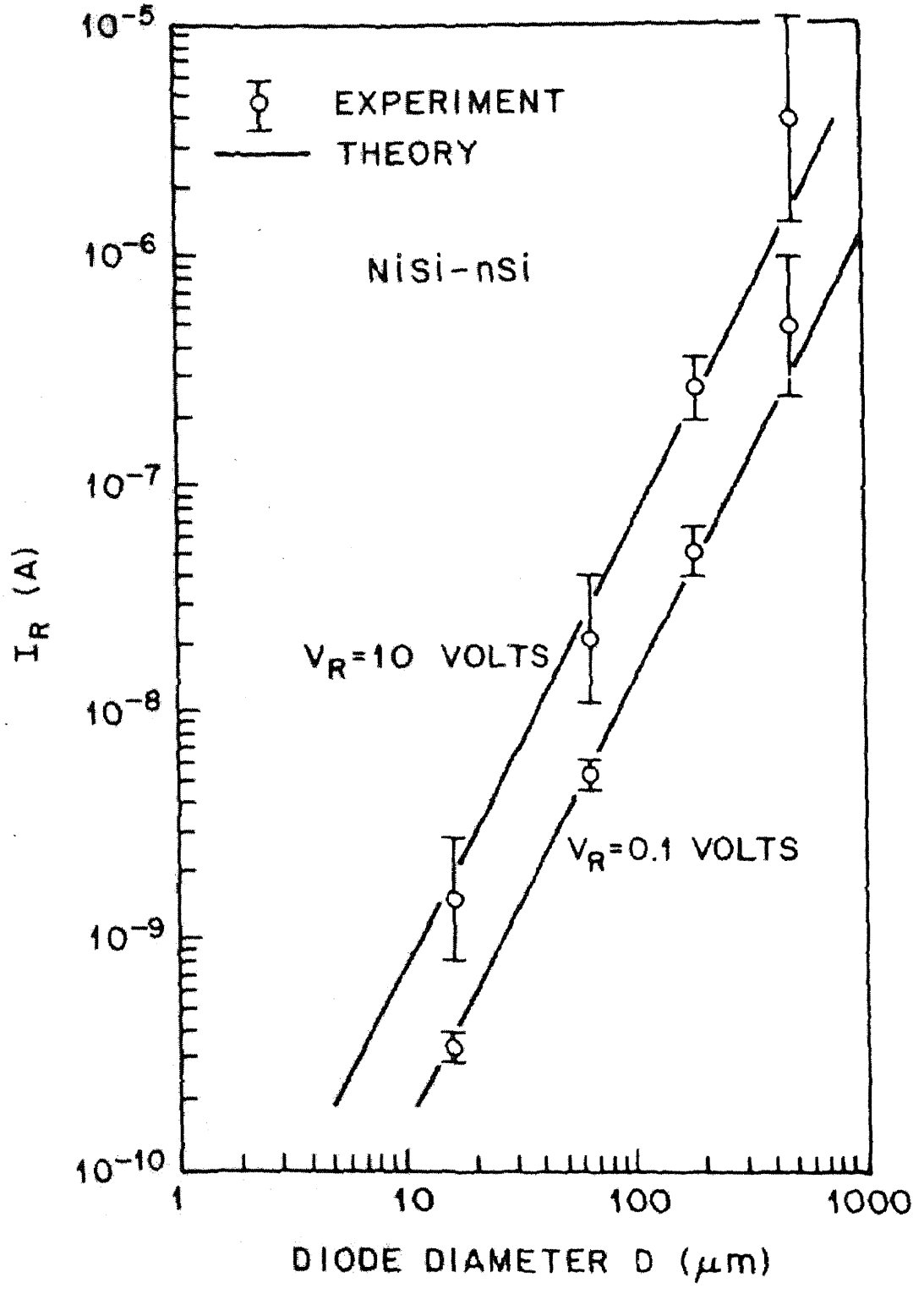


Fig. 2.11 Reverse leakage current as a function of diode diameter formed on n-type silicon with $N_D = 6 \times 10^{15}$ cm^{-3}[2].

The value of ϕ_{Bn} is not very sensitive to the choice of A**, since at room temperature, a 100% increase in A** will cause an increase of only 0.018V in ϕ_{Bn}. The theoretical relationship between J_S and ϕ_{Bn} at room temperature is shown in Fig. 2.9 for A** = 120 $A/cm^2/K^2$. For other values of A**, parallel lines can be drawn on this plot to obtain the proper relationship. In the reverse direction, the dominant effect is due to the Schottky-barrier lowering, or

$$J_R = J_S \qquad \text{(for } V_R > 3kT/q\text{)}$$

$$= A^{**}T^2 \exp\left(\frac{-q\phi_{B0}}{kT}\right)\exp\left(\frac{+q\sqrt{\frac{q\xi}{4\pi\varepsilon_S}}}{kT}\right) \quad [2] \qquad (2.6)$$

Where $$\xi = \sqrt{\frac{2qN_D}{\varepsilon_S}\left(V + V_{bi} - \frac{kT}{q}\right)}$$

If the barrier height $q\phi_{Bn}$ is sufficiently smaller than the bandgap so that the depletion-layer generation-recombination current is small in comparison with Schottky emission current, then the reverse current with the reverse bias is as given in Eqn. (2.6).

However, for most of the practical Schottky diodes, the dominant reverse component is the edge-leakage current, which is caused by the sharp edge around the periphery of the metal plate. To eliminate this effect, metal-semiconductor diodes have been fabricated with a diffused guard ring as shown [9] in Fig. 2.10(a). The guard ring is a deep p-type diffusion, and the doping profile is tailored to give the p-n junction a higher breakdown voltage than that of the metal-semiconductor. Because of the elimination of

the sharp-edge effect, near-ideal reverse and forward I-V characteristics have been obtained. Fig. 2.10 (b) shows a comparison between experimental measurement from a Pt/Si diode with guard ring and theoretical calculation based on the equation for J_R.

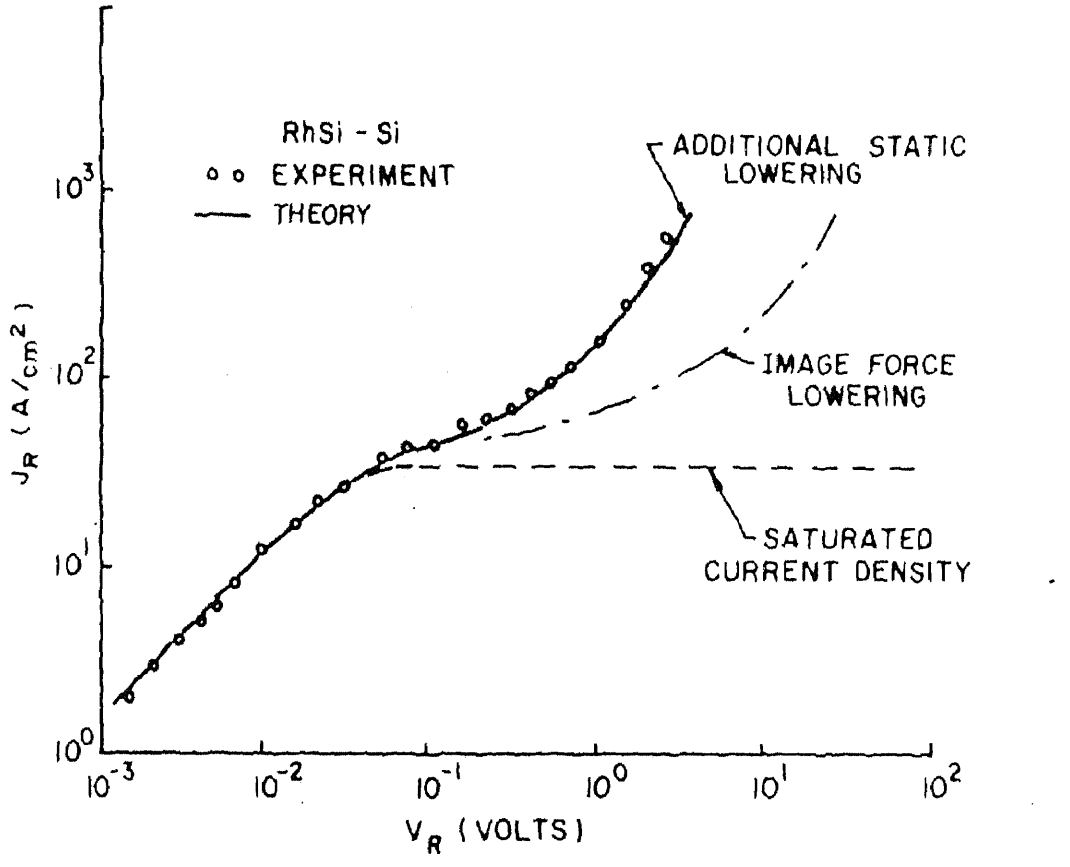


Fig. 2.12 Theory and experiment of reverse characteristics for a RhSi/Si diode[2].

The sharp increase in current near 30 V is due to avalanche breakdown and is expected for the diode with a donor concentration of 2.5 X10^{16}cm^{-3}.

The efficacy of guard ring structures in presenting premature breakdown and surface leakage can be ascertained by studying reverse leakage current as a function of

diode diameter at constant reverse bias. For this purpose, arrays of Schottky diodes with different diameters can be formed on the semiconductor. Fig. 2.11 demonstrates the measured reverse leakage currents as a function of diode diameter[10]. The solid lines drawn through the experimental data have slopes equal to 2, showing that the leakage currents are proportional to the device area. If, on the other hand, the leakage currents are dominated by edge effects, the data would be expected to be along straight lines with slopes equal to unity.

For some Schottky diodes, the reverse current has additional voltage dependence. This dependence arises from the fact that if the metal-semiconductor interface is free from intervening layers of oxide and other contaminants, the electrons in the metal have wave functions that penetrate into the semiconductor energy gap. This is a quantum-mechanical effect that results in a static-dipole layer at the metal-semiconductor interface. The dipole layer causes the intrinsic barrier height to vary slightly with the field, so $\partial\phi_{BO}/\partial\xi_m \neq 0$. To a first approximation the static lowering can be expressed as:

$$(\Delta\phi)_{static} \cong \alpha\xi_m$$

Where $\alpha = \partial\phi_{BO}/\partial\xi_m$. Fig. 2.10 shows good agreement between the theory and measurement of the reverse current in a RhSi-Si diode, based on an empirical value of $\alpha = 17\text{Å}$.

CHAPTER 3

IMPLEMENTATION OF LABVIEW™

3.1 Graphical Programming

Conventional programs for data acquisition are text-based, meaning that the program code is entered as lines of text. In recent years, though, a more powerful approach to programming has emerged with the development of better programming environments – the graphical programming language – 'G'. Programs are written in block-diagram form, rather than in text-based form. One of the most widely used languages in the graphical programming paradigm, LabVIEW™, has been used here for device characterization of Schottky and MOS devices.

3.1.1 Structure of LabVIEW™

LabVIEW™ is a general-purpose programming system, but it also includes libraries of functions and development tools designed specifically for data acquisition and instrument control. LabVIEW™ programs are called virtual instruments (VIs) because their appearance and operation can imitate actual instruments. However, VIs are similar to the functions of conventional language programs.

A VI consists of an interactive user interface, a dataflow diagram that serves as the source code, and icon connections that allow the VI to be called from the higher level VIs. More specifically, VIs are structured as follows:

- The interactive user interface of a VI is called the front panel, because it simulates the front panel of physical instrument. The front panel can contain knobs, push buttons, graphs and other controls and indicators.

- The VI receives instructions from a block diagram, which is written in G. The block diagram is a pictorial solution to the programming problem. The block diagram is also the source code for VI.
- VIs are hierarchical and modular in that they can be used as top-level programs or as subprograms within other programs or subprograms. A VI within another VI is called a subVI. The icon and connector of a VI work like a graphical parameter list so that other VIs can pass data to a subVI.

Thus it is seen that LabVIEW™ is a modular programming language. The application can be divided into a series of tasks, which can be divided again until a complicated program can be divided into a series of simple subtasks. A VI can be built to accomplish each subtask and these VIs can be combined on another block diagram to accomplish a larger task. Finally, the top-level VI contains a collection of subVIs that represent application functions.

Front Panel

The user interface of a VI is like the user interface of a physical instrument – the front panel. The front panel of a VI is primarily a combination of controls and indicators. Controls simulate instrument input devices and supply data to the block diagram of the VI. Indicators simulate instrument output devices that display data acquired or generated by the block diagram of the VI.

Block Diagram

The diagram window holds the block diagram of the VI, which is the graphical source code of a graphical VI. The block diagram is constructed by wiring together objects that send or receive data, perform specific functions, and control the flow of execution. The

principle that governs a LabVIEW™ program execution is called data flow. This means that a node executes only when all data inputs have arrived; the node supplies data to all of its output terminals when it finishes executing; and data passes immediately from source to sink (or destination) terminals.

Data flow contrasts with the control flow method of executing a conventional program, in which instructions are executed in the sequence in which they are written. Data flow execution is data driven or data dependent.

Icon and Connector

When an icon of a VI is placed on the diagram of another VI, it becomes a subVI, the LabVIEW version of subroutine. The controls and indicators of a subVI receive data and return data to the calling VI's diagram. The connector is like the parameter list of function call; the connector terminals act like parameters. Each terminal corresponds to a particular control or indicator on the front panel. A connector receives data at its input terminals and passes the data to the subVI code via the subVI controls, or receives the results at its output terminals from the subVI indicators.

3.1.2 Performance Parameters in LabVIEW™

In traditional LabVIEW™ programming, the programs are designed in a top-down design where a program is composed of hierarchical subVIs. In addition to this, application state information is implemented with global variables, which results in complicated data dependencies and rate conditions. Its ease of maintenance and the ability of the user to add new functionality or fix existing bugs define the efficiency of a program in

LabVIEW™. Thus, certain parameters have been defined by which the efficiency of a LabVIEW™ program is measured[11].

Scalability

A way of increasing the performance of an application is to distribute its work among several machines. An example of this approach is seen in data acquisition applications. Traditionally, all the functional units are implemented as a single entity. The scalability of the system can be improved by distributing the work such as performing the data acquisition on one computer, computationally intense analysis and processing on another, while yet another computer archives results in a database. The key factor for being able to distribute the functionalities of the system is to isolate key parts of the application from one another and to decouple the Graphical User Interface (GUI) handling from the application logic.

Maintainability

A basic LabVIEW™ program consists of an application logic, which runs the program, and the GUI, which acts as an interface between the system and the user. As the application logic or the GUI grows more complicated, the code becomes even harder to understand and modify if both the GUI handling and the application logic are in the same VI or intertwined throughout the VI hierarchy. In cases where the change cycles for the GUI and the application logic are different, multiple GUIs for the same application logic are needed. If the code of both the GUI and the application logic is located in the same VI, they cannot be separately changed according to their own change cycle.

3.2 Applications of LabVIEW™

Data Acquisition and Signal Conditioning

LabVIEW™ is used to acquire data and control devices via IEEE-488 (GPIB), RS-232/422 and modular (VXI or CAMAC) instruments as well as plug-in I/O boards[12]. PC-based data acquisition (DAQ) systems and plug-in boards are used in a very wide range of applications in the laboratory, in the field, and on the manufacturing plant floor. Typically, DAQ plug-in boards are general-purpose data acquisition instruments that are well suited for measuring voltage signals. However, most real-world sensors and transducers generate signals that must be conditioned before a DAQ device can reliably and accurately acquire the signal. This front-end processing, referred to as signal conditioning, includes functions such as signal amplification, filtering, electrical isolation, and multiplexing. Therefore, most PC-based DAQ systems include some form of signal conditioning in addition to the plug-in DAQ board and personal computer.

Industrial Automation

For Industrial Automation, a component of LabVIEW™ called BridgeVIEW™ is utilized. Using OPC (Object Linking and Embedding for Process Control) connectivity, BridgeVIEW™ combines monitoring and control with industrial measurements such as high-speed data acquisition for vibration analysis, image acquisition for machine vision, and motion control.

BridgeVIEW™ provides the flexibility to monitor and control the system while giving access to industrial measurements and analysis. BridgeVIEW™ adds a configurable tag processing engine that performs functions such as alarm and event management, historical data logging, networking, and security. With this functionality, BridgeVIEW™

is the ideal system for monitoring applications and larger channel-count applications for SCXI, FieldPoint, and industrial devices.

Multithreading

Multithreading is the ability of the operating system to subdivide specific operations within a single operation into individual threads, each of which can theoretically be executed in parallel. Thus the operating system divides its time not only between each application, as in multitasking, but also between each thread in an application. A multithreaded LabVIEW™ program is divided into three threads – a user-interface thread, a data acquisition thread, and an instrument control thread, each of which can be assigned a priority and operated independently. Thus, multithreaded applications can have multiple tasks progressing in parallel with other applications.

Data Analysis

The LabVIEW™ analysis VIs process blocks of information represented in digital form. They cover the major processing areas[11]:

- Pattern generation – contains VIs that generate digital patterns and waveforms.
- Digital signal processing – contains VIs that perform frequency domain transformations, frequency domain analysis, time domain analysis, and other transforms, such as the Hartley and Hilbert transforms.
- Measurement-based analysis – contain VIs that perform measurement-oriented functions such as single-sided spectrums, scaled windowing, and peak power and frequency estimation.
- Digital filtering – contain VIs that perform IIR, FIR, and nonlinear, digital filtering functions.

- Smoothing windows – contain VIs that perform data windowing.
- Probability and Statistical analysis – contain VIs that perform descriptive statistic functions, such as identifying the mean or the standard deviation of a set of data, as well as inferential statistics for probability and analysis of variance (ANOVA).
- Curve fitting – contains VIs that perform algebraic functions and interpolations.
- Numerical analysis – contains VIs that use numerical methods to perform root-finding, numerical integration, and peak detection.

The analysis VIs perform numerical operations using the central processing unit (CPU) and a floating-point coprocessor (FPC). Many of the VIs take advantage of the processing capabilities of the CPU and the FPU, thereby minimizing execution time of data analysis tasks.

The data analysis VIs use the in-place data processing algorithms. That is, the algorithms allocate minimal data space and process the data within that space. In-place processing minimizes memory requirements, so that the larger blocks of data can be processed.

Communication Applications

Networking is done in software applications to allow one or more applications (clients) to use the services of another application, such as a data collection application running on a dedicated computer, which acts as the server.

Several networking *protocols* have emerged as accepted standards for communications between the processes, most of which are in-built in LabVIEW™, such as Transmission Control Protocol (TCP), User Datagram Protocol (UDP), Dynamic Data Exchange (DDE) and Object Linking and Embedding (OLE).

Fast Fourier Transforms

The Fast Fourier Transforms is one of the most powerful signal analysis tools applicable to a wide variety of fields such as spectral analysis, digital filtering, acoustics, applied mechanics, medical imaging, model analysis, numerical analysis, seismography, instrumentation and communications.

3.3 LabVIEW™ in Device Characterization

3.3.1 Introduction

One of the primary applications of LabVIEW™ in the field of device characterization is in determining the current-voltage characteristics of semiconductor devices. In this particular application, it has been used as the driver for the Source-Measure Unit (SMU), which is interfaced with the Device Under Test (DUT) using the GPIB IEEE 488.2 interface.

3.3.2 Program Description

The program can be basically divided into parts. The front panel of the program simulates the front panel of the Source Measure Unit (SMU) and allows the user to input parameters such as the start and stop voltages, integration time, delay time, step voltage, current compliance value, etc. Device-dependent parameters, such as the oxide thickness in MOS Capacitors can also be entered on the front panel. LabVIEW™ uses the concept of Graphical Object-oriented programming which implies that each module of the program is independent of the others, among other aspects.

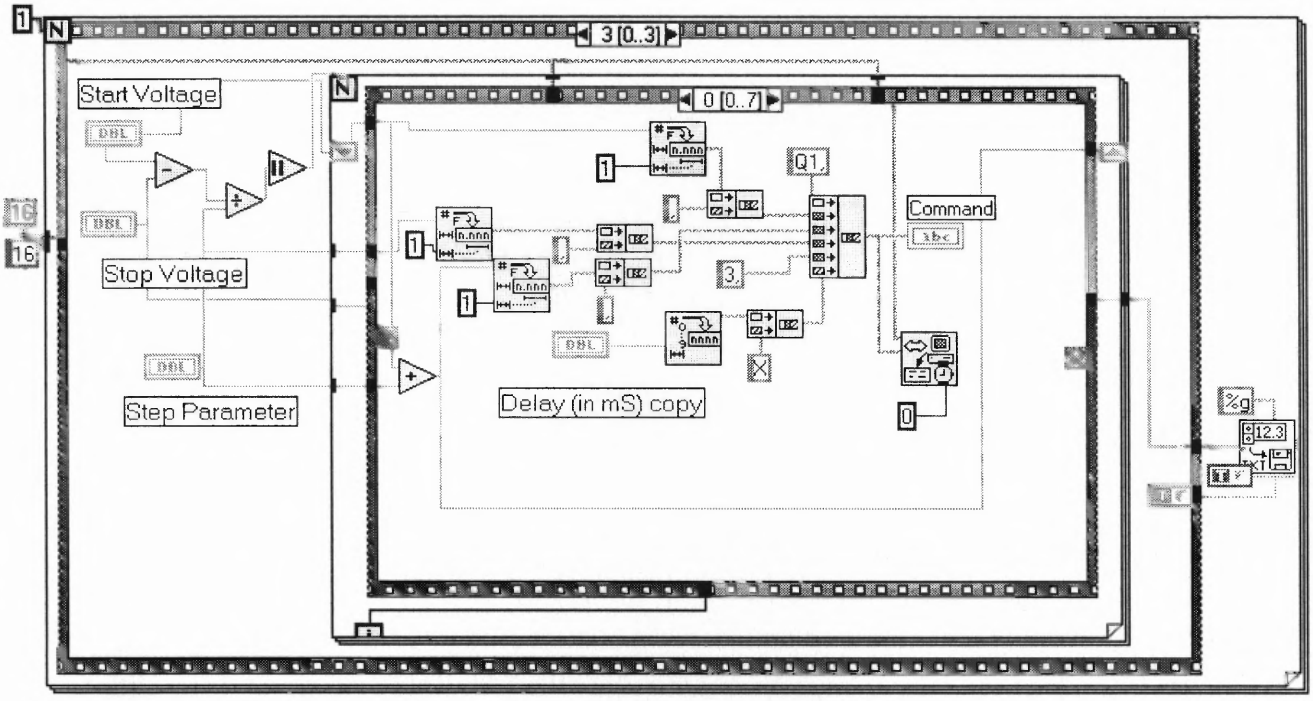


Fig.3.1. A sequence of the block-diagram of LabVIEW™ program used for device characterization

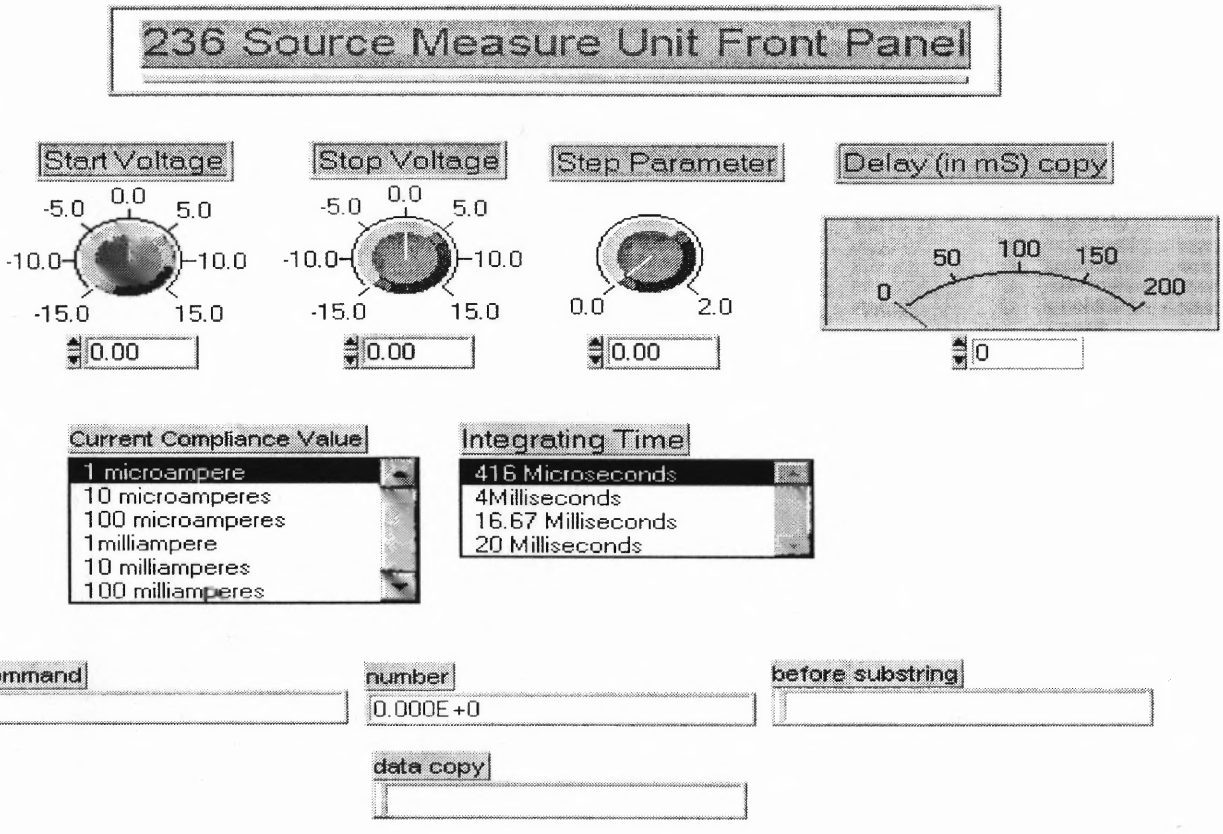


Fig.3.2. Front-panel simulation of the SMU in LabVIEW™

As shown in Figs.3.1 and 3.2, while the front panel is only the simulation of the instrument, the diagram contains the actual program (given in Appendix A). Various GPIB interface commands are available in LabVIEW^{TM} to drive any instrument with the software. Communication between the instrument and the DUT takes place with the help of these interface commands. Two of them are listed here, along with their functionality.

GPIB Write: With the proper address provided, this module writes data to the instrument (Source Measure Unit) after each increase in the supply voltage with the step provided. Written data comprises of the above-mentioned parameters.

GPIB Read: This command is used to read data from the Source Measure Unit. This data comprises of measured current values read after each iteration.

CHAPTER 4

THE SOURCE MEASURE UNIT

4.1 Introduction

The Keithley 236 Source Measure Unit (SMU) is a programmable instrument capable of sourcing and measuring current or voltage simultaneously. This instrument has been the principal tool of measurement of the electrical characteristics of the various samples considered in this study. The fundamental models of the Source Measure Units are shown in Fig. 4.1. When programmed to source voltage, the I_{METER} is connected in series with the V_{SOURCE} and output. When programmed to source current, the V_{METER} is connected across (in parallel to) the I_{SOURCE} and output[13].

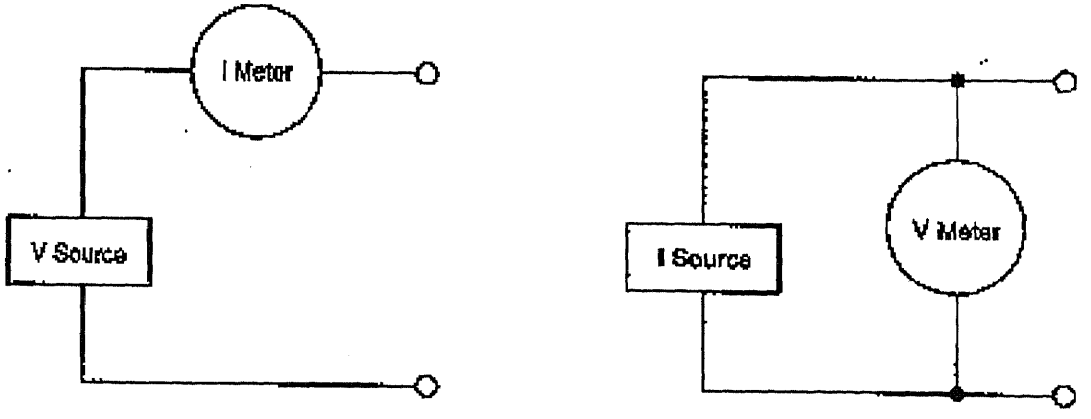


Fig. 4.1: Fundamental Methods (a) Source V Measure I, (b) Source I Measure V[13]

4.1.1 Source Capabilities

V_{SOURCE} – As a voltage source, the Model 236 can source from ±100μV to ±110V with a programmable current compliance limit of up to 100 mA.

I_{SOURCE} – As a current source, the Model 236 can source from ±100fA to ±100mA with a programmable voltage compliance of up to 110V.

Compliance limits are used to protect external circuitry or DUT (Devices Under Test). Setting an appropriate current compliance (I-limit) can prevent excessive power dissipation in a device. Setting an appropriate voltage can protect a device susceptible to damage by overvoltage.

4.1.2 Measure Capabilities

I_{METER} – When configured to measure current, the Model 236 can measure from ±10fA to ±100mA.

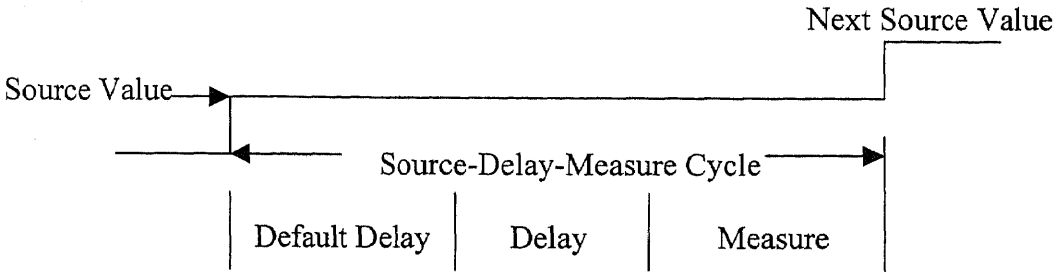
V_{METER} – When configured to measure voltage, the Model 236 can measure from ±10μV to ±110V.

In addition to these modes of operations, the Source Measure Unit can also be used in Source only and Measure only modes.

4.1.3 Source-Delay-Measure

Source Measure Unit operation (dc and sweep) consists of a series of source-delay-measure (SDM) cycles, in which a delay is introduced to allow for the source to settle before the measurement is made. The total time period of the delay includes an internal (default) delay and the user programmed delay, as shown in Fig. 4.2. With the default

delay enabled, a short delay is used to allow for internal settling on the low current ranges. The default delay is approximately equivalent to five RC time constants of the selected current range for either Source I or Source V.



Default Delay: Fixed delay for instrument settling

Delay: Additional delay for device under test or system capacitance

Fig. 4.2 Source-Delay-Measure (SDM) Cycle[13]

A programmable delay (from 0 msec to 65 sec) can also be used to compensate for the longer settling caused by external circuitry. The more the capacitance seen at the output, the more settling time that is required for the source. The actual delay period needed can be calculated or determined by trial and error. For resistive loads and higher currents, the programmable delay is set to 0 msec.

4.1.4 Operating Functions (dc and sweep)

In dc operation (dc function selected), a constant dc voltage or current is applied to the output. This operation consists of a continuous series of SDM cycles. During each SDM cycle, the measured reading is internally updated, making them available for display. The programmed source value is displayed on the left side of the display and the subsequent measurement is shown on the right side. All readings are not displayed. The display is

slower than the internal measure update rate. However it is possible to get all the readings over the bus and read out on the PC.

In sweep operation (sweep function selected), the Source Measure Unit sweeps through a user-defined list of points specifying source values and delay times for a waveform (fixed-level, staircase or pulse). An SDM cycle occurs during each programmed step or point of the sweep. Each measurement in the sweep is stored in the sweep buffer.

4.2 Operating Boundaries

Depending on the approach to the program and the nature of the output (passive or active load), the 236 Source Measure Unit can operate in any of the four quadrants. The source-measure capabilities of the SMU are shown in Fig.4.3. When operating in the first or third quadrant, Source Measure Unit is operating as a source. That is, the Source Measure Unit is delivering power to a load. When operating in the second or fourth quadrant, Source Measure Unit is operating as a sink. As a sink, it is dissipating power rather than sourcing it. An external source or an energy storage device, such as a capacitor or a battery, can force operation in the sink region. For example, if a 12 V battery is connected to a Source Measure Unit that is programmed for +10V, sink operation will occur in the second quadrant (source +V and measure –I).

4.2.1 Source I Measure V

The operating boundaries in a single quadrant for Source I and Measure V is shown in Fig. 4.4. The voltage limit load line represents the programmed compliance limit set by the user. The current source load line represents the source current programmed by the

user. These load lines are boundary lines that represent the operating limits of the Source Measure Unit for this quadrant of operation. The operating boundaries for the other three quadrants are similar.

The load (DUT) that is connected to the output determines the location on the boundary line that the Source Measure Unit operates. Fig. 4.5 shows operation examples for resistive loads that are 500Ω and 1KΩ respectively. In these examples, the Source Measure Unit is programmed to source 16mA and limit (measure) 12V.

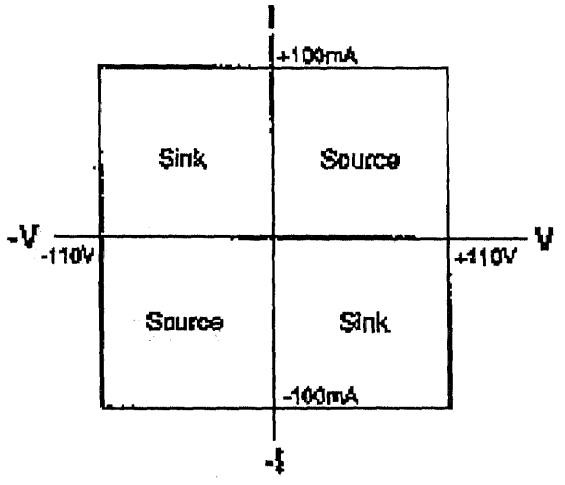


Fig. 4.3: Source-Measure Capabilities[13]

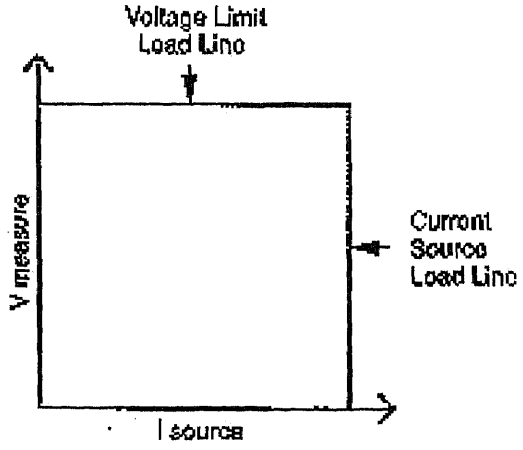


Fig. 4.4: I-Source Operating Boundaries

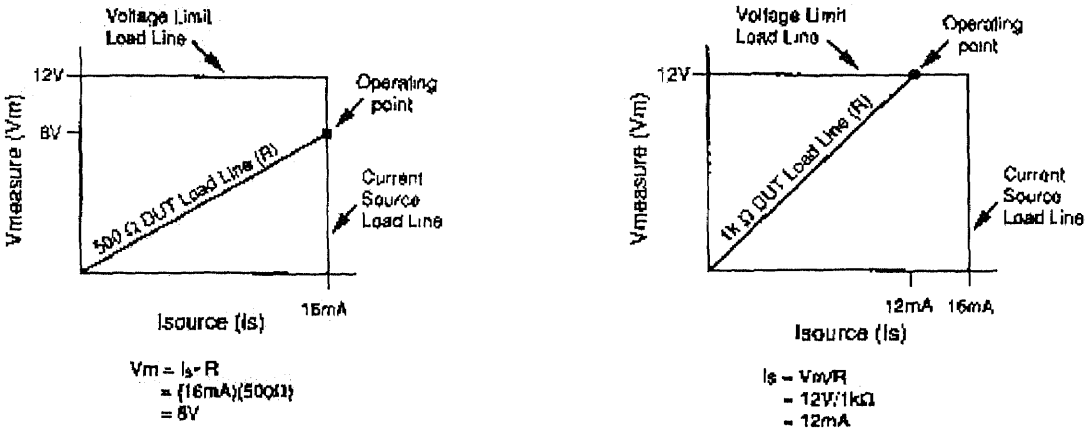


Fig. 4.5 I-Source Operations (a) Normal I-Source Operation (b) I-Source in Compliance[13]

In Fig.4.5 (a), the Source Measure Unit is sourcing 16mA to the 500Ω load and subsequently measures 8V. As long as the DUT load line intersects the current source load line, the Source Measure Unit will be able to source its programmed current (16mA). Fig.4.5 (b) demonstrates the effect of increase in the resistance of the load to a value of 1kΩ. The DUT load line intersects the voltage limit load line placing the Source Measure Unit in compliance. In compliance, the Source Measure Unit will not be able to source its programmed current (16 mA). Instead, it will source only 12mA.

As the resistance increases, the slope of the DUT load line increases. As resistance approaches infinity (open output), the Source Measure Unit will source virtually 0 mA at 12V. Conversely, as resistance decreases, the slope of the DUT load line decreases. At zero resistance (shorted output), the Source Measure Unit will source 16mA at virtually 0 V. Regardless of the load, voltage will never exceed the programmed compliance of 12V. Also, the maximum power to a DUT in this case will never exceed 192 mW (12 V X 16 mA).

4.2.2 Source V Measure I

The operating boundaries in a single quadrant for Source V Measure I are shown in Fig.4.6. The current limit load line represents the programmed compliance limit programmed by the user. The voltage source load line represents the source voltage programmed by the user. These load lines are boundary lines that represent the operating limits of the Source Measure Unit for this quadrant of operation. The operating boundaries for the other three quadrants are similar.

The location of operation of the SMU in the boundary depends on the load (DUT) that is connected to its output. Fig.4.7 shows operation examples for resistive loads that are 500 Ω and 200 Ω respectively. In these examples, the Source Measure Unit is programmed to source 10 V and limit (measure) 25 mA. In Fig.4.7 (a), the Source Measure Unit is sourcing 10 V to the 500 Ω load and subsequently measuring 20 mA.

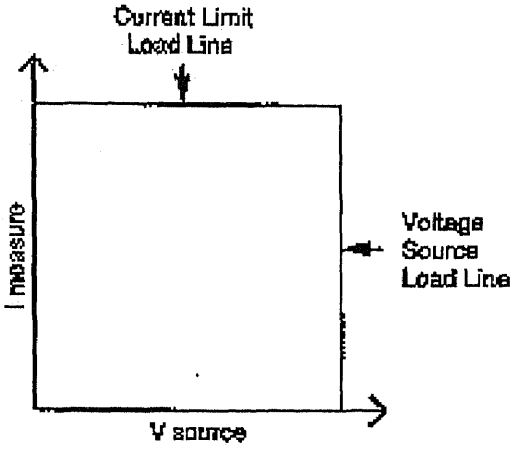


Fig. 4.7 V-Source Operating Boundaries

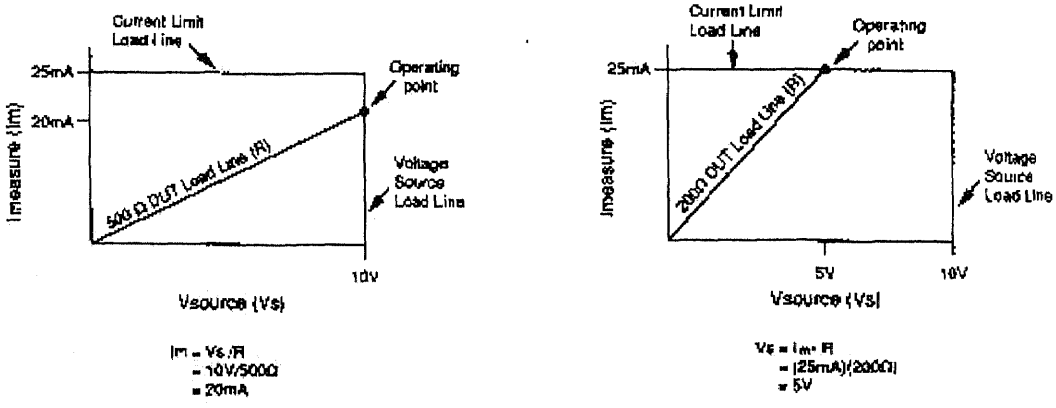


Fig. 4.8 V-Source Operations(a) Normal V-Source Operation(b) V-Source in Compliance

As long as the DUT load line intersects the voltage source load line, the Source Measure Unit will be able to source its programmed voltage (10V). Fig. 4.7 (b) shows the effect of the resistance of the load as it is decreased to 200 Ω. The DUT load line intersects the current limit load line, placing the Source Measure Unit in compliance. In compliance, the Source Measure Unit will not be able to source its programmed voltage (10V). Instead, it will source only 5V.

As the resistance decreases, the slope of the DUT load line increases. At zero resistance (shorted output), the Source Measure Unit will source virtually 0 V at 25 mA. Conversely, as resistance increases, the slope of the DUT load line decreases. At infinite resistance (open output), the Source Measure Unit will source 10 V at virtually 0 mA. Regardless of the load, the current will never exceed the programmed compliance of 25 mA. Also, maximum power to a DUT in this case will never exceed 250 mW (10V X 25 mA).

4.2.3 Mode of Operation Used

The Source Measure Unit has been used in the Source V Measure I mode for obtaining the Current-Voltage characteristics of the DUTs considered. The device-dependent commands for the 236 Source Measure Unit are given in Appendix B.

4.3 The 236 Source Measure Unit Features

4.3.1 Dc Operation

The 236 SMU can operate in the sweep and the dc modes. In the experiments performed, the dc mode has been used. Some of the features of this mode are as given below.

SELECT SOURCE AND FUNCTION – The SOURCE MEASURE button toggles the Source Measure Unit between Source V, Measure I and Source I, Measure V. The FUNCTION button toggles the Source Measure Unit between dc operation and sweep operation.

SET COMPLIANCE AND MEASURE RANGE – Compliance limits are set in order to protect the external circuitry (i.e., DUT) from damage. When sourcing voltage, a current compliance value is set. The Source Measure Unit will never source a current that will exceed the programmed current compliance limit. Conversely, when sourcing current, a voltage compliance limit is set.

AUTORANGE – With AUTORANGE enabled, the Source Measure Unit will go to the lowest possible (most sensitive) range to make the measurement. The AUTORANGE button toggles between autorange and the fixed range selected when compliance was set.

INTEGRATION TIME – The integration time is used to check and /or change the integration period of the Source Measure Unit. The selectable integration times offer a trade-off between speed, resolution and noise rejection. The fast integration period provides the fastest measurements and should be used when speed is the most important consideration. At the other extreme, the line-cycle integration period provides the slowest but most stable (quieter) measurements.

FILTER – Filtering is used to stabilize noisy measurements. The unit does this by averaging a number of reading conversions and then displaying (or storing) the result. The number of readings that can be averaged (filtered) is 2, 4, 8, 16 or 32. FILTER disabled is synonymous to averaging one reading.

SUPPRESS – Suppression allows a stored offset value to be subtracted from subsequent measured readings. When SUPPRESS is enabled, the next conversion will be internally stored as a baseline. All subsequent readings will be the difference between the suppressed value and the actual signal level. A suppressed value can be stored for both the voltage source and the current source. Suppressing a value while in dc operation will process readings already stored in the sweep buffer. The suppressed value will be algebraically subtracted from every measurement point in the sweep.

4.4 The GPIB (General Purpose Interface Bus)

The GPIB is an interface for connecting controllers to test instruments. It uses high transfer rates to exchange data between the controller and the test instrument either in the Talk, Listen or Control modes. A Talker sends data messages to one or more listeners, which receive the data. The Controller manages the flow of information on the GPIB by sending commands to all devices. The GPIB is similar to an ordinary computer bus, except that a computer has its circuit cards interconnected via a backplane – the GPIB has stand-alone devices interconnected to standard cables. Thus, a computer equipped with GPIB hardware performs the roles of Talker/Listener and Controller.

4.4.1 Interfacing the SMU with GPIB IEEE 488.2

The IEEE 488.2 standard defines the way in which the GPIB controller sends commands and data to the test instrument, which contains the DUT, and this is interfaced with the controller. As described in section 3.2, LabVIEW^{TM} can be used to acquire data and

simulate test instruments. The 236 Source Measure Unit has been interfaced with the computer using the National Instruments GPIB IEEE 488.2.

4.4.2 IEEE 488.2 Controller Requirements

The IEEE 488.2 defines a number of controller-specific protocols that include interface capabilities, bus control sequences and bus protocols. An IEEE 488.2 controller must be able to[14]:

- Set the Remote Enable (REN) signal line either TRUE or FALSE
- Pulse the Interface Signal (IFC) line TRUE for greater than 100μsec
- Send or receive the IEEE 488.2 codes, data formats, protocols and common commands
- Sense the state of the Service Request (SRQ) signal line
- Investigate each bit of an instrument status line
- Timeout an I/O transaction

IEEE 488.2 has the capability to interface with a number of instruments, but has been used to control only instrument here – the Keithley 236 SMU, which in turn controls the set-up in which the DUT is housed. The DUT set-up is explained in detail in section 4.4.

4.4.3 IEEE 488.2 Data Coding and Formats

The IEEE 488.2 defines the coding and formats for all numerical data and character strings – for example 7-bit ASCII code for alphanumerics, 8 - bit binary code for integers, and IEEE standard 754 codes for binary floating-point numbers[15]. IEEE 488.2

also defines the formats for decimal, hexadecimal and octal numbers, as well as formats to send blocks of 8-bit bytes and ASCII character strings.

4.4.4 IEEE 488.2 Common Commands and Queries

IEEE 488.2 defines programming commands for executing operations to command and report status of the instrument and queries used to receive common status information. The functions of these commands and queries fall into the following categories[16]:

- Automatic address configuration (Auto Configure)
- Instrument-specific information and parameters (System data)
- Internal Instrument Operations (Internal Operations)
- Operation synchronization (Synchronization)
- Macro definitions (Macro)
- Parallel poll responses (Parallel Poll)
- Device trigger and responses (Trigger)
- Passing control (Controller)
- Setting the state of the instrument (stored settings)

A table containing a complete list of the common commands and queries along with a brief functional description, the designated query and the compliance requirements for the GPIB IEEE 488.2 is shown in Appendix C.

4.5 The AT-GPIB/TNT Board

The AT-GPIB/TNT is an IEEE 488 interface for the IBM PC AT and compatible computers equipped with 16-bit ISA slots. The AT-GPIB/TNT sustains data transfer rates of up to 1.5 Mbytes/s using the IEEE 488.1 3-wire handshake.

4.5.1 The Plug and Play Concept

A plug and play version of the AT-GPIB/TNT has been used in the experiment. In the plug and play version, the hardware resources of the interface (I/O address, DMA channel, and interrupt level) is allocated by the operating system through the NI 488.2 driver. This eases the system configuration of PCI ISA systems by automatically configuring each board address, interrupt and DMA channel, without user intervention at system startup.

4.5.2 Features of the AT-GPIB/TNT (Plug and Play)

ISA Bus Interface Logic – The ISA Bus Interface Logic decodes the control signals of the ISA bus to provide access to the internal registers of the AT-GPIB/TNT. The AT-GPIB/TNT can be used with DMA disabled in an 8-bit PC/XT slot as well.

FIFO – A 16-bit by 16-deep FIFO buffer on the AT-GPIB/TNT buffers data sent to or received from the GPIB. By buffering the data, the ISA bus and the GPIB overlap their respective accesses to the FIFO, rather than one bus waiting for the other to complete the cycle.

I/O Address Decode - AT-GPIB/TNT (Plug and Play) occupies 32 bytes in the ISA I/O space. The Plug and Play software configures the AT-GPIB/TNT automatically.

DMA Channel and Interrupt Level Selection – The AT-GPIB/TNT (Plug and Play) uses one out of at least 7 interrupt levels and one out of at least 3 DMA channels. In the AT-GPIB/TNT (Plug and Play), the DMA channel and interrupt level are automatically configured by the Plug and Play software.

CHAPTER 5

RESULTS AND DISCUSSION

This chapter focuses on the current-voltage (I-V) characteristics and theoretical analyses of the experimental data. Two sets of devices were considered in the analysis – Metal Semiconductor Contacts and Metal Oxide Semiconductor (MOS) structures. The measurements were performed using a Keithley 236 Source Measure Unit (SMU), driven by LabVIEW^{TM} software, described in Appendix A. As discussed in a previous section, the interface between the SMU and the software was provided by the GPIB IEEE 488.2. The I-V measurement technique consists of applying a desired voltage across the device and measuring the corresponding current. The technique can be non-destructive by placing a compliance limit on the current, which prevents it from crossing a certain limit that might damage the DUT.

5.1 Tantalum Silicide/Silicon

In recent years, device performance has been limited by the high sheet resistance of polycrystalilline silicon. Thus, refractory metal silicides, such as Titanium Silicide ($TiSi_2$) and Tantalum Silicide ($TaSi_2$) have been investigated because of their low contact resistance at the source, drain and gate regions of MOS transistors and their high thermal stability. There is a layer of native oxide present at the metal-silicon interface, which is dissoluted and the reaction between Tantalum and Silicon takes place[11].

Process Description

The process flow for the fabrication of the $TaSi_2$/Si is shown schematically in Fig. 5.1. The wafers are initially rinsed in cold de-ionized water and then spin-dried. This is followed by rinsing them in hot de-ionized water and spin-drying again. The wafers are then pre-cleaned in a furnace and metal deposition takes place. The photoresist is first applied on the frontside and then hard baked at a temperature of 115°C. The photolithography process is then completed by aligning the mask and exposing the wafers to form the pattern. This process is followed by $TaSi_2$ dry etch and annealing in forming gas at a temperature of 400°C for 30 minutes.

The Tantalum Silicide films are in the thickness range of 100-900 Å. The patterned $TaSi_2$/Si devices are circular in geometry with diameters in the range of 100 - 500μm. The $TaSi_2$ films are deposited on n-silicon and p-silicon of orientation <100> and resistivity in the range of 2-20 Ωcm. The backside metal comprises of 3000 Å of sputter-deposited Al films.

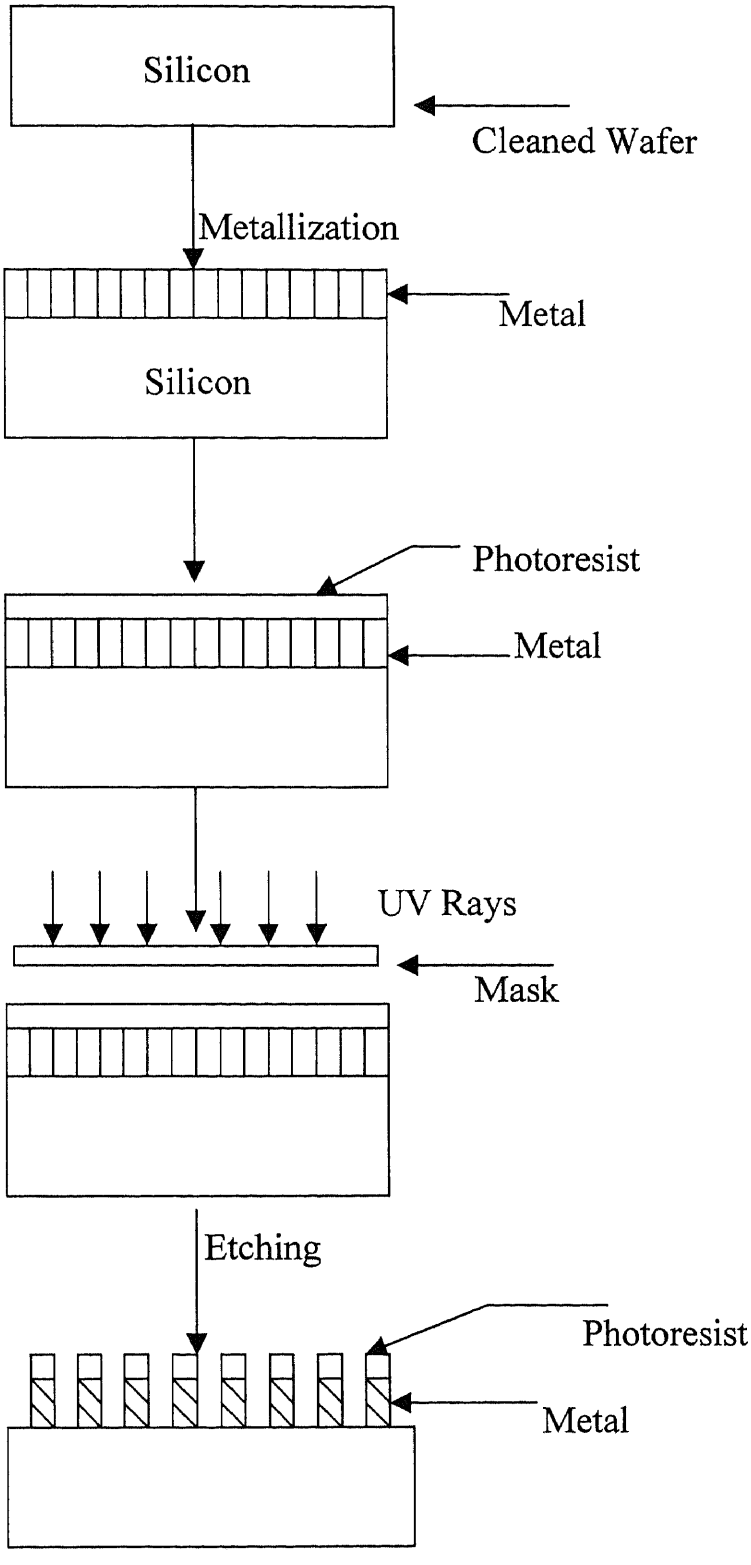


Fig. 5.1 Process Flow for the fabrication of $TaSi_2$/Si diode (continued)

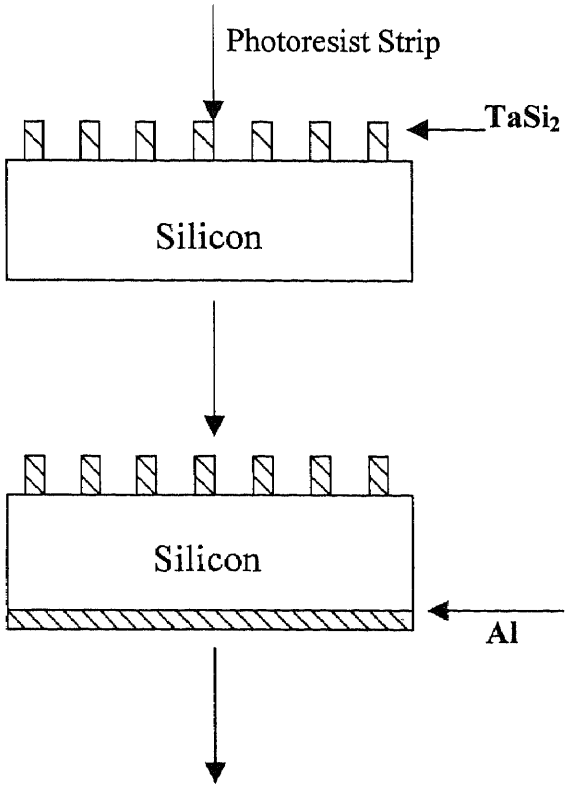


Fig. 5.1 Process Flow for the fabrication of $TaSi_2$/Si (continued)

5.1.2 Results

Sheet resistances of $TaSi_2$/Si were carefully measured using the standard four-probe technique. The values of sheet resistance obtained were in the range of 34.5Ω/□ to 421Ω/□ depending on the substrate and the film thickness. These values lead to resistivities in the range of 34.5μ Ωcm to 421μ Ωcm for a tantalum silicide film thickness of 100 Å. These values are in accord with those reported in the literature[18], as can be seen in Table 5.1.

Table 5.1 Published values of Tantalum Silicide Resistivities[18]

Researcher	Robins	Padnos	Keifer and Benesovsky	Wehrmann
Resistivity ($\mu\ \Omega$-cm)	38.0	8.5 – 38.0	46	38.0

It is to be noted here that the resistivity is simply the product of sheet resistance and thickness. In Table 5.1, the published values of the $TaSi_2$ resistivities are summarized.

The experimental I-V plots obtained for $TaSi_2$/Si devices are presented in Figs.5.2, 5.3, and 5.4. The actual I-V plots are shown in Figs. 5.2 (a), 5.3 (a) and 5.4 (a). The ln I v/s V plots are shown in Figs. 5.2 (b), Fig. 5.3 (b) and 5.4(b). The value of the barrier height ϕ_b is obtained by extrapolating the curves to zero voltage, as demonstrated in the ln I v/s V plots. The extrapolated value of the current density at zero voltage is the saturation current density J_S, and the barrier height can be obtained from the equation:

$$\phi_{Bn} = \frac{kT}{q} \ln\left(\frac{A^{**}T^2}{J_S}\right)$$

It is to be noted here that the evaluation of the barrier height, in this study, has been made for the most simplistic situation. It is assumed here that the device has zero series resistance. The A** values are assumed from the literature. The dependency of A** on the doping concentration in the semiconductor, temperature, voltage, etc., has been neglected. In addition, the value of the diode quality factor, n, has been taken to be unity. This is true only for moderately doped silicon and under specific voltage conditions. The

experimental plots of I v/s V have been compared to the plots generated by the simulation program (written in Visual Basic 6.0[19]) assuming the established values for barrier height from literature[18] and using it in the equation given below:

$$J = J_S \exp\left(\frac{V - IR_S}{nkT}\right)$$

Where $J_S = A^{**}T^2 \exp\left(\frac{-\phi_B}{kT}\right)$.

For n = 1 and $R_S = 0$, the above equation reduces to:

$$J = J_S \exp\left(\frac{V}{kT}\right)$$

The simulated ln I v/s V plots are shown in Figs. 5.5 and 5.6. The experimental results are tabulated in Table 5.2 below. The simple user interface designed to enter the device parameters into the simulation program in Visual Basic 6.0 is shown in Fig. 5.2. The detailed results of the simulation are presented in Appendix D.

Table 5.2 Experimental Values for Barrier Height (I_S in Amps)

Ln I_S	-13.5	-12.0	-9.0	-5
ϕ (eV)	0.6	0.564	0.49	0.38

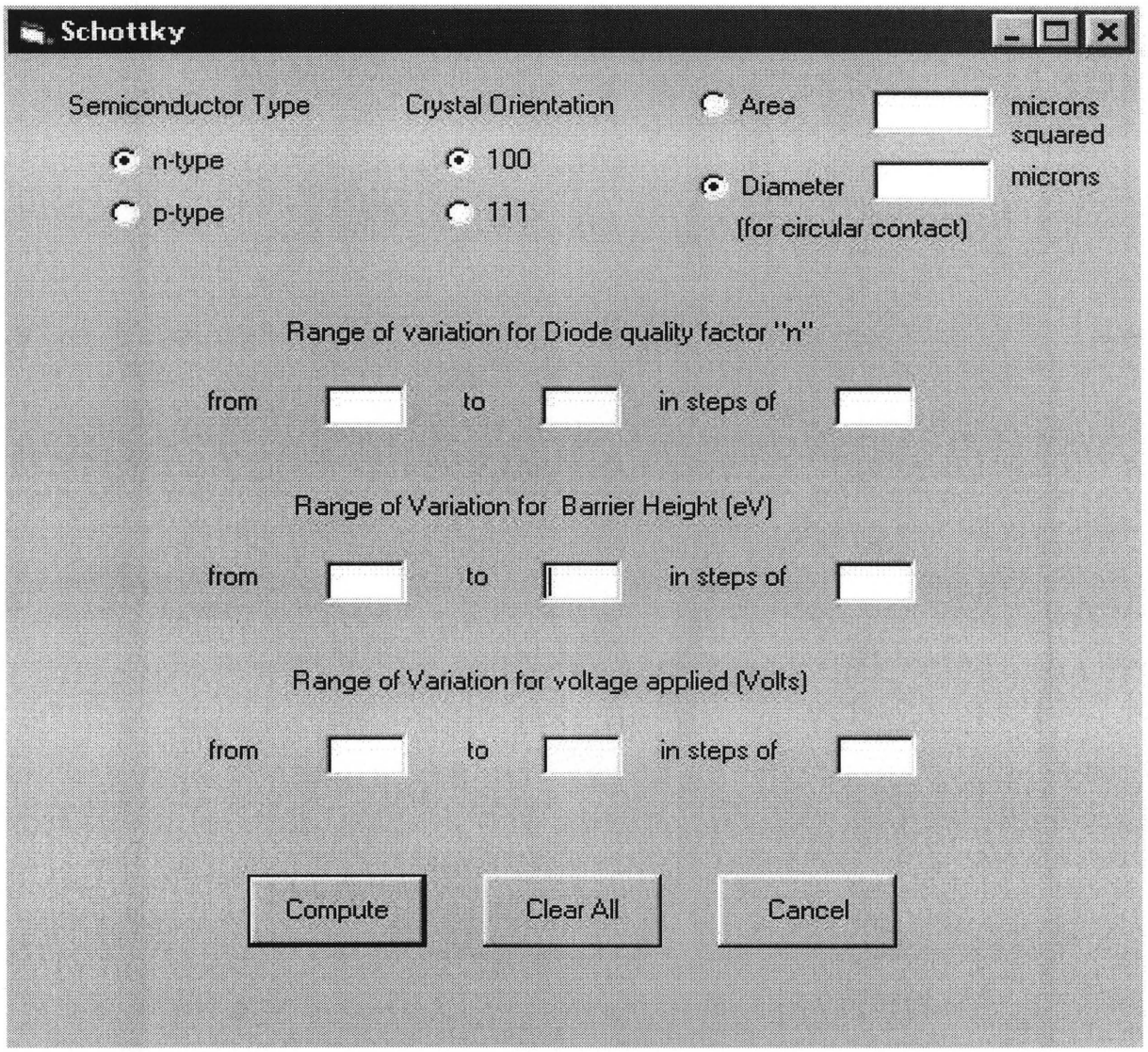
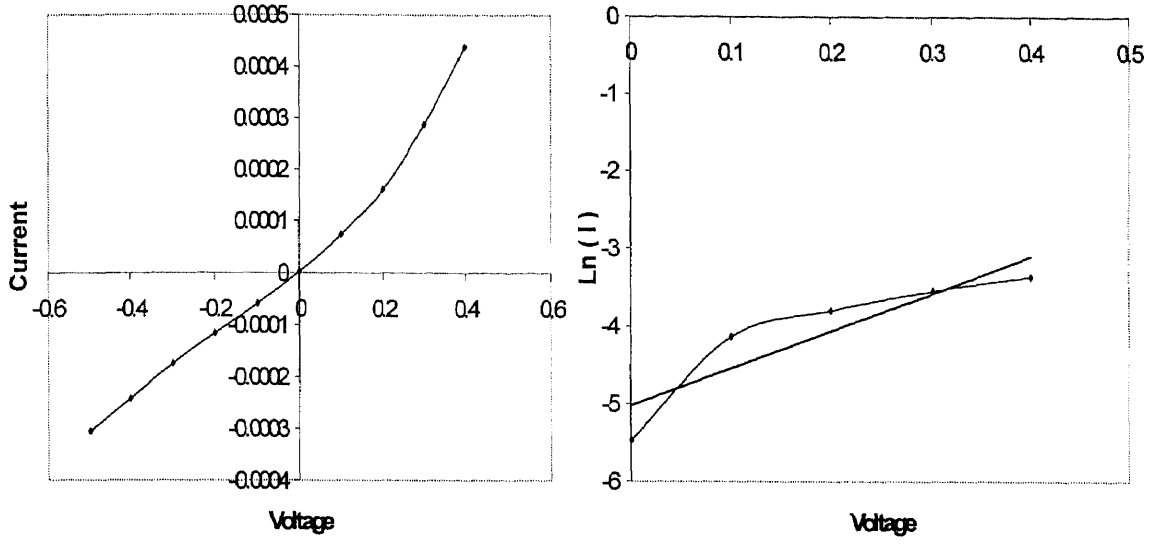
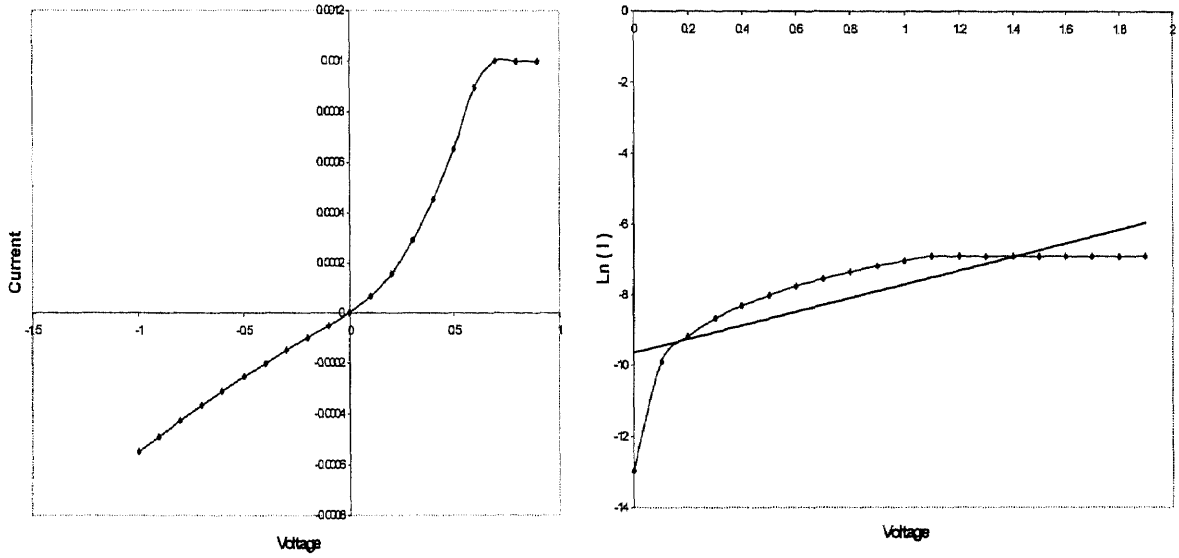


Fig. 5.2 The simple user interface written in Visual Basic 6.0[19]



(a) (b)

Fig. 5.3. (a) I-V plot, (b) Ln(I) v/s V plot for $TaSi_2$ for the positive I-V range.



(a) (b)

Fig. 5.4. (a) I-V plot, (b) Ln(I) v/s V plot for $TaSi_2$ for the positive I-V range.

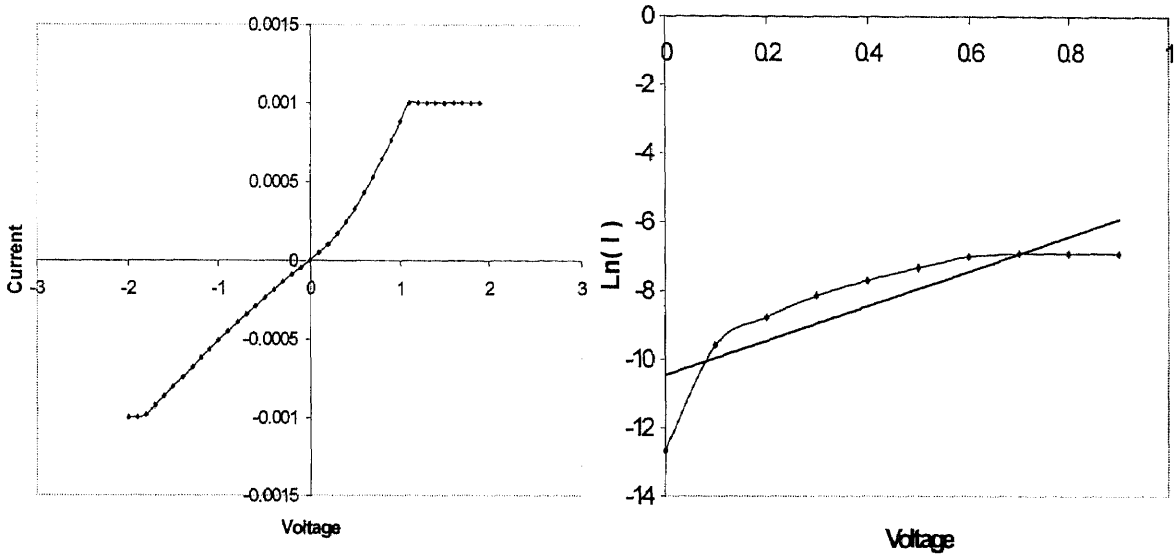


Fig. 5.5. (a) I-V plot, (b) Ln(I) v/s V plot for $TaSi_2$ for the positive I-V range.

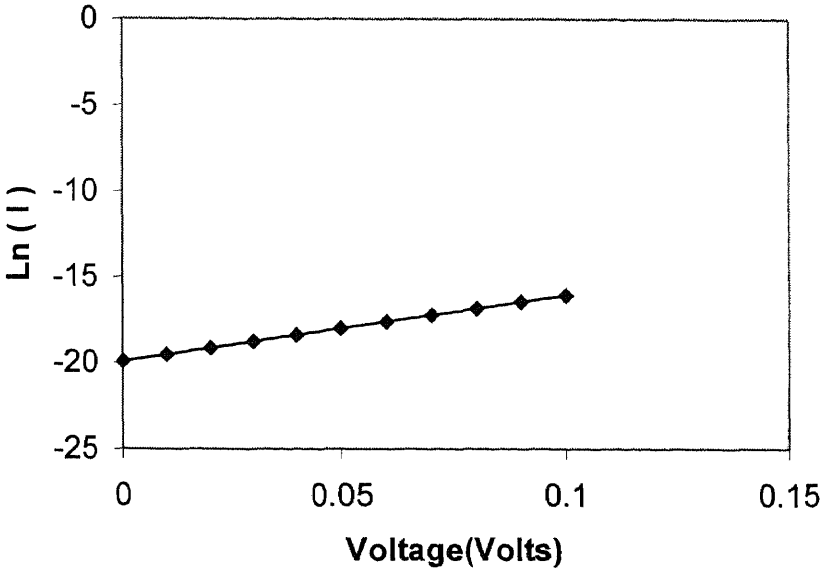


Fig. 5.6. Simulated plot for V v/s Log (I) plot for $TaSi_2$.

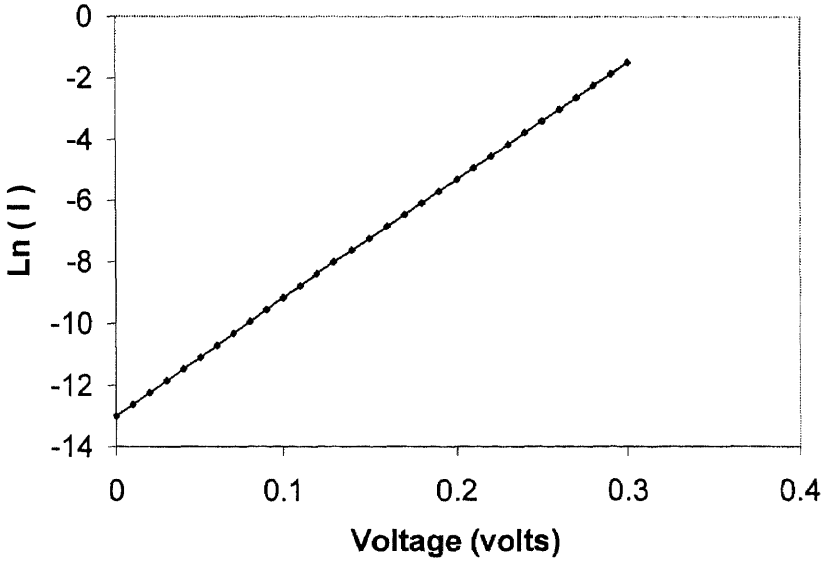


Fig. 5.7. Simulated plot for V v/s Log (I) plot for $TaSi_2$.

In Fig. 5.3(a), 5,4(a) and 5.5(a), the experimentally obtained current-voltage characteristics of $TaSi_2$/Si are presented. These measurements have been performed on three different samples of $TaSi_2$/Si. In order to obtain the barrier height from the experimentally measured I-V data, ln I v/s V plots corresponding to these measurements are presented in Figs. 5.3(b), 5.4(b), 5.5(b) respectively. These ln I values are fit to a straight line. The intercept on the ln I axis corresponding to V = 0 yields the values of I_S, which subsequently results in J_S and hence the barrier height. The results of the simulation of ln I v/s V are presented in Figs. 5.6 and 5.7. Again, the ln I intercept corresponds to V = 0 yields I_S and hence J_S. The barrier height is then determined from the value of J_S.

5.2 Metal Oxide Semiconductors (MOS)

A schematic showing the different stages of MOS capacitor process fabrication scheme is shown in Fig. 5.8. The bare wafers considered are of p-type Silicon of 4 inch diameter. They are cleaned in a 5:1 H_2SO_4 : H_2O_2 mixture for 10 minutes, followed by mixing in hot and cold de-ionized water respectively for 10 minutes each. This is followed by wet etch in native oxide for 3 minutes and cold de-ionized water rinse for 5 minutes and spin-drying. After this, furnace pre-cleaning is done in a mixture of 100:1 H_2O:HF for 1 minute. Then oxidation is performed at a temperature of 950° C to achieve a target thickness of 100 Å.

The second step is the deposition of the metal, which is performed by first furnace pre-cleaning the wafer in a mixture of 100:1 H_2O:HF for 1 minute, and cold de-ionized water rinse for 5 minutes. The actual deposition is performed at a base pressure of 8 X 10^{-7} Torr and at a temperature of 75° C to achieve a thickness of 4000 Å. The sheet resistivity is then measured. The third step is photolithography, involving transfer of a pattern of circular shapes of diameters in the range of 100-500μm in steps of 100μm, which forms the contact to the devices (capacitors). The step begins with application of photoresist to the frontside and hardbaking it on a hard bake at115°C. The wafer is then exposed to UV rays through a glass mask that is opaque at the circles that form the pattern. The UV rays that are incident pass through the transparent region of the mask. When this is developed, we get the derived pattern with the photoresist on it. This is followed by dry etch at 115°C for 1 minute to remove the metal that is exposed. Finally, the photoresist is stripped and annealed in forming gas at 400°C for 30 minutes to complete the process.

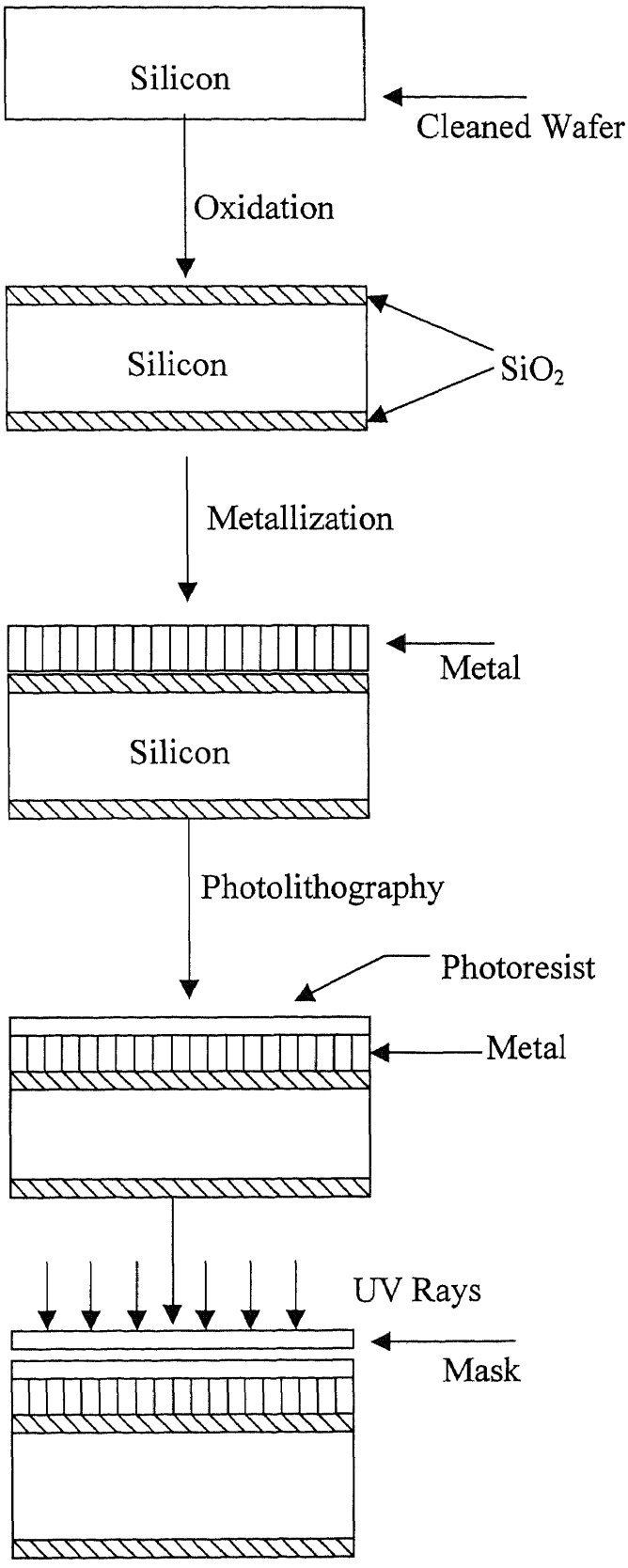


Fig. 5.8. Process Flow for the fabrication Metal Oxide Semiconductors

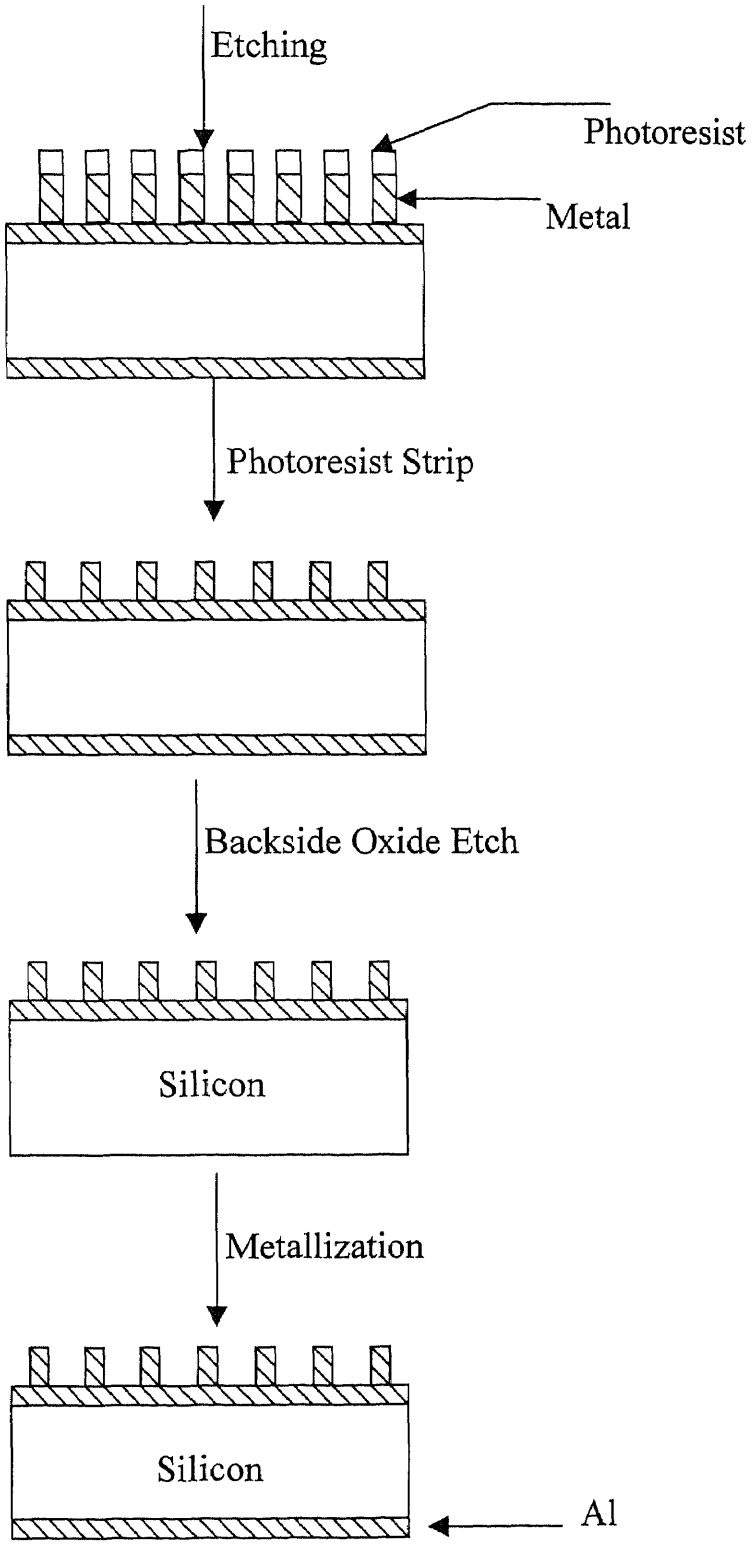


Fig. 5.8. Process Flow for the fabrication of Metal Oxide Semiconductors (continued)

5.2.1 Fowler-Nordheim Tunneling

The Fowler-Nordheim Tunneling (FNT) effect deals with current-conduction in SiO_2 films. The F-N current (J_{FN}) is given by the FNT equation[20]:

$$J_{FN} = AE_{OX}^2 e^{-B/E_{OX}}$$

$$A = \frac{q^3}{8\pi h \phi_b}; \quad B = \frac{8\pi (2m_{FN})^{1/2}}{3qh} \phi_b^{3/2}$$

Where, E_{OX} is the uniform electric field strength in the oxide, given by V_{OX}/t_{OX}, V_{OX} is the voltage across the oxide, t_{OX} is the oxide thickness, q is the electronic charge, h is the Planck's constant, ϕ_b is the tunneling barrier height and m_{FN} is the tunneling electron effective mass for F-N tunneling. The parameters A and B can be derived from the intercept and the slope of the F-N plot; i.e., the $\ln(J_{FN}/E^2_{OX})$ v/s $1/E_{OX}$ plot.

5.2.2 Results

In Fig.5.9, the measured I-V characteristics of MOS capacitors as a function of temperature are presented. These measurements were made at temperatures of 100, 200 and 300 K. The FN plots are presented in Fig. 5.10. As can be seen in the figures, within experimental errors, $\ln(J/E^2)$ v/s 1/E is indeed linear. These plots have been compared with previously performed experiments[21], shown in Fig.5.11.

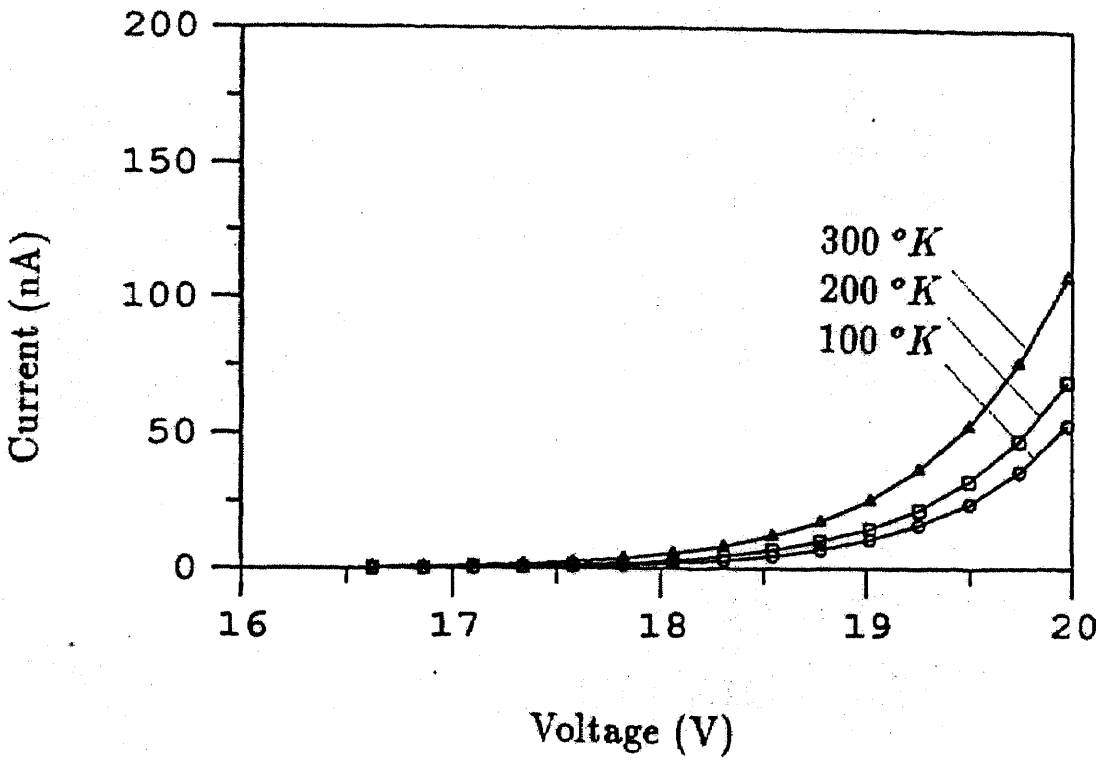


Fig.5.9. The comparison of experimental data (solid line) with the calculated data (dotted line) of I-V characteristics at temperature of 100, 200 and 300 K[22].

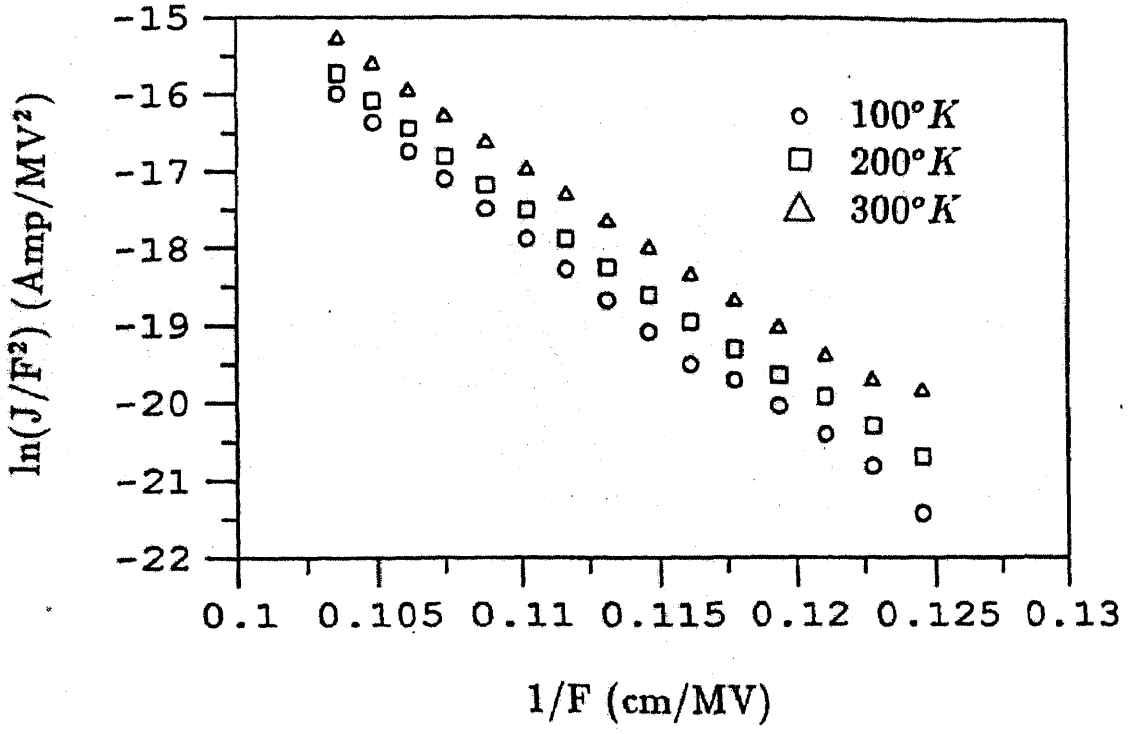


Fig.5.10. The FN plots of tunneling data from silicon into SiO_2 at temperatures of 100, 200 and 300 K[22].

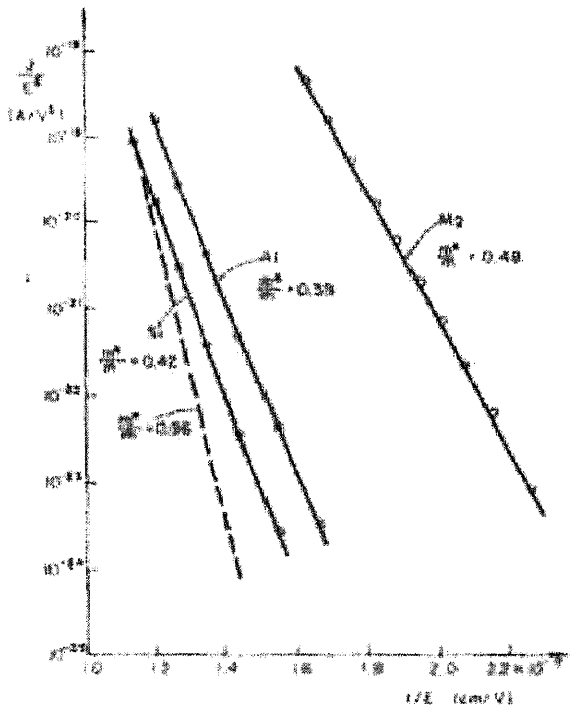


Fig.5.11. FNT plot showing the relative effective mass m*/m corresponding to the respective slopes[21].

CHAPTER 6

CONCLUSIONS

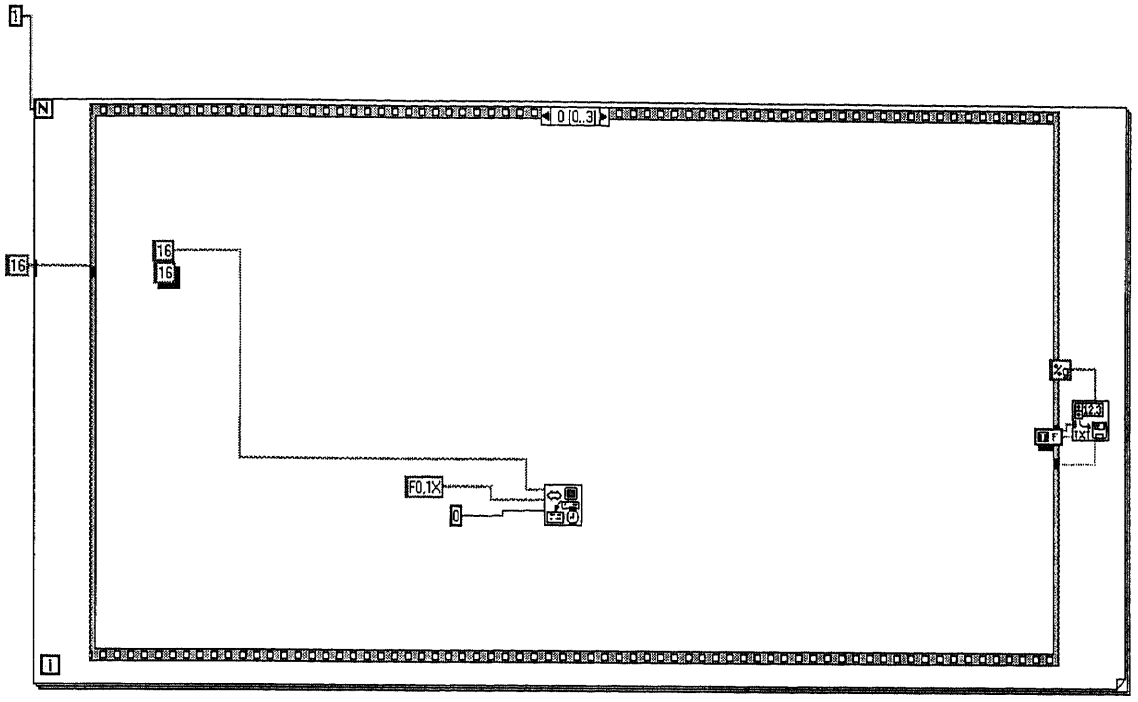
In this study, LabVIEW^{TM} has been successfully implemented and demonstrated for real-time data acquisition of I-V measurements. The demonstration has been shown for two particular device structures – Metal Semiconductor contact and Metal Oxide Semiconductor capacitor. The fabrication steps involved in these devices have been summarized. The current-voltage relationships in metal semiconductor contacts and MOS devices have been discussed and verified experimentally. Sheet resistance measurements have been made on $TaSi_2$ films. These measurements are in agreement with those reported in the literature.

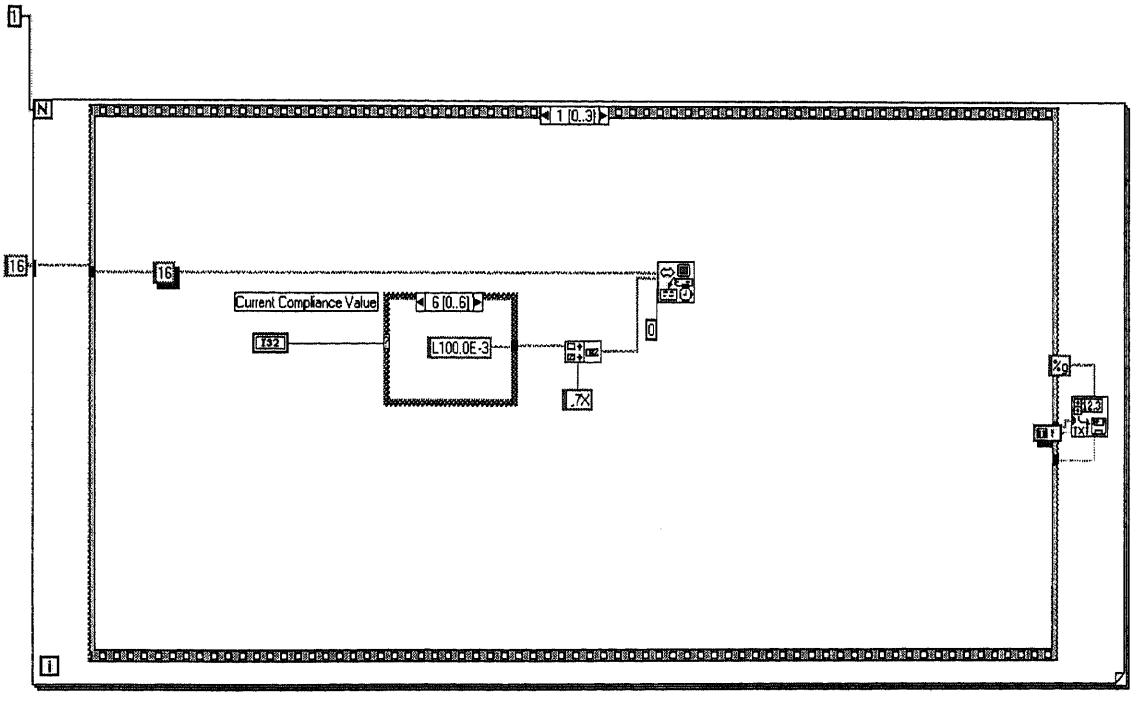
For metal-semiconductor contacts, simulation of the current-voltage characteristics have been made using Visual Basic6.0. The value of the barrier height of $TaSi_2$/Si obtained from experimental measurements of the current-voltage characteristics have been shown to be in accord with expectations. The saturation current density values are in accord with simulations.

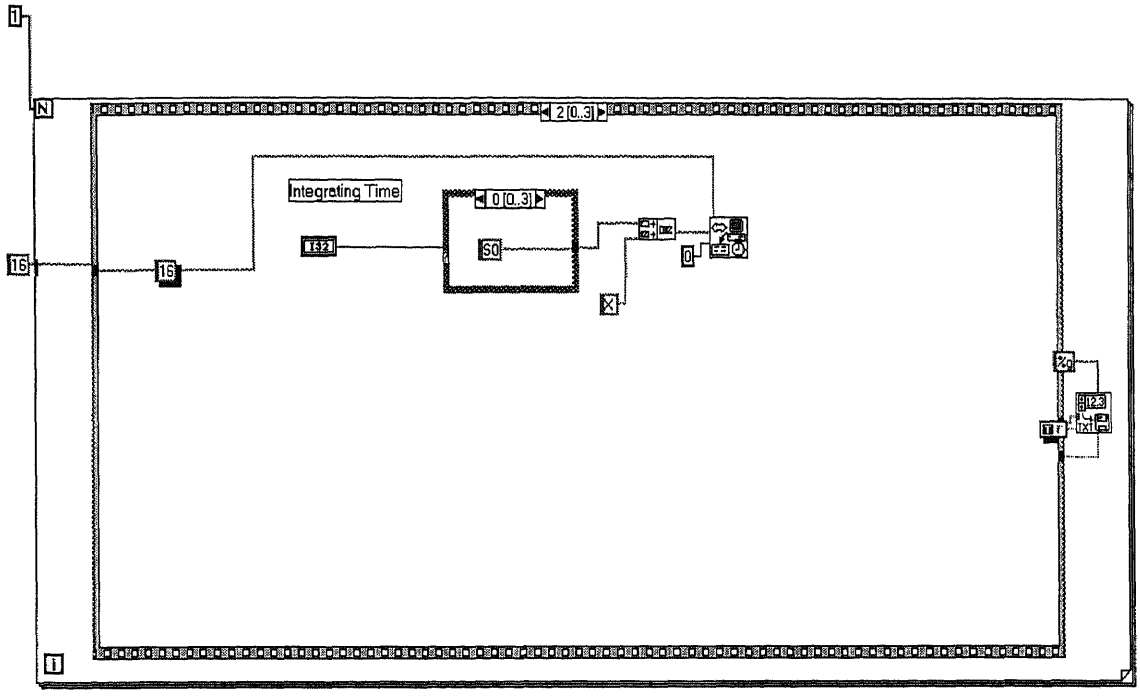
For MOS devices, the measured current-voltage characteristics are seen to follow the well-known Fowler-Nordheim tunneling mechanism of current conduction in thin SiO_2 films.

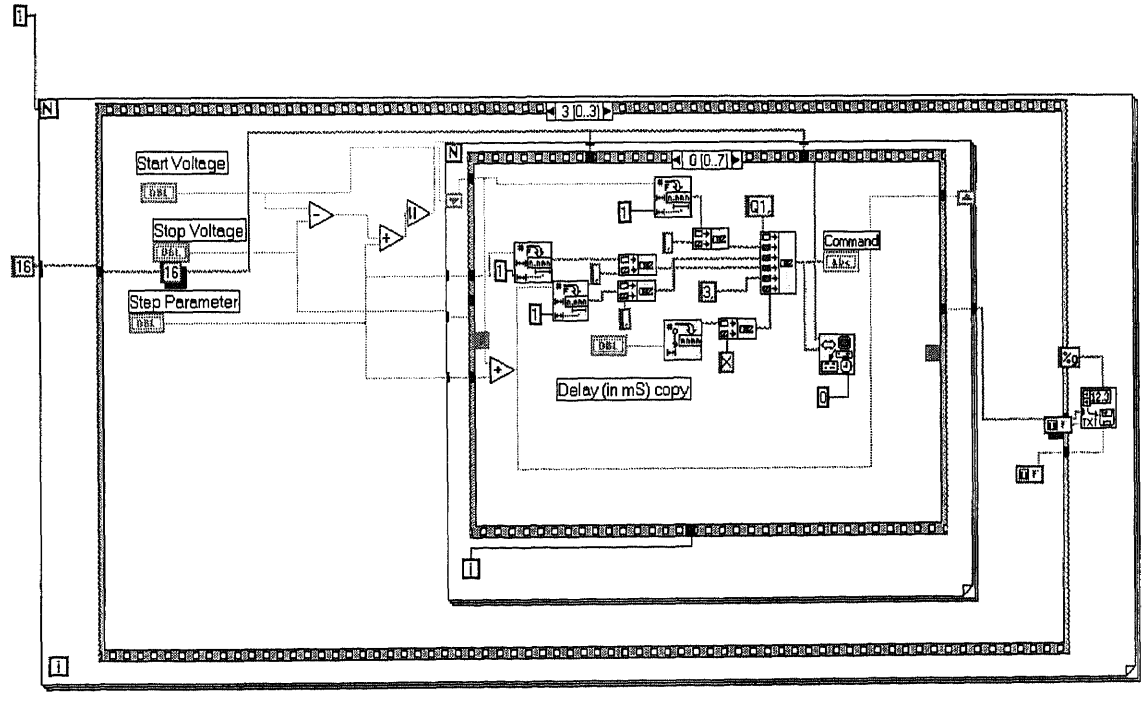
APPENDIX A

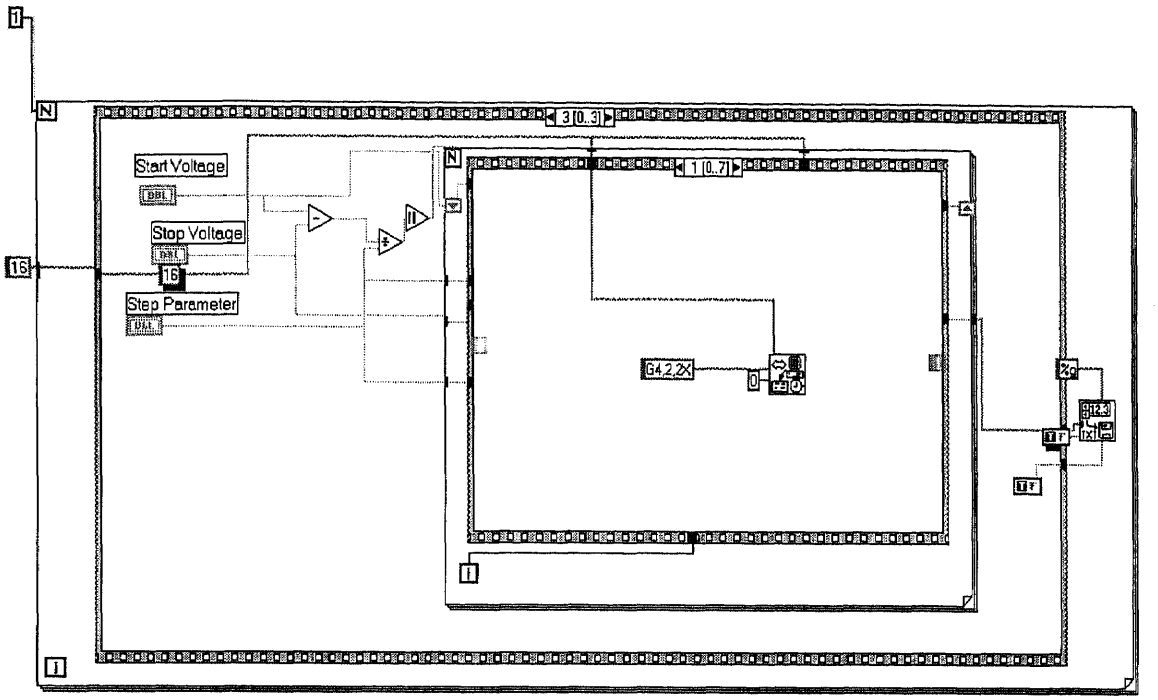
LABVIEW PROGRAM FOR I-V CHARACTERISTICS

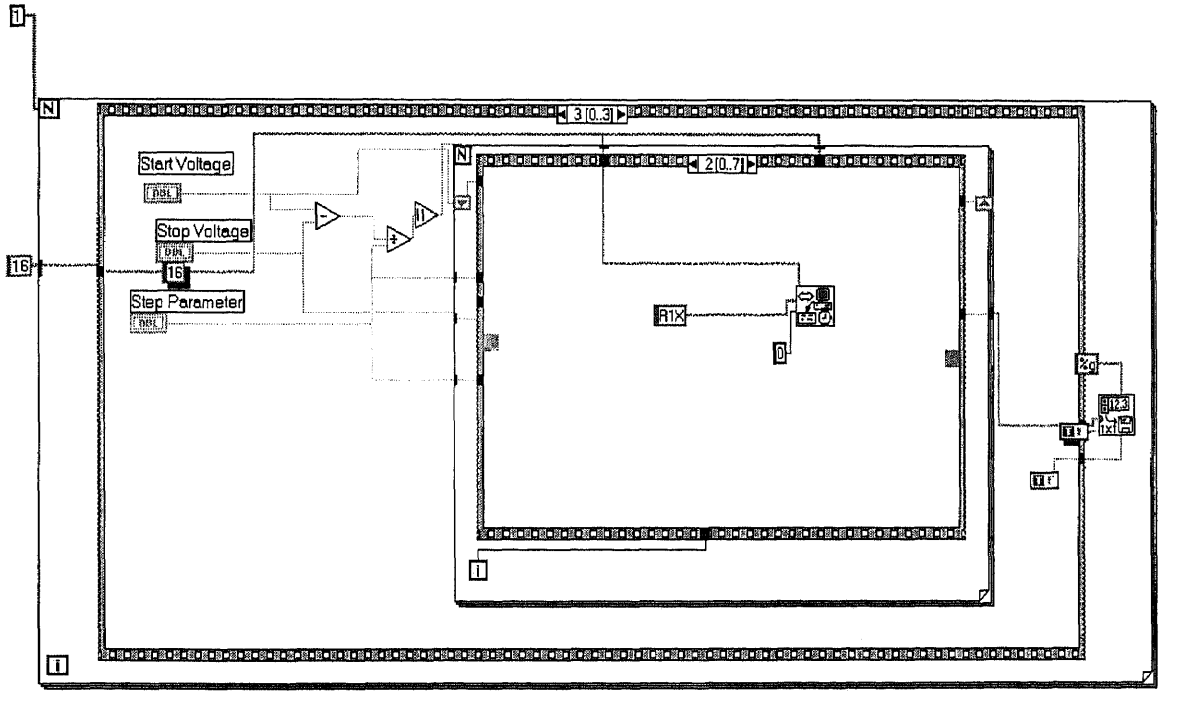

i
N
0 [0..3]
16
16
16
F0.1X
0

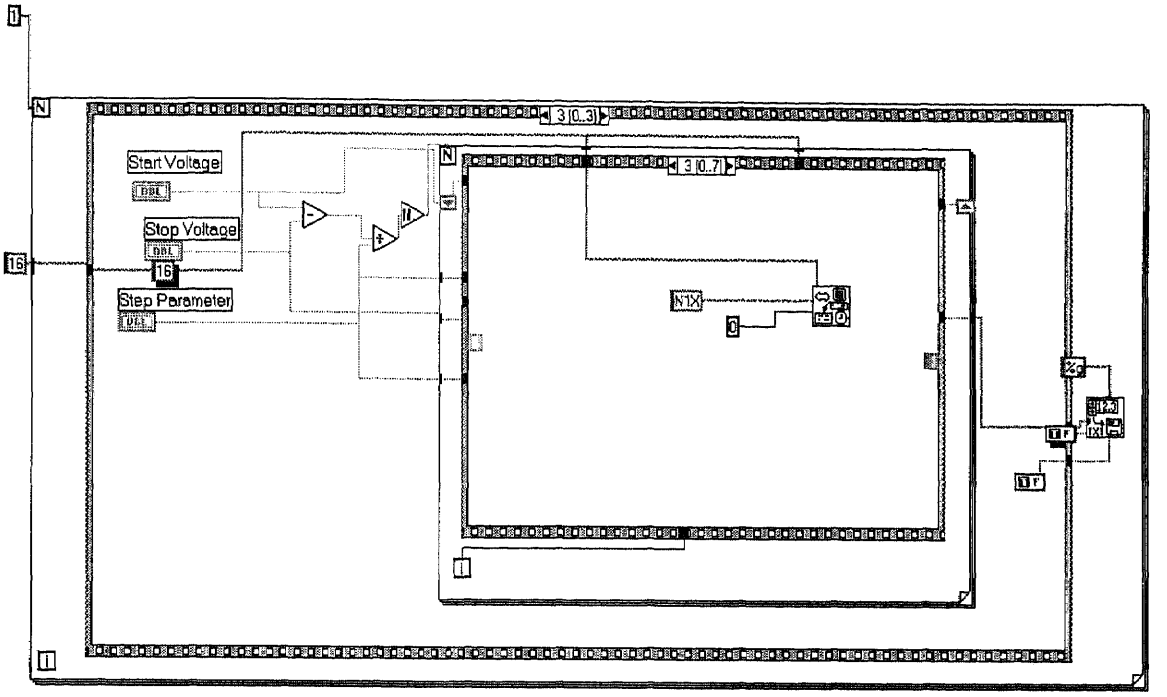

i
N
1 [0..3]
16
16
Current Compliance Value
I32
6 [0..6]
L100.0E-3
.7X
0

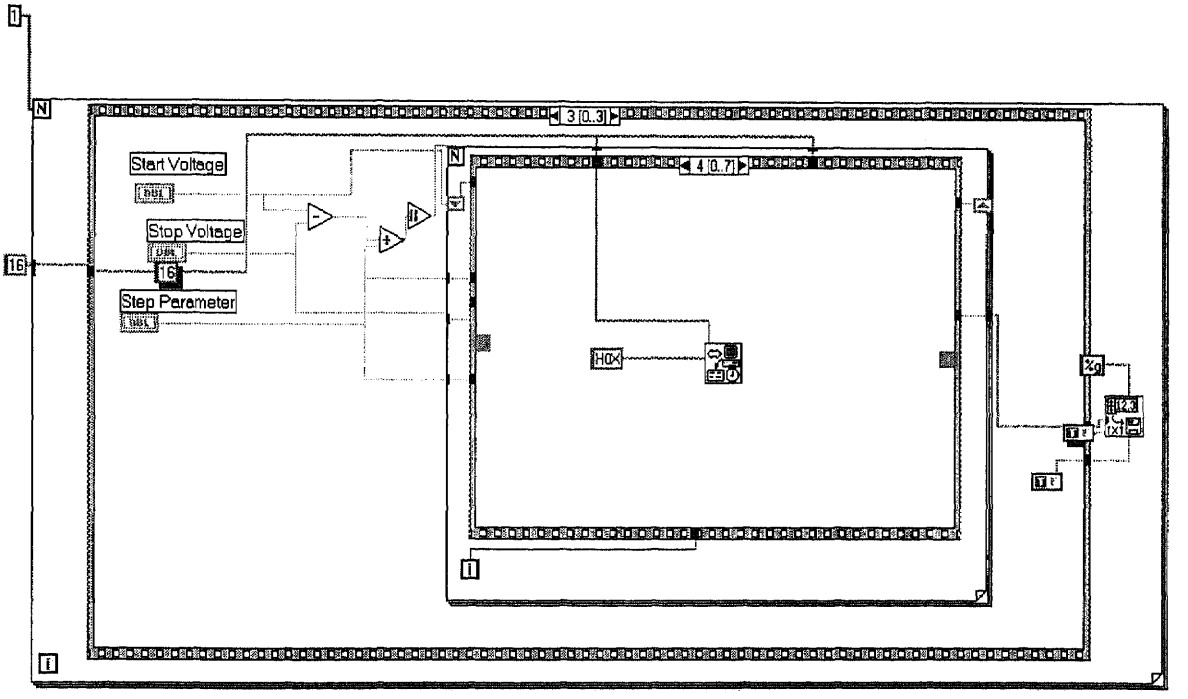

i
N
2 [0..3]
Integrating Time
0 [0..3]
16
16
I32
S0
0
i

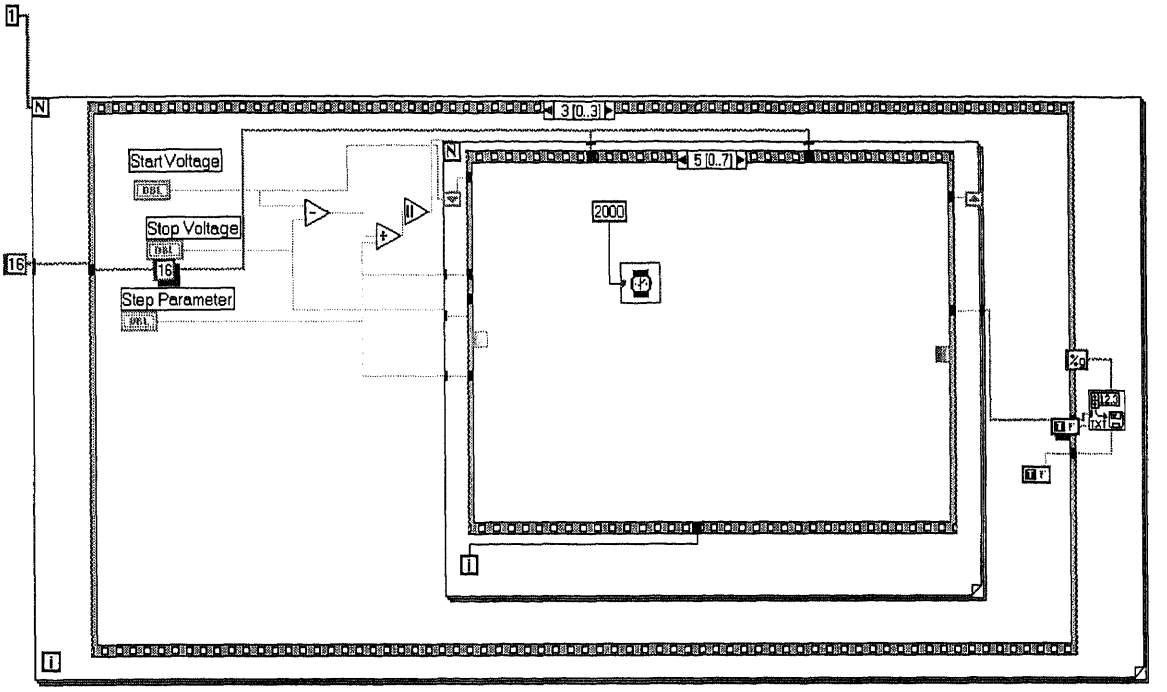

i
N
3 [0..3]
Start Voltage
Stop Voltage
16
Step Parameter
N
0 [0..7]
Command
Delay (in mS) copy
16
i

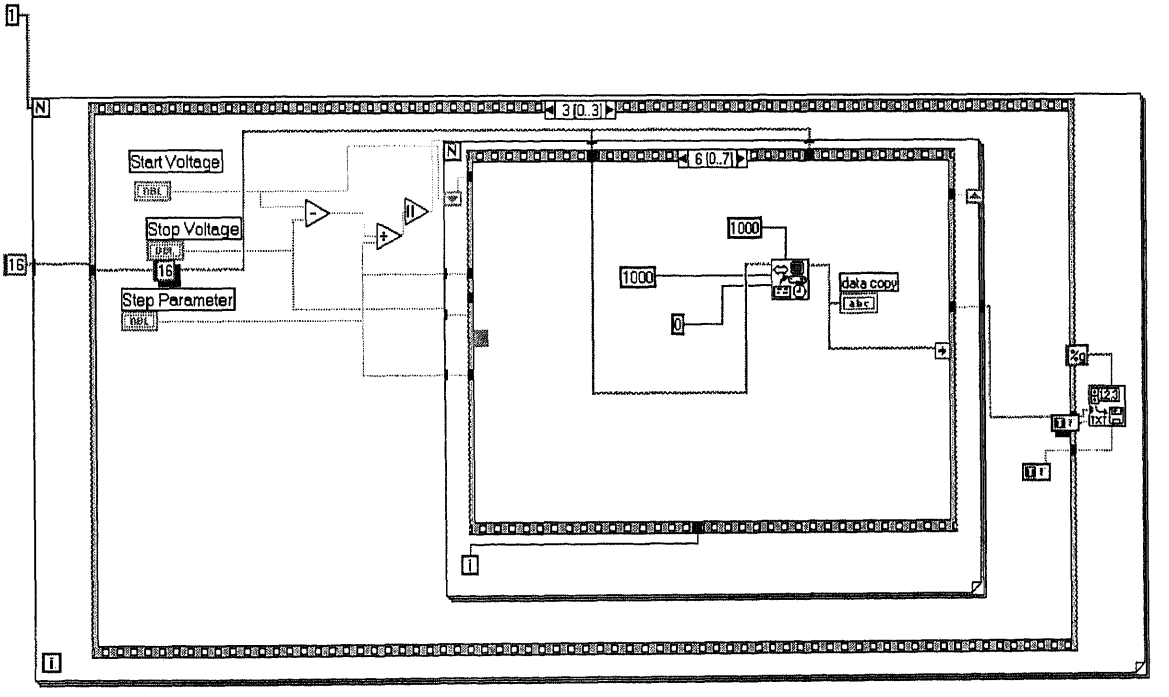

i
N
3 [0..3]
Start Voltage
DBL
Stop Voltage
DBL
16
16
Step Parameter
DBL
N
1 [0..7]
G4,2,2X
0
i
i

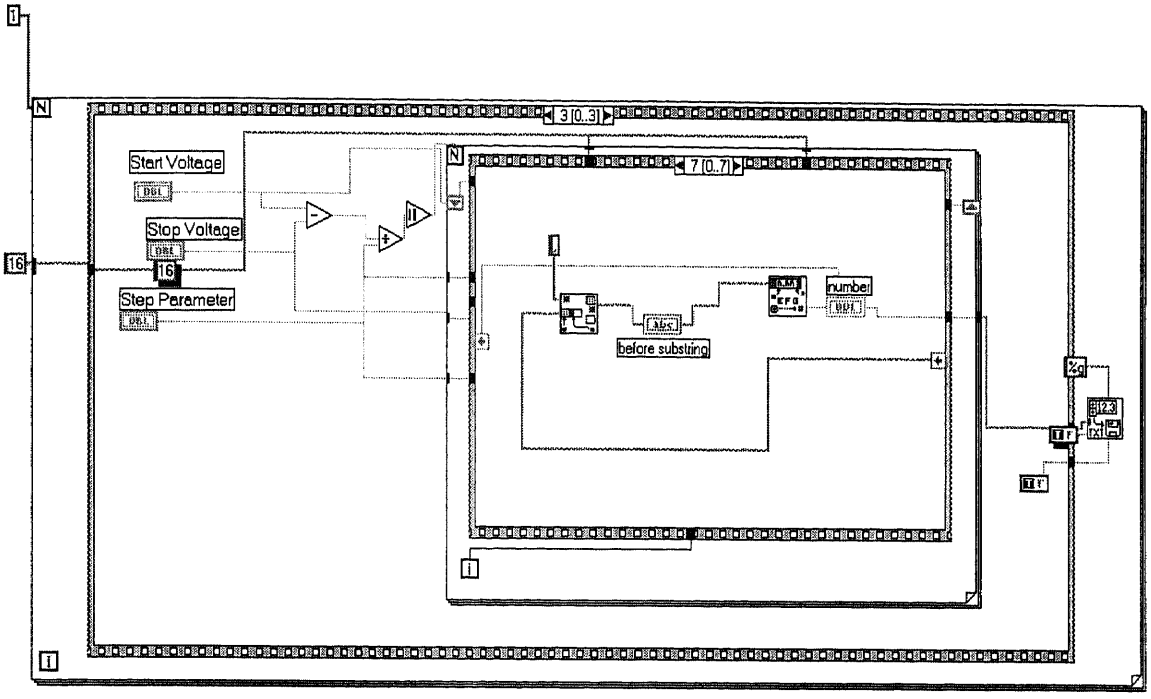

i
N
3 [0..3]
Start Voltage
DBL
Stop Voltage
DBL
16
16
Step Parameter
DBL
N
2 [0..7]
R1X
0
i
i


Start Voltage
Stop Voltage
Step Parameter
3 [0..3]
3 [0..7]
N1X
0


Start Voltage
Stop Voltage
Step Parameter
3 [0..3]
4 [0..7]
H0X


Start Voltage
Stop Voltage
Step Parameter
3 [0..3]
5 [0..7]
2000


Start Voltage
Stop Voltage
Step Parameter
3 [0..3]
6 [0..7]
1000
1000
0
data copy


1
N
3 [0..3]
Start Voltage
DBL
Stop Voltage
DBL
16
16
Step Parameter
DBL
N
7 [0..7]
number
I32
before substring
i
I
123

APPENDIX B

PROCESS SHEETS FOR METAL SEMICONDUCTOR CONTACTS AND MOS DEVICE STRUCTURES

RAJ

$TaSi_2$
Wafer Cleaning and Oxidation

	Date	Wafers	Operator	Comments
Starting material: 4", p-type Si wafers, (100) ρ= ..... Ω.cm, thickness .....µm 4", n-type Si wafers, (100) ρ= ..... Ω.cm, thickness .....µm Wafers identification: back side (1 - 3) n-type (20-25) p type	9/8/99	15 6 15 3	RAJ	3 wafers: 100A; 3 wafers: 300A, 3 wafers: 500A 3 wafers: 700A; 3 wafers: 900A 3 wafers: 100A; 3 wafers: 300A, 3 wafers: 500A 3 wafers: 700A; 3 wafers: 900A
1. M-pyrol 95°C 10 minutes ~~PRIMARY~~ 10 minutes SECONDARY	11/3/99	1	RAJ	
2. Rinse COLD DI 10 minutes	11/3/99	"	RAJ	
3. Spin dry	11/3/99	"	RAJ	
4. P-clean 5:1 H_2SO_4:H_2O_2 110°C 10 minutes	10/9/99 11/1/99	9 3	RAJ SS	New n type samples
5. Rinse HOT DI 10 minutes	10/5/99	9	RAJ	
6. Rinse COLD DI 5 minutes	10/5/99	9	RAJ	
7. Spin dry	10/5/99	9	RAJ	
8. Wet etch native oxide BOE p-type Temp 25°C Time: 3 min	10/5/99 11/1/99	9 3	RAJ SS	New n type
9. Rinse COLD DI 5 minutes	10/5/99	9	RAJ	
10. Spin dry				
11. Measure the resistivity on the test wafer 4-point probe	11/1/99	9	RAJ	[illegible] ~ 0.[illegible] x 10[illegible]
12. Furnace pre-clean 100:1 H_2O:HF 1 minute	10/5/99	9		
13. Rinse COLD DI 5 minutes	10/5/99	9	RAJ	
14. Spin dry	10/5/99	9	RAJ	
15. Dry Oxidation TUBE # 3 O_2: 7.5SLM Temp: 950°C Time: ..10.... Min Target Tickness: ..100.....A	10/15 11/1	9 3	SS/RAJ SS	For RAJ - 2 min run
16. Measurement oxide thickness				Thk ~ 200 ± 3 A° and ~ 151 ± 3 A°

11/1 3 SS Thk ~ 135 A°

$TaSi_2$ Deposition

	Date	Wafers	Operator	Comments
1. Furnace pre-clean 100:1 H_2O:HF 1 minute	10/22/99	9	KAJ	
2. Rinse COLD DI 5 minutes	10/22/99	9	KAJ	
3. Spin dry	10/22/99	9	KAJ	
4. $TaSi_2$ - FRONTSIDE Base Pressure: 8.0×10^{-7} torr Temperature: ~~300°C~~ 750°C Dep. Rate: 2 Å/sec Thickness: 100 Å Thickness: 300 Å 4000Å Thickness: ~~500 Å~~ Thickness: ~~700 Å~~ Thickness: ~~900 Å~~	10/22/99	6	KAJ	3p x 3in wafers for Ti/Si alignment p-type - Wafer # 20, 21, 22 n-type - Wafer # 1, 2, 3
8. Measure sheet resistivity 5 pts. / wafer 2 wafers / 10 wafers	10/22/99	C	KAJ	Measurement of sheet resistivity

Photolithography – FRONTSIDE

	Date	Wafers	Operator	Comments
1. Apply Photoresist - FRONTSIDE Shipley 3813 2000rpm	10/29	6	KAJ	Caution! Keep clean the FRONTSIDE 3p x 3in wafers
2. Hard Bake: HOT PLATE 115°C	10/29	C	KAJ	
3. Align and expose Mask: DOTS/~~SQUARES~~ Time: 15 seconds	10/29	C	KAJ	
4. Develop	10/29	C	KAJ	
5. Inspect	10/29	C	KAJ	

$TaSi_2$ Dry Etch

	Date	Wafers	Operator	Comments
1. Hard bake PR: HOT PLATE 115°C 1 30 min	11/7	6	RAJ	
2. Dry etch $TaSi_2$ (FRONTSIDE) Trion Phantom	11/7 X 11/12	6	RAJ	
3. Inspect Etched to completion? YES	11/12	6	RAJ	
4. Strip PR M-pyrol 95°C 10 minutes PRIMARY 10 minutes SECONDARY	11/12	6	RAJ	
5. Rinse COLD DI 10 minutes	11/12	6	RAJ	
6. Spin dry	11/12	6	RAJ	
7. Inspect.	11/12	6	RAJ	

ANNEAL

	Date	Wafers	Operator	Comments
1. M-Pyrol 10min. SECONDARY ONLY	11/21	6	RAJ	
2. Rinse COLD DI 10min.	11/21	6	RAJ	
3. Spin Dry	11/21	6	RAJ	
4. Anneal in Forming gas 400C 30min.	11/21	6	RAJ	

	Date	wafer	operator	comment

Photolithography-FRONTSIDE

1. apply photoresist—frontside
   Shipley 3813
2. Hard bake: Hot plate
   115C
3. Align and expose
   Mask: Dots/squares
   Time: 15 seconds
4. Develop
5. Inspect

Comments: Keep clean thee Frontside

TaSi2 Dry Etch

1. Hard bake PR: HOT Plate
   115C
   30min
2. Dry etch TaSi2 (FRONT SIDE)
   Trion Phantoom
3. Inspect
   Etched to completion?
4. Strip PR
   M-pyrol
   95C
   ~~10~~ Minutes PRIMARY
   ~~10~~ minutes SECONDARY
5. Rinse COLD DI
   10 minutes
6. Spin dry
7. Inspect

Anneal

1. M-Pyrol
   10min. SECONDARY ONLY
2. Rinse COLD DI
3. Spin dry
4. Anneal in Forming gas
   400C
   30min.

1553 Å

APPENDIX C

IEEE-488.2 DEVICE-DEPENDENT COMMANDS

IEEE-488.2 device-dependent commands are the most important commands associated with instruments programming because they control most instrument operating modes. The IEEE-488.2 bus treats these commands as data. All Source Measure Unit (SMU) front panel operations can be programmed with these commands. A summary of the commands, some of which have been implemented in the program, is given below:

Mode	Command	Description
Modify Sweep List	A(level),(range),(delay), First(,last)	Modify sweep list points
Bias Operation	B(level),(range),(delay)	Select Bias Operation
Calibration	C step(,value) X	Calibrate Instrument
Display	D0X	Return display to normal
	D1,aaa...aX	Display ASCII characteristics
	D2,aaa...aX	Display and store ASCII Characters
Source and Function	F(source),(function)	Select source (V or I) and function (dc or sweep)
Output Data Format	G(items),(format),(lines)	Selects items included, format, and lines per talk in output
IEEE Immediate Trigger	H0X	Cause an immediate bus trigger

Mode	Command	Description
Self-tests	J0X	Restore factory defaults
	J1X	Perform memory test
	J2X	Perform display test
EOI and Bus Hold-off	K0	Enable EOI, enable Hold-off on X
	K1	Display EOI, enable Hold-off on X
	K2	Enable EOI, disable Hold-off on X
	K3	Disable EOI, disable Hold-off on X
Compliance	L(level),(range)	Set compliance level and range
SRQ Mask and Serial Poll Byte	M(mask), (compliance)	Select conditions that will cause a service-request
Operate	N0	Place unit in standby mode
	N1	Place unit in operate mode
Output Sense	O0	Select local sensing
	O1	Select remote sensing
Filter	P0	Measurement filter disabled
	P1	2-reading filter
	P2	4-reading filter
	P3	8-reading filter
	P4	16-reading filter
	P5	32-reading filter
Create/Append Sweep List	Q0,(level),(range),(delay), (count)	Create fixed-level sweep

Mode	Command	Description
	Q1,(start),(stop),(step), (range),(delay)	Create linear stair sweep
	Q2,(start),(stop),(points), (range),(delay)	Create logarithmic stair sweep
	Q3,(level),(range),(pulses), (t_{ON}),(t_{OFF})	Create fixed level pulsed sweep
	Q4,(start),(stop),(step), (range),(t_{ON}),(t_{OFF})	Create linear stair pulsed sweep
	Q5,(start),(stop),(t_{ON}),(t_{OFF})	Create logarithmic stair pulsed sweep
	Q6,(level),(range),(delay), (count)	Append fixed level sweep
	Q7,(start),(stop),(step), (range),(delay)	Append linear stair sweep
	Q8,(start),(stop),(points), (range),(delay)	Append logarithmic stair sweep
	Q9,(level),(range),(pulses) (t_{ON}),(t_{OFF})	Append fixed level pulsed sweep
	Q10,(start),(stop),(step), (range),(t_{ON}),(t_{OFF})	Append linear stair pulsed sweep
	Q11,(start),(stop),(points), (range),(t_{ON}),(t_{OFF})	Append logarithmic stair pulsed sweep

Mode	Command	Description
Trigger Control	R0	Disable input/output triggers
	R1	Enable input/output triggers
Integration Time	S0	416μsec integration time
Integration Time (contd.)	S1	4msec integration time
Trigger Configuration	S2	16.67msec integration time
	S3	20msec integration time
	T(origin),(in),(out),(end)	Program input trigger origin and effects, output triggers, and end-of-sweep output trigger.
Status	U0	Send model no. and revision
	U1	Send error status word
	U2	Send stored ASCII string
	U3	Send machine status word
	U4	Send measurement parameters
	U5	Send compliance value
	U6	Send suppression value
	U7	Send calibration status word
High Voltage Current	U8	Send defined sweep value
	U9	Send warning status word
Default delay	V0	Disable high voltage output
	V1	Enable high voltage output

Mode	Command	Desciption
Execute	W0	Disable default delay
Terminator	W1	Enable default delay
	X	Execute commands
	Y0	<CR><LF>
Suppress	Y1	<LF><CR>
	Y2	<CR>
	Z0	Disable suppression
	Z1	Enable suppression

APPENDIX D

SIMULATION PROGRAM IN VB 6.0 FOR MOS

```
Dim T, f2, f, f3, cnt, z As Integer
Dim x As Excel.Application


Private Sub Command1_Click()

Dim A, b, kT, n, v, area, d, Isat, term As Double
If Not (ntype.Value Or ptype.Value) Then
MsgBox "Please check one of the type of substrates" & "n" & "p", vbOKOnly
ntype.SetFocus
Exit Sub
End If

If Not (orientn_100.Value Or orientn_111.Value) Then
MsgBox "Please check one of the crystal orientations" & "100" & "111", vbOKOnly
orientn_100.SetFocus
Exit Sub
End If

If Not (area_opt.Value Or Dia_opt.Value) Then
MsgBox "Please check the either area or diameter to calculate area", vbOKOnly
area_opt.SetFocus
Exit Sub
End If

If area_opt.Value And area_txt.Text = "" Then
MsgBox "Please enter the area of the contact", vbOKOnly
area_txt.SetFocus
Exit Sub
End If

If (Not IsNumeric(area_txt.Text) And area_opt.Value) Then
MsgBox "Please enter a numerical value for the area", vbOKOnly
area_txt.Text = vbNullString
area_txt.SetFocus
Exit Sub
End If

If Dia_opt.Value And dia_txt.Text = "" Then
MsgBox "Please enter the diameter of the circular contact", vbOKOnly
dia_txt.SetFocus
```

```
Exit Sub
End If

If Not IsNumeric(dia_txt.Text) Then
MsgBox "Please enter a numerical value for the diameter", vbOKOnly
dia_txt.Text = vbNullString
dia_txt.SetFocus
Exit Sub
End If

If B_range_frm.Text = "" Then
MsgBox "Please enter the starting value of Barrier voltage variation", vbOKOnly
B_range_frm.SetFocus
Exit Sub
End If

If Not IsNumeric(B_range_frm.Text) Then
MsgBox "Please enter a numerical value for the starting value of Barrier voltage
variation", vbOKOnly
B_range_frm.Text = vbNullString
B_range_frm.SetFocus
Exit Sub
End If

If B_range_to.Text = "" Then
MsgBox "Please enter the final value of Barrier voltage variation", vbOKOnly
B_range_to.SetFocus
Exit Sub
End If
If Not IsNumeric(B_range_to.Text) Then
MsgBox "Please enter a numerical value for the final value of Barrier voltage
variation", vbOKOnly
B_range_to.Text = vbNullString
B_range_to.SetFocus
Exit Sub
End If

If B_steps.Text = "" Then
MsgBox "Please enter the step voltage by which the Barrier voltage has to be varied",
vbOKOnly
B_steps.SetFocus
Exit Sub
End If
If Not IsNumeric(B_steps.Text) Then
MsgBox "Please enter a numerical value for the step voltage by which the Barrier
voltage has to be varied ", vbOKOnly
```

```
B_steps.Text = vbNullString
B_steps.SetFocus
Exit Sub
End If

If V_range_frm.Text = "" Then
MsgBox "Please enter the starting value of Applied voltage variation", vbOKOnly
V_range_frm.SetFocus
Exit Sub
End If
If Not IsNumeric(V_range_frm.Text) Then
MsgBox "Please enter a numerical value for the starting value of Applied-voltage
variation", vbOKOnly
V_range_frm.Text = vbNullString
V_range_frm.SetFocus
Exit Sub
End If


If V_range_to.Text = "" Then
MsgBox "Please enter the final value of Applied voltage variation", vbOKOnly
V_range_to.SetFocus
Exit Sub
End If
If Not IsNumeric(V_range_to.Text) Then
MsgBox "Please enter a numerical value for the final value of Applied-voltage
variation", vbOKOnly
V_range_to.Text = vbNullString
V_range_to.SetFocus
Exit Sub
End If

If V_steps.Text = "" Then
MsgBox "Please enter the step voltage by which the Barrier voltage has to be varied",
vbOKOnly
V_steps.SetFocus
Exit Sub
End If
If Not IsNumeric(V_steps.Text) Then
MsgBox "Please enter a numerical value for the step voltage by which the Barrier
voltage has to be varied ", vbOKOnly
V_steps.Text = vbNullString
V_steps.SetFocus
Exit Sub
End If
```

```
If ntype.Value And orientn_100.Value Then
A = 252
ElseIf ntype.Value And orientn_111.Value Then
A = 264
ElseIf ptype.Value Then
A = 79.2
End If
T = 300
kT = 0.026
If area_opt.Value = True Then
area = area_txt.Text * (10 ^ -8)
ElseIf Dia_opt.Value = True Then
d = dia_txt.Text
area = ((10 ^ -8) * (3.1415927 * d * d)) / 4
End If
z = (Abs(V_range_frm.Text) - 0) / (V_steps.Text)

Set x = CreateObject("Excel.application")
f = 1
f3 = 0
x.Visible = True
x.Workbooks.Add
x.Worksheets("sheet1").Activate
For n = nfrm_text.Text To nto_text.Text Step nstep_text.Text
  f2 = 3
  Cells(1, (f3 + 1)).Value = "Diode Quality Factor" & "n=" & n
  Cells(2, (f3 + 1)).Value = "Barrier Height"
  Cells(2, (f3 + 2)).Value = "Voltage"
  Cells(2, (f3 + 3)).Value = "LOG(I)"
  Cells(2, (f3 + 4)).Value = "Current"

  For b = B_range_frm.Text To B_range_to.Text Step B_steps.Text
    Isat = (A * T * T * Exp(-b / kT)) * area                    'Value of Is for each barrier
height value
      cnt = 1
      For v = V_range_frm.Text To V_range_to.Text Step V_steps.Text
      term = Isat * Exp(v / (n * kT))
      Cells(f2, (f3 + 1)).Value = b
      If (cnt = (z + 1)) Then
      Cells(f2, (f3 + 2)).Value = 0
      Else: Cells(f2, (f3 + 2)).Value = v
      End If
      Cells(f2, (f3 + 4)).Value = term
      Cells(f2, (f3 + 3)).Value = Log(Abs(term)) / Log(Exp(1))
            f2 = f2 + 1
      cnt = cnt + 1
```

```
        Next v
    Next b
    f3 = f3 + 4
Next n
End Sub

Private Sub Command2_Click()
area_txt.Text = vbNullString
dia_txt.Text = vbNullString
nto_text.Text = vbNullString
nfrm_text.Text = vbNullString
nstep_text.Text = vbNullString
B_range_frm.Text = vbNullString
B_range_to.Text = vbNullString
V_range_frm.Text = vbNullString
V_range_to.Text = vbNullString
B_steps.Text = vbNullString
V_steps.Text = vbNullString
ntype.SetFocus
If f Then
x.Quit
f = 0
End If
End Sub

Private Sub Command3_Click()
x.Quit
RAJ.Visible = False
Unload RAJ
End Sub
```

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