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ABSTRACT

PREPARATION AND PROPERTIES OF TANTALUM SILICIDE FILMS ON SILICON SUBSTRATES

by

Lei Jin

Tantalum silicide ($TaSi_2$) thin films were sputter deposited on p- type and n- type silicon substrates using VARIAN 3125 magnetron DC sputtering system with $TaSi_2$ target. The thicknesses of $TaSi_2$ thin films considered in this study are 200Å, 600Å and 1000Å, respectively. The $TaSi_2$/Si wafers were annealed at temperatures in the range of 400 to 900°C. The sheet resistances of $TaSi_2$ thin films with various thicknesses were measured by four-point probe before and after annealing. The sheet resistance decreases with increase in annealing temperature and decreases with the increase in thickness of $TaSi_2$ thin films. The structure of tantalum silicide thin films are investigated utilizing Fourier Transform Infrared Spectroscopy (FTIR), Energy Dispersion X-ray Analysis (EDAX) and X-ray diffraction (XRD). Due to the absorption of photons in the Si substrate, we cannot get reliable results from FTIR. EDAX results show the composition characteristics of $TaSi_2$ thin films. X-ray diffraction results show changes in the structure of $TaSi_2$ thin film from amorphous to crystalline after annealing. Oxidation characteristics of the $TaSi_2$ films have been investigated in the temperature range of 500°C-900°C in wet steam ambients. The oxidation time ranged from 0.5 to 1.5 hours. No oxide formation of tantalum was observed in the experiment because the surface layer of the mixed Ta-Si oxides prevented the further oxidation of tantalum silicide.

PREPARATION AND PROPERTIES OF TANTALUM SILICIDE FILMS ON SILICON SUBSTRATES

by
Lei Jin

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To my husband and to my parents

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CHAPTER 1

INTRODUCTION

With continuously decreasing device dimensions in silicon integrated circuit technology, the relatively high sheet resistance of polycrystalline silicon as the gate metal has become a limiting factor for device performance. This has led to increased interest to incorporate refractory metal silicides into the device fabrication process. The potential benefits of smaller integrated-circuit dimensions can only be realized if measures are taken to prevent parasitic effects from dominating the electrical characteristics. One of the most urgent needs is to find a low-resistivity substitute for heavily doped polycrystalline silicon (poly-Si) at the gate level. Due to the advantages of ease of formation, low resistivity and thermal stability, $TiSi_2$ and $TaSi_2$ are particularly promising to silicon device technology.

Silicides are most commonly used in DRAM and CMOS logic processes[1-5] as conducting layers that can withstand high temperature processes and have a significantly low sheet resistivity. Besides their role as a stable conductor, silicides have more interesting applications and properties. These include their use as a diffusion source[13] for impurities to generate shallow junctions, or as an alternative to self-aligned silicides[12]. As to the future formation method, a selective CVD process is interesting because of the lack of silicon consumption. Implantation into silicide or even an in-situ

doped silicide deposition are candidates to eliminate implantation damage in the silicon and reduce defects[3].

Among the metal silicides, $TaSi_2$ has higher temperature stability and low contact resistance. The most interesting point of $TaSi_2$ is that it can be directly used as a gate material without the need for poly-Si. Studies on $TaSi_2$ have been published in the literature[6-12]. The present research focuses on the preparation and properties of $TaSi_2$ thin films on n- and p- silicon substrates.

In this work, DC sputtering methods have been utilized to sputter deposited $TaSi_2$ thin films on silicon substrates. It has been found that the sheet resistance changes with film thickness and annealing temperature. With increase in film thickness and annealing temperature, the sheet resistance decreases. $TaSi_2$ thin films with thickness of 1000Å annealed at temperature of 900°C have the sheet resistance of 6-7Ω/□. Utilizing X-ray diffraction methods, the microstructure of $TaSi_2$ thin films have been investigated. $TaSi_2$ thin films were oxidized in the temperature range of 500-900°C in steam ambients, the oxidation time ranging from 0.5 to 1.5 hours. It has been found that the silicide does not oxidize in the experiment at conditions considered in this study. This may be due to the shielding effect of a surface layer of Ta-Si oxides. Further research will be focused on methods to obtain Ta_2O_5 by etching off the surface Ta-Si oxides layer.

In Chapter 2, a brief introduction to the background, properties, applications, formation and oxidation of silicides is presented. The silicides are mainly used as gate, source and

drain material in VLSI fabrication due to their low sheet risistance and high temperature stability. The methods of silicide formation consist of sputtering, evaporation and chemical vapor deposition (CVD).

The methods used to prepare and analyze the properties of $TaSi_2$ thin films and methods used for oxidation are discussed in Chapter 3. DC sputtering methods have been employed to form $TaSi_2$ thin films and wet oxidation methods were used to oxidize these thin films. Their compositional and structural properties have been investigated by using 4-point probe, Fourier Transform Infrared Spectroscopy (FTIR), Energy Dispersion X-ray Analysis (EDX) and X-ray Diffraction (XRD) methods.

In Chapter 4, the experimental procedures utilized in this study such as sputter deposition, annealing and wet oxidation of $TaSi_2$ thin films are presented.

Results of characterization on pre- and post- annealed $TaSi_2$ thin films and wet oxidation of these films are presented and discussed in Chapter 5. The characterization methods include Four-Point Probe, FTIR, EDAX and X-ray diffraction.

Conclusions based on this study are presented in Chapter 6.

CHAPTER 2

SILICIDES AS ELECTRONIC MATERIALS

2.1 Background of Silicides

Metal silicides have attracted scientific curiosity and attention for many decades[3,14-16]. The main reason for this is that some of the silicides have high temperature stability (e.g. $TaSi_2$, $MoSi_2$, WSi_2) and some of them have low resistivity (e.g. $TiSi_2$, $CoSi_2$, $NiSi_2$, $PtSi_2$) [2,3]. They can be used as Schottky barriers and Ohmic contacts in integrated-circuit technology. Recently, interest in silicides has increased considerably because of their potential usefulness as low-resistivity contacts, gate and interconnection metallization in silicon-integrated circuits. The evolution of very large scale integration (VLSI) has necessitated a further study in transition metal silicides, such as their thermodynamic, electrical, and mechanical properties, and their stability at high temperatures.

The rapid development of very large scale integration (VLSI) has resulted in the requirement of smaller and faster devices that will consume less power. The continued evolution of smaller and smaller devices has aroused a renewed interest in the development of new metallization schemes for low-resistivity gates, interconnections, and Ohmic contacts. This is because of the fact that as the device sizes are scaled down, the linewidth gets narrower and the sheet resistance contribution to the RC delay

increases. With sheet resistance of 30 to 60Ω/□, polysilicon is widely used in VLSI technology. Some of the metals are first considered as the direct replacements for polysilicon. Aluminum, tungsten, molybdenum and very recently copper are notable among the metals proposed for gate and interconnect metallization. The use of aluminum, however, requires all post-gate processing of the devices be limited to very low temperatures, preferably below 500°C. The use of refractory metals such as tungsten and molybdenum requires: a) complete passivation of these metals from oxidizing ambient; b) deposition by methods that will not lead to unwanted traps in the gate oxide; c) reliable etching of the metals for pattern generation. Table 2.1 lists the undesirable properties of most metals for application in silicon technology. The uncertainties associated with the stability of these metal films have led to a search for substitute materials.

Silicides have low and metal-like resistivity with value of about one-tenth (or lower) of polysilicon[2] and high temperature stability which makes them the most suitable replacement materials[17-20] for polysilicon. Silicides are also attractive for gate and interconnection metallization for the following reasons: expected higher electromigration resistance, and the possibility of forming silicides directly on polysilicon[17,21], thus preserving the basic polysilicon MOS gate, while decreasing the resistance.

Table 2.1 Properties that make metals unsuitable for VLSI applications[2]

Undesirable Property	Metal
Low eutectic temperature (<800°C)	Au, Pd, Al, Mg
Medium eutectic temperature (800-1100°C)	Ni, Pt, Ag, Cu
High diffusivity in silicon	All
High oxidation rate, poor oxidation stability	Refractory metals, rare earth; Mg, Fe, Cu, Ag
Low melting point	Al, Mg
Interaction with substrate or polysilicon at temperature less than 450°C	Pt, Pd, Rh, V, Mo, Cr
Interaction with substrate or polysilicon at temperature up to 1000°C	All
Interaction with SiO_2	Hf, Zr, Ti, Ta, Nb, V, Mg, Al
Poor chemical stability, especially in HF containing solution	Refractory metals, Fe, Co, Ni, Cu, Mg, Al
Poor etchability	Pt, Pd, Ni, Co, Au
Electromigration problems	Al
Contact spiking due to interdiffusion	Al

2.2 Properties of Silicides

With continuously decreasing device dimensions, the relatively high sheet resistance of polycrystalline silicon has become a limiting factor for device performance. This has led to increased interest in refractory metal silicides for their use as contacts and interconnects in microelectronic devices. Common silicide choices are $TiSi_2$, $TaSi_2$, $MoSi_2$ and WSi_2. Table 2.2 summarizes the basic properties of some common silicides. These silicides are attractive because of their low contact resistance at the source, drain and gate regions of silicon-based MOS transistor.

Table 2.2 Basic properties of most common silicides[3]

Silicide	Lowest eutectic Temperature (°C)	Silicide Formation	Sintering Temperature (°C)	Resistivity (μΩ-cm)
$TiSi_2$	1330	Metal on poly Si	900	13-16
$TaSi_2$	1385	Cosputtering	1000	50-55
$MoSi_2$	1410	Cosputtering	1000	-100
WSi_2	1440	Cosputtering	1000	-70
$CoSi_2$	1195	Metal on Poly Si	900	18-20
$NiSi_2$	966	Metal on Poly Si	900	-50
PtSi	830	Metal on Poly Si	600-800	18-35

- **Resistivity**

The resistivity of silicides is the most important criterion in considering them for metallization in integrated circuits. The resistivity of some common silicides is listed in Table 2.2. Resistivity of silicides increases with the increasing number of d-electrons (e.g., two electrons for Ti to four electrons for Cr). The relative change in the resistivities of silicides of group IVA metals to those of group VIA metals decreases as one moves from the elements of the fourth period in the periodic table to those of the sixth period. This behavior can be attributed to the increasing size of the metal atoms such that outer electrons are relatively less affected by the rest of the atom core. All silicides behave like metals, i.e., resistance increases with increasing temperature, i.e., conductivity increases with decreasing temperature. The temperature dependence of the sheet resistance of some metals on polysilicon is shown in Fig 2.1[2]. Different metals show different behavior.[8,22] The change in resistivity also depends on the microstructure of silicides. Under certain temperature, the amorphous microstructure of silicides will become crystallized, which results in the decrease of sheet resistance. The grains of silicides become more and more orderly during the microstructure change leading to the decrease in sheet resistance.

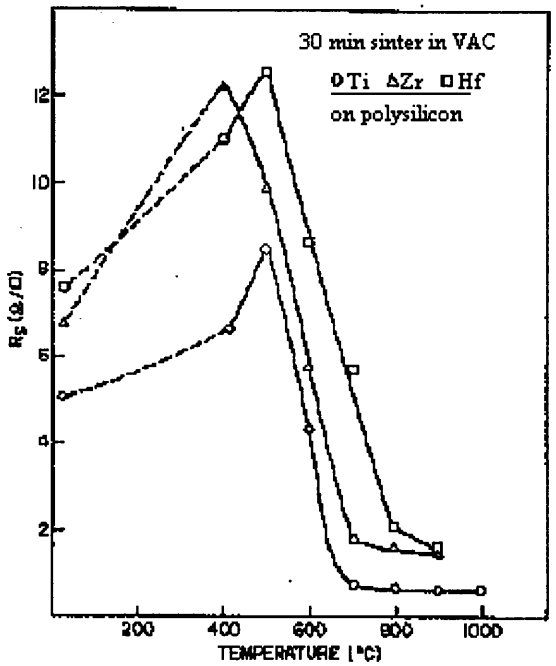


Fig 2.1 Sheet resistance(R_s) as a function of sintering temperature (starting metal film thicknesses are Ti-1000Å, Zr-1100 Å, and Hf 1150 Å)[2].

- **Shallow silicide contacts**

The most important point of scaling down the size of the device is the reduction of junction depths, which will result in some contact problems.[2] Shallow junctions limit the use of aluminum due to its known penetration in silicon. Forming silicides in the contact windows by reaction between the silicon substrate and a thin metal layer offers a possibility of obtaining contacts with lower contact resistances. The possibility of using deposited silicides directly into contact windows offers the advantage of preserving shallow junctions, which may be penetrated by a conventional silicide.

The increase in device complexity and the increased device density per unit area requires reductions in both the lateral and vertical dimensions of the junctions. The source and drain regions shown in Fig 2.2 are formed by diffusing dopants of opposite polarity in the substrate, thus creating the desired p-n or n-p junction. Such a junction forms a basic building block of MOS or bipolar devices.

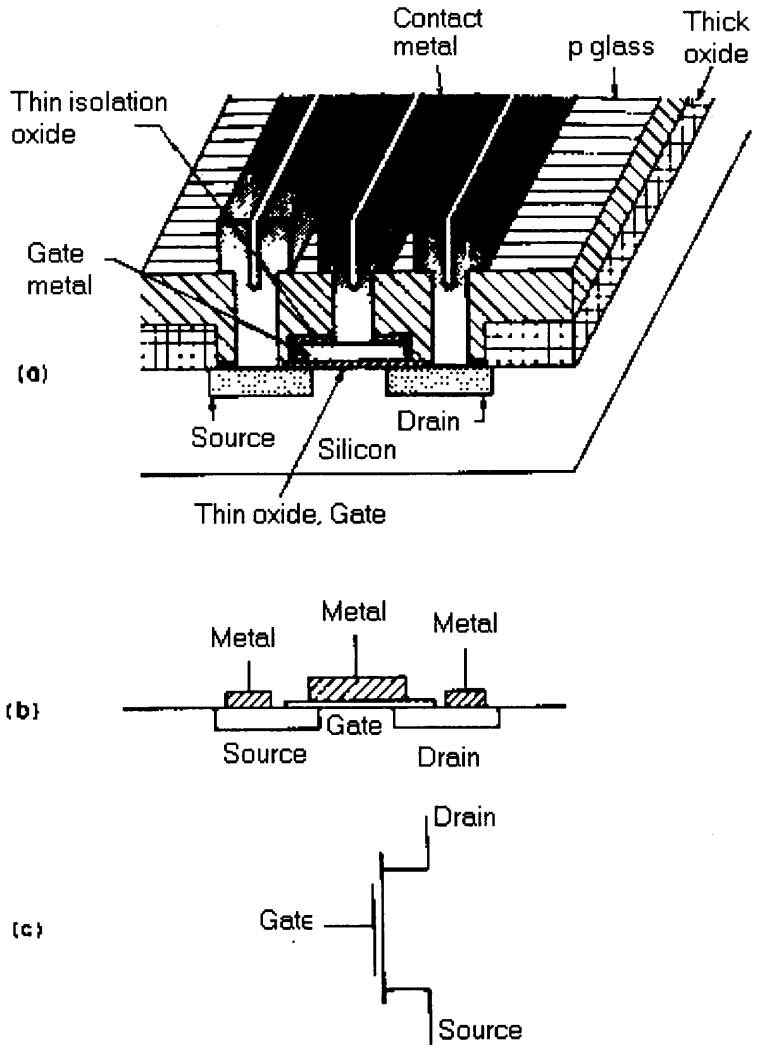


Fig 2.2 A typical MOS device structure a) cross section b) a simple schematic representation c) a designer's symbolic representation

Fig 2.3 shows a schematic of a p-n junction on an expanded scale. The junction depth X_j, is of the order of contact dimensions that are also shallow. These shallow contacts, however, must not lead to spiking shorts, which are observed with aluminum contacts, or to contact depths that are any significant fraction of the junction depth.

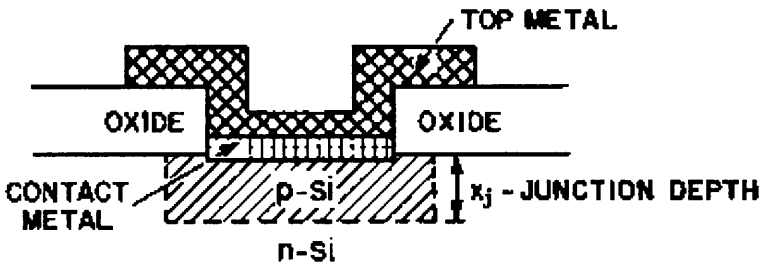


Fig 2.3 Cross section of a p-n junction where a silicide contact is desirable. For shallow junctions, the X_j, which is the junction depth, is less then 2000Å

Besides the desired low resistivity, the usefulness of the silicide metallization scheme depends on the ease with which the silicides can be formed and patterned and on the stability of the silicides throughout the device-processing and during actual device usage. The desired properties of a silicide for use in integrated circuits are the following[2]:

1. Low resistivity
2. Easy to form
3. Easy to etch for pattern generation
4. Should be stable in oxidizing ambients; oxidizable
5. Mechanical stability; good adherence, low stress
6. Surface smoothness
7. Stability throughout processing, including high-temperature sinter, dry or wet oxidation, phosphorus glass (or any other material) passivation, metallization

8. No reaction with final metal, aluminum
9. Should not contaminate devices, wafers, or working apparatus
10. Good device characteristics and lifetimes
11. For window contacts—low contact resistance, minimal junction penetration

Silicides used to produce gates and interconnections must satisfy all these requirements but all silicides do not have these characteristics. Silicides used for contacts, however, do not have to meet all the requirements, since the contacts are formed towards the end of the processing.

Of all the silicides, studies are focused on the silicides of groups IVA, VA, and VIA, which are called the refractory metal silicides. These refractory metal silicides are suitable for gate metallization. Among the refractory metal silicides, $TiSi_2$ and $TaSi_2$ are particularly promising, since these silicides have the lowest resistivity with good thermal stability.[21,23]

2.3 Application of Silicides

The most common application of silicides is their use in DRAM and CMOS logic devices.

- **Silicides in DRAMS**

The increasing complexity of dynamic memories is still the driving force for the rapid progress in CMOS technology development. Every three years, the number of bits in

DRAMs increases by a factor of four.[3] Today the 64 Mbit DRAM is in mass production.[24] Fig 2.4 shows a schematic of one transistor DRAM cell consisting of a capacitor and an adjacent select transistor. These cells are arranged in an array configuration with word lines connecting the gates and bit lines connecting the drains of the select transistors. The resistances of long word and bit lines limit the memory access time by excessive RC delays.

Silicides are used in DRAM technologies since the introduction of the 256 kbit generation. The main stream in DRAM technologies is the application of cosputtered silicides as bit line. In the 64 Mbit generation, both poly silicon or polycide word line are used. Polycide is one of the approaches that combines the advantages of a polysilicon gate with that of the silicides. This leads to a reduction in the sheet resistance by the use of a refractory metal silicide on top of the polysilicon gate. This approach preserves the polysilicon-SiO_2 interface while lowering the overall sheet resistance to about 1 to 3Ω/□. The most common types of silicides used for this application are $MoSi_2$, WSi_2, $TaSi_2$ and $TiSi_2$.

With the increasing speed of microprocessors, the access time of DRAMs limits the system performance. Therefore, the access time becomes a major issue. Future DRAMs with high performance will require minimized word and bit line resistivites. The bit line resistivity can be reduced by replacing the polycide by a metal layer like W, and a further reduction of the word line resistivity can be achieved by low resistive silicides like $TaSi_2$ and $TiSi_2$ for the gate polycide.[8,12,25]

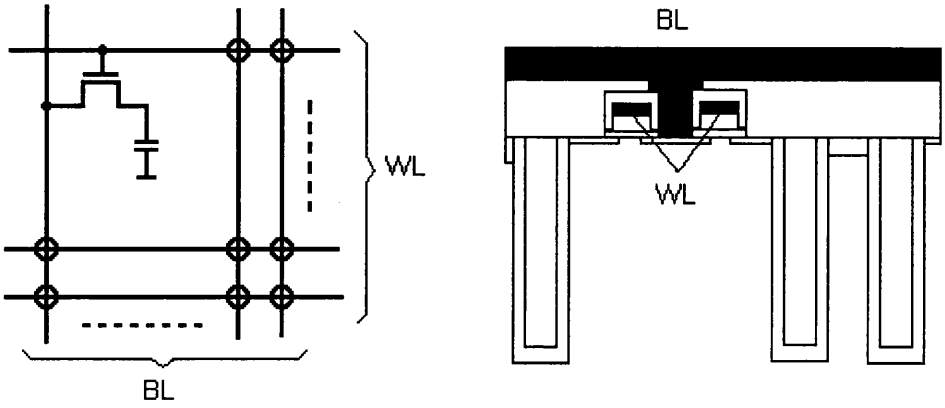


Fig 2.4 Schematic view of DRAM cell array with word lines (WL), bit lines (BL), and a trench capacitor cell[3].

- **Silicides in state of the art logic**

In CMOS logic, basically two different concepts are observed. In the first approach, the polycide gates are used to reduce the gate resistivity. The gate polycides can then be used for short range interconnects and this increases the design flexibility, which is an important issue in random logic. The low resistive silicide lies on top of a polysilicon layer and forms polycide gates. Usually the silicide is not in contact with the gate oxide. It has been shown that the silicides, e.g. $TaSi_2$, can be directly used as a gate material without a polysilicon. Compared to a polycide gate, the sheet resistance of a silicide for a given total layer thickness is lower (equal to the silicide value).

The second approach found in CMOS logic is the selective silicidation of gates and source/drain resulting in polycide gates and low-resistive diffusions that allow for flexible contacts even for wide transistors. Reducing the series resistance of the source/drain regions is an important factor in the design of smaller transistors. As channel

conductance increases with shorter channel lengths, the resistance of the shallow source/drain region stays fixed or actually increases because of the need for shallower junctions. The result is that the resistance of the source/drain limits the current-delivering capability of short-channel devices. The resistance of the source/drain can be substantially reduced by using a refractory metal silicide in the source/drain region similar to the way it was used to reduce the polysilicon resistivity. The effect of this approach on the device characteristics can be seen in Fig 2.5, in which the Current-Voltage (I-V) characteristics are shown for device structures specially designed to emphasize the source/drain resistance.[27] The results of silicidation can be clearly seen in the current characteristics, showing a substantial increase in drive for the silicided device.

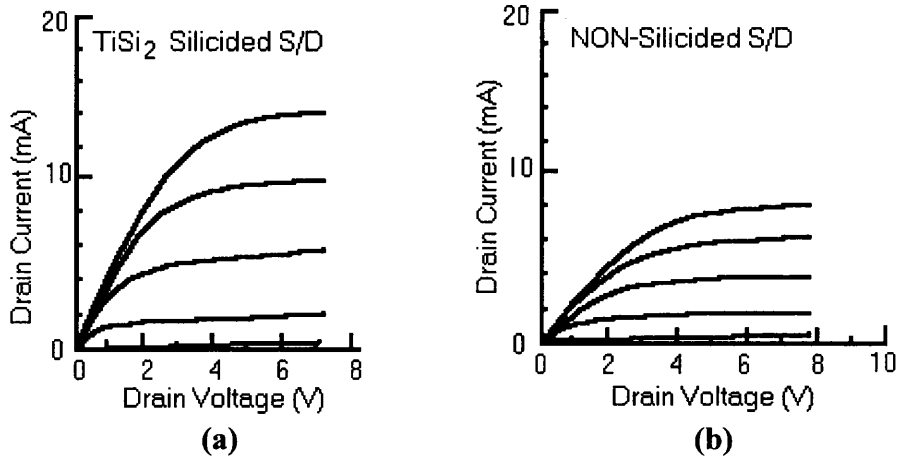


Fig 2.5 a) I-V characteristics of MOSFET with $TiSi_2$ source/drain b) I-V characteristics without silicided S/D[27].

2.4 Preparation of Silicides

Slilicide films can be obtained by sputtering, evaporation, and CVD techniques.[38-40]

- **Evaporation**

In evaporation method, a film is deposited by the condensation of the vapor on a substrate, which is maintained at a lower temperature than that of the vapor. All metals vaporize when heated to sufficiently high temperatures. Several methods, such as resistive, inductive (or radio frequency, RF), electron bombardment, or laser heating, can be used to attain these temperatures. For transition metals, especially the refractory metals, evaporation using an electron gun (e-gun) is very common. For co-depositing silicides, two evaporation sources using metal and silicon charges are used. The evaporation rate of the metal and silicon is determined under various conditions. Subsequently, suitable process conditions are adopted to deposit an alloy in the desired silicon to metal ratio.

However, resistive heating is limited in application because of the lower throughput associated with the smaller metal charge generally used in such systems. On the other hand, e-gun evaporations cause radiation damage, but high-temperature sintering required for silicide formation anneals out the radiation damage. This method is advantageous because the evaporations take place at pressures considerably lower than that of sputtering pressures and, therefore, the gas entrapment in the film is negligible or

nonexistent. Radio frequency heating of the evaporating source in an appropriate crucible could prove to be the best compromise in providing large throughput, clean environment, and minimal levels of radiation damage.

- **Sputtering**

In sputter deposition, the target material is bombarded by the energetic ions to let loose some atoms. These atoms are then condensed on the substrate to form a film. Sputtering processes are very well controlled and are generally applicable to all materials such as metals, alloys, semiconductors, and insulators. Both Radio Frequency (RF) and DC-magnetron sputtering can be used for silicide formation. One limitation of DC-magnetron sputtering, however, is that it requires the target material to be a conductor. Therefore, for cosputtering (simultaneous sputtering from two targets) using the metal and silicon elemental targets, a silicon target must contain a dopant to make it a reasonably good conductor. The use of doped targets leads to incorporation of the dopants in the silicide film. Another limitation in DC-magnetron sputtering is that backsputter etching cannot be used to remove the surface layers from the substrates prior to deposition. Deposition of silicide films by sputtering from a composite target has the advantage of producing high quality films with high throughput. It has been extensively used in silicide and polycide gates in very large scale integration processing. The reason for this is that high quality films can be obtained with high throughput.

Sputtering is carried out at relatively higher pressures (1 to $10x10^{-3}$ Torr range). Because gas ions are the bombarding species, the films usually end up including small amounts of

the gas. These gases are nonreactive except when sputtering gas is contaminated with chemically active gases.

- **Chemical Vapor Deposition (CVD)**

In CVD technique, the formation of a solid film on a substrate is produced by the reaction in the vapor-phase chemicals (reactants) that contain the required constituents. The reactant gases are introduced into a reaction chamber and are decomposed and/or reacted at a heated surface to form the thin film. Generally, the reaction is induced by heat, which causes either a decomposition (pyrolysis) of the vapor or a reaction between different gaseous species in the ambient. Note that in CVD, the reactant gases do not react with (and therefore do not consume) any substrate surface material. Such decompositions are limited only by the availability of the reactants that are in the gas phase or that will easily vaporize. The reactants must decompose or react to produce the desired film at usable temperatures. The process is usable as long as the temperatures are low enough so that they do not affect the characteristics of the processed substrates (devices). The depositions, especially those carried out at sub-atmospheric pressures, have the advantages of large throughput and good step coverage.

Most transition metals or their silicides are difficult to deposit using CVD because of the nonavailability of compounds that can be used as the metal source and the high temperatures required to produce the deposits. However, the advantages of large throughput and good step coverage are so attractive that attempts are being made in various laboratories to find ways to deposit silicides using CVD.

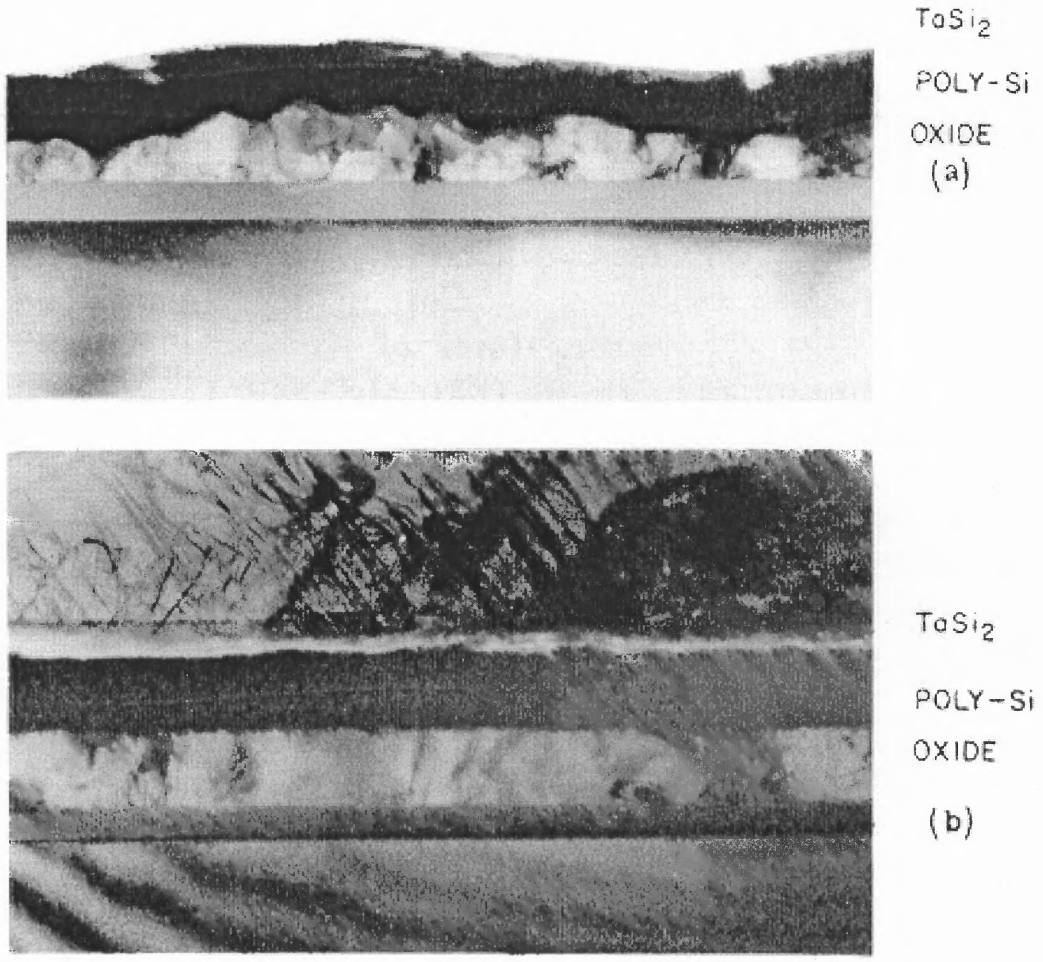


Fig 2.6 TEM cross sections of tantalum disilicide on polysilicon structures formed by a) metal on polysilicon and b) cosputtered film on polysilicon[2].

A comparison of the several processing techniques leads to the conclusion that cosputtering of the metal and silicon from two different elemental targets is by far the best choice. The most attractive feature of cosputtering is its ability to control the metal-to-silicon ratio in the deposit. In Fig 2.6, the roughness of the cosputtered silicides is compared with those formed by reacting metal with polysilicon substrate. The TEM cross-sections of the reacted and cosputtered silicide films show the roughness both at the

surface and at the silicide-polysilicon interface. These cross-sections confirm that cosputtered silicide is smoother even at the silicide-silicon interface.

2.5 Oxidation of Silicides

Besides the property of resistivity, silicides oxidize as well, making silicides analogous to polysilicon. Often during VLSI processing, an insulating layer must be formed on the top surface of the polycide structure to isolate it from subsequently deposited layers. The polysilicon gate has been successful because the oxidation of polysilicon leads to insulating layers. Similar insulating layers can be grown on most silicides. The oxide formed must be stable and exhibit adequate electrical and physical properties.

Bartur and Nicolet[43] have compiled data on the oxidation kinetics of various silicides from published reports, and their findings are summarized in Table 2.3. The linear part of the linear parabolic law is given by: $d_0=B/A(t+\tau)$[1] (where d_0 is the oxidation thickness, t is oxidation time, τ represents a shift in the time coordinate to account for the presence of the initial oxide layer d_i and B/A is the linear rate constant). The variation in oxidation rates of silicides is due to different linear rate constants (B/A)[44]. Silicides in which the metal is the moving species oxidize more rapidly than silicon, and only parabolic growth is observed. Silicides in which silicon is the moving species are usually formed at high temperatures, and the limited Si diffusion may impede the oxidation, therefore reducing the B/A term.

Table 2.3 Data on the oxidation kinetics of various silicides [43]

Silicide Film	Substrate	Kinetics x=thickness t=time	Condition	Rate constants at 1000 °C Linear rate[1] B/A(cm/s)	Parabolic rate[1] B(cm^2/s)	Activation energy (eV) B/A	B
Si	Si<?>	$x^2+Ax = B(t+\tau)$	wet	$3.5x10^{-8}$	$8.0x10^{-13}$	1.96	0.71
		$x^2+Ax = B(t+\tau)$	dry	$2.0x10^{-9}$	$3.3x10^{-14}$	1.99	1.24
$TiSi_2$	Si<?>	$x^2+Ax = B(t+\tau)$	wet	$5.6x10^{-8}$	$6.4x10^{-13}$	2.00	1.39
$TiSi_2$	Si<poly>	$x^2+Ax = Bt$	wet	$6.6x10^{-8}$	$6.4x10^{-13}$	2.10	1.51
$MoSi_2$	SiO_2	$x^2+Ax = B(t+\tau)$	dry	$2.8x10^{-9}$	$1.9x10^{-14}$	1.90	1.60
$MoSi_2$	Si<?>	$x^2+Ax = B(t+\tau)$	wet	$1.2x10^{-7}$	$1.0x10^{-12}$	0.84	1.10
$TaSi_2$	Si<poly>	$x^2 = Bt$	wet		$1.4x10^{-13}$		1.40
	Si<poly>						
	Si<100>	$x^2 = Bt$	dry		$2.8x10^{-14}$		1.20
	Si<111>						
$TaSi_2$	Si<?>	$x^2+Ax = Bt$	wet	$8.2x10^{-8}$	$1.0x10^{-12}$	0.93	1.10
WSi_2	Si<poly>	$x^{1.82} = B^*t$	wet	$B^*=4.4x10^{-12a}$			1.00
	SiO_2	$x^{1.82} = B^*t$	wet	$B^*=6.9x10^{-12a}$			0.40
WSi_2	Si<?>	$x^2+Ax = Bt$	wet	$1.3x10^{-7}$	$6.8x10^{-13}$	1.0	1.30

2.6 Importance of Tantalum Silicide

As junctions in semiconductor devices are scaled down to a quarter micron, high contact resistance becomes a serious problem in a reliable device[11]. As a result, thermally and chemically stable materials, such as refractory metal silicides become necessary for replacing polysilicon.

Among the refractory metal silicides, $TiSi_2$ and $TaSi_2$ are particularly promising. Some studies has been done on $TaSi_2$ in the literature[6,8-12]. $TaSi_2$ is interesting to scientists because of its higher temperature stability and low contact resistance. From Table 2.1, we can see that the $TaSi_2$ temperature stability is better than that of $TiSi_2$[3]. According to Hyun-Choon Cho[8], the contact resistance of $TaSi_2$ /Si(p+) is much lower than that of $TiSi_2$/Si(p+) even though the sheet resistance of $TaSi_2$ layer is higher than that of the $TiSi_2$ layer. Fig. 2.7 shows the results of the measured contact resistance of $TiSi_2$/Si(p+) and $TaSi_2$/Si(p+) structures. Fig. 2.8 shows the results of sheet resistance of $TiSi_2$/Si(p+) and $TaSi_2$/Si(p+) structures.

It is also shown in Cho's work[8] and Mahmood's work[21] that sheet resistance decreases with increasing annealing temperature for $TaSi_2$/Si samples (See Fig.2.8 a). This reduction was primarily proportional to the extent of crystallization of the silicide layer as determined by X-ray diffraction results[8]. In Fig. 2.8, for $TaSi_2$/Si(p+) sample, when the annealing temperature is above 1000°C, the sheet resistance does not change significantly with increase in annealing temperature. It is shown that, around 1000°C, the silicide layer is crystallized and attains its final phase. In this work, the resistance of 500Å $TaSi_2$ film at its final phase is about 5Ω/□. According to Ivanov's work [41], annealing at 1273K resulted in crystallization of the film with the formation of $TaSi_2$.

DRAM and logic processes use polycide gates (the low resistive silicide lies on top of a polysilicon layer). Usually the silicide is not in contact with the gate oxide. It has been

shown that $TaSi_2$ can be directly used as a gate material without a polysilicon. The main advantage of a silicide gate is that its work function lies approximately in the middle of the band gap. It therefore combines the advantages of n^+ and p^+ doped polysilicon gates without the necessity of an individual doping process[26].

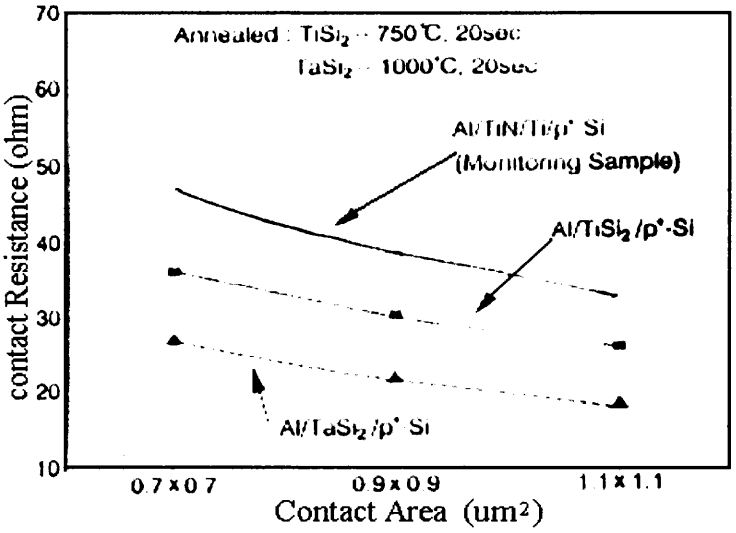


Fig 2.7 Contact resistance of $TaSi_2$/Si(p+), $TiSi_2$/Si(p+) and TiN monitoring samples for three contact sizes.

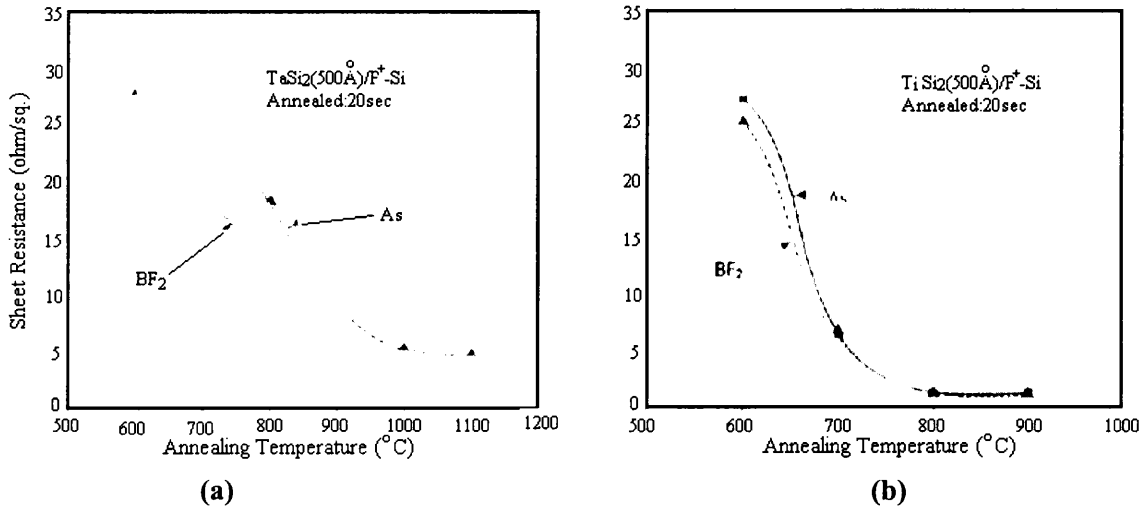


Fig 2.8 Changes in sheet resistance of $TaSi_2$ and $TiSi_2$ as a function of annealing temperature

2.7 Compositions of Tantalum Silicide

Apart from $TaSi_2$, there are other tantalum silicide compositions as Ta_2Si and Ta_5Si_3. The crystallographic structures of all these compositions are different. Analyzed with X-ray diffraction method, the positions of diffraction angles(2θ) also vary for different compositions. Table 2.4 lists the crystallographic structures, lattice parameters, and densities of the various tantalum-silicides. The X-ray diffraction spectra of various compositions are shown in Fig.2.9[11].

Table 2.4 Crystallographic structures and densities of tantalum-silicides[2]

			Lattice parameter (Å)		Density
Silicide	Structure*	Type	a	c	g/cm^3
Ta_2Si	T	Al_2Cu	6.157	5.039	13.544
Ta_5Si_3	T	W_5Si_3	9.88	5.06	13.401
$TaSi_2$	H	$CrSi_2$	4.7821	6.5695	9.08

*T, tetragonal; H, hexagonal.

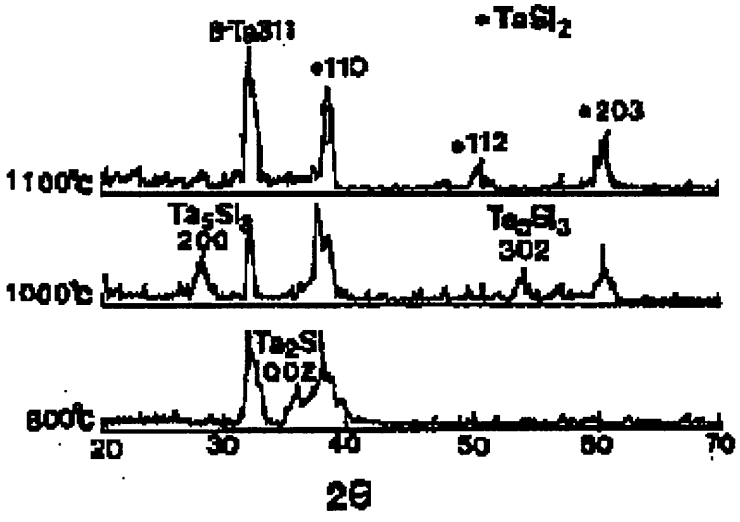


Fig 2.9 X-ray diffraction spectra of tantalum silicide for various compositions [11].

Several factors influence the intermetallic compound formation, for example, the atomic diffusivities in various phases, concentration gradients, temperature, free-energy considerations, and impurities. The kinetics of the metal-silicon interaction also strongly depend on the nature of the metal film (its thickness, grain size, purity, and defects), substrate preparation, interfacial oxide thickness, and film deposition parameters (such as energy, temperature, and ambient pressure).

In Ivanov's work[41], under certain conditions of reactive sputter deposition, $TaSi_x$ with various compositions (x=0.1-0.6) are formed. The structures of these compositions are also different as can be seen from the X-ray diffraction spectra shown in Fig 2.10.

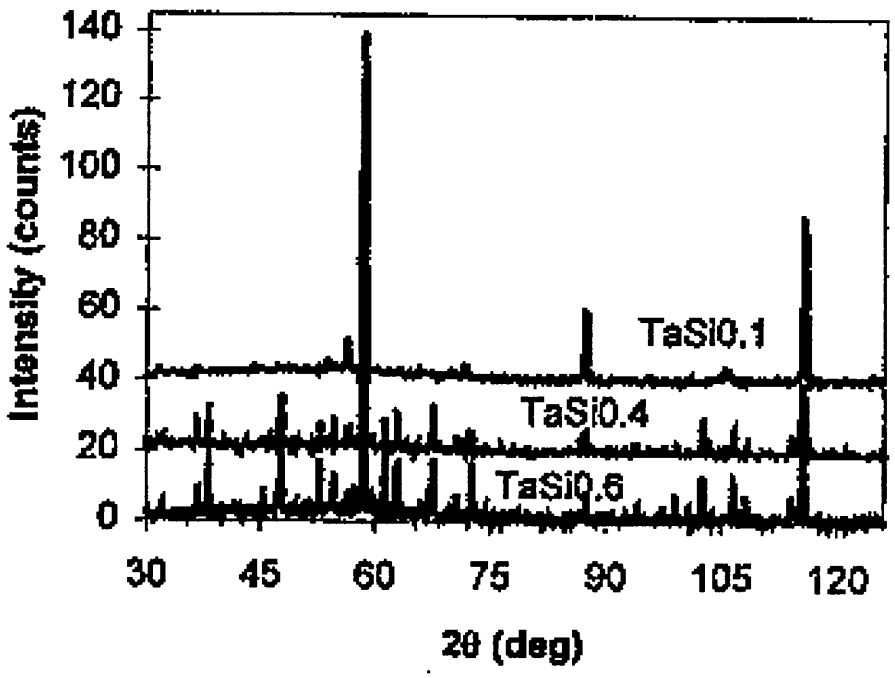


Fig. 2.10 X-ray diffraction spectra of $TaSi_x$ (x=0.1-0.6) [41].

CHAPTER 3

PROCESS AND ANALYSIS METHODS

3.1 Processing Methodologies

3.1.1 Sputtering and Annealing Techniques

Sputtering has been widely used as a metallization technique in VLSI processing[28-30]. The schematic of a sputter deposition system is shown in Fig 3.1. Sputtering is a physical phenomenon involving the acceleration of ions, usually Ar^+, through a potential gradient, and the bombardment of a "target" or cathode by these ions. Through momentum transfer, atoms near the surface of the target material become volatile and are transported as vapors to the substrates. At the substrates, the film accumulates through deposition. Conventional sputtering has found a large number of applications in IC processing. A high electron density is required in the discharge to increase the ion current density at the target surface and thus prevent oxide formation. The high electron density may be achieved by introducing an auxiliary discharge, as in triode sputtering, or through the use of magnetic fields to capture the electrons and increase their ionizing efficiency, as is done in magnetron sputtering.

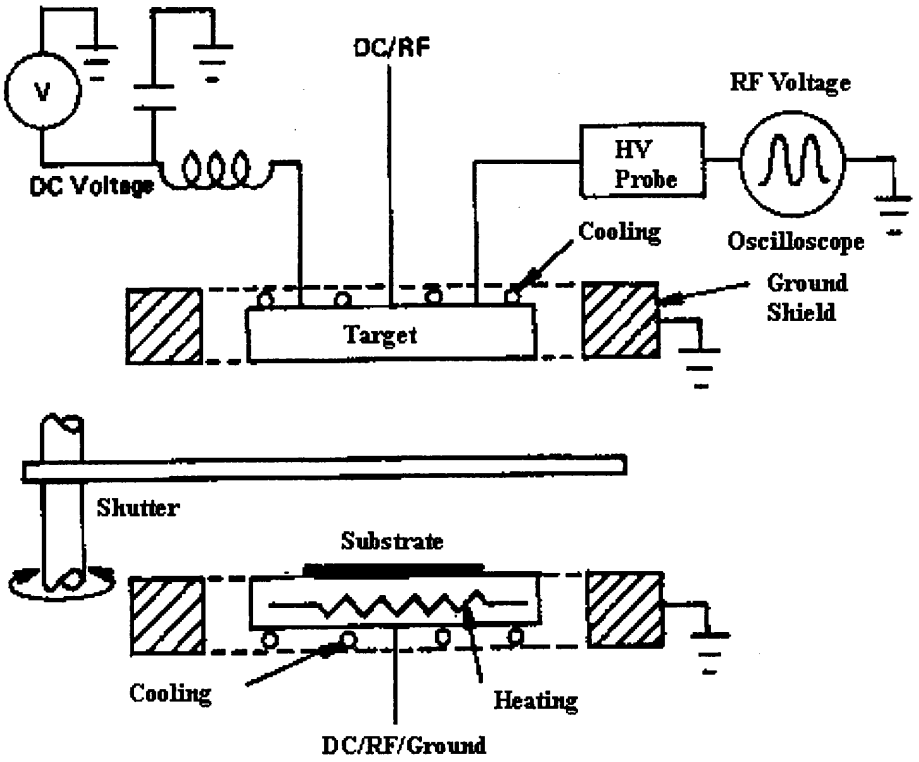


Fig 3.1 Schematic of a sputtered deposition system showing ground shields, shutter, electrode, cooling and heating, rf and dc voltage measurement

In magnetron sputtering process, ideally, electrons do not even reach the anode but are trapped near the target, enhancing the ionizing efficiency there. This is accomplished by placing a magnetic field oriented parallel to the target and perpendicular to the electric field.

Consider the motion of a charged particle (e.g. an electron or an Ar ion) having mass m, velocity v and charge q. Assume the electron to be moving perpendicular to a uniform magnetic field B. The addition of the electric field e on the target changes the orbits of electron from circular to cycloidal with r = mv/Bq. Its instantaneous radius of curvature,

r, will decrease as it travels further from the target surface. Thus the electron will be trapped near the surface from which it was emitted.

Magnetrons have proved to be very useful addition to the sputtering devices[31]. The primary advantages are:

1. high deposition rate (which is grater than one micron per minute);
2. virtual elimination of bombardment of the substrate by fast charged particles;
3. high-purity of the deposited films;
4. good adhesion of films to substrate;
5. ability to coat heat sensitive substrates;
6. excellent uniformity on large-area substrates.

Due to the above advantages, magnetron sputtering has become a powerful technique used in a wide range of applications.

The process of annealing of metallic films is usually performed in a furnace with forming gas or N_2 ambient. The annealing of continuous amorphous layers that extend to the Si surface can cause amorphous layers to become crystallized[8,11, 42]. As to the $TaSi_2$ layer, the sheet resistance of the film decreases with increasing annealing temperature, and is nearly independent of annealing times[11]. The reduction in thermal budget after ion implantation is particularly important for forming shallow junction, which is one of the most important requirements to realize scaled devices with short channel effects. So far, many attempts have been made to achieve ultra-shallow junctions by rapid thermal

annealing (RTA)[7] at high temperatures. Using such techniques, it is possible to form shallow junctions with low reverse-bias currents.

3.1.2 Oxidation Techniques

The oxidation technique chosen depends upon the thickness and desired oxide properties. Oxides that are relatively thin and those that require low charge at the interface are typically grown in dry oxygen. When sodium ion contamination is of concern, HCl-O_2 is the preferred technique. Where thick oxides are desired, steam is used. Higher pressure allows thick oxide growth to be achieved at moderate temperatures in reasonable amounts of time.

One-atmosphere oxide growth, the most commonly used technique, is typically carried out in a horizontal diffusion tube, although vertical diffusion furnaces are being used more frequently. In the case of the horizontal furnace, the wafers are held vertically in a boat, which is normally loaded using cassette-to-cassette equipment. Typical oxidation temperatures range from 700 to 1200°C and should be held to within $\pm$ 1°C to ensure uniformity. In a standard procedure, the wafers are chemically cleaned, dried, loaded onto the boat, and automatically inserted into the furnace, which is then ramped up to oxidation temperature. Ramping is used to prevent wafer warpage. Following oxidation, the furnace is ramped down and the wafers are removed.

Eliminating particles during oxidation is necessary to grow high-quality, reproducible oxides. In earlier procedures, the boat rested directly on the tube during insertion and

withdrawal, or an integrated roller boat design was used. In either case, particulates were generated. Innovative designs now use a cantilevered arrangement or a soft contact system in which the boat is inserted into the oxidation tube in a contactless manner and then lowered onto the tube. It is removed by reversing the steps.

A major new development in oxidation equipment is vertical diffusion furnaces, which have the processing tube in the vertical position. The wafers can be loaded from either the top or bottom, depending on the system, and are horizontal during oxidation, facing either up or down. In certain systems, the wafers can be rotated to provide better uniformity. The claim of these systems is that they provide excellent thickness uniformity and low particle density. The quoted temperature uniformities range from $\pm$ 0.25°C to $\pm$1.0°C along the flat zone with oxide uniformity in the $\pm$1% range[1]. In some systems, the heating element can be moved relative to the wafers, allowing rapid cooldown of wafers in and around most of the periphery.

Dry oxidation or HCl assisted dry oxidation is straightforward, using microprocessor-controlled equipment. The desired insertion and withdrawal rates, ramp rates, gas flows, and temperatures are all programmable. Wet oxidation can be carried out conveniently by the pyrogenic technique in which H_2 and O_2 react to form water vapor. A microprocessor controls the H_2/O_2 mixture. The pyrogenic technique assures high-purity steam, provided that high-purity gases are used. If wet oxidation by the bubbler technique is used, a carrier gas is typically flowed through a water bubbler maintained at a temperature of

95°C. This temperature corresponds to a water vapor pressure of approximately 640 Torr. In this research, wet oxidation technique was used.

3.2 Analysis Techniques

3.2.1 Four-Point Probe Technique

Four-Point Probe technique is used to measure the sheet resistance R_s (also often called the sheet resistivity) of a diffused layer[28,32]. Fig 3.2 shows the co-linear probe arrangement used for measuring R_s. The value of R_s is expressed in units of Ω/sq, and is related to the average resistivity ρ of a diffused layer by:

$$R_s\ (\Omega/sq\ ) = \rho\ (ohm\text{-}cm)/X_j\ (cm)$$

$$R_s = 2\pi sF(V/I)$$

Where, I is the current flowing in the outer two probes; V is the voltage drop measured across the two inner probes. When all of the probes are equally spaced, in addition to V and I, the resistivity is determined by s, the probe spacing, and F, a correction factor (which arises from the fact that the sample is not semi-infinite, but has a finite thickness and diameter).

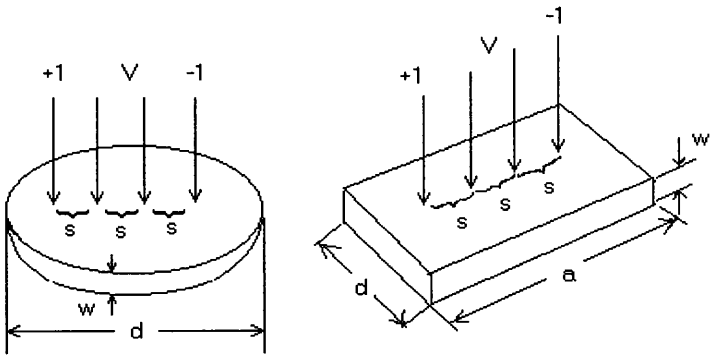


Fig 3.2 Co-linear four-point probe arrangement for the measurement of resistivity

The sheet resistance measurement is first performed with the current in the forward direction, and then in the reverse direction (in order to minimize errors due to thermoelectric heating and cooling effects). The two (V/I) readings are averaged. The measurements should also be made at several current levels, until the proper level is found. That is, if the current is too low, the values of the forward and reverse readings will be different. If it is too high, I^2R heating will cause the measured reading to drift with time. The amount of pressure applied to the probes during measurement is also important, since excessive pressure can drive the probes past the junction, while too little pressure results in poor electrical contact to the sample.

3.2.2 Fourier Transform Infrared Spectroscopy (FTIR)

FTIR is the preferred method for infrared detection of chromatographically separated species[37]. The popularity of FTIR is primarily due to the multiplex and rapid scanning features of interferometry. The interferometer was developed by Albert A.Michelson. Interferometers used in FTIR instruments today are similar in design to the one built by Michelson as shown in Fig3.3(a). Interferometry produces a complex waveform that is a sum of contributions from all wavelengths emitted by the source. Wavelength discriminations are modulated at different frequencies. In contrast, a diffraction grating disperses source radiation and each wavelength occupies a different position in space as shown in Fig3.3 (b).

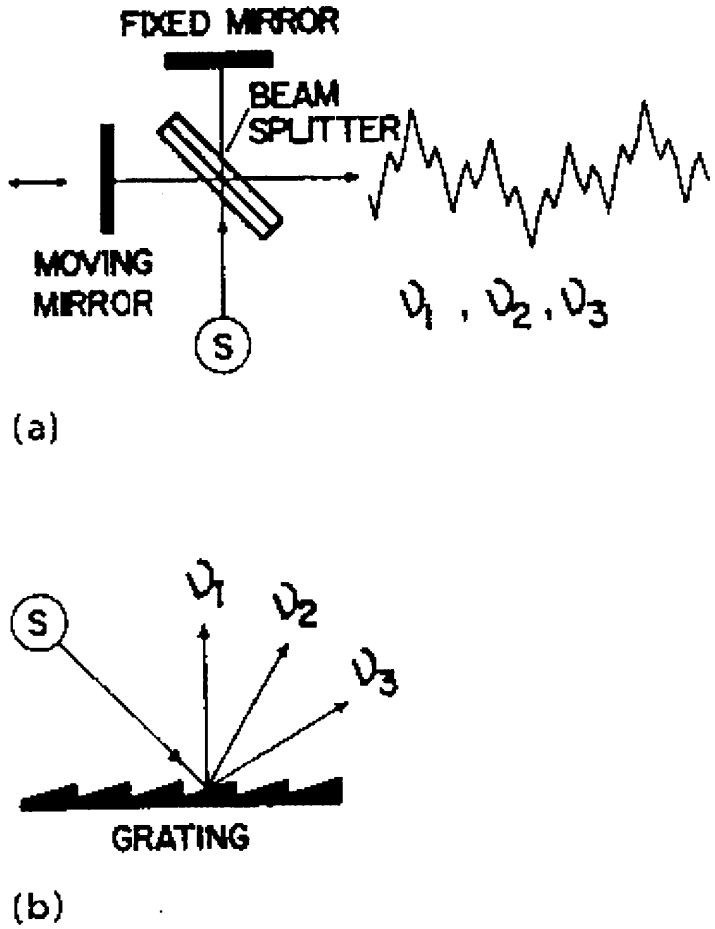


Fig 3.3 a) Schematic of an interferometer b) Wavelength dispersion by diffraction grating

When infrared radiation interacts with matter, it can be absorbed causing the chemical bonds in the material to vibrate. The presence of chemical bonds in a material is a necessary condition for the infrared absorption to occur. There is a relation between the wavenumbers at which a molecule absorbs infrared radiation and its structure. The correlation allows the structure of unknown molecules to be identified from the infrared spectrum of the molecule. A typical FTIR spectrum is shown in Fig 3.4.

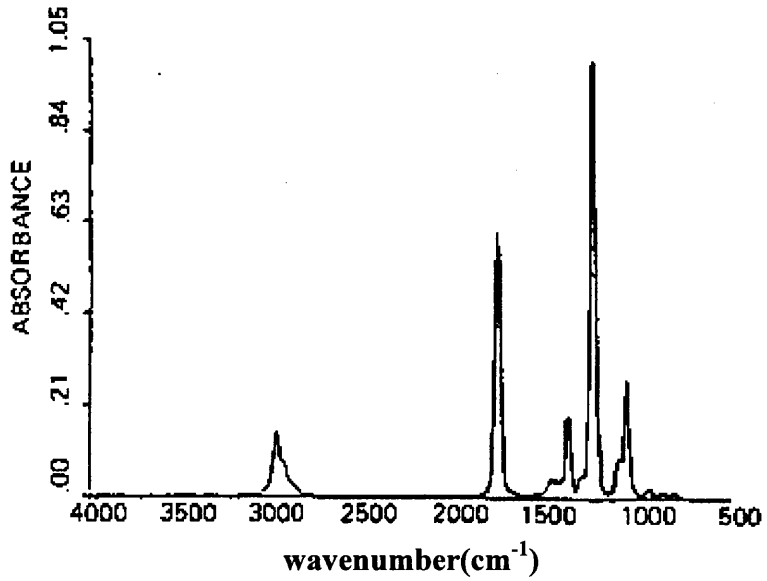


Fig3.4 Phase infrared absorption spectra of ethyl acetate

Transmission and reflection techniques are two main infrared techniques available.

3.2.3 Energy Dispersion X-ray analysis (EDAX)

Energy Dispersion X-ray analysis is a useful technique in the fields of X-ray fluorescence, electron microprobe analysis, scanning electron microscopy (SEM), and transmission electron microscopy (TEM). It always has the advantage of speed of analysis because of its ability to analyze all elements at once and its high detection efficiency.[36]

The components of an energy dispersion X-ray analysis system is illustrated in Fig 3.5.

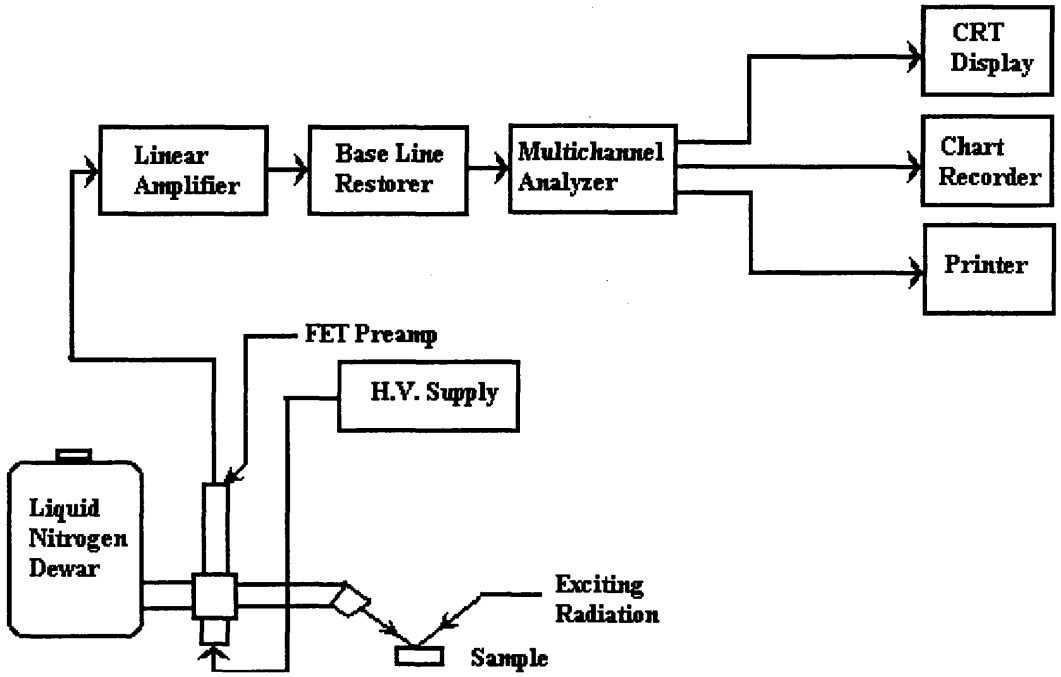


Fig 3.5 Diagram of energy dispersive X-ray analysis (EDAX) system

The first three segments of the system are important, and even more important is their integration. These are the detector, the field-effect transistor (FET) preamplifier, and their cryogenic enclosure. The enclosure must be designed to cool the detector and the FET to their individual optimum temperature in order to damp any significant microphonic noise and to present the detector to the X-rays to be detected. The detector is a lithium drifted silicon diode. It must have very low leakage current ($>10^{-12}$A) and low capacitance. An incoming X-ray generates a photoelectron that eventually dissipates its energy by creating electron-hole pairs. The incident photon energy is linearly proportional to the number of pairs produced or equivalently proportional to the amplitude of the voltage pulse they generate when separated. The pulses are amplified and then sorted according

to voltage amplitude by a multi-channel analyzer, which also counts and stores the number of pulses within given increments of the voltage (energy) range.

3.2.4 X-ray Diffraction (XRD)

The aim of X-ray diffraction experiment is to determine the distribution of the scattering power, s, as a function of :

$$s = (S-S_0)/\lambda$$

Where, S and S_0 are the unit vectors along the diffracted and incident rays, and λ is the wavelength of the incident radiation[33].

From the directions of the diffracted rays corresponding to a given incident beam, the geometry of the reciprocal lattice can be determined, from which we determine the crystalline lattice without difficulty. The most important part (angle detector) and light path of XRD meter is shown in Fig 3.6. There are two coaxial rotary platforms, at the center of the platform is the sample holder H. Detector D and slit RS are fixed on justify jig E. Rotary platforms can rotate around axial of XRD meter O. The X-ray source S is fixed and is on the same circle (as is called XRD circle) as slit RS. Sample holder and detector can be rotated with the rotary platform, rotary angle can be displayed on the ruler K. A and B are Solar optical gratings. The light beams pass through A and slit DS and are incident on the sample, the diffracted light which passes through slit SS, B, slit RS and detector is then recorded as an electronic signal. Slits DS, SS and RS are used to control the light divergence[33-35].

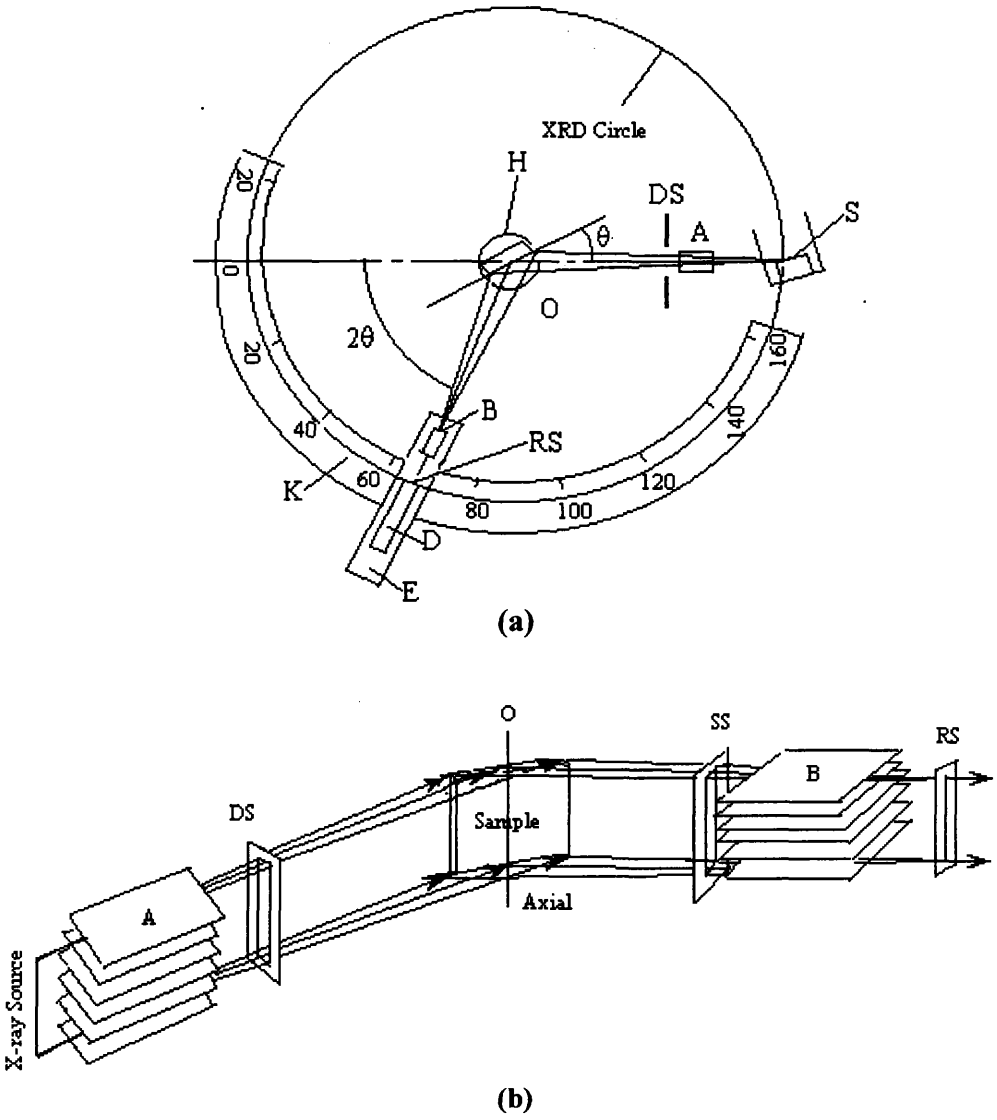


Fig 3.6 a) Angle detector of XRD meter b) Light path of XRD meter

The beam of X-rays with wavelength λ is incident on the specimen and is diffracted by the crystalline phase in the specimen. According to Bragg's law:

$$n\lambda = 2d\sin\theta$$

Where, λ is X-ray wavelength, d is the inter-planar spacing, θ is the Bragg diffraction angle and n is the order of diffraction (n=0, 1,2....)

The intensity of the diffracted X-ray is measured as a function of the diffraction angle 2θ and the specimen's orientation. It can be used to identify the specimen's crystalline phases and to measure its structural properties.

Considering the materials of certain structure, some are obviously crystalline in composition while others are not. The ability to detect crystallinity improved enormously with the Laue experiments in 1912[33], which showed that X-rays are diffracted by crystals to give a characteristic X-ray pattern. Some solids, such as glasses, appear to be obviously noncrystalline (amorphous), but they give weak and diffuse diffraction which indicate that their structures are at least partly ordered. Thus comparing crystalline and amorphous materials, the X-ray diffraction pattern of crystalline material will be more clear and sharp. Examples of X-ray diffraction spectra are shown in Fig 3.7.

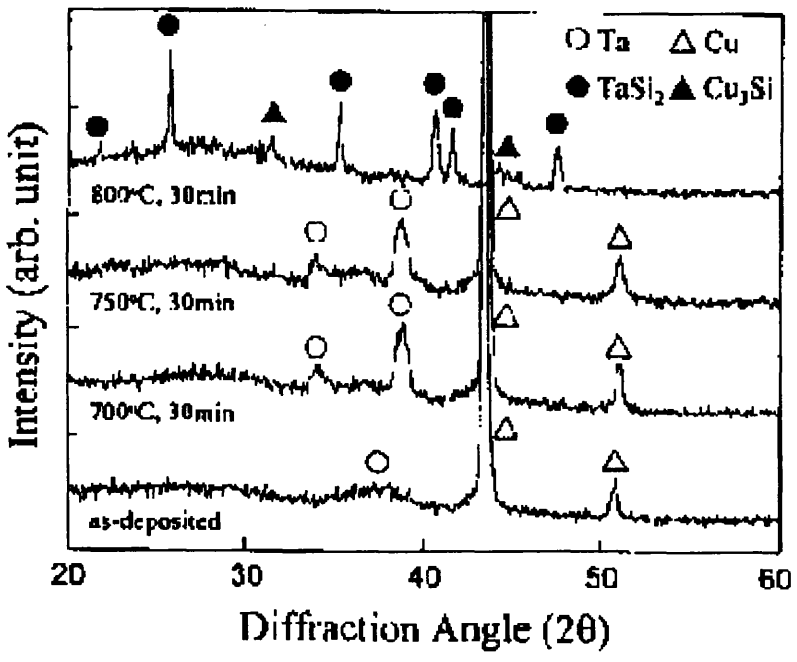


Fig 3.7 Examples of X-ray diffraction spectra of some metals[42]

CHAPTER 4

EXPERIMENTAL DETAILS

4.1 Processing

4.1.1 Wafer Cleaning

In this study, silicon wafers of orientation (100), type p and n, resistivity 5-10Ω.cm and thickness of 600μm have been considered as substrate materials. These wafers were cleaned using the following cleaning procedures:

1. Use M-pyrol (10 minutes Primary and 10 minutes Secondary) at 95^0C to remove native SiO_2 and any particle bonded on the surface of the wafers, rinse in cold de-ionized (DI) water for 10 minutes.
2. P-clean (5:1 H_2SO_4:H_2O_2) at 110^0C to remove any organic residues on the wafers. Then the wafers are rinsed in hot DI water for 10 minutes followed by cold DI water rinse for 5 minutes. In addition, the silicon wafers are dipped into a 100:1 H_2O:HF mixture immediately before they are loaded into the sputtering chamber to etch off the native oxide after the acid clean.

4.1.2 Sputter Deposition and Annealing of $TaSi_2$ Thin Films

The VARIAN 3125 magnetron DC sputtering system with a composite target $TaSi_2$ was used to deposit tantalum silicide thin films. The sputter chamber was pumped to a pressure of better than $8x\ 10^{-7}$ Torr. Sputtering was done at an argon pressure of 5-7 mTorr. Tantalum silicide thin films deposited on silicon wafer had thickness values

of 200, 600 and 1000Å. The film thickness was measured by Quartz Resonator Thickness Monitor which is fixed inside the sputtering machine. The deposition parameters are given in Table 4.1.

Table 4.1 Deposition parameters for tantalum silicide

Parameter	Value
Steady State Substrate Temperature	75°C
Base Pressure I	8.0×10^{-7} Torr
Base Pressure II	0.9×10^{-6} Torr
Deposition pressure	5-7 mTorr
Backfill Gas	Argon
Deposition Rate	3Å/second
Target Composition	$TaSi_2$

The $TaSi_2$/Si(p type) wafers were annealed in forming gas (90%N_2+10%H_2) for 30 min. at temperatures of 400, 500, 700, 900°C and in N_2 ambient at temperatures of 600 and 800°C. The schematic of the annealing furnace utilized in this study is shown in Fig. 4.1.

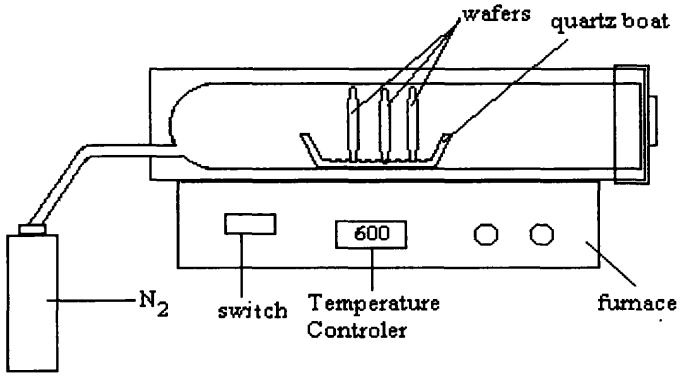


Fig 4.1 Schematic of annealing furnace

4.1.3 Wet Oxidation of $TaSi_2$/Si wafers

Wet oxidation of $TaSi_2$/Si wafers after annealing was carried out in steam at various temperatures from 500°C to 900°C. The experimental system utilized in this study is shown in Fig. 4.2.

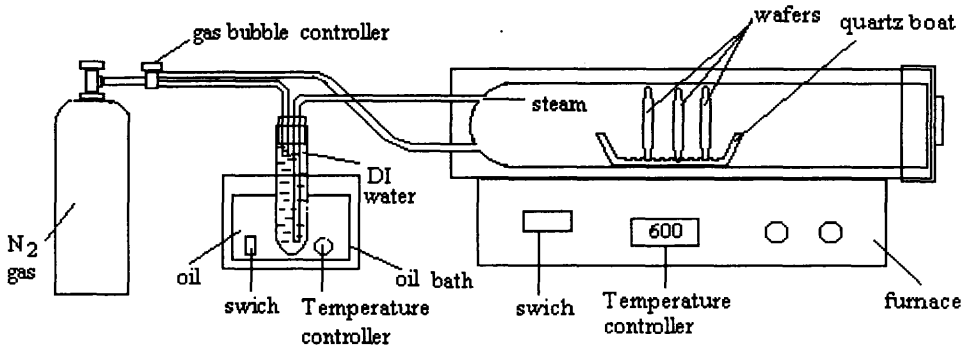


Fig 4.2 Experimental system of wet oxidation

The temperature of oil bath was set to 98°C and the samples were introduced into the furnace after the furnace temperature became stable. The samples were oxidized in steam for durations of 30 min to 1.5 hours.

4.2 Characterization Techniques

4.2.1 Four Point Probe

Sheet Resistance of sputter deposited wafers before and after annealing were measured by four-point probe technique. The sheet resistance was measured by lightly pressing a four-point metal-tip probe assembly into the surface of wafer. During these measurements, the outer probes are connected to the current source, and the inner probes detect the voltage drop.

4.2.2 FTIR

FTIR was first used to analyze the compositional properties of the $TaSi_2$/Si wafers before annealing, blank Si wafer was used as the background.

4.2.3 EDAX

EDAX was used to measure the compositional properties of $TaSi_2$/Si wafer before annealing. In this case, the wafer is a p-type Si substrate with 600Å sputter deposited $TaSi_2$ thin film. The energy of EDAX is in the range of 0-20KeV and the step size is 2354 Counts/Second.

4.2.4 X-ray Diffraction

Rigaku X-ray diffraction system has been utilized to evaluate the structural properties of $TaSi_2$(1000Å) thin films before, after annealing and after oxidation. The parameters of X-ray diffraction analysis before annealing are :

Start 2Theta:	15	Stop 2Theta:	75
Step Size:	0.01	Scan Speed:	0.5
KV:	30	mA:	20

The scanning parameters of $TaSi_2$ (1000Å) thin films after annealing and after oxidation were set as:

Start 2Theta:	20	Stop 2Theta:	50
Step Size:	0.04	Scan Speed:	0.2
KV:	30	mA:	20

CHAPTER 5

RESULTS AND DISCUSSIONS

5.1 Measurements on Pre-Annealed $TaSi_2$ Films

5.1.1 Four Point Probe

The sheet resistance of sputter deposited films before annealing are listed in Table 5.1. As is shown in the table, the sheet resistance increases with the increase in thickness of $TaSi_2$. The sheet resistance (R_s) of film deposited on p-type wafer is higher than that deposited on n-type wafer for the same thickness.

Table 5.1 Sheet resistances of sputter deposited $TaSi_2$/Si

Wafer Type	Wafer Thickness (Å)	R_s of $TaSi_2$ (Ω/□)
n	200	66.0
n	600	36.7
n	1000	22.5
p	200	130.1
p	600	46.9
p	1000	27.5

5.1.2 FTIR

The FTIR spectra of 1000Å $TaSi_2$/n-Si before annealing is shown in Fig 5.1. From the measured spectra, we can see that except for the peaks in the wavenumber range of 3000 to 4000 cm^{-1}, there are no observable peaks. That is to say, we cannot detect the Ta-Si peak from FTIR. This could be due to the fact that silicon wafer absorbs all the infrared radiation possibly due to its heavy doping. For the other sputter deposited wafers in the experiment, the FTIR spectra are almost similar to results in Fig. 5.1.

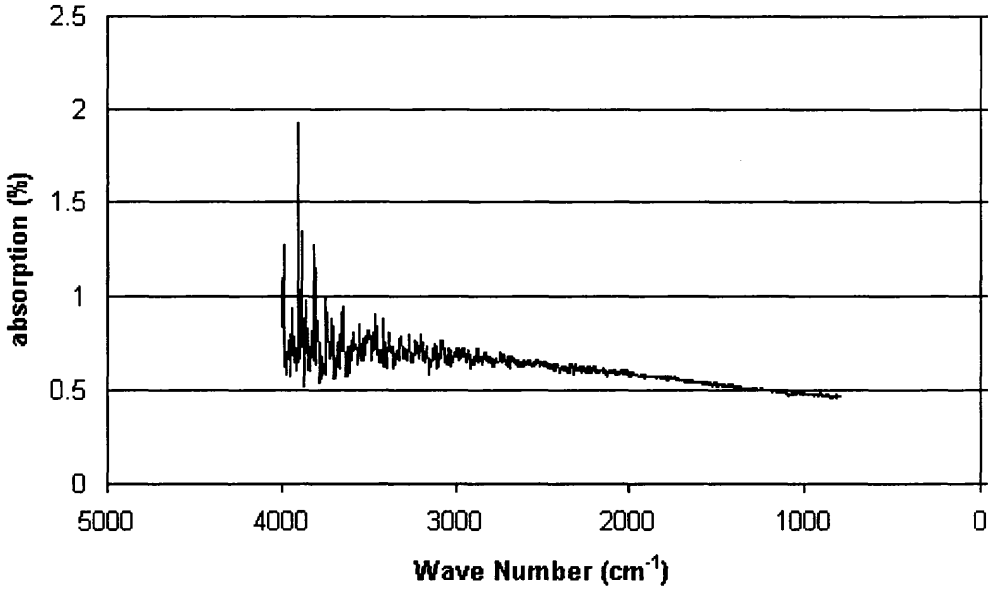


Fig 5.1 FTIR Spectra of 1000Å $TaSi_2$/n-Si

5.1.3 EDAX

The EDAX spectra of 600Å sputter deposited $TaSi_2$/p-Si is shown in Fig. 5.2. In this spectra, peaks due to Si, Ta, Ga and Ag can be seen. Ga is the dopant, and Ag is the glue (Ag paint was used to fix the sample on the sample holder). The quantitative analysis results of EDAX are shown in Table 5.2.

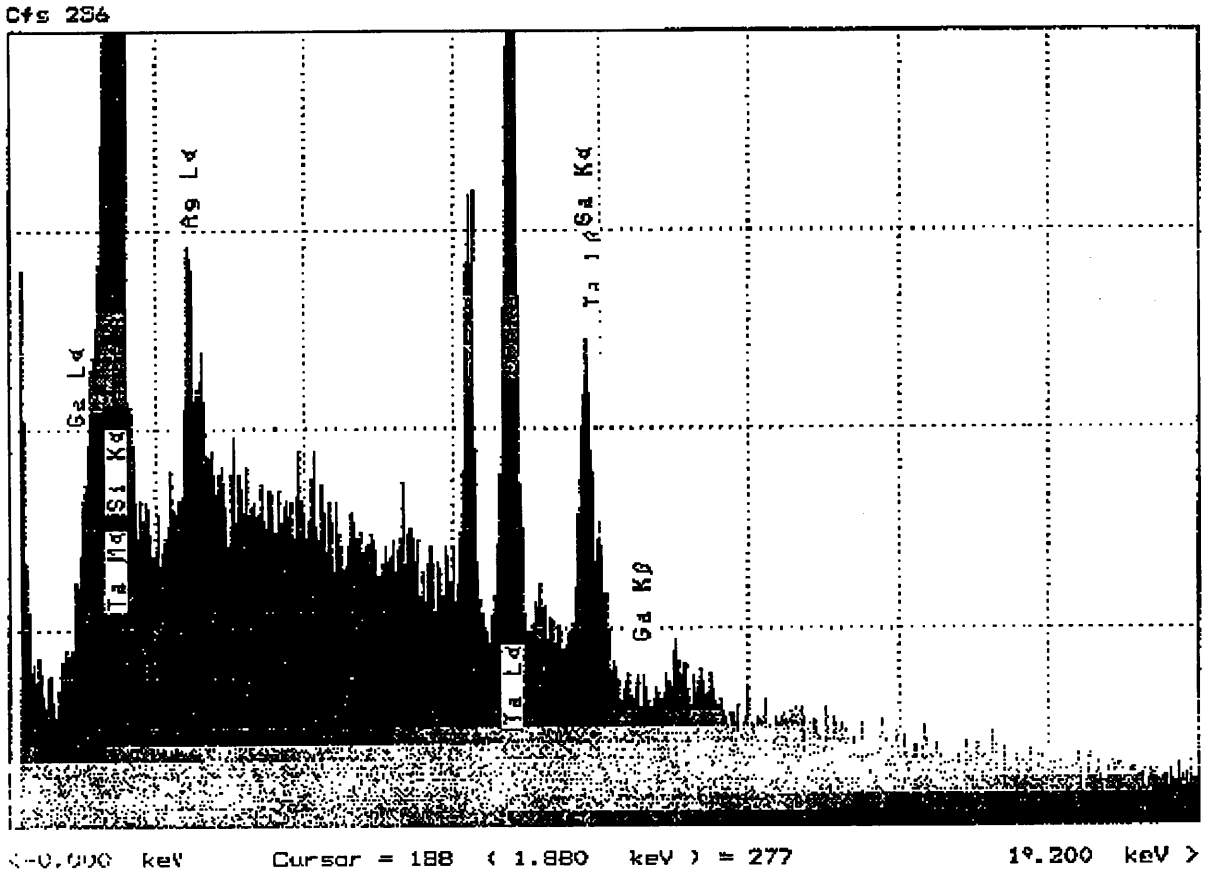


Fig 5.2 EDAX spectra of 600Å $TaSi_2$ on p – Si

Table 5.2 EDAX results of $TaSi_2$ (600Å) thin films

Element	Line	Weight %	Atomic %*	Net Intensity
Si	K	41.80	79.5	70.90
Ga	K	6.25	4.8	0.48
Ag	L	2.07	1.0	0.85
Ta	L	49.88	14.7	3.17

* Data are approximate, not calibrated

5.1.4 X-ray Diffraction

From the X-ray diffraction spectra shown in Fig. 5.3, for an unannealed 1000Å $TaSi_2$ film, there is no detectable peak due to $TaSi_2$. It may be because of the amorphous structure of $TaSi_2$. The values of the main peaks as determined from the peak finding program are shown in Table 5.3.

Table 5.3 Characteristic peaks of $TaSi_2$ obtained from "peak find" program

Peak	2-Theta	D-space(Å)	I(REL)	I(CPS)	FWHM	Identification Orientation
1	68.63	1.3664	100.00	210294.5	0.136	(400)
2	32.41	2.7602	0.26	554.9	0.167	(200)

The most intense peak in the spectrum occurs at $2\theta = 68.63^{\circ}$, d = 1.3664 Å. From the standard X-ray diffraction card of Si shown in Appendix B, it can be verified that the peaks in the spectrum are due to Si(400) and Si(200).

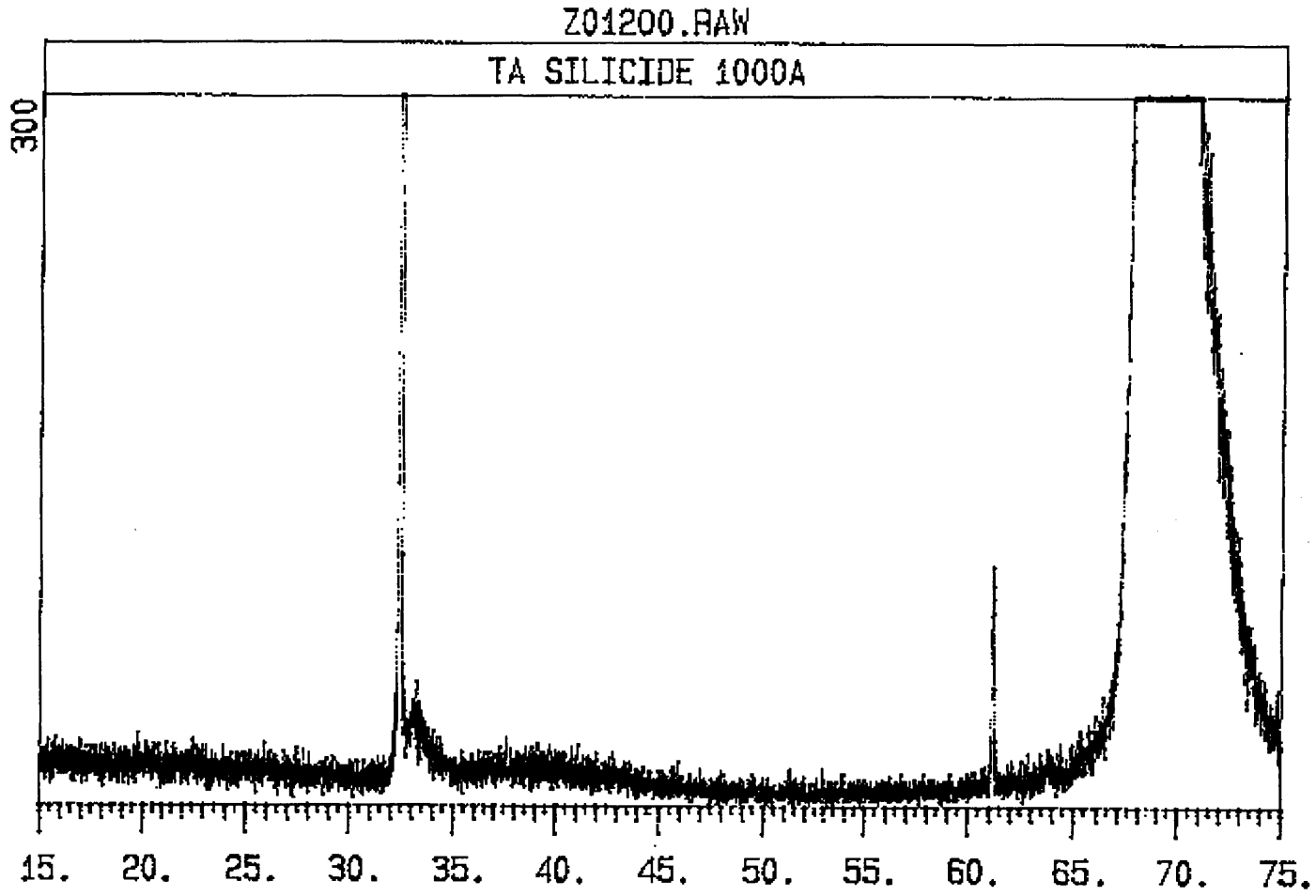


Fig 5.3 XRD of $TaSi_2$ thin film (1000Å) before annealing

5.2 Measurements on Post-Annealed $TaSi_2$ Films

5.2.1 Four Point Probe

1000Å $TaSi_2$/Si wafers were annealed from 400°C to 900°C for 30 min, respectively, and the sheet resistance of wafers was measured for each annealing temperature. The results of resistance data are shown in Fig. 5.4.

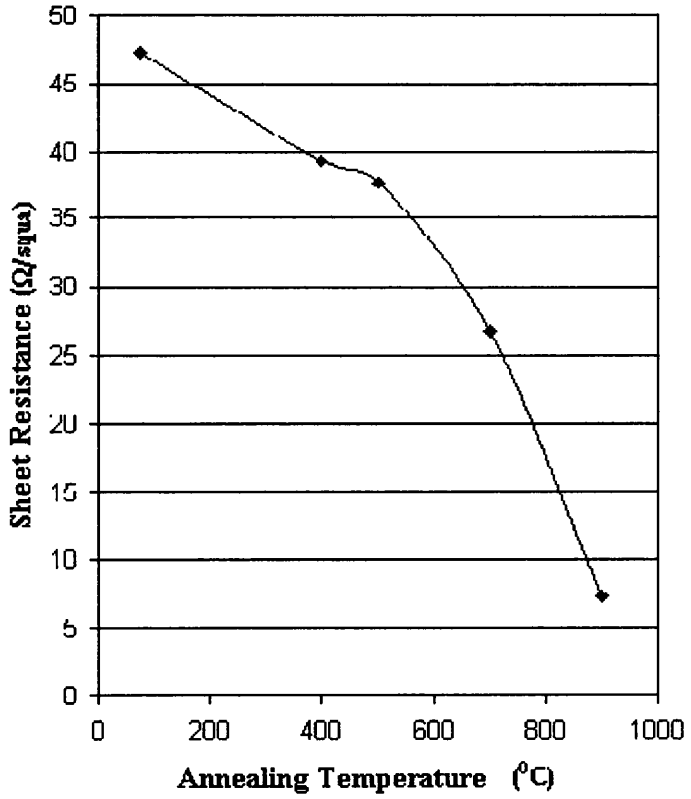


Fig 5.4 Sheet resistance of $TaSi_2$ thin films versus annealing temperature

It maybe noted that the sheet resistance of $TaSi_2$ thin films decreases with increase in annealing temperature. Between 500 and 900°C, there is an abrupt change in sheet resistance. A Comparison with literature[8,11,21,41] shows that our results are in agreement

with the published sheet resistance data. Fig 5.5 shows Cho's experimental data of sheet resistance of $TaSi_2$ thin films [8].

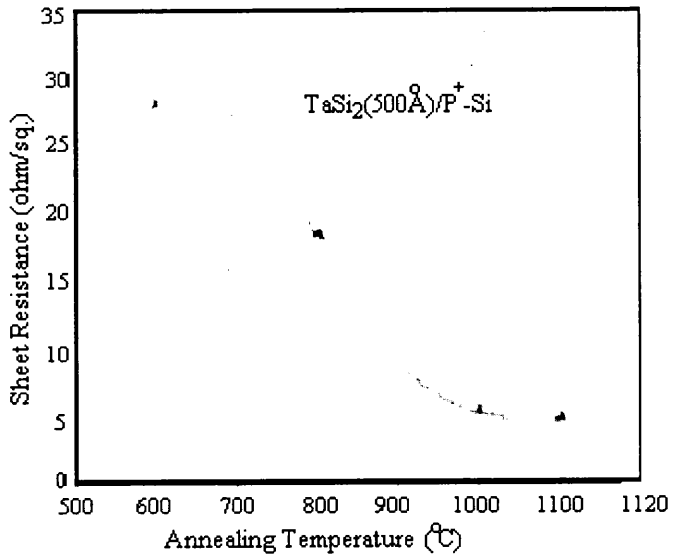
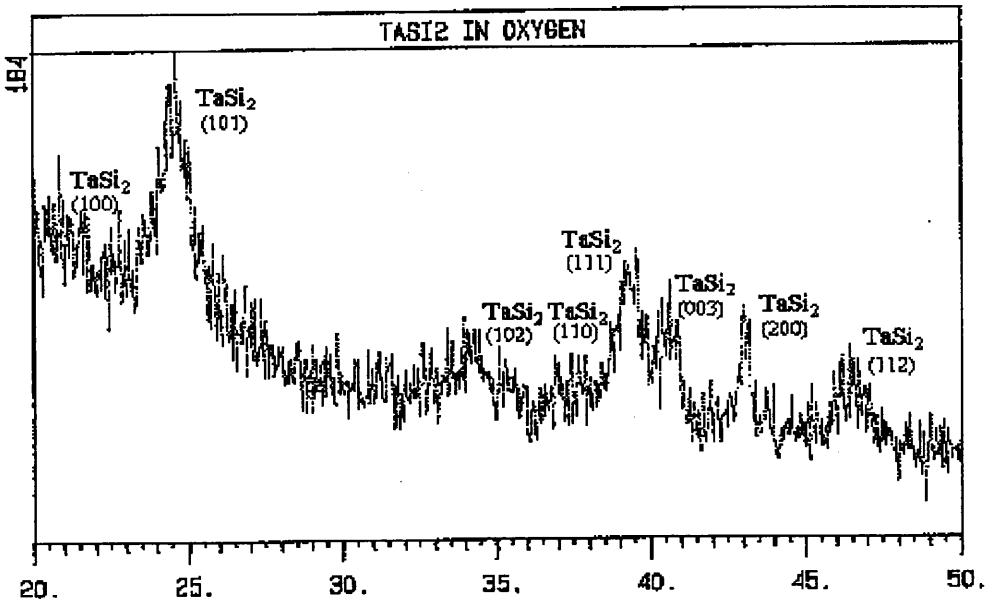


Fig 5.5 Cho's experimental data of sheet resistance of $TaSi_2$ thin films [8]

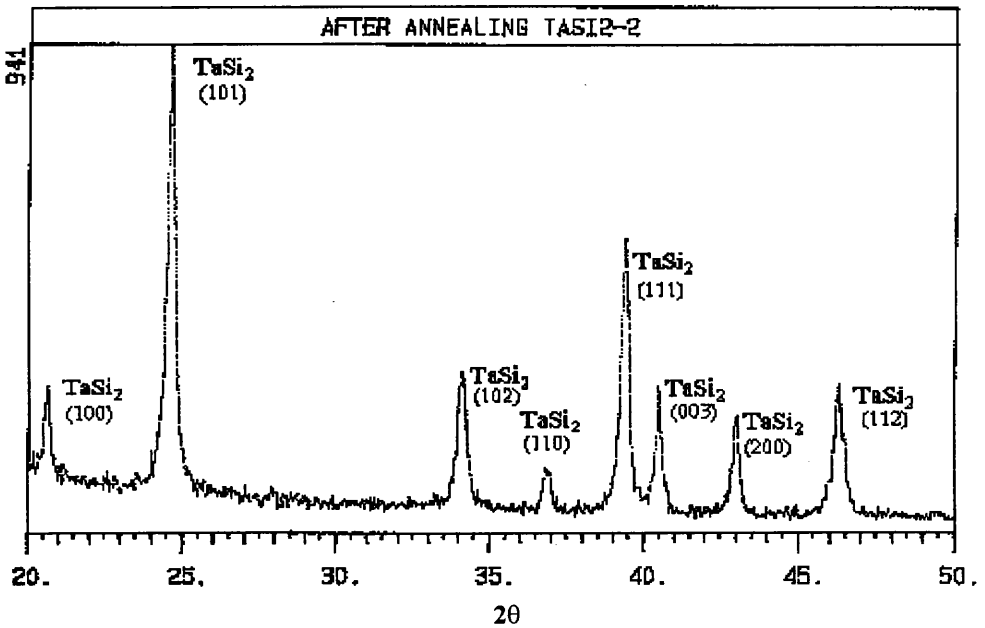
5.2.2 X-ray Diffraction

$TaSi_2$ thin films prepared in forming gas or N_2 under various annealing temperatures were analyzed by X-ray diffraction methods. XRD spectra of $TaSi_2$ thin films annealed at 600 and 900°C are shown in Fig.5.6. From the X-ray diffraction result shown in Fig 5.6, forming gas and N_2 did not have differences in their influence on $TaSi_2$/p-Si wafers. From this spectra, it is clear that peaks other than Si peak are observed. A comparison with the standard X-ray diffraction card of $TaSi_2$ shown in Appendix B confirms peaks obtained as due to $TaSi_2$ (100), (101), (102), (110), (111), (003), (200) and (112) orientations. Other phases, such as Ta_2Si and Ta_5Si_3 (X-ray diffraction spectrum shown in Fig 2.9 in Chapter 2) were not found within the detection limit of the experiment. This result agrees well with the X-ray diffraction peaks published in the literature[11,42] (See Fig 5.8). Comparing these two XRD spectra, the peaks in Fig 5.6 (a) are wider and have less intensity than those in Fig.5.6 (b). That is to say, the micro-structures of $TaSi_2$ thin

film become crystallized after annealing, and become more and more orderly with increase in annealing temperature.



(a)



(b)

Fig5.6 XRD spectra of 1000ÅTaSi$_2$ thin films on n- Si after annealing (a) 600°C annealing in N_2 (b)900°C annealing in forming gas

From Fig. 5.7, it can be seen that as annealing temperature increases, the peaks of $TaSi_2$ thin film become more narrow and exhibit increased intensity. The data of intensity and full width-half maximum (FWHM) of peak (101) are listed in Table 5.4 in order to give a quantitative comparison. From Table 5.4, we can see that from annealing temperature 800 to 900°C, the characteristic of diffraction peak changes abruptly. It can be concluded from this result that crystallization of $TaSi_2$ occurs mainly between 800 and 900°C. Hyun-Choon Cho's work[11] shows (Fig. 5.8) the result that continuous phase transformation occurs above 800°C. In the spectra of sample annealed at 700°C, only β-tantalum(002) peak is detected. In this study, however, $TaSi_2$ peaks have been observed at annealing temperature of 600°C. This may be because of the differences in thickness of the $TaSi_2$ thin film and characteristics of Si substrates (doping concentration, thickness, etc.).

Table 5.4 Data of $TaSi_2$ (101) peaks for different annealing temperature.

Annealing Temperature(°C)	2-Theta(°)	D-space(Å)	Intensity	FWHM
600	24.60	3.6259	124	2.594
700	24.680	3.6044	135	1.187
800	24.760	3.5929	187	0.836
900	24.640	3.6101	887	0.312

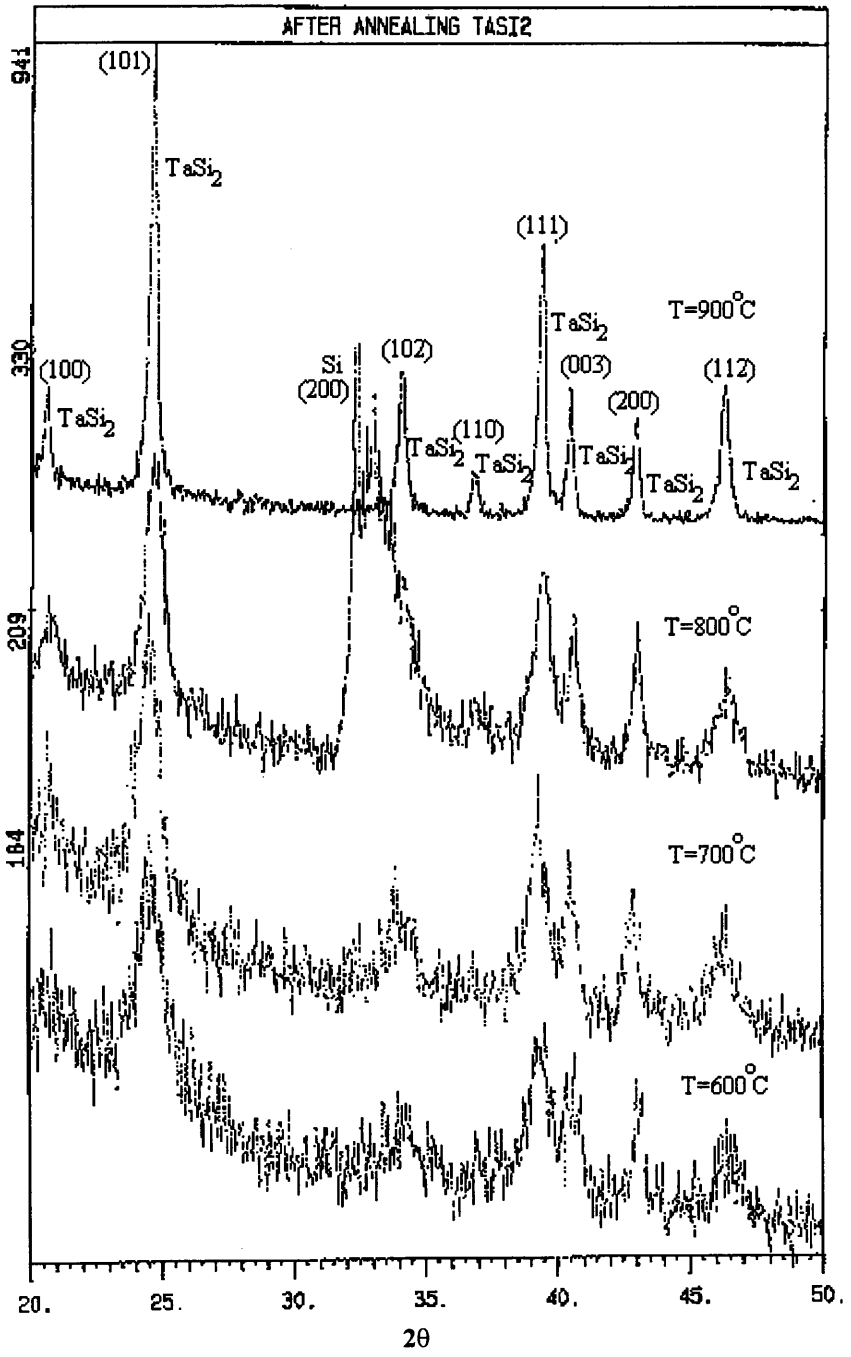


Fig5.7 Comparison of XRD spectra of 1000ÅTaSi$_2$ thin films on n- Si after annealing (from 600°C to 900°C)

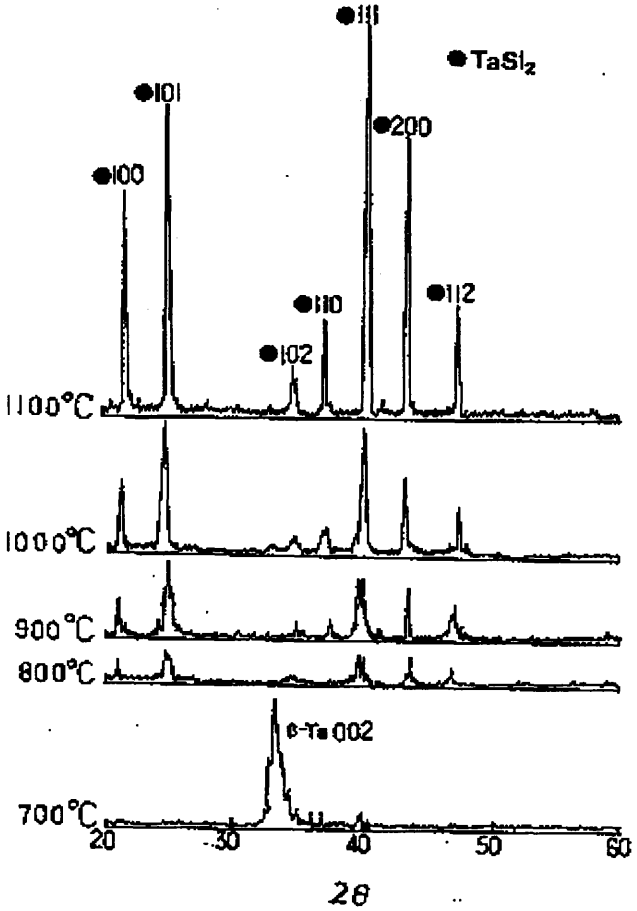


Fig 5.8 X-ray diffraction spectra of $TaSi_2$/Si (Hyun-Choon Cho's work)[11]

5.3 XRD Measurements on $TaSi_2$ Films After Wet Oxidation

It can be predicted that the phases connected by a solid tie line are stable according to the ternary Ta-Si-O phase diagram shown in Fig. 5.9. Thus, Ta_2O_5 can be produced by the oxidation of $TaSi_2$ at temperatures of 600-1100°C. A comparison of this work with Fang-Xing Jiang's work[45] of X-ray diffraction spectra of Ta_2O_5 thin films (Fig. 5.10) shows that there is no Ta_2O_5 phase formation after wet oxidation of $TaSi_2$ thin films. From the spectra of XRD shown in Fig 5.11, no visible tantalum oxide peaks were found. All the peaks obtained in this spectrum are $TaSi_2$ peaks comparable to spectra in Fig 5.7. It can

be concluded that there is no oxidation occurring in $TaSi_2$ thin film. This result is in agreement with Murarka et al. [44]. They had found that $TaSi_2$ does not oxidize in dry O_2 and oxidizes in steam, giving SiO_2 and a surface layer of mixed Ta-Si oxides. During wet oxidation of $TaSi_2$, the top oxide layers do not act as diffusion barrier for water molecules. On continued oxidation, SiO_2 is formed, and silicon in the silicon-rich layer is replenished continuously by steady diffusion of silicon from polycrystalline silicon to the silicide-SiO_2 interface. This steady flow is established during the early stages of oxidation. No further oxidation of tantalum takes place because of the shielding effect of the silicon-rich layer[44].

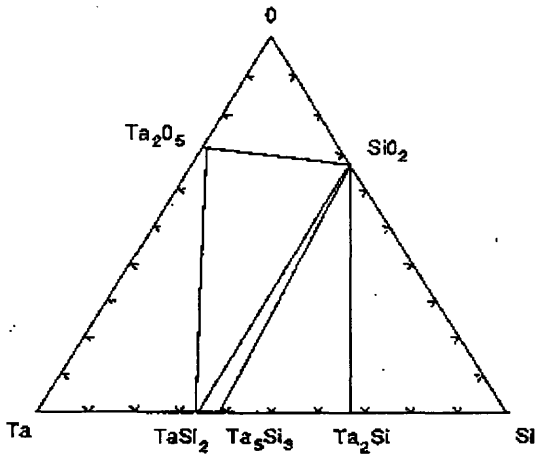
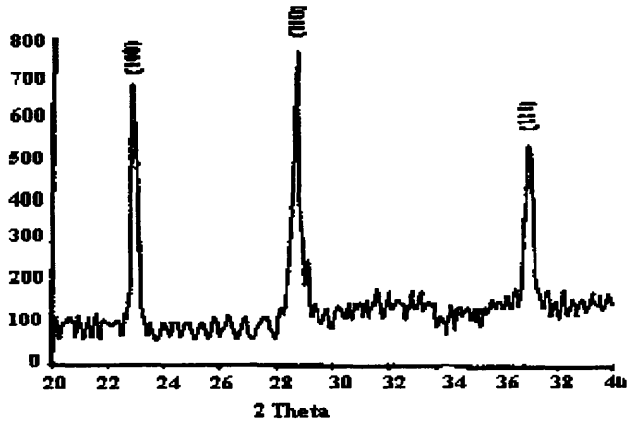


Fig 5.9 Ternary Ta-Si-O phase diagram (600-1100°C)[11]



5.10 X-ray Diffraction spectra of Ta_2O_5 thin films (Fang-Xing Jiang's work)[45]

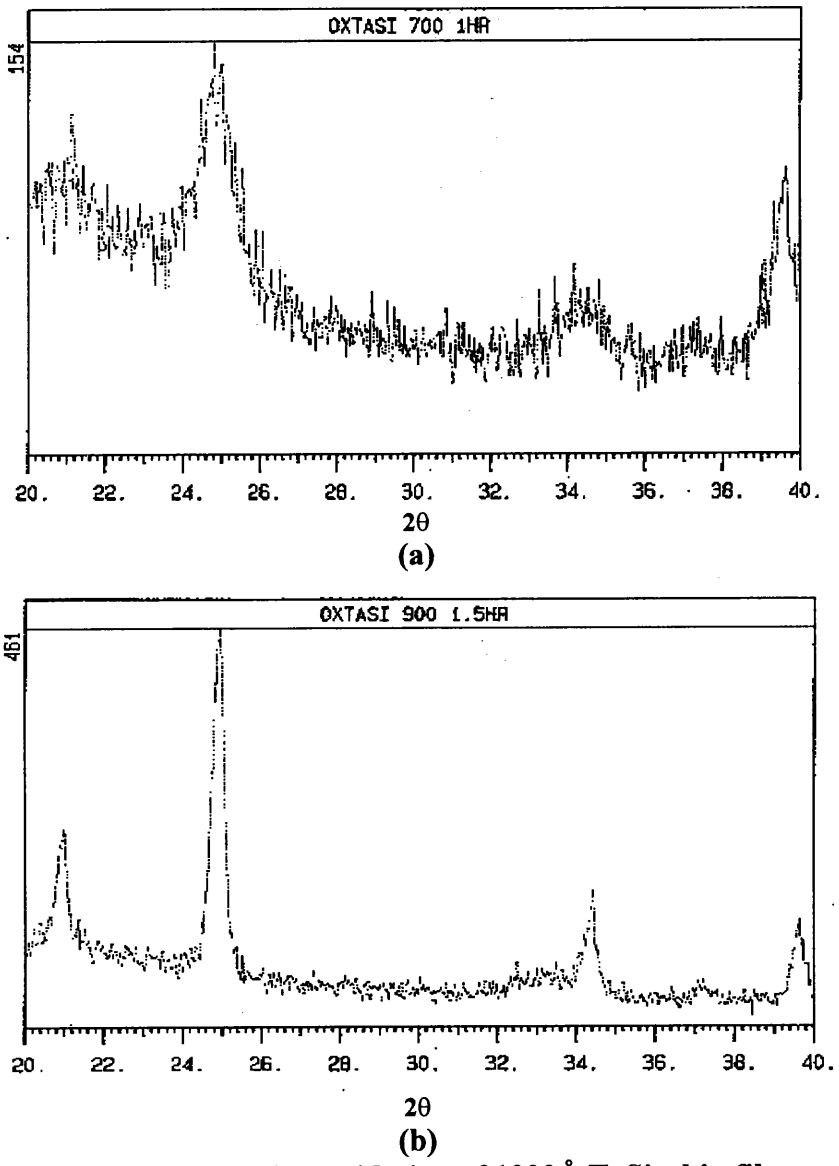


Fig. 5.11 XRD spectra after oxidation of 1000Å $TaSi_2$ thin film on n- Si (a) 700°C for 1 hour (b) 900°C for 1.5 hours

CHAPTER 6

CONCLUSIONS

$TaSi_2$ thin films were sputter deposited on p-Si and n-Si by using VARIAN 3125 magnetron DC sputtering system with $TaSi_2$ target. The thicknesses of $TaSi_2$ thin films are 200, 600 and 1000Å, respectively. The wafers were then annealed at temperatures in the range of 400 to 900^0C. The results of this study lead to the following conclusions:

1. FTIR cannot be used to characterize $TaSi_2$ thin films, because the films are metallic and thin enough such that the absorption is too weak to be detected by FTIR. The heavily doped silicon substrates add to the complexity of the problem.

2. EDAX results lead to the conclusion that the main compositions of thin film are Si and Ta.

3. Four Point Probe results show that the sheet resistance of $TaSi_2$ thin film increases with increase in film thickness and annealing temperature. Sheet resistance has an abrupt change in the annealing temperature range of 700 to 900^0C.

4. X-ray diffraction results show that the microstructure of $TaSi_2$ thin film changes from amorphous to crystalline as annealing temperature increases. In the

annealing temperature range of 800 to 900°C, the characteristics of diffraction peaks changes considerably.

5. Oxidation characteristics of $TaSi_2$ thin films have been investigated in the temperature range of 500- 900°C. According to XRD results, there are no detectable Ta_2O_5 peaks. It may be due to the shielding effect of surface Ta-Si oxides formed on $TaSi_2$ thin films.

APPENDIX A

CLEANROOM TRAVELER

Wafer annealing and sheet resistance measurements

Starting Materials 4" p-type $TaSi_2$/Si wafer (1) (100), 1000Å	Date	Wafer(s)	Operator	Comments
1. M-pyrol 95°C 10min secondary				
2. Rinse hot DI water 10 min				
3. Rinse cold DI water 5 min				
4. Spin dry				
5. Annealing at 400-900°C				
6. Measure the sheet resistance for different annealing temperatures (4-point probe)				

Wafer labeling and cleaning

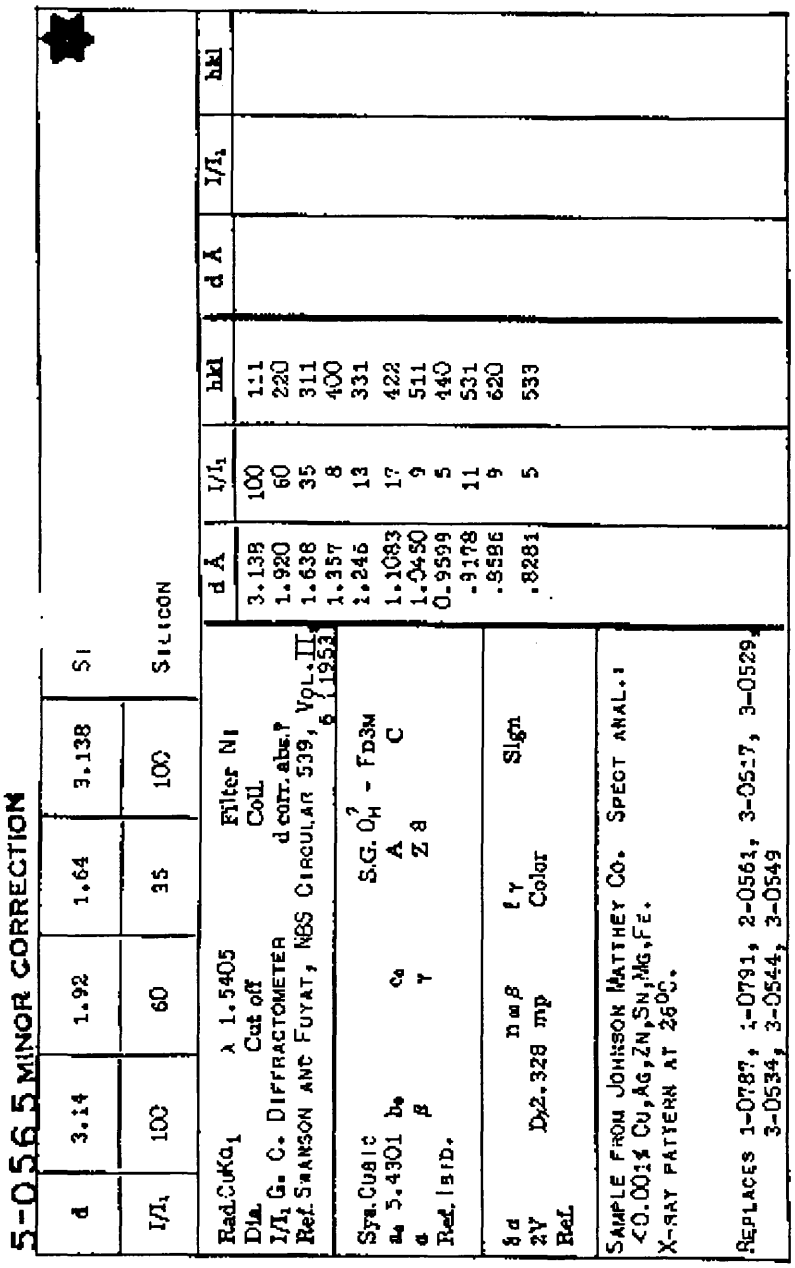
	Date	Wafer(s)	Operator	Comments
Starting material: 4", p-type Si wafer (3) and n-type Si wafer (3) thickness 600μm				
Wafer labeling				
Wafer cleaning **1. M-pyrol, 95°C,** **10 min Primary** **10 min Secondary**				
2.Rinse cold DI water 10min				
3. Spin dry				
4. P-clean **5:1 H_2SO_4:H_2O_2** **110°C, 10 min**				
5. Rinse hot DI water 10min				
6. Rinse cold DI water 5min				
7. Spin dry				
8. Furnace pre-clean 100:1 H_2O:HF, 1 min				
9. Rinse cold DI 5 min				
10. Spin dry				

Sputter deposition and sheet resistance measurements

Starting materials: **4", n-type Si wafers (3)** **p-type Si wafers (3)**				
1. Furnace pre-clean **100:1 H_2O:HF** **1 min**				
2. Rinse cold DI water **5 min**				
3. $TaSi_2$ Sputtering **Thickness(Å): 200, 600, 1000.**				
4. measure the sheet resistance of wafers after sputtering (4-point probe)				

APPENDIX B

XRD STANDARD CARDS



5-0565 MINOR CORRECTION

d	3.14	1.92	1.64	3.138	Si
I/I1	100	60	35	100	

SILICON

Rad. CuKα1 λ 1.5405 Filter Ni
Dia. Cut off Coll.
I/I1 Ge. C. Diffractometer d corr. abs.?
Ref. Swanson and Fuyat, NBS Circular 539, Vol. II, 6 (1953)

d Å	I/I1	hkl
3.138	100	111
1.920	60	220
1.638	35	311
1.357	8	400
1.246	13	331
1.1083	17	422
1.0450	9	511
0.9599	5	440
.9178	11	531
.8586	9	620
.8281	5	533

Sys. Cubic S.G. O_h^7 - Fd3m
a_o 5.4301 b_o c_o A C
α β γ Z 8
Ref. Ibid.

ε α	n ω β	ε γ	Sign
2V	Dx 2.328	mp	Color
Ref.			

Sample from Johnson Matthey Co. Spect anal.: <0.001% Cu, Ag, Zn, Sn, Mg, Fe.
X-ray pattern at 26°C.

Replaces 1-0787, 1-0791, 2-0561, 3-0517, 3-0529, 3-0534, 3-0544, 3-0549

XRD standard card of Si

8-53

d	3.50	2.25	1.93	4.13
I/I_1	100	94	63	22

$TaSi_2$

TANTALUM SILICIDE

Rad. $CuK\alpha_1$ λ 1.5405 Filter Ni Dia.
Cut off I/I_1 DIFFRACTOMETER
Ref. NBS CIRCULAR 539, 8 (1958)

Sys. HEXAGONAL S.G. $D_6^4 - P6_322$
a_o 4.7821 b_o c_o 6.5695 A C
α // γ Z 3 Dx 9.073
Ref. Ibid.

$\varepsilon\alpha$ $n\omega\varepsilon$ $\varepsilon\gamma$ Sign
2V D mp Color DARK GRAY; OPAQUE
Ref.

SAMPLE PREPARED AT THE NBS BY SOLID STATE REACTION OF THE ELEMENTS AT 1300°C FOR THREE HOURS. SPECT. ANAL. SHOWED <0.01% AL, CR, CU, FE, MG, NI, TI; <0.001% AG, CA, MN. $CrSi_2$ STRUCTURE TYPE. PATTERN MADE AT 25°C.

d Å	I/I_1	hkl	d Å	I/I_1	hkl
4.13	22	100	1.1580	4	303
3.50	100	101	1.1513	10	115
2.57	58	102	1.1330	9	214
2.389	17	110	1.1316	11	311
2.366	34	111	1.0947	5	006
2.187	32	003	1.0846	7	312
2.070	36	200	1.0569	8	304
1.932	63	112	1.0493	17	223
1.619	10	113	1.0357	3	400
1.565	6	210	1.0172	1	313
1.525	21	104	1.0064	6	215
1.523	27	211	0.9975	1	116
1.505	24	203	.9879	6	206
1.413	17	212	.9518	5	305
1.380	4	300	.9412	9	314
1.353	21	114	.9404	9	321
1.351	25	301	.9360	3	403
1.2726	17	213,302	.9152	2	107
1.2519	6	105	.9129	7	322
1.1956	13	220	PLUS 12 LINES TO 0.7629		

XRD standard card of $TaSi_2$

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