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ABSTRACT

MICRO ELECTROMECHANICAL RELAYS AND THEIR APPLICATION IN VARIABLE INDUCTOR NETWORKS

by
Shifang Zhou

A family of microrelay devices together with integrated inductor networks has been designed, simulated, fabricated and experimental characterized. These switched networks utilize microelectromechanical systems (MEMS) as a fabrication technology and take advantage of the economies of semiconductor cleanroom batch-processing.

A new type of microrelay has been developed using a suspended $TaSi_2/SiO_2$ bimorph cantilever beam, gold-to-gold electrical contact, aluminum as sacrificial layer, and a combined thermal and electrostatic means of actuation. For the first time a micro variable inductor network which is digitally controlled by microrelays has been demonstrated. A test structure for electrical micro contact characterization has been designed, built and characterized as a support task in this research. The microrelay design has utilized the Rayleigh-Ritz method to simulate the actuation and the electrical contact force.

The cantilever structure of the microrelay contains a specially-shaped area which provides a symmetric force to the electrical contact region and thus reduces the electrical contact resistance. The required thermal power and electrostatic voltage for the combined actuation of microrelays were measured typically as 11 mW and 30 ~ 40 volts, respectively. The electrical contact resistance was typically 0.6 to 0.8 Ohms. The maximum operation frequency was 10 KHz and the microrelay closure and opening time

were typically 12 μS. A limited number of lifetime tests were performed indicating the device lifetime to be about 10^6 cycles.

A micro variable inductor network consisting of a 16-turn rectangular spiral coil and four controlling microrelays was designed and fabricated. A larger coil structure was divided into four segments. Each inductor segment had a microrelay connected with it in parallel. The network inductance values were determined by combinations of switching states of microrelays. Sixteen different inductance values ranging from 2.5 nH to 324.8 nH were obtained. The silicon substrate underneath the inductor region was etched out to reduce the substrate loss. The minimum self-resonant frequency was measured 1.9 GHz.

MICRO ELECTROMECHANICAL RELAYS AND THEIR APPLICATION IN VARIABLE INDUCTOR NETWORKS

by
Shifang Zhou

A Dissertation
Submitted to the Faculty of
New Jersey Institute of Technology
in Partial Fulfillment of the Requirements for the Degree of
Doctor of Philosophy

Department of Electrical and Computer Engineering

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APPROVAL PAGE

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To the memory of
my father

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CHAPTER 1

INTRODUCTION

This research work has developed a new type of microrelay with a combined thermal and electrostatic actuation mechanism, and has used it for the first time to form a variable inductor network which can serve as a switched inductance component for RF & microwave matching impedance networks. The experimental work presented in this dissertation was done under the direction of Prof. William N. Carr in the Department of Electrical & Computer Engineering at New Jersey Institute of Technology.

1.1 Objective

The growing needs for miniature wireless communication have prompted interest in the integration of RF & microwave systems on silicon. Although monolithic inductors have been fabricated by standard silicon technology for several decades, programmable inductor networks are much more desired. For this purpose, basically we need electrical switches which introduce low parasitic effects together with adequate electrical isolation in open state.

Electronic devices such as field effect transistors, thyristors and transistors can not be used to make adjustable inductor networks because they suffer variously from high on-state resistance, low off-state resistance caused by none-zero leakage currents, excessive parasitic capacitance, and cross talk between the control signal and the passing signal. Recently, MEMS (Micro ElectroMechanical System) relays are receiving increasing

attention for their low on-state resistance, high off-state resistance, low parasitic capacitance, and low power consumption.

Based on aforementioned factors, we developed a new type of microrelay and a micro variable inductor network using MEMS relays [1]. The normally opened microrelays were made by bimorph cantilever beams. Status of relays are controlled by external data bits. The inductors is a rectangular spiral coil with underpass connections divided it into several segments. Each inductor segment has a microrelay connected with it in parallel. With different status combinations of relays, different inductance values were obtained.

1.2 Background Information

1.2.1 Review of MEMS Switches and Relays

Microactuated electrical switching devices have two operation modes. In one, the actuation and switching signals are the same. This is classified as a MEMS switch or microswitch. The second is with separated actuation and switching signals, and is referred to as a MEMS relay or microrelay.

Micromachined silicon switches were demonstrated in 1979 by K. E. Petersen [2]. These devices were bulk micromachined, gold-to-gold electrical contact and electrostatically actuated. The contact resistance and switching voltage were about 5 Ω and 70 volts, respectively.

In 1987, H. V. Allen reported their products of pressure switches which were driven by applying pressure on silicon diaphragm [3]. The contact resistance was 1 KΩ when pressure exceeded 3 Bar.

H. Hosaka's work on electromagnetic microrelays which had no integrated magnetic coils was reported in 1993 [4]. These devices required an external coil for electromagnetic actuation. Although the research work revealed electrical characteristics of contact electrodes, no contact resistance values of devices were reported.

The polysilicon microrelays were reported in 1994 with high contact resistance (10 kΩ) caused by polysilicon-to-polysilicon electrical contact [5, 6]. The author further used MEMCAD to analyze the electromechanical behavior based on this type of electrostatic microrelays in 1997 [7]. A nickel microrelay, based on electrostatic actuation and lateral motion was reported by S. Roy in 1995 [8]. The reported contact resistance of 20 Ω is relatively high.

More recent versions of electrostatically-driven microswitches and microrelays with lower contact resistance (<1 Ω) have been reported. J. Drake used a polysilicon paddle as an actuation structure with a higher actuation voltage about 100 volts [9]. The fabrication required wafer bonding technology which caused a complicated process. J. J. Yao used the Al/SiO_2 bimorph as cantilever beams and the polyimide as sacrificial layers to develop microrelays with lowest actuation voltage as 28 volts [10]. P. M. Zavracky used the Ni/Au bimorph as cantilever beams and created two contact tips on the end of the beam for lower electrical contact resistance [11]. This type of microswitches had actuation voltage ranging from 30 to 400 volts according to switch geometry. The modeling for its contact resistance was further studied by the author [12].

A thermally-driven microrelay was reported by J. Simon in 1996 [13]. The device employed the use of a mercury droplet which was a difficult process step. This device had a contact resistance on the order of 1 Ω with a 100 mW power input to the heater.

The only reported electromagnetically-driven microrelays with a fully integrated magnetic coils were made by W. P. Taylor [14, 15]. The fabrication process contained six photomasks and three electroplating steps. The chip area for one microrelay was large (about 8mm x 8mm). The power dissipation and contact resistance were 33~320 mW and 2~3 Ω, respectively.

1.2.2 Review of IC Compatible Inductors

Planar inductors have been implemented in practical systems for many years using a variety of substrates. These include standard PC boards, ceramic and sapphire hybrids, and more recently GaAs IC's [16]. In the early development of Si IC's, planar inductors were investigated [17] but the low quality factor Q and low operation frequencies led to their abandonment as impractical. The losses from the conductive Si substrate, the limited metal thickness, and the parasitic capacitance of component structures to the substrate are the major contributors to low quality factor Q and low self-resonant frequency f_{sr}.

The efforts toward increasing the quality factor Q at microwave and millimeter-wave frequencies for monolithic inductors fabricated by standard silicon technology have been reported [18, 19, 20]. These reports described utilizing multilevel interconnects for inductor integration in two ways: (1) several metal layers can be shunted in parallel to achieve an effective conductor thickness beyond the metal thickness limit; (2) the lower metal levels can be excluded to increase the spacing between inductor and substrate and thus reduce substrate losses.

In addition, adequate inductance L and quality factor Q have mostly been achieved through considerable deviations from standard silicon processing [21, 22]. J. Y.-

C. Chang removed Si substrate under the inductor using bulk micromachining technology to minimize the substrate loss [21]. This increased self-resonant frequency f_{sr} from 800 MHz to 3 GHz. R. G. Arnold used MCM-D technology (multichip module technology) to increase the thickness of both the inductor coil layer and the isolation layer [22]. This increased the quality factor Q from 3 to 6.5 and the self-resonant frequency f_{sr} from 2.47 GHz to 15 GHz.

1.2.3 Development of this Research

In this research work, we created a new concept which introduced microrelays to develop variable inductor networks for the first time. The microrelays were designed to be driven by thermal and electrostatic actuation to provide an optimum match for applied voltage and power consumption, electrical contact force, and switching speed [23]. The inductors are made from gold metal in the form of rectangular spiral coils. The silicon substrate under inductors was etched out to reduce the parasitic oxide capacitance and the eddy current power loss in the substrate semiconductor bulk. The output inductance value is determined by status combinations of individual microrelays and is digitally controlled. The simulation, design, fabrication, testing and results of this device will be described in later chapters in detail.

CHAPTER 2

ELECTRICAL CONTACT CHARACTERIZATION

Characterization of electrical contacts with microdimensions and micronewton contact forces is required for design and modeling of micro electromechanical relays. A range of contact forces which were needed to form stable electrical contact has been reported, depending on the contact shape, area and metal. Forces of ~50 μN for gold-to-gold contact and ~120 μN for palladium-to-palladium were reported with unspecified area [4]. The force required for contact between an AFM tip and a metal-coated surface was less than 1 μN [24]. For microcone-based contacts with contact area of 7.5 mm^2, the applied force of ~20 g was needed [25]. Another reported result of contact force was about 2 g with contact area of 10^5 μm^2[26].

In this chapter a family of measurements obtained using a novel stressed-microdiaphragm structure to provide forces in the range from 23 μN to 686 μN will be described. The electrical contact resistance of structures with metal to metal contacts of varying area and contacting force has been measured. A minimum contact resistance R_{mc} was observed when the contacting force exceeded a force threshold F_t in the micronewton range. For contact areas varying from 10 x 10 μm^2 to 50 x 50 μm^2 the threshold force F_t increased from 40 μN to 159 μN for palladium-to-palladium contacts. Also we will discuss the electrical contact mechanism.

2.1 Design and Simulation of Test Structure

2.1.1 Experimental Structure Description

The physical test structure is shown schematically in Figure 2.1. Wafer A contains a metal film A which is brought into a forced contact with wafer B and corresponding metal film B. Both wafers have a SiO_2 layer to isolate the metal film from the bulk silicon substrate. Electrical switching SPST action occurs when the electrically floating metal film A shorts together the two electrodes of metal film B. The contact force F of the contact closure is determined by the height of the pedestal B and the stiffness of the flexed diaphragm A. The structure contains two contacting areas in series to provide the electrical continuity upon closure. The contact resistance was measured through two pads in wafer B (Figure 2.1(c)).

2.1.2 Geometry Parameters

Figure 2.2 shows the overview of wafer A and B. The side length of diaphragm in wafer A are represented by a while its thickness is t. The mask design determined the size of a and the process controlled the diaphragm thickness t. The dimension of metal A is labeled by L_A, w_A and h_A which represent its length, width and thickness, respectively (Figure 2.3(a)). Similarly, the length, width and height of pedestal B are L_B, w_B and h_B, respectively (Figure 2.3(b)). The mask design made $L_A>L_B$ and $w_A>w_B$ to insure that the electrical contact area was determined by l_B x w_B. There are two electrodes on one pedestal which are separated by a space s. The deflection of the diaphragm Y during the test was determined by the height of pedestal and the thickness of metal A, that is

$Y=h_A+h_B$. Table 2.1 lists the mask controlled dimension parameters and Table 2.2 lists the process controlled dimension parameters.

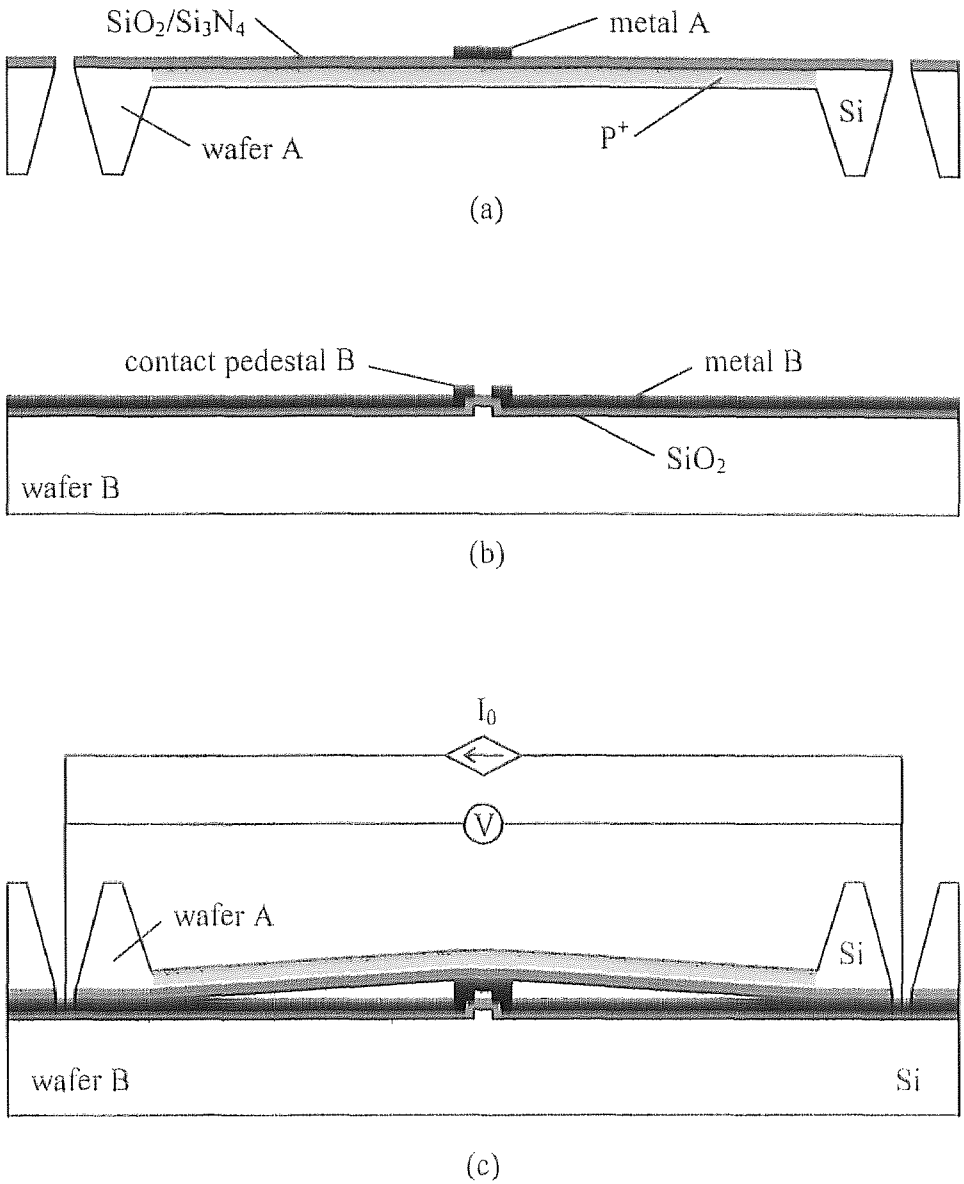


Figure 2.1 Cross section of (a) diaphragm structure A, (b) substrate B with pedestal and (c) two wafers A & B mated

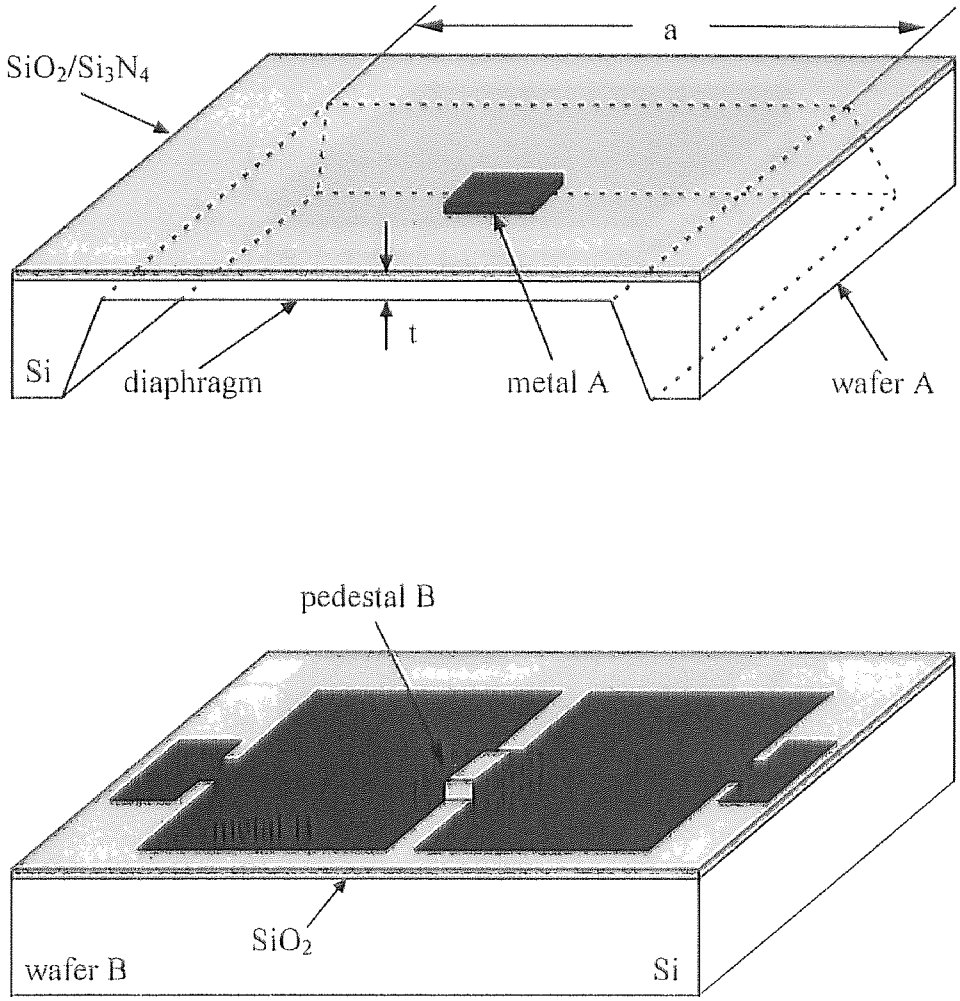
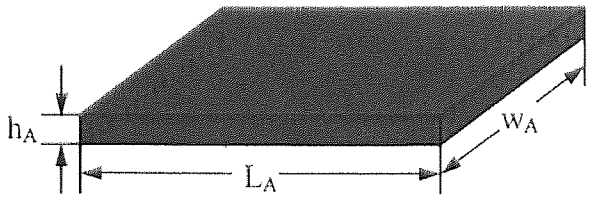
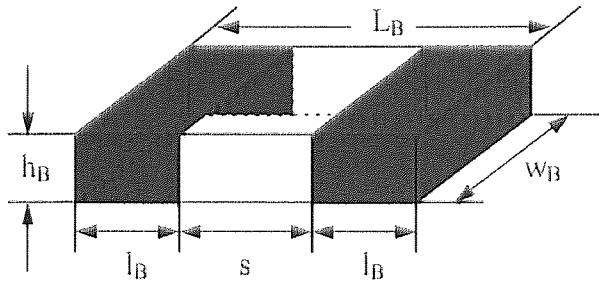


Figure 2.2 Overview of wafer A and B



(a)



(b)

Figure 2.3 Schematic view and geometry parameters of (a) metal A and (b) pedestal B

Table 2.1 Mask controlled dimension parameters

diaphragm	a (μm)	1100			1600		
metal A	L_A (μm)	80	120	160	80	120	160
	w_A (μm)	50	70	90	50	70	90
pedestal B	L_B (μm)	40	80	120	40	80	120
	w_B (μm)	10	30	50	10	30	50
metal B	l_B (μm)	10	30	50	10	30	50
	s (μm)	20	20	20	20	20	20

Table 2.2 Process controlled dimension parameters

diaphragm	t (μm)	2.5	3.0	3.6	4.2	5.3	2.5	3.0	3.6	4.2	5.3
metal A	h_A (μm)	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5
pedestal B	h_B (μm)	1.05					1.67				
deflection	$Y = h_A + h_B$	1.55					2.17				

2.1.3 Simulation of Electrical Contact Forces

When a force is applied uniformly to a small area at the center of a square diaphragm with all edges fixed (Figure 2.4), the relation of the applied force and the maximum deflection at the center of the diaphragm can be expressed as [27]:

$$F = \frac{Et^3Y}{0.0611a^2} \tag{2.1}$$

where F is the applied force, E is Young's modulus of the diaphragm, t is the thickness of the diaphragm, Y is the deflection of the diaphragm at the center, a is the side length of the diaphragm.

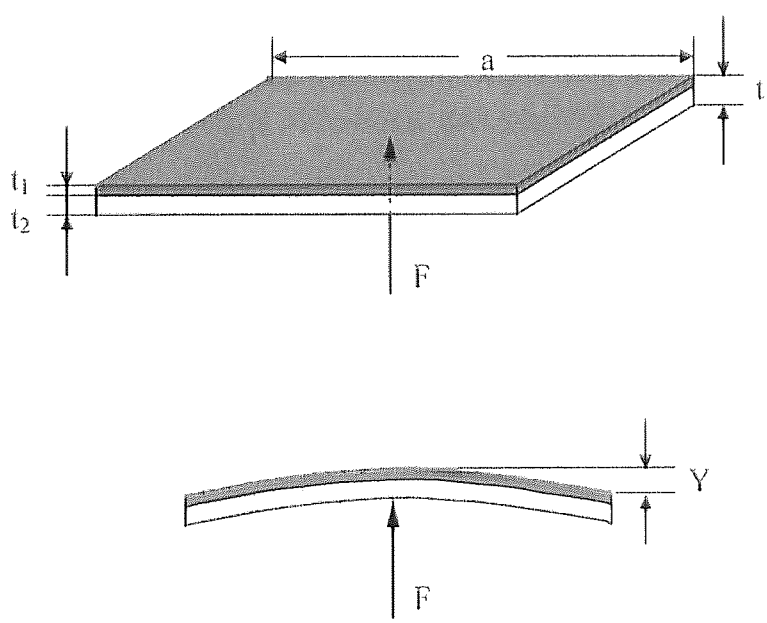


Figure 2.4 Deflection of the diaphragm with a force applied at the center

For bimorph structures, the equivalent stiffness EI is [27]:

$$EI = \frac{a t_1 t_2^3 E_1 E_2}{12\left(t_1 E_1 + t_2 E_2\right)}\left[4 + 6\frac{t_1}{t_2} + 4\left(\frac{t_1}{t_2}\right)^2 + \frac{E_1}{E_2}\left(\frac{t_1}{t_2}\right)^3 + \frac{E_2 t_2}{E_1 t_1}\right] \tag{2.2}$$

where t_1, t_2 and E_1, E_2 are thickness and Young's modulus of layer 1 and layer 2, respectively. For equivalent Young's modulus E_e of bimorph structures, we have:

$$E_e = \frac{EI}{I_0} \tag{2.3}$$

where

$$I_0 = \frac{a}{12}\left(t_1 + t_2\right)^3 \tag{2.4}$$

Substituting (2.2) and (2.4) into (2.3):

$$E_e = \frac{t_1 t_2^3 E_1 E_2}{\left(t_1 E_1 + t_2 E_2\right)\left(t_1 + t_2\right)^3}\left[4 + 6\frac{t_1}{t_2} + 4\left(\frac{t_1}{t_2}\right)^2 + \frac{E_1}{E_2}\left(\frac{t_1}{t_2}\right)^3 + \frac{E_2 t_2}{E_1 t_1}\right] \tag{2.5}$$

In our test structure, layer 1 is a SiO_2/Si_3N_4 (2000Å/1500Å) bimorph structure with Young's modulus 74GPa/155GPa [28]. Its equivalent Young's modulus is equal to 103.5 Gpa. Choosing out layer 1 to be a 0.35 μm thick SiO_2/Si_3N_4 film with Young's modulus 103.5 GPa and layer 2 to be single crystal Si with Young's modulus 169 Gpa [29], the equivalent Young's modulus of diaphragms has been simulated as a function of the thickness of Si using expression (2.5). The result is shown in Figure 2.5.

Using the equivalent Young's modulus obtained from Figure 2.5, the forces applied to the diaphragms have been simulated as a function of the side length using expression (2.1) and shown in Figure 2.6 with the deflection Y=1.55 μm and in Figure 2.7 with the deflection Y=2.17 μm.

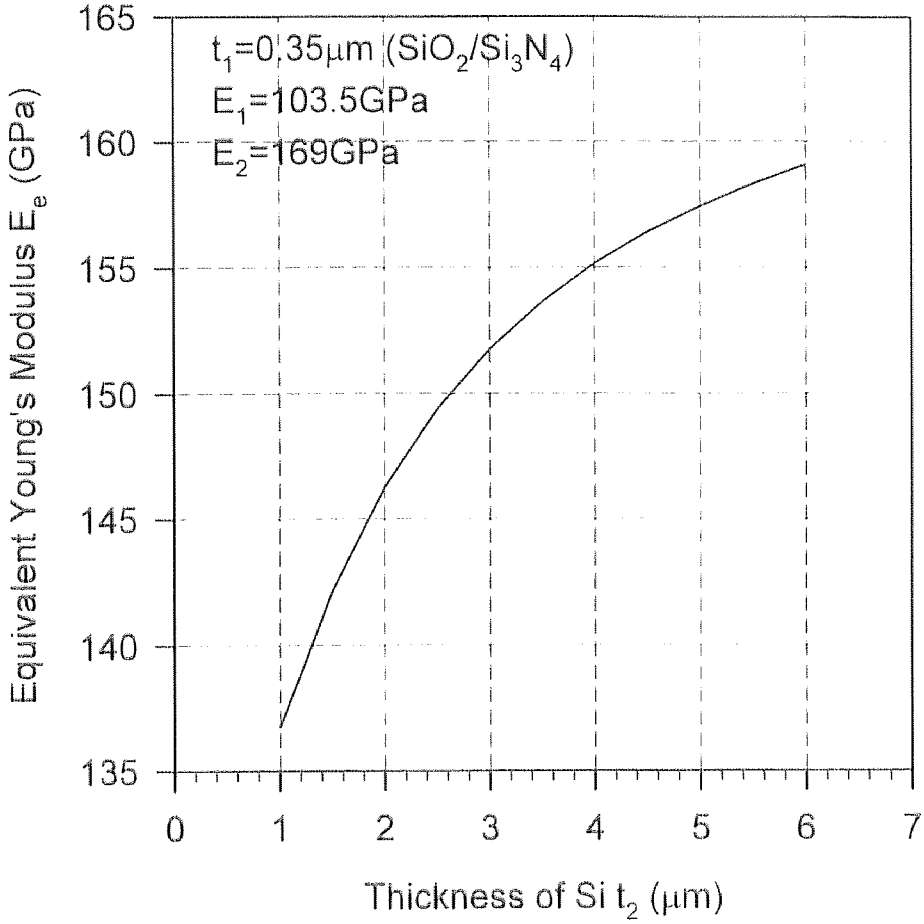


Figure 2.5 Equivalent Young's modulus as the function of thickness of Si

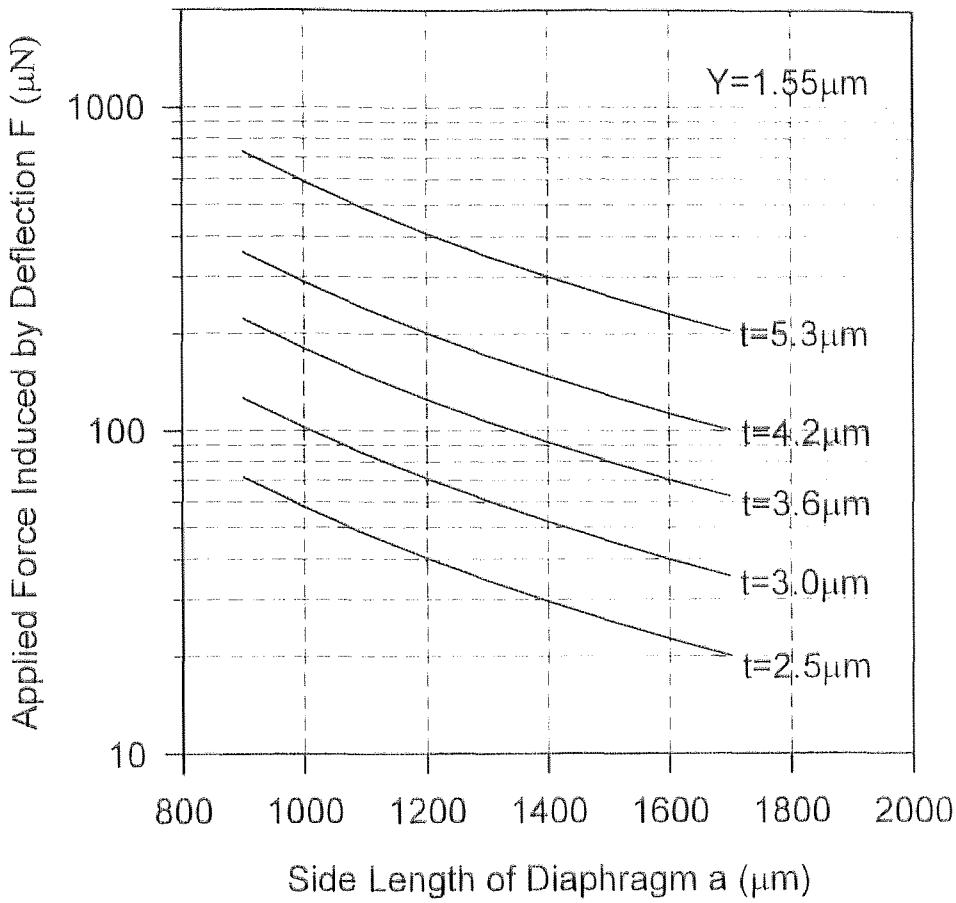


Figure 2.6 Applied forces as the function of side length of diaphragm for the deflection Y=1.55μm

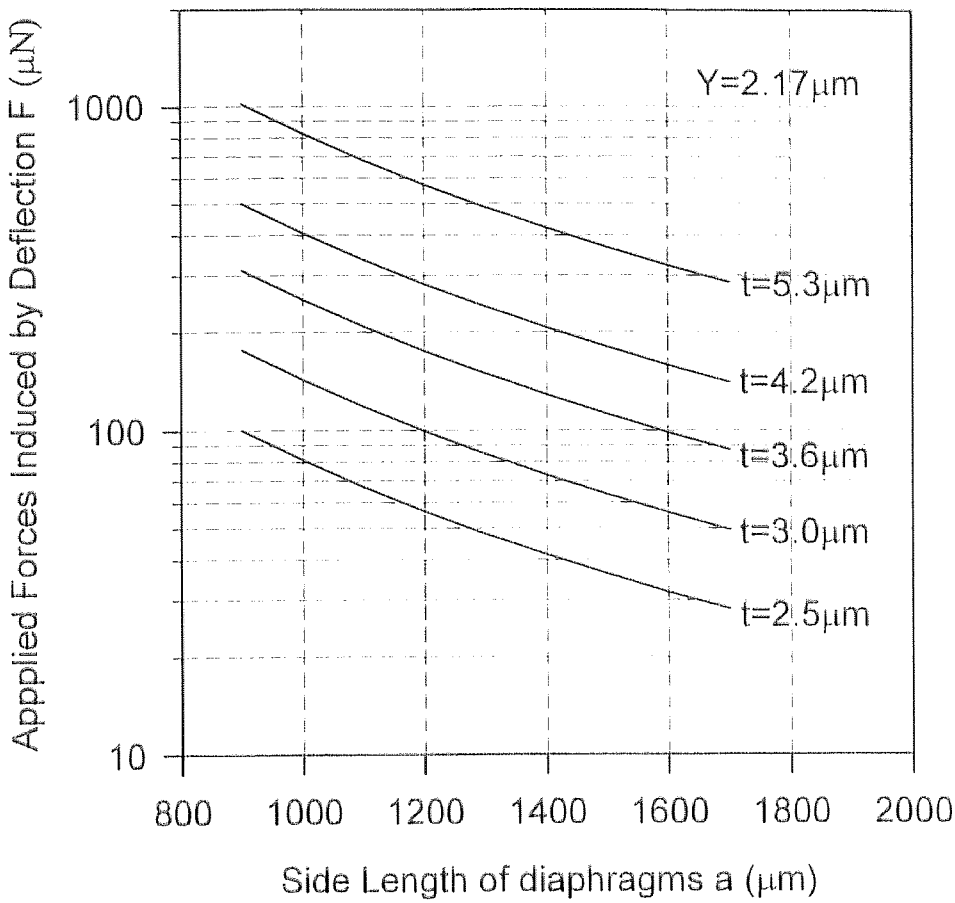


Figure 2.7 Applied forces as the function of side length of diaphragm for the deflection Y=2.17μm

2.1.4 Flat Error Estimation

When wafer A and wafer B mate together, the curved diaphragm will induce a small space Δd at the center of the diaphragm as illustrated schematically in Figure 2.8. The relation of Δd with dimension parameters of diaphragm and pedestal can be derived as follow:

$$R\vartheta_2 = a/2 \tag{2.6}$$

$$h_B + \Delta d = R - R\cos\vartheta_2 \tag{2.7}$$

$$L_B = 2R\sin\vartheta_1 \tag{2.8}$$

$$\Delta d = R - R\cos\vartheta_1 \tag{2.9}$$

Substituting $\sin\vartheta \approx \vartheta$ and $\cos\vartheta \approx 1 - \vartheta^2/2$ into (2.7), (2.8) and (2.9), finally we obtain the flat error Δd as:

$$\Delta d = \frac{h_B}{\frac{a^2}{L_B^2} - 1} \tag{2.10}$$

The simulation results based on (2.10) are shown in Figure 2.9 and Figure 2.10 with the dimension parameters chosen from Table 2.1 and Table 2.2. We notice that the flat error Δd ranges from 10 Å to 200 Å with 200 Å as the worst case (a=1100μm, L_B=120 μm, h_B=1.67μm). Considering the roughness δt of the sputtered metal surface, we have Δd ≤ δt. From this we can conclude that the contacts between metal A and metal B are flat contacts.

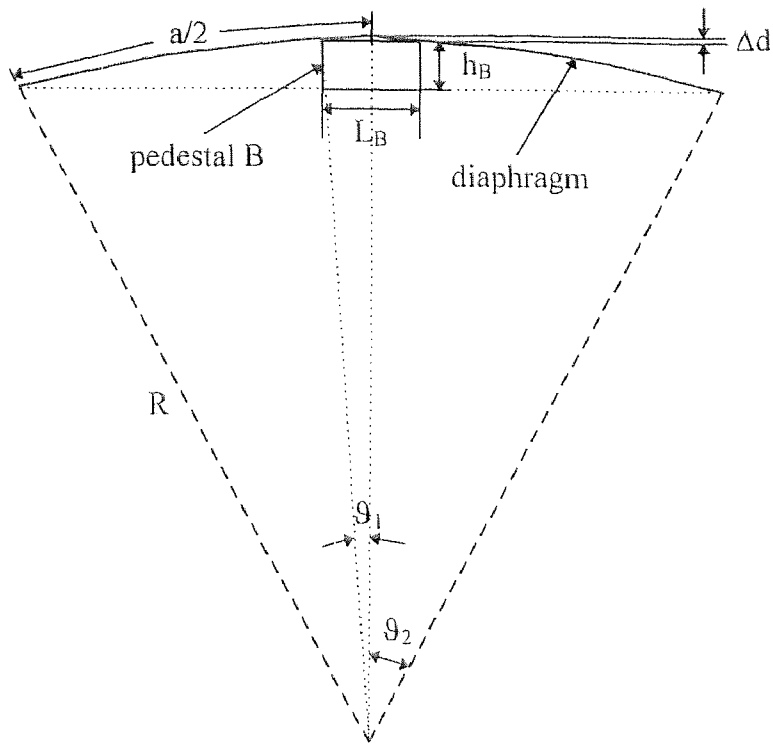


Figure 2.8 Schematic side view of the diaphragm forced by pedestal B

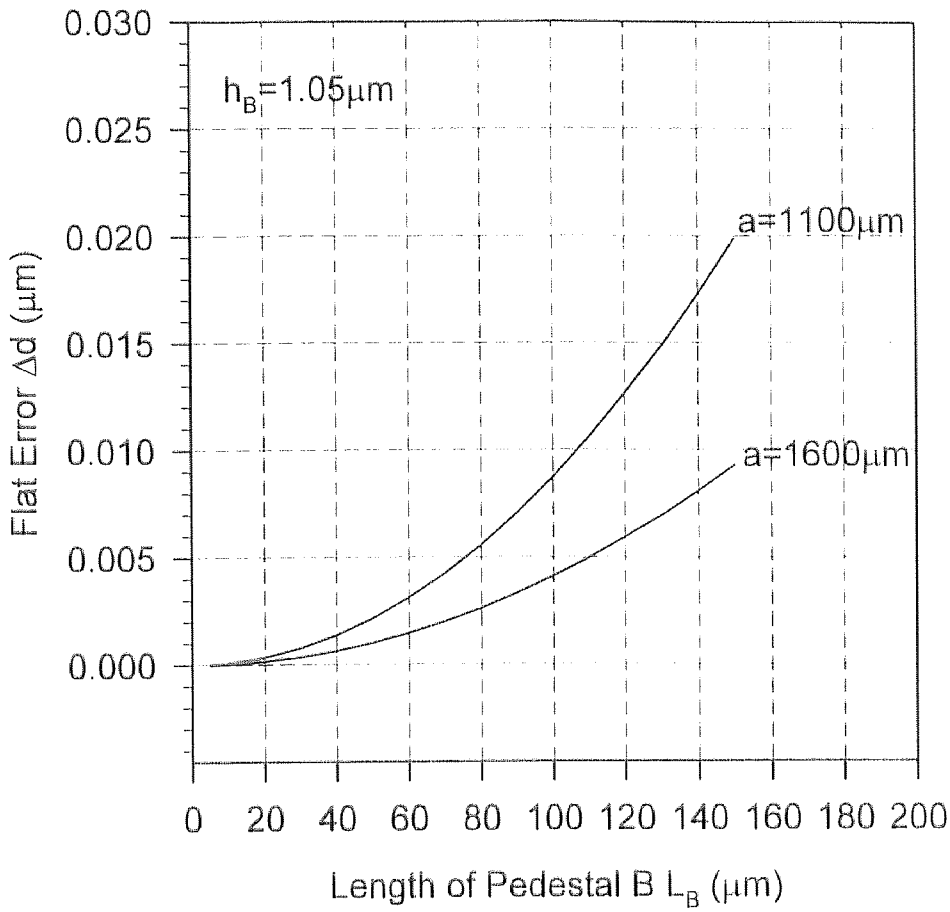


Figure 2.9 Flat error as the function of the length of pedestal for the height of pedestal h_B=1.05μm

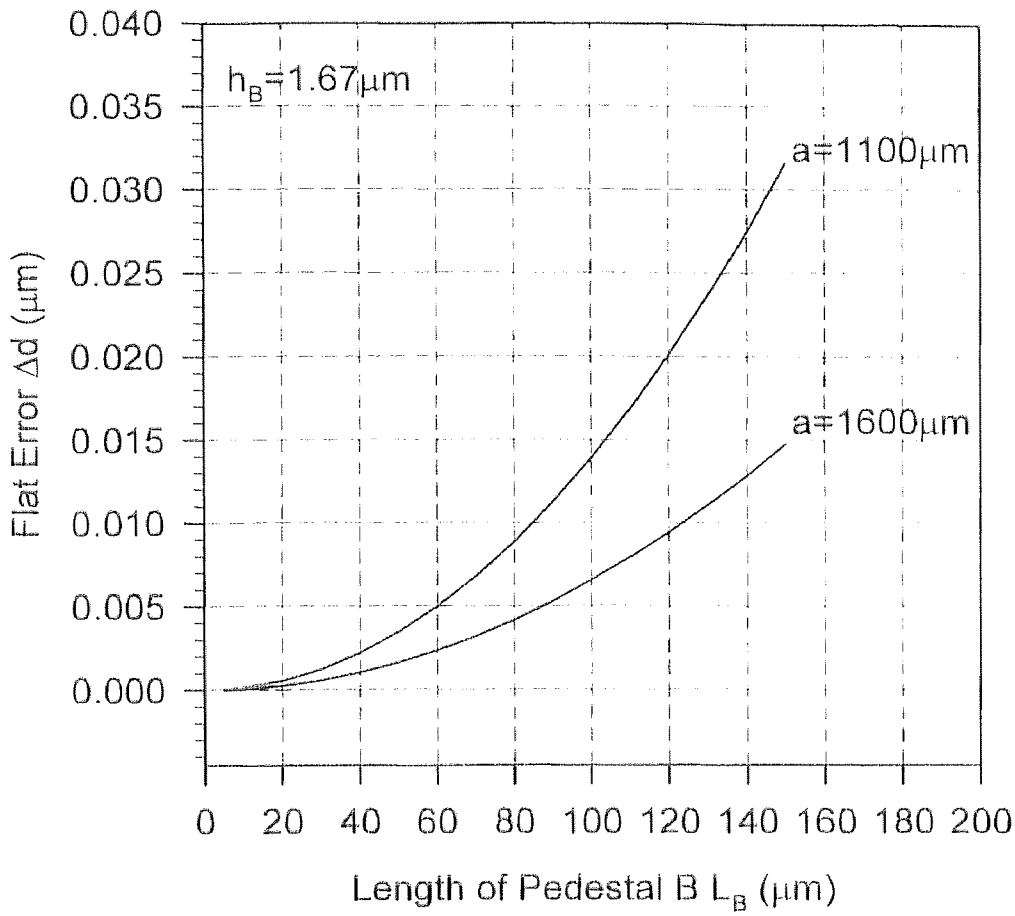


Figure 2.10 Flat error as the function of the length of pedestal for the height of pedestal h_B=1.67μm

2.2 Fabrication of Test Structure

The fabrication sequences are illustrated in Figure 2.11 for wafer A and Figure 2.12 for wafer B. The process begins with n-type (100) Si wafer. The steps are listed as follow:

Wafer A

1) wafer cleaning, photolithography (mask A1) and RIE Si (3~6 μm depth)
2) steam oxidation (8000 Å) and patterning (mask A2)
3) boron diffusion (1100°C, 1.5 hrs deposition, 6~8 hrs drive-in)
4) SiO_2 removal (6:1 BOE 20 min, 750°C O_2 1 hr, 6:1 BOE 20 min)
5) LPCVD Si_3N_4 (1500 Å) and LPCVD SiO_2 (2000 Å)
6) Pd sputtering (5000 Å) and patterning (mask A3)
7) backside photolithography (mask A4) and RIE SiO_2/Si_3N_4
8) KOH backside etching

Wafer B

1) wafer cleaning, photolithography (mask B1) and RIE Si (about 1~1.5 μm)
2) steam oxidation (3000 Å)
3) Pd sputtering (8000 Å) and patterning (mask B2)

The formation of diaphragms utilized the etch-stop function at the heavy boron-doping region in KOH solution [30, 31]. The ratio of etching rate for doped:undoped silicon is 1:10 at 42% KOH solution with temperature of 60°C when the doped boron concentration reaches $1 \times 10^{20} cm^{-3}$.

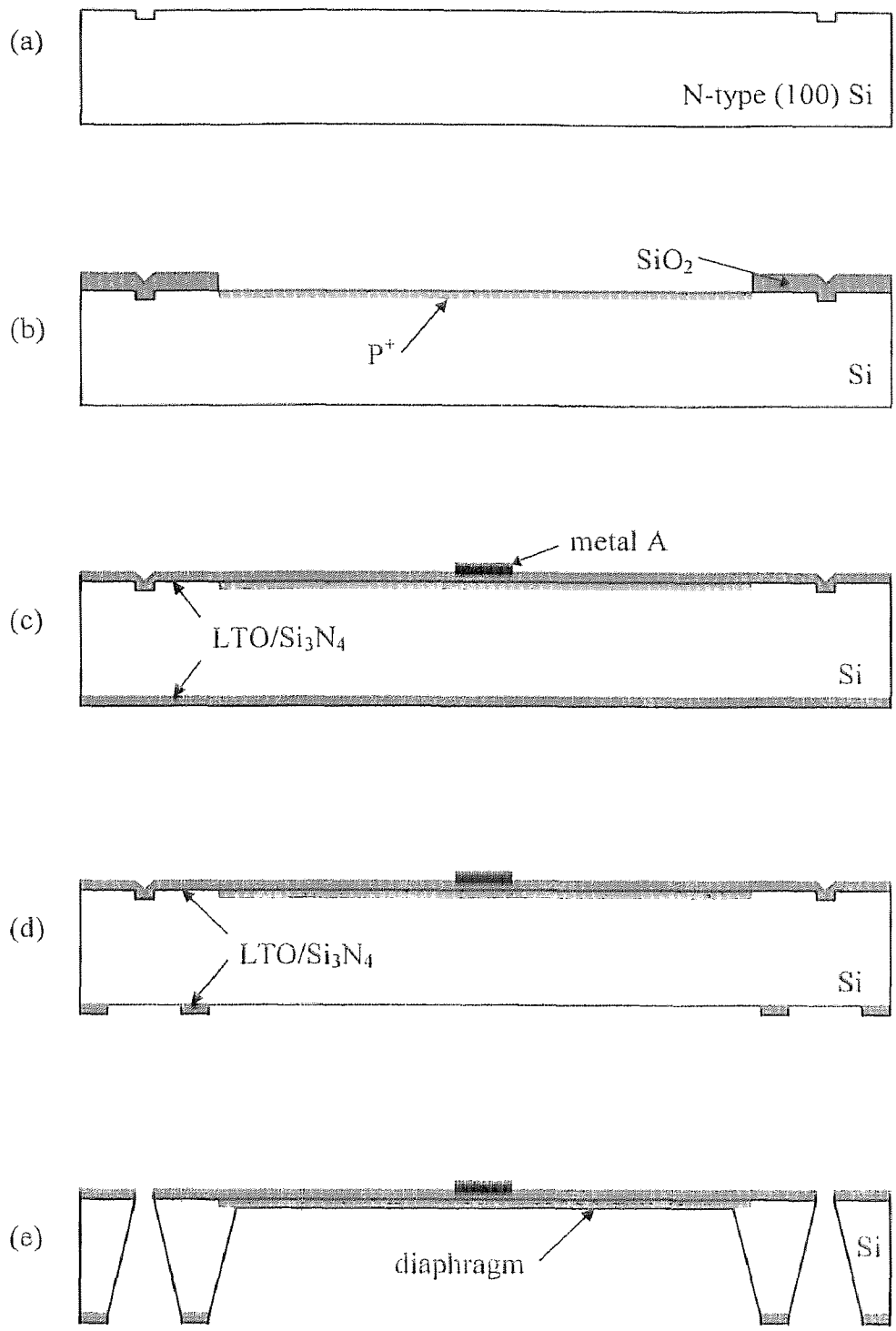


Figure 2.11 Process flow for wafer A

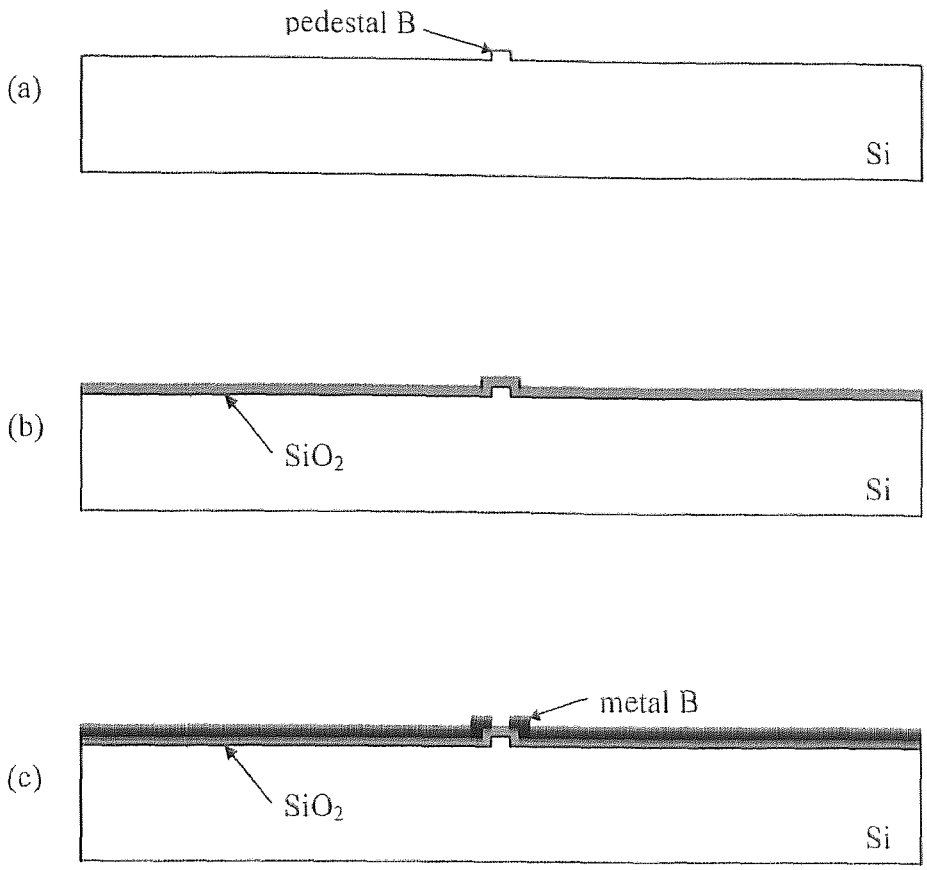


Figure 2.12 Process flow for wafer B

2.3 Experimental Results and Discussions

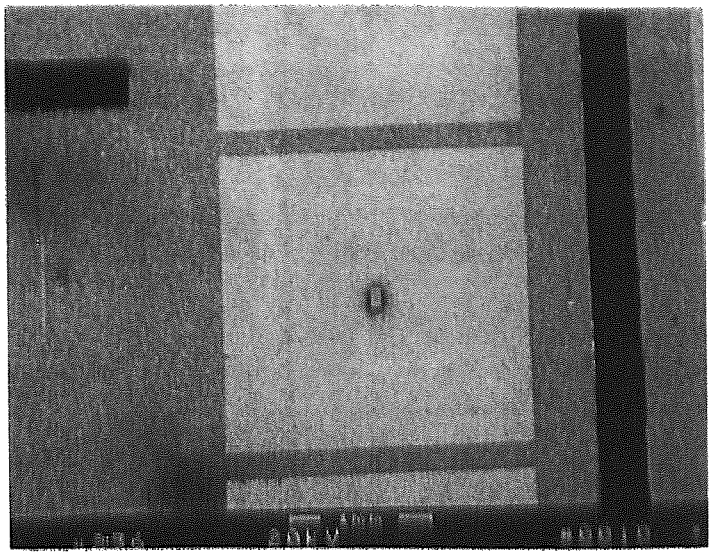
Figure 2.13 shows SEM pictures of wafer A with Pd metal on the center of the diaphragm and wafer B with a close view of pedestal B. The measured contact resistance R_c versus contact closure force F is plotted in Figure 2.14 for different contact areas with Pd-to-Pd contact. A threshold force F_t is required to provide the minimum contact resistance R_{mc}. For the experimental sample in Figure 2.14 with the contact areas of 100 μm^2, 900 μm^2 and 2500 μm^2 the threshold forces are 40 μN, 99 μN and 159 μN and the minimum contact resistances are 2.16 Ω, 1.41 Ω and 1.04 Ω, respectively (Table 2.3).

From the results it can been seen that the threshold force increases with contact area increasing and the larger contact area had the lower minimum contact resistance, that is, $F_{tc}>F_{tb}>F_{ta}$ and $R_{mc(c)}<R_{mc(b)}<R_{mc(a)}$. This phenomenon can be explained as follow: when two bodies are brought into contact under very low pressure they will touch first at isolated points whose dimensions are very small in relation to the dimensions of the bodies. The contact resistance is high and unstable at this time. As applied pressure is increased, the contact becomes more effective, owing to an increase in the number and size of the conducting regions. The contact resistance becomes low and stable then. For smaller contact area, a small force can make the contact surface reach its maximum effective contact area. While for larger contact area, a small force causes a much lower pressure than that in the small contact area case. Therefore a larger force is needed to obtain the maximum effective contact area and thus minimum stable contact resistance. Other factors which influence the value of minimum contact resistance include the kind of materials used for each contact member, the condition of the contact surfaces and the shape of the contact surfaces [32].

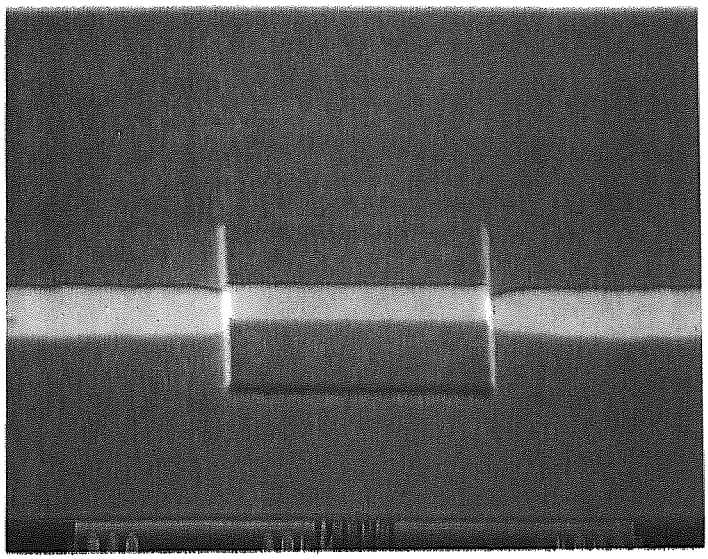
The measured breakdown current ranged from 600 mA to 800 mA. Figure 2.15 shows two SEM pictures of surface erosion after breakdown. The pits including ablation of the surface is due to the electrical discharge and the metal melting at the time of breakdown. Contact pitting and surface ablation caused by electrical discharge are primary factors correlating with the contact lifetime of the current carrying switch.

Table 2.3 Measured threshold forces and minimum contact resistances with different contact areas

	(a)	(b)	(c)
contact area (μm^2)	100	900	2500
threshold force F_t (μN)	40	99	159
minimum contact resistance (Ω)	2.16	1.41	1.04



(a) wafer A with Pd metal on the center of the diaphragm



(b) wafer B with a close view of pedestal

Figure 2.13 SEM pictures of (a) wafer A and (b) wafer B

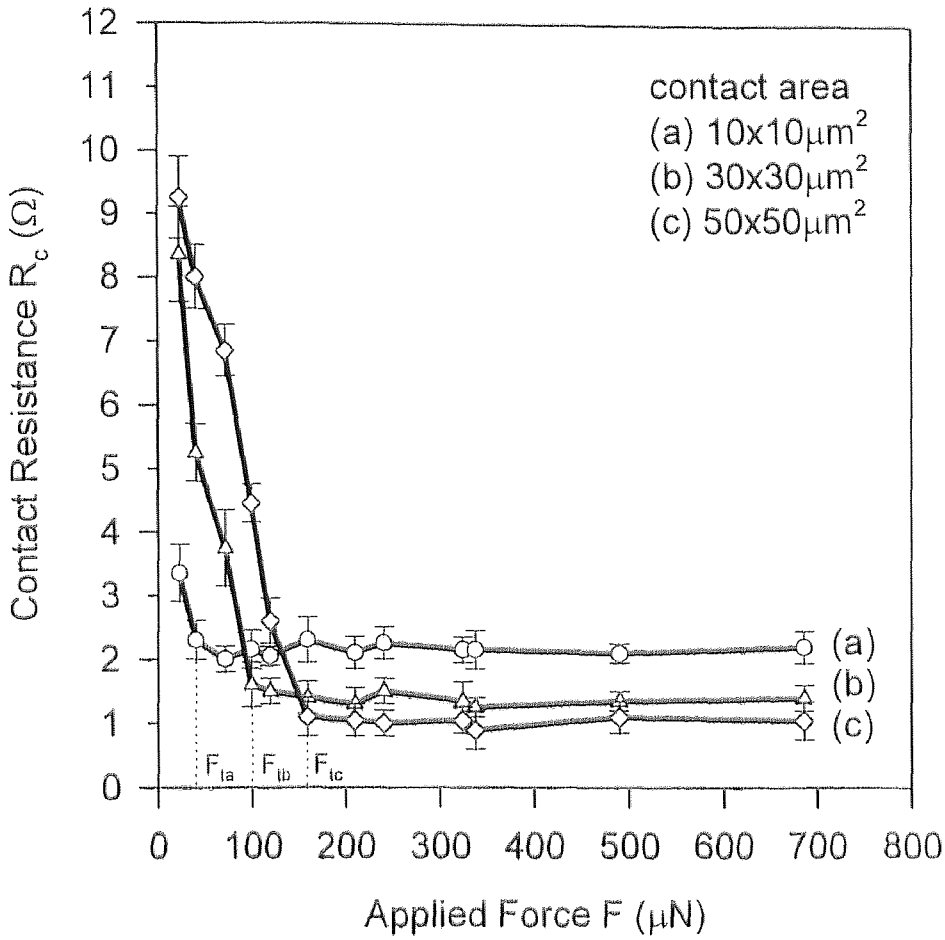
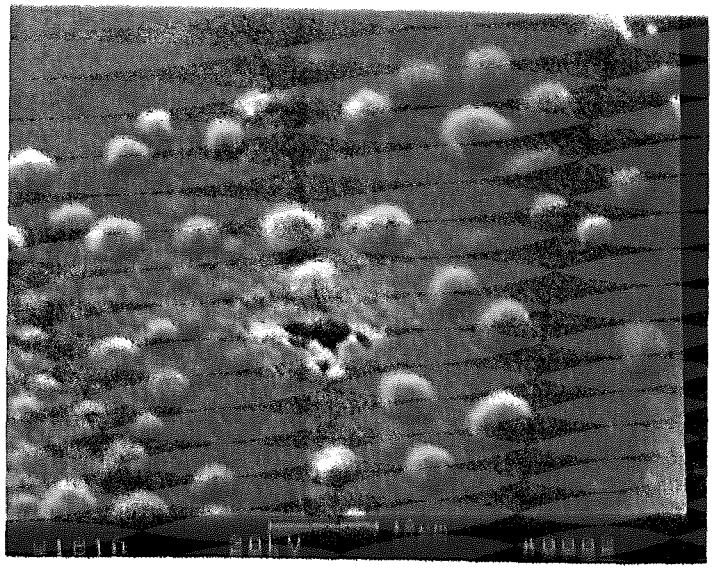


Figure 2.14 Measured contact resistance as the function of applied force with contact area of (a) 100 μm^2, (b) 900 μm^2 and (c) 2500 μm^2



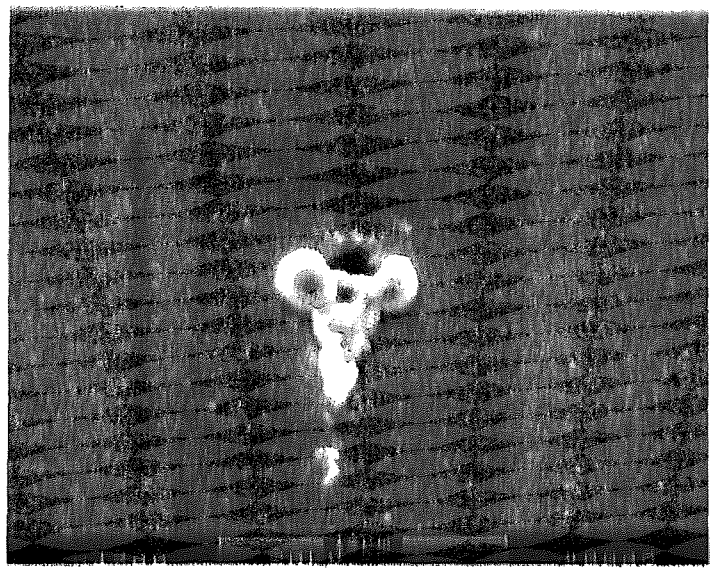


Figure 2.15 SEM pictures of surface erosion of contact metals

CHAPTER 3

DESIGN AND SIMULATION OF MICRORELAYS

Microrelays reported by other researchers have two actuation modes, one is electrostatically actuated, the other is electromagnetically actuated. Both of them have some inherent advantages but also limitations. The microrelays driven by the electrostatic mechanism need higher actuation voltage. The complicated fabrication process and large chip area restrict the application of microrelays driven by electromagnetic mechanism. To solve these limitations, a new type microrelay with combined thermal and electrostatic actuation was developed and is described in this chapter. In addition to its small chip area, this microrelay with new operation mode provided an optimum match for applied voltage and power consumption, electrical contact force, and switching speed.

3.1 Design of Microrelays

3.1.1 Concept of Microrelays Operation

The microrelay is schematically shown in Figure 3.1. The microrelays were designed using a suspended bimorph cantilever beam. Upon release, the cantilever buckles upwards naturally in an open state because of the difference of thermal expansion coefficients of two layers as illustrated in Figure 3.2 (a). For transition to a closed state, a thermal voltage V_a is applied first to the cantilever. When the cantilever is heated, the upper layer which has a larger thermal expansion coefficient will expand more than the lower layer, causing the cantilever to bend downwards. By controlling the voltage value V_a, we can make the cantilever stay in the flat position as shown in Figure 3.2 (b). A

electrostatic voltage V_b is then added to provide sufficient pull-down and clamping force to reach the fully closed state in Figure 3.2 (c). Thus a low electrical contact resistance is obtained.

The movement of the cantilever can also be implemented by applying either thermal voltage or electrostatic voltage only. The combined thermal and electrostatic actuation mechanism is used instead of separate thermal and electrostatic drive because thermal actuation cannot create the sufficient force needed to obtain low contact resistance and electrostatic actuation alone requires a voltage excessively high to achieve the closed state. The detailed analysis will be given in section 3.2.

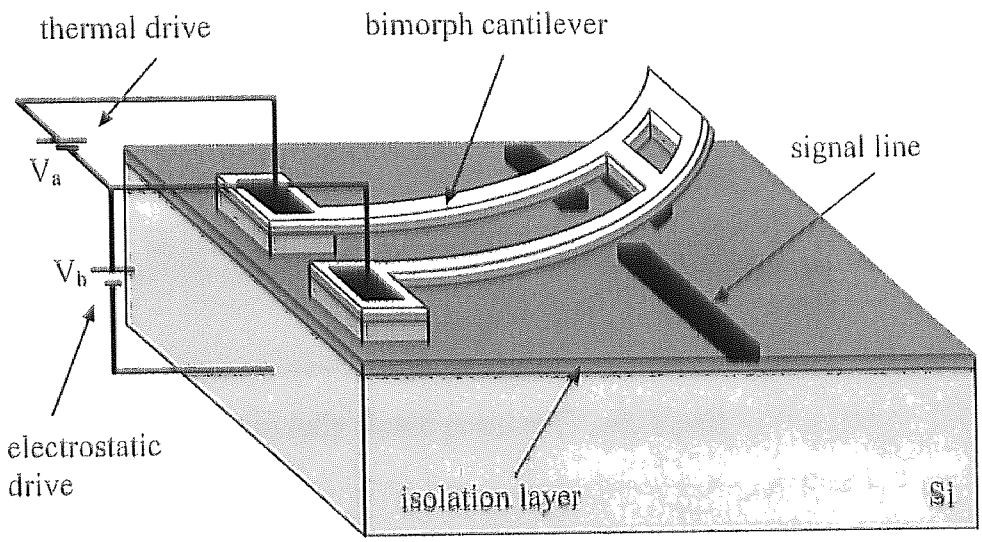
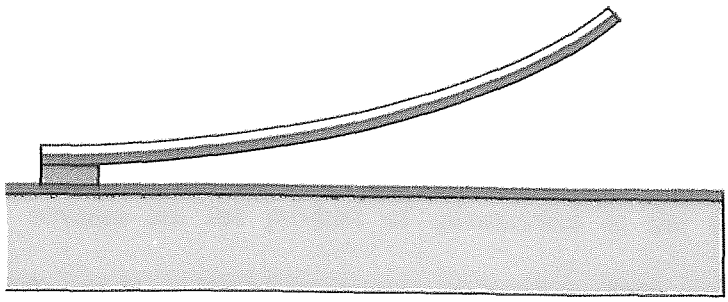
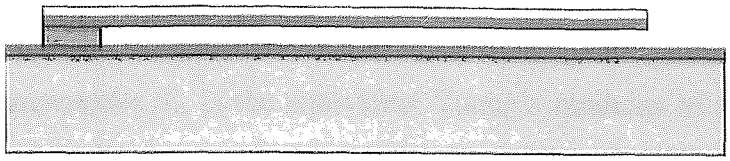


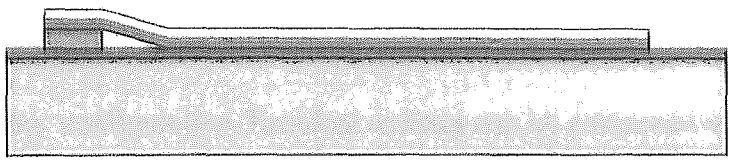
Figure 3.1 A schematic view of the microrelay



(a) initial buckled upwards position (V_a=0, V_b=0)



(b) intermediate partially actuated position ($V_a \neq 0$, V_b=0)



(c) fully closed position ($V_a \neq 0$, $V_b \neq 0$)

Figure 3.2 Actuation sequence illustration

3.1.2 Physical Design

The thermal actuation of bimorph cantilever is based on the stray stresses of the films. Stray stresses are stresses that are present in the absence of external forces. There are two sources of stray stresses. One is the thermal stress σ_{th}, the other is the residual stress $\sigma_{residual}$ [33].

Thermal stresses are the product of mismatches in the thermal expansion coefficients of different films. For bimorph structure, we have [34]:

$$\sigma_{th} = (\alpha_u - \alpha_l) \cdot \Delta T \cdot E_e \tag{3.1}$$

where α_u and α_l are thermal expansion coefficients of the upper layer film and the lower layer film, respectively. ΔT is the difference of the film growth temperature and the measurement temperature. E_e is the equivalent Young's modulus of the films which is given by the expression (2.5). The σ_{th} can be of either sign (positive is tensile, negative is compressive), based on the relative values of α_u and α_l. If $\alpha_u > \alpha_l$, the bimorph structure will bend upwards upon release.

Residual stresses develop because as-deposited thin film are not in the most favorable energetic configuration. Residual stresses can be compressive, which makes the film expand, or tensile, which makes the film shrink. Residual stresses can be relaxed by high-temperature anneals; however, the anneal temperature are quite high and may not be practical for the production of micromechanical devices.

In the design of the microrelay, we do not expect the large initial stress which will cause large initial bending of the released cantilever and thus consume more power to move the cantilever down to the flat position. With this consideration and the process

restriction, we chose $TaSi_2$ as the upper layer film and SiO_2 as the lower layer film to consist of the bimorph cantilever. The thermal expansion coefficients of $TaSi_2$ and SiO_2 are 8.8×10^{-6}/K and 0.4×10^{-6}/K [34], respectively.

Figure 3.3 shows a side view of the microrelay structure. The microrelay was designed to use a suspended $TaSi_2/SiO_2$ bimorph cantilever beam, a gold-to-gold electrical contact, aluminum as sacrificial layer, and $LTO/Si_3N_4/SiO_2$ composite layer as the isolation layer. The $TaSi_2$ layer serves as both the heater for thermal actuation and the upper electrode for electrostatic actuation. The actuated tip of the cantilever contains an extended area which was designed to get symmetric electrostatic force at the electrical contact area and thus the low contact resistance.

Figure 3.4 shows the top views of two different structures of microrelays. Structure 2 contains more extended area than structure 1 so that it will obtain more electrostatic force under the same applied voltage. Another difference of two types of structures is the connection of the electrical contact. Structure 2 has two contact resistance in parallel for the purpose of reducing the value of contact resistance.

Table 3.1 lists the geometry parameters of two structures of microrelays. The choice of the different widths of cantilever beams is for the control of the release process. The different lengths of cantilever beams will cause the different combinations of applied voltage and power consumption for microrelays actuation.

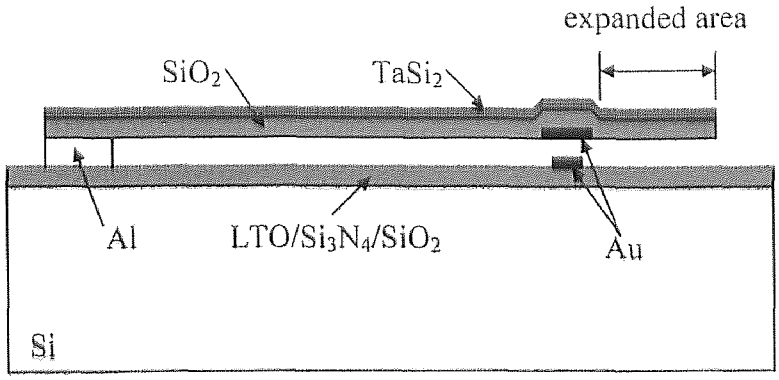
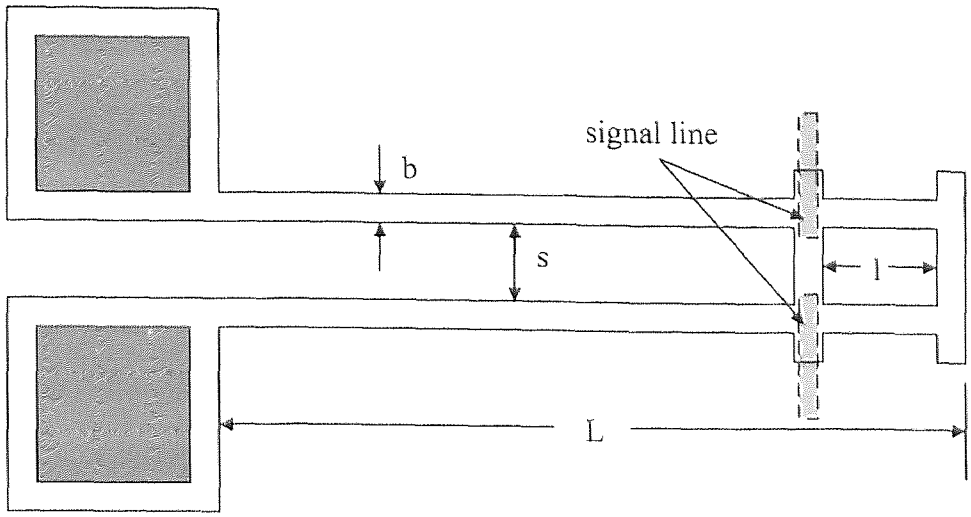
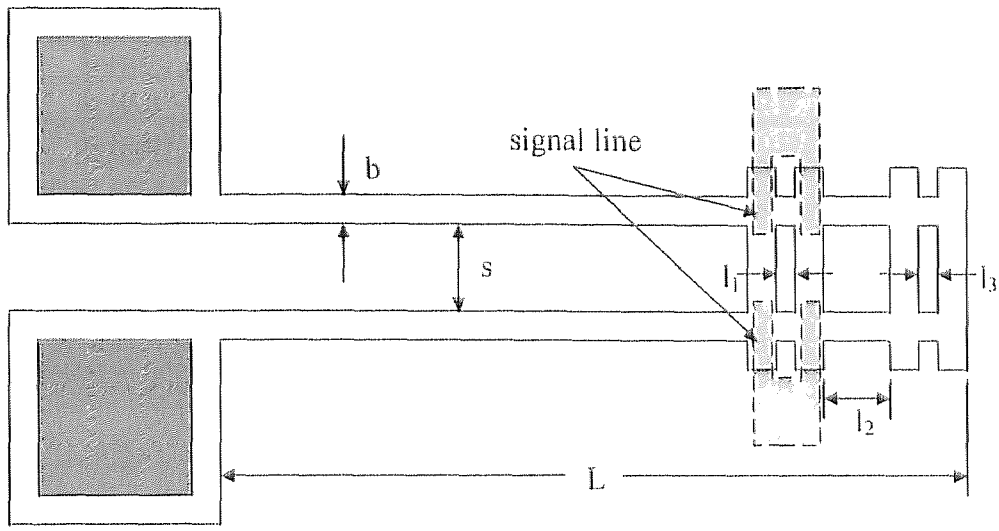


Figure 3.3 A schematic view of the cross section of the microrelay



(a) Structure 1



(b) Structure 2

Figure 3.4 Schematic top views of two different structures of microrelays

Table 3.1 Geometry parameters of microrelays

	Structure 1	Structure 2	
	relay 1	relay 2	relay 3
b (μm)	14	14	16
L (μm)	278	278	328
s (μm)	16	16	16
l (μm)	37	—	—
l_1 (μm)	—	10	10
l_2 (μm)	—	17	30
l_3 (μm)	—	6	8
contact area (μm^2)	200	290	340

3.2 Modeling and Simulation of Microrelays

3.2.1 Analysis of Electrostatically Actuated Curved Cantilever

In this subsection, we will analyze the actuation of the initially curved beam which is driven by electrostatic mechanism only. Figure 3.5 illustrates the actuation sequence of the cantilever.

For a beam in pure bending as shown in Figure 3.5 (a), the deflection profile of the cantilever can be written as:

$$w_0(x) = H + \delta \cdot \left(\frac{x}{L}\right)^2 \tag{3.2}$$

where H is the height of the anchor, δ is the maximum distance between the curved cantilever and the isolation layer, L is the length of the cantilever.

When a voltage V is applied between the upper layer of cantilever beam and the substrate as shown in Figure 3.5 (b), the electrostatic force will pull down the beam to the substrate. The fully closed position is obtained upon applied voltage exceeding threshold voltage, that is $V>V_{th}$ as shown in Figure 3.5 (c).

To obtain the value of V_{th}, we use a simplified model based on the method of total potential energy using small deflection theory, e.g. the Rayleigh-Ritz method, where an approximate solution to the differential equation is constructed in the form of admissible trial functions [35, 36]. The total potential energy, denoted by Π, can be expressed as:

$$\Pi = U_m + U_e \tag{3.3}$$

where U_m and U_e are the strain energy of bending and the potential energy of the electrostatic force given by:

$$U_m = \frac{EI}{2}\int_0^L \left\{\frac{d^2\left[w(x)-w_0(x)\right]}{dx^2}\right\}^2 dx \tag{3.4}$$

and

$$U_e = -\frac{1}{2}\int_0^L \frac{\varepsilon_0 b V^2}{\frac{d}{\varepsilon}+w(x)}\,dx \tag{3.5}$$

where EI is the bending stiffness, ε_0 is the permittivity in vacuum, ε is the dielectric constant of the insulator, b is the width of the cantilever beam, d is the thickness of the insulator, V is the drive voltage.

For the admissible trial function of the deflection profile of the cantilever beam, the deflection profile of a uniformly loaded cantilever beam has been used [37]:

$$w(x) = H + Ax^2\left(x^2 - 4Lx + 6L^2\right) \tag{3.6}$$

where A is a constant that has to be determined..

The system is in equilibrium when the first variation of the potential energy with respect to the constant A equals zero. Whether this equilibrium is stable or unstable is determined by the second variation of the potential energy with respect to A. At the transition from a stable to an unstable equilibrium the first and the second derivative of the potential energy with respect to A are zero:

$$\frac{\partial \Pi}{\partial A} = 0 \tag{3.7}$$

$$\frac{\partial^2 \Pi}{\partial A^2} = 0 \tag{3.8}$$

Solving equations (3.2) ~ (3.8) with the parameters of table 3.2, the threshold voltage V_{th} which is needed to pull down the cantilever to the substrate is shown in Figure 3.6 as the function of δ with different cantilever length.

Table 3.2 Parameters of the cantilever

permittivity in vacuum	$\varepsilon_0 = 8.854 \times 10^{-12}$ F/m
dielectric constant of the insulator	$\varepsilon = 3.8$
Young's modulus	E = 107 GPa
thickness of the cantilever	t = 2.0 μm
thickness of the insulator	d = 2.3 μm
height of the anchor	H = 2.0 μm
thickness of the lower contact metal	h=0.8 μm

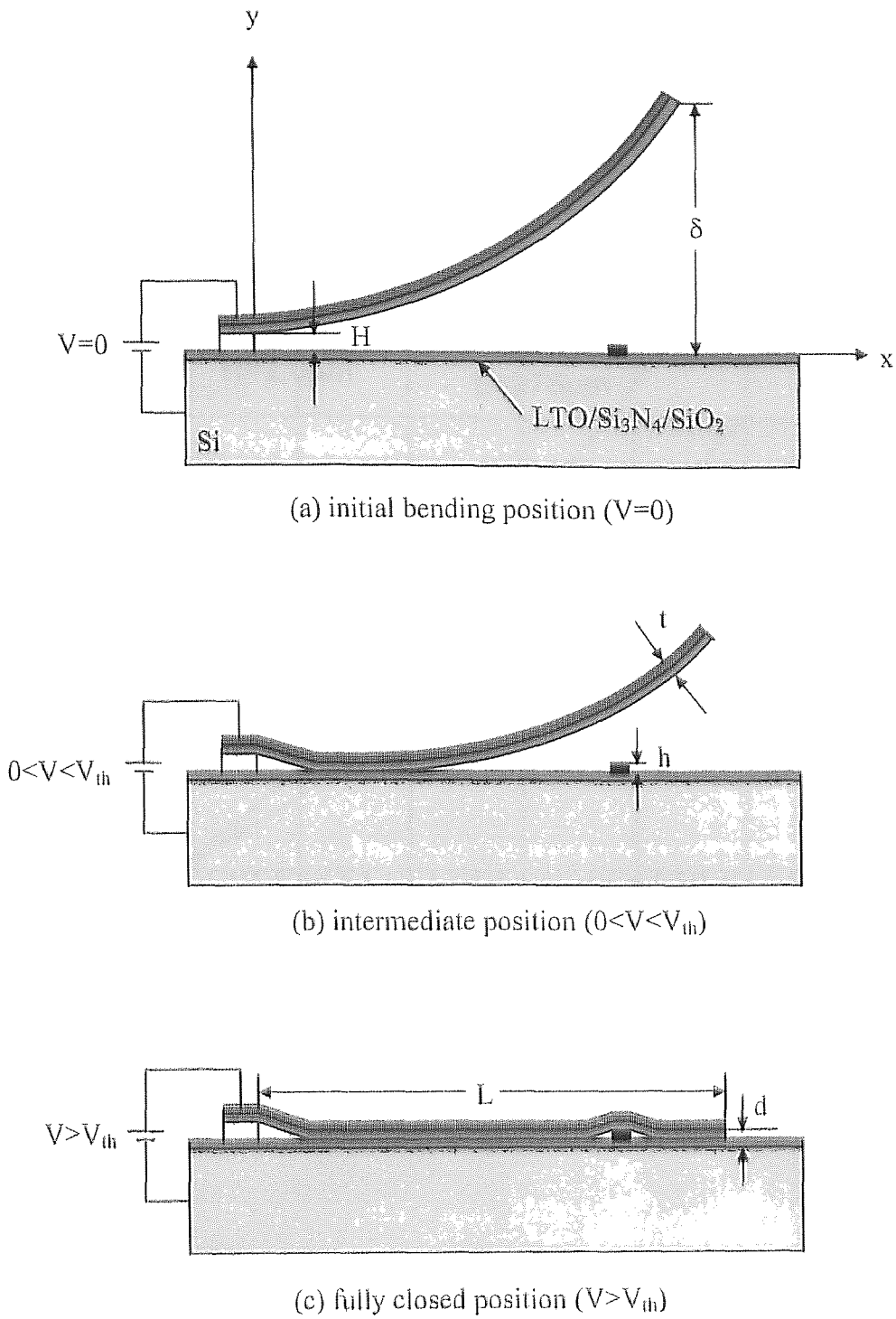


Figure 3.5 Actuation sequence of the cantilever driven by electrostatic force

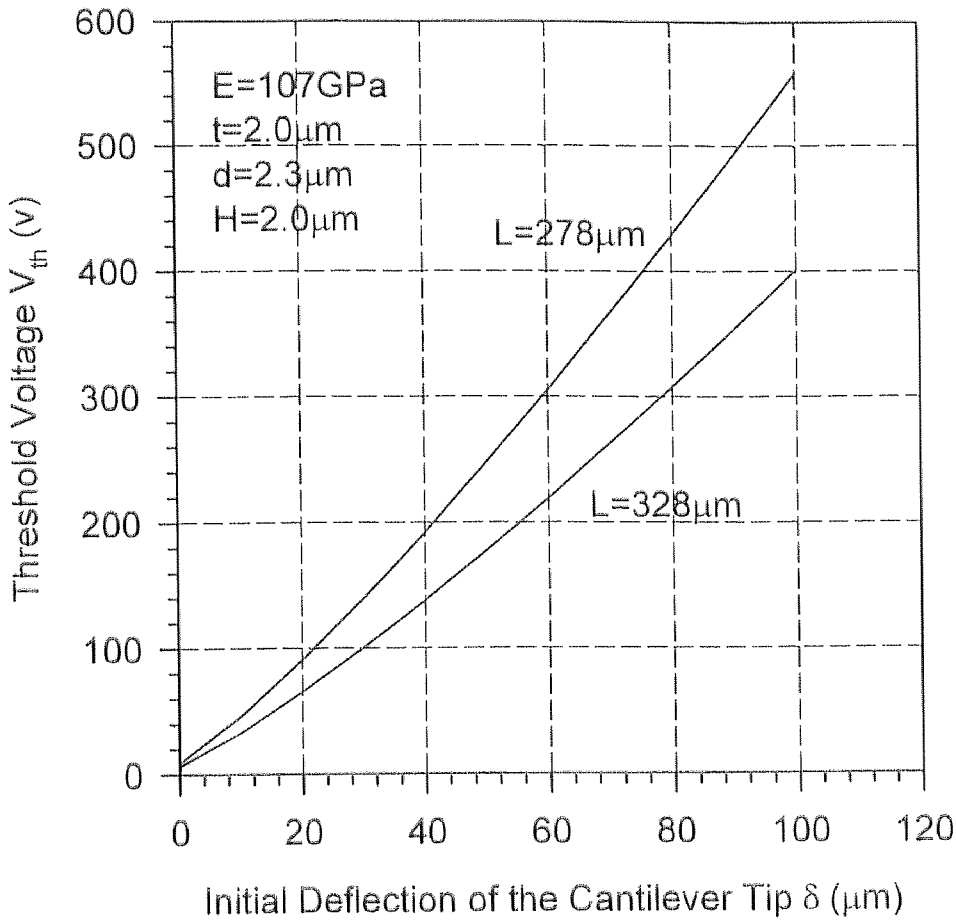


Figure 3.6 Threshold voltage as the function of initial deflection

3.2.2 Analysis of Thermally Actuated Curved Cantilever

For an initially curved bimorph cantilever with one end fixed and another end free, a flat state can be obtained through increasing the temperature of the cantilever beam. When the cantilever is heated, the upper layer which has a large thermal expansion coefficient will expand more than the lower layer, causing the cantilever to a flat position at a certain temperature t_w as shown in Figure 3.7. For an initially curved beam with its maximum deflection of δ at the free end, the temperature change ΔT which is required for transition to a flat state can be expressed as [38]:

$$\Delta T = \frac{\delta}{L^2} \cdot \frac{\left(b_1 E_1 t_1^2\right)^2 + \left(b_2 E_2 t_2^2\right)^2 + 2 b_1 b_2 E_1 E_2 t_1 t_2 \left(2t_1^2 + 3t_1 t_2 + 2t_2^2\right)}{3 b_1 b_2 E_1 E_2 t_1 t_2 \left(t_1 + t_2\right)\left(\alpha_1 - \alpha_2\right)} \tag{3.9}$$

where E_1 and E_2 are Young's modulus, b_1 and b_2 are width of the cantilever, t_1 and t_2 are thickness of the cantilever, for upper and lower layer, respectively. When b_1=b_2, the expression (3.9) can be reduced to:

$$\Delta T = \frac{\delta}{L^2} \cdot \frac{\left(E_1 t_1^2\right)^2 + \left(E_2 t_2^2\right)^2 + 2 E_1 E_2 t_1 t_2 \left(2t_1^2 + 3t_1 t_2 + 2t_2^2\right)}{3 E_1 E_2 t_1 t_2 \left(t_1 + t_2\right)\left(\alpha_1 - \alpha_2\right)} \tag{3.11}$$

With the parameters chosen from table 3.3, the temperature change ΔT as the function of δ for the different cantilever length L is shown in Figure 3.8. As a comparison, the curves obtained from ANSYS analysis also are plotted in Figure 3.8.

Table 3.3 Parameters of the bimorph cantilever

$TaSi_2$	SiO_2
E_1 = 175 GPa	E_2 = 74 GPa
t_1 = 0.5 μm	t_2 = 1.5 μm
α_1 = 8.8 x 10^{-6} /K	α_2 = 0.4 x 10^{-6} /K

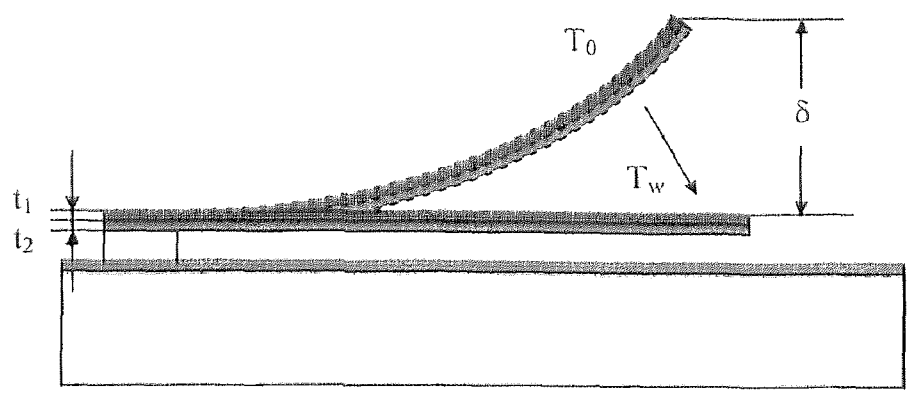


Figure 3.7 A schematic view of the bimorph cantilever transition from the curved state ($T=T_0$) to the flat state ($T=T_w$)

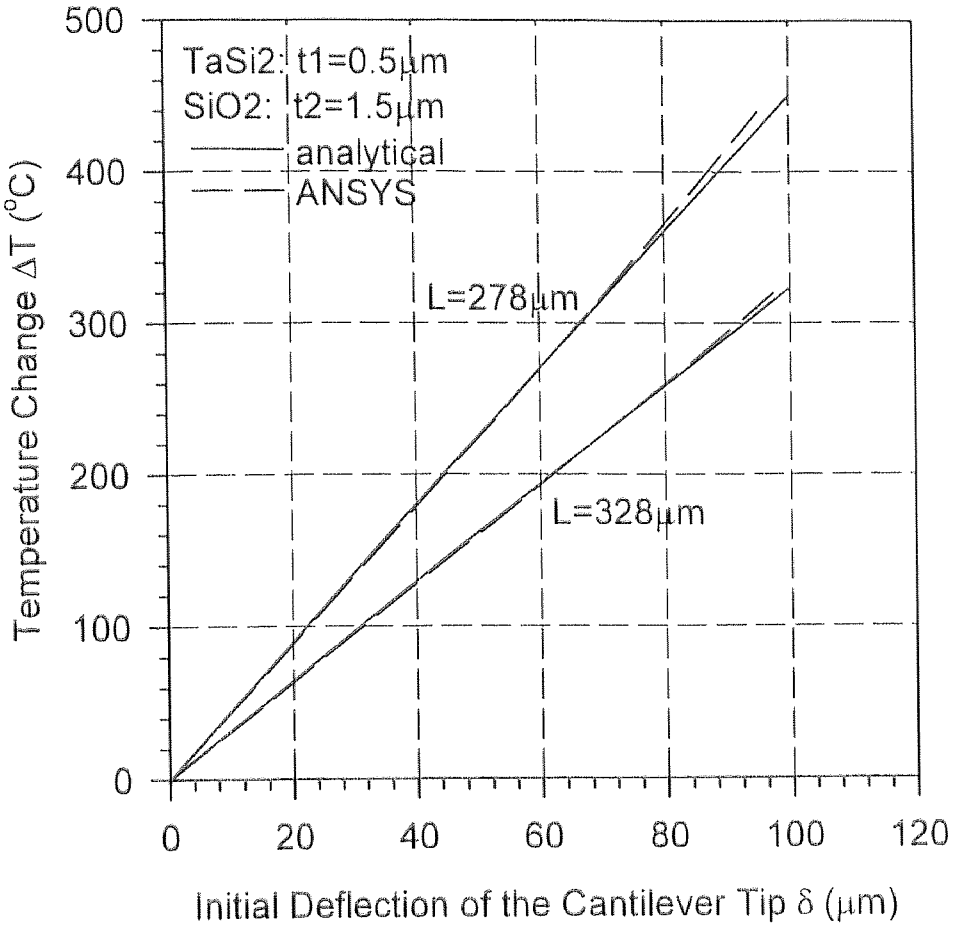


Figure 3.8 Temperature change as the function of initial deflection of the cantilever

Combining the results of Figure 3.6 and Figure 3.8, we can give threshold voltage needed to pull down the cantilever as the function of temperature change of the cantilever, as shown in Figure 3.9 for the initial tip deflection of δ_0=50 μm.

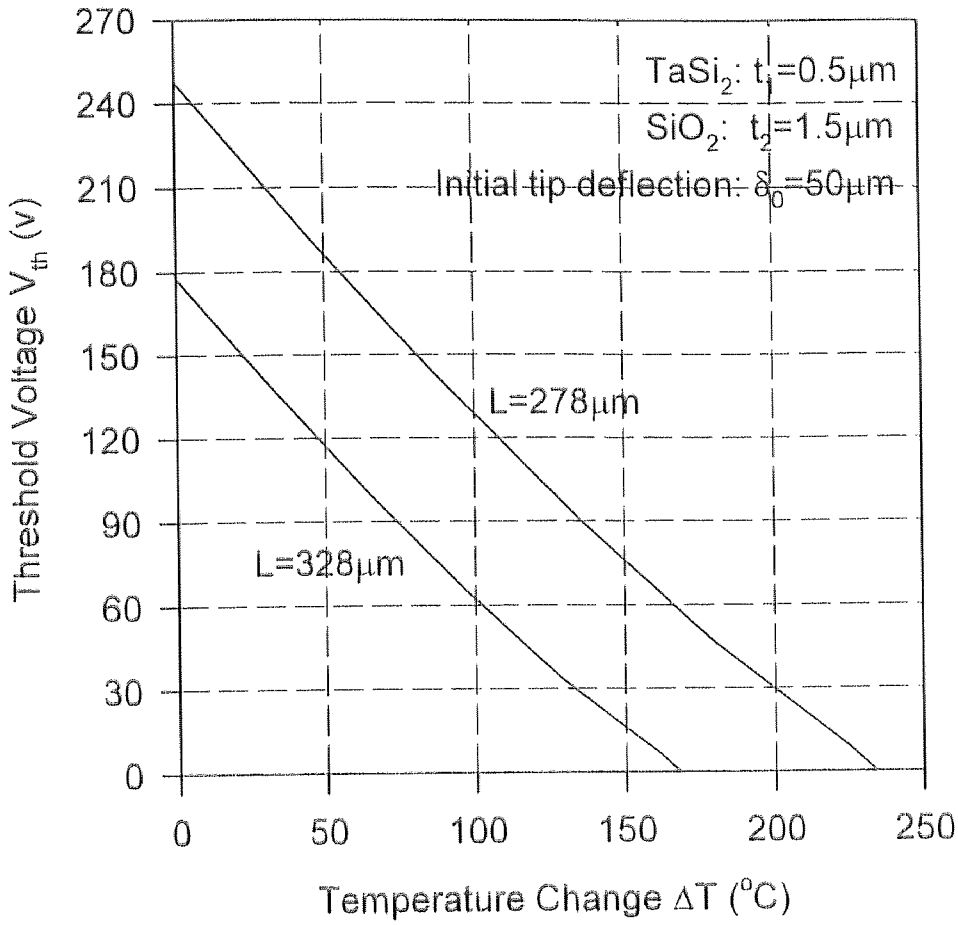


Figure 3.9 Threshold voltage as the function of temperature change of the cantilever in the combined thermal and electrostatic actuation

When current passes through the resistor which consists of $TaSi_2$ film, Joule heat will cause its temperature rising. All the power generated in the resistor will be dissipated by heat conduction and heat convection when system is in equilibrium. Assuming the temperature of $TaSi_2$ resistor on the cantilever beam is T_w, we can classify the heat flow into three parts as shown in Figure 3.10(a): (1) heat conduction to the anchor q_1; (2) free-convection of upper surface of $TaSi_2$ layer q_2; (3) heat conduction to SiO_2 layer and free-convection of lower surface of SiO_2 layer q_3. Because the mean free path of gas molecule at atmosphere pressure is less than 0.1 μm and much more smaller than the gap distance of 2 μm, we can still consider that the heat flow of the lower surface of SiO_2 layer to be the free-convection. The power consumption P can be written as [39]:

$$P = 2\left(q_1 + q_2 + q_3\right) \tag{3.12}$$

and

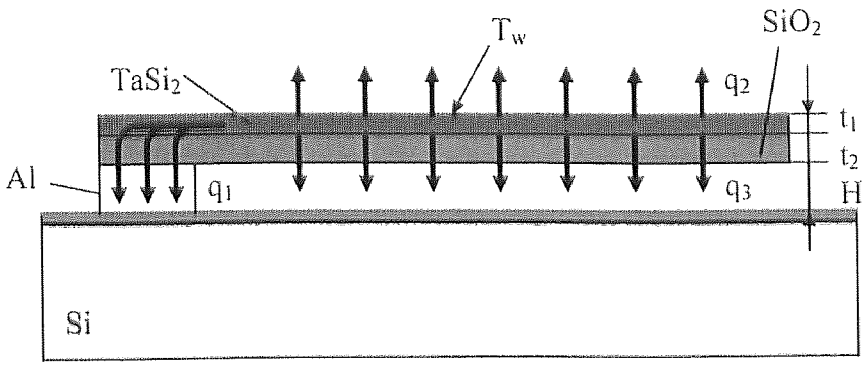
$$q_1 = \frac{T_w - T_0}{\dfrac{n}{K_1 t_1} + \dfrac{t_2}{K_2 A_1} + \dfrac{H}{K_3 A_1}} \tag{3.13}$$

$$q_2 = h_1 A_2 \left(T_w - T_0\right) \tag{3.14}$$

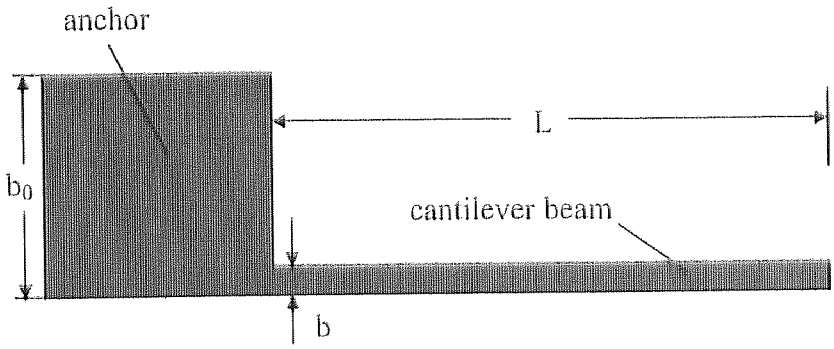
$$q_3 = \sqrt{h_2 p K_2 A_2}\left(T_w - T_0\right) \cdot \frac{\sinh mL + \left(\dfrac{h_2}{mK_2}\right)\cosh mL}{\cosh mL + \left(\dfrac{h_2}{mK_2}\right)\sinh mL} \tag{3.15}$$

where T_0 is the room temperature, K is the thermal conductivity, h is the convection heat-transfer coefficient, A is the interface area, H is the height of the anchor, p is the perimeter of the cantilever, L is the length of the cantilever, and $m = \sqrt{h_2 p / K_2 A_2}$. The constant n is determined by ratio of b_0 to b, where b_0 is the side length of the anchor and b

is the width of the cantilever as shown in Figure 3.10(b). The parameters used for calculation are listed in table 3.4. The power consumption as the function of the temperature change is shown in Figure 3.11. Combining the results from equation (3.11) and (3.12), the power consumption as the function of initial cantilever deflection is illustrated in Figure 3.12.



(a) side view of the cantilever



(b) top view of the cantilever and the anchor

Figure 3.10 A schematic view of the heat flow in the cantilever

Table 3.4 Parameters used in the heat flow calculations

thermal conductivity for $TaSi_2$	K_1	373 w/m·°C	
thermal conductivity for SiO_2	K_2	2.66 w/m·°C	
thermal conductivity for Al	K_3	202 w/m·°C	
heat transfer coefficient for upper surface of $TaSi_2$	$h_1 = 1.32\left(\frac{T_w - T_0}{L}\right)^{\frac{1}{4}}$	w/m^2·°C	
heat transfer coefficient for lower surface of SiO_2	$h_2 = 0.59\left(\frac{T_w - T_0}{L}\right)^{\frac{1}{4}}$	w/m^2·°C	
height of the anchor	H	2.0 μm	
thickness of $TaSi_2$ layer	t_1	0.5 μm	
thickness of SiO_2 layer	t_2	1.5 μm	
length of the cantilever	L	278 μm	328 μm
width of the cantilever	b	14 μm	16 μm
perimeter of the cantilever	$p = 2(L + b)$	584 μm	688 μm
constant	n	5.4	5.0
interface area of the anchor	$A_1 = b_0^2$	200 x 200 μm^2	
interface area of the beam	$A_2 = L \times b$	3892 μm^2	5248 μm^2

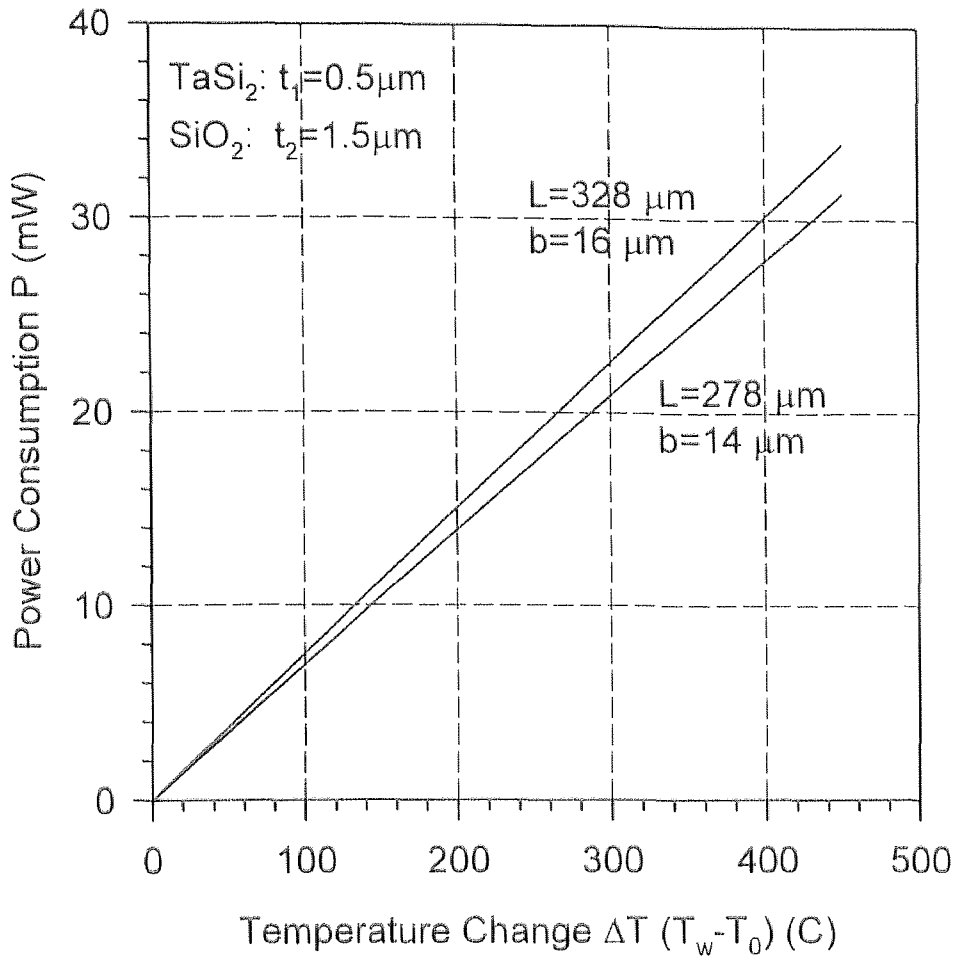


Figure 3.11 Power consumption as the function of the temperature change for bimorgh cantilever $TaSi_2/SiO_2$

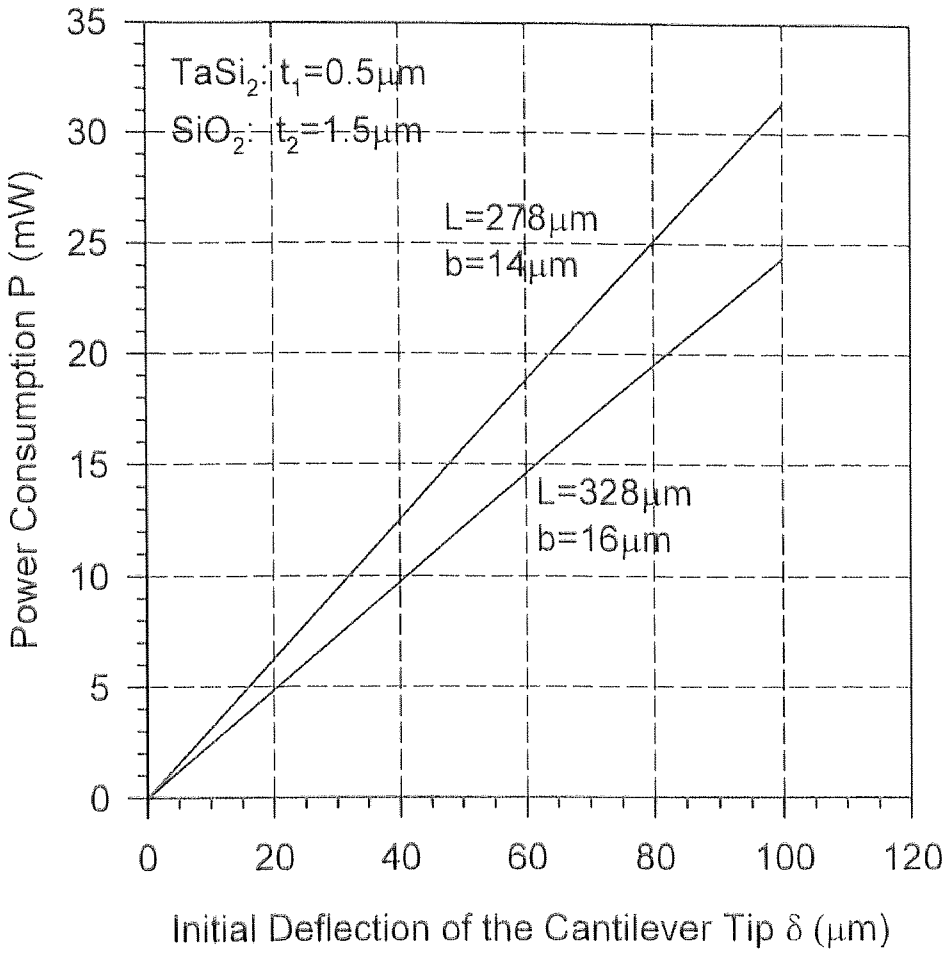


Figure 3.12 Power consumption as the function of the initial cantilever deflection for bimorph structure $TaSi_2/SiO_2$

3.2.3 Analysis of Electrostatically Actuated Flat Cantilever

For an initially flat cantilever beam with one end fixed and another end free, the electrical force which applied between upper $TaSi_2$ layer and the Si substrate will pull down the cantilever tip to touch the substrate first as shown in Figure 3.13(b). The required voltage for this actuation V_0 are 6.4 v and 8.9 v for cantilever length of 328 μm and 278 μm, respectively. The data are got from Figure 3.6 with initial deflection δ=0. The beam is partly in touch with the substrate and partly free stranding as shown in Figure 3.13(c). Increasing the applied voltage, the cantilever and the substrate touch point B will move towards the fixed end. The problem have a variable boundary condition with respect to the free stranding part of the beam. Therefore the system has to be divided into two regions. From fixed end of the beam to point B, the beam is deflected by electrostatic forces. Beyond point B, the beam is in physical contact with the substrate and the deflection profile equals to zero. By using the same method described in section 3.2.1, we can get the total potential energy expressed as:

$$\Pi = U_m + U_e \tag{3.16}$$

Choose the admissible trial function of the deflection profile as [27]:

$$w_1(x) = H - H\left[2\cdot\frac{x}{B} - \left(\frac{x}{B}\right)^2\right]^2 \qquad (0<x<B) \tag{3.19}$$

$$w_2(x) = 0 \qquad (B<x<L) \tag{3.20}$$

Where H is the height of the anchor. The strain energy of bending U_m and the electrostatic potential energy U_e can be written as:

$$U_m = \frac{EI}{2}\int_0^B \left[\frac{d^2 w_1(x)}{dx^2}\right]^2 dx \tag{3.17}$$

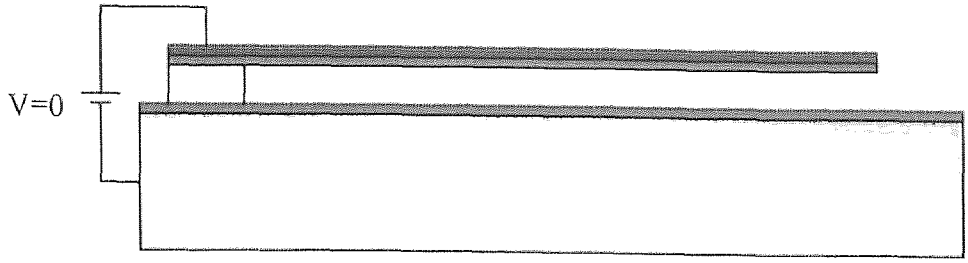
$$U_e = -\frac{1}{2}\int_0^B \frac{\varepsilon_0 b V^2}{\frac{d}{\varepsilon} + w_1(x)} dx + \frac{\varepsilon\varepsilon_0 b V^2}{2d}\cdot(L - B) \tag{3.18}$$

where w(x) is the deflection profile of the beam, EI is the bending stiffness, ε_0 is the permittivity in vacuum, ε is the dielectric constant of the insulator, b is the width of the cantilever beam, d is the thickness of the insulator, L is the length of the beam.

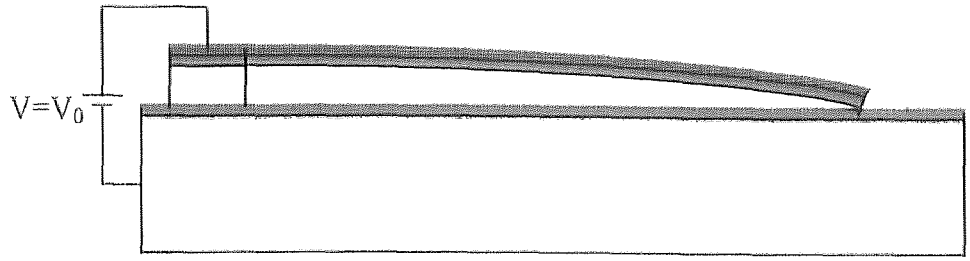
The system is in equilibrium when the first variation of the potential energy with respect to the constant B equals zero:

$$\frac{\partial \Pi}{\partial B} = 0 \tag{3.21}$$

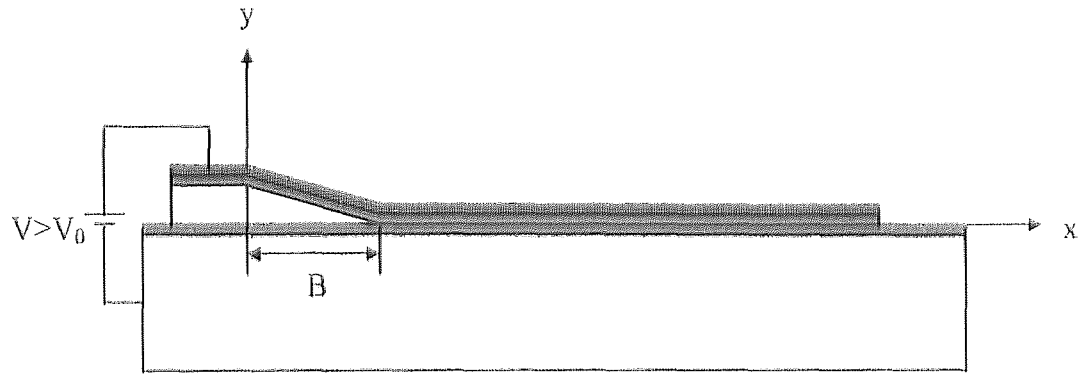
Using the parameters of table 3.2, the numerical solution was obtained by solving the equations (3.16) ~ (3.21). The position of the touch point B as the function of the applied voltage V is shown in Figure 3.14.



(a) initial flat state (V=0)



(b) free end of the beam touch the substrate ($V=V_0$)



(c) fully closed state ($V>V_0$)

Figure 3.13 Actuation sequence of the flat cantilever

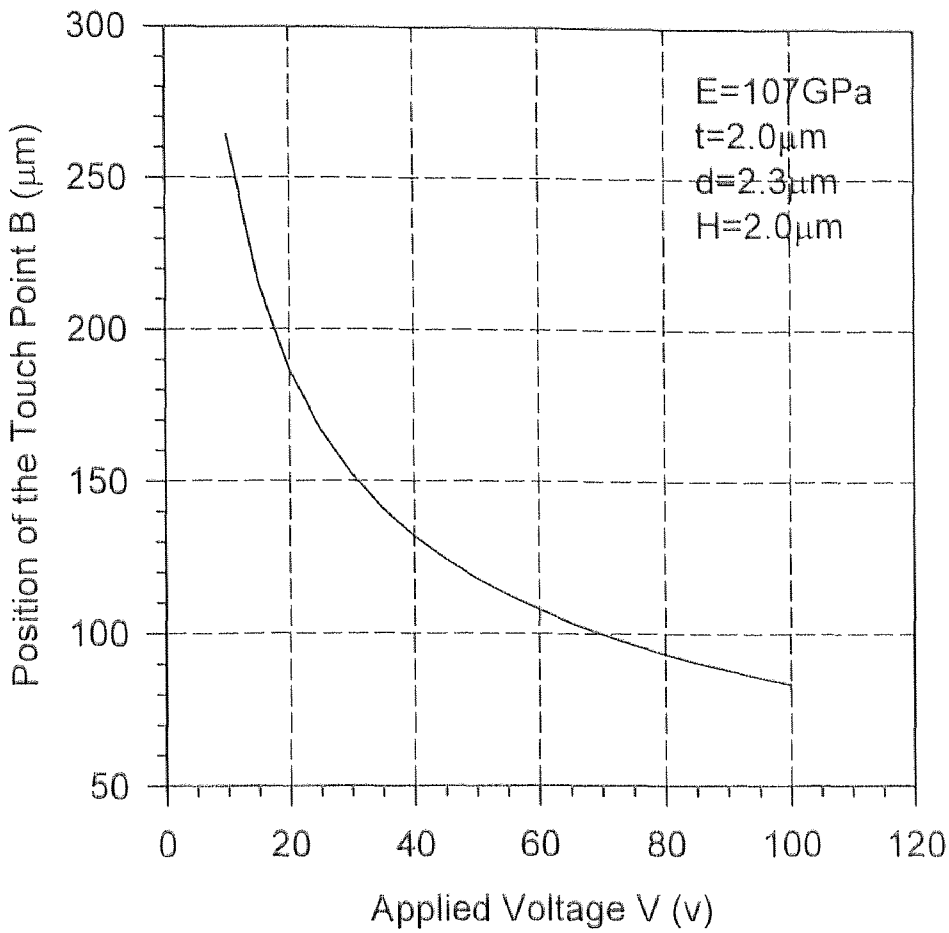


Figure 3.14 Position of the touch point as the function of applied voltage

3.2.4 Analysis of Force Generation at the Electrical Contact Region

In this section the force generation at the electrical contact region will be modeled. An external force F acting on the point C of the beam will bend the beam upwards, in that part where the beam will be not in contact with the substrate, see Figure 3.15. With respect to the range from B to L, the deflection profiles are [27]:

$$\begin{cases} w_1(x) = \dfrac{F}{24EI}\left[-2(x-C)^3 - 3a(x-C)^2 + a^3\right] & (C-a<x<C) \\ w_2(x) = \dfrac{F}{24EI}\left[2(x-C)^3 - 3a(x-C)^2 + a^3\right] & (C<x<C+a) \\ w_3(x) = 0 & \left(B<x<C-a,\quad C+a<x<L\right) \end{cases} \tag{3.22}$$

where a is the half length of the beam of bent part. The expression for the strain energy is $U_m = U_{m1} + U_{m2}$ for transverse loading and axial tension:

$$U_{m1} = \frac{EI}{2}\left[\int_{C-a}^{C}\left(\frac{d^2w_1}{dx^2}\right)^2 dx + \int_{C}^{C+a}\left(\frac{d^2w_2}{dx^2}\right)^2 dx\right] \tag{3.23}$$

$$U_{m2} = \frac{N}{4}\left[\int_{C-a}^{C}\left(\frac{dw_1}{dx}\right)^2 dx + \int_{C}^{C+a}\left(\frac{dw_2}{dx}\right)^2 dx\right] \tag{3.24}$$

where $N = \dfrac{\pi^2 Ebt}{16a^2}\cdot w(C)$ is the axial tension [27]. The potential energy of the electrostatic force can be written as:

$$U_e = -\frac{\varepsilon_0 bV^2}{2}\left[\int_{C-a}^{C}\frac{dx}{\frac{d}{\varepsilon}+w_1} + \int_{C}^{C+a}\frac{dx}{\frac{d}{\varepsilon}+w_2}\right] + \frac{\varepsilon\varepsilon_0 bV^2}{2d}(L-B-2a) \tag{3.25}$$

An additional term has to be added to the total potential energy. This term is the work from the external force acting on the point C of the beam, given by:

$$U_f = -F \cdot w(C) \tag{3.26}$$

If the external force keep the point C at a certain height h as shown in Figure 3.15, we have $w(C) = h$. The total potential energy is:

$$\Pi = U_m + U_e + U_f \tag{3.27}$$

The system , now, is in equilibrium when the first variation of the potential energy with respect to a:

$$\frac{\partial \Pi}{\partial a} = 0 \tag{3.28}$$

Solving all the equations simultaneously with parameters of table 3.2, by numerical iteration, gives the values of a and F at a certain applied voltage V. With the height h equals to the metal thickness of the signal line, the force F is just the same as the electrical contact force. The force F and the half length of bent beam part a as the function of applied voltage are shown in Figure 3.16 and Figure 3.17.

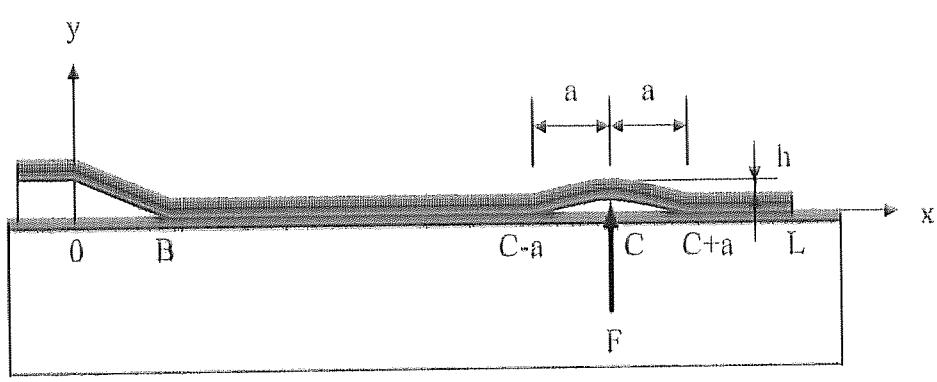


Figure 3.15 A schematic view of the cantilever with a force F applied at the point C

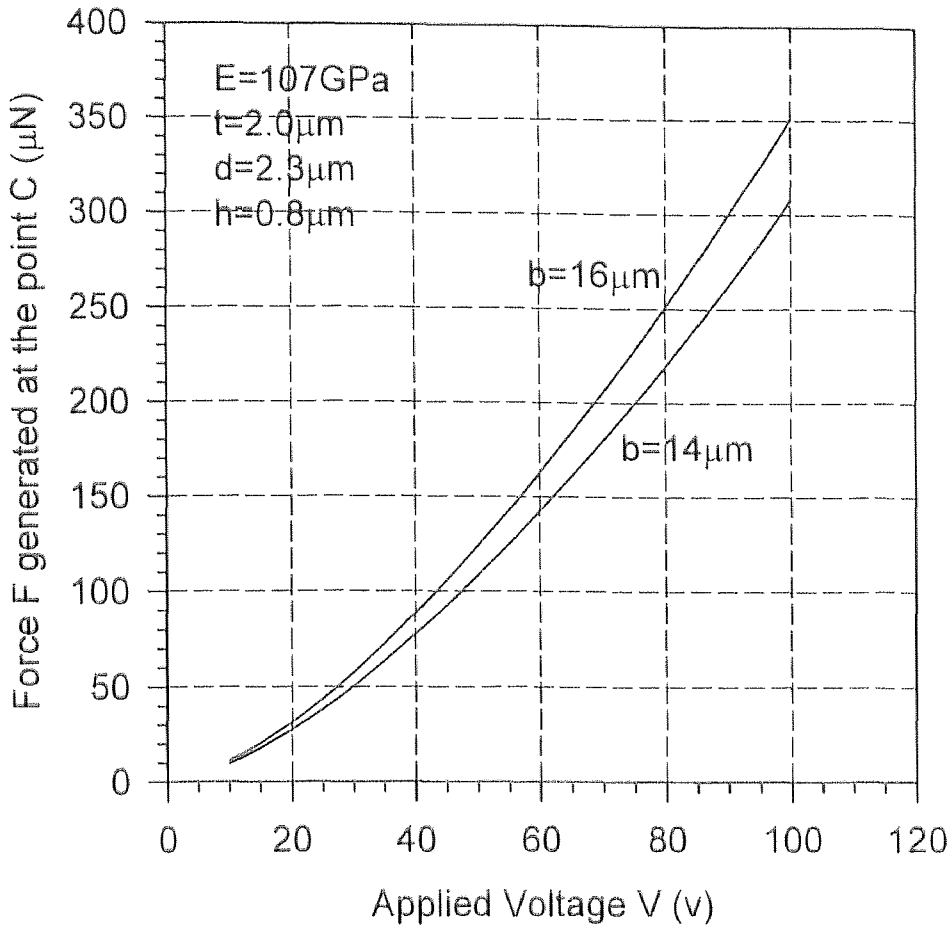


Figure 3.16 Force generated at the point C as the function of applied voltage with different cantilever width b

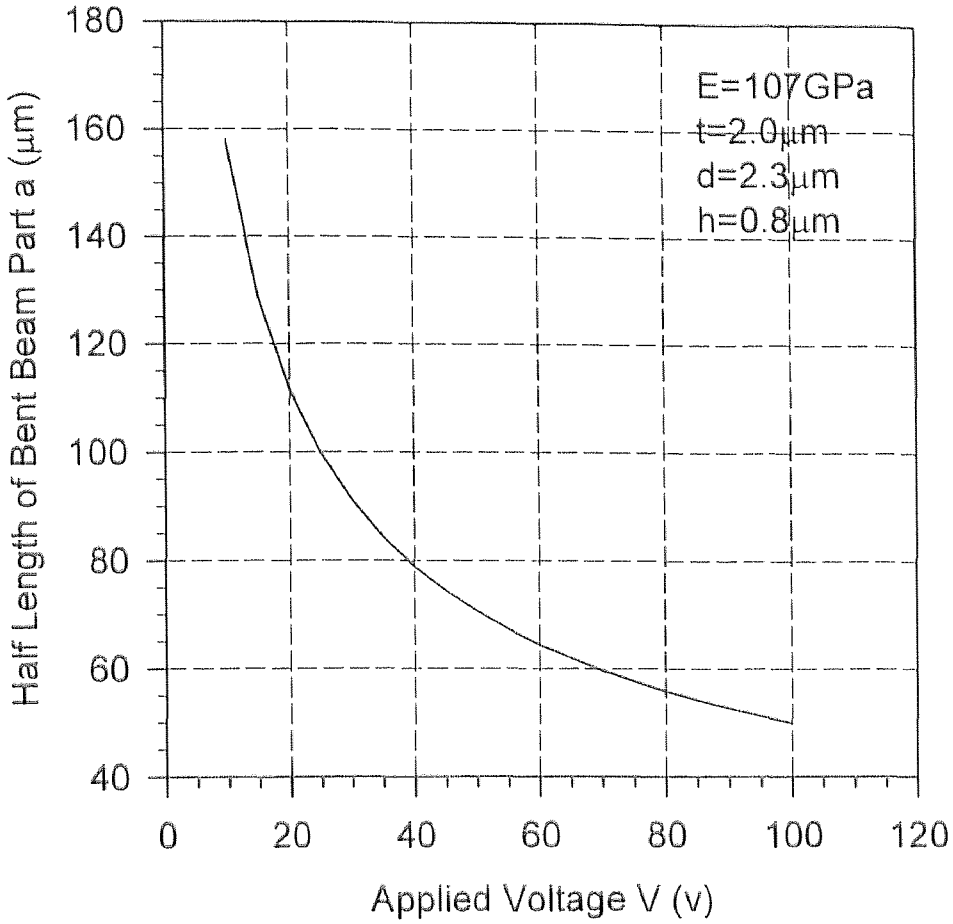


Figure 3.17 Half length of bent beam part as the function of applied voltage

3.2.5 Comparison of Two Operation Modes

From aforementioned analysis, we can summarize the performance of two operation modes for three different sizes of microrelays as listed in Table 3.5 and Table 3.6 with the initial curvature of ρ=1mm. One mode is electrostatically actuated microrelay, another mode is combined thermally and electrostatically actuated microrelay. The data for electrostatically driven mode are extracted from Figure 3.6 and Figure 3.15. The data for combined thermally and electrostatically driven mode are extracted from Figure 3.11, Figure 3.13, Figure 3.15 and Figure 3.16 with the condition of $C-a \geq B$ and $L \geq C+a$.

The lowest generated force is 73μN which is compatible with the results from chapter 2 while consider the small contact area and the use of Au metal with lower resistivity than Pd. The generated force acts as the electrical contact force to obtain a low and stable electrical contact resistance. The lowest required driven voltage for electrostatic actuation is 185 volts. For combined thermal and electrical actuation the lowest required power supply and driven voltage are 13 mW and 35 volts, respectively. The simulation results show that the combined thermal and electrostatic actuation mode reduce the driven voltage dramatically while requiring 10 to 20 milliwatt power supply as trade-off.

Table 3.5 Parameters of microrelays

	relay 1	relay 2	relay 3
cantilever length L (μm)	278	278	328
cantilever width b (μm)	14	14	16
upper layer $TaSi_2$ thickness t_1 (μm)	0.5		
lower layer SiO_2 thickness t_2 (μm)	1.5		
electrical contact position C (μm)	220	208	237

Table 3.6 Comparison of two operation modes

initial curvature ρ=1mm	electrostatically driven			combined thermally and electrostatically driven		
types of microrelays	relay 1	relay 2	relay 3	relay 1	relay 2	relay 3
temperature change ΔT (°C)	—	—	—	174	174	174
power consumption P (mW)	—	—	—	12	12	13
driven voltage V (v)	185	185	194	75	50	35
generated force F (μN)	773	773	836	228	109	73

CHAPTER 4

MICRO VARIABLE INDUCTOR NETWORKS

In this chapter, we will describe the design, fabrication and characterization of micro variable inductor networks. The adjustable inductors are digitally controlled by microrelays which are driven by thermal and electrostatic actuation mechanism. The fabrication process uses seven photomasks and combined surface and bulk micromachining technology.

4.1 Concept and Design

4.1.1 Concept of Micro Variable Inductor Networks

The specific switched inductor circuit chosen has the switched series connection of inductors shown in Figure 4.1. Microrelays connect and disconnect the inductor segments. In this experimental version four inductors (L_3, L_2, L_1 and L_0) switch with four microrelays are chosen to form the variable inductor network, as shown in the schematic circuit of Figure 4.1. Each inductor has a relay connected with it in parallel. Status of relays are controlled by external data bits D_3, D_2, $D_1$and D_0. The microrelay is open for D=0 and is closed for D=1. When all relays are open ($D_3D_2D_1D_0$=0000), the output inductance measured between A and B is at its maximum value. The minimum inductance occurs when all relays are closed, that is, the data bits value equals 15 ($D_3D_2D_1D_0$=1111). With the different status combination of microrelays, 16 different inductance values can be obtained.

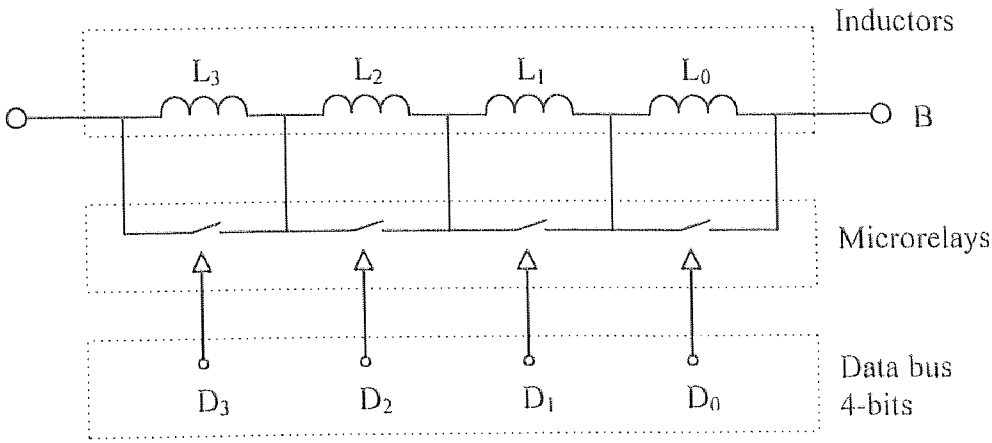


Figure 4.1 Variable inductor circuits diagram

4.1.2 Design of Micro Variable Inductor Networks

The inductors is a 16-turn planar rectangular spiral shape with five underpass connections which divide the coil into four segments corresponding to L_3, L_2, L_1 and L_0. An optical picture in Figure 4.2 shows connections of inductor coil and underpass. The coil was designed with 10 μm-wide line made from 1.5 μm thick gold metal separated by 10 μm spaces. The outer dimension of the four coil segments is 2100μm x 660μm.

The theoretical equation for calculation of planar rectangular microelectronic inductors with one or more turns can be written as follow [40]:

$$L_T = L_0 + M_+ - M_- \tag{4.1}$$

where L_T is the total inductance, L_0 is the sum of self-inductance for straight conductors, M_+ is the sum of the positive mutual inductances which have current flow in two parallel conductors in the same direction, M- is the sum of the negative mutual inductances which have current flow in two parallel conductors in opposite directions. L_0, M_+ and M- can be expressed as:

$$\begin{cases} L_0 = \sum_{i=1}^{Z} L_i \\ L_i = 0.002 l_i \left[\ln\left(\frac{2l_i}{w+t}\right) + 0.50049 + \frac{w+t}{3l_i} \right] \end{cases} \tag{4.2}$$

$$\begin{cases} M_+ = 2\sum_{n=1}^{Z/4}\sum_{i=1}^{Z} M_{i,i+4n} \\ M_{i,i+4n} = 2pQ(p) - 2qQ(q) \\ p = l_i - n(w+s) \\ q = n(w+s) \end{cases} \tag{4.3}$$

$$\begin{cases} M_{-} = 2\sum_{n=1}^{Z/4}\sum_{i=1}^{Z-4n+2} M_{i,i+4n-2} \\ M_{i,i+4n-2} = 2uQ(u) - 2vQ(v) \\ u = l_i - \left(n - \frac{1}{2}\right)(w+s) \\ v = \left(n - \frac{1}{2}\right)(w+s) \end{cases} \tag{4.4}$$

and

$$\begin{cases} Q(x) = \ln\left[\frac{x}{GMD} + \sqrt{1+\left(\frac{x}{GMD}\right)^2}\right] - \sqrt{1+\left(\frac{GMD}{x}\right)^2} + \frac{GMD}{x} \\ \ln GMD = \ln d - \frac{1}{12(d/w)^2} - \frac{1}{60(d/w)^4} - \frac{1}{168(d/w)^6} - \frac{1}{360(d/w)^8} \\ d = n(w+s) \end{cases} \tag{4.5}$$

where l is the length of the straight conductor, w is the width of the coil, t is the thickness of the coil, s is the space of two adjacent straight conductor, z is the total number of the straight conductors.

By solving these equations, the calculated values of the inductor segments L_3, L_2, L_1 and L_0 are 77 nH, 42 nH, 29 nH and 15 nH. The maximum inductance value is 302 nH due to the mutual inductance fraction between inductor segments.

The silicon substrate under inductors were designed to be etched out to reduce the parasitic oxide capacitors and the eddy current power loss in the substrate semiconductor bulk, as illustrated in Figure 4.3. This reduces the substrate loss substantially and thus increases the self-resonant frequency f_{sr} and quality factor Q.

Figure 4.4 shows the overview of a micro variable inductor network. The total area including relays and inductor segments measures 3150 x 930 μm^2.

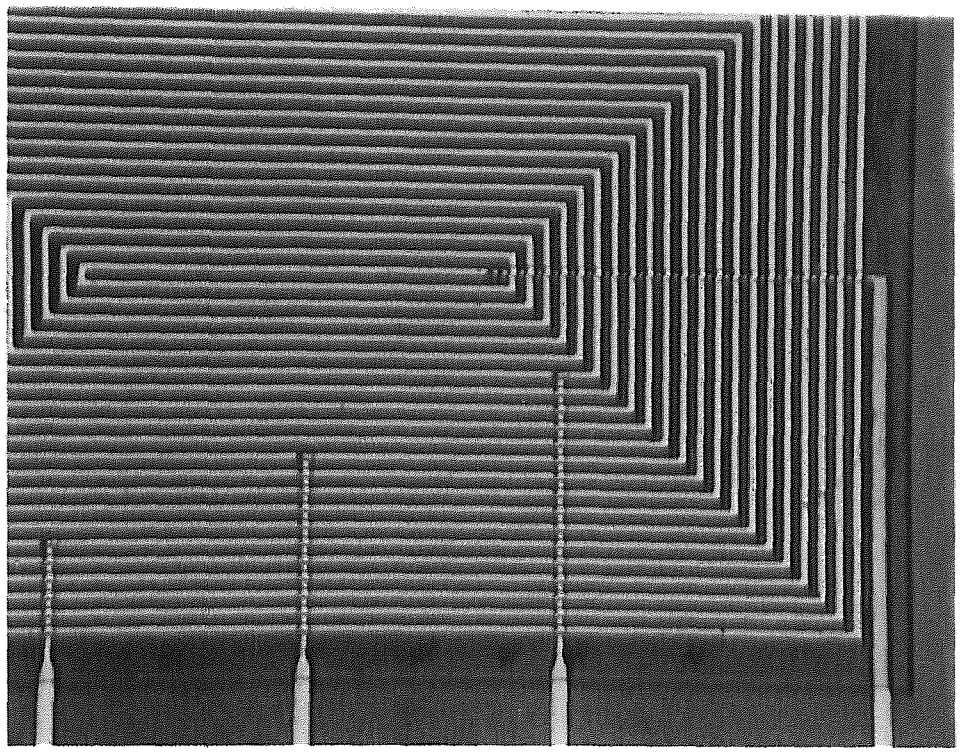


Figure 4.2 Optical photograph shows connections of inductor coil and underpass

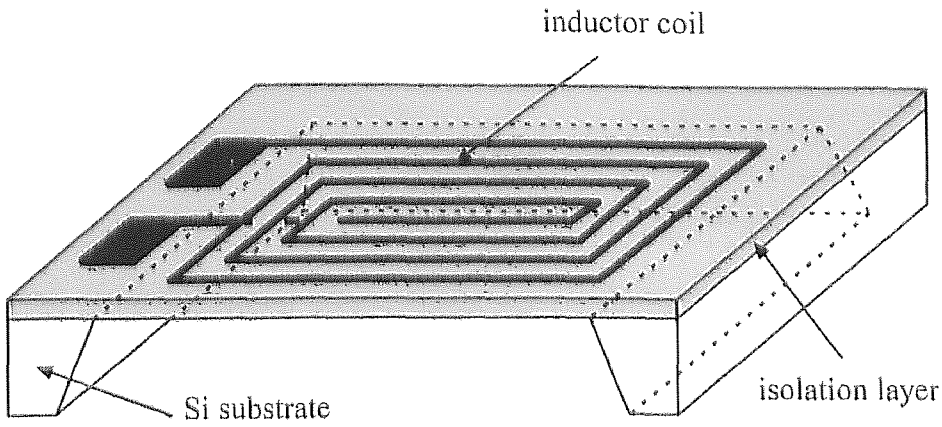


Figure 4.3 A schematic view of the inductor with the underneath Si substrate etched out

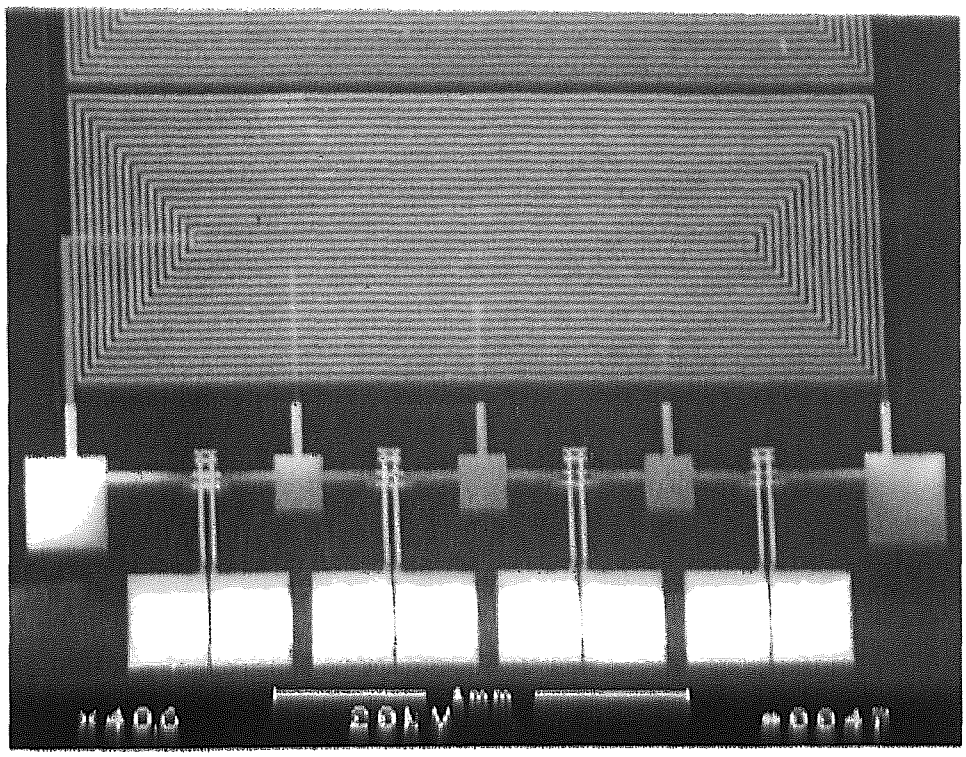


Figure 4.4 A SEM picture shows the overview of a micro variable inductor network

4.2 Fabrication

4.2.1 Photomask Design

The total fabrication process consist of seven photomasks including microrelays and inductor segments. The layout was designed using the design tool of Mentor Graphics. The photomasks were fabricated by Photo Sciences Inc. Mask 1 is used to form the underpasses of inductors. Mask 2 is used to define the inductor region. Mask 3 is used to form the upper electrical contact metal of microrelays. Mask 4 is used to form $TaSi_2$ heater. Mask 5 is used to form cantilever structure and to define via between the inductor coils and the underpasses coil taps. Mask 6 is used to form inductor coils and bonding pads of microrelays. Mask 7 is used to form KOH etching windows at the backside of the wafers.

4.2.2 Process Flow Description

The most of steps of the fabrication were carried out in the class 10 clean room of NJIT. The metals sputtering were performed at the laboratory of materials science in NJIT. Several other steps were done in Cornell Nanofabrication Facility (CNF) of Cornell University. The process included two times Al deposition and three times Au deposition.

The fabrication sequence is illustrated in Figure 4.5. The process began with (100) oriented, 100mm-diameter silicon wafers. The first step was to grow a 400 nm thermal oxidation layer on both sides of the wafer. The front side SiO_2 layer served as the isolation layer. The backside SiO_2 layer needed to be removed because it would influence the later process step of backside KOH etching. For removing the backside oxidation layer, a photoresist layer was spun on the front side of the wafer. After 20 min. bake in

box oven with 115°C, the wafer was immersed in 6:1 BOE (buffered HF solution) for backside SiO_2 layer removal. Then the front side photoresist was cleaned out and the wafer was waiting for the next step.

The second step was a low pressure chemical vapor deposition (LPCVD) of silicon nitride (Si_3N_4). A dry oxidation of 30 nm was performed first with 950°C, 45 min. which was served as a buffer layer to reduce Si_3N_4/Si interface stress. Then a 200 nm Si_3N_4 layer was grown by LPCVD with 775°C, 40min. under 400 mT pressure. The front side Si_3N_4 increased the thickness of the isolation layer. The backside Si_3N_4 was used as a mask layer for later KOH backside etching.

The third step was a 200 nm SiO_2 LPCVD with 425°C, 3 hr. under 500 mT pressure. We called this layer as LTO (low thermal oxidation) layer. It was grown for the adhesion consideration of the later metal deposition step.

The front side isolation layer consisted of 400 nm SiO_2, 200 nm Si_3N_4 and 200 nm LTO as shown in Figure 4.5(a). The total thickness equals 800 nm.

The forth step was 800 nm first aluminum layer Al(1) deposition which was performed at 100°C.

The fifth step was photolithography with the photomask 1 as shown in Figure 4.5(b). The patterning must consider the wafer orientation which would influence the later KOH patterning and thus KOH etching. The photoresist used at this step was remained after Al etching and served as liftoff material for the next step. For this reason, we needed a thick photoresist layer which was realized by applying photoresist (Shipley 827) two times. The thickness of the photoresist was measured 8~9 μm. The standard Al

etchant (H_3PO_4, HNO_3, CH_3COOH, H_2O) was used to etch aluminum with 40°C. After Al etching, the wafers were baked in box oven with 115°C, 10 min.

The sixth step was the first gold layer Au(1) deposition and patterning by liftoff process. The thickness of Au film was 800 nm and the same as Al(1). The liftoff procedure was completed using Acetone to dissolve the photoresist with ultrasonic about 5 min, leaving a planar gold/aluminum surface as shown in Figure 4.5(c). This patterned Au layer served as underpasses of inductors.

The seventh step was 1.2 μm second aluminum layer Al(2) deposition and patterning with photomask 2. Both the Al layers in the inductor region were moved in this step as shown in Figure 4.5(d). The remaining Al layers in the microrelay region served as sacrificial layer for the last release step.

The eighth step was using liftoff process to form upper electrical contacts of microrelays as shown in Figure 4.5(e). The photoresist was used as liftoff material again and was patterned by using photomask 3. An 800 nm second gold layer Au(2) was then deposited. The wafer was immersed into Acetone to get final gold metal patterns.

The ninth step was plasma enhanced chemical vapor deposition (PECVD) of silicon oxidation. The film deposition temperature was 240°C and the film thickness was 1.5 μm. The low process temperature was required to avoid the reaction between aluminum and gold. This SiO_2 layer served as both cantilever structures of microrelays and the isolation layer between inductor coils and underpasses as shown in Figure 4.5(f).

The tenth step was $TaSi_2$ layer deposition. The film thickness was 500 nm, see Figure 4.5(g).

The eleventh step was photolithography using photomask 4 to form $TaSi_2$ heater as shown in Figure 4.5(h). The etching of $TaSi_2$ was performed by RIE in SF_6 chemistry. The $TaSi_2$ layer served as both the heater for thermal actuation and the upper electrode for electrostatic actuation.

The twelfth step was photolithography PECVD SiO_2 using photomask 5 to form cantilever structures of microrelays and to define via between the inductor coils and underpasses coil taps as shown in Figure 4.5(i). A CF_4 and CHF_3 based RIE was used to etch SiO_2.

The thirteenth step was 1.5 μm third gold layer Au(3) deposition and patterning with photomask 6 using liftoff process. The inductor coils and bonding pads of microrelays were formed at this step, as illustrated in Figure 4.5(j).

The fourteenth step was backside photolithography with photomask 7 to open KOH etching windows as shown in Figure 4.5(k). The backside film consisted of $TaSi_2$, SiO_2 and Si_3N_4 layers while Si_3N_4 layer served as KOH etching mask. SF_6 based RIE, CF_4 and CHF_3 based RIE, and CF_4 based RIE were used to etch $TaSi_2$, SiO_2 and Si_3N_4, respectively. Before backside pattering, a thick photolithography layer was spun on the front side of the wafer to prevent mechanical damages during the process. After RIE, the wafer was cleaned to strip the both side photoresist on the wafer.

The fifteenth step was backside KOH etching. A special chunk was used for the front side device protection during KOH etching. An 8 μm thick photoresist was coated on the front side of the wafer with 115°C box oven bake for 30 min. prior to the KOH to protect the devices. The wafer was immersed in a 45% KOH solution with 80°C for the first 7 hours and 60°C for the next 2 hours, approximately. The double polished wafer

was 450 ± 25 μm thick. The etch was stopped at the front Si_3N_4 layer. The KOH etching moved out the Si substrate under the inductor as shown in Figure 4.5(l).

The last step was cantilever releasing which was performed in a standard Al etchant. The time of 20 ~ 30 min. were needed to completely release the cantilever structure. After DI water and alcohol clean, the wafer was baked several minutes for dry. The fabrication of the variable inductor networks was then completed as shown in Figure 4.5(l).

4.2.3 Summary of Process Flow

The sequence of the fabrication procedure can be summarized as following steps:

1) Wafer cleaning. Thermal oxidation 400 nm thick SiO_2 at 1050°C. Applying photoresist on the front side of the wafer and baking. Backside SiO_2 removal in 6:1 BOE. Removing photoresist.
2) Dry oxidation 30 nm thick SiO_2 at 950°C and LPCVD 200 nm thick Si_3N_4 at 775°C.
3) LPCVD 200 nm thick SiO_2 at 425°C.
4) An 800 nm thick aluminum Al(1) sputtering
5) Photolithography using photomask 1. Al(1) layer patterning with standard aluminum etchant. Remaining photoresist.
6) An 800 nm thick gold Au(1) sputtering and patterning by liftoff.
7) An 1.2 μm thick aluminum layer Al(2) sputtering and photolithography with photomask 2. Al(2) layer patterning with standard aluminum etchant. Removing photoresist.

8) Photolithography using photomask 3. An 800 nm thick gold Au(2) sputtering and patterning by liftoff.

9) PECVD 1.5μm thick SiO_2 at 240°C.

10) A 500 nm thick $TaSi_2$ sputtering.

11) Photolithography using photomask 4. $TaSi_2$ patterning by SF_6 based RIE. Removing photoresist.

12) Photolithography using photomask 5. SiO_2 patterning by CF_4 and CHF_3 based RIE. Removing photoresist.

13) Photolithography using photomask 6. An 1.5 μm thick gold Au(3) sputtering and patterning by liftoff.

14) Applying photoresist on the front side of the wafer and baking. Backside photolithography using photomask 7. $TaSi_2$, SiO_2 and Si_3N_4 patterning by SF_6 based RIE, CF_4 and CHF_3 based RIE, and CF_4 based RIE, respectively. Removing photoresist.

15) Applying photoresist on the front side of the wafer and baking. Backside KOH etching with 45% KOH solution at 80°C first and at 60°C then.

16) Cantilever structure releasing by standard Al etchant.

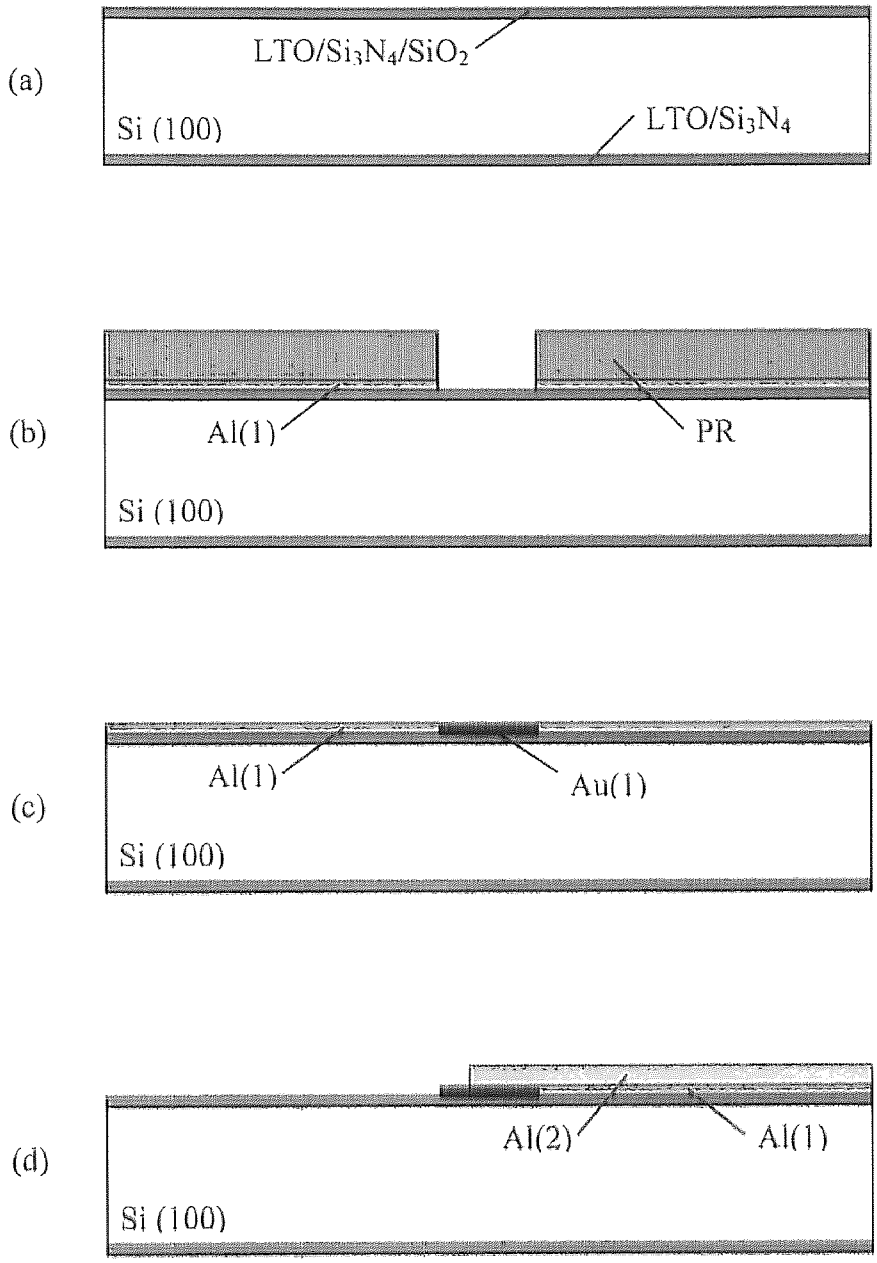


Figure 4.5 Process flow of the variable inductor (a) ~ (d)

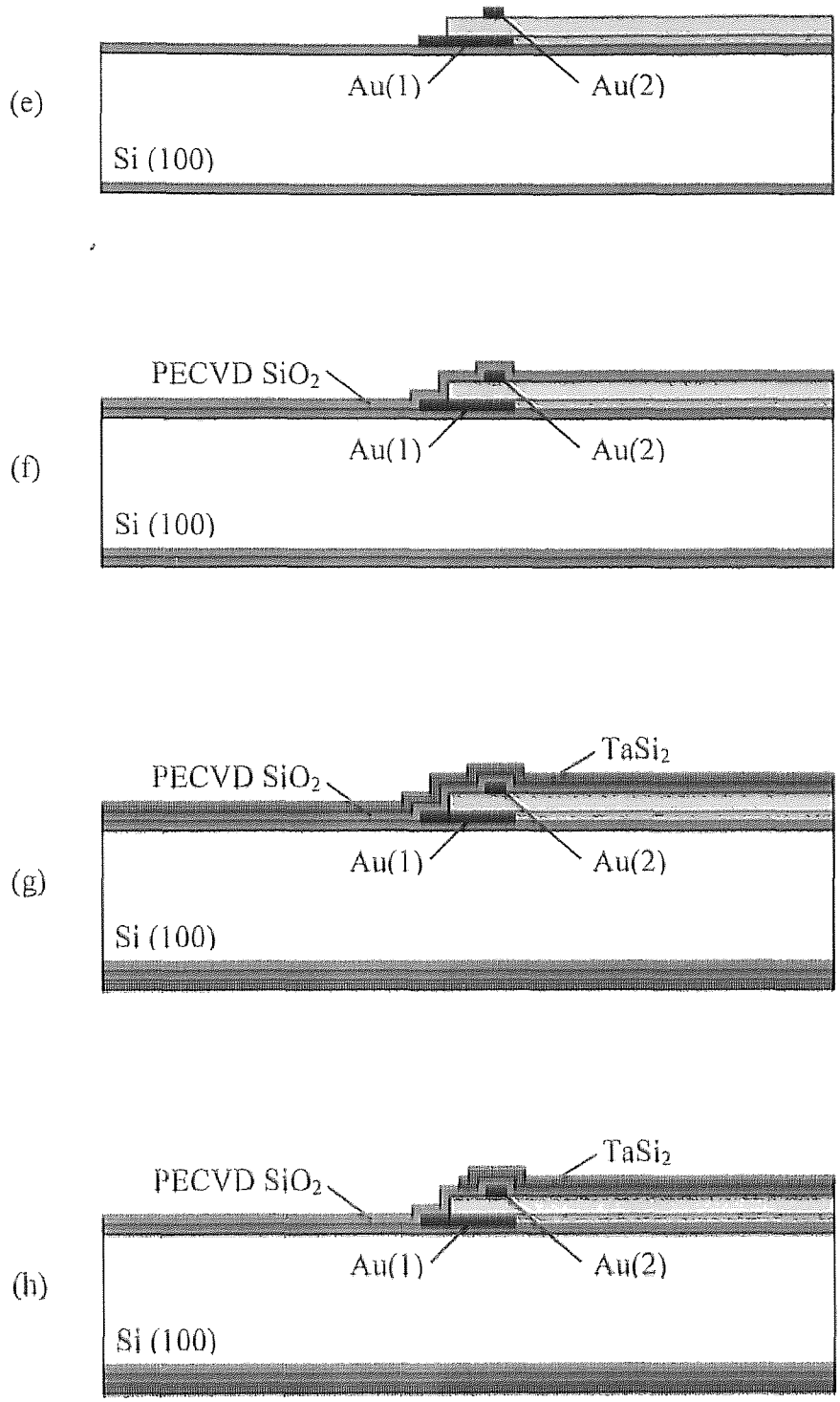


Figure 4.5 Process flow of the variable inductor (e) ~ (h)

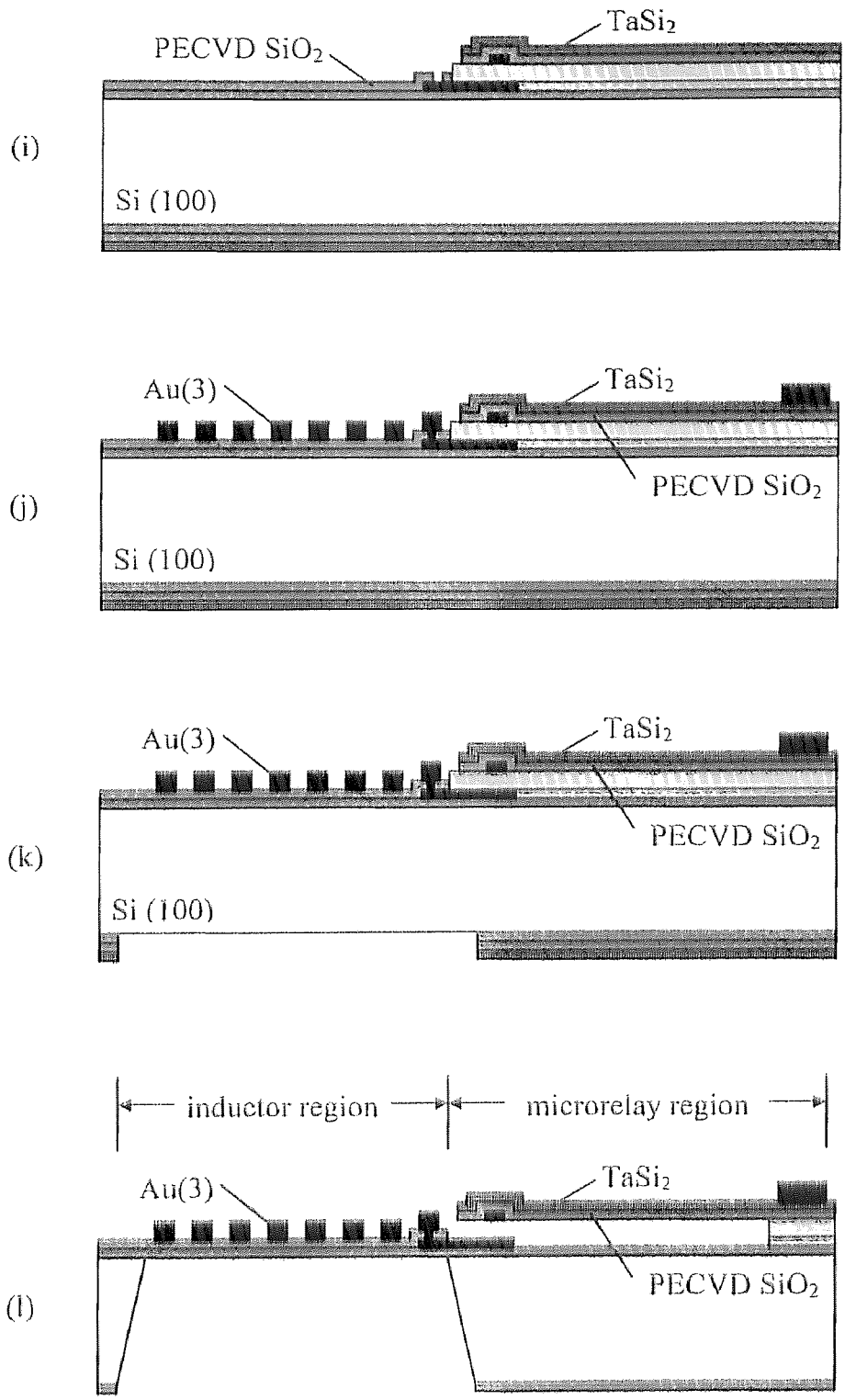


Figure 4.5 Process flow of the variable inductor (i) ~ (l)

4.3 Experimental Characterization and Discussions

Four different types of micro variable inductor networks based on four different types of microrelays have been successfully fabricated and characterized. Figure 4.6 shows a SEM picture with two variable inductor networks in one cell. The inductors are the same but the microrelays are different for each variable inductor network. Each variable inductor has four microrelays connected with it. The two groups of microrelays have the same structure but different sizes. The arrangement of two inductor networks in one cell is for reducing the chip area.

4.3.1 Characterization of Microrelays

There were four different types of microrelays with three different structures have been fabricated. Figure 4.7 shows a SEM picture of two microrelays with structure 1 (relay 1) after release. This type of microrelay has one contact resistance and its cantilever has an expanded length of 51 μm. Figure 4.8 shows a SEM picture of a microrelay with structure 2 (relay 2) after release. This type of microrelay has two contact resistance in parallel and its cantilever has an expanded length of 51 μm too. Figure 4.9 shows another SEM picture of two microrelays with structure 2 (relay 3) after release. Both the length and the width of the cantilever are larger than relay 2. This type of microrelay also has two contact resistance in parallel but its cantilever has an expanded length of 70 μm. Figure 4.10 shows a SEM picture of a microrelay with structure 3 (relay 4) after release. This type of microrelay has three contact resistance in parallel and its cantilever has an expanded length of 78 μm. Detailed parameters of the structures are listed in Table 4.1.

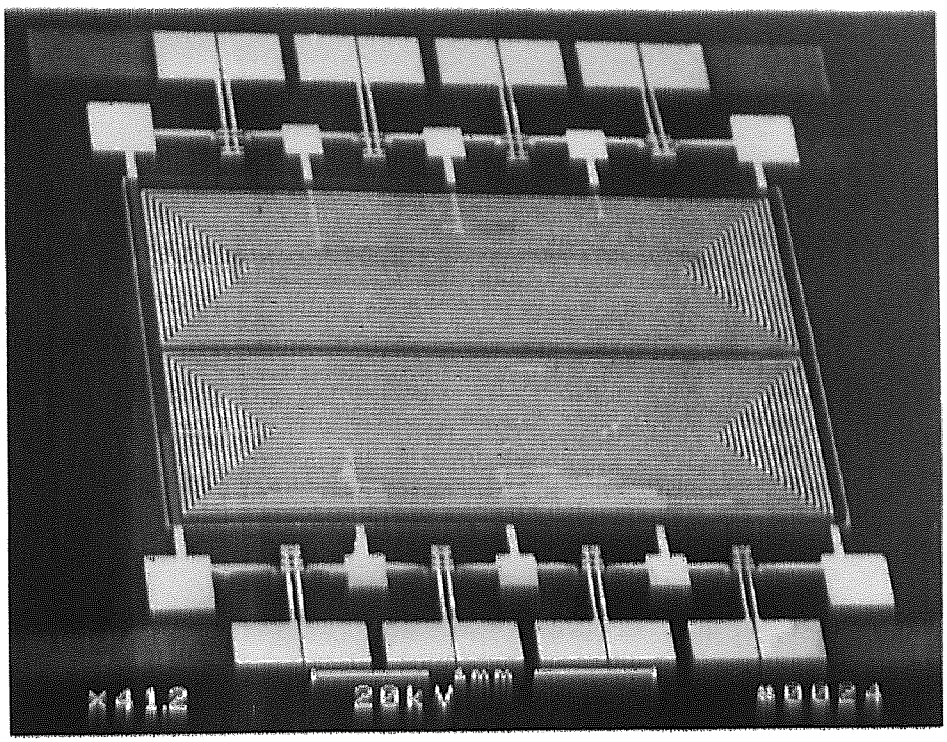


Figure 4.6 A SEM picture shows two variable inductor networks in one cell

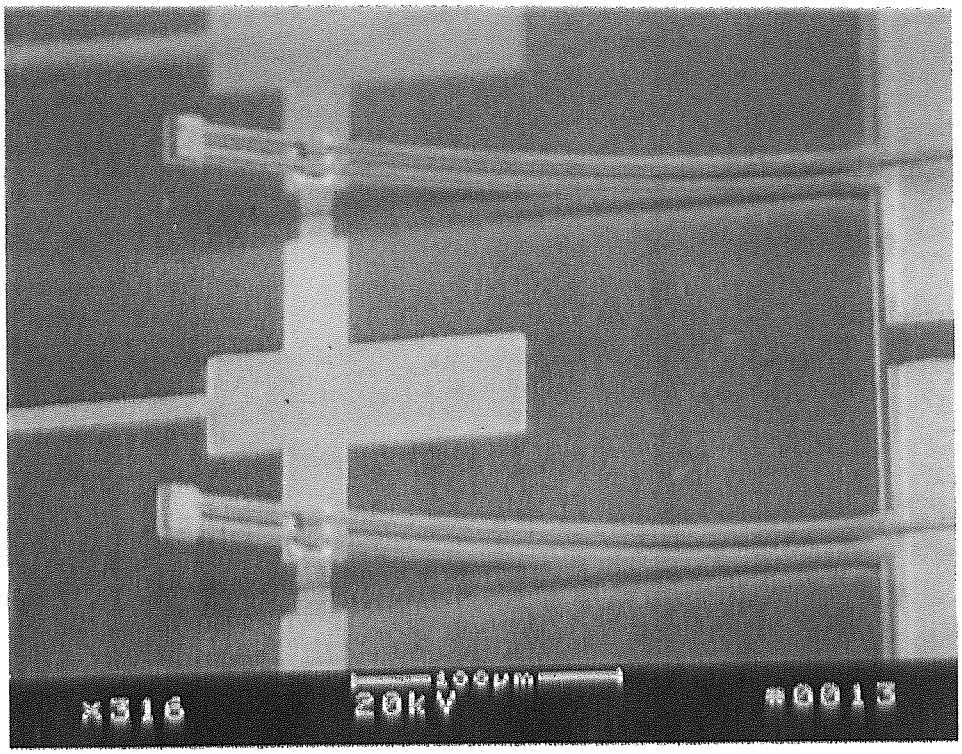


Figure 4.7 A SEM picture shows two microrelays (relay 1) after release

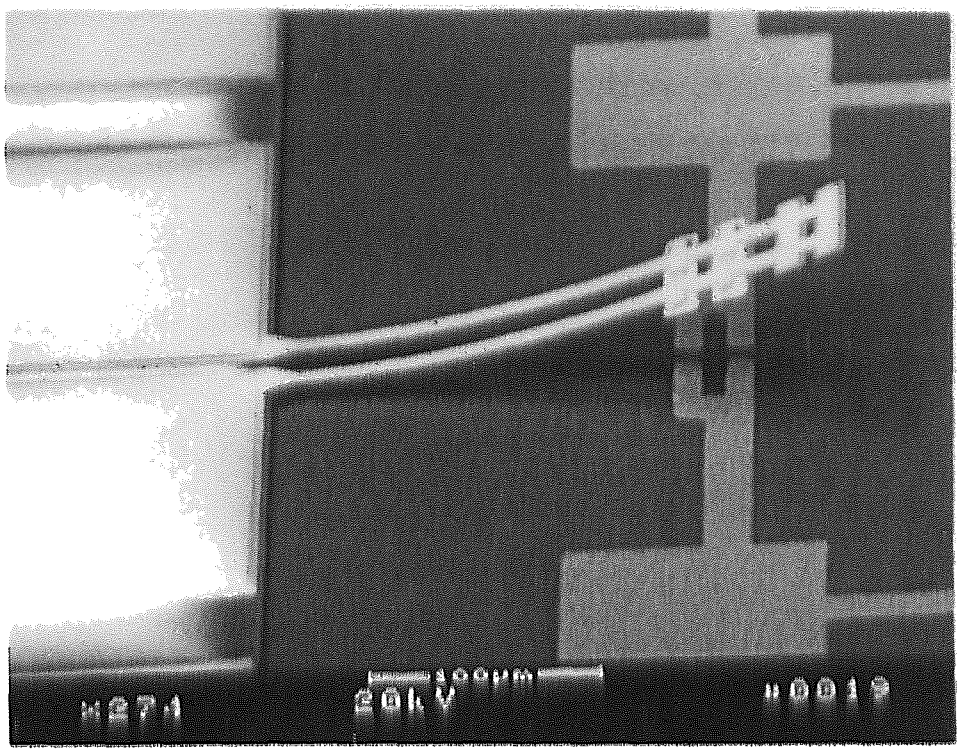


Figure 4.8 A SEM picture shows a microrelay (layer 2) after release

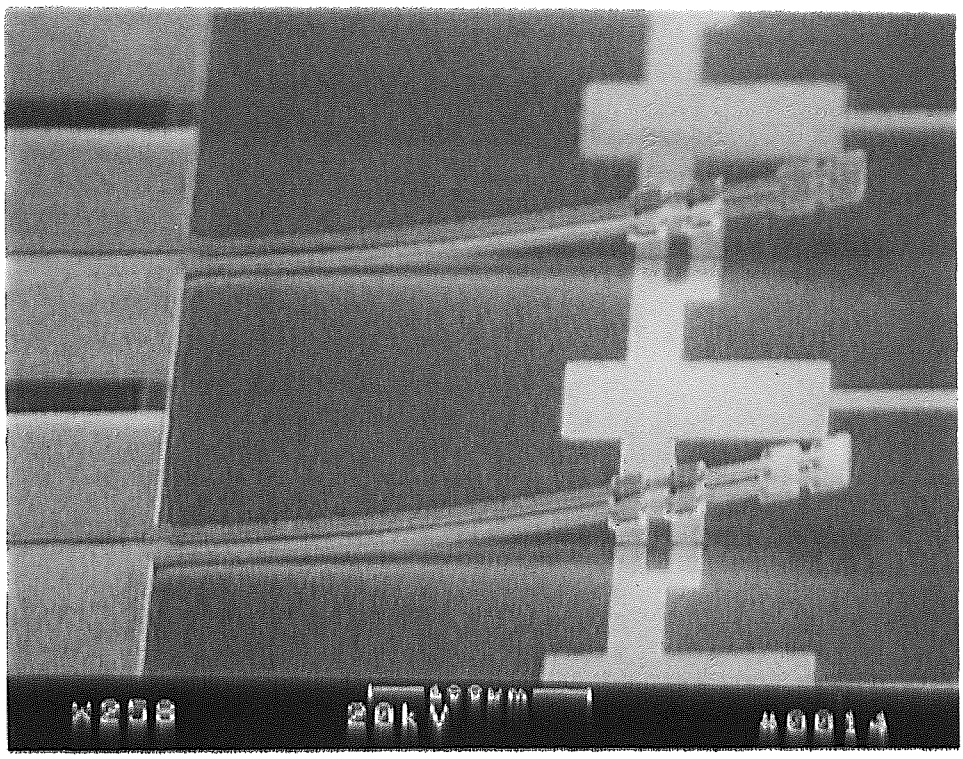


Figure 4.9 A SEM picture shows two microrelays (relay 3) after release

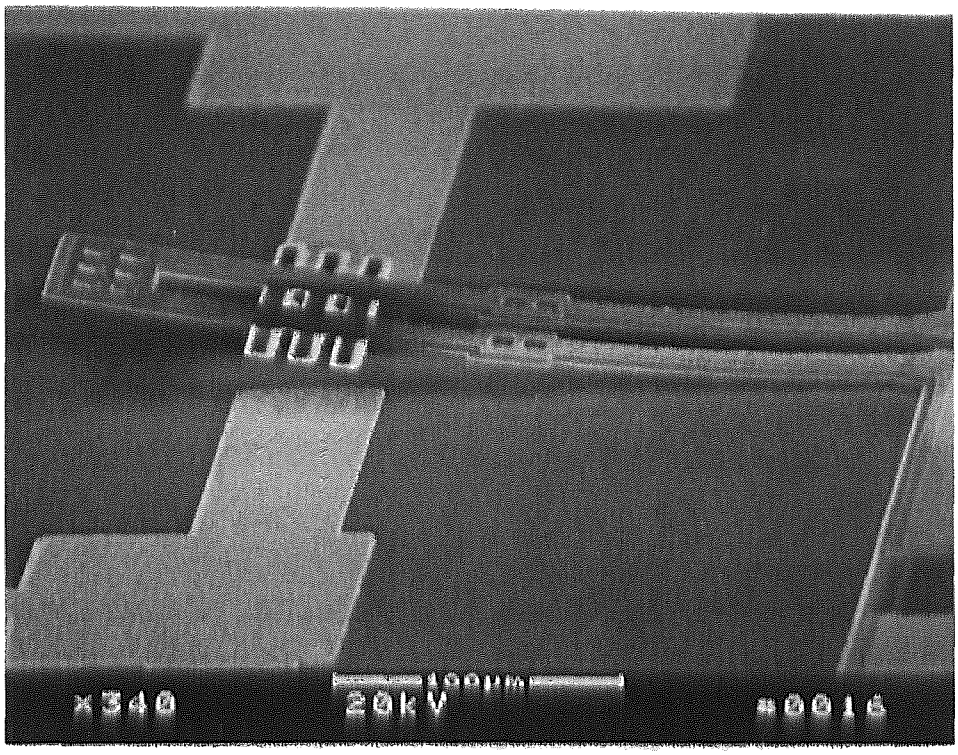


Figure 4.10 A SEM picture shows a microrelay (relay 4) after release

The measurement of electrical contact resistance was performed with two steps. First, a thermal voltage V_a was applied to make initially upwards buckled cantilever bend downwards and stop at a near flat position. Second, an electrostatic voltage V_b was added to provide sufficient clamping and hold down force to get a low electrical contact resistance. The measured results are listed in Table 4.1.

As expected, the combined actuation mechanism reduced the applied voltage much. For example, the voltage needed to drive relay 3 with electrostatic actuation mechanism only is 160 ~ 180 volts, while with the combined actuation mechanism, the thermal power and applied voltage are 11 mW and 30 ~ 40 volts, respectively. With different structures and different dimensions, the combined thermal power and electrostatic voltage which is needed to obtain a low and stable electrical contact resistance are different. The measured on-state contact resistances range from 1.0 ohms to 1.2 ohms for relay 1 and 0.6 ohms to 0.8 ohms for others. The results show that the type of relay 3 is a better choice compared with other three types of microrelays because it needs lower thermal power and electrostatic voltage and has lower contact resistances.

The experiments operating the relay 3 in the AC mode have been carried out. With a constant thermal power supply of 11 mW, an AC switching voltage with peak-to-peak in the range of -10 v to 10 v riding on a DC bias of 20 v was applied between the upper electrode and the silicon substrate resulting an AC operation voltage in the range of 10 v to 30 v. The output voltage has been measured over a resistance load of 1 KΩ, as illustrated in Figure 4.11. The driving signal of square wave at different frequencies have been used to characterize the relay. The results are shown in Figure 4.12, Figure 4.13, Figure 4.14 and Figure 4.15 with frequencies of 200 Hz, 1 KHz, 7 KHz and 10 KHz,

respectively. For higher frequencies the relay was either on or off, since the mechanical structure was no longer able to follow the driving. The closure time of the relay was about 12 μs obtained from Figure 4.15.

The lifetime of the microrelay has been tested by using AC switching voltage at the frequency of 2 KHz. The device was hot switched with 2 mA and failed at 10^6 cycles because of the contact resistance increasing. The device operated at low frequency and hot switching current of 5 mA failed at only several cycles with two contact metals sticking together due to welding.

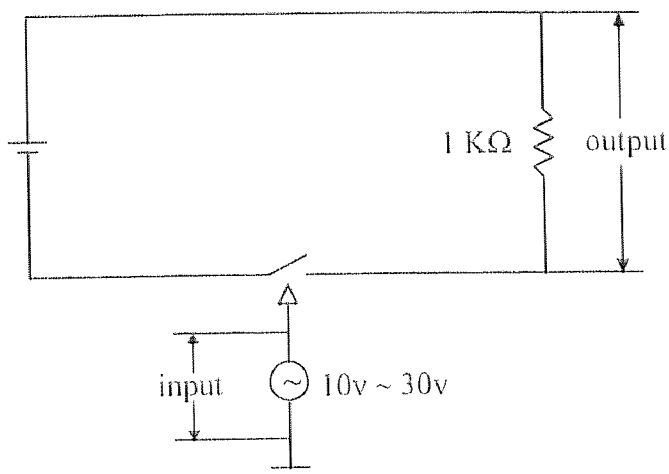


Figure 4.11 Circuit diagram for the measurement of AC mode operation

Table 4.1 Parameters of microrelays and the measured results

structures of microrelays		structure 1	structure 2		structure 3
types of microrelays		relay 1	relay 2	relay 3	relay 4
cantilever length L (μm)		278	278	328	328
cantilever width w (μm)		14	14	16	20
expanded length l (μm)		51	51	70	78
contact area A (μm^2)		200 x 2	290 x 4	340 x 4	200 x 6
initial deflection of the tip δ (μm)		34	32	42	39
combined actuation mechanism	power for thermal actuation P (mW)	10	10	11	14
	voltage for electrostatic actuation V (v)	65~80	45~55	30~40	50~60
voltage needed for electrostatic actuation mechanism only		210~230	190~200	160~180	175~190
measured contact resistance R_c (Ω)		1.0 ~ 1.2	0.6 ~ 0.8		

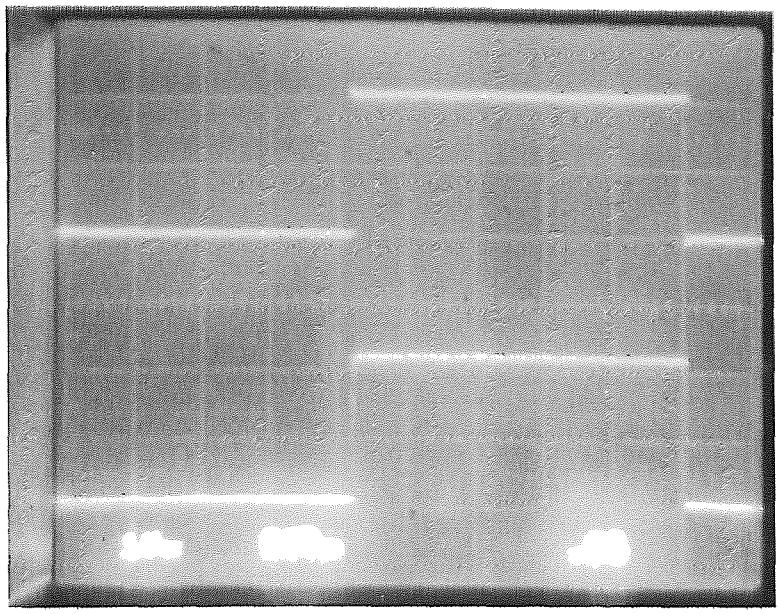


Figure 4.12 Switching behavior at 200 Hz

Upper trace: 10 v/div, 0.5 ms/div; actuation voltage
Lower trace: 0.5 v/div, 0.5 ms/div; output voltage

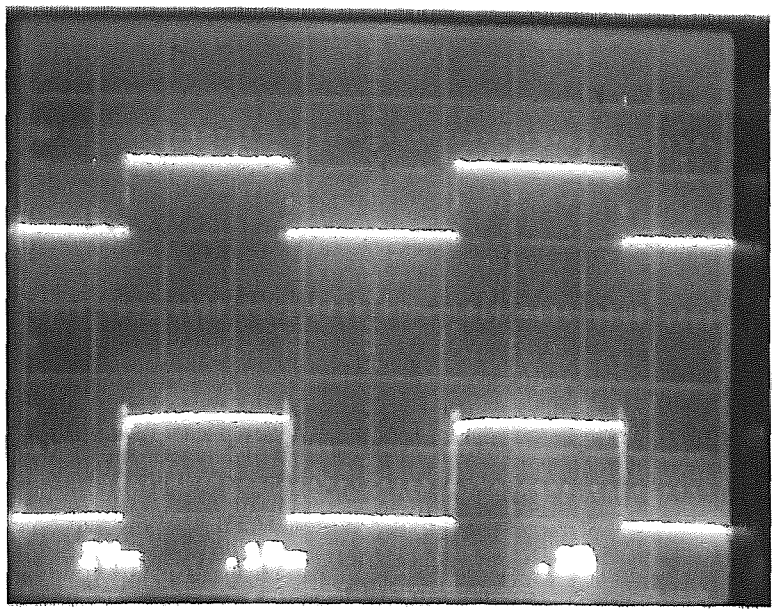


Figure 4.13 Switching behavior at 1 KHz

Upper trace: 20 v/div, 0.2 ms/div; actuation voltage
Lower trace: 1 v/div, 0.2 ms/div; output voltage

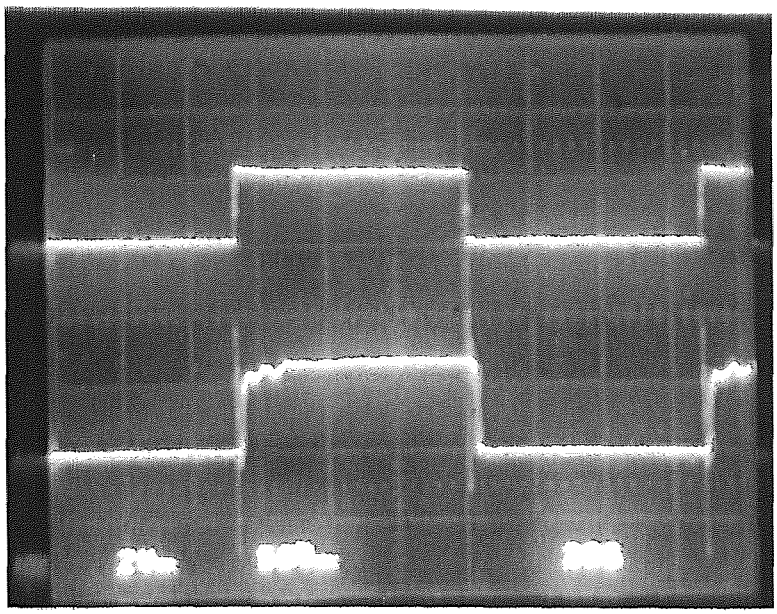


Figure 4.14 Switching behavior at 7 KHz

Upper trace: 20 v/div, 20 μs/div; actuation voltage
Lower trace: 0.5 v/div, 20 μs/div; output voltage

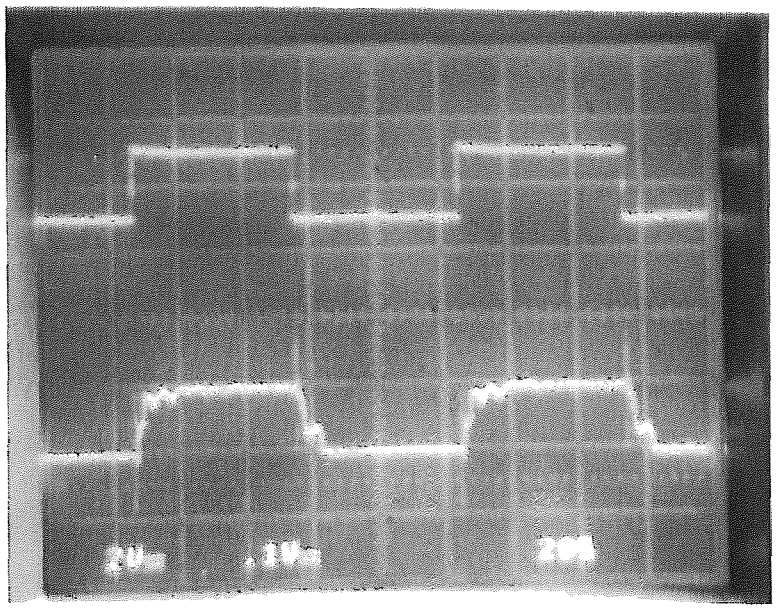


Figure 4.15 Switching behavior at 10 KHz

Upper trace: 20 v/div, 20 μs/div; actuation voltage
Lower trace: 1 v/div, 20 μs/div; output voltage

4.3.2 Characterization of Variable Inductor Networks

Four different types of micro variable inductor networks have been fabricated and characterized. Figure 4.16 ~ Figure 4.19 show SEM pictures of these four variable inductor networks with relay's type of relay 1, relay 2, relay 3 and relay 4 listed in Table 4.1. A 16-turn rectangular spiral coil inductor was divided into four segments which connected with four microrelays in parallel. The output inductance value was controlled by status combination of microrelays.

Figure 4.20 shows an optical photograph of the inductor part after backside KOH etching. The dark area shows the silicon substrate under the inductor was etched out for the purpose of reducing the substrate loss. The inner line is the edge of the silicon substrate. The outer line is the edge of PECVD SiO_2. The inductor coil and the underpass were isolated by PECVD SiO_2 layer. The suspended membrane consisted of PECVD SiO_2 and combined LTO/Si_3N_4/SiO_2 layers.

The inductors were characterized by using HP network analyzers. HP 85046A is used to measure the sample in the frequency range of 300 KHz to 3 GHz, while HP 8510 works in the range of 45 MHz to 20 GHz. The open circuit, short circuit and 50 Ω calibration were performed before the measurements [41]. The S_{11} network port parameter was extract from an one-port measurement of the reflection coefficient. The measured inductance values with the digitally increased data bits $D_3D_2D_1D_0$ are shown in Table 4.2. The data bits $D_3D_2D_1D_0$ represent the different combinations of switching states of microrelays. Sixteen different values ranging from 2.5 nH to 324.8 nH were measured. Mutual inductance was found among the individual inductors L_3, L_2, L_1 and L_0

due to the present layout design. The mutual inductance reduced the linearity of the actual inductance versus the programmed value of inductance.

Two Smith chart of S_{11} measurements are shown in Figure 4.21. One was measured with all microrelays opened, that is $D_3D_2D_1D_0$=0000 in Figure 4.21(a). The self-resonant frequency was 1.9 GHz and the maximum quality factor was 1.7 at 530 MHz. The other was measured with only one relay opened, that is $D_3D_2D_1D_0$=1110 in Figure 4.21(b). The self-frequency was 4.6 GHz and the maximum quality factor was 3.3 at 1.6 GHz.

Table 4.2 Measured inductance values with the different combinations of switching state of microrelays

$D_3D_2D_1D_0$	L (nH)	$D_3D_2D_1D_0$	L (nH)
0000	324.8	1000	162.4
0001	277.9	1001	105.7
0010	223.2	1010	67.4
0011	185.0	1011	45.9
0100	166.9	1100	60.5
0101	127.3	1101	31.5
0110	103.8	1110	16.2
0111	83.1	1111	2.5

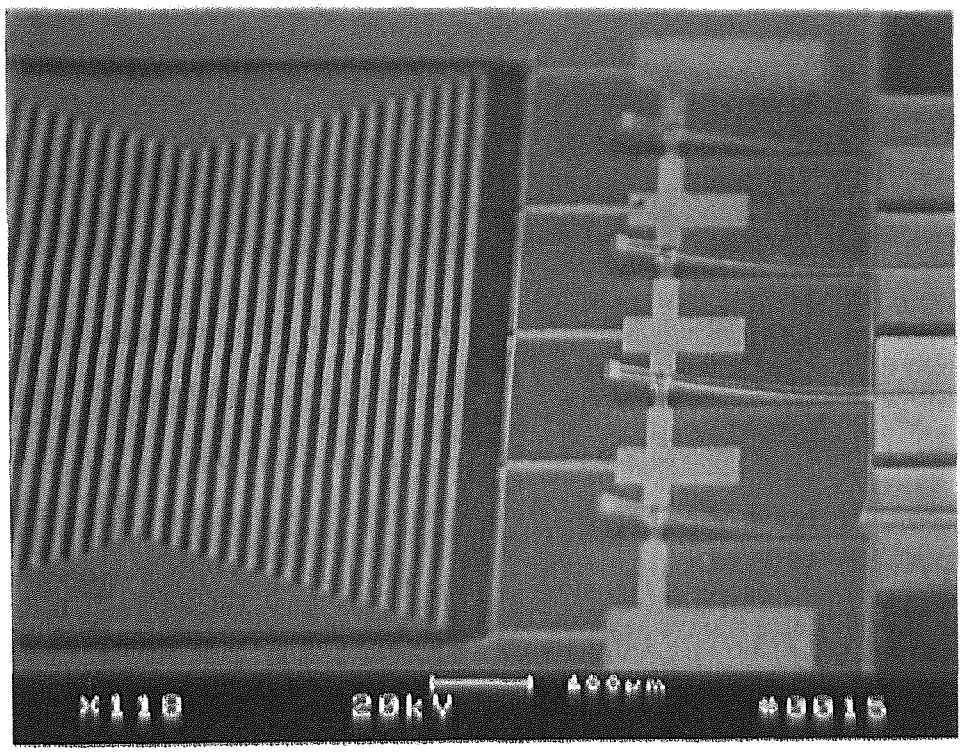


Figure 4.16 A SEM picture of the variable inductor network with a group of relay 1

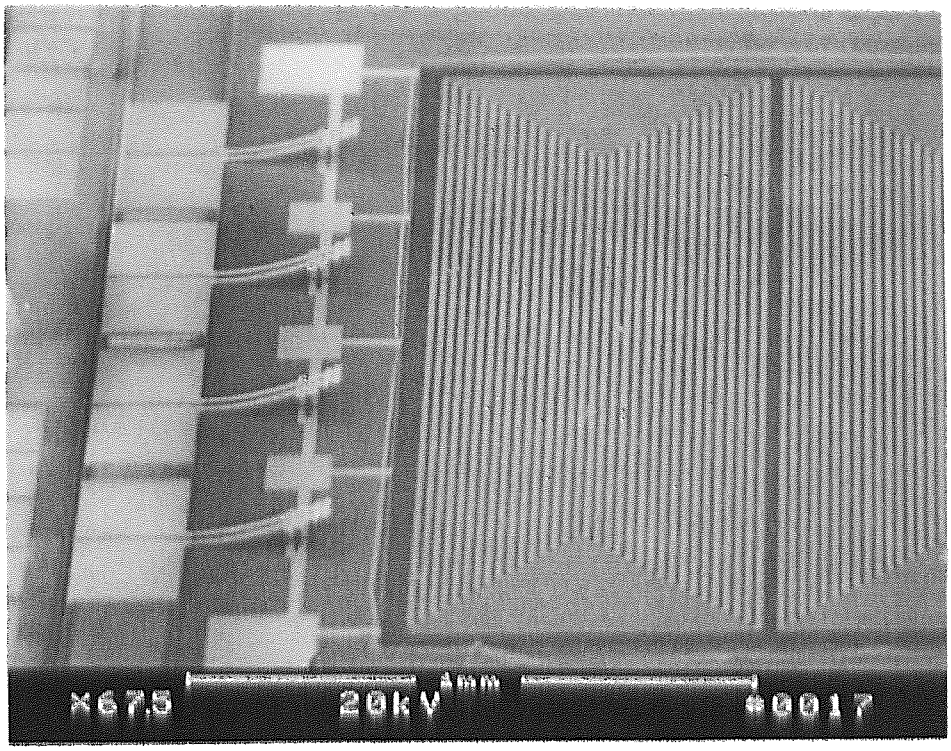


Figure 4.17 A SEM picture of the variable inductor network with a group of relay 2

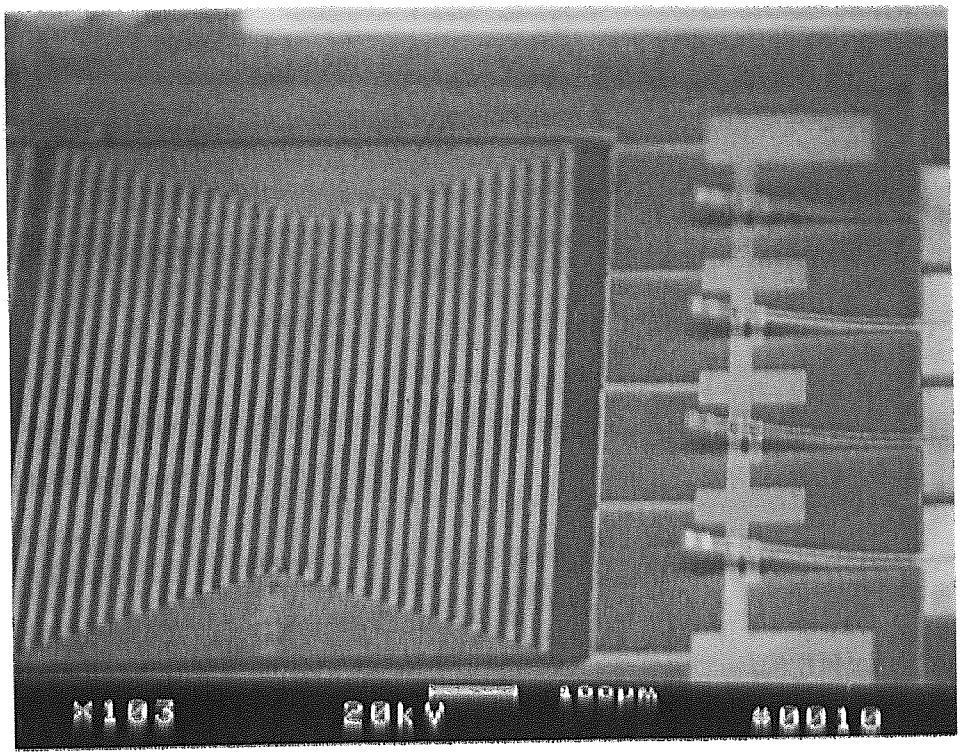


Figure 4.18 A SEM picture of the variable inductor network with a group of relay 3

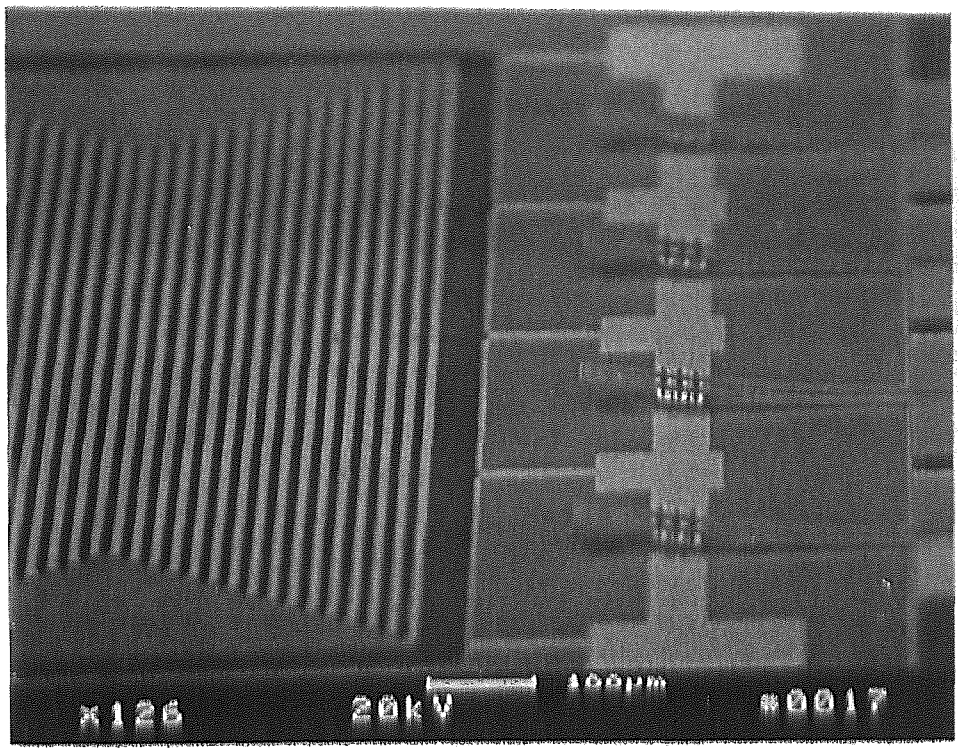


Figure 4.19 A SEM picture of the variable inductor network with a group of relay 4

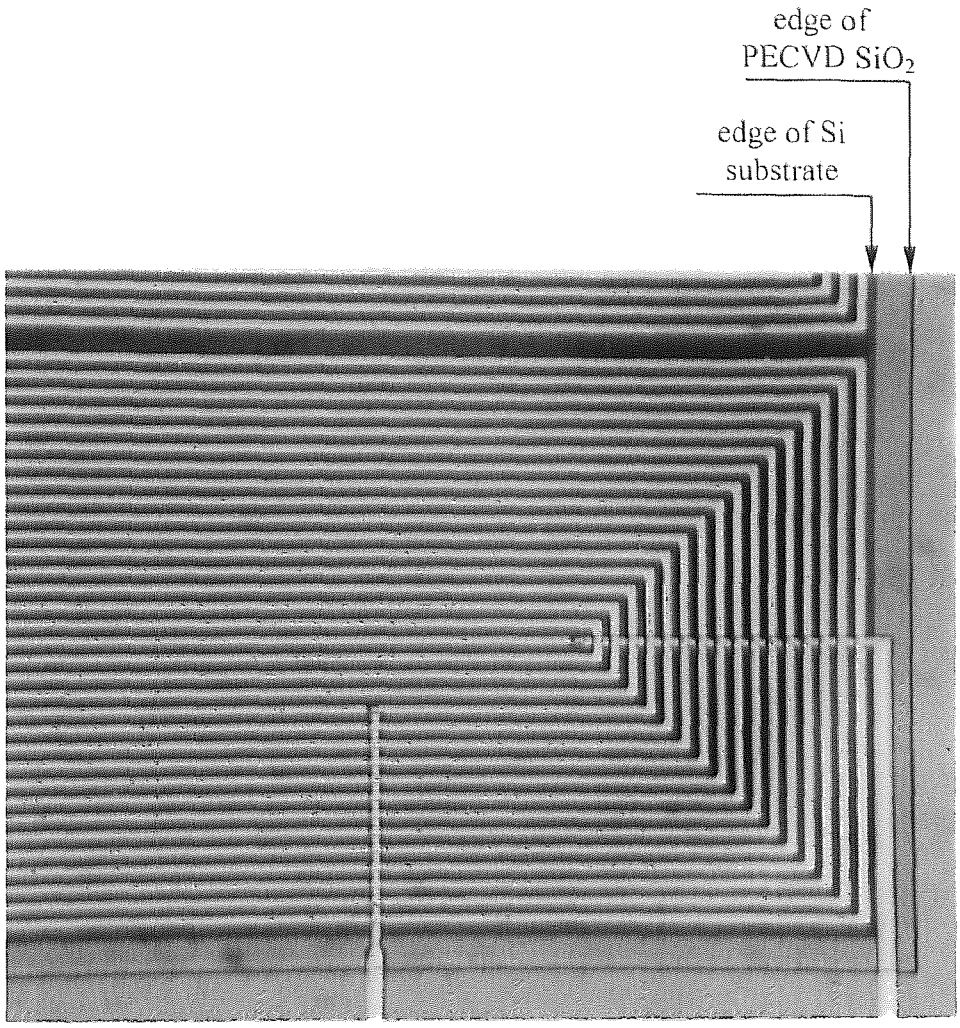
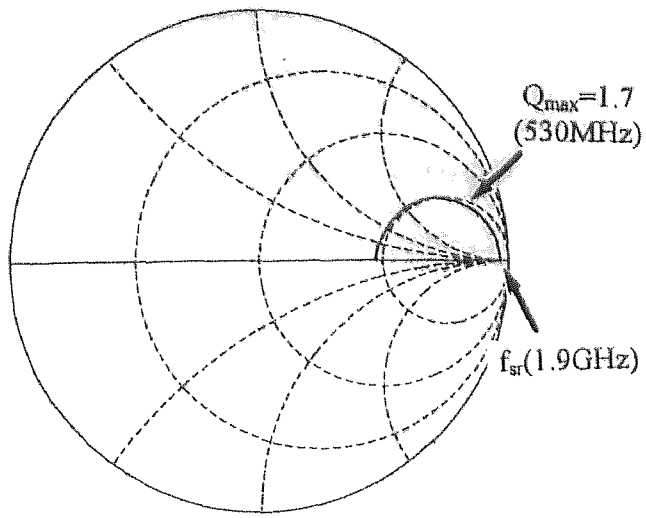
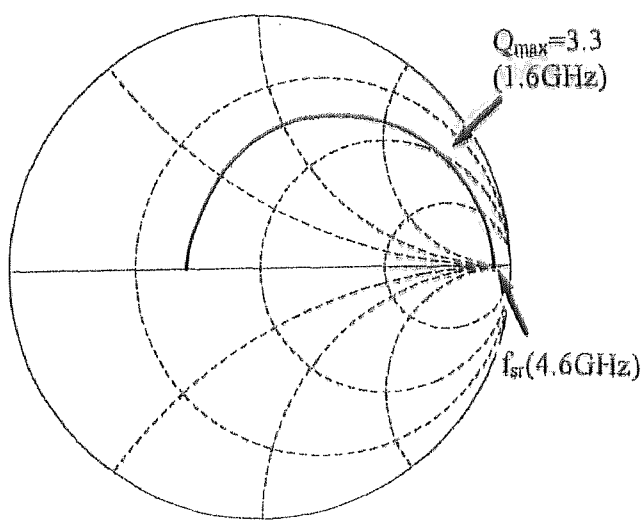


Figure 4.20 Optical photograph shows the substrate beneath inductors were etched out



(a) $D_3D_2D_1D_0$=0000



(b) $D_3D_2D_1D_0$=1110

Figure 4.21 Two Smith chart of S_{11} measurement

4.3.3 Discussions and Suggestions

The measured results of microrelays show that the relay structures with two or more contact resistance in parallel have relatively lower electrical contact resistance. The relay 4 has a low yield because of the choice of the cantilever width as 20μm which needs longer time to be released. The metal/SiO_2 interface cannot bear such a long release time in Al etchant, resulting in the peel of the contact metal which were specially happened in the metal with the narrow width.

The expanded area of the cantilever was designed to get symmetric force at the electrical contact region. The cantilever length and the expanded part length both effected the applied electrostatic voltage which was required to obtain low contact resistance. The results show that the relay 3 is the better choice compared with the relay 2 because it needed lower electrostatic voltage.

By considering all the factors of contact resistance, yield, and required electrostatic voltage, the relay 3 is obviously the best one among the four different types of microrelays.

For variable inductor network, the quality factor Q could be increased by increasing the thickness of the metal which consists of the inductor coil. This can be realized by using the method of electroplating. One more mask and two more process steps are needed for this purpose.

The linearity of the actual measured inductance versus the programmed value of inductance can be improved by changing layout design with four separated spiral coils instead of one rectangular spiral coil to form inductors L_3, L_2, L_1 and L_0. This will reduce the mutual inductance between these four inductors but increase the chip area.

CHAPTER 5

SUMMARY AND CONCLUSIONS

This research work consists of the design, simulation, fabrication and characterization of a microrelay with combined thermal and electrostatic actuation mechanisms. The research also includes the demonstration of important application in programmable inductor network. The main results are summarized and the key conclusions are as follows:

1. A microrelay with a suspended $TaSi_2/SiO_2$ bimorph cantilever beam, gold-to-gold electrical contacts, aluminum sacrificial layer, and combined thermal and electrostatic actuation mechanisms has been developed. Contact resistance ranging from 0.6 to 0.8 ohms was achieved. The thermal power and electrostatic voltage required to obtain low and stable contact resistance were 11 mW and 30 ~ 40 volts, respectively. The maximum operation frequency was 10 KHz and the microrelay closure and opening time were typically 12 μS. The lifetime was measured about 10^6 cycles based on a limited test. This is the first time that combined actuation has been demonstrated in microrelays. From the results, one observes that the combined thermal and electrostatic actuation reduces the electrostatic drive voltage requirement dramatically. However, the thermal actuation component does require a 10 milliwatt power supply as trade-off.
2. For the first time a micro variable inductor network which is digitally controlled by the microrelays has been demonstrated. The output inductance values are determined by combinations of switching states of microrelays.

Sixteen different inductance values ranging from 2.5 nH to 324.8 nH were obtained. The silicon substrate underneath the inductor region was etched out to reduce parasitic capacitance and the eddy current power loss. The minimum self-resonant frequency was measured 1.9 GHz. The measured results show that the micro variable inductor is promising for application as a programmable inductance component for microwave matching impedance networks.

3. A new type of test structure for electrical contact characterization has been developed as a support task. The contact forces ranging from 23 μN to 686 μN were created using unique stressed-microdiaphragm structure. The relation between the applied force and the electrical contact resistance was experimentally determined for different contact areas. The measured threshold forces required to get low and stable contact resistance with Pd-to-Pd contacts were 40 μN, 99 μN and 159 μN for contact area 100 μm^2, 900 μm^2 and 2500 μm^2, respectively. These results together with SEM studies have been very helpful in understanding the micro electrical contact mechanism.
4. The behavior of the microrelay has been simulated using the Rayleigh-Ritz analytical method and heat transfer theory. These results provide a useful model of microrelay actuation and were used to guide the microrelay design.
5. The process used for fabricating the micro variable inductor networks is based on seven photomasks. Surface and bulk micromachining technologies are combined to the best advantage. The overall fabrication process takes

advantage of the economies of semiconductor cleanroom batch-processing. The dimensions of the chip including the array of microrelays and the inductor network are 3150 x 930 μm^2.

APPENDIX A

MASK LAYOUT

The mask layout for microrelay types of relay 2 and relay 3 are shown from page 102 to 109. The detailed description are listed below:

Page103 Overview

Page104 Mask layer 1: underpass of inductors

Page105 Mask layer 2: define the inductor region

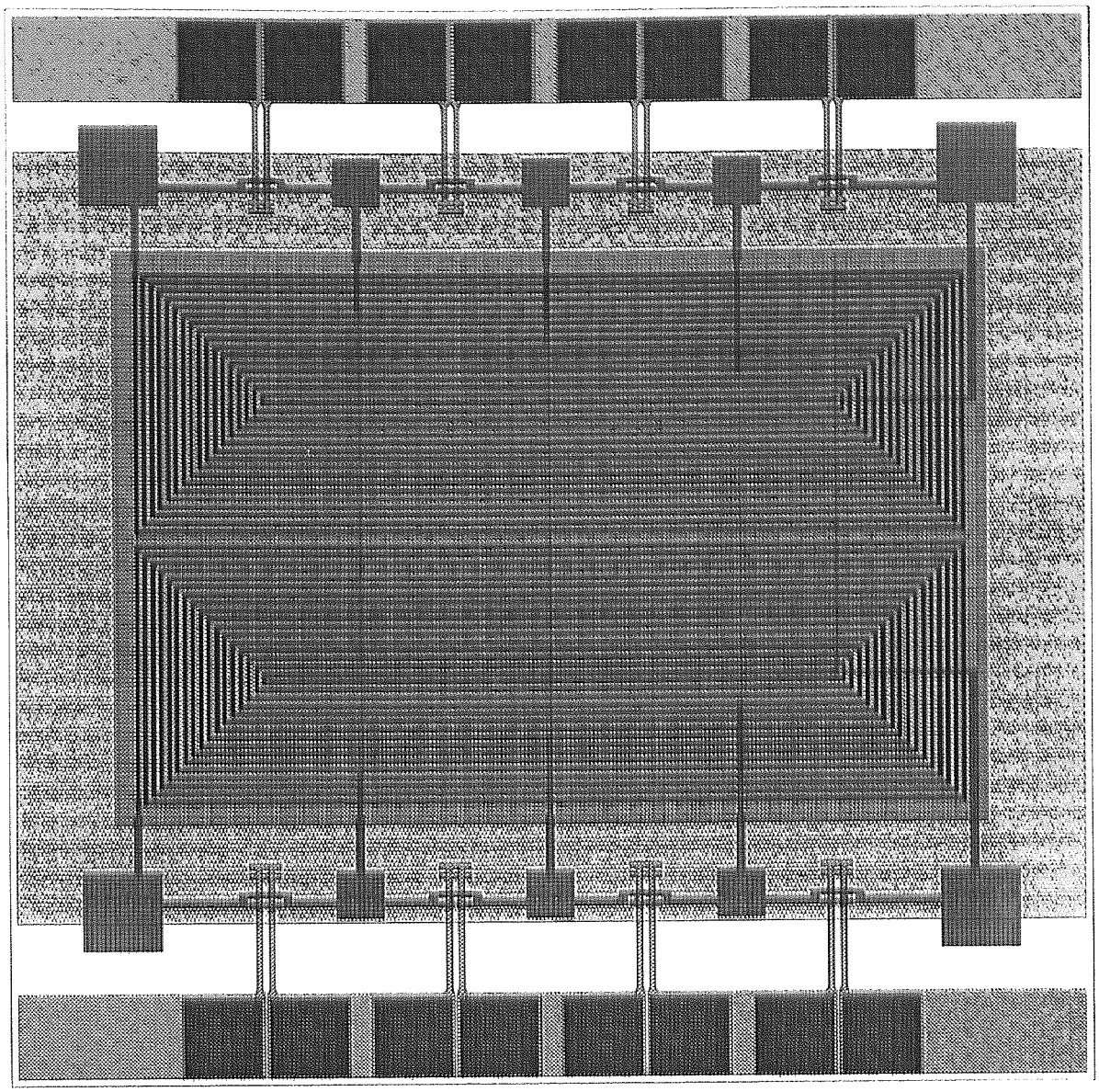
Page106 Mask layer 3: upper electrical contact metal of microrelays

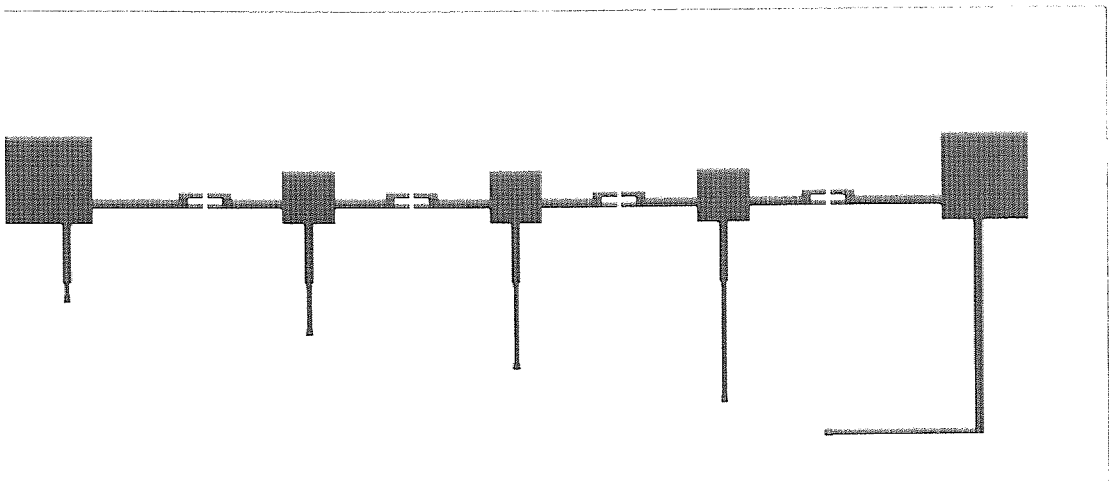
Page107 Mask layer 4: $TaSi_2$ heater

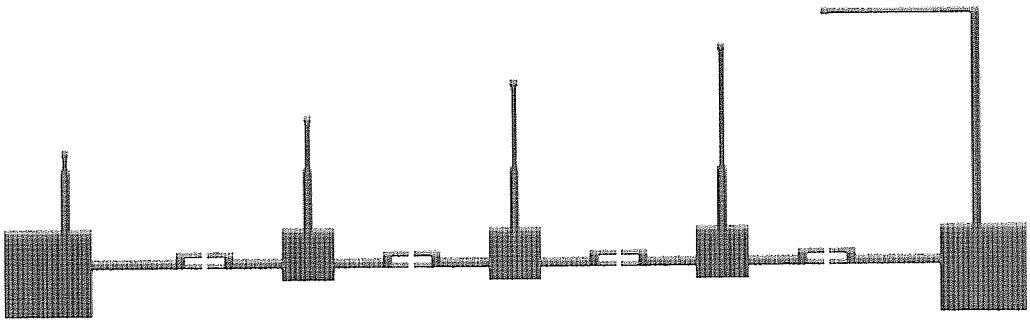
Page108 Mask layer 5: cantilever structure and via between the inductor coils and the underpasses coil taps

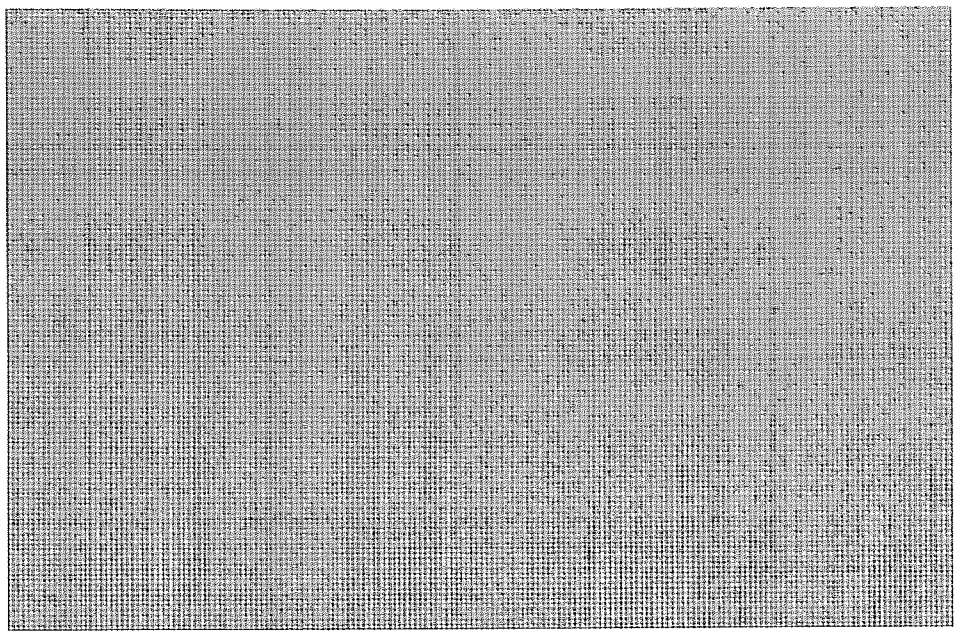
Page109 Mask layer 6: inductor coils and bonding pads of microrelays

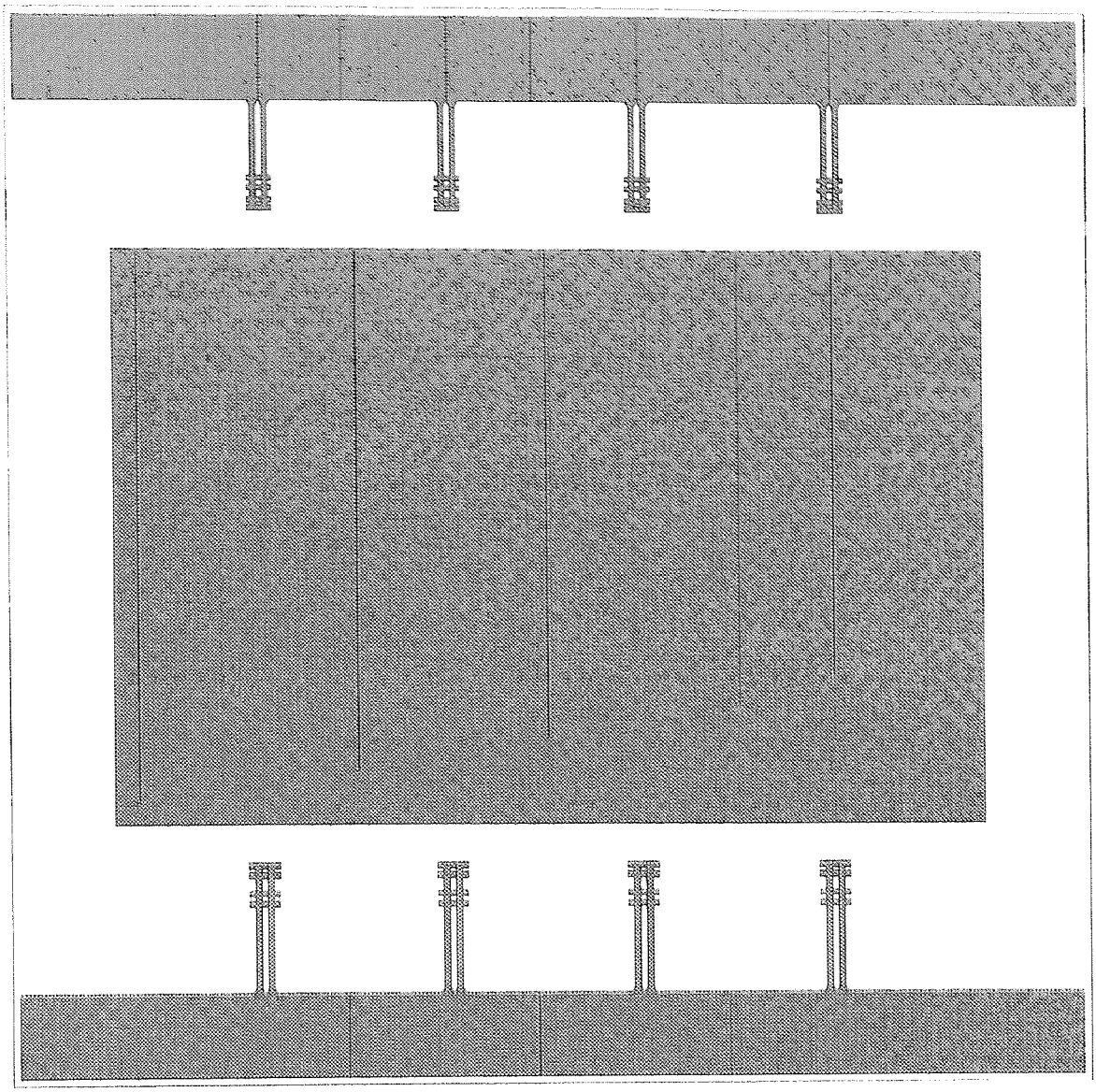
Page110 Mask layer 7: KOH etching window

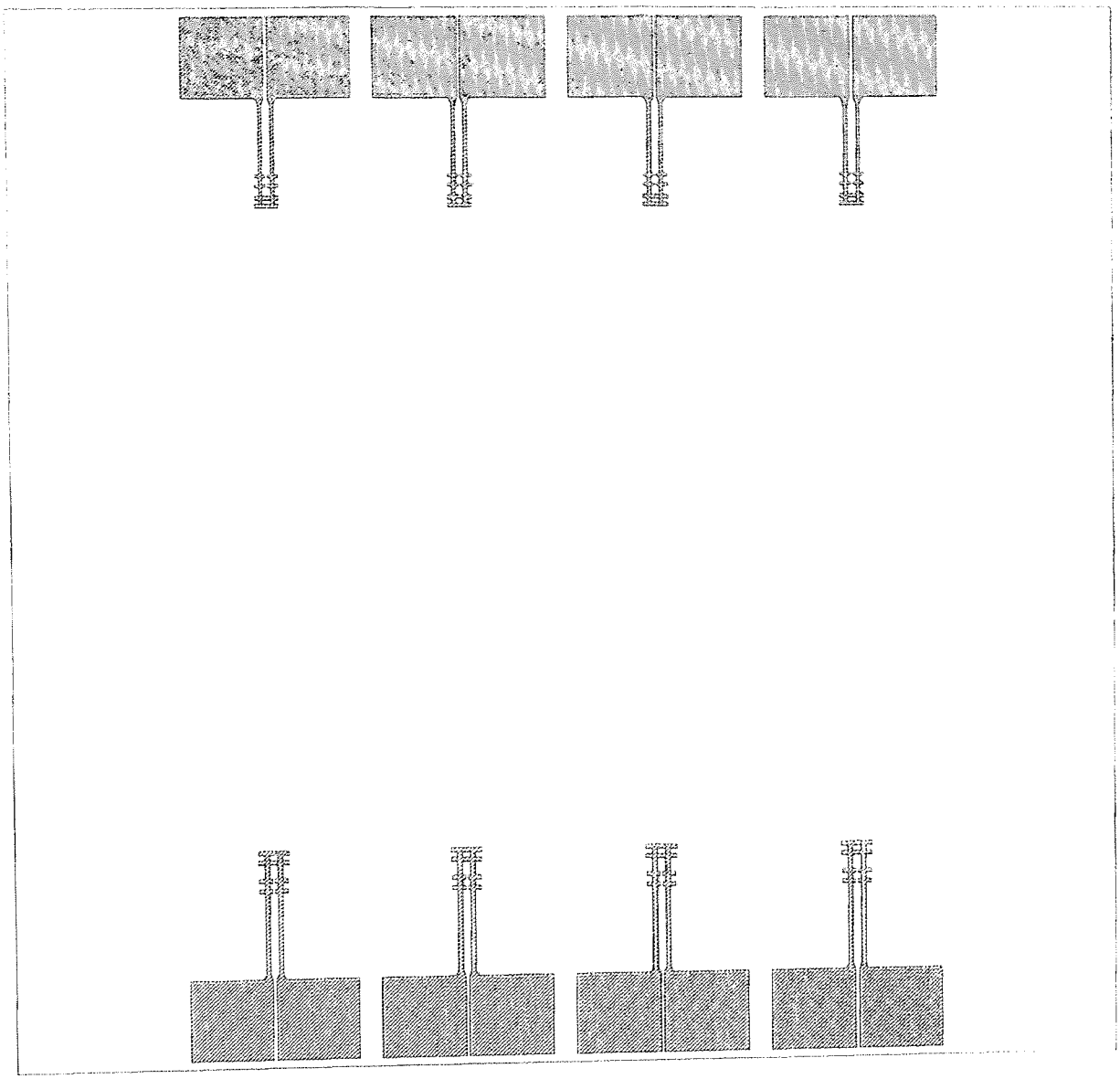


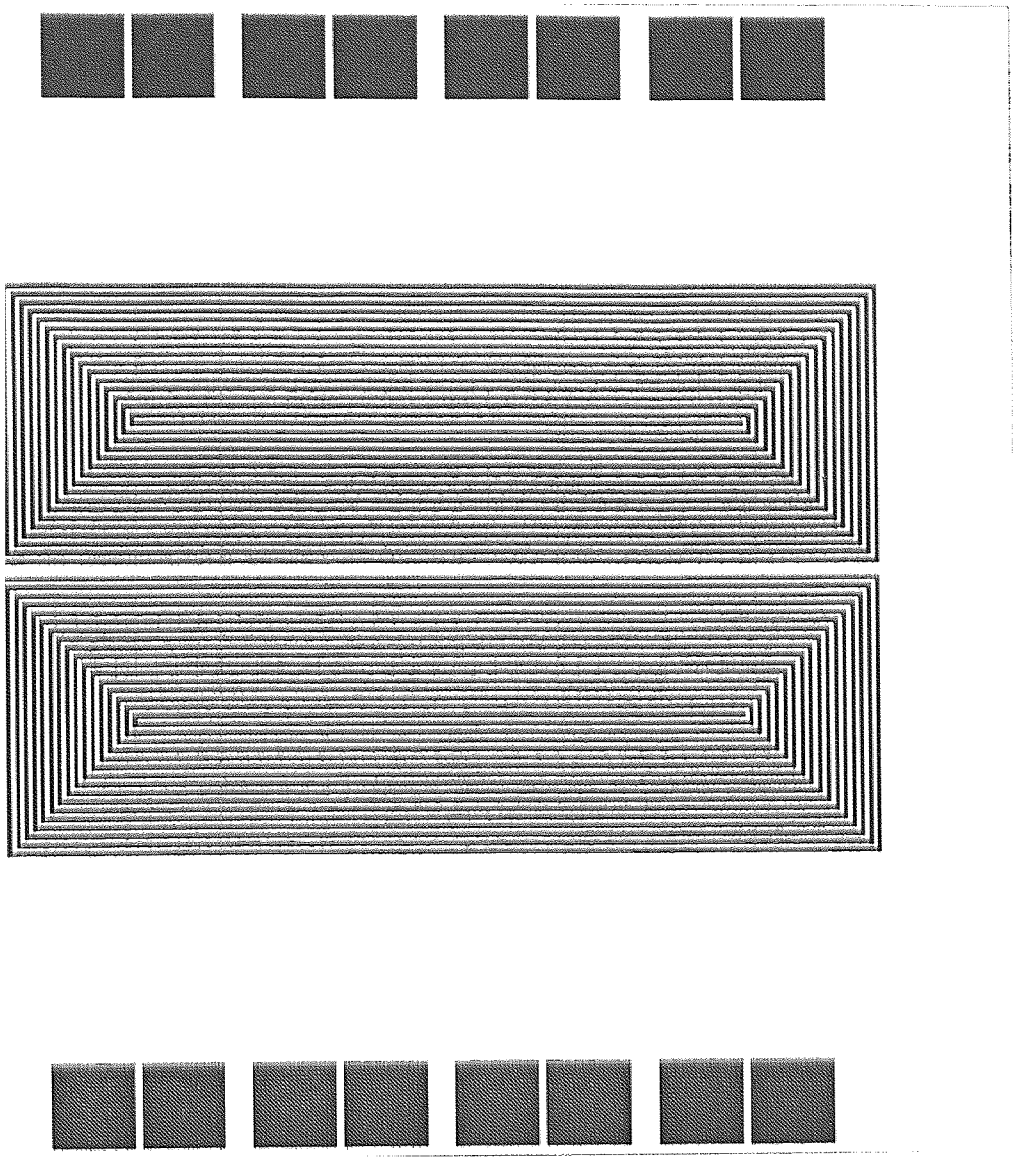


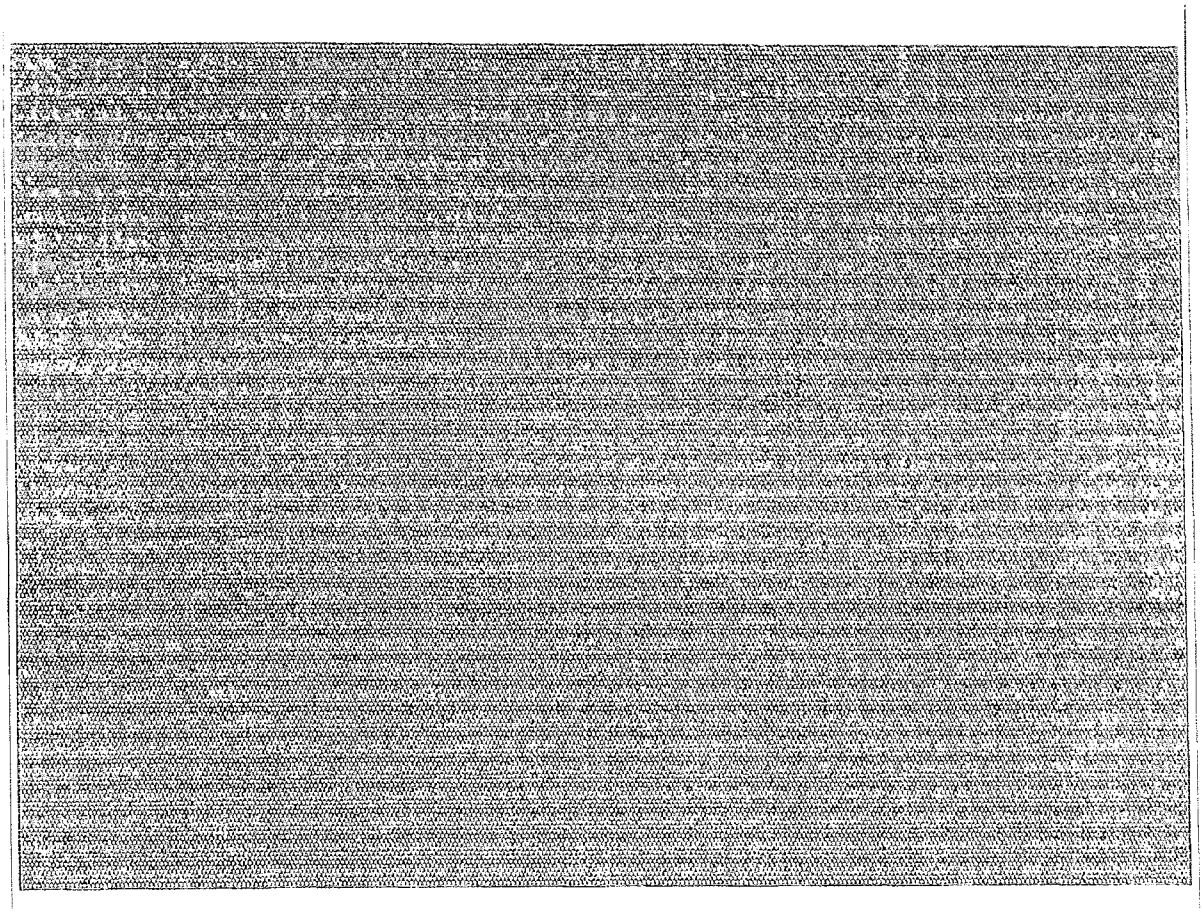












APPENDIX B

COMPUTER PROGRAM FOR THE CALCULATION OF PLANAR RECTANGULAR SPIRAL INDUCTOR

```
#include <stdio.h>
#include <math.h>
#include <stdlib.h>

double l(int);
double A(int);
double B(int);
double GMD(int, int);

#define l1 0.064
#define l2 0.208
#define w 0.001
#define s 0.001
#define t 0.0015
#define z 66

void main(void)
{
    int i, n;
    double L, L0, M, N;

    printf("i\tL0(nH)\n");
    i=0, L0=0;
    while(i<z) {
        i=i+1;
        L0=L0+2*l(i)*(log(2*(l(i)/(w+t))+0.50049+(w+t)/(3*l(i)));
        printf("%d\t%f\n". i, L0);
    }

    printf("\nn\tM(nH)\t\tN(nH)\n");
    n=0, M=0, N=0;
    while(n<z/4) {
        n=n+1;
        M=M+2*A(n);
        N=N+2*B(n);
        printf("%d\t%f\t%f\n", n, M, N);
    }
```

```
    L=L0+M-N;
    printf("\nL0(nH)\t\tM(nH)\t\tN(nH)\t\tL(nH)\n");
    printf("%f\t%f\t%f\t%f\n", L0, M, N, L);
}


/********************************** l(i) **********************************/
double l(int, i)
{
    double l;

    if(i==1)
        l=l1;
    else if(i==2)
        l=l2;
    else if(i%2==0)
        l=l1-((i+1)/2-2)*(w+s);
    return l;
}



/********************************** A(n) **********************************/
double A(int, n)
{
    int y;
    double d, gmd, p, q, Qp, Qq, F;

    d=n*(w+s);
    gmd=exp(log(d)-1/(12*(d/w)*(d/w))-1/(60*(d/w)*(d/w)*(d/w)*(d/w)));

    y=0, F=0;
    while(y<z-4*n {
        y=y+1;
        p=l(y)-n*(w+s);
        q=n*(w+s);
        Qp=log(p/gmd+sqrt(1+(p/gmd)*(p/gmd)))-sqrt(1+(gmd/p)*(gmd/p))+gmd/p;
        Qq=log(q/gmd+sqrt(1+(q/gmd)*(q/gmd)))-sqrt(1+(gmd/q)*(gmd/q))+gmd/q;
        F=F+2*p*Qp-2*q*Qq;
    {
    return F;
}
```

```
/********************************** B(n) ********************************/
double B(int, n)
{
    int a;
    double u, v, Qu, Qv, E;

    a=0, E=0;
    while(a<z-4*n+2) {
        a=a+1;
        u=l(a)-(n-0.5)*(w+s);
        v=(n-0.5)*(w+s);
        Qu=log(u/GMD(n,a)+sqrt(1+(u/GMD(n,a))*(u/GMD(n,a))))
            -sqrt(1+(GMD(n,a)/u)*( 1+(GMD(n,a)/u))+GMD(n,a)/u;
        Qv=log(v/GMD(n,a)+sqrt(1+(v/GMD(n,a))*(v/GMD(n,a))))
            -sqrt(1+(GMD(n,a)/v)*( 1+(GMD(n,a)/v))+GMD(n,a)/v;
        E=E+2*u*Qu-2*v*Qv;
    }
    return E;
}


/***************************** GMD(n,a) ****************************/
double GMD(int n, int a)
{
    double d, G;

    if(a%2==0)
        d=l1-(a/2+n-2)*(w+s);
    else
        d=l2-((a-1)/2+n-1)*(w+s);

    G=exp(log(d)-1/(12*(d/w)*(d/w))-1/(60*(d/w)*(d/w)*(d/w)*(d/w)));
    return G;
}
```

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