ABSTRACT

DESIGN AND CHARACTERIZATION OF ULTRA HIGH FRAME RATE BURST IMAGE SENSORS

by
Rakesh K. Kabra

This thesis research was aimed at investigating and designing novel architectures required for ultra high frame rate (UHFR) imagers capable of operating at frame rates in excess of 10^6 frames/sec. To demonstrate the feasibility of these architectures, a 180 × 180 element UHFR-I imager was designed and fabricated. The imager chip stored the latest 32 frames at its on-chip memory locations rather than performing a continuous readout. It was demonstrated that this architecture approach could achieve a frame acquisition rate of 2×10^6 frames/sec. Additionally, other novel design features were incorporated to minimize optical cross talk and output amplifier noise, and maximize charge handling capacity.

Two-dimensional (2-D) process and device simulations were performed to optimize optical cross talk and results compared favorably with experimental data of the fabricated chip. This tested imager was fabricated at the research laboratory of Sarnoff Corporation and had 4-levels of polysilicon, 3-levels of metal, eight implants and 21 photo mask levels. Simulations were also performed to characterize optical cross talk as a function of wavelength, optical shield aperture and epi-substrate doping. The measured value of optical cross talk was at least a factor of 40 times lower and maximum frame rate was a factor of 4 higher than previously published results for very high frame rate (VHFR) imager.

The experimental results were used to design a new 64 × 64 element UHFR-II imager with an architecture capable of an image capture rate of 10^7 frames/sec. This architecture requires only 3-levels of polysilicon and 2-levels of metal and stores the latest 12 frames at its on-chip memory locations. Simulation results indicate that a frame rate of 10^7 frames/sec can certainly be obtained.

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IMAGE SENSORS

by
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Dedicated to my parents and my lovely wife Seema

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CHAPTER 1

INTRODUCTION

Many scientific applications require image acquisition at a frame rate significantly higher than 50/60 Hz required for consumer applications. Major high frame rate imaging applications include optical wavefront measurements, explosion study and hypersonic gas turbulence imaging. The required time resolution for these applications is between $0.1\mu s$ to $1\mu s$, hence the imager should be able to capture images at the rate of 10^6 to 10^7 frames/sec.

The conventional charge coupled device (CCD) design can not achieve this speed, as the CCD transport speed and the output amplifier bandwidth is limited primarily due to gate capacitances. To overcome these limitations, various imager architectures have been devised for high frame rate imaging applications using multiport readout schemes. The maximum frame rate reported using a 32 output port design[1,2] is about 20,000 frames/sec. However, the use of many output ports makes the output signal processing and image reconstruction task extremely complex and the maximum achievable frame rate is still not adequate for the applications described earlier in this chapter.

In July 1991, Professor Walter F. Kosonocky and Mr. John L. Lowrance[3] proposed a general architecture for high frame rate CCD imaging applications. This architecture allows to capture a limited number of images at a very high speed. Subsequently, Dr. Guang Yang and Mr. Chao Ye developed an imager based on this architecture which could operate at a rate up to 500,000 frames/sec. The author led the testing team for this imager. The performance of these devices suffered from low fill

factor (~13 %), poor optical response due to large cross-talk between detector and pixel memory and limited maximum achievable frame rate of only 500,000 frames/sec.

The main objective of this dissertation is to advance the area of high frame rate imaging. There are a number of applications in numerous areas of science and engineering, which require image sensing of ultra fast transient phenomena, which would immensely benefit with the successful completion of this research.

Two new High Frame Rate Imager architectures have been invented as part of this research. First, a 180 × 180 element ultra high frame rate (UHFR-I) imager has been designed to capture images at a 2×10^6 frames/sec frame rate. This device has been fabricated at the Sarnoff Corporation and employs a process consisting of 4-layers of polysilicon, 3-layers of metal and eight implants using 21 photo mask levels. Currently, this imager is operational at Princeton Scientific Instrument Inc.(PSI), meeting all the design specifications. Second, a 64 × 64 element UHFR-II imager has been designed to capture images at a 1×10^7 frames /sec frame rate. The layout of this proposed design is complete and the devices will be fabricated at the Sarnoff Corporation using a process consisting of 3- layers of polysilicon, 2- layers of metal and eleven implants using 22 photo mask levels.

The performance of these imager structures was optimized through extensive process and device simulations. For this study, commercially available 2-D process and device simulation tools were used at the Sarnoff Corporation. The major objectives of these simulations were to minimize the optical crosstalk between the detector and pixel memory, and to achieve a very high readout speed from the photodetector structure

consistent with the required frame rate for the imager. Detailed delay timing analysis was also performed using SPICE simulations to optimize the frame rate of the imager.

Princeton Scientific Instruments, Inc. (PSI) developed the hardware, software and camera electronics for UHFR-I imager. The D.C. shorts testing of the wafers was performed at Sarnoff using automated test setup. The author led the test team and obtained all the experimental results presented in this dissertation with the help of PSI and Sarnoff.

The second chapter of this dissertation gives an overview of solid-state imaging using CCDs. This chapter reviews the definition of performance parameters used to describe CCD imagers and introduces different types of imager architectures.

The third chapter describes the design, process and operational details of UHFR-I imager. It includes design and layout of imager macropixel, output serial register and output amplifier. The process steps used for fabrication of this device are also described in this chapter followed by the operational details of the UHFR imager.

The fourth chapter reviews various techniques used to achieve 2×10^6 frames/sec frame rate and verification of layout of the UHFR-I imager. Interconnection methodology and detailed timing models are presented along with the timing delay simulation results and experimental results. Special layout versus schematic (LVS) techniques used to verify the CCD layout with its schematic are also described in the last section of this chapter.

The fifth chapter describes the process and device simulations results obtained by using TSUPREM IV and MEDICI tools for optimization of optical crosstalk. Basics of CCD modeling and simulation techniques are described first. Effect of total number of

integrated carrier, optical shield aperture, wavelength and epi-substrate doping, on optical crosstalk were studied to optimize the imager performance. The simulation and experimental results of this study are described in this chapter.

The sixth chapter describes the design, process and operational details of UHFR-II imager. It includes design and layout of imager macropixel, output serial register and output amplifier as well as delay analysis results for maximum achievable frame rate calculations.

Finally, the conclusions of this dissertation and suggestions for future research work are presented in the seventh chapter.

CHAPTER 2

FUNDAMENTALS OF SOLID-STATE IMAGING

2.1 Introduction

Solid-state imaging is based on the physical principle of converting quanta of light energy (photon) into a measurable quantity (voltage, electric current, etc.). The link between the photons at the input side of an imager and the voltage at the output side of the device is the collected and transported signal, which could be electrons or holes. Most fundamental operations in this chain are the generation, capture, and transport of this signal. With the invention of Charge-Coupled Devices (CCD) in 1970 by Boyle and Smith[4], the classical imaging tube disappeared gradually, first from the consumer imaging applications and later from the professional broadcasting scene. The ability to detect optical signals allows CCDs to be constructed into very effective self-scanned image sensors. These sensors can store and transfer the detected charge image under the control of clock pulses, yet remain free of unwanted switching-transient pick-up noise, a unique characteristic.

There are three major sections in this chapter. The first section describes the fundamentals of CCDs and image sensing. This section also gives a brief overview of photon-conversion mechanism and the subsequent electron collection. The following section defines various specifications and performance parameters, which are used to characterize CCD imagers and are used throughout this thesis. The last section describes various imager architectures for linear and area imaging applications. This study will

conclude with an overview of the advantages and disadvantages of the various architectures.

2.2 Fundamentals of CCDs and Image Sensing

The basic concept of CCDs is a simple series connection of Metal-Oxide-Semiconductor (MOS) capacitors. The individual capacitors are physically located very close to each other. The CCD is a type of charge storage and transport device in which charge carriers are stored on the MOS capacitors and transported. The charge packets can be transported from one capacitor to its neighbor capacitor under the control of digital pulses, which are applied to the top plates of the MOS structures. The input of charge packets into CCDs, their transfer through the CCDs by means of the digital clocks on the gates and the output of charge packets is illustrated in Figure 2.1.

2.2.1 Overview of Charge-Coupled Devices

The basic device physics and operation of CCDs is very well documented in several references[5,6]. This section reviews some of the important concepts of imaging using CCDs.

The basic working principle of a CCD rests on the theory of Metal-Oxide-Semiconductor capacitors. Depending on the gate voltage, the structure is forced into accumulation or into depletion. A CCD is just a line of these MOS capacitors spaced very closely together. The charge moves from one gate to another one, as these gates change under the control of gate clocks. Figure 2.2 illustrates the charge transport in a CCD.

The charge transfer or movement of free electrons from one gate to another, along the surface of the CCD is driven by three different and independent mechanisms[7]:

1) The thermal diffusion of charge carriers;

2) Self induced fields; and

3) Fringing fields.

Compared with the fringing field induced transfer, the thermal diffusion and the self-induced drift are slow processes. To operate CCDs at high speeds, devices have to be designed and operated for maximizing the benefit from the presence of fringing fields. The fringing electric field generated by the voltages on the gate forces the charge to move from OFF gate to under ON gate. When the channel potential is completely flat underneath the CCD gates, the fringing field E_f are locally zero. But when the channel potential has a certain gradient, the fringing field E_f differs from zero. The substrate doping can also influence the fringing fields. When the substrate doping is lower, the thickness of the depletion layer is greater leading to higher fringing fields.

2.2.2   Surface Channel CCDs and Buried Channel CCDs

In a real CCD structure, a certain level of inefficiency, which results in charge loss and noise, will degrade charge transport. The two major factors, which contribute to transfer inefficiency, are:

1) The finite time available to perform the charge transport; and

2) Charge trapping by the surface states.

If gate clocking is too fast or not enough fringing field is present, then due to the first effect mentioned above, some part of the present charge is left behind resulting in

incomplete transfer. The second effect which makes the charge transport no longer perfect is the trapping of charges in bulk and surface states. These trapping states are crystalline defects present throughout the silicon but are in much higher concentration at the surface than in the bulk due to Si-SiO$_2$ interface. However, these electrons do not remain trapped in the surface states indefinitely and are subsequently released. The high transport efficiencies can only be achieved if:

1) The number of surface states is low;

2) The interaction between charge and surface states is minimized; and

3) The transport of the charges is faster than the time constant of surface states filling.

All these important characteristics can be obtained if the charge transport can take place in the bulk of the silicon instead of along Si-SiO$_2$ interface. These type of devices are called Buried-Channel CCD (BCCD). In these devices, charge transport channel is designed such that the minority carriers cannot interact with the surface states and hence the charge trapping is minimized. By moving the transport channel deeper in the bulk, transport is also guided by larger fringing fields resulting in much higher charge transfer efficiency.

2.2.3 Image Sensing Using CCD

Energetic photons impinging on and penetrating into a semiconductor substrate can transfer part of their energy to the substrate. This energy transfer can take place by the generation of electron-hole pairs. If the energy content of the incoming photons is high enough, electrons will be released from the valence band to conduction band. In silicon,

if incoming photons have energy higher than 1.1 eV [band gap for silicon] or their wavelength is shorter than about 1000 nm, electron-hole pairs will be created. The easiest way to separate these electrons and holes is by applying an electric field by which the electrons are captured and the holes are drained. Figure 2.3 illustrates two alternatives, a metallurgical n+p junction (reverse biased photodiode) and an externally induced np junction (MOS capacitor). The separation of the electrons and the holes is affected by the electric field across the np junction: electrons are stored as signal charge and the holes are drained to the p-type substrate.

The next link in the imaging chain is the transport of the charge packets from the integrating sites toward the output of the device. Two alternatives are again possible and are shown in Figure 2.4, a MOS switch with a sensing line and a CCD shift register. In both cases the imaging cell or pixel is a photodiode built on a p-type silicon substrate. The technology of the CCD shift register is somewhat more complicated, and the transfer of the charge packet from the pixel towards the output diffusion needs appropriate clocking. The charge packet from the CCD shift register is transferred to the small capacitance of the output diffusion, which results in a relatively improved signal-to-noise performance.

The conversion from a charge packet to a voltage at the output node of the imager is typically done by sensing the voltage changes on a floating diffusion region by means of a source-follower amplifier.

2.3 Performance Parameters of CCD Image Sensors

This section describes various performance parameters, used to measure, characterize and evaluate CCD image sensors. These parameters have been used throughout this thesis to evaluate and characterize the ultra high-speed CCD image sensors.

2.3.1 Fill Factor

Fill factor is defined as the percentage of the total pixel area, which is photosensitive. Higher fill factor results in higher photoelectron generation for a given amount of time.

2.3.2 Optical Crosstalk

Optical crosstalk signal is generated in different ways in different types of imager configurations. The effect of this signal for different imager configurations is discussed in section 2.4 of this chapter. Fundamentally, all the "unwanted" optical coupling phenomena between detector-to-pixel or pixel-to-pixel is known as optical crosstalk. Optical crosstalk is also referred as "smear" in many references.

2.3.3 Dark Current

Dark current is defined as the thermally generated charge during the operation of the imager, which becomes part of the signal charge. Dark current can be generated at different locations in the CCD but has, in all cases, to do with irregularities in the fundamental crystal structure of the silicon. Dark-current generation is highly temperature-dependent, doubling with approximately 8°C increase in temperature. Dark

current reduces the full well capacity and the non-uniform generation of it creates a fixed-pattern noise component which is very difficult to control.

2.3.4 Charge Handling Capacity

Charge handling capacity is defined as the maximum charge packet, which can be passed through the CCD without significant degradation. Buried-channel CCD can handle only about one-third of a charge packet as compared to surface-channel CCD of similar size. This is due to the fact that buried-channel CCD stores their charge in the bulk of silicon compared to at Si-SiO$_2$ interface as in surface-channel CCD.

2.3.5 Quantum Efficiency

Quantum efficiency (QE) (η) is a practical value for comparing output of different sensors with each other. QE is defined as the number of collected electrons (E$_{total}$) divided by the number of photons (P$_{total}$) impinging on the device. The total number of electrons and photons are given by:

$$E_{total} = \frac{Q_n}{qT_{int}} \tag{2.1}$$

$$P_{total} = \frac{\Phi_0}{h\nu} \tag{2.2}$$

hence quantum efficiency is defined as:

$$\eta = \frac{Q_n hc}{qT_{int}\Phi_0\lambda} \tag{2.3}$$

Where

Q_n - is Total integrated charge;

T_{int} - is Integration time;

h — is plank's constant;

c — is velocity of light;

v — is photon frequency;

Φ_0 - is incoming photon flux; and

λ - is the wavelength of the incoming photons.

For front-illuminated conventional frame transfer CCDs with polysilicon gates,[5] the quantum efficiency has three different regions depending upon the wavelengths.

1) For wavelengths shorter than 500 nm, CCDs are somewhat insensitive. This is due to the absorption of photons in the polysilicon gates which completely covers the pixels of the CCD imager;

2) For wavelengths larger than 1000 nm, CCDs are again insensitive. Now, the photons are rarely absorbed due to large absorption depths and are penetrated deep into the bulk;

3) The region in between which is the visible spectrum, the quantum efficiency reaches its maximum of about 30% to 60%.

For Back-illuminated CCDs, the photons impinge on the silicon substrate. Hence, the quantum efficiency band is same as silicon absorption band. The maximum value of quantum efficiency could be as high as 90-100% for Si substrate with anti-reflection (AR) coating.

2.3.6 Dynamic Range

The dynamic range of a CCD image sensor is expressed as the ratio of the saturation signal of the device to the r.m.s. noise measured at the output.

2.3.7 Resolution

An important parameter of any image sensor is the spatial resolution that it provides, i.e., the ability to discriminate between closely spaced points in the image. This detection limit depends on the total number of pixels available, and the area of the device. Resolution is a measure for the highest spatial frequency, which can be resolved by the device taking a specific contrast in account.

The resolution of the device is assessed in terms of the modulation transfer function (MTF) of the output. The MTF is a combination of different modulation transfer functions, each of which can independently degrade the overall performance of the device. The main components are:

1) The diffusion MTF which describes the degradation of the device's MTF due to the possibility of miss-diffusion of the electrons generated outside the depletion layer;

2) The transfer MTF which includes the non-ideal charge transfer effects; and

3) The geometric MTF taking into the influence of the geometrical features of the pixels themselves.

2.3.8 Spectral Response

Spectral response (R) is the output response of the imager due to an optical input signal. It is defined as the ratio of the output current (I_{out}) of the sensor to the incoming light power (Φ_o).

$$R = \frac{I_{out}}{\Phi_0} = \frac{C_{FD} V_{OUT}}{A_{SF} A_{cell} T_{int} \Phi_0} \qquad (2.4)$$

Where

C_{FD} - is floating diffusion node capacitance;

A_{SF} - is gain of the source-follower structure;

A_{cell} - is area of a single pixel; and

V_{OUT} - is output voltage measured at output amplifier.

Spectral response of an imager is closely dependent on the wavelength of the incoming light as the absorption and the collection of charges depend on the energy of the photons impinging the imager surface[8]. On the other hand, the spectral response for a given wavelength is linear in relation to the integration time and the incoming photon flux.

2.4 Imager Architectures

Over the years, a number of different imager configurations have been developed for numerous applications[9]. This section describes typical architectures for area imaging. For area or two-dimensional imaging, most CCDs can be divided into frame-transfer imagers, interline transfer (IL) imagers, and frame-interline-transfer imagers.

2.4.1 Frame-Transfer CCD

Figure 2.5 shows a typical architecture of a frame-transfer type CCD image sensor. In the light-sensitive top part of the device or image section, all CCD cells are biased into the integration mode. Some of the CCD phases are connected to a high DC level so to collect photogenerated electrons and some are to a low DC level so to act as a barrier between pixels. At the end of the integration time, the CCD shift registers transfer their charge packets to the corresponding CCD lines in the storage section. Once the entire frame has been transported to the memory section, horizontal shift register can transfer charge towards the output amplifier.

By virtue of the basic principle of the frame-transfer CCD, smear is inevitable. Spurious signals are generated when the frame is transferred from image section to storage section. During this transfer, the imager is not shielded from the incoming light, charge-carrier generation continues and spurious signals are added to the charge packets in transport. To minimize the smear signal, transport from the image section to the storage section should be achieved as fast as possible.

2.4.2 Interline-Transfer CCD

Figure 2.6 shows the general interline-transfer type CCD image sensor. The integration of charge takes place in the pixels, which can be photodiodes or photogates. At the end of the integration time, the charge packets are shifted from the pixels into the vertical CCD shift register alongside. These registers are shielded from light and act as memory elements. After this transfer, a new integration period can begin and simultaneously the vertical shift registers are emptied into the horizontal-output register line by line. The

serial information in the horizontal output register is transferred to the output and consequently converted into an electrical voltage.

Interline-transfer device architectures are also not immune from smear signals but their generation phenomenon is completely different from frame-transfer devices. In the interline-transfer imagers, smear is caused by either:

1. Stray electrons generated underneath the photodiode area and diffused into the vertical CCD shift registers.

2. Stray photons, which arrive in the vertical CCD shift registers via, for instance multiple reflections at the Si-SiO_2 interface and generate electron-hole pairs locally.

2.4.3 Frame-Interline-Transfer CCD

Figure 2.7 shows the frame-interline-transfer type architecture, which is a combination of frame-transfer and interline-transfer devices. The device architectures described in subsequent chapters are based on this architecture. It has the light-sensitive area of the interline-transfer device, combined with the storage area of the frame-transfer device. Its basic operation also combines these two devices: integration of the charge in the pixels, transferring the charge packets into the vertical shift register, followed by fast vertical transport toward the shielded memory part of the imager.

CHAPTER 3

ULTRA HIGH FRAME RATE BURST IMAGE SENSOR

3.1 Introduction

This chapter describes the overall design, architecture and operation of a ultra high frame rate (UHFR-I) burst image sensor. UHFR-I is a 180×180 element, 3-phase CCD imager capable of capturing images at a maximum rate of 2×10^6 frames/sec and stores the last 32 integrated frames at its on-chip storage pixels. This imager has been fabricated at Sarnoff and is operational at PSI Inc. This device design is conceptually based on a device architecture invented by Professor Walter F. Kosonocky and Mr. John L. Lowrance for high frame rate imaging applications. The previous work consists of a very high frame rate (VHFR) imager architecture with a maximum achievable frame rate of about 500,000 frames/sec. The author was extensively involved in the testing and development of the camera system for these devices[10]. The performance of VHFR devices was severely degraded due to high level of optical crosstalk between photodetector and storage area. The UHFR-I imager not only improves the frame rate by a factor of 4 as compared with VHFR imagers, but it also offers numerous performance enhancements of parameters such as fill-factor, charge handling capacity, noise performance and optical crosstalk.

3.2 Design of UHFR-I Image Sensor

3.2.1 Specifications

This UHFR-I imager was designed for adaptive optics applications. The initial specifications for this imager were:

Table 3.1 *UHFR-I Imager Design Specifications*

Maximum Frame Rate	2×10^6 frames/sec
Resolution	180 x 180
Frame Storage Memory	32 frames
Pixel Size	$< 100 \times 100 \ \mu m^2$
Fill Factor	> 40 %
Saturation Signal, Q_{max}	$> 40,000 \ e^-$/pixel
Dynamic Range	2000:1
Spectral Response	250 to 900 nm
Readout Noise	< 10 rms e^-/pixel
Technology	3-phase BCCD, 4-level poly, 3-level metal
Design Rules	1.5 μm

3.2.2 Chip Architecture

The general block diagram of the 180×180-element UHFR-I burst imager is shown in Figure 3.1. The chip size is approximately 19.2×19.2 mm^2. Due to the large chip size, the imager was divided into two halves, (Q_Left and Q_Right) to improve the yield as these two halves could also be operated completely independent of each other. Each half consists of 90 x 180 macropixels, output serial register, and floating-diffusion and on-chip amplifier.

As shown in the block diagram, two halves of the imager have separate outputs and can be operated independently. The integrated frames can be reconstructed with these two outputs outside the chip. There is a common gate, which acts as a separator to

two output serial registers. It is also possible to move the charge in only one direction, either left or right by applying high DC bias on common gate and appropriate clocking of serial registers. If one of the output amplifiers does not function properly, this feature of the chip allows both halves to be readout using the other output amplifier; thus further improving the yield. Each macropixel consists of a photodetector and 32 storage elements. The photodetector generates the charge, which is moved to macropixel memory at a very high speed. This operation is similar to inter-line-transfer imagers. Once the new image acquisition is stopped, imager operates as a frame transfer imager and charge moves to output serial register line-by-line. Output serial register moves the charge to floating diffusion pixel-by-pixel at a slow speed to improve signal to noise ratio, as bandwidth of the floating diffusion amplifier is limited. The operation of the imager is described in more detail in subsequent sections. Figure 3.2 illustrates the basic operation of this imager by showing charge movement in 2×2 macropixel in combination of output serial register and amplifier.

3.2.3 Pixel Design

Figure 3.3 shows a schematic diagram of two macropixels. Each macropixel has a dimension of 92.2 μm × 92.2 μm. A macropixel consists of a photodetector PD, a charge collection gate G1, antiblooming gate G2, a drain D, charge transfer gate G3, and a storage of 32 pixel elements in the form of an array of 4×8 pixels. The first row of 4 pixels is also called serial-parallel (SP) register.

The photodetector is designed to be of 45-μm wide and 71-μm long. This design achieves a fill factor (i.e., ratio of the light sensitive area to the total area of the

macropixel) of 37%. The drain D (n^+ diffusion) is used for control of blooming (i.e., to drain excessive charge above the saturation signal from the PD) during the integration time under the control of gate G2. During the normal frame acquisition mode, gate G1 is biased high to collect electrons generated in PD. At the end of the integration time, charge is moved from G1 to SP register via gate G3. Once the SP register is full, charge is moved to the next row of the memory. This process continues till all the 32 memory pixels are full. The drain D is also used to dump excess frames from SP register of the adjacent macropixel. Using this strategy, the imager is able to continuously store last integrated 32 frames and all previously stored frames get dumped into the macropixel drains as new frames get stored. Thus, when frame acquisition is stopped, latest 32 frames are available in macropixels memory.

To achieve an area-efficient layout, the design of the 3-phase CCD SP register uses four levels of polysilicon. This is due to the fact that during serial transfer, SP register needs to be isolated from surrounding memory arrays and during parallel transfer, it needs to be isolated from gate G3. This could be most efficiently performed using four levels of polysilicon as shown in Figure 3.4.

The SP register phases S1, S2, and S3 are designed using poly-2, poly-3, and poly-4, respectively. During the parallel transfer, the charge is transferred in P register, phase S3 (poly-4) acts as the induced channel stop and phases S1 and S2 are clocked as phase P1 of the P register. During the horizontal transfer, phases P2 and P3 (poly-1) act as induced channel stop.

3.2.4 Output Serial Register Design

Output serial (OS) register is a 3-phase CCD structure, which allows the transfer of charge signal from 90 × 180-macropixel array towards a single output amplifier. Transferring in one line of information at a time and moving the charge towards the output amplifier pixel by pixel performs this operation. Figure 3.5 shows a schematic diagram of OS register along with a macropixel and output amplifier. The OS register was also designed with four levels of polysilicon, as is operationally similar to the SP register. During the vertical transfer, OS3 (poly-4) acts as induced channel stop. During horizontal transfer, phase P1 (poly-1) acts as induced channel stop.

3.2.5 Output Amplifier Design

Output amplifier is one of the most critical sections in a CCD imager design as its performance greatly affects the overall CCD performance. The two important parameters associated with output amplifier design are output amplifier noise and output amplifier sensitivity. Figure 3.6 is the schematic diagram of the output stage used in this UHFR-I imager. OS1 and OS3 are OS phases, OG1 and OG2 are the output control gates, RS is the reset gate, V_{rsd} is the reset drain voltage and V_{out} is the signal output voltage.

During normal operation, the output control gate OG1 is biased to a DC voltage, the output signals are periodically clocked out to the floating diffusion (FD) by controlling the voltage of OS3 to be higher and lower than OG1 bias. The clocked out signal is sensed at the FD and pre-amplified by the on-chip source follower and Vout is sampled by off-chip correlated double sampling circuitry. The FD is reset to a known voltage after each charge sampled by the reset gate RS.

Output Amplifier Noise

The output stage is used to convert the charge electrons into a voltage and to buffer the output voltage towards the outside world. It also adds some uncertainty to the signals in the form of noise electrons. The overall noise from the output amplifier can be split up into various elements depending on the mechanism by which it is generated. The noise characteristics of the output stage can be separated into thermal noise, reset noise, and 1/f noise.

Inherent to the reset action of the floating-diffusion capacitance is an uncertainty about the voltage on the capacitor C_{FD}. The uncertainty or reset noise can be quantified and is equal to kTC_{FD}. The only way to deal with the reset noise is to "measure" its value and compensate for it off chip. This is done using a method known as Correlated-Double Sampling (CDS)[5]. The output signal of the CCD is sampled twice; once for its reset level and once for its actual signal output. One of these samples is subtracted from the other, the video signal remains, and the reset noise is canceled out. An additional component in the reset noise is the channel layer charge underneath the gate of the amplifier transistor. When the transistor is turned off, this charge has to be directed to either FD or reset drain to diminish the inversion layer. This uncertainty causes some extra voltage fluctuation from one reset operation to the other[11].

Output Amplifier Sensitivity

Apart from the noise of the output amplifier, the conversion factor or sensitivity, which is expressed as μV/electron is a very important parameter. A large conversion factor

prevents extra signal-to-noise reduction caused by peripheral signal processing circuits. Dumping the electrons on a floating-diffusion capacitor and subsequently sensing them by means of on chip source follower performs the conversion of charge into voltage. The sensitivity is primarily determined by the value of the floating-diffusion capacitance in parallel with the parasitic capacitances associated with the source follower gate and the metal buses.

There are a number of techniques used in the design and layout of the output stage of UHFR-I imager to minimize noise and improve sensitivity. To reduce the clock pick up and readout noise at FD, the reset is achieved by keeping the gate OG2 at a DC bias and periodically resetting the FD by a minimum length gate RS. The gate OG2 shields the reset transistor from the floating-diffusion and drastically reduces the clock feed-through from RS on C_{FD}. The partitioning noise is minimized by an appropriate design of the reset transistor BCCD channel as funnel-shaped as shown in Figure 3.7. In this configuration, the narrow-channel effect pushes the electrons out of the inversion channel towards the reset-drain side during the switching-off of the reset transistor and thus reduces the partitioning noise on the floating-diffusion. The capacitance of the FD and parasitic capacitances have also been minimized by various layout techniques and optimized design achieved by using thick oxide (field oxide) around the critical areas to improve the sensitivity.

3.3   Process for UHFR-I Burst Image Sensor

3.3.1   Process Technology

The UHFR-I burst-image sensors were fabricated by Sarnoff using a 1.5 μm three-phase

buried-channel CCD technology with four level polysilicon and three levels of aluminum.

As described in sections 4.2.4 and 4.2.5, the use of fourth level of polysilicon facilitates a

more efficient design and operation of serial-parallel register at macropixel and output

serial register. Two levels of aluminum were used for metal interconnection and the third

level of aluminum was used as an optical shield to cover the CCD pixel area. Also,

SiO_2/Si_3N_4 channel dielectrics were used to improve the charge transfer efficiency and

possibly yield.

Arsenic and phosphorus dual-implantation was used to form the BCCD channels

on a p-type substrate to maximize the charge handling capacity and to achieve high

fringing field for low transfer losses[11]. Since arsenic has a small diffusion coefficient,

majority of the implanted arsenic will stay near the Si/ SiO_2 interface and form a high

concentration n-type layer. The arsenic contributes to the larger charge handling capacity

of the BCCD well. On the other hand, phosphorus has a large diffusion coefficient,

therefore, the implanted phosphorus forms a deep diffusion responsible for large fringing

field which improves charge transfer efficiency. A modified form of pinned-buried

detector was used as high-speed photodetector[12] at each macropixel using a thin p^+

implant, the BCCD implant, and three additional n-type implants to achieve less than 0.1

μsec readout time.

3.3.2 Process Specifications

The process specifications for fabrication of the UHFR-I burst-image sensor are summarized below:

- The UHFR-I burst image sensors were fabricated using nominally 17.5-μm thick p-type epi wafer with resistivity of 43 ohm-cm on <100> CZ p^+ substrate with resistivity in the range of 0.008 to 0.025 ohm-cm.

- Four levels of polysilicon are used for BCCD gates.

- Three levels of metal, of which two metal levels are used for interconnections and one for optical shield of the BCCD region excluding the photo sensitive (detector) region.

- A dual dielectric of SiO_2/Si_3N_4 is used.

- BCCD implants consisting of phosphorus and arsenic.

- The channel stops for BCCD channels have been defined by SCCD regions in the form of the p-type substrate without the BCCD implant.

- The pinned-buried graded photodetector was constructed by BCCD implant with three additional n-type implants and a top thin p^+ implant.

- The n^+ diffusions for blooming/dumping drain and source drains are defined by polysilicon gates surrounding the diffusion area.

- As a general design/layout procedure, the pinned-buried photodetector, the output amplifiers, and whenever possible the outside perimeter of the burst-image sensor were surrounded by a P^+ field implant.

3.3.3 Fabrication Sequence

The process for fabrication of the UHFR-I burst image sensor includes four levels of polysilicon, three levels of metal, eight implants, and requires a total of 21 mask levels.

Mask level 1:   ACT, defining the active area;

Mask level 2:   VTFN, p-type implant below the recessed thick oxide;

Mask level 3:   THOX, defining the thick oxide;

Mask level 4:   BCCD, BCCD implants;

Mask level 5: p^+ field implant surrounding the photodetector, output amplifiers, and the imager perimeter;

Mask level 6:   POLY-1, BCCD polysilicon-1 gates and output source follower MOSFET gates;

Mask level 7:   POLY-2, BCCD polysilicon-2 gates;

Mask level 8:   POLY-3, BCCD polysilicon-3 gates;

Mask level 9:   POLY-4, BCCD polysilicon-4 gates;

Mask level 10:   DET-1, first photodetector additional n-type implant, covering the whole photodetector region;

Mask level 11:   DET-2, second photodetector additional n-type implant, forming the first potential step in photodetector;

Mask level 12:   DET-3, third photodetector additional n-type implant, forming the second potential step in photodetector;

Mask level 13:   DET, photodetector p^+ implant, forming the pinned-buried BCCD channel photodetector;

Mask level 14: N^+, source and drain N^+ implants;

Mask level 15:   C2PL, defining contacts from metal-1 to polysilicon gates;

Mask level 16:   AACT, active area contacts, including contacts to source and drain, as

well as to the substrate;

Mask level 17:   MTL-1, metal-1 interconnection lines;

Mask level 18:   VIA, VIAs between metal-1 and metal-2;

Mask level 19:   MTL-2, metal-2 interconnection lines;

Mask level 20:   MTL-3, metal-3 optical shield; and

Mask level 21:   BPAD, bonding pads.

The alignment of the 21 mask levels and fabrication sequence of the UHFR-I imager are illustrated in Figure 3.8, where the mask levels are denoted by the mask names described above, and the process sequence is given by number from 1 to 21.

3.4   Operation of UHFR-I Imager

3.4.1   Photodetector Readout

Figure 3.9 shows the photodetector and surrounding control gates of a macropixel in different states. Figure 3.9(a) shows the schematic diagram of the photodetector and surrounding control gates. Figure 3.9(b) shows the charge integration mode in which charge collecting gate G1 acts as a sink for the photodetector charge. If the generated charge is higher than the maximum charge handling capacity of the smallest BCCD storage element, the extra charge is dumped into the drain under the control of gate G2, the blooming gate. This ensures that the maximum charge collected under the gate G1 is not higher than the maximum charge, which can be stored at macropixel memory.

A periodical transfer of the charge from gate G1 to gate G3, and eventually to SP register phase S2 performs the readout of the collected charge signal. During this operation, gate G2 acts as a barrier to prevent charge transfer from G1 to drain as illustrated in Figure 3.9(c). The drain shown in Figure 3.9 is also used by the adjacent left macropixel to dump the extra signal charge when its all-32 memory pixels are full. This operation allows all the macropixels to retain latest 32 signal samples with all previous samples discarded into the drain. This charge dumping is illustrated along the B-B' line in Figures 3.9(b) and (c). As the serial clock S1 is turned on, the charge signals clocked out by the SP register of the macropixels move into the adjacent drain.

3.4.2   Frame Integration and Readout

During frame integration mode, imager can continuously capture images at the maximum speed of 2×10^6 frames/sec and stores the last 32 frames at its macropixel memory locations. As the new frames are acquired, previously integrated frame charges are continuously drained in the on chip drain thus macropixel always stores the latest 32 frame signal. By virtue of the architecture of the macropixel, transfer of the first frame each time after row above SP register is full, is the most critical operation from speed point of view. This operation requires a parallel to serial transfer which is illustrated in Figure 3.10. During this operation, when the last row of signal from the upper pixel is transferred to SP register under S1 gates via S3 gates to be eventually dumped in the drain, the new integrated frame signal is entering into SP register via G3 gate. To avoid this bottleneck, these frames, i.e., 1st, 5th, 9th, 13th, 17th, 21st, 25th, and 29th frames could have subframe integration. In this mode, integration time is doubled and gate G2 is

used to empty gate G1 after half of this increased integration time. This ensures that the actual signal integration time remains the same for all frames and overall maximum frame rate could be achieved.

During the frame readout period, the frame acquisitions are stopped and gate G3 acts as a barrier between gate G1 and SP register. The entire new signal collected under gate G1 from photodetector is directly dumped into the drain. The SP register acts as one of the parallel phases and imager gets reconfigured as a large frame-transfer type imager. Signal gets transferred line by line into OS register and from OS register, and moves pixel by pixel towards output amplifier to be readout. This operation could be performed at a slow rate to improve the transfer efficiency.

3.5 Experimental Setup and Results

Following the completion of the design and simulation (described in Chapter 4 and 5) of the UHFR-I Imager and based on the process described in this chapter, a wafer lot was fabricated at the Sarnoff Corporation. After the successful completion of this lot, the operation of this imager was demonstrated at the Princeton Scientific Instruments (PSI), Inc. using camera electronics developed by PSI. The author led the test team and obtained the experimental data for UHFR-I imager as well as some earlier test devices and are described in this section.

Test Setup and experimental results

The test setup developed by PSI for UHFR-I Imager demonstration used an optical test pattern, which is illuminated by a sequence LED pulses. The imager chip is cooled to -

30° C to minimize the dark current. The required control clocks for the imager as well as LED is controlled by programmable hardware/software. This set-up allows to change frame rate, voltage levels on various phases, LED ON time, and readout speed. The output of the imager is readout by an external dual-slope correlated-double sampling electronics to eliminate the reset noise. After the analog-to-digital conversion, the acquired data is stored in the host computer. The host computer does all the processing required in reformatting the acquired 32 frames and displays them on a monitor. For the imager readout rate of 120 kHz, the total readout time is about 8 seconds. An optical shutter is used to eliminate the optical smear during this readout time. The switching time of the shutter is about 20 msec. The experimental results obtained are summarized in the following table. The test results of this imager have met all of the design specifications.

Table 3.2 *Experimental Results from UHFR-1 Imager*

Maximum Frame Rate	$>2 \times 10^6$ frames /sec
Resolution	180 x 180
Frame Storage Memory	32 Frames
Pixel pitch	92.2 µm
Fill Factor	38 %
Saturation Signal, Q_{max}	~15,000 e-/pxel
Dynamic Range	>2000:1
Spectral Response	400 to 900 nm
Readout Noise	9 rms e-/pixel
Optical Cross-Talk	Atleast 40 times improved over VHFR
CTE	~2x10^{-5} in Output Serial Register
Output Amplifier Char.	~2.2 µV/electrons
Technology	3-phase BCCD, 4-level poly, 3-level metal
Design Rules	1.5 µm

In conclusion, the UHFR-I device can acquire images at a very high frame rate and stores the last 32 of these frames at its on-chip memory locations. Once the new image acquisitions are stopped, the stored frames could be readout at a slower speed. The operation of these devices was demonstrated at 2-million frames/sec speed and experimental results are described in this chapter. Next chapter discusses the various design techniques used to optimize the imager for its high-speed operation.

CHAPTER 4

FRAME RATE OPTIMIZATION AND DESIGN VERIFICATION

4.1   Introduction

This chapter describes the full custom design methodology used for layout design of the

UHFR-I imager chip.   Large chip size (19.2 mm × 19.2 mm) and the specification of

extremely high frame rate (2 × 10^6 frames/sec) makes the layout and verification task

extremely complex.   At present, there is no in-built verification support available on

electronic design automation (EDA) tools for CCD devices as all these tools are primarily

developed for analog and digital CMOS design verification.   Special techniques to verify

layout against schematic were developed for CCD chips as part of this research and are

described in this chapter.

The RC time constants of different CCD phases are extremely critical in achieving

2 × 10^6 frame rate.   These time constants were optimized using full custom layout

methodology.   Two metal layers were used for interconnection purpose to give more

freedom in routing and minimizing RC time constants.   The 180 × 180-element UHFR-I

chip has a 32-pixel memory at each macropixel, and hence the total number of pixels for

the imager is 1.0368 million.   Since a 3-phase BCCD technology was used, the chip has

3.11 million poly gates.   To ensure that layout corresponds to the conceptually drawn

schematic, automated layout versus schematic (LVS) verification tools were used.

Mentor Graphics V 8.2_5 IC design tools running on SUN Sparc 10 machine were used

for this chip layout.   Detailed RC delay timing analysis was performed using SPICE

simulation models to ascertain target frame rate of 2 × 10^6 frames/sec.

4.2 Interconnection Methodology

To have a systematic approach for interconnection of this complex chip, metal-1 is used for horizontal interconnection and metal-2 is used for vertical interconnection. Critical phases of this chip were separated from non-critical phases to minimize RC delay of critical phases using various layout techniques.

4.2.1 Macropixel Interconnection

Figure 4.1 shows a complete macropixel layout. Each macropixel has a size of 92.2 × 92.2 μm^2 and has 10 clock phases, which are connected to the bond pads. To have an area efficient layout which meets timing requirements, 4 less critical clocks are interconnected using metal-1 buses, which run horizontally. Metal-2 buses are used to interconnect six critical clock phases running vertically, due to its lower capacitances compared to metal-1. In this design 10 contacts and 6 vias are used at each macropixel location. The chip is divided into completely independent two halves, left and right, to improve the speed (by minimizing the poly layer capacitance) and the yield. The major advantage of running critical buses vertically is that these buses can be double-end connected, reducing the capacitance loading in half. This feature is illustrated in next section. Figure 4.2 shows the contacts, vias, and metal interconnections in a macropixel. The 4 horizontal buses are G1, G2, G3 and drain. The 6 vertical buses are P1, P2, P3, S1, S2, and S3.

4.2.2 Chip Interconnection

Figure 4.3 shows the metal-1 (horizontal) and metal-2 (vertical) layers used to interconnect four of the macropixel clocks to the bond pads. Figure 4.4 shows the metal-1 (horizontal) and metal-2 (vertical) layers used to interconnect six of the macropixel clocks to the bond pads. As shown, these six macropixel lines are double ends connected to the outside buses to reduce the capacitance loading.

4.3   Timing Analysis

The RC delay constant of each macropixel clock phase determines the maximum achievable frame rate of the overall imager. The task of achieving the maximum frame rate (2×10^6 frames/sec) is divided into two parts:

1.   During the macropixel layout, utmost care is taken to minimize the capacitance of clock phases by efficient layout design; and

2.   Using innovative interconnection methodology, slower clocks are double ends connected so that the metal width for these phases does not become extremely wide at the expense of larger chip size.

The RC constant of each driving clock phase is dependent on the resistance of the interconnecting metal layer and the poly line, and the capacitance of metal-to-metal, poly-to-poly, poly-to-metal, and poly-to-substrate. By virtue of the structure of the macropixels, some clock phases, such as P1, P2 and P3, have a larger gate area than other phases. The capacitance of these polysilicon gates is much larger due to larger area and hence resistance of its metal buses needs to be minimized, to keep RC delay constant. The maximum frame rate achievable is dependent on the slowest phase, hence it is

important to keep RC constants of all the slower phases in the same range. The RC delay

constant of each macropixel phase has been calculated using following steps:

1. Calculate the unit capacitances between each layer based on the inter layer dielectric

   thickness. These parameters can then be incorporated in the process rules file of

   layout tool. Then, using the layout tool, extract the exact resistance and capacitance

   values of each clock phase based on the drawn layout.

2. Define the interconnection structure used for each clock phases. Model the structure

   as distributed R and C nodes.

3. Generate a SPICE netlist from the structure created in step 2. Simulate the RC delay

   time by applying a step response at the input. Output response generates the rise and

   fall time delays.

4.3.1 RC Delay of Each Driving Clock Phase in Macropixel

<u>**Unit Capacitance Between Each Layer**</u>

The dielectric used between metal-to-metal, poly-to-poly, and ploy-to-metal layers are

SiO$_2$. The capacitance per unit area is calculated by the appropriate planar capacitance,

which is given by:

$$C = \frac{\varepsilon_r^{oxide} \varepsilon_0}{d_{oxide}}$$ (4.1)

Where d_{oxide} is the thickness of the oxide layer and ε_0 and ε_r^{oxide} are the absolute

permittivity and relative permittivity of oxide respectively.

The unit capacitance between polysilicon to silicon substrate has two values. The

first is the capacitance between polysilicon to BCCD channel, which is calculated as a

serial connection of the capacitance of gate oxide, nitride, and BCCD channel. The BCCD channel thickness is about 1294 A°. This capacitance is given by:

$$\frac{1}{C} = (\frac{d_{oxide}}{\varepsilon_r{}^{oxide}} + \frac{d_{nitride}}{\varepsilon_r{}^{nitride}} + \frac{d_{BCCD}}{\varepsilon_r{}^{Si}}) \frac{1}{\varepsilon_0}$$ (4.2)

Where $d_{nitride}$ and d_{BCCD} are the thickness of the nitride and BCCD implant, respectively.

The second major capacitance component is between polysilicon to SCCD channel stop, which is calculated as a serial connection of the capacitance of gate oxide and nitride layer. It is given by:

$$\frac{1}{C} = (\frac{d_{oxide}}{\varepsilon_r{}^{oxide}} + \frac{d_{nitride}}{\varepsilon_r{}^{nitride}}) \frac{1}{\varepsilon_0}$$ (4.3)

The capacitances per unit area obtained by Equations (4.1), (4.2), and (4.3) are given in Table 4.1.

Total capacitance of each clock phase in macropixel

Mentor Graphics layout tools can extract the resistance and capacitance of each clock phase in the macropixel layout. To extract these parameters, sheet resistance of different layers (poly-1, poly-2, poly-3, poly-4, metal-1, and metal-2) and unit capacitances values from Table 4.1 were included in the process rules file. To simplify the delay estimation, resistance of metal layers and capacitances of poly layers are used as other layer values are insignificant as compared with these dominating values.

The macropixel clock phase capacitances and output serial register clock capacitances are given in Table 4.2.

Table 4.1 *Unit area capacitances between layers of UHFR-I Process*

RELATED LAYERS	CAPACITY PER UNIT AREA (fF/μm^2)	RELATED LAYERS	CAPACITY PER UNIT AREA (fF/μm^2)
Poly-to BCCD	0.3065	Poly_2-to-Metal_3	0.0123
Poly-to SCCD	0.4917	Poly_3-to-Poly_4	0.2300
Poly_1-to-Poly_2	0.2305	Poly_3-to-Metal_1	0.0416
Poly_1-to-Poly_3	0.1501	Poly_3-to-Metal_2	0.0192
Poly_1-to-Poly_4	0.1279	Poly_3-to-Metal_3	0.0128
Poly_1-to-Metal_1	0.0367	Poly_4-to-Metal_1	0.0443
Poly_1-to-Metal_2	0.0182	Poly_4-to-Metal_2	0.0192
Poly_1-to-Metal_3	0.0123	Poly_4-to-Metal_3	0.0128
Poly_2-to-Poly_3	0.2303	Metal_1-to-Metal_2	0.0345
Poly_2-to-Poly_4	0.1501	Metal_1-to-Metal_3	0.0182
Poly_2-to-Metal_1	0.0384	Metal_2-to-Metal_3	0.0384
Poly_2-to-Metal_2	0.0182		

Table 4.2 *Pixel level capacitances of all clock phases*

Clock Phase	Pixel Capacitance (fF)	Clock Phase	Pixel Capacitance (fF)
G1	77.7	S1	187.3
G2	52.1	S2	120.9
G3	63.3	S3	137.1
P1	659.5	OS1	648.1
P2	943.8	OS2	829.1
P3	923.3	OS3	768.1

4.3.2 Metal Connection Structure and Delay Modeling

The RC delay of all of the phases primarily depends on the resistance of metal wires and capacitance of poly gates, which acts as a load to these wires. In the UHFR-I design, clock phases have several different metal connection structures. In general, metal-1 and metal-2 lines are running horizontally and vertically, respectively. The schematic

diagrams of different structures and its equivalent SPICE models are described in this section.

Structure-1

This structure is used for macropixel clock phases, which are connected by metal-1 layer. Clock phases G1, G2, G3 and drain have this structure. The schematic diagram of this structure and equivalent RC delay model is illustrated in Figure 4.5(a) and (b), respectively. Following notations are used in Figure 4.5:

R_{M20}, C_{M20}:   Resistance and capacitance of metal-2 bus between two rows of macropixels.

R_{M21}, C_{M21}:   Resistance and capacitance of metal-2 bus in the upper side of the bonding pad.

R_{M22}, C_{M22}:   Resistance and capacitance of metal-2 bus in the lower side of the bonding pad.

R_{M23}, C_{M23}:   Resistance and capacitance of metal-2 bus in the upper side of the first row of macropixels.

R_{M24}, C_{M24}:   Resistance and capacitance of metal-2 bus in the lower side of the lowest row of macropixels.

R_{P0}:   Resistance of metal-1 bus to the first column of macropixels.

R_P, C_P: Resistance and capacitance of each macropixel.

Structure-2

This structure is used for macropixel clock phases, which are connected by metal-2 layer. Clock phases P1, P2, P3, S1, S2, and S3 have this structure. The schematic diagram of

this structure and equivalent RC delay model is illustrated in Figure 4.6(a) and (b), respectively. Following notations are used in Figure 4.6

R_{M21}, C_{M21}:	Resistance and capacitance of metal-2 bus in the lower side of the bonding pad.
R_{M10}, C_{M10}:	Resistance and capacitance of metal-1 bus between two columns of macropixels.
R_{M11}, C_{M11}:	Resistance and capacitance of metal-1 bus before the first column of macropixels.
R_{P0}:	Resistance of metal-1 bus to the first row of macropixels.
R_P, C_P:	Resistance and capacitance of each macropixel.

Structure-3

The output shift registers, which are driven by clock phases OS1, OS2, and OS3, have only one row of interconnected arrays. The schematic diagram of this structure and equivalent RC delay model is illustrated in Figure 4.7(a) and (b), respectively. Following notations are used in Figure 4.7:

R_{M21}, C_{M21}:	Resistance and capacitance of metal-2 bus in the lower side of the bonding pad.
R_{M10}, C_{M10}:	Resistance and capacitance of metal-1 bus between the output shift register cell.
R_{M11}, C_{M11}:	Resistance and capacitance of metal-1 bus before the first output shift register cell.
R_S, C_S:	Resistance and capacitance at each output shift register cell.

4.3.3 Timing Simulation

The rise/fall time delay simulation can be performed based on the RC delay models for these phases as discussed in section 4.3.2. The capacitance of all the driving clock phases C_P are given in Table 4.. The value of R_P can be extracted from the layout tool which depends on the sheet resistance of the metal, width of the metal in macropixel and macropixel size (92.2 µm). The resistance and capacitance related to all other metal segments are calculated based on its equivalent length and width, which is different for different phases.

To estimate the maximum achievable driving frequency for each clock phase, the worst case analysis needs to be performed. The delay analysis of such a massively distributed RC circuit can be performed by two ways:

1. Use SPICE to simulate the rise/fall delay time for the phase in the inner most macropixel in the equivalent RC model shown earlier. This analysis reflects the worst case response of the particular phase. The rise/fall time is defined, as the time required for gate voltage swing from 10% to 90% of its final value.

2. Using Π-net approximation to simplify the equivalent RC model and calculate the rise/fall delay of the gate in the inner most macropixel.

For timing simulation, Π-net approximation technique was used and results were verified by using Spice simulations. In the Π-net approximations, the array row is modeled as a lumped connection of five R and C components. The driver and load of the model is approximated as having 50% of R and C values of these 5 blocks.

Table 4.3 shows the rise/fall time as well as the total capacitance and equivalent resistance of the clock phases for the UHFR-I imager.

The results presented in Table 4.3 shows that clock phases P2 and P3 have the largest rise/fall time of 0.0895 and 0.0876 μs, respectively. For a three-phase CCD, the minimum period of a clock phase is about 6 times of its rise/fall time. Thus, the estimated maximum operating frequency of the imager is about 2 MHz.

4.4 Verification Techniques

Once the chip layout is complete, it needs to be verified with a conceptually drawn schematic to ensure that none of the metal interconnections and poly gates are missing or incorrectly connected. This technology is popularly called as Layout versus Schematic (LVS) checking. Direct LVS at chip level is extremely complex as more than a million polysilicon gates are used in UHFR-I imager layout. To circumvent this problem, macropixel layout is independently verified with its equivalent schematic. After this step, at the chip level, LVS is performed to check correct interconnection from bonding pads to macropixel level. At this stage, no poly gate verification is performed to simplify the problem. The other blocks of the imager, output serial register and output amplifier is also independently verified similar to the macropixel.

In IC layout design tools, there is no in-built support to perform LVS for a CCD chip. These tools has built in models to recognize PMOS and NMOS transistor layouts but can not recognize CCD gates due to missing source and drains. For the verification of this CCD chip, a special CCD model using existing models for MOS transistors was developed with help of Dr. Don Sauer and Dr. Fu-lung Hsueh (Sarnoff). This approach allows checking various CCD structures, the sequence of different layers of polysilicon as well as polysilicon line connections. Basically, each CCD gate is considered as

equivalent to an MOS device. CCD structure of different polysilicon layers as gate materials are considered as different types of MOS devices. For four polysilicon layers of CCDs, four types of MOS devices are defined as ND1 (for poly-1), ND2 (for poly-2), ND3 (for poly-3), and ND4 (for poly-4). Each polysilicon layer is overlapped with other polysilicon layers in CCD region. The polysilicon overlapping area is considered equivalent to the source-drain region of MOS device. Polysilicon region other than the overlapping region is considered as equivalent to the gate of MOS device. For the first and the last CCD structures, one side of the polysilicon layer is not overlapped by other polysilicon layer.

In order to have an equivalent source-drain region for the CCD structure, it is necessary to have a pseudo layer, which provides the overlapping region on the polysilicon gate. This technique provides a simple way to check the CCD structures by considering them as the MOS devices in linear CCD array. Figure 4.8 shows the example of single channel CCD linear array with triple poly layers and its equivalent MOS circuit. The shaded regions are equivalent to the source-drain regions due to poly overlapping or pseudo overlapping area at the edges of CCD structures.

For the case when multiple CCD channels are merged, which is very common in CCD applications, there are more than two CCD 'source-drain' regions associated with the merged polysilicon gate. No existing device symbol can represent the CCD structure at the merged node. The solution is first to split the merged poly gate into multiple gate regions associated with the multiple channels. At the same time an equivalent MOS circuit for the merged CCD structure is created. Figure 4.9 shows two examples of merged CCD structures to illustrate how to split the merged gate and to create an

equivalent MOS circuit. The shaded region is added to split the merged gate into multiple gates and to create a common output source-drain region. For example, two merged channels as in Figure 4.9(a), the shaded area splits the gate into two gates for channels 1 and 2, and also serves as the common output node. In Figure 4.9(b), the shaded region split the merged gate into three gates for channels 1, 2, and 3, and serves as the common output node. The equivalent MOS circuits clearly illustrate the CCD configurations. Figure 4.10 shows the equivalent schematic developed using the techniques described in this section for LVS checking of the macropixel layout shown in Figure 4.1.

In conclusion, various timing optimization and design verification techniques were developed for UHFR-I imager design and were discussed in this chapter. Apart from these structural techniques, research was also performed to optimize the electrical performance of the device. Extensive device and process simulations were also performed to optimize UHFR-I imager design and these are discussed in next chapter.

Table 4.3 *RC Delay Analysis for UHFR-1 Clock Phases*

Clock Phase	Connection Structure	Metal-1 Width (μm)	Metal-2 Width (μm)	C_{total} (nF)	R_{equiv} Ω	Computed $\tau_{rise/fall}$ (μsec)	Simulated $\tau_{rise/fall}$ (μsec)
G1	Structure-1		12	0.631	27.66	0.0383	
G2	Structure-1		10	.422	33.192	0.0308	
G3	Structure-1		30	0.513	11.064	0.0125	
P1	Structure-2	65	150	5.34	6.043	0.0710	0.122
P2	Structure-2	80	150	7.645	5.324	0.0895	0.135
P3	Structure-2	80	150	7.478	5.324	0.0876	0.166
S1	Structure-2	30	50	1.517	14.936	0.0499	0.109
S2	Structure-2	30	50	0.978	14.936	0.0322	0.101
S3	Structure-2	50	80	1.111	9.128	0.223	0.098
OS1	Structure-3	60		58.334 (pF)	4.149	0.532 (ns)	9.0 (ns)
OS2	Structure-3	50		74.616 (pF)	4.978	0.817 (ns)	9.2 (ns)
OS3	Structure-3	40		69.127 (pF)	6.223	0.946 (ns)	9.2 (ns)

CHAPTER 5

DEVICE PERFORMANCE OPTIMIZATION AND EXPERIMENTAL RESULTS

5.1 Introduction

Charge coupled devices (CCDs) are used in various imaging systems to transport charge generated at the pixels of the imager to an amplifier where the charge packets are converted to an equivalent electrical signal. Some of the key CCD design parameters include the the maximum charge that the CCD can transmit, the charge transfer efficiency, the maximum clock speed, optical crosstalk and the minimum pixel size that can be used to fabricate the CCD. The two most critical issues associated with the design of UHFR-I imager architecture are the clocking speed and the optical crosstalk. Clocking speed, which determines the maximum achievable frame rate of these devices, is described in detail in the Timing Analysis section of Chapter 4. Crosstalk, which is also known as smear or diffusion MTF degradation, is a spurious signal which softens (reduces sharpness) the image for normal frame-transfer and interline-transfer area imagers. Visual effects of crosstalk are totally different for UHFR-I devices because of its unique macropixel architecture. This issue is described in a separate section of this chapter.

A number of process and device simulations were performed to understand, optimize and predict various performance parameters of the UHFR-I imagers. This chapter begins with a brief review of the process and device modeling for the CCD technology. Effect of crosstalk on these devices simulated for performance optimization is described in a separate section. Extensive simulation results and experimental results

are summarized in the following section. The simulations were performed with the TMA Company tools that include TSUPREM IV and MEDICI, which are 2-D process simulator and 2-D device simulator, respectively.

5.2 Review of CCD Modeling and Simulation Techniques

The buried channel and the surface channel CCDs are the most commonly used CCD structures. The buried channel devices have the advantage that there is less chance for electrons to become trapped in interface states, which lie along the $Si-SiO_2$ interface boundary. This is because, in buried channel device, electrons are transported deeper in the bulk, while in a surface channel device, electrons are transported along the $Si-SiO_2$ interface. Implanting an N-type region just under the $Si-SiO_2$ interface forms the buried channel. This N-type region creates a potential maximum below the surface. Charge flows horizontally in this region rather than at the surface. The depth of this well is a function of the gate bias, dielectric thickness, the number of electrons in the well, and the doping concentration of the n region. The maximum number of electrons, which the wells can hold and transfer properly, determines the maximum charge handling capacity of the CCD. In a typical CCD device, this number is determined when the electrons overflow the barrier region or fill the buried channel to the point where a large number of electrons exist at the surface. It has been well established that if the transfer barrier height (V_b) (the potential difference between the well and the channel stop or adjucunt gate) remain greater than the thermal energy 10 kT/q, the CCD will operate correctly.

The process simulation program (2-D SUPREM IV) is used to replicate actual process conditions and generate a device structure. The device simulation program

MEDICI analyzes the device structure generated by SUPREM IV by solving the Poission and Continuity equations in two dimensions. MEDICI can therefore analyze charge transfer in the CCD. The detailed description of these tools can be found in SUPREM IV user's manual[63] and Medici user's manual[64], and only the most relevant models are summarized in this section. In the static case when no charge transfer is occurring and no current is flowing in the CCD, Medici can determine the empty well potential conditions. When the current is zero, the electron and the hole quasi fermi potentials are set to be constant throughout the device since the current is proportional to the gradient of the quasi fermi potential.

When the simulation program performs a zero-carrier analysis, the continuity equations are not solved and the electron and hole quasi fermi potentials are set to constant values. The electron and hole concentration is given by:

$$n = n_{ie} \exp[(\psi_F - \phi_n)\frac{q}{kT}] \tag{5.1}$$

$$p = n_{ie} \exp[(\phi_p - \psi_F)\frac{q}{kT}] \tag{5.2}$$

The potential is determined by solving the two-dimensional Poission equation:

$$\nabla^2 \varepsilon \psi_F = -q(p - n + N_D - N_A) \tag{5.3}$$

Where

n_{ie} - is the intrinsic carrier concentration;

ψ_F - is the fermi level potential;

ϕ_n - is the conduction band potential;

ϕ_p - is the valance band potential;

q – is the electronic charge;

T – is the temperature;

k – is the bolzmann's constant;

N_D - is the donor concentration; and

N_A - is the acceptor concentration.

Using these equations, the program can determine the maximum number of carriers which can be placed in the well while maintaining $V_b > 10kT/q$. The time dependent charge transfer simulation is performed by first creating a zero carrier simulation to generate an appropriate number of carriers[13]. After this, a 2-carrier time dependent simulation is performed to simulate the charge transfer by solving both continuity equations.

From the analytical point of view, the charge transport of the minority carriers through CCD channel is analyzed by means of the current density and continuity equations. The current density equation is given as:

$$J(y,t) = J_d + J_s + J_f \qquad (5.4)$$

Where

$J(y,t)$ - is the due to the movement of charge packet in distance and time;

J_d – is the current density due to thermal diffusion;

J_s – is the current density due to self-induced drift; and

J_f – is the current density due to fringing field.

These three current component expressions are:

$$J_d = qD_n \frac{\partial Q_n(y,t)}{\partial y} \qquad (5.5)$$

$$J_s = Q_n \mu_n E_s \qquad (5.6)$$

$$J_f = Q_n \mu_n E_f \qquad (5.7)$$

Where

D_n - is the diffusion constant of electrons;

$Q_n(y,t)$ – is the charge distribution as a function of place and time;

μ_n – is the mobility of electrons;

E_s – is the self-induced electric field; and

E_f – is the fringing field.

The continuity equation which relates the amount of charge to be transferred with the current density is given by:

$$\frac{\partial Q_n(y,t)}{\partial t} = \frac{\partial J(y,t)}{\partial y} \qquad (5.8)$$

The distribution of charge and movement in the structure is analyzed by solving these fundamental equations.

5.2.1 Basics of Optical Absorption

This section describes the optical absorption phenomena in the semiconductors. This subject has been reviewed in detail by S. M. Sze[14]. When the semiconductor is illuminated, photons are absorbed to create electron-hole pairs as shown at (a) in Figure 5.1(a) if the photon energy ($h\nu$) is equal to the bandgap energy (E_g). If $h\nu$ is greater than E_g , an electron-hole pair is generated and, in addition, the excess energy ($h\nu$ - E_g) is dissipated as heat as shown at (b) in Figure 5.1(a). Both of these processes are called intrinsic transitions. On the other hand, for $h\nu$ less than E_g, a photon will be absorbed

only if there are available energy states in the forbidden bandgap due to chemical impurities or physical defects as shown in (c) in Figure 5.1(a). This process is called extrinsic transition. This discussion also is generally true for the reverse situation. For example, an electron at the conduction band edge combining with a hole at the valence band edge will result in the emission of a photon with energy equal to that of the bandgap.

Assume that a semiconductor is illuminated from a light source with $h\nu$ greater than E_g and a photon flux of Φ_0. As the photon flux travels through the semiconductor, the fraction of the photons absorbed is proportional to the intensity of the flux. Therefore, the number of photons absorbed within an incremental distance Δx as shown in Figure 5.1(b) is given by $\alpha\Phi_0\Delta x$, where α is a proportionality constant defined as the absorption coefficient. From the continuity of photon flux as shown in Figure 5.1(b), it could be derived that $\Phi(x) = \Phi_0 e^{-\alpha x}$.

The absorption coefficient α is a function of photon energy $h\nu$ or wavelength. Figure 5.1(c) is a plot of absorption distance (α^{-1}) as a function of wavelength for silicon. Table 5.1 lists the measured values of absorption distance at various wavelengths at 300K for silicon material. In general, absorption distance values increase approximately exponentially as the wavelength is linearly increased. Photons with low $h\nu$ (larger wavelengths) can penetrate much deeper in the substrate before being absorbed. Photons, which are absorbed deeper in the substrate, are the dominant source of optical crosstalk in UHFR devices.

Table 5.1 *Absorption length of Silicon at 300K*

Wavelength (nm)	α^{-1} (μm)
413.3	.122
495.9	.541
574.0	1.52
659.5	3.28
708.5	4.90
756.0	6.68
826.5	13.16
880.0	25.0
940	50

5.2.2 Model for Diffusion Crosstalk

A simple one-dimensional photodetector model consists of a depletion region at the surface and, underneath the depletion region, a semi-infinite neutral region of uniform minority carrier diffusion length. Diffusion response is defined as the collection of the carriers generated in the neutral region into the depletion region, where they become part of the total integrated signal. However, it is this portion of the response that gives rise to virtually all of the crosstalk observed in silicon imaging devices. The diffusion response is predominant at the higher wavelengths for front-illuminated devices because the absorption length (α^{-1}) is the higher.

In a simple case, an infinitesimal diameter beam of collimated monochromatic radiation at normal incidence on a large area-imaging device could be considered. Photoelectrons generated in the neutral region will, on the average, diffuse laterally a distance comparable with the depth of generation measured from the top of the neutral region and then be collected in the depletion region at the nearest potential minimum. This process is the basis of the crosstalk model.

The most useful form of the characterization of this crosstalk is the modulation transfer function (MTF) factor. This is obtained by spatially integrating the above lateral diffusion process over a sine wave modulated large area of irradiation[14]. The most prominent feature of the optical crosstalk characteristic of most silicon imaging devices, is a large decrease in MTF as the wavelength is increased from approximately 800 nm to approximately 900 nm in front-illuminated devices.

5.3   Crosstalk in UHFR-I Devices

Crosstalk is a phenomenon, which adds spurious signal into a pixel's integrated charge. In the earlier VHFR devices, the imager performance was severely degraded due to the optical crosstalk between photodetector and the frame storage area of the macropixels during the frame integration mode. It should be noted that during the frame integration mode, the high frame rate (HFR) device operation is similar to an interline-transfer imager. In the design of UHFR-I imager, a major effort has been made to understand the physical parameters responsible for optical crosstalk generation and optimize the design to minimize it. This section describes the source of the crosstalk and the techniques used to minimize it.

5.3.1   One-Dimensional Simulation Model for Crosstalk

The crosstalk in UHFR-I device can be explained with a cross-sectional drawing of the macropixel along A-A' line of Figure 4.1[Macropixel layout of UHFR-I chip] and is shown in Figure 5.2. It should be noted that the line A-A' intersects all the photodetector

implants and BCCD channels within the macropixel. This cross-sectional model is used as the basis of various simulations presented in this section.

Extensive process and device simulations were performed along this cross-section to optimize UHFR-I macropixel. Figure 5.3 illustrates results of 2-D device simulations, showing maximum potential in the device structure along X-dimension of the cross-section shown in Figure 5.2. As can be seen in this figure, the photodetector has a stair-case type potential profile which is critical for its high speed operation. The BCCD channel under poly-1 gate is also completely depleted and has a channel potential of about 9.1V (at 0V gate voltage). The BCCD and photodetector depleted regions are separated by a p^+ implant which acts as a barrier for electron movement between photodetector and BCCD channel-1. The surface channel potential of p^+ region is about 0V. These simulated potential values are compared with experimentally measured values in Table 5.2. In general, there is a good agreement in these values which establishes a basis for more detailed simulations presented in this Chapter. The difference in the measured and simulated values could be accounted for that fact that simulation models do not include variations in process and device parameters.

Table 5.2 *Simulated and Measured potentials in UHFR-I device*

Region	Simulated (V)	Measured (V)
Detector 4+3+2 implant	4.5	4.2
Detector 4+3 implant	3.2	2.9
Detector 4 implant	2.0	1.8
Poly-1 Gate	9.1	8.9

As discussed in the previous section, photogenerated electrons underneath the photodetector area can diffuse into the macropixel storage area. This effect is a major

source of the crosstalk signal in UHFR-I device architecture. This crosstalk is due to the lateral diffusion of photocarriers generated below the depleted portion of the photodetector. Figure 5.4 shows the simulated values of potential in the epi-layer (i.e. potential vs. depth) along the lines illustrated in Figure 5.2. From this figure, the depletion potential and depletion depth could be measured for the major sections of the macropixel. A virtual phase pinned photodiode structure used in this device has a shallow p^+ region (~0.3 μm deep) on the top which is biased at ground potential. As could be observed in Figure 5.4, detector depletion region extends from 0.3 μm to about 4.0 μm deep (measured from the top of the surface) in the epi-substrate. The BCCD channel depletion thickness is about 4.5 μm. The substrate region below this depleted region is also at ground potential.

Photocarriers generated in the photodetector depletion region (from 0.3 μm to 4.0 μm depth) are quickly drifted towards deepest potential region due to built in electric field. Thus, carriers generated in this region do not contribute to crosstalk signal significantly. The region below this depleted area does not have any field in it (ground potential). Photocarriers generated in this area do not experience any electric field and their motion is primarily diffusion driven. As the wavelength of the photons is increased, more carriers are generated in this field free region. The distance which these carriers can travel before getting recombined would be determined by the electron life time in the epi-substrate (40 Ω-cm resistivity)[14]. Some of these carriers can travel up to the BCCD registers and get collected in that region, thus generating crosstalk signal. Figure 5.5 shows the effect of this charge movement on UHFR-I macropixel. The BCCD channel-1

and channel-4 collect more of this crosstalk signal as compared with channel-2 and channel-3 as channel-1 and channel-4 are closer to photodetector region. Most of the crosstalk signal gets collected in BCCD channel-1 compared with BCCD channel-2, which is another 2.4 μm apart in X dimension. This effect is also verified by simulation and experimental results presented in section 5.4. It should be noted that source of crosstalk signal in BCCD channel-1 is from its macropixel's photodetector while BCCD channel-4 collects crosstalk signal from adjacent macropixel's photodetector. However, the spacing of BCCD channel-1 and BCCD channel-4 with respect to its nearest photodetector is the same (6.3 μm), which results in almost similar crosstalk effect. The optical crosstalk simulations presented in this section includes the contribution of both the photodetector associated with BCCD channels.

5.3.2 Effects of Diffusion Crosstalk in UHFR-I Devices

In frame-transfer type area image sensors, the only effect of diffusion crosstalk is on MTF. In interline-transfer area imagers, there are opaque vertical register interdigited with columns of sensor elements. Crosstalk into these registers leads to an analogous effect, namely, vertical image smearing. For example, crosstalk from an intense spot image will result in a uniform increase in signal in all the charge packets moving through the adjacent shift registers because of the way the device is clocked. At the display, this increase in signal will appear as a vertical crosstalk, which is uniform over the full height of the picture.

The effect of crosstalk is entirely different for UHFR-I devices due to its unique macropixel architecture. Figure 5.5 schematically depicts the effect of crosstalk on a

UHFR-I macropixel. As described in earlier chapters, the macropixel photodetector integrates charge for different frames at different times. For this reason, the effect of crosstalk results into frame-to-frame optical crosstalk as signal can diffuse from photodetector to the nearest storage frame pixels in the memory area. The effect is most dominant on the left and right columns of the storage array as these are closest to a photodetector. The total crosstalk signal in a frame is also dependent on its location in the storage array. For example, if all 32 frames are illuminated, frame #1 would get crosstalk signal from all 31 subsequent exposures, while frame #31 would get crosstalk signal from only one exposure (during illumination of frame 32). Due to this effect, minimization of optical crosstalk has been the major challenge in this device design apart from obtaining 2×10^6 frames /sec frame rate. For example, even if crosstalk signal add 1% extra signal per exposure, frame #1 would have 31% spurious signal in the above example.

5.4 Simulation and Experimental Results

As mentioned in earlier sections, the design of UHFR-I imager was optimized using extensive simulations. Some of the timing related simulation results are described in Chapter 4 along with the experimentally measured results. This section describes various simulations performed to optimize the optical performances of the UHFR-I imager and experimental results are discussed.

As mentioned in previous sections, commercially available 2-dimensional (2-D) process and device simulation tools were used for optical crosstalk study. Process simulation models were developed which basically replicate every process step in the

fabrication of actual UHFR-I imager devices. Output of these 2-D process simulation results in a device structure geometry, which could be used for further electrical and optical characterization. This structure is used as an input to the device simulation tool in this study. Several electrical and optical simulations were performed on this structure to optimize the performance by varying various process and device parameters. Since these simulations are extremely computation intensive and take large amount of simulation time, only the most relevant portion of the imager macropixel geometry is generated and simulated. This cross-section includes photodetector region, BCCD storage area and is shown in Figure 5.2. This structure is then simulated in the width dimension (X) and in depth dimension in the epi-substrate (Y). All the simulations are performed at -30° C to mimic the real operating conditions.

The major objective of this study was to develop fundamental understanding of the optical crosstalk in high frame rate devices and to apply it for optimization of the UHFR-I macropixel structure.

5.4.1 Photocarrier Distribution and Transient Response

The objective of this study was to characterize the photocarrier distribution and transient response of the macropixel. Figure 5.6 illustrates the initial potential condition of the device, assuming the BCCD polysilicon frame storage gates are biased at 0V and substrate is grounded. X dimension is the width of the device structure and Y dimension is the depth of the structure. Since the macropixel width is 92.2μm, the X dimension is from 0-92.2μm and the Y dimension shows the top 8 μm of 18 μm thick epi-layer (-18 μm being the top surface). As can be seen in Figure 5.6, the detector area is depleted in

the absence of any photo-carriers and the peak depth of the depletion region is approximately 4 μm and the maximum potential in the detector 4+3+2 implant region is about 4.5V. The stair-case type potential profile connection different detector regions could also be seen in this figure, which results from graded implants in the detector used to optimize photodetector response time. The four BCCD storage pixels are also completely depleted and the peak potential in this region is about 9.1V.

For optical simulations, the detector area (X = 0 to 45 μm) of this structure is exposed with a light source. The light source used for this study is of 600 nm wavelength, 4×10^{20} photons/cm^2 intensity, and is on for 0.1 μs. Figure 5.7 shows the free electron concentration (cm^{-3}) in the structure at the end of 0.1 μs exposure. As could be seen in this figure, large number of photo-carriers are already collected in the detector region (electron concentration axis is in log scale). There is also some lateral diffusion of the carriers towards the frame storage region and subsequently some of these are collected in the BCCD gates, which results in crosstalk. As can also be seen from this figure, the BCCD gates closer to the detector region collects more carriers. Figure 5.8 illustrates the potential distribution in the structure at 0.1 μs. The maximum potential and the depletion depth reduces in detector region due to collection of negative charge in the form of electrons. The depletion depth reduces by about 0.4 μm and the maximum potential reduces by 1.5 V in the detector region

Since the target frame rate of UHFR-I device is 2×10^6 frames/sec, the detector response time should be no longer than 0.5 μs to achieve this frame rate. Figure 5.9 shows the device state at 0.4 μs after the light source is turned off. Comparision of

Figure 5.7 and Figure 5.9 shows that majority of the photo-carriers are collected in the detector and the frame storage area. It should be noted here that very few stray carriers (carrier concentration axis is in log scale) are still floating in the epi-substrate below the detector region. Since there is no electric field present (ground potential) in this region, the motion of these carriers is diffusion driven. This simulation results clearly shows that the response time of the detector is less than 0.5 µs, meeting the target frame rate of 2 × 10^6 frames/sec. Figure 5.10 illustrates the potential profile in the structure at this instance. In the photodetector region, the total reduction in depletion depth is about 0.4 µm and total reduction in maximum potential is about 1.6 V. The measured value of electron concentration in the detector region is about 2 × 10^4 electrons per µm of width. The BCCD channel-1 collects about 7.93 electrons µm of width, representing a optical crosstalk of 0.039%. The reduction of depletion depth and maximum potential in the BCCD channel regions is negligible. This is due to the fact that, this region has a higher potential and depletion depth, and receives only 0.039% of the signal compared with photodetector region.

5.4.2 Effect of Illumination Intensity and Wavelength on Optical Crosstalk for UHFR-I and VHFR Devices

The objective of this study was to characterize the optical cross talk performance of VHFR devices to establish a baseline for simulation and use it to optimize the UHFR-I devices. Crosstalk was studied as a function of illumination intensity and wavelength for both the devices, and the results are discussed in this section. Figure 5.11 illustrates the simulated cross talk values in BCCD-1, 2 and 3 registers as a function of illumination

intensity. Measured values of cross talk in BCCD-1 register for VHFR devices are also plotted on this figure for comparison. It should be noted that the total integrated signal in the photodetector is proportional to the illumination intensity. Figure 5.12 is a similar illustration as in Figure 5.11, for UHFR-I devices. As can be seen from Figure 5.11 and Figure 5.12, the simulated results correlate with experimental data. It should be noted that there are number of real device effects which could not be modeled in the simulations. The effect of these factors on simulation results is secondary in nature. The key factors, which are expected to generate second order mismatches between the simulation and experimental results, are:

- Device fabrication process variations, i.e. variations in dielectric thickness, line widths, uniformity etc.;

- Device parameters used in the simulation models are not precisely characterized and can vary from one process to another;

- 3-D models not included in the simulator (due to unavailability of 3-D simulation tools); and

- LEDs used for light source in experimental setup has a peak response at some wavelength, which is used in simulation models. However, it also has some broadband response around this peak wavelength point which is not modeled in simulation.

The cumulative effect of all these factors could be significant and limits the accuracy of simulated results. In general, it should be assumed that simulation results can vary by as much as 20-30 % compared with experimental data.

In general, the cross talk increases as the total integrated signal increases for both VHFR and UHFR-I devices. This is due to the fact that cross talk is primarily a lateral diffusion phenomenon. As the illumination intensity increases, the carrier gradient increases between the photodetector and frame storage region. This higher gradient results in a higher lateral diffusion current generating higher crosstalk.

These results also conclude that, in general, cross talk in UHFR-I devices is reduced by a factor of 40 compared to VHFR devices, thus improving the optical performance significantly. The primary reason for the reduction in optical crosstalk is due to the improved photodetector design for UHFR-I imager. In UHFR-I, the photodetector boundary is surrounded by typically 4.3 μm wide p$^+$ region compared to only about 1.5 μm p$^+$ region in VHFR photodetector. This p$^+$ region produces electric field barrier for electron movement between the photodetector and BCCD channel region. Apart from this, the BCCD channel-1 spacing with photodetector is about 6.3 μm in UHFR-I design compared with only about 2.7 μm in VHFR design.

This higher spacing also improves the optical crosstalk performance of UHFR-I imager at higher wavelengths. This effect is clearly visible in Figure 5.13. Figure 5.13 illustrates measured and simulated values of cross talk in BCCD-1 register for VHFR and UHFR-I devices at different wavelengths. The performance of both devices degrades sharply at higher wavelengths (> 750 nm) due to very long absorption distance of photons (13.16 μm at 826.5 nm). This is due to the fact that photo-carriers are generated deeper in the substrate as wavelength is increased, which results in large diffusion driven motion of these carriers in the absence of any electric field, thus increasing the possibility of being

collected in BCCD storage regions significantly. Based on this experiment, it could be concluded that, UHFR-I devices have shown excellent optical performance for wavelengths shorter than 700 nm where absorption distance is low (lower than 4 µm). At wavelengths lower than 700 nm, most of the carriers are generated in the photodetector depletion region (4 µm deep). Most of the stray electrons which lie outside this region are unable to reach to BCCD channels due to potential barrier presented by p^+ region.

By comparing the crosstalk performance of UHFR-I and VHFR devices in Figure 5.13, it can be concluded that the differential improvement in UHFR-I devices reduces as the wavelength is increased. This effect is due to the correlation between absorption distance of photons with the width of p^+ region between detector and frame storage region. It can be concluded from this study that the optical crosstalk performance could further be improved at higher wavelengths by increasing the width of p^+ region at the cost of reduced fill-factor.

5.4.3   Effect of Optical Shield Aperture on Crosstalk

The UHFR-I imager array of 180 × 180 macropixel has a 1 µm overlap of metal shield. In the macropixel layout, metal-3 layer is an optical shield, which covers entire macropixel region except the photodetector area. This shield is used to illuminate only the photodetector region to incoming photons and mask the storage region and control gates. The p^+ guard ring and the metal-3 layer boundary define the photodetector boundaries. To study the effect of shield aperture on crosstalk, a test row was designed which includes eight different cases of metal-3 shield geometry, which are -4 µm to +3

μm overlap of p$^+$ guard ring in 1 μm increments. Optical simulations were performed using eight different cases of light exposure only in the area not covered by metal-3 shield. This is equivalent to the test row structures, as metal-3 is a light shield layer. It should be noted that all the other simulations presented outside of this section uses metal-3 shield overlap of 1μm over the detector region.

Figure 5.14 illustrates simulated values of optical crosstalk in BCCD-1 register as a function of wavelength for eight different metal shield overlap cases. As could be seen in this figure, increase in the shield overlap of detector does not reduce the crosstalk significantly. It should be noted that having a large metal shield overlap of detector region reduces the photosensitive area and hence the fill-factor, so there are practical limitations to having large overlap. Figure 5.15 and Figure 5.16 show the measured and simulated results of crosstalk in BCCD-1 and BCCD-2 registers at 574 nm wavelength (green light) and 659.5 nm wavelength (red light), respectively. These results show an excellent match between experimentally measured and simulated results, considering the limitations of simulation models discussed in the previous section. Based on the simulation and experimental results presented in this section, it can be concluded that metal shield overlap of photodetector region does not reduce the optical crosstalk. However, if the metal shield overlap is increased further significantly, it is expected to improve the optical significant. This is phenomena is likely to happen when the overlap width is significantly higher than the absorption distance of the carrier. However, large overlap width is not practical in imager design as the fill factor is considerably reduced. These results can be incorporated in future designs and the fill-factor can be improved by not overlapping the shield over the photodetector.

5.4.4 Characterization of Photodetector as a function of Wavelength for VHFR and UHFR-I Devices

To characterize the photodetector of VHFR and UHFR-I devices, simulations were performed to depict the effect of wavelength on the total integrated carriers, and the results are shown in Figure 5.17. In general, the effect is similar for both devices due to the similar photodetector construction. The UHFR-I macropixel has a fill-factor of about 40% compared to 13% of VHFR macropixel, thus resulting in higher number of photo-carriers in UHFR-I macropixel.

As explained in earlier sections, the pinned-buried photodetector structure has a top thin p^+ layer. This region determines the optical response of the pinned photodetector structure to shorter wavelength. At short wavelengths, large portion of incoming photons are absorbed in the top thin p^+ layer (~0.3 µm thick) of the detector due to smaller absorption distance. The carriers generated in this region could get recombined at the surface, as semiconductor surface is the location of an abundance of extra localized states or recombination centers. This signal could also diffuse to the underlying depleted region and become part of the integrated signal, or it can get recombined in p^+ region itself. As wavelength of the light is increased further, the carriers are generated away from the surface and probability of these being collected in the depletion region increases. This effect would sharply increase the total integrated signal at these wavelengths. As can be seen from Figure 5.17, total integrated signal increases from 600 nm to 800 nm wavelength for this detector structure. As wavelength is continuously increased, photons are absorbed deeper in the epi-substrate (due to higher absorption distance), farther from the depletion region of the photodetector, thus reducing the possibility of being collected

in photodetector. This phenomenon generates higher optical crosstalk and also reduces the total integrated signal as wavelength of the photons is increased. For the fabrication of this imager, a 18μm thick epi-layer was grown on p^+ substrate. After a certain wavelength, almost all the photons are absorbed in the underlying p^+ substrate. The generated carriers in this region are quickly recombined due to a very short lift time, thus generating almost no integrated signal. This effect determines the optical response of the pinned photodetector structure to longer wavelength.

It can be concluded from these results that the pinned photodetector structure used in VHFR and UHFR-I has a wavelength band in which it could be used. The lower wavelength cutoff of this structure is determined by the thickness of top p^+ layer. By increasing the thickness of top p^+ region, it is possible to improve the detector performance at low wavelengths. The higher wavelength cutoff of this structure is determined by the thickness of epi-layer. The detector performance at higher wavelengths can be improved by increasing the thickness of the epi-layer. However, thicker epi-layer will increase the optical crosstalk at higher wavelengths. To decrease the optical crosstalk, epi-layer doping could be optimized, which is discussed in next section.

5.4.5   Effect of Epi-layer Doping on Crosstalk

As mentioned in previous section, the epi-layer doping can be used to optimize the crosstalk in UHFR-I imager. Figure 5.18 shows simulated values of optical crosstalk at various wavelengths as a function of epi-layer doping. As can be seen in this figure, crosstalk decreases significantly as the epi-layer doping is reduced. This is due to the fact

that the depletion thickness in the photodetector region is a strong function of epi-layer doping and lower doping (higher resistivity) of epi-layer results higher depletion thickness. The simulated values of depletion depth as a function of epi-layer doping are listed in Table 5.3. The higher depletion depth results in more of the photocarriers to be generated in this region, thus reducing the crosstalk significantly. However, as the wavelength of the photons is increased, carriers are generated deeper and deeper in the substrate due to larger absorption distance of the photons and this offsets the effect of thicker detector depletion region, as shown in Figure 5.18. It could be concluded from these results that epi-substrate doping has a critical effect on the optical crosstalk. Very good optical crosstalk performance could best be achieved by selecting epi-substrate doping which results in depletion depth, which is comparable to the absorption distance of the photons.

Table 5.3 *Depletion depth in the photodetector as a function of Epi-doping*

Epi-layer doping (cm^{-3})	Depletion Depth (μm)
3.0×10^{15}	2.0
6.0×10^{14}	3.4
4.0×10^{14}	4.0
3.5×10^{14}	4.2
3.0×10^{14}	4.4
2.5×10^{14}	4.6
1.9×10^{14}	5.0
1.5×10^{14}	6.4

In conclusion, the results described in this section represent a comprehensive study in understanding the cross-talk phenomena. The key findings from this study are:

- The photodetector response time is expected to be lower than 0.5 μs. This is consistent with the maximum frame rate target of 2×10^6 frames/sec.

- Optical crosstalk increases as the illumination intensity of the light source is increased.

- Crosstalk performance is significantly improved in UHFR-I devices compared with VHFR devices.

- Crosstalk performance does not improve with a larger optical shield overlap of the detector region.

- Top thin p^+ layer on detector structure determines the short cutoff wavelength of the detector.

- Epi-layer thickness determines the long wavelength cutoff of the detector.

- Epi-layer doping value significantly influences the optical crosstalk.

These results will be useful in optimizing optical performance of future imager devices. Next chapter discusses a imager design which is capable of capturing images at a maximum frame rate of 1×10^7 frames/sec and stores 12 frames at the macropixel location. This design has been optimized using the results from this chapter.

CHAPTER 6

TEN MILLION FRAME RATE UHFR-II IMAGER

6.1 Introduction

A 2×10^6 frame rate UHFR-I burst imager is described in chapters 3, 4 and 5. Upon successful completion of this design, further research was performed to achieve a 1×10^7 frame rate speed. This chapter describes the results obtained for designing a 1×10^7 frame rate imager, UHFR-II.

Another important goal of this new design has been to reduce the process complexity. UHFR-I was based on a 3-phase BCCD 4-level poly technology, which is a very complex process. By virtue of its macropixel architecture, 4-level of polys are required. UHFR-II architecture has been further improved to carry out the design using 3-phase BCCD and 3-level of polysilicon and allow a storage of 12 frames at its pixel location instead of 32 frames in UHFR-I.

6.2 Design of UHFR-II Image Sensor

6.2.1 Specifications

The initial design specifications for the proposed UHFR-II imager are summarized in Table 6.1.

6.2.2 Chip Architecture

The general block diagram of the 64 × 64-element UHFR-II imager is shown in Figure 6.1. The chip was divided into two halves, as with UHFR-I chip, to improve the yield

and maximum achievable frame rate. Each half is completely independent and consists of 32×64 macropixels, output serial register, and floating-diffusion and on-chip amplifier.

Table 6.1 *Design Specification of UHFR-II Imager*

Image Format Size	6.8 mm × 6.8 mm
Number of Pixels	64 × 64
Pixel size	106-µm × 106-µm
Optical Fill Factor	> 45%
CCD memory stages per pixel	12
Technology	3-phase BCCD with 3-level of poly, 3-level of metal
Design Rules	1.5 µm
Frame Rate during acquisition	1×10^7 frames/sec
Exposure time, t_{exp}	50 ns
12-frame readout time	0.1 s
Saturation signal, Q_{max}	20,000 e⁻
Spectral Response	250 to 900 nm
Readout noise	< 6 rms electrons

The detected frames can be reconstructed with the two outputs of the chip. It is also possible to move the charge in only one direction by turning common gate "ON". Each macropixel consists of a photodetector and 12 storage elements. The photodetector generates the charge and this charge is moved to macropixel memory at a very high speed. Once the image acquisition is completed, imager operates as a frame-transfer imager and charge moves to output serial register line-by-line. Output serial register moves the charge to floating diffusion amplifier pixel-by-pixel at a slow speed to reduce the noise component. Figure 6.2 shows a block diagram of the 2 × 2 macropixel along with output serial register. In general, the signal is collected in photodetector and

transferred to 12 frame storage area during the frame acquisition mode. During the frame transfer mode, these stored frame charges are transferred to output serial register and subsequently to amplifier where these get converted to voltage signal.

6.2.3 Pixel Design and Operation

Figure 6.3 is a schematic diagram of a macropixel. Each macropixel has a dimension of 106-μm(H) $\times$ 106-μm(V). A macropixel consists of a photodetector PD, a charge collection gate G1, antiblooming gate G2, a drain D, charge transfer gate G3, and storage of 12 pixel elements in the form of a vertical array. Figure 6.4 shows the layout of the macropixel of UHFR-II imager. The pinned-buried photodetector region has a top shallow p$^+$ implant, which is biased at substrate potential (ground). The photodetector is constructed using 6 n-type implants, which create a stair-case type potential profile in the epi-substrate. The electric filed profile generated due to this structure drift the photocarriers towards the deepest potential point (innermost implant around G1 and G2 gate edge). This operation is critical in optimizing detector response time for 10 MHz frame rate operation of the imager. G1 and G2 gates are independently biased to control the amount of charge, which is transferred into G1 gate and remaining charges are dumped into drain via G2 gate. This photodetector design also facilitates the operation under sub-frame integration mode where only a fraction of the integrated signals during a frame acquisition are transferred to storage area. This is achieved by first emptying the photodetector by biasing G2 gate high and turning it off. Subsequently, G1 gate is biased high and samples the additionally integrated signal. The successful operation of this feature at a 1×10^7 frame rate requires very low rise and fall time delays. Integrated

signal collected by G1 gate is transferred to vertical storage register through gate G3. G3 gate also acts as a barrier between the vertical storage register and G1 gate during the frame readout mode.

The photodetector has a dimension of 52.8-μm (H) × 100-μm(V), making the fill factor of the imager 45%. The drain is used for the control of blooming during frame integration time under the control of gate G2, by turning it on. The drain is also used to dump excess frames from vertical storage register of the upper macropixel under the control of gate Φ. This feature is used to store the last integrated 12 frames in the macropixel memory and all previously integrated frames get dumped into the drain. The operation of the UHFR-II imager during frame acquisition and readout mode is as follows:

Frame Acquisition Mode

Figure 6.5 illustrates the clock waveforms used during the frame acquisition mode. To achieve the sub-frame integration, G1 and G2 are kept as non-overlapping clocks. In this mode, each frame acquisition consists of two periods, t_{dump} and t_{exp}. During the t_{dump} period, G1 gate is off and G2 gate is on, thus all the photocarriers are being dumped into the drain. During the t_{exp} period, G1 gate is on and G2 gate is off, thus all the photocarriers are being collected as the integrated signal under the gate G1. If the sub-frame integration mode is not desired, G1 and G2 clocks could be overlapping. In this mode, the channel potential difference between G1 and G2 gate determines the amount of charge collected as the integrated signal.

Figure 6.6 shows the macropixel operation during the frame acquisition mode. As shown in Figure 6.6, readout of the detected charge under the photodiode is performed by charge transfer from gate G1 to G3 to CCD well under the clock phase $\Phi1$. The operation of the 12 stage CCD memory is controlled by three clock phases, $\Phi1$, $\Phi2$, $\Phi3$ and two additional clocks Φ and neg-Φ. During the frame acquisition mode, the 3-phase 12-stage CCD pixel memory registers are continuously clocked with the control clock Φ having the same waveform as the CCD clock phase $\Phi3$, while the control clock neg-Φ is in the OFF state. This forms a potential barrier at the macropixel vertical boundary. This result in the storage of the last 12 detected frames and all previous frames being dumped into the drain D under the control of clock phase Φ.

Frame Readout Cycle

During the frame readout cycle, illustrated in Figure 6.8, the control clock Φ is maintained in the OFF state while the control clock neg-Φ assumes the same waveform as the CCD clock $\Phi3$.

Now the CCD pixel memory registers are reorganized into 64 pixel columns, each having $64 \times 12 = 768$ stages and are operating as two 32×64 pixel parallel serial CCD. In this design, the 64 column registers are on 106-μm centers. The serial output register is configured in the form of two sets of 32 stage, 106-μm long sections each having 12 CCD stages. This would result in the total of $32 \times 12 = 384$ CCD stages at each of the two serial output registers. The main advantage of this readout architecture is that the twelve exposures of a given photodiode are read out in the correct temporal sequence,

facilitating real-time sequential signal processing of the charge signal detected by each detector corresponding to 12 stored frames at the pixel memory. This simplifies the demultiplexing of the data to generate the twelve images.

6.2.4 Clock Rise Times and the Frame Rate

The operation of the UHFR-II imager requires a DC bias for the pixel drain D and 8 clocks. Clocks $\Phi1,\Phi2,\Phi3$ are required for operation of the 3-phase BCCD 12-stage pixel memory clocking. Clocks Φ and neg-Φ are used to switch between the frame acquisition cycle and the frame readout cycle. Clocks G1, G2 and G3 are control clocks, where G1 and G3 perform the detector charge readout. Clock G2 dumps into the drain D the detector charge integrated during the time t_{dump}, separating the successive exposure times.

Detailed timing analysis was performed and clock delay times were calculated which are critical to achieve the frame rate of 10^7 frames/sec. Empirically calculated results are summarized in Table 6.2. Transient simulations were performed to verify these calculated results.

The calculated values of the drain D and the clock capacitances of the 106-μm $\times$ 106-μm pixel are listed in the first column of the Table 6.2.

The next table column gives the column or row capacitance in pF. Given in the next column are RC time constants, assuming 2.0-μm wide aluminum-1 with ρ_1=0.03 Ω and 2.5-μm wide aluminum-2 with ρ_2=0.04 Ω. An aluminum-2 traces 17 mm long and 68 μm wide has a resistance of 10.8 Ω.

The next column gives the total capacitance for each clock terminal. Finally, the last column lists the estimated time constant, $\tau_{0.9}$,from 0 to 90% of the final value and the required total resistance of the aluminum buses. The asterisk (*) in Table 6.2 indicates that these clocks are double strapped. The time constant $\tau_{0.9}$ of 8.33 ns for phase clocks $\Phi 1, \Phi 2$ and $\Phi 3$ was estimated assuming that $12\tau_{0.9} = 100$ns frame time.

Table 6.2 *Capacitances and delay times of the UHFR-II imager*

Clock Phase	C_{pixel} (fF)	$C_{column/row}$ (pF)	$\tau_{column/row}$ (ns)	C_{total} (pF)	$\tau_{0.9}/R$ (ns/Ω)
Drain,D	6.6	0.056	0.42	26.9	2/34
G1(poly-1)	28.4	0.185	1.82	116.5	5/20
G3(poly-2)	29.2	0.190	1.87	119.7	5/19.5
G2(poly-2)	22.0	0.146	1.41	90.2	5/26
Φ(poly-1)	45.7	0.312	2.88	184.3	5/25*
Φ(poly-2)	25.0	0.173	1.60	102.4	5/45*
Φ(poly-1)	170.7	1.18/0.3*	10.92	698.9	8.33/10.8*
Φ(poly-3)	196.7	1.37/0.34	12.59	805.8	8.33/9.4*
Φ(poly-2)	180.3	1.25/0.31*	11.54	738.7	8.33/10.2*

* Double strapped aluminum buses.

UHFR-II imager should be able to exceed the specified frame rate of 10^7 frames/sec based on these results.

6.3   Process for UHFR-II Burst Image Sensor

6.3.1   Process Technology

The UHFR-II burst image sensors will be fabricated by Sarnoff using a 1.5 μm three-phase buried-channel CCD technology with three level polysilicon and two levels of

aluminum. This process is based on the combination of the Sarnoff's standard three level polysilicon, one level metal CCD process and one level poly and two level metal CMOS process. One levels of aluminum are used for metal interconnection and the other level of aluminum as an optical shield over the non-optical sensitive area. SiO_2/Si_3N_4 channel dielectric are used to improve the charge transfer efficiency and possibly yield. Apart from these changes, the process for UHFR-II devices remains the same as for UHFR-I devices, and is described in section 3.3.1.

6.3.2 Process Specifications

The process specification for fabrication of the UHFR-II burst-image sensor is summarized below:

- The UHFR-II burst image sensors will be fabricated using nominally 17.5-μm thick p-type epi wafer with resistivity of 43 ohm-cm on <100> CZ p^+ substrate with resistivity in the range of 0.008 to 0.025 ohm-cm.

- Three levels of polysilicon are used for BCCD gates.

- Two levels of metal, of which two metal levels are used for interconnections outside the pixel array and one for interconnection, one for optical shield of the BCCD region not including the detectors inside the pixel array.

- A dual gate dielectric of SiO_2/Si_3N_4 is used.

- BCCD implants consisting of phosphorus and arsenic.

- The channel stops for BCCD channels have been defined by SCCD regions in the form of the p-type substrate without the BCCD implant.

- The pinned-buried graded photodetector was constructed by BCCD implant with six additional n-type implants and a top thin p^+ implant.

- The N^+ diffusions for blooming/dumping drain and source drains are defined by polysilicon gates on the channel side and p^+ implant on the other surrounding sides.

- As a general design/layout procedure, the pinned-buried photodetector, the output amplifiers, and whenever possible the outside perimeter of the burst-image sensor were surrounded by a P^+ field implant.

6.3.3 Fabrication Sequence

The process for fabrication of the UHFR-II burst image sensor includes three levels of polysilicon, three levels of metal, eleven implants, and requires a total of 23 mask levels.

Mask level 1:   ACT, defining the active area;

Mask level 2:   VTFN, p-type implant below the recessed thick oxide;

Mask level 3:   THOX, defining the thick oxide;

Mask level 4:   BCCD, BCCD implants;

Mask level 5: p^+, p^+ field implant surrounding the photodetector, output amplifiers, and the imager perimeter;

Mask level 6:   POLY-1, BCCD polysilicon-1 gates and output source follower MOSFET gates;

Mask level 7:   POLY-2, BCCD polysilicon-2 gates;

Mask level 8:   POLY-3, BCCD polysilicon-3 gates;

Mask level 9:   DET-1, first photodetector additional n-type implant, covering the whole photodetector region;

Mask level 10:   DET-2, second photodetector additional n-type implant, forming the second potential step in photodetector;

Mask level 11:   DET-3, third photodetector additional n-type implant, forming the third potential step in photodetector;

Mask level 12:   DET-4, forth photodetector additional n-type implant, forming the forth potential step in photodetector;

Mask level 13:   DET-5, fifth photodetector additional n-type implant, forming the fifth potential step in photodetector;

Mask level 14:   DET-6, sixth photodetector additional n-type implant, forming the sixth potential step in photodetector;

Mask level 15:   DET, photodetector p^+ implant, forming the pinned-buried BCCD channel photodetector;

Mask level 16: N^+, source and drain N^+ implants;

Mask level 17:   C2PL, defining contacts from metal-1 to polysilicon gates;

Mask level 18:   AACT, active area contacts, including contacts to source and drain, as well as to the substrate;

Mask level 19:   MTL-1, metal-1 interconnection lines;

Mask level 20:   VIA, VIAs between metal-1 and metal-2;

Mask level 21:   MTL-2, metal-2 interconnection lines;

Mask level 22:   MTL-3, metal-3 optical shield; and

Mask level 23:   BPAD, bonding pads.

In conclusion, the development of UHFR-II imager represents a significant advancement in the area of high frame rate imaging. This new device architecture is

demonstrated with the use of only 3-levels of polysilicon and 2-levels of metal, which reduces the process complexity significantly. The design of UHFR-II is complete and the device fabrication is scheduled to start in January 1998 at Sarnoff Corp.

CHAPTER 7

CONCLUSIONS AND RECOMMENDATION FOR FUTURE WORK

The focus of this research was to advance the area of high framing burst image sensor design. Two new device architectures were developed to operate at a frame rate as high as 1×10^7 frames/sec as part of this dissertation. A comprehensive study was done to develop fundamental understanding of optical crosstalk phenomena in high framing imagers. Brief description of these key achievements are as follows:

UHFR-I Burst-Image Sensor Chip

The 180 × 180-element UHFR-I burst image sensor (described in Chapter 3 and Chapter 4) is capable of capturing images at a maximum frame rate of 2×10^6 frames/sec, and continuously storing the last integrated 32 image frames at the macropixel memory locations. The imager chip is partitioned into two separate halves of 90 × 180-elements, each with separate output serial register and amplifiers to improve the device yield. The operation of this device was experimentally demonstrated and results showed that it could be operated at a maximum frame rate of 2.0×10^6 frames/sec rate.

Device and Process Simulations to Model Optical Cross-talk

A number of process and device simulations were performed to understand, optimize and predict cross-talk performance of the UHFR-I imager architecture. Simulations were performed to model and characterize the effect of metal shield aperture, epi-layer doping

and incoming light wavelength, on the cross-talk and the results were compared with the experimentally obtained data. These results are described in Chapter 5. In general, the simulation results are in good agreement with the experimental data thus validating the simulation models developed. These models could be extensively used in design of future image sensors to minimize the cross-talk impact on the device performance.

UHFR-II Burst-Image Sensor Chip

The 64 × 64-element UHFR-II burst image sensor (described in Chapter 6) is capable of capturing images at a maximum frame rate of 1×10^7 frames/sec, and continuously storing the last integrated 12 image frames at the macropixel memory. A new architecture for this design was developed to simplify the process requirements, which uses only 3-levels of polysilicon and 2-levels of metal. This simplified process is expected to improve the device yield substantially.

Suggestions for Future Research

On the basis of the research performed in this dissertation, the suggestions for future work in the general area of high frame rate imaging are as follows:

- The device architecture of UHFR-II imager could be further improved to realize larger number of storage locations without increasing the complexity of the process.

- Further research could be performed to improve the optical crosstalk performance of high framing rate imagers. It may be possible to create a buried drain structure between photodetector and frame storage memory which would act as a sink for signal diffusing from detector towards BCCD region. This drain structure could be

similar to the pinned-photodetector structure being used in VHFR, UHFR-I and UHFR-II devices. Detailed simulations could be performed to see the effect of this buried drain on optical crosstalk.

- Back-illumination CCD imager offers some significant advantages like prospect of 100% fill-factor compared with front-illuminated imaging technology. Significant research effort would be required to develop back-illuminated high frame rate burst-image sensor technology. The successful realization of this technology would require new pixel architecture and process development. This technology would be of great importance for applications requiring large number of frame storage without increasing the macropixel size significantly.

- Research could be performed to implement on-chip drivers for different clock phases of high frame rate imagers. This would greatly improve the performance of these devices and simplify the external electronics required at present, thus making this technology commercially more attractive. The required process changes will have to be carefully chosen as these could have significant effect on the existing process complexity.

APPENDIX

FIGURES
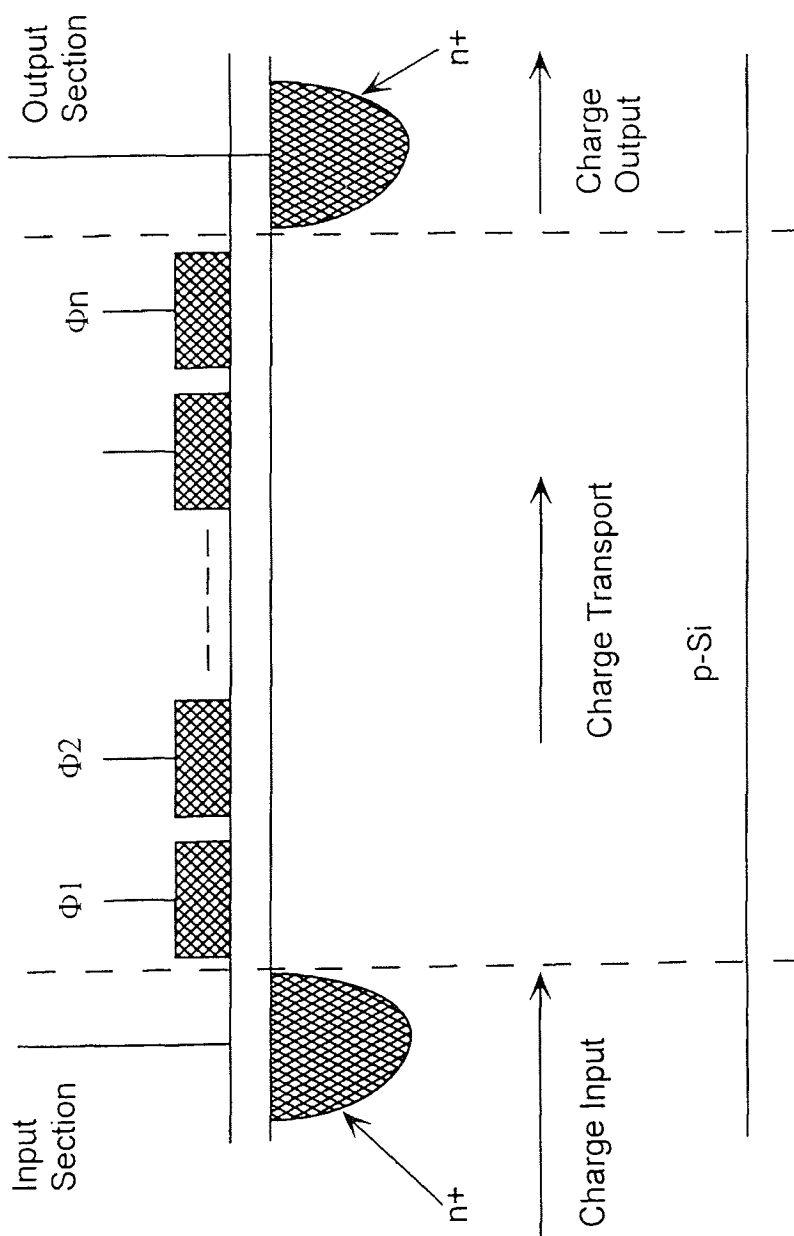
Figure 2.1 *Cross section of a CCD*
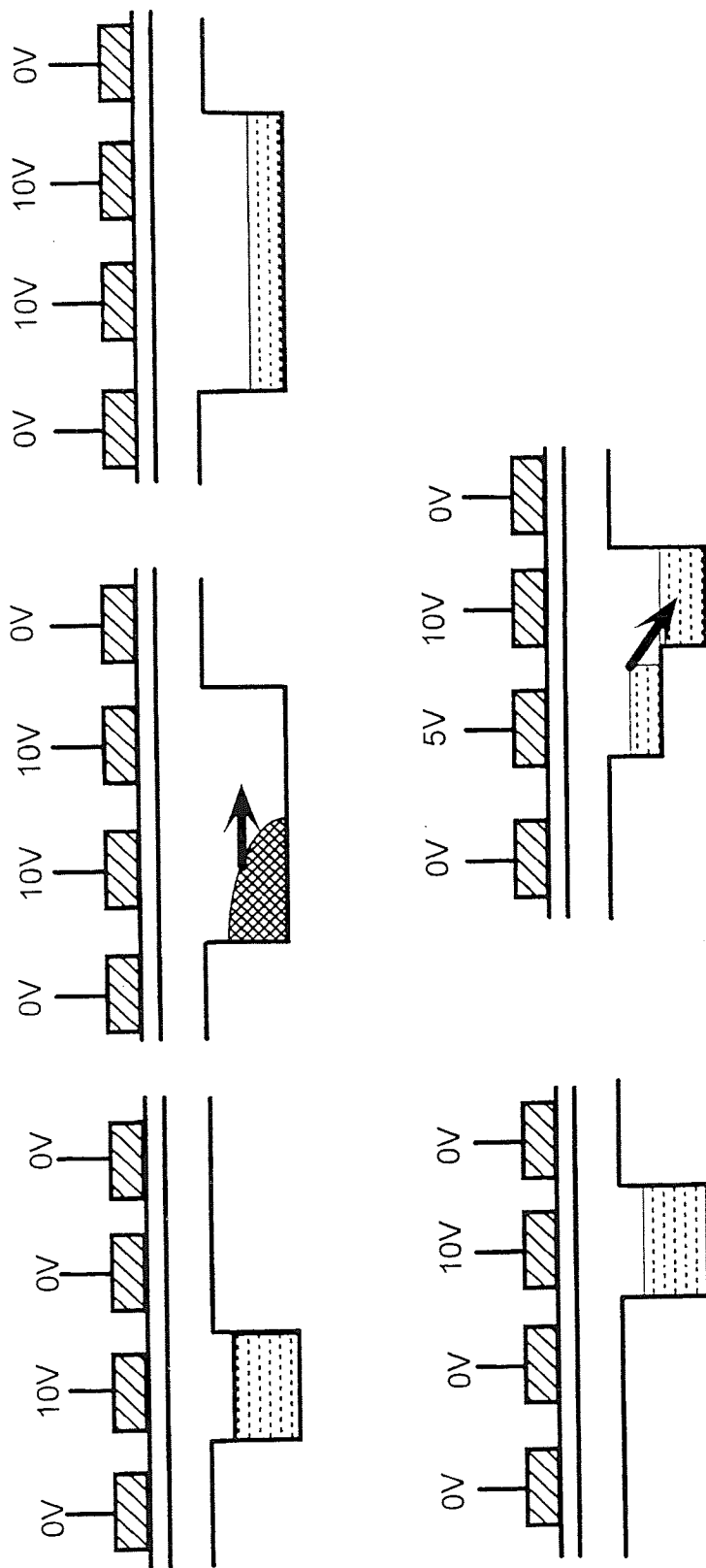
Figure 2.2 *Charge transport in a CCD*
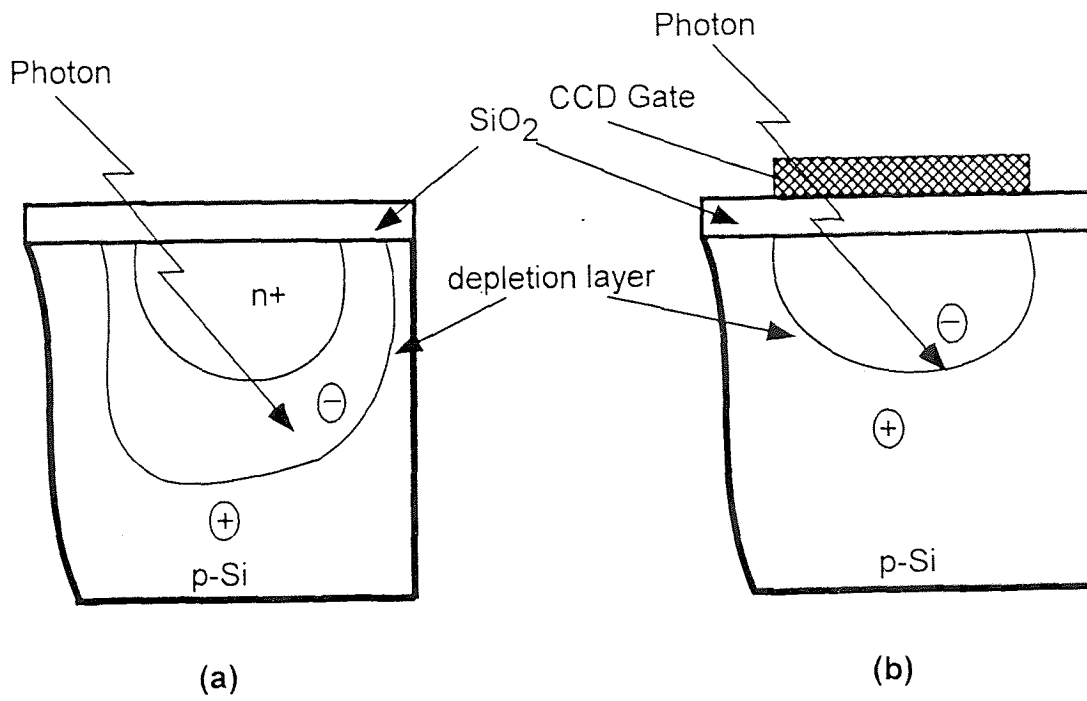
Figure 2.3 (a) *A metallurgical n+p junction,* (b) *voltage induced np junction*
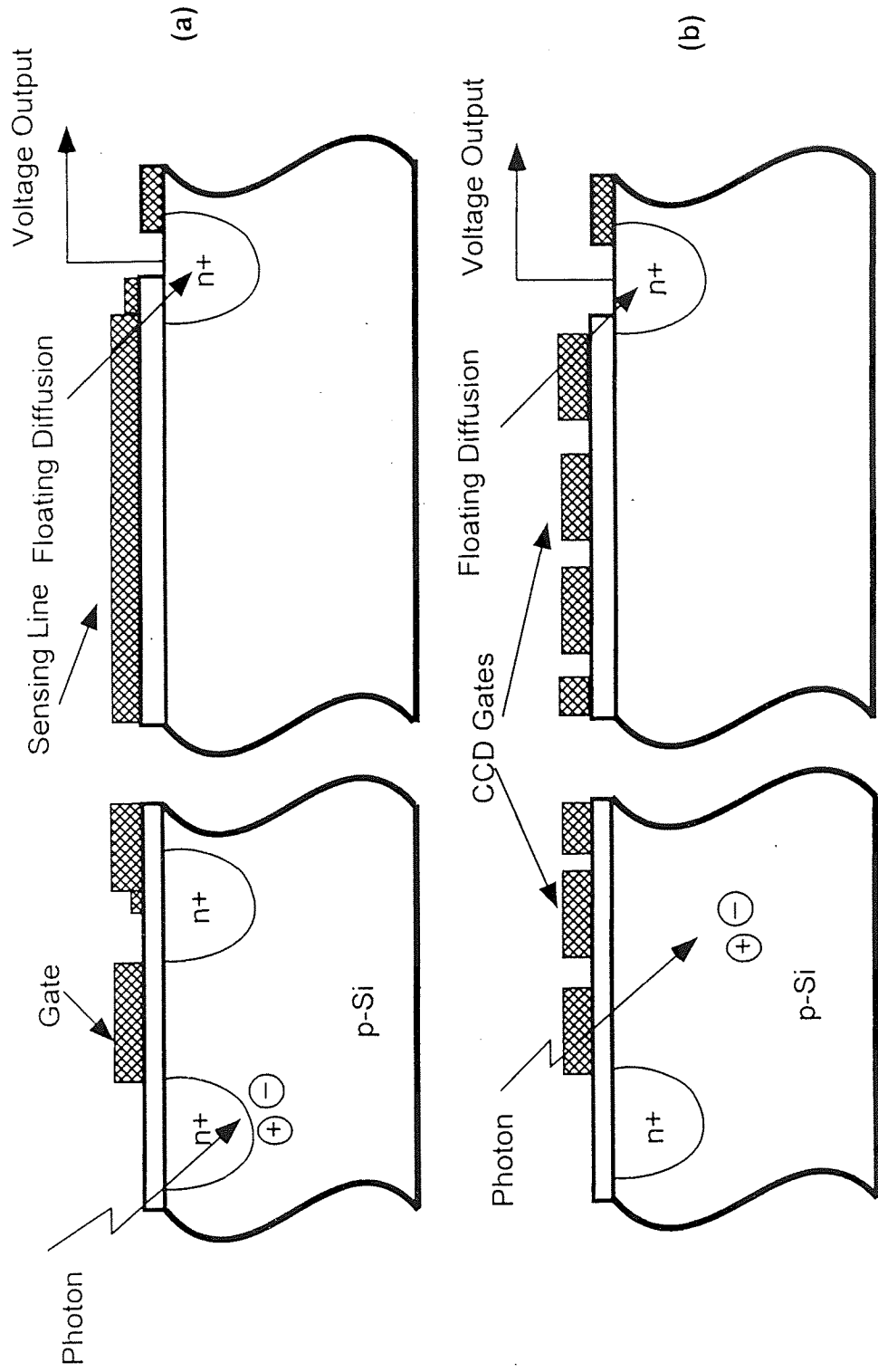
Figure 2.4 *Readout structure for Image Sensors (a) an MOS switch (b) CCD array*
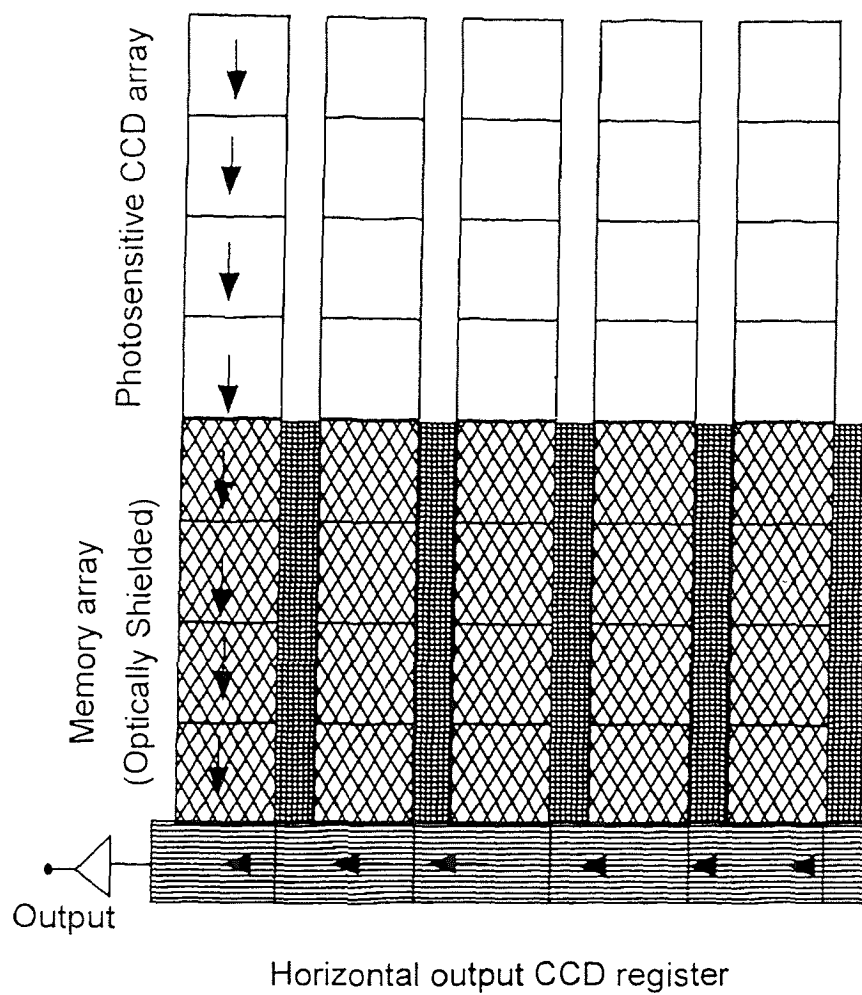
Figure 2.5 *Device architecture of a frame-transfer image sensor*
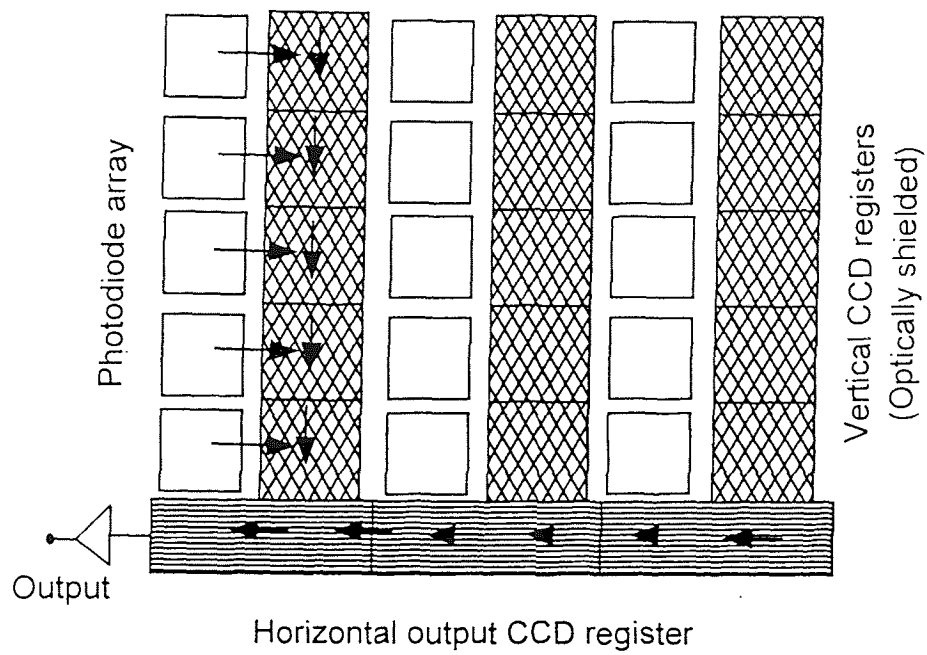
Figure 2.6 *Device architecture of an interline-transfer imager*
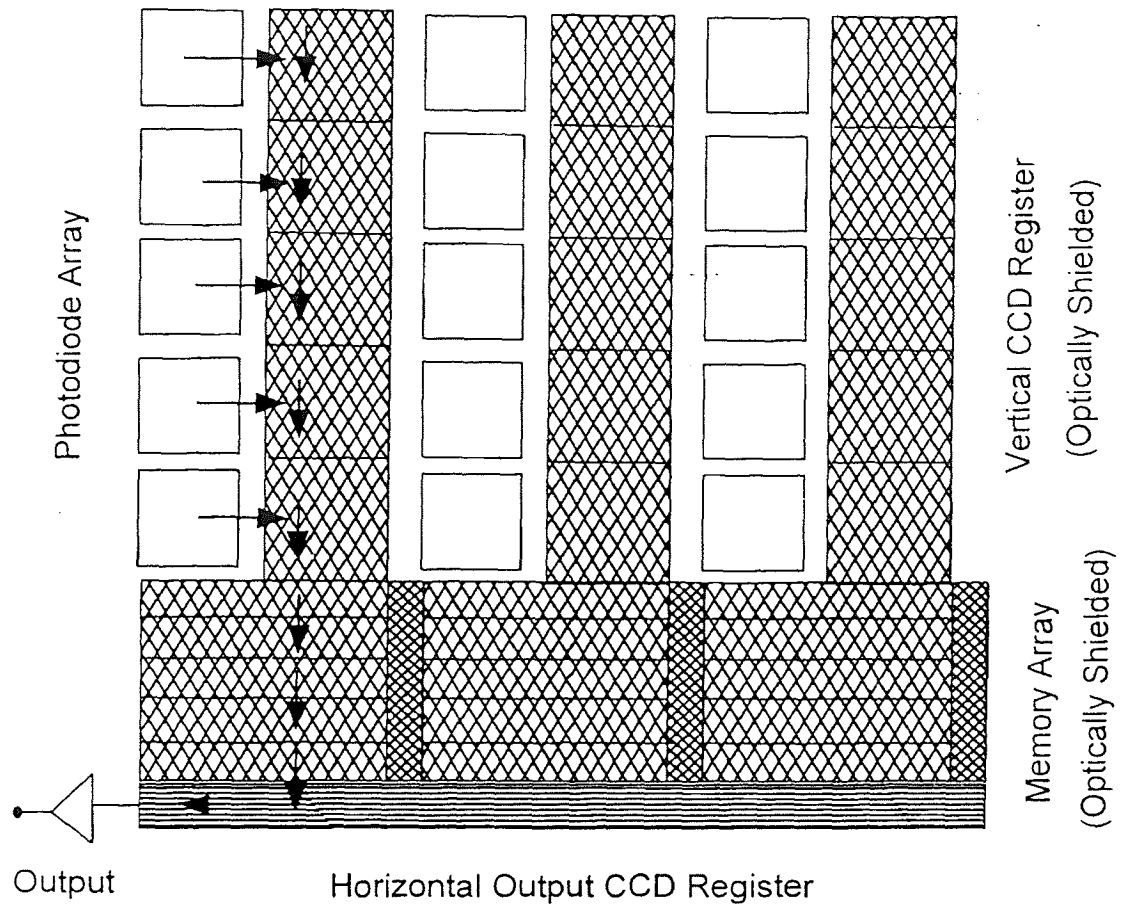
Figure 2.7 *Device architecture for frame-interline-transfer imager*
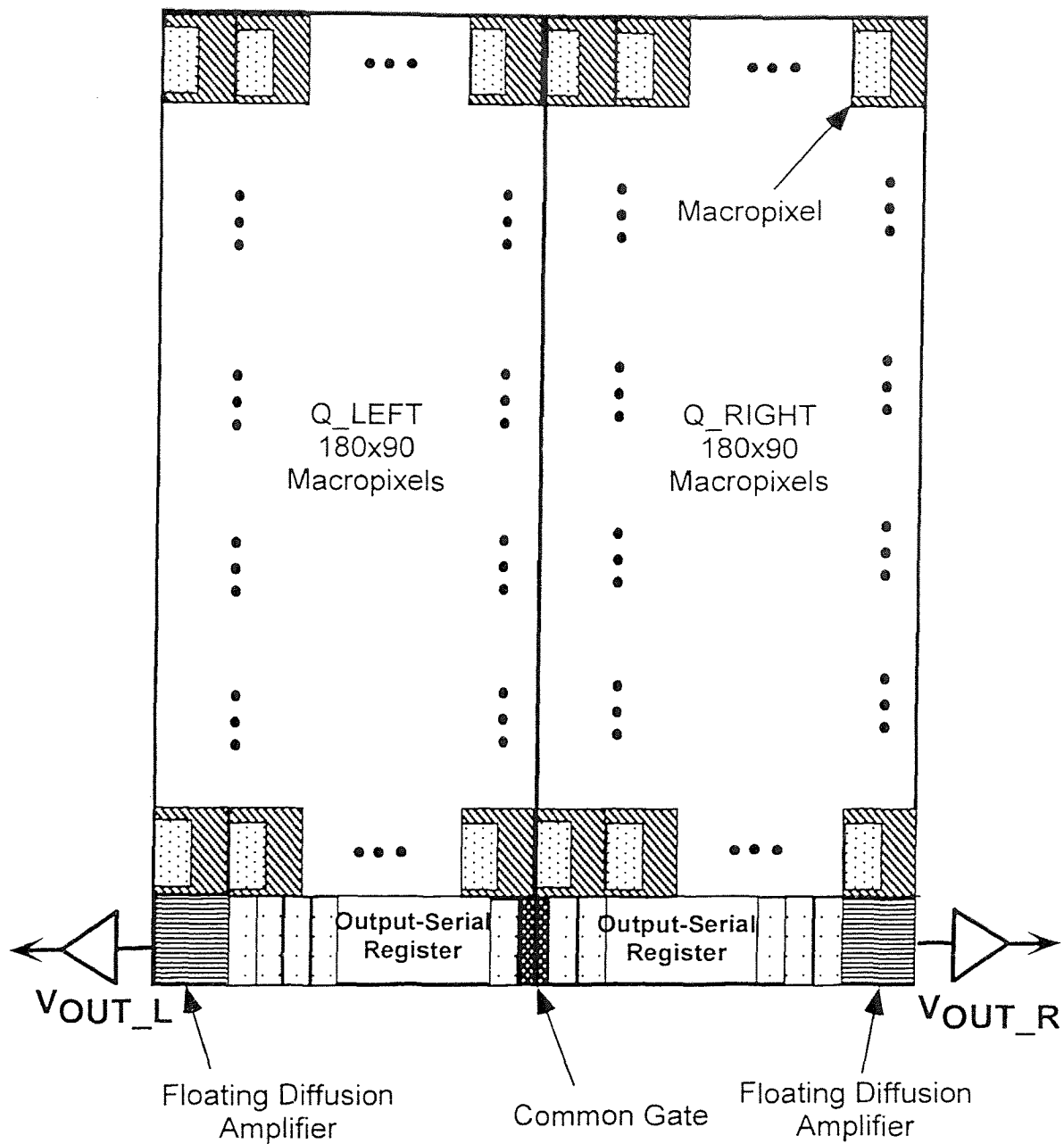
Figure 3.1 *Block diagram of the 180x180 element UHFR-1 chip*
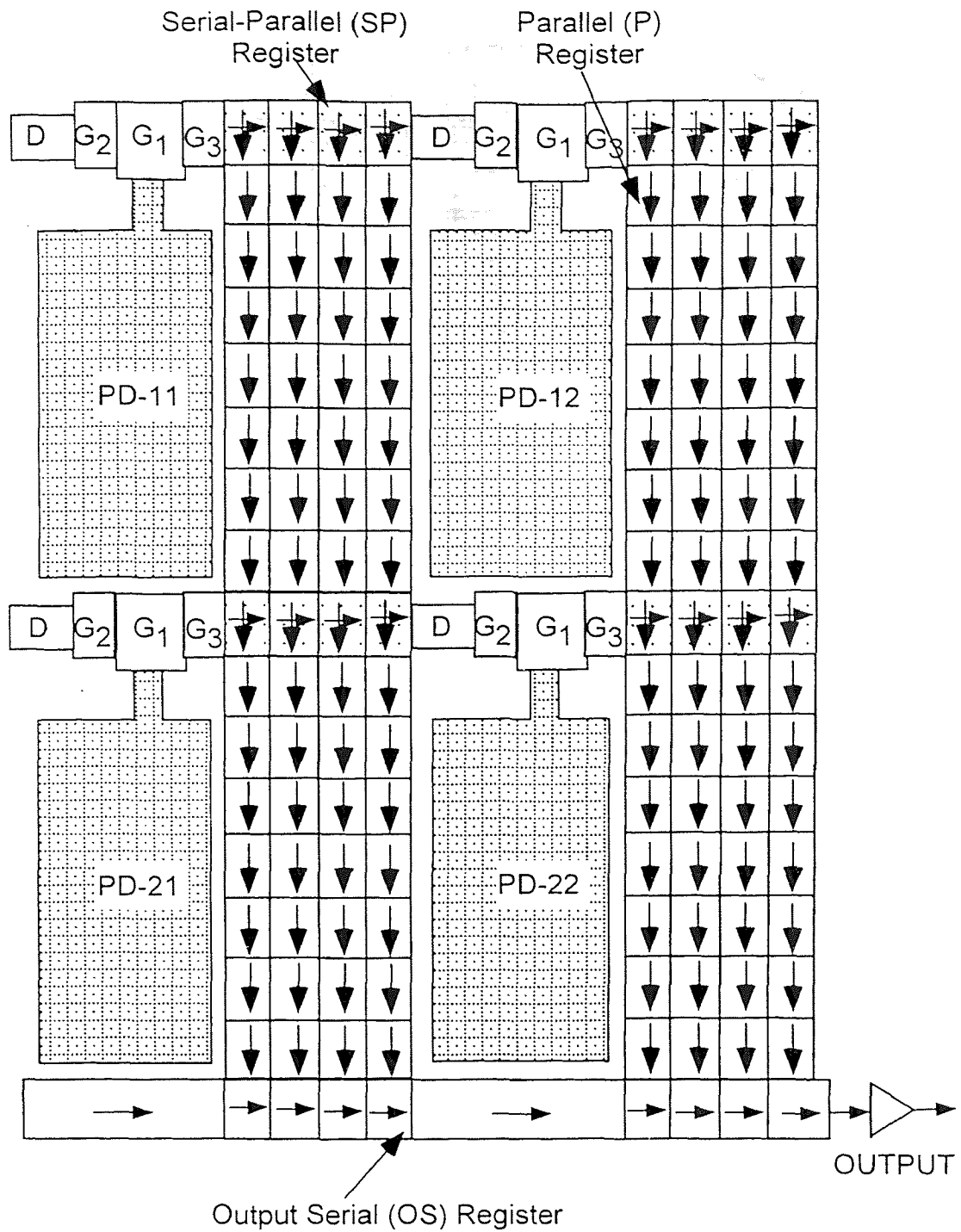
Figure 3.2 *Functional block diagram of UHFR-I burst imager*
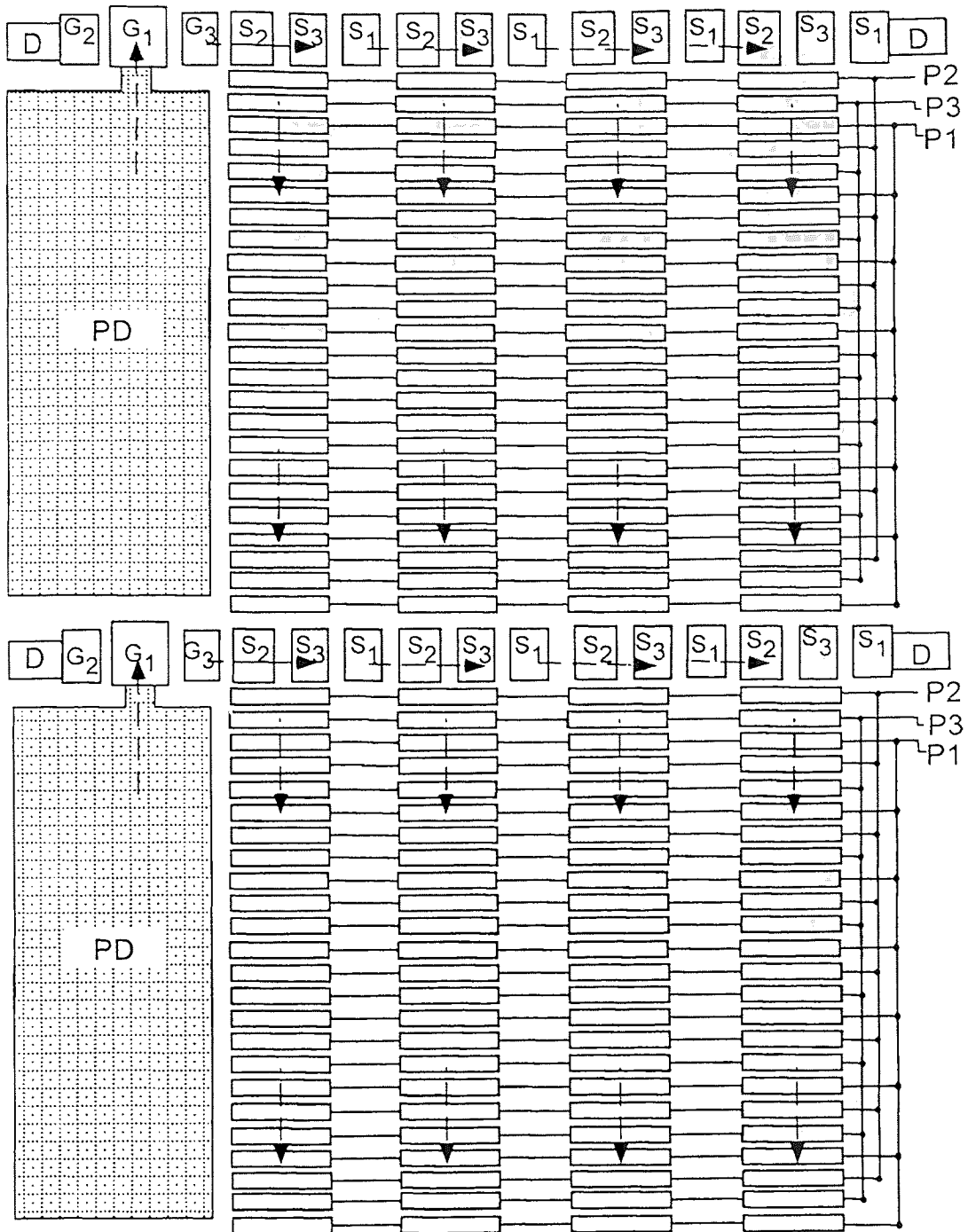
Figure 3.3 *Schematic diagram of two macropixels*
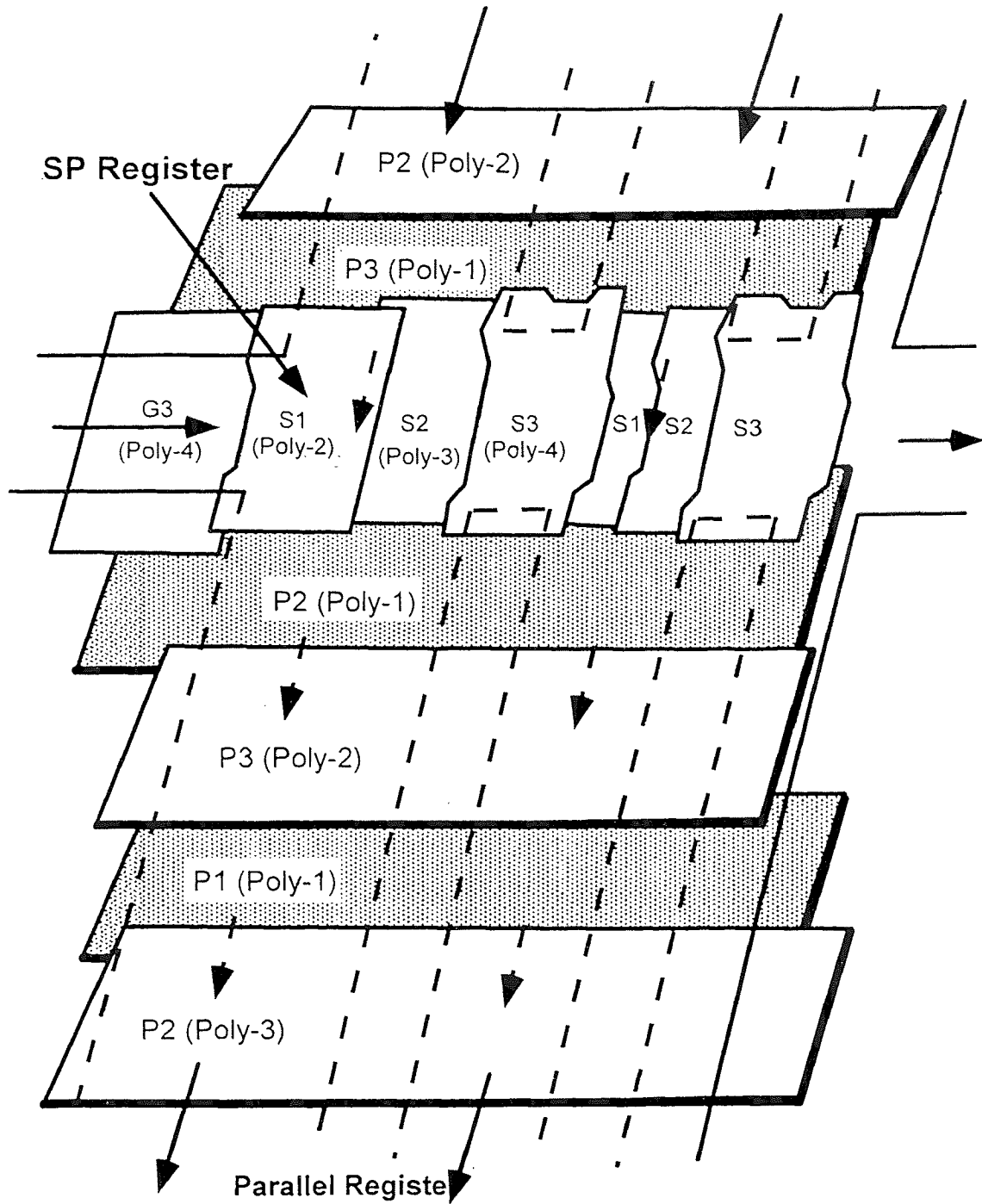
Figure 3.4 *SP and P Register design for 3-phase, 4-Poly CCD*
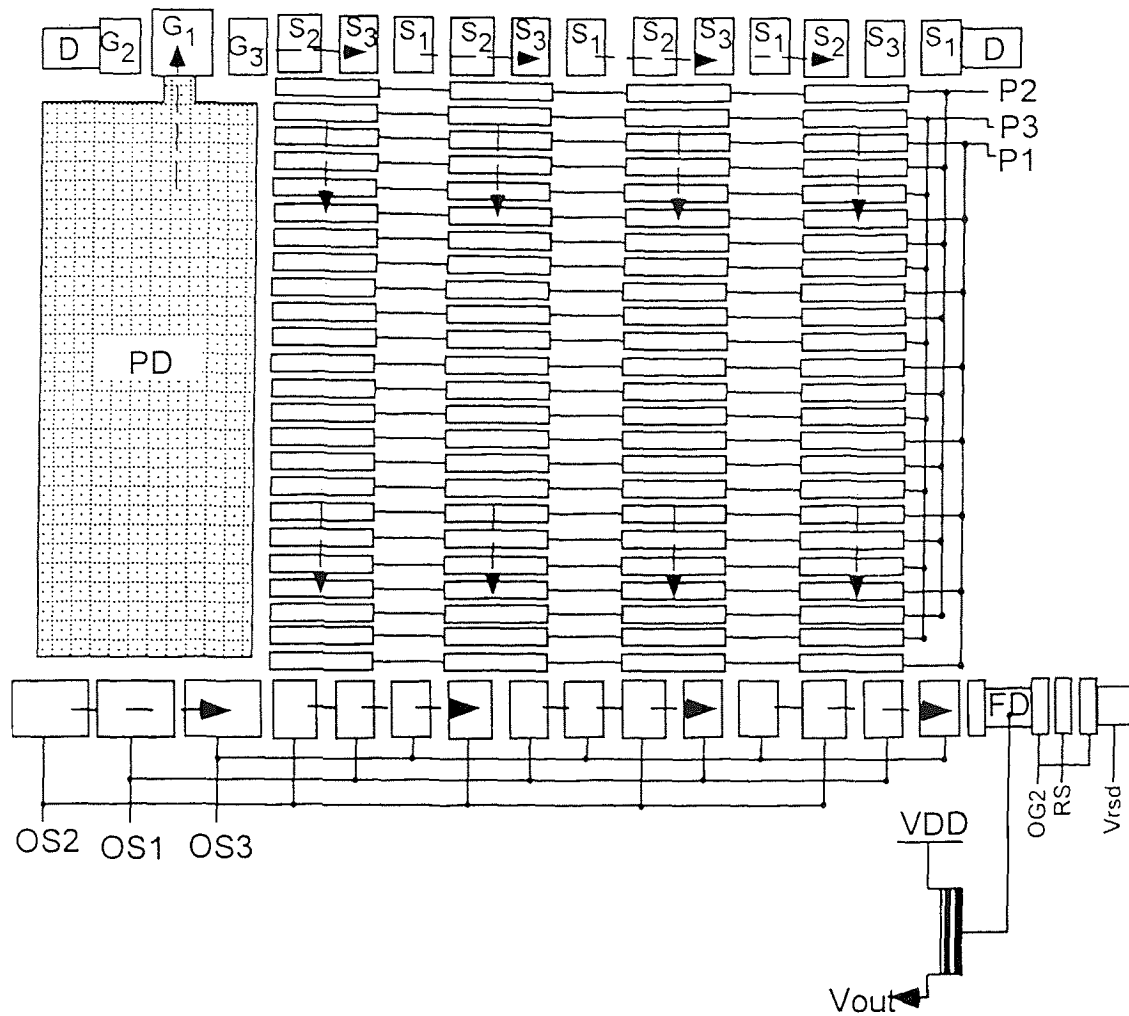
Figure 3.5 *Schematic Diagram of a macropixel with OS register and output amplifier*
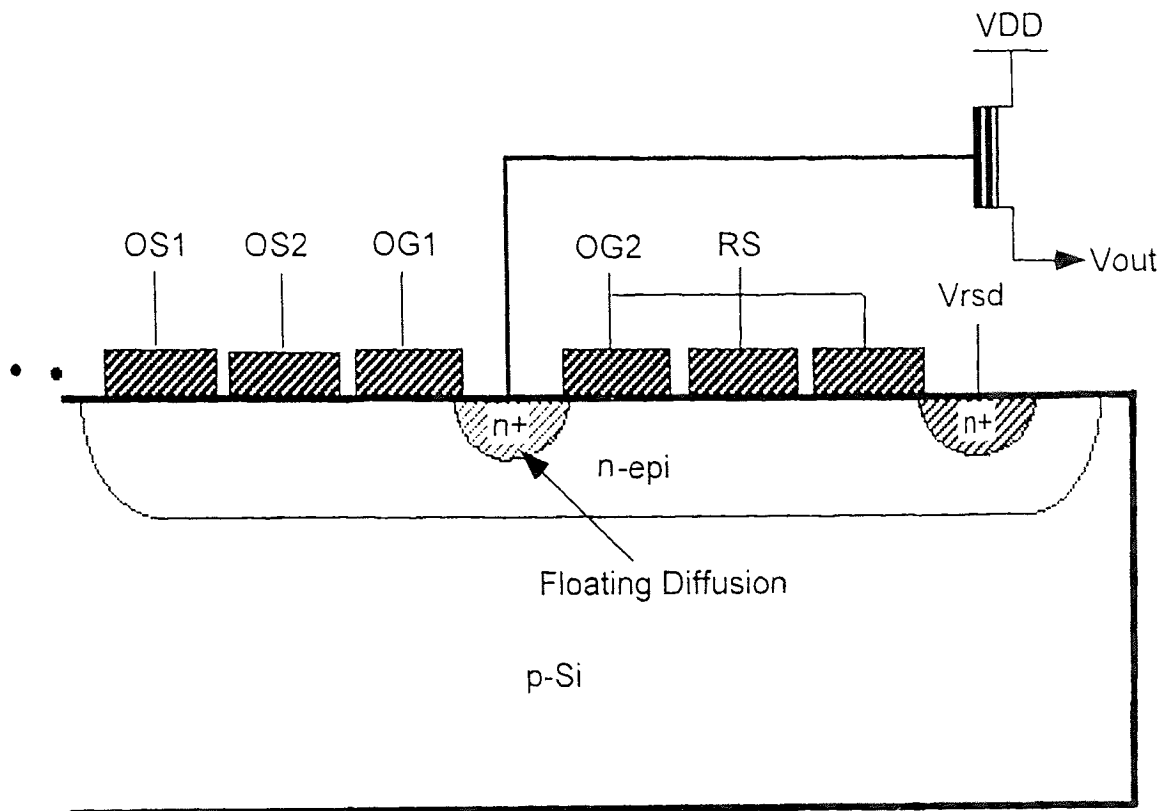
Figure 3.6 *Output stage for UHFR-I imager*
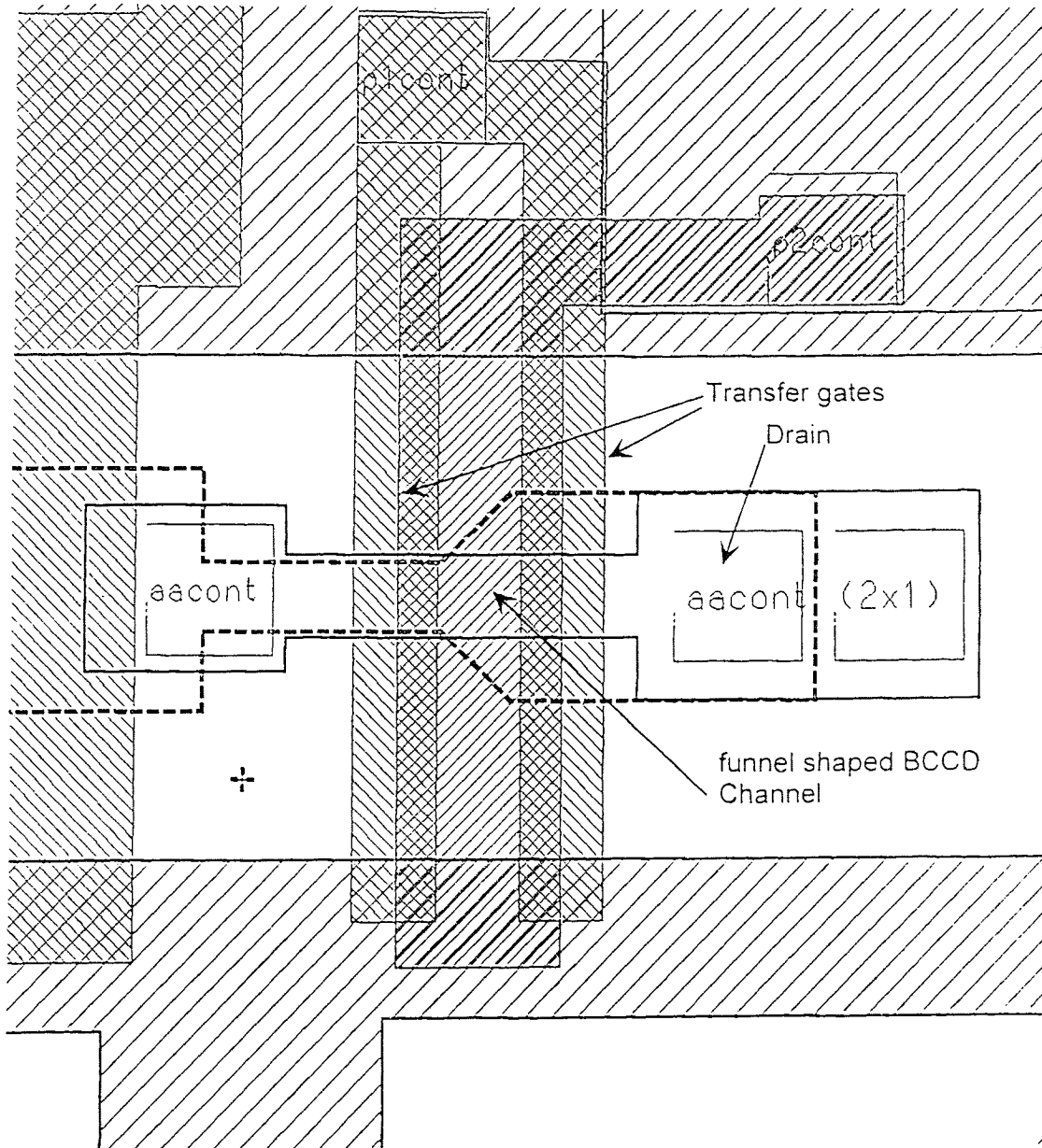
Figure 3.7 *Funnel shaped output amplifier*
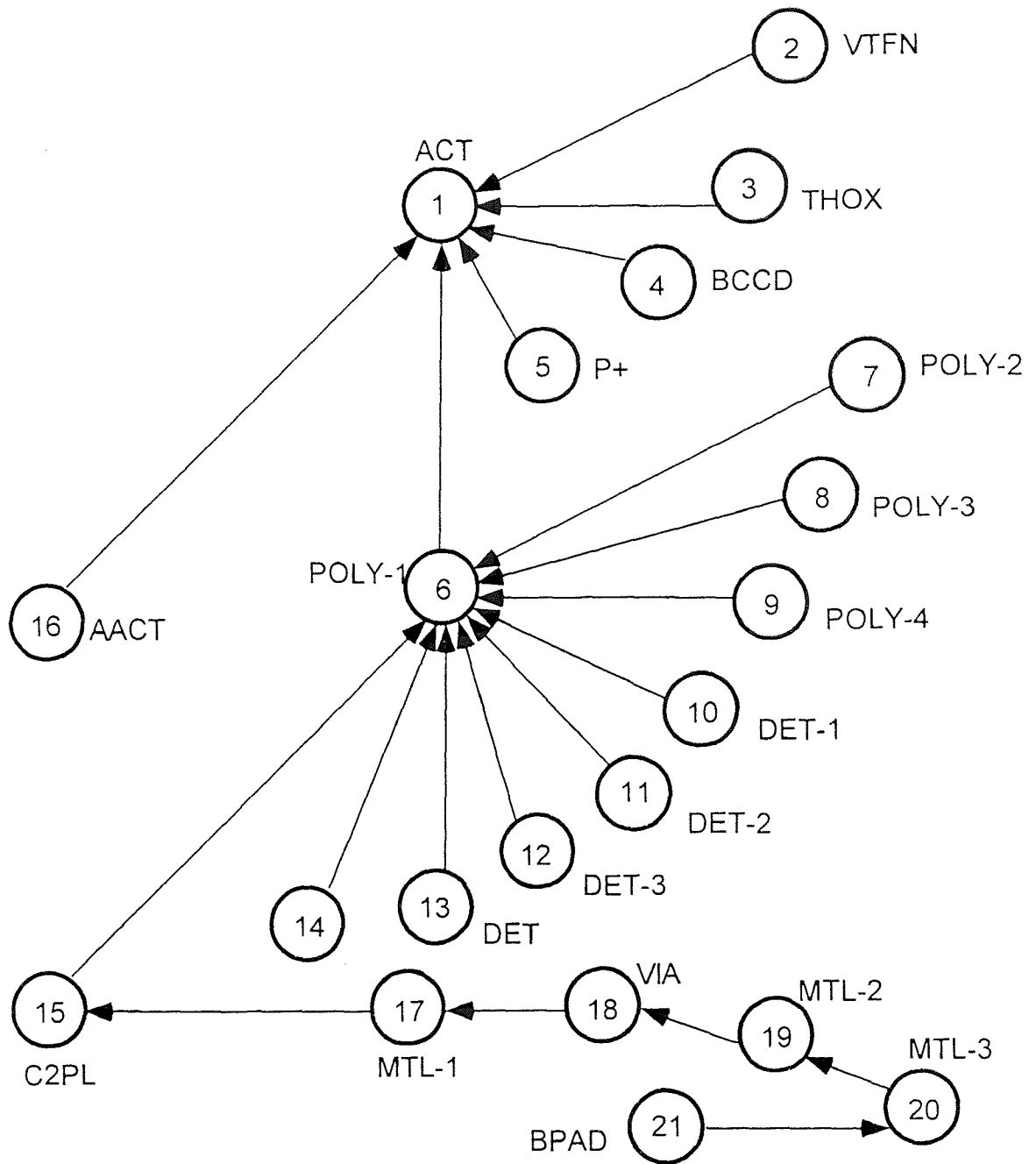
Figure 3.8 *Alignment of 21 mask levels and fabrication sequence*
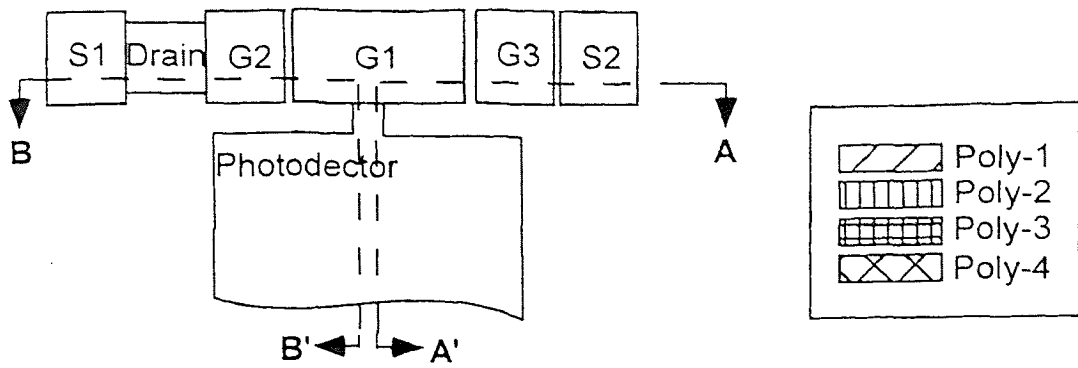
(a) Top view of the photodector output structure
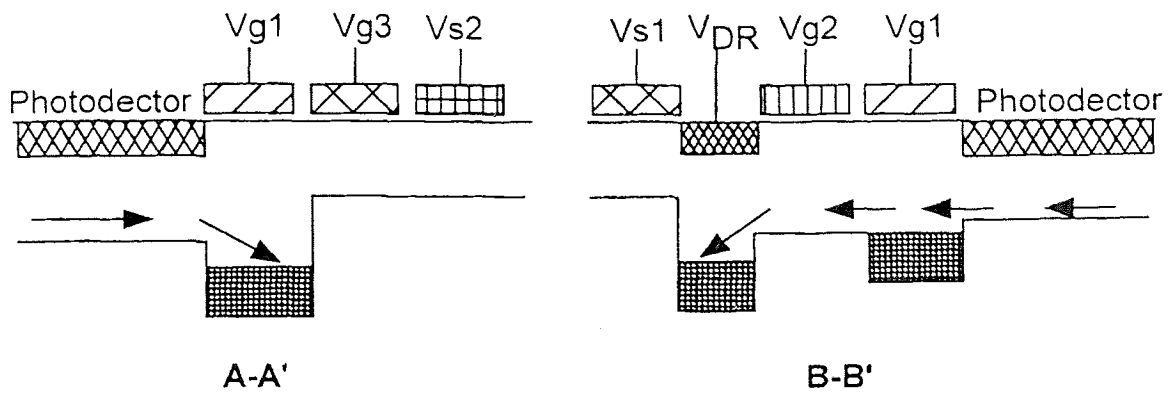
(b) Cross-section along A-A' and B-B' lines during charge integration period
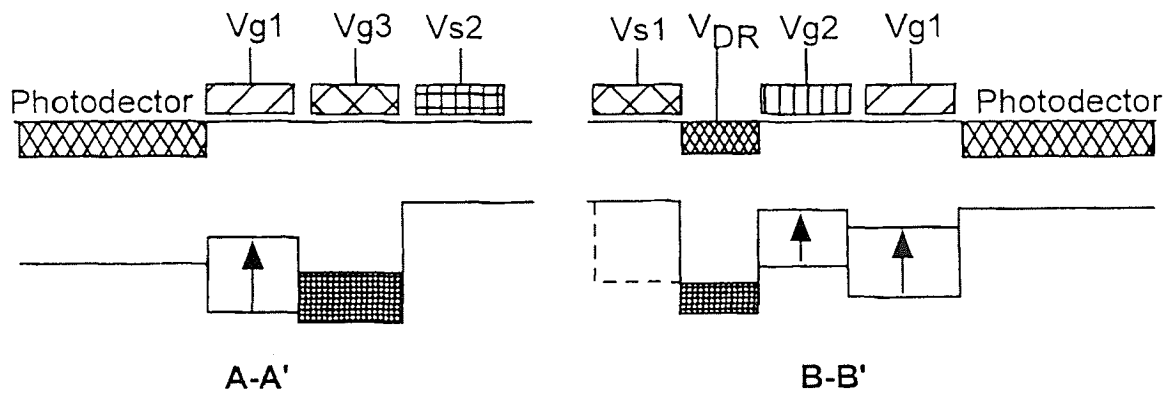
(c) Cross-section along A-A' and B-B' lines during charge readout period

Figure 3.9 *Operation of photodetector in charge integration and readout mode*
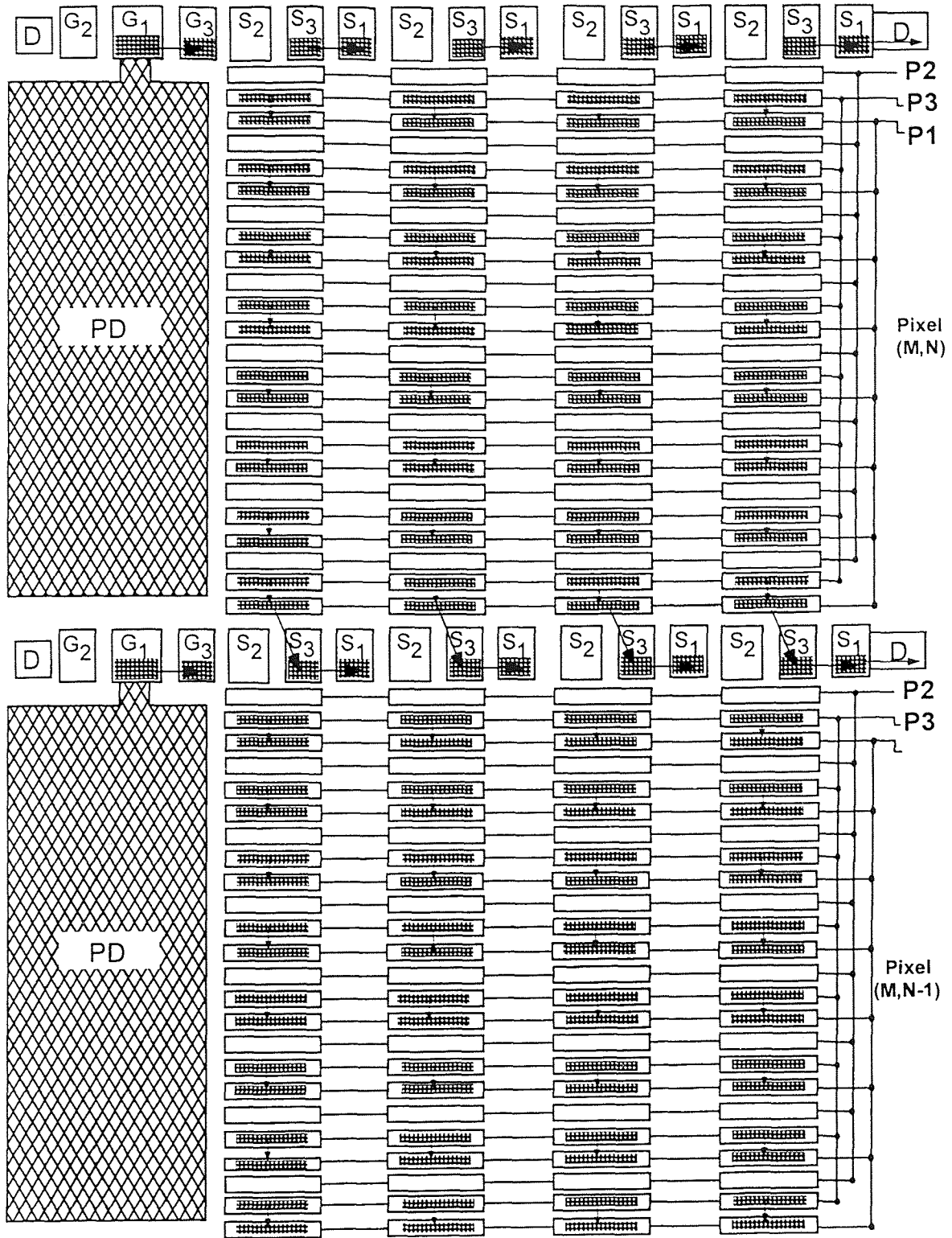
Figure 3.10 *Schematic diagram of UHFR-I imager during collection of first frame charge of each 4 frames sequence.*

Figure 4.1 *Macropixel layout of UHFR-1 chip*

Metal1 Interconnections

BCCD
Channels

Metal-2
Interconnections

Photodetector
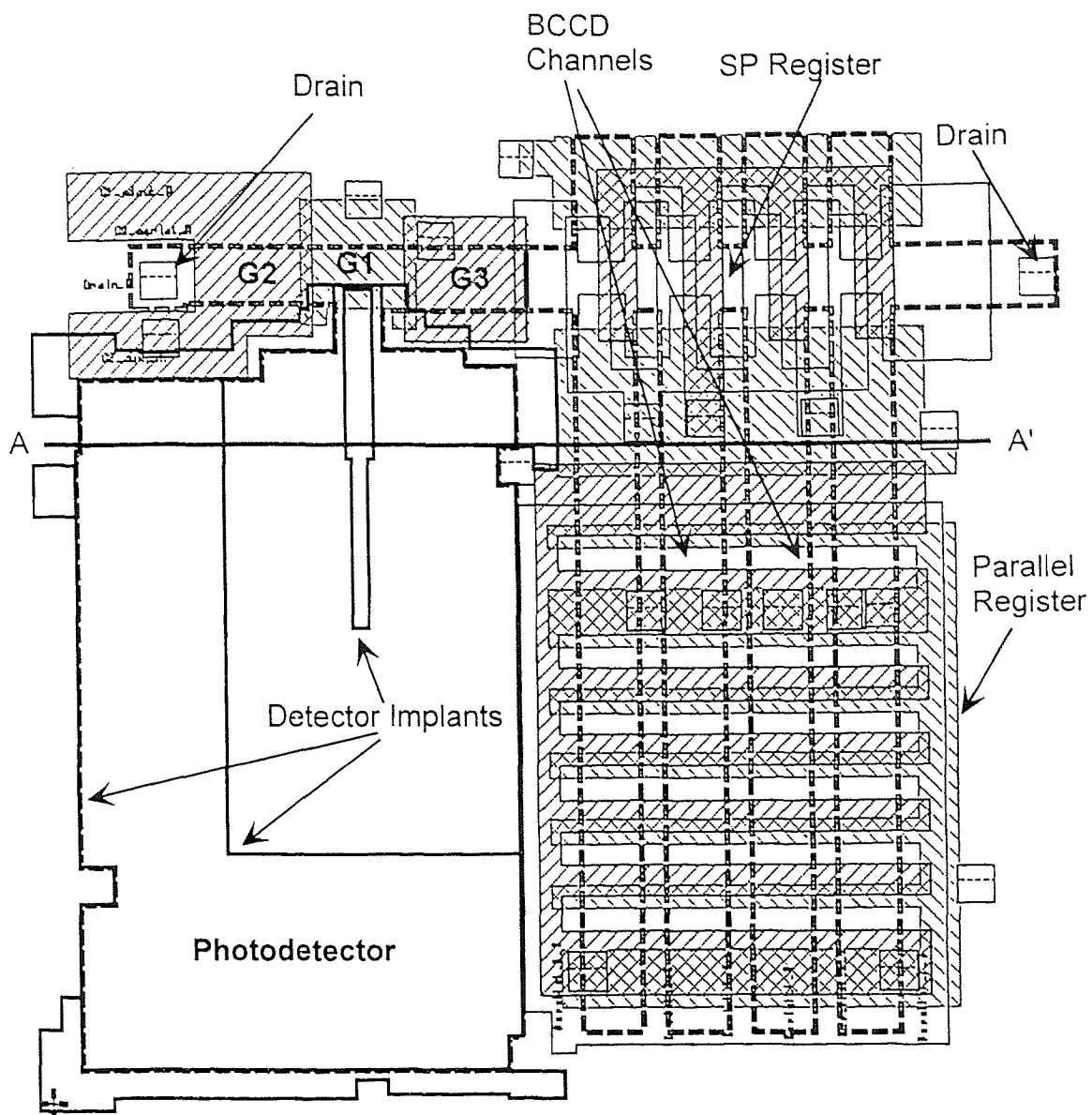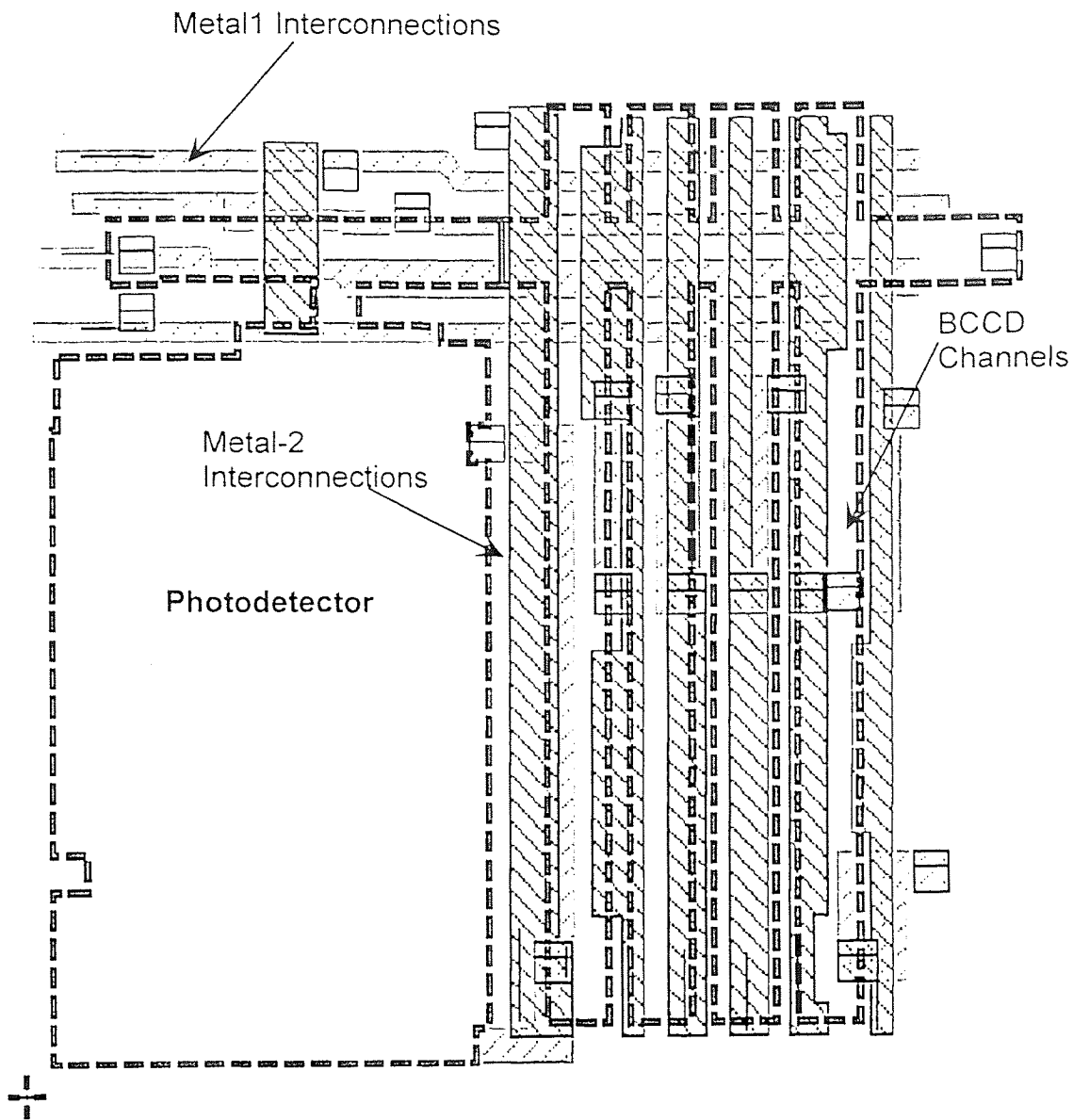
Figure 4.2 *Metal interconnections in a macropixel*
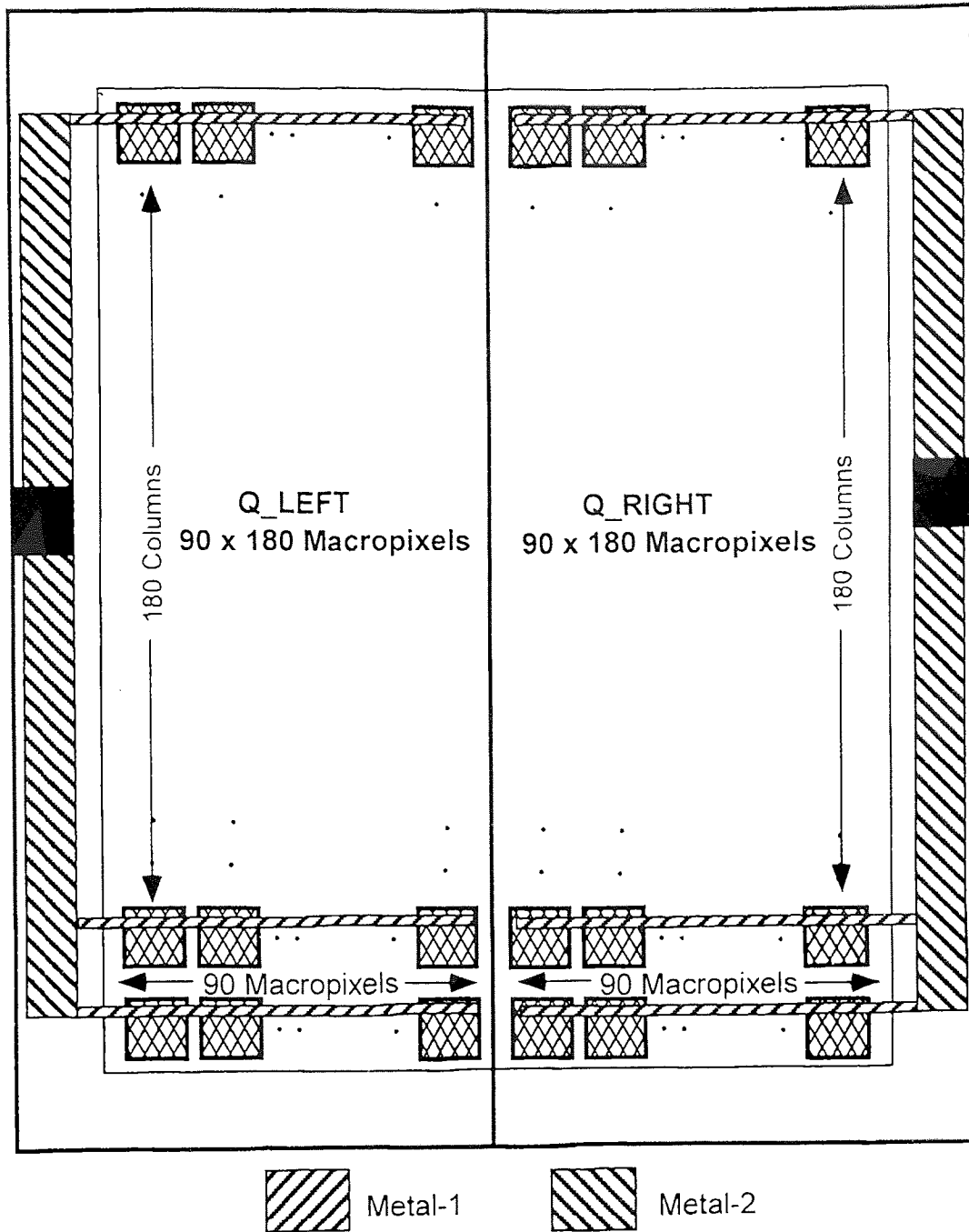
Figure 4.3 *Metal routing for non-critical clocks*
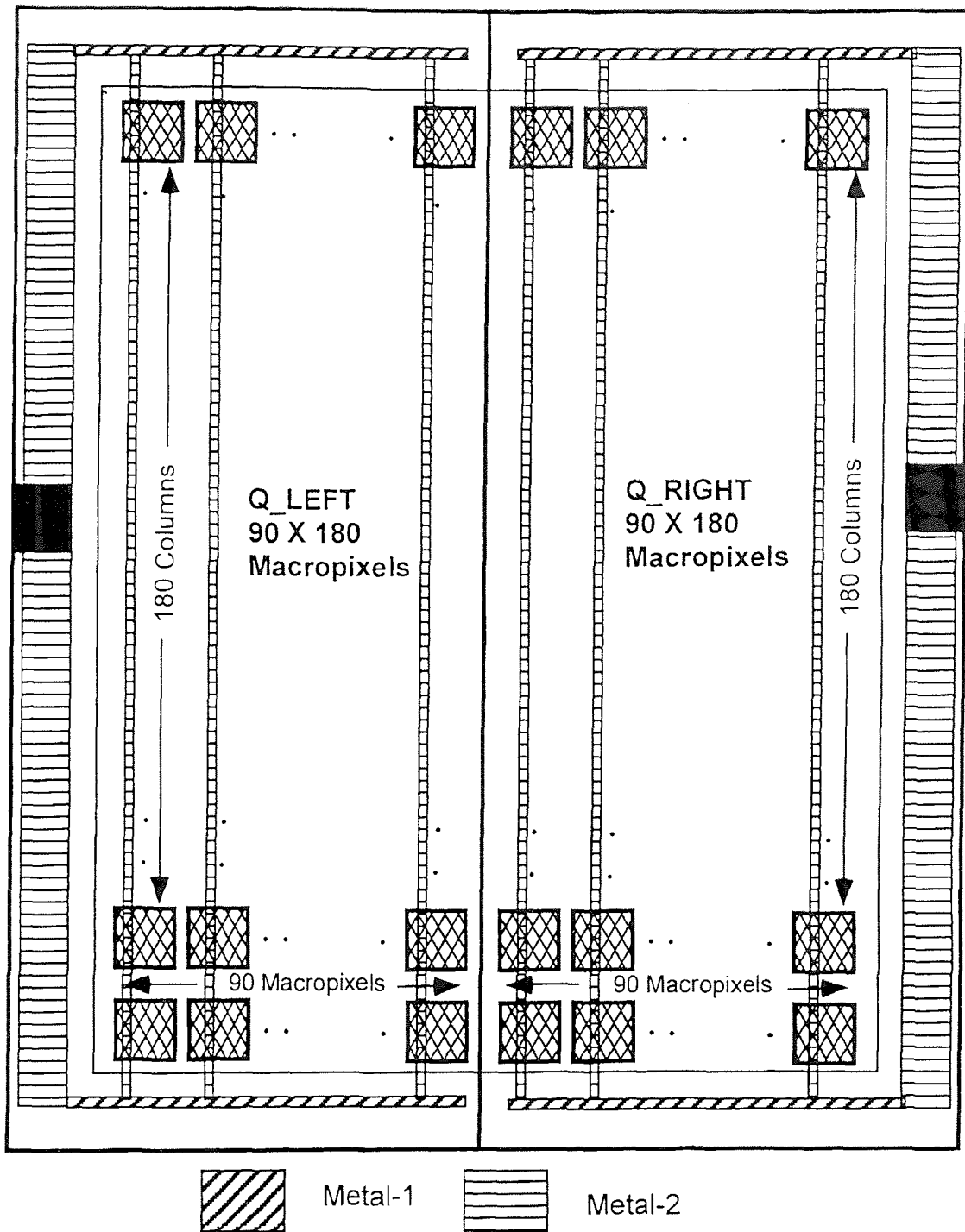
Figure 4.4 *Metal routing for critical clocks*

(a)

(b)
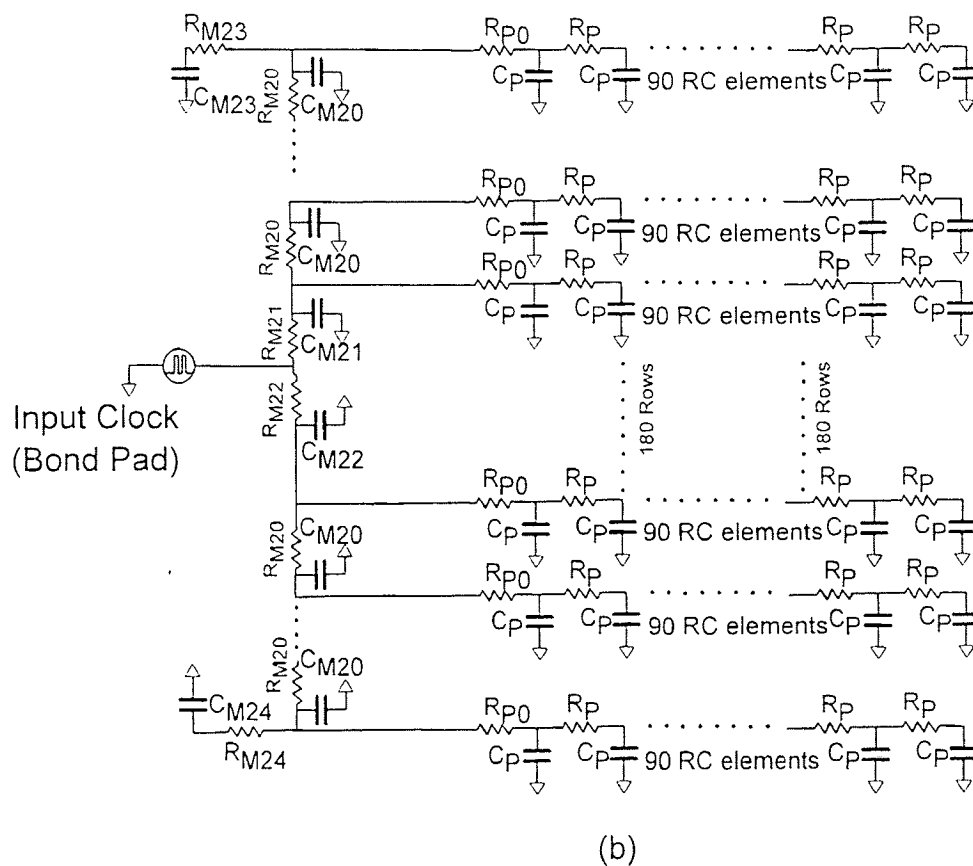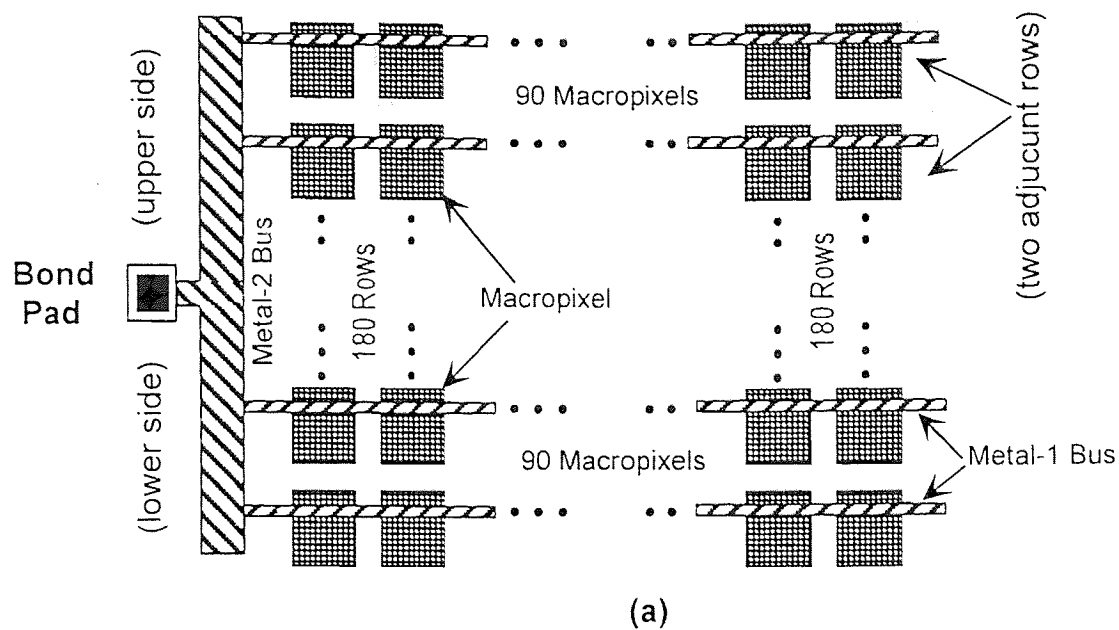
Figure 4.5 *Metal interconnections for structure-1 in (a), and its equivalent RC circuit in (b)*
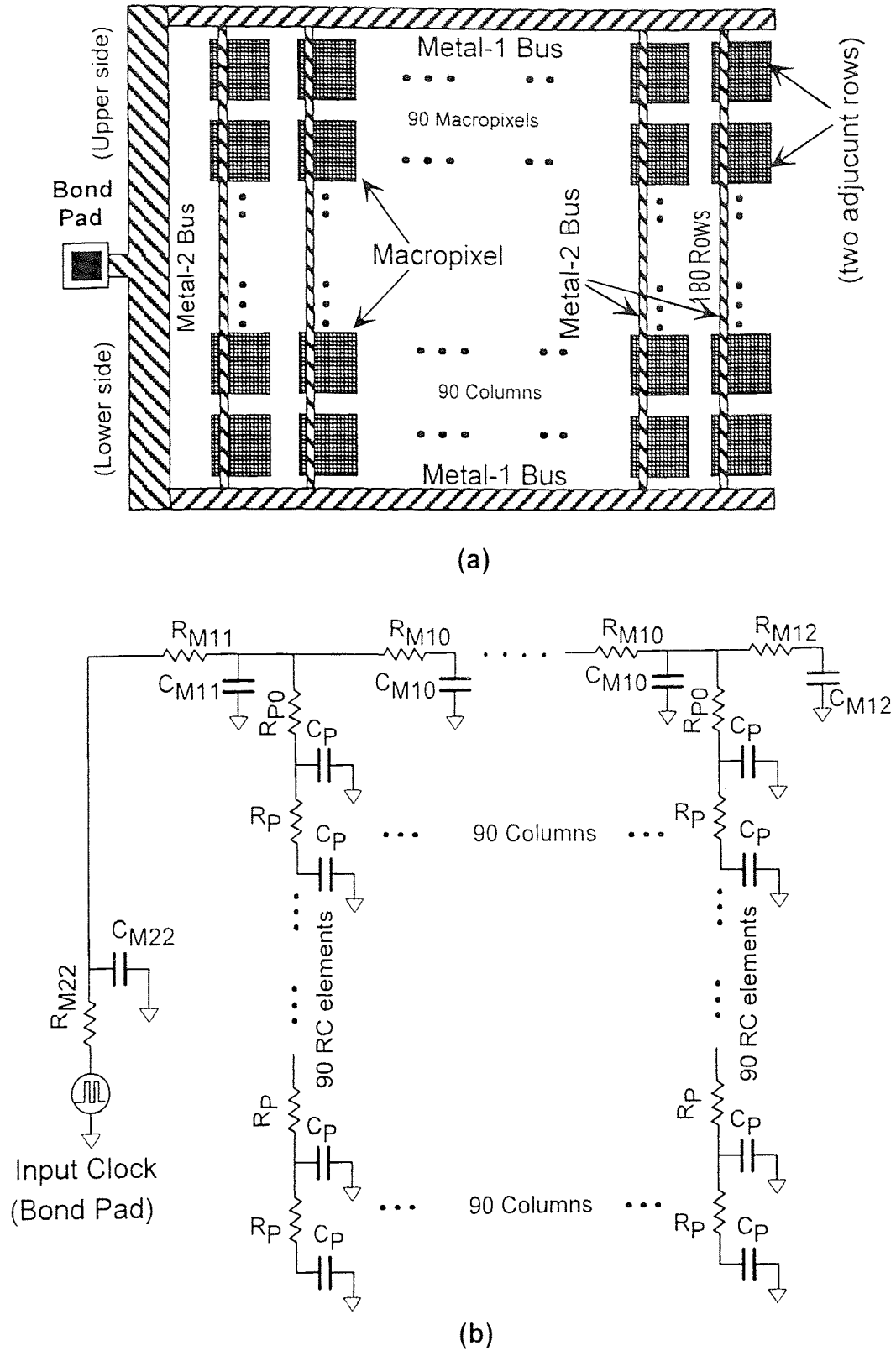
Figure 4.6 *Metal interconnections for structure-2 in (a), and its equivalent RC circuit in (b)*
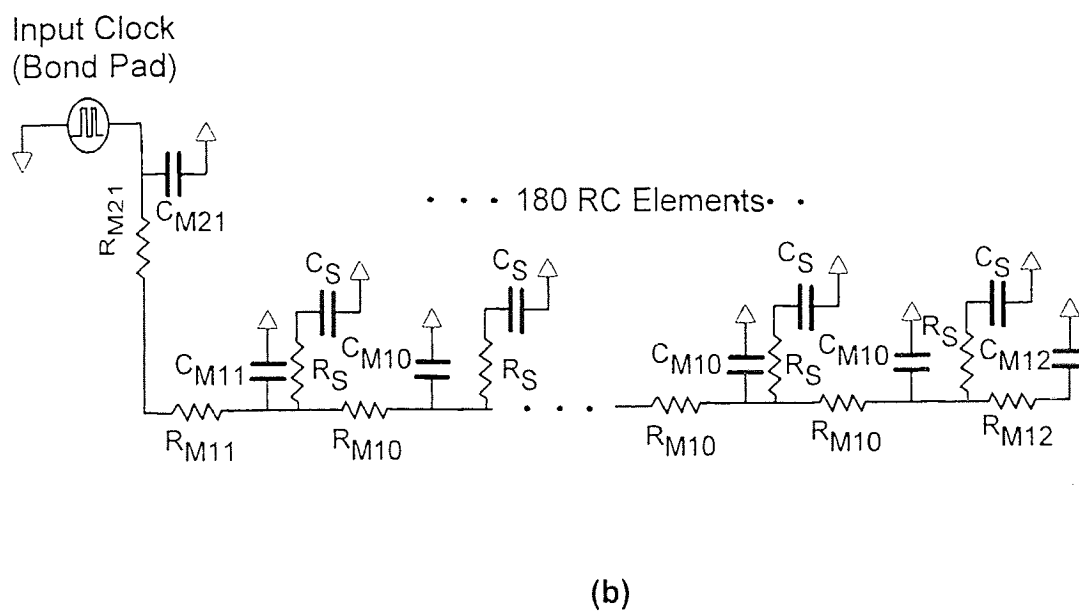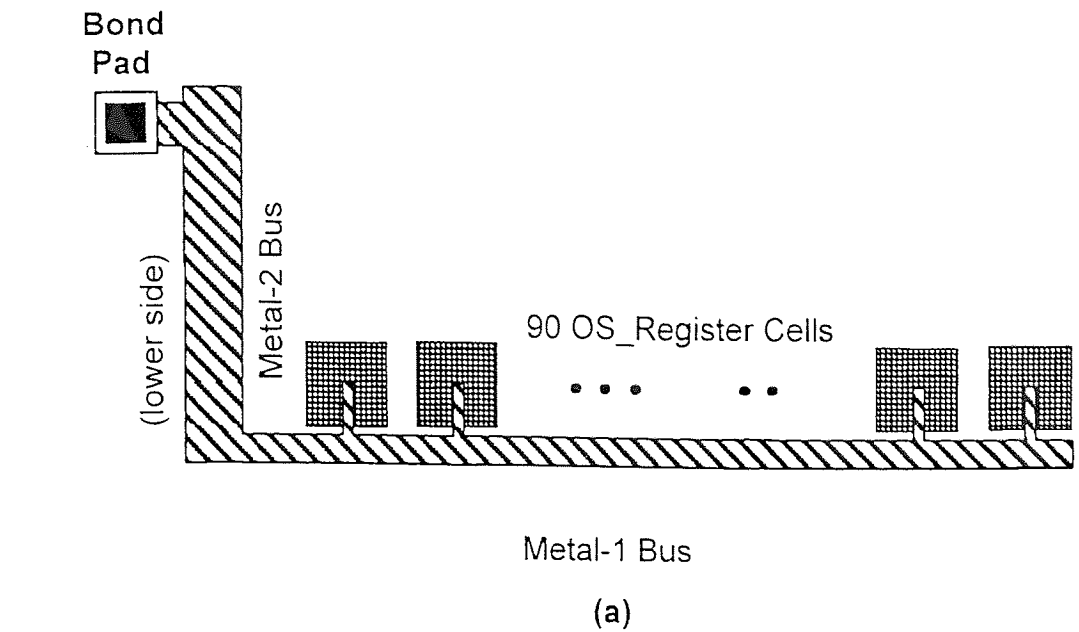
Figure 4.7 *Metal interconnections for structure-3 in (a), and its equivalent RC circuit in (b)*
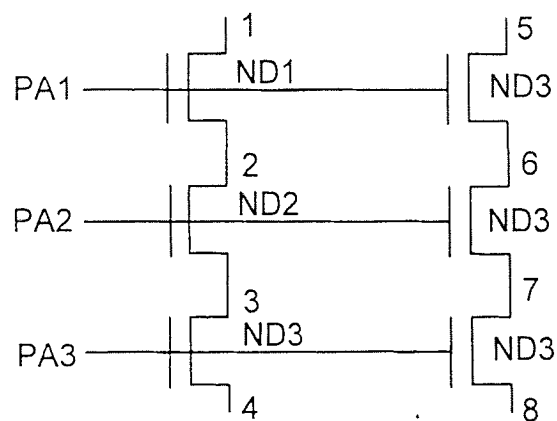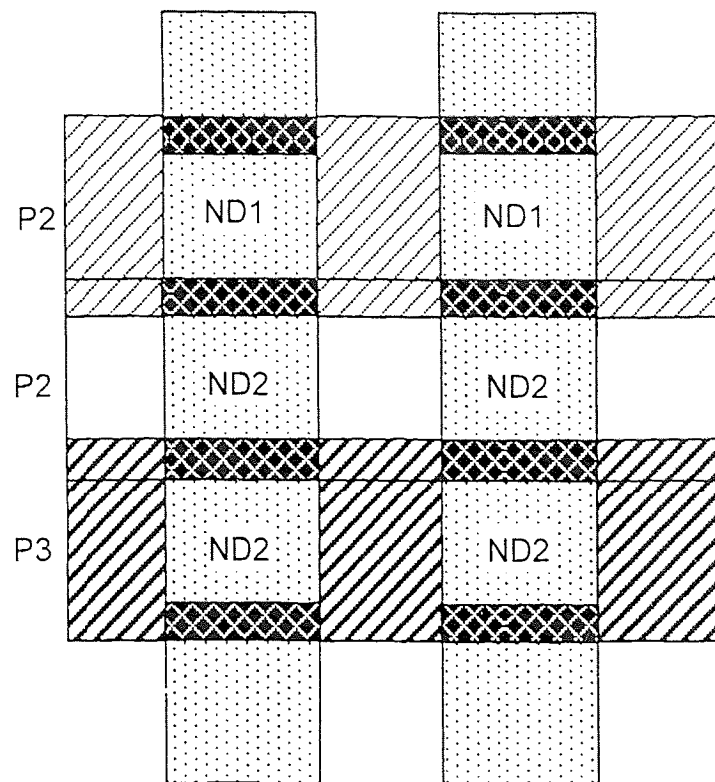
Figure 4.8 *Linear CCD array and its equivalent MOS circuit*
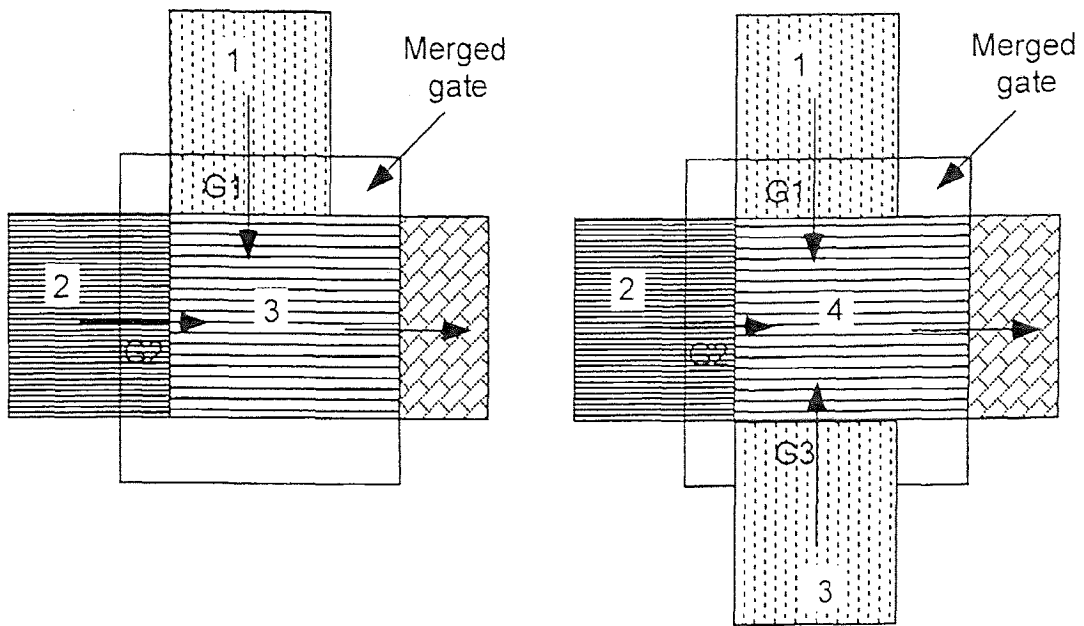
(a)
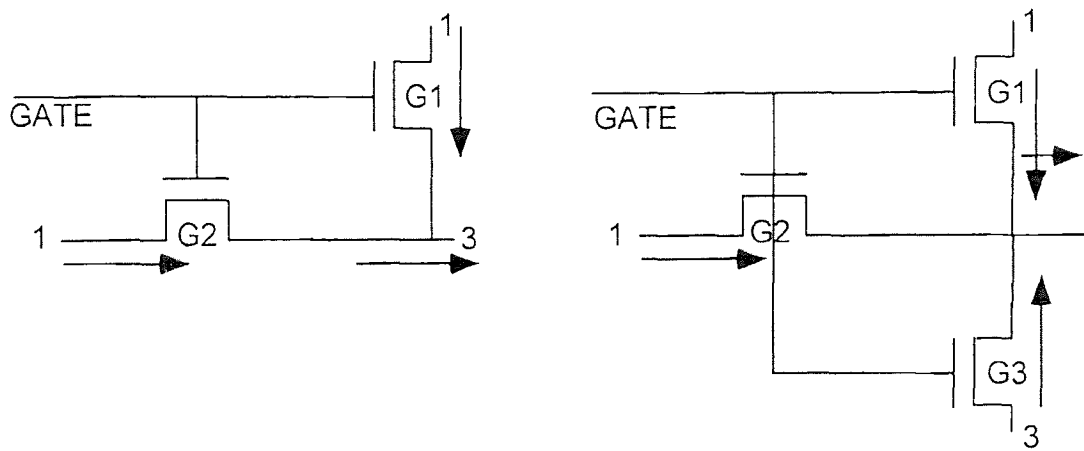
(b)

Figure 4.9 *Merged channel CCDs and its MOS equivalent circuits, (a) two channels merged and (b) three channels merged*
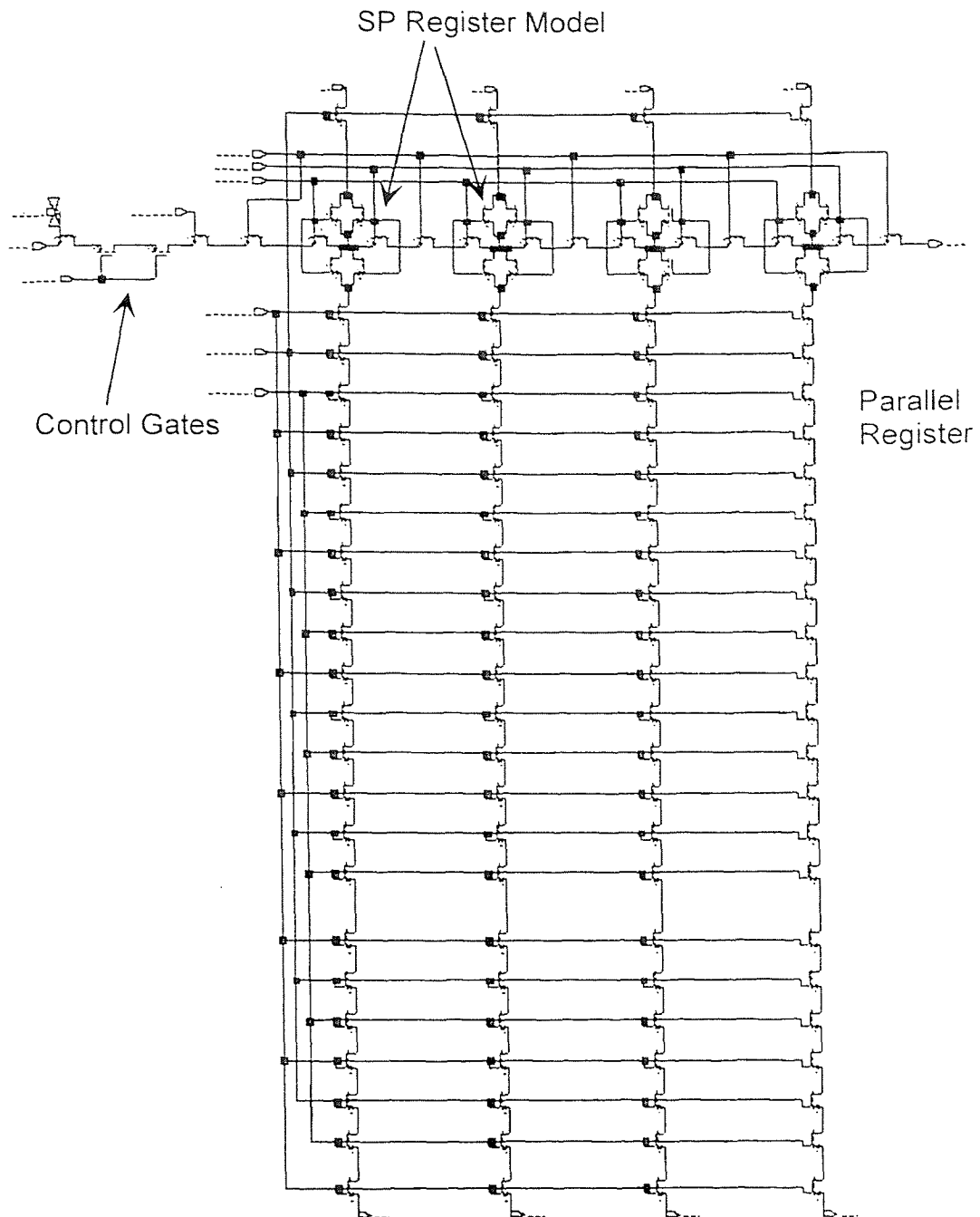
Figure 4.10 *Equivalent schematic for macropixel*
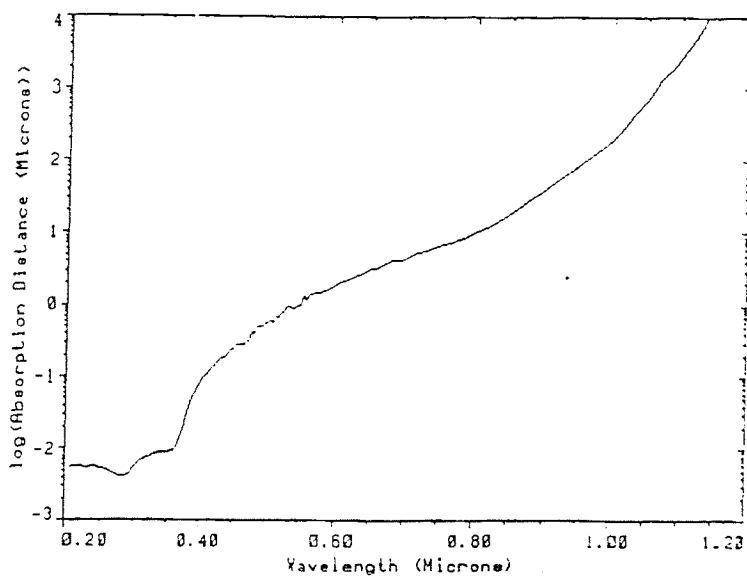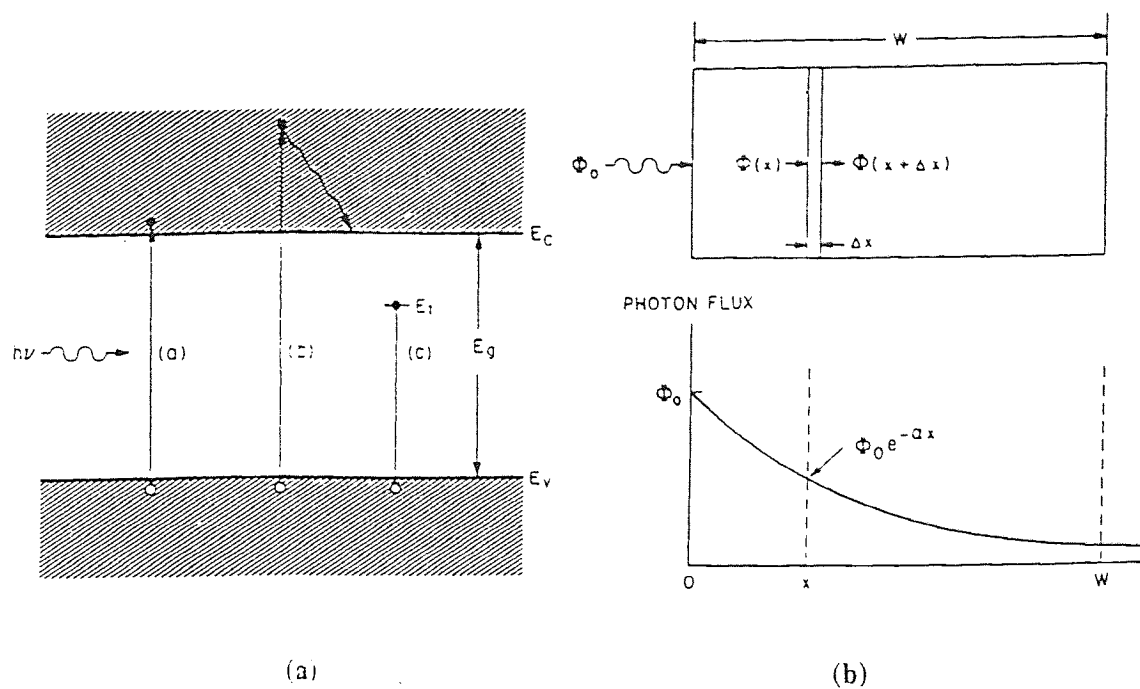
Figure 5.1 *Optical absorption for hv=E_g, hv> E_g and hv< E_g in (a), optical absorption in semiconductor under illumination and exponential decay of photon flux in (b), and absorption distance of light in silicon as a function of wavelength in (c).*
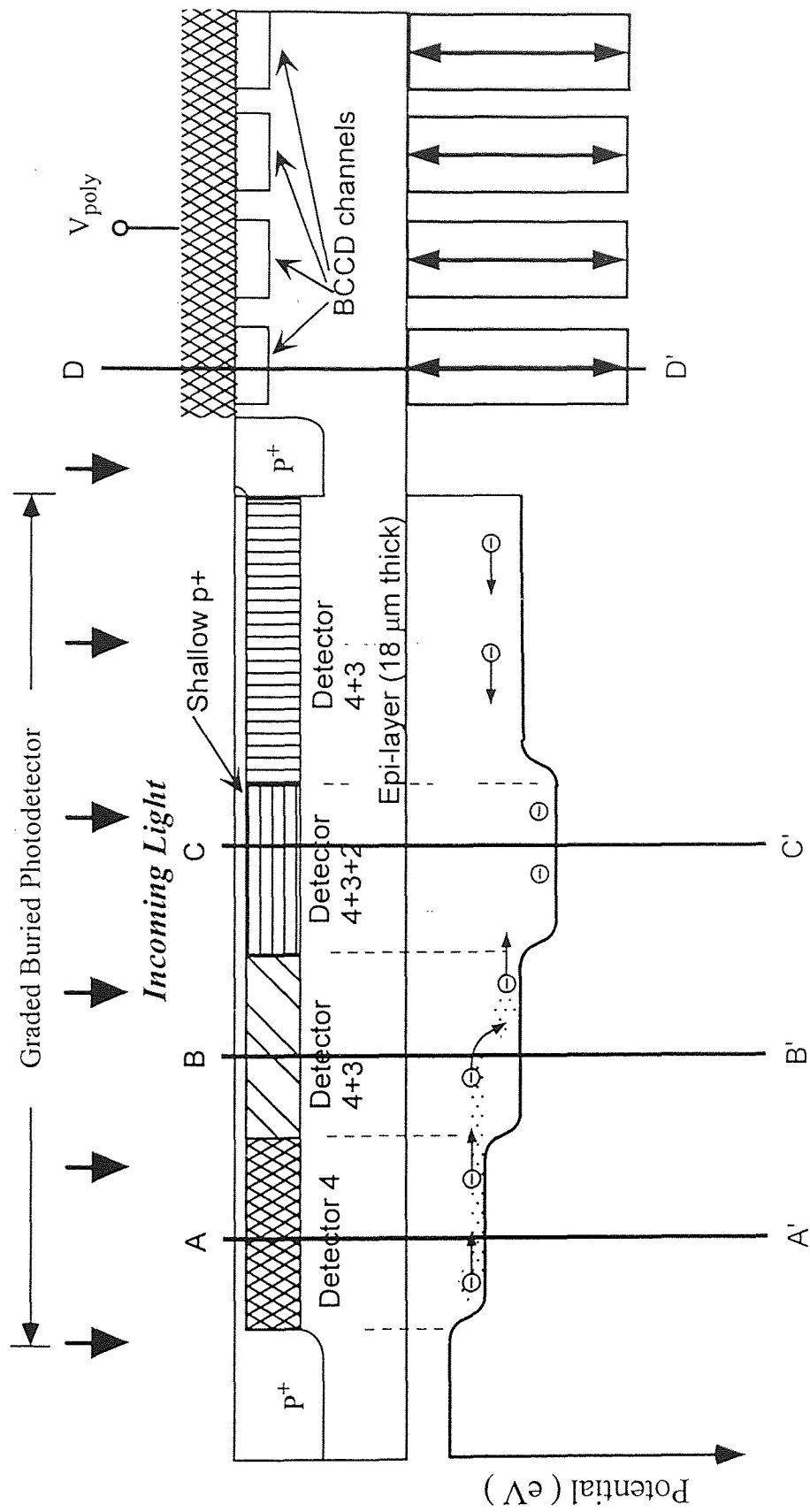
Figure 5.2 *The cross-sectional drawing of the UHFR-1 macropixel layout along the A-A' line shown in figure 4.1.*
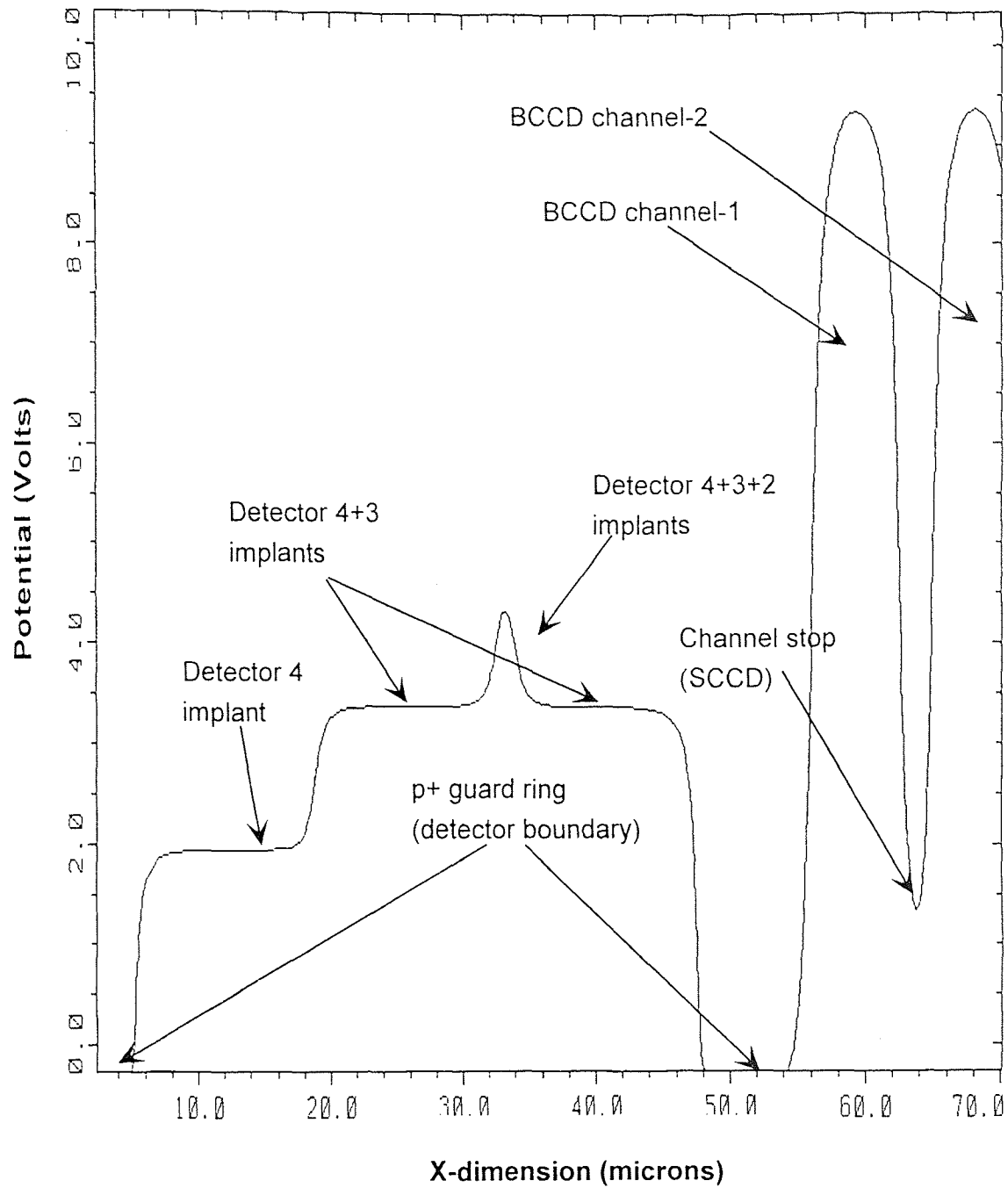
Figure 5.3 *Simulated values of maximum potential in the UHFR-1 device cross-section shown in figure 5.2 along the X-dimension.*
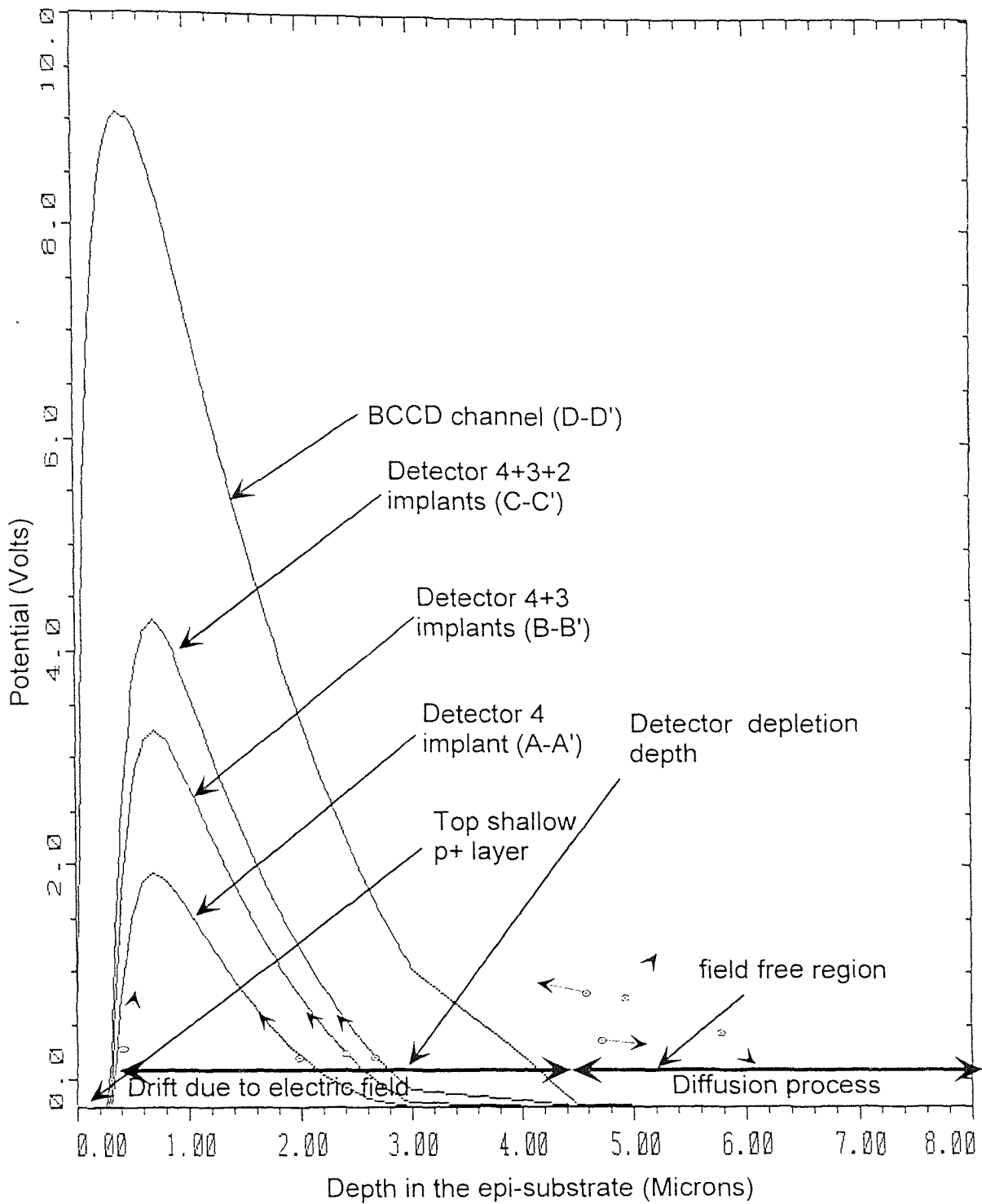
Figure 5.4 *Simulated values of potential in the UHFR-I macropixel regions shown in figure 5.2 along the depth dimension.*
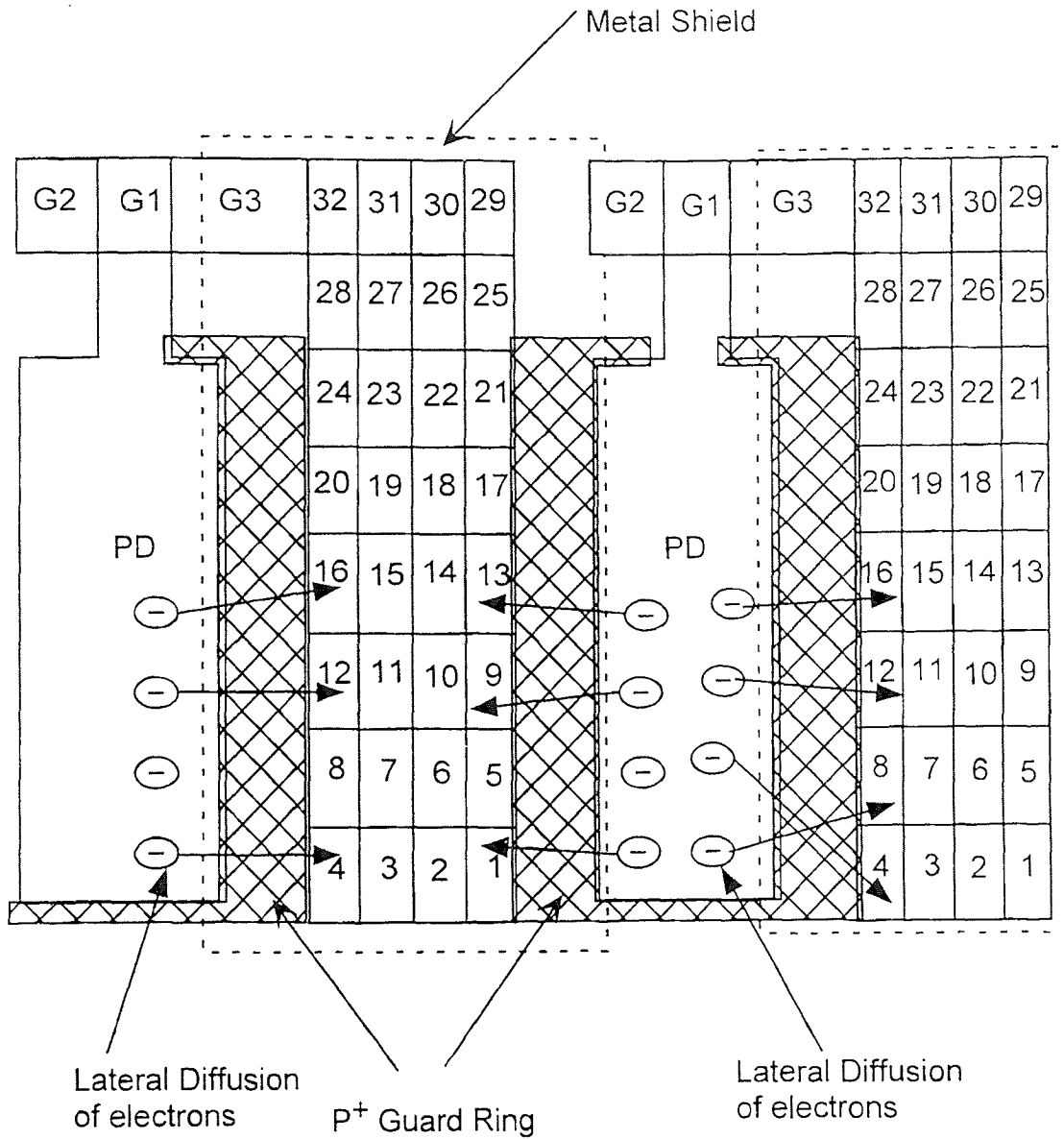
Figure 5.5 *Crosstalk Signal generation in a UHFR-1 Macropixel*

Detector
4+3+2 implants

Detector
4+3 implants

Detector
4 implant

BCCD Channel-4

BCCD Channel-3

BCCD Channel-2

BCCD Channel-1

p+ region

Pot (Volts)

5.00

0.00

Pot (Volts)

5.00

0.00
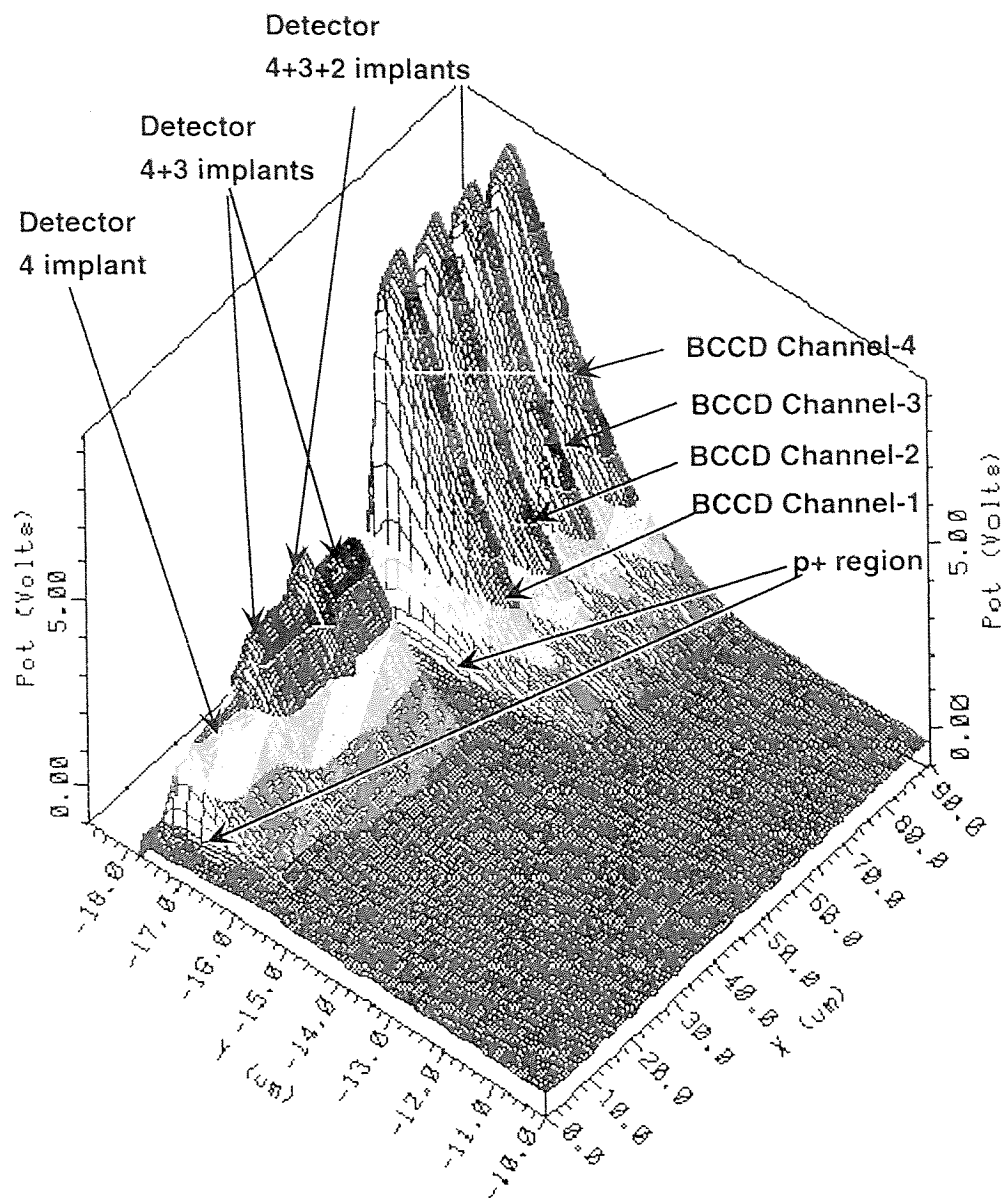
Figure 5.6 *Initial potential distribution in the macropixel region of UHFR-I device.*
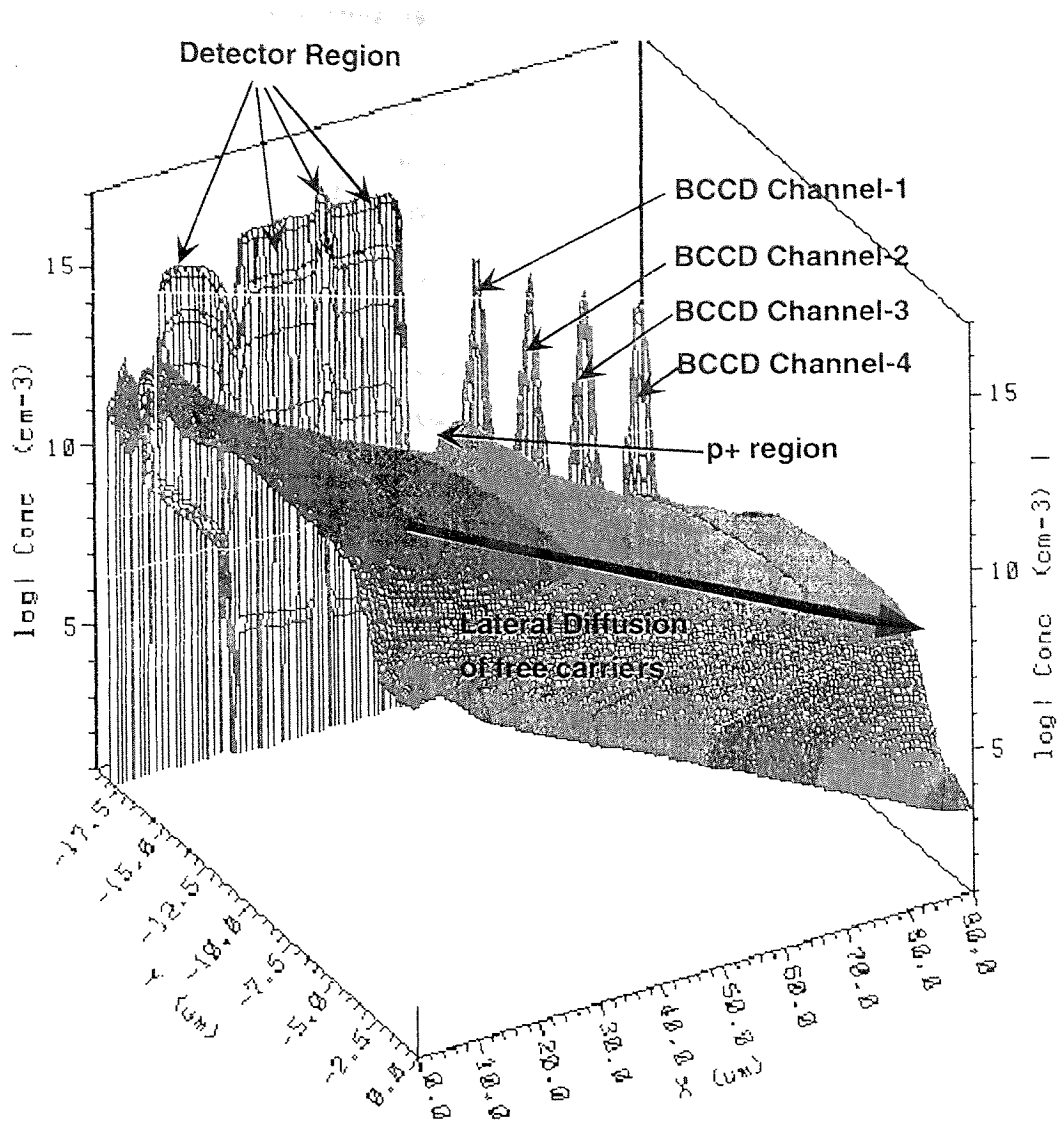
Figure 5.7 *Photogenerated electron distribution in the macropixel region after a light source of 600 nm wavelength, 4 × 10^{20} photons/cm^2 intensity and 0.1 microsecond ON time is stopped.*
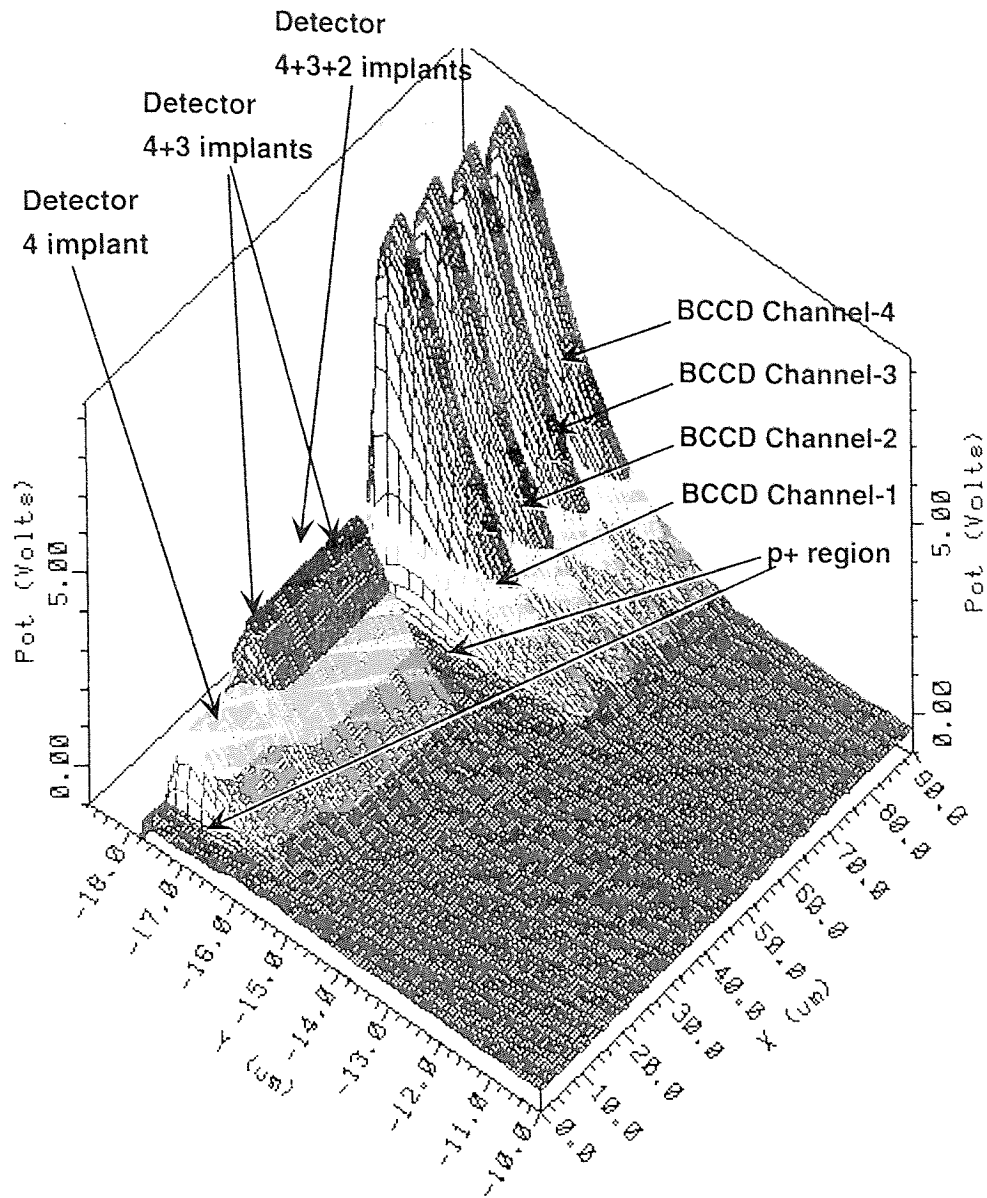
Figure 5.8 *Potential distribution in the macropixel region after a light source of 600 nm wavelength, 4×10^{20} photons/cm^2 intensity and 0.1 microsecond ON time is stopped.*
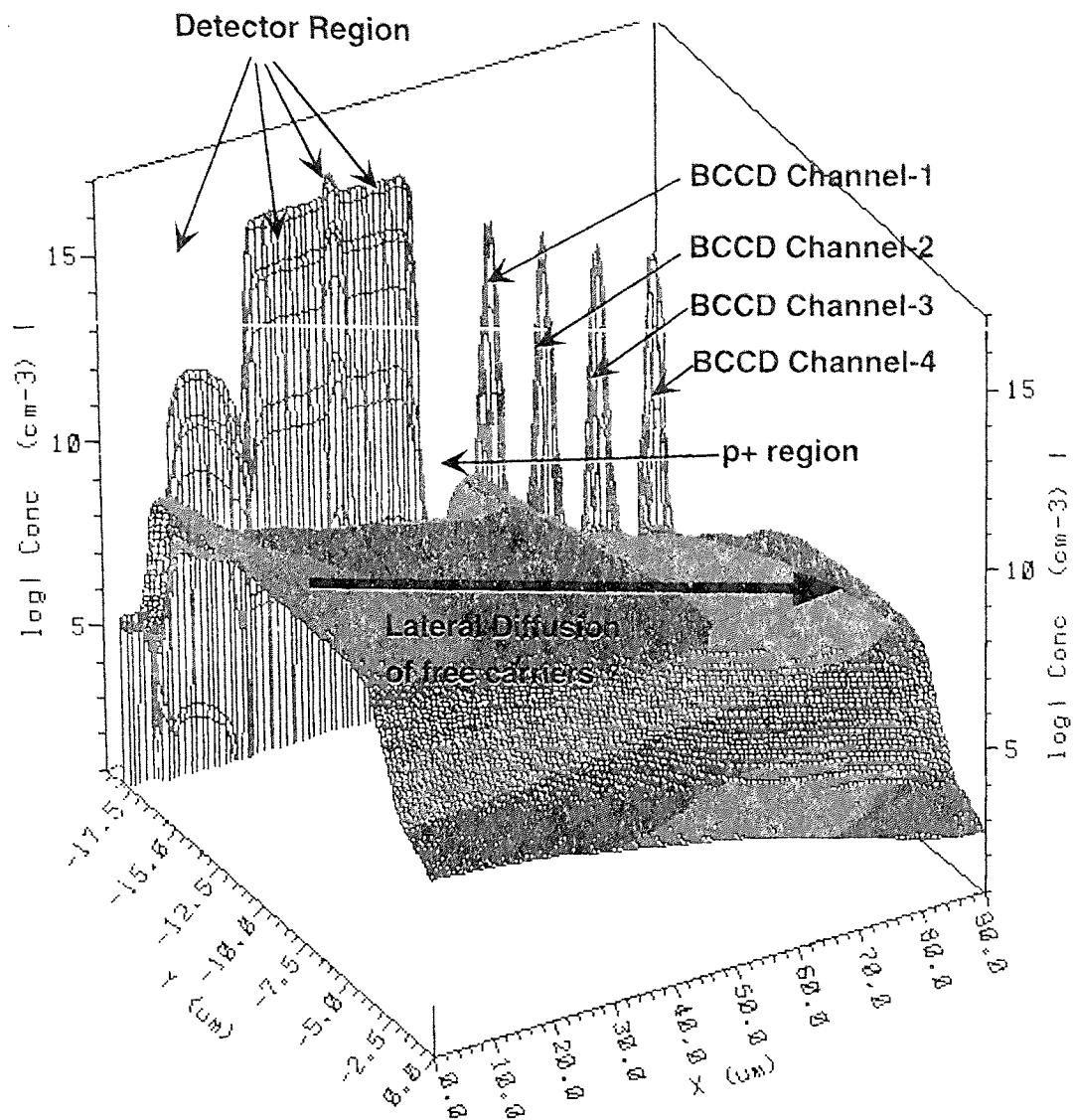
Figure 5.9 *Photogenerated electron distribution in the macropixel region after 0.4 microsecond diffusion of the carriers once the light source is turned off.*
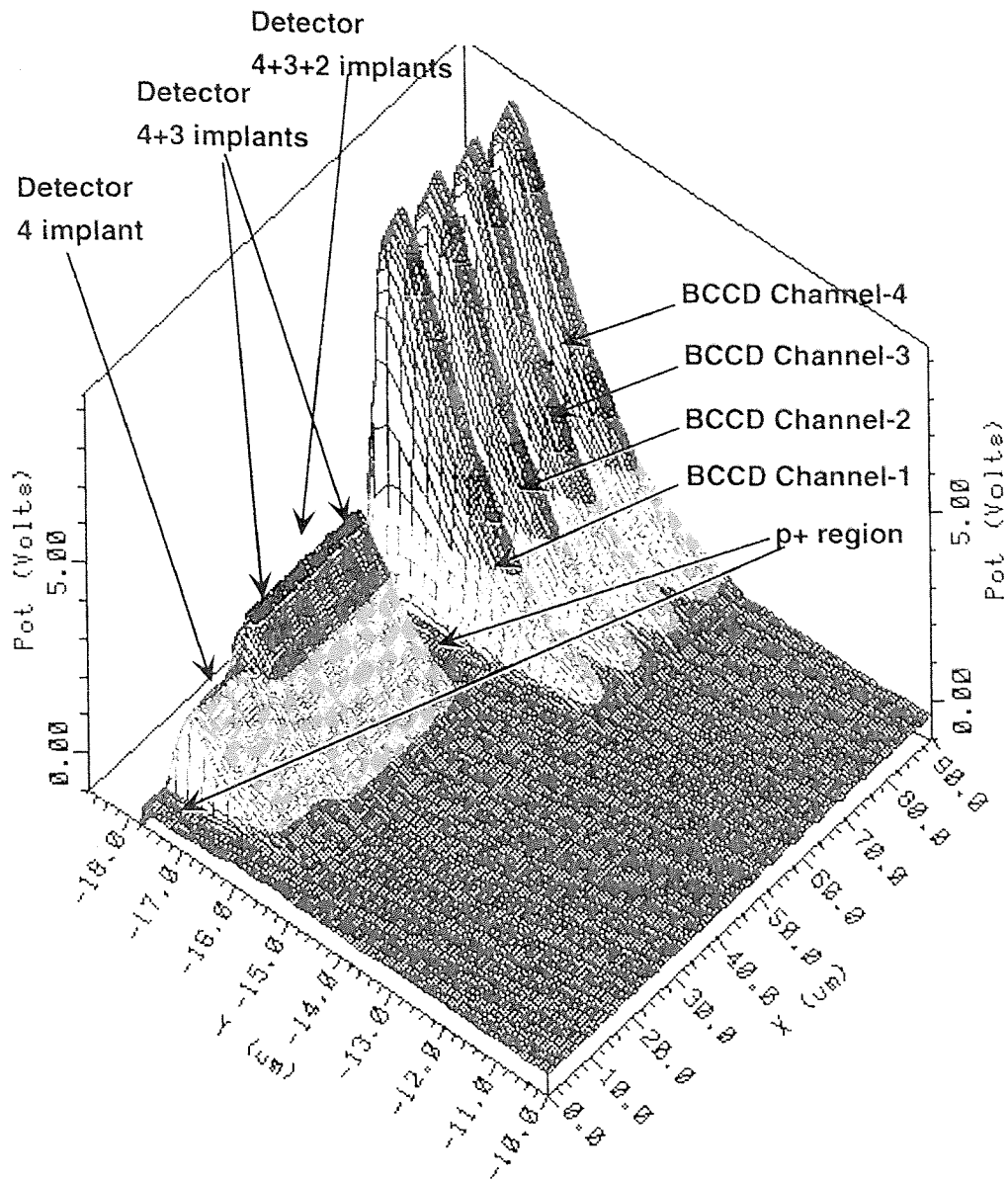
Figure 5.10 *Potential distribution in the macropixel region after 0.4 microsecond diffusion of the carriers once the light source is turned off.*
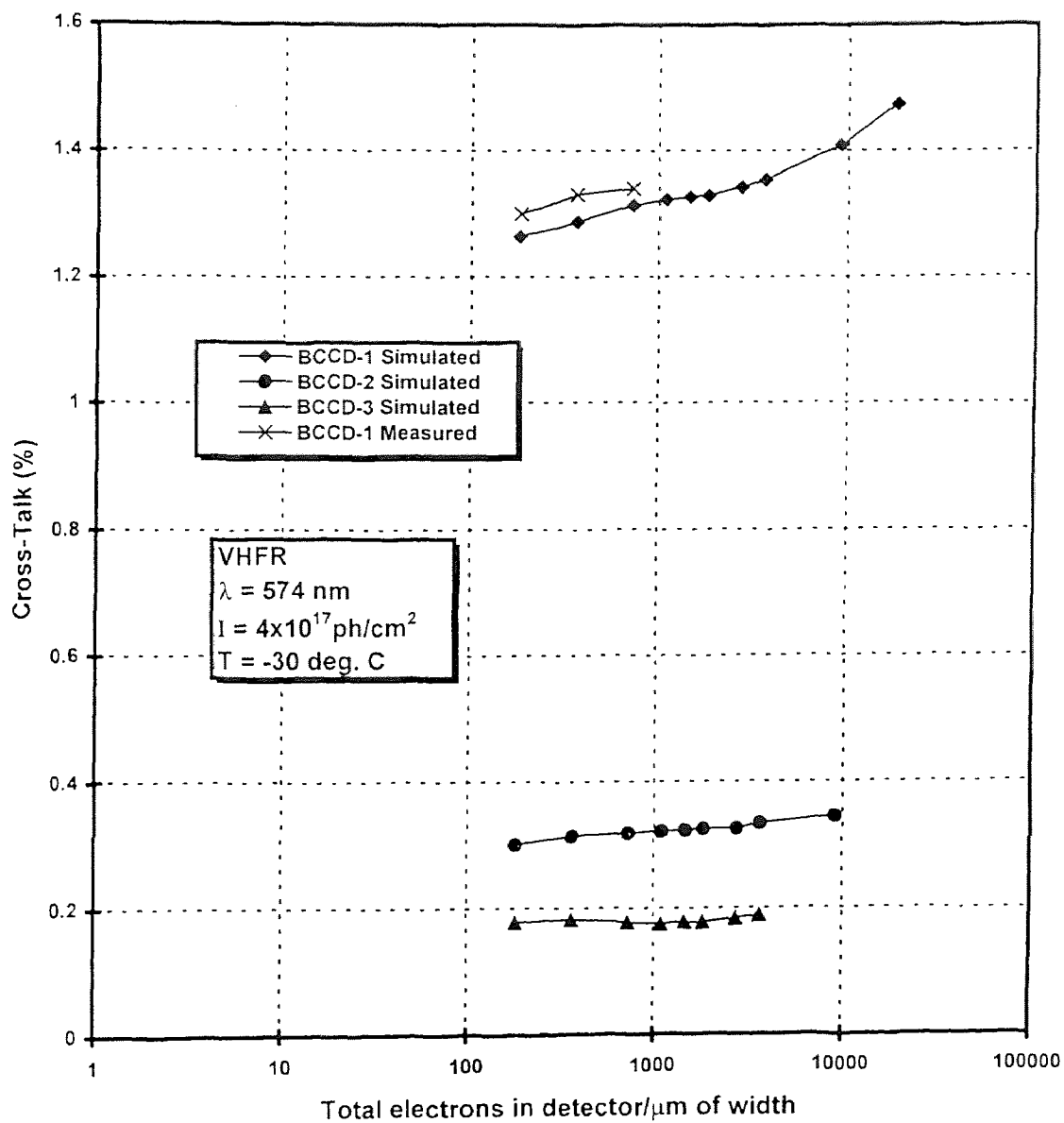
Figure 5.11 *Simulated and Measured values of optical cross talk for VHFR devices as a function of total integrated signal.*
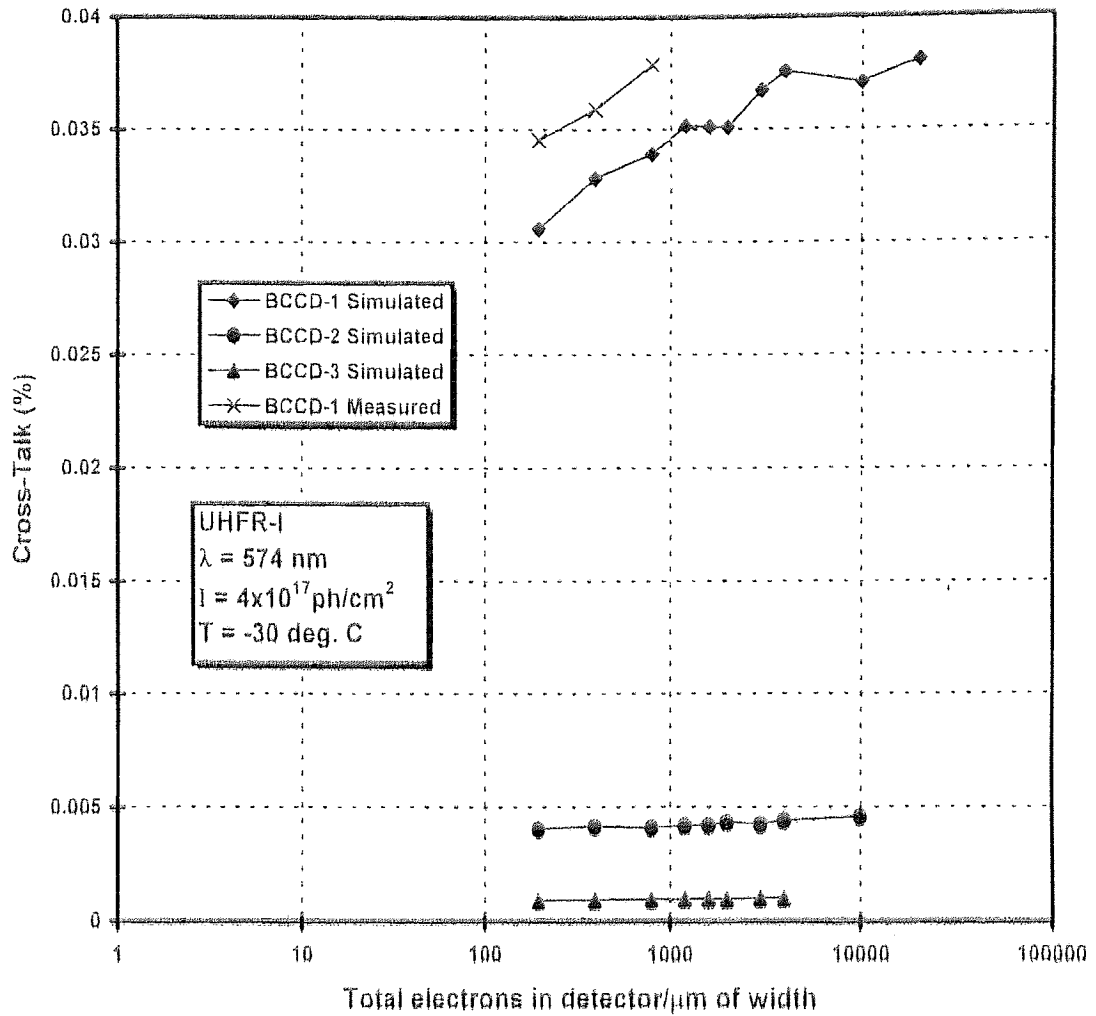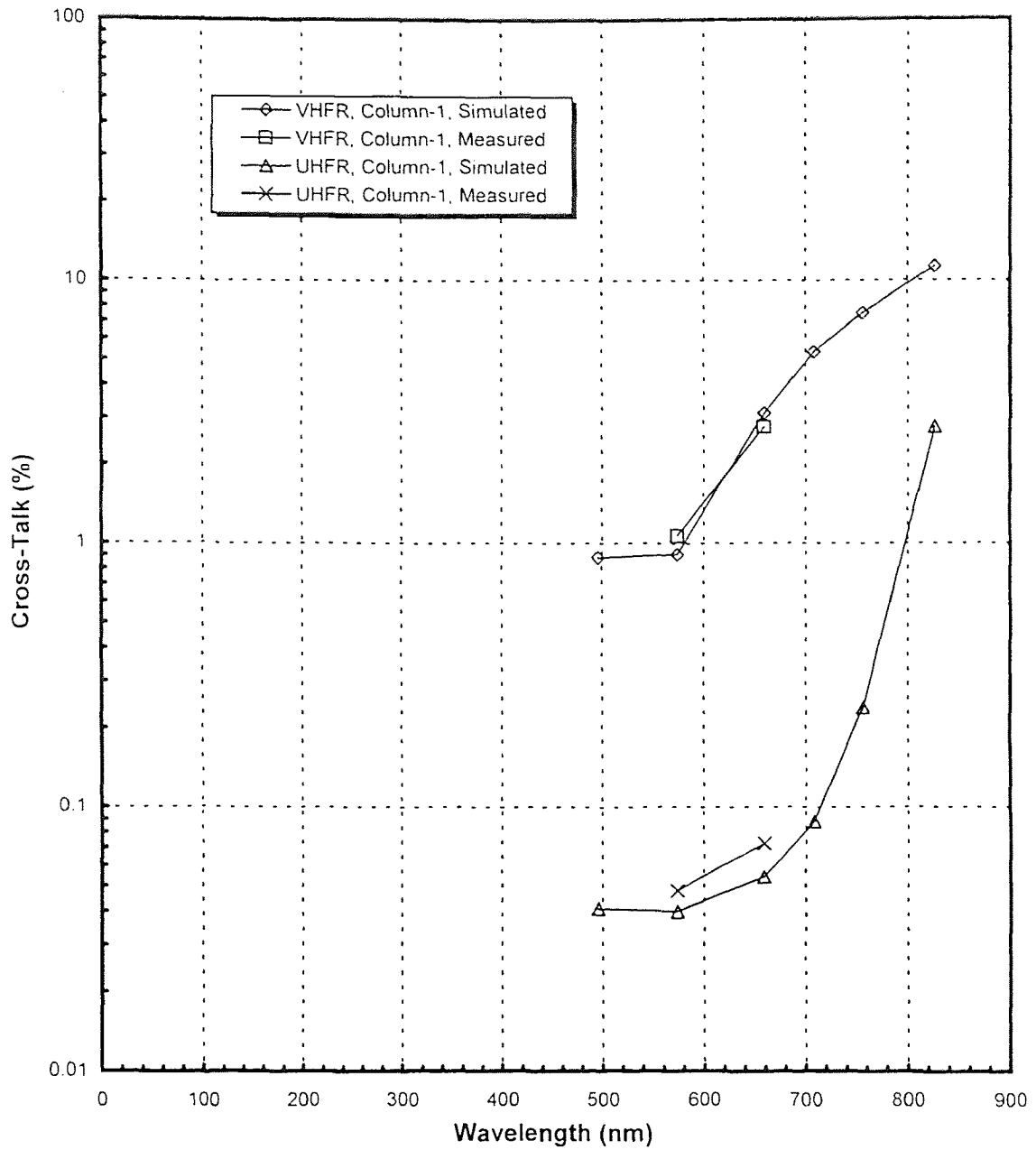
Figure 5.12 *Simulated and Measured values of optical cross talk for UHFR-I devices as a function of total integrated signal.*

Figure 5.13 *Simulated and measured values of optical cross talk for VHFR and UHFR-1 devices at different light source wavelengths.*
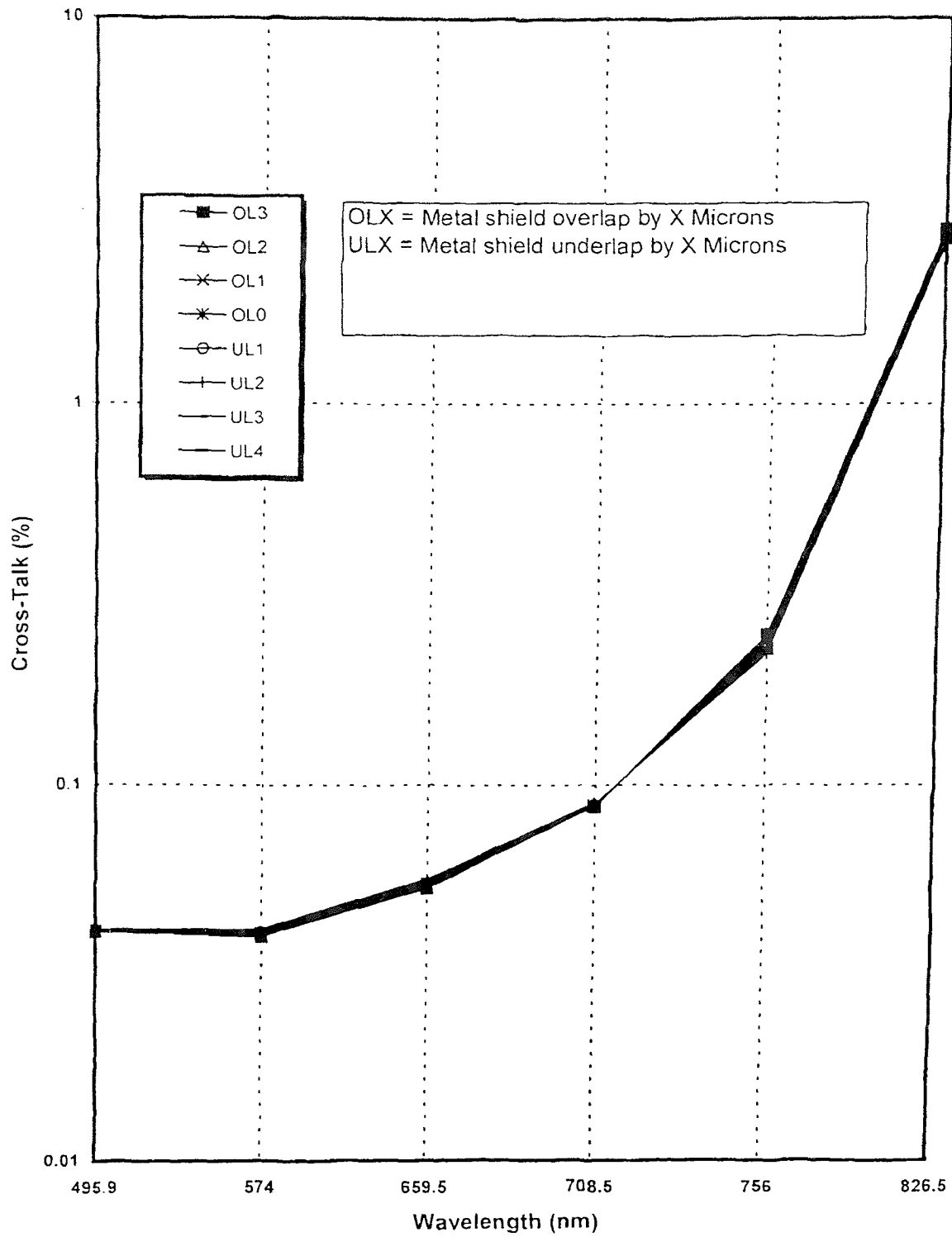
Figure 5.14 *Simulation results characterizing effect of metal shield aperture on the optical cross talk at different light wavelength.*
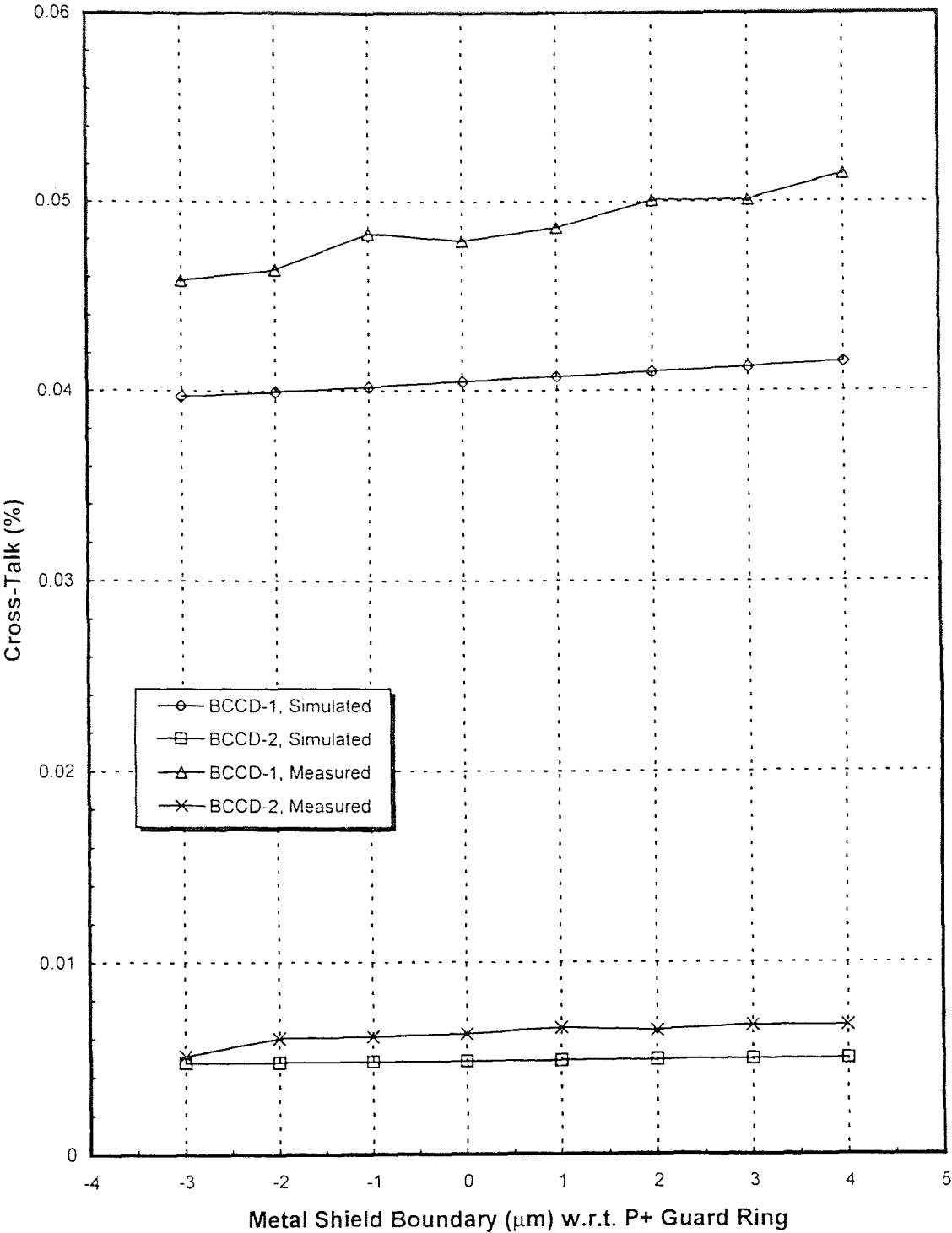
Figure 5.15 *Simulated and measured values of optical cross talk in BCCD-1 and BCCD-2 registers as a function of Metal Shield Opening at 574 nm light source wavelength.*
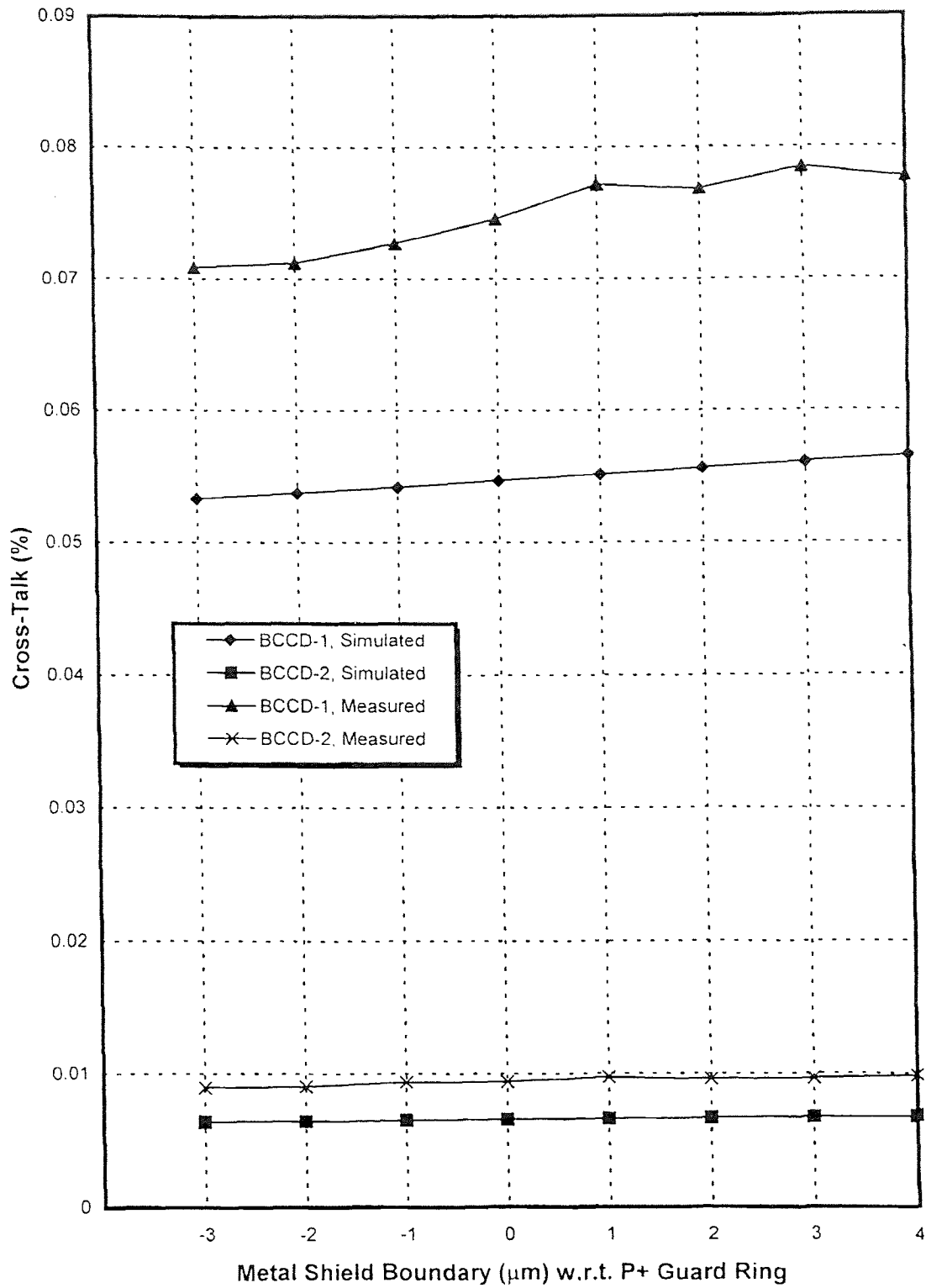
Figure 5.16 *Simulated and measured values of optical cross talk in BCCD-1 and BCCD-2 registers as a function of Metal Shield Opening at 659.5 nm light source wavelength.*
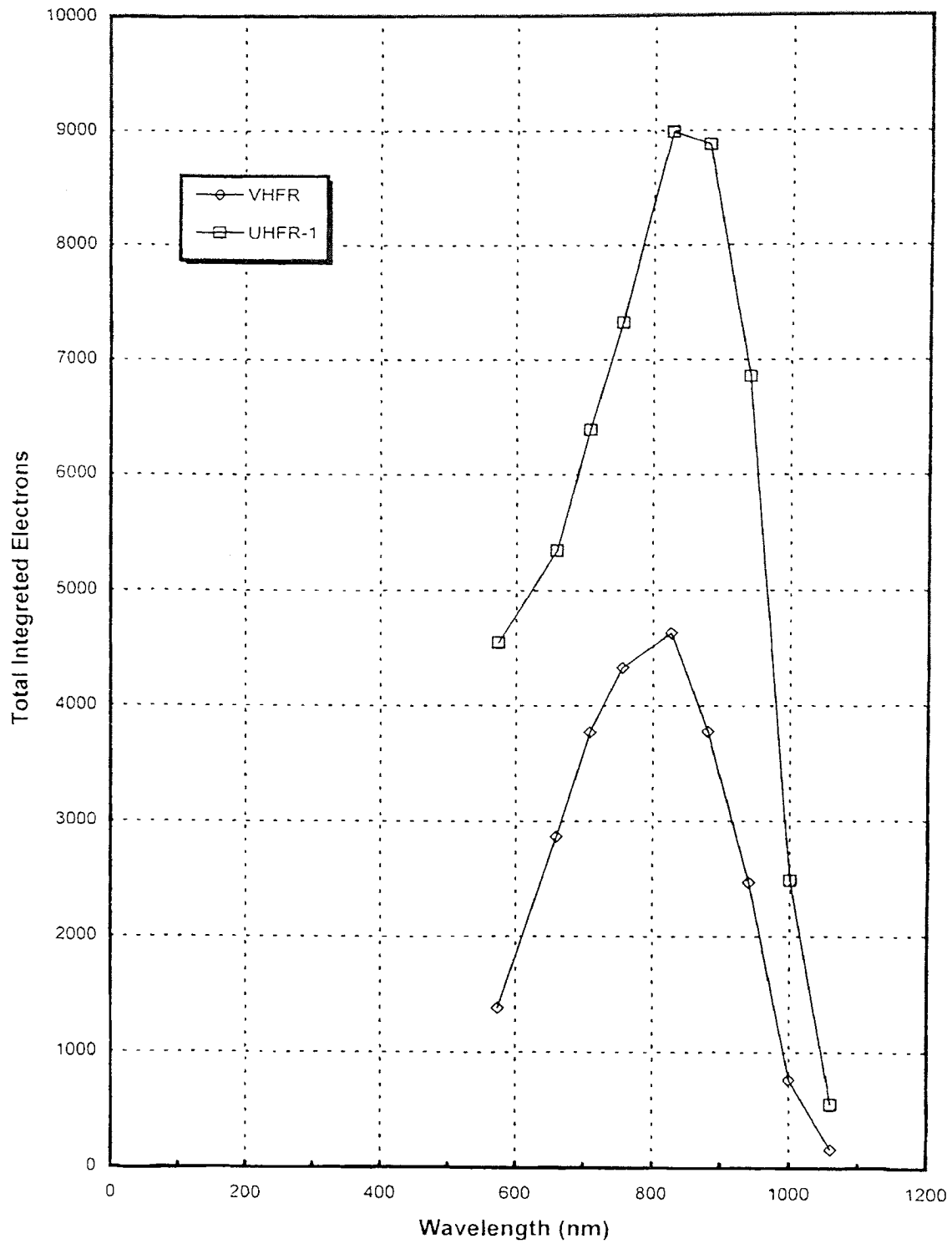
Figure 5.17 *Simulated values of total integrated signal as a function of wavelength for VHFR and UHFR-1 devices.*
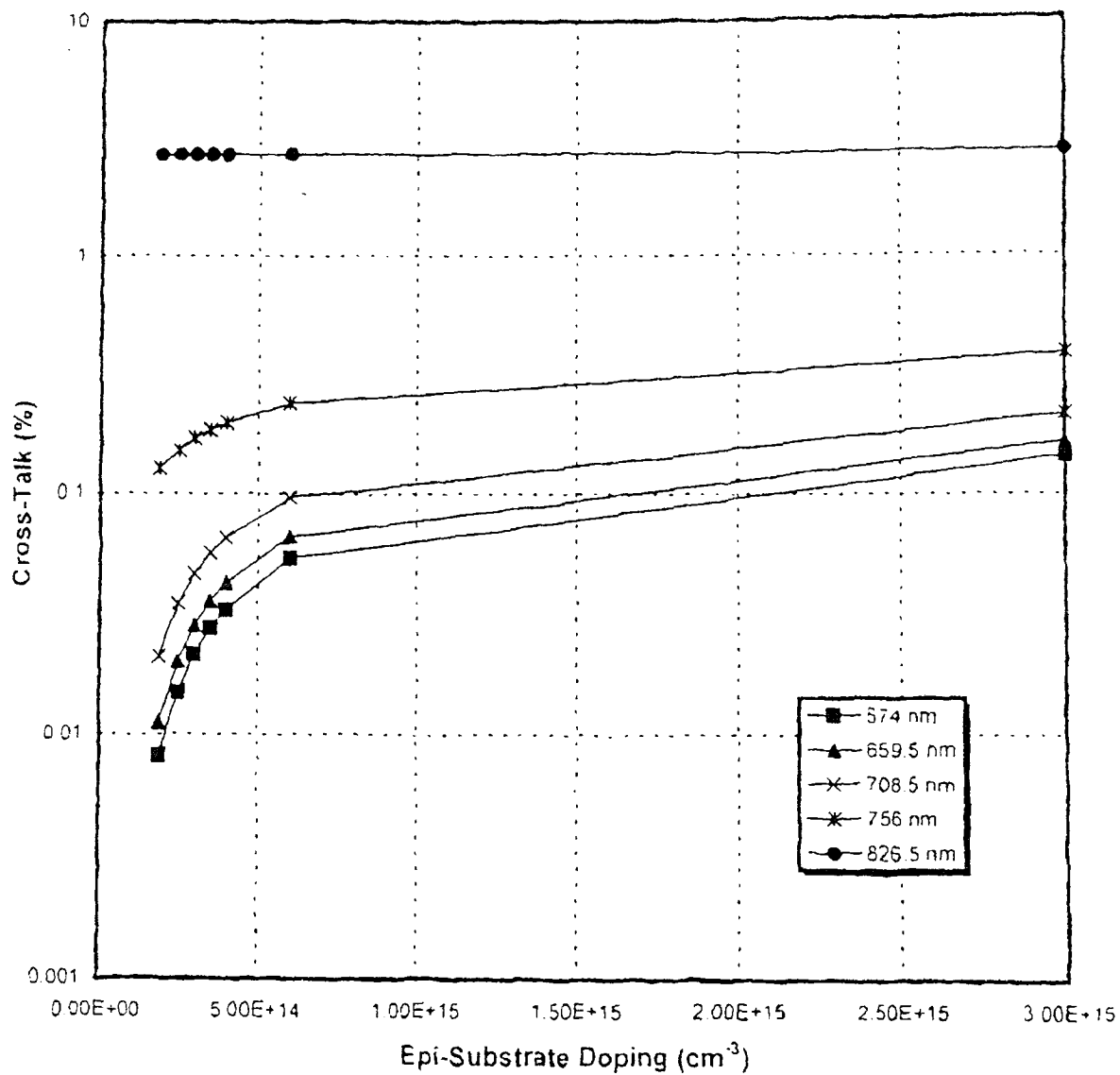
Figure 5.18 *Simulation results characterizing effect of epi layer doping on the optical cross talk at different light wavelength.*
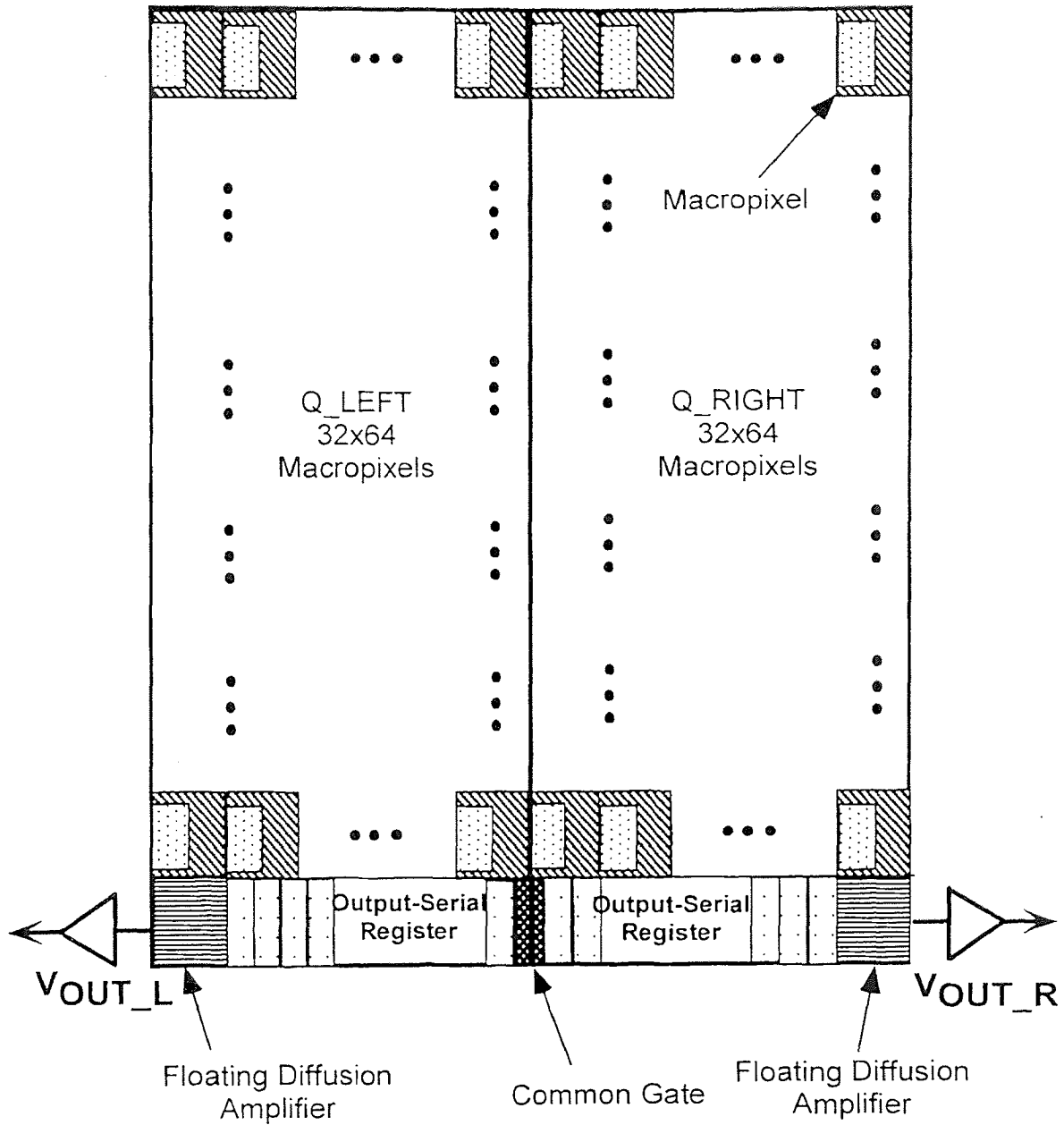
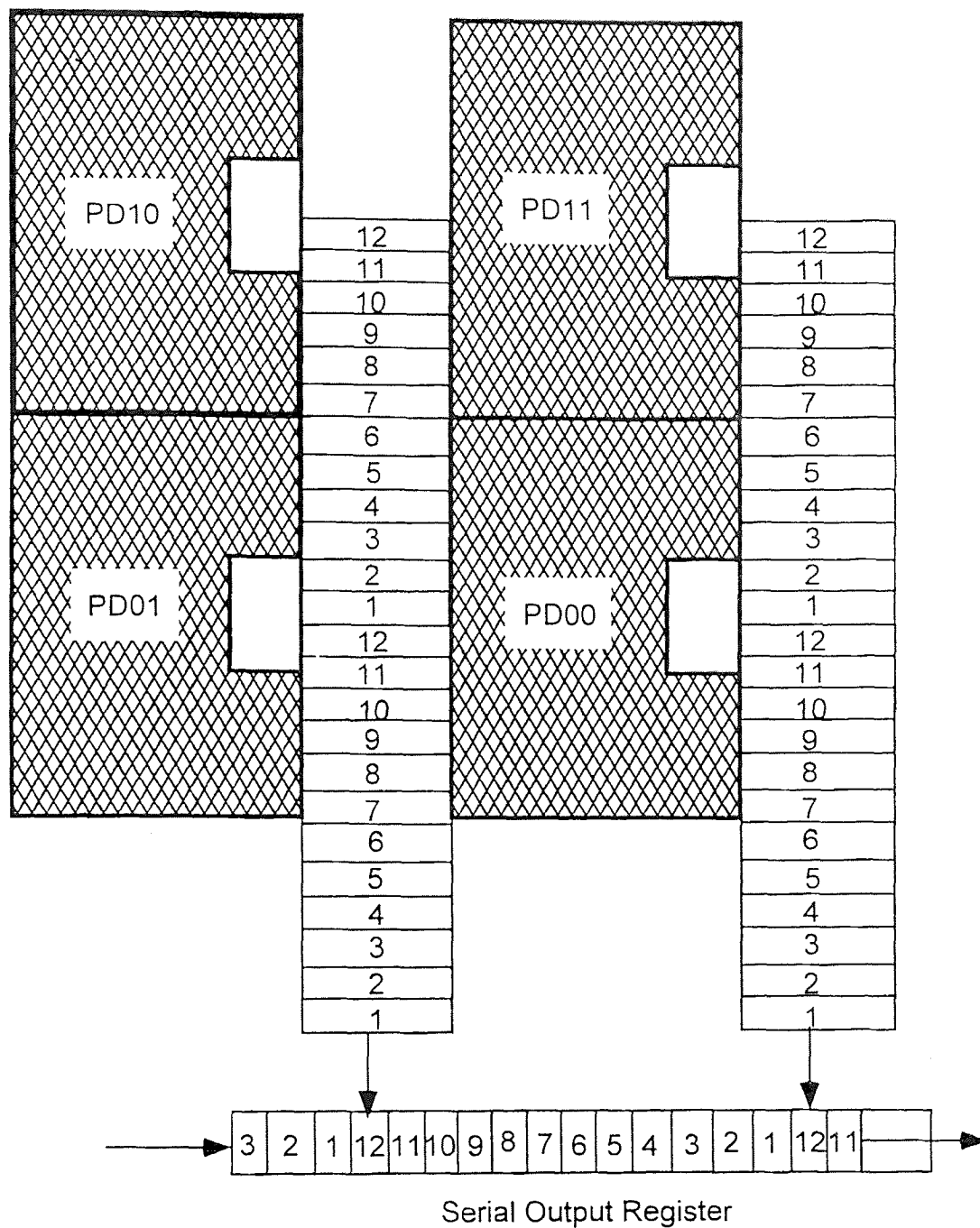**Figure 6.1** *Block diagram of the 64 × 64 element UHFR-II chip*

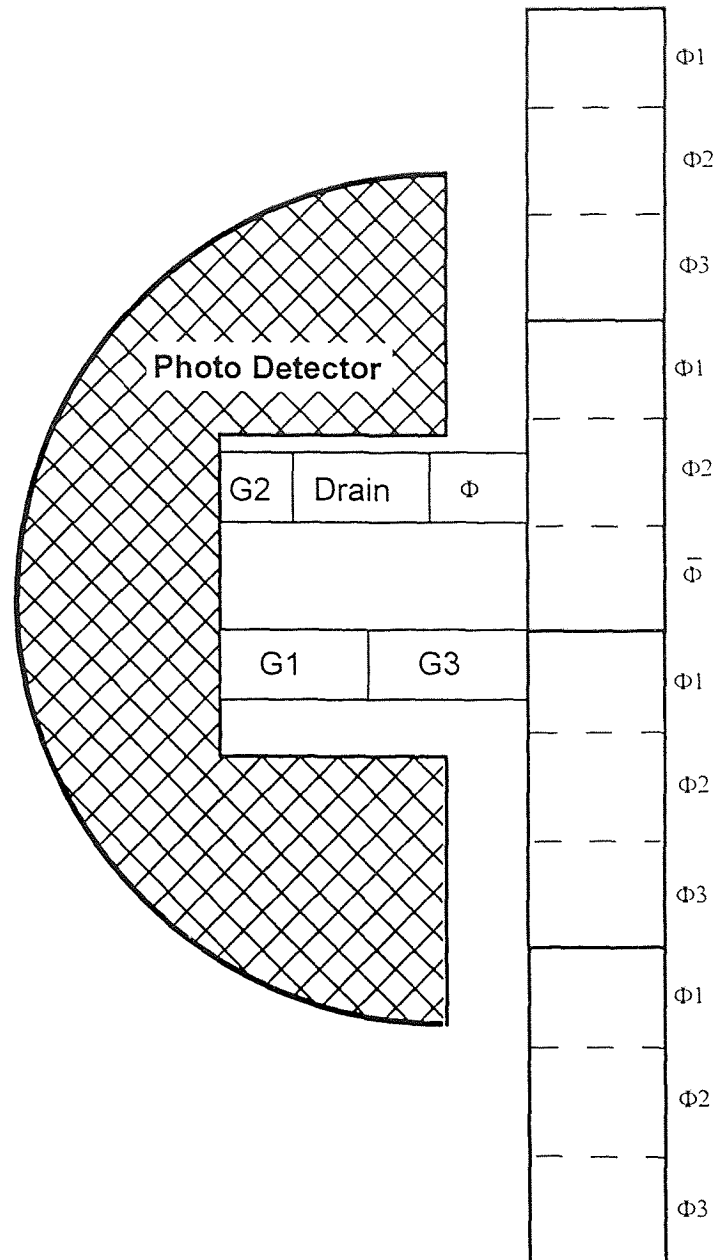**Figure 6.2** *Block diagram of the 2 × 2 macropixel*
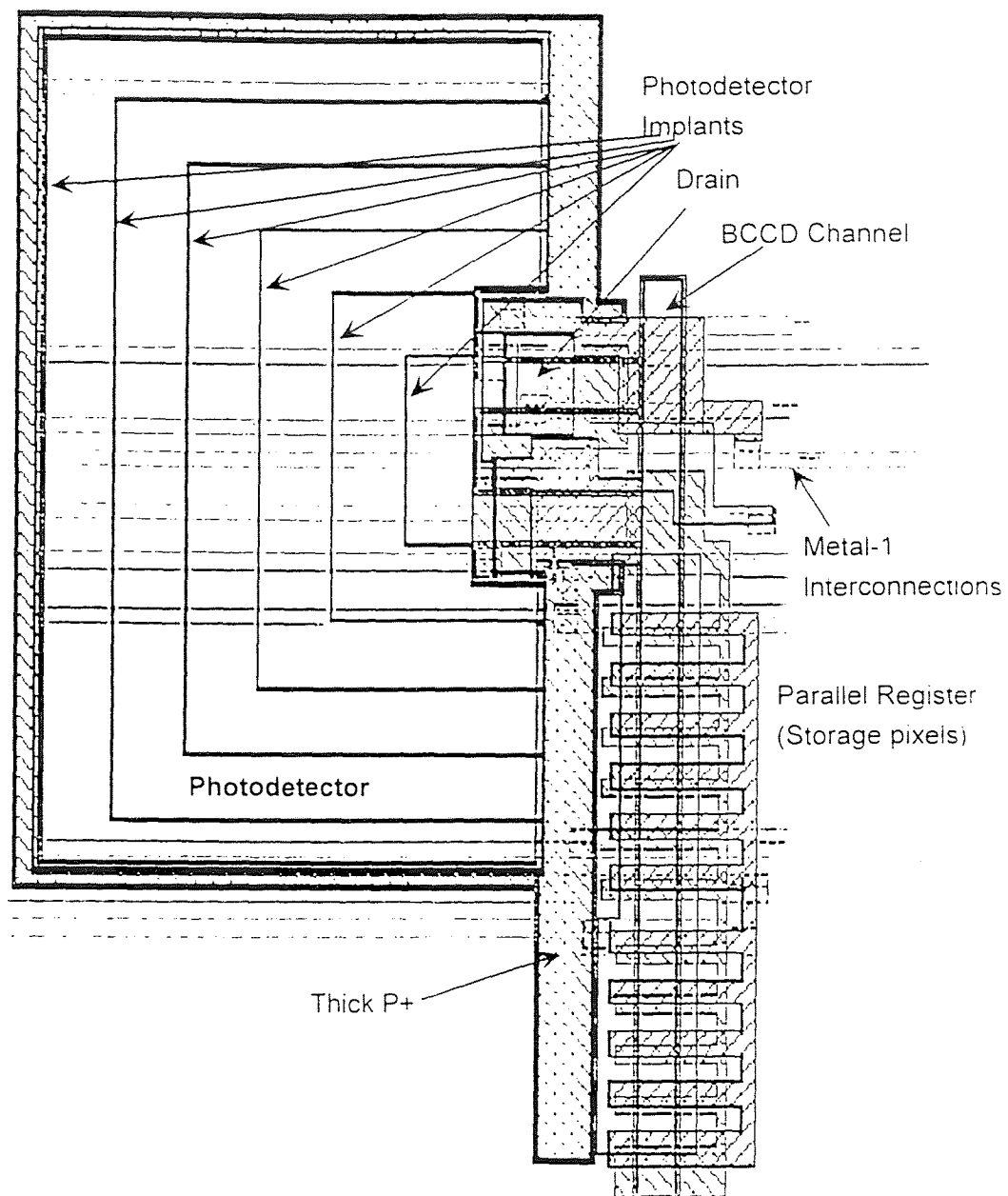
Figure 6.3 *Macropixel architecture*
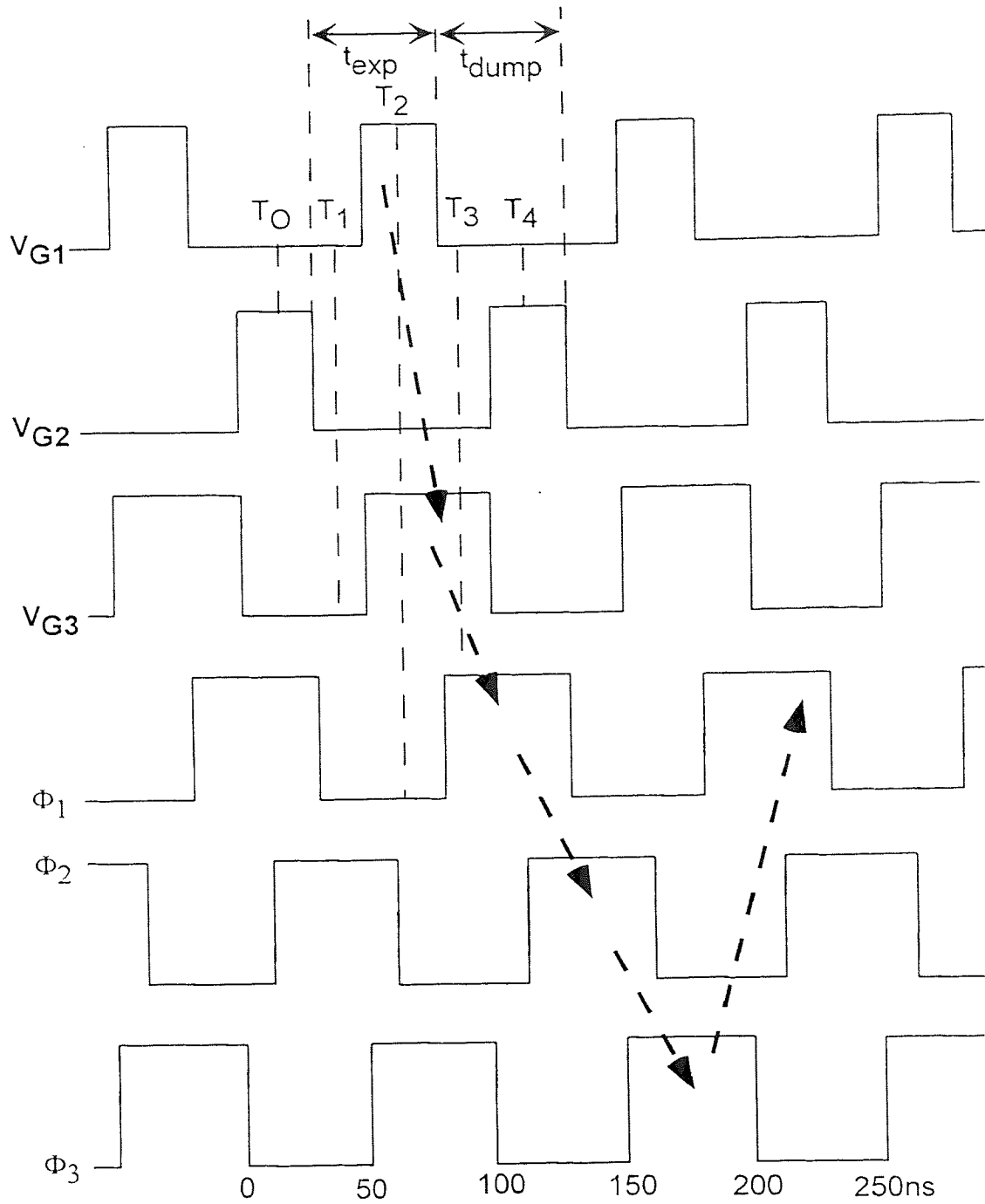
Figure 6.4 *Macropixel layout*

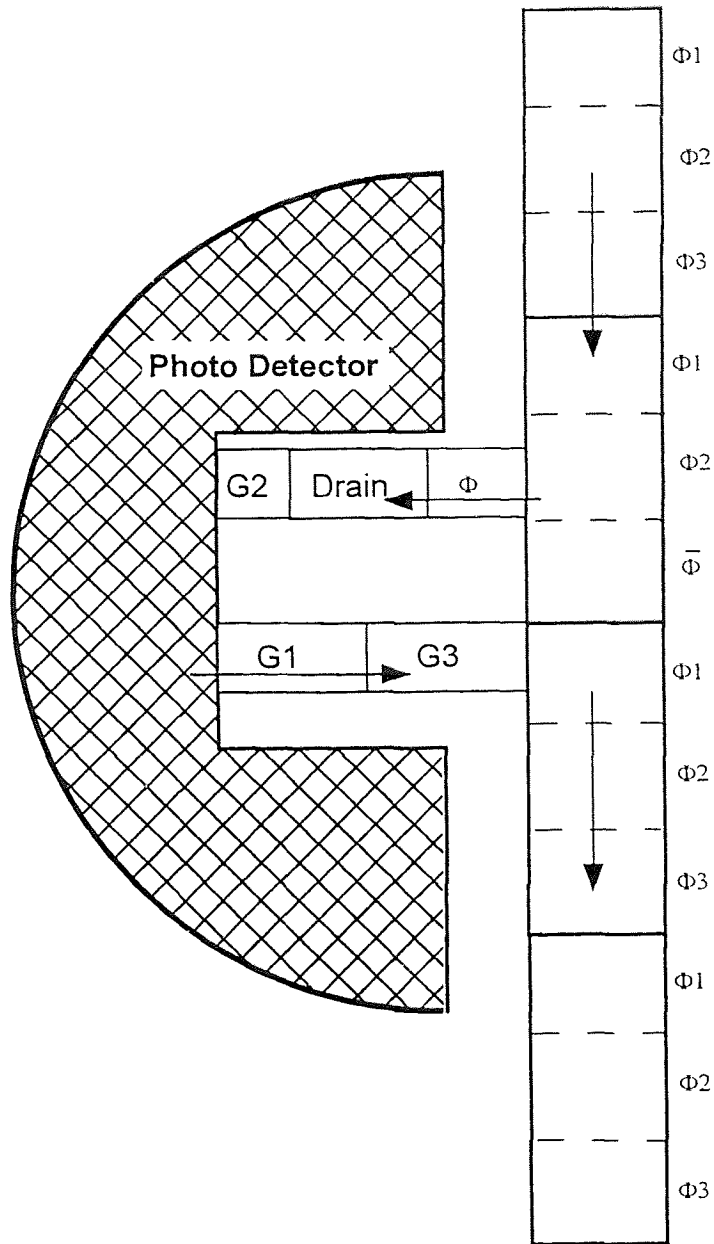**Figure 6.5** *Clock waveforms during image acquisition cycle*
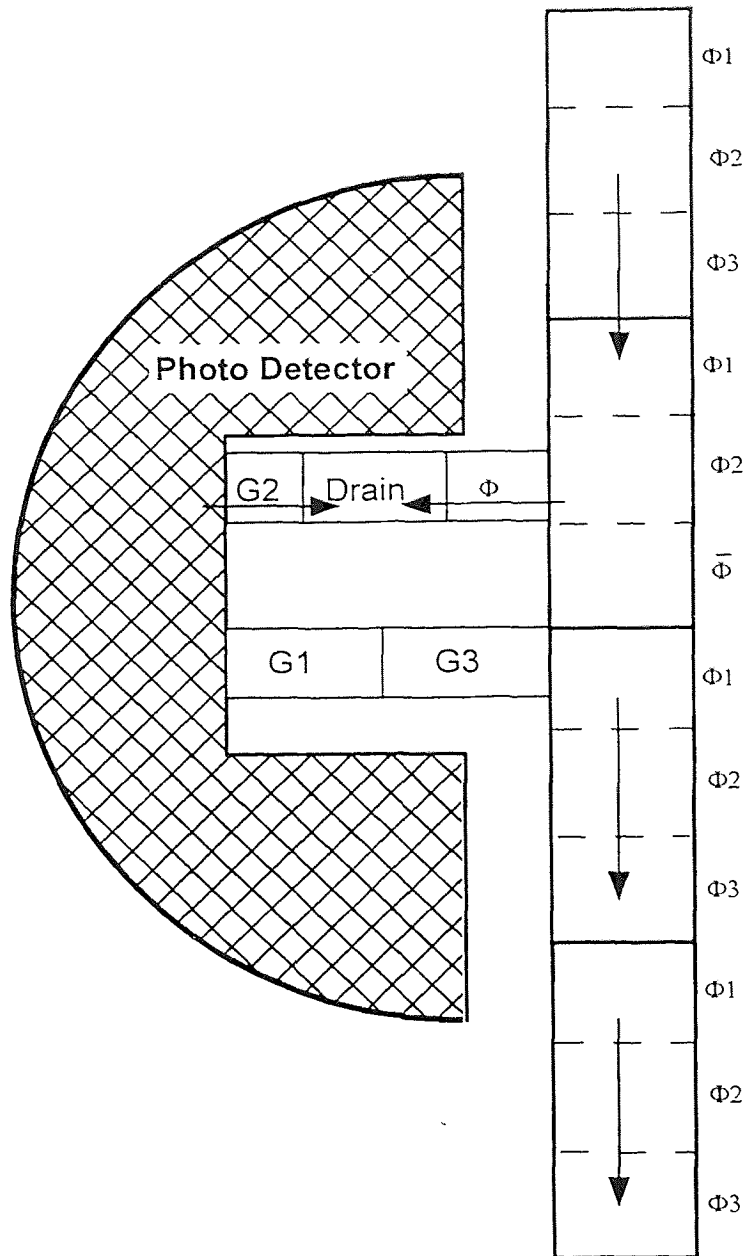
Figure 6.6 *Macropixel operation at t=t2*

Figure 6.7 *Macropixel operation at t=t4*

Figure 6.8 *Macropixel operation during frame readout cycle*

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