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ABSTRACT

PERFORMANCE OPTIMIZATION OF VERY HIGH FRAME RATE CCD BURST-IMAGE SENSORS

by
Zeynep M. Pektas

The primary objective of this work was to demonstrate the feasibility of an image sensor that is capable of capturing images at 10^7 frames per second. Such high frame rate operation is based on storage of a certain (N) number of frames into the BCCD memory registers and readout at a slower rate at the end of the frame collection period. To accommodate an optical frame time of 100ns, a high-speed virtual-gate photodetector with six multiple n-type implants was proposed and a novel design strategy was developed. The feasibility of this design was demonstrated by simulating the entire photodetector readout operation using optimized parameters.

A novel contribution in this research is the application of the channel widening effect in the design which reduced the transit time of carriers in the photodetector by a factor of two. The proposed unique geometry was applied to the last implant region by gradually widening the layout design of this section. Extensive 2D simulations were carried out to account for the 3D effects and results were presented.

Another main objective of this research was the characterization of the 3-phase BCCD memory registers in order to obtain higher charge handling capacity. Both 2D and 3D simulations were performed and compared with the available experimental results. The influence of the major factors affecting the charge handling capacity were investigated in detail. The effect of the reduction in channel length was demonstrated by 2D device simulations. Additionally, 3D device simulations showed that a correction in effective channel width adds linearly to the 2D results. The simulations indicated that a key limiting factor on the charge handling capacity was the overetch of the silicon nitride gate dielectric layer during formation of the polysilicon gate electrodes.

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Zeynep M. Pektas

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- Z. Pektas, G. Yang and W. F. Kosonocky, "New Design and Performance of Multi-Implant Pinned-Buried High-Speed Zero-Lag Large Photodetector." To be submitted to IEEE T-ED.

Dedicated to my mother

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CHAPTER 1

INTRODUCTION

The main objective of this research is the optimization of the performance of a Very High Frame Rate (VHFR) burst-image sensor that is capable of operating at 10^7 frames per second. The captured frames are stored into a buried channel CCD (BCCD) type memory register [1] at this high frame rate during image collection period. The last N detected frames corresponding to the number of the BCCD memory elements are then readout at a slower rate by reconfiguring the BCCD registers into a large full frame type CCD readout.

Applications of such high frame rate burst-image sensors include laser illuminated long range imaging to sense the optical wavefront during the short interval of the laser pulse, analysis of the high speed mechanical processes and also deep space surveillance.

The realization of the VHFR burst-image sensor requires a complicated fabrication process that involves three layers of polysilicon, three layers of metal and a large number of implant steps. Because of the high costs involved in this complex processing and the long time period required to complete the fabrication, an extensive study of the process and device characteristics of the image sensor is essential before any fabrication step is initiated. This research proposes new concepts for the comprehensive study of the design strategies using various process and device simulation tools. The obtained simulation results demonstrate the feasibility of realization for the future generations of the VHFR burst-image sensors with improved features. The described work in this dissertation represents a significant advance towards the realization of a very high frame rate imager.

The first chip designed for the very high frame rate imaging applications is the 360x360-element VHFR burst-image sensor consisting of four quadrants with 180x180-

elements and capable of capturing the last 30 image frames at a frame rate of 8.33×10^5 frames per second. Following this design, the chip was fabricated at David Sarnoff Research Center and the performance was tested at Princeton Scientific Instruments, Inc. The 1D process definition was performed with the available data for the fabrication process obtained from David Sarnoff Research Center and the concept of the high-speed photodetector with multiple n-type implants was introduced [2]. Some of the 2D device simulations for optimization of the BCCD channel characteristics performed by the author were also reported in this initial work.

This dissertation introduces a new concept by applying the effect of channel widening to the last detector implant stage in order to obtain two fold decrease in carrier transit time; i.e. this time has been reduced from 700ns to 350ns. Extensive process and device simulations were carried out to account for the 3D effects of the geometry in the 2D analysis. The application of this unique geometry to the photodetector structure and the presented simulation results are novel contributions to the field of imaging.

The 360x360-element Very High Frame Rate burst-image sensor is followed by the 180x180-element VHFR burst-image sensor which is currently being fabricated at David Sarnoff Research Center. This sensor design was optimized according to the results obtained by 2D device and process simulations in order to obtain higher device yield, higher charge handling capacity and increased fill factor. The problem associated with the 3D edge effects on the 2D simulation results were solved by the 3D process and device simulations for a potential well surrounded by channel-stop region and barrier wells. With the suggested correction of the effective channel width, it is found that the 2D results provide a good estimate of the charge handling capacity. 3D effects add linearly to the 2D results. The limiting factors that affect the charge handling capacity are discussed by comparing the available experimental data with the simulation results obtained by novel strategies developed in this work. One such design strategy for the high-speed photodetector is the application of multiple n-type implants. This strategy is applied to

the next phase of the Very High Frame Rate sensor; the 64x64-element imager that should be capable of capturing images at 10^7 frames per second during a single laser pulse. This strategy involves comprehensive transient analysis for the response of the photodetector readout both to pulse illumination and to continuous illumination. The effect of the dual buried channel implants on the graded potential profile is given and a complete simulation of the photodetector readout with 100ns frame time is demonstrated.

The second chapter gives an overview of CCDs. After a short review of the surface-channel CCD (SCCD) and buried-channel CCD (BCCD) fundamentals, this chapter reviews the recent developments in CCDs.

The third chapter reviews the design of the 360x360-element VHFR burst-image sensor. It also describes the process specification and demonstrates the performance of this image sensor. Also presented in this chapter is the topography adjustment of 2D cut-lines by comparing the SEM photographs of the processed imager chip obtained from David Sarnoff Research Center with the 2D topography simulation results by using ISE-TCAD tools.

The fourth chapter describes the process and device simulations by using Suprem III and Pisces IIB for the characterization of the BCCD channel. Effect of the gate dielectric thickness and reduction of channel length on charge handling capacity are demonstrated. By 1D process simulations, new results are obtained for the pinning gate voltages for both options of the BCCD implant dose and these results are compared with the available experimental data obtained from David Sarnoff Research Center. The difference between the measured and simulated values of the charge handling capacity and the limiting factors are studied in detail in this chapter.

Chapter five describes the design strategy of the photodetector with multiple implants for very high-speed imaging applications. The entire photodetector readout operation by applying the appropriate clock voltages to the adjacent gate electrodes is studied. A virtual-gate photodetector is designed with six multiple n-type implants to

capture images at 10MHz frame rate. New implant levels are suggested for this design.

The effect of channel widening on potential profile is given in chapter six. These results are applied to the layout design of the last implant stage of the photodetector with three implants. Extensive 2D simulations were performed to account for the 3D effects. Simulation results demonstrate an improved carrier transit time in this region.

Chapter seven presents results of the 3D process and device simulations in order to obtain the charge handling capacity of the 360x360-element VHFR imager. The 3D simulation results are consistent with the 2D characterization of the BCCD register which is described in Chapter 4. The 3D analysis of the buried channel allows to include the effect of channel narrowing on the charge handling capacity which is discussed in this chapter. The distribution of charge and potential profile in the 3D structure are also demonstrated in this chapter.

Chapter eight presents the summary and conclusions.

Chapter nine includes suggestions for future research.

CHAPTER 2

CHARGE-COUPLED DEVICES

2.1 Introduction

Charge-coupled devices (CCDs) were first introduced to the world in 1970 by Boyle and Smith [3] in an attempt to produce an electrical analogue of magnetic bubble devices. The original concept of the CCD was a memory device. In order to function as memory there must be a physical quantity which represents a bit of information. In the CCD, a bit of information is represented by a packet of charges (electrons or holes). These charges are stored in the depletion region, the so called *potential well* of a metal insulator semiconductor (MIS) capacitor. Charges are moved about in the CCD circuit by placing the MIS capacitors very close to one another and manipulating the voltages on the gates of the capacitors so as to allow the charge to spill from one capacitor to the next: thus the name charge-coupled device. A charge detection amplifier detects the presence of the charge packet providing a useful voltage to the outside world. Charge packets can be created by injecting charge from a diode adjacent to a CCD gate. Charge can be entered into the device also by optical signal. Absorption of incident photons near the depletion regions charge carriers can be collected and subsequently clocked out of the structure enabling the CCD to act as an image sensor.

Although the original concept of the CCD was a memory device it became immediately clear to a large number of workers in the semiconductor field that the CCD had potential uses that ranged far wider than simple memory applications [4]-[6]. During the past two decades, the primary goal of CCD manufacturers has been to develop CCD sensors to replace tube type sensors (e.g., vidicon tube). The emphasis has been on realizing the CCD's advantages in size, weight, low-power consumption, ultra-low noise, linearity, dynamic range, photometric accuracy, broad spectral response, geometric stability, reliability and durability, while attempting to match tube characteristics in

format, frame rate and cost. The rapid progress of CCDs can be explained by the already existing highly-developed MOS technology. With the present VLSI technology it is possible to realize large chip size with small pixel size so that the CCDs can be made in large area with high resolution.

2.2 Theory and Operation

The fundamental building block of the CCD is the MIS capacitor which can be fabricated on a p-type epitaxial silicon on which an insulator layer on the order of 1000Å is grown, usually composed of silicon dioxide or silicon dioxide and silicon nitride - dual insulating system. This layer is followed by a conductive gate deposition; typically doped poly silicon. The CCD is composed of an array of closely spaced MIS capacitors. There are numerous ways to arrange these capacitors to form a CCD imager. The simplest CCD is a three-phase device [7], the arrangement that Boyle and Smith used for their first CCD. In the three-phase device, a number of gates are arranged in parallel with every third gate connected to the same clock driver. The basic cell in the CCD, which corresponds to one pixel, consists of a triplet of these gates, each separately connected to phase 1, 2 and 3 clocks. If phase 1 is biased high, a depletion region forms and represents a region of higher electrostatic potential relative to the lower biased neighboring gates. It is under this phase where signal electrons would collect in a pixel. The potential well under the gates of phase 1 where charge collects is referred to as *the charge collecting well* whereas the neighboring regions are referred to as *the barrier wells* since they confine charge for the pixel on either side of the charge collecting well.

A CCD area array imager can be thought of as many shift registers composed of many pixel elements. The image-forming section of the CCD is covered with closely spaced vertical registers or columns. The columns are separated by implanted potential barriers called *channel-stops* which prevent the spread of the signal charge from one column into the other. Channel-stops are usually highly doped boron p-regions which are

held at ground potential. Photoelectrons generated in these regions migrate and diffuse to the nearest charge collecting well of a pixel. The vertical columns are subdivided into pixels in the manner described above, by a series of conductive parallel gates that run perpendicular to the channel-stops. A picture is read out of a CCD by a succession of shifts through the vertical registers. At each shift of the vertical section the last line of pixels transfers into a horizontal register. This register is also a CCD channel, oriented at right angles to the vertical channels situated at the top and/or bottom of the device. Then, before the next line is shifted, the charge in the horizontal register is transferred to an on-chip output amplifier where charge for each pixel is converted to an output voltage. The sensitivity of the amplifier is expressed in volts per electron; approximately 1μV/electron to 4μV/electron is exhibited for most scientific CCDs. The device is then serially readout line by line, representing the scene of photons incident on the device.

Charge storage and charge transfer are the two processes that are fundamental to CCD operation. Charge transfer in the CCD structure can be accomplished in an almost perfect way, without any noticeable deterioration of the charge content. In order to store the charge packet there are two different types of CCD structures, which are the surface channel CCD (SCCD) and the buried channel CCD (BCCD). They can be further divided into the two-, three-, and four-phase CCDs [8]-[11].

2.3 Surface Channel CCD (SCCD)

When a positive voltage is applied to the gate, majority carriers (holes) in the silicon are repelled from the region beneath the silicon/silicon dioxide interface leaving a depletion region. The potential variation within the depleted silicon is such that a potential well for electrons forms at the surface of silicon. In the absence of an inversion layer the depletion region extends much further into the bulk of the semiconductor (deep depletion). If minority carriers are subsequently made available, the depletion layer will shrink and the surface potential will fall as the inversion layer charge increases.

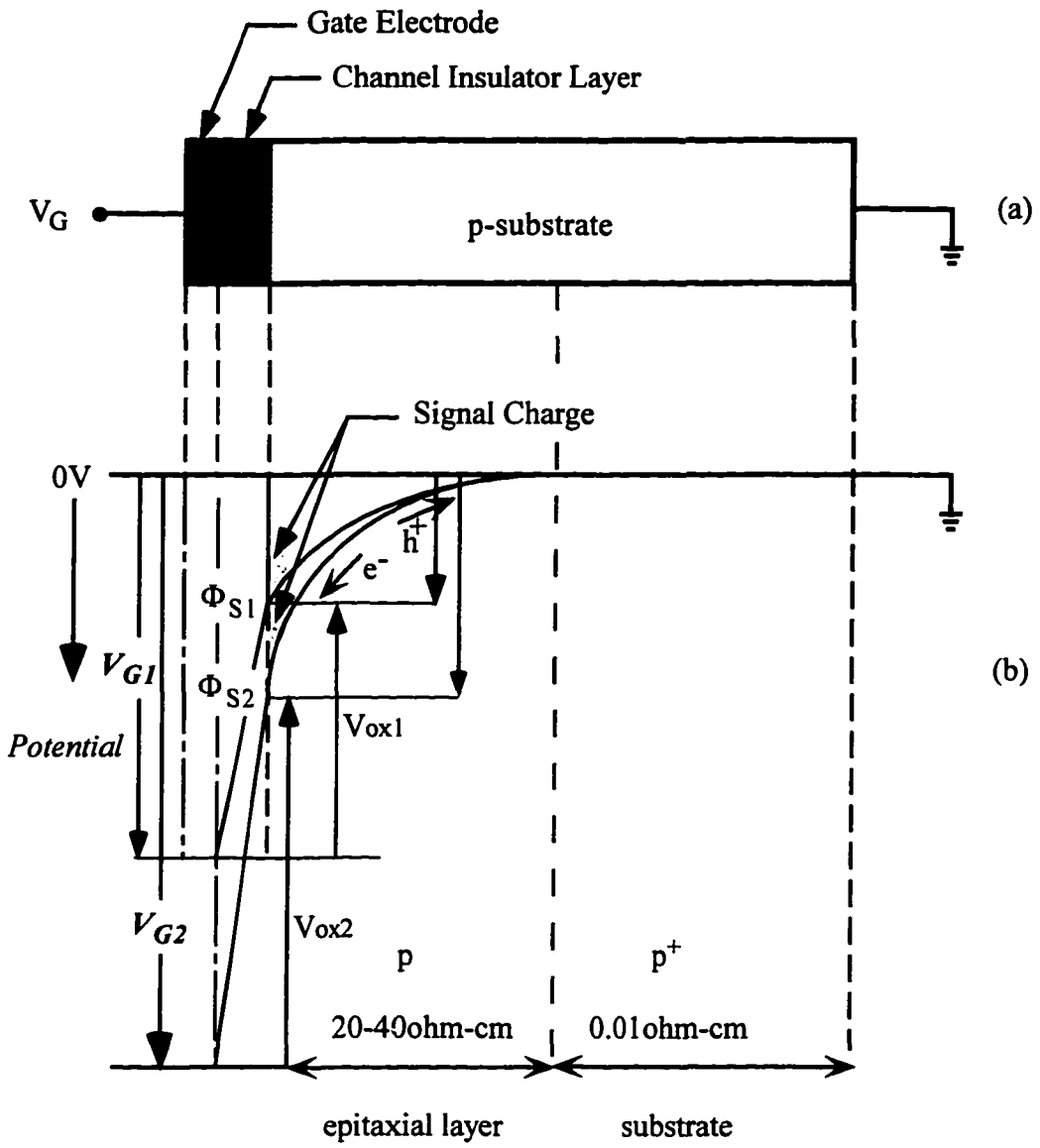


Figure 2.1 *(a) Cross-sectional view of the surface channel CCD structure. (b) Potential diagram of SCCD illustrating the charge storage mechanism with applied positive gate voltages V_{G1} and V_{G2}.*

The figure above illustrates the potential profiles of a surface channel device with p-type substrate for two different voltages V_{G1} and V_{G2} applied to the gate electrode. Φ_{S1} and Φ_{S2} are the corresponding surface potentials at the silicon/insulator interface. V_{ox1} and V_{ox2} are the voltage drops across the insulator layer, respectively.

Charge storage occurs in a CCD by sequentially driving the MOS capacitors into deep depletion through applying digital pulses to the gates. When the CCD elements are in deep depletion, free electrons will be generated by the process of thermal generation of minority carriers, behaving in a non-equilibrium mode. Free electrons will be also supplied to the MOS capacitors in the form of charge packet, however this charge signal can be stored in the CCD pixel elements only for a time that is much shorter than the time needed to build-up the equilibrium inversion layer by thermal generation. Otherwise, the thermally generated minority carriers would eventually saturate the charge handling capacity of the CCD pixel elements. Under operation in thermal non-equilibrium, an expression for the surface potential Φ_S as function of the charge density Q_n in deep depletion can be obtained as follows:

$$V_G = -V_{ox} + \Phi_S . \tag{2.1}$$

From the charge neutrality in the device:

$$Q_G + Q_n + Q_D = 0 . \tag{2.2}$$

In the equation above Q_G , Q_n and Q_D are the charge densities per unit area on the gate, in the inversion layer and the depletion layer. By the depletion approximation

$$Q_D = -qN_A x_d = -\sqrt{2qN_A \varepsilon_S \Phi_S} , \tag{2.3}$$

where q is the magnitude of the electronic charge, N_A is the acceptor atom doping concentration, x_d is the depletion layer width and ε_S is the permittivity of silicon. Noting that $V_{ox} = -Q_G/C_{ox}$ where C_{ox} is the capacitance per unit area of the oxide, we can obtain the following equation:

$$V_G = \frac{-Q_n + (2qN_A \varepsilon_S \Phi_S)^{1/2}}{C_{ox}} + \Phi_S . \tag{2.4}$$

This can be rearranged to yield the following expression of the surface potential Φ_S:

$$\Phi_S = V_G + V_o + \frac{Q_n}{C_{ox}} - \left[2\left(V_G + \frac{Q_n}{C_{ox}}\right)V_o + V_o^2\right]^{1/2}, \qquad (2.5)$$

where V_o is a constant given by $(qN_A\varepsilon_S)/C_{ox}^2$. Variation of Φ_S with V_G is almost linear because for lightly doped substrates and thin oxides, V_o is quite small compared to the applied gate voltage. Therefore, Equation (2.5) can, to a good approximation, be written as

$$\Phi_S = V_G + \frac{Q_n}{C_{ox}}. \qquad (2.6)$$

Since Q_n is negative for p-type substrate, with increasing signal charge in the inversion layer the magnitude of Φ_S decreases. In other words, Φ_S becomes maximum for an empty potential well. Charge handling capacity of a surface channel device can be obtained by rearranging Equation (2.4) and including the active electrode area A:

$$-Q_n = AC_{ox}(V_G - \Phi_S) - A\sqrt{2qN_A\varepsilon_S\Phi_S}, \qquad (2.7)$$

where Q_n is in coulomb in Equation (2.7). The thickness of the oxide is the most significant parameter for a surface channel device. It should be noted that the charge handling capacity of a surface channel device decreases as the channel insulator layer thickness increases for a given gate bias.

The above discussion described a surface channel CCD (SCCD), since charge packets are stored and transferred along the surface of the semiconductor (i.e., at the Si/SiO_2 interface). A major problem exists with surface channel CCDs because charge can become trapped in interface traps found at the surface severely limiting transfer efficiency performance. These are states found near the silicon / silicon dioxide interface which rapidly acquire charge as a potential well fills, but which are reluctant to release their charge when the well subsequently empties. The first surface channel CCDs fabricated exhibited charge transfer efficiencies of 98% per phase transfer, much too low

for scientific work. Although different attempts have been made to passivate and reduce the density of interface states through various process schemes, it became clear that surface channel operation could not be used especially when small charge packets are transferred. In addition, large area arrays to be developed requires thousands of transfers demanding ultra-high performance; charge transfer efficiencies that surface channel sensors could never achieve. To avoid the surface state trapping and significantly improve charge transfer efficiency, the *buried channel CCD (BCCD)* [12]-[15] was proposed in 1972, only two years after the invention of the SCCD.

2.4 Buried Channel CCD (BCCD)

In a buried channel device charge packets are confined to a channel that lies beneath the surface buried in the silicon. In contrast to surface channel operation, the charge transfer efficiency for buried channel CCDs is amazingly high. Efficiencies of greater than 99.999% per pixel transfer are routinely achieved for buried channel CCDs.

Figure 2.2 represents a cross-sectional view of a BCCD showing a region of n-type material (typically a phosphorus implant) forming the buried channel. In comparison to a surface channel structure, the extra n-doping reshapes the potential well so that electrons are forced to collect below the silicon/insulator interface. The photoelectrons move to the highest potential seen a region which is now situated between the silicon/insulator interface and p-n junction. Photogenerated holes leave the silicon through the substrate contact which is referenced to ground potential.

The charge carrying capability of BCCDs is significantly less than that of SCCDs because in a buried channel device the signal charge resides further away from the gate electrode and therefore, the effective gate-channel capacitance of a buried channel device is smaller than that of a surface channel device. The capacitor equivalent circuits for a BCCD and a SCCD are illustrated in Figure 2.3.

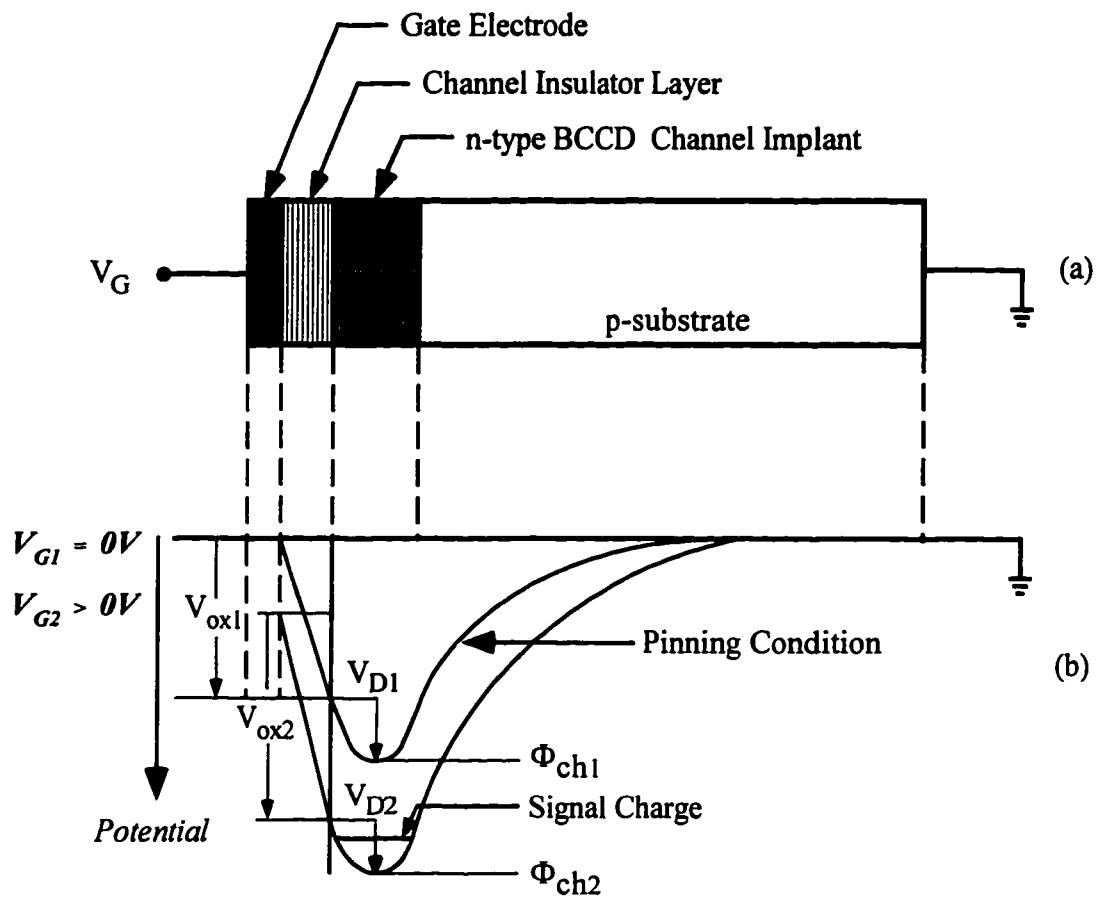


Figure 2.2 *(a) Cross-sectional view of the buried channel CCD structure. (b) Potential diagram of BCCD illustrating the charge storage mechanism with applied gate voltages V_{G1} = 0V and V_{G2} > 0V.*

Defining the voltage dropped across the depletion layer x_{d1} by V_{D1}, the maximum of the channel potential Φ_{ch} can be given by

$$\Phi_{ch} = V_G + V_{ox} + V_{D1}. \tag{2.8}$$

Assuming an empty potential well and using the charge neutrality, the following equation is obtained where Q_{D1} is the charge per unit area in the depletion layer x_{d1}.

$$Q_G + Q_{D1} = 0. \tag{2.9}$$

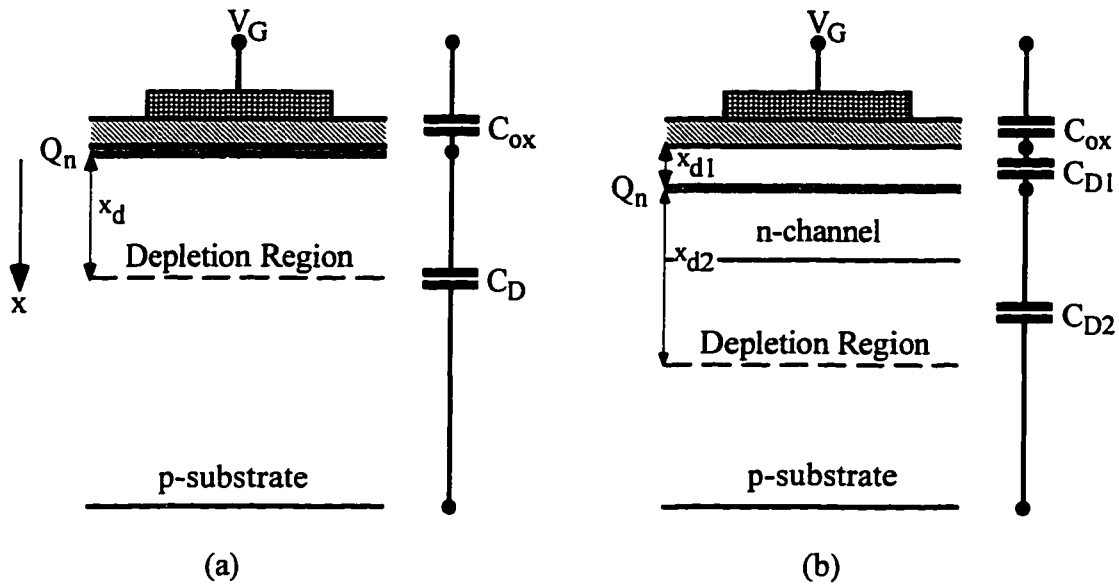


Figure 2.3 *Capacitor equivalent circuits of (a) SCCD, (b) BCCD.*

From depletion-approximation theory V_{ox} and V_{D1} are related to x_{d1} by Equations (2.10) and (2.11) where N_D is the buried channel doping concentration.

$$V_{ox} = \frac{Q_{D1}}{C_{ox}} = \frac{qN_D x_{d1}}{C_{ox}}, \tag{2.10}$$

$$V_{D1} = \frac{qN_D x_{d1}^2}{2\varepsilon_S}. \tag{2.11}$$

Equation (2.8) for the channel potential Φ_{ch} can be rewritten as:

$$\Phi_{ch} = V_G + \frac{qN_D x_{d1}}{C_{ox}} + \frac{qN_D x_{d1}^2}{2\varepsilon_S}. \tag{2.12}$$

For a physical structure, it will be observed that the channel potential varies approximately linearly with the gate voltage. With increasing gate oxide thickness the channel potential Φ_{ch} increases so that deeper potential wells are created for a given gate bias. Increasing the n-channel doping concentration or the n-layer thickness also results in greater values of Φ_{ch}.

The potential well of a buried channel structure changes shape when signal electrons fill the well. Three important changes in the potential profile occur. First, the potential maximum (or channel potential) of the charge collecting well decreases as it approaches the potential of the adjacent barrier wells. Second, the potential maximum of the charge collecting well shifts towards the surface. Third, the potential well flattens and broadens as charge is collected. To analyze the charge handling capacity of a BCCD is more difficult than the analysis of a SCCD and a simple equation comparable to Equation (2.7) relating the charge packet size to the gate voltage for a given structure is not available. For a uniformly doped channel, the charge packet size is given by

$$Q_n = -qN_D x_z A\,, \tag{2.13}$$

where x_z is the depth of the neutral channel region carrying the charge packet. For non-uniform doping profile, a numerical solution of Poisson's equation must be used to find the potential distribution through the device. In general, for non-uniform doping, the doping concentration will decrease from the silicon surface through the channel toward the substrate. Therefore, as the charge packet size is increased the charge distribution spreads mainly toward the silicon surface. To produce a BCCD with maximum charge carrying capability, a steeply graded doping profile near the silicon surface is required in order to prevent the charge coming into contact with the surface, in other words to avoid the potential of the charge collecting well becoming equal its surface potential. If the surface and the channel potentials of the charge collecting well become equal, the BCCD operates completely as a surface channel device.

Another mechanism of charge spreading is when the potential of the charge collecting well and the adjacent barrier wells become equivalent. In this case, charge will spill over the barrier well into neighboring pixels. This type of charge spreading among pixels is referred to as *blooming*. The full well capacity of a pixel is defined when either

blooming or surface channel operation is reached depending on the positive bias to the charge collecting gate.

From the discussion above optimum full well capacity for a multi-phase CCD is achieved when blooming and surface full well occur simultaneously. That is, when the surface potential of the charge collecting well equals the potential maximum of the neighboring barrier well. It should be noted that the surface potential of the charge collecting well is initially greater than the channel potential of the barrier well when the collecting well is empty. As the collecting well fills, the surface potential decreases approaching the channel potential of the barrier well. Optimum full well occurs when the two potentials become equivalent.

New CCD design and process developments are likely in the near future to drive the full well capacity (charge handling capacity) even higher. It is known that increasing the phosphorus doping of the signal channel increases the charge handling capacity. However, there is a limit to how much doping can be employed because the electric fields generated internal to the device also increase. If the electric fields are too strong breakdown will result leading to excessive dark current generation. The fields are strongest in the region where the channel-stops and signal channel meet.

Inversion and Pinning

A particularly important condition develops when a controlling gate voltage is decreased. The surface potential keeps decreasing when the gate voltage is made further negative until the n-channel at the Si/SiO_2 interface inverts, that means, holes from the channel-stops are attracted and collected at the interface. By reducing the gate voltage further, more holes are accumulated at the interface that maintain the surface potential at the substrate potential (0V). This state is called *pinning* [16]. Usually, the potential wells acting as barrier gates are in pinning condition. The thin layer of holes at the surface is

conductive and shields the silicon layer from the gate voltage fixing the potential well shape; when inverted any change in gate bias goes directly across the gate insulator.

2.5 Charge Transfer

Three primary mechanisms [17], [18] are responsible for charge transfer in a CCD: self-induced drift, thermal diffusion and fringing field effect. The relative importance of each of these is dependent on the charge packet size. Both thermal diffusion and fringing fields are important for transferring small amounts of charge whereas self-induced drift caused by mutual electrostatic repulsion of the carriers within a packet dominates charge transfer for large packets. From the analytical point of view the charge transport of the carriers through a CCD channel can be described by current density and continuity equations. The three components of the current density are J_d, J_s and J_f corresponding to the thermal diffusion, self-induced drift and fringing field effect respectively.

$$J(y,t) = J_d + J_s + J_f. \tag{2.14}$$

These three components are given by the classical expressions for diffusion current and drift current generated by an electric field:

$$J_d = qD_n \frac{\partial Q_n(y,t)}{\partial y}, \tag{2.15}$$

$$J_s = Q_n \mu_n E_s, \tag{2.16}$$

$$J_f = Q_n \mu_n E_f. \tag{2.17}$$

D_n is the diffusion constant of electrons, $Q_n(y,t)$ is the charge distribution as function of place and time, y is the direction along the silicon surface in which the charge signal moves, μ_n is the electron mobility, E_s is the self-induced electric field and E_f is the

fringing field. Charge carriers which are transferred from one position to another define the current between these two positions. The continuity equation connects the amount of charge to be transferred with the current density [10]:

$$\frac{\partial Q_n(y,t)}{\partial t} = \frac{\partial J(y,t)}{\partial y}. \tag{2.18}$$

If the charge transport is fast enough, the rate of total amount of charge carrier generation and recombination is negligible relative to the total amount of charge. Equation (2.18) is only valid if no extra charge is added or subtracted from the original charge packet or the recombination and generation of the carriers is not considered.

Thermal Diffusion

Even in the absence of any electric field, a charge packet will redistribute its local gradient toward an equilibrium. This mechanism results in an exponential decay of the remaining charge with the time constant τ_{th} under the transferring electrode. For small amounts of signal charge this process is governed by thermal diffusion.

$$Q_n(t) = \frac{8}{\pi^2} \cdot Q_n(0) \cdot e^{-\frac{\pi^2 D_n}{4L^2} t}, \tag{2.19}$$

$$\tau_{th} = \frac{4L^2}{\pi^2 D_n}. \tag{2.20}$$

In this expression L represents the length of a single CCD gate, which is in the direction of charge transport. The time constant of the process is inversely proportional to the diffusion constant D_n and proportional to L^2.

Self-induced Drift

For reasonably large charge packets, however, the transfer is dominated by the self-induced drift produced by electrostatic repulsion of the carriers. Due to the presence of

the self-induced drift, the total diffusion of charge carriers during the transport becomes much faster compared to the case of thermal diffusion only. The drift current is important only during the initial period of the charge transfer for about 99% of the charge signal. The transfer efficiency of the transport is only high, if enough time is available to allow the thermal diffusion to transport also the latest part of the charge packet.

Fringing Fields

Fringing fields from adjacent electrodes produce electrical fields with longitudinal components. The presence of these fields speeds up the transfer of the last residues of charge and is thus extremely important for devices in high speed applications. The fringing field in the longitudinal direction is minimum in the center of the transferring electrode and increases almost linearly from the edges to the center of the middle transfer electrode (Figure 2.4).

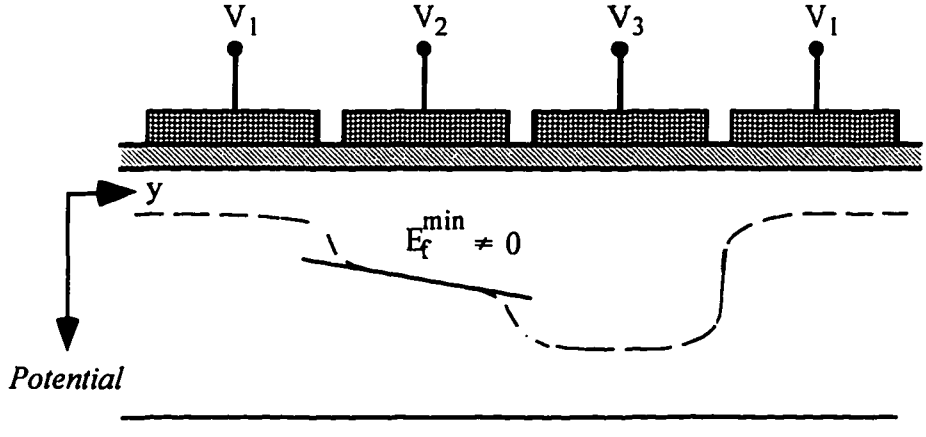


Figure 2.4 *Potential profile with longitudinal fringing fields E_f*

The minimum fringing field can be approximated by

$$E_f^{min} = 6.5\frac{t_{ox}}{L^2}\Delta V\left[\frac{5\cdot x_d / L}{(5\cdot x_d / L)+1}\right]^4, \qquad (2.21)$$

where ΔV is the potential difference between adjacent electrodes and x_d is the thickness of the depletion region under the center electrode. A smaller electrode length L gives a much higher fringing field and a significant improvement in transfer efficiency. Other parameters to increase the fringing fields are the oxide thickness t_{ox} and the potential difference ΔV applied to the adjacent gates. Decreasing the substrate doping level also increases the fringing fields. By proper consideration of these factors and allowing enough time that is required to transfer the charge in the packet from one well to another, the losses due to free charge transfer can always be kept small compared to other sources of transfer inefficiency.

Trapping Effects

Two important factors that influence the charge transfer efficiency are design induced traps and process induced traps. The design induced trap is usually the result of a design feature that results in a small potential trap or barrier. This type of trap is typically characterized by a region in the device where the signal channel narrows and charge is forced to transfer from a wider region of the channel into or through a constriction. This, in turn, produces a potential barrier in the channel where small quantities of charge can be trapped.

The second type of defect which can severely degrade the charge transfer efficiency performance is the process induced traps. These traps can be classified into two categories: uniformly distributed traps and localized traps (randomly distributed traps). Uniformly distributed traps cause a global effect on charge transfer efficiency. These effects, often due to the polysilicon edge lifting, and boron lateral diffusion, are relatively easy to identify because a fixed amount of charge is deferred for each pixel transfer. The most serious charge transfer efficiency problem for the CCD is associated with the localized trap. The behavior of a localized trap is similar to the design induced trap as discussed above. The localized trap is usually confined to a single pixel. The traps are

capable of capturing a wide range of charge and the filling and emptying of these traps affect the operation of the CCD. Although the presence of a trap in a vertical column is undesirable, its occurrence in the horizontal register can make the CCD useless.

2.6 Dark Current

There are several types of intrinsic noise sources. One important source generated internally to the CCD is dark current. Dark current is due to thermally generated electrons within the device and represents an inherent limitation on the noise performance due to the *dark shot noise* that is produced. Thermally generated charge is governed by Poisson statistics as *photon shot noise*.

For CCD imagers there are three main sources of dark current within the device. These are (1) thermal generation and diffusion in the natural bulk, (2) thermal generation in the depletion region and (3) thermal generation due to surface states at the Si/SiO_2 interface. Of these sources, the contribution from surface states is the dominant factor for CCD's operation. *Surface dark current* [19]-[22] is between two to three orders of magnitude greater than the dark current generated in the bulk of the structure. Dark current generation at the Si/SiO_2 interface depends on two factors, namely the density of the interface states and the density of free carriers that populate the interface. The surface under each gate must be depleted during at least part of the clocking sequence. The generation of free carriers at a depleted surface is a two-step process. Electrons that thermally move from the valence band to an interface state and then to the conduction band will produce an electron-hole pair that will be collected in the potential well. The presence of free carriers will fill the interface states. However, when the surface is inverted and driven into pinning condition, holes will accumulate at the Si/SiO_2 interface so that the free electrons will rapidly recombine with the holes eliminating the surface dark current. The simplest system would consist of a single phase to derive the device. An important approach to a single phase is the development of the virtual-phase CCD

[23]. *Multi pinned-phase (MPP) CCDs* [24], [25] can be biased into a mode referred to as partially inverted. For a 3-phase CCD partial inversion is accomplished by biasing barrier wells strongly negative so that inversion occurs at the Si/SiO_2 interface whereas the collecting well is biased to a positive voltage. The partial inversion reduces dark current generation significantly.

All Gates Pinning (AGP) CCDs [26]-[28] can operate totally inverted to achieve ultra-low dark current generation rates. AGP CCDs are processed slightly different than conventional devices in order to provide a collecting potential well adjacent to barrier wells while all of them are in pinning. In order to provide a potential difference an additional implant is necessary. It should be noted that dark current rates achieved by AGP CCDs is significantly lower than the dark current rates achieved by partially inverted operation. On the other hand, the charge handling capacity of a AGP CCD is two to three times lower compared to when the device is operated partially inverted.

CHAPTER 3

360 x 360-ELEMENT VERY HIGH FRAME RATE BURST-IMAGE SENSOR

3.1 General Description

A 360 x 360 element Very High Frame Rate (VHFR) burst image sensor [1], [29] was developed for rapid mechanical motion and transient photometric phenomena. The VHFR imager captures images at the maximum frame rate of up to 10^6 frames/second. This is accomplished by continuously storing the last 30 image frames at the pixel locations. The general characteristics of this imager are summarized in Table 3.1

The imager consists of 360 x 360 elements, also called macropixels which are designed in the form of four quadrants. The chip size is 2cm x 2cm. There are 180 x 180 macropixels in each quadrant with a CCD readout register and separate output amplifier. Each macropixel occupies 50μm x 50μm and consists of a 337μm^2 photodetector representing a fill factor of 13.5% and a 3-phase 30-stage series-parallel type buried channel CCD (BCCD) register for continuously storing the last 30 detected image frames. The detected and stored charge is then readout at a slower rate, simultaneously from each quadrant. This new chip architecture reduces the transfer losses by reducing the number of transfers and enhances the yield of usable device. The resulting maximum number of transfers is comparable to the largest state-of-the art CCD image sensors.

3.2 Chip Architecture and Operation

The general architecture of the VHFR imager is shown in Figure 3.1 for an array of 2 x 2 macropixels. Each macropixel consists of a photodetector, a photodetector charge read-out structure, a serial-parallel (SP) register and a parallel (P) register. The photodetector charge readout structure has a charge collecting well under gate G_1, a blooming barrier gate G_2 , a drain D and the gate G_3 separating the charge collecting well from 5-stage SP register. The shape of the CCD pixel storage is different for upper and lower quadrants in

order to assure that the photodetectors have the same spacing as well as the symmetry of the signal storage sequence in the upper and lower quadrants.

Table 3.1 Characteristics of the VHFR burst image sensor.

Chip Size	2cm x 2cm
Number of Pixels	360 x 360 (4 quadrants of 180 x 180)
Pixel size	50μm x 50μm
Photodetector size	337μm^2
Fill Factor	13.5%
Number of Frame-Storage CCD Elements per Pixel	30
Frame Transfer CCD Type Readout Format	4 x 900 x 1080 3-phase CCD elements
Minimum Design Rule	1.5μm
Size of the Smallest CCD Storage Element	1.5μm x 3.0μm
Measured Saturation Signal Q_{max} (electrons/pixel)	11000
Readout Noise (rms electrons/pixel)	9
Dynamic Range	1200:1
Measured Maximum Frame Rate (frames/second)	5x10^5 for equal frame time of 2.0μs or 8.33x10^5 with 2.0μs frame time for the 1st frame and 1.0μs for the next 4 frames

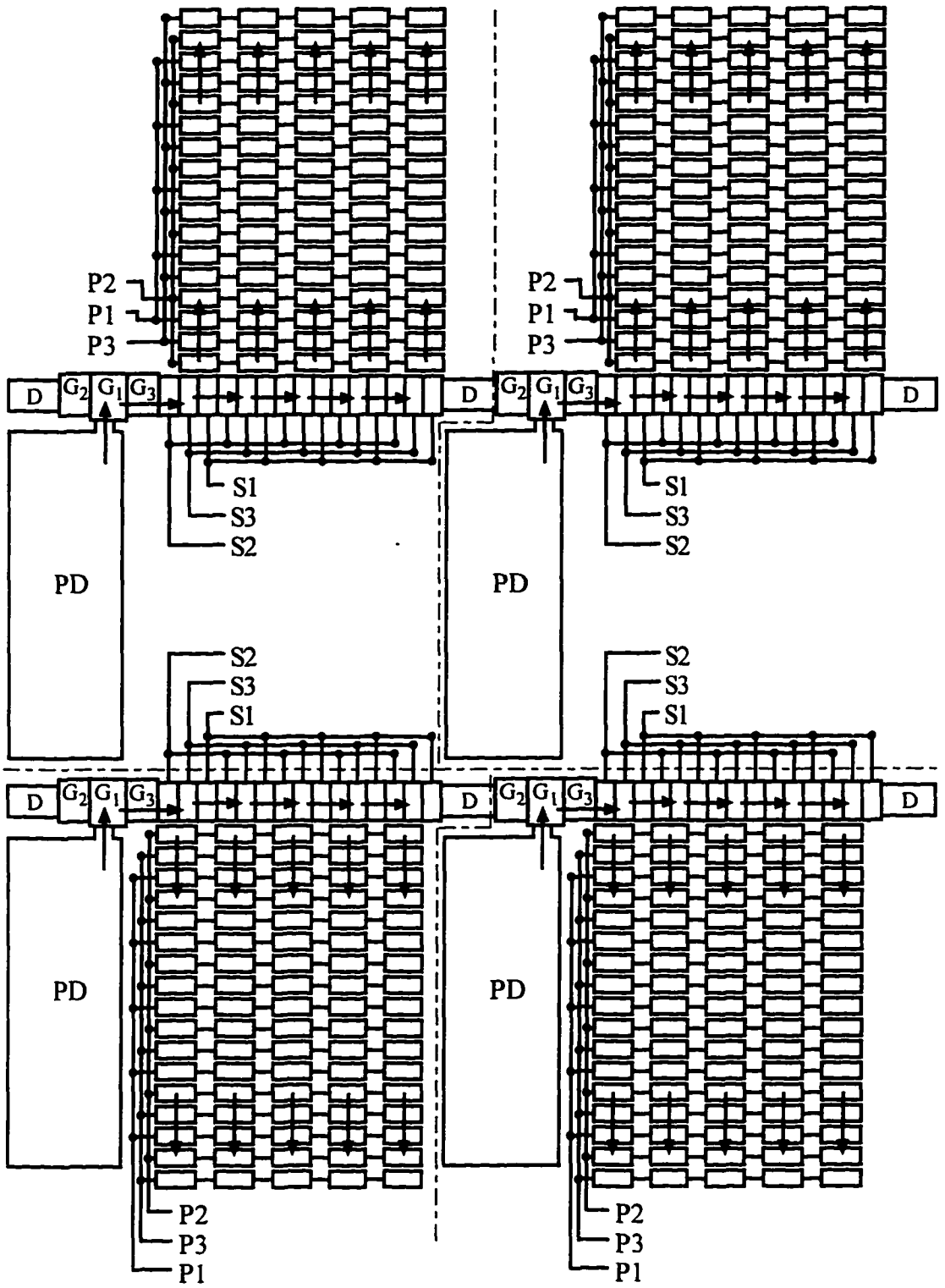
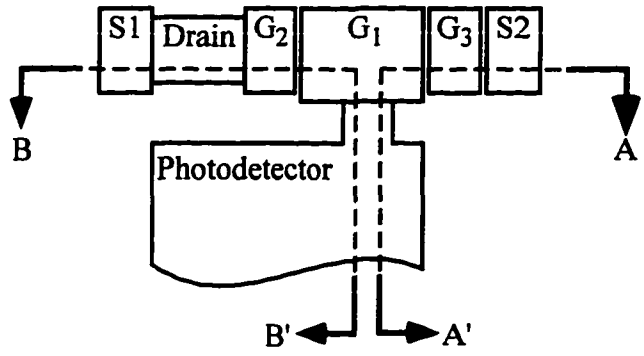


Figure 3.1 *Schematic diagram of 2x2 macropixels in the center of the VHFR burst-image sensor.*

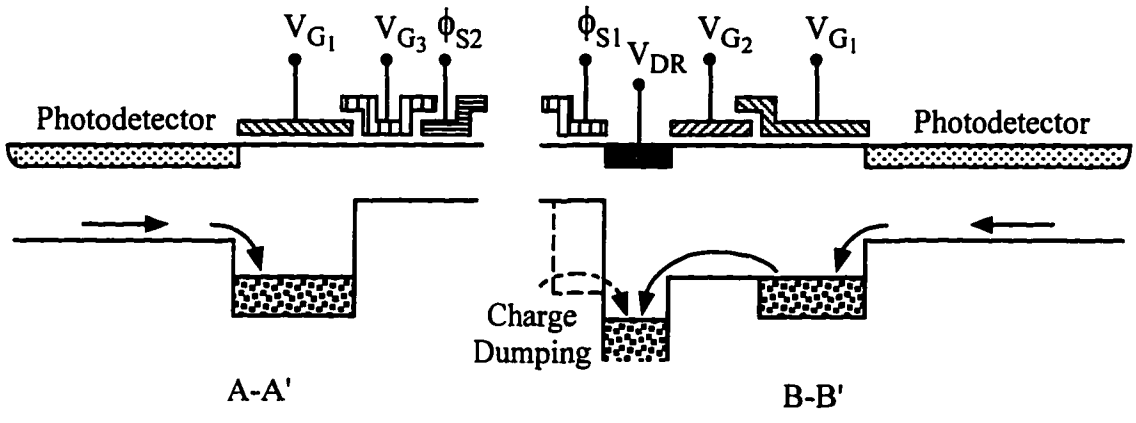
Therefore, the charge storage and readout follows exactly the same pattern for both upper and lower parts. The drain D is used for blooming control during optical (frame) integration time and for dumping the excess charge signals (excess frames) from the serial-parallel SP register. The 5-stage serial-parallel SP register coupled to a 5 x 5-stage parallel P register forms a 30-frame CCD storage at each pixel location. The chip is designed with 1.5μm design rules and 1.5μm x 3.0μm minimum size of BCCD storage elements.

The construction and operation of the photodetector readout is illustrated in Figure 3.2, showing the top view of the photodetector read-out structure in (a), potential profiles during the frame integration time in (b), and the potential profiles during the readout from the charge collecting well in (c). During the charge integration time the potential well under the charge collecting gate G_1 acts as a sink for photodetector charge. Blooming control in the presence of a large optical overload is achieved by controlling gate G_2 in conjunction with blooming drain D. The readout of the collected charge signal is obtained by a periodical transfer of the charge from gate G_1 to gate G_3. In the mean time, the channel potential of G_2 forms a barrier to prevent the charge from flowing into the blooming drain D.

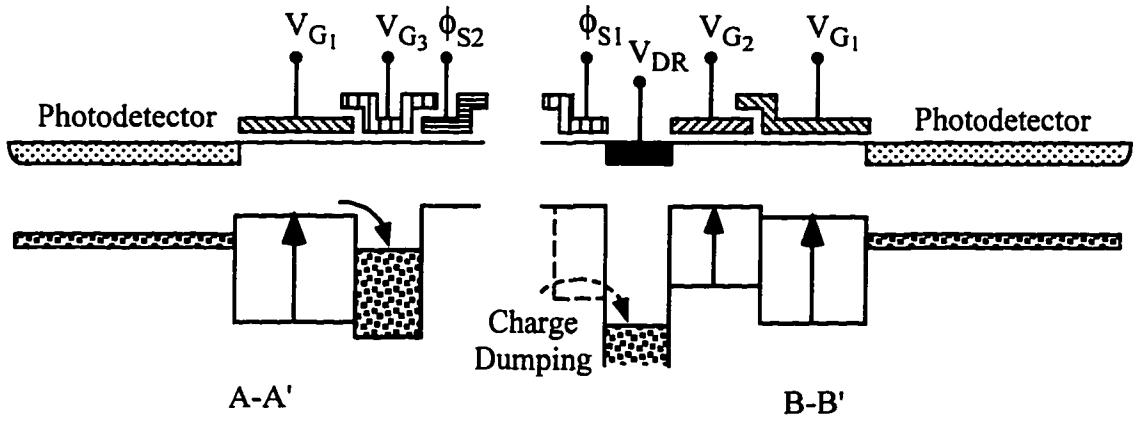
The operation of the VHFR imager consists of two periods: the frame collection or accumulation period and the frame readout period. During the frame collection period, the charge signal detected by the photodetector is transferred in series into the serial-parallel SP BCCD register. After the detection of each 5 frames, the detected charge signals are transferred in parallel from the serial-parallel SP register to the 5 x 5 parallel P BCCD register, providing storage for the last 30 detected image frames. The continuous storage of the last 30 frames is achieved by a parallel transfer into the serial-parallel SP register of the charge signals from the last row of the parallel P register of the macropixel above, preceding the loading of the serial-parallel SP register from the photodetector.



(a) *Top view of the photodetector output structure*



(b) *Cross-section of A-A' and B-B' and potential profiles during the charge accumulation*



(c) *Cross-section of A-A' and B-B' and potential profiles during the charge readout*

Figure 3.2 *Construction and operation of photodetector readout.*

The last row of 5 charge signals is transferred to the dumping drain D while a new row of 5 pixels corresponding to the next 5 frames is transferred from the photodetector into the serial-parallel SP register. Finally, at the end of charge collection period, last 30 frames are stored in the BCCD storage register of the macropixel.

The readout of the detected 30 frames is initiated by completing the loading of the serial-parallel SP register with the last 5 frames. During the frame readout period, the frame collection operation is stopped and the photogenerated signal detected by the photodetector is transferred (drained) directly to the blooming drain D. At this point in time, all of the BCCD storage registers of each quadrant are converted under control of the BCCD clocks into a single large frame-transfer type CCD readout of 180 x (5 + 1) rows and 180 x 5 columns. For the 3-phase BCCD design, this charge readout involves up to 180 x 6 x 3 = 3240 transfers in vertical direction by the parallel registers and up to 180 x (5 + 1) x 3 = 3240 transfers in horizontal direction by the serial output register.

3.3 Process Technology and Chip Topography

The VHFR burst-image sensors were fabricated at David Sarnoff Research Center with a four layer of poly silicon and three layer of metal fabrication process. The imager sensors were fabricated on 17.5μm thick p-type epi wafer with resistivity of 43Ωcm on <100> CZ p^+ substrate with resistivity in the range of 0.008Ωcm to 0.025Ωcm. Two layers of aluminum were used for metal interconnections and third layer of aluminum served as an optical shield over the BCCD memory regions.

Four layers of polysilicon were employed in the fabrication process for an area efficient design of the macropixel layout. To achieve high density and low transfer losses [30]-[32], the 3-phase buried channel CCD storage register was constructed with an additional layer of polysilicon functioning as the channel stops during serial charge transfer at each macropixel (Figure 3.3).

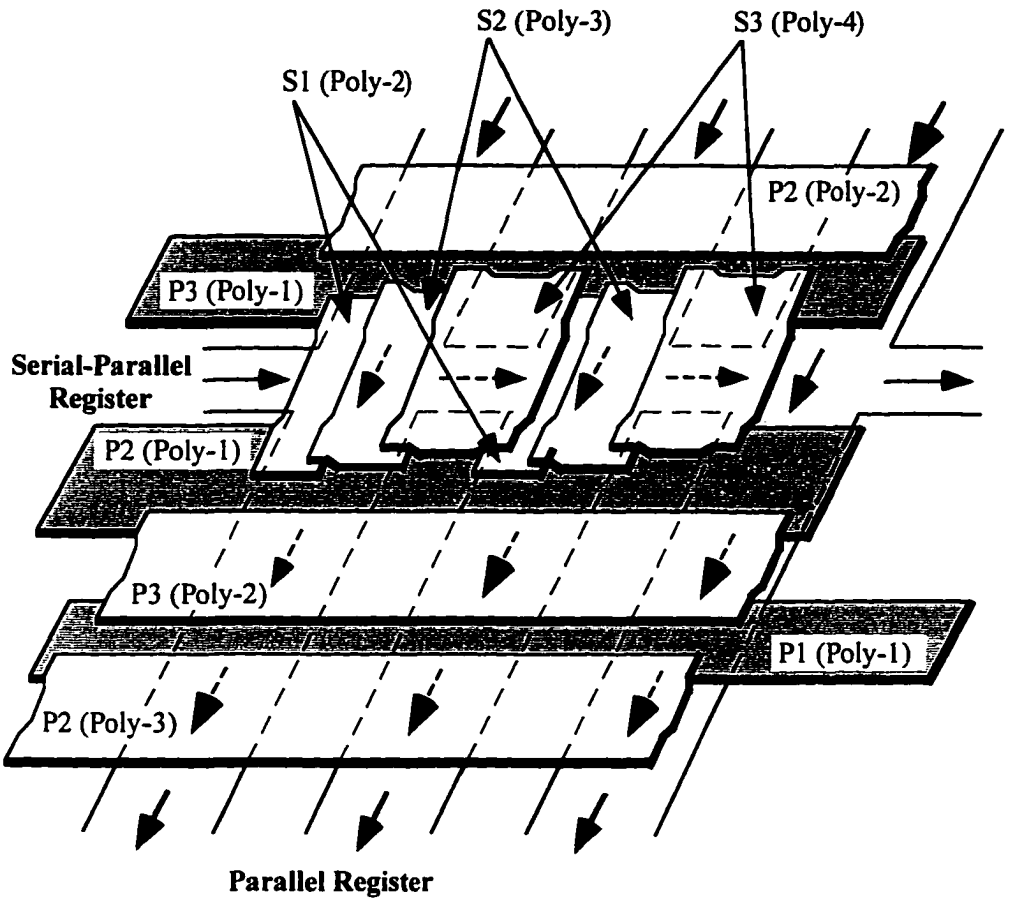


Figure 3.3 *Design of serial-parallel SP and parallel P registers with 3-phase CCD, four-level-polysilicon construction.*

The serial-parallel SP register phases S1, S2 and S3 are constructed by poly-2, poly-3 and poly-4 respectively. When the charge is transferred in SP register, two poly-1 layers (shown as phases P2 and P3) act as induced channel-stop in vertical direction for horizontal charge transfer. When the charge is transferred in P register, poly-4 gates (phase S3) act as the induced channel-stops for vertical charge transfer, and poly-2 and poly-3 gates (phases S1 and S2) are clocked as P1 of P register.

Dual gate insulator [33] of silicon dioxide (350Å) /silicon nitride (650Å) was fabricated to improve the yield and to enhance the charge transfer efficiency. Silicon

nitride layer was deposited on the thermally grown channel oxide to prevent the gate lift-up at polysilicon edges and to avoid the possible transfer losses.

1D and 2D device simulations were performed to optimize the operation of the VHFR imager. The choice of BCCD implant doses and energies for the fabrication was based on 1D simulation results performed by Suprem III [34], [35] Arsenic and Phosphorus dual implantation was employed to form the n-channel of BCCD storage elements. The fabrication lot was split between two options of BCCD implants. Arsenic and Phosphorus implant doses were kept at $6.5 \times 10^{11} cm^{-2}$ for one set of wafer fabrication. In the second set of wafers Arsenic and Phosphorus implant doses were increased to $1.2 \times 10^{12} cm^{-2}$ and $1.0 \times 10^{12} cm^{-2}$ respectively to achieve higher charge handling capacity. For both cases, the maximum electric field intensity at Si/SiO_2 interface was found to be less than the critical field value [36], [37] of $3 \times 10^5 V/cm$ by Suprem III. The doping profile for higher BCCD channel option implant obtained by Suprem III is illustrated in Figure 3.4 . The junction depth is mainly determined by Phosphorus implant and is calculated as 1.0μm for high BCCD implant dose option and 0.94μm for low BCCD implant dose option. The thickness of gate insulator is obtained as 0.035μm of silicon dioxide and 0.064μm of silicon nitride by simulation.

Cross-sectional view of the chip was simulated by ISE-TCAD [2], [38]. Figure 3.5 and 3.6 illustrate the SEM photographs of the VHFR imager in (a) and the results of 2D process simulation at the corresponding cut-lines in (b). Figure 3.5 shows the topography of four poly silicon layers operating as gate electrodes of the 3-phase imager and a metal-1 contact to poly-4 layer. Using the pixel layout as input and defining the fabrication process flow, the same cut-line was simulated by the 2D process simulator Tedios of ISE-TCAD package. The anisotropic deposition of Aluminum as metal-1 was defined precisely by the step coverage factor of the available process model and the glass flow on polysilicon gate layers was calibrated according to the SEM picture [39].

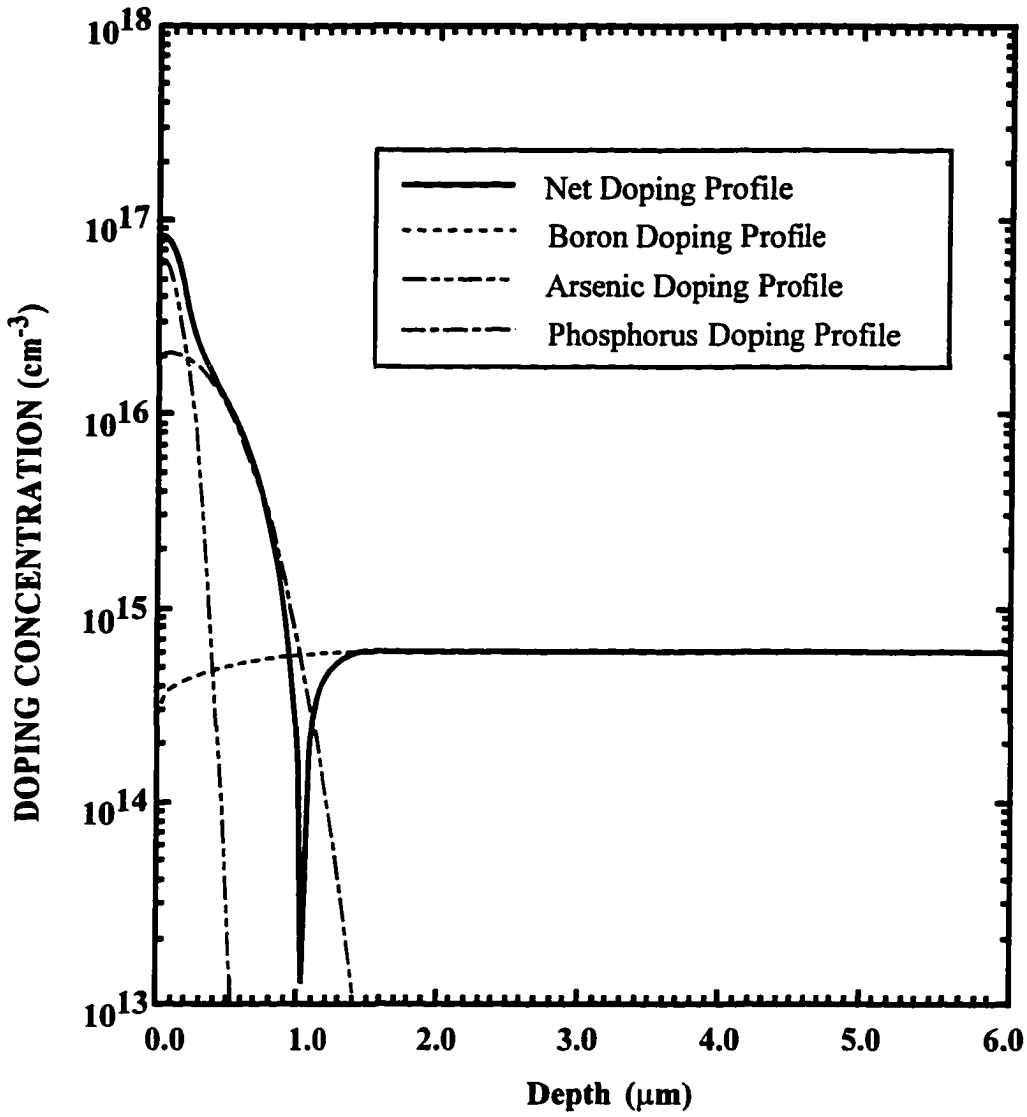
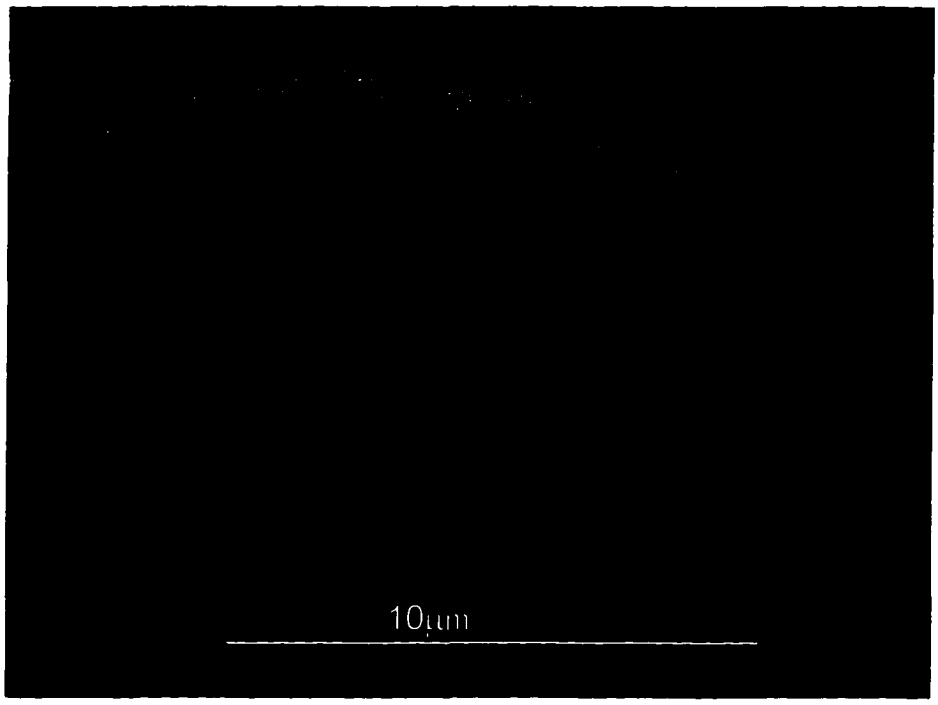
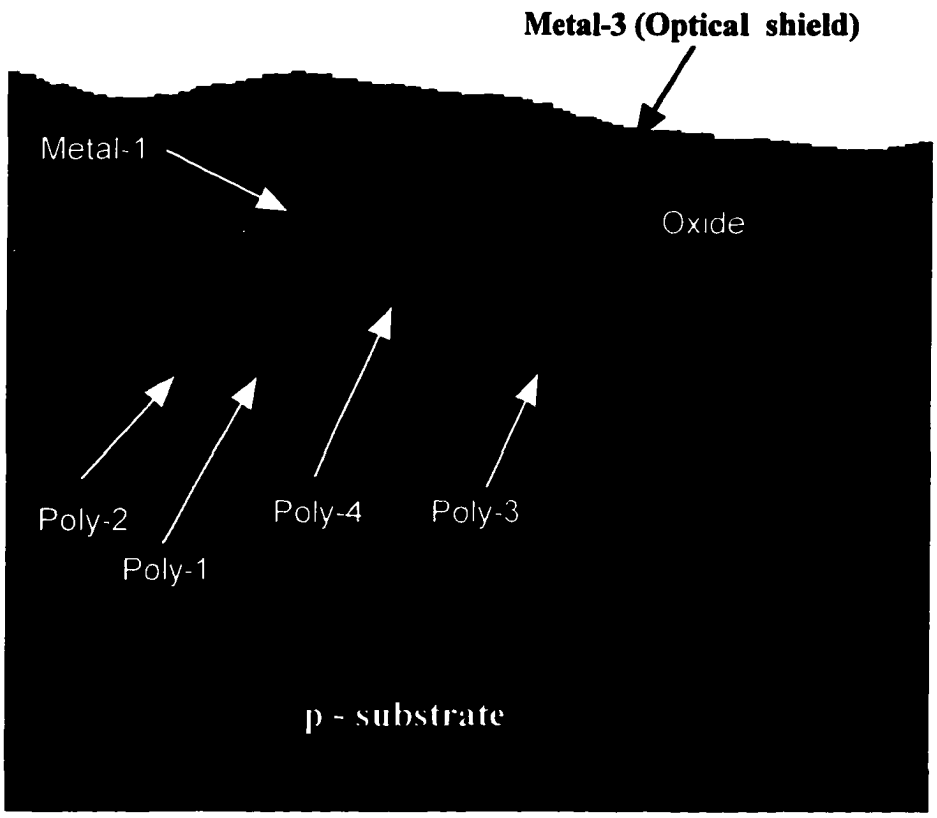


Figure 3.4 *Doping profile of BCCD implant. (As : 1.2x10^{12}cm^{-2}, 120keV P : 1.0x10^{12}cm^{-2}, 180keV)*

Figure 3.6 illustrates the SEM picture of the bird's beak effect at the boundary of field oxide to poly-2 and the simulated effect of the bird's beak at the corresponding cut-line. Figure 3.7 and Figure 3.8 illustrate the cross-sectional view simulated by ISE-TCAD across the serial-parallel (SP) register including the photodetector readout structure with dumping drain D and the simulated cross-sectional view of a horizontal cut-line across the parallel (P) register.

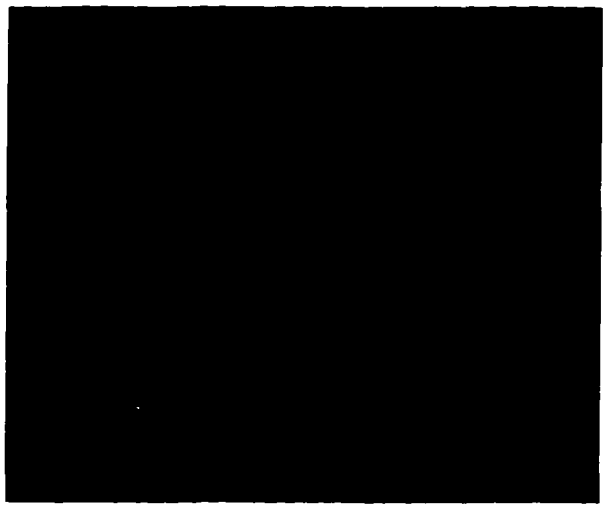


(a)

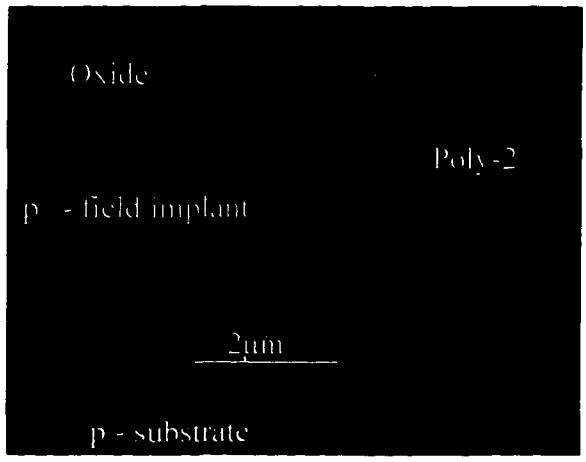


(b)

Figure 3.5 *(a) SEM picture of a cut-line across serial-parallel SP register.*
(b) Cross-sectional view obtained by 2D simulation at the same cut-line.



(a)



(b)

Figure 3.6 *(a) SEM picture illustrating the bird's beak effect at poly-2 layer.*
(b) Cross-sectional view obtained by 2D simulation at the same cut-line.

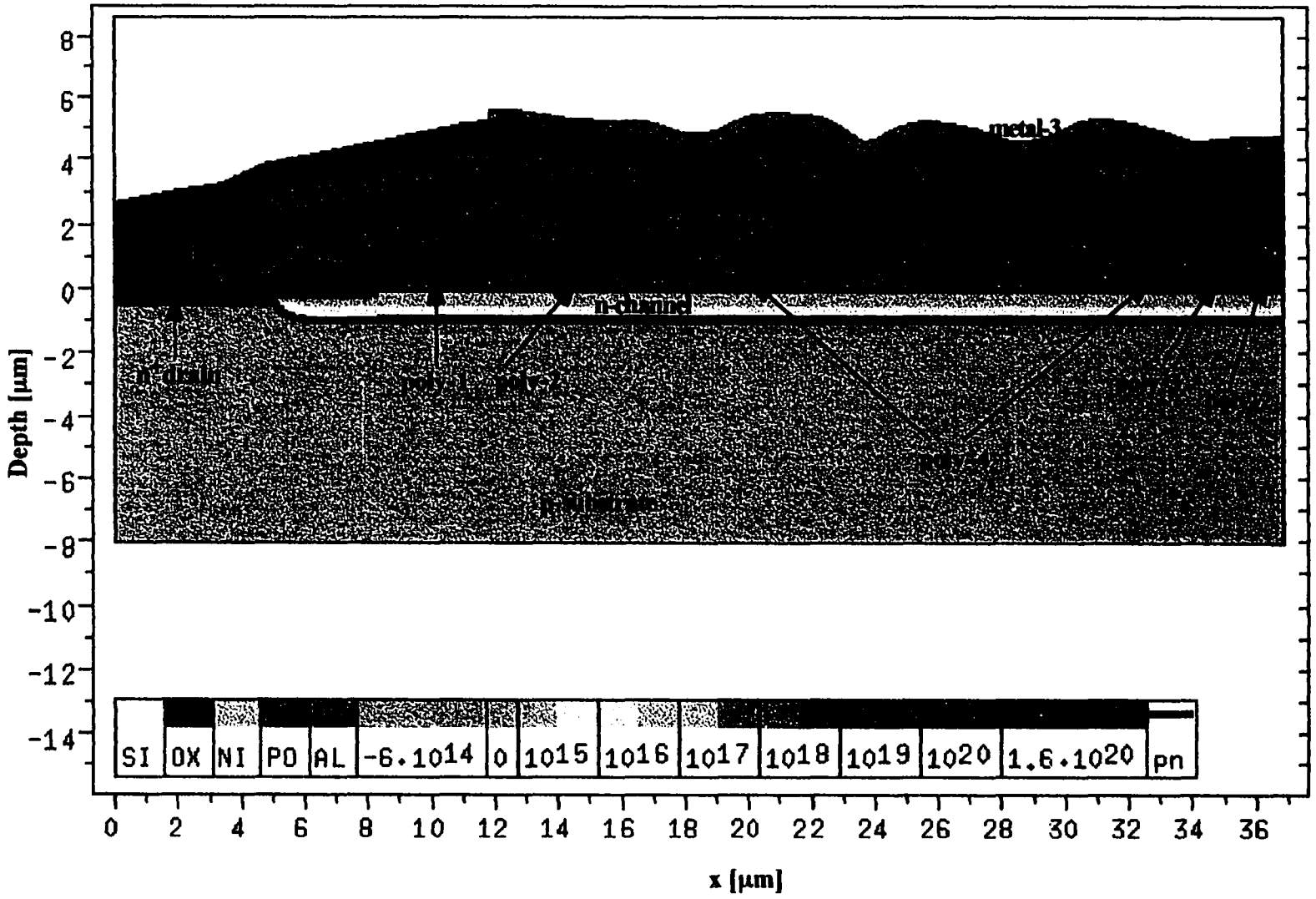


Figure 3.7 *Simulated cross-section across the serial-parallel (SP) register.*

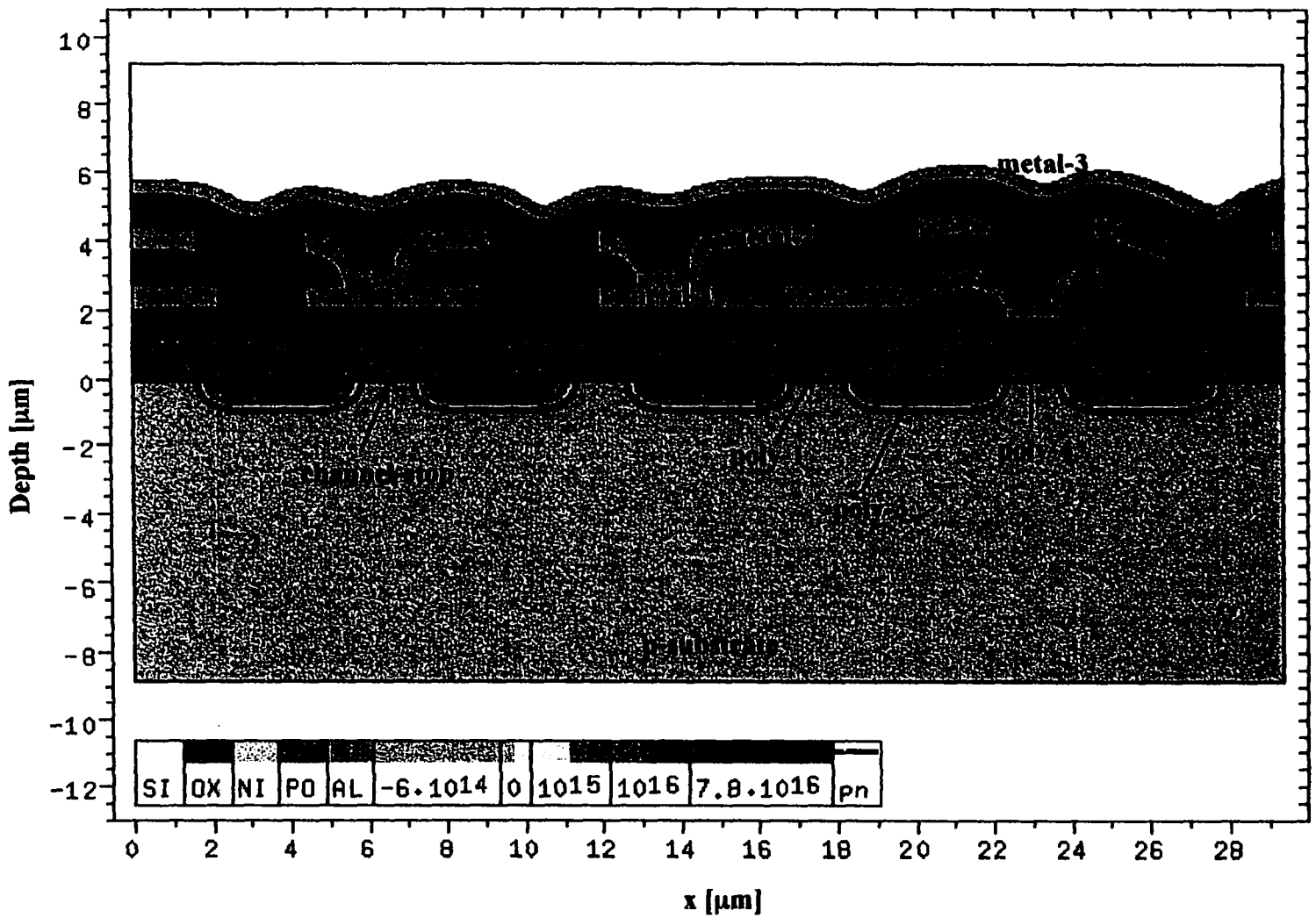


Figure 3.8 *Cross-sectional view of a horizontal cut-line in the parallel (P) register.*

3.4 Process Specification

The process specification for fabrication of the VHFR burst-image sensor is summarized below:

- 17.5-μm thick p-type epitaxial wafer with resistivity of 43 ohm-cm on <100> CZ p^+ substrate with resistivity in the range of 0.008 to 0.025 ohm-cm were used as substrate material.
- Four layers of polysilicon and three layers of metal were used.
- A dual channel dielectric of SiO_2/Si_3N_4 is employed.
- Two BCCD implant doses were chosen: low implant dose with $6.5x10^{11}cm^{-2}$ of Arsenic and $6.5x10^{11}cm^{-2}$ of Phosphorus, and high implant dose with $1.2x10^{12}cm^{-2}$ of Arsenic and $1.0x10^{12}cm^{-2}$ of Phosphorus with implant energy of 120keV for arsenic and 180keV for Phosphorus.
- The channel stops for BCCD channels have been defined by regions in the form of p-type substrate.
- The pinned-buried graded photodetector was constructed by BCCD implant with three additional n-type implants with Phosphorus implant doses of $1.4x10^{12}cm^{-2}$, $1.2x10^{12}cm^{-2}$, and $1.0x10^{12}cm^{-2}$ and a top thin p^+-implant with BF2 dose of $2.5x10^{14}cm^{-2}$ for the low BCCD implant dose option and $3.0x10^{14}cm^{-2}$ for the high BCCD implant dose option. Implant energy was 120keV for Phosphorus n-type detector implants and 30keV for the BF2 p^+-detector implant.
- The estimated total thermal diffusion of BCCD Arsenic and Phosphorus implants is about 330 minutes at 950°C and 90 minutes at 1050°C. Total thermal diffusion of the additional photodetector Phosphorus implants is about 90 minutes at 1050°C and 30 minutes at 950°C. The total thermal diffusion for BF2 p^+ photodetector implant is about 30 minutes at 950 °C.
- The n^+ diffusions for blooming/dumping drain and source drains are defined by polysilicon gates on the channel side and thick-oxide regions formed as recessed

oxide with a p-type implant. To avoid voltage breakdown of the n^+ diffusions, recessed thick oxide p-type implant was selected to be 3.0×10^{12} cm^{-2}.

- As a general design/layout procedure, the pinned-buried photodetector, the output amplifiers, and whenever possible the outside perimeter of the burst-image sensor were surrounded by a p^+-field implant corresponding to Boron implant dose of $2.5 \times 10^{15} cm^{-2}$ at 35keV.

3.5 Demonstrated Performance

The operation of the imager was demonstrated at the Princeton Scientific Instruments, Inc. using camera electronics developed for testing. The test results are available only for operation of a single quadrant consisting of 180x180 pixels fabricated with high channel implant dose option [2]. Figure 3.12 illustrates a sequence of 30 images of optical test pattern for operation with 2μs frame time for the first frame and 1μs frame time for the next 4 frames of each 5-frame sequence. This demonstrates an effective frame rate of 8.33 x 10^5 frames per second. To reduce the dark current, the imager is operated at -30°C. The test pattern is illuminated by a sequence of 0.4μs LED pulses which is controlled by computer to be turned ON at any frame time. The output signal of the imager is readout by correlated double sampling to eliminate the reset noise. For clock frequency of the output amplifier of 120kHz, the readout time of 30 frames is about 8 seconds. The resulting dark current was found to be in the range of 100 to 200 electrons/pixel.

The initial tests of the VHFR imager reported by Princeton Scientific Instruments indicate that the useful charge handling capacity, Q_{max}, without observable transfer losses ($<< 10^{-5}$) is about 11000 electrons/pixel depending on the clock voltages. The readout noise (with no illumination) was measured as 9rms electrons/pixel resulting in a dynamic range of 1200:1. The effective conversion gain of the output amplifier was measured to be 2.2μV/electron.

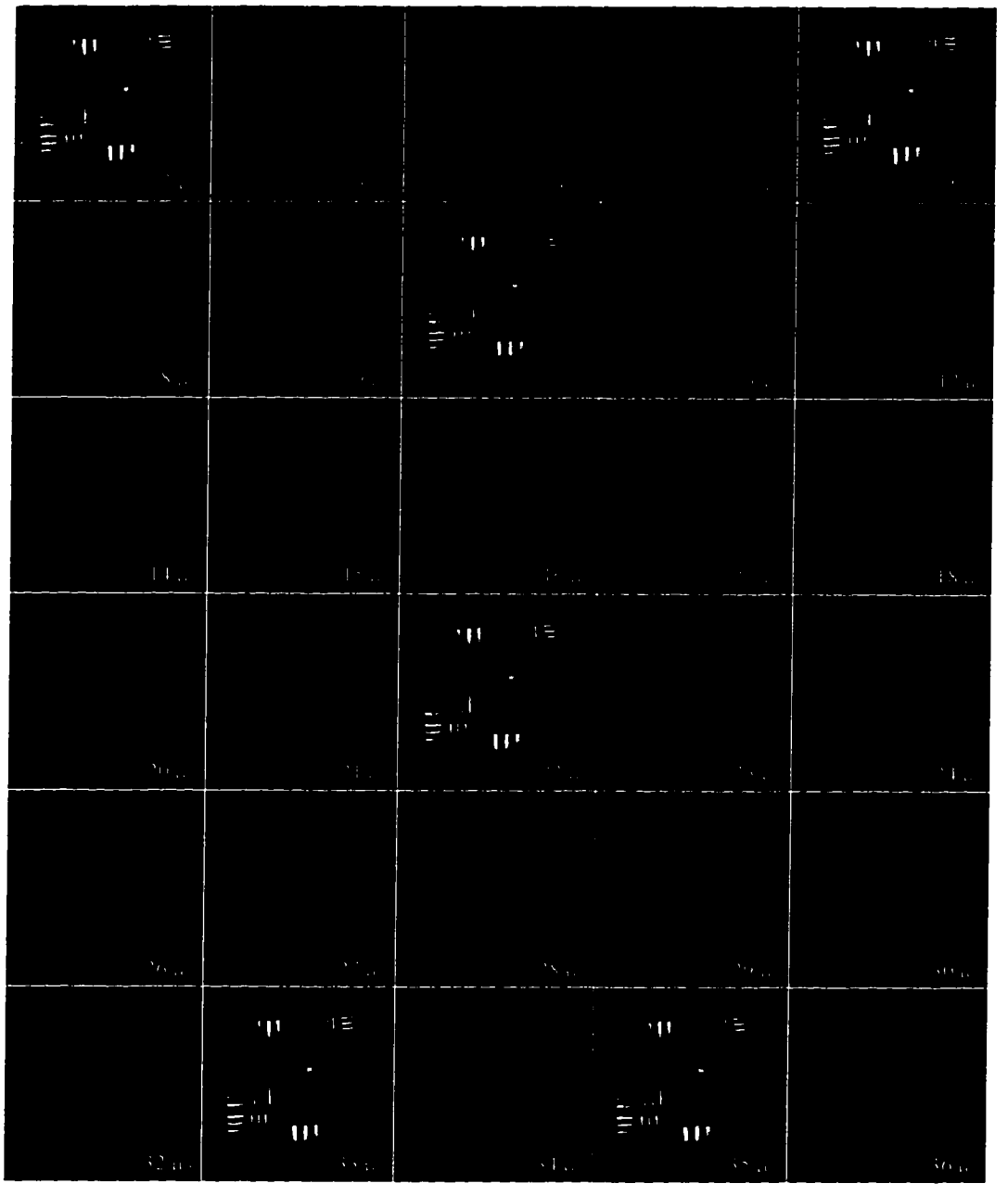


Figure 3.9 *Reconstructed images of 30 frames with the resolution pattern illuminated by LED for 0.4μs during optical integration time of frame 1, 5, 8, 18, 27 and 29.*

CHAPTER 4

CHANNEL CHARACTERISTICS OF 360 x 360 ELEMENT VERY HIGH FRAME RATE VISIBLE BURST IMAGE SENSOR

4.1 Channel Potential Variation as Function of Gate Voltage

In order to analyze the different operation modes of the VHFR BCCD register, it is useful to look at the channel potential variation as function of the applied gate voltage. Different curves were obtained for both high and low dose BCCD channel implant options, and for various dielectric thicknesses. Comparison of experimental results with simulation results show that the experimental data obtained by measurements at David Sarnoff Research Center is in good agreement with the results obtained by computer simulations. 1D simulations were performed to plot the channel potential variation as function of gate voltage using Suprem III and obtained results were verified by Pisces IIB [40]-[42]. Consistent results were obtained using both 1D and 2D simulation tools.

4.1.1 Measurement Results

The test device fabricated on the imager chip is illustrated in Figure 4.1.

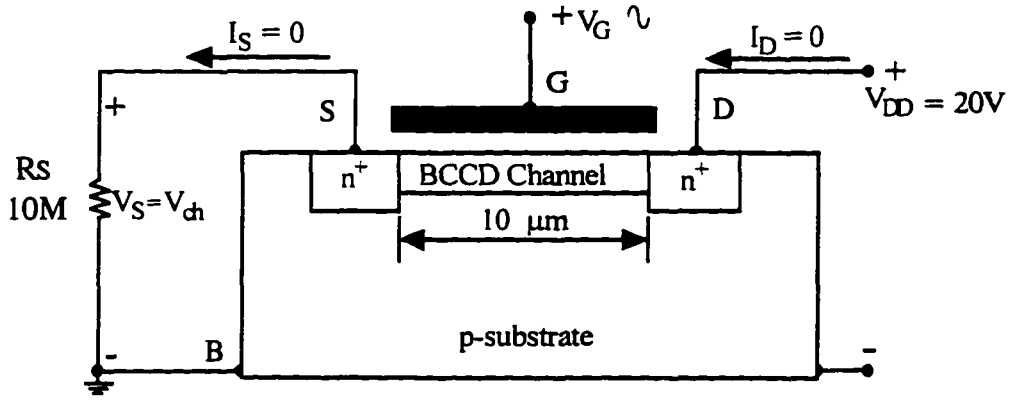


Figure 4.1 *Test structure and experimental set-up for measuring channel potential V_{ch} as function of gate bias.*

It is constructed as a MOSFET with a BCCD channel and highly doped n-type source and drain regions. The gate length and width of the test structure are 10μm and 20μm respectively. The first deposited polysilicon layer (poly-1) was used as the gate electrode to ensure that the thickness of the gate dielectric remains unaffected from the following fabrication steps. However, the gate dielectric thickness under the following polysilicon layers (poly-2 , poly-3 and poly-4) are expected to be thinner because during the etch process of the polysilicon layers, it was observed that part of the silicon nitride of the channel dielectric layer was also etched. But the gate dielectric thickness under the first deposited polysilicon layer, consisting of a dual dielectric of 350Å silicon dioxide and 650Å silicon nitride, will not be affected by the further processing steps.

The positive voltage applied to the drain of the test structure is to maintain the BCCD channel completely depleted of the majority carriers at any gate bias. The source resistor of 10MΩ ensures that there is no current flow from drain to source. In order to obtain the relationship between the channel potential and the gate bias, a sinusoidal voltage was applied to the gate electrode. Measurement of the corresponding source voltage gives a plot of the channel potential as function of the gate voltage, where

$$V_{ch} = V_S. \tag{4.1}$$

Measurements were taken at David Sarnoff Research Center for both high and low BCCD implant doses. Result for low dose BCCD implant option is illustrated in Figure 4.2. Inspection of this curve provides useful information about the buried channel characteristics.

As marked in this figure, the vertical and horizontal scale is 1V/division. The pinning gate voltage is approximately -4.6V and the corresponding channel potential (the channel potential in pinning) is 1.4V. The channel potential at applied 0V gate bias is about 4.7V.

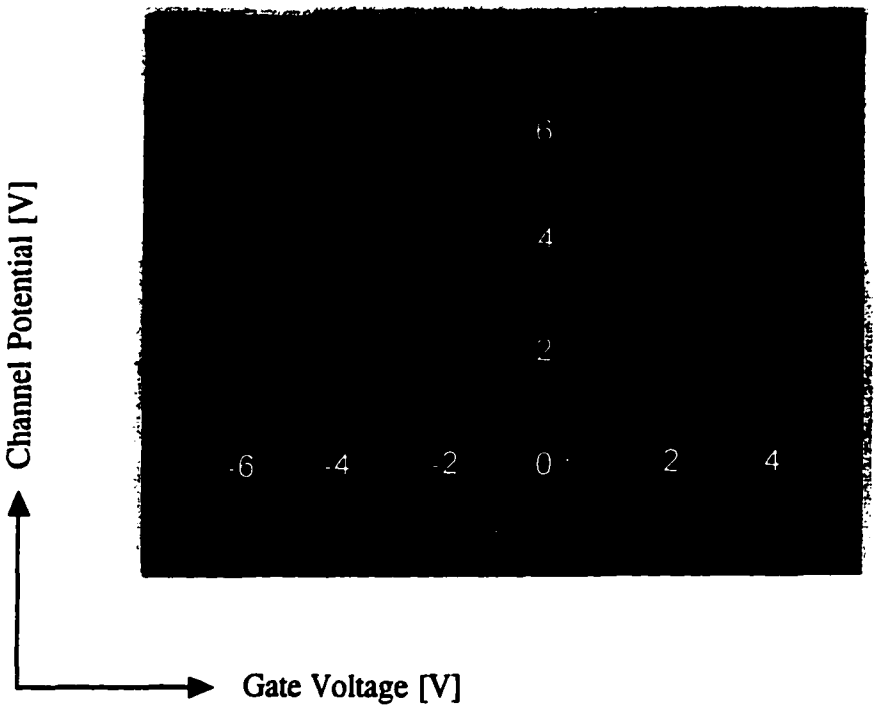


Figure 4.2 *Measurement of the channel potential variation under poly-1 layer gate electrode with applied gate bias for low BCCD implant dose option.*

Figure 4.3 illustrates the channel potential variation with the applied gate bias for high dose BCCD implant option. The vertical and horizontal scale in this figure is now 2V/division. Through inspection of this figure the following values can be extracted: The pinning gate voltage is approximately -6.8V and the corresponding channel potential is 3.0V. The channel potential at applied 0V gate bias is about 8.4V.

The measured data is of great importance for the further study of the BCCD register. The parameters such as charge handling capacity, barrier channel potential and different operation modes of the BCCD register, as well as channel-stop potential profiles can be understood and analyzed more easily with the obtained data. For further analysis, it is also important to obtain consistent data by simulations. These values provide a basis for design and optimization of new structures with different features before any fabrication is accomplished.

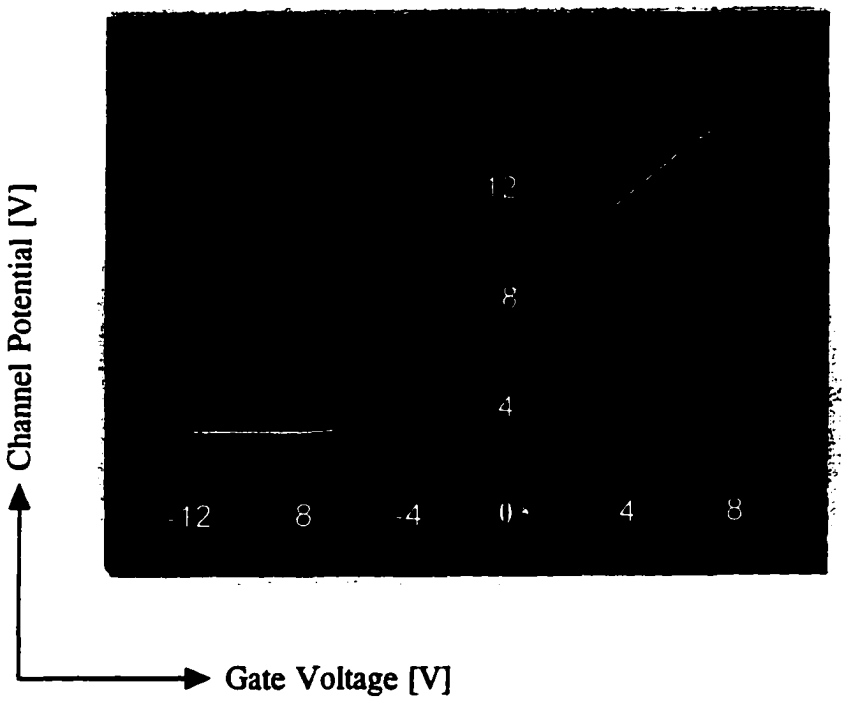


Figure 4.3 *Measurement of the channel potential variation under poly-1 layer gate electrode with applied gate bias for high BCCD implant dose option.*

4.1.2 Simulation Results of Channel Voltage as Function of Gate Bias

1D simulations were performed using Suprem III to plot the channel potential as function of the applied gate voltage. The simulations were repeated for dual channel implants with low (Arsenic: $6.5 \times 10^{11} cm^{-2}$, 120keV and Phosphorus: $6.5 \times 10^{11} cm^{-2}$, 180keV) and high (Arsenic: $1.2 \times 10^{12} cm^{-2}$, 120keV and Phosphorus: $1.0 \times 10^{12} cm^{-2}$, 180keV) BCCD implant dose options. Results are presented in Figure 4.4 for both low and high doping profiles.

The pinning gate voltage obtained by Suprem III for low BCCD implant dose is around -5.1V and the corresponding channel potential is 1.5V. The channel potential at 0V gate bias is obtained as 5.25V by Suprem III for low BCCD implant option. The simulation for pinning gate voltage was also performed by the 2D simulator Pisces IIB and found to be as -4.9V.

The pinning gate voltage simulated by Suprem III for high dose BCCD implant option is -7.6V and the corresponding channel potential is 3.4V. The channel potential at zero gate bias is 9.6V. According to the results obtained by Pisces IIB, the pinning gate voltage is calculated as -7.4V. Comparing with the measurements, the values of pinning gate voltages, and the channel potentials at pinning and zero gate bias for both low and high dose BCCD implant options are within 10% agreement with the experimental data.

Figure 4.4 also shows that the potential maximum varies linearly with the increasing gate voltage [40]. The channel potential is determined by the substrate doping, thickness of the gate dielectric and doping profile of the n-channel. For a given gate bias the potential maximum increases with the increasing gate dielectric thickness. Increasing implantation dose of Arsenic or Phosphorus also results in higher values of channel potential. However, increasing the substrate doping concentration decreases the junction depth and consequently the channel potential for the same gate bias [43].

The difference obtained by the simulation results and the measured data is due to the inaccuracy of implant dose and energy values used during imager fabrication and the default parameters such as diffusion coefficients of dopant atoms used in process simulations [44].

4.1.3 Effect of Gate Dielectric Layer Thickness on Channel Voltage

It is also useful to estimate the pinning gate voltages and the corresponding channel potentials of the channels under poly-2, poly-3 and poly-4 gate electrodes. The 650Å thick silicon nitride layer is expected to be etched off partially or even completely under these electrodes during etching process to form these polysilicon gates with poly-2, poly-3 and poly-4 layers. Therefore, the analysis of channel potential variation as function of applied gate voltage was extended to investigate the dependence of channel potential variation on gate dielectric thickness as function of applied gate voltage.

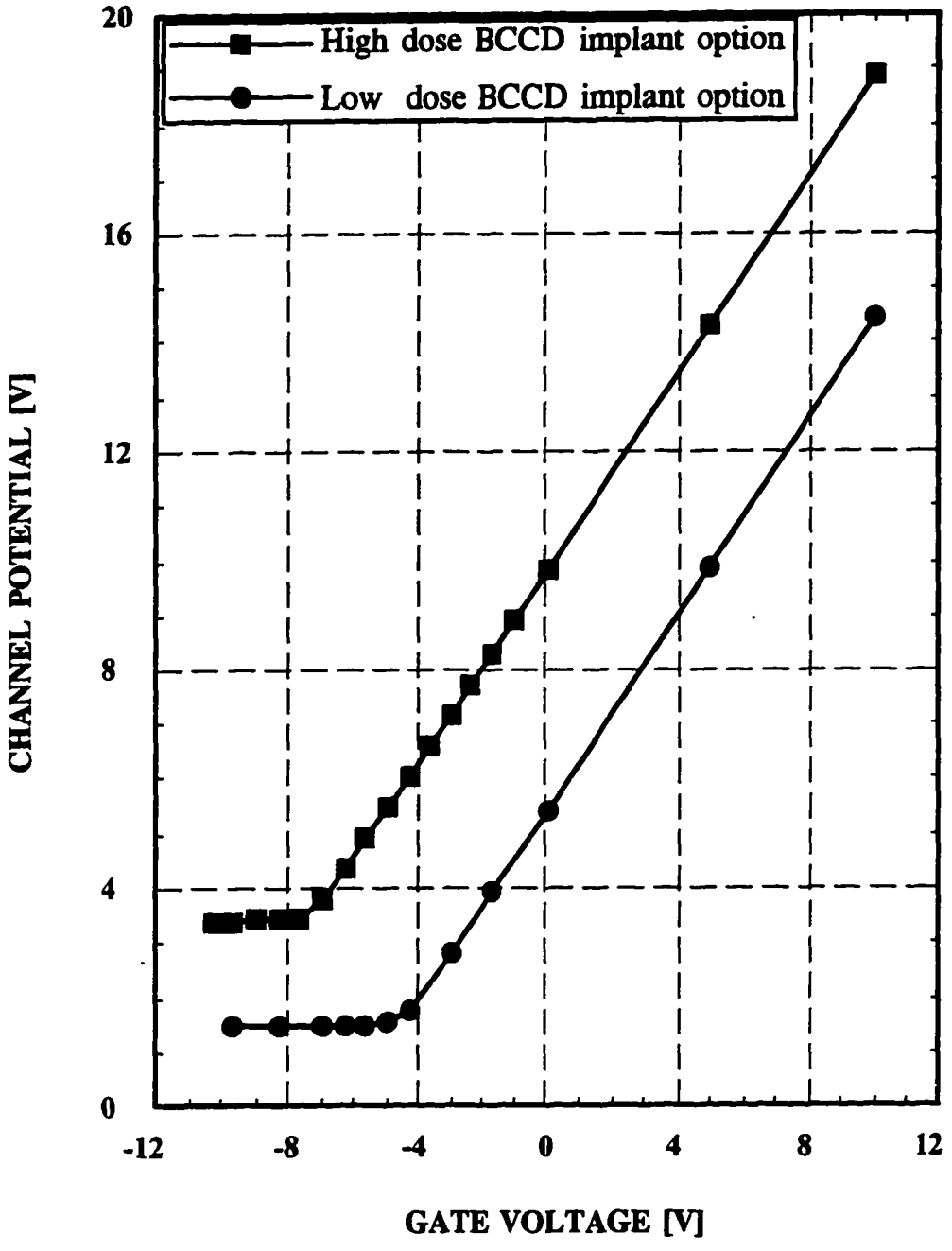


Figure 4.4 *Simulation results of variation of the channel potential as function of the applied gate voltage for low and high BCCD implant dose options.*

Calculations were performed for two cases for low BCCD implant dose option: In the first case, silicon nitride is assumed to be partially etched and its thickness is reduced to about half of the initially deposited value (317Å). In the second case, analysis was done for gate insulator consisting of only 349Å silicon dioxide assuming an almost entirely removed silicon nitride layer with thickness of 7Å. Results obtained for low BCCD implant dose option are illustrated in Figure 4.5.

A more detailed analysis was performed for the high BCCD implant dose option and these results are presented in Figure 4.6. The channel potential as function of gate voltage is simulated for the following thicknesses of the silicon nitride layer: 637Å, 477Å, 317Å, 162Å and 7Å. Results are summarized in Tables 4.1 and 4.2 for both BCCD channel doping profiles.

Table 4.1 Simulation results obtained for low dose BCCD implant.

Dielectric Layer Thickness	Pinning Voltage [V]	Channel Voltage [V]
637Å Si_3N_4 / 349Å SiO_2	-5.136	1.505
317Å Si_3N_4 / 349Å SiO_2	-4.326	1.503
7Å Si_3N_4 / 349Å SiO_2	-3.426	1.509

Table 4.2 Simulation results obtained for high dose BCCD implant.

Dielectric Layer Thickness	Pinning Voltage [V]	Channel Voltage [V]
637Å Si_3N_4 / 349Å SiO_2	-7.625	3.435
477Å Si_3N_4 / 349Å SiO_2	-6.833	3.438
317Å Si_3N_4 / 349Å SiO_2	-6.041	3.435
162Å Si_3N_4 / 349Å SiO_2	-5.248	3.436
7Å Si_3N_4 / 349Å SiO_2	-4.456	3.438

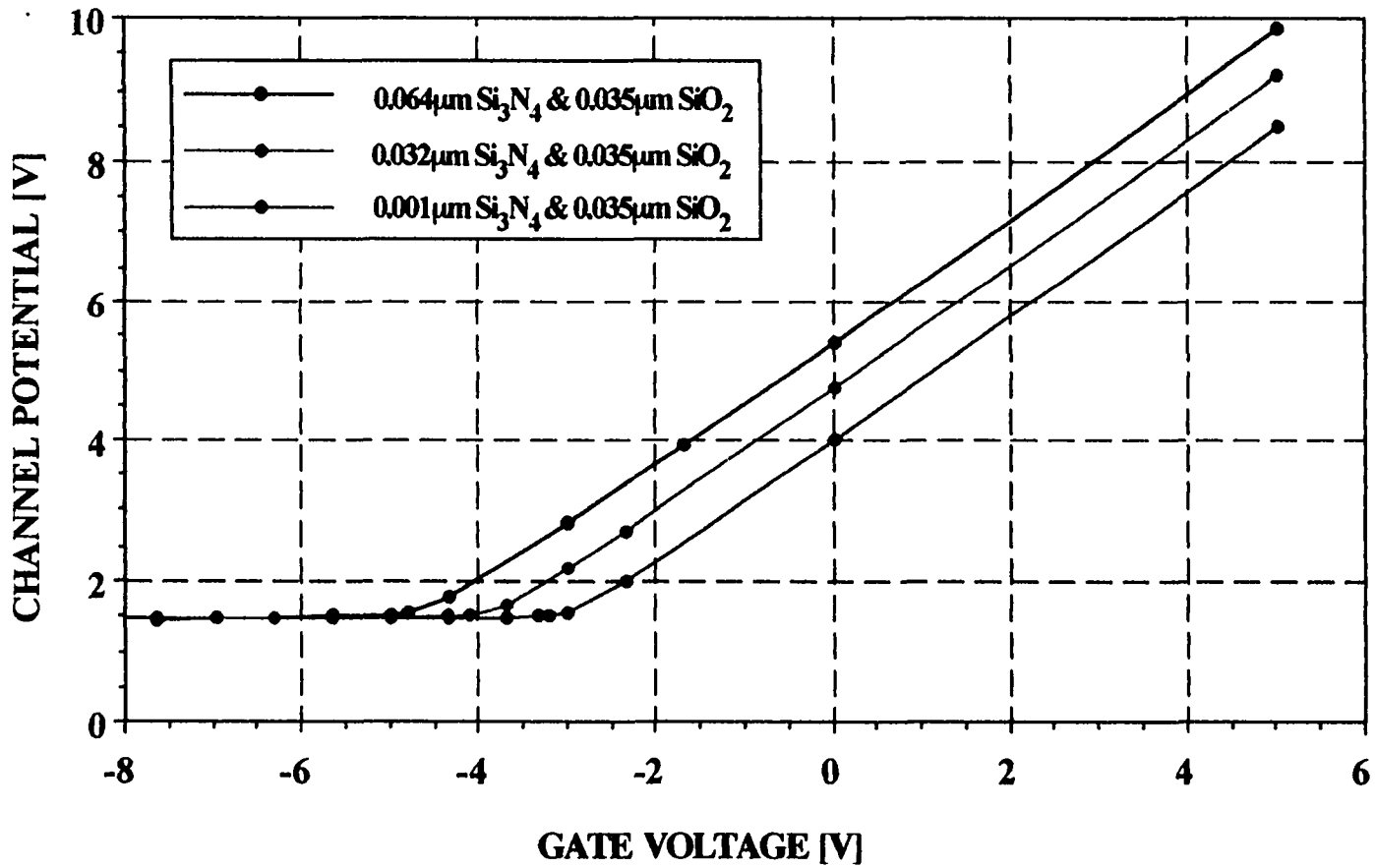


Figure 4.5 *Simulation result of variation of the channel potential vs gate voltage as function of dielectric layer thickness for low dose BCCD implant option.*

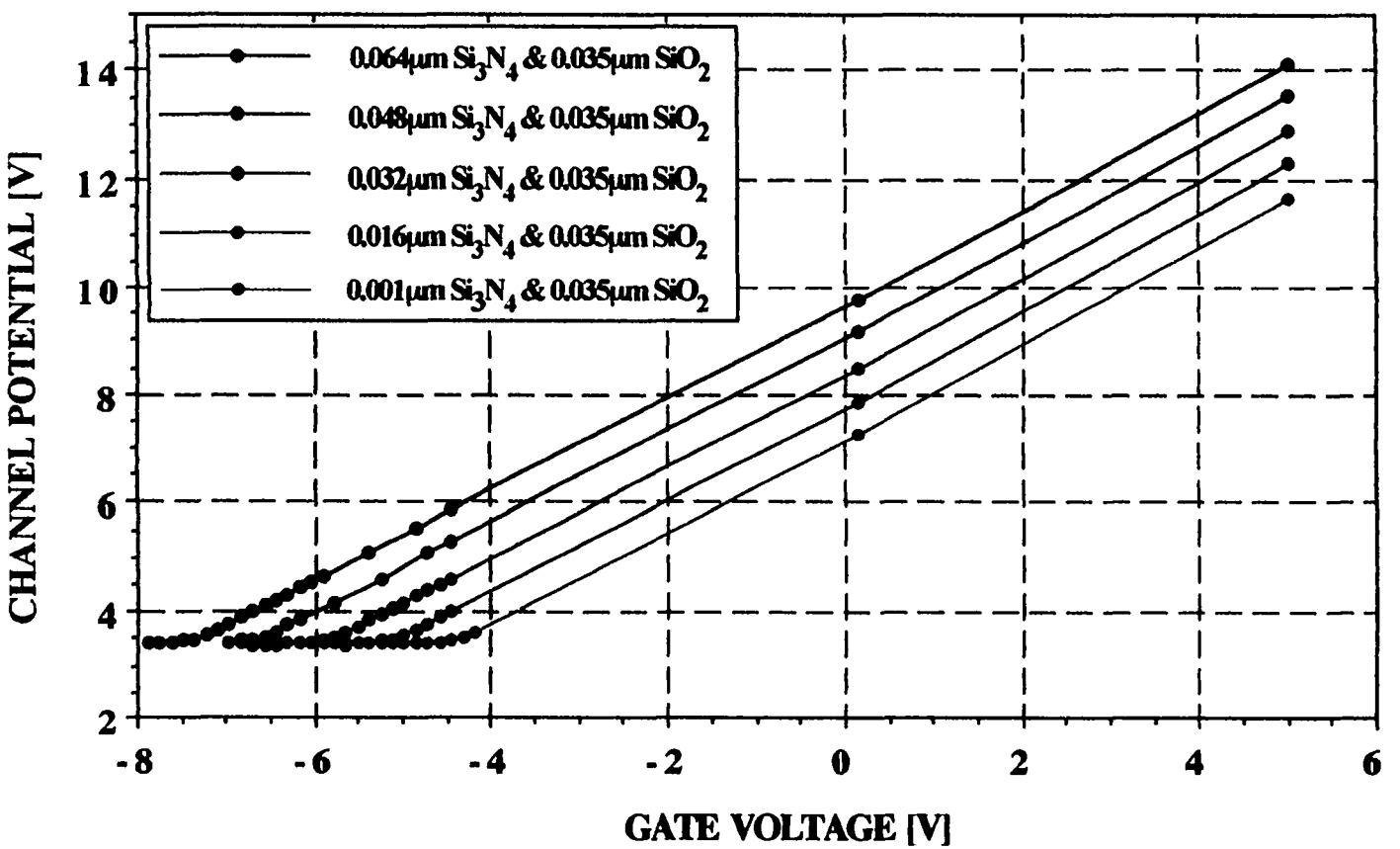


Figure 4.6 *Simulation result of variation of the channel potential vs gate voltage as function of dielectric layer thickness for high dose BCCD implant option.*

Inspection of Figures 4.5 and 4.6 show that the thickness of gate dielectric does not affect the channel potential under pinning gate electrode. However, the pinning gate voltages become more positive with decreasing gate dielectric thickness. Also, the channel potential (the potential maximum in BCCD channel region) decreases under thinner gate dielectric layers for a given gate bias.

4.2 Different Clocking Schemes of the BCCD Register

The gates with a high voltage applied form potential wells for storage of charge packet, whereas the gates with a low voltage applied form the potential barriers to confine the charge packet under the storage gates between the barrier gates. As negative voltage is applied to the gate of the BCCD the peak potential in the channel as well as the potential at the silicon/insulator interface tends to decrease. The channel stops of the device are adjacent to the buried channel and provide a source of holes. Thus, the channel potential can not move above ground potential without attracting an unlimited number of holes from the channel stop [16]. If the potential applied to the gate is allowed to become more negative, holes moved to the channel region from the channel stops pin the channel potential so that no further reduction in channel potential occurs. When the device is operating with an applied gate voltage equal or more negative than the pinning voltage, the device is said to be operating in pinning.

To store and confine charge in BCCD pixel memory elements for reliable operation, two constraints were set on the full well conditions [35], [45]. The first condition requires that the peak potential of a full well should be at least 10kT/q higher than the surface potential. This ensures a buried-mode operation. The second condition is fulfilled by a 20kT/q difference between the full well potential and the maximum of adjacent barrier channel potentials. The determination of the full well condition is given by:

$$\phi_{Full} \geq \{ \phi_{max}(pin) + 20kT/q , \phi_{Surface} + 10kT/q \}. \qquad (4.2)$$

Gate voltage swing for three different modes of operation is shown in Figure 4.7. In operation **Mode A** gate voltage varies from 0V to pinning; $\Delta V_G = 0 - V_G(pin)$ where a potential well forms under zero biased gate, and the gate biased in pinning forms a barrier between the adjacent wells. The maximum full well is determined either by a 10kT/q difference of the full well potential to the surface potential or by a 20kT/q difference of the full well potential to the maximum of barrier channel potential of the adjacent wells.

Optimum full well capacity for a multi-phase CCD is achieved when both constraints are satisfied, i.e. when blooming and surface full well occur simultaneously.

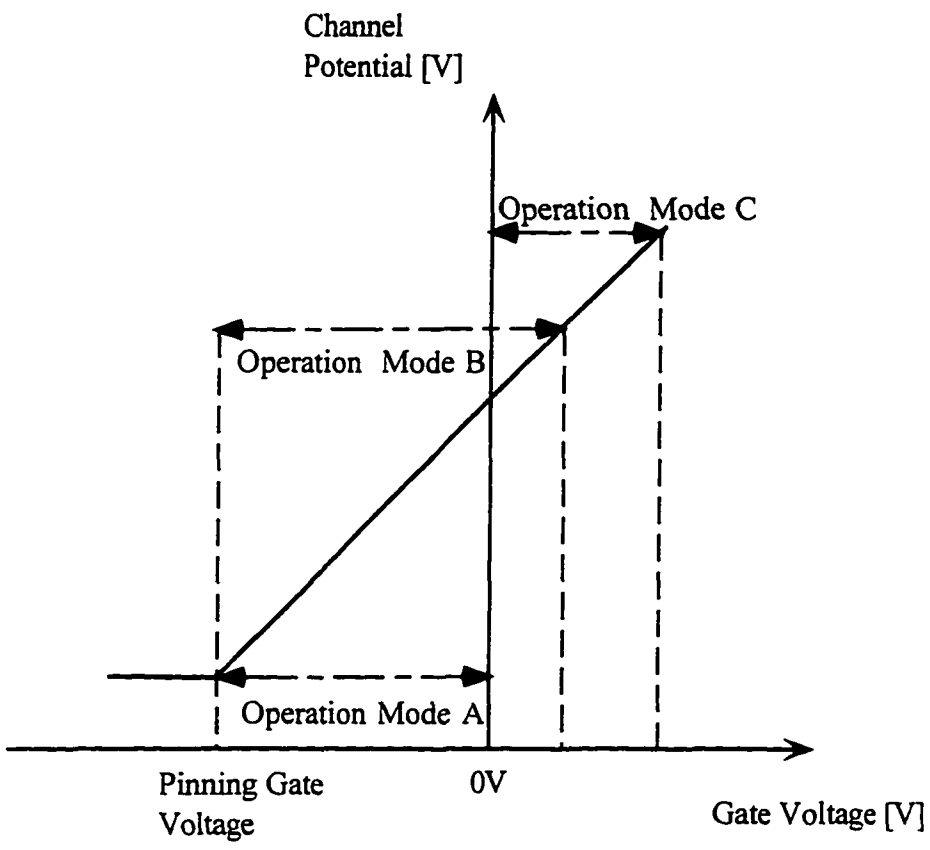


Figure 4.7 *Different modes of operation illustrated on the BCCD channel potential variation with the applied gate bias.*

Gate voltage varies between the pinning gate voltage and V_g ; $\Delta V_G = V_g - V_G(pin)$. This operation has been defined as **Mode B** of the BCCD register. The conditions of difference of the full well potential to the surface potential as well as to the maximum of barrier channel potential of the adjacent wells are satisfied.

Operation with gate voltage swing; $\Delta V_G = V_g(+) - 0$ where zero biased gates form the barrier while the potential wells are created under the gates with positive voltage $V_g(+)$ is defined as **Mode C**. Adjusting the applied positive voltage V_g carefully, both conditions for maximum charge handling capacity can be satisfied. In this case, the maximum charge handling capacity is determined by the following condition :

$$\phi_{Full} \geq \{ \phi_{max}(0) + 20kT/q , \phi_{Surface} + 10kT/q \}. \qquad (4.3)$$

4.3 Charge Handling Capacity of the VHFR Imager

4.3.1 Effect of Short Channel Length on Charge Handling Capacity

The buried channel of 360x360-element VHFR image sensor was designed with a relatively short channel length of 1.5μm resulting in a smaller macropixel size. However, shorter channel lengths limit also the charge handling capacity of the BCCD register. To analyze the effect of shorter gate (channel) lengths on the charge handling capacity of the VHFR pixel memory elements per unit area, 2D simulations were performed by Pisces IIB. The doping profiles for this structure were imported from the 1D Suprem III analysis with assumption of a 0.7 lateral diffusion ratio. The charge handling capacity of the VHFR BCCD register has been studied for gate lengths varying from 1μm to 7μm. Edge effect has been included into the calculated results. Figure 4.8 and 4.9 show results of charge handling capacity per unit area for three different modes of operation and both low and high dose BCCD implant options, respectively.

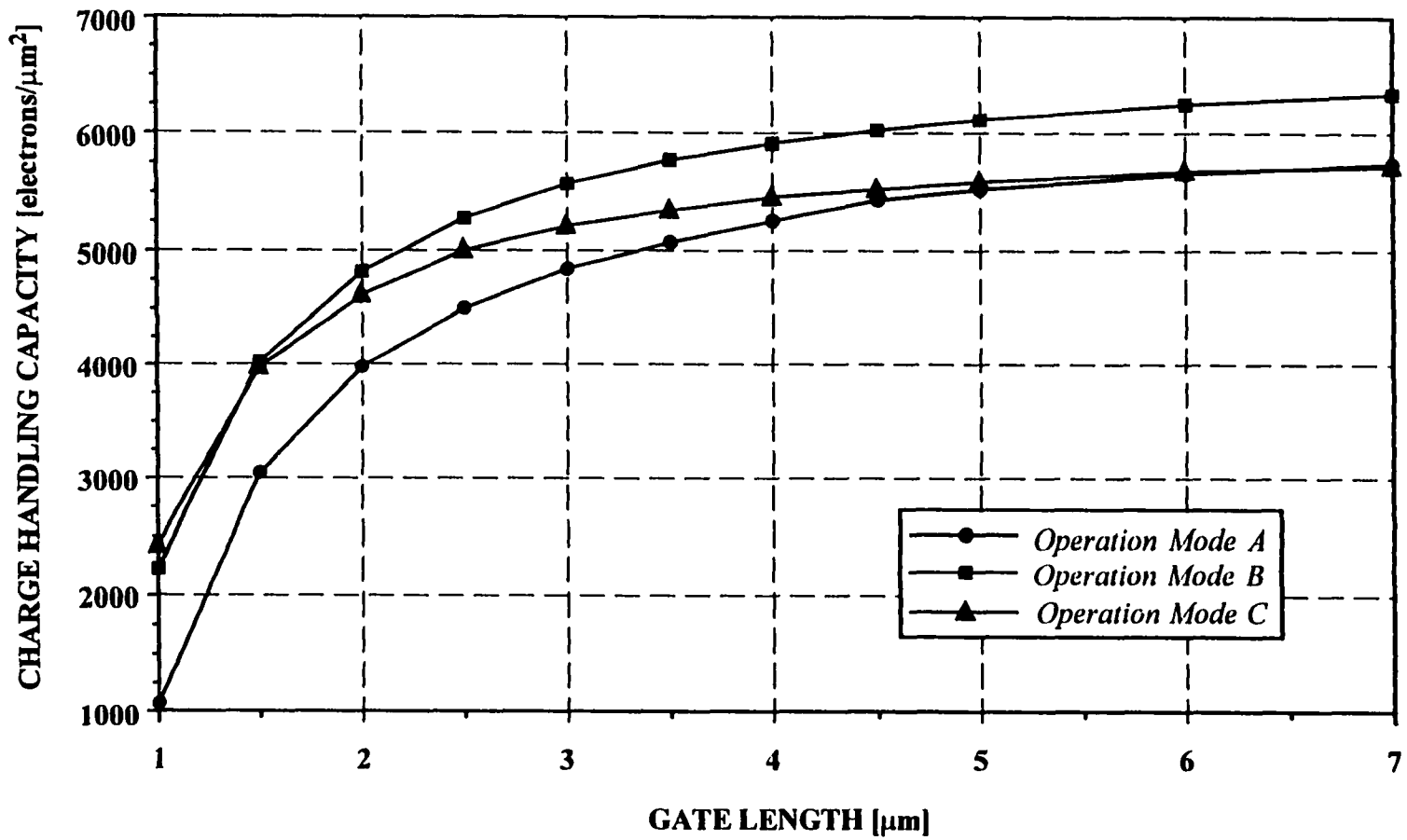


Figure 4.8 *Variation of charge handling capacity per unit area vs gate length for operation in three different modes (Mode A, B and C) performed for low dose BCCD implant option.*

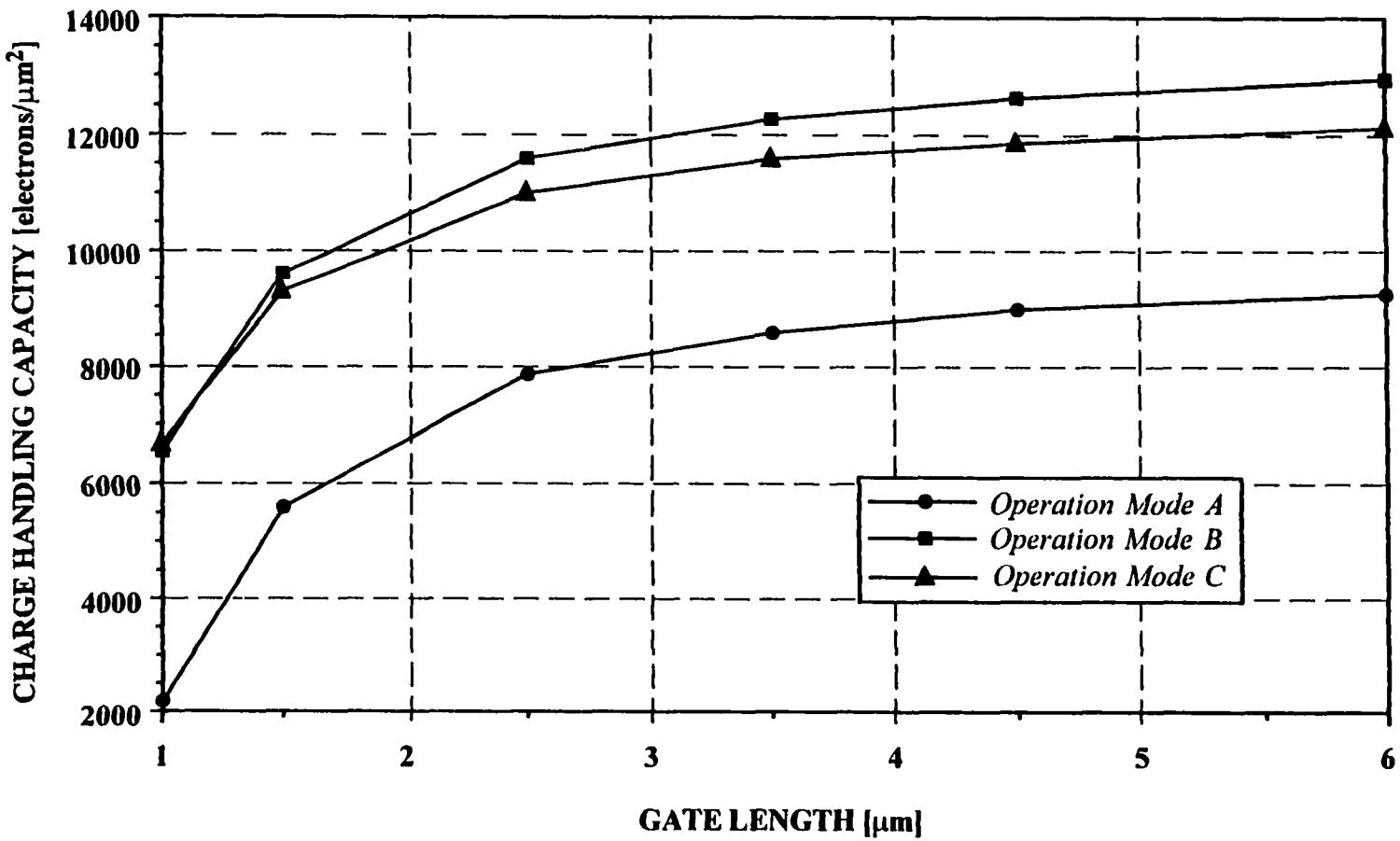


Figure 4.9 *Variation of charge handling capacity per unit area vs gate length for operation in three different modes (Mode A, B and C) performed for high dose BCCD implant option.*

As gate length increases the maximum signal charge that can be confined in the potential well reaches a saturation value Q_{max}. For low channel implant dose in Mode A, Q_{max} is obtained as 5750 electrons/μm^2, in Mode B 6350 electrons/μm^2, and in Mode C 5730 electrons/μm^2. However, as the channel gate length is reduced there is a significant decrease in Q_{max} due to the ***short channel length effect.***

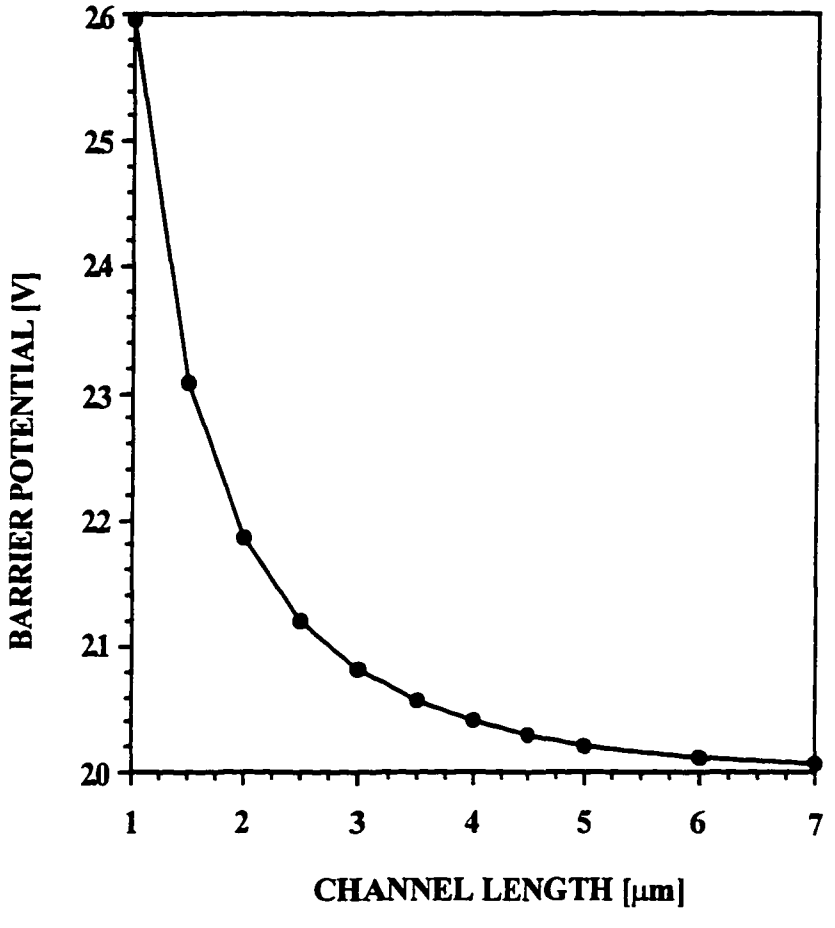


Figure 4.10 *Variation of barrier potential as function of channel length for low BCCD channel implant option in operation Mode B.*

Figure 4.10 illustrates the variation of barrier potential under pinning gate as function of channel gate length in operation Mode B for low dose BCCD implant option. For short gate lengths the barrier potential under pinning gate electrode next to the zero biased

gates remains at much higher values than it reaches as the gate length becomes longer. Same effect applies to the empty well potential in the opposite direction: For short channel lengths, the well potential under zero biased gate is less positive as it is for longer gates. Variation of the empty well potential with the channel length is illustrated in Figure 4.11.

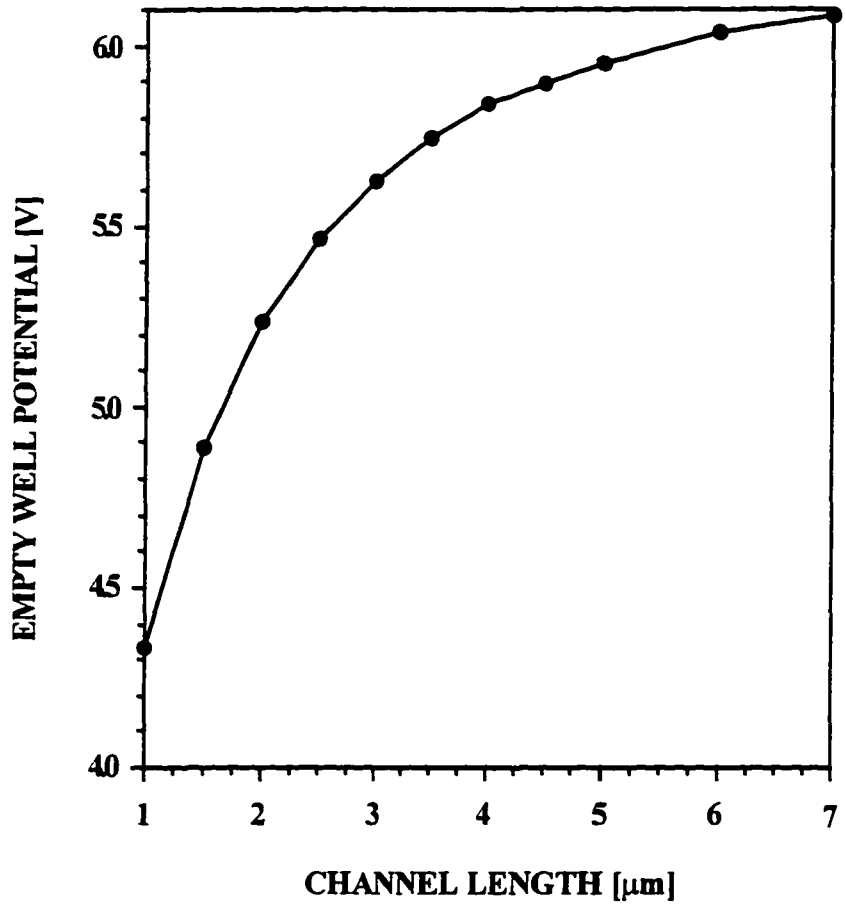


Figure 4.11 *Variation of empty well potential as function of channel length for low BCCD channel implant under zero biased gate electrode for operation Mode B.*

As a result, with increasing barrier potential and decreasing empty well potential deep potential wells cannot be achieved for shorter channel lengths. Figure 4.12 illustrates the depth of empty potential well under positively biased gate as function of channel length.

The effect of short channel length on potential profiles is demonstrated with results obtained in operation Mode B (optimum full well capacity) and for low dose BCCD implant option. However, same effect applies to all operation modes of the BCCD register. This can be seen in Figure 4.13 which illustrates the charge handling capacity per unit area vs gate length for both channel doping profiles and in all three operation modes of the BCCD register.

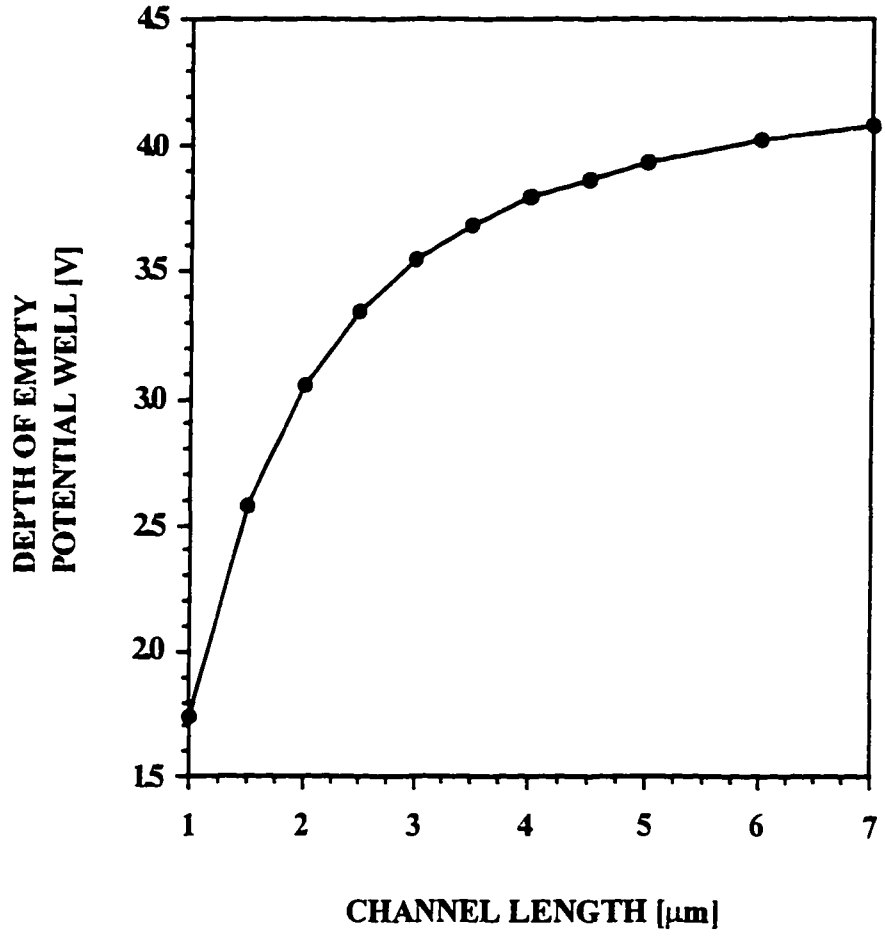


Figure 4.12 *Variation of depth of empty potential well potential as function of channel length for low BCCD channel implant under zero biased gate electrode for operation Mode B.*

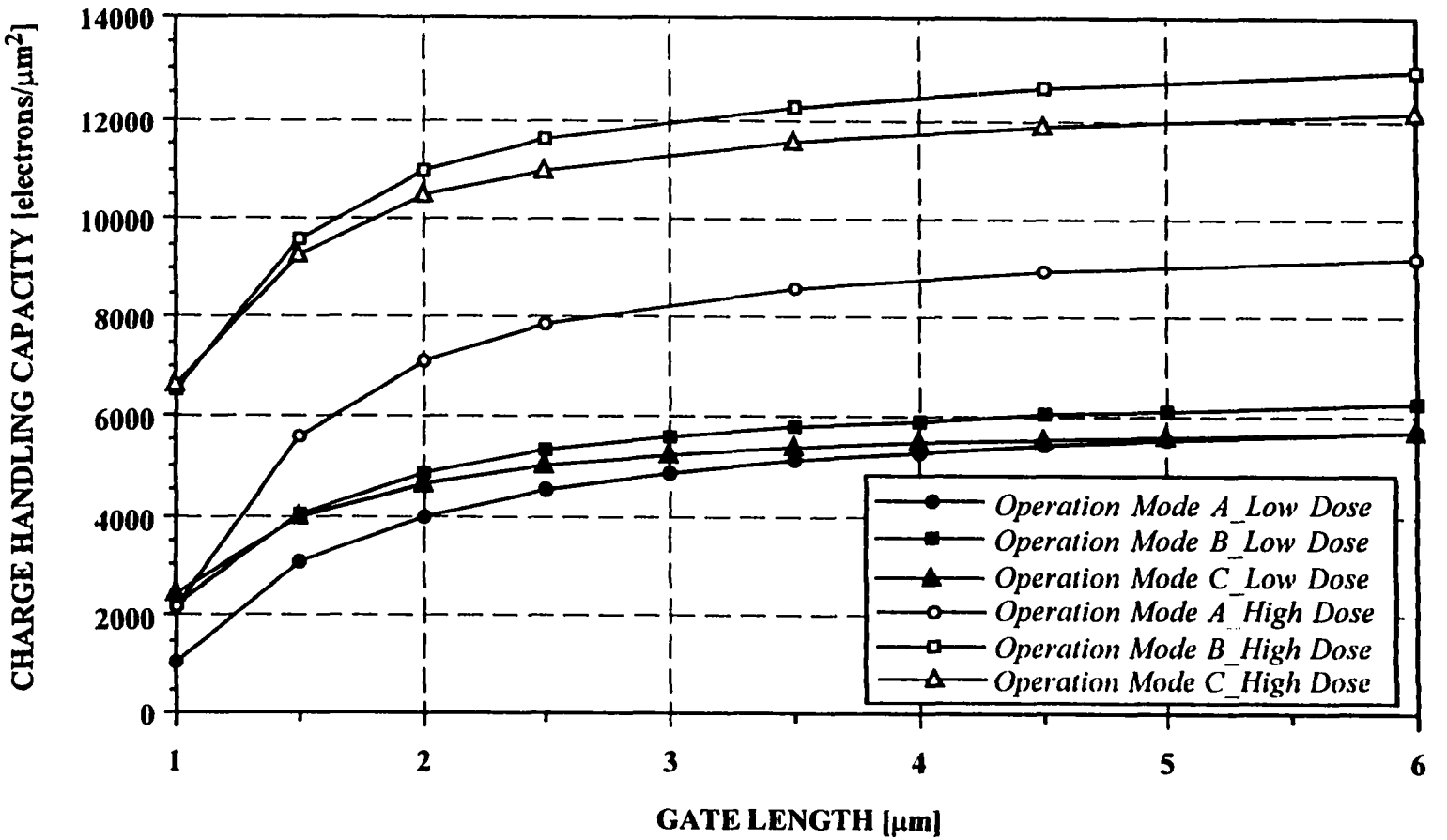


Figure 4.13 *Variation of charge handling capacity per unit area vs gate length for operation in three different modes (Mode A, B and C) performed for both buried channel doping profiles.*

4.3.2 Effect of Gate Dielectric Layer Thickness on Charge Handling Capacity

The effect of gate dielectric layer thickness on charge handling capacity has been studied for higher channel doping profile in operation Mode A. The actual gate length of 1.5μm was used for this simulation. 2D results show that the charge handling capacity per micron width in operation Mode A is reduced under gates with thinner channel dielectric layer as shown in Figure 4.14.

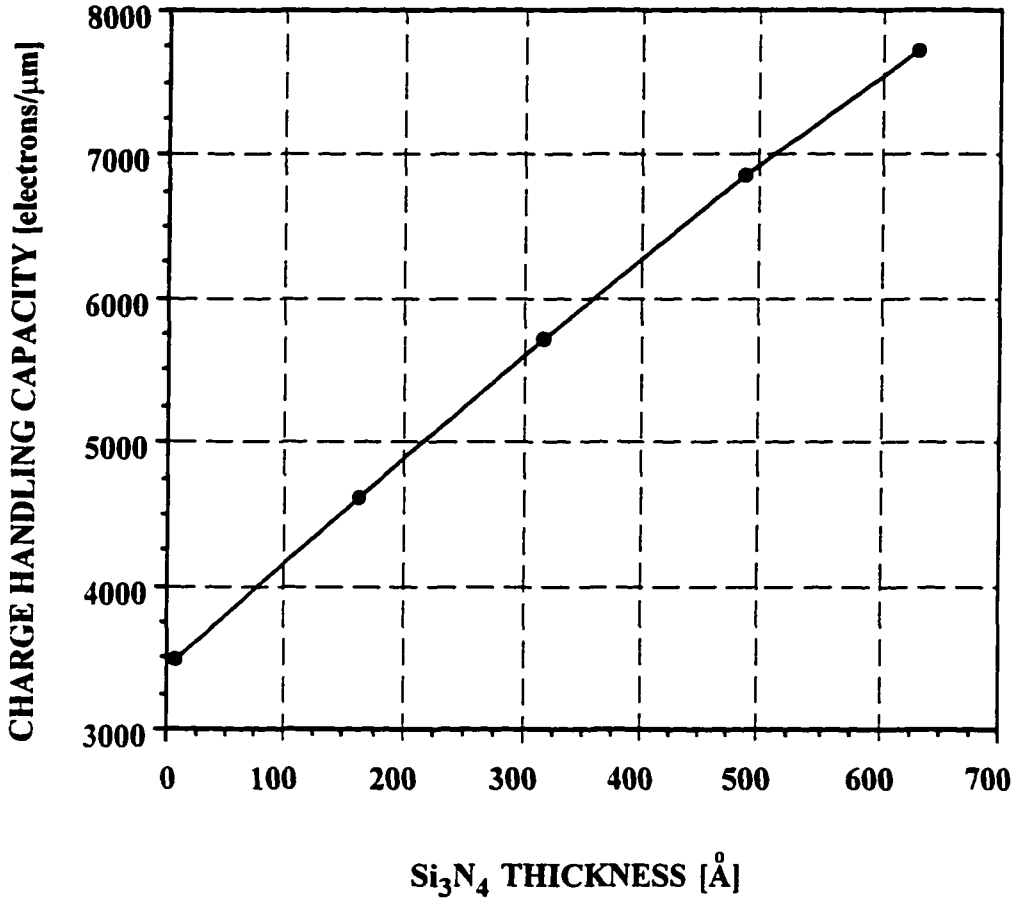


Figure 4.14 *Charge handling capacity per unit width as function of silicon nitride layer thickness in operation Mode A for high BCCD implant dose option.*

This result is also expected since the pinning gate voltage is shifted to more further positive voltages under gates with decreasing channel dielectric layer thickness. The

channel potential is shifted as well so that the depth of empty potential well reduces for operation Mode A with decreasing thickness of channel dielectric layer.

4.3.3 Measured Charge Handling Capacity of VHFR Imager

On the basis of minimum design rules of 1.5μm, the minimum size of the micropixel is 4.5μm^2. Results are available for high dose option of the BCCD channel implant and operation Mode A. The measured signal charge obtained during the operation of VHFR imager in Mode A is about 11000 electrons/pixel. Assuming that for the gates formed with poly-4 layer, the silicon nitride of channel dielectric was removed completely during imager fabrication steps, the charge handling capacity of the imager becomes limited by the charge handling capacity of the potential wells created under these gates even though the charge handling capacity of the gates with full thickness of channel dielectric is much higher. Comparing the simulated data with the measurement shows that under some gate electrodes most of the silicon nitride layer was removed after first polysilicon deposition while forming the remaining polysilicon gate electrodes. The measured value of charge handling capacity corresponds to about 100Å thickness of silicon nitride layer on 349Å channel oxide under poly-4 layer gate electrodes (Figure 4.14). Therefore, the charge handling capacity of the VHFR imager is mainly determined by the charge handling capacity of potential wells under these gate electrodes.

4.3.4 Simulation Approach

Figure 4.15 illustrates the 2D device of five serial gate electrodes defined for calculation of charge handling capacity and the simulation approach in order to account for fringing field of the adjacent gate voltages. The available version of Pisces IIB has the capability of introducing charge into the device by photogeneration. An other method of introducing charge into the potential wells is to artificially set the quasi-fermi level of electrons and find the steady-state solution.

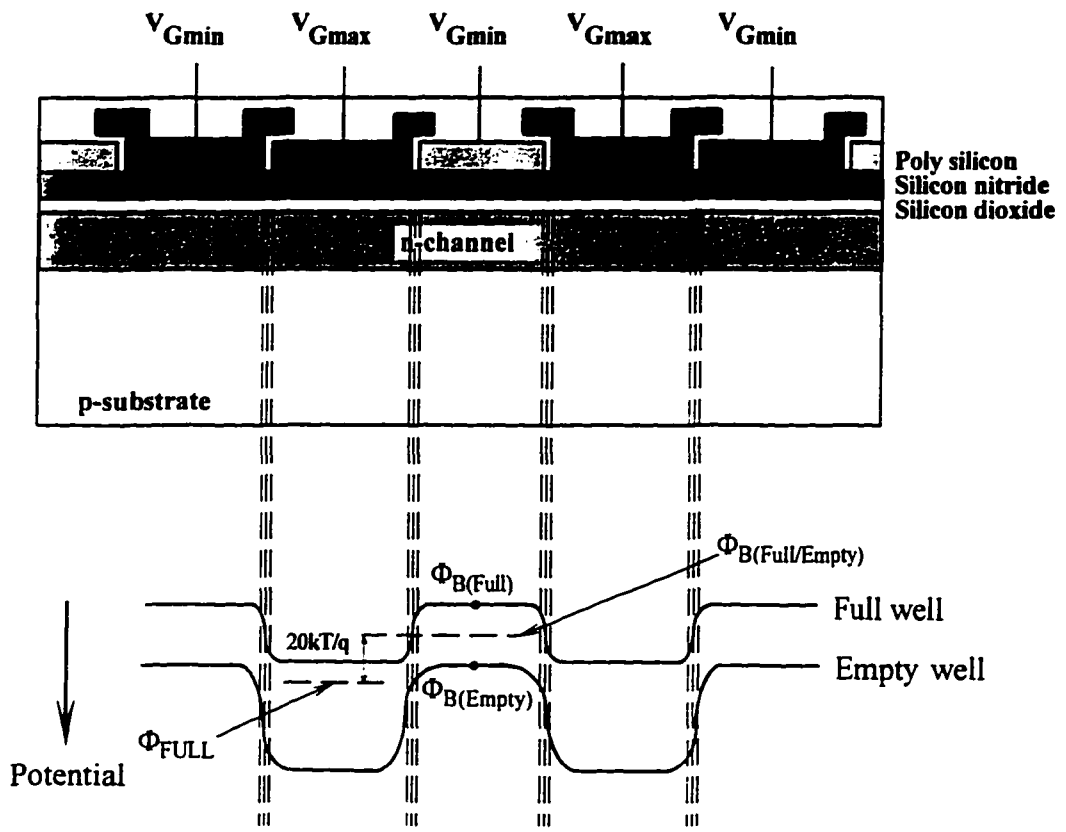


Figure 4.15 *Simulation approach in order to account for fringing field of the adjacent gate voltages.*

Both methods suffer from the limitation that the area of introducing charge cannot be specified throughout the device and the whole device is solved for the desired condition. The gates with an applied voltage V_{Gmax} form the potential wells whereas the gates with applied voltage V_{Gmin} create potential barriers. The oxide thickness between gate electrodes was obtained as 1400Å by 1D and 2D process simulations. By adjusting the quasi-fermi level of electrons to a sufficiently high value, the n-channel can be completely depleted of majority carriers and the empty well potentials next to the barrier gates can be calculated. The amount of charge can be controlled by varying the quasi-

fermi level appropriately and the Poisson equation is solved to obtain the potential profile and carrier distribution. Full well potential and the corresponding electron concentration can be calculated as defined by equations (4.2) and (4.3). However, the current version of Pisces IIB cannot solve the condition where a full well is separated from an empty well by a barrier potential and the effect of fringing field caused by adjacent gate voltages cannot be included directly into the simulation.

Therefore a simulation approach was developed in collaboration with Guang Yang [2] in order to account for fringing fields caused by the adjacent gate voltages :

- A potential profile of two full wells separated by a barrier potential $\phi_{B(Full)}$ was calculated.
- A potential profile of two empty wells separated by a barrier potential $\phi_{B(Empty)}$ was calculated.
- $\phi_{B(Full/Empty)}$ was estimated to be in the middle of the both barrier levels and expressed by the following equation :

$$\phi_{B(Full/Empty)} = \frac{1}{2}[\phi_{B(Empty)} - \phi_{B(Full)}] + \phi_{B(Full)}. \qquad (4.4)$$

- Charge handling capacity is recalculated by a 20kT/q difference between the new barrier potential and the full well potential.

$$\phi_{FULL} \geq \phi_{B(Full/Empty)} + 20kT/q. \qquad (4.5)$$

The results obtained with and without the proposed simulation approach are presented in Figures 4.16 and 4.17 for low and high BCCD implant dose options respectively. In these figures operation Mode A, B and C represent the charge handling capacity obtained without including the fringing field effect of the adjacent storage gate voltages. Operation

Mode A', B' and C' represent the results obtained after applying the described simulation approach.

The average time to solve for charge handling capacity of a particular channel length without using the described simulation approach takes a few hours, which includes the computation time and several iterations performed by the user to fulfill the constraints (4.2) and (4.3). In this case the solution can be obtained only for two full potential wells which are separated by a barrier gate.

The computational time and effort increases significantly with the required number of iterations if the above described simulation procedure is followed. The effect of proposed approach in charge handling capacity becomes more dominant especially with shorter channel lengths. The difference is about 20% for minimum gate length of 1.0μm, and 15% for 1.5μm. Results were obtained by convergence up to the 3rd decimal for both cases.

Other results obtained while simulating the charge handling capacity of the BCCD register are the quasi-fermi levels of electrons for each channel length at operating in all defined modes of the BCCD register and the gate voltages that have to be applied to store the charge packet operating in both modes; Mode B and Mode C. These results were obtained for low and high BCCD implant dose options; for gate lengths varying from 1μm to 7μm for low BCCD implant dose and for gate lengths varying from 1μm to 6μm for high BCCD implant dose. The values of quasi-fermi level and gate voltage for all operation modes and for each gate length are necessary for further analysis of the BCCD register, especially for analysis of the channel-stop regions. The obtained data is used as input to demonstrate the performance of the channel-stop region and to determine the channel-stop width for safe operation of the BCCD register.

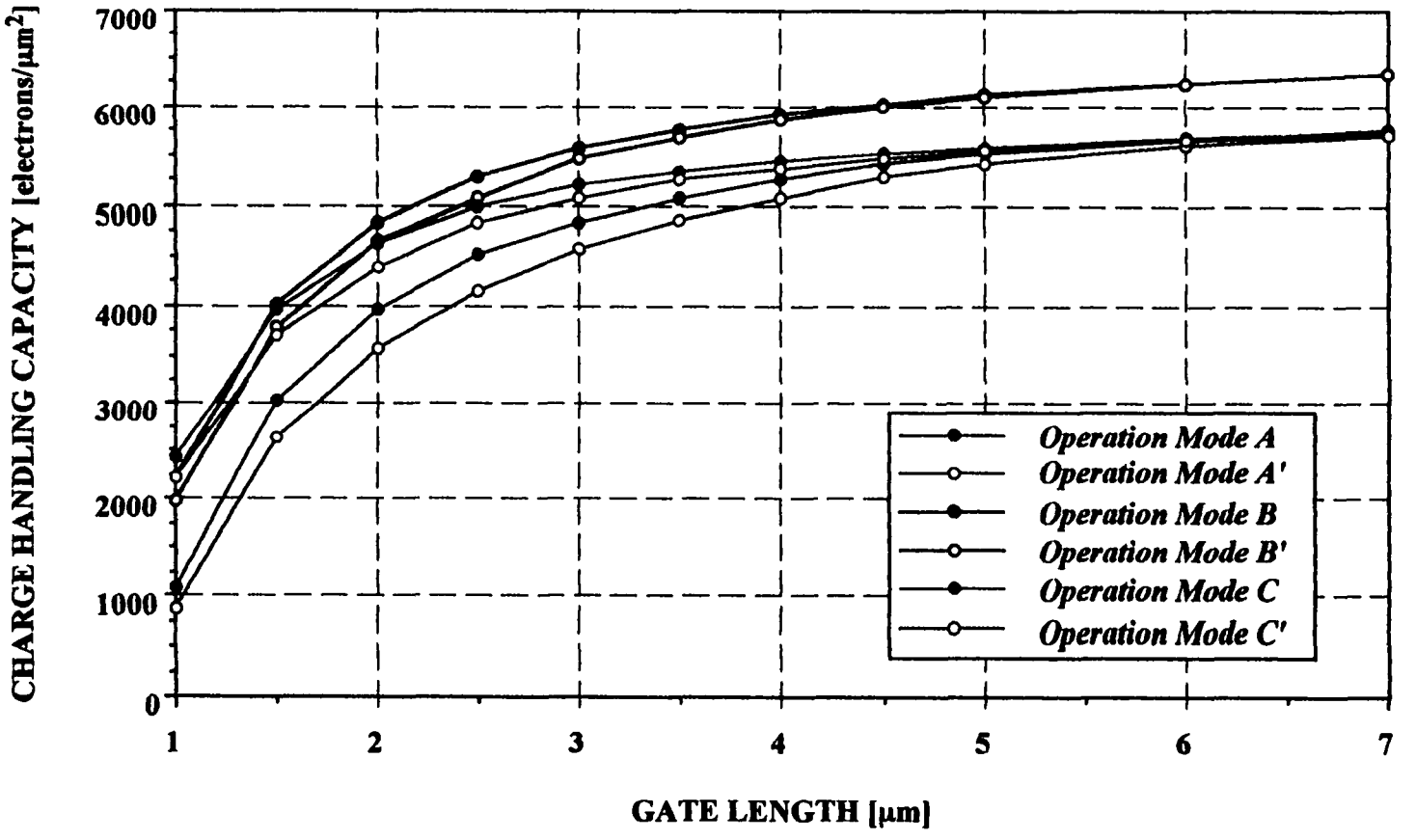


Figure 4.16 *Comparison of the results obtained by two different procedures of simulation for low dose BCCD implant option.*

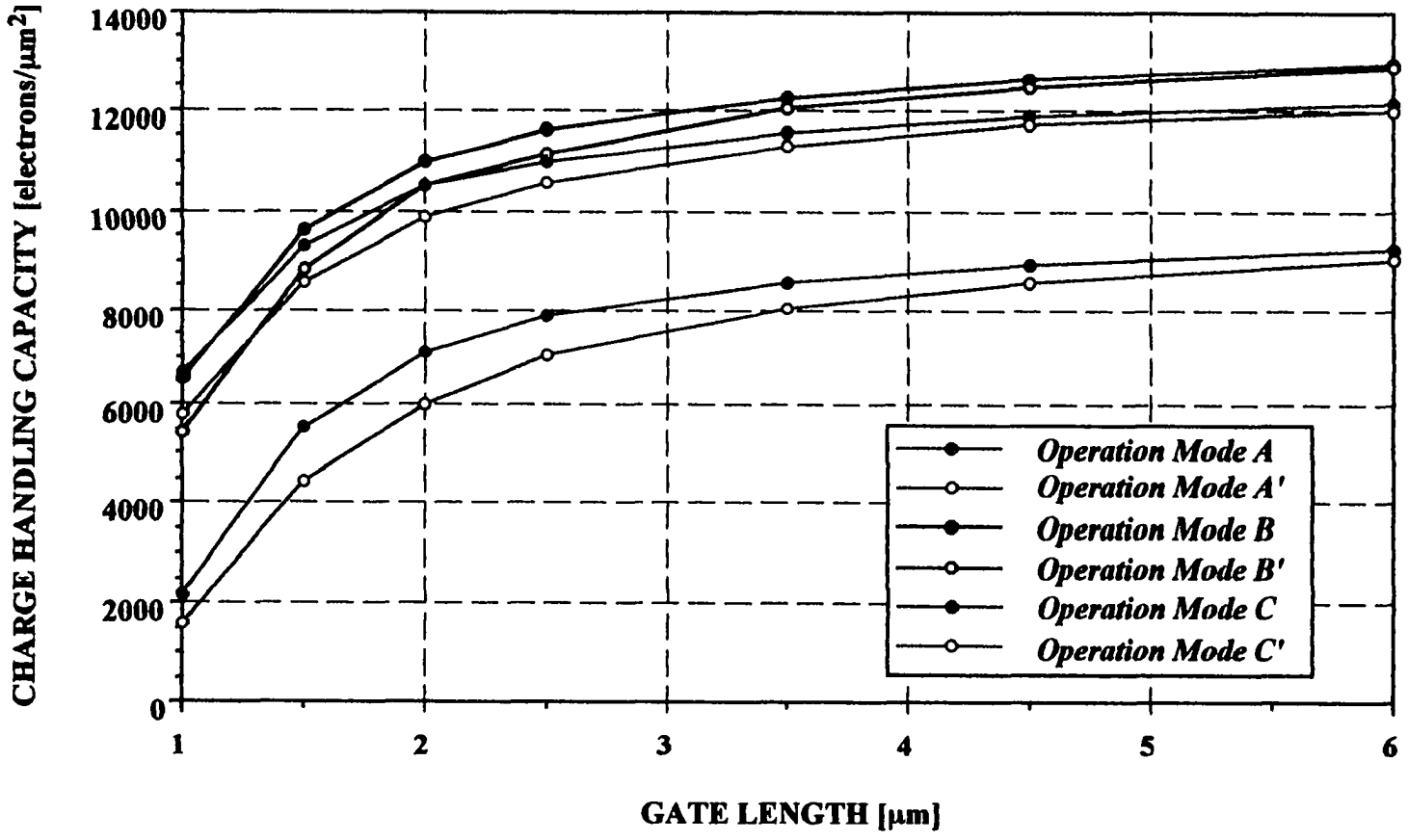


Figure 4.17 *Comparison of the results obtained by two different procedures of simulation for high dose BCCD implant option.*

4.4 Channel-Stop Region

The results obtained for simulation of the full well capacity of the BCCD register for both buried channel doping profiles were used to determine the performance of the channel-stop region. For safe operation of the BCCD register, the nominal width of the channel-stop region was determined as 2.5μm. Figure 4.18 illustrates the potential profile of two full wells which are separated by the channel-stop region. The potential of the channel-stop acts as barrier between the two full-wells and ensures that charge packets are kept separated in adjacent potential wells. In this figure, the width of the n-channel is 3.0μm. Figure 4.19 illustrates the electron concentration in the potential wells separated by the 2.5μm channel stop region.

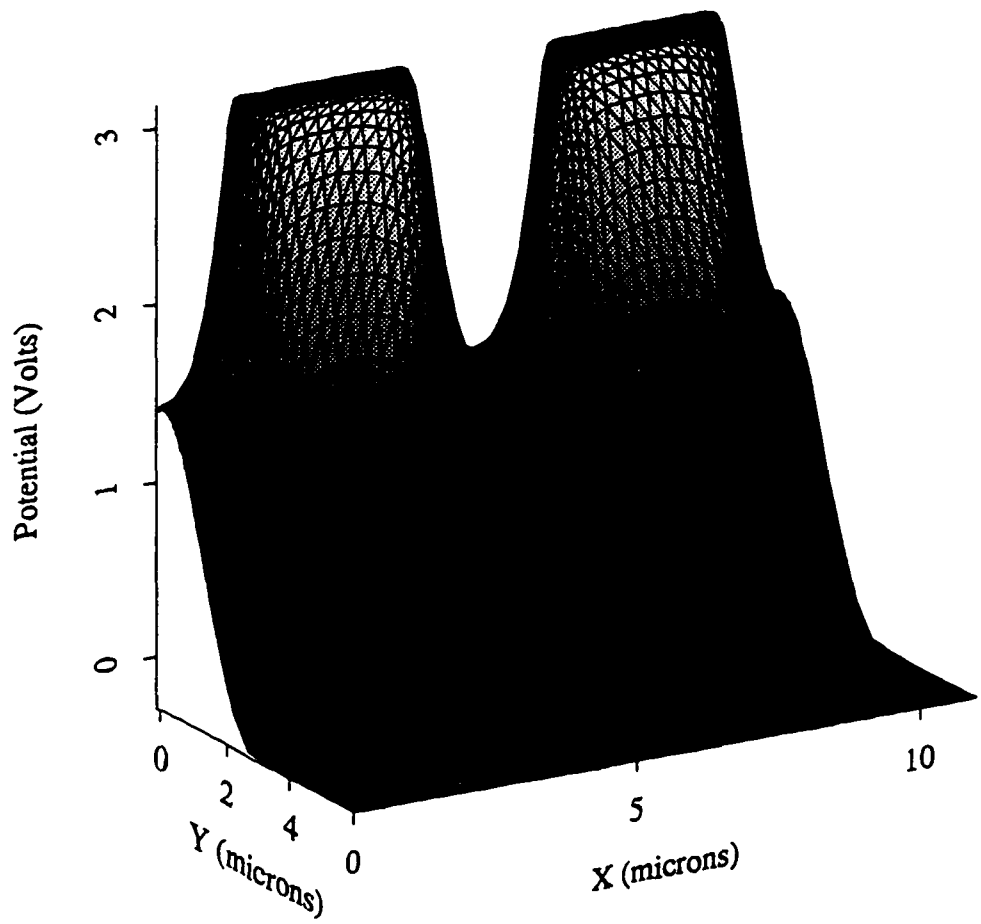


Figure 4.18 *Potential profile of two full wells separated by 2.5μm channel-stop.*

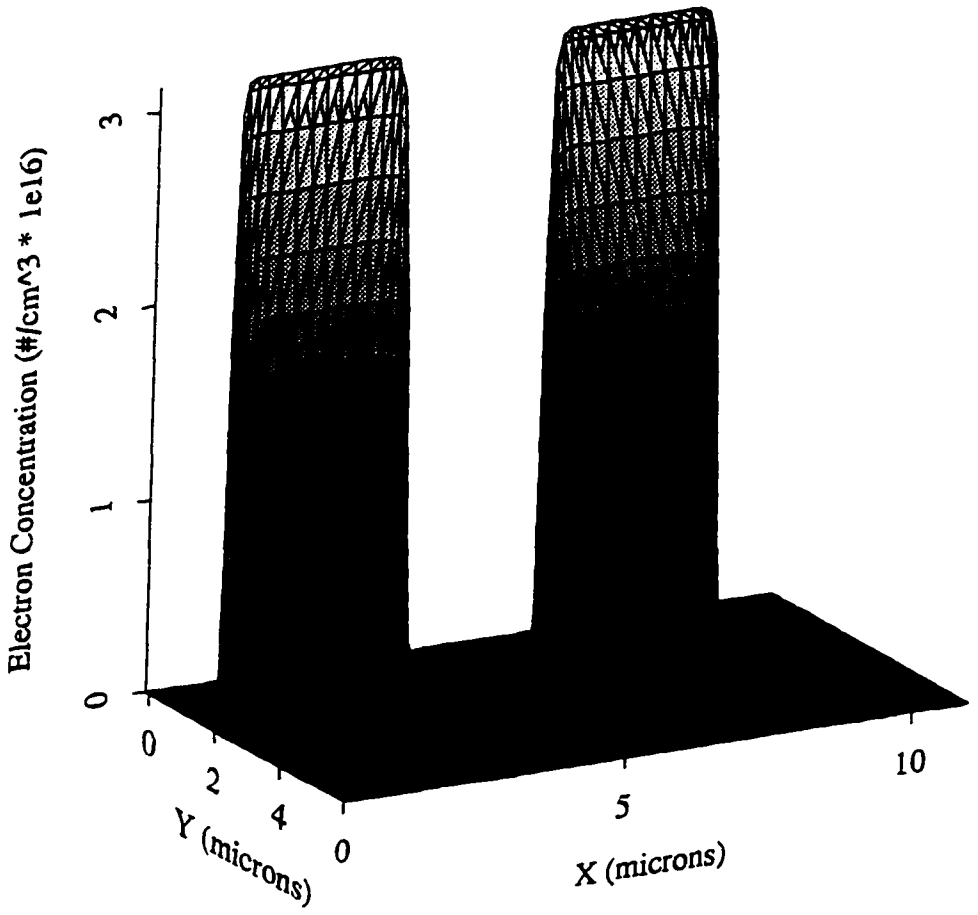


Figure 4.19 *Electron concentration in potential wells separated by 2.5μm channel-stop.*

4.4.1 Simulation Approach

The channel-stop region is made of p-substrate with no additional implants. The 2D structure used for simulations is illustrated in Figure 4.20. The barrier potential across the channel-stop was simulated using Pisces IIB for both low and high dose BCCD implant options. The structure was defined by exporting the doping profile of each different region using Suprem III output. Simulations were performed for channel-stop widths varying from 0.75μm to 2.5μm with 0.25μm increments. The channel-stop width is marked as W in Figure 4.20 and which is the nominal width of the channel stop region defined by the implant mask.

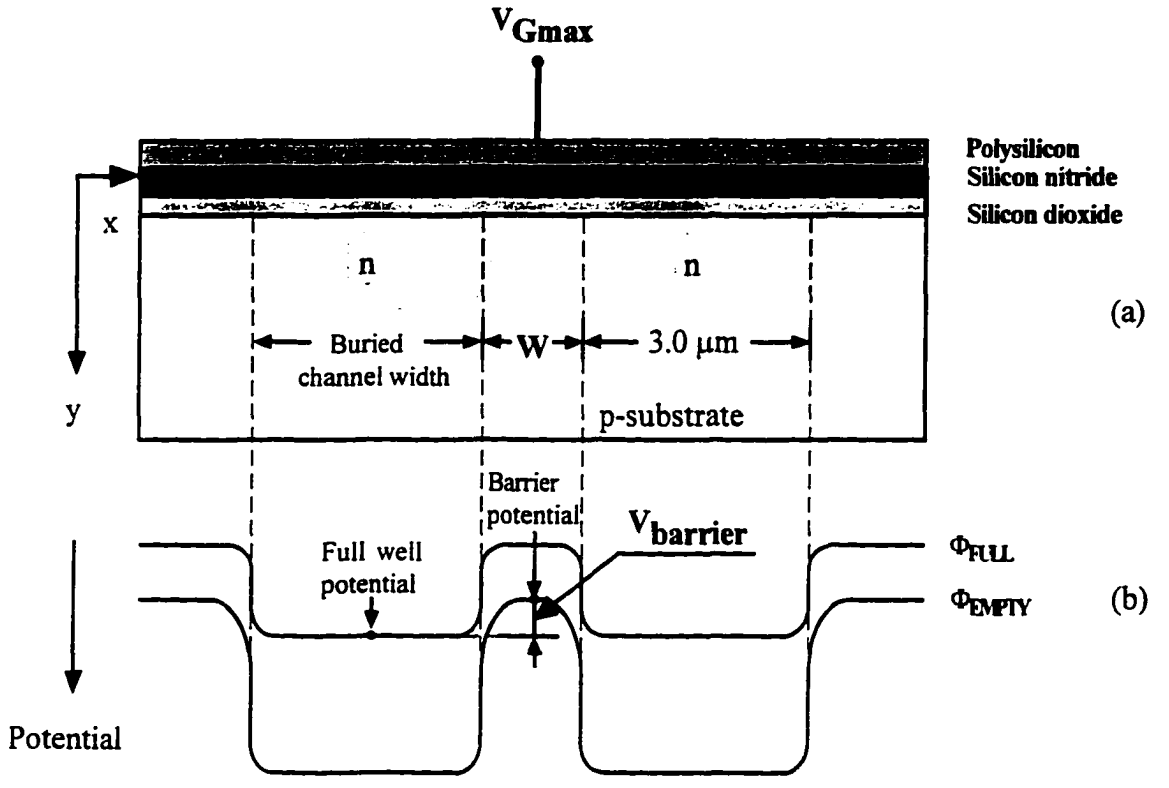


Figure 4.20 *Simulation approach to obtain the barrier potential across the channel-stop region. (a) 2D structure defined by Pisces IIB. (b) Potential profile.*

Simulating the 2D structure by applying a highly positive quasi-fermi level for electrons provide the steady-state solution of two empty potential wells separated by the channel-stop region and is marked as Φ_{EMPTY} in Figure 4.20. A second simulation has to be performed to obtain full-well condition of the same structure which corresponds to the potential profile along x-axis and is marked as Φ_{FULL}. Inspection of Figure 4.20 clearly shows that the critical barrier height to confine the charge packet in the BCCD register is the voltage difference between the full well potential of Φ_{FULL} and the barrier potential of Φ_{EMPTY} . This difference is marked as $V_{barrier}$ and obtained through the simulations for both channel doping profiles with varying channel-stop widths.

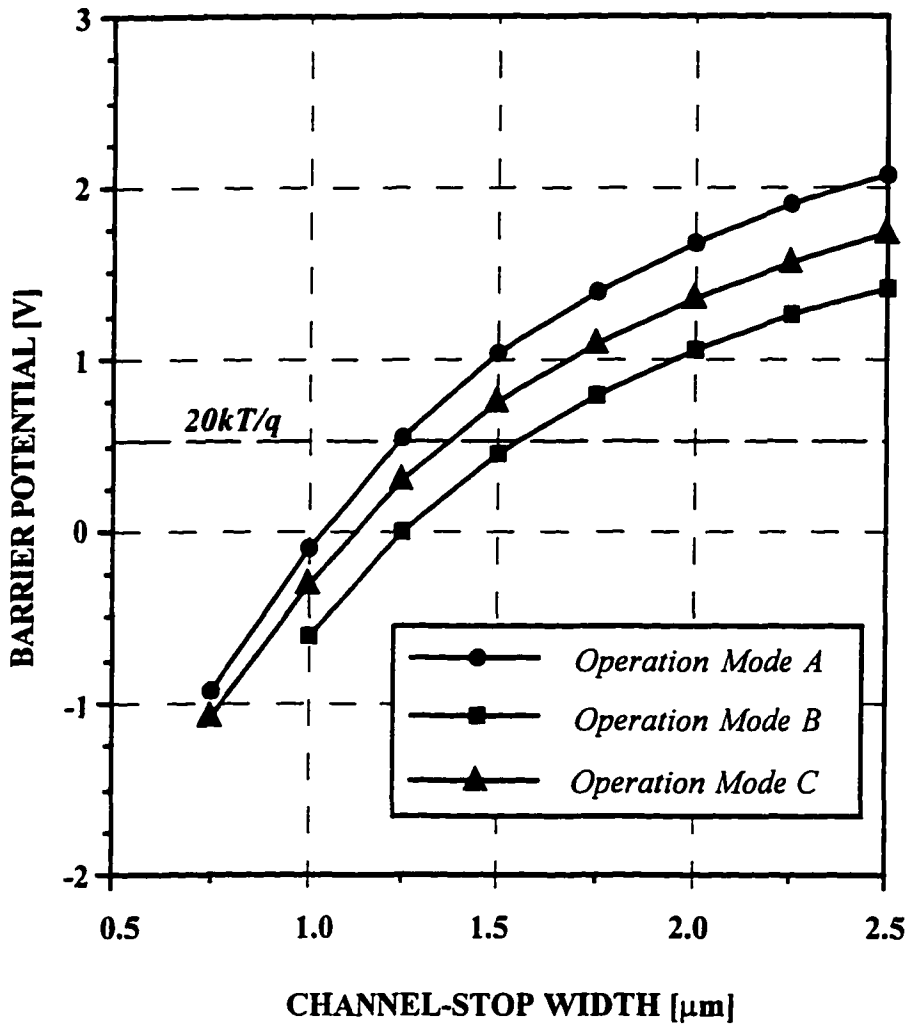


Figure 4.21 *Channel-stop barrier height for three different modes of operation simulated with low dose BCCD implant option.*

4.4.2 Simulation Results

Channel-stop barrier potential vs channel-stop width are demonstrated in Figures 4.21 and 4.22 for low and high dose BCCD implant options, respectively. Solutions were obtained corresponding to all three different operation modes of the BCCD register.

To confine and transfer the charge packet in the BCCD register safely the barrier height provided by the channel-stop region has to be minimum 20kT/q. Considering all possible modes of operating the BCCD register, operation Mode B determines the

minimum width of the channel stop for low channel doping profile and requires a minimum of 1.75μm channel-stop width. Since Mode B is the operation mode with optimum full well capacity, this result is also expected. Inspection of Figure 4.22 shows that there is significantly higher amount of charge confined in the buried channel in operation Modes B and C compared to operation Mode A. Mode B carries the highest amount of charge signal and according to the results obtained for operation Mode B, the minimum width of the channel-stop region has to be 2.0μm or wider.

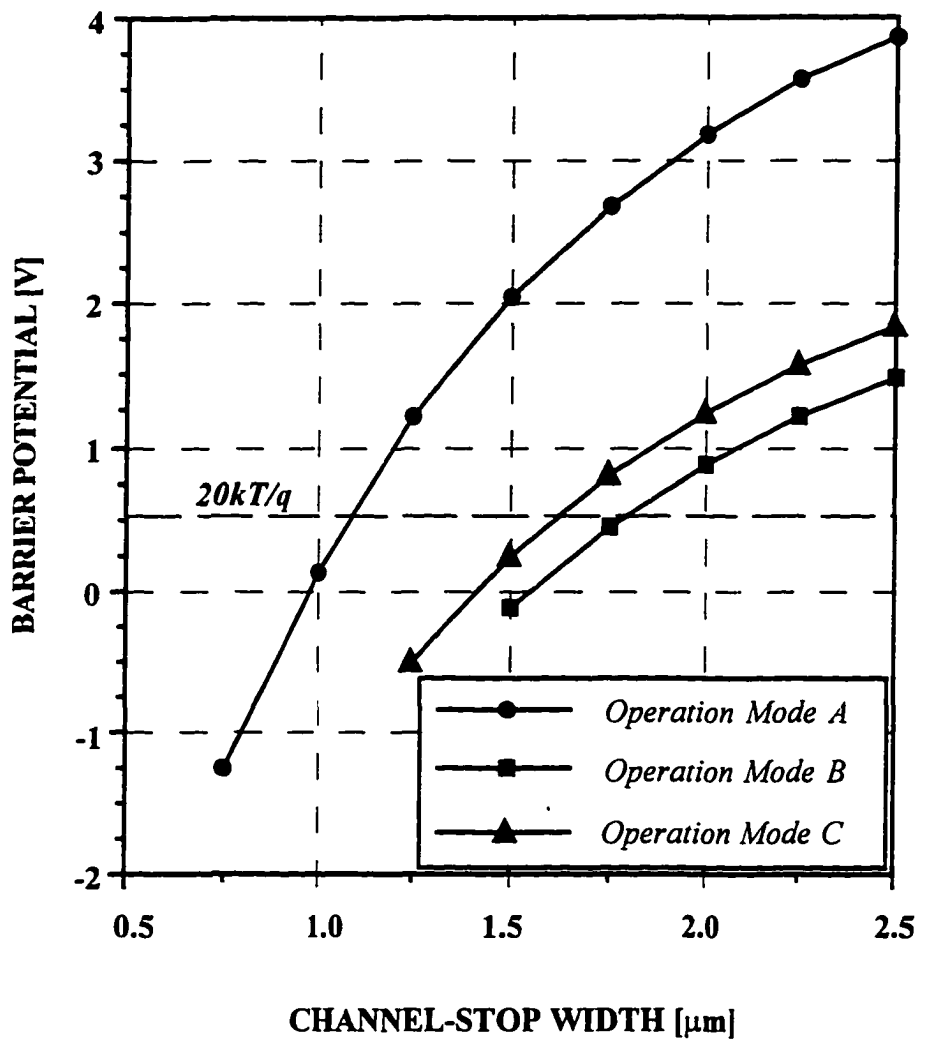


Figure 4.22 *Channel-stop barrier height for three different modes of operation simulated with high dose BCCD implant option.*

CHAPTER 5

PHOTODETECTOR DESIGN FOR OPERATION WITH 100NS FRAME TIME

5.1 Introduction

To increase the charge transfer speed for very high frame rate and essentially zero lag operation, the photodetector was designed with a graded doping by means of multiple implants. The photodetector is a virtual-phase [23] buried structure with multiple n-type detector implants in addition to a thin p^+ and the regular buried channel (BCCD) implants. Each macropixel is constructed by a photodetector adjacent to a BCCD type analog memory register. The size of the photodetector for 360 x 360-element VHFR imager consisting of 50μm x 50μm macropixels is approximately 30μm x 11μm which corresponds to a fill factor of 13.5% .

5.2 Design and Operation of the Photodetector

The top view of the photodetector with the BCCD charge read-out structure of the 360x360-element VHFR burst imager is illustrated in Figure 5.1 The cut-line A-A' represents the longest charge transfer distance in the photodetector. The fabrication of the photodetector includes the n-channel dual BCCD implants which are performed before the deposition and definition of the polysilicon gates. The photodetector employs three additional n-type implants which are self-aligned to the polysilicon layer of the charge collecting gate electrode G_1. This is followed by a shallow p-type implant to form the pinned-buried detector structure. The photodetector is surrounded by p^+ - field implant. The cross-sectional view across the horizontal cut-line B-B' was obtained by 2D process simulation using ISE-TCAD package and is illustrated in Figure 5.2. The graded potential profile along the photodetector is created by the variation of the doping concentration in the photodetector and the resulting fringing field. The differently doped n-regions can be recognized easily by the increasing junction depth into the p-substrate.

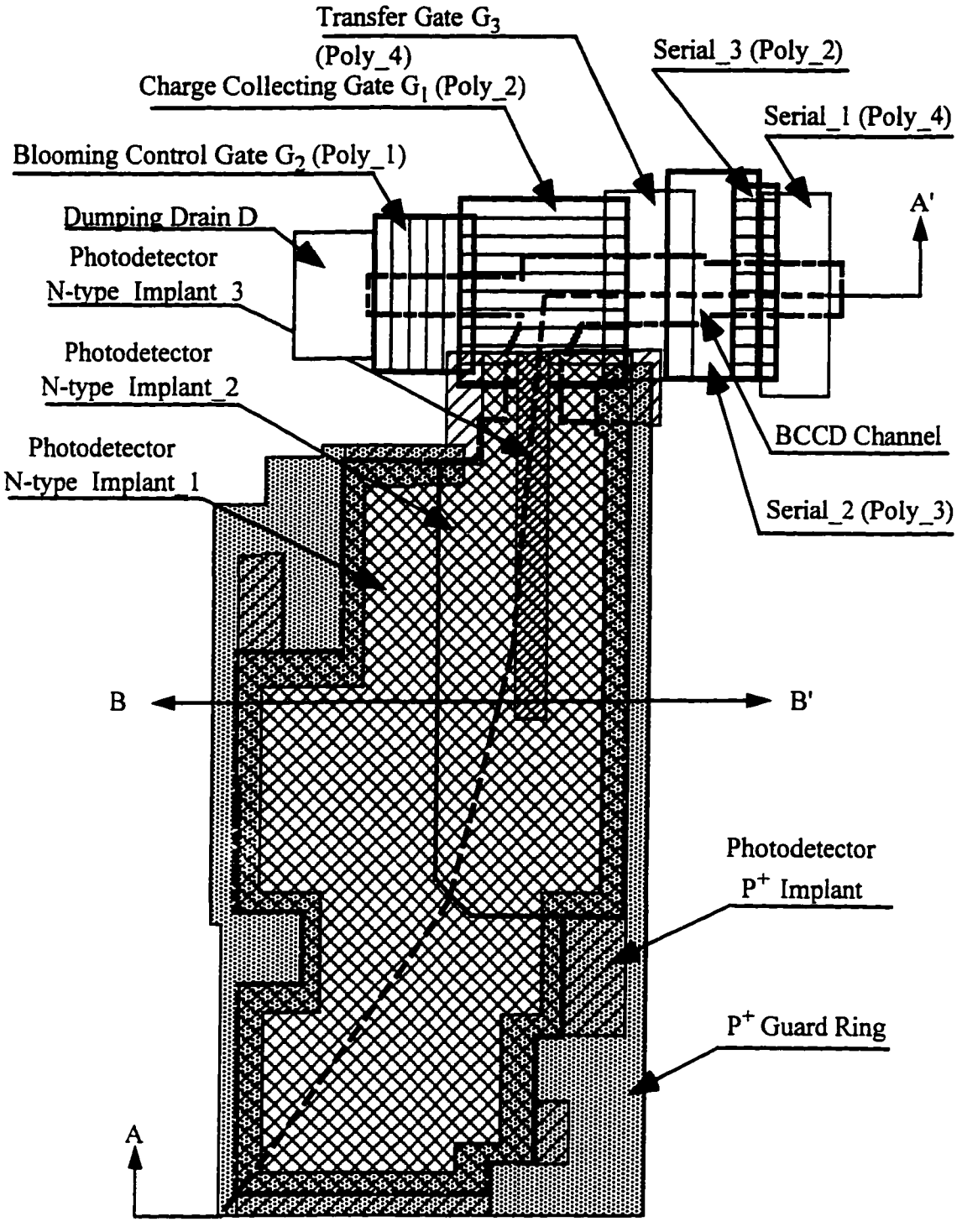


Figure 5.1 *Layout of the multi-implant (graded) pinned-buried high-speed photodetector.*

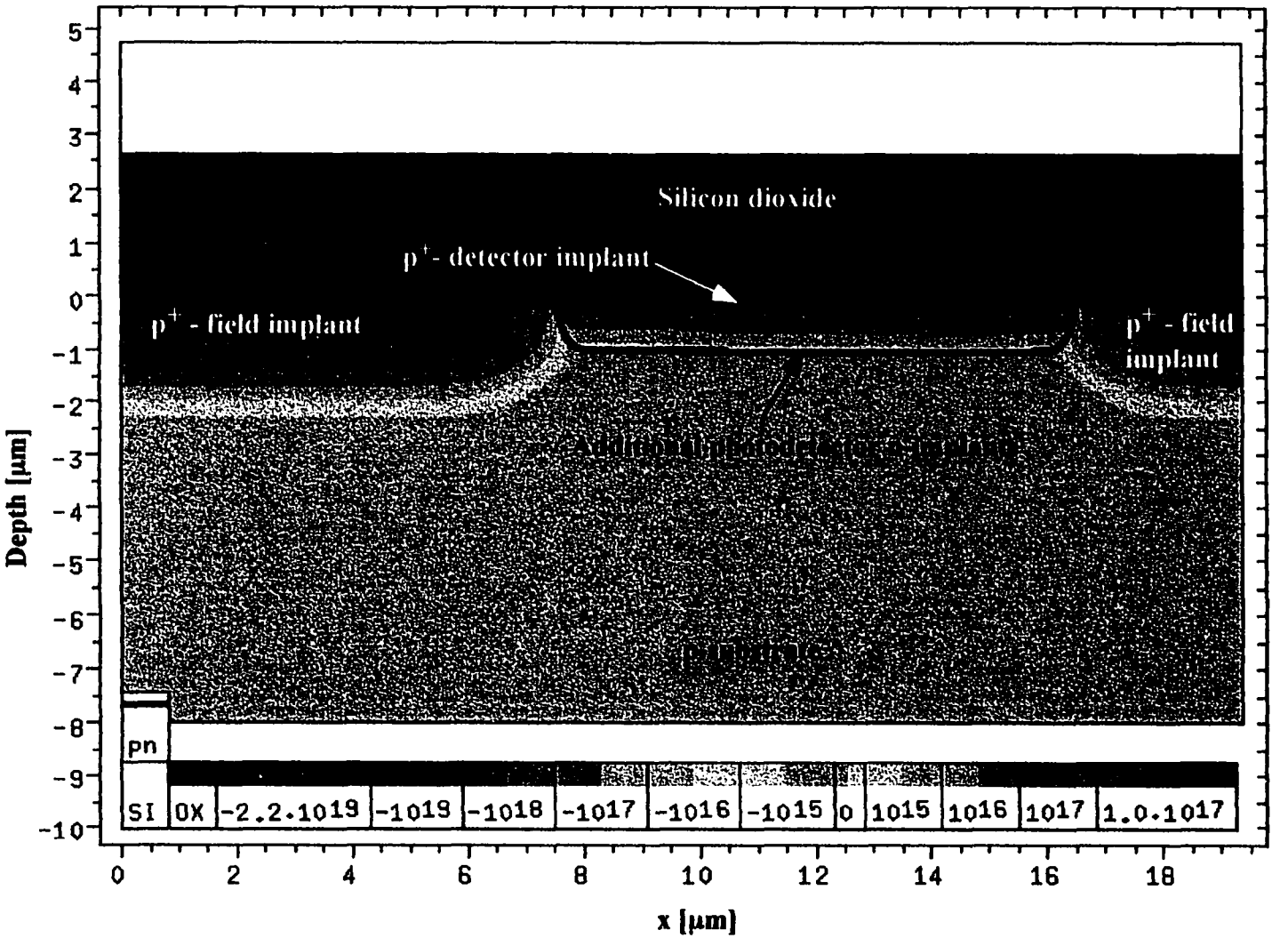


Figure 5.2 *Cross-sectional view simulated by ISE-TCAD across the cut-line B-B'.*

The construction and operation of the multi-implant pinned-buried photodetector and the BCCD readout was expected as sketched in Figure 5.3, showing a cross-sectional view along the cut-line A-A' in (a) and the corresponding potential profile in (b). The high-speed photodetector was designed to have a potential difference between each implant step $\Delta\Phi_1$, $\Delta\Phi_2$ and $\Delta\Phi_3$ of approximately 0.5V. The values of the photodetector implants were selected on the bases of 2D device simulation along the cut-line A-A' by Pisces IIB. (P: $1.4\text{x}10^{12}\text{cm}^{-2}$, $1.2\text{x}10^{12}\text{cm}^{-2}$, $1.0\text{x}10^{12}\text{cm}^{-2}$, 120keV)

The resulting stair-case potential profile breaks up the photodetector structure into three regions with equal length where region-2 acts as a charge sink for region-1, and region-3 acts as a charge sink for region-2. Finally, the potential well under the charge collecting gate G_1 acts as a charge sink for the charge collected by the photodetector during the optical integration time. In this architecture, G_2 is placed between the drain D and gate G_1 to be used for horizontal blooming control. G_3 is the transfer gate that separates the charge collecting well from the serial-parallel SP BCCD register.

At the end of the optical integration time, the charge signal accumulated in the charge collecting well is transferred to the BCCD register for temporary storage during the charge collection cycle of the imager operation. In other words, the charge signal detected by the photodetector is continuously accumulated in the charge collecting well that is periodically emptied into the BCCD serial-parallel SP readout register. The charge collection can be stopped at any time preceding the loading of the serial-parallel register from the photodetector. Last N frames corresponding to the number of BCCD registers will be temporarily stored in the macropixel.

During image readout period of the VHFR imager operation, the BCCD registers are formed into a single full frame type CCD through manipulating the charge transfer by changing the clocking of gate electrodes. The image collection is stopped and the photogenerated signal detected by the photodetector is transferred (drained) directly to the blooming drain D.

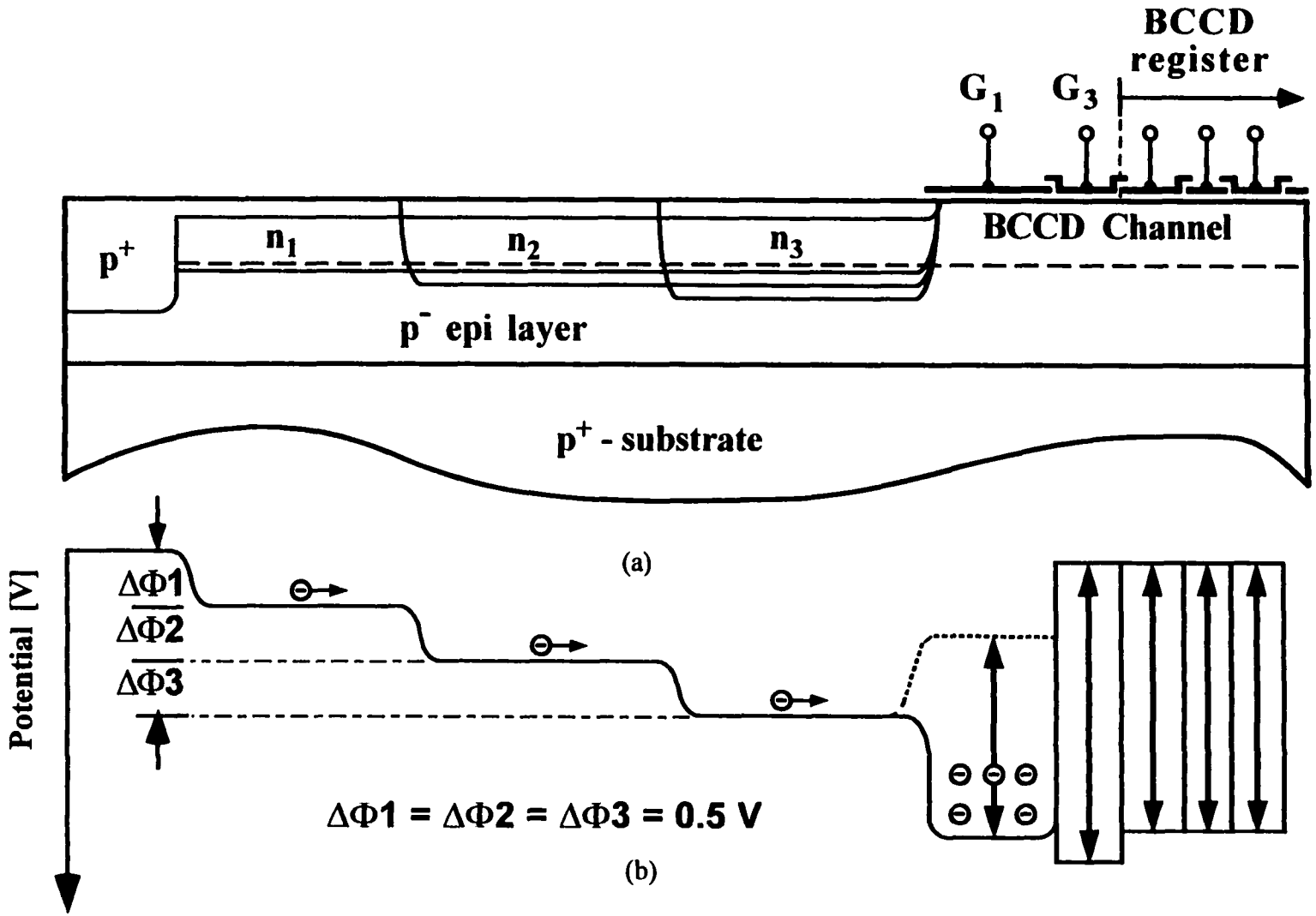


Figure 5.3 *Sketched view at the cross-section AA' illustrating photodetector doping profile in (a) and the corresponding potential distribution in (b).*

A frame time of about 10^6 frames/s had already been demonstrated with the existing design. However, the imager had to be operated with a mechanical shutter and there was a large leakage of electrons from the photodetector into the serial-parallel SP register. Therefore, expected readout operation as described in the discussion above and as sketched in Figure 5.3 is simulated by the author using Pisces IIB and results are presented in the following sections of this chapter. The research on photodetector readout operation demonstrates an important design error at the photodetector charge readout which explains the observed charge leakage from the photodetector into the serial-parallel SP BCCD register and clearly affects the readout operation of the existing imager. A corrected photodetector structure was designed by the author using simulation and will be presented below.

5.3 The Graded Potential Profile

5.3.1 Simulation Approach

The initial step of simulating the performance of the photodetector readout operation for very high frame rate imaging applications was to analyze the stair-case potential profile obtained employing multiple n-type implants. The 2D structure generated for device simulation using Pisces IIB is shown in Figure 5.4. The doping profiles of different regions were imported from 1D process simulation results using Suprem III with 0.7 lateral diffusion ratio. In this analysis, a photodetector structure constructed by 3 - 14μm long n-type detector regions (marked as n_1, n_2 and n_3) and a shallow p^+- detector implant in addition to the regular n-type dual buried channel implants was employed. The described photodetector is surrounded by 2μm long p^+- field implant regions. The total length of the 2D structure is 46μm. In order to obtain the stair-case potential profile, the multiple n-implant regions have to be depleted of electrons. This condition can be accomplished by adjusting the electron quasi-fermi level to a sufficiently high value and setting the hole quasi-fermi level to 0V.

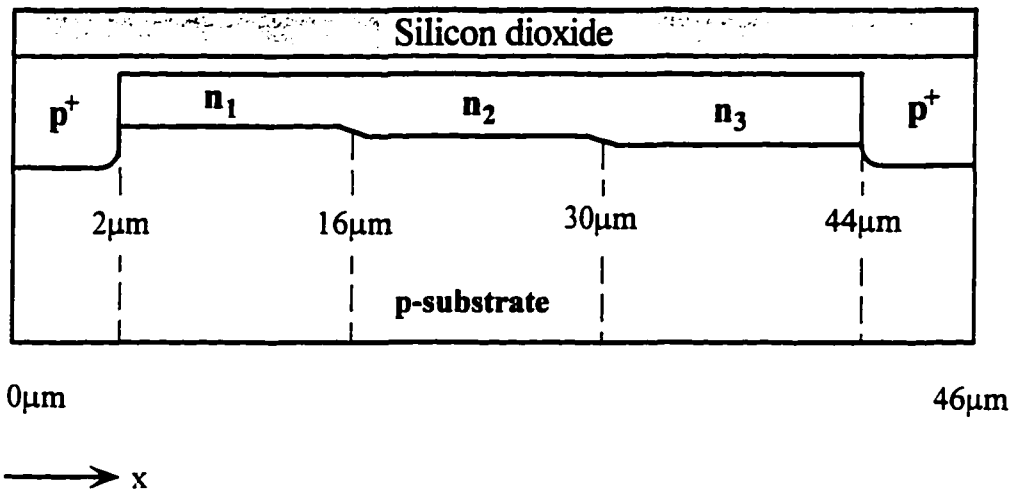


Figure 5.4 *Photodetector structure generated for 2D device simulation of stair-case potential profile.*

The result obtained by solving the Poisson's equation throughout the 2D device is illustrated in Figure 5.5. The Fermi potential in the highly doped p^+- field implant regions is about -0.55V which surrounds the stair-case potential profile and prevents the cross-talk (electron migration) between the photodetector and the neighboring BCCD registers. The multiple n-type implants, additional to the regular buried channel of the photodetector create the stair-case potential profile with approximately 0.5V voltage difference between each step. Not shown in this figure is the effect of the shallow p^+-detector implant which pins the surface potential at the silicon/silicon dioxide interface to about -0.5V in the region from x equal to 2μm to 44μm.

The data presented in Figure 5.5 was obtained by employing the high dose BCCD channel implant option as regular buried channel implant. However, to maintain the desired operation of the photodetector readout, it is essential to study the effect of different n-channel doping options of the BCCD register on the graded potential profile.

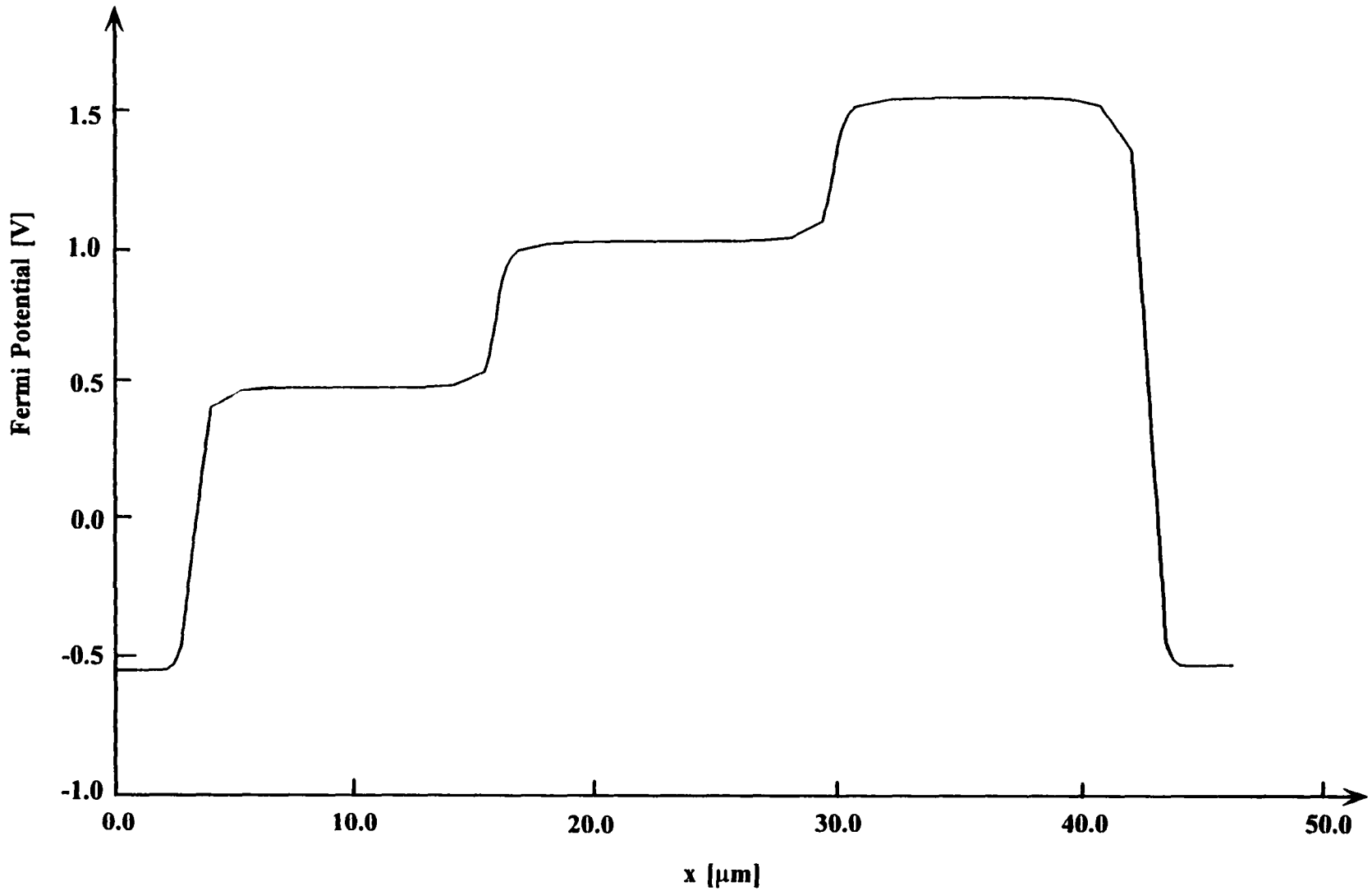


Figure 5.5 *Simulation result obtained by Pisces IIB illustrating the graded potential profile.*

5.3.2 Effect of Dual Buried Channel Implant on Graded Potential Profile of the Photodetector

Simulation results were obtained for the following values of dual (P and As) channel implant options by applying the simulation approach described in the previous section:

I) Low dose n-channel implant, *As: $6.5x10^{11}cm^{-2}$, 120keV, P: $6.5x10^{11}cm^{-2}$, 180keV,*

II) High dose n-channel implant, *As: $1.2x10^{12}cm^{-2}$, 120keV, P: $1.0x10^{12}cm^{-2}$, 180keV,*

III) Higher dose of As implant, *As: $2.2x10^{12}cm^{-2}$, 120keV, P: $1.0x10^{12}cm^{-2}$, 180keV,*

IV) Higher dose of P implant, *As: $1.2x10^{12}cm^{-2}$, 120keV, P: $2.0x10^{12}cm^{-2}$, 180keV.*

Figure 5.6 clearly shows that increasing Phosphorus dose in the buried channel implant shifts the graded potential profile to a more positive operation region of the photodetector readout. This can be seen from the potential profiles for implant options I, II and IV. Therefore, the obtained performance of the photodetector for low dose BCCD implant option may not be exactly valid and applicable for the high dose BCCD implant option. The graded potential profile can be shifted to the desired region of operation by controlling the additional Phosphorus implant dose values.

Another important result obtained by this analysis, is that increased dose of Arsenic doping has no effect on the graded potential profile of the photodetector which can be seen from the potential profiles for implant options I, II and III. Thus, it can be concluded that the steep Arsenic doping profile near the silicon/silicon dioxide interface is confined in the much higher doped p^+- detector implant region and the effect of increasing the Arsenic dose is therefore negligible.

This result is especially important for the design of the next phases of VHFR image sensors since one of the most important considerations in the imager design is to obtain higher charge handling capacity. The charge handling capacity of the VHFR imager can be increased directly by doping the buried channel with a higher dose of Arsenic without having any effect on charge collection and charge readout operation of the imager.

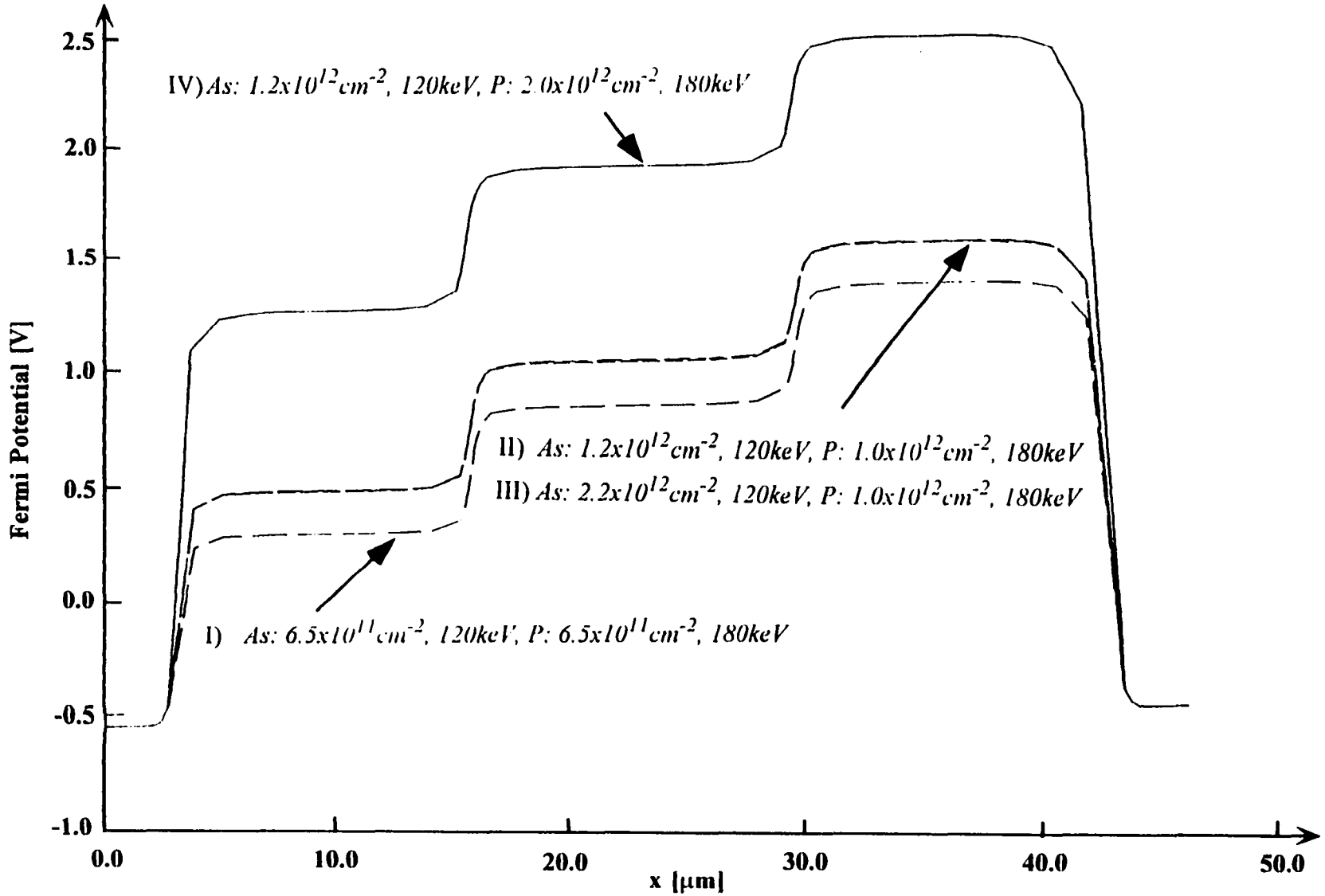


Figure 5.6 *Effect of different As and P dual buried channel implant dose options on graded potential profile.*

5.4 Simulated Photodetector Readout Operation

5.4.1 Simulation Approach

The 2D structure shown in Figure 5.7 (a) was generated by Pisces IIB to simulate the photodetector readout operation. Due to the limited number of mesh points of the currently available version of Pisces IIB for transient analysis, the 2D structure had to be defined very carefully to use the limited number of mesh points (1500 for transient analysis) with maximum efficiency. The photodetector readout sequence is as follows:

- In the first half frame time, the detected charge is accumulated in the last implant stage of the photodetector with multiple n-type implant regions. During charge accumulation, gates G_1 and G_3 are kept OFF (Figure 5.7 (b)).
- In the next half frame time, the detected charge in the photodetector is transferred to the charge collection well by turning gate G_1 ON. At the same time, charge detection in the photodetector continues so that new charge is directly stored in the charge collecting well under gate G_1. During this operation period, the charge transfer gate G_3 is still OFF in order to keep the detected charge separated from the serial-parallel SP register. The sketched potential profile and charge accumulation is illustrated in Figure 5.7 (c).
- At the end of one integration time T_i (or frame time), G_3 turns ON and G_1 turns OFF so that the charge that is collected under gate G_1 is transferred to the potential well under gate G_3. During the first half cycle of the second frame time, new charge also starts to accumulate in the photodetector. Figure 5.7 (d) illustrates the potential profile of new charge detection.

The above described operation of the photodetector requires transient analysis in order to perform the charge detection in the photodetector by photogeneration and consequently charge transfer from one gate to the next. Therefore, continuity equations for both carriers must be solved also in addition to the initial conditions obtained by the steady-state solution throughout the device. The timing diagram for the clock signals to be applied for the above described operation is given in Figure 5.8.

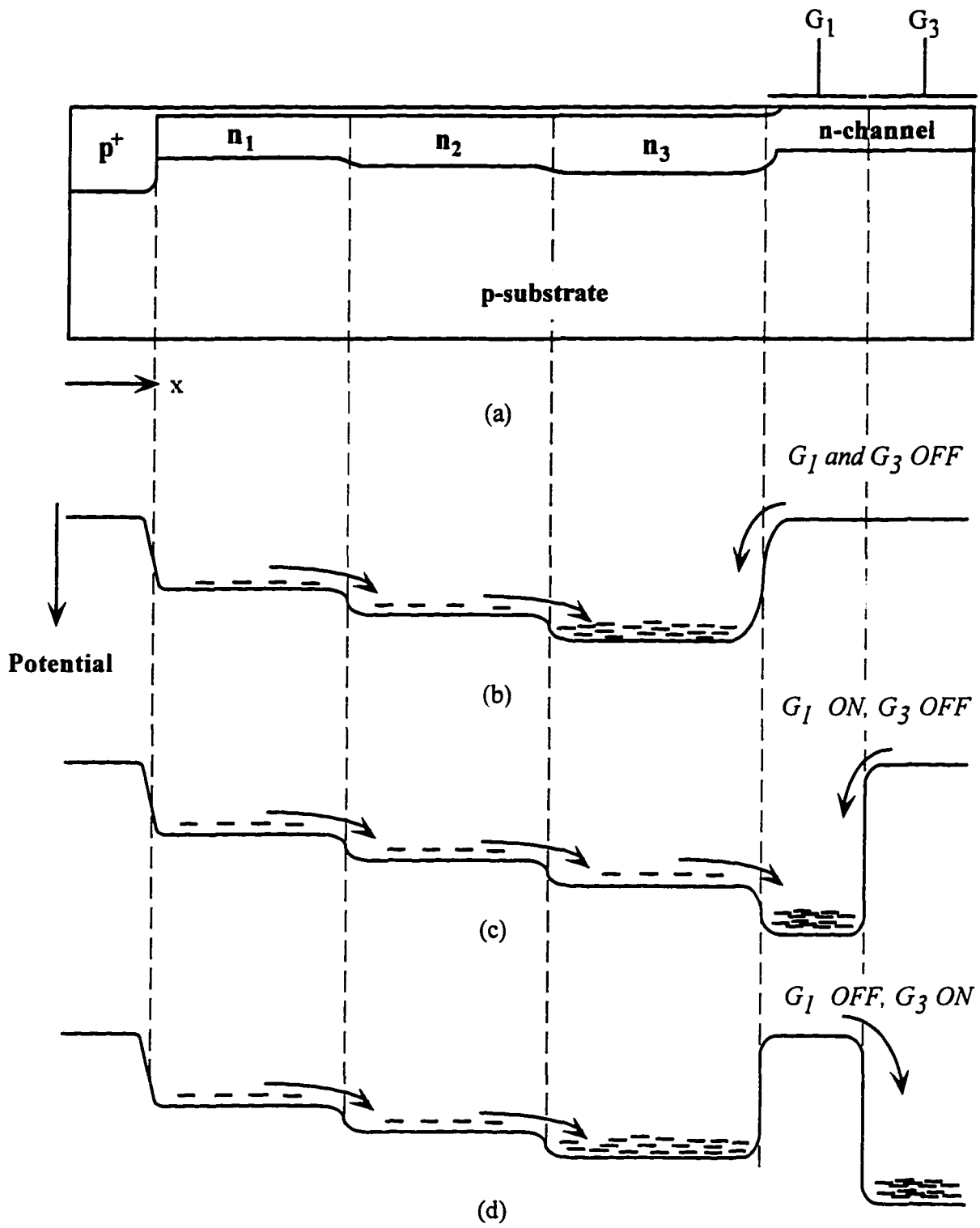


Figure 5.7 *Transient analysis of photodetector readout operation.*
(a) 2D structure. (b) Charge accumulation in photodetector.
(c) Charge transfer to the charge collecting well.
(d) New charge detection in the photodetector.

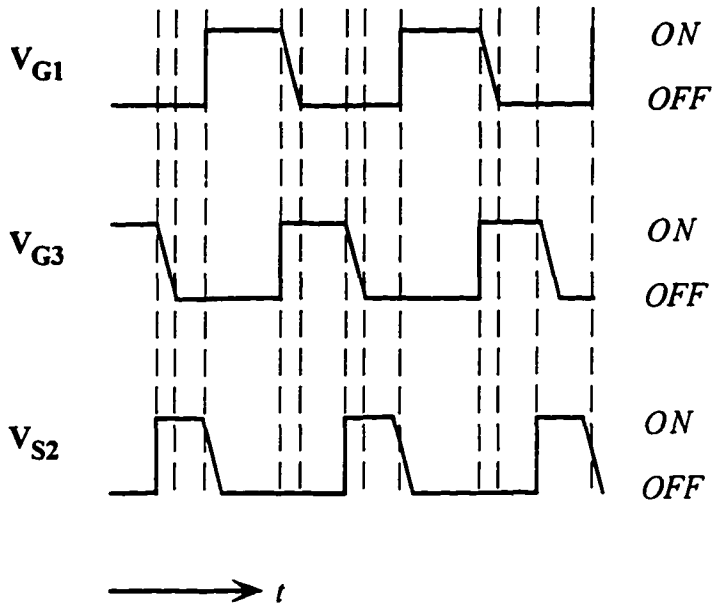


Figure 5.8 *Timing diagram.*

The clock pulses that have to be applied in order to perform the described operation of the photodetector readout is given in Figure 5.8. In this figure, V_{S2} represents the first stage of the serial-parallel SP register. The next step of charge transfer is from gate G_3 to S_2 which is not included into this simulation due to the previously mentioned limitations of Pisces IIB. Therefore, gate G_3 has been kept ON for the whole cycle of third half frame time. Turning gate G_3 OFF without having defined the adjacent gate S_2, results only the charge to spill back into the photodetector and is meaningless.

5.4.2 Photodetector Readout Operation

Simulation results obtained by the previous approach demonstrated that the photodetector readout does not perform as sketched in Figure 5.3. The photodetector readout suffers from a large amount of charge leakage from the photodetector region into the charge collecting gate G_1 and from G_1 to the next stages of the serial-parallel SP register. This result can be concluded directly by inspecting Figure 5.9 (a) and (b) which were obtained by following the simulation approach described in the previous section.

In this figure, results are illustrated for the first frame time only. The *total charge* corresponds to the total photogenerated charge in the whole device which is the sum of the *charge in the collecting well*, *charge under gate* G_3 and *charge in the photodetector region*. The large charge leakage can be seen from the first half cycle of the frame time where both G_1 and G_3 are OFF. During this half-cycle the total charge is expected to be confined in the photodetector region only and the amount of the total charge must be equal to the amount of detected charge by the photodetector.

However, the simulation result demonstrates a large amount of charge leakage into the adjacent potential wells and the detected charge is not entirely confined in the photodetector. This leakage results in a continuous charge transfer from gate G_1 to gate G_3 and to the next stages of the BCCD register at all times when G_1 is OFF unless illumination is not terminated in order to prevent the charge built-up in the photodetector by either applying light in the form of pulses or employing a mechanical shutter. The charge leakage clearly affects the performance of the imager and hence, must be avoided.

5.4.3 Correct Operation of the Photodetector Readout

Changes were made to correct the design error and verified by 2D simulation. The correct operation of the photodetector readout is illustrated in Figure 5.10.

- In the first half-cycle (from 0 to 0.5μs), the charge detection is observed in the photodetector region so that the detected charge equals to the total charge in the whole device.
- From 0.5μs to 1.0μs, gate G_1 is ON and the detected charge is transferred to the charge collecting well. At the same time, charge detection in the photodetector continues; the detected charge directly moves into the charge collecting well. The charge in the photodetector falls to a saturation value $Q_{S(sat)}$.
- At the end of one frame time, there is saturation charge $Q_{S(sat)}$ in the photodetector due to continuous illumination whereas the rest of the charge is collected under gate G_1.

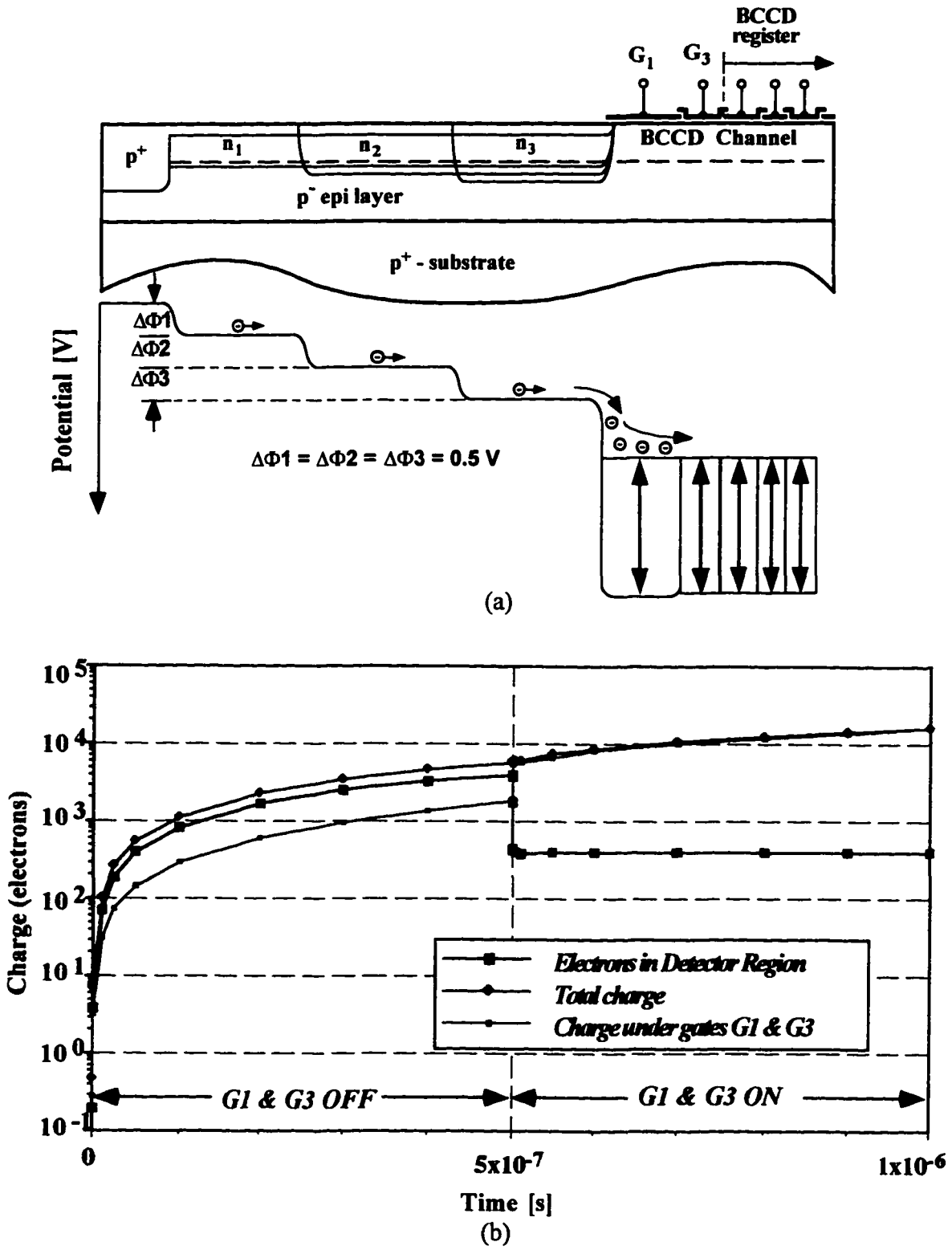


Figure 5.9 *Charge leakage from the photodetector into adjacent BCCD registers.*
(a) Sketch of the 2D structure and corresponding potential profile.
(b) 2D simulation result illustrating the charge leakage to the BCCD register.

- In the third half-cycle (from 1.0μs to 1.5μs), new charge starts to be detected and stored in the photodetector while gate G_1 is turned OFF again and gate G_3 is turned ON allowing the collected charge under gate G_1 to be transferred to gate G_3.

5.5 Design of High-Speed Photodetector for 10 Million Frames/Second Operation

The performance result of the photodetector with three n-type implants was presented in Chapter 3 Figure 3.12 of this thesis. This result was obtained by testing the 360x360-element VHFR image sensor at Princeton Scientific Instruments by applying 0.4μs LED pulses. The integration time T_i was 1μs. To operate the imager at even higher frame rates, a new chip architecture was proposed as the second phase of this project. The primary objective of Phase II is to develop an ultra-fast frame rate image sensor and associated camera electronics capable of capturing, during a single laser pulse, 12 images at a frame rate of 10^7frames/second. It is the further objective to demonstrate this performance and to deliver the prototype camera system to Phillips Laboratories at the end of Phase II, for deep space imaging experiments. In this new architecture, the memory array is configured into a single column at the photodetector output, thus eliminating the time taken to vertically shift horizontal rows during image collection period. With this new architecture, the fabrication technology was also simplified by accommodating only 3-layers of polysilicon. Since the vertical transfer of row charge is eliminated in this design there is simply no need for poly-4 layer. Due to the less capacitance, the RC time constant of the BCCD gate electrodes are reduced. The photodetector for operation with 100ns frame time was designed by the author to allow the ultra-fast frame rate image sensor to operate at a frame rate 10^7frames/second. As part of this project requirements extensive device simulations by Pisces IIB were performed at Electronic Imaging Center, NJIT and results will be presented in the following sections of this thesis. The detector size is 100μm x 52.8μm corresponding to a fill factor of 45%. The pixel size of this new design is 106μm x 106μm employing minimum design rules of 1.5μm.

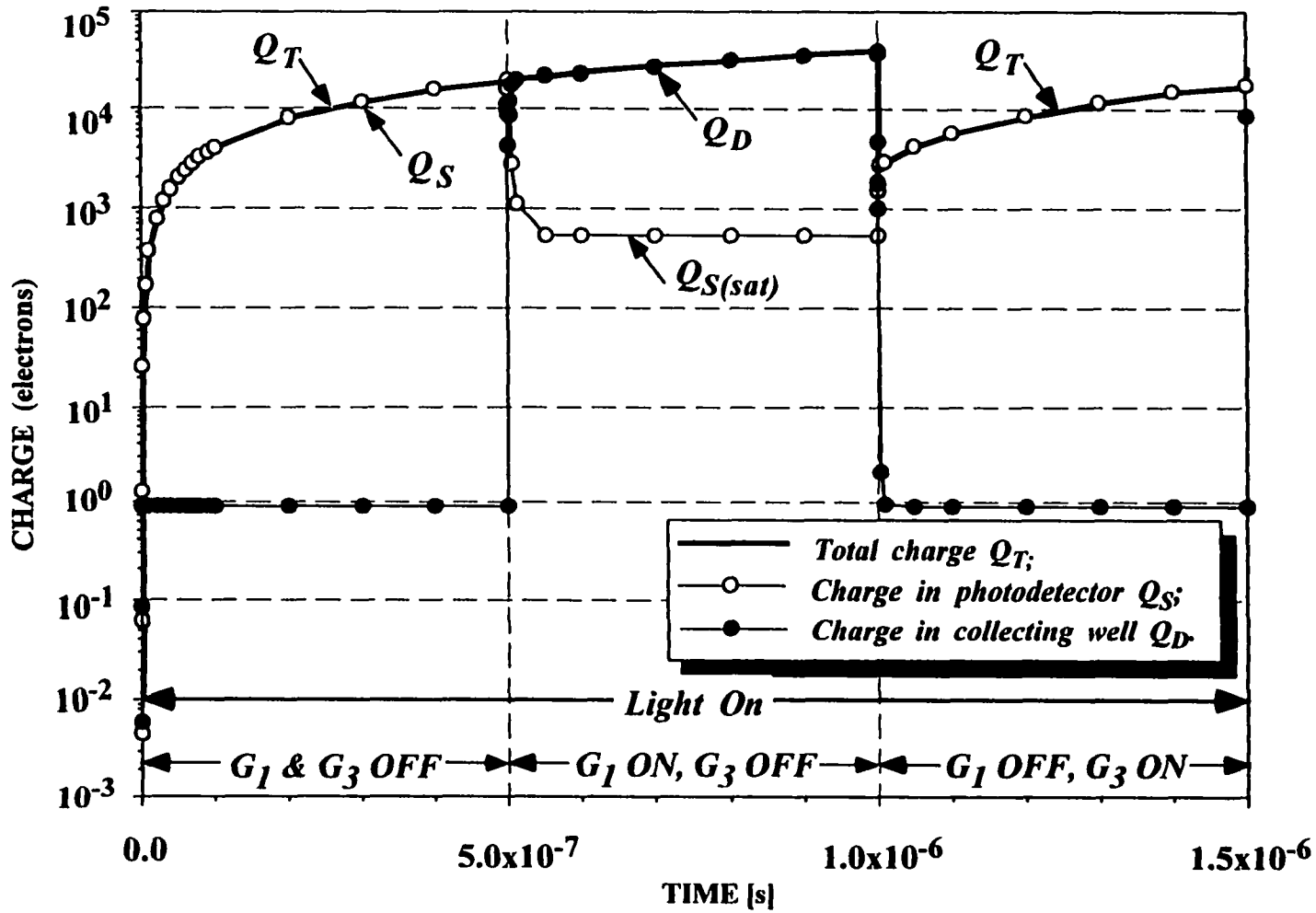


Figure 5.10 *Simulated result of photodetector readout operation with corrected structure. Illumination intensity: 20000 electrons/0.5μs.*

5.5.1 Response of the Photodetector with Multiple Implants to a Step Illumination

It is interesting to analyze the time response of the photodetector with multiple implants to a step illumination. These results demonstrate the performance of the photodetector if illumination is not continuous and provided in the form of pulses. To allow the high-speed operation, the time for transferring the generated photoelectrons from photodetector to the charge collecting well should be equal or less than 100ns. Results will be presented for charge build-up in the photodetector during the pulse illumination and for following charge decay from the photodetector into the adjacent potential well after the illumination is terminated.

The simulated time response of the photodetector to a step illumination of intensity collecting 12000 photogenerated electrons in optical illumination time of 100ns is illustrated in Figure 5.11. In this simulation, the photodetector structure consists of six implant regions with equal distance of 5μm. Figure 5.11 also illustrates the relationship between the total photogenerated charge Q_T, the charge stored in the photodetector Q_S and the charge Q_D collected in BCCD collecting well under gate G_1. For total charge, Q_T, increasing at a constant rate, the photodetector channel charge Q_S reaches a steady-state saturation level of about 400 electrons in 10ns. Once the stored detector charge Q_S reaches steady-state, the rate at which the detected charge, Q_D , is collected under gate G_1 becomes equal to the rate of the photogeneration of the total charge, Q_T, or when $Q_S \rightarrow Q_{S(sat)}$:

$$\frac{dQ_D}{dt} = \frac{dQ_T}{dt}. \tag{5.1}$$

The photodetector structure defined for 2D simulation by Pisces IIB consists of six implant regions with equal length L. Simulations were performed for four values of L which are 10μm, 8.8μm, 7μm and 5μm. The width of the structure was assumed as 80μm for calculation of the total charge in the device.

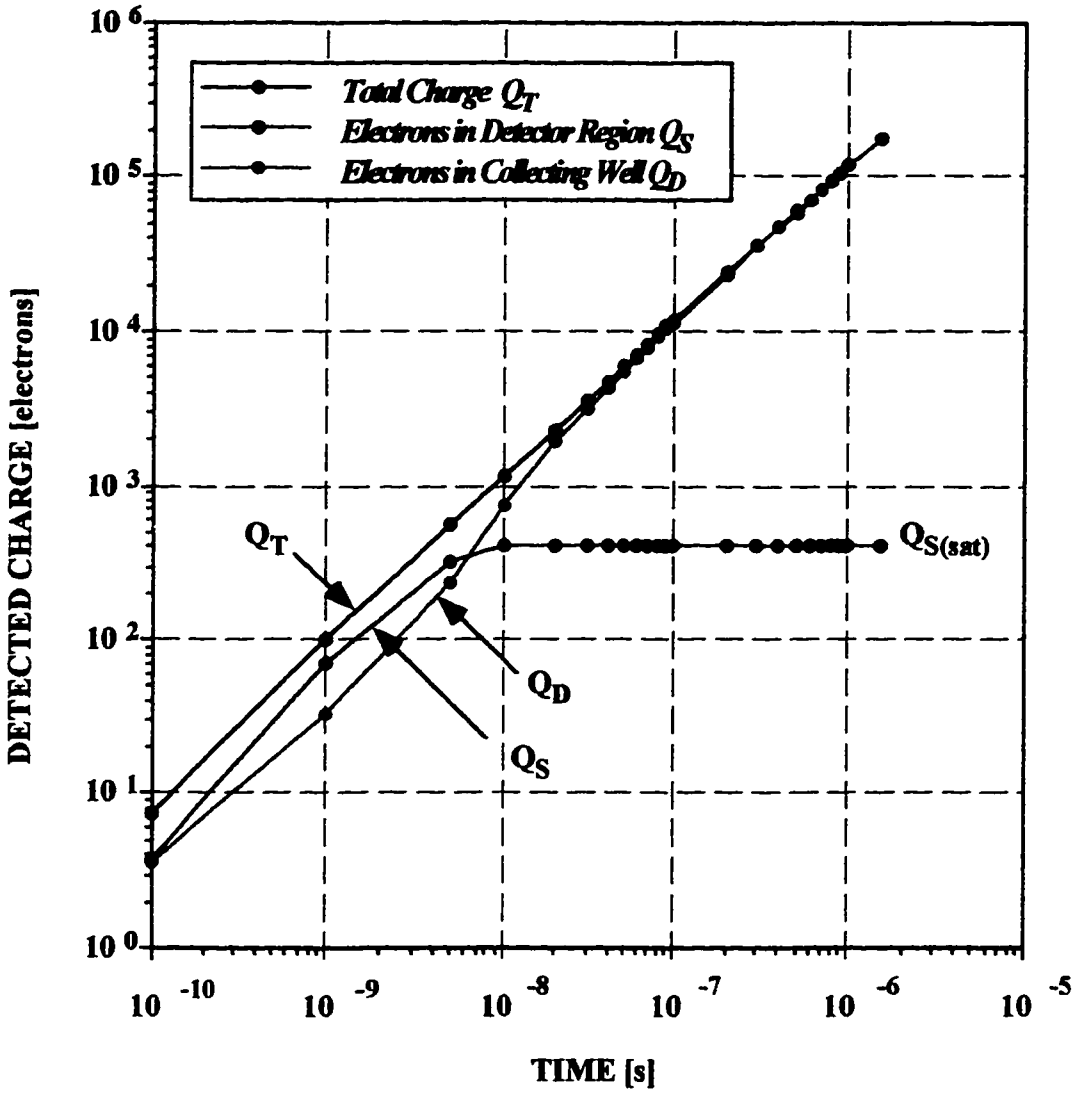


Figure 5.11 *Time response of the photodetector with six n-type implants to a step illumination with intensity of 12000 electrons in 100ns.*

For simulation of the time response to a pulse illumination of the photodetector structure, the illumination intensity was adjusted so that the total charge Q_T was kept constant for all values of L. This result is illustrated in Figure 5.12. By adjusting the illumination intensity, the total charge is obtained as about 12000 electrons in 100ns for all photodetectors with different values of L.

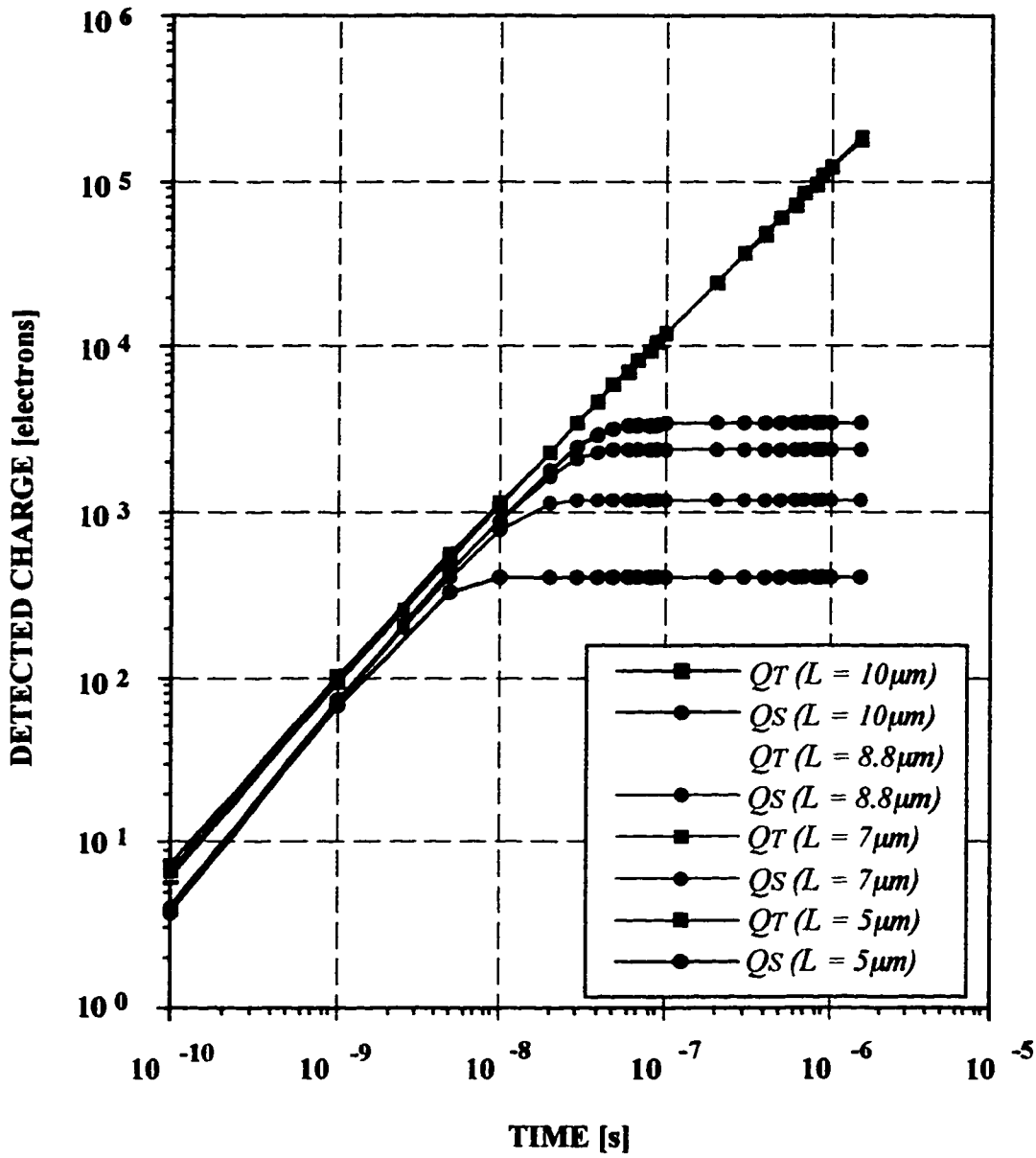


Figure 5.12 *Time response of the photodetectors with six n-type implants with four different values of L to a step illumination with intensity of 12000 electrons in 100ns.*

The relationship between the charge build-up per unit width in the photodetector and the distance between implant stages is further demonstrated in Figure 5.13. It should be noted that the photodetector charge reaches the steady-state saturation level in about 10ns for a structure with six implants of 5μm distance between each implant stage. For a structure with 10μm distance, the time needed to reach the saturation level is significantly higher and is obtained as approximately 80ns. There is also significant increase in the level of saturation charge with increasing length of implant stages; the saturation charge level is 5 electrons per micron width in the smallest photodetector whereas it becomes about 42 electrons per micron width for the photodetector with 10μm distance between implant stages.

The transfer of the saturation charge $Q_{S(sat)}$ per unit width from the photodetector region into the charge collecting well is also simulated. Figure 5.14 is continuation of Figure 5.13 and illustrates the charge decay in the photodetector following a 100ns step illumination. In other words, in this figure the illumination is terminated at time t equal to 100ns. From this figure, the time needed for the charge to fall from the saturation level $Q_{S(sat)}$ to one electron per micron width is obtained as 5ns for the smallest photodetector. The decay time increases rapidly for longer structures and becomes 62ns for the photodetector with 10μm distance between implant stages.

For operation with 100ns frame time both charge build-up in the photodetector during illumination and the charge decay after the illumination is terminated have to be completed in one frame time. For this operation, the duration of the pulse illumination can be estimated as half of the frame time. According to the results given in Figure 5.13, the photodetector structure with 8.8μm equal implant spacing can reach the steady-state charge level in about 50ns. Charge decay in the same structure takes about 40ns as shown in Figure 5.14. Therefore, it can be concluded that a photodetector with six implants having 8.8μm distance between each implant stage is fast enough to operate the imager at a frame rate of 10 million frames/second.

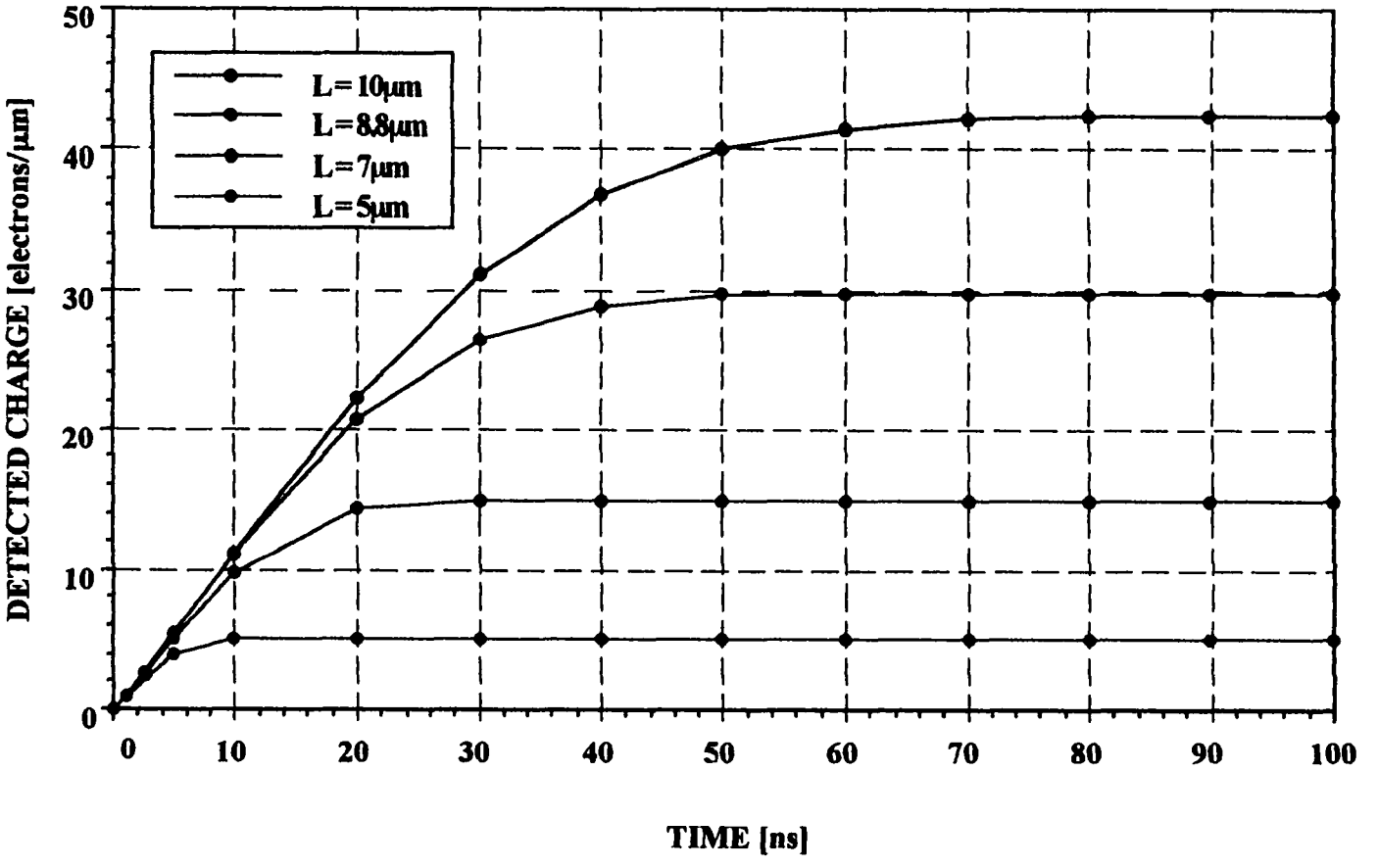


Figure 5.13 *Charge build-up per unit width in the photodetector with six equal long (L) implant stages for illumination intensity of generating 12000 electrons in 100ns.*

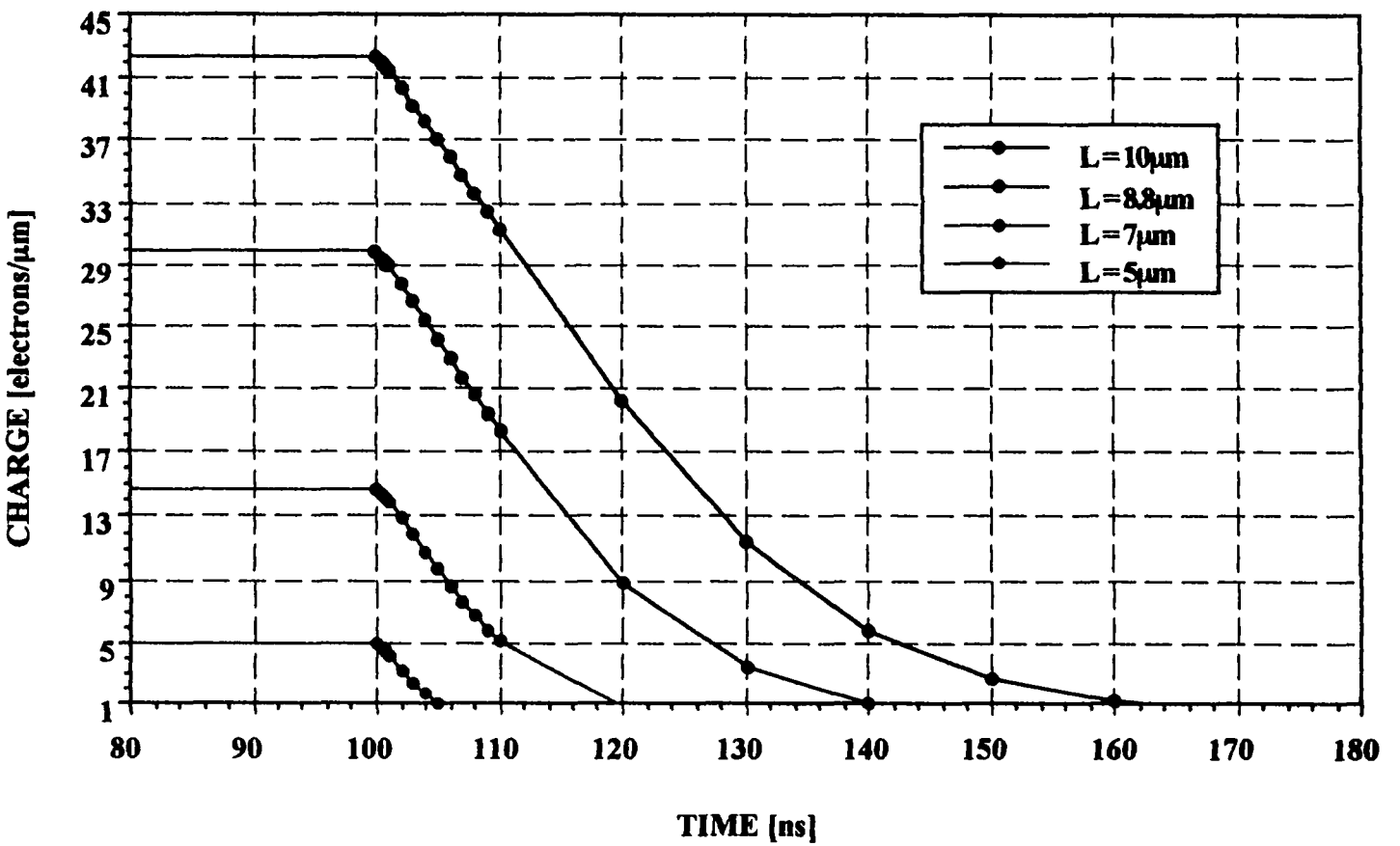


Figure 5.14 *Transfer of the detected charge per unit width from the photodetector into charge collecting well following a 100ns pulse illumination.*

The sketch of the designed photodetector with six implant stages of each 8.8μm long is shown in Figure 5.15. The total time needed for charge detection and transfer is simulated as about 90ns for this structure. The final width of the detector is determined as 100μm.

This new photodetector structure was designed to have a large detector well which is 8.8μm x 12μm so that the detected charge can be stored in the last implant region during charge collection cycle. The stored charge can be directly dumped to the dumping drain over a control gate G_2 or it can be transferred to the output serial BCCD register controlled by G_1 and G_3. Both outputs from the detector well were shown in this figure as Detector Dump and Detector Readout respectively. This modification in the photodetector readout enables the readout to operate with exposure times less than one frame time which can be controlled by appropriate clocking of the gate electrodes.

5.5.2 Photodetector Readout with Continuous Illumination

The design allows the photodetector to operate with a pulse illumination as described in the previous section. However, since there is no charge leakage from the photodetector into the adjacent potential wells, it can be operated with continuous illumination as well. 2D simulations were performed to illustrate the readout operation of two photodetector structures with six implants, first having 5μm distance between implant regions, and second having 10μm distance between implant regions. The illumination intensity was adjusted so that same amount of charge was detected in both structures at the end of one frame time.

Figure 5.16 and 5.19 illustrate the photodetector readout operation with 100ns frame time for both 60μm and 30μm long photodetectors respectively. It should be noted that both photodetectors were assumed to be 80μm wide, and the number of electrons collected is about 12000 electrons in 100ns. Therefore, any amount of charge less than 80 electrons in both figures is actually a computational artifact corresponding to less than 1 electron per micron width and should be ignored.

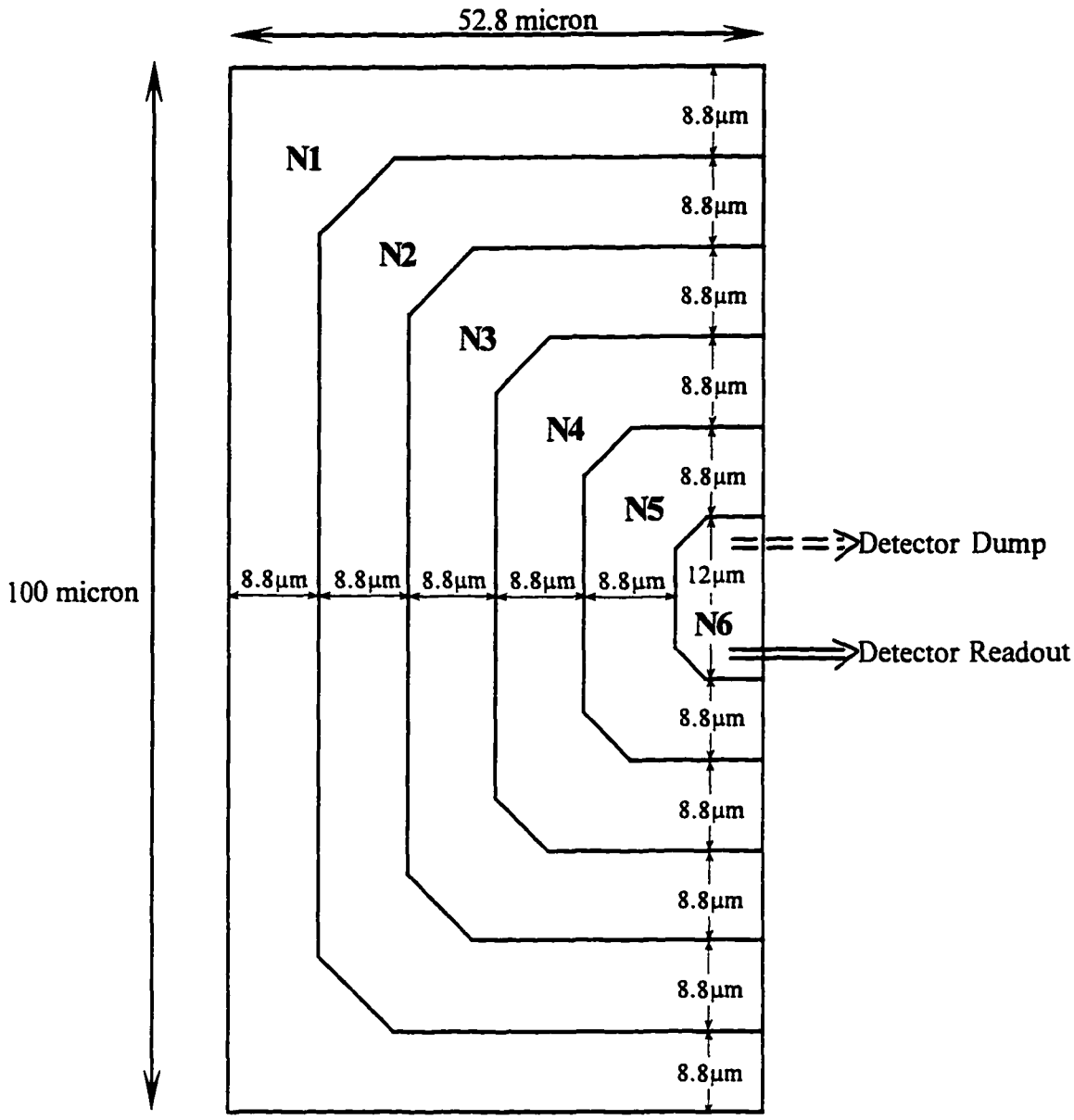


Figure 5.15 *Sketch of the ultra-fast photodetector with six implant regions.*

Inspection of both figures clearly demonstrate that there is no charge leakage from the photodetector into the adjacent potential wells during the entire readout operation. In the first 50ns (half-frame cycle) charge is detected by the photodetector and stored in the detector well by keeping gates G_1 and G_3 at low clock voltage. In this cycle, the detector charge Q_S is equal to the total charge Q_T of the whole device and increases linearly with time. At the end of 50ns, the detected charge is transferred to the potential well under gate G_1 by turning this gate ON. In this cycle gate G_3 is still OFF. The time that is needed for the charge to be transferred from the photodetector into the charge collecting well under gate G_1 is crucial for the readout operation. Thus, the time that is needed for the detected charge in the photodetector to fall from the total amount of Q_S to the steady-state saturation level $Q_{S(sat)}$ determines the speed of the photodetector. For the 60μm structure, the decay time under continuous illumination is about 10ns, whereas the 30μm structure needs only 5ns to transfer the charge from the photodetector into the charge collecting well.

At the end of one frame time , gate G_3 is turned ON and gate G_1 is turned OFF so that the charge is transferred from G_1 to G_3 by the fringing field effect. In this cycle, new charge starts to accumulate in the detector region.

The charge transfer in the photodetector can be further explained using the results presented in Figures 5.17 and 5.18 obtained for 60μm and Figures 5.20 and 5.21 obtained for 30μm long photodetectors with six equally spaced implants. Figures 5.17 and 5.20 illustrate the distribution of charge in each implant region with the total amount of photodetector charge Q_S for both photodetectors, respectively. These figures illustrate that the charge distributed in the first five implant regions reach the steady-state saturation value after the illumination is turned on and remain at this value for the rest of the whole imager operation. The last implant stage acts as detector well; where charge is confined for the first half frame cycle before it is transferred to the adjacent potential well. It should be noted that with shorter distance between implant regions, the level of

saturation charge decreases significantly. This result is also expected since detected charge moves faster for shorter values of L from one implant region to the next, eventually accumulating in the last implant region. The only variation in the amount of charge as function of time is therefore observed for the charge confined in the last implant region.

Figures 5.18 and 5.21 compares the sum of the distributed charge in the first five implant regions with the charge of the last implant region together with the total saturation charge Q_S for both photodetectors. As the distance between implant stages get shorter, the saturation level in all implant regions become less significant compared to the total of saturation charge Q_S. As a result, the charge in collecting well Q_D approaches the total detected amount Q_T in the second half frame time. Charge transfer from the last implant region into the adjacent potential well under gate G_1 becomes also faster due to the shorter values of L.

Figure 5.22 illustrates the photodetector readout for a 60μm structure with unequal implant spacing. The first three implants of this structure have 6μm spacing between implant stages and the remaining three implants have 14μm spacing between implant stages. It can be concluded that unequal spacing of the implant regions would increase the saturation charge in longer stages rapidly to higher values resulting in a higher total saturation charge level that can be obtained with equal spacing. Furthermore, fluctuations of the charge with time in the stages in front of the detector well is observed (Figure 5.23) and more charge is confined in the first stages rather than in the detector well (Figure 5.24). Therefore, for optimum design of the photodetector with multiple implants equal spacing between implant regions must be accommodated.

Simulation results for 60μm long photodetector with 10μm distance between implant stages show that 100ns operation can be easily achieved under continuous illumination. The photodetector can be operated even with shorter exposure times.

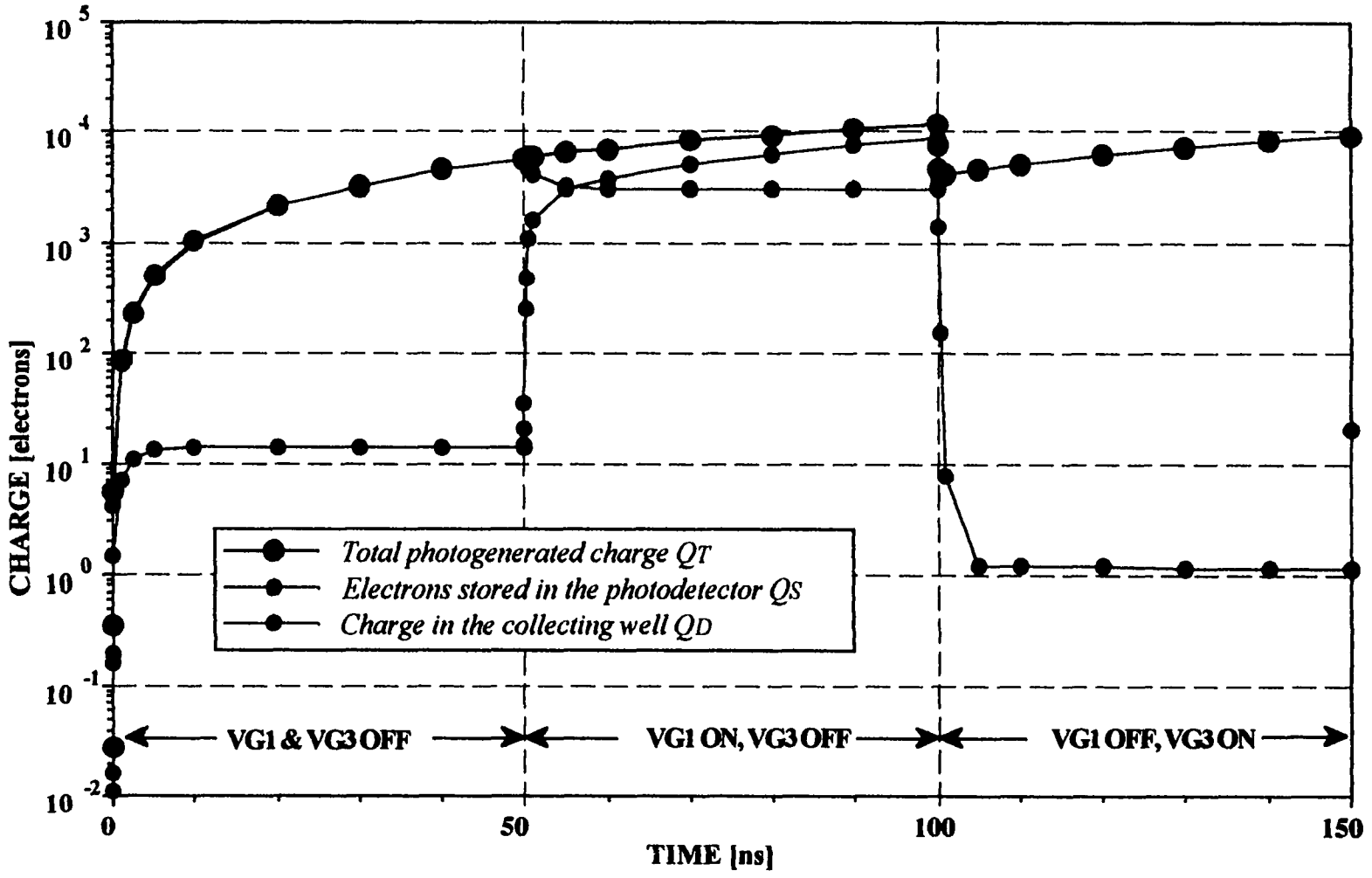


Figure 5.16 *Photodetector readout for a 60μm long structure with six equally spaced implant stages under continuous illumination with intensity 12000 electrons / 100ns.*

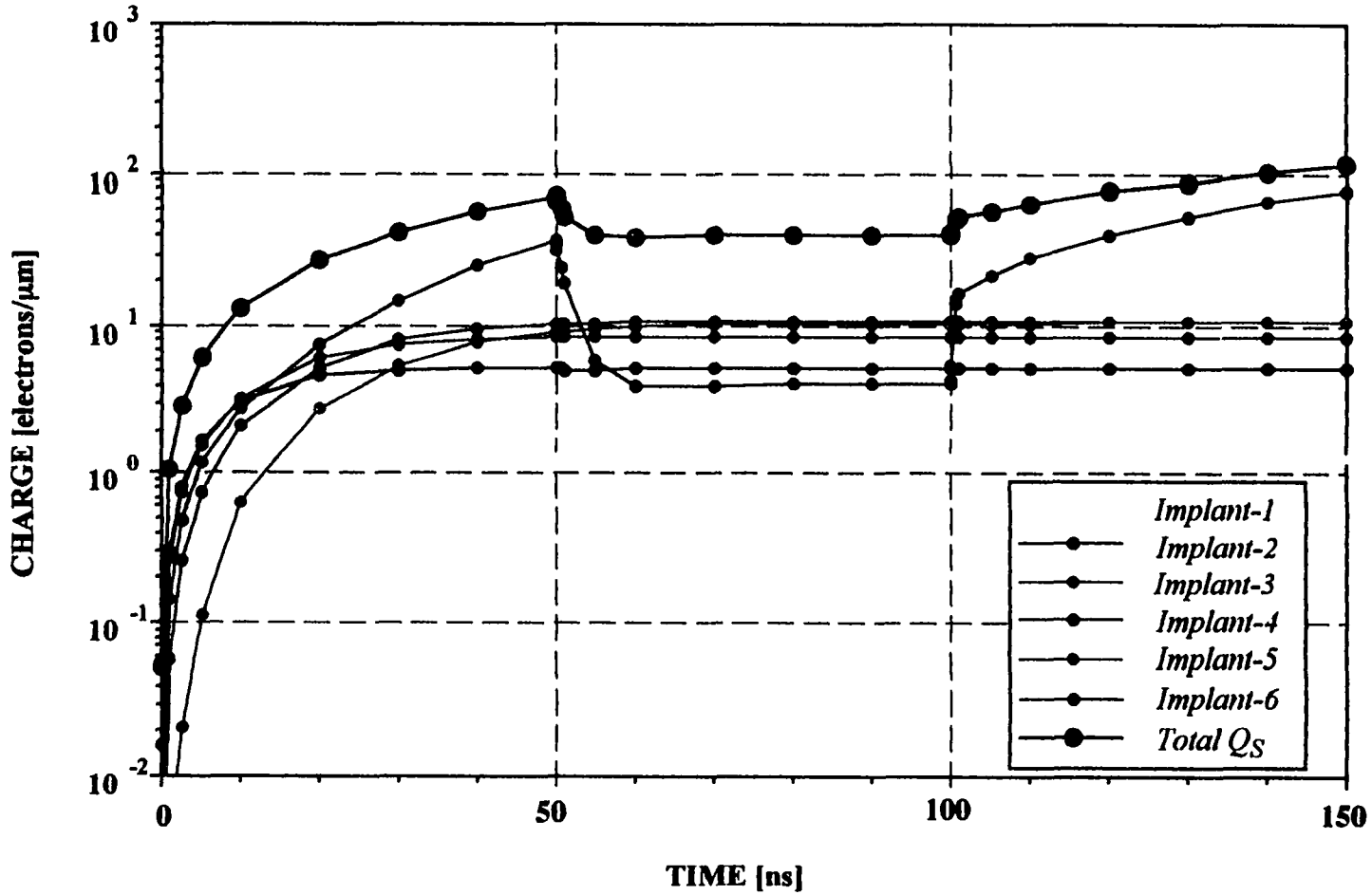


Figure 5.17 *Distribution of charge stored in the 60μm long photodetector.*

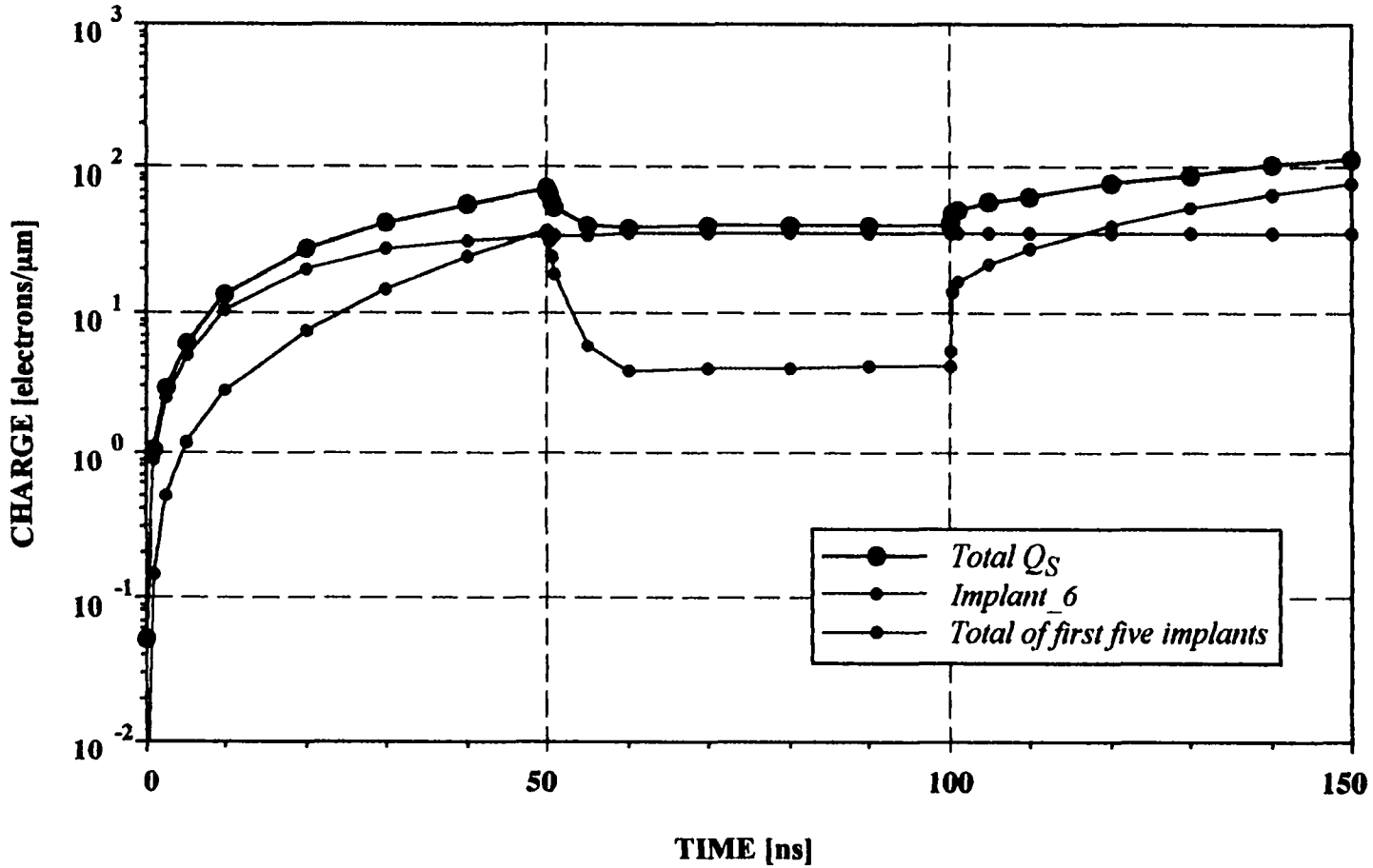


Figure 5.18 *Charge distribution between the first five implant stages and the last implant stage, and comparison to the total photogenerated charge of 60μm long photodetector.*

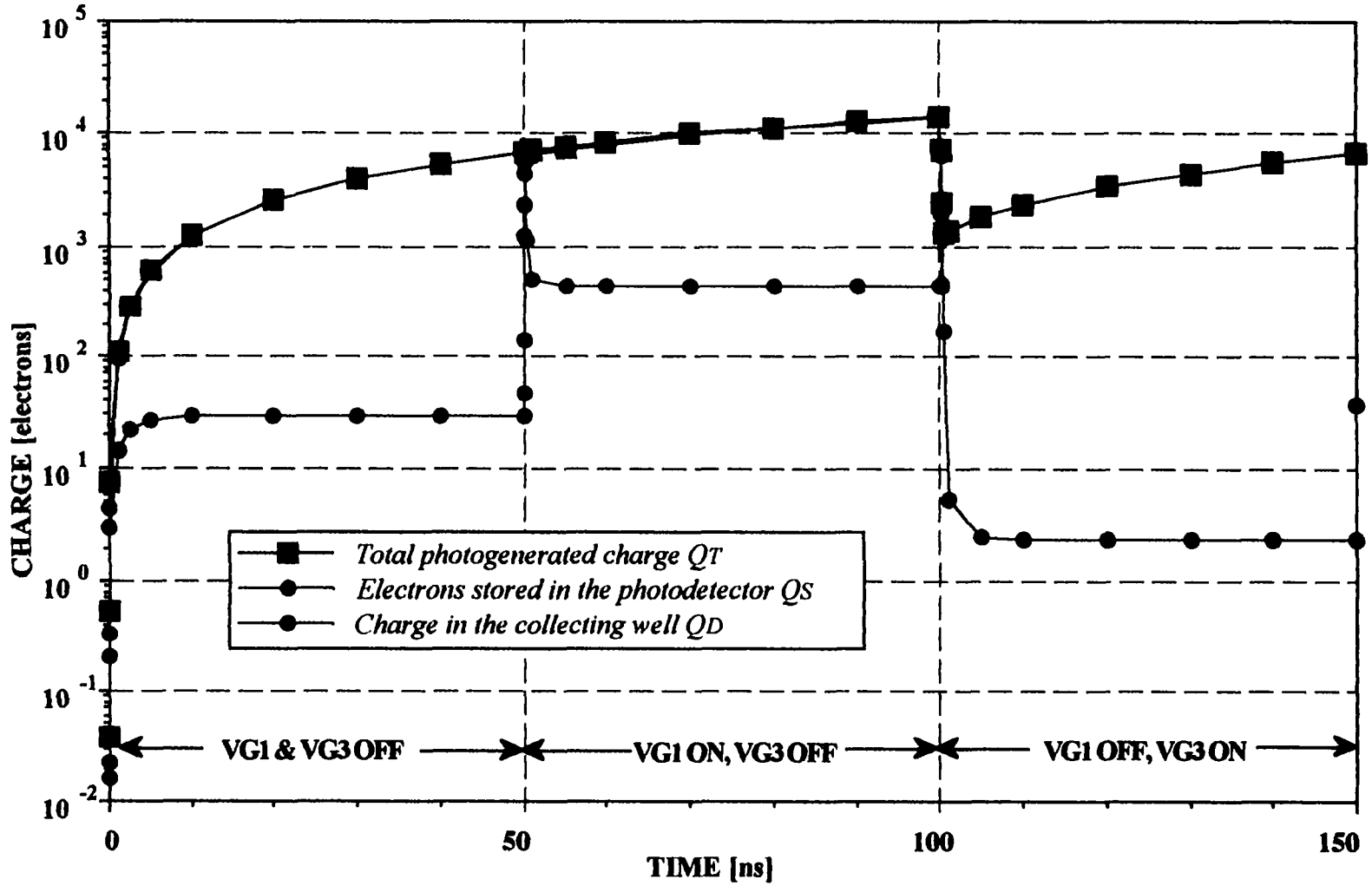


Figure 5.19 *Photodetector readout for a 30μm long structure with six equally spaced implant stages under continuous illumination with intensity 12000 electrons / 100ns.*

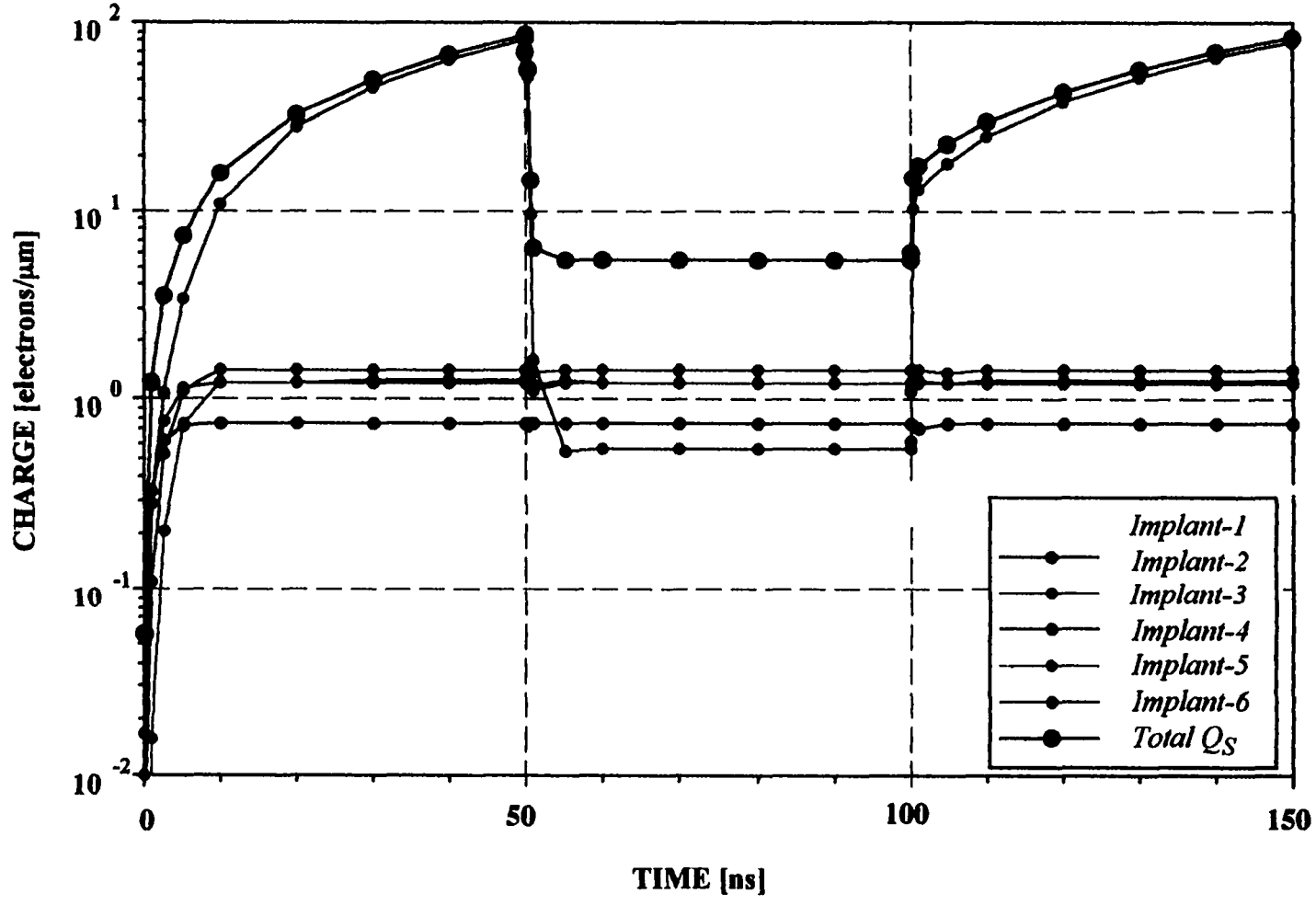


Figure 5.20 *Distribution of charge stored in the 30μm long photodetector.*

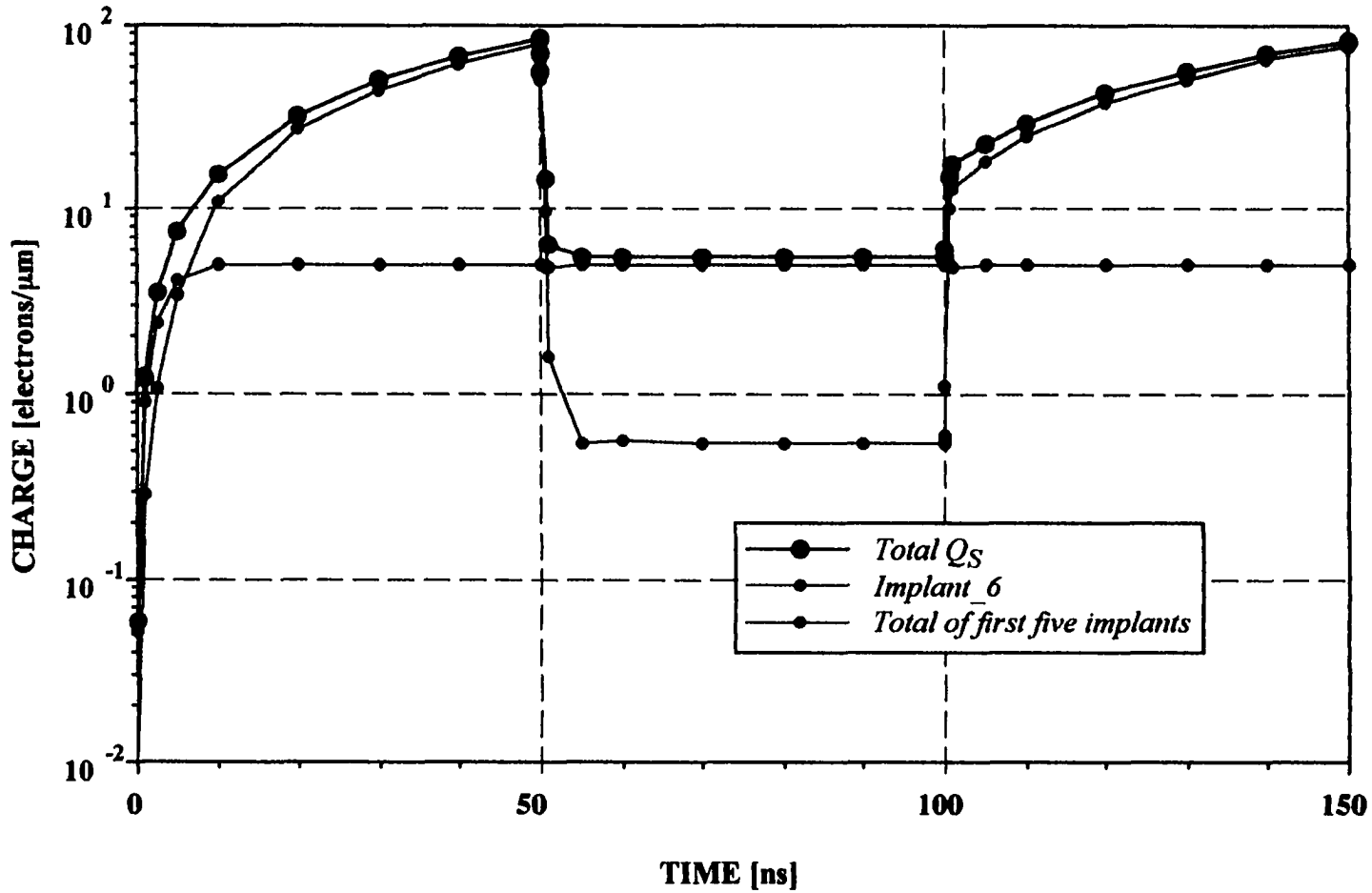


Figure 5.21 *Charge distribution between the first five implant stages and the last implant stage, and comparison to the total photogenerated charge of 30μm long photodetector.*

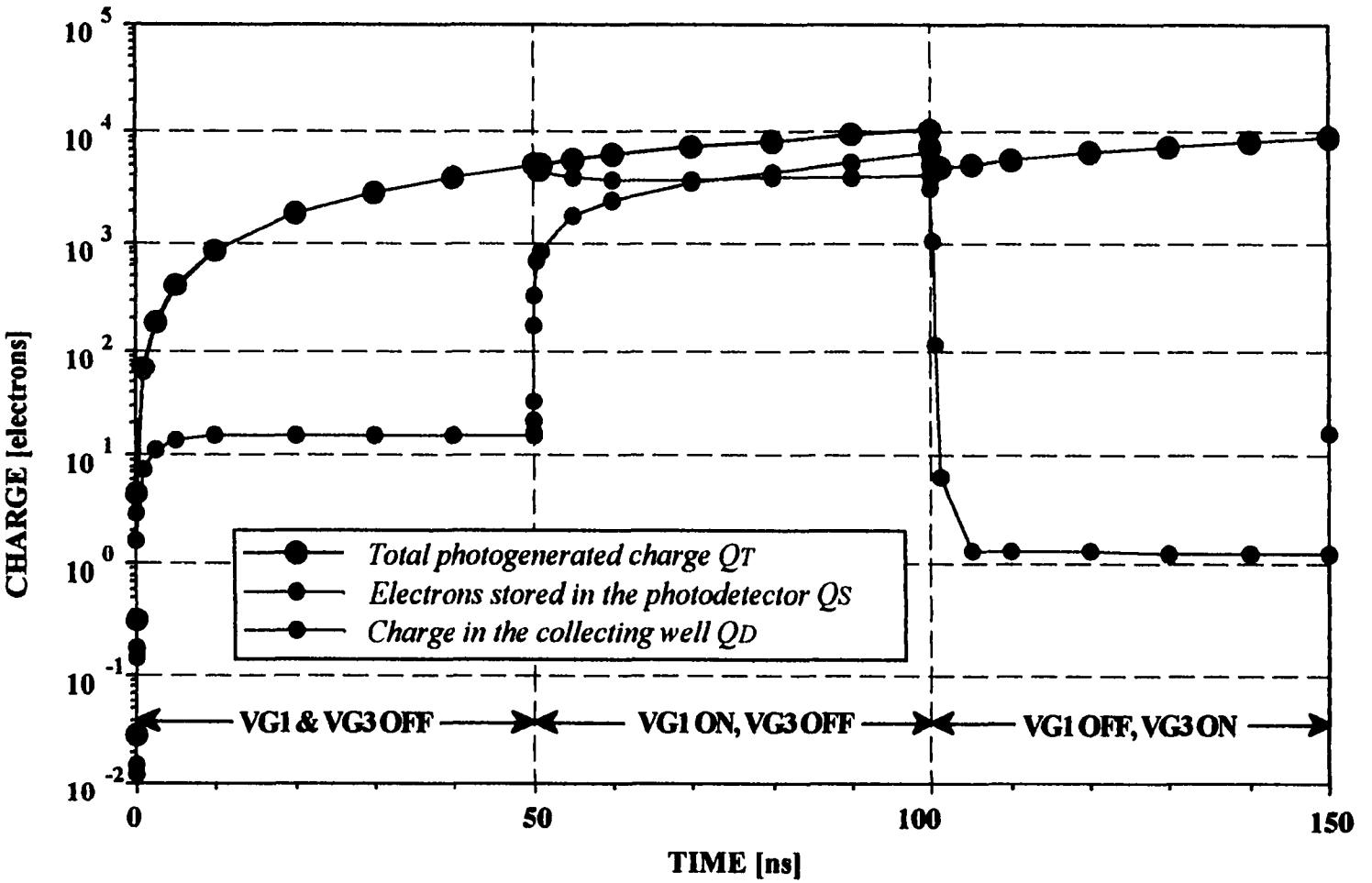


Figure 5.22 *Photodetector readout for a 60μm long structure with three 6μm and three 14μm long implant stages under continuous illumination with intensity 10000 electrons / 100ns.*

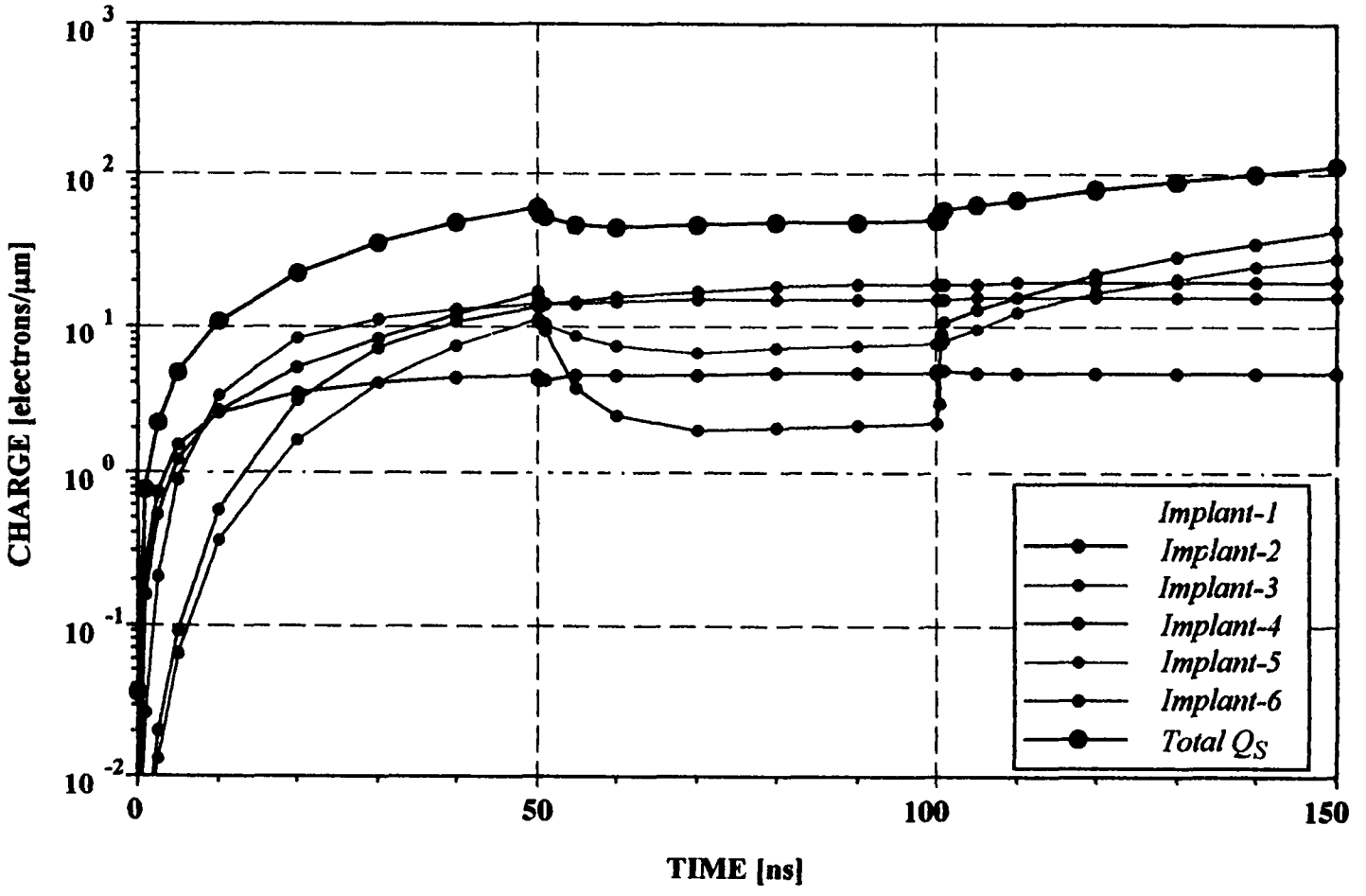


Figure 5.23 *Distribution of charge stored in the 60μm long photodetector with six implants with three 6μm and three 14μm long implant stages.*

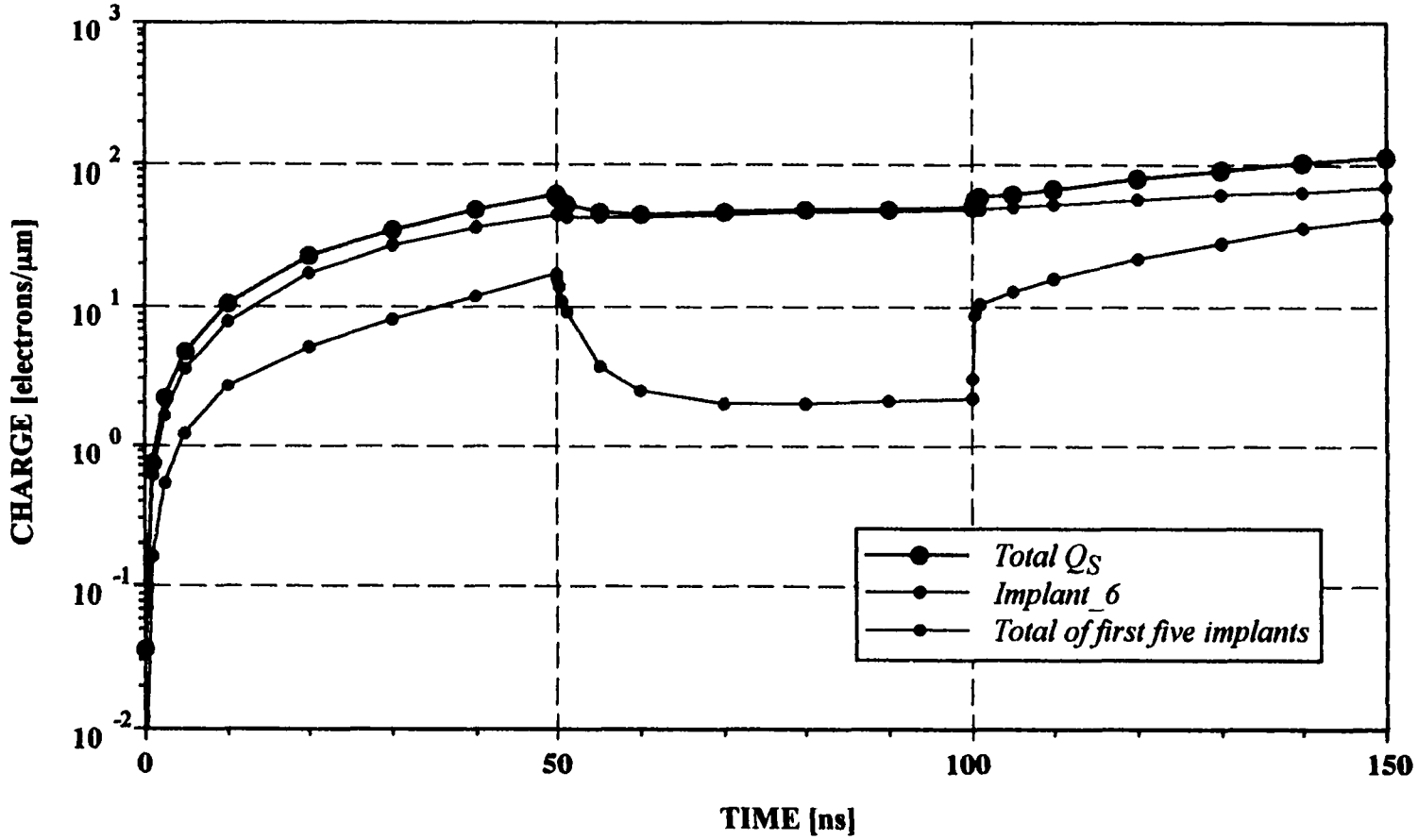


Figure 5.24 *Charge distribution between the first five implant stages and the last implant stage, and comparison to the total photogenerated charge of 60μm long photodetector with three 6μm and three 14μm long implants.*

The photodetector with six 8.8μm implant regions operates slightly faster and charge transfer from the detector well to the BCCD register is completed in about 8ns.

Finally, Figure 5.25 and 5.26 illustrate results obtained for a 30μm long photodetector with three equally spaced implant regions.

Summary

A design method is studied to speed the charge collection by using non-uniform well doping in the photodetector. Simulations demonstrate that the collection time can be reduced by as much as 10 times with the photodetector with six multiple implants. The design is obtained by following the described strategy. The optimization of the photodetector design is studied with the following points:

- Increasing the number of implants within a photodetector structure increases the readout speed significantly and decreases the saturation charge in the photodetector region. This result can be seen by comparing Figure 5.19 with Figure 5.25.
- For the same number of implants, decreasing the spacing between implant stages, and eventually the size of the photodetector, increases the speed of the photodetector (Figures 5.19 and 5.16). The time needed to reach the saturation is much less for the shorter structure (Figures 5.20 and 5.17) and more charge is accumulated in the detector well (Figures 5.21 and 5.18).
- Keeping the spacing between implant stages constant and increasing the photodetector size and number of implants result in a larger photodetector with a higher fill factor. Comparing the Figures 5.17 and 5.18 with Figure 5.26 show that the detector implants reach the steady-state condition faster for the shorter photodetector, resulting in a lower amount of saturation charge confined in the first implant stages of the longer structure. However the charge transfer is faster for the longer structure (Figures 5.16 and 5.25).
- For the design of the photodetector with multiple implants, optimum solution is found as having equal distance between implant stages.

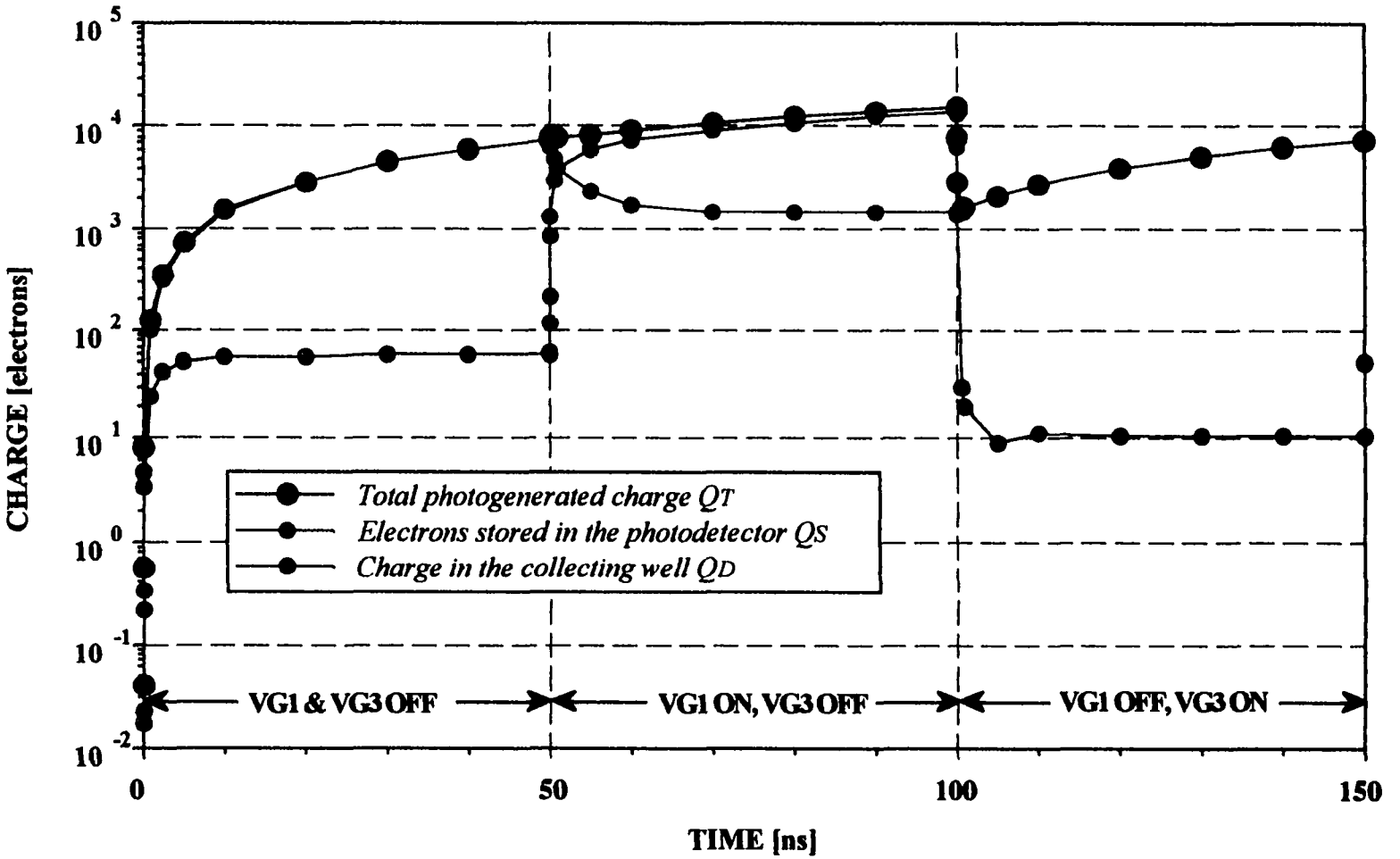


Figure 5.25 *Photodetector readout for a 30μm long structure with three equally spaced implant stages under continuous illumination with intensity 12000 electrons / 100ns.*

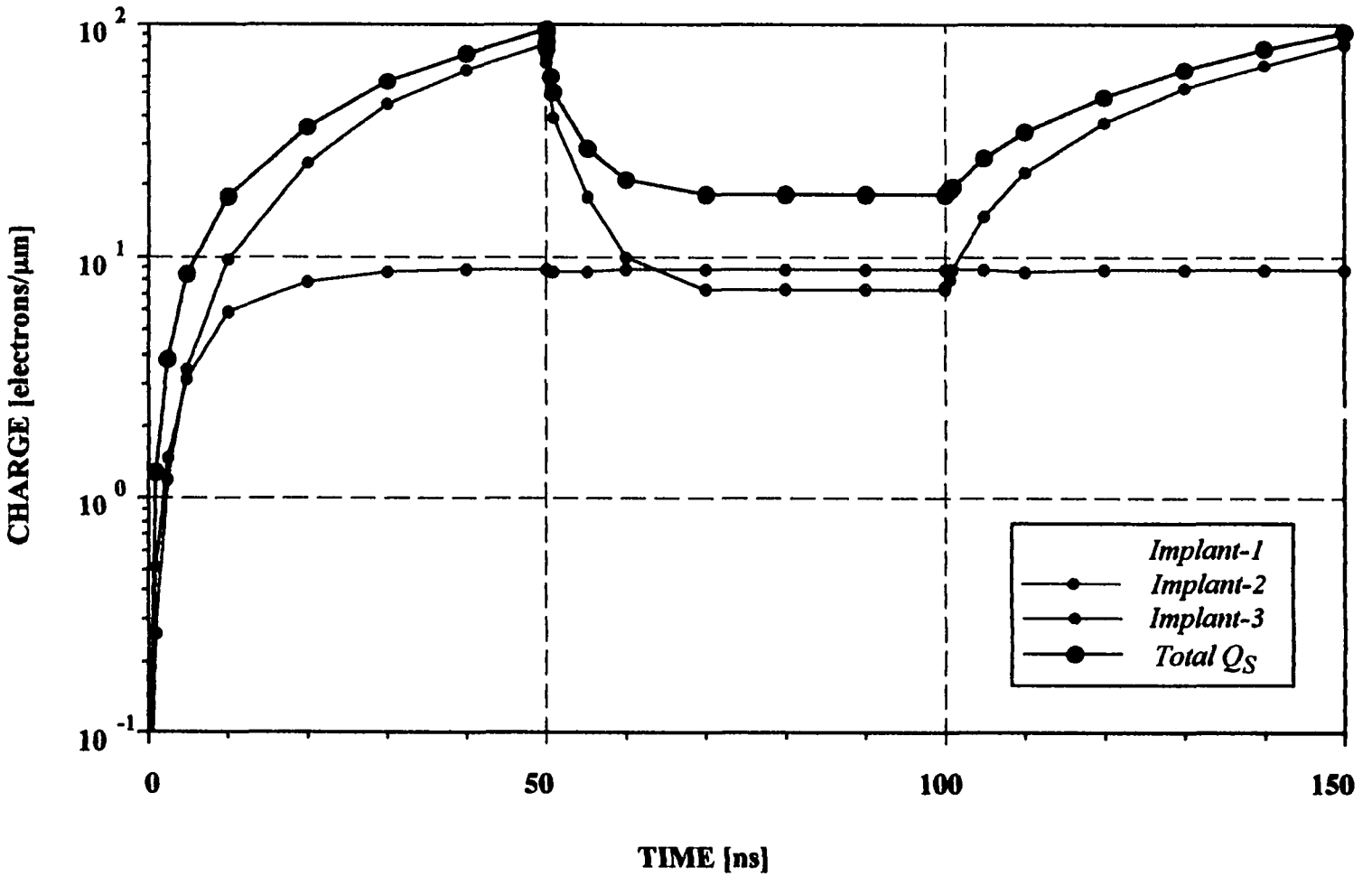


Figure 5.26 *Distribution of charge stored in the 30μm long photodetector.*

CHAPTER 6

3D EFFECT OF CHANNEL WIDENING ON CARRIER TRANSIT TIME IN THE HIGH-SPEED PHOTODETECTOR

6.1 180x180-Element VHFR Imager

A 180x180-element image sensor was designed after completion of the fabrication and testing of the 360x360-element VHFR image sensor as part of phase I. This sensor is being fabricated at David Sarnoff Research Center with modified design rules in order to obtain higher device yield. The 180x180-element imager is constructed of two quadrants each containing 180 x 90 macropixels. The size of the new macropixel is about 100μm x 100μm, consisting of a photodetector, a photodetector readout structure and BCCD memory pixels. The number of frames that can be detected and stored in this imager is 32 (4 x 8). The imager fabrication employs only the higher BCCD implant dose option for the n-channel of the first fabrication process (As: $1.2\text{x}10^{12}\text{cm}^{-2}$, 120keV and P: $1.0\text{x}10^{12}\text{cm}^{-2}$, 180keV). To reach even higher charge handling capacity, As dose is further increased for one set of wafers from $1.2\text{x}10^{12}\text{cm}^{-2}$ to $2.2\text{x}10^{12}\text{cm}^{-2}$. The channel length of the smallest BCCD element is also increased from 1.5μm to 2.5μm.

6.2 Photodetector Design

The size of the photodetector for this new design is increased to 80μm x 44μm corresponding to a fill factor of 34%. The photodetector employs three additional n-type implants as described for the 360x360-element VHFR image sensor. The sketch of the photodetector is illustrated in Figure 6.1. A detailed simulation analysis is performed for the last (inner) implant stage in order to utilize the channel widening effect to speed up the carrier transport in this region. A tapered shape for the layout of the last implant stage is proposed by the author according to the results obtained by 2D device simulations were performed for both A-A' and B-B' cross-sections, as shown in Figure 6.1.

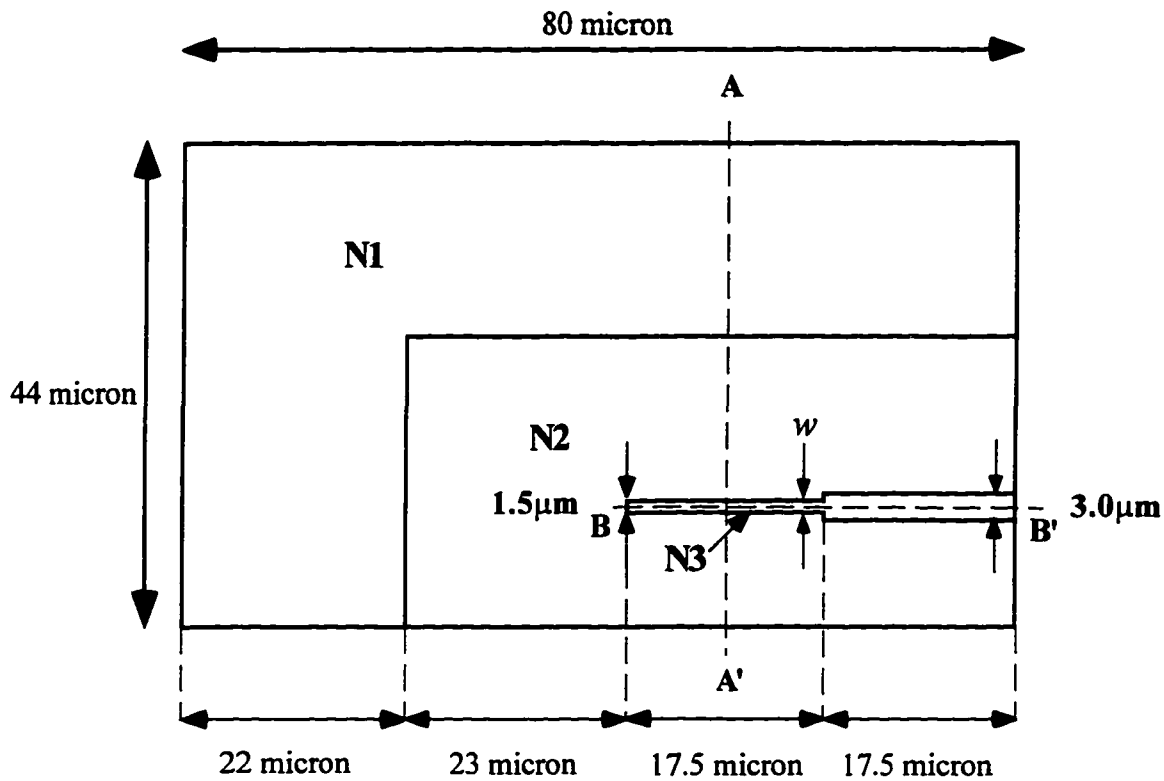


Figure 6.1 *Sketch of the photodetector structure.*

The nominal width of the last channel implant stage is marked with *w* in this figure. Results obtained from the A-A' with varying values of *w* were applied as initial condition to the B-B' to solve for the carrier transit time in this implant region.

6.2.1 Simulation of the Cross-section A-A'

Figure 6.2 illustrates the 2D structure used for device simulation across A-A'. In order to demonstrate the effect of channel widening on potential profile of the photodetector, *w* was varied from 1.0μm to 6.0μm. The potential profile obtained across A-A' of the photodetector for different values of *w* is illustrated in Figure 6.3. In this figure, the most positive potential profile corresponds to the widest implant region with *w* of 6.0μm.

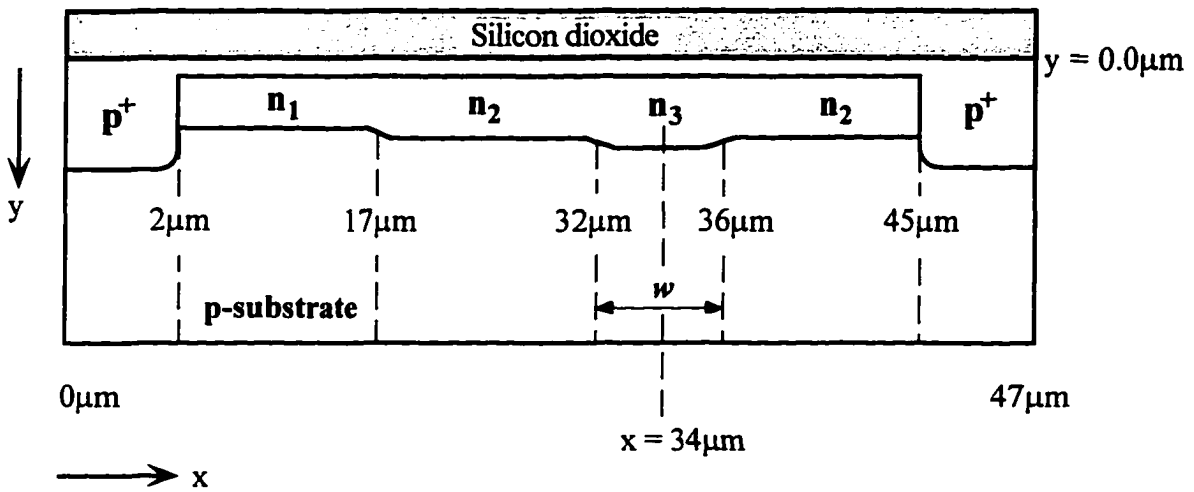


Figure 6.2 *2D structure defined for simulation of potential profile at A-A' for w=4μm.*

The next highest potential profile belongs to the structure with *w* decreased from 6.0μm to 5.0μm. By inspection of these two curves, it can be concluded that from 6.0μm to 5.0μm, there is no significant decrease in the potential maximum in the middle of the last implant stage (x=34.0μm); therefore, the channel with 6.0μm width can be assumed as wide channel so that no further widening of the implant stage was analyzed. The following simulations across A-A' were performed for decreasing values of the width *w* from 6.0μm to 4.0μm with 1.0μm steps and from 4.0μm to 1.0μm with 0.5μm steps.

Figure 6.4 illustrates the channel potential maximum in the center of the last implant stage (x=34.0μm) as function of the width *w* of this implant stage. This result demonstrates an increase in potential maximum from 1.624V for 1.5μm wide implant region to 1.675V for 3.0μm wide implant region. The ΔV obtained by channel widening from 1.5μm to 3.0μm is 0.051V.

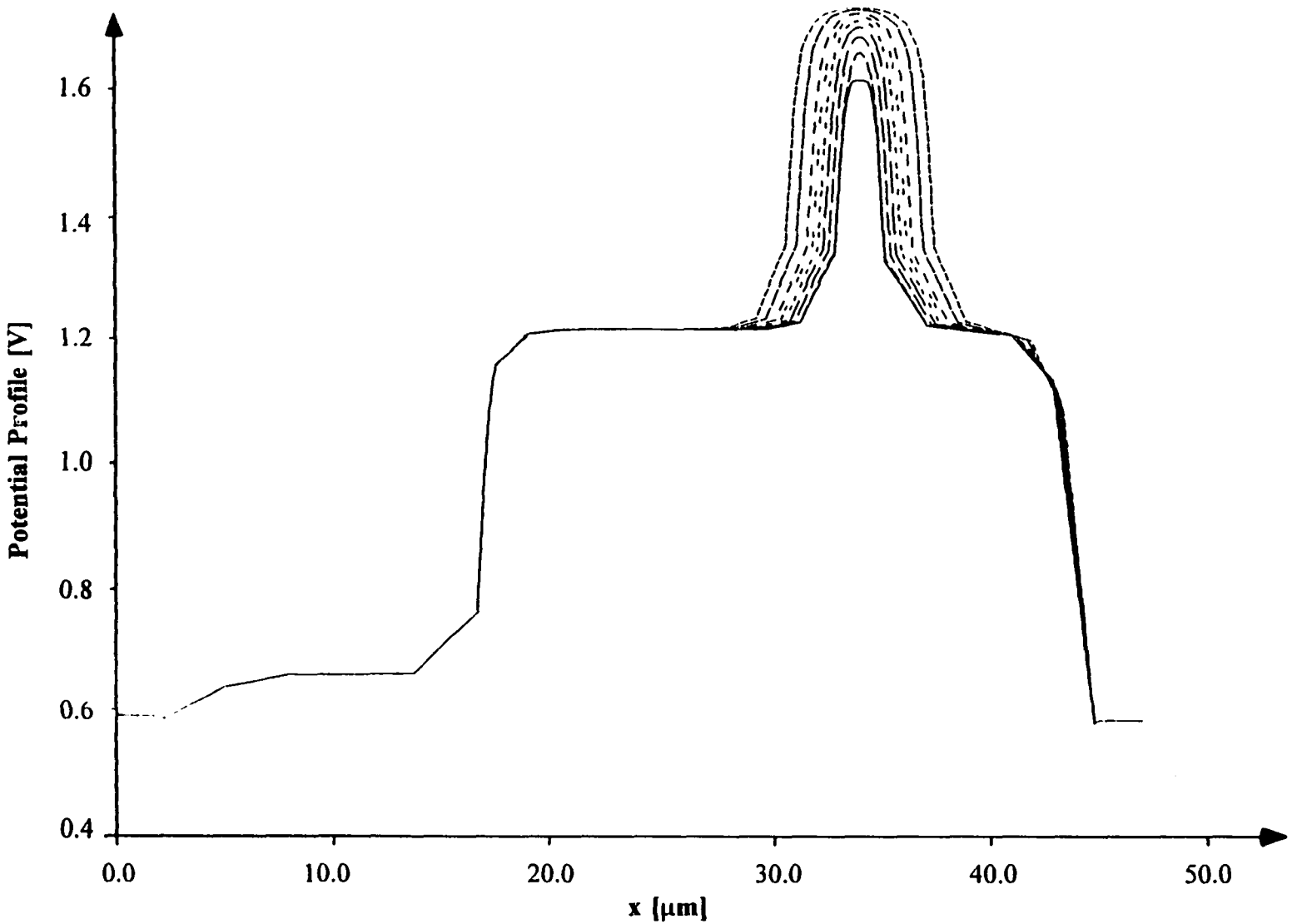


Figure 6.3 *Potential profile for varying width w of the last photodetector implant region (y≠0.0).*

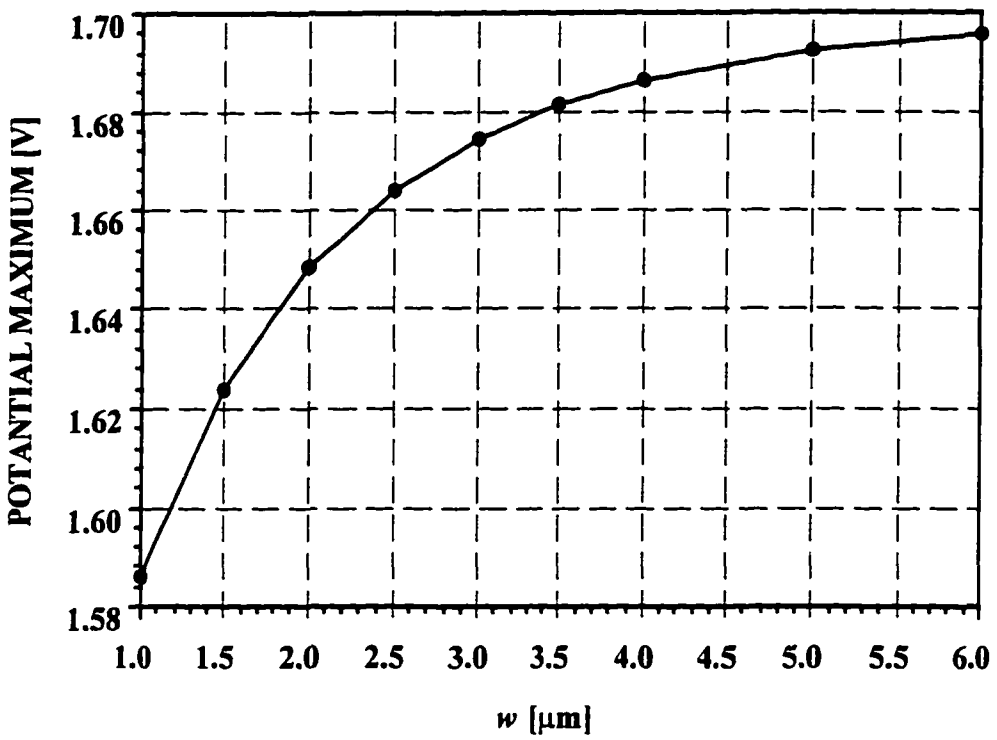


Figure 6.4 *Variation of potential maximum as function of the width w of the last implant region.*

The increase in ΔV becomes less significant for wider implant regions which is about 0.02V for widening from 3.0μm to 6.0μm and can be therefore neglected.

6.2.2 Simulation of the Cross-section B-B'

The obtained values of channel potential maximums with varying width *w* of the last implant region from the simulation across the A-A' were used to adjust the potential profile across the B-B'. Simulations were performed for three cases:

(a) for a wide implant region,

(b) for a tapered implant region with four steps, and

(c) for a tapered implant region with two steps.

The top view of these structures are shown in Figure 6.5.

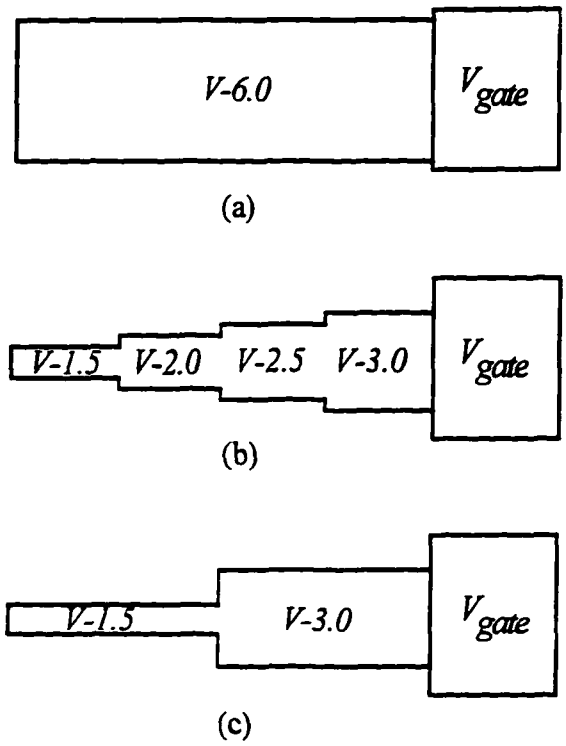


Figure 6.5 *Top view: (a) Wide implant region, (b) Tapered implant region with four steps, (c) Tapered implant region with two steps.*

The potential profile across B-B' adjusted to the potential difference ΔV as function of *w* varying from 1.5μm to 3.0μm for a tapered layout with two steps is illustrated in Figure 6.6. In this figure, ΔV1, ΔV2 and ΔV3 correspond to potential steps of 0.02404V, 0.01499V and 0.01057V, respectively, obtained by widening the implant region.

Figure 6.7 illustrates the potential profile across B-B' for a tapered implant region with two steps and a potential well adjacent to the photodetector region. The potential well is obtained under the charge collecting gate G_1 which was kept ON during the charge detection in this analysis. ΔV1, ΔV2 and ΔV3 correspond to potential steps of 0.45V, 0.05V and about 2.5V in this figure, respectively. ΔV2 demonstrates clearly the gradual increase of the potential profile due to the channel widening, whereas ΔV1 is obtained as the potential step by the multi-implant structure.

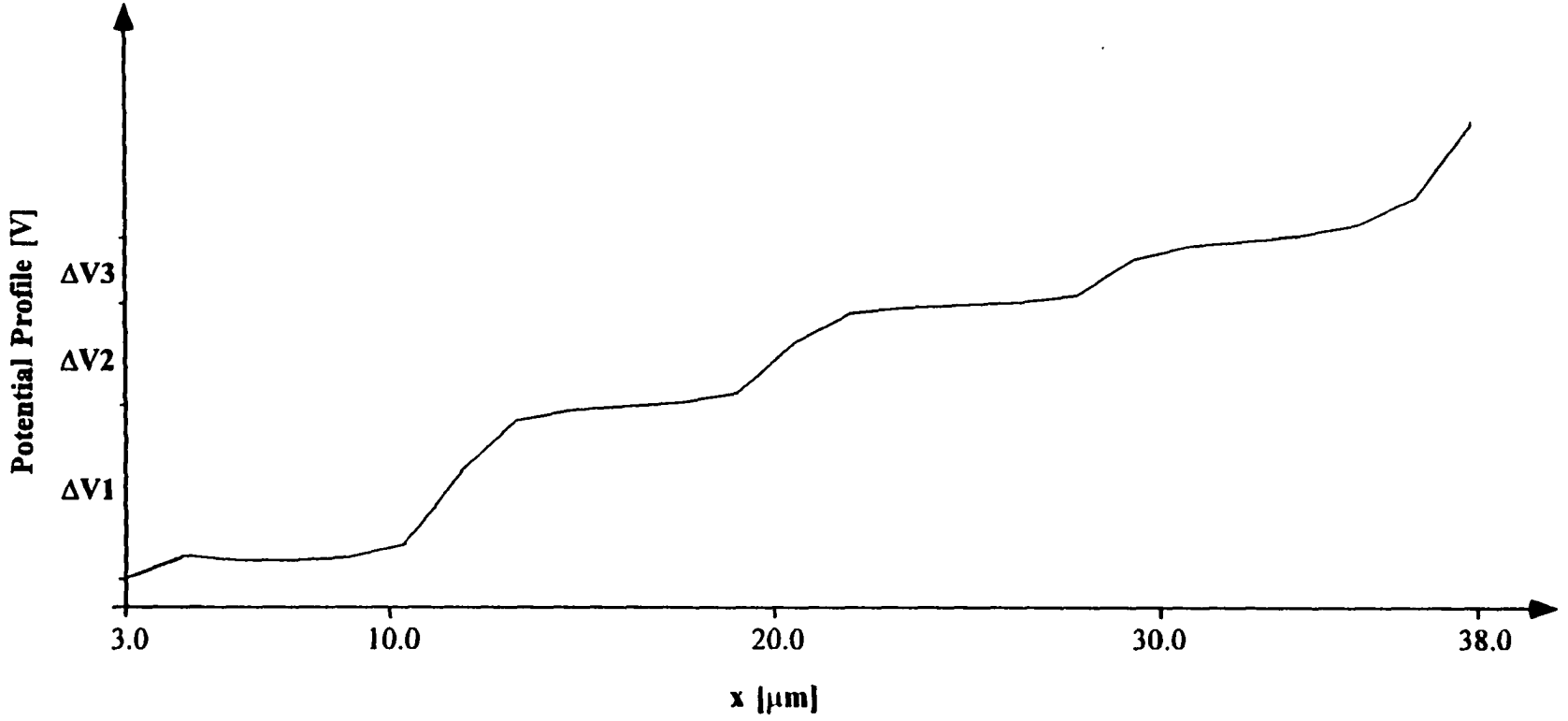


Figure 6.6 *Potential profile across B-B' with adjusted voltages for the last implant region consisting of four steps (y≠0.0).*

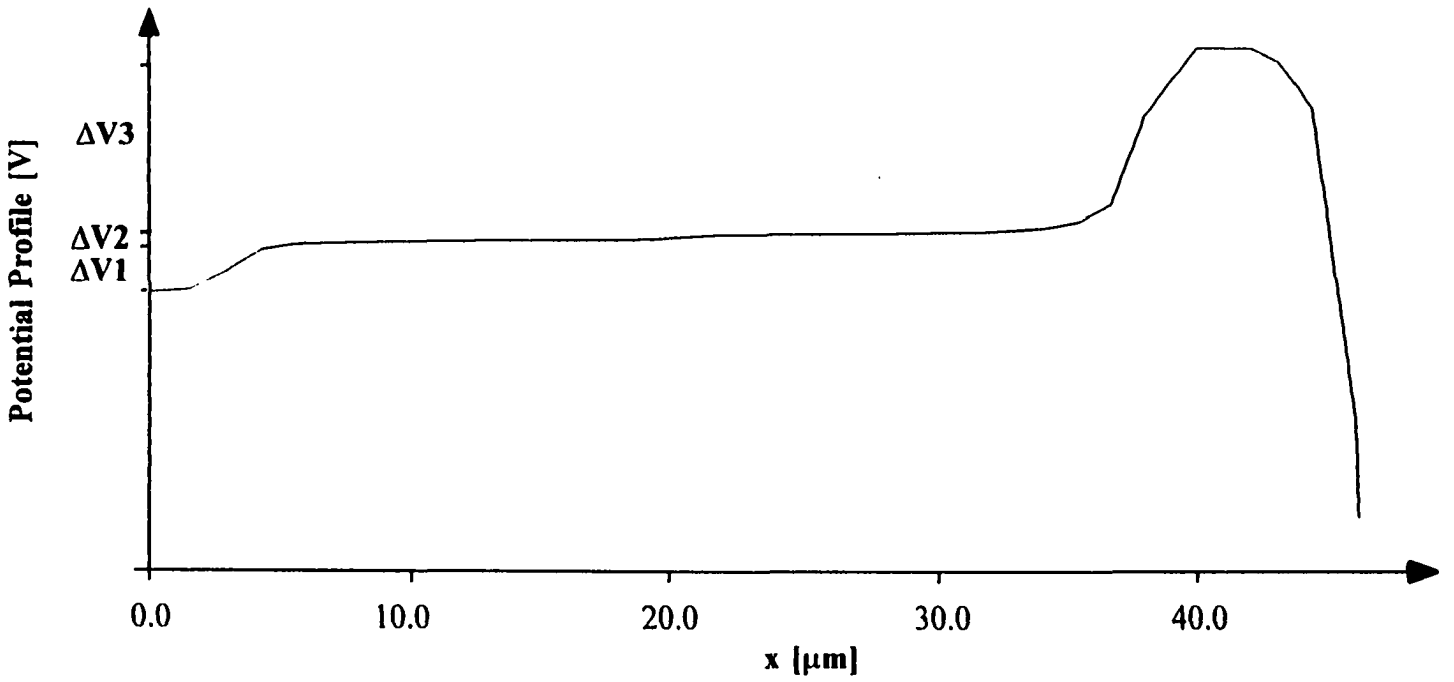


Figure 6.7 *Potential profile across B-B' of the last photodetector implant region with two steps adjacent to the charge collecting gate G_1 which is biased to a positive voltage ($y \neq 0.0$).*

6.3 Simulated Effect of the Tapered Shape on Carrier Transit Time

The photogeneration of the electrons and the charge transfer time from the photodetector region into the charge collecting well was simulated for the three cases described in the previous section. The results obtained by this analysis are shown in Figure 6.8 for all three shapes of the last implant region. Inspection of this figure shows that the time required for the electrons to diffuse through the 35.0μm long implant region is about 745ns. However, the carrier transfer is much faster for the other two structures; the decay of photogenerated electrons from 1500 electrons/μm up to 1 electron/μm in this region with the tapered shape is about 400ns.

The results presented in Figure 6.8 for three cases clearly demonstrate that gradually widening the width *w* of the last implant stage from 1.5μm to 3.0μm speeds up the carrier transfer in this region and provides an improvement in transit time of the photogenerated electrons by a factor of two. The actual layout was designed accordingly by widening the implant region in two steps starting from 1.5μm and ending at 3.0μm at the edge of the charge collecting gate G_1.

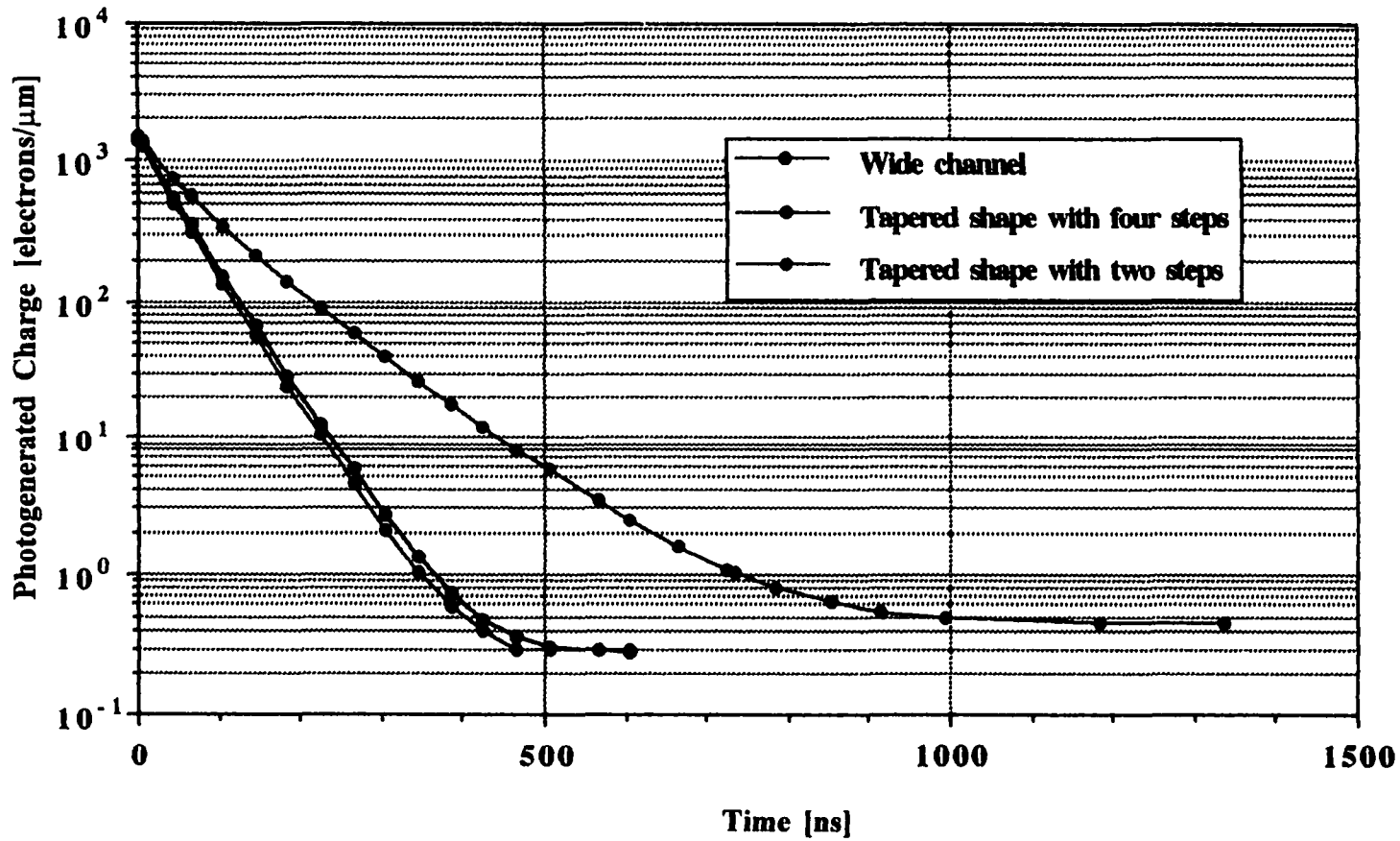


Figure 6.8 *Charge decay after the illumination is terminated for the three different cases of the last photodetector implant region.*

CHAPTER 7

3D ANALYSIS OF THE CHARGE HANDLING CAPACITY

7.1 Generation of the 3D Structure

The charge handling capacity of the Very High Frame Rate imager is simulated using 3D process and device simulators [46], in order to include the 3D edge effects into the obtained results. The use of this simulation also provides results for the charge confinement in the potential well which is surrounded by barrier wells and the channel-stop regions at the same time.

Figure 7.1 illustrates the contour of the structure defined for 3D simulation of the Very High Frame Rate image sensor with 3.0μm channel width and 1.5μm channel length. This structure consists of a uniformly doped p-type silicon substrate and a 350Å thick thermally grown silicon dioxide layer. To build the dual channel dielectric, a 650Å silicon nitride layer is deposited on top of the silicon dioxide. There are three overlapping poly silicon gate electrodes, poly-1, poly-2 and poly-3 as shown in this figure which are separated by 1400Å thick silicon dioxide layer from each other. Finally, there is a passivation layer of BPSG with 0.8μm thickness that covers the whole surface.

In order to generate the 3D structure, the process simulator Prophet was used. The mesh profile of this structure is illustrated in Figure 7.2. The dimensions of the structure are 4.5μm in y-direction, 4.0μm in z-direction. The depth of the structure is 6.0μm which is the -x direction. The mesh profile shown in this figure consists of about 20000 nodes. Figure 7.3 illustrates the sketch of the top view of the structure corresponding to the yz-plane. The n-doping for the buried channel was created in the rectangular area defined between 2.5μm to 4.0μm in z-direction and 0.0μm to 4.5μm in y-direction. The region outside of the n-type buried channel implant functions as SCCD and serves as channel-stop.

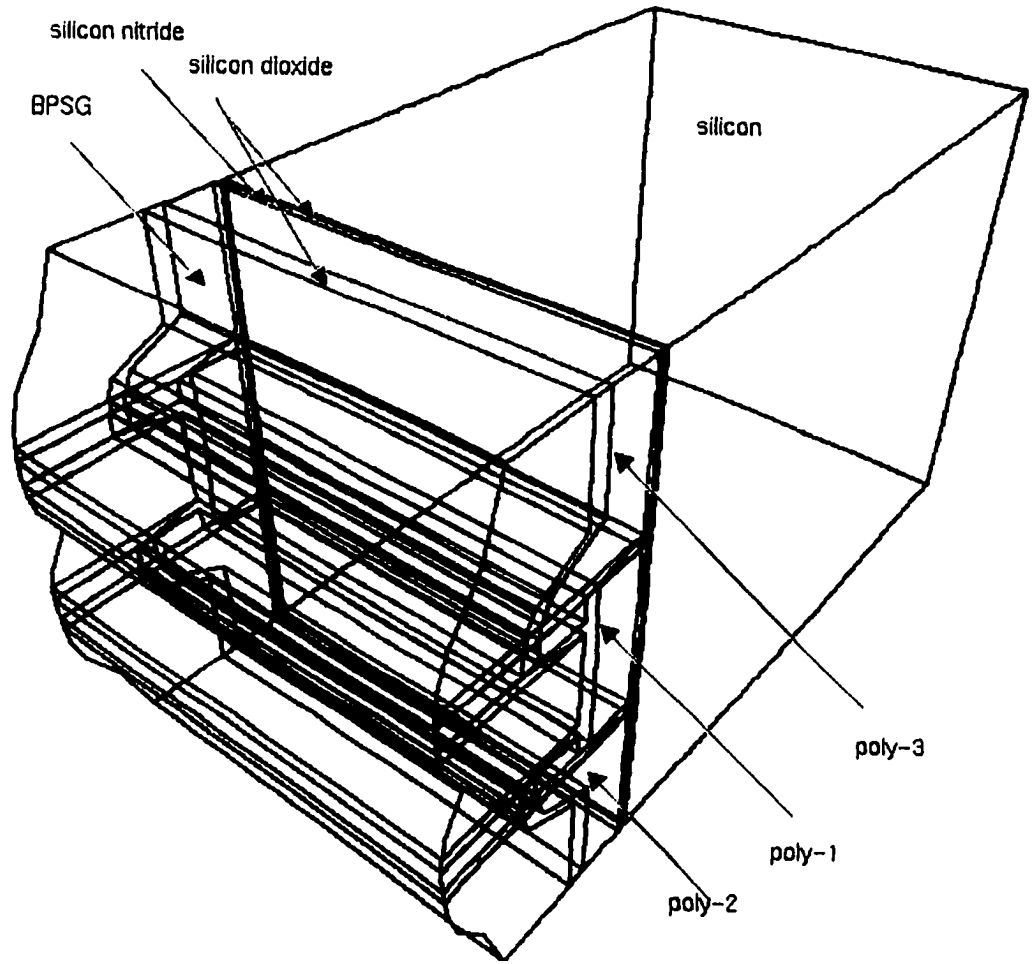


Figure 7.1 *Contour of the 3D structure generated by the process simulator PROPHET.*

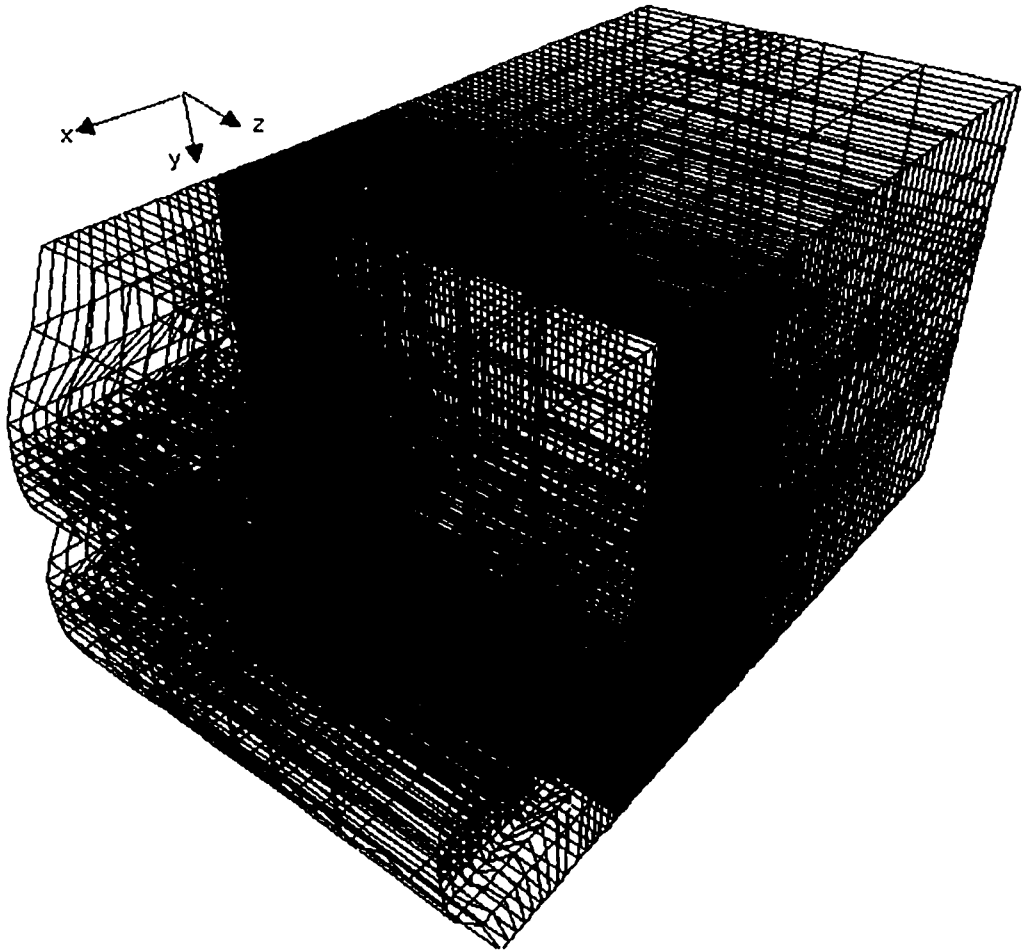


Figure 7.2 *Mesh profile of the 3D structure.*

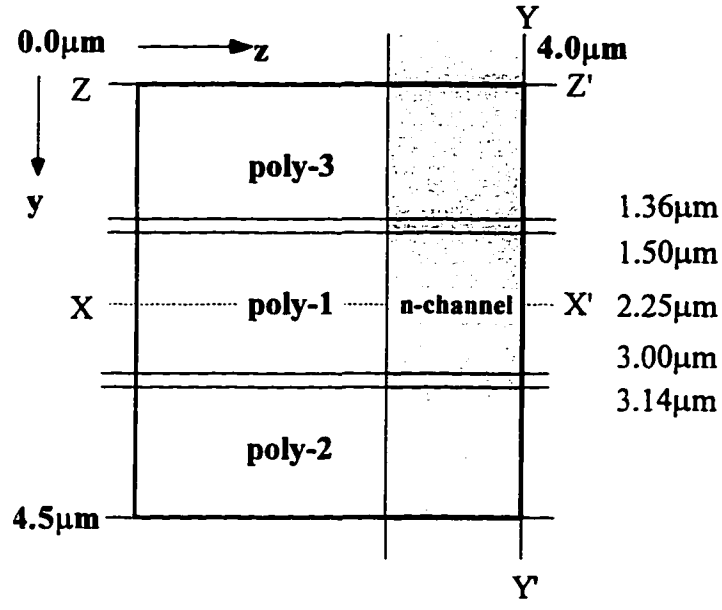


Figure 7.3 *Sketch of the top view (yz-plane).*

7.2 Doping Profile of the Buried Channel

Dual channel implant of Arsenic and Phosphorus were employed with the process parameters of high BCCD implant dose option. All temperature steps of the fabrication process have been included into the generation of the 3D structure.

In Figure 7.4 only the silicon region is displayed in order to demonstrate the 3D net doping profile. The 2D cut-line along Y-Y' (z=4.0μm) is illustrated in the next figure (Figure 7.5). The junction depth obtained by the 3D process simulation with Prophet is about 1.0μm. The channel-stop region adjacent to the n-channel can be seen also in Figure 7.6 which illustrates the 2D net doping profile along the cut-line Z-Z' (y=0.0μm).

A 1D net doping profile obtained by dual buried channel implant of Arsenic and Phosphorus is as shown in Figure 7.7 which is in good agreement with the doping profile obtained using Suprem III as illustrated in Figure 3.4.

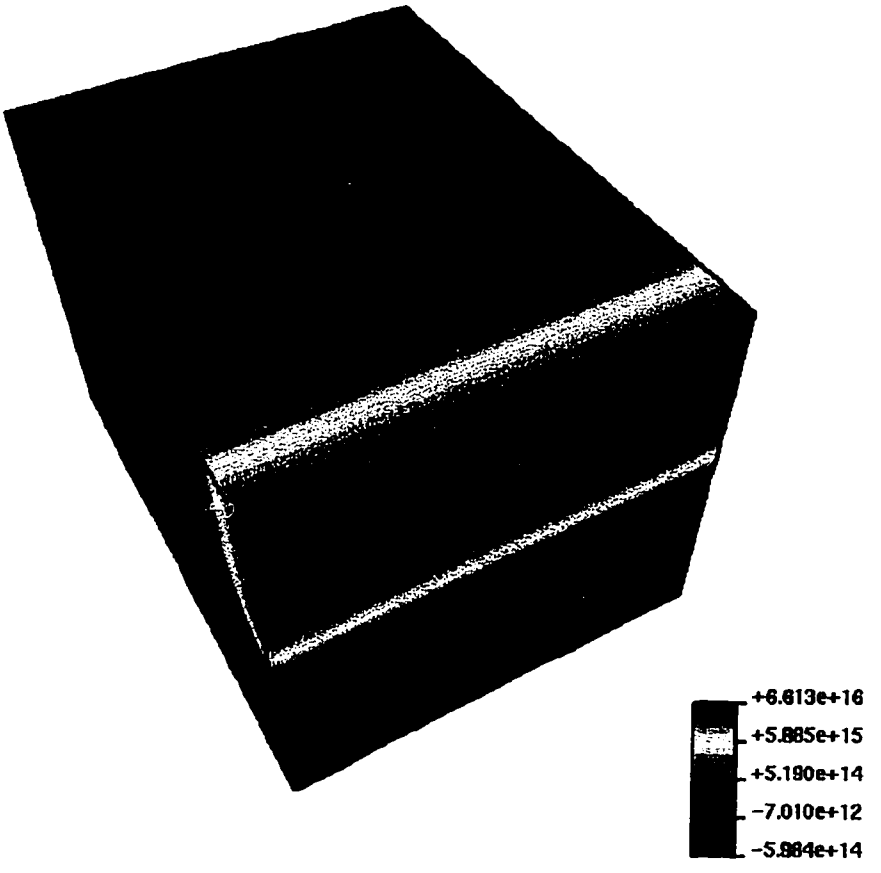


Figure 7.4 *3D net doping profile.*

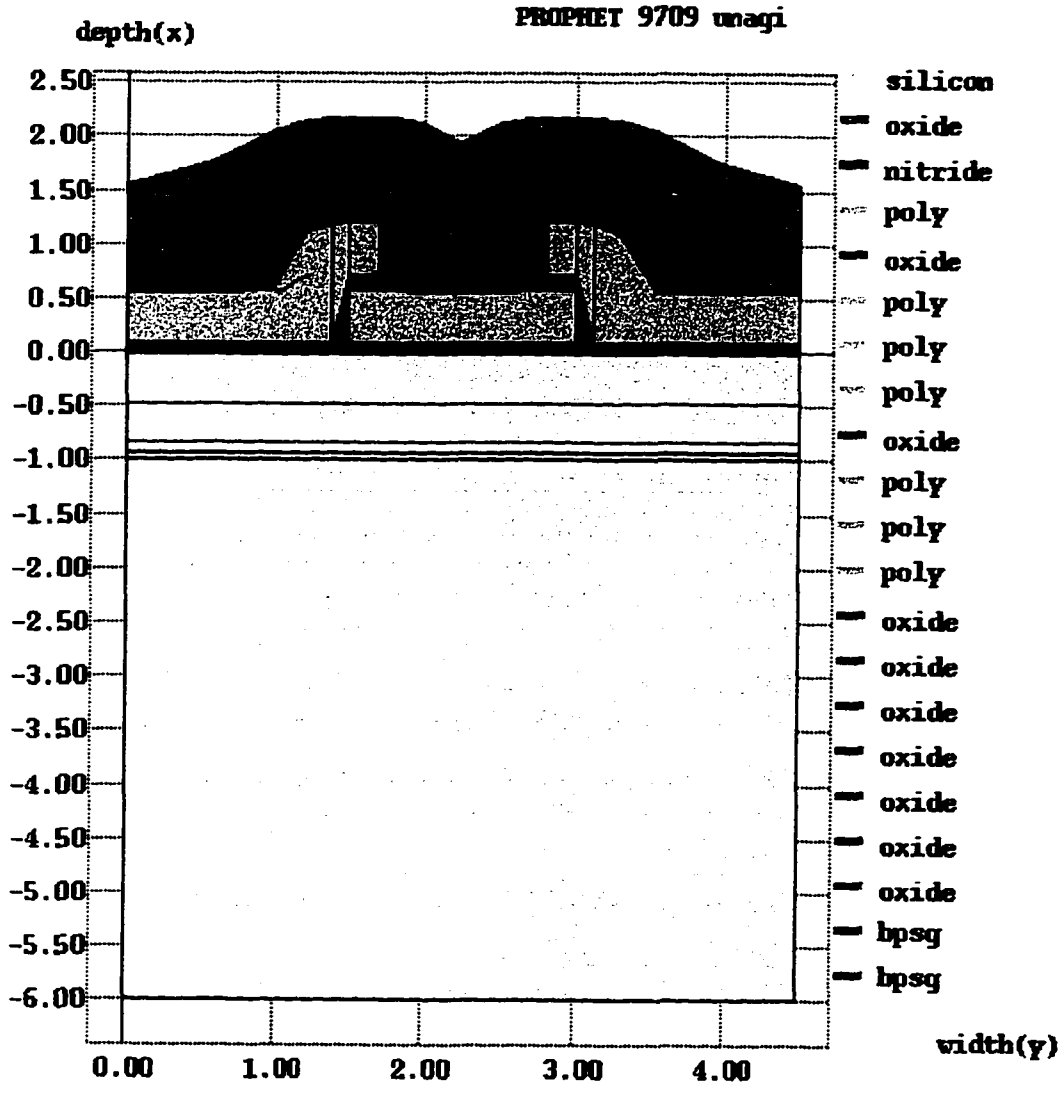


Figure 7.5 *2D cut-line along Y-Y'.*

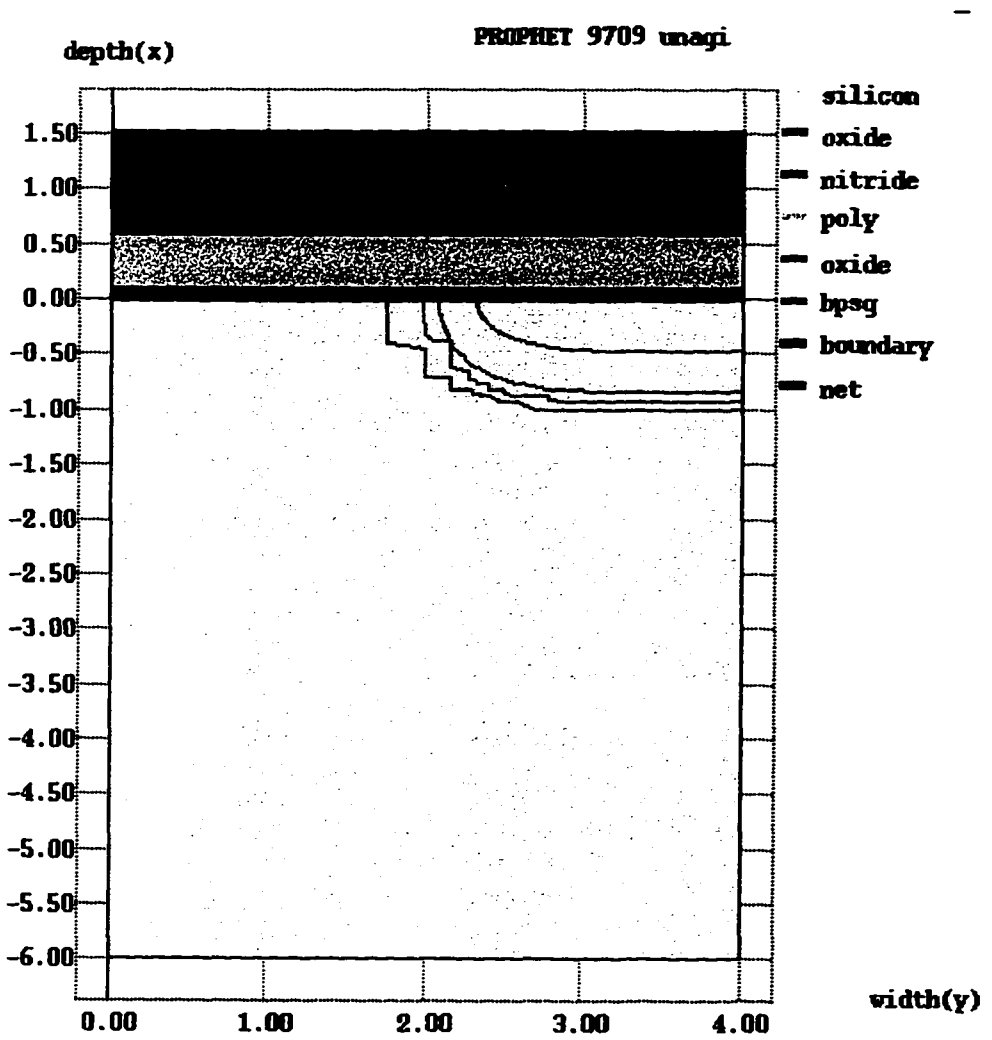


Figure 7.6 *2D cut-line along Z-Z'.*

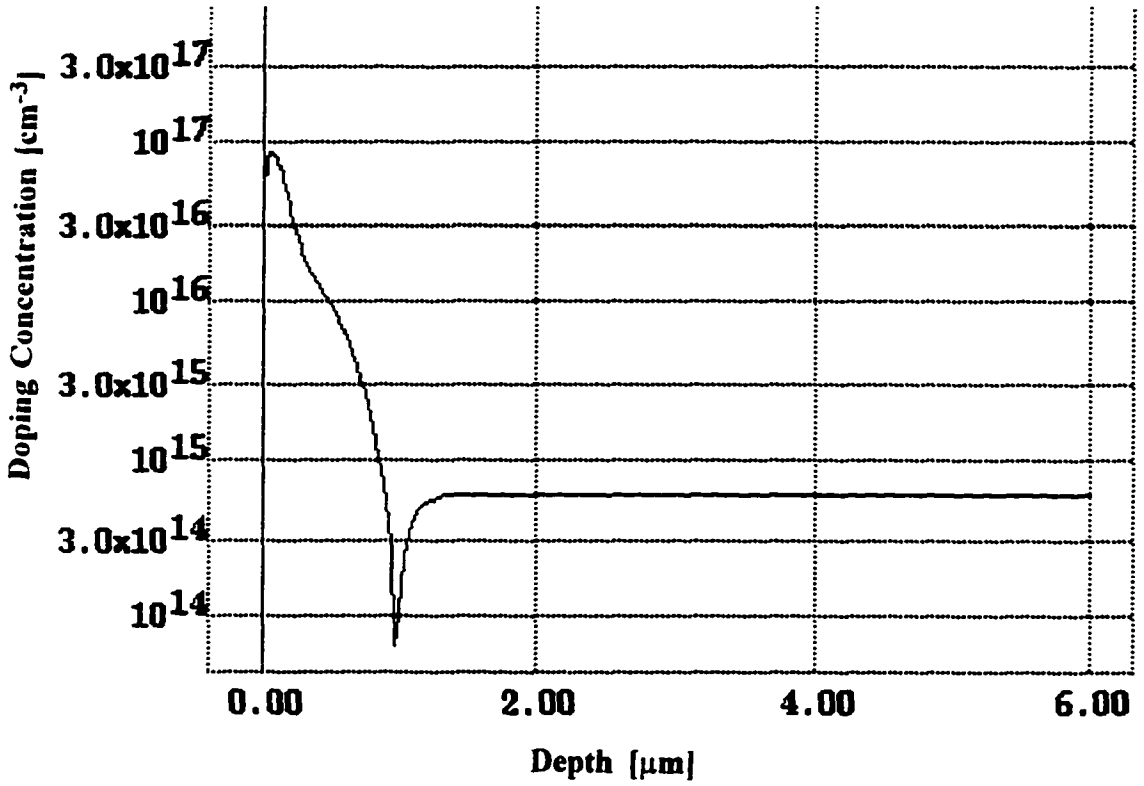


Figure 7.7 *1D net doping profile.*

7.3 3D Charge Distribution

Figure 7.8 illustrates the 3D structure used for device simulation with Padre. It consists of the uniformly doped p-type silicon substrate with n-channel for the BCCD operation, dual channel insulator layers of silicon dioxide and silicon nitride, and three gate electrodes which are defined on the surface of the silicon nitride layer as described in the previous section.

To simulate the 3D charge handling capacity, the poly-1 gate electrode which is placed from 1.5μm to 3.0μm in y-direction and from 0.0μm to 4.0μm in z-direction is biased to a positive voltage. The other two gate electrodes, poly-2 and poly-3 which are located from 0.0μm to 1.36μm and from 3.14μm to 4.5μm in y-direction, and both from 0.0μm to 4.0μm in z-direction, respectively , are kept at a sufficiently low voltage so that the n-buried channel under these gate electrodes is driven into the pinning condition.

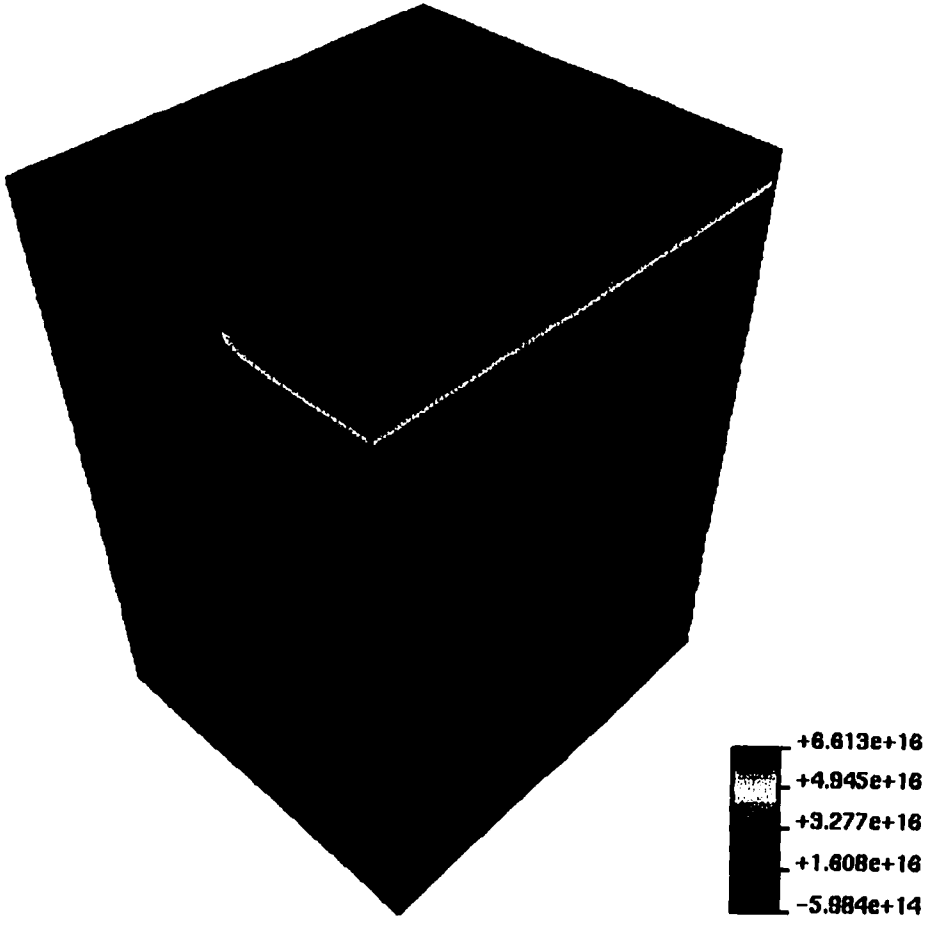


Figure 7.8 *3D structure used for device simulation with PADRE.*

Figure 7.9 illustrates 1D potential profiles as function of the depth (-x axis) of the full potential well in (a), barrier well in (b) and SCCD region under positively biased gate electrode in (c). The channel potential under pinning gate electrode is about 3.4V in this figure which is consistent with the previously obtained value by 2D simulation using Pisces IIB. The charge is accumulated in the buried channel region under the positively biased gate electrode and the area outside of this region is completely depleted of electrons. The voltage difference between the surface potential and the maximum of the channel potential is large enough so that buried-mode operation is ensured. The 2D charge confinement can be also seen in Figure 7.10 which illustrates the potential profiles across the cut-line Y-Y'. The simulation has verified that the design satisfactorily meets the full well criterion defined by Equation 4.2 given in Chapter 4.

The channel-stop barrier height was obtained as about 3.8V from 2D simulation using Pisces IIB in Chapter 4 (Figure 4.22). Inspection of the curves illustrated in Figure 7.9 (a) and (c) concludes that the 3D results are very consistent; the voltage difference between the maximum of the channel potential of the full well and the SCCD potential is about the same. The channel-stop barrier height is further illustrated by the potential profile across the cut-line X-X' in Figure 7.11. The variation of the voltage starting from the depleted SCCD region to the full potential well in the buried channel region is shown in this figure. The mask edge of the implant is at 2.5μm; it can be seen that the potential is flat almost to the edge, meaning that the channel can be considered almost as wide as its mask dimension. Visually the channel width reduction is about 0.25μm which will be quantified next.

The charge handling capacity is obtained as about 19500 electrons for this design as result of 3D simulation with Padre which includes the effect of channel narrowing, in addition to the effect of the short channel as described in Chapter 4. By the earlier 2D simulation as illustrated in Figure 4.14 the total charge that can be confined in the potential well was calculated as about 23000 electrons. The difference is due to narrow

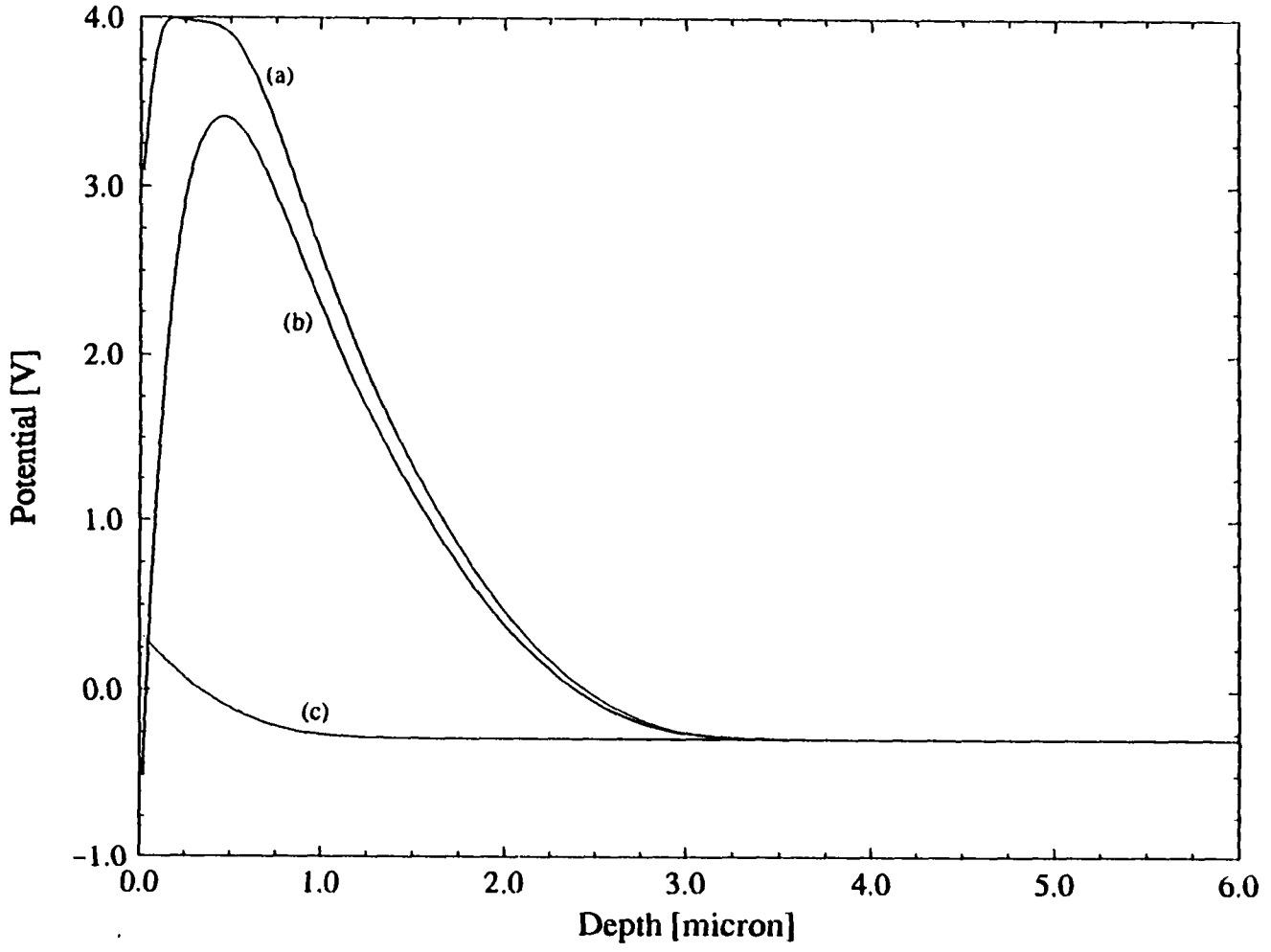


Figure 7.9 *1D potential profiles of BCCD and SCCD regions as function of depth: (a) Full potential well, (b) Barrier well, (c) Channel-stop.*

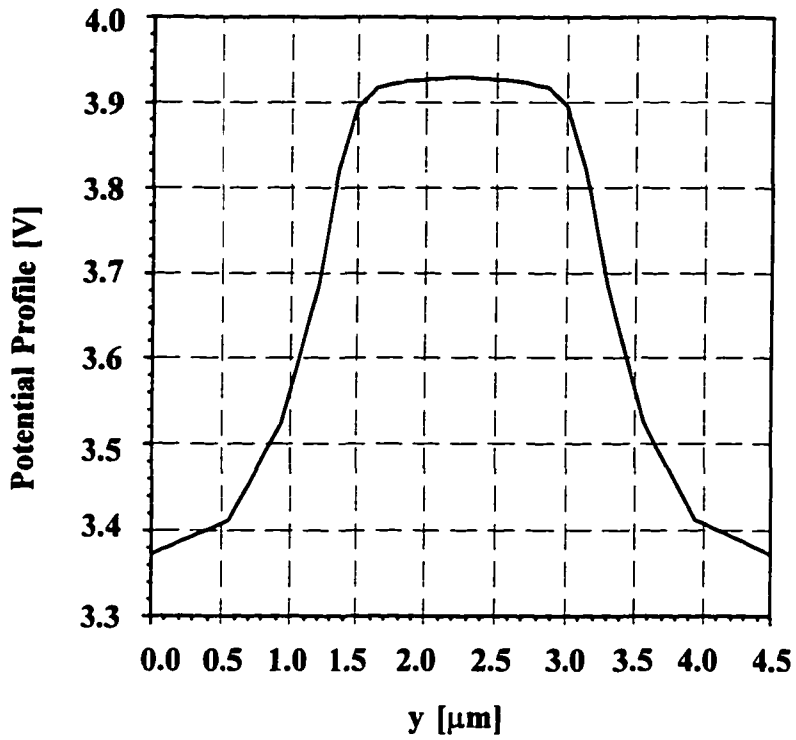


Figure 7.10 *Potential profile across the cut-line Y-Y'.*

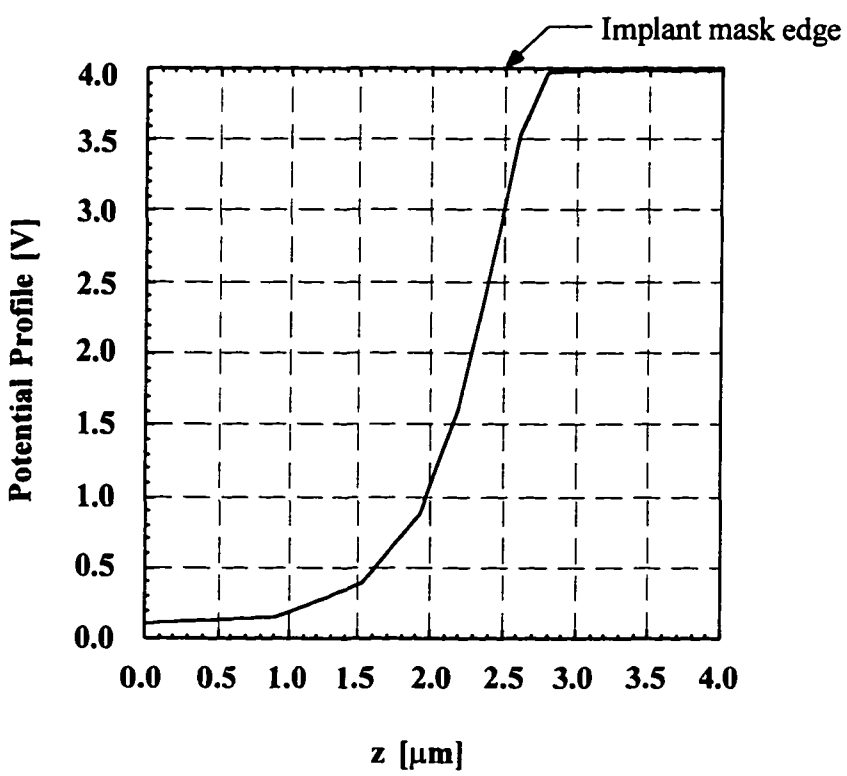


Figure 7.11 *Potential profile across the cut-line X-X'.*

channel effects. The ratio 19500/23000 gives an effective channel width of 1.25μm for a drawn channel of 1.5μm, or a 0.25μm reduction in effective channel width. This confirms the visual estimate made above.

Finally, 3D potential profile in this structure is illustrated in Figure 7.12 (a). The buried channel region under the middle gate electrode biased with V_{G1} has the highest potential in the 3D structure corresponding to the full potential well where electrons are located. The resulting 3D charge distribution is demonstrated in Figure 7.12 (b).

In summary, the 3D calculations show that the narrow channel effect and the short channel effect add linearly. This simplifies the analysis and allows a 2D estimate of the short channel effect to arrive at a good estimate of the total charge handling capacity. The narrow width effect was found to give rise to about 0.25μm reduction in this technology.

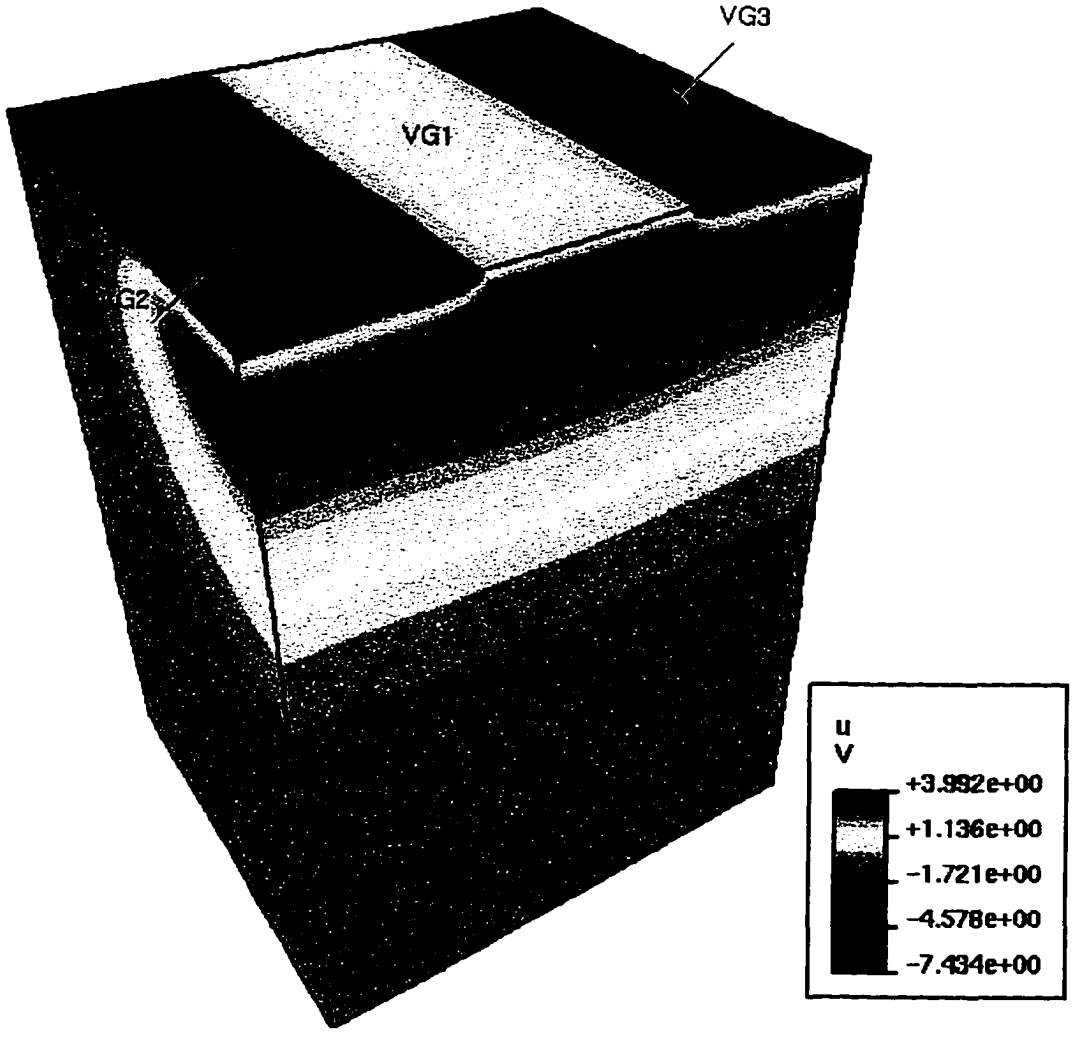


Figure 7.12 (a) *3D potential profile illustrating the full potential well under gate electrode poly-1 biased to a positive gate voltage VG1.*

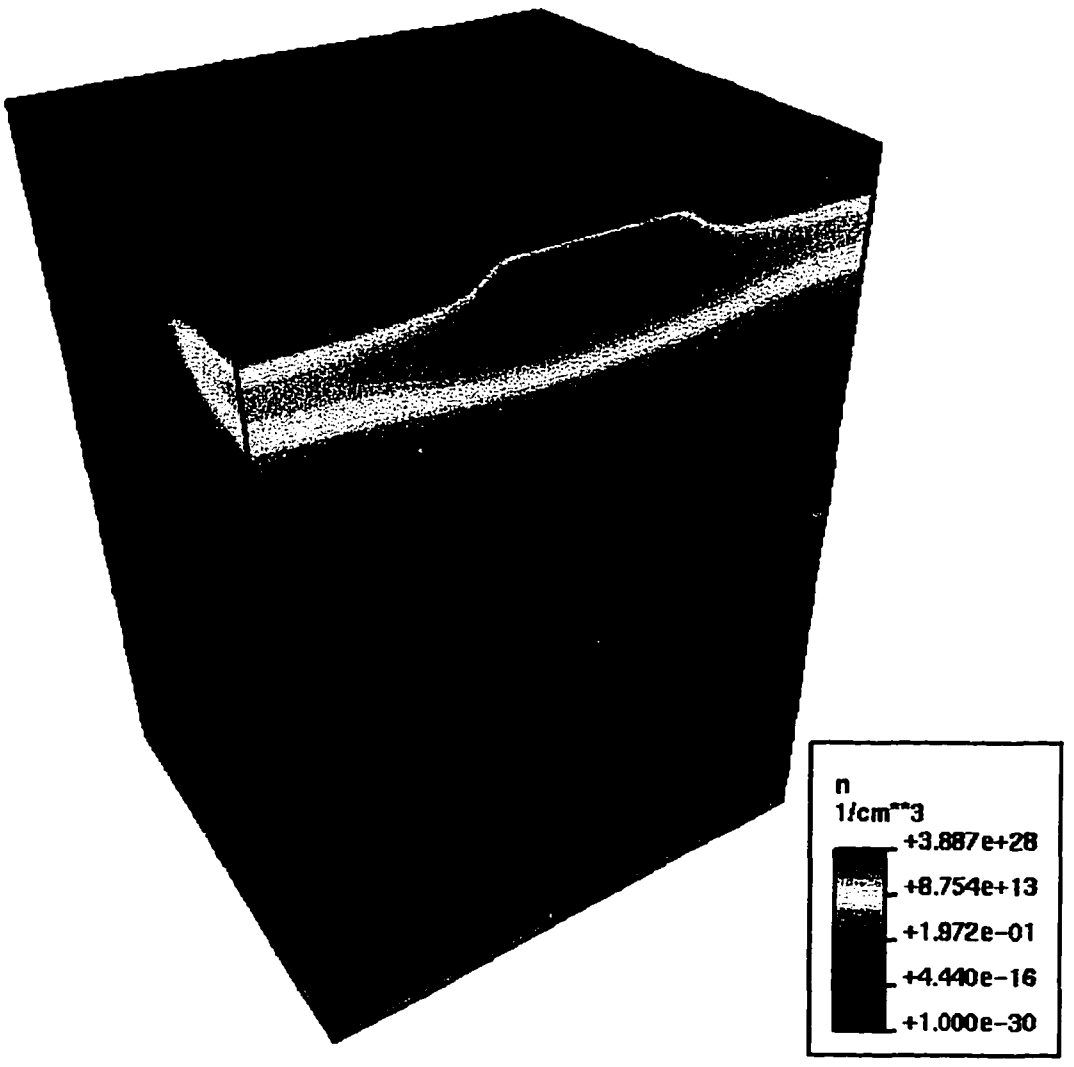


Figure 7.12 (b) *Distribution of the electrons in the 3D structure.*

CHAPTER 8

SUMMARY AND CONCLUSIONS

This dissertation describes the comprehensive design, process and performance simulations of the very high frame rate CCD burst-image sensors. Efforts were made to verify available experimental data taken from slower speed devices using simulation in order to be able to predict and optimize the performance of the future higher speed designs. Novel design strategies were introduced in two main parts: characterization and design of the BCCD registers, and design of the pinned-buried high-speed photodetectors with multiple n-type implants. Discussions in this thesis focused both on the initial design, which is the 360x360-element Very High Frame Rate image sensor and the design of the next generations; the 180x180-element Very High Frame Rate imager and the 64x64-element Ultra High Frame Rate imager.

The 360x360-element Very High Frame Rate image sensor was fabricated at David Sarnoff Research Center with a complicated fabrication process that involves four-layers of polysilicon, three layers of metal and eight implants steps. The design, construction and operation were reviewed including the process specifications. These concepts were related to the simulation results illustrating the cross-sectional view at certain cut-lines of the pixel to give a better understanding of the pixel design. The topography was perfectly adjusted to the SEM photographs taken at David Sarnoff Research Center with the purpose to predict the topography of the pixels of next phases at critical regions. The test results obtained at Princeton Scientific Instruments demonstrated an effective frame rate of 8.33×10^5 frames per second and a charge handling capacity of about 11000 electrons per pixel. Based on the results of the initial design, simulations were carried out to verify the experimental data, leading to new suggestions in optimizing performance. The 180x180-element Very High Frame Rate image sensor was designed in order to obtain higher device yield, higher charge handling capacity and increased fill

factor. This sensor is currently being fabricated at David Sarnoff Research Center. It will be followed by the next phase of the high framing rate imager; the 64x64 element 10 million frames per second Ultra High Frame Rate image sensor.

The behavior of the buried-channel CCD memory registers was analyzed thoroughly and compared with the experimental results. These include the analysis of the channel potential variation as function of the gate voltage and the dielectric layer thickness, providing the pinning gate voltages that should be applied for clocking the BCCD registers. The characteristics of the channel potential variation as function of applied gate bias for the two different options of the buried channel implant dose were performed and consistent results were obtained with the experiments. As a next step, the channel potential variation was analyzed as a function of gate dielectric thickness and its effect was observed on the charge handling capacity of the imager. The effect of reduction in channel length on charge handling capacity was demonstrated by the 2D device simulations. The difference between the measured value of the charge handling capacity and the predicted value obtained by device simulations were explored by 2D and 3D simulations. The 3D analysis demonstrates the effective width of the buried channel providing correction of the 2D results according to the channel narrowing effect. Furthermore, the dependence of the charge handling capacity on the dielectric layer thickness reveals useful information about the actual thickness of the dielectric layer after several steps of poly silicon gate formation.

A design strategy was developed and described in order to construct the high-speed pinned-buried photodetector structure with multiple n-type implants in addition to the buried channel implants. The additional implants provide a stair-case potential profile which speeds up the transit time of the photogenerated electrons through the photodetector region. The effect of the buried channel implants on potential profile was discussed by 2D simulations. New values for the additional implants were suggested. The response of the photodetector to pulsed illumination was obtained and the design strategy

was described. The photodetector for the 10 million frames per second operation employs six implant regions with 8.8μm distance between each implant. The entire photodetector readout operation was demonstrated.

A novel tapered implant mask for charge collection was analyzed. The design takes advantage of widening the implant region from 1.5μm to 3.0μm resulting in a gradually increasing potential profile. These results were applied to the photodetector design of the 180x180-element Very High Frame Rate imager and an improvement of a factor of two in the transit time of the photogenerated electrons in this region was demonstrated. Since the photodetector is a pinned-buried structure, various approaches were used to adjust the potential profile according to the results obtained from the channel widening effect.

3D results of the charge handling capacity provided consistent results with the 2D characterization of the BCCD register. The effective width of the buried channel was obtained by this simulation and its effect on charge handling capacity was discussed. As result of these simulations, the 3D distribution of the charge and the potential profile were obtained and illustrated. The edge effect was found to give rise to about 0.25μm reduction in the nominal width defined by the implant mask in this technology.

The analysis of the BCCD memory registers and the photodetector readout characteristics of the multi-implant high-speed pinned photodetector leads to the conclusion that the design of the 10^7 frames per second Very High Frame Rate burst-image sensor is realizable. Furthermore, the simulation results of the photodetector readout with multiple implants indicate that operation rates beyond 10^7 frames per second can be achieved for transferring the charge from the photodetector into the BCCD memory register.

CHAPTER 9

SUGGESTIONS FOR FUTURE RESEARCH

The performance of the high-speed photodetectors were carried out using approximate 2D analysis, due to the difficulty in carrying out transient analysis of large 3D devices. As computer hardware and simulators improve, the exact calculations of 3D simulations will replace the 2D estimates. It will be interesting to analyze and improve the design methods from the following aspects:

- The photodetector readout operation should be obtained by the 3D simulations in order to include the effects associated with the geometry. Photodetector readout operation with 100ns frame time could be analyzed and compared with the 2D results given in this research.
- The effect of the tapered geometry for the last implant region could be analyzed with the 3D simulation tools and compared with the 2D results. The feasibility of applying a similar geometry to the floating diffusion amplifier could be investigated in order to reduce the output amplifier noise.
- 3D simulations could be performed to study the horizontal blooming control in conjunction with the charge collection gate and the photodetector. Correct operation could be verified by applying the clock pulses to the gates and performing transient analysis.
- The effect of the reduction in gate length was demonstrated by 2D simulation results and a simulation approach was described in order to account for the fringing fields of the adjacent gate electrodes. However, the short channel effect could be investigated by 3D simulation directly so that a more accurate data for the charge handling capacity can be obtained. This will also reduce the time and effort of using the described simulation approach for this analysis.

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