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ABSTRACT

DESIGN, FABRICATION AND CHARACTERIZATION OF HIGH PERFORMANCE InGaAs/InP FOCAL PLANE ARRAYS IN THE 1-2.6 μm WAVELENGTH REGION

by
Krishna R. Linga

This research thesis describes a new $In_xGa_{1-x}As/InA_ysP_{1-y}/InP$ technology for long wavelength photodetectors and photodetector arrays. A unique and novel detector structure was designed and fabricated using Hydride Vapor Phase Epitaxy, for low leakage current photodetector arrays in the 1-2.6 μm wavelength region. Potential applications of InGaAs focal plane arrays include near-infrared spectroscopy, fluorescence, remote sensing, environmental sensing, space and astronomical applications. The unique design concepts included the step grading of InAsP layers, lower lattice mismatch between the two InAsP graded layers, lattice matched InAsP cap layer and InGaAs absorption layer, sulphur doping of InGaAs absorption layer and InAsP layers. Improved device fabrication techniques including rapid thermal annealing and precisely controlled diffusion were implemented during the processing of 1024 element linear photodetector arrays to reduce the dislocation density. An analysis of dark current, which is the critical parameter was required and is described in detail. The dark current analysis and the experimental results showed that the dark current is bulk dominated and is due to the crystal defects and dislocation density.

Each element of the focal plane array consisted of a 13 X 500 um^2 active area with an element to element spacing (pitch) of 25 um. The focal plane architecture designed had

two 512 element (left and right) multiplexers and a 1024 element detector array and was integrated in a 24 pin dual-in-line package.

A unique and novel Si read-out multiplexer was designed and fabricated using radiation hardened N-well CMOS process. Each multiplexer unit cell consisted of a capacitive transimpedance amplifier, correlated double sampling circuit, threshold non uniformity correction circuit and an output buffer stage.

Integration and testing of InGaAs focal plane arrays with cut-off wavelengths of 1.7 μm, 2.2 μm and 2.6 μm are described. The performance of the focal plane arrays was analyzed in detail and the results showed that the 10 fA dark current levels could be achievable with 1024 element InGaAs/InP focal plane arrays in the 1-2.6 um wavelength region. The dark current achieved from the test focal plane arrays was < 1 fA for 1.7 um, < 20 fA for 2.2 um and < 50 fA for 2.6 um cut-off wavelength. Radiation testing using proton, gamma and electron particle radiation on InGaAs photodetectors and photodetector arrays showed that InGaAs/InP focal plane arrays can with stand upto 15 Krad (Si) particle radiation. Comparison of the results achieved with published results of other technology (HgCdTe) operating at the same temperature shows that InGaAs/InP Focal Plane Arrays have lower dark current by a factor of 10-100.

DESIGN, FABRICATION AND CHARACTERIZATION OF HIGH PERFORMANCE InGaAs/InP FOCAL PLANE ARRAYS IN THE 1-2.6 μm WAVELENGTH REGION

by
Krishna R. Linga

A Dissertation
Submitted to the Faculty of
New Jersey Institute of Technology
in Partial Fulfillment of the Requirements for the Degree of
Doctor of Philosophy

Department of Electrical and Computer Engineering

May 1997

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APPROVAL PAGE

DESIGN, FABRICATION AND CHARACTERIZATION OF HIGH PERFORMANCE InGaAs/InP FOCAL PLANE ARRAYS IN THE 1-2.6 μm WAVELENGTH REGION

Krishna R. Linga

Dr. Durga M. Misra, Dissertation Advisor — Date
Associate Professor of Electrical and Computer Engineering, NJIT

Dr. Roy Cornely, Committee Member — Date
Professor of Electrical and Computer Engineering, NJIT

Dr. Kenneth Sohn, Committee Member — Date
Associate Chairman of Electrical and Computer Engineering, NJIT

Dr. N. M. Ravindra, Committee Member — Date
Associate Professor of Physics Department, NJIT

Dr. C. S. Wang, Committee Member — Date
Vice President, Advanced Research, Epitaxx, Inc., W. Trenton, NJ

BIOGRAPHICAL SKETCH

Author: Krishna Rao Linga

Degree: Doctor of Philosophy

Date: May 1997

Undergraduate and Graduate Education:

- Doctor of Philosophy in Electrical Engineering,
  New Jersey Institute of Technology, Newark, NJ 1997
- Master of Science in Electrical Engineering,
  New Jersey Institute of Technology, Newark, NJ 1990
- Bachelor of Science in Electrical Engineering,
  University of Mysore, Mysore, India, 1987

Major: Electrical Engineering

Presentations and Publications:

1. G.H. Olsen, S. Mason, G. Gasparian, A. M. Joshi, K. Woodruff, K. Linga, D. Rodefeld, M. Lange, F. Speer, V. S. Ban and G. Erickson, "Room temperature properties of Indium Gallium Arsenide detectors optimized for 1.8, 2.1 and 2.5 um," in Proc. IEEE LEOS Conf., Boston, Nov. 1990.

2. K.R. Linga, G.H. Olsen, V.S. Ban, A.M. Joshi and W.F. Kosonocky, "Dark current analysis and characterization of $In_xGa_{1-x}As/InAs_yP_{1-y}$ graded photodiodes with $x > 0.53$ for response to longer wavelength (> 1.7 um)," IEEE Journal of Lightwave Technology, Vol. 10, No. 8, pp. 1050-1055, Aug. 1992.

3. K.R. Linga, A.M. Joshi, V.S. Ban and S. Mason, "1024 element $In_xGa_{1-x}As/InAs_yP_{1-y}$ detector arrays for environmental sensing from 1 um to 2.6 um," Proc. SPIE, Vol. 2021, pp. 90-97, July 1993.

4. N.B. Urli, V.S. Ban and K. Linga, "Defects in infrared detectors based on In-Ga-As alloys," Proc. 4th International Conf. on New Tech., pp. 88-94, Pula, Oct. 1993.

5. W.F. Kosonocky, W. Kleinhans, C. Lau, K.R. Linga and M. Lourie, "Low-Bias CTIA Multiplexer for 1024-Element InGaAs Line Sensors," Pro. SPIE, Vol. 2226, pp. 152-171, Apr. 1994.

6. K. R. Linga, C.S. Wang, Y. Dzialowski, M. Lourie, S. Mason and W.F. Kosonocky, "High performance 1024 element InGaAs hybrid focal plane arrays from 1 to 2.6 um," Proc. Of OPTO94 Conf., pp. 1024-1030, Paris Apr. 1994.

7. A.S. Kanofsky and K. Linga, "Effects of radiation on long wavelength devices," Proc. SPIE, Vol. 2074, pp. 214-220, Aug. 1994.

8. R. McKee, D. Lampe, J. Halvis, T. Henricks, T. Wilson, W. Kleinhans, K. Linga, M. Lange, "Near room temperature performance of a SWIR InGaAs/Si hybrid 96X25 element TDI performance FPA," Proc. SPIE, Vol. 2746, pp. 152-161, Apr. 1996.

9. K. Linga, C.S. Wang, M. Lourie, W. Xu and W.F. Kosonocky, "High Performance InGaAs/InP Focal Plane Arrays," POEM Annual Review Meeting, Princeton University, March 1997.

10. K. Linga, C.S. Wang, W.F. Kosonocky and D. Misra, "Noise Sources in Long Wavelength InGaAs/InP Focal Plane Arrays," To be published, 1997.

In memory of
Walter Kosonocky

ACKNOWLEDGMENT

I wish to express my sincere gratitude to Dr. Walter F. Kosonocky and Dr. Durga Misra for their valuable guidance, inspiration and encouragement during the entire course of this research. I am very thankful to Dr. Durga Misra for accepting to be my advisor during the difficult times and providing valuable guidance, support and reassurance. I am also thankful to Dr. Roy Cornely, Dr. Kenneth Sohn and Dr. Ravindra of New Jersey Institute of Technology and Dr. C.S. Wang of Epitaxx, Inc. for accepting to be in my committee. I am very thankful to Epitaxx, Inc. and Dr. Kosonocky for supporting me financially through out my graduate study.

I also express my sincere thanks to Ken Fujiwara, Nobu Hiraguri, Dr. Yves Dzialowski, Dr. C.S. Wang and Epitaxx, Inc. management and staff who has provided me with an excellent environment and resources for the research work. I would especially like to acknowledge the help provided by my colleagues Suzanne McCoy for epitaxial layer growth using Hydride Vapor Phase Epitaxy reactor, Hisao Nagata and Krys Slomkowski for detector fabrication and Mark Lourie, Wei Xu and Doug Nelson for focal plane array testing development and data collection. I would also like to acknowledge the help provided by Dr. Walter Kosonocky and W. Kleinhans of Valley Oak Semiconductors for the design and layout and Honeywell Semiconductors for the fabrication of the multiplexers. I am very thankful to Dr. Mike Scott of Epitaxial Products International and Dr. Y. Miura of Sumitomo Electric Industries for valuable discussions on the Organo Metallic and Chloride Vapor Phase Epitaxial growth of InAsP layers on InP substrate. I gratefully acknowledge the encouragement and support of Dr. W. Fricke

and D. Schink of Dornier GmbH, Dr. R. Hoogeveen, Dr. J. de Vries and T. Kamperman of Space Research Organization of Netherlands(SRON), R. Van Aalst of Fokker Space & Systems, Dr. B. Burmester of Ball Aerospace, Dr. J. Geary of Smithsonian and Dr. J. Burrows of University of Bremen. This work was supported by Dornier GmbH, Germany under the contract "Channel 8 InGaAs Detector Array Sliver Breadboard Phase" and Fokker Space & Systems, Netherlands under the contract "Focal Plane Arrays for NIR channels of SCIAMACHY".

Finally, I thank my wife Sujaya and my brother Rao N. Linga for their support and understanding through out my graduate study.

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CHAPTER 1

INTRODUCTION

Indium gallium arsenide is finding an important role in the 1-2.6 μm spectrum because of its unsurpassed performance and high reliability. Environmental remote sensing missions such as SCIAMACHY designed to measure the atmospheric trace gas abundance's on a global scale in the stratosphere as well as in the troposphere will require a high signal to noise ratio in the near infra-red channel focal plane arrays because of very low photon signal (< $2.2X10^{10}$ Photons/(cm^2-nm-s)$^{1/2}$. In InGaAs detectors, the major noise contribution is from the shot noise due to leakage current. Therefore, especially low leakage current InGaAs photodiodes is highly desirable in order to detect the atmospheric constituents in the 1-2.6 μm spectral region. To realize such challenging technological applications, a detector array of several thousand pixels having an average leakage currents as low as 10 fA is required for the spectral region 2.265 - 2.385 μm.

This research investigates the possibility of achieving leakage currents of less than 50 fA using InGaAs/InP technology by designing a novel and unique InGaAs/InAsP/InP p-i-n detector structure, growth of uniform InGaAs/InAsP layers with abrupt interfaces using Hydride Vapor Phase Epitaxy (HVPE), Chloride Vapor Phase Epitaxy (CVPE) and Metal Organic Chemical Vapor Deposition (MOCVD) techniques. To achieve these objectives, comparison and analysis of the detector results from the three wafer growth methods mentioned above will be presented. Also described are the post wafer growth fabrication techniques to reduce number of defects, design and fabrication of 1024 element detector arrays and design and development of a capacitive transimpedance

amplifier (CTIA) multiplexer for the readout of InGaAs detector arrays to operate at near zero-bias voltage. Testing, measurement and analysis of the 1024 element focal plane array results will be described in detail.

Chapter 2 describes the previous research work done on the development of InGaAs/InP detectors and detector arrays in the 1 to 2.6 μm wavelength region, the research objectives of this thesis describing the major problems that had to be addressed in order to achieve leakage currents of < 50 fA for the InGaAs/InP p-i-n detectors and detector arrays in the wavelength spectrum of 1 to 2.6 μm. Also described in this chapter are the general requirements or specifications of InGaAs/InP focal plane arrays for environmental sensing applications.

Chapter 3 describes the technology overview used to fabricate InP, InGaAs and InAsP materials for the wavelength of operation, device design and architecture of p-i-n detector using InP/InGaAs/InAsP material system and the growth of InAsP/InGaAs/InAsP/InP layers using the three most advanced material growth techniques, the Hydride Vapor Phase Epitaxy (HVPE), Chloride Vapor Phase Epitaxy (CVPE) and Metal Organic Chemical Vapor Deposition (MOCVD). The device fabrication and device electro-optical results are described. Also described in this chapter are the radiation hardness testing and results of proton, gamma and electron radiation on InGaAs detectors.

Dark current which is the important parameter in the operation of a Focal Plane Array for high signal to noise requirements or to integrate low optical signals is analyzed in Chapter 4. The mechanisms and origin of dark current in InGaAs/InP p-i-n

photodetectors is explained in this chapter. The dark current model used to simulate the dark current behavior was developed and described in this chapter. The measured device dark current results are compared with the the simulated values.

Chapter 5 describes the 1024 element InGaAs Focal Plane Array architecture using the Si read out multiplexer and InP/InGaAs detector arrays. This chapter also describes the pixel layout and hybridization of detector arrays and Si readout multiplexer using wire bonding and advanced mounting techniques that were used. Testing and test setup development for the electro-optical characterization of Si read-out multiplexer and InGaAs Focal Plane Arrays are also described in this chapter.

Chapter 6 describes the readout electronics developed for the read-out of InGaAs detector arrays. The design of read-out electronics consists of 512 element Capacitive Transimpedance Amplifier (CTIA) multiplexer for the readout of 1024 element InGaAs detector arrays. The fabrication method and testing results of the multiplexer are also described in this chapter.

Chapter 7 describes the 1024 element InP/InGaAs/InAsP Focal Plane Array test results and analysis of the test results. This chapter includes the detailed analysis of the electro-optical test results of InP/InGaAs/InAsP Focal Plane Arrays with cut-off wavelengths of 1.7, 1.9, 2.2 and 2.6 μm. Noise and quantum efficiency, the two important parameters for the signal to noise ratio requirements are analyzed, simulated and compared the simulated and measured results with great detail in this chapter. The radiation hardness testing and test results of gamma radiation on InGaAs Focal Plane Arrays with a cut-off wavelength of 2.6 μm is described in this chapter.

Chapter 8 describes the conclusions of this research thesis and future directions for the InGaAs Focal Plane Arrays development. Major conclusions achieved in this thesis are the long wavelength Focal Plane Arrays with a detector noise < 400 rms e^- can be achieved with InGaAs/InP technology. Also described in this chapter are the proposed ideas to further overcome the difficulties of dark current generation in the lattice mis-matched devices.

In Appendix A, theoretical equation was derived for the dislocation density using two dimensional Poisson's equation based on the diffusion approximation. This equation was used to estimate the defect density in the 1.7, 2.2 and 2.6 μm cut-off InGaAs photodetectors.

The research reported in this thesis was done as part of a joint research of the New Jersey Institute of Technology and Epitaxx, Inc., in support of a contract from Dornier, GmbH and Fokker Space & Systems, Holland. All of the wafers, devices, fabrication and the experimental facilities for this work were provided by Epitaxx, Inc., West Trenton, NJ.

CHAPTER 2

BACKGROUND

Optical communication is expected to play an important role in the upcoming information technology. The requirement for infrared detectors for low-loss, low dispersion silica fibers in the 1.0 - 1.6 μm wavelength range has been readily satisfied by the PIN photo diodes fabricated from $Ga_{0.47}In_{0.53}As$, which can be grown lattice matched to InP substrates. For future communication systems based on novel fluoride fibers, for which losses of <= 0.01 dB/km have been predicted[1], detectors operating at longer wavelengths will be required.

Indium gallium arsenide is finding an important role in the 1-2.6 μm spectrum because of its unsurpassed performance and high reliability[2]. Environmental remote sensing missions such as SCIAMACHY designed to measure the atmospheric trace gas abundance's on a global scale in the stratosphere as well as in the troposphere[3] requires challenging task of high signal to noise ratio in the near infra-red channel focal plane arrays[4]. In InGaAs detectors, the major noise contribution is from the shot noise due to leakage current. Therefore, reduction of leakage current in InGaAs photodiodes is an important task in order to detect the atmospheric constituents in the 1-2.6 μm spectral region. Leakage currents as low as 7 fA is required for the spectral region 2.265 - 2.385 μm detector array[5].

In order to satisfy the high signal to noise ratio, it is necessary to use low noise, near zero-bias multiplexers[6] and to cool the detector array to lower temperatures. Since a major portion of an instrument's mass and power is consumed by the focal plane cooler,

detector technologies that require only modest cooling can contribute significantly to the realization of a miniature infrared instrument[7]. The scientific space programs are in continuing trend towards smaller and more affordable missions. The advantage of an infrared detector that operates at lower temperatures (150 K - 200 K) will reduce the cooling requirement which is a key ingredient in the design and construction of scientific instruments such as SCIAMACHY. The 1024 element focal plane array consists of an InGaAs detector array connected to a CMOS multiplexer using wire bonding.

Potential applications of such a device include NIR spectroscopy, fluorescence, remote sensing, environmental sensing, space and astronomical applications. The InGaAs detector arrays are especially appropriate device since sensitive absorption, luminescence, emission and Raman spectroscopies require focal plane arrays with high quantum efficiency, low dark current and low noise.

Lattice mismatched $In_xGa_{1-x}As/InAs_yP_{1-y}$($x>0.53$, $y>0$) hetero-structures are suitable for the fabrication of photodiode arrays with spectral response up to 2.6 μm. Most applications require high uniformity of device performance as well as process reproducibility. However, InGaAs hetero-structures are extremely sensitive to defects and non-uniformity's existing in epitaxial growth of layers and those defects introduced in the processing. This thesis describes a novel and unique detector structure, growth of uniform InGaAs/InAsP layers with abrupt interfaces using Hydride Vapor Phase Epitaxy (HVPE), Chloride Vapor Phase Epitaxy (CVPE) and Metal Organic Chemical Vapor Deposition (MOCVD) techniques, post wafer growth fabrication techniques to reduce number of defects, design and development of a capacitive transimpedance amplifier

(CTIA) multiplexer for the readout of InGaAs detector arrays to operate at near zero-bias voltage, measurement and analysis of the focal plane array results.

2.1 Research Objective

Several authors have proposed different growth techniques, different detector structures and different fabrication methods aimed at developing the long wavelength indium gallium arsenide photodetectors [8]-[20]. Past work was aimed at achieving the InGaAs detector arrays with cut-off wavelengths of 1.7 μm with 256 eleement pixels. The aim of this thesis is to explore the technological limitations of long wavelength (> 1.7 μm) InGaAs photodetectors and photodetector arrays and to design, fabricate, test and analyze the results of a proposed novel detector structure aimed at minimizing the dark current due to excessive defect densities because of the lattice mismatch between the epitaxial layers and the substrate. To achieve the objective of low dark current novel material processing techniques are implemented. The results of the proposed device structures demonstrates that InGaAs/InP technology is suitable for the fabrication of 1024 element linear arrays with long cut-off wavelengths.

One of the main draw back of any near-infrared focal plane arrays is the read-out circuit. The read-out circuit has to be designed and developed depending on the requirements to limit the noise contribution and also depends on the signal requirements. To achieve the objective of low noise (400 rms e^-), it is necessary to design and develop a novel and unique 512 element Si read-out multiplexer for the read out of 1024 element InGaAs detector arrays. This include the design, development, fabrication, testing and

analysis of the results of Capacitive Transimpedance Amplifier (CTIA) multiplexer for the readout of 1024 element linear InGaAs detector arrays to operate at near zero bias.

2.2 Main Problems

2.2.1 Material and Detector Design Problems

Figure 2.1 shows the bandgap energy, cutoff wavelength and lattice constant (atomic spacing) of different semiconductor elements, compounds and alloys[21]. The dots represent the binary materials (e.g. InP), the lines that connect two dots are ternary materials (e.g. InGaAs) and in between the lines are the quaternary material (e.g. InGaAsP). The binary alloys have fixed lattice parameters and bandgaps, ternary alloys have one degree of freedom and quaternary alloys have two degrees of freedom since a range of lattice parameters is available for each bandgap. Figure 2.1 aids in the selection of detector materials.

As seen from Figure 2.1, the composition of InGaAsP "quaternary" alloys can be adjusted so that their atom spacing is "lattice matched" to that of InP substrates. This enables low stress transitions from the substrate material to the active layers. $In_{0.53}Ga_{0.47}As$ is the quaternary alloy (albeit without phosphorous) with the smallest bandgap that can still achieve lattice matching with indium phosphide.

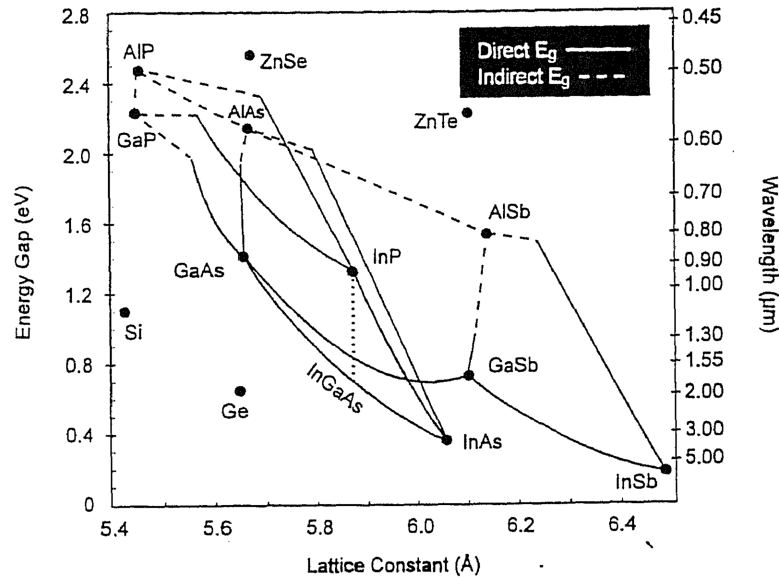

Figure 2.1 Energy bandgap, cut-off wavelength and lattice constant for a variety of semiconductor materials.

As shown in Figure 2.1, the cut-off wavelength of InGaAs material can be extended beyond 1.7 μm by increasing the composition of InAs content. The $In_xGa_{1-x}As$ layers with x>0.53, lattice mismatched to InP makes it possible to extend the absorption edge or cut-off to longer wavelengths. This necessitates the use of higher Indium content alloys which are mismatched with respect to the InP substrate with the problems of dislocation induced, junction leakage and low quantum efficiency[13]. By increasing the Indium content of the alloy, the band gap decrease and thus extends the spectral response, since

$$\lambda_c = 1.24 / E_g$$

where, λ_c = cut off wavelength in μm

E_g = bandgap energy in eV.

An $In_{0.82}Ga_{0.18}As$ alloy thus extends the spectral response to 2.6 μm since it has a band gap of 0.48 eV at room temperature[22]. Since $In_xGa_{1-x}As$ with $x > 0.53$ is not lattice matched to the InP substrate, the graded layer technique is used to accommodate the large mismatch between the InP substrate and the $In_xGa_{1-x}As$ absorption layer. There exists a critical thickness below which a lattice mismatched layer is elastically deformed and thus biaxially strained[23]. In this case the layer has the same lattice constant as the substrate in the plane parallel to the substrate-layer interface and there are no dislocations. When the layer thickness is above the critical thickness, the (biaxial) strain becomes too high and the layer will relax. The layer will take his own lattice constant which is different from that of the substrate. In a relaxed lattice mismatched layer, many dislocations are introduced and the layer will exhibit poor electrical and optical performances. The critical thickness as a function of strain was reported in [24][25]. Because of the lattice mismatch between the layers, the misfit dislocations are generated[26[[27]. These misfit dislocations are electrically active as generation and recombination centers[15]. The main effects of misfit dislocations in photodiodes are to generate excess dark current and to reduce minority carrier life time[28].

This thesis describes the design and development of $In_{0.53}Ga_{0.47}As$, $In_{0.72}Ga_{0.28}As$ and $In_{0.82}Ga_{0.18}As$ detector arrays using the ternary compound material grown by Hydride Vapor Phase Epitaxy (HVPE), Chloride Vapor Phase Epitaxy(CVPE) and Metal Organic Chemical Vapor Deposition (MOCVD) methods. Methods of reducing the dislocation density during the epitaxial layer growth and during the fabrication of photodetectors and

detector arrays are introduced. Comparison of the results of the three growth methods and performance of the long wavelength detectors and detector arrays are presented. In addition, a new detector design with improved performance of low dark current is presented. Detailed analysis of the dark current, origin of the dark current and the methods of reducing the dark current are also presented.

2.2.2 Read-out Electronics

In InGaAs detector arrays, the main source of the noise is from the shot noise due to the dark current. In order to improve the signal to noise ratio, the dark current should be improved. At low bias voltages (< 100 mV) the dark current is approximately proportional to the detector reverse bias voltage. To reduce the dark current and hence the noise from the focal plane array, the detector must be operated either at zero bias voltage (photo-voltaic) or at near zero bias voltage. To operate the detector array at near zero-bias voltage, a Si read-out circuit (multiplexer) has been designed and fabricated using a Capacitive Transimpedance Amplifier (CTIA), Correlated Double Sampling (CDS) at each pixel. The multiplexer fabrication and the test results will be described and analyzed. The focal plane architecture for 1024 element linear InGaAs arrays with cut-off wavelengths of 1.7 μm, 2.2 μm and 2.6 μm will be presented.

2.3 Performance Requirements

The Focal Plane Array consisting of InGaAs detector array and Si readout multiplexer was designed and developed to meet the following requirements.

Number of pixels	:	1024
cut-off wavelength	:	1.7 μm
		2.2 μm
		2.6 μm
Operating temperature	:	200 K for 1.7 μm cut-off FPA
		150 K for 2.2 & 2.6 μm cut-off FPA
Pixel size	:	500 x 13 μm^2
Detector pitch	:	25 μm
Internal quantum efficiency	:	> 55 %
Max. signal level	:	> 1E7 e^-
Integration time	:	> 1 ms (up to several minutes)
Dark current	:	< 4 fA for 1.7 μm cut-off detector
		< 2 fA for 2.2 μm cut-off detector
		< 7 fA for 2.6 μm cut-off detector
Noise	:	< 800 rms. e^-
Pixel-to pixel signal variation	:	< 5 % rms.

CHAPTER 3

OVERVIEW OF TECHNOLOGY

In an epitaxial heterostructure, if the lattice constants (spacing between the two neighboring atoms) of the substrate and the epitaxial layer parallel to the interface are not equal, a certain misfit is present. When an epitaxial layer of lattice constant other than that of its substrate is grown, it produces strain ($\Delta a/a$) in the grown layer. It requires less energy for a thin epitaxial layer to strain elastically and adopt the substrate spacing rather than form dislocation[24]. However, this energy increases with thickness and eventually a "critical thickness" is reached where it is energetically more favorable to form a dislocation, rather than remain totally strained. The critical thickness (t_c) is inversely proportional to the lattice mismatch between the two adjoining epitaxial layers[29].

$$t_c = (\Delta a/a)^{-1}$$

On exceeding the critical thickness, the strain in the mismatched epitaxial layer releases through the formation of misfit dislocations[24][30][31][32]. Usually, the critical thickness is of the order of few nanometers for structures up to 4% mismatch and is mostly exceeded in the hydride vapor phase epitaxy (HVPE), which is characterized by fast epitaxial crystal growth (0.5 to 1 um/min). Thus, the InGaAs/InAsP detector structures grown for this research work exceeded their critical thickness values, thereby generating misfit dislocations.

The mismatch (or misfit) dislocations have detrimental effect on the electrical and optical characteristics of many devices like lasers, photodetectors and transmission photo cathodes[33]. The reduction of dislocation density is a key to improve the device

performance. G.H. Olsen et. al [30] and J. W. Matthews et. al [16][34] has studied the lattice mismatched layers extensively and grown heteroepitaxial lattice mismatched semiconductors with dislocation densities as low as $10^5/cm^2$. They concluded that an abrupt interface between the mismatched layers bends most of the dislocations into the plane of the growth and prevents them from propagating into the active layer. Therefore, for the reduction of dark current in the lattice mismatched InGaAs detectors, growth of epitaxial layers with compositionally sharp and abrupt interfaces is very important.

The dislocation density in a lattice mismatched crystal is dependent on the lattice mismatch between the two adjoining epitaxial layers. In InAsP layers, the lattice mismatch between the two neighboring layers can be reduced by reducing and accurately controlling the arsenic concentration. During this research work, as many as 18 $InAs_yP_{1-y}$ buffer layers were grown on top of InP substrate to reduce the lattice mismatch between the two layers to < 0.1%.

3.1 Crystal Growth Techniques

An $In_{0.82}Ga_{0.18}As$ alloy has a band gap of 0.48 eV at 300K and thus extends the absorption of photons up to 2.6 um wavelength at room temperature. A graded layer technique is used to accommodate the large lattice mismatch between the InP substrate(a_o = 5.8694) and the $In_{0.82}Ga_{0.18}As$ absorption layer(a_o = 5.990) which is about 2%. To reduce the defect density, the mismatch is accommodated by growing several $InAs_yP_{1-y}$ layers, where the composition of As is increased from layer to layer. Step grading is very effective in decreasing dislocation density than continuous grading because most dislocations bend at

the step interface and do not propagate along the growth direction[34][35]. Misfit dislocations can be electrically active as generation-recombination centers, generate excess dark current and reduce minority carrier life time. InAsP was chosen over InGaAs as the material to grade because in the hydride VPE process it is easier to adjust AsH_3/PH_3 ratios than InCl/GaCl ratios. $InAs_yP_{1-y}$ was also used as the "cap" layer to terminate the p-n junction because of it's high band gap which helps in reducing the dark current. About 15 layers of $InAs_yP_{1-y}$ with y increasing from 0.0 to 0.68, each layer about 0.8 um are grown on InP substrate. This results in lattice constant change from 5.8694 to 5.9926 A° and the band gap energy change from 1.35 to 0.65 eV. The final graded layer of $InAs_{0.68}P_{0.32}$ was about 1.0 um thickness to provide a good quality sub-layer for the growth of the absorption layer. The cap or window layer is $InAs_{0.68}P_{0.32}$ and is about 1.5 um. The p-n junction is formed by zinc diffusion through the window layer. The 3.7 um thick absorption layer assures strong absorption of the transmitted radiation with energy slightly greater than the bandgap energy of the absorption layer.

3.1.1 Hydride Vapor Phase Epitaxy (HVPE)

The group V element is introduced as a hydride (e.g. PH_3) and HCl is passed over the group III metal to form the group III chloride[36]. The group III and group V composition can be accurately controlled[37][38]. The As and P controllability is much simpler in hydride VPE than that in other growth methods, such as MOVPE and MBE[12]. Therefore, hydride VPE is an effective method by which accurate control of the $InAs_yP_{1-y}$ graded buffer layer is possible[39]. By controlling the AsH_3 with a faster

response time and smaller flow range controller helps to obtain abrupt interfaces between the graded layers. A drawback of HVPE is the need for hydrides, which are extremely toxic.

3.1.2 Chloride Vapor Phase Epitaxy (CVPE)

Chloride Vapor Phase Epitaxy is one of the earliest vapor growth techniques. The group V chloride (e.g. $AsCl_3$) passes over the group III metal, which is heated in the hottest zone of the reactor, to form a group III chlorides (e.g. GaCl). This group III chloride diffuses to a cold zone, which contains the substrate and react with a group V species to form a III-V compound. Multilayer structures are achieved by shuttling back and forth between the chambers. The disadvantage of this growth technique is that the group V chlorides are introduced by heating a liquid which means that the concentration varies exponentially with temperature and is thus difficult to control.

3.1.3 Metal Organic Vapor Phase Epitaxy (MOVPE)

Metal-Organic Vapor Phase Epitaxy uses a group V hydrides and group III metalorganics (e.g. TriMethylIndium or TMI or $(CH_3)_3In$) which are introduced in the reactor by means of a carrier gas. The source metalorganics are kept in temperature controlled bubblers in order to stabilize the vapor pressure. Carrier gas flows through the bubbler and is saturated by the vapor pressure in the bubbler. The reactants are cracked above the hot wafer surface and combine on the wafer. MOVPE growth can be performed at atmospheric pressure but also at reduced pressures (20 - 200 mbar), enabling more abrupt

interfaces. MOVPE was the first technique that was able to grow high purity layers with monolayer abruptness. The past 10 years the reactor designs have much improved resulting in uniform growth over large areas. Because of this flexibility and rather simple reactor, MOVPE is at this moment the moist widely used growth technique for basic research as wells as for large scale production. The main disadvantage of MOVPE is the high consumption of expensive and hazardous sources, which requires high investments for source materials and safety equipment. However, the past ten years a strong effort has been put in the development of alternative and less hazardous source materials.

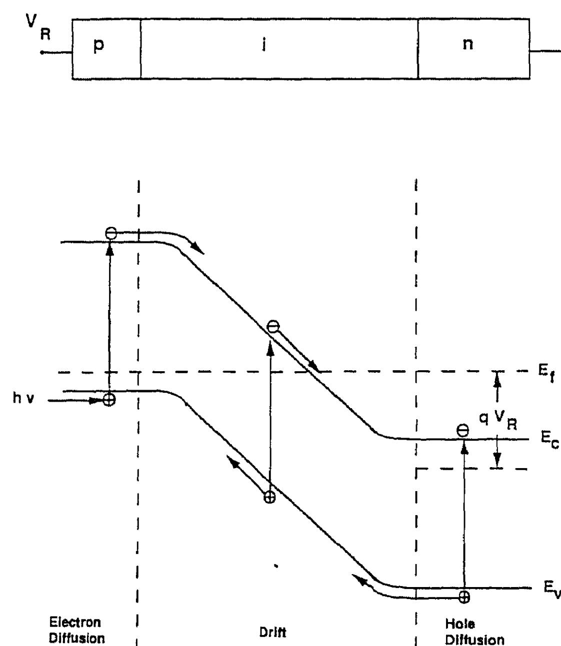

Figure 3.1 Cross-section and energy band diagram of a p-i-n diode.

3.2 Device Design and Cross-section

The p-i-n photodiode is one of the most common photodetectors and is usually reverse biased, since light absorbs in the intrinsic layer, the intrinsic layer can be adjusted to optimize the quantum efficiency and frequency response. The basic schematic representation of a p-i-n diode and an energy band diagram is shown in Fig. 3.1. Light absorption in the semiconductor produces electron-hole pairs. Electron-hole pairs produced in the depletion region or within a diffusion length will eventually be separated by the electric field and hence the carriers drift across the depletion layer. The material requirement for p-i-n photodiodes with good device performance are lattice matched, dislocation free epitaxial layers with controlled doping and thickness.

3.2.1 Lattice Matched $In_{0.53}Ga_{0.47}As$/InP Device Structure and Fabrication

Figure 3.2 is a schematic cross section of standard planar $In_{0.53}Ga_{0.47}As$ p-i-n photodiode which is lattice-matched to InP substrate[40][41]. Figure 3.3 shows it's band diagram. This device operates in the wavelength region 0.8 - 1.7 μm. As shown in figure 3.2, the device consists of several epitaxial layers on InP substrate. The substrate is sulfur (n+) doped InP. The first layer on top of the InP substrate is about 1 μm thick InP buffer layer. This layer reduces the defect migration from the InP substrate to the $In_{0.53}Ga_{0.47}As$ absorption layer, which is the second layer. The $In_{0.53}Ga_{0.47}As$ absorption layer is about 3.5 um thick and assures complete absorption of the incoming photons. The third layer is a 1 um thick InP cap layer. Although $In_{0.53}Ga_{0.47}As$ has high internal absorption for photons, photo generated electrons and holes can often recombine at the top surface

thereby reducing over all quantum efficiency. Deposition of the high bandgap InP on this surface eliminates the dangling bonds at this free surface, allows free transmission of light and tends to repel carriers from the interface so they don't recombine. This large bandgap(1.34 eV) layer also acts as a cap region to passivate the small band gap(0.75 eV) InGaAs, avoiding surface leakage current of the diode. Therefore, the top cap layer reduces the surface leakage currents, and the surface recombination of photo generated carriers. This enhances the noise performance also. The doping of the three layers were optimized to reduce the dark current. The very top layer is a plasma deposited Si_3N_4 dielectric coating, which provides passivation and assures the reliability of the device. This Si_3N_4 also serves as an antireflection coating to enhance the responsivity of the detector. The p-n junction was formed by Zn diffusion through the opening in the Si_3N_4 passivation layer. Each detector element consists of 13 um X 500 um^2 Zn diffusion area with a pitch of 25 um between the neighboring two pixels. The 'p' contact was made using alloyed AuZn contact. The contact was extended using the electron-beam deposited TiPtAu to reduce the diffusion area and effective dark current. The final step is the thermally evaporated AuSn 'n' contact to provide low resistance ohmic contacts. The planar structure shown in Fig. 3.2 is expected to show advantages in durability and reliability[40]41] [42].

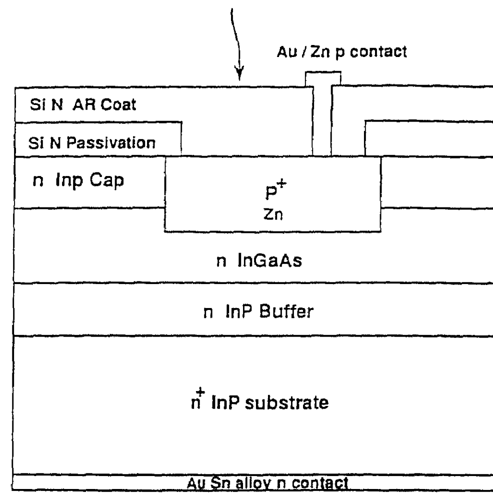

Figure 3.2 Schematic cross-section of 1.7 um cut-off InGaAs detector.

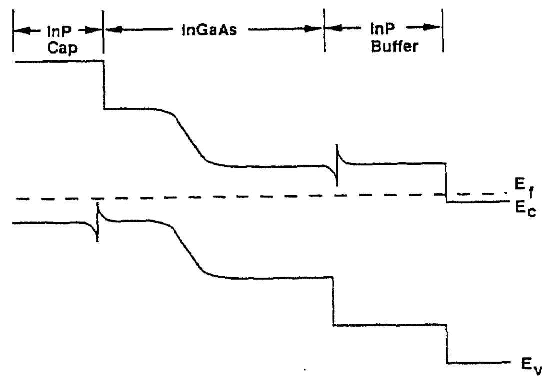

Figure 3.3 Band diagram of the planar lattice matched $In_{0.53}Ga_{0.47}As$ photodiode.

3.2.2 Lattice mis-matched $In_xGa_{1-x}As/InP$ Device Structure and Fabrication

The detector cross-section for the wavelength range 1000 - 2200 nm and 1000 - 2600 nm is shown in Figure 3.4[43]. The detector structure consists of InP substrate and $InAs_yP_{1-y}$ graded buffer layers, $In_xGa_{1-x}As$ absorption layer and $InAs_yP_{1-y}$ cap layer. The composition of In (x) and the composition of As (y) is varied to get the required cut-off wavelength of 2.2 um and 2.6 um and to achieve the perfect lattice match between $In_xGa_{1-x}As$ and $InAs_yP_{1-y}$ layers.

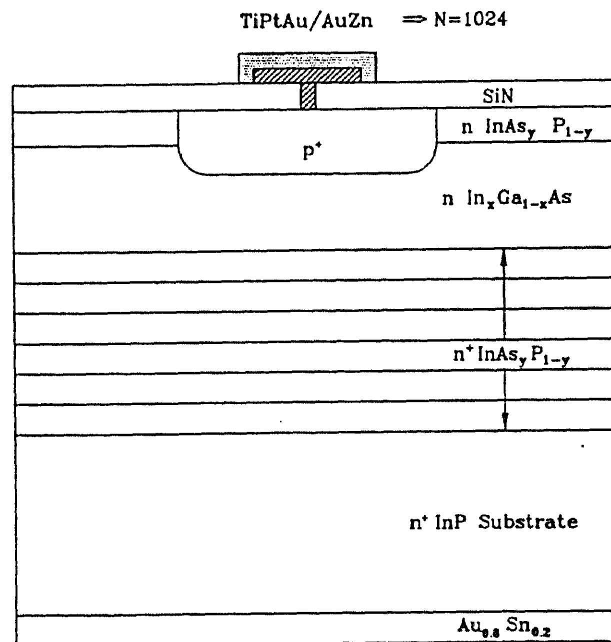

Figure 3.4 Schematic cross-section of 2.2 um and 2.6 um cut-off wavelength InGaAs detector.

	Layer	Doping type	Concentration
	$InAs_{0.6}P_{0.4}$	p^+	n $1\text{-}3X10^{16}$
	$In_{0.82}Ga_{0.18}As$	n	$1X10^{17}$
y = 0.60	$InAs_{0.6}P_{0.4}$	n^+	$1\text{-}2X10^{18}$
	InAsP	n^+	$1\text{-}2X10^{18}$
	InAsP	n^+	$1\text{-}2X10^{18}$
	InAsP	n^+	$1\text{-}2X10^{18}$
	InAsP	n^+	$1\text{-}2X10^{18}$
	InAsP	n^+	$1\text{-}2X10^{18}$
$InAs_yP_{1-y}$	InAsP	n^+	$1\text{-}2X10^{18}$
	InAsP	n^+	$1\text{-}2X10^{18}$
	InAsP	n^+	$1\text{-}2X10^{18}$
	InAsP	n^+	$1\text{-}2X10^{18}$
	InAsP	n^+	$1\text{-}2X10^{18}$
	InAsP	n^+	$1\text{-}2X10^{18}$
	InAsP	n^+	$1\text{-}2X10^{18}$
	InAsP	n^+	$1\text{-}2X10^{18}$
y = 0.015	InAsP	n^+	$1\text{-}2X10^{18}$
	InP	n^+	$1\text{-}3X10^{18}$

Figure 3.5 Schematic cross-section of the 2.6 um photodiode.

Figure 3.5 shows the schematic cross-section of the lattice mismatched $In_{0.82}Ga_{0.18}As$ p-i-n photodiode. A graded layer technique was used to accommodate the large lattice mismatch between the InP substrate(a_o=5.86944) and the $In_{0.82}Ga_{0.18}As$ absorption layer(a_o=5.990). This lattice mismatch between the neighboring layers introduces the misfit dislocations. Misfit dislocations can be electrically active as generation-recombination centers, generate excess dark current and reduce minority carrier life time. The graded layer technique was used to bend the threading dislocations and reduce the dislocation density. Fifteen layers of graded InAsP layers were grown on

the InP substrate keeping the lattice mismatch between the neighboring layers to as low as 0.13%[44]. Making the lattice mismatch smaller between the neighboring layers reduces the number of misfit dislocations[45]. In addition, the surface morphology of the wafers grown with higher (0.33%) lattice mismatch between the consecutive mismatched layers was very often rough with no distinct cross hatch pattern. This rough surface reduces the number of consecutive good pixels in a long photodetector arrays in addition to increasing the dark current. The surface morphology of wafer grown with a lattice mismatch of 0.33% between the neighboring two InAsP graded layers was shown in Figure 3.6. As seen from Figure 3.6, the surface morphology was rough with no clear pattern. By reducing the flow range of AsH_3 mass flow controller with a faster response time allowed us to grow smaller lattice mismatched InAsP layers with a better accuracy of controlling the mismatch. Additionally, the faster response time helped to obtain the abrupt interfaces between the graded layers. Abrupt interfaces bend dislocations into the plane of growth and thus prevent their propagation into the InGaAs absorption layer[34][46]. Figure 3.7 shows the surface morphology of a wafer grown using small mismatch (<0.13%) between the neighboring InAsP graded layers. As seen from Fig. 3.7, the surface morphology was smooth with clear and distinct cross hatch pattern. The smooth surface also helps in the fabrication of photodetectors during the photo-lithography and alignment of 'p' metal contact.

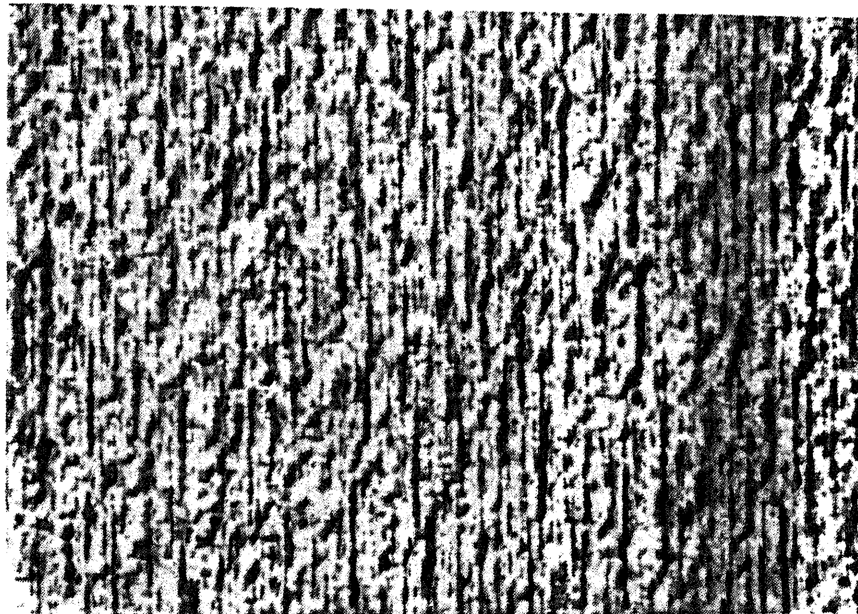

Figure 3.6 Optical micrograph showing surface morphology of an $In_xGa_{1-x}As/InAs_yP_{1-y}$ 2.6 um photodetector structure on a (100)-2° InP substrate with a lattice mismatch of 0.33% between consecutive mismatched InAsP graded layers (100X magnification). The short axis of the photograph is 1.4 mm.

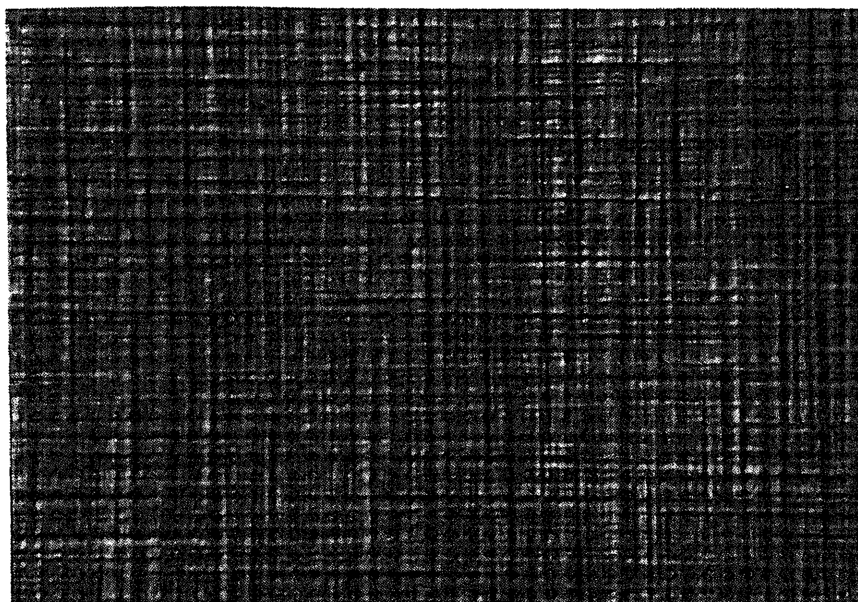

Figure 3.7 Optical micrograph showing surface morphology of an $In_xGa_{1-x}As/InAs_yP_{1-y}$ 2.6 um photodetector structure on a (100)-2° InP substrate with a lattice mismatch of 0.13% between consecutive mismatched InAsP graded layers (100X magnification). The short axis of the photograph is 1.4 mm.

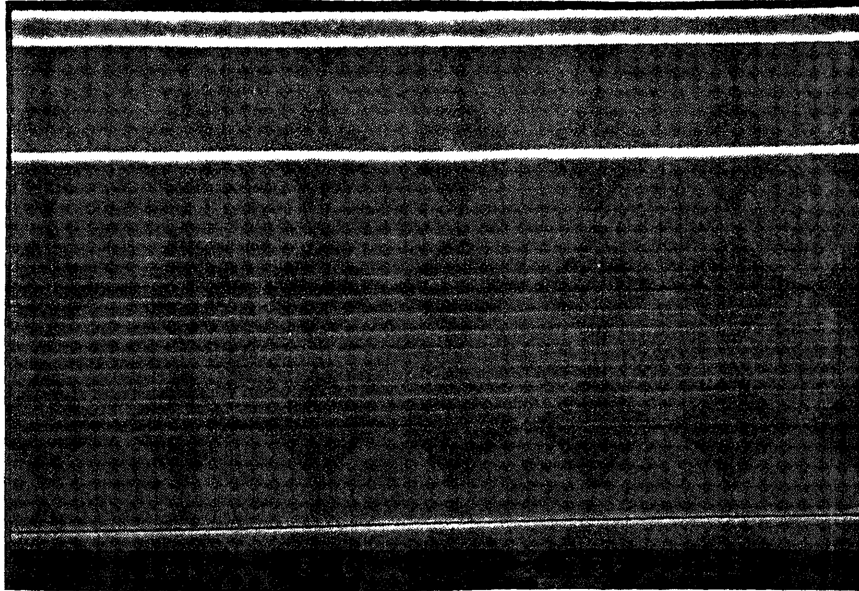

Figure 3.8 SEM cross-section of an $In_xGa_{1-x}As/InAs_yP_{1-y}$ 2.6 um photodiode structure on a (100)-2° InP substrate.

Figure 3.8 shows the SEM photomicrograph of the grown structure which shows the sharp and abrupt interfaces between the graded layers. An abrupt interface bends the dislocations into the plane of growth and prevents propagating them into the absorption layer. The InAsP graded layers were doped with sulfur and the doping concentration is in the range of 1-5 X 10^{18} cm^{-3}. The high doping of InAsP graded layers may pin down the dislocations and prevent the propagation into the InGaAs layer. The $In_{0.82}Ga_{0.18}As$ absorption layer was grown on the final $InAs_{0.6}P_{0.4}$ sub-absorption layer and is doped with sulfur to a concentration of 0.8-1 X $10^{17}cm^{-3}$. The doping of the absorption layer reduces the depletion width at low bias voltages. Before the p-n junction depletes completely, the dark current at low temperatures is dominated by generation-recombination current[22].

By reducing the depletion width, the generation recombination current can be reduced and hence the total dark current decreases. The very final layer is a 1 um thick $InAs_{0.6}P_{0.4}$ cap layer and is doped with sulfur to a concentration of 1-5 X 10^{16} cm^{-3}. The cap doping helps to reduce the surface depletion width and therefore the surface generation current can be reduced. Surface generation plays an important role at low temperatures, where the bulk leakage is comparable with the surface leakage.

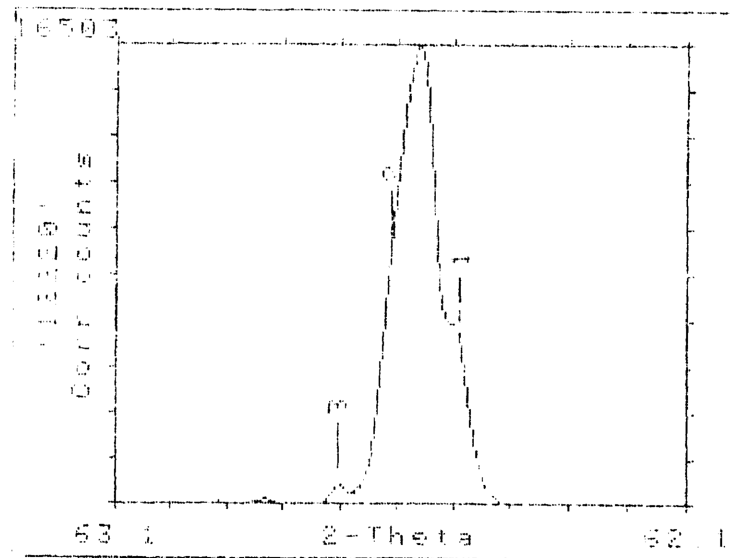

Figure 3.9 X-ray diffraction spectra of an $In_{0.82}Ga_{0.18}As$ photodiode structure.

Figure 3.9 shows the single crystal x-ray diffraction measurement of the grown $InAs_{0.6}P_{0.4}/In_{0.82}Ga_{0.18}As/InAs_{0.6}P_{0.4}/InP$ device structure. The first peek in the x-ray diffraction measurement was that of InGaAs and the second peek was that of InAsP cap layer. In Fig. 3.9 there is only one peak indicating that the mismatch between the cap layer and the absorption layer was ~ 0% and the lattice constant of both layers are same.

The measured results of the x-ray diffraction measurement across the wafer shows the uniformity of the lattice mismatch ~ 0.1%.

Defects such as dislocations and interfaces play a crucial role in the performance of hetero-structure devices. Several methods have been employed to reduce the dislocation density in lattice mismatched epi-layers, including the rapid thermal annealing[47], introduction of strained layer superlattices in the epi-layer[24][30] and using the substrates having varying degrees of mismatch or different crystal symmetry[48][49]. High temperature thermal annealing was performed on the grown wafer. Annealing techniques have been very effective in eliminating some of the defects like stacking faults and twin boundaries[50][51]. At annealing temperatures, the mobility of dislocations can lead to the reorganization and annihilation of dislocations. To prevent excessive dissociation of the wafer surface, the wafers were coated with a silicon nitride protective coating. The wafer was annealed from 400°C to 650°C temperatures for about 5 cycles by keeping approximately 1 minute at each temperature. Figure 3.10 shows the TEM micro graph of the $In_{0.82}Ga_{0.18}As$ non annealed wafer. Figure 3.11 shows the TEM micro graph of the same wafer after the thermal annealing. From both figures 3.10 and 3.11, it is clearly seen that the thermal annealing reduces the number of dislocations. Table 3.1 shows the measured dark current values of the detectors fabricated using the same wafer with and with out thermal annealing.

Table 3.1 Effect of RTA on dark current

Wafer	RTA	I_d @ 10 mV, 300 K
wafer #1	No	200 nA
wafer #2	Yes	50 nA

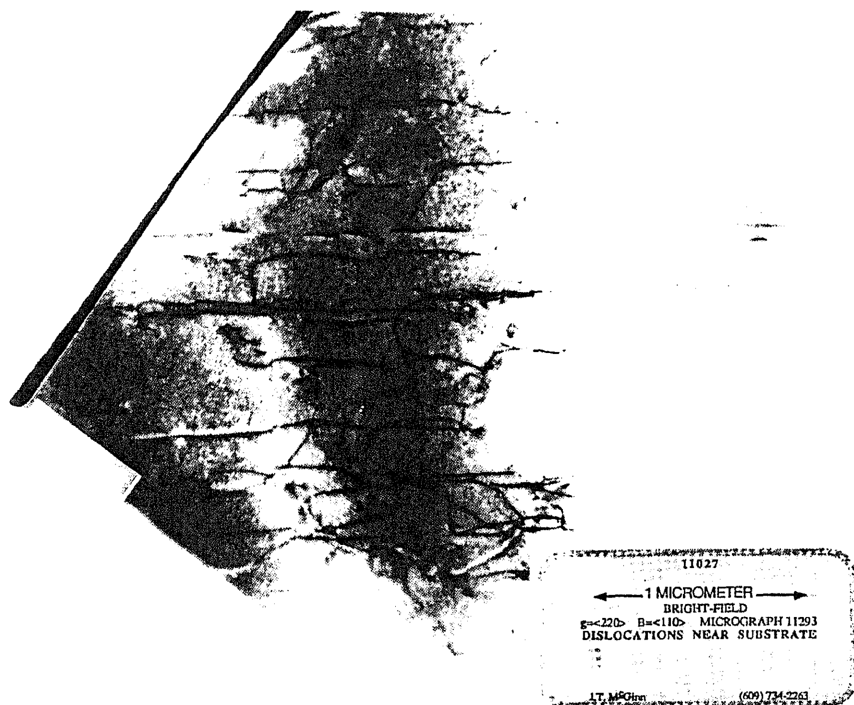

Figure 3.10 TEM micro graph showing the cross section of an $In_{0.82}Ga_{0.18}As$ photodiode structure before thermal annealing.

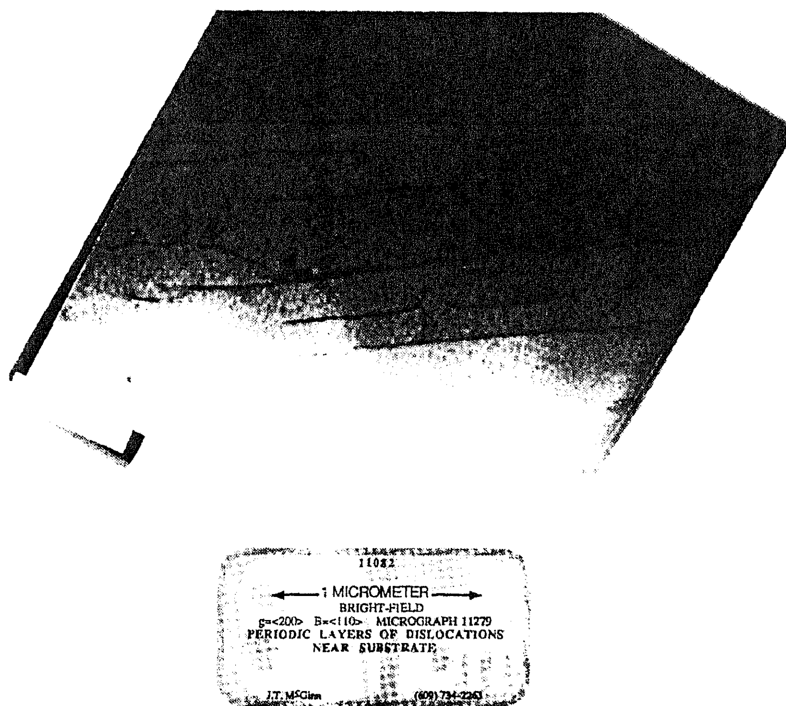

Figure 3.11 TEM micro graph showing the cross section of an $In_{0.82}Ga_{0.18}As$ photodiode structure after thermal annealing.

3.3 Device Fabrication

After the thermal annealing of the grown wafer, the silicon nitride protective coating was wet etched and redeposit a new layer of silicon nitride passivation layer using Plasma Enhanced Chemical Vapor Deposition (PECVD) method. A diffusion window was opened in the silicon nitride for a 'p^+' diffusion. The p-n junction was formed using zinc diffusion through the InAsP cap layer at 500°C for 37 minutes in a closed ampule boat method of diffusion. The depth of the zinc diffusion is important as it may influence the quantum efficiency, leakage current and speed of the detector. Zinc diffusion was optimized to form the p-n junction below InAsP/InGaAs interface. From the experiments, it was found that the zinc diffusion rate is faster in InAsP than InP. Figure 3.12 shows the Secondary Ion Mass Spectroscopy (SIMS) profile of the $In_{0.82}Ga_{0.18}As$ photodetector structure. As seen from Figure 3.12, the InAsP cap is about 1.5 μm thick and the diffusion is about 0.5 μm deep in to the 4 μm thick InGaAs absorption layer. A deep diffusion may deplete more misfit dislocations and generate excess leakage current[52].

After the zinc diffusion, silicon nitride anti-reflection coating was deposited using the PECVD deposition method. The thickness and refractive index of silicon nitride was optimized for the quarter-wave thickness of operating wavelength. The refractive index of Si_3N_4 was measured as 2.0. The required thickness of anti-reflection coating was calculated using the equation[53]

$$\frac{\lambda}{4} = n \cdot t_{ar}$$

where, λ = Operating wavelength in nm

n = refractive index of the coating material

t_{ar} = thickness of the coating in nm

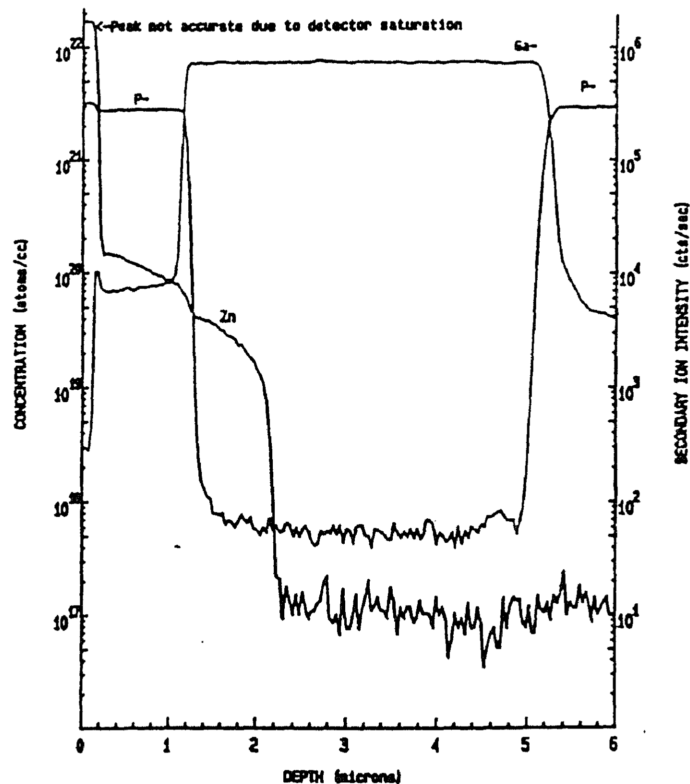

Figure 3.12 SIMS profile of an $In_{0.82}Ga_{0.18}As$ photodetector structure.

For $In_xGa_{1-x}As/InAs_yP_{1-y}/InP$ detector arrays with a cut-off wavelength of 1.7 um, 2.2 um and 2.6 um, the thickness of anti-reflection coating was optimized for 1.3 um, 2.0 and 2.38 um wavelength.

After the anti-reflection coating deposition, the ‘p’ contact window was opened using the wet chemical etching. The first level ‘p’ contact was formed with Au-Zn-Au using the thermal evaporation technique. After the Au-Zn-Au evaporation, the contact was alloyed for forming ohmic-contact with lower contact resistance. The second level

'p' contact was formed using Ti-Pt-Au deposition using electron beam evaporation method. The second metal makes contact to the Au-Zn-Au alloyed contact and the contact area was 30 um X 100 um extending on to the silicon nitride passivation layer. Since the second level 'p' metal extends onto the silicon nitride passivation layer, it reduces the active (diffused) p-n junction area required for making the 30 um X 100 um contact which is required for wire bonding (integration) the detector array to the Si multiplexer. The reduction of total diffused area reduces the amount of dark current.

Figure 3.13 shows the cross-section of the $In_xGa_{1-x}As/InAs_yP_{1-y}$ photodetector array after the fabrication. As seen from Fig. 3.13, each pixel is isolated by 12 um from the neighboring pixel and the two level 'p' metal contact is shown on top of the Au-Zn-Au ohmic contact.

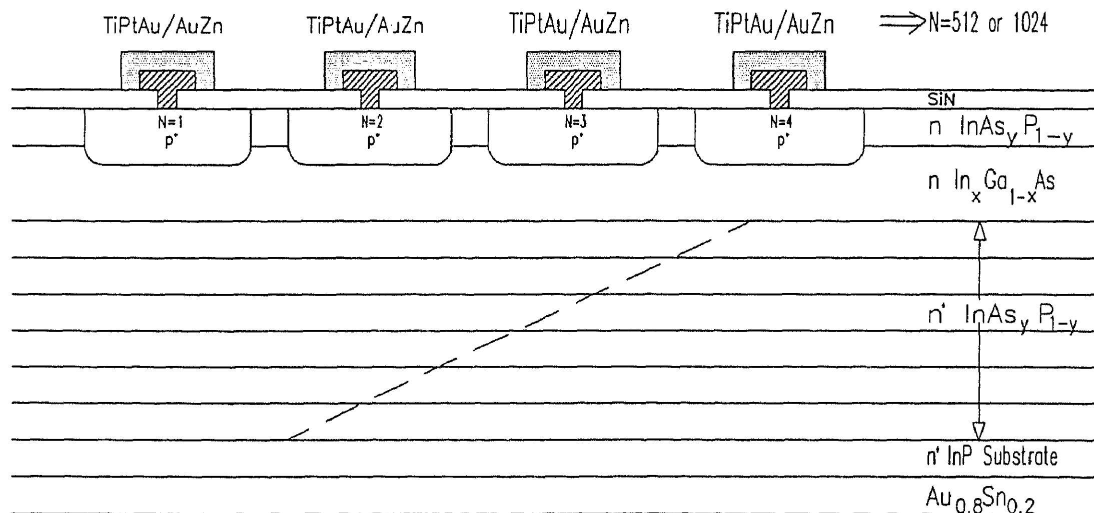

Figure 3.13 Cross-section of 1024 element $In_xGa_{1-x}As/InAs_yP_{1-y}$ photodetector array.

After the Ti-Pt-Au second metal deposition, about 1 um thick Au was plated using electrochemical process[54] with electrolytes (electrolysis). This thick metal assures the mechanical integrity and improve the adhesion of Au wire bond to the contact.

The wafer was back lapped and polished using a chemo-mechanical lapping and polishing method. The wafer was polished as mirror-like surface. The 'n' contact was formed with Au-Sn using the thermal evaporation deposition method. The wafer was then probed for the leakage current and scribed into slivers.

The $In_{0.82}Ga_{0.18}As$ detector array sliver was processed with stripping and non stripping of the silicon nitride after the thermal annealing of the wafer. The wafer was split into two parts and processed identically to investigate the improvement of leakage current due to the stripping and non stripping of silicon nitride. Rapid thermal annealing was performed on both parts of the wafer at 650°C for 1 minute and repeated for 5 cycles. There was no significant damage to the surface of the wafer after the thermal annealing of both parts of the wafer except for a few spots of nitride peeling. Figure 3.14 shows the surface of the wafer after annealing and Figure 3.15 shows the surface before annealing. As shown in Figure 3.14 there are nitride peeling spots on the surface after the thermal annealing. The spots vary from 1 um to 100 um in diameter and there are about 15-20 spots on a 2" wafer. Nitride peeling may create excessive lateral diffusion of zinc and electrically short the neighboring pixels. Therefore, stripping and re-deposition of silicon nitride is important in fabricating the array slivers with few dropouts(bad pixels).

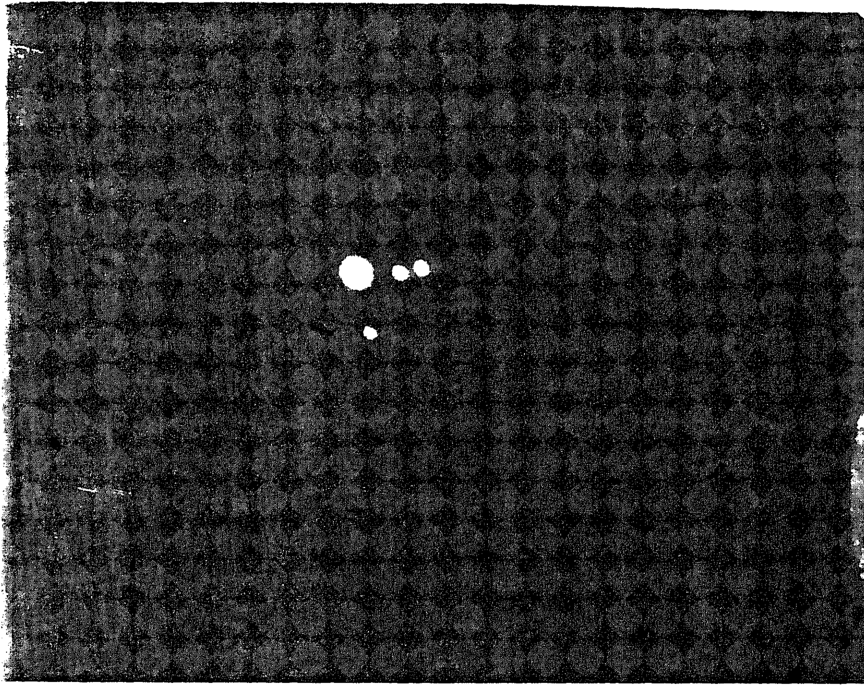

Figure 3.14 Wafer Surface(coated with silicon nitride) after annealing.

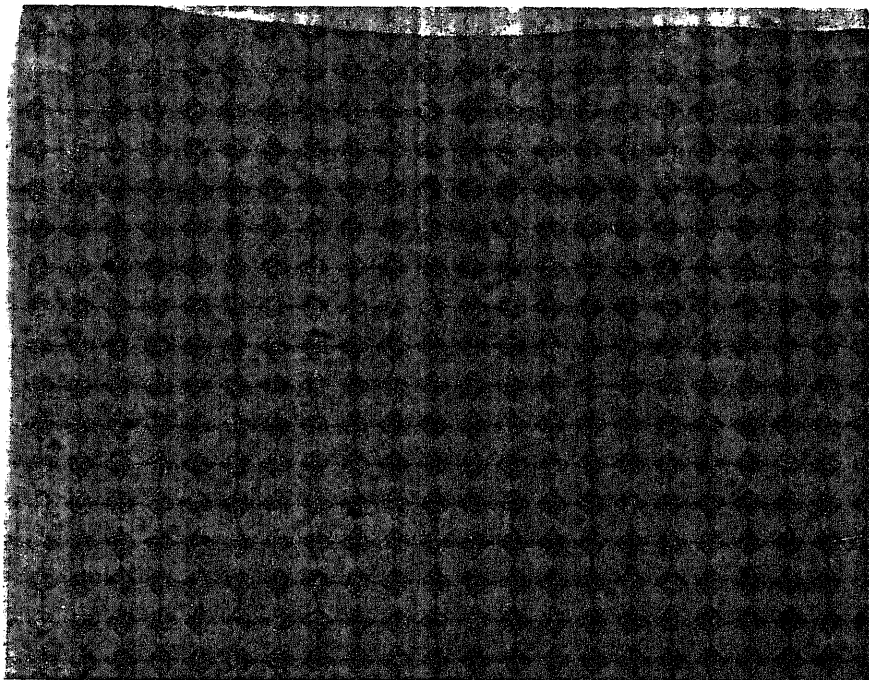

Figure 3.15 Wafer surface(coated with silicon nitride) before annealing.

The leakage current was measured on(the processed detector array sliver) both parts of the wafer at room temperature, 200K and 150K. There is no significant difference in leakage current from stripping and non stripping of silicon nitride at the operating temperature of 150K and 10 mV bias. The measured dark current results of 1024 element InGaAs Focal Plane Arrays with cut-off wavelengths of 1.7, 2.2 and 2.6 μm are discussed in Chapter 7. The measured dark current of 2.6 μm detector array sliver is about 50 fA at 10 mV and 150K. As discussed in Chapter 7, the measured dark current is not uniform enough to meet the required uniformity specification(<10%) on a 1024 element array sliver.

To improve the uniformity of dark current from pixel to pixel in a 1024 element linear InGaAs detector array, further investigation of the silicon nitride stripping to reduce the surface traps and improved crystal growth to reduce the dislocation density is required. Silicon nitride stripping and re deposition may destroy the shallower traps and may introduce the deep traps in the lower half of the bandgap, close to the middle of the bandgap that is normally occupied by the electrons as they are located below the fermi level. Both the traps may be associated with some complex defects such as sulfur impurity and created during the annealing procedure. The behavior of deep traps in the annealed InGaAs photo diodes requires further investigation concerning the capture mechanism and its temperature dependence. Deep traps, which influence the temperature behavior of the leakage current, may be introduced due to the nitride stripping and also due to the bulk defects. The dislocations formed because of the lattice mismatch between

the adjacent epitaxial layers are usually electrically active as generation recombination centers. Therefore, the misfit dislocations generate excess dark current and also reduce the minority carrier life time. Because of the reduction of minority carrier life time, the recombination of photo generated carriers is fast and hence the responsivity is lower.

3.4 Device Results

3.4.1 $In_{0.53}Ga_{0.47}As$ Detector Results

Each detector element has a measured dark current value of < 1 pA at room temperature and 10 mV reverse bias voltage. Figure 3.16 shows the typical dark current-voltage characteristics for a 13 um X 500 um detector at room temperature and at 235 K. At 235 K, the measured dark current was < 1 fA at 10 mV reverse bias voltage. Table 3.2 shows the measured results of dark current as a function of InGaAs absorption layer and InP cap layer doping. As seen from Table 3.2, a factor of 5 improvement in the dark current was achieved by intentionally doping the absorption layer. As explained in Chapter 4, this improvement was attributed to the decrease of generation-recombination current in the bulk depletion region. Increasing the doping in the InP cap layer further reduced the dark current at room temperature and at 235 K. This decrease in dark current was attributed to the decrease in the surface depletion width and hence the contribution of surface traps to the total dark current will be lower. The measured capacitance of each detector element was 12 pF at 10 mV reverse bias voltage. The measured responsivity of the detector as a function of wavelength and temperature is shown in Figure 3.17. As seen in Fig. 3.17, each detector element has a quantum efficiency greater than 80%.

Table 3.2 Dark current as a function of InGaAs and InP layer doping

Wafer No.	InP Cap doping cm^{-3}	InGaAs doping cm^{-3}	InP Buffer doping cm^{-3}	Id @ 300 K 10 mV pA	Id @ 235 K 10 mV fA
0468A	1×10^{16}	$< 1 \times 10^{15}$	3×10^{17}	15-20	5-8
0510A	1×10^{16}	2.2×10^{17}	3×10^{17}	3	2-5
0511A	1×10^{17}	2.5×10^{17}	3×10^{17}	1	< 1

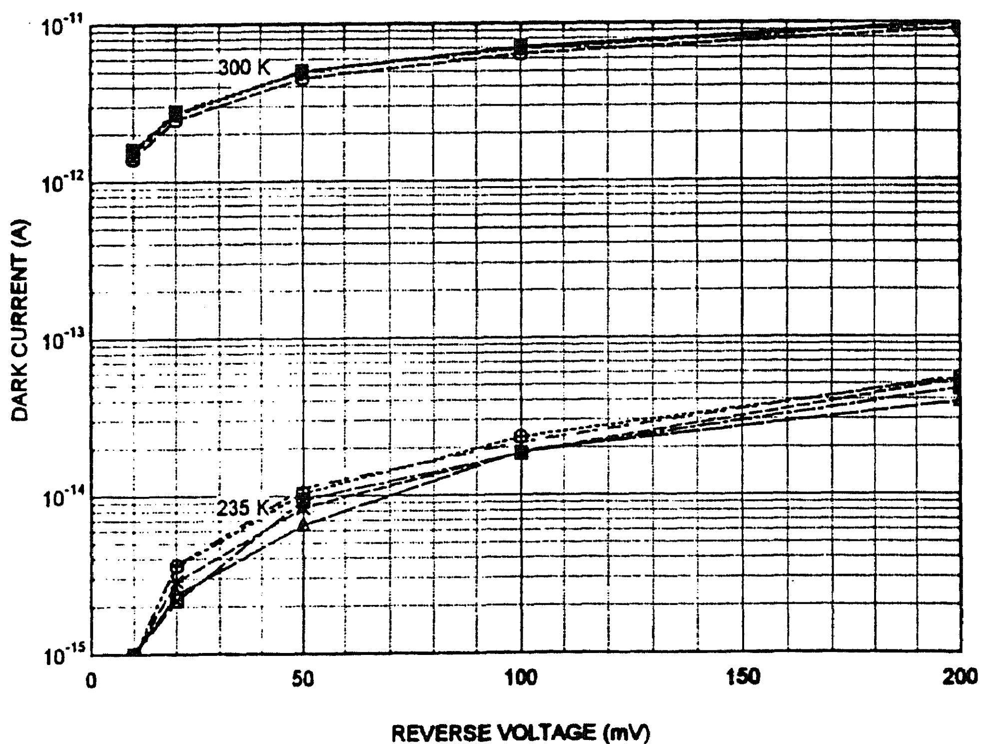

Figure 3.16 Dark current-voltage characteristics of 1.7 um cut-off InGaAs detector.

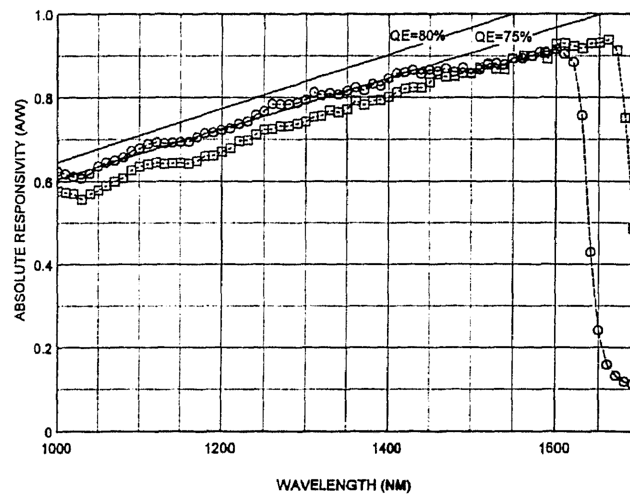

Figure 3.17 Spectral response of 1.7 um cut-off InGaAs detector.

3.4.2 $In_{0.72}Ga_{0.28}As$ Detector Results

The detector element of the 2.2 um cut-off wavelength array has a measured dark current of 2 nA at 10 mV reverse bias voltage and at room temperature. At 150 K, the measured dark current was < 25 fA at 10 mV reverse bias voltage. Figure 3.18 shows the dark current current-voltage characteristics of the detector element at 300 K and at 150 K. Each detector element has a measured capacitance value of about 15 pF at 10 mV reverse bias voltage. The measured responsivity of the detector element as a function of wavelength and temperature is shown in Figure 3.19. The quantum efficiency of each element is greater than 70% at peak wavelength. As seen from Fig. 3.19, the internal quantum efficiency is lower than the lattice matched detector quantum efficiency shown

in Fig. 3.17. The decrease of quantum efficiency is due to the decrease in the minority carrier life time. The minority carrier life time decreases with the increase of misfit dislocations[55]. The cut-off wavelength decreases 1 nm per °C lower in temperature from the room-temperature. This change in cut-off wavelength was due to the increase in band-gap while lowering the temperature.

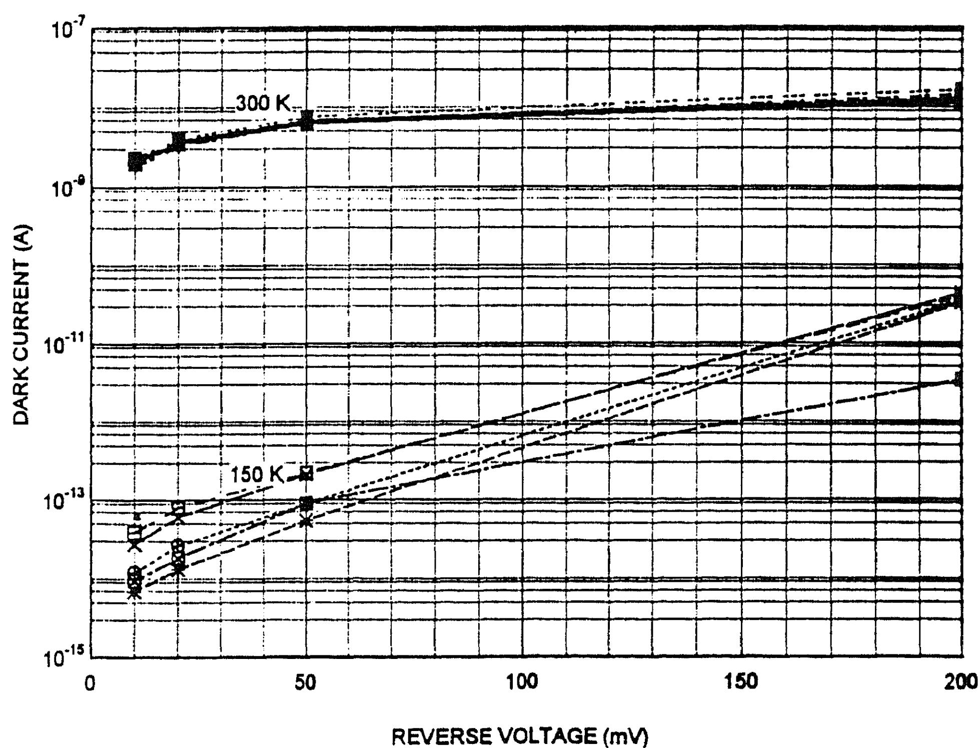

Figure 3.18 Dark current-voltage characteristics of 2.2 um cut-off InGaAs detector.

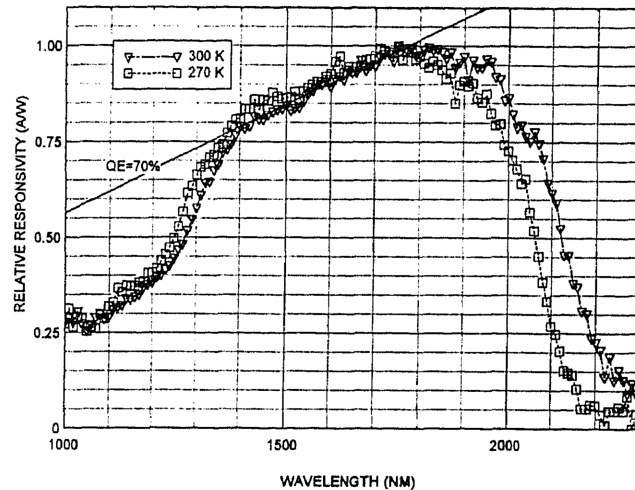

Figure 3.19 Spectral response of 2.2 um cut-off InGaAs detector.

3.4.3 $In_{0.82}Ga_{0.18}As$ Detector Results

The detector element of the 2.6 um cut-off wavelength array has a measured dark current of 40 nA at 10 mV reverse bias voltage and at room temperature. At 150 K, the measured dark current was < 100 fA at 10 mV reverse bias voltage. Figure 3.20 shows the dark current-voltage characteristics of the detector element at 300 K and at 150 K. Each detector element has a measured capacitance value of about 15 pF at 10 mV reverse bias voltage. The measured responsivity of the detector element as a function of wavelength and temperature is shown in Figure 3.21. The quantum efficiency of each element is greater than 55%. The lower quantum efficiency is due to the shorter carrier life time[56][57].

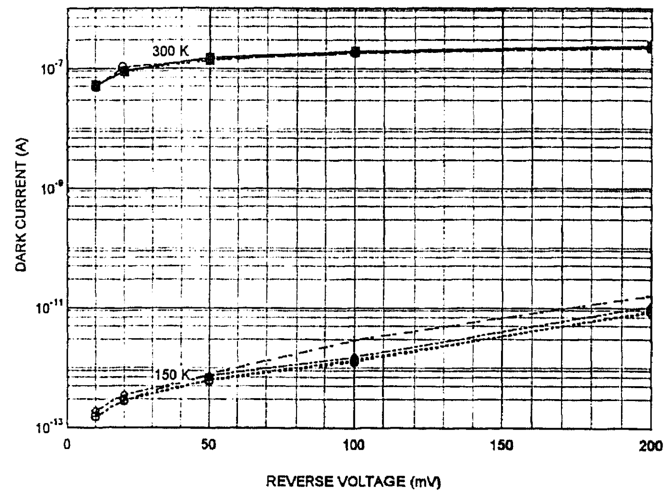

Figure 3.20 Dark current-voltage characteristics of 2.6 um cut-off InGaAs detector.

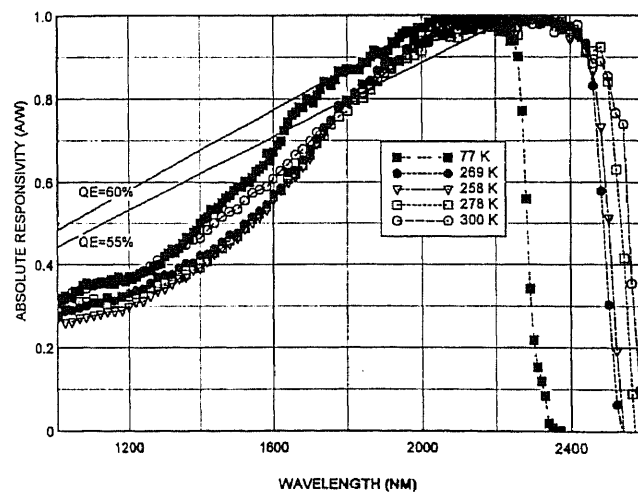

Figure 3.21 Spectral response of 2.6 um cut-off InGaAs detector.

As a result of the high shunt resistance, low dark current, these detectors contributes minimum noise to the FPA. The high capacitance of the detector element is not a concern, since each pixel cell of the multiplexer was designed with a differential Capacitive Transimpedance Amplifier (CTIA) and Correlated Double Sampling (CDS) circuit to compensate the noise due to the detector capacitance.

3.4.4 Radiation Hardness Testing Results of InGaAs Detectors

The effects of space radiation on InGaAs detectors with a cut-off wavelength of 2.6 um was measured using proton, gamma and electron radiation sources. The 2.6 um cut-off wavelength InGaAs detectors were chosen for this testing because of its lower band-gap compared with 1.7 and 2.2 um cut-off wavelength detectors. The detectors were exposed to radiation of continuous electron and gamma beams at the Lehigh University Van de Graaff Radiation facility and proton beams at the Brookhaven National Laboratory's Tandem facility. The 3 Mev High voltage Van de Graaff provided beams of electrons which could be used directly or gamma rays from the electron beam brehmstrahlung[58]. The dark current of each detector was measured before and after the radiation exposure. The radiation dose used was 5, 10, 15 and 20 Krads with a dose rate of 200 rad/min for electron rays, 100 rad/min. for gamma rays. The dose rate for gamma rays was measured with a Geiger counter.

The measured dark current results does not show any change in dark current up to 20 Krad of electron, gamma and proton radiation. Further increasing the dose to 2 Mrad

of proton radiation, the dark current increased significantly. This increase in dark current was attributed to the introduction of a defect level located in the band gap which acts as a generation center[58][59].

CHAPTER 4

DARK CURRENT ANALYSIS

4.1 Theoretical Analysis of Dark Current

The dark current in *pn* or *pin* junction diode under reverse bias condition consists of bulk and surface components. The major bulk components are diffusion current (J_{dif}), generation-recombination current ($J_{g\text{-}r}$), and tunneling current (J_{tun}). The surface components consist of the surface generation-recombination current (J_{sg}) and the ohmic conduction current (J_{ohm}). The latter is the dark current via shunt path formed at the semiconductor-dielectric interface. Generally, the diffusion current is dominant at high temperature or low reverse voltage. The total dark current (density) of diode is expressed as the sum of them

$$J = J_{dif} + J_{g-r} + J_{tun} + J_{ohm} + J_{sg} \tag{4.1}$$

Since every component has different temperature and voltage dependence, measurements of dark current at various temperatures and voltage help to determine the contribution of each component to the total dark current. In the case of InP/InGaAs hetero-structure diode, additional current related to the hetero-interface may be one of the component of the dark current.

Diffusion current

The diffusion current is due to minority carriers diffusing away from or towards the junction in the diode neutral regions. For large p^+-n diodes, namely when the diode size is much longer than the diffusion length of minority hole in the n region, with n region

thickness larger than the minority hole diffusion length, the diffusion current density is expressed as[21]

$$J_{\text{dif}} = J_{\text{s}}\left[\exp(qV / kT) - 1\right] \tag{4.2}$$

where q is the elementary charge of electron, V is the applied voltage that is negative, k is Boltzmann constant and T is the junction temperature. The saturation current density J_{S} is given by

$$J_{\text{s}} = q n_{\text{i}}^2 D_{\text{p}} / n L_{\text{p}} \tag{4.3}$$

where D_{p} and L_{p} represent the hole diffusivity and the hole diffusion length in the n region, respectively. n is the equilibrium carrier density in the n region. The intrinsic carrier density n_{i} is

$$n_{\text{i}} = 2\left(4\pi^2 m_{\text{e}} m_{\text{h}} k^2 / h^4\right)^{3/4} T^{3/2} \exp\left(- E_{\text{g}} / 2kT\right) \tag{4.4}$$

In Eq. (4.4), m_{e} and m_{h} are the effective masses of electron and hole, respectively. h is Plank constant and E_{g} is the band gap energy.

Generation-recombination current

The bulk generation-recombination current is due to generation and recombination of electron-hole pairs in the diode depletion region. The generation-recombination current density is approximately given by[60]

$$J_{\text{g-r}} = \left(q n_{\text{i}} W / \tau_{\text{eff}}\right)\left[\exp\left(qV / 2kT\right) - 1\right] \tag{4.5}$$

where τ_{eff} is the effective carrier lifetime. The generation-recombination current is proportional to the depletion width W that for an abrupt p^+-n junction is given by

$$W = \left[-2\varepsilon(V - V_{bi})/qn\right]^{1/2} \tag{4.6}$$

and for graded junction

$$W = \left[-12\varepsilon(V - V_{bi})/qa\right]^{1/3} \tag{4.7}$$

where ε is the semiconductor dielectric constant, V_{bi} is the built-in potential and a is the impurity gradient. In this calculation the junction is considered as an abrupt junction. The built-in potential is

$$V_{bi} \approx \frac{kT}{q}\ln\left(\frac{N_A N_D}{n_i^2}\right) \tag{4.8}$$

Tunneling current

For band-to-band tunneling in a direct band-gap semiconductor, the tunneling current density is given by[61]

$$J_{tun} = \frac{(2m_e^*)^{1/2} q^3 F_m V}{h^2 E_g^{1/2}} \exp\left(-\frac{2\pi\beta m_e^{*1/2} E_g^{3/2}}{qhF_m}\right) \tag{4.9}$$

where F_m is the maximum electric field which for an abrupt p^+-n junction is given by

$$F_m = \left[-2qn(V - V_{bi})/\varepsilon\right]^{1/2} \tag{4.10}$$

The parameter β depends on the detailed shape of the tunneling barrier and $\sqrt{2}/3$ for parabolic barrier and is $\pi / 2\sqrt{2}$ for triangular barrier.

Ohmic conduction current

When the diffusion and generation-recombination current are low, usually at low temperature, the ohmic conduction current is observed. The ohmic conduction current is given by

$$J_{\mathrm{ohm}} = V/ R_{\mathrm{eff}} \tag{4.11}$$

where R_{eff} is the effective resistance and

$$R_{\mathrm{eff}} = R_{\infty} \exp\left(E_{\mathrm{a}} / kT\right) \tag{4.12}$$

where E_a is the thermal activation energy and R_{∞} is the constant.

Surface generation-recombination current

The dark current due to the surface generation-recombination current is expressed as

$$J_{\mathrm{sg}} \propto \sqrt{V_{\mathrm{bi}} - V} \exp(- E_{\mathrm{g}} / 2kT) \tag{4.13}$$

The surface generation-recombination current is the function of the surface recombination velocity, which depends on the surface or interface condition, pinning of surface Fermi-level, etc. The surface recombination rate corresponds to W/τ_{eff} in the expression of the bulk generation-recombination current density.

4.2 Interpolation of Parameters from Lattice Matched ($In_{0.53}Ga_{0.47}As$) Photodetector

The unknown parameters, which correspond to fitting parameters, are D_p/L_p for the diffusion current, τ_{eff} for the generation-recombination current, β for the tunneling current, and R_{∞} and E_a for ohmic conduction current. The proportional constant of the surface generation-recombination current is also unknown. Since the temperature and applied voltage dependencies of the surface generation-recombination current is almost same as the bulk generation-recombination current, the surface generation-recombination current can be included to the bulk generation-recombination current.

To obtain the unknown parameters, the dark current of a lattice matched (1.7 um cut-off wavelength) InP/InGaAs/InP photodetector with 100 μm diameter (0551-149) on a thermoelectric cooler was measured at various temperatures. The photodetector with extremely low dark current was selected. The InGaAs active layer is assumed to be perfectly lattice matched to the InP substrate (x = 0.468) and has a band gap energy of 0.75 eV. The temperature dependence of the InGaAs band-gap energy is approximately

$$E_g(T) = E_g(300\text{K}) + 3.266 \times 10^{-4} (T - 300) \tag{4.14}$$

The effective mass of electron and hole, and dielectric constant of the lattice matched InGaAs were interpolated using the values of GaAs and InAs. The values are $m_e = 0.0436\ m_0$, $m_h = 0.437\ m_0$, $\varepsilon = 13.9\ \varepsilon_0$. The carrier concentration in the InGaAs layer is 1.8×10^{20} m^{-3}. The donor concentration of Zn diffused area was assumed as $N_D = 2.0 \times 10^{25}$ m^{-3}. The dark current density obtained from the above expressions was converted to the dark current using the junction area of 1.0×10^{-8} m^2.

As a result of the fitting to the experimental results, the parameters listed below were determined.

$D_p/L_p = 5.8$ m^2 s^{-1}
$\tau_{eff} = 9 \times 10^{-4}$ s
$\beta = 1.88$
$R_\infty = 8.0 \times 10^4\ \Omega$ m^{-2}
$E_a = 8.0109 \times 10^{-20}$ C (0.50 eV)

Figure: 4.1 shows the reverse voltage dependence of the dark current. The measured data and calculated values are indicated by markers and solid lines, respectively. The calculated values are well consistent with the measured dark current.

Each dark current component is also calculated separately and is shown in Fig. 4.2 (a). The dark current at 298.4 K temperature is dominated by the diffusion current at low reverse voltage region. The generation-recombination current, however, is dominant at 243.14 K as in Fig. 4.2 (b). Since temperature dependence of the diffusion current is much stronger than that of the generation-recombination currents, the generation-recombination current is dominant at lower temperature and the diffusion current is dominant at higher temperature region. Apparently the ohmic conduction current is small and negligible when the reverse bias voltage is less than several volts. Even when the parameter β depending on the tunneling barrier shape is 1.11 that corresponds to triangular tunneling barrier, the tunneling current is negligible as compared with the diffusion and generation-recombination current, because the carrier concentration of the InGaAs is low. This is also expected from the comparison between the breakdown voltage and the band gap energy. The breakdown voltage (the reverse voltage when the dark current is about - 5 μA) was about - 45 V at 298.4 K and - 49 V at 243.14 K. For the junction with the breakdown voltage V_b in excess $6E_g/q$, the breakdown is caused by the avalanche multiplication mechanism. When the breakdown voltage is less than $4E_g/q$, *th*e breakdown can be considered due to the tunneling effect. In the case of measured diode the breakdown voltage is about 60 times as large as E_g/q. While parameters D_p/L_p and τ_{eff} have also relatively weak temperature dependencies precisely, they were neglected.

4.3 Simulation of Dark Current in 2.2 and 2.6 um Cut-off InGaAs Detectors

The estimation of the dark current of $In_{0.72}Ga_{0.28}As$ (2.2 μm) and $In_{0.82}Ga_{0.18}As$(2.6μm) photodetector was carried out using the fitting parameters mentioned above. To calculate the dark current, the band-gap energy and accompanied parameters such as the effective masses of carrier were changed but the parameters used in the calculation are listed in Table 4.1.

Table 4.1 Interpolated parameters of $In_xG_{1-x}As$ absorption layer

	$In_{0.53}Ga_{0.47}As$	$In_{0.72}Ga_{0.28}As$	$In_{0.82}Ga_{0.18}As$
λ_{cutoff} at 300 K (μm)	1.7	2.2	2.6
E_g at 300 K (eV)	0.75	0.579	0.487
x	0.53	0.71	0.82
m_e	0.0436 m_o	0.0358 m_o	0.0309 m_o
m_h	0.437 m_o	0.423 m_o	0.414 m_o
ε	13.9 ε_o	14.2 ε_o	14.3 ε_o

The temperature dependence of dark current was calculated for 2.2 and 2.6 um cut-off wavelength detectors as a function of carrier concentration of the *n* layer (InGaAs absorption layer). The calculation was carried out at -10 mV. The result shown in Fig. 4.3(a) for 2.2 um cut-off photodetector shows that the dark current do not follow exp(- E / kT) or exp(- E / $2kT$) when the carrier concentration of the absorption layer is higher than 1.5×10^{17} cm^{-3}. Because the tunneling current is dominant at lower temperature region where the diffusion and the generation-recombination current are relatively small, the dark current is saturated. This is caused by the relatively weak temperature dependence of the tunneling current compared with the other dark current components. In the case of channel 8 photodetector indicated in Fig. 4.3(b), this phenomenon is much

clear. The dark current at 235 K ($1000/T = 4.26$) is merely one order of magnitude smaller than that at 300 K ($1000/T = 3.33$). Although the detector with the lower carrier concentration in the absorption layer has higher dark current at 300 K, the dark current ratio between 300 K and 235 K is large. On the other hand, the detector with higher carrier concentration in the absorption layer shows very low dark current at 300 K, but the large reduction of the dark current by the decreasing temperature is not expected.

For 2.6 um cut-off photodetector with carrier concentration of InGaAs absorption layer as 1.0×10^{17} cm^{-3}, the temperature dependency of each dark current component is indicated in Fig. 4.4. At the temperature above 240 K the diffusion current is the dominant component in the total dark current and is proportional to $\exp(- E / 2kT)$. The tunneling current is principal at the temperature below 190 K. The dark current is almost constant at the temperature region, because the temperature dependence of the tunneling current is very weak.

The carrier concentration dependency of dark current at 300 K, 235 K and 150 K is shown for 2.2 um cut-off photodetector in Fig. 4.5 (a) and for 2.6 um cut-off photodetector in Fig. 4.5 (b). The dark current has a minimum that depends on the temperature. The dark current is the lowest as the carrier concentration in the absorption layer is about 1.5×10^{17} cm^{-3} for 2.2 um cut-off photodetector at 300 K. However the carrier concentration is too high to get the lowest dark current at 235 K or 150 K. It is apparent from Fig. 4.5 (a) that the carrier concentration of the absorption layer should be $0.8 - 1.0 \times 10^{17}$ cm^{-3} to obtain the lowest dark current at the operating temperature of 235 K.

The contribution of each component of dark current to the total dark current is considered. Fig. 4.6 shows the carrier concentration dependencies of the dark current components for 2.6 um cut-off photodetector. Fig. 4.6(a) corresponds to the temperature of 300 K and 4.6(b) for 150 K. As in the case of 1.7 um cut-off photodetector, the diffusion current is dominant at 300 K and the generation-recombination current is dominant at 150 K. When the carrier concentration is higher than about 1×10^{17} cm^{-3}, the tunneling current is the principal component at both temperatures.

The calculation under estimates the total dark current for both 2.2 um and 2.6 um cut-off photodetector at room temperature. One of the reason may be that the fitting parameters of lattice matched (1.7 um cut-off) photodetector (D_p/L_p and τ_{eff}) are different from the 2.2 um and 2.6 um cut-off photodetector. Another reason may be that the carrier concentration dependencies of D_p/L_p and τ_{eff} are neglected. High concentration of deep levels induced by defects in the absorption layer of 2.2 um and 2.6 um cut-off detectors should be considered in the calculations. The generation-recombination current is much higher than the calculated value because deep levels reduce the effective carrier lifetime.

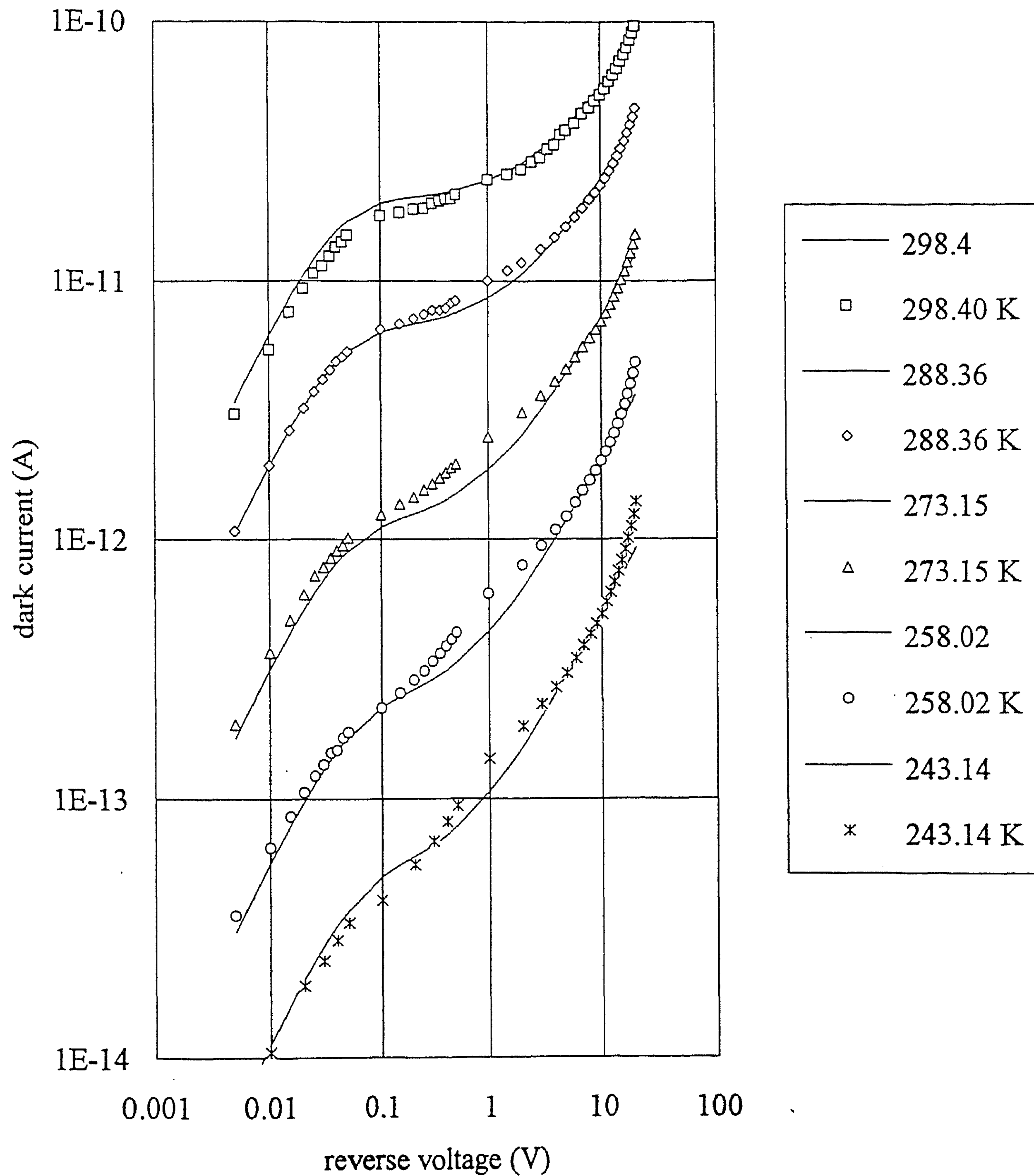

Figure 4.1 Measured and simulated results of dark current as a function of reverse voltage.

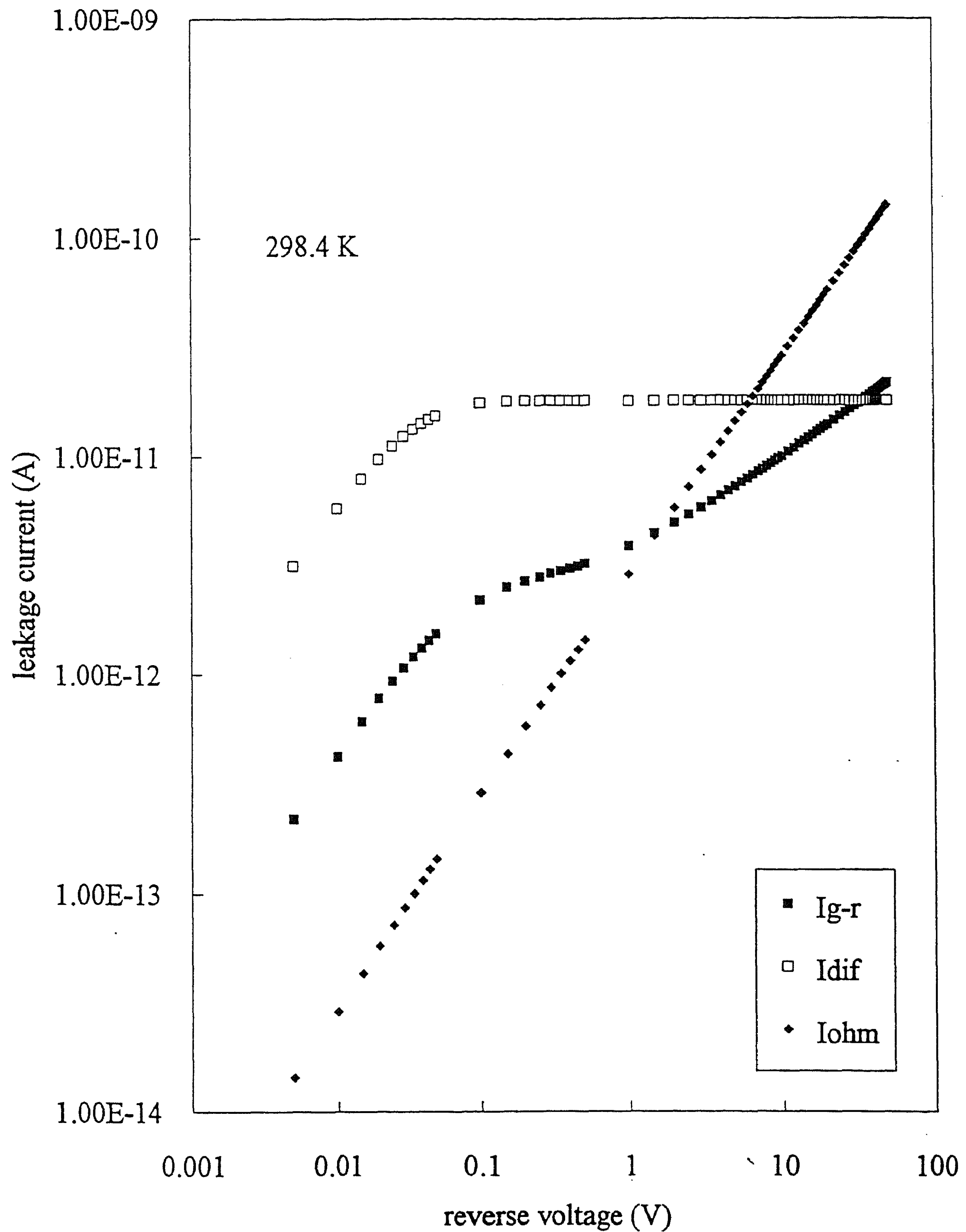

Figure 4.2(a) Simulated results of dark current contributions as a function of reverse voltage at room-temperature.

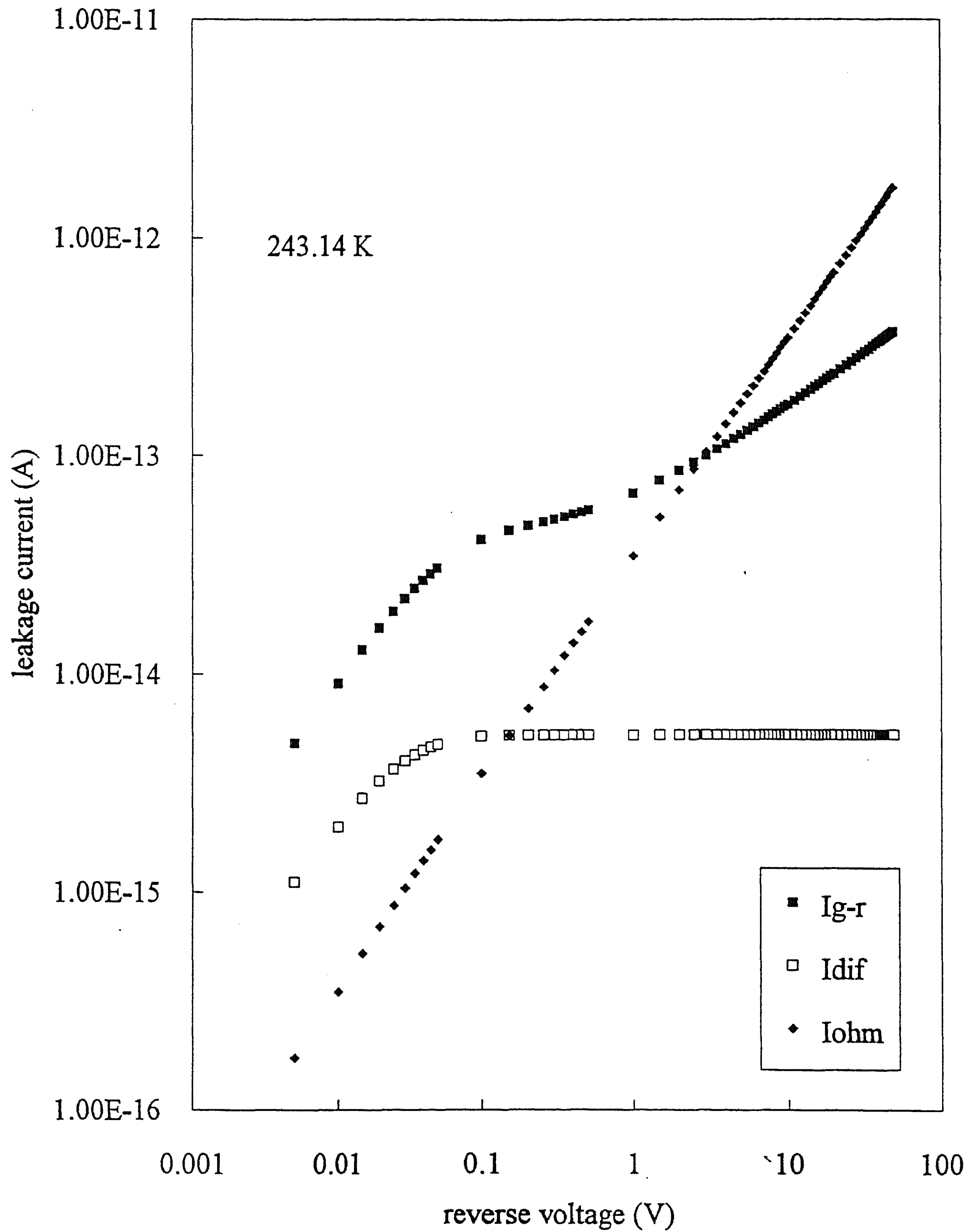

Figure 4.2(b) Simulated results of dark current contributions as a function of reverse voltage at 243 K.

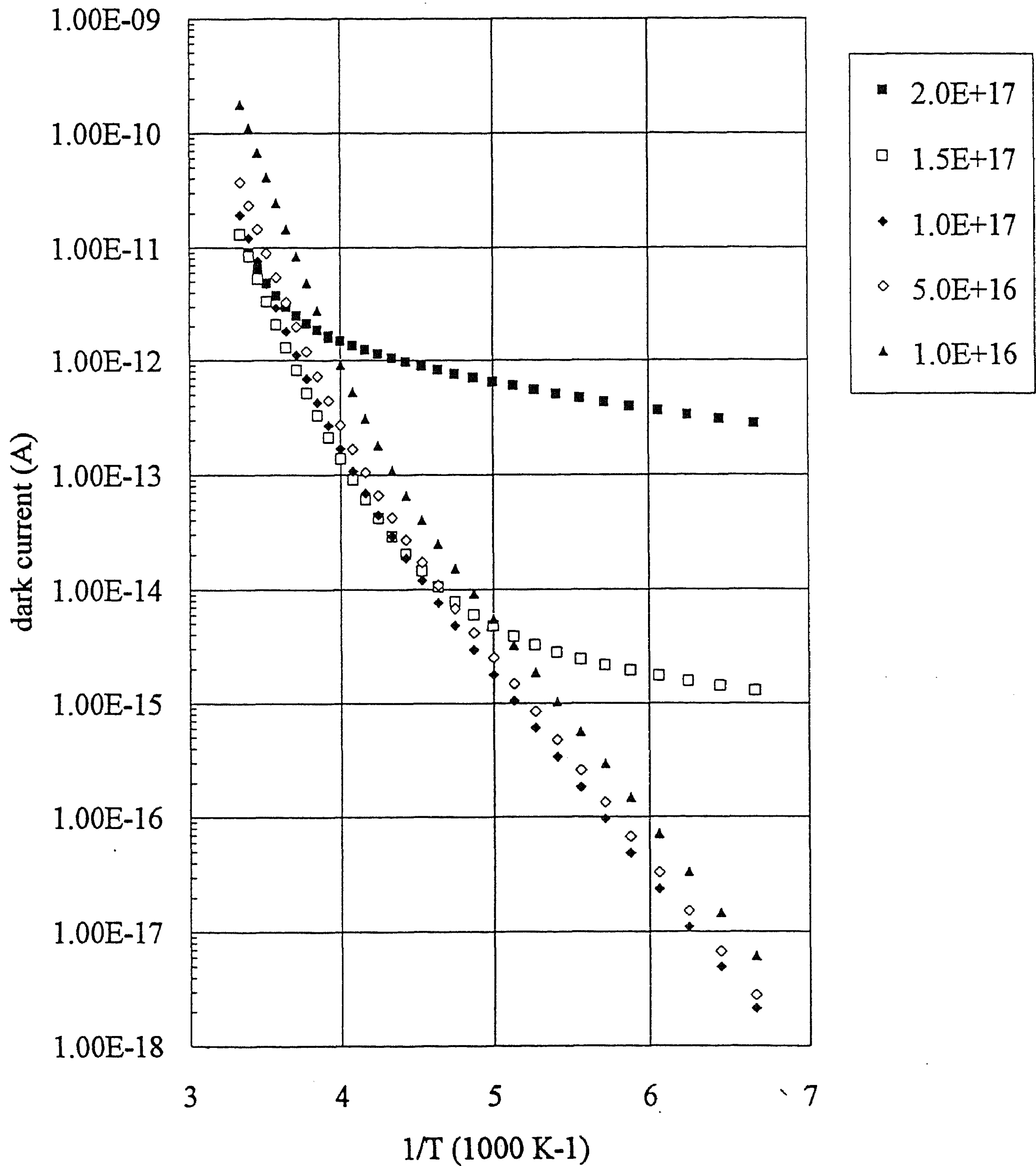

Figure 4.3(a) Simulated results of dark current as a function of temperature and $In_{0.72}Ga_{0.28}As$ layer (2.2 um cut-off) doping.

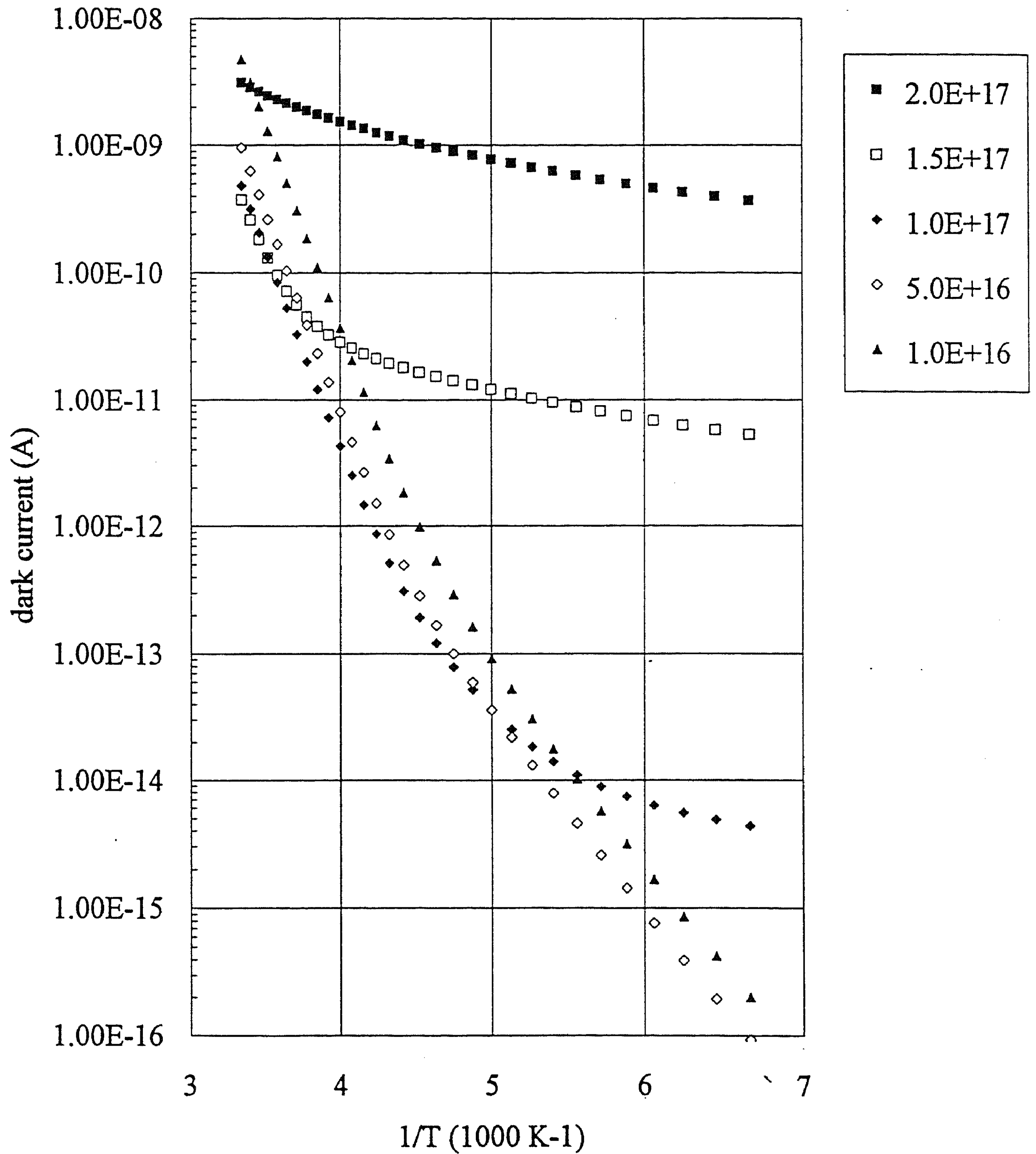

Figure 4.3(b) Simulated results of dark current as a function of temperature and $In_{0.82}Ga_{0.18}As$ (2.6 um cut-off) layer doping.

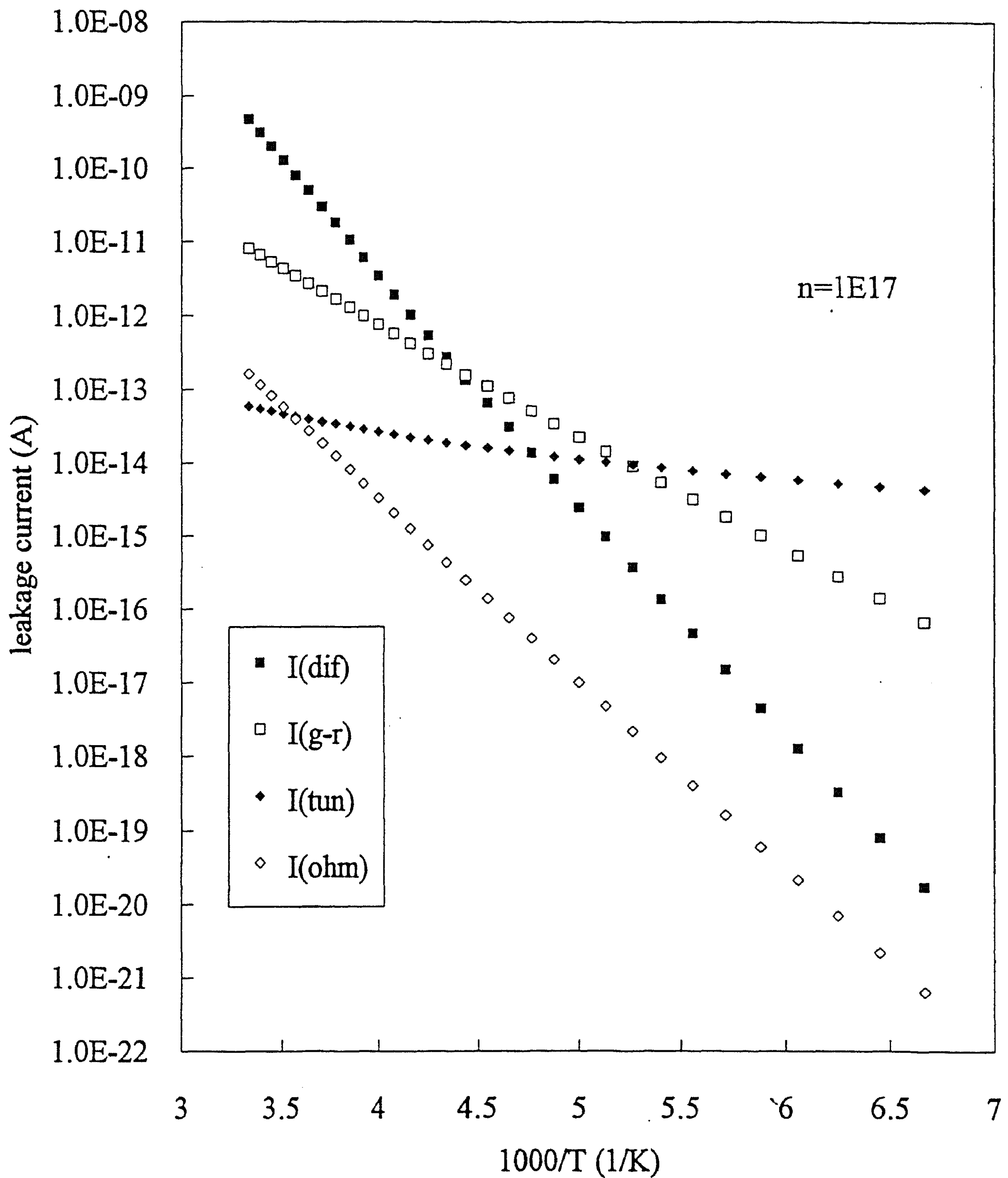

Figure 4.4 Simulated results of dark current contributions as a function of temperature for $In_{0.82}Ga_{0.18}As$ (2.6 um cut-off) detector.

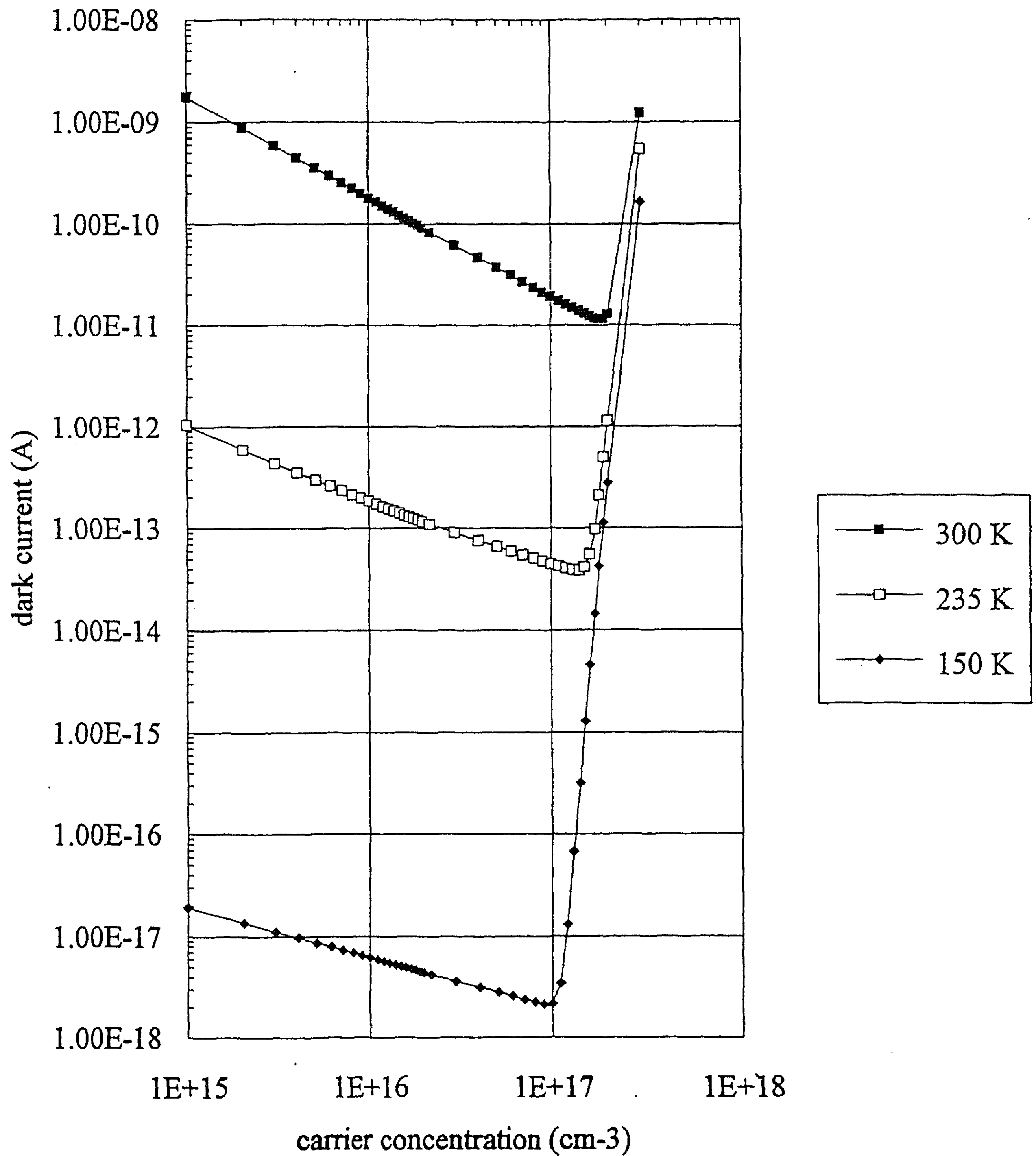

Figure 4.5(a) Simulated results of dark current as a function of temperature and $In_{0.72}Ga_{0.28}As$ (2.2 um cut-off) absorption layer doping.

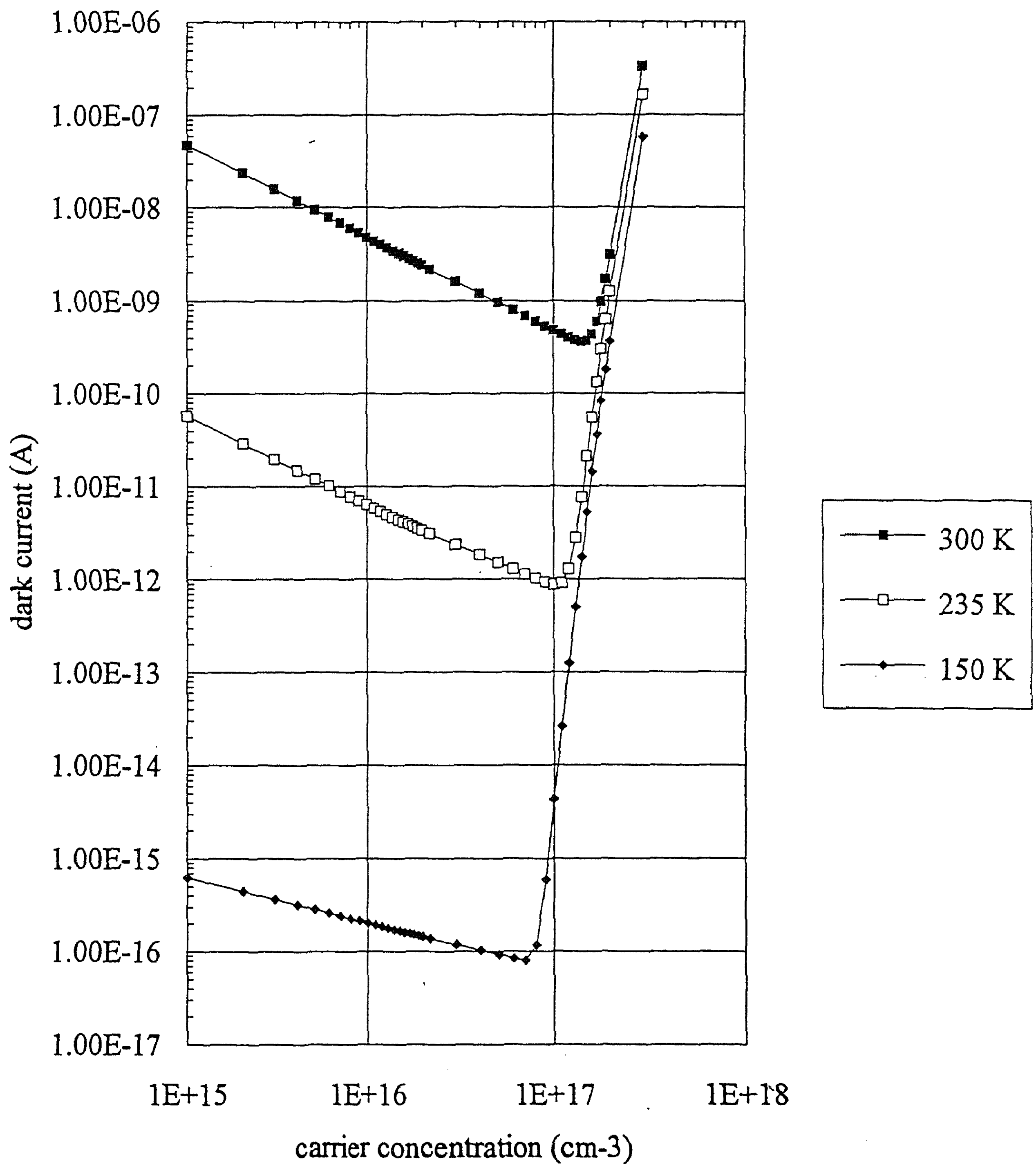

Figure 4.5(b) Simulated results of dark current as a function of temperature and $In_{0.82}Ga_{0.18}As$ (2.6 um cut-off) absorption layer doping.

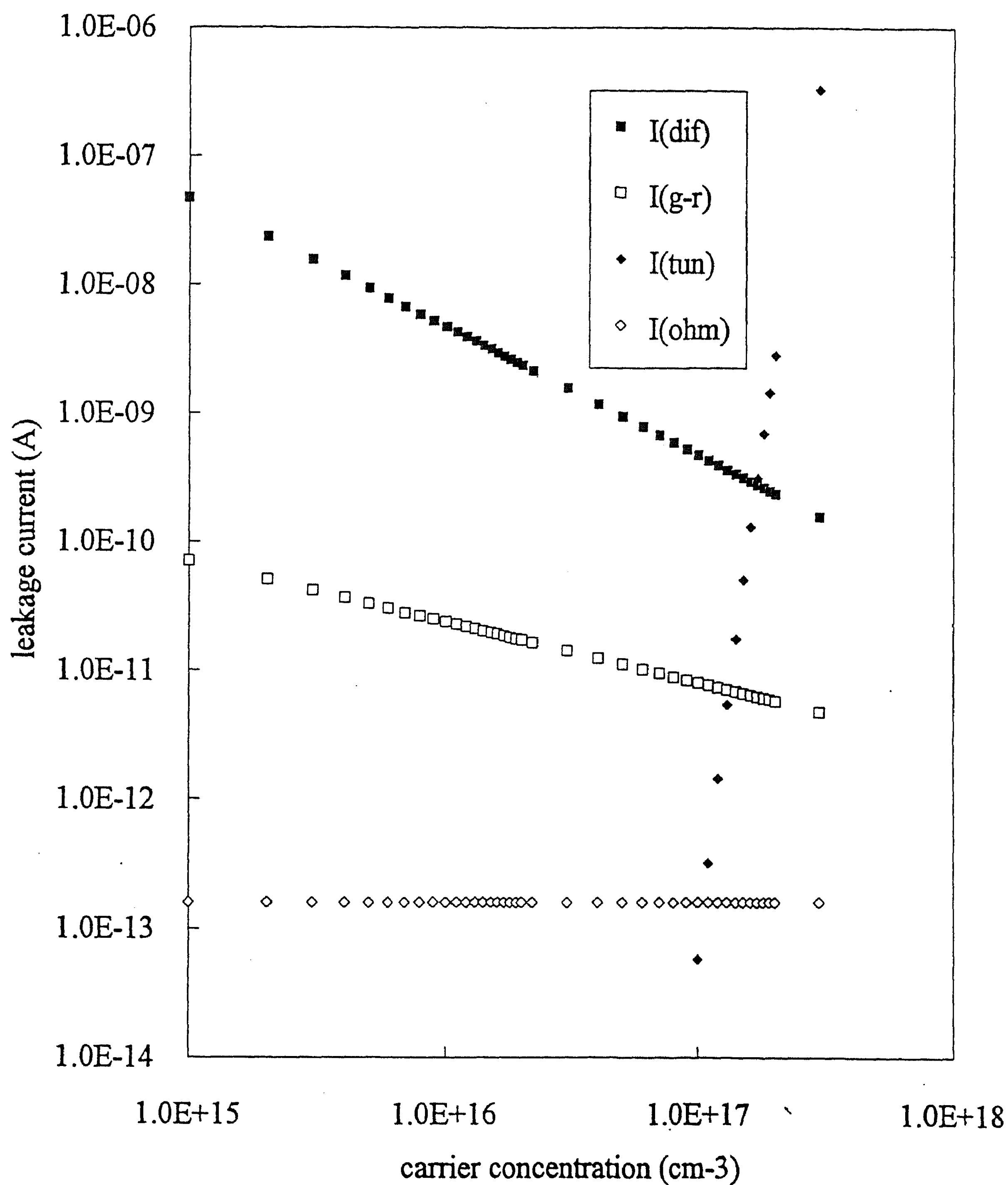

Figure 4.6(a) Simulated results of dark current components as a function of $In_{0.82}Ga_{0.18}As$ (2.6 um cut-off) absorption layer doping at 300 K temperature.

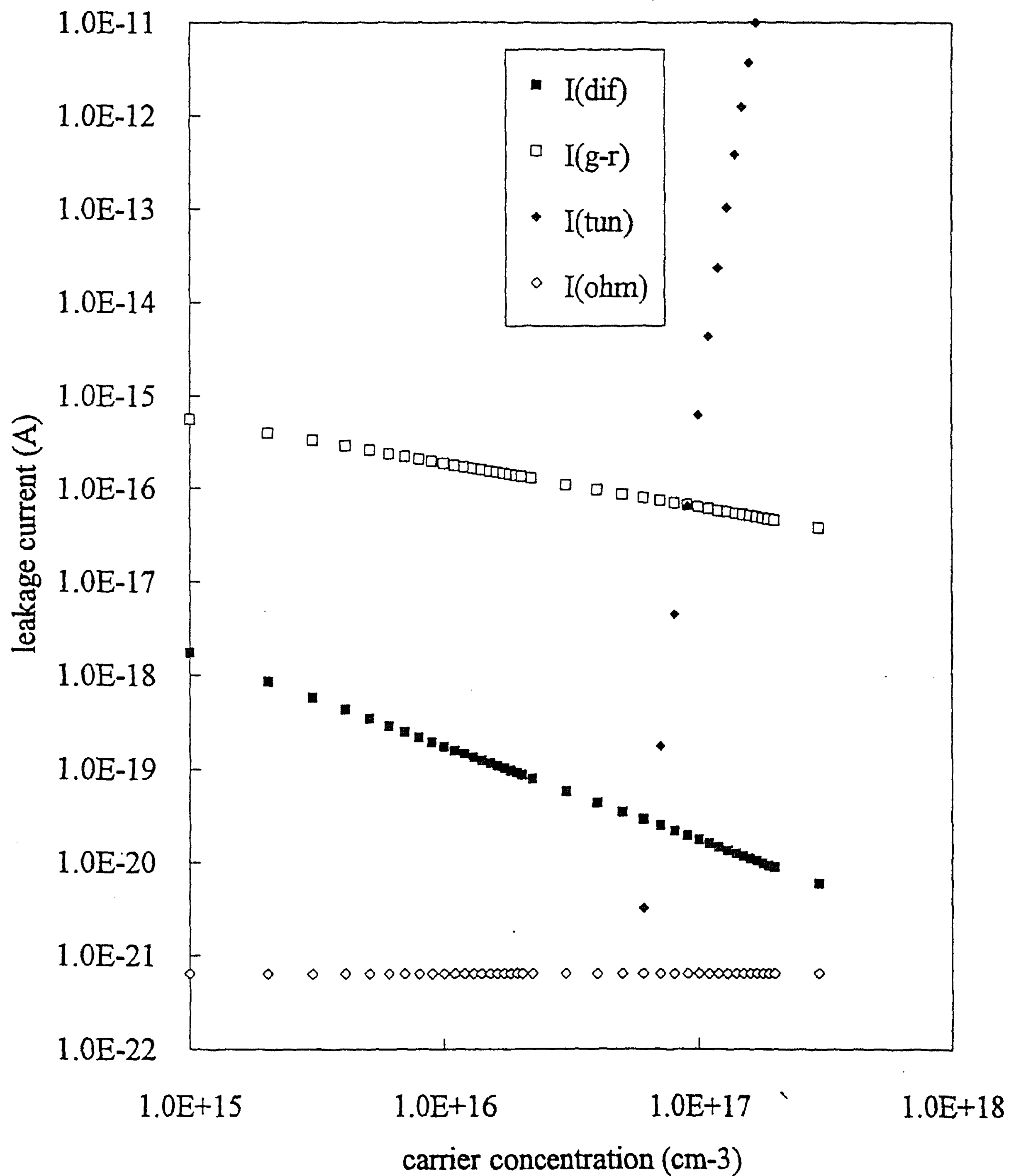

Figure 4.6(b) Simulated results of dark current components as a function of $In_{0.82}Ga_{0.18}As$ (2.6 um cut-off) absorption layer doping at 150 K temperature.

CHAPTER 5

FOCAL PLANE ARRAY (FPA) ARCHITECTURE

5.1 Focal Plane Architecture

The Focal Plane Array arrangement with the detector element and multiplexer metal pads is shown in Fig. 5.1. The two multiplexers are inter-connected through a hybrid multilayer ceramic with isolated and shielded power lines. The two multiplexers and the detector array are integrated in a 24 pin dual-in-line package. The 1024 detector elements and two 512 element (left and right) multiplexers were bonded using a manual wedge bonder.

The focal plane arrays were integrated with 1.7 μm, 1.9 μm, 2.2 μm and 2.6 μm cut-off wavelength InGaAs detectors and the Si read-out multiplexer. The hybrid focal plane arrays were tested in two operating modes. The first mode is without using the non-uniformity compensation and the second with the non-uniformity compensation. The output from the focal plane array was digitized using 16 bit-A/D converter and the data was acquired using a 16 bit frame grabber. The A/D converter was opto-isolated from the frame grabber for better noise immunity.

5.2 Focal Plane Array Integration and Testing

The Si read out multiplexer and 1024 element InGaAs/InP detector arrays are integrated in a 22 pin Dual In Line (DIL) package. The interconnection from the left multiplexer to right multiplexer was done by designing a multi layer hybrid ceramic with 9 layers. The

AC and DC power lines were isolated for better noise immunity. The detectors are connected to the multiplexer contact pads using advanced wedge bonding technique.

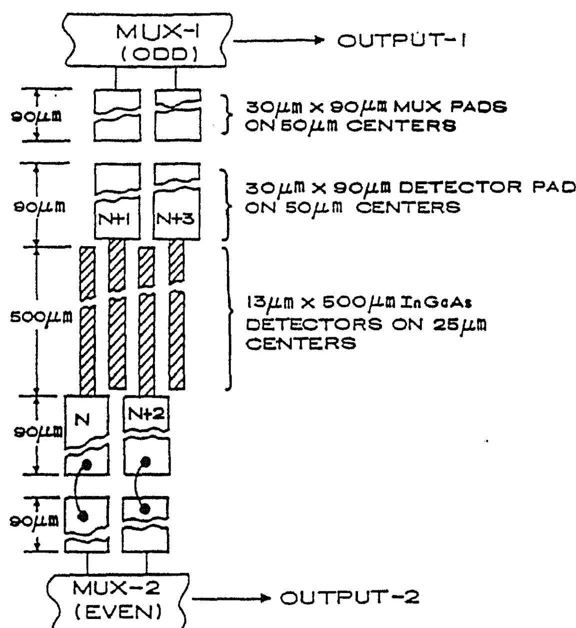

Figure 5.1 Focal Plane Array architecture.

A test set up was designed and developed to test the Si read out multiplexer and completed assembly of Focal plane Arrays. A block diagram of the multiplexer test setup is shown in Fig. 5.2. As shown in Fig. 5.2, the test setup consists of a control module and driver board module on a bench top and connect the two together. Wafer level testing was done using a probe card and connecting the probe card to the driver board module. The master timing sequence board contains the Master Timing Sequencer (MTS) that

generates the FPA timing relationship in accordance to the requirements of the operation of the FPA. The control module implements the timing relationships required by the operational modes. Opto-isolation is provided between the driver board and the digital out put port. The driver board buffers the timing pulses to the focal plane array and develops the low noise biasing circuits for the focal plane array. In addition a unity gain buffer is provided on this board for the output video. The analog processing and A/D converter board contains the HI/LOW gain amplification, Sample/Hold, buffered S/H video and A/D converter. The power supply board contains the AC to DC linear power supplies.

A block diagram of the sequence of the multiplexer control pulses generated by the test setup is shown in Fig. 5.3. The clocks and other logic pulses are supplied to the multiplexer by the clock generator board. These waveforms are shifted from 0 to 5 V rails to -3V to 2V rails on the driver board.

Two different analog channels was provided prior to A/D conversion. LOW gain was to match the dynamic range of the Focal Plane Array (0-2V) to the dynamic range of the A/D converter. HIGH gain will add a factor of 10x to LOW gain. This is provided to improve the signal to noise ratio for low level signals.

The A/D converter board provides 16 bit digitization of the multiplexer voltage output. The integration time is coded during the blanking interval. This data, in addition to the appropriate sync pulses are driven to the frame grabber in the host computer. The digital data from the A/D converter is opto-isolated from the frame grabber.

The frame grabber in the host computer allow the video output signal to be acquired and stored in an ASCII file for later manipulation with a spreadsheet software (MS Excel). The acquisition software interfaces libraries of functions written for the acquisition board with a Microsoft C compiler.

The timing relationships for the clock pulses that run the Focal Plane Array are developed in the MTS. A set of timing waveforms corresponding to mode of operation with periodic uniformity correction will be used as the master timing generator. All the other modes of operation was derived by gating on or off the appropriate waveforms.

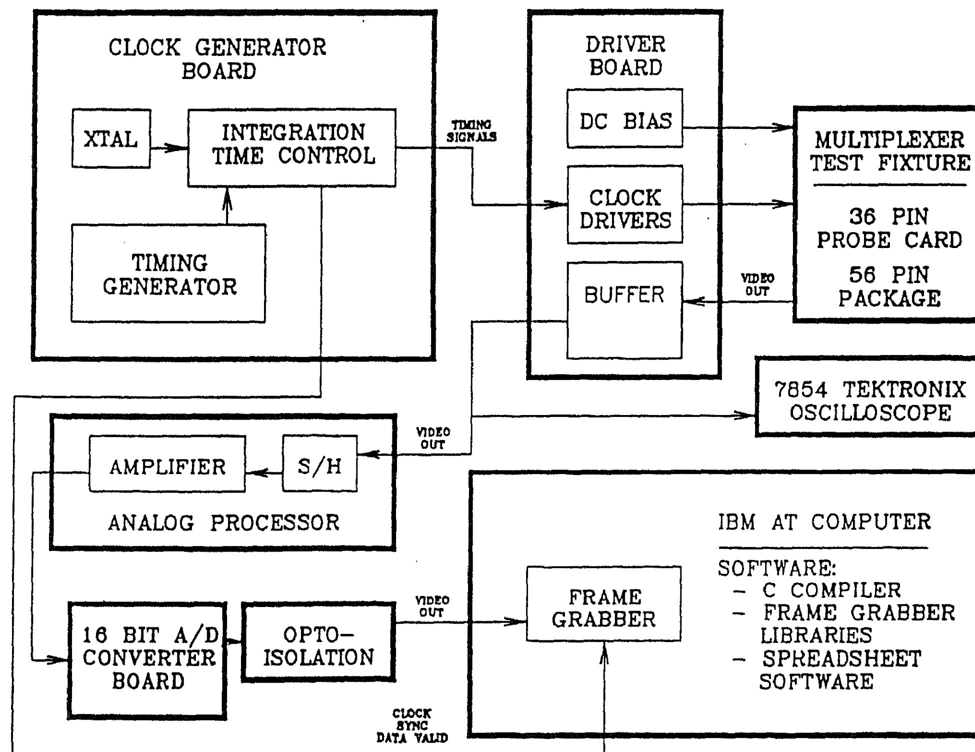

Figure 5.2 Block diagram of the multiplexer test setup.

The electro-optical test setup for the characterization of the completed assembly of InGaAs Focal Plane Array is shown in Fig 5.4. The Focal Plane Array test setup requires a temperature controller to control the operating temperature of the FPA from 300 K to 77 K, Ln_2 dewar to cool the FPA to 150 K, a sorption pump to pump the dewar vacuum to < 10^{-3} Torr and a black body radiation source to test the optical performance of the focal plane array[62]. The electrical schematic of the FPA test setup is similar to the multiplexer test setup shown in Fig. 5.2.

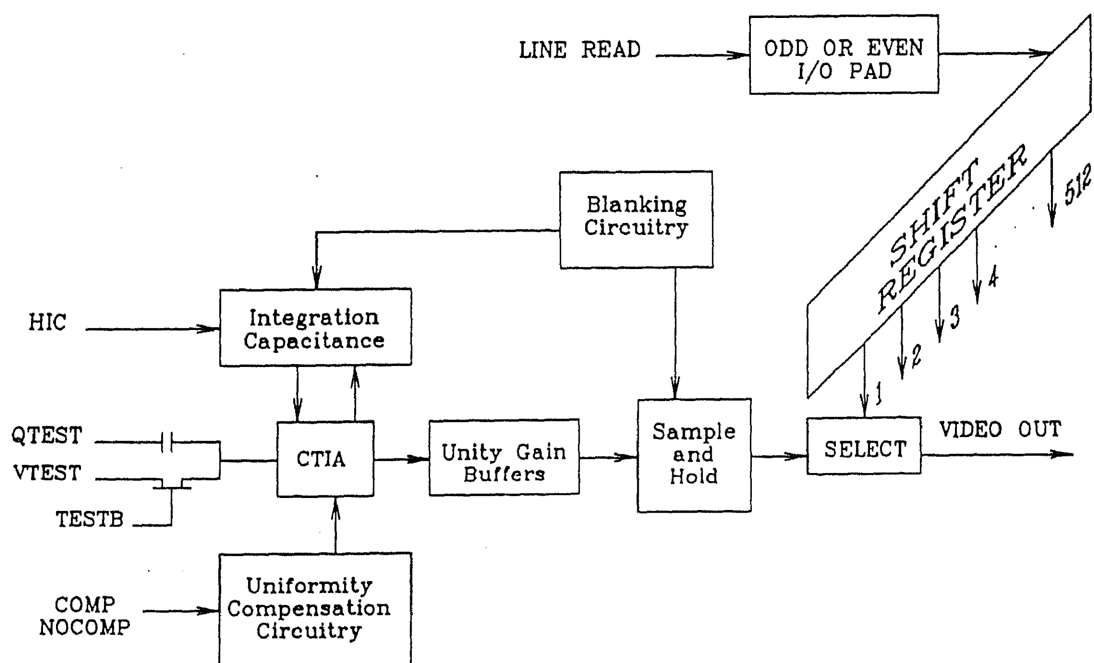

Figure 5.3 Functional block diagram of the multiplexer test setup.

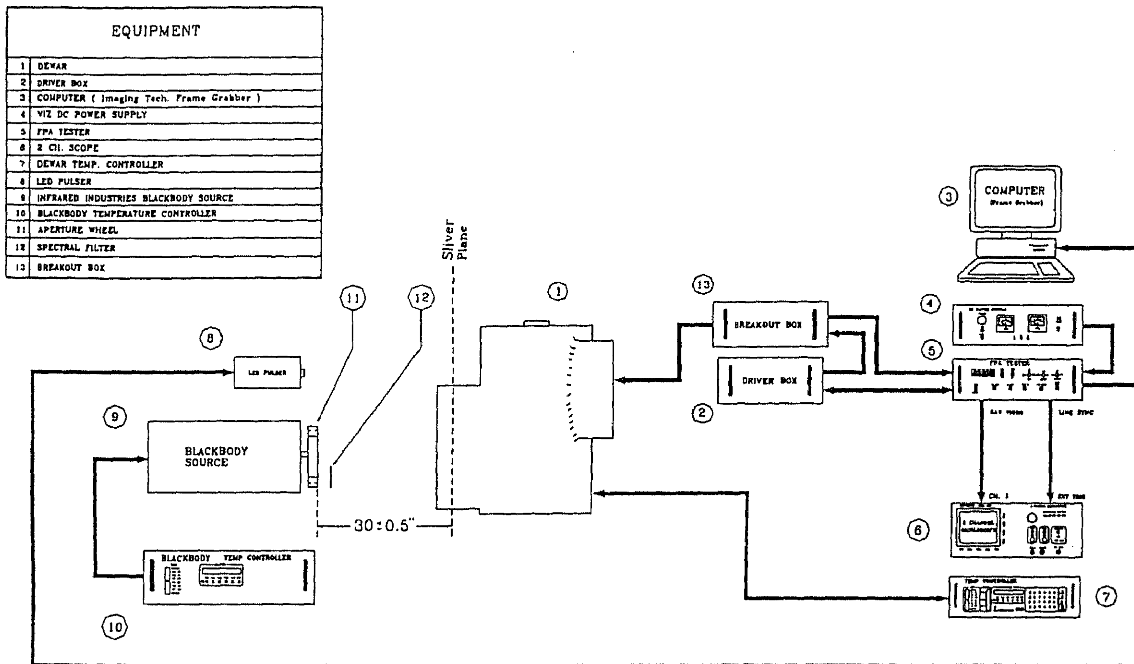

Figure 5.4 Block diagram of the InGaAs Focal Plane Array test setup.

CHAPTER 6

READ-OUT ELECTRONICS

This chapter describes the design of a 512-element CTIA multiplexer developed for readout of an array of 1024-element InGaAs detectors for operation with a bias voltage in the range of ±10 mV[63]. This multiplexer can be operated with a left-to-right or right-to-left scan, a non-destructive sequential readout with line-by-line selectable detector reset, and with or without input-MOSFET-threshold uniformity correction. The optical integration time in the range from 20 ms to 10 min is selectable in multiples of 20 to 40 ms line times. The multiplexer cell architecture includes a differential CTIA with open-loop gain of about 5000, a CDS circuit, and two unity-gain buffer amplifiers. The CTIA integrator can be operated with a feedback capacitance of 0.8 pF or 2.4 pF for saturation charge signal of either 10^7 and $3x10^7$ electrons/pixel, respectively. The multiplexer was designed for operation with power dissipation of less than 10 mW, with maximum non-linearity < 0.1%, and for readout noise of < 400 rms. e^-/p for $Qmax=10^7$ e^-/p and 600 rms. e^-/p for $Qmax=3x10^7$ e^-/p when operating with InGaAs detectors having capacitance of 12 pF and shunt resistance in the range of 10^{11} to 10^{13} ohms. The multiplexer is fabricated with 1.25-μm N-well radiation hard Honeywell CMOS process (RICMOS III) and measured performance results are presented.

6.1 Introduction

The dark currents of InGaAs detectors at a bias voltage of 10 mV are in the ranges[64] of 0.8 to 1.0 fA at 200K for 1.7 um cut-off, 2.0 to 50 fA at 150K for 2.2 um cut-off, and 7.0 to 150 fA at 150K for 2.6 um cut-off wavelength, corresponding to detector shunt resistanceís of > 10^{13} ohm for 1.7 um cut-off, 5×10^{12} to 2 $\times 10^{11}$ ohms for 2.2 um cut-off, and 1.5×10^{12} to 6.6×10^{10} ohms for 2.6 um cut-off wavelength. To achieve the required sensitivity and dynamic range, a saturation charge signal (QMAX) has been selected as 3×10^7 electrons/pixel for 1.7 um cut-off detectors and 10^7 electrons/pixel for 2.2 and 2.6 um cut-off wavelength detectors. The Multiplexer readout noise should not exceed 400 rms. electrons/pixel for QMAX of 10^7 electrons/pixel and 700 rms. electrons/pixel for QMAX of 3×10^7 electrons/pixel, and the optical integration time, t_{int}, has been selected to be from 31.25 ms (one line time) up to 10 min. To obtain the required radiometric accuracy, the InGaAs FPA should have non-linearity < 0.1% over full dynamic range and pixel-to-pixel readout memory of 0.1%.

6.2 Performance and Design Specifications

The performance and design specifications of InGaAs multiplexer (MUX) for detectors with cut-off wavelengths of 1.7, 2.2 and 2.6 um are summarized in Table 6.1. The above performance goals and design specifications are reflected in the design of the multiplexer described in section 6.3.

Table 6.1 Performance and design specifications of InGaAs multiplexer.

1. IR detector array to be readout	1024-element InGaAs with 1.7, 2.2, and 2.6 μm cut-off wavelength, C_D=16pF and I_{dark}=1.0 -150 fA at 10 mV bias
2. Multiplexer detector pads	30 x 90 μm on 50 μm centers
3. FPA Readout organization	Two 512-element CMOS CTIA multiplexers (odd and even) with CDS at each pixel and interlaced readout
4. Scan direction control	Single multiplexer with electrically controllable left-to-right or right-to-left scan
5. Package	24-pin dual-in-line (DIP) with ceramic lead insert
6. Multiplexer readout modes	Non-destructive sequential (serial) detector readout with line-by-line selectable detector reset (1) with or (2) without uniformity correction
7. Optical integration time, t_{int}	31.25 ms to 10min —— selectable in multiples of line time of 31.25 ms
8. All clock voltages and power supplies	0 to 5 V with detector substrate (DSUB) nominally at 3V as the analog signal reference, or -3V to 2V with DSUB as the reference ground
9. CTIA power supply rejection ratio	~1000:1
10. Detector (photodidode) bias voltage	0 Volts nominal with diode-to-diode bias variation of ≤ 2mV adjustable from -10 to +10 mV by -5 to 5V through 500:1 attenuator with respect to DSUB
11. Saturation charge signal, Q_{max}	10^7 and 3×10^7 e^-/p selectable by external control
12. Operating temperature	150 K for Channel 7 and 8 and 200 K for Channel 6
13. Temperature stability	Maximum obtainable (TBD experimentally)
14. Power dissipation	< 25 mW for t_{int} = 31.25 ms
15. Multiplexer readout noise	< 400 rms e^-/p for $Q_{max} = 10^7 e^-/p$ < 700 rms e^-/p for $Q_{max} = 3\times10^7 e^-/p$ [Not including the compensation noise]
16. Nonlinearity	< 0.1% over the dynamic range
17. Memory between successive pixels	< 0.1%
18. Radiation hardness	9 to 15 Krad (Si) total dose and immunity to latch-up for single event upset

6.2.1 MUX Architecture

The 1024-element InGaAs near infrared detector arrays, with 1.7, 2.2, and 2.6 μm cut-off wavelengths are readout by two 512-element CMOS CTIA multiplexers (ODD and EVEN) with correlated-double-sampling (CDS) circuit at each pixel location.

The odd and even multiplexers are designed for operation with an interlaced readout when the outputs of both multiplexers are connected to the same output terminal.

6.2.2 MUX Scan Control

The scan direction of the 512-element multiplexer is electronically controlled to enable the scan direction to go from 1 to 512 element for ODD multiplexer or from 512 to 1 for EVEN multiplexer. This control is accomplished depending to which MUX pad (ODD or EVEN) the line read pulse is connected.

6.2.3 24-pin Package

The 1024-element InGaAs detector focal plane assembly with ODD and EVEN MUX readout is bonded in a 24-pin DIP package with a thick-film multilayer substrate for in-package connections.

6.2.4 Modes of Operation

The multiplexer can be operated either with (COMP) or without (NOCOMP) compensation for MOSFET threshold voltage (V_{TH}) of the CTIA. The third mode of operation is a stored compensation (STORECOMP). In this case the MOSFET threshold correction is performed once and is stored for an extended time (hours or days). The normal mode of operation of the multiplexer consists of a non-destructive sequential (serial) readout with line-by-line selectable detector reset. In this case, the optical integration time, t_{int}, is selectable in multiples of 31.75 ms line times.

6.2.5 Optical Integration Time

To allow optical integration time, t_{int}, of up to 10 min., the CTIA of the MUX input circuit has been designed with an open-loop gain of 5000. Thus the effective time constant of the detector input terminal is

$$\tau_{DET} = 5000 \cdot C_{fd} \cdot R_D \tag{6.1}$$

where C_{fd} is the CTIA feedback capacitance of 0.8 or 2.4 pF and

R_D is the detector shunt resistance near zero bias of 10^{11} to 10^{13} ohms.

Assuming $R_D=10^{12}$ and $C_{fd}=0.8$ pF the value of τ_{DET} is 4000 s.

6.2.6 Clock Voltages and Power Supplies

The multiplexer has been designed for operation with digital (V_{DD} and V_{SS}) and analog (AMPHI and AMPLO) power supplies as well as all external clock voltages of 0 to 5V with the detector substrate (DSUB) nominally at 3V. However, all material presented in this paper assumes that the multiplexer is operated with a nominal low voltage of -3V and a nominal high voltage of 2V with reference to the detector substrate voltage, DSUB.

6.2.7 Detect Bias Voltage

The multiplexer has been designed to operate the InGaAs detector array at zero or near zero bias voltage. An externally controllable detector bias voltage from 0 to ±10 mV is provided via 500:1 attenuator for a ±5 V external control voltage (FINEBIAS).

6.2.8 Power Supply and FINEBIAS Stability

Assuming a total input capacitance of 16 pF and CTIA feedback capacitance C_{fb}=0.8 pF, a power-supply-induced CTIA input voltage of 1.0 μV is expected to result in MUX output fluctuation corresponding to 100 electrons. Therefore, in order to maintain power supply induced noise not exceeding 100 rms. electrons/pixel, the design goal of the multiplexer was to achieve a power supply rejection ratio (PSRR) of 1000. However, the initial tests of the multiplexer indicate a low frequency PSRR of 100:1 and less than 10:1 at clock frequency of 18 kHz. But an effective PSRR is provided for the control of the detector bias voltage by 500:1 attenuation of external FINEBIAS control voltage.

6.2.9 Saturation Charge Signal

The multiplexer has been designed for operation with saturation charge signal, Qmax, 10^7 or $3X10^7$ electrons/pixel. For a maximum sensing voltage of 2V, a fixed CTIA feedback capacitor of 0.8 pF was used and an additional capacitor of 1.6 pF that can be added under an external control.

6.2.10 Operating Temperature and Temperature Stability

The operating temperature is 150K for 2.2 and 2.6 um cut-off wavelength detectors and 200K for 1.7 um cut-off wavelength detectors. Temperature stability, ΔT, requirement represents a parameter that still has to be determined experimentally. The multiplexer, however, was designed with an objective to achieve a maximum obtainable temperature stability.

6.2.11 Power Dissipation

The total power dissipation is about 18 mW for two multiplexers operating at the minimum integration time of 31.75 ms (i.e. requiring continuous clocking).

6.2.12 Readout Noise

As illustrated in Table 2, the readout noise of < 400 and 700 rms. electrons/pixel is expected for operation without compensation for CTIA non-uniformityís for QMAX of 10^7, and $3x10^7$ electrons/pixel, respectively.

Table 6.2 Calculated Readout Noise of InGaAs Multiplexers.

	Readout Noise (rms electrons/pixel)		
	Channel 6 T=200 K $R_D=10^{13}\,\Omega$ C_D=10 pF C_{fb}=2.4 pF	Channel 7 T=150 K $R_D=10^{12}\,\Omega$ C_D=16 pF C_{fb}=0.8 pF	Channel 8 T=150 K $R_D=10^{11}\,(10^{12})\,\Omega$ C_D=16 pF C_{fb}=0.8 pF
Compensation Noise $\left[\frac{kT}{C_{OFFSET}}\right]^{\frac{1}{2}} \cdot \frac{t_{int}}{R_D}$, for $t_{int} = 1.5s$	17.6	176	1760 (176)
kTC Noise not removed by CDS $C_{fb}\sqrt{\frac{kT}{C_S}+\frac{kT}{C_{S-H}}}$;	489	130	130
MOS Channel Broadband Noise $\left[\frac{2kT C_{fb}(C_D + C_{fb})}{C_L}\right]^{\frac{1}{2}}$	506	273	273
MOS Channel 1/f Noise (a) $\frac{1.0\mu V(t_{int})}{R_D}$ for $t_{int} = 1.5s$ (b) $1.0\mu V(C_D + C_{fb})$	0.9 76	9 105	90 (9) 105
Total Readout Noise (a) With Compensation (b) Without Compensation or with Stored Compensation	708 708	365 320	1791 (376) 332 (319)

Note: C_{OFFSET}=5.8 pF, C_L=28.7 pF, C_S=5.6 pF, C_{S-H}=6.7 pF

However, for operation with compensation for CTIA non-uniformityís, the MUX readout noise has an additional noise component that is linearly dependent on the detector resistance, R_D, and optical integration time, t_{int}, and can be significant for $R_D < 10^{12}$ ohms and $t_{int} > 1.0$ s.

The additional compensation noise, however, could be avoided by operation in a "stored compensation" mode. In this case a compensation cycle is followed by a correction for the fixed pattern noise induced by the operation of the multiplexer for hours or days with the compensation voltage stored on the C_{OFFSET} capacitors (Fig. 6.1).

6.2.13 Non-Linearity

The design goal was to achieve a linear operation over full signal range with non-linearity of less than 0.1%. To obtain this linear capacitor process was developed (see Section 6.5.2). The measured data shows a non-linearity of < 0.3%.

6.2.14 Pixel Memory

The slowest part of the multiplexer readout is the output buffer that has a slew rate of 0.75 V/μs and time constant of 0.133 μs. These parameters should assure that the MUX output bus will decay between pixel readouts to less than 0.1%.

6.2.15 Radiation Hardness

To achieve the radiation hardness requirement of 9 to 15 Krad (Si) total dose and immunity to latch-up for single event upset the multiplexers were fabricated by Honeywell radiation-hard (RICMOS III) process.

6.3 Design of the Multiplexer

6.3.1 General Description

The design of the multiplexer input circuit, i.e. a unit cell or a pixel cell, shown in Fig. 6.1 consists of:

(1) A capacitive transimpedance amplifier, CTIA, in the form of a differential opamp with an open loop gain of about 5,000 at a bias current, I_{BIAS}, of 2.0 μA. As will be explained in Sections 6.3.2 and 6.3.4, this CTIA can be operated with or without uniformity compensation. The CTIA normally operates with a feedback capacitor $C_{fb\text{-}1}$=0.8 pF but with HIC control voltage at AMPLO voltage (-3V) an additional feedback capacitor $C_{fb\text{-}2}$=1.6 pF is added to increase the maximum charge signal nominally from 10^7 to 3×10^7 electrons/pixel.

(2) A correlated double sampling (CDS) circuit with an unity-gain buffer No.1 before the sampling switch and an unity-gain buffer No.2 after the sampling switch (or transmission gate). The second buffer was introduced to remove the effect of voltage feedthrough from the selected T1 MOSFET (see Fig. 6.3) to the sample-and-hold capacitor, $C_{S\text{-}H}$.

(3) A PFET buffered CMOS switch, SW9. As shown in Fig. 3, the above PFET, T1, serves as an input transistor for a differential pair circuit configured at the multiplexer output bus with a current mirror for compensation of the threshold voltage, V_{TH}, drop at the source of the T1 input PFET.

The combination of the CDS and a buffered sample-and-hold circuit at the pixel cells allows non-destructive readout and line-by-line resettable operation with optical

integration time adjustable in multiples of 31.75 ms line times. It should also be mentioned that low noise readout from a large capacitance (14 pF) IR detector by a CTIA requires large load capacitance (C_L=28.7 pF in Fig. 6.1).

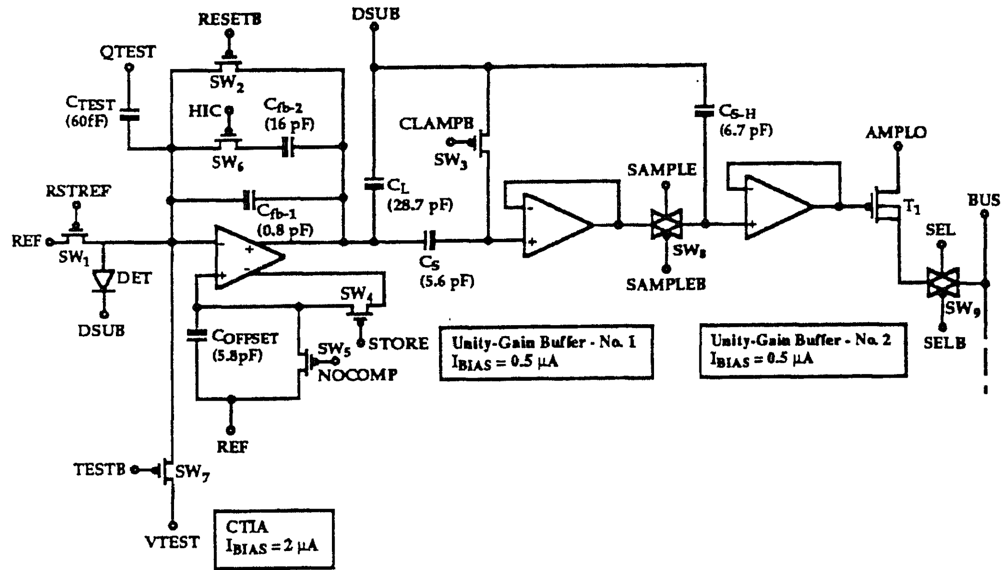

Figure 6.1 Schematic of the multiplexer input circuit.

For estimation of the response time of the CTIA, the closed loop time constant can be expressed as:

$$Closed\ \ loop\ \ \tau = \frac{C_L\left(C_D + C_{fd}\right)}{gm \cdot C_{fd}} \tag{6.2}$$

where: C_L=28.7 pF is the CTIA load capacitance,

C_D=14 pF is the detector capacitance for 2.6 um detector,

C_{fb}=0.8 or 2.4 pF is the CTIA feedback capacitance, and

g_m=10 I_D=10 μmhos is the transconductance of the input PFETs.

Since for normal closed loop operation C_L=28.7 pF and during the CDS clamp operation the effective C_L=34.3 pF, the time constants for CTIA are 45 μs and 54 μs for C_{fb}=0.8 pF and 17 μs and 21 μs for C_{fb}=2.4 pF. However, during the CTIA reset operation the slew rate is:

$$\frac{I_D}{C_L} = \frac{1.0\mu A}{34.3\,pF} = \frac{1.0V}{34.3\mu s}, \tag{6.3}$$

and the time constant is

$$\tau = \frac{C_L}{10 I_D} = \frac{34.3\,pF}{10 \times 1.0\mu A} = 3.4\mu s \tag{6.4}$$

For operation with a bias current I_{BIAS}=2.0 μA, the total CTIA power dissipation for two multiplexers is 10 mW.

The unity-gain buffers No.1 and No.2, shown in Fig. 6.4, were designed for operation with I_{BIAS}=0.5μA and total power dissipation of 2.5 mW. The slew rate of the slower unity-gain buffer No.1 is 1.0 V/24 μs, and time constant of 2.4 μs.

The selectable (gated) pixel output amplifier split between the pixel cell and the multiplexer output bus, shown in Fig. 6.2, was designed with I_{BIAS}=50 μA. The resulting total power dissipation for two multiplexers is estimated as 0.75 mW. Assuming a total bus capacitance of 20 pF, the slew rate is estimated as 1.0 V/0.8 μs, and the time constant as 0.08 μs.

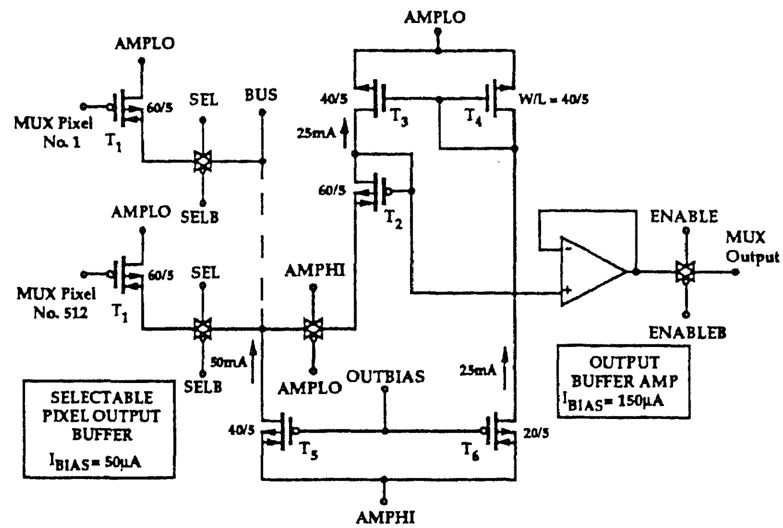

Figure 6.2 Selectable MUX pixel buffer.

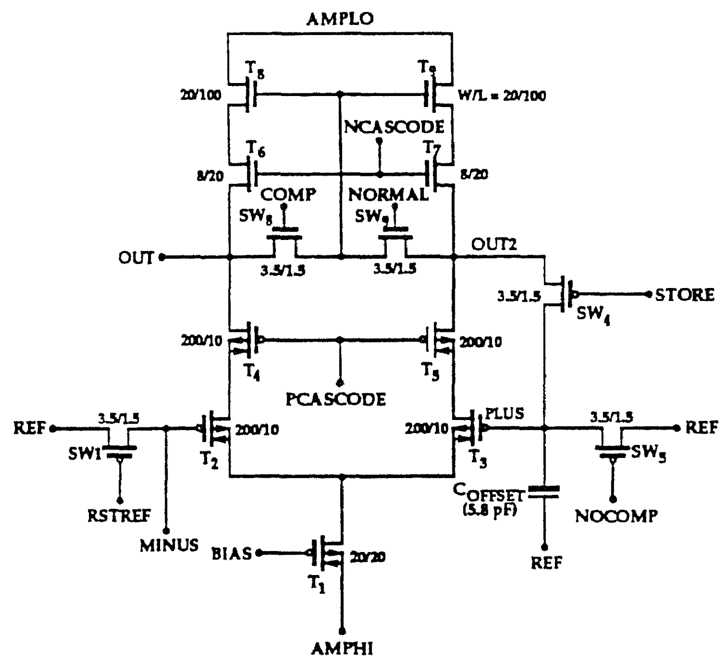

Figure 6.3 CTIA of the MUX input circuit.

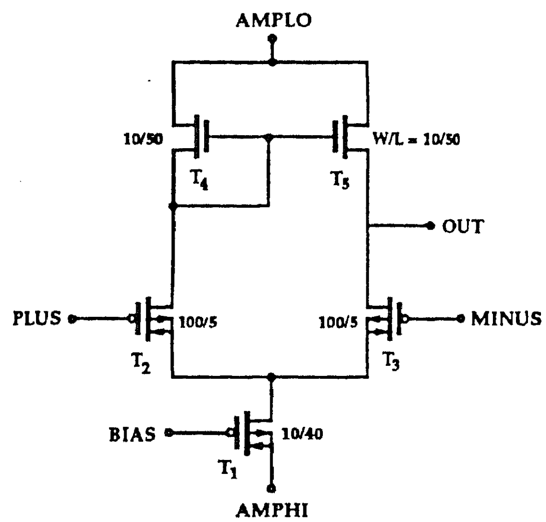

Figure 6.4 Opamp for unity-gain-buffer No.1 and No.2.

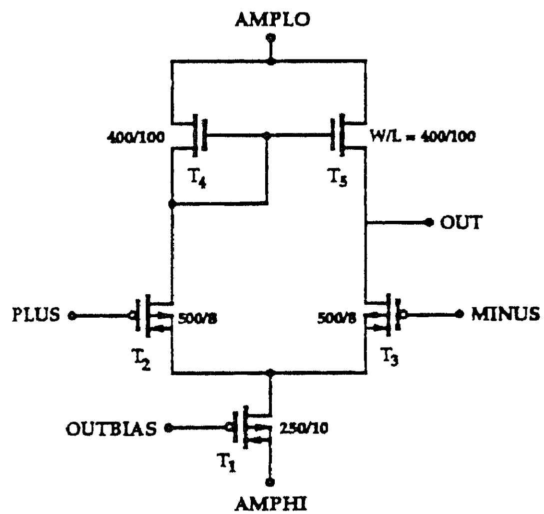

Figure 6.5 Opamp for output buffer.

The unity-gain output buffer (Fig. 6.5) was designed for operation with I_{BIAS}=150μA. This results in total power dissipation for the two multiplexers of 1.5 mW. Assuming an output capacitance of 100 pF, the slew rate is estimated as 0.75 V/μs and the time constant as 0.133 μs.

As illustrated in Fig. 6.1, the polarity of the linear capacitor has been chosen to place the polysilicon gate (designated by the thicker terminal) at the critical high impedance mode requiring low leakage current. The reversed biased N^+ terminal is shown as the thinner electrode.

6.3.2 Operation without Uniformity Compensation

This section describes the operation of the multiplexer without compensation for MOSFET threshold voltage (V_{TH}) non-uniformity at the CTIA. For this mode of operation (Fig. 6.2) the PFET switch SW-4 is opened (for STORE=2V) and the plus (+) input terminal of the CTIA is connected to the reference voltage by the switch SW5 (for NOCOMP=-3V). The switch SW8 is kept opened (for COMP=-3V) and switch SW9 is kept closed (for NORMAL=2V). Note, the switches SW8 and SW9 (shown in Fig. 6.5) control the connection of the bias voltage for T8 and T9 NFETs to facilitate the operation with uniformity compensation described in the next section. However, for operation without uniformity compensation, the switch SW9 is kept closed while the switch SW8 is kept opened. This keeps the NFET bias at the CTIA negative output potential (Out 2).

The critical waveforms for operation without uniformity compensation are shown in Fig. 6.6. A read-reset cycle is started by closing switch SW8 with the SAMPLE pulse

during the line blanking time, T_{BK}. This operation stores the charge signals from the previous line on the sample-and-hold capacitors, $C_{S\text{-}H}$, and makes them available during the line readout time, T_{RD}. Note, that assuming a blanking time T_{BK}=3.16 ms and line time T_L=31.75 ms, the available line readout time T_{RD}=28.59 ms.

The next operation consists of closing the switch SW2 by application of RESET pulse. At the end of the RESET pulse the CTIA feedback capacitance is reset to zero voltage. Then at the end of the CLAMP pulse which clamps the series capacitance C_S of the CDS circuit to DSUB voltage, the kTC noise as well as other noise associated with the resetting of the feedback capacitor C_{fb} is stored with a reversed polarity on the series capacitor C_S. At this point a new optical integration time, t_{int}, is initiated. Since all of the CTIAs are reset simultaneously during the line blanking time, T_{BK}, the minimum optical integration time in this mode of operation is about one line time, T_L, and the t_{int} can be externally controlled in multiples of T_L.[1]

Figure 6.6 also illustrates the non-destructive readout in which case the output of the CTIA is sampled without resetting the CTTI and the CDS circuit.

6.3.3 Operation with Uniformity Compensation

To facilitate operation of the multiplexer with very low and nominally zero bias detector voltage, the CTIA shown in Fig. 6.3 has been designed to be operated with periodic

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[1] More precisely, the minimum value of t_{int} is the line time minus the time from the end of the SAMPLE pulse to the end of the CLAMP pulse.

compensation for MOSFET threshold voltage non-uniformities. This feature is also expected to improve the radiation hardness of the multiplexers.

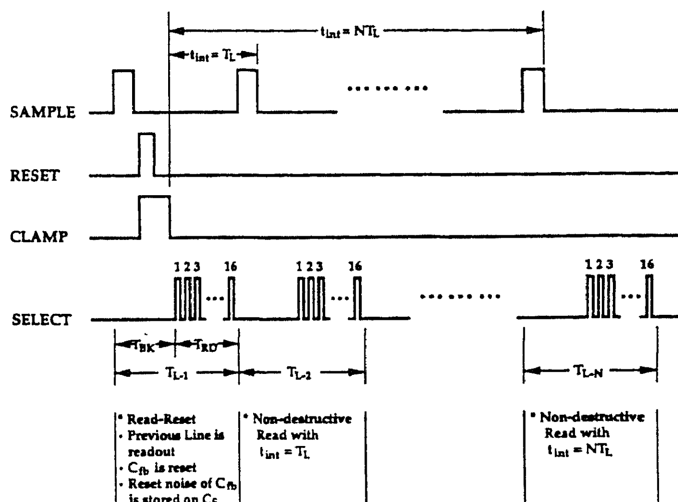

Figure 6.6 Clock waveforms for operation of multiplexer without non-uniformity correction.

The clock waveforms for operation of the multiplexer with MOSFET-threshold-voltage uniformity compensation are shown in Fig. 6.7. In this mode of operation the SW5 switch is open by external control voltage NOCOMP=2V. As in the case of operation without uniformity compensation, the read-reset cycle in this mode of operation is started by the SAMPLE pulse at the beginning of the line blanking time, T_{BK}, that

closes the SW8 PFET-NFET switch. This operation stores the charge signals from the previous line on the sample-and-hold capacitors, C_{S-H}, for subsequent readout during the line readout time, T_{RD}.

The next sequence of events resets the CTIA feedback capacitors C_{fb-1} or $C_{fb-1}+C_{fb-2}$ to zero volts (0V) and stores an off-set voltage on the C_{OFFSET} capacitor at the positive (+) input to the CTIA. The above sequence of events is initiated by the following clock pulses that can have the same starting time:

(1) The clock pulse RSTREF closes SW1 PFET switch and connects the negative (-) input of CTIA to the reference voltage, REF. The generation of the detector bias voltage, REF, is shown in Fig. 6.8.

(2) The RESET pulse closes SW2 switch and resets the feedback capacitors C_{fb-1} or $C_{fb-1}+C_{fb-2}$ (for HiC=-3V) to zero volts.

(3) CTIA is reconfigured by switching the bias for NFET, T8 and T9 from positive (+) output (OUT2) to the negative (-) output (OUT) shown in Fig. 6.3. This operation is accomplished by opening SW9 and closing SW8 switch by COMP clock going positive (to 2V) and NORMAL clock going negative (to -3V). The reconnection of the NFET bias is needed, since the CTIA shown in Fig. 6.3. is not symmetrical and has rather low gain at the output terminal OUT2 to which the gates of T_8 and T_9 load NFETs are normally connected.

(4) The generation of the off-set voltage at the C_{OFFSET} capacitor connected to the positive input CTIA is accomplished by clock pulse STORE that closes the SW4 switch. The above off-set voltage re-balances the operation of CTIA

and will assure that the bias voltages of all IR detectors will be practically the same.

(5) The generation of the CTIA off-set voltage is completed at the end of the STORE clock at which time the SW4 is opened.

(6) Closing of SW9 switch and opening of SW8 switch at the end of clock pulses NORMAL and COMP returns the CTIA to the normal internal bias connection. It should be noted that the above two clocks are made to overlap in order to prevent both switches from being opened at the same time. The operation of uniformity compensation is completed when the SW1 switch is opened by RSTREF returning to +2 V and the voltage REF is disconnected from the negative (-) input of the CTIA.

(7) The resetting of the feedback capacitance C_{fb} to zero volts is accomplished by closing the SW2 switch by RESET clock pulse. It should be noted here, that for operation with uniformity compensation illustrated in Fig. 6.7, the reset pulse (solid line) should be applied after the compensation operation is completed. However, it should also be desirable to precede this reset pulse by another reset pulse shown in Fig. 6.7 as a dotted line. The function of the first reset pulse is to preset the CTIA to the same initial condition.

6.3.4 Auto-Bias Generators

The auto-bias generator circuit shown in Fig. 6.8 provides the bias voltages for the current sources of all analog circuits. Using appropriate current mirrors, this circuit

assures that the generated bias voltages track together and that their respective current sources are effectively functions of only one reference current. This reference current of 2 μA for operation at 150K should be produced by connecting the AUTOBIAS and AMPBIAS terminals to AMPLO voltage while the ATBIAS terminal is left floating. The terminal ATBIAS was provided possible adjustment of the reference current.

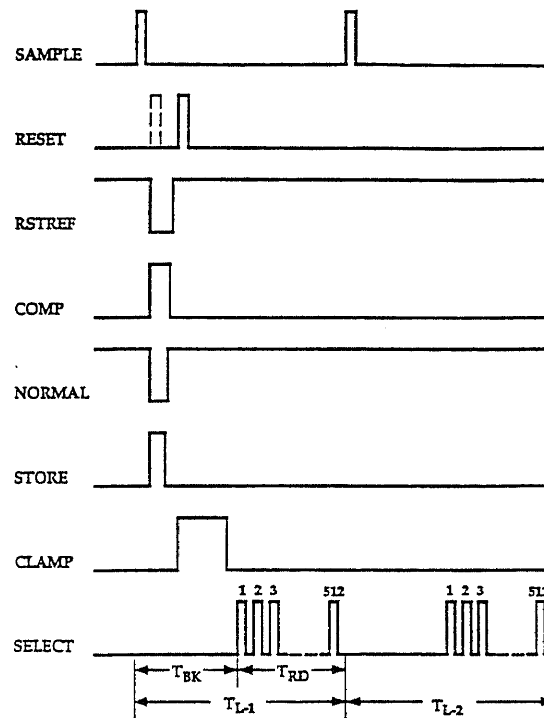

Figure 6.7 Clock waveforms for operation of multiplexer with non-uniformity correction.

Bias Voltage Generated	External Controls
REF ±10 mV	FINEBIAS ±5 V
PCASCODE	AMPBIAS = AMPLO (0V)
NCASCODE BIAS OUTBIAS	AUTOBIAS = AMPLO (0V)

Figure 6.8 Auto-bias generators.

In order to gain flexibility for controlling the PCASCODE bias voltage, an independent control of the PCASCODE bias voltage is provided by AMPBIAS and with a possibility for application of a bias current to the CASBIAS terminal.

The auto-bias circuit in Fig. 6.8 also generates the reference voltage REF which determines the bias voltage for IR detectors. During "normal" operation of the CTIA as a detector current integrator, a voltage REF applied to the positive CTIA input maintains the detector bias approximately at this fixed voltage, provided that the CTIA is in balance. Otherwise any effective imbalance between the negative and the positive

terminals (Fig. 6.1) is expected to result in a corresponding change of the actual detector bias voltage.

To obtain an externally controllable ±10 mV variation of the detector bias voltage, the auto-bias circuit on the left side of Fig. 6.8 provides a 500:1 polysilicon-resistor attenuator. For an external FINEBIAS in the range of +5V to -5V.

6.3.5 Scanning Shift Register

A bidirectional shift register for generation of the select pulses (SEL1, SEL2...) for scanning the multiplexer unit cell on the output bus is achieved by the following two external clocks:

(1) CLOCK that represents a continuous external clock providing the pixel timing for reading out the output of the multiplexer, and

(2) LINE READ pulse applied either to the ODD or EVEN pad that determines the number of clock pulses forming the internal clock for scanning the bidirectional shift register.

6.3.6 Connection and Operation of ODD and EVEN Multiplexers

Figure 6.9 shows the connections of two 512-element multiplexers for serial scanning of 1024-element linear detector array. As shown in these figures, the outputs of two registers are connected in parallel while the line read pulse, that determines the number of clock pulses applied for scanning the multiplexer pixels, is bonded to either ODD or EVEN pad. Thus MUX1, with the LINE READ applied to the ODD pad becomes the ODD multiplexer and MUX2 with the LINE READ applied to the EVEN pad becomes the

EVEN multiplexer. The ENABLE signals of MUX1 and MUX2 are 180° out of phase, so there is no signal contention at the output.

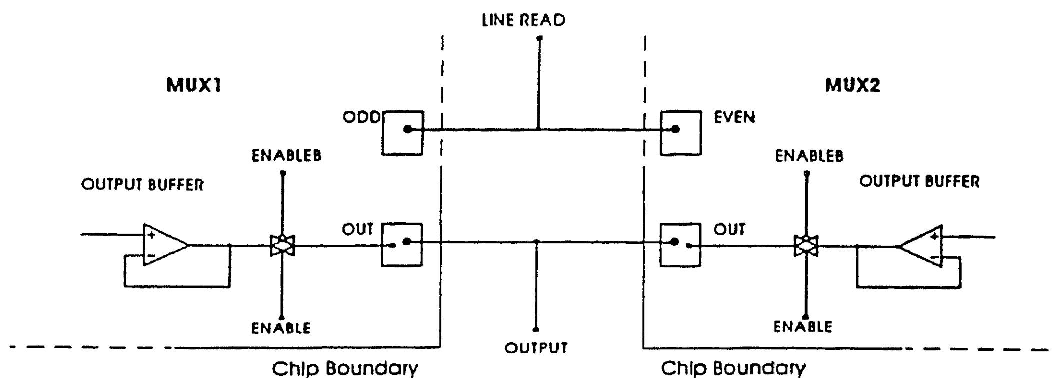

Figure 6.9 Output connection of ODD MUX and EVEN MUX.

6.4 Multiplexer Chip Layout

6.4.1 Main Features of the MUX Chip

The chip size of the multiplexer corresponds to 26.4 x 6.6 mm^2. A schematic sketch of the multiplexer chip is shown in Fig. 6.10. This figure illustrates the general approach for the layout of the MUX chip and the locations of all of the pads that need to be bonded. On the left of the MUX chip there are 512 30-µm x 90-µm pads on 50-µm centers for bonding of the InGaAs detectors.

The major area of the MUX chip is used for the pixel cells. A schematic connection of the pixel cells and their arrangement is shown in Fig. 6.10. Because of the relatively large size of the MOSFETs of the CTIA and the other opamps, the MUX pixel cells are staggered in groups of five cells. This gives a more efficient layout by allowing the pixel cells to extend 250 μm in the vertical direction (width). The horizontal dimension of these cells (length) is 1060 μm.

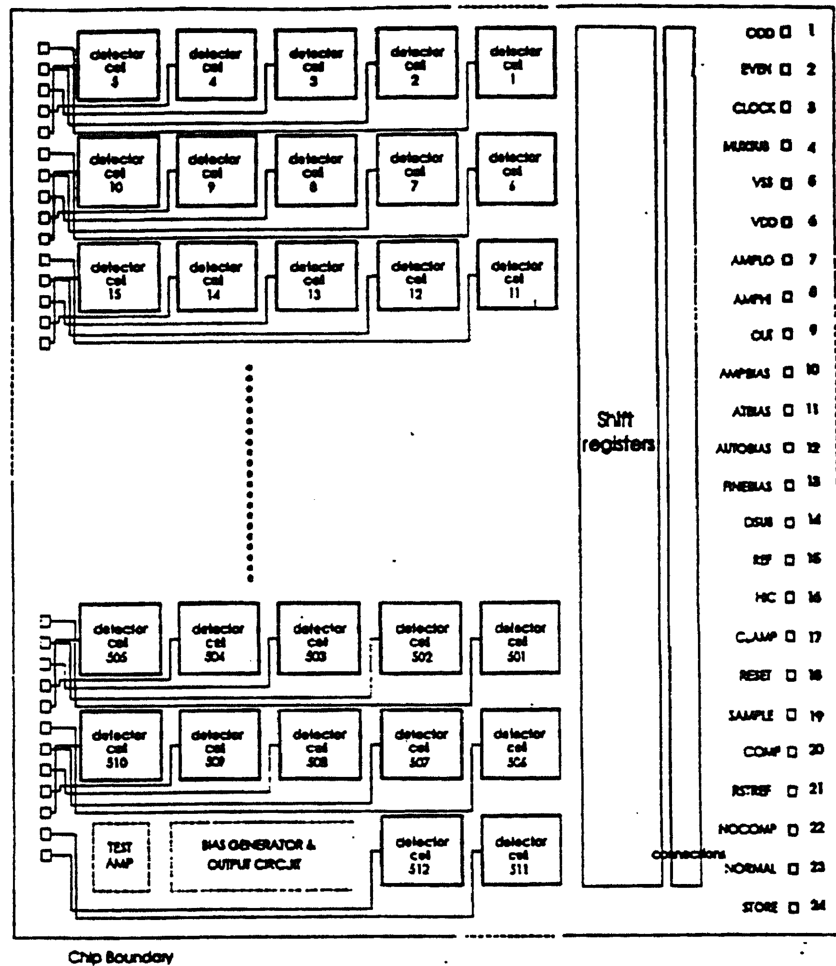

Figure 6.10 Schematic of the MUX chip layout.

At this point it might be noted that the MUX scanning shift register has been laid out on 50-μm centers. The size of the shift register stage (including the master and slave flip-flop) is 50 x 530 μm^2.

Other parts of the MUX chip include the auto-bias generators, internal clock generators, and connection buses to the detector pads shown on the left and to MUX pads shown on the right side of the chip All external control clocks have on-chip buffers.

6.5 Wafer Fabrication

6.5.1 Wafer Processing

The multiplexer was fabricated by 1.25 μm radiation hardened N-well CMOS (RICMOS III) process at the Solid State Electronics Center, Honeywell, Plymouth MN, under the general supervision of Clifford Sandstrom. This process used 15 mask layers including the implant mask for linear polysilicon-N^+ capacitors. Five monitor test devices were measured by Honeywell for each wafer. The results of several key parameters are listed below.

1. Gate threshold voltage, V_{TN}, for NMOS FET with W/L=10/1.2 μm is about +1.2V with st. dev. of 0.6 to 2.2%.
2. Gate threshold voltage, V_{TP}, for PMOS FET with W/L=10/1.2 μm is about -0.9V with st. dev. of 0.6 to 4.0%.
3. Field threshold voltages V_{FTN} and V_{FTP} for NMOS and PMOS FETs with W/L=100/2.6 μm or +20V and -20V, respectively.

4. $k_N^{'}$ ($\mu C_o/2$) for NMOS FET with W/L=100/10 μm is about 56 $\mu A/V^2$ with st. dev. of 1.2 to 2.7% for different wafers.

5. $k_P^{'}$ ($\mu C_o/2$) for PMOS FET with W/L=100/10 μm is about 18 $\mu A/V^2$ with st. dev. of 4 to 9% for different wafers.

6.5.2 Process for Linear Capacitors

The Honeywell radiation-hardened CMOS process used for fabrication of the InGaAs multiplexers did not include linear capacitors. To obtain the capability to fabricate linear capacitors with large capacitance per unit area, Honeywell RICMOS-III process was optimized with N^+ implants for fabrication of linear capacitors in the form of polysilicon gates on N^+ diffusions. A cross-section of such a capacitor is shown in Fig. 6.11. As illustrated in this figure the linear capacitor has a polysilicon gate as one electrode and a N^+ diffusion implant as the other electrode that in turn can be contacted by the source-drain N^+ diffusion. The spacing between the two electrodes is formed by the channel oxide that on the p-type substrate would be 250 Å.

Figure 6.12 shows the results of an experiment for optimization of the process for linear capacitors illustrating the trade-off between linearity ($\Delta C_{OX}/C_{OX\ avg}$) and capacitance per unit area ($C_{OX\ avg}$).* The value of ΔC_{OX} was determined as $C_{OX\ max}$ - $C_{OX\ min}$ measured from -2.0V to +2.0V between the gate and the N^+ terminal with the substrate floating and dividing by a factor of 2, i.e. $\Delta C_{OX}=\ (C_{OX\ max} - C_{OX\ min})/2$. Nine

wafers were used for the experiment summarized in Fig. 6.12. Three groups of three wafers each were exposed to phosphorous implants 5E14, 1E14, and 2E15, all at 60 kV. These wafers were then subjected to three types of 550°C and 850°C anneals before proceeding with the standard process steps.

To maximize linearity, the linear capacitors were fabricated with C_{OX} of nominally 0.8 pF/μm^2 that according to the data in Fig. 6.12 corresponds to non-linearity of less than 0.08% for +2.0V or -2.0V range. In this case a phosphorous implant of 1E15 at 60 KeV was followed by N_2 anneals of 1.0 hr at 550°C and 20 min at 850°C before proceeding with the standard process.

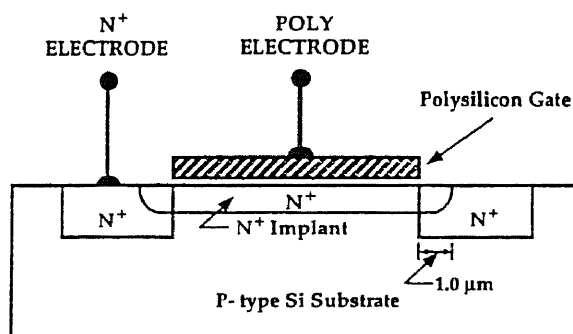

Figure 6.11 Cross-sectional view of linear capacitor.

* This study was done by Jeff Sather, Gordon Show, and Terry Fabian of Honeywell Solid State Electronics Center, Plymouth, MN.

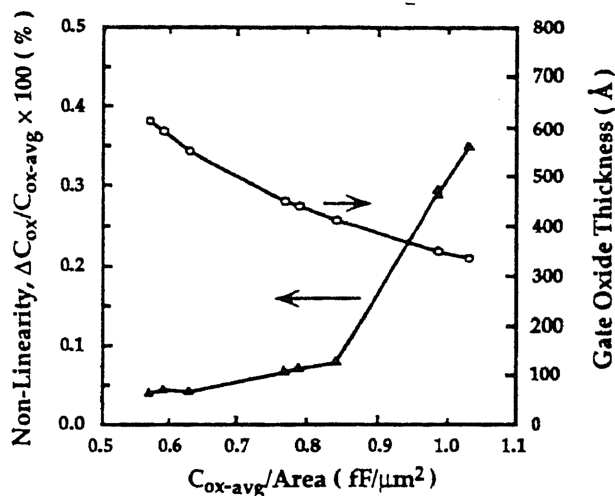

Figure 6.12 Tradeoff of non-linearity Vs capacitance for polysilicon-on N^+ capacitors.

6.6 Testing and Performance of the Multiplexers

6.6.1 Pretesting of the MUX

As shown in Fig. 6.1, the multiplexer chip is provided with two inputs for pretesting the operation of the multiplexers on the wafer or in a package without IR detectors. One way to accomplish this is to apply a pulse QTEST to the 60 fF test capacitors. This pulse will injects essentially the same test charge to all CTIA integrators in parallel and could be used to determine the charge-to-voltage transfer characteristics of the multiplexer.

Another way to test multiplexer operation is to study the response of the MUX to the same signal applied to all CTIA inputs. This can be accomplished by applying a voltage VTEST to the drain and a voltage TESTB to the gate of a minimum size PFET

connected to the input of the CTIA integrator. This test can be used to measure the uniformity and off-set threshold of the MUX pixel cells.

6.6.2 Waveforms of Clock Pulses for Operation of the MUX

Figures 6.13, and 6.14 illustrate a proposed set of external clock waveforms used for operation of the MUX with 31.75 ms line time, T_L, 28.59 ms read time, T_{read}, and 3.16 ms blank time, T_{blank}. For this operation the external clock pulse, CLOCK, has a period of 55.5 μs, a duty cycle of 50%, and a frequency of 18.02 kHz. The external clock waveforms for two modes of operation of the MUX are illustrated in Figs. 6.13 and 6.14.

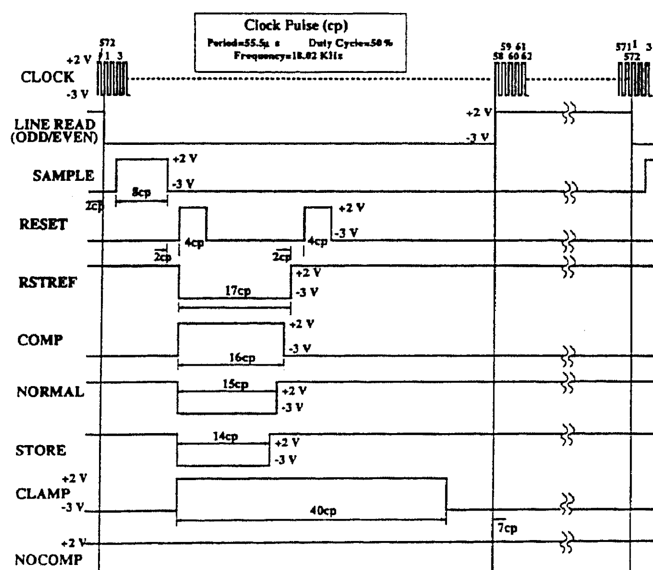

Figure 6.13 Clock waveforms for operation with periodic non-uniformity correcion.

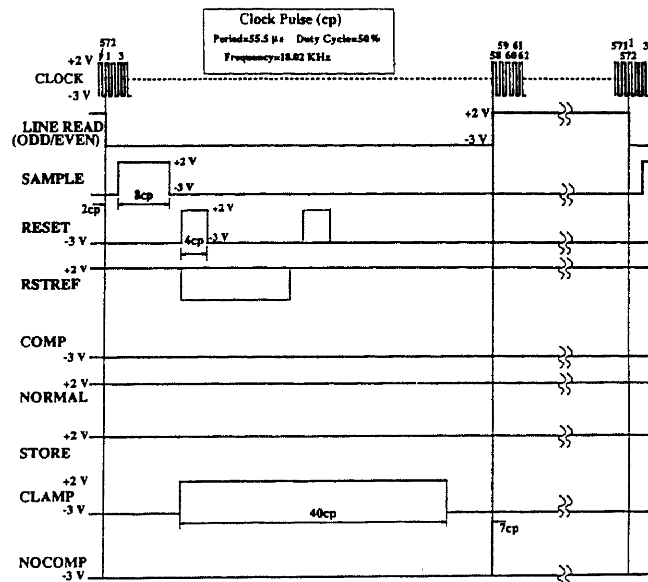

Figure 6.14 Clock waveforms for operation without non-uniformity correcion.

6.6.2.1 Operation with Compensation for Non-uniformity: Figure 6.13 illustrates the external clock waveforms for operation with non-uniformity compensation. It should be noted that the optical integration time, t_{int}, is initiated at the end of the CLAMP pulse and is terminated at the end of the SAMPLE pulse.

The waveform of the RESET clock is in the form of two pulses. The first pulse resets the feedback capacitor, C_{fb}, to zero volts before the compensation cycle is started. The second RESET pulse resets C_{fb} again to make sure that no charge signal is present on C_{fb} at the beginning of the new optical integration time.

6.6.2.2 Operation without Compensation for Non-uniformity: Figure 6.14 illustrates the clock waveforms for operation of the MUX without non-uniformity compensation. Comparison of Figs. 6.13 and 6.14 shows that for this mode of operation external clocks RSTREF, COMP, NORMAL, and STORE assume constant voltages corresponding to their values during the optical integration time in the case of Fig. 6.13. However, the NOCOMP voltage that connects the positive CTIA input to REF keeps the SW5 switch opened in the case of operation shown in Fig. 6.13 while it keeps the SW5 switch closed for the case in Fig. 6.14.

At this point it should be added that (as explained in Section 6.6.3) a RSTREF pulse is needed for QTEST input. Furthermore, there is also a possibility that RSTREF together with the second RESET pulse (shown in Fig. 6.13) may also improve the operation for the NOCOMP mode. Therefore, the second version of the clock waveform for the NOCOMP mode include the dotted waveforms for RESET and RSTREF clock pulses.

6.6.2.3 Operation with Stored Non-uniformity Compensation: The kTC noise associated with the non-uniformity-correction-offset voltage results in a fixed pattern noise (FPN) due to variation of the detector bias voltage that changes with each uniformity correction. This noise component may be appreciable for detectors with relatively low shunt resistance of less than 10^{12} ohms. However, due to a very low leakage current of the C_{OFFSET} node for operation at 150K and 200K, the uniformity correction may be performed only once and stored for hours or even days. This mode of

operation is referred to as stored uniformity compensation (STORECOMP). In this case a single uniformity correction clock sequence such as shown in Fig. 6.13, is followed by operation without uniformity compensation (NOCOMP) with clock waveforms such as shown in Fig. 6.14 except that the NOCOMP voltage is maintained at +2V to keep the switch SW5 (see Fig. 1) open. Finally, the compensation-induced FPN can be removed now by periodic external two-point uniformity corrections (for offset and gain) that would be repeated after each uniformity correction.

6.6.3 Operation of the MUX

The operation of the fabricated multiplexers was demonstrated using a specially constructed MUX/FPA tester with digital power supplies V_{DD} = +2V, V_{SS} = -3V, GND = 0V and analog power supplies AMPH1 = +2V, AMPLO = -3V, and GND = 0V (direct or buffered).

To minimize readout noise, the tester was made with opto-isolated links between the clock logic board and the clock drivers and between the output of 16-bit A/D converter and the PC for data acquisition.

The tester has been operated with 26 ms line times consisting of 583 clock pulses. This included 512 clock pulses for the selection of 512 detectors, 14 overscan clock pulses, and 57 clock pulses for timing of the control pulses during the blanking time. The tester provides three modes of operation. They include:

(1) NORMAL or NOCOMP mode for operation without non-uniformity compensation,

(2) COMP mode for operation with non-uniformity compensation, and

(3) STORECOMP mode of operation with stored compensation for non-uniformity.

The operation of the multiplexer was verified by QTEST input, a global charge input via 60 fF capacitors at each CTIA input, for feedback capacitance, C_{fb}, of either 0.8 or 2.4 pF. The clock waveforms used for the QTEST for NOCOMP and COMP mode of operation is shown in Fig. 6.15. It should be noted that, as shown in this figure, the negative step of the QTEST input occurs during the time when the CTIA input is connected to the REF (a low impedance voltage reference) by the RSTREF pulse. Thus, only the positive step of the QTEST pulse injects a charge signal to the CTIA integrator.

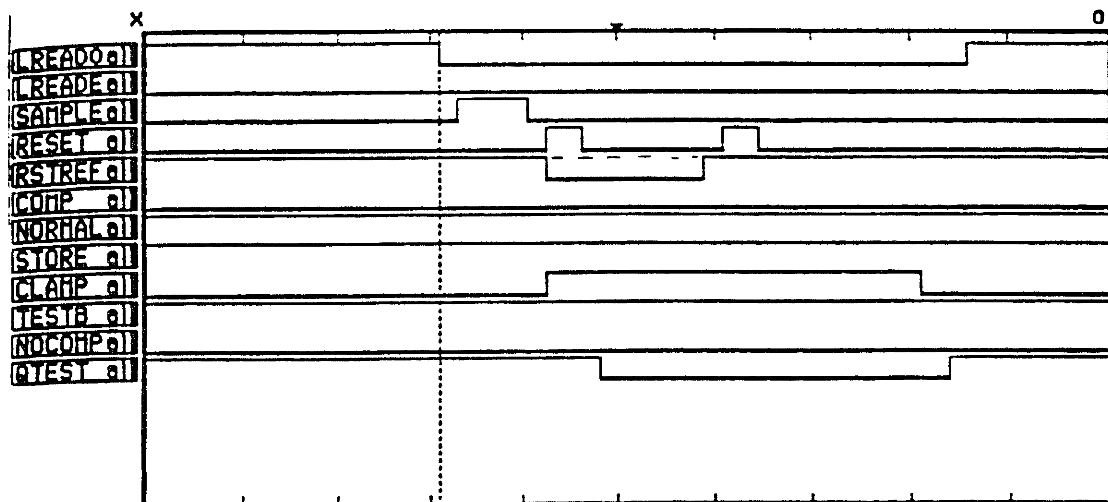

Figure 6.15 Clock waveforms for MUX normal (NOCOMP) mode with QTEST.

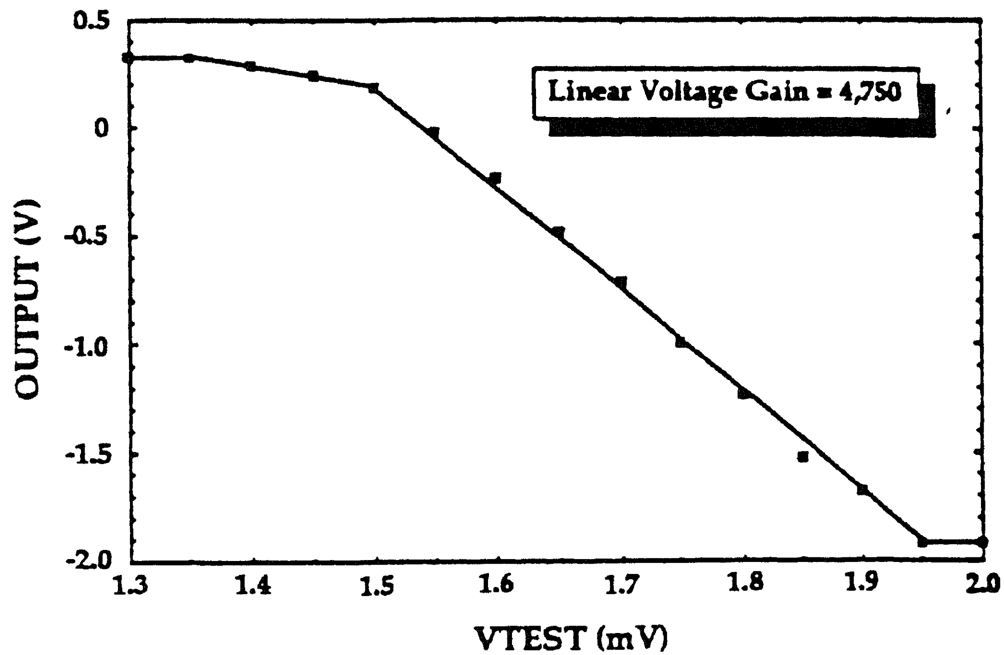

Figure 6.16 Multiplexer transfer characteristics.

6.6.4 Multiplexer Performance Tests

Open-loop voltage gain

Open-loop voltage gain was measured with VTEST voltage input relative to the DSUB reference voltage for voltage REF=0V. The measured multiplexer transfer characteristics curve, shown in Fig. 6.16, indicates the value of open-loop gain of 4,750.

Linearity

A linear charge integration was demonstrated by (a) QTEST for feedback capacitance, C_{fb}, of 0.8 and 2.4 pF, and (b) readout of dark current from InGaAs detectors with λ_c=1.7 um, bonded to the multiplexer. Increase of the feedback capacitance during QTEST from 0.8 to 2.4 pF, resulted in the increase of the MUX output signal by a factor of 3.

A further test of linearity was demonstrated by room-temperature operation of the multiplexer bonded to InGaAs detectors with λ_c=1.7 um. The results of this test for one pixel output are shown in Fig. 6.17.

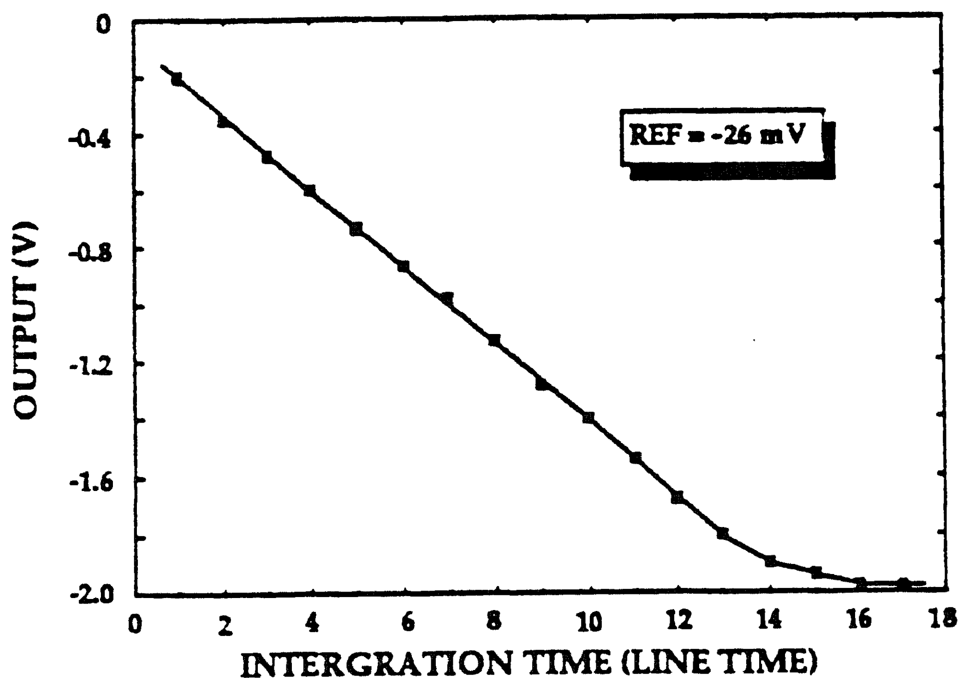

Figure 6.17 MUX output linearity with integration of dark current in NOCOMP mode.

Power supply rejection

Initial tests of power supply rejection indicates a power supply rejection ratio (PSRR) at low frequency of 100:1 and less than 10:1 at the clock frequency of 18 KHz.

Readout noise

A temporal readout noise of 100 μV rms corresponding to 500 rms electrons/pixel was measured for NOCOMP mode with zero input voltage and C_{fb}=0.8 pF.

6.6.5 Input Threshold Non-uniformity

VTEST input was used to measure the uniformity of the CTIA input threshold non-uniformity for operation in the NOCOMP mode. Typically, for REF=1.0 a VTEST input of +2.0 mV drives all MUX outputs into saturation of about -2.0 V and a VTEST input of -2.0 V drives all MUX outputs into a minimum output signal of about +0.5 V. Therefore, the CTIA input threshold non-uniformity is < 4.0 mV peak-to-peak or < 0.8 mV rms.

The above DC test, however, could not be used for testing the resulting input threshold non-uniformity for the COMP mode. Because in this case the applied VTEST input is automatically compensated for by the process of uniformity correction. The input threshold uniformity after uniformity correction was checked by connecting the VTEST input to DSUB and observing the resulting output voltage. The results of this test are shown in Fig. 6.18. Inspection of this figure shows that the resulting output voltage variation, ΔVout, is less than 10 mV including the fixed pattern noise (FPN). Since for a low impedance input source, this is essentially an open-loop test. Therefore, taking into

account the open-loop gain of 4750 and the fact that the detected output voltage, Vout, has a net gain of 0.5, the effective variation of the input voltage is estimated as $\Delta Vin <$ $4.0\mu V$ peak-to-peak (p-p).

6.6.6 Fixed Pattern Noise

The measured results shows that for operation with or without uniformity compensation, the InGaAs multiplexer exhibits a periodic fixed pattern noise (FPN) that repeats every five pixels.

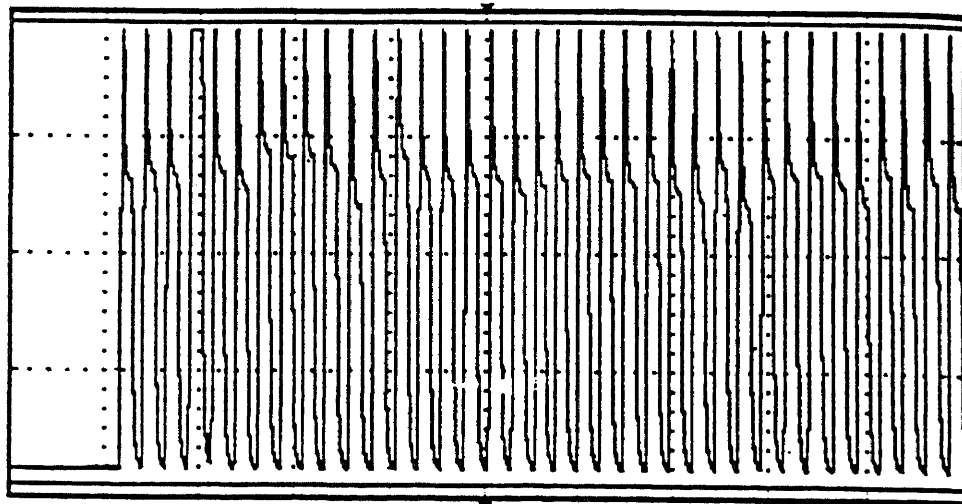

Figure 6.18 ODD MUX output waveforms for COMP mode with VTEST=DSUB for Cfb=0.8 pF (scale: 20 mV/div).

The observed FPN apparently results from the fact that the multiplexer cells are staggered in groups of five pixel cells (see Fig. 6.10). This allowed more efficient layout with the pixel cells extending 250 μm in vertical direction (width) and having a horizontal dimension (length) of 1050 μm.

The observed FPN is illustrated in Figs. 6.19 and 6.20. Figure 6.19 shows the output waveforms for operation of the multiplexer with QTEST input for ODD and EVEN MUX scan directions and CTIA feedback capacitance of 0.8 pF. For QTEST input, a +3.0 V step is applied in parallel to all multiplex inputs via 60 fF on-chip capacitors. This results in an injection of about 1.125×10^6 electrons to each integrating CTIA cell. It should be noted that the waveforms in Fig. 6.19 are truncated (offset) and detected with an output gain of 0.5. Therefore, the scale of 15 mV/div in Fig. 6.19 and 6.20 corresponds to about 150,000 electrons/div at the integrating feedback capacitance of 0.8 pF.

Furthermore, it should be noted that the mid-point in Figs. 6.19 and 20 corresponds to the location in the multiplexer chip at which two halves of MUX masks were stitched by photocomposition. Inspection of Figs. 6.19 and 20 shows that FPN is larger for the first half of the pixels by a constant value of about 7.5 mV corresponding to 75,000 electrons. The constant increase in the fixed pattern noise is attributed to the fact that the digital scanning shifter in the upper half of the multiplexer was moved by 10 μm from the original position (that was maintained in the lower half) to allow for photocomposition overlap tolerance.

Inspection of the waveforms in Figs. 6.19 and 20(a) shows that the FPN is largest at pixel cells next to the scanning register and decrease more or less monotonically to the pixel cells on the left side of the MUX chip next to the MUX input pads. The difference between the maximum and the minimum FPN is estimated to be about 22,500 electrons in Fig. 6.19 for QTEST input and about 17,500 electrons in Fig. 6.20(a) for zero input. This FPN component will be referred to as the variable FPN.

Comparison of waveforms in Fig. 6.20(a) and Fig. 6.20(b) shows that the change in the CTIA feedback capacitance, C_{fb}, from 0.8 pF to 2.4 pF results in a reduction by about a factor of three of the variable FPN (i.e., between the first and fifth pixel). However, constant component of FPN present at the first half of pixels appears to be the same for C_{fb}=0.8 pF and for C_{fb}=2.4 pF.

In summary, the following conclusions can be made on observed FPN:

On the basis of the presented data, it may be concluded that the variable FPN is due to charge injection at the unshielded parasitic capacitances of the CTIA input nodes. The values of the unshielded CTIA input parasitic capacitances are estimated to be 760, 575, 390, 205 and 20 fF for the 1st, 2nd, 3rd, 4th and 5th pixel from the scanning shift register, respectively.

Since the constant value of FPN (present at the upper half of the MUX chip) is about the same for C_{fb}=0.8 and 2.4 pF, it may be concluded that this component of the FPN represents a voltage pick-up at the sample-and-hold capacitance ($C_{S\text{-}H}$) or/and directly at the output bus.

The comparison of the variable FPN for QTEST input (see Fig. 6.19) and zero input (see Fig. 6.20(a)) indicates that the variable FPN may be dependent on the signal level. However, if this dependence is linear, this FPN can be corrected by the two-point (off-set and gain) correction that is also needed for the InGaAs detectors. But only one-point (offset) correction may be needed to correct for the constant level FPN.

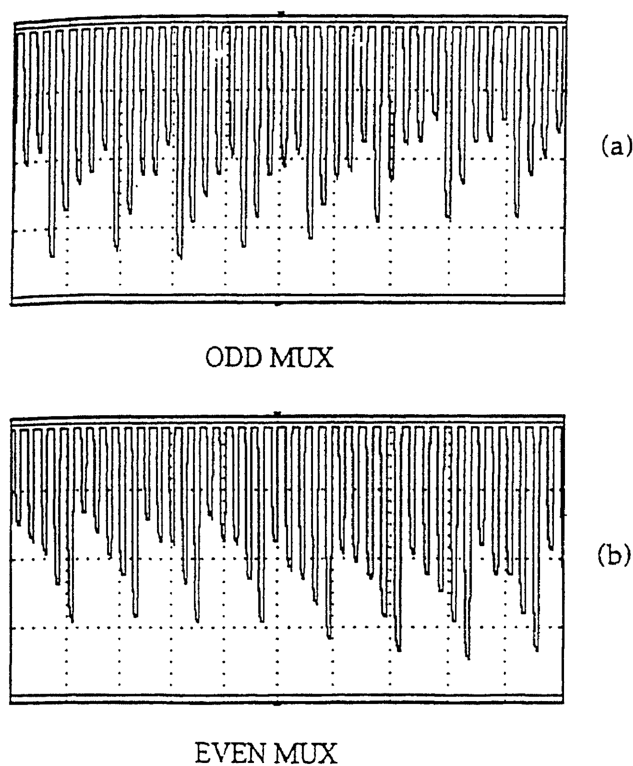

Figure 6.19 MUX output waveforms for QTEST=+3V step input for ODD MUX in (a) and EVEN MUX in (b) (scale: 15 mV/div).

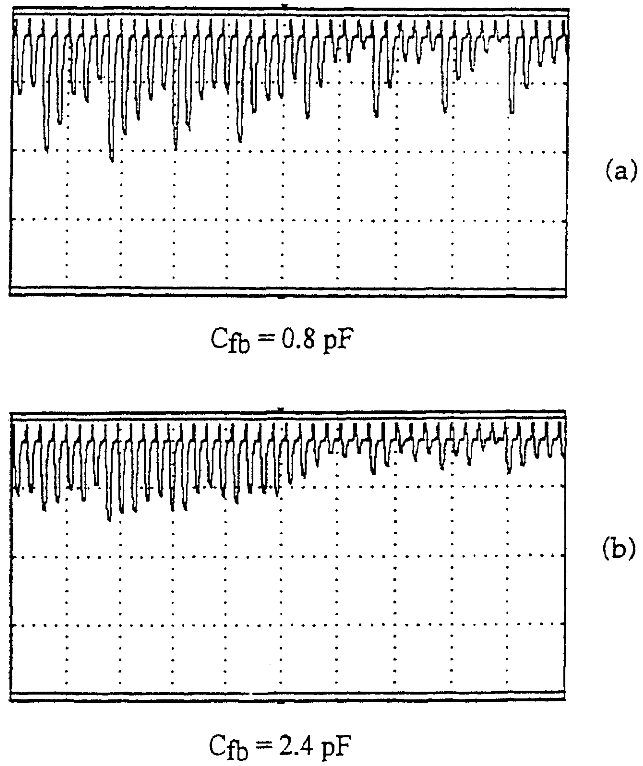

Figure 6.20 MUX output waveforms for ODD MUX with QTEST=0 V for C_{fb}=0.8 pF in (a) and C_{fb}=0.8 pF in (b) (scale: 15 mV/div).

CHAPTER 7

FOCAL PLANE ARRAY TEST RESULTS

7.1 Focal Plane Array Results

7.1.1 $In_{0.53}Ga_{0.47}As$ Focal Plane Array Results

The measured dark current of 1024 elements of the 1.7 um cut-off wavelength InGaAs focal plane array is shown in Figure 7.1. The feed-back capacitance used was 0.8 pF. The dark current was measured at 200 K temperature and with variable integration times until the pixels are saturated in multiples of line times (33 ms). As seen from figure 7.1, the measured dark current is very uniform across the length of 1024 element array. The mean value of dark current is < 1 fA at 10 mV reverse bias. The number of bad pixels was < 1%. The number of bad pixels include three bad multiplexer unit cells.

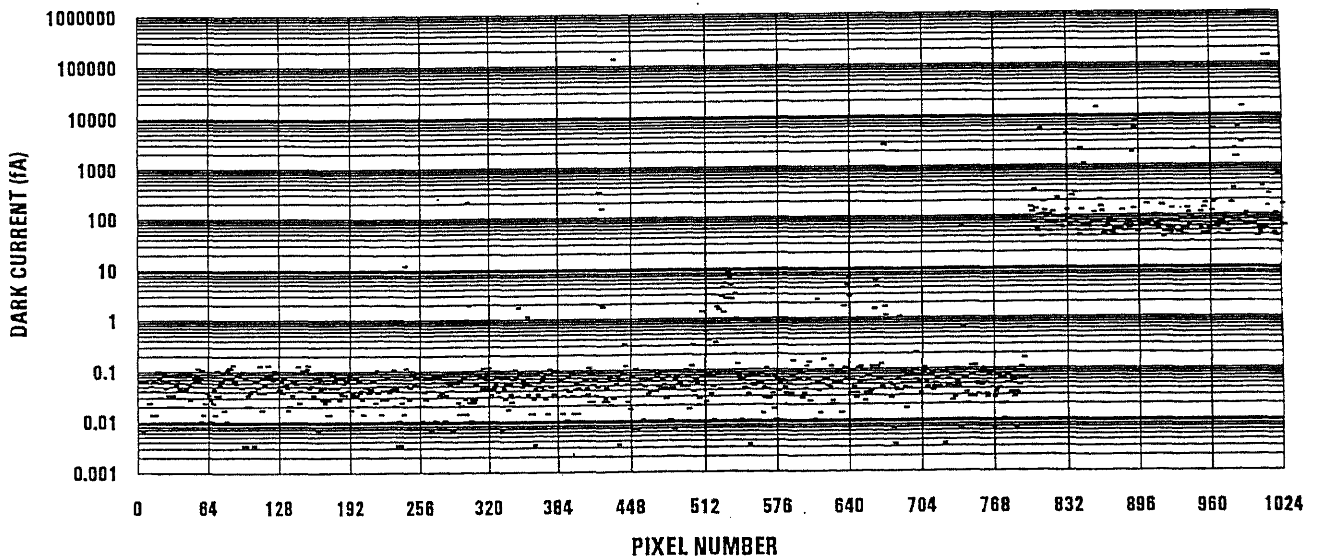

Figure 7.1 Dark current vs. pixel number of 1.7 um InGaAs focal plane array.

Figure 7.2 shows the flat-filed optical response of the focal plane array measured using a black-body at a temperature of 200 K. The black body temperature was kept at 1000° K. A narrow band pass spectral filter, with a center wavelength of 1496 nm was used in front of the blackbody. As seen from figure 7.2, the detector response is very uniform from pixel to pixel. The measured quantum efficiency was 95% with a narrow slit (70 um) in front of the detector array. With out the narrow slit, the quantum efficiency measured was greater than the 100% indicating the long diffusion length and the contribution of diffusion length to the absorption of photons in the non-diffused area of the pixel. To reduce the effect of long diffusion length on the uneven splitting of photons from the odd and even pixels, a Si lens was designed to focus the beam on to the detector. Also shown in Fig. 7.2, is the pixel to pixel variation of the quantum efficiency. The measured quantum efficiency non-uniformity from pixel to pixel is < 5%.

The measured noise of the focal plane array was shown in Figure 7.3. As seen from figure 7.3, the measured noise was bout 800 rms. e^-. The measured noise is the total amount of noise which includes the noise of the multiplexer, shot noise and Johnson noise of the detector. As mentioned in Chapter 6, the measured noise of the multiplexer alone was about 400 rms. e^-.

The measured linearity of the focal plane array was shown in Figure 7.4. As seen from Fig. 7.4, the linearity of the array is less than 0.1%. The measured linearity is better than the best results reported to date and is achieved due to the linear capacitor development and the selection of proper implant dosage in the bulk Si substrate.

The memory effect or the un collected charge during the integration time is measured using the optical signal only during the current read out cycle of the integration time. At the end of the integration time, the optical signal was removed and the charge from the next integration time was measured. The measured memory effect result as a function of pixel number is shown in Fig. 7.5. As seen from Fig. 7.5, the measured value is less than 0.7% indicating that some of the charge is still either in the integrating capacitor or being collected by the integrating capacitor after read-out cycle of the present integration time. This additional charge carriers are due to the diffusion of carriers from the non-diffused area and is due to the long diffusion length of the carriers. The diffusion process is the slowest process of collection of charge carriers and is not dependent on the electric field. This process could be improved by increasing the doping in the non-diffused area of the absorption layer there by increasing the recombination rate.

The maximum integrated charge or the well capacity was measured using very long integration times by integrating the dark current until the integrating capacitor was completely filled. The measured charge capacity as a function of pixel number in a 1.7 um cut-off wavelength InGaAs Focal Plane Array is shown in Fig. 7.6. As seen from the measured results, the maximum charge handling capacity is with in the design value of the integrating capacitor and is very uniform from pixel to pixel.

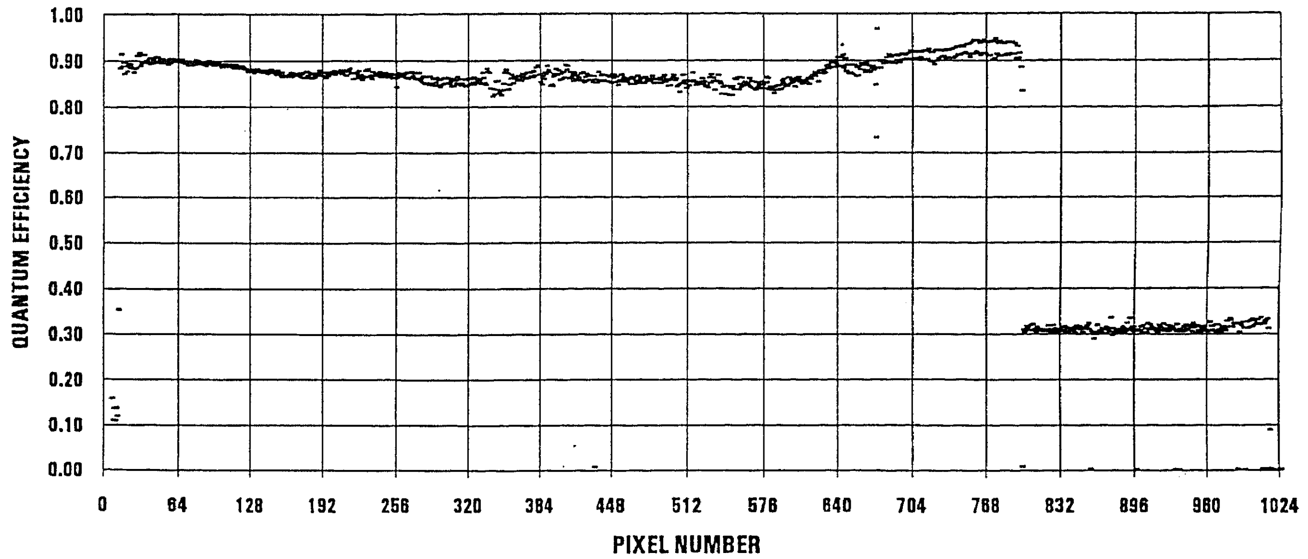

Figure 7.2 Flat-field optical response of 1.7 um InGaAs focal plane array.

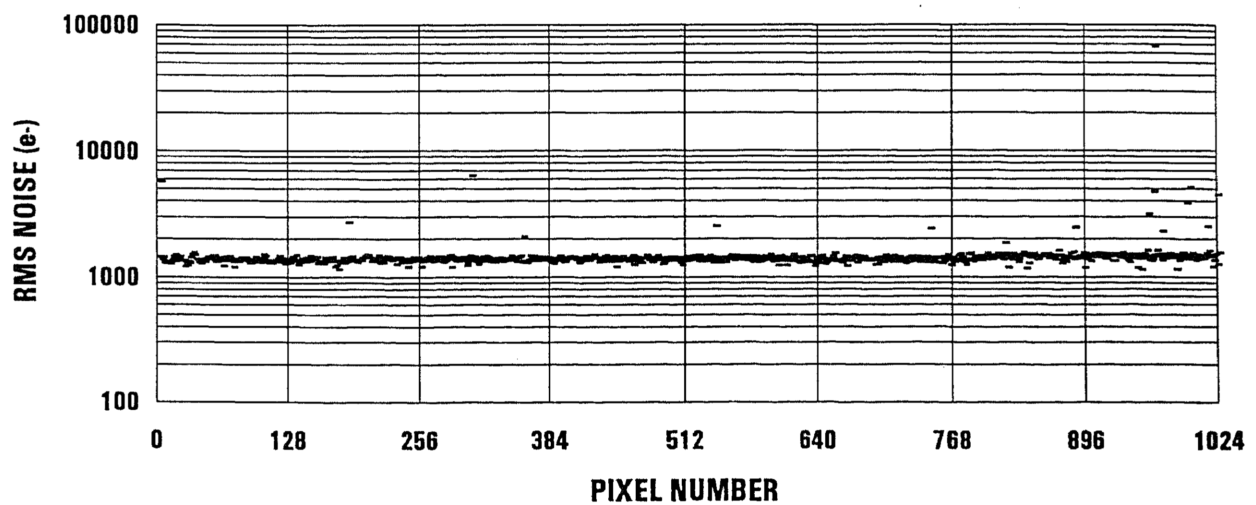

Figure 7.3 Measured noise results of 1.7 um InGaAs focal plane array.

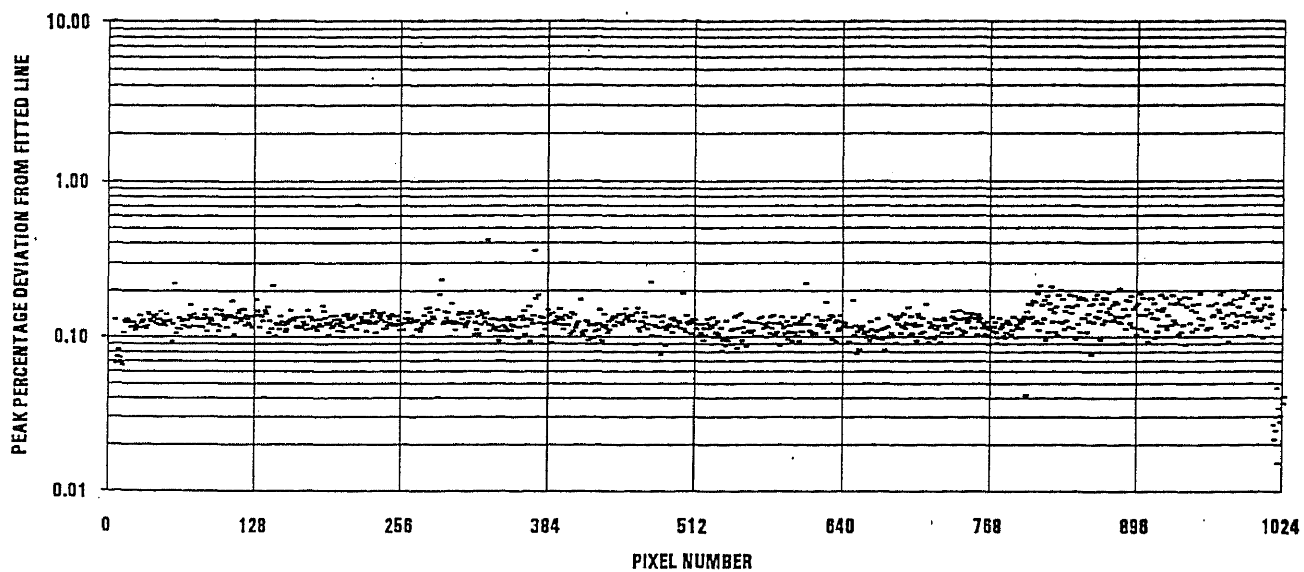

Figure 7.4 Measured linearity results of 1.7 um InGaAs focal plane array.

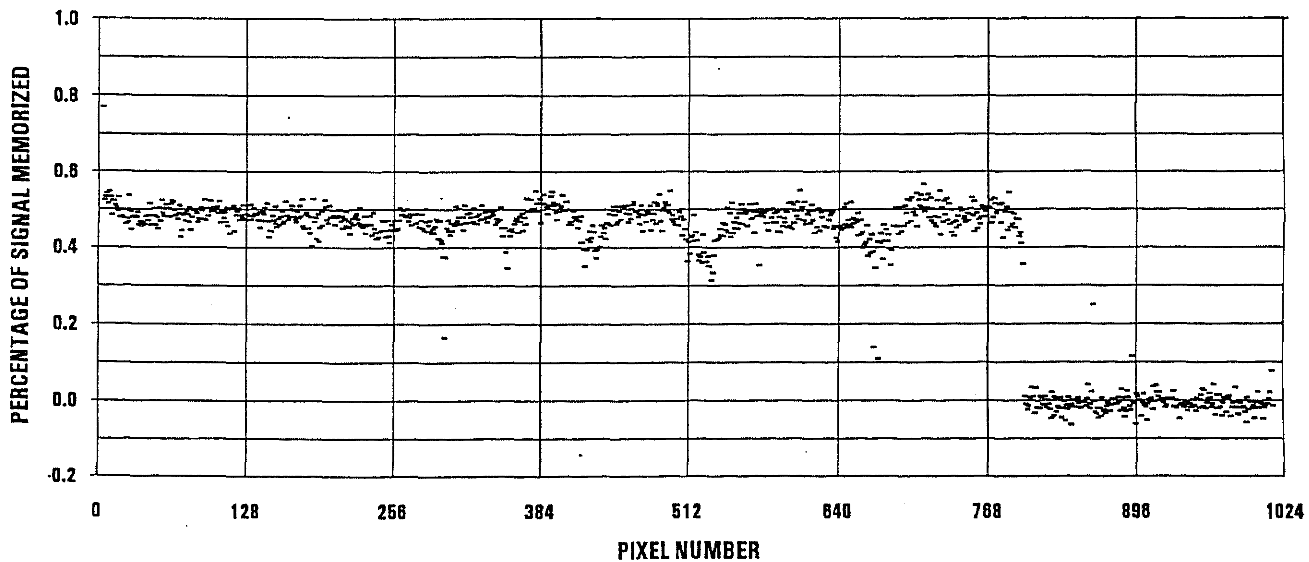

Figure 7.5 Measured memory effect results of 1.7 um InGaAs focal plane array.

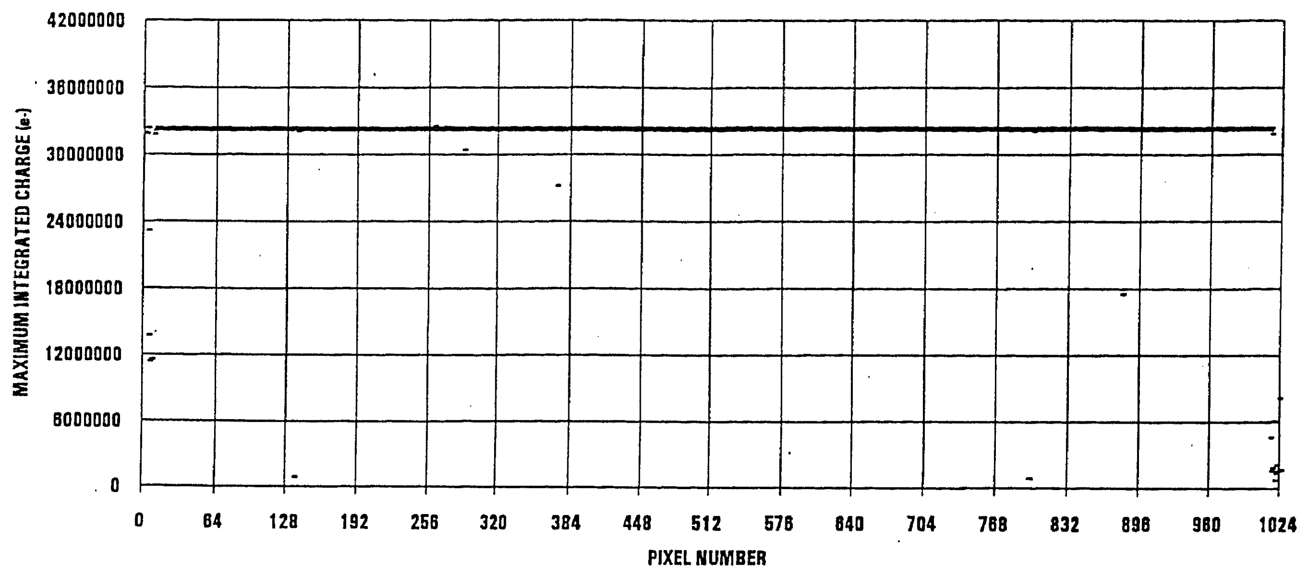

Figure 7.6 Measured maximum charge results of 1.7 um InGaAs focal plane array.

7.1.2 $In_{0.72}Ga_{0.28}As$ Focal Plane Array Results

The 2.2 um focal plane array consists of two detector slivers butted together to achieve the required 1024 element array. One single pixel was sacrificed at the splice between the two adjacent slivers. The dark current of 1024 elements of the 2.2 um cut-off wavelength InGaAs focal plane array is shown in Figure 7.7. The feed-back capacitance used was 0.8 pF. The measured dark current was at 150 K and measured at variable integration times until the pixel saturates in multiples of line times (33 ms). As seen from figure 7.7, the measured dark current is non-uniform from element 700 to 1024. This non-uniformity at the end pixels is probably due to the two different slivers from two different areas on the wafer where there may be different energy traps which have different energy levels. The mean value of dark current is about 25 fA at 10 mV reverse bias. The focal plane array dark current was measured with uniformity compensation and without the uniformity

compensation. The difference in dark current uniformity from compensation and non-compensation is shown in Figure 7.7. As seen from figure 7.7, the dark current uniformity is better with the non-uniformity compensation circuit.

As explained in the dark current analysis section, the difficult and important parameter that effect the dark current and the temperature behavior of dark current in a lattice mis-matched semiconductors are the dislocations and the deep levels that are created in the band gap. As seen from Fig. 7.7, the deep levels appear to be random in nature and have different energy levels in the band-gap. These traps freeze out at different temperatures supporting the random nature of these deep levels in side the band gap. Further study is required to understand the nature and behavior of these deep levels. One possible way to understand the energy levels of the deep levels is by using the deep level transient spectroscopy (DLTS) measurements.

Figure 7.8 shows the flat-filed optical response of the focal plane array measured using a black-body at a temperature of 150 K. The black body temperature was kept at 1000 K and the light source was through a narrow band pass spectral filter, with a center wavelength of 1984 nm. As seen from figure 7.8, the detector response is very uniform from pixel to pixel. The measured quantum efficiency non-uniformity from pixel to pixel is $< 5\%$. The absolute value of the quantum efficiency is measured using the 500 X 25 um area for each pixel. This area also includes the 500 um X 12 um non-diffused area (optically dead space). As explained in the dark current analysis section, the carrier life times are increasingly smaller and smaller as the mis-match between the InGaAs absorption layer and the InP substrate increases. This could be due to the increase in the

defect density which will increase the recombination rate. The measured external quantum efficiency values also shows that the diffusion length in the mis-matched InGaAs/InP photodetectors is much smaller than the lattice matched InGaAs/InP photodetectors. This decrease in the diffusion length may be due to the decrease in the band-gap (from 0.75 eV to 0.56 eV) and the increase in the defect density.

From the measured values of quantum efficiency, the threading dislocation density was calculated using the expression[65][66]

$$\frac{\eta}{\eta_o} = \left(1 + \Pi^2 L_n^{\,2} \rho_d\right)^{-1} \tag{7.1}$$

Where, ρ_d = Threading dislocation density

η_o = Peak quantum efficiency in the absence of dislocations

η = Peak quantum efficiency in the presence of dislocations

L_n = Electron diffusion length

By allowing the η_o to be same as the lattice matched detector (> 85%), η to be the measured peak value of the diffused devices, and L_n to be the values deduced from the fitting parameters described in Chapter 4, the dislocation density is calculated as 2.4 X $10^5\,/\mathrm{cm}^2$.

The measured noise of the focal plane array was shown in Figure 7.9. As seen from figure 7.9, the measured noise was bout 700 rms. e^-. The measured noise is the total amount of noise which includes the noise of the multiplexer, shot noise and Johnson noise of the detector. As mentioned in Chapter 6, the measured noise of the multiplexer alone was about 400 rms. e^-.

The measured linearity of the focal plane array was shown in Figure 7.10. As seen from Fig. 7.10, the linearity of the array is less than 0.1%. The measured linearity is better than the best results reported to date and is achieved due to the linear capacitor development and the selection of proper implant dosage in the bulk Si substrate.

The memory effect or the un collected charge during the integration time is measured using the optical signal only during the current read out cycle of the integration time. At the end of the integration time, the optical signal was removed and the charge from the next integration time was measured. The measured memory effect result as a function of pixel number is shown in Fig. 7.11. As seen from Fig. 7.11, the measured value is less than 0.1% indicating that all of the charge is collected in the integrating capacitor after read-out cycle of the present integration time. This lower value of charge carriers also indicates the reduction of diffusion length and hence minimum diffusion process of collection of carriers. As mentioned in the above section, the diffusion process is the slowest process of collection of charge carriers and is not dependent on the electric field.

The maximum integrated charge or the well capacity was measured using very long integration times by integrating the dark current until the integrating capacitor was completely filled. The measured charge capacity as a function of pixel number in a 2.2 um cut-off wavelength InGaAs Focal Plane Array is shown in Fig. 7.12. As seen from the measured results, the maximum charge handling capacity is with in the design value of the integrating capacitor and is very uniform from pixel to pixel.

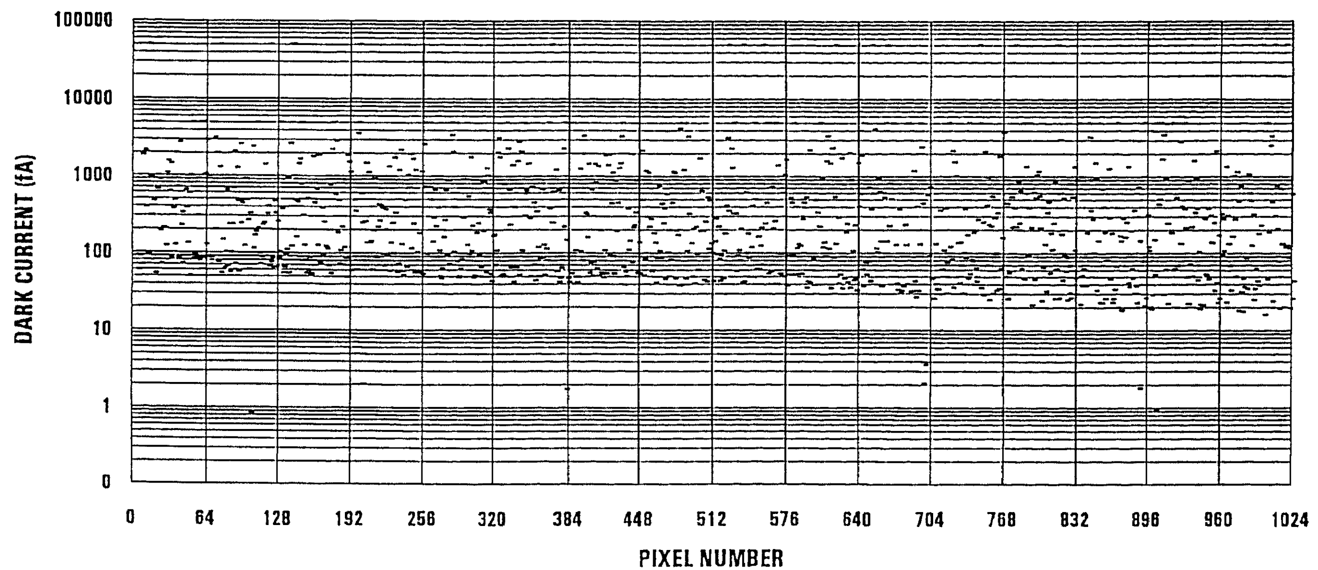

Figure 7.7 Dark current vs. pixel number of 2.2 um InGaAs focal plane array.

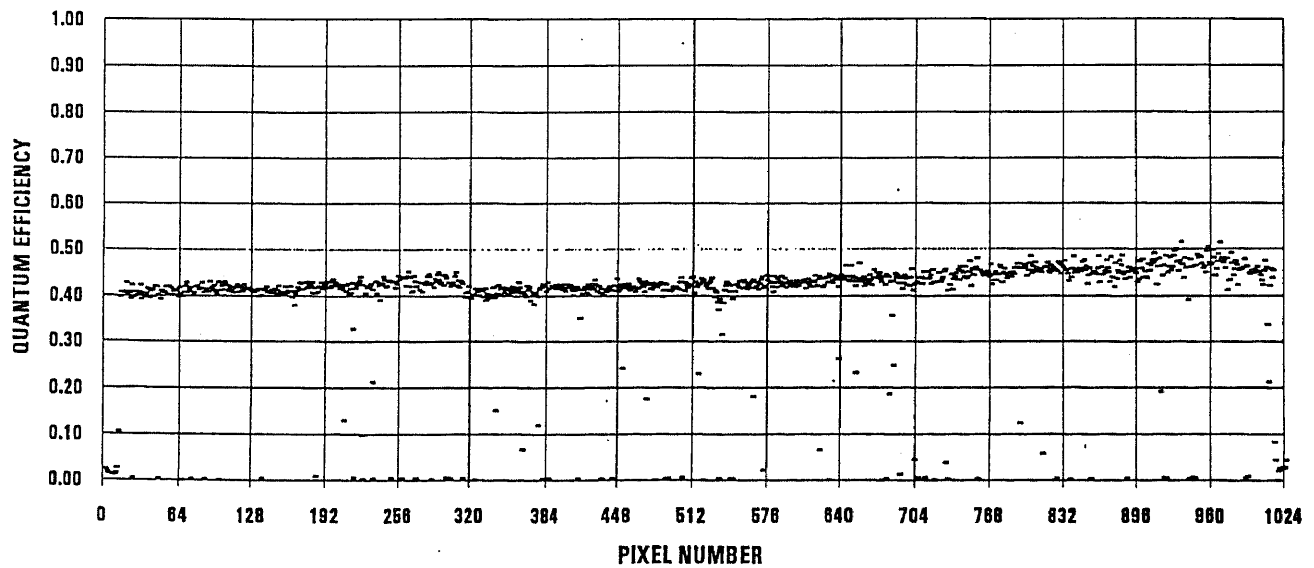

Figure 7.8 Flat-field optical response of 2.2 um InGaAs focal plane array.

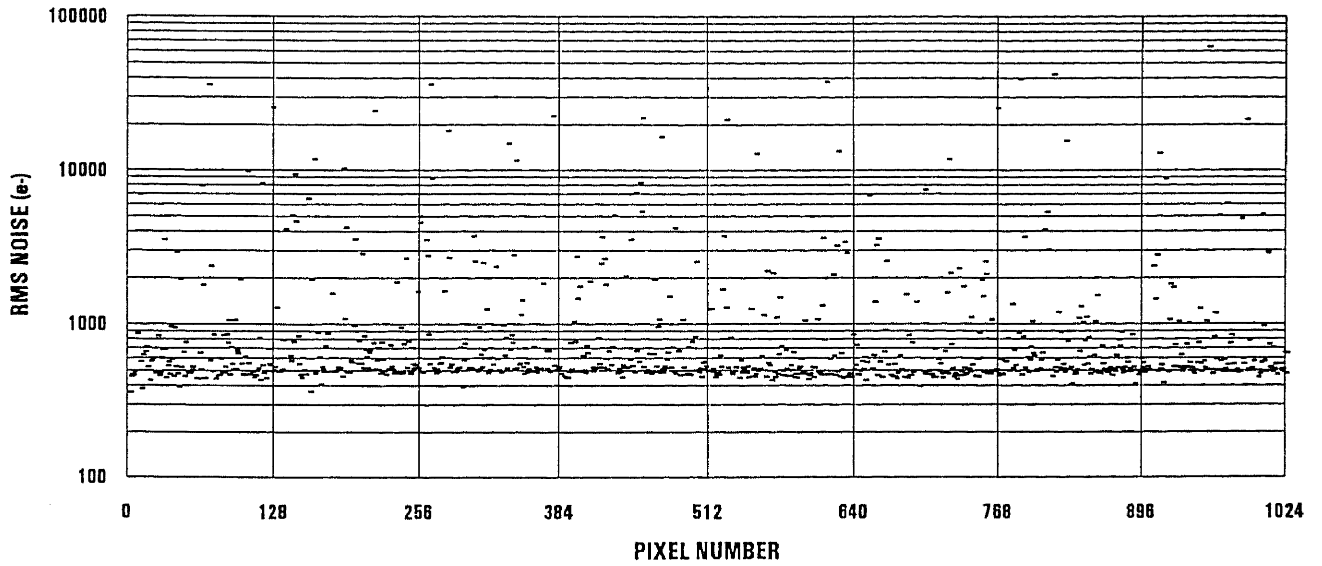

Figure 7.9 Measured noise results of 2.2 um InGaAs focal plane array.

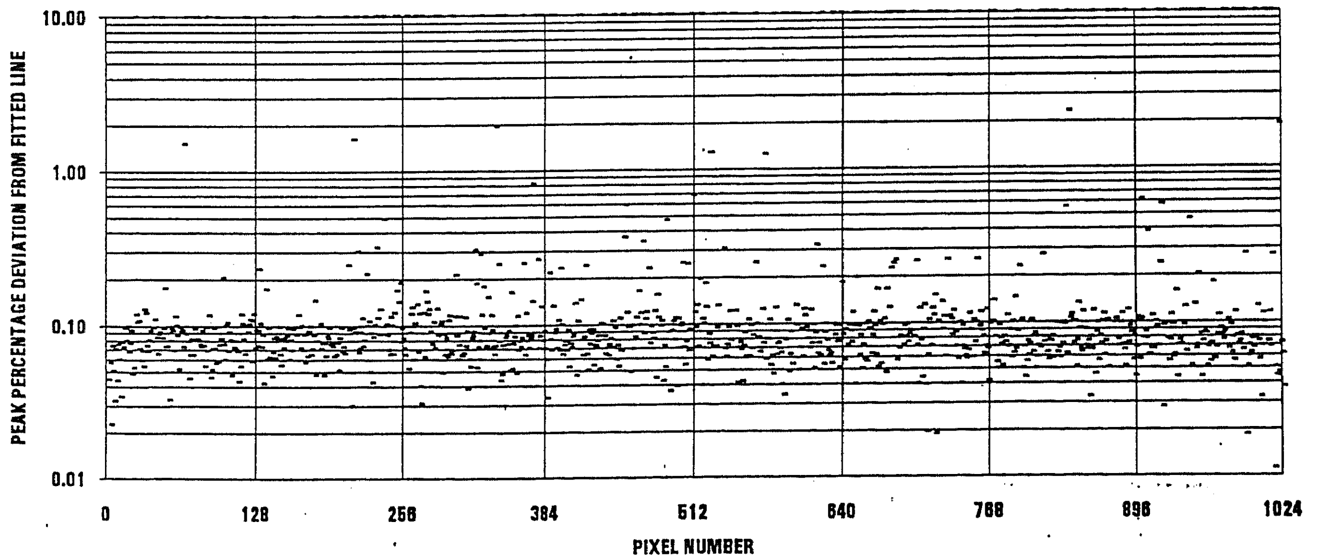

Figure 7.10 Measured linearity results of 2.2 um InGaAs focal plane array.

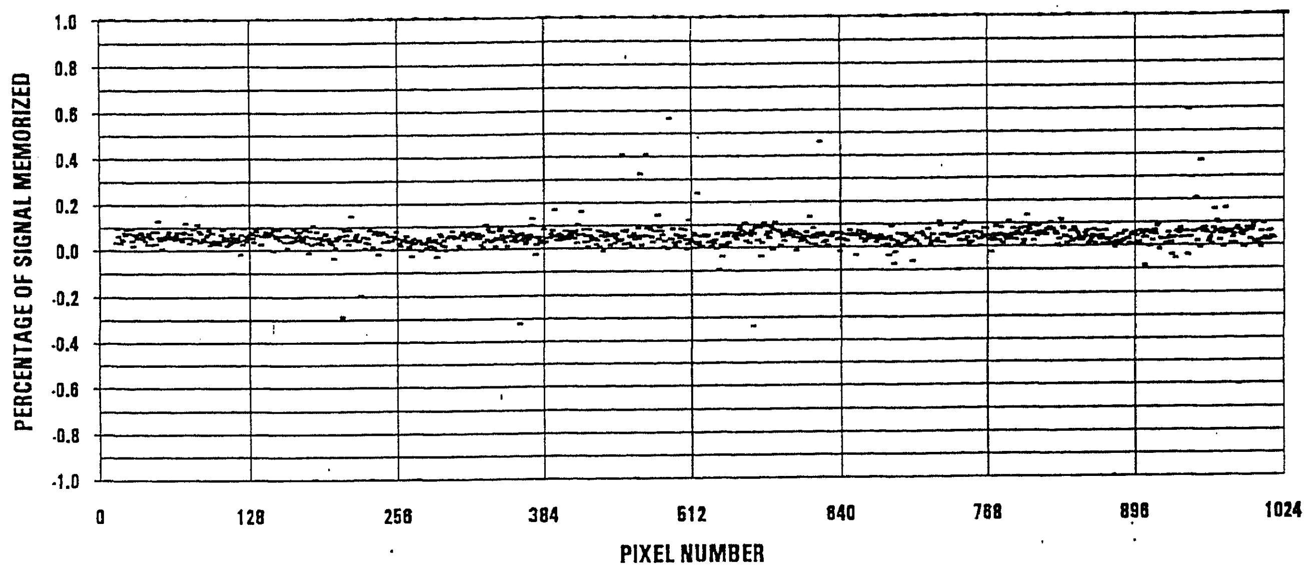

Figure 7.11 Measured memory effect results of 2.2 um InGaAs focal plane array.

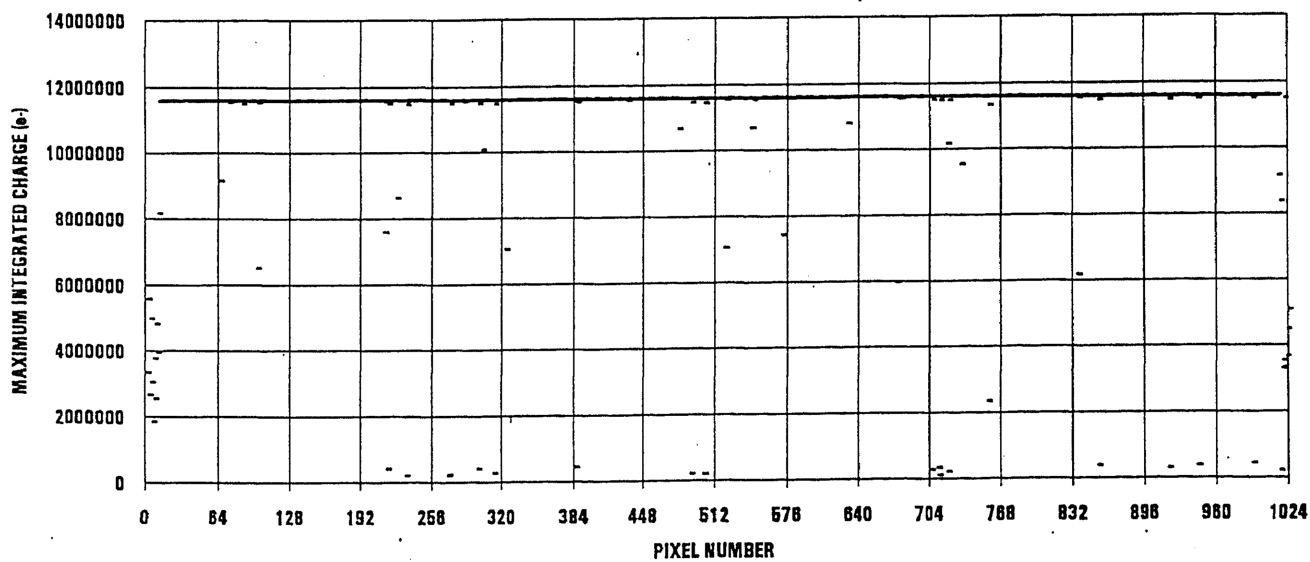

Figure 7.12 Measured maximum charge results of 2.2 um InGaAs focal plane array.

7.1.3 $In_{0.82}Ga_{0.18}As$ Detector Array Results

Figure 7.13 shows the measured dark current of the 1024 element 2.6 um cut-off InGaAs detector array at room temperature and 10 mV reverse bias voltage. This detector array sliver is integrated with the multiplexer. As seen from figure 7.13, the dark current is very uniform at room temperature across the 1024 element array. The number of bad pixels < 1% before integrating with the multiplexer. The dark current of seven elements were measured at 150 K and the mean value of seven pixels was 100 fA at 10 mV reverse bias.

The 2.6 um focal plane array consists of two detector slivers butted together to achieve the required 1024 element array. One single pixel was sacrificed at the splice between the two adjacent slivers. The dark current of 1024 elements of the 2.6 um cut-off wavelength InGaAs focal plane array is shown in Figure 6.25. The feed-back capacitance used was 0.8 pF. The measured dark current was at 150 K and measured at variable integration times until the pixel saturates in multiples of line times (33 ms). As seen from figure 7.13, the measured dark current is non-uniform from pixel to pixel. As explained in the dark current analysis section, this non-uniformity of dark current is attributed to the defect density from the misfit or threading dislocations, which acts as energy traps and have different energy levels in side the band gap. The mean value of dark current is about 200 fA at 10 mV reverse bias. The focal plane array dark current was measured with uniformity compensation and without the uniformity compensation. The dark current uniformity is better with the non-uniformity compensation circuit.

As explained in the dark current analysis section, the difficult and important parameter that effect the dark current and the temperature behavior of dark current in a

lattice mis-matched semiconductors are the dislocations and the deep levels that are created in the band gap. As seen from Fig. 7.13, the deep levels appear to be random in nature and have different energy levels in the band-gap. These traps freeze out at different temperatures supporting the random nature of these deep levels in side the band gap. Further study is required to understand the nature and behavior of these deep levels. One possible way to understand the energy levels of the deep levels is by using the deep level transient spectroscopy (DLTS) measurements.

Figure 7.14 shows the flat-filed optical response of the focal plane array measured using a black-body at a temperature of 150 K. The black body temperature was kept at 1000 K and the light source was through a narrow band pass spectral filter, with a center wavelength of 2291 nm. As seen from figure 7.14, the detector response is non-uniform from pixel to pixel. The measured quantum efficiency non-uniformity from pixel to pixel is < 5%. The absolute value of the quantum efficiency is measured using the 500 X 25 um area for each pixel. This area also includes the 500 um X 12 um non-diffused area (optically dead space). As explained in the dark current analysis section, the carrier life times are increasingly smaller and smaller as the mis-match between the InGaAs absorption layer and the InP substrate increases. This could be due to the increase in the defect density which will increase the recombination rate. The measured external quantum efficiency values also shows that the diffusion length in the mis-matched InGaAs/InP photodetectors is much smaller than the lattice matched InGaAs/InP photodetectors. This decrease in the diffusion length may be due to the decrease in the band-gap (from 0.75 eV to 0.46 eV) and the increase in the defect density.

From the measured values of quantum efficiency, the threading dislocation density was calculated using the expression 7.1

By allowing the η_o to be same as the lattice matched detector (> 85%), η to be the measured peak value of the diffused devices, and L_n to be the values deduced from the fitting parameters described in Chapter 4, the dislocation density is calculated as 1.5 X 10^6 /cm^2.

The measured noise of the focal plane array was shown in Figure 7.15. As seen from figure 7.15, the measured noise was bout 700 rms. e^-. The measured noise is the total amount of noise which includes the noise of the multiplexer, shot noise and Johnson noise of the detector. As mentioned in section 5, the measured noise of the multiplexer alone was about 400 rms. e^-.

The measured linearity of the focal plane array was shown in Figure 7.16. As seen from Fig. 7.16 the linearity of the array is less than 0.1%. The measured linearity is better than the best results reported to date and is achieved due to the linear capacitor development and the selection of proper implant dosage in the bulk Si substrate.

The memory effect or the un collected charge during the integration time is measured using the optical signal only during the current read out cycle of the integration time. At the end of the integration time, the optical signal was removed and the charge from the next integration time was measured. The measured memory effect result as a function of pixel number is shown in Fig. 7.17. As seen from Fig. 7.17, the measured value is less than 0.1% indicating that all of the charge is collected in the integrating capacitor after read-out cycle of the present integration time. This lower value of charge

carriers also indicates the reduction of diffusion length and hence minimum diffusion process of collection of carriers. As mentioned in the above section, the diffusion process is the slowest process of collection of charge carriers and is not dependent on the electric field.

The maximum integrated charge or the well capacity was measured using very long integration times by integrating the dark current until the integrating capacitor was completely filled. The measured charge capacity as a function of pixel number in a 2.6 um cut-off wavelength InGaAs Focal Plane Array is shown in Fig. 7.18. As seen from the measured results, the maximum charge handling capacity is with in the design value of the integrating capacitor and is very uniform from pixel to pixel.

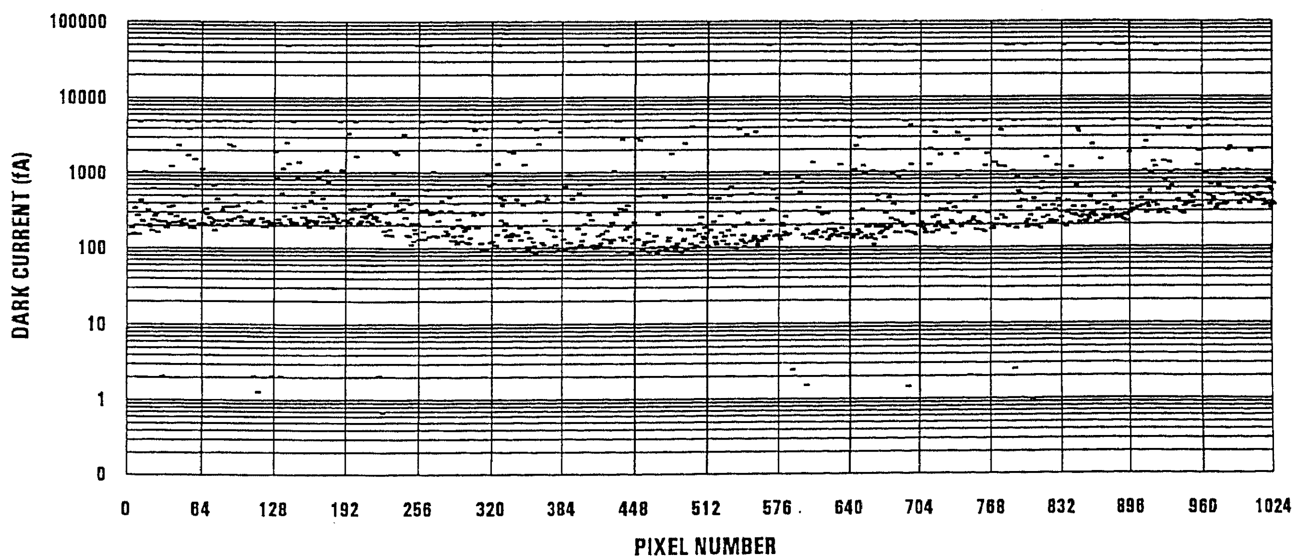

Figure 7.13 Dark current vs. pixel number of 2.6 um InGaAs focal plane array.

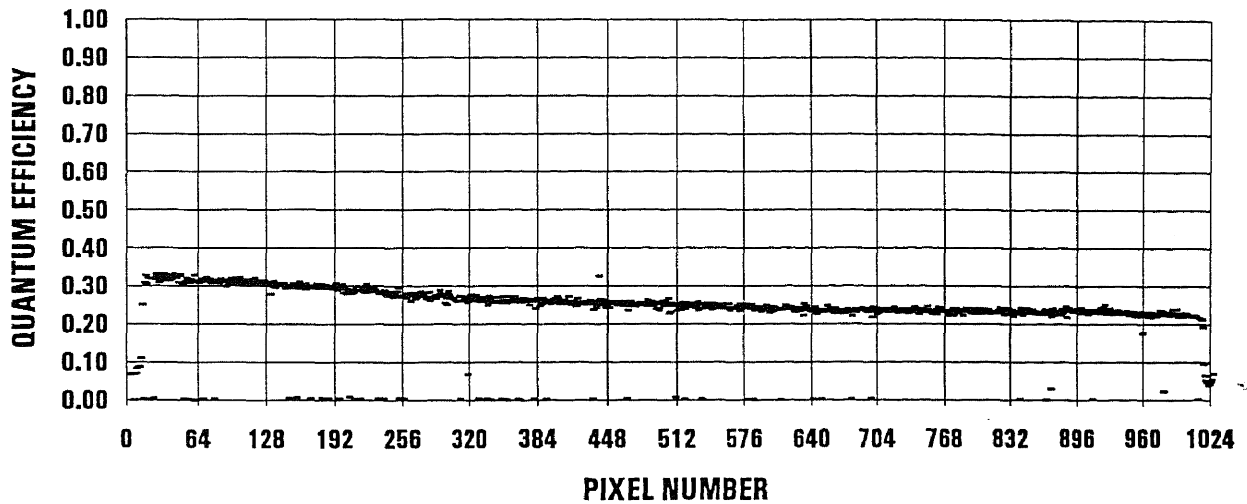

Figure 7.14 Flat-field optical response of 2.6 um InGaAs focal plane array.

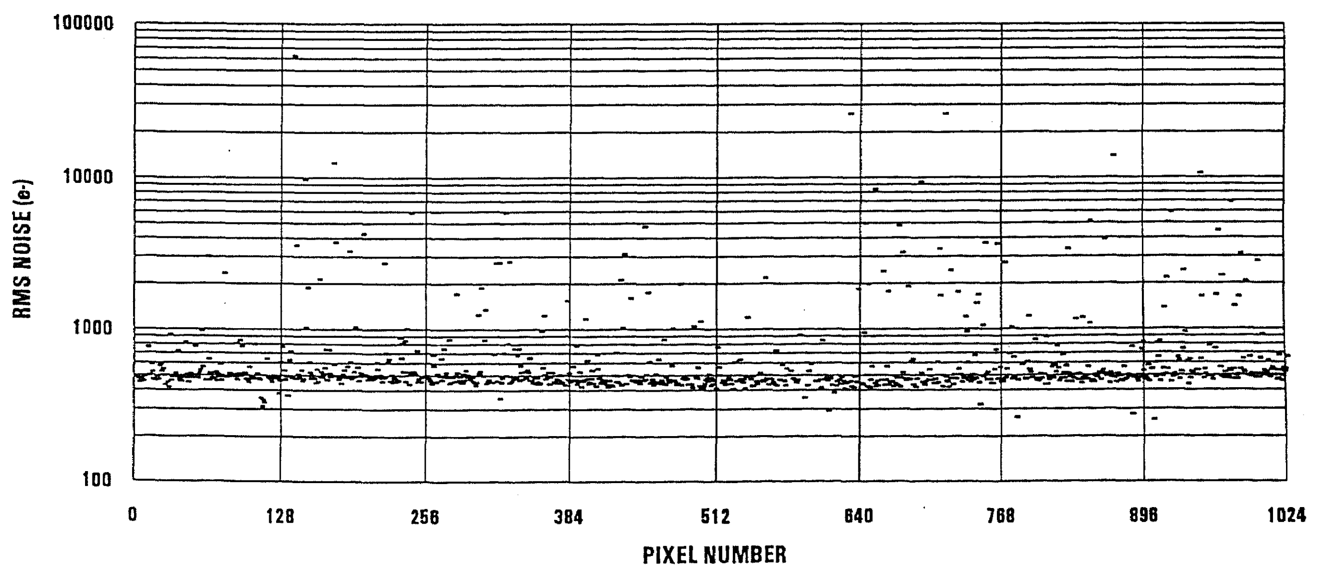

Figure 7.15 Measured noise results of 2.6 um InGaAs focal plane array.

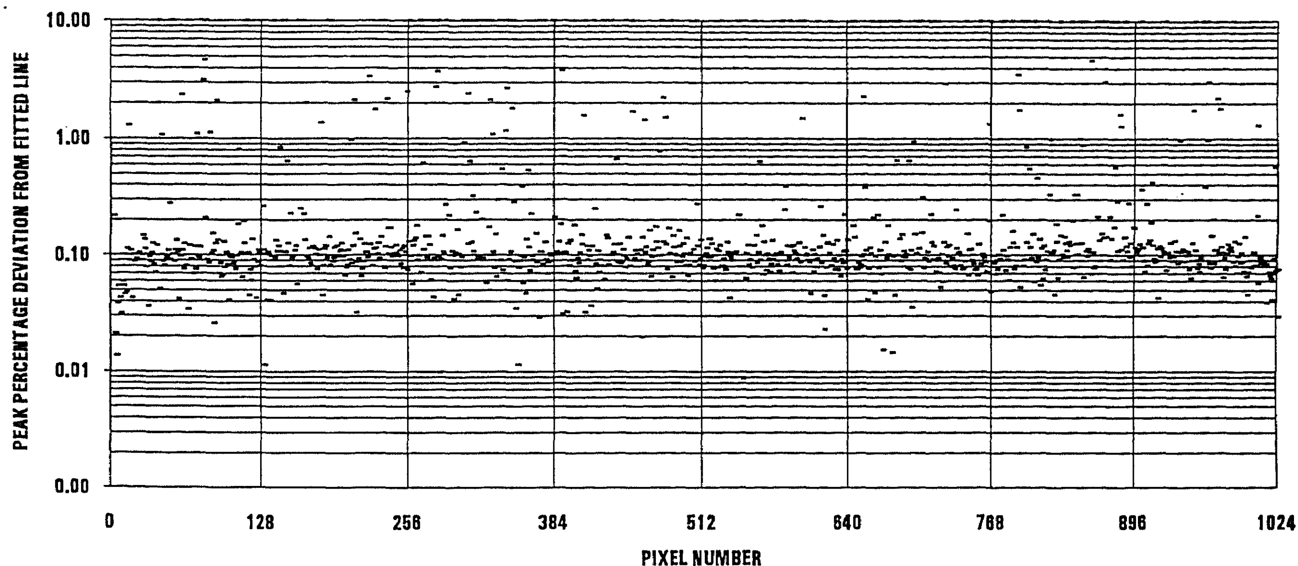

Figure 7.16 Measured linearity results of 2.6 um InGaAs focal plane array.

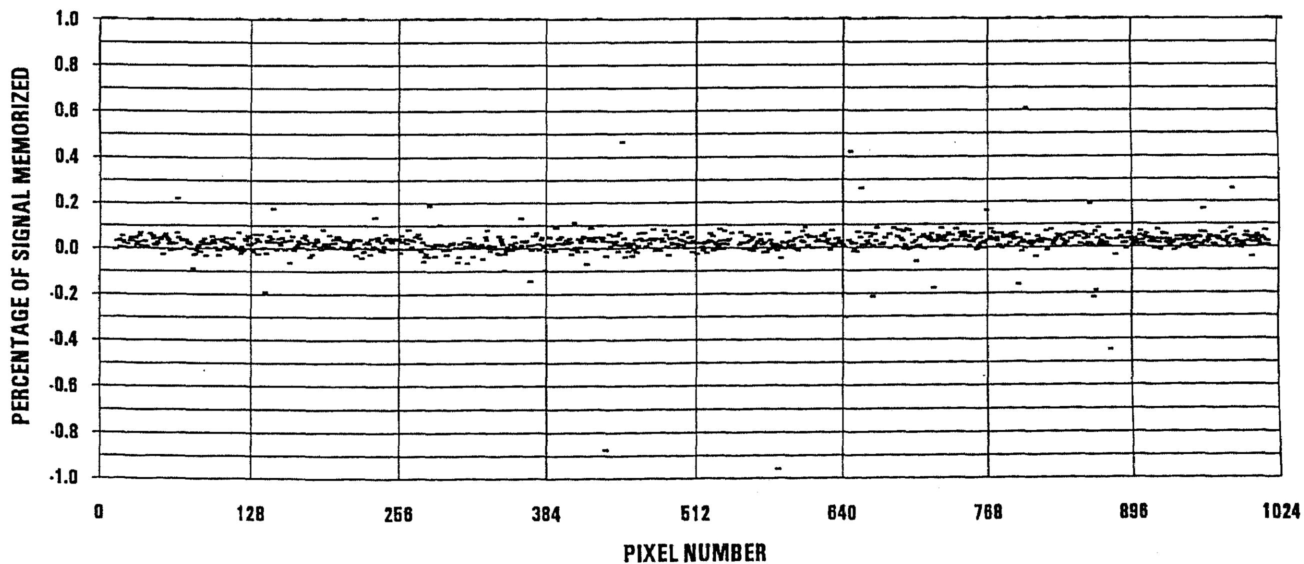

Figure 7.17 Measured memory effect results of 2.6 um InGaAs focal plane array.

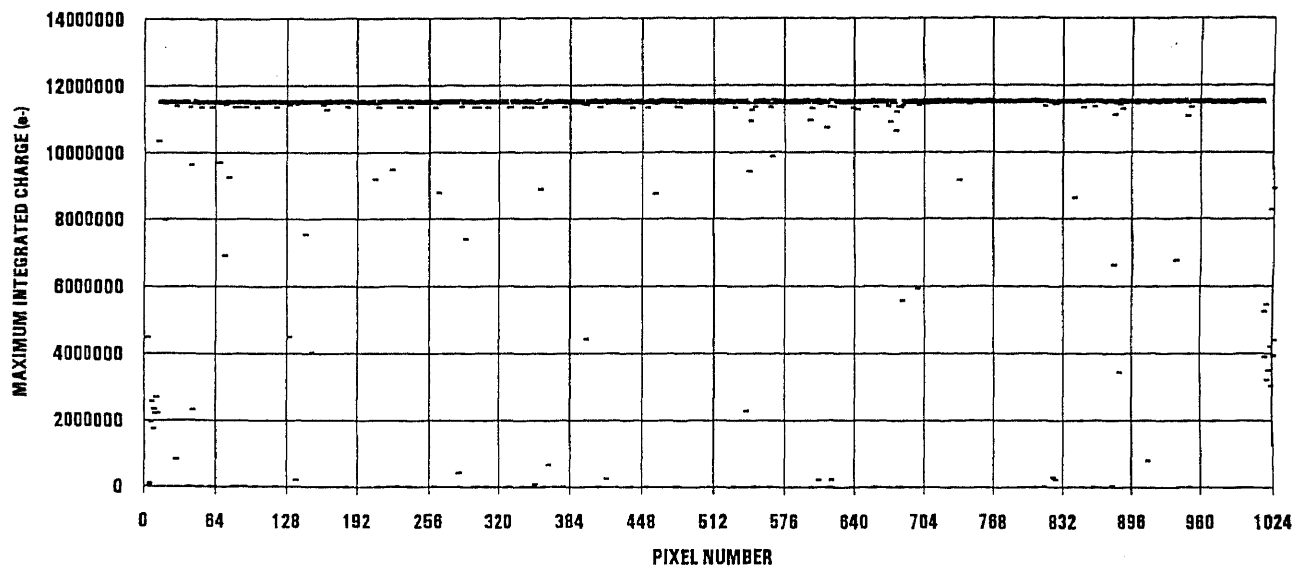

Figure 7.18 Measured maximum charge results of 2.6 um InGaAs focal plane array.

7.2 Radiation Hardness Testing Results of InGaAs Focal Plane Arrays

The InGaAs Focal Plane Array was subjected to a total dose of 5 ± 1 Krad , 10 ± 1 Krad, 15 ± 1 Krad of radiation from a cobalt 60 (CO 60) gamma particle source. The dose rate was between 50 rad(Si)/min and 300 rad (Si)/min. The irradiation was done when the Focal Plane Array was at operating temperature of 150 K. The irradiation dose was measured using a calibrated thermoluminescent detectors (TLD's).

After the irradiation, the measured dark current results doesn't show a significant difference from the initial measured results up to 10 Krad radiation. However, the dark current measurement after 15 Krad radiation shows an increase in the dark current from

the initial measured results. Further measurements of dark current shows a non uniformity of dark current also increased noticeably and a group of 25 pixels are forward biased. When the mode of operation was changed from NOCOMP to COMP, the change in bias voltage uniformity from pixel to pixel disappears. This change in dark current was attributed to the change of bias voltage. The bias voltage change could be due to the increase in the interface charge which changes the threshold voltage of the MOSFET. The increase in threshold voltage could also be due to the introduction of defect level in the energy gap, which acts as a generation center[59].

7.3 Noise Analysis of InGaAs Focal Plane Arrays

As explained in section 6.2.12, the read-out noise of the Si multiplexer with out threshold non-uniformity compensation is about 400 rms. electrons/pixel with a maximum integrating charge of 1 X 10^7 electrons/pixel and 700 rms. electrons/pixel with a maximum integrating charge of 3 X 10^7 electrons/pixel. As seen from table 6.2, the multiplexer noise is fairly constant with integration time and detector bias voltage. The major contribution of the Si multiplexer noise is from the KTC noise not removed by the Correlating Double Sampling (CDS) circuit and from the MOS channel broadband noise. The MOS channel 1/f noise contribution is small compared with the KTC and MOS channel broadband noise and can be neglected at the operating frequencies.

In the FPA noise calculations, it was assumed that the Si multiplexer noise is constant for a given maximum integrating charge. The major noise contributions in an InGaAs p-i-n detectors are dark current shot noise, Johnson-Nyquist noise and 1/f noise.

In addition to the shot noise, Johnson-Nyquist noise and 1/f noise, the InGaAs Focal Plane Arrays have noise contributions from the dark current variations due to the fluctuation in operating temperature and the burst noise or pop-corn noise or flicker noise due to the charge fluctuations from the dislocations which originate in the InP substrate and migrate to the InGaAs absorption layer. These charge fluctuations are due to the random charging and discharging of mis-fit dislocations and can be neglected for lower operating bias voltage. A lower reverse bias voltage prevents the depletion width from reaching these defects and thereby prevents the possible generation of burst noise.

The rms. value of dark current shot noise is given by

$$N_1 = \sqrt{\frac{I_d \times t_{\text{int}}}{q^2}} \tag{7.2}$$

Where I_d = Dark current of the detector in amps.

t_{int} = Integration time or the exposure time in sec.

The rms. value of Johnson-Nyquist noise is given by

$$N_2 = \sqrt{\frac{4KT\left(\frac{t_{\text{int}}}{2}\right)}{q^2 \times R_d}} \tag{7.3}$$

Where R_d = Detector resistance at a reverse bias voltage in ohms

t_{int} = Integration time or the exposure time in sec

K = Boltzman constant

T = Operating temperature

The total rms. noise of InGaAs focal plane array at an integration time of t_{int} is given by

$$N(t_{\text{int}}) = \sqrt{shot_{noise}^2 + JN_{noise}^2 + MUX_{noise}^2} \quad (7.4)$$

i.e.,

$$N(t_{\text{int}}) = \sqrt{\left(\sqrt{\frac{I_d \times t_{\text{int}}}{q^2}}\right)^2 + \left(\sqrt{\frac{4KT\left(\frac{t_{\text{int}}}{2}\right)}{q^2 \times R_d}}\right)^2 + MUX_{noise}^2} \quad (7.5)$$

The simulated rms. noise in electrons as a function of integration time is shown in Fig. 7.19 for dark current values of 20 fA, 40 fA, 80 fA and 120 fA. As shown in Fig. 7.19, the dark current shot noise is dominated for higher values of dark current even at small integration times. The increase in the dark current shot noise is because of the constant multiplexer noise and constant Johnson-Nyquist noise. The value of the detector resistance is constant for small operating voltages (< 100 mV) because the dark current is a linear function of bias-voltage. The measured total noise of the FPA with pixels having a dark current value of 20 fA, 40 fA, 80 fA and 120 fA is shown in Fig. 7.20 as a function of integration time. As seen from Fig. 7.19 and Fig. 7.20, the measured results agree with the simulated values.

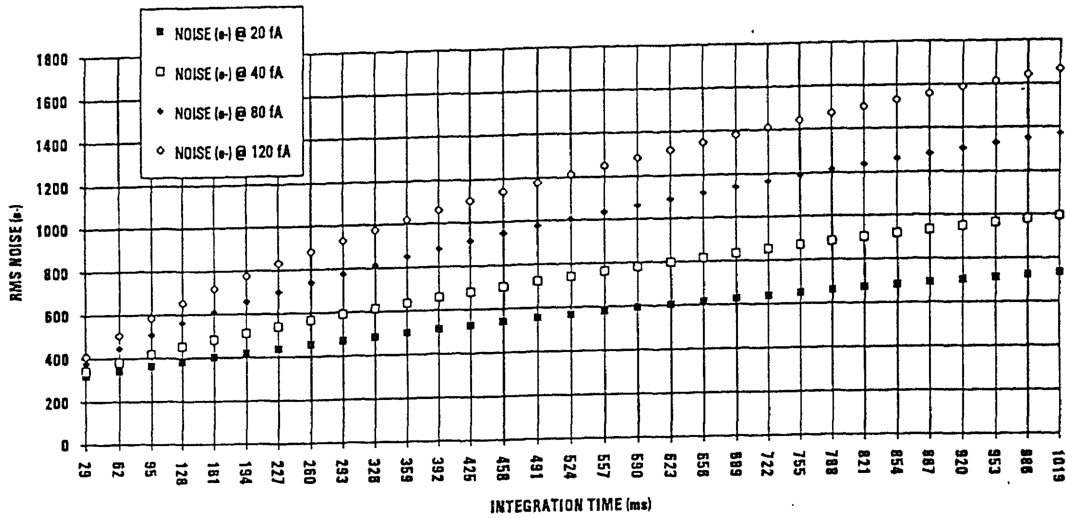

Figure 7.19 Simulated rms. noise electrons as a function of integration time.

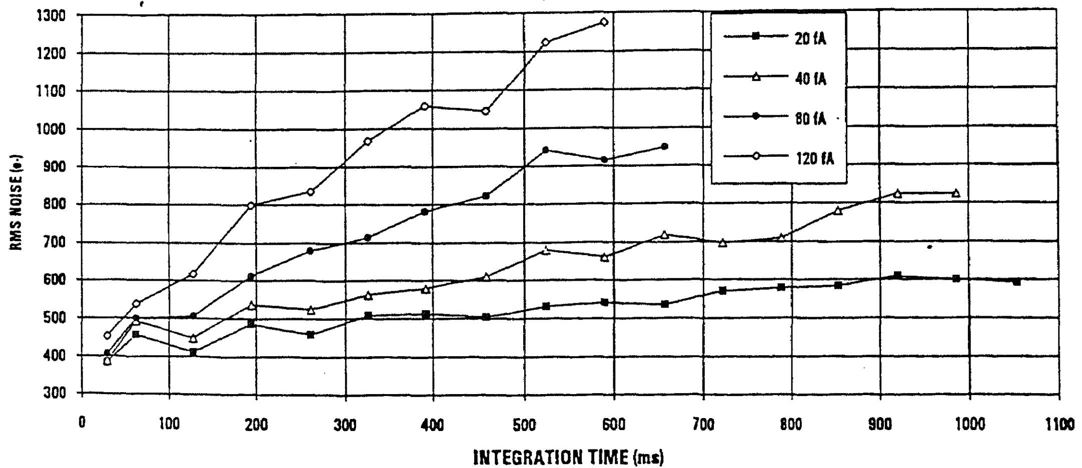

Figure 7.20 Measured rms. noise electrons as a function of integration time.

Measured rms. noise results as a function of dark current is shown in Fig. 7.21. As seen from Fig. 7.21, the rms. noise value is fairly constant as the dark current increases up to 100 fA. Beyond the 100 fA value of dark current, the rms. value of the FPA noise increases significantly because of the decrease in the detector resistance (dark current is not a linear function of bias voltage) and the Johnson-Nyquist noise dominates.

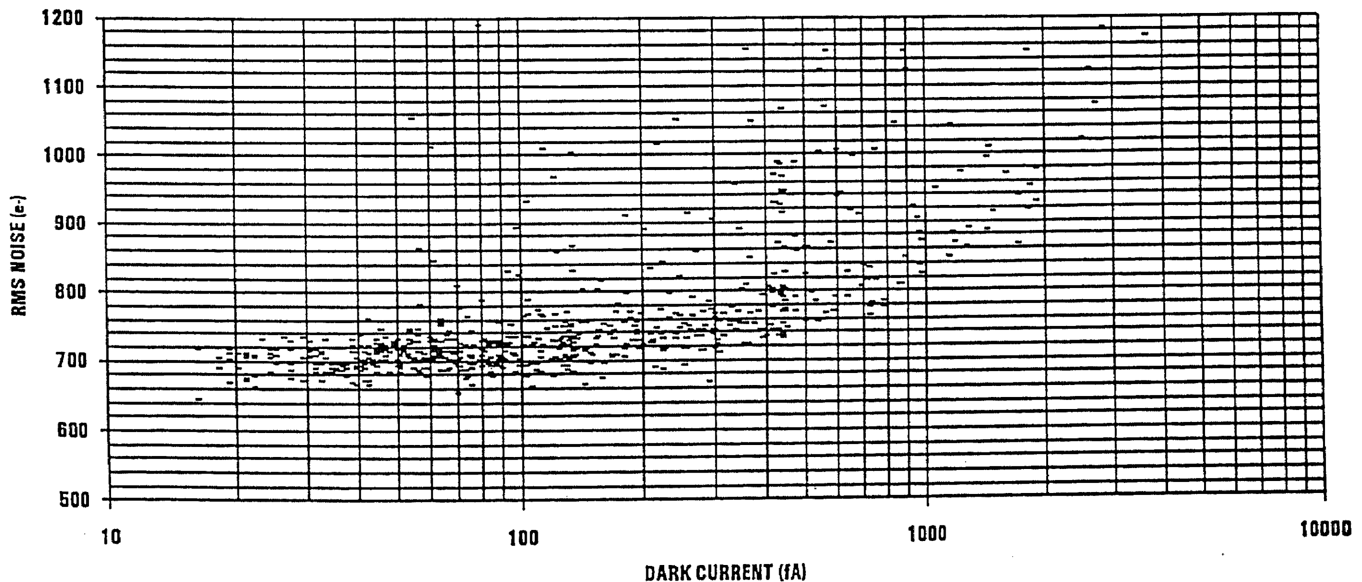

Figure 7.21 Measured rms. noise electrons as a function of dark current.

7.4 Comparison of Results with Other Technology

As mentioned in Chapter 1, one of the reason for making the InP/InAsP/InGaAs photodetectors attractive for long wavelength applications it's ability to get lower dark current and higher quantum efficiency using this technology. It is obviously interesting to know, what other materials and/or technology can achieve in the same wavelength region. One competing technology is of interest is the HgCdTe material grown on CdTe substrates using Molecular Beam Epitaxy (MBE). There is not much published data on HgCdTe material concerning dark currents, shunt resistance or the product of shunt resistance and detector active area, R_0A. Much of the work on HgCdTe material and detectors in the wavelength region of 1-2.6 um has been done at large aerospace companies which tend to keep data unpublished. The following table summarizes the comparison of performance between InGaAs photodetectors and HgCdTe detectors using the published information on both technologies[67]-[78]. It is extremely difficult to find data at exactly the same cut-off wavelengths and temperature with the same area devices. The table shows R_0A product, which is product of the shunt resistance (often measured at -10 mV reverse bias voltage) and active area of the detector. As seen from Table 7.1, the InGaAs technology has 10-100 X better performance than HgCdTe technology a given cut-off wavelength. Figure 7.22 shows the comparison measured R_0A value as a function of temperature for both InGaAs and HgCdTe technologies[7]. Also seen from this figure is that the InGaAs technology has better performance than the HgCdTe technology.

Table 7.1 Comparison of HgCdTe and InGaAs detector R_0A performance

Cut-off Wavelength	Temperature	RoA (Ω-cm^2)		Ref.
(μm)	(°K)	HgCdTe	InGaAs	
1.4	292	4E4	2.5E5	76
	230	7E6	1.3E8	76
1.7	300	2E2	2.5E5	
	220	2E5	1.3E8	68
2.1	300	7E1	2.5E3	
	220	7E3	6.5E5	68
2.5	300	1E1	1.3E2	
	210	1E3	1.0E5	
	150	1E6	1.3E7	69, 74, 75
	150	0.3E6	7E6	67

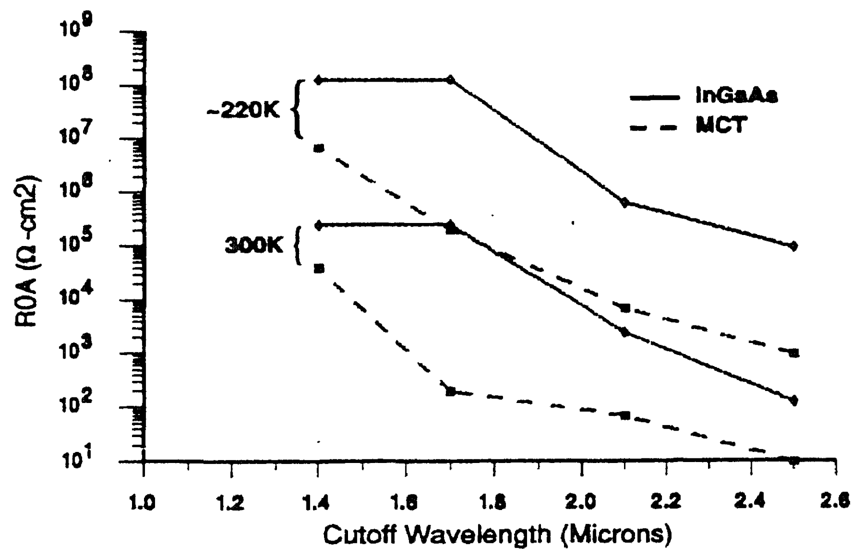

Figure 7.22 Comparison of InGaAs and HgCdTe detector performance as a function of wavelength and temperature.

CHAPTER 8

CONCLUSIONS

This research described the development of state of the art 1024 element linear InGaAs/InP Focal Plane Arrays with cut-off wavelengths of 1.7 um, 1.9 um, 2.2 um and 2.6 um. Detailed analysis of the material selection, crystal growth, device fabrication, and testing was presented. Introduction of sulfur doping in the InGaAs layer, reducing the lattice mismatch between the two $In_yAs_{1-y}P$ layers, post growth annealing techniques, the dielectric coating deposition and optimization of diffusion was discussed in detail. The doping in the InGaAs layer was optimized to 0.8 X 10^{17} cm^{-3} to avoid tunneling current at the operating temperature of 150 K, the composition of $In_yAs_{1-y}P$ layers was chosen to reduce the lattice mismatch to < 0.1%, thermal annealing techniques was implemented to reduce the number of dislocations, silicon nitride stripping and re-deposition was implemented to avoid the pin holes, and the diffusion conditions (500° C for 37 min.) was optimized to avoid deep junctions.

Dark current which is the critical parameter in the InGaAs/InP Focal Plane Arrays for achieving higher S/N ratio was discussed in detail and theoretical expressions was derived to simulate the dark current as a function of doping in the absorption layer and as a function of temperature and bias voltage. Dark current analysis shows that the dark current in the lattice matched (1.7 um cut-off wavelength) detectors is dominated by the surface generation-recombination current due to the interface states between the InP cap layer and the InGaAs absorption layer. Dark current improvement was achieved in the

lattice matched detectors by increasing the doping in the InP cap layer which reduced the number of surface states. The dark current analysis also shows that the dark current in the lattice mismatched (1.9, 2.2 and 2.6 um cut-off wavelength) devices was dominated by the defect density due to the misfit dislocations introduced during the crystal growth due to the lattice mismatch between the neighboring layers. The dark current reduction was achieved in the lattice mismatched devices by increasing the doping in the InGaAs absorption layer and implementing the post wafer growth thermal annealing, optimizing diffusion depth, silicon nitride deposition and using two level 'p' metal contacts. The measured dark currents of these devices was as low as 1 fA for 1.7 um, 20-30 fA for 1.9 um devices at 200 K temperature and 10-20 fA for 2.2 um and 50 fA for 2.6 um devices at an operating temperature of 150 K.

Detailed design and fabrication of a unique and novel Si read-out multiplexer using radiation hardened N-well CMOS process was presented. Each multiplexer unit cell was designed with capacitive transimpedance amplifier, correlated double sampling circuit, threshold non uniformity correction circuit and an output buffer stage for low noise, low power supply rejection ratio and low power dissipation to operate at near-zero bias voltage. Significant improvement for low noise operation was achieved with this optimized multiplexer design.

Integration and testing results of InGaAs focal plane arrays with cut-off wavelengths of 1.7 μm, 2.2 μm and 2.6 μm are described. The measured noise levels are as low as 600 rms. electrons on the complete focal plane array and as low as 400 rms. electrons for the multiplexer. Analysis of the performance results of focal plane arrays are

described in detail and the results shows that the InP/InGaAs technology is suitable for the long wavelength focal plane arrays with 1024 elements. Results of radiation testing using proton, gamma and electron particle radiation on InGaAs photodetectors and photodetector arrays are described. The results of InGaAs/InP Focal Plane Arrays achieved by this research are compared with published results of other technology (HgCdTe) in the same wavelength range and the results shows that InGaAs/InP Focal Plane Arrays have 10-100X lower dark current than the HgCdTe Focal Plane Arrays at the same operating temperature.

8.1 Future Direction

Future direction for the improvement of the performance of the InGaAs/InP Focal Plane Arrays for long wavelength applications should include the development of ternary bulk crystal growth (substrates) to grow the lattice matched $In_xGa_{1-x}As$ ($x>0.53$) absorption layer and development of native oxide for InP/InAsP to reduce the interface traps or surface states at the dielectric/semiconductor boundary, integration of read-out circuit on InP substrate using Opto-Electronic Integrated Circuit (OEIC) technology, understanding of the energy levels and reduction of the dislocation induced defects in the absorption layer by using crystal growth on mis-oriented and angled substrates.

APPENDIX A

DISLOCATION DENSITY USING DIFFUSION APPROXIMATION

A simplified model is used to explain the deleterious effect of dislocations on the external quantum efficiency of p-i-n detectors. Let us suppose that dislocations are perpendicular to the plane of the p-n junction, extending from the surface of the p-side to the surface of the n-side. To simplify the problem, the following assumptions are made:

(1) A "two-dimensional" projection is to be used, so that the volume of the diode is reduced to a plane, and dislocations are represented as lines perpendicular to the p-n junction.

(2) the electron injection efficiency in to the p-side is unity and p-side extends to infinity and

(3) the dislocation acts as a very effective non radiative recombination center characterized by an infinite recombination velocity.

Finally, after assuming that there is negligible recombination in the space charge region, the diffusion equation for the injected carriers is to be solved in the semi-infinite rectangular region depicted in figure A1.

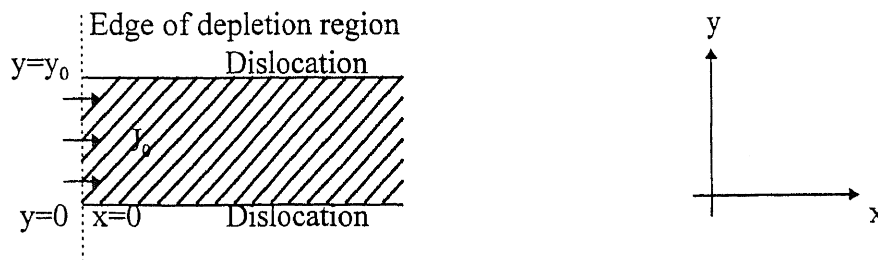

Figure A1 Region of application of the diffusion equation

$$D.\frac{\partial^2 n}{\partial x^2} + \frac{\partial^2 n}{\partial y^2} - \frac{n}{\tau} = 0 \qquad \text{(A.1)}$$

Subject to

$$n\,(x,0) = 0 \qquad \text{(A.2)}$$

$$n\,(x,y_0) = 0 \qquad \text{(A.3)}$$

$$n\,(\infty,y) = 0 \qquad \text{(A.4)}$$

$$-D.\frac{\partial\, n}{\partial x}\bigg|_{x=0} = J_0 \qquad \text{(A.5)}$$

Where,

n = excess minority carrier density,

D = diffusion constant

τ = average life time

y_0 = average spacing between the dislocations

$$y_0 = \frac{1}{\sqrt{\rho_d}} \qquad \text{(A.6)}$$

The boundary conditions (A.2) and (A.3) reflect the condition of infinite recombination velocity at the dislocation. Equation (A.4) is required to let the excess carrier density be zero at x = ∝, and equation (A.5) insures that the flux of minority carriers, J0 injected across the edge of the depletion region is constant.

The solution of Equation (A.1) is

$$n(x,y) = \frac{4.J_0}{\pi D}\sum_{l=0}^{\infty}\frac{\lambda_1}{(2l+1)}\sin\frac{(2l+1)\pi y}{y_0}e^{-\frac{x}{\lambda_1}} \tag{A.7}$$

Where,

$$\lambda_1 = \frac{L}{\sqrt{1+\frac{(2l+1)^2\pi^2L^2}{y_0^2}}} \tag{A.8}$$

and

$$L = \sqrt{D\tau} = \text{Diffusion length} \tag{A.9}$$

The number of carriers injected into each "cell"

$$N_{total} = \int_0^{y_0}\frac{\partial n}{\partial x}\bigg|_{x=0} dy \tag{A.10}$$

and the number of carriers lost nonradiatively by diffusion into dislocations

$$N_{lost} = 2\int_0^{\infty}\frac{\partial n}{\partial x}\bigg|_{y=0} dx \tag{A.11}$$

The change in bulk luminescent efficiency

$$\frac{\eta_{\text{int}}}{(\eta_{\text{int}})_0} = \frac{N_{rad}}{N_{total}} = 1-\frac{N_{lost}}{N_{total}} \tag{A.12}$$

Where,

N_{rad} = number of carriers that recombine radiatively.

By keeping only the first term in (A.10) and (A.11), and by assuming the external quantum efficiency varies the same way as the internal quantum efficiency, one can get

$$\frac{\eta}{\eta_0} = \frac{1}{1+\pi^2 L^2 \rho_d} \tag{A.13}$$

Many simplifying assumptions have been made in arriving at this result. The reduction of the three dimensional of real dislocations to a two dimensional sheet is unrealistic[79]. In addition, this model was developed for the case when the dislocations are perpendicular to the plane of the p-n junction. Equation (A.13), which has the same form as that in [80][81] contains several features that are expected on physical grounds. As the dislocation density shrinks to zero, the external quantum efficiency increases to its maximum value, η_0 and as ρ_d increases to ∞, the efficiency drops to zero. Moreover, equation (A.13) demonstrates that samples with long diffusion lengths are more sensitive to the effects of dislocations than samples with short diffusion lengths.

REFERENCES

1. S. Shibata, M. Horiguchi, K. Jinguji, S. Mitachi, T. Kanamori, T. Manabe, "Prediction of loss minima in Infra-red optical fibers," Electronics Letters, Vol. 17, No. 21. pp. 775, 15th Oct. 1981.

2. G.H. Olsen, "InGaAs fills the Near-IR detector array vacuum," Laser Focus, Vol. 27, pp. 48-51, 1991.

3. J.P. Burrows, K.V. Chance, P.J. Crutzen, H. van Dop, J.C. Geary, T.J. Johnson, G.W. Harris, I.S.A. Isaksen, G.K. Moortgat, C. Muller, D. Perner, U. Platt, J.P. Pommereau, H. Rodhe, E. Roeckner, W. Schneider, P. Simon, H. Sundqvist and J. Vercheval, "SCIAMACHY - A European proposal for atmospheric remote sensing from ESA Polar Platform," Max-Plank Institute fur Chemie, D6500 Mainz F.R.G., July 1988.

4. A.P.H. Goede, P. de Groene, R.W.M. Hoogeveen, J.de Vries, R.J. van der, A.C. Smorenburg and H. Visser, "SCIAMACHY Instrument Development for POEM-1," World Space Congress, 29 COSPAR, pp. A.2-S.7x, Washington, DC. 1992.

5. J.P Burrows, K.V. Chance, V. Rozanow and R.J. Spurr, "GOME and SCIAMACHY: Scientific Objectives," Proc. SPIE, Vol. 1715, 1992.

6. G.H. Olsen, A.M. Joshi and V.S. Ban, "Current Status of InGaAs detector arrays for 1-3 um," Proc. SPIE, VOL. 1540, pp. 596-604, 1991.

7. T.N. Krabach, C. Staller, S. Dejewski, T. Cunningham, M. Herring and E.R. Fossum, "InGaAs detectors for miniature infrared instruments," Proc. SPIE, VOL. 1874, pp. 1-10, 1992.

8. M. Wada, H. Hosomatsu, "Wide wavelength and low dark current lattice mismatched InGaAs/InAsP photodiodes grown by metalorganic vapor phase epitaxy," Appl. Physics Letters, Vol. 64, pp. 1265, 1994.

9. M.A. Poisson, C. Brylinski, et al., "$Ga_{1-x}In_xAs/InAs_yP_{1-y}/InP$ photodiodes for the 1.6 to 2.4 um spectral region grown by low pressure MOCVD," Journal of Crystal Growth, Vol. 124, pp. 782, 1992.

10. W. Wada, S. Sakakibara, M. Higuchi and Y. Sekiguchi, "Wide wavelength and low dark current lattice mismatched GaInAs photodiodes," Electronics Letters, Vol. 28, pp. 747, 1992.

11. F. Ducroquet, et al., "Electrical characterization of lattice mismatched $In_xGa_{1-x}As$ photodiode arrays for detection to 1.7 um," IPRM3 Conf. Proc., pp. 142, 1991.

12. K. Makita et al., "$Ga_{1-y}In_yAs/InAs_xP_{1-x}$ (y>0.53, x>0) pin photodiodes for long wavelength regions (> 2 um) grown by hydride vapour phase epitaxy," Electronics Letters, Vol. 24, pp. 379, 1988.

13. A.J. Moseley, M.D. Scott, A.H. Moore and R.H. Wallis, "High efficiency low leakage MOCVD grown GaInAs/AlInAs heterojunction photodiodes for detection to 2.4 um," Electronics Letters, Vol. 22, pp. 1206, 1986.

14. I M. Poulain, M.A. Poisson, K. Kazmierski, B. Cremoux, J.P. Moy and P. Radisson, "$In_xGa_{1-x}As$ photodiodes for the 1.0 to 2.4 um spectral region prepared by low-pressure MOCVD," Int. Symp. GaAs & Rel. Comp. 1984, pp. 421, 1984.

15. R.U. Martinelli, T.J. Zamerowski and P. Longeway, "2.6 um InGaAs photodiodes," Applied Physics Letters, 53(11), pp. 989, Sept. 1988.

16. V.S. Ban, G. Erickson, S. Mason, K. Woodruff, G. Gasparian and G.H. Olsen, "Room-temperature detectors for 800-2600 nm based on InGaAsP alloys," SPIE Proc., Vol. 1106, pp. 151-164, 1989.

17. G.H. Olsen, A.M. Joshi, S.M. Mason, K.M. Woodruff, E. Mykietyn, V.S. Ban, M.J. Lange, J. Hladky, G.C. Erickson and G.A. Gasparian, "Room Temperature InGaAs Detector Arrays for 2.5 um," SPIE Proc., Vol. 1157, pp. 276-282, 1989.

18. M.D. Scott, A.H. Moore, A.J. Moseley and R.H. Wallis, "$Ga_{0.28}In_{0.72}As/Al_{0.28}In_{0.72}As$ 2 um photodiode heterostructures prepared by atmospheric pressure MOCVD," J. of Cryst. Growth, Vol. 77, pp. 606-612, 1986.

19. A.M. Joshi, G.H. Olsen, S.M. Mason, M.J. Lange and V.S. Ban, "NIR (1-3 um) InGaAs Detectors and Arrays: Crystal Growth, Leakage Current, and Reliability," Proc. SPIE, Vol. 1715, 1992.

20. A.M. Joshi, V.S. Ban, S.M. Mason, and M.J. Lange, "512 and 1024 element linear InGaAs detector arrays for NIR (1-3 um) environmental sensing," Proc. SPIE, Vol. 1992.

21. S.M. Sze, High Speed Semiconductor Devices, John Wiley & Sons Inc., NY 1990.

22. K.R. Linga, G.H. Olsen, V.S. Ban, A.M. Joshi and W.F. Kosonocky, "Dark current analysis and characterization of $In_xGa_{1-x}As/InAs_yP_{1-y}$ graded photodiodes with $x > 0.53$ for response to longer wavelength (> 1.7 um)," Journal of Lightwave Technology, Vol. 10, No. 8, pp. 1050-1055, Aug. 1992.

23. K. Oe, Y. shinoda, and K. Sugiyama, "Lattice deformations and misfit dislocations in GaInAsP/InP double-heteostructure layers," Appl. Phys. Lett., Vol. 33, No. 11, pp. 962-964, Dec. 1978.

24. J.M. Matthews and A.E. Blakeslee, "Defects in Epitaxial Multilayers: I. Misfit Dislocations," J. of Crystal Growth, Vol. 27, pp. 118-125, 1974.

25. H. Temkin, et al , "Critical layer thickness in strained $Ga_{1-x}In_xAs/InP$ quantum wells," Applied Physics Letters, Vol. 55, pp. 1668, 1989.

26. C.D. Lee and S.R. Forrest, "Effects of lattice mismatch on $In_xGa_{1-x}As/InP$ heterojunctions," Appl. Phys. Lett., Vol. 57, No. 5, pp. 469-471, July 1990.

27. R.L. Moon, "The effect of mismatch on the performance of GaAsSb photodiodes," J. Appl. Phys., Vol. 51, No. 10, pp. 5561-5564, Oct. 1980.

28. E. Ishimura, T. Kimura, T. Shiba, Y. Mihashi, and H. Namizaki, "Dark current and diffusion length in InGaAs photodiodes grown on GaAs substrates," Appl. Phys. Lett., Vol. 56, No. 7, pp. 644-646, Feb. 1990.

29. R. People and J.C. Bean, "Calculation of critical layer thickness verses lattice mismatch for Ge_xSi_{1-x}/Si strained-later heterostructures", Applied Phys. Letters, Vol. 47, No. 3, pp. 322-324, 1985.

30. J.M. Matthews and A.E. Blakeslee, "Defects in Epitaxial Multilayers: II. Dislocation Pile-ups, Threading Dislocations, Slip Lines and Cracks," J. of Crystal Growth, Vol. 29, pp. 273-280, 1975.

31. P.M.J. Maree, J.C. Barbour, J.F. van der Veen, K.L. Kavanagh, C.W.T. Bulle-Lieuwma and M.P.A. Viegers, "Generation of misfit dislocations in semiconductors," J. of Appl. Phys., Vol. 62, No. 11, pp. 4413-4420, 1987.

32. D.I. Westwood, D.A. Woolf, A. Vila, A. Cornet and J.R. Morante, "Influence of mismatch on the defects in relaxed epitaxial InGaAs/GaAs(100) films grown by molecular beam epitaxy," J. Appl. Phys., Vol. 74, No. 3, pp. 1731-1735, Aug. 1993.

33. G.H. Olsen, "Interfacial Lattice Mismatch Effects in III-V Compounds," J. of Crystal Growth, Vol. 31, pp. 223-229, 1975.

34. G.H. Olsen, M.S. Abrahams, C.J. Buiocchi, and T.J. Zamerowski, "Reduction of Dislocation Densities in Heteroepitaxial III-V VPE Semiconductors," J. of Appl. Phys., Vol. 46, No. 4, pp. 1643-1646, 1975.

35. J.C.P Chang, T.P. Chin, C.W. Tu and K.L. Kavanagh, "Multiple dislocation loops in linearly graded $In_xGa_{1-x}As$ ($0 \leq x \leq 0.53$) on GaAs and $In_xGa_{1-x}P$ ($0 \leq x \leq 0.32$) on GaP," Appl. Phy. Lett., Vol. 63, No. 4, pp. 500-502, July 1993.

36. R. Kudela, "Growth of $In_{1-x}Ga_xAs$ by vapour phase epitaxy and analysis of growth conditions," J. of Crystal Growth, Vol. 133, pp. 289-295, 1993.

37. N. Susa, Y. Yamauchi and H. Kanbe, "Continuous Growth of High Purity InP/InGaAs on InP Substrate by Vapor Phase Epitaxy," Jap. J. of Appl. Phy., Vol. 20, No. 4, pp. L253-L256, April 1981.

38. S.B. Hyder, R.R. Saxena, S.H. Chiao and R. Yeats, "Vapor-Phase epitaxial growth of InGaAs lattice matched to (100) InP for photodiode application," Appl. Phys. Lett., Vol. 35, No. 10, pp. 787-789, Nov. 1979.

39. T. Mizutani, M. Yoshida, A.Usui, H. Watanabe, T. Yuasa and D. Hayashi, "Vapor phase growth of InGaAsP/InP DH structures by the dual-growth-chamber method," Jpn. J. of Applied Physics, Vol. 22, pp. L364-366, 1983.

40. G.H. Olsen, A.M. Joshi, E. Mykietyn, J. Colosi, K.M. Woodruff, M.J. Lange, G.C. Erickson, V.S. Ban and G.A. Gasparian, "Room-Temperature InGaAs Detector Arrays for 1.0-1.7 um Spectroscopy," Proc. SPIE, Vol. 1107, 1989.

41. K.R. Linga, 'Study and characterization of InGaAs photodiodes and photodiode arrays," M.S. thesis, Dept. of ECE., New Jersey Institute of Technology, Newark, Dec. 1990.

42. J.P Moy, J.J. Chabbal, S. Chaussat, J. Veyrier, and M. Villiard, "Buttable Arrays of 300 Multiplexed InGaAs Photodiodes for SWIR Imaging," Proc. SPIE, Vol. 686, pp. 93-95, 1989.

43. A.M. Joshi, K.R. Linga, "Low Leakage Current Photodetector Arrays," US Patent #: 5,387,796, Feb. 7, 1995.

44. K.R. Linga, A.M. Joshi, V.S. Ban and S. Mason, "1024 element $In_xGa_{1-x}As/InAs_yP_{1-y}$ detector arrays for environmental sensing from 1 um to 2.6 um," Proc. SPIE, Vol. 2021, pp. 90-97, July 1993.

45. J.Y. Yao, T.G. Anderson and G.L. Dunlop, "Structure of lattice strained $In_xGa_{1-x}As/GaAs$ layers studied by Transmission Electron Microscopy," Appl. Phys. Lett., Vol. 53, pp. 1420-1422, 1988.

46. K. Nakajima, S. Yamazaki, S. Komiya, and K. Akita, "Misfit dislocation-free $In_{1-x}Ga_xAs_{1-y}P_y/InP$ hetero-structure wafers grown by liquid phase epitaxy," J. Appl. Phys., Vol. 52, No. 7, pp. 4575-4582, July 1981.

47. C. Choi, N. Otsuka, G. Munns, R. Houdre, H. Morkoc, S.L. Zhang, D. Levi and M.V. Klein, "Effect if In situ and Ex situ Annealing on Dislocations in GaAs on Si Substrates," Appl. Phys. Lett., Vol. 50, No. 15, pp. 992-994, 1987.

48. J. Washburn, E.P. Kvam and Z.L. Weber, "Defect formation in Epitaxial Crystal Growth," J. of Elec. Materials, Vol. 20, No. 2, pp. 155-161, 1991.

49. M. Nakamura, S. Katsura, N. Makino, E. Ikeda, K. Suga and R. Hirano, "Effect of substrate misorientation on tear-drop like hillock defect densities in InP and GaInAsP grown by metalorganic chemical vapor deposition," J. of Crystal Growth, Vol. 129, pp. 456-464, 1993.

50. J. Narayan and O.W. Holland, "Rapid thermal annealing of ion-implanted semiconductors," J. of Appl. Phys., Vol. 56, pp. 2913-2921, 1984.

51. S. Sharan and J. Narayan, "Defect and defect reduction processing in semiconductor heterostructures," J. of Electronic Materials, Vol. 20, NO. 2, pp. 163, 1991.

52. N.B. Urli, V.S. Ban and K. Linga, "Defects in infrared detectors based on In-Ga-As alloys," Proc. 4th International Conf. on New Tech., pp. 88-94, Pula, Oct. 1993.

53. T.P. Pearsall, "$Ga_{0.47}In_{0.53}As$: A Ternary Semiconductor for Photodetector Applications," IEEE J. of Quantum Elec., Vol. QE-16, No. 7, pp. 709-720, July 1980.

54. N.J. Wu, T. Hashizume, H. Hasegawa and Y. Amemiya, "Unpinning of fermi level at InP schottky diode interfaces produced by novel in situ electrochemical process," IEEE VII Int. Conf. on IPREM, pp. 813 - 816, May 9-15, 1995.

55. T. Mizutani, M. Yoshida, A.Usui, H. Watanabe, T. Yuasa and D. Hayashi, "Vapor phase growth of InGaAsP/InP DH structures by the dual-growth-chamber method," Jpn. J. of Applied Physics, Vol. 22, pp. L364-366, 1983.

56. G.H. Olsen, S. Mason, G. Gasparian, A. M. Joshi, K. Woodruff, K. Linga, D. Rodefeld, M. Lange, F. Speer, V. S. Ban and G. Erickson, "Room temperature properties of Indium Gallium Arsenide detectors optimized for 1.8, 2.1 and 2.5 um," IEEE LEOS Conf. Proc., Boston, Nov. 1990.

57. K. R. Linga, C.S. Wang, Y. Dzialowski, M. Lourie, S. Mason and W.F. Kosonocky, "High performance 1024 element InGaAs hybrid focal plane arrays from 1 to 2.6 um," OPTO94 Conference Proceedings, pp. 1024-1030, Paris Apr. 1994.

58. A.S. Kanofsky and K. Linga, "Effects of radiation on long wavelength devices," Proc. SPIE, Vol. 2074, pp. 214-220, Aug. 1994.

59. G.J. Shaw, R.J. Walters, S.R. Messenger and G.P. Summers, "Time dependence of radiation-induced generation currents in irradiated InGaAs photodiodes," Journal of Applied Physics, Vol. 74, No. 3, pp. 1629-1635, 1993.

60. S.R. Forrest, R.F. Leheny, R.E. Nahory and M.A. Pollack, "$In_{0.53}Ga_{0.47}As$ Photodiodes with dark current limited by generation-recombination and tunneling," Applied Physics Letters, Vol. 37(3), pp. 322, 1980.

61. S.R. Forrest, M. DiDomenico, R.G. Smith and H.J. Stocker, "Evidence for tunneling in reverse-biased III-V Photodetector diodes," Applied Physics Letters, Vol. 36(7), pp. 580, 1980.

62. M.W. Smith and S.F. Bigger, "Calibration and performance evaluation of a portable shortwave infrared (1.05 to 2.45 um) spectrometer," Optical Eng., Vol. 33, No. 11, pp. 3781-3792, Nov. 1994.

63. W.F. Kosonocky, W. Kleinhans, C. Lau, K.R. Linga and M. Lourie, "Low-Bias CTIA Multiplexer for 1024-Element InGaAs Line Sensors," Pro. SPIE, Vol. 2226, pp. 152-171, Apr. 1994.

64. K.R. Linga. C.S. Wang, M. Louire, W. Xu and W.F. Kosonocky, "High Performance InGaAs/InP Focal Plane Arrays," POEM Ann. Rev. Mtg., Princeton Univ., Princeton, NJ, Mar.1997.

65. C.B. Morrison, S.M. Bedair and K. J. Bachmann, "$In_xGa_{1-x}As$ Photodetector for the 1.7-2.0 um Spectral Region," J. Electrochem. Soc., Solid-State Science and Technology, Vol. 132, No. 7, pp. 1717-1720, 1985.

66. R. J. Roedel, A.R. Van Neida, R. Caruso and L.R. Dawson, " The effect of dislocations in $Ga_{1-x}Al_xAs$:Si light-emitting diodes," J. of Electrochem. Soc., Vol. 126, No. 4, pp. 637-641, 1979.

67. O. saint-Pe, O. Donnadieu, R. Davancens, D. Charlton, A. Menardi, M. Fabbricotti, B. Harnisch, R. Meynart and B. Kunkel, "Development of a 2-D Array for 1 to 2.35 um Hyperspectral Imager," To be published.

68. L.O. Bubulac, W.E. Tennant, J.G. Pasko, L.J. Kozlowski, M. Zandian, M.E. Motamedi, R.E. DeWames, J. Bajaj, N. Nayar, W.V. McLevige, N.S. Gluck, R. Melendes, D.E. Cooper, D.D Edwall, J.M. Arias, R. Hall and A.I. D'Souza, "High performance SWIR HgCdTe Detector Arrays," To be published.

69. L.J. Kozlowski, S.L. Johnston, W.V. McLevige, A.H.B. Vanderwyck, D.E. Cooper, S.A. Cabelli, E.R. Blazejewski, K. Vural, W.E. Tennent, "128X128 PACE-I HgCdTe hybrid FPAs for thermoelectrically cooled applications," SPIE Proc., Vol. 1874, 1992.

70. L.J. Kozlowski, J.M. Arias, G.M. williams, K. Vural, D.E. Cooper and S.C. Cabelli, "Recent advances in staring hybrid focal plane arrays:Comparision of HgCdTe, InGaAs, and GaAs/AlGaAs detector technologies", SPIE Proceedings, Vol. 2274, 1994.

71. L.J. Kozlowski, J.M. Arias and W.E. Tennant, "Experimental comparison of staring IR sensor technologies including PV HgCdTe, PV InGaAs, and quantum well GaAs/AlGaAs," 11th Conf. on Solid and liquid crystals-Material science and applications, Zakopane, Oct. 1994.

72. J.M. Arias, M. Zandian, R. Zucca and R.E. DeWames, "P-i-n HgCdTe photodiodes grown by Molecular Beam Epitaxy," Appl. Phys. Letters. Vol. 58, N0. 24, June 17, 1991.

73. J. Thompson, P. Mackett, G.T. Jenkin, T. Nguyen Duy and P. Gori, "The growth of CdHgTe by Metalorganic Chemical Vapour Phase Deposition," J. of Crystal growth, Vol. 86, pp. 917-923, 1988.

74. R.J. Van der, R.W.M. Hoogeveen, H.J. Spruijt, A.P.H. Goede, "Low noise InGaAs infrared (1.0-2.4 um) focal plane arrays for SCIAMACHY," European Symp. on Sat. Remote Sensing III, Sept. 1996.

75. L.J. Kozlowski, K. Vural, W.E. Tennant, R. Kezer and W.E. Kleinhans, "Low-noise 2.5 um PACE-I HgCdTe 10 X 132 FPA with 25 um pitch and on-chip signal processing including CDS and TDI," IRIS mtg., Ext. Abstracts, 1991.

76. L.J. Kozlowski, V.H. Johnson, J.K. Chen, D.D. Edwall, A.M. Blume, I.S. Gergis, K. Vural, W.J. Parrish and J.D. Blackwell, "Low Noise SWIR HgCdTe FPA with advanced signal processing in a CMOS readout," IRIS mtg., Ext. Abstracts, 1988.

77. M. Blessinger and M. Herring, "Results of testing short wavelength HgCdTe hybrid focal plane arrays for earth remote sensing applications," SPIE Proc., Vol. 501, pp. 136-141, 1984.

78. J. Flachet, M. Royer, Y. Carpentier and G. Pichard, "Emission and detection in the 1 to 3 um spectral range with $Hg_{1-x}Cd_xTe$ diodes," SPIE Proc., Vol. 587, pp. 149-155, 1985.

79. M. Lax, "Junction Current and Luminescence Near a Dislocation or a Surface," J. Appl. Phys., Vol. 49, pp. 2796-2810, 1978.

80. R.P. Joshi, "Microscopic calculations of density and field-dependent electronic trapping via attractive coulomb centers," J. Appl. Phys., Vol. 74, No. 3, pp. 1810-1817, Aug. 1993.

81. K. Kazmierski, P. Philippe, P. Poulain and B. de Cremoux, "C-V measurement and modelization of GaInAs/InP heterointerface with traps," J. Appl. Phys., Vol. 61, pp. 1941-1946, 1987.

82. J.P. Moy, X. Hugon, J. Chabbal, J. De Cachard, C. Lenoble, D. Mollaret, M. Villard, B. Villotitch, "3000 InGaAs photodiode multiplexed linear array for the Spot 4 SWIR Channel," SPIE Proc., Vol. 1107, pp. 137-151, 1989.

83. J.P. Moy, J. de Cachard and S. Chaussat, "CCD for SWIR photodiode multiplexing," SPIE Proc., Vol. 865, pp. 59-64, 1987.

84. M.A. di Forte-Poisson, C. Brylinski, P. Poulain, J.P. Moy, M. Villard, S. Chaussat, J. Decachard and B. Vilotitch, "LP-MOCVD multiplexed SWIR $In_xGa_{1-x}As$ photodiode arrays for spot IV satellite," Int. Symp. GaAs and Related Compounds, pp. 785-788, 1987.

85. A.K. Chin, B.V. Dutt, W.S. Trimmer, J.R. Zuber, T. Boone and K.D. Trapp, "Evaluation of misfit dislocations in planar, zinc-diffused $In_{0.53}Ga_{0.47}As$ pin photodiodes," Materials Letters, Vol. 1, No. 5,6, pp. 152, 1983.

86. M. Cohen and G. H. Olsen, "Near-IR imaging cameras operate at room temperature," Laser Focus World, pp. 109-113, June 1993.

87. G.H. Olsen, "InGaAs fills the near-IR detector-array vacuum," Laser Focus World, pp. A21-A30, March 1991.

88. V.S. Ban, G.H. Olsen and A.M. Joshi, "High performance InGaAs detectors and arrays for Near-Infrared Spectroscopy," Spectroscopy, Vol. 6, No. 3, pp. 49-53, 1991.

89. G. Olsen, A. Joshi, M. Lange, K. Woodruff, E. Mykietyn, D. Gay, G. Erickson, D. Ackley, V. Ban and C. Staller, "A 128X128 InGaAs Detector for 1.0-1.7 Microns," SPIE Proc., Vol. 1314, pp. 31-35, 1990.

90. P.A. Longeway and R.T. Smith, "Compositional gradients in InGaAs - A growth model and the electrical effects on photodetectors", Journal of Crystal Growth, Vol. 89, pp. 519-526, 1989.

91. C.D. Lee and S.R. Forrest, "$In_{0.53}Ga_{0.47}As/InP$ heterojunctions with low interface defect densities," J. Appl. Phys., Vol. 69, pp. 342, 1991.

92. T.P. Lee, C.A. Burrus, W.B. Sessa and W.T. Tsang, "$InAs_xP_{1-x}/InP$ photodiodes prepared by molecular beam epitaxy," Electronics Letters, Vol. 20, No. 9, pp. 363, 1984.

93. R.P. Schneider, D.X. Li and B.W. Wessels, "Structural and optical properties of highly strained $InAs_xP_{1-x}/InP$ heterostructures," J. of Electrochem. Soc., Vol. 136, No. 11, pp. 3490, 1989.

94. W.Y. Lum and A.R. Clawson, "Thermal degradation of InP and its control in LPE growth," J. Appl. Phys., Vol. 50, No. 8, pp. 5296-5301, Aug. 1979.

95. W.Y. Han, L. Calderon and Y. Lu, "Effects of annealing conditions on heavily carbon-doped InGaAs," Appl. Phys. Lett., Vol. 62, No. 20, pp. 2578-2580, May 1993.

96. J.M. Tartagilia, S.M. Crochiere, C.E. Kalnas and D.L. Farrington, "A study of etch pit density and x-ray rocking curves for GaAs substrate evaluation," J. of Elec. Mat., Vol. 20, No. 5, pp. 345-352, 1991.

97. D.J. Tweet, H. Matsuhata, R. Shioda, H. Oyanagi, and H. Kamei, "Island Growth and Phase Separation in strained $InAs_{1-x}P_x$/InP heterostructures," IEEE VII Int. Conf. on IPREM, pp. 206-209, May 9-15, 1995.

98. S.F. Yoon, K. Radhakrishnan, H.M. Li and D.H. Zhang, "A photoluminescence study of the effect of well thickness in strained InGaAs/AlGaAs heterostructures grown by molecular beam epitaxy," J. Mater. Res., Vol. 9, No. 7, pp. 1834-1838, Jul. 1994.

99. J.J Tietjen, H.P. Maruska and R.B. Clough, "The Preparation and Properties of Vapor-Deposited Epitaxial $InAs_{1-x}P_x$ Using Arsine and Phosphine," J. Electrochem. Soc., pp. 492-494, April 1969.

100. C.J. Nuese, G.H. Olsen, M. Ettenberg, J.J. Gannon and T.J. Zamerowski, "CW Room-temperature $In_xGa_{1-x}As/In_yGa_{1-y}P$ 1.06 um Lasers," Applied Phys. Letters, Vol. 29, pp. 807-809, Dec. 1976.

101. R.R. Saxena, S.B. Hyder, P.E. Gregory and J.S. Escher, "Vapor phase epitaxial growth of InGaAs/InAsP heterojunctions for long wavelength transferred electron photo cathodes," J. of Cryst. Growth, Vol. 50, pp. 481-484, 1980.

102. P.E. Gregory, J.S. Escher, R.R. Saxena and S.B. Hyder, "Field-assisted photoemission to 2.1 microns from a Ag/p-$In_{0.77}Ga_{0.23}As$ photocathode," Appl. Phys. Lett., Vol. 36, No. 8, pp. 639-640, Apr. 1980.