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ABSTRACT

DESIGN AND DEVELOPMENT OF FOUR TO SIXTEEN CHANNEL VIDEO MULTIPLEXERS

**by
Ronan Rahimi**

Video multiplexer series were successfully designed and built for prototype and evaluation both in terms of hardware and software. The hardware platform was designed to accommodate up to sixteen color video input channels for time lapse or real time recording on a single video cassette recorder. This product implements four modes of operation; Live, Record, Playback and Menu mode, which is not a full mode of operation. Menu mode is a series of on-screen programming menus which appears on Live, Record and Playback modes. Menu mode enables the user to program the machine to work under specific modes of application. For Video encoding a new video-capture processor, called Bt819 made by BrookTree, was chosen to minimize the cost and system overhead of adding video input and capture to PC video/graphics systems. This development by BrookTree employs the firm's time-tested digital Ultralock technology to generate the required number of pixels per line using fixed frequency clock. On-chip pixel buffering and image scaling are provided for our QUAD picture on a monitor. Inter-integrated circuit (I²C) communication was chosen to talk to this chip directly. The video syncs were generated from PIC microcontroller using assembly language. This program was designed at 13.5 Mhz (74 nsec) clock rate which follows NTSC CCIR-601 digital video standards. Alarm package design idea came from understanding of link-list programming and was tested on four separate video signals.

**DESIGN AND DEVELOPMENT OF FOUR TO SIXTEEN
CHANNEL VIDEO MULTIPLEXERS**

**by
Ronan Rahimi**

**A Thesis
Submitted to the Faculty of
New Jersey Institute of Technology
in Partial Fulfillment of the Requirements for the Degree of
Master of Science in Electrical Engineering**

**Department of Electrical and Computer Engineering
January 1996**

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This Thesis is dedicated to
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CHAPTER 1

INTRODUCTION

The purpose of this document is to provide a unique and summarized description of the Video Multiplexer (V.M.), both in terms of software coding and hardware design.

A time lapse VCR is a proven and valuable tool for documenting video events captured on a single VCR. Applications employing multiple cameras require additional VCRs, sequential switchers or Multi - format displays such as Quads, Nano and Hex. Each of these has its tradeoffs; for example, the VCR is an expensive piece of equipment and requires maintenance. The switcher reduces the rate at which each camera is recorded, and since the switcher output in most cases is non - synchronized and VCR expects to see constant sync, during playback the picture will contain instabilities like “picture flagging”.

The video multiplexer technology substitute the use of costly time lapse VCRs for the CCTV customers with small budgets to spend on some expensive VCRs and its maintenance. Therefore, the four channel digital Video Multiplexer (V.M.) is a non-expensive state of art, time base corrected product for those type of customers. This digital Video Multiplexer is designed to fit on a single rack height, half rack cabinet with a desk or rack mount capability. All the hardwares are using surface mount technology with some through hole exceptions.

This product implements three mode of operations which all modes (Live, Record and Playback) use the full digital video capability available in this 4 channel

multiplexer. Every mode also behaves interactively and separately through user front panel modifications.

The software and hardware are designed side by side using simulators and real time hardware bread board prototyping, so the final PC board can be debugged in less time and in more efficient way. This video multiplexer is capable of encoding (recording) up to four cameras on a single time lapse VCR and on the playback decoding these cameras are either displayed in full screen or quad (four digitized pictures) modes. The encoding/decoding for this machine is done through a two powerful encoding/decoding processors made by the Brooktree Corporation, which uses the latest technology in terms of buffering and sampling video signals. These two processors are capable of adjusting the picture for compression and recalibration of video signal in terms of color modulation/demodulation and number of vertical and horizontal syncs. All the encoded video signals are transferred to 12,000,000 dual ram memory cells; 6,000,000 for Chrominance and 6,000,000 for Luminance. The dual ram memory gets loaded with digital video through its parallel ports, and the stored digital video is transferred to the decoder processor via dual ram's serial port. The timing signals for transferring these digital bytes to and out of memory are done through another powerful processor made by American Dynamics known as ASYC controller. This timing processor basically produces the addressing counts for the dual ram's rows and columns as well as video synchronization. All these processors are discussed in more detailed through out the rest of this document.

The back of this multiplexer has seven BNC connectors, four for camera inputs, one for VCR output, one for monitor output and one for VCR input during VCR playback

and one external connector for four alarm inputs. Each pin on the external connector is used for one camera input, which when activated TAG the associated camera images with VID (Vertical Interval Data), meaning that on the VCR tape before video gets stored on to a tape, we store information about that camera input in this order; camera ID, the field bit indicator and the alarm bit. All the alarms also stored in an ALARM LOG tables, which then presented to the user on the screen in multiple lists. These lists are displayed to the user using an Alpha Numeric processor which uses video sync to mix video with pure ASCII characters. The protocol used to send ASCII characters to this character display processor uses serial communication. The ASCII datas are not stored in the dual ram memory because the alpha numeric processor is sitting in front of the encoding processor (Brooktree Bt819). The unit housing as well front and back panels are illustrated on the diagram below. On the back panel alarms, BNCs and two pins (S1 , S2) for future code transfers can be viewed.

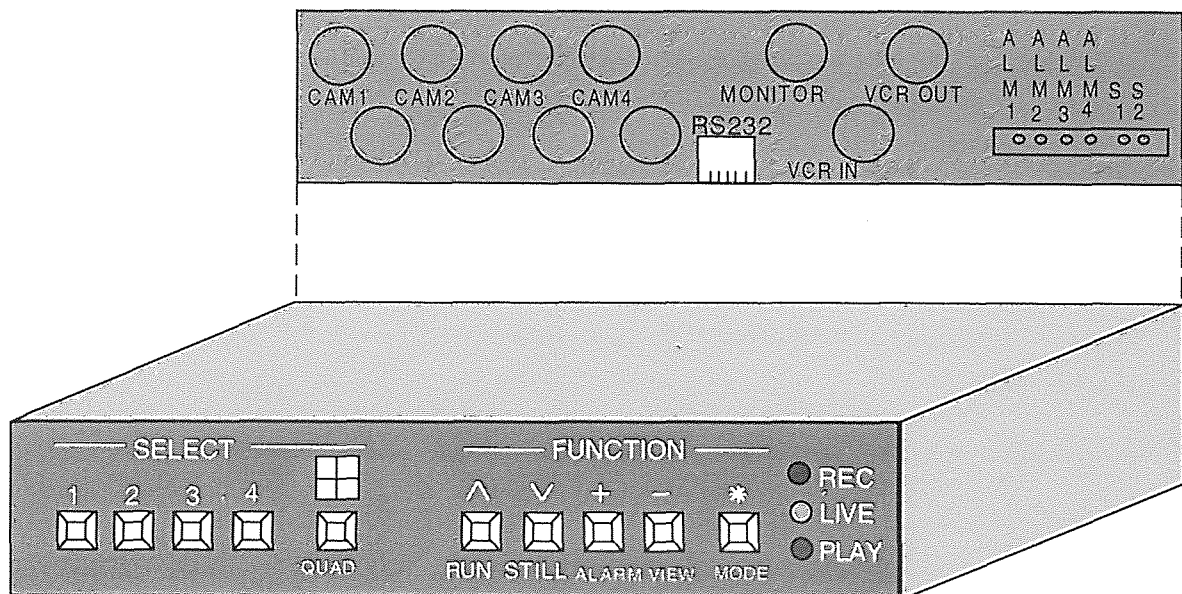


Figure 1.1 Unit Housing

Switching video signals are done through an eight by four analog matrix switch, which is also uses serial communication protocol. This analog matrix switch is controlled from front panel keys and all the communications including switching are controlled via Motorola microcontroller MC68HC11A1.

The some of features are;

- High resolution color display, 256-level gray scale over 16 million colors
- Automatic Gain Control (AGC)
- Password -protected setup program with on screen menus
- manual instant STILL button
- Full screen manual call-up of cameras or Quad display
- Automatic Alarm Call-up of full screen display of alarmed cameras
- alarms are tagged on the tape for easy review during playback
- Alarm logging
- Four alarm inputs and RS-232 remote control capability enhance product flexibility
- Multiple alarms can be sequenced
- Sequencing of Quad display with full-screen displays
- Video-Loss Detection on each video input
- On-screen displays include time, date, video loss indication and camera titles
- User-programmed data is saved in nonvolatile memory (EEPROM)
- Compact cabinet design optimizing the available workspace
- Remote control via RS-232 interface

This Video Multiplexer designed to be expanded from 4 camera switch to 9 and then 16 camera switch multiplexers. All these versions will have the same type of hardware components and software modules to accommodate the design time and expenses for all three products. The main feature of this 4 channel switcher/multiplexer is the use of full scale digital video processing to lower the unit cost.

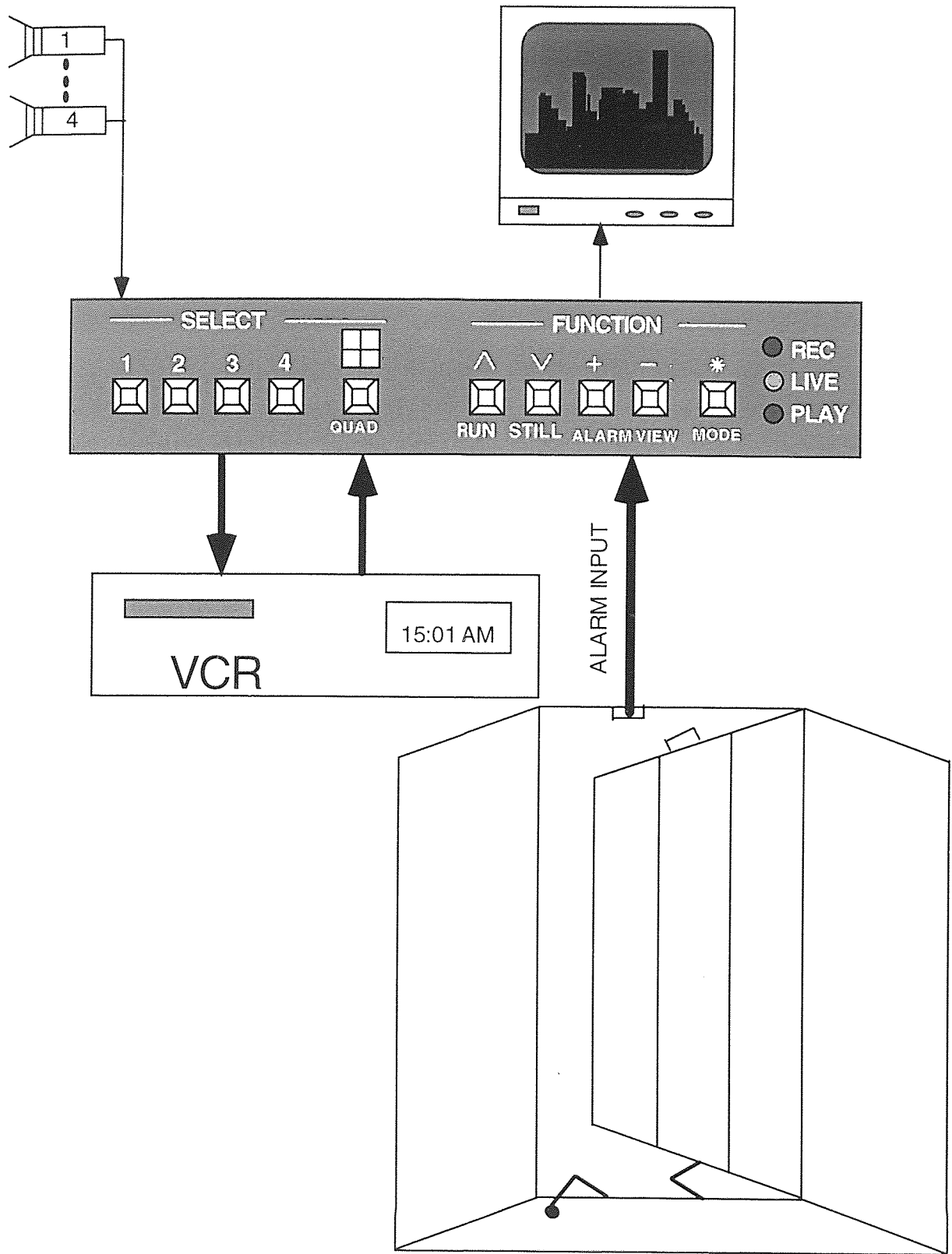


Figure 1.2 System Configuration

CHAPTER 2

HARDWARE

The hardware is designed to be housed in a single rack height, half rack cabinet. The unit will be available configured for desk or rack mounting. The new cabinet design in this unit will eliminate the need for separate top and bottom covers and makes the conversion from desk mount to rack mount as simple as possible. The reason for this kind of cabinet design is, historically the test department at American Dynamics has had the requirement to be able to test and examine both top and bottom of the printed circuit board while in its cabinet. However, because of the evolution in ATE (Automatic Test Equipment) and SMT (Surface Mount Technology) at American Dynamics, this requirement is no longer exists. This new cabinet design will not only play a significant role in helping us reach our cost objectives in the design of Video Multiplexer (V.M.), but will contribute to the cost reduction of existing products that are presently using the old style single rack height, half rack cabinet.

The SMT made us to design the circuit board in four layers. The top layer for surface mount components, the bottom layer for through hole components and middle layer for ground and five volts power supply. The design of this hardware is done on the CAD and the routing of the board is implemented by CAD internal automation and also by CAD operator.

2.1 Hardware Components

2.1.1 Motorola 68HC11A1

The high-density complementary metal-oxide semiconductor (HCMOS) MC68HC11A1 is an advanced 8-bit MCU with highly sophisticated, on-chip peripheral capabilities. New design techniques were used to achieve a nominal bus speed of 2 Mhz. In addition, the fully static design allows operation at frequencies down to dc, further reducing power consumption.

The HCMOS technology used on the MC68HC11A1 combines smaller size and higher speeds with the low power and high noise immunity of CMOS. On-chip memory systems include 256 bytes of random-access memory (RAM), and 512 bytes of electrically erasable programmable ROM (EEPROM).

Major peripheral functions are provided on-chip. An eight-channel analog-to-digital (A/D) converter is included with eight bits of resolution. An asynchronous serial communications interface (SCI) and a separate synchronous serial peripheral interface (SPI) are included. The main 16-bit, free running timer system has three input-capture lines, fine output-compare lines, and real-time interrupt function. An 8-bit pulse accumulator subsystem can count external events or measure external periods.

Self monitoring circuitry is included on-chip to protect against system errors. A computer operating properly (COP) watchdog system protects against software failures. A clock monitor system generates a system reset in case the clock is lost or runs too slow. An illegal opcode detection circuit provides a nonmaskable interrupt if an illegal opcode is detected.

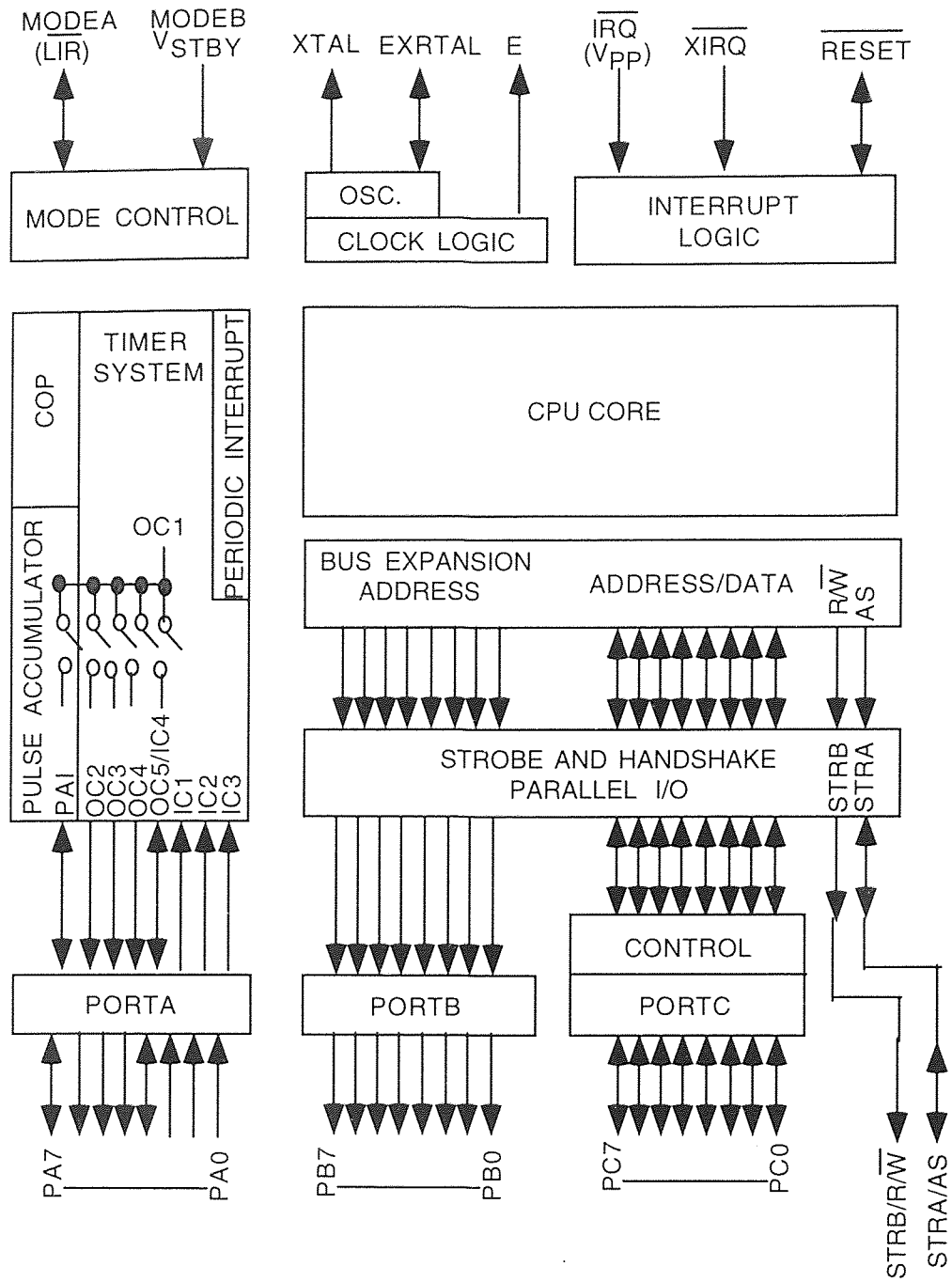


Figure 2.1 Hc11 Interrupt and Timer Block Diagram

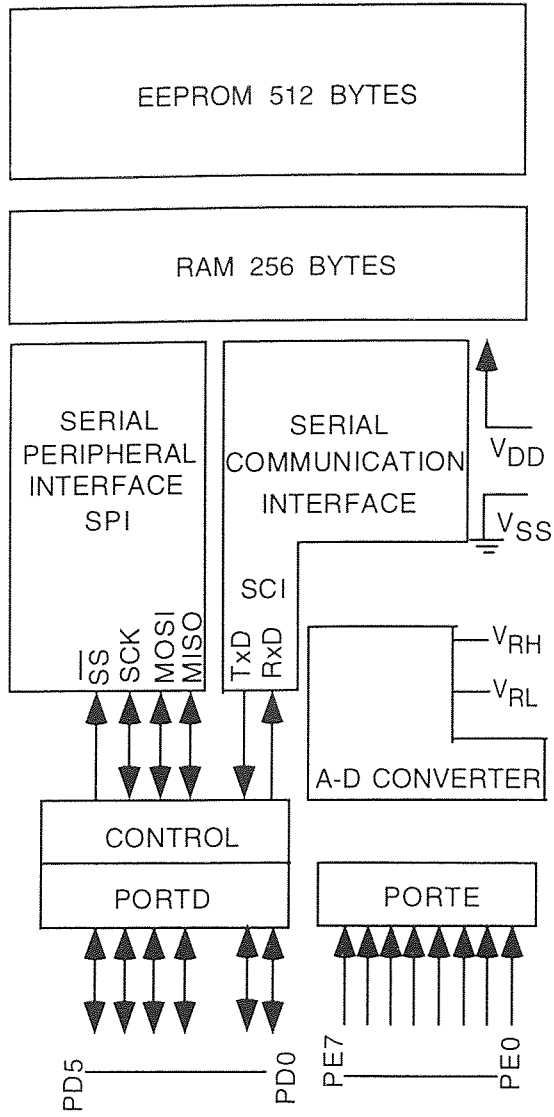


Figure 2.2 Hc11 Communication and Memory Block Diagram

2.2.2 32k External Rom

The NMC27c256 is a high speed 256K UV erasable and electrically reprogrammable CMOS EPROM. The NMC27c256 is packaged in a 28 pin dual in-line package with transparent lid. Two of its most important features are TRI-STATE[®] and single 5V power supply.

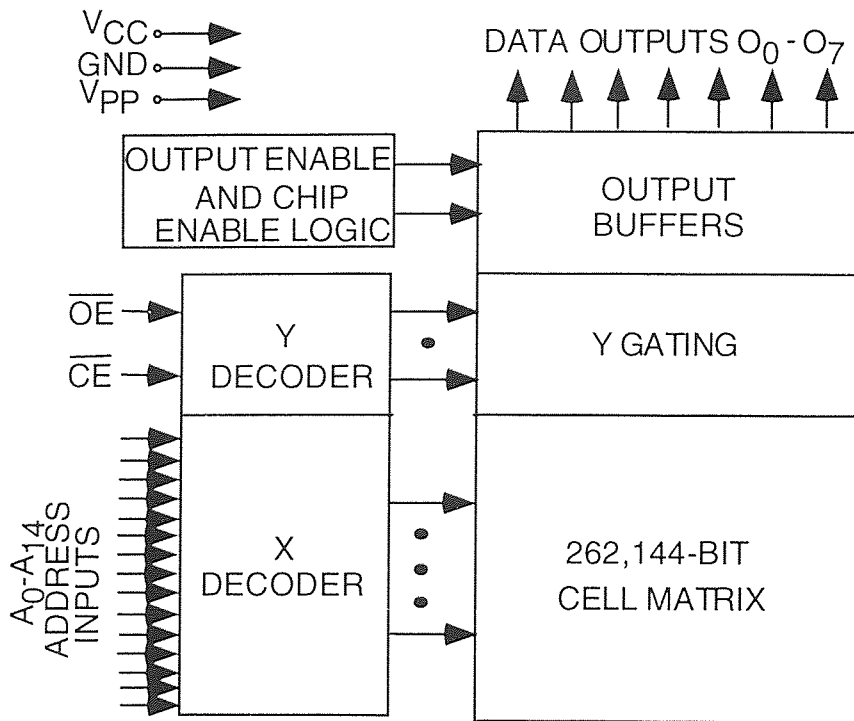


Figure 2.3 NMC27C256 Block Diagram

2.2.3 Brook Tree (BT851, YCrCb or RGB to NTSC/PAL Encoder)

The Bt851 is designed specifically for video systems requiring the generation of 525-line (M) NTSC or 625-line (B, D, G, H, I) PAL composite or Y/C (S-video) video signals.

The Bt851 generates HSYNC (horizontal sync) and VSYNC (vertical sync) outputs. BLANK is an input and may be externally controlled, this external signal produced from PIC Processor called Active Video (Refer to pic processor section). 24-bit

linear RGB data is gamma-corrected and converted to YCrCb. Alternately, 16-bit (4:2:2) YCrCb data may be input directly. The YCrCb is low pass filtered to 1.3 Mhz and modulated. The rise and fall times of sync and the burst envelope are internally controlled.

Analog luminance (Y), and Chrominance (C) information are available on the Y and C outputs for interfacing to S-video equipment. The composite analog video signal is output simultaneously onto both NTSC/PAL analog outputs. This allows one output to provide baseband composite video and another output to drive an RF modulator.

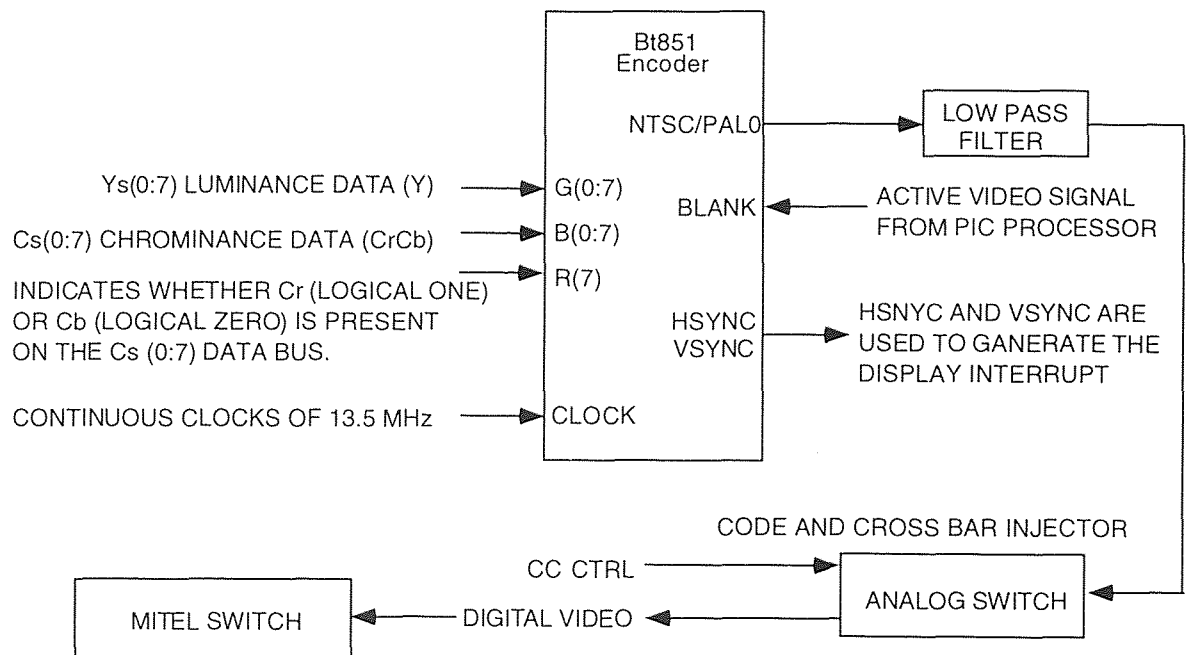


Figure 2.4 Video Encoder Circuit Diagram

2.2.4 BT819, Video Capture Processor for TV/VCR Analog Input

The Bt819 Video Capture Processor is a fully integrated single-chip decoding and scaling solution for analog NTSC/PAL input signals from TV tuners, VCRs, Cameras, and other sources of composite or Y/C video. It is first front-end input solution for low-cost PC video/graphics systems to deliver complete integration and high performance video synchronization, Y/C separation, filtered scaling and optional FIFOed output pixel data. The Bt819 has all the mixed signal and DSP circuitry required to convert an analog composite waveform into a scaled digital video stream supporting a variety of video formats, resolutions and frame rates (The detailed Architectural are discussed in Bt819 section).

2.2.5 Alpha Numeric Generator

The NEC6450 is on-screen character display CMOS LSI which is combined with microcontroller and used for displaying character strings on the monitor screen. Character format is 12 x 18 dots, and one character enables displaying numbers kanji and hiranaga. Since this LSI has built in video switches, video signals can be input and output by composite video signals, and video signals can be generated internally so that characters can be displayed with no external signals. Only three wires are required to communicate with this character generator: 1- STB (strobe), 2- I/O (data line), and 3- CLK (serial clock). Data can be transferred to this IC one character (1 byte) at a time. For this transferring 72 μ sec is a required time.

2.2.6 MicroChip Processor PIC16C56

The PIC16c56 from Microchip Technology is a family low cost, high performance, 8-bit, fully static, EPROM based CMOS microcontrollers. It employs RISC like architecture with only 33 single word/single cycle instructions to learn.

This processor is used in conjunction with other digital Ics to produce signals necessary in digital video to produce digital pictures. One of the conjunction Ics is ASIC processor made by American Dynamics which is basically the production of row and column clocks for DRAM memory. This PIC program basically marks regions of video every 60HZ (16.5 msec) for the hardware; for example the active video portion of the video or the place below active video for storage of data such as alarm bits.

This processor has the ability to synchronize itself with input video signals. This synchronization is accomplished by applying 13.5 Mhz clock to the processor, and on end of each NTSC line the processor clock will be stopped and then restarted at the beginning of each NTSC line. The duration of each NTSC line is 63.5 μ sec, and during this time the PIC processor outputs signals necessary for hardware to produce, store and output digital video.

2.2.7 I²C Bus

The I²C bus is a multimaster bus. This means that more than one device capable of controlling the bus that can be connected to it. The I²C bus is controlled via two lines SDA (serial data line), and SCL (serial clock line). Both SDA and SCL are bi-directional lines, connected to a positive supply voltage via a pull-up resistor. When the line is free both

lines are high. Data on the I²C bus can be transferred at a rate up to 100Kbits/s. The bus capacitance is 400pF.

Bit transfer due to variety of different technology devices (CMOS, NMOS, I²L) which can be connected to the I²C bus, the levels of the logical 0(low) and 1(high) are not fixed and depend on the appropriate level of V_{DD}. One clock pulse is generated for each data bit transferred. For data to be valid the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCL line is low.

2.2.8 Mitel Switch (MT8806 8 x 6 Analog Switch Array)

The mitel MT8806 is fabricated in Mitel's ISO-CMOS technology providing low power dissipation and high reliability. The device contains a 8x4 array of crosspoint switches along with 5 to 32 line decoder and latch circuits. Any one of the 32 switches can be addressed by selecting the appropriate five address bits. The selected switch can be turned on or off by applying a logical one or zero to the DATA input. V_{SS} is the ground reference of the digital inputs. The range of analog signal is from V_{DD} to V_{EE}. Chip Select (CS) allows the crosspoint array to be cascaded for matrix expansion.

2.2.9 Dallas Semiconductor (DS1202 Serial Timekeeping Processor)

The DS1202 Serial Timekeeping Chip contains a real time clock/calendar and 24 bytes of static RAM. It communicates with a microprocessor via a simple serial interface . The real time clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with less than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with an AM/PM indicator. Interfacing the DS1202 with a

microprocessor is simplified by using synchronous serial communication. Only three wires are required to communicate with the clock/RAM: 1- /RST (reset), 2- I/O (data line), and 3- SCLK (serial clock). Data can transferred to and from the clock/RAM one byte at a time or in a burst of up to 24 bytes. The DS1202 is designed to operate on a very low power and retain data and clock information on less than 1 microwatt.

2.2.10 Silicon Gate Cmos 262,144 Words by 8 Bits Multiport Dram

The Tc582257 is a 2M bit CMOS multiport memory equipped with a 262,144 words by 8 bits dynamic random access memory port and a 512 words by 8 bits static serial access memory port (SAM). The TC52857 supports three types of operations; Random access to and from the RAM port, high speed serial access to and from the SAM port and bi-directional transfer of data between any selected row in the Ram and the SAM. The diagrams on the next pages shows the use of this device.

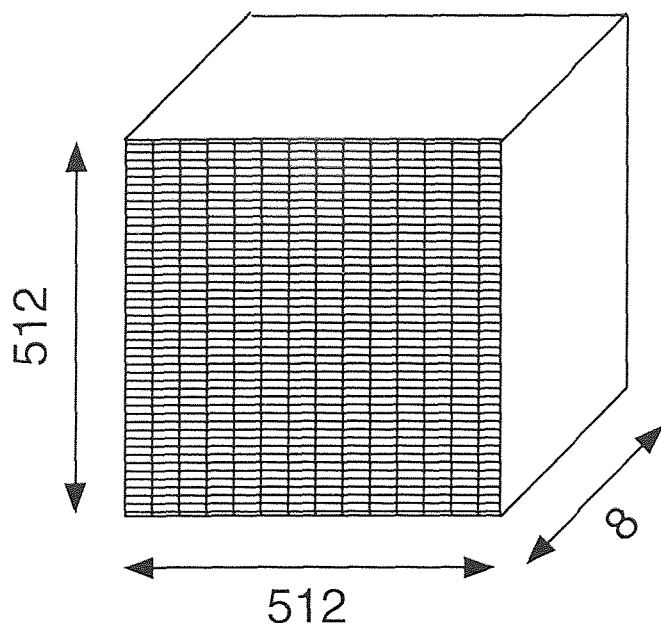
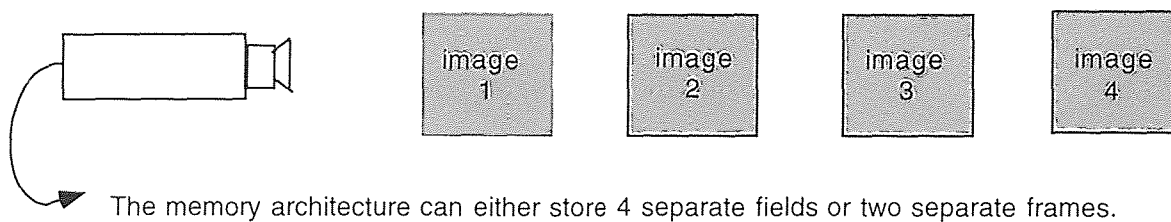


Figure 2.5 Single Dual Port Dram

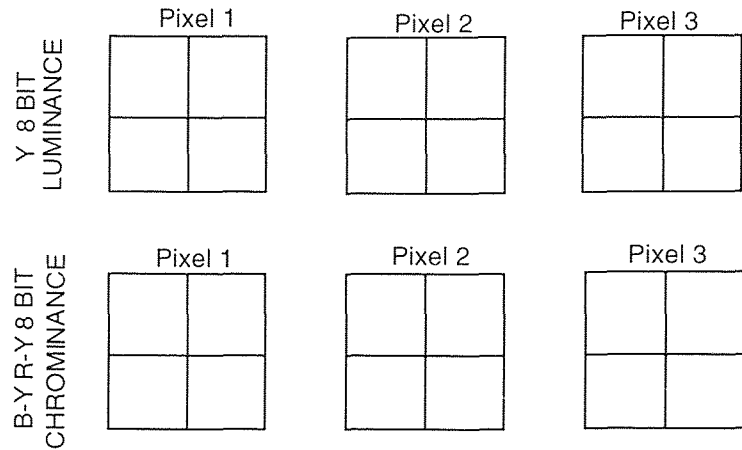
Memory array size is 6 Dual Port Drams = 12,582,912 bits



The memory architecture can either store 4 separate fields or two separate frames.

Figure 2.6 Image Storage

For each physical address there are three corresponding pixels,
 240 addresses by 3 pixels = 720 active pixels



The black area is the unwritten part of the memory
 Horizontally there are 512 addresses in which 480 are used (93.8%) in NTSC mode
 Vertically there are 512 addresses in which 482 are used (94.1%). in NTSC mode

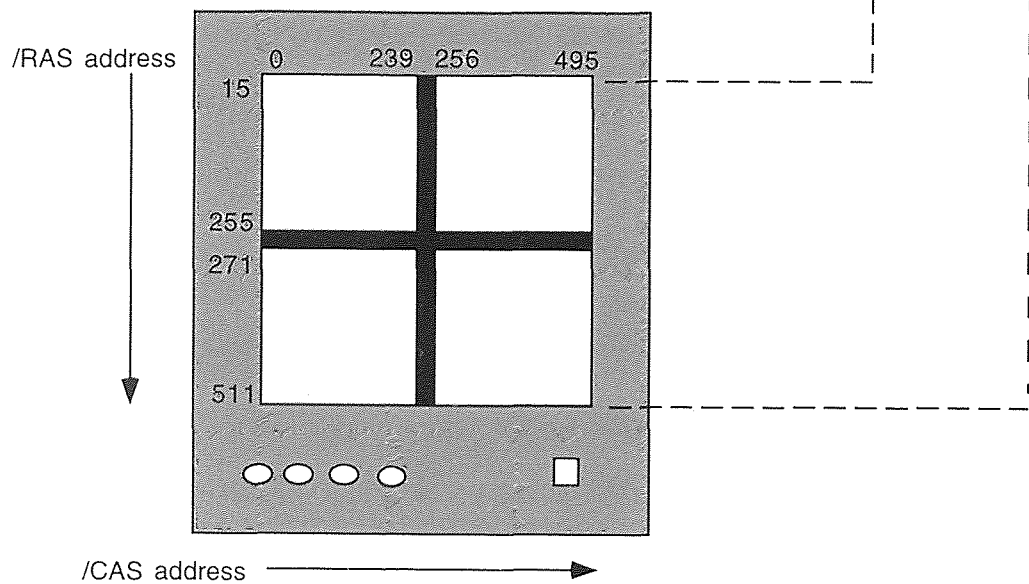


Figure 2.7 Memory Storage Locations

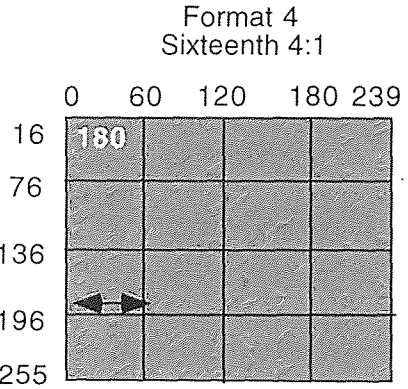
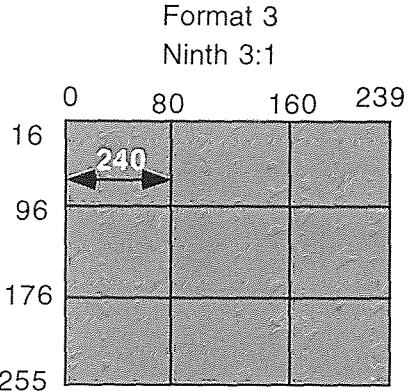
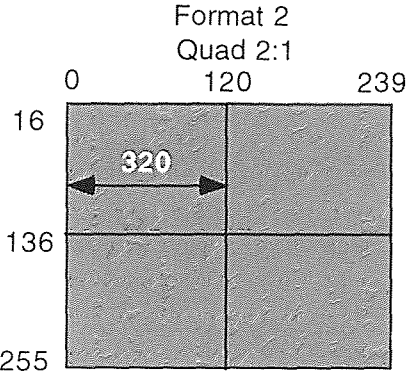
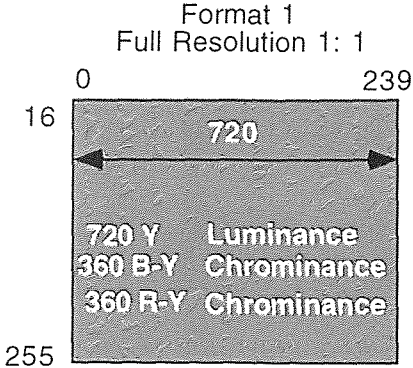


Figure 2.8 Horizontal and Vertical Address Map for Formats 1 Through Format 4

CHAPTER 3

SOFTWARE

Software design in this product is separated into different modules and generalized functions. This software set tried to implement the idea of Object Oriented Programming (Oops) to simplify the use of modules. Module groups are separated to hardware and pure software groups. One of the features of this program is the use of Array of function pointers. The reason is the ability to use the software set for 9 and 16 channel by a few modification to hardware modules. These array of function pointers are based on the functionality of front panel keys in different modes.

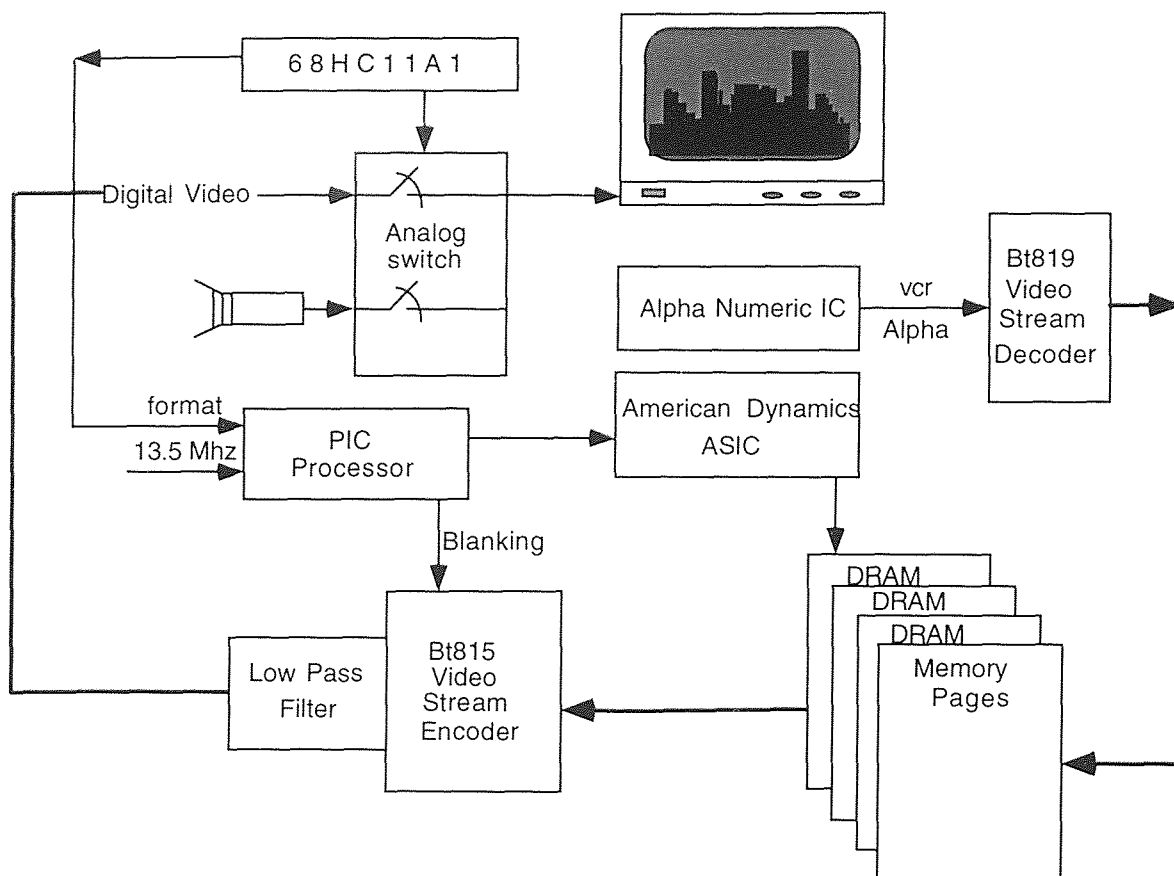


Figure 3.1 Digital Video Production Diagram

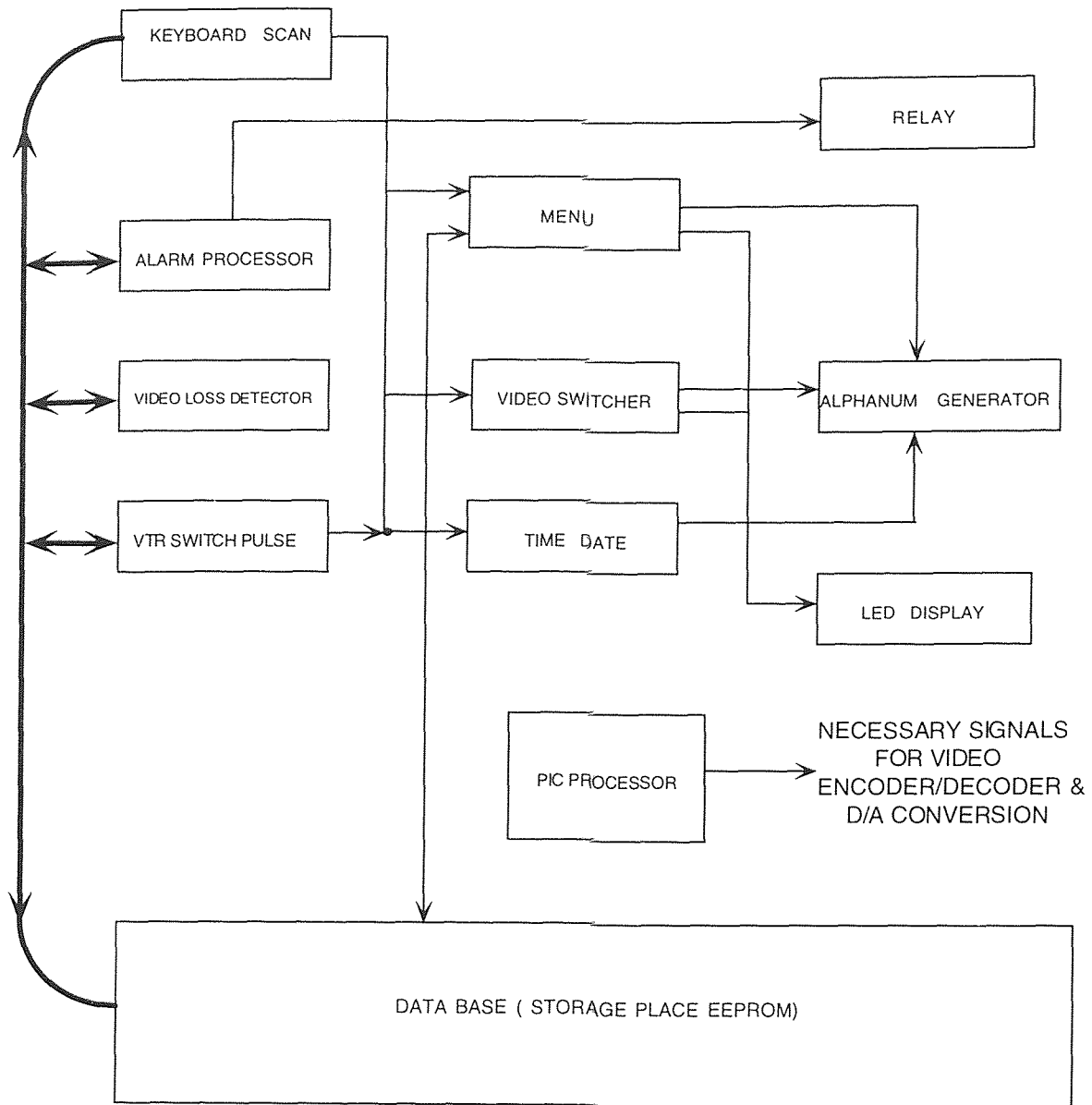


Figure 3.2 Software Block Diagram

3.1 Modes of Operation

This multiplexer as described earlier has three modes of operation (LIVE, PLAY, and RECORD). These modes are shown in the next few diagrams. PLAY and LIVE modes are similar, except for that fact that in LIVE mode the inputs to the system are from live input cameras, and in the PLAY mode the input is from a video tape recorder.

3.1.1 Live Mode

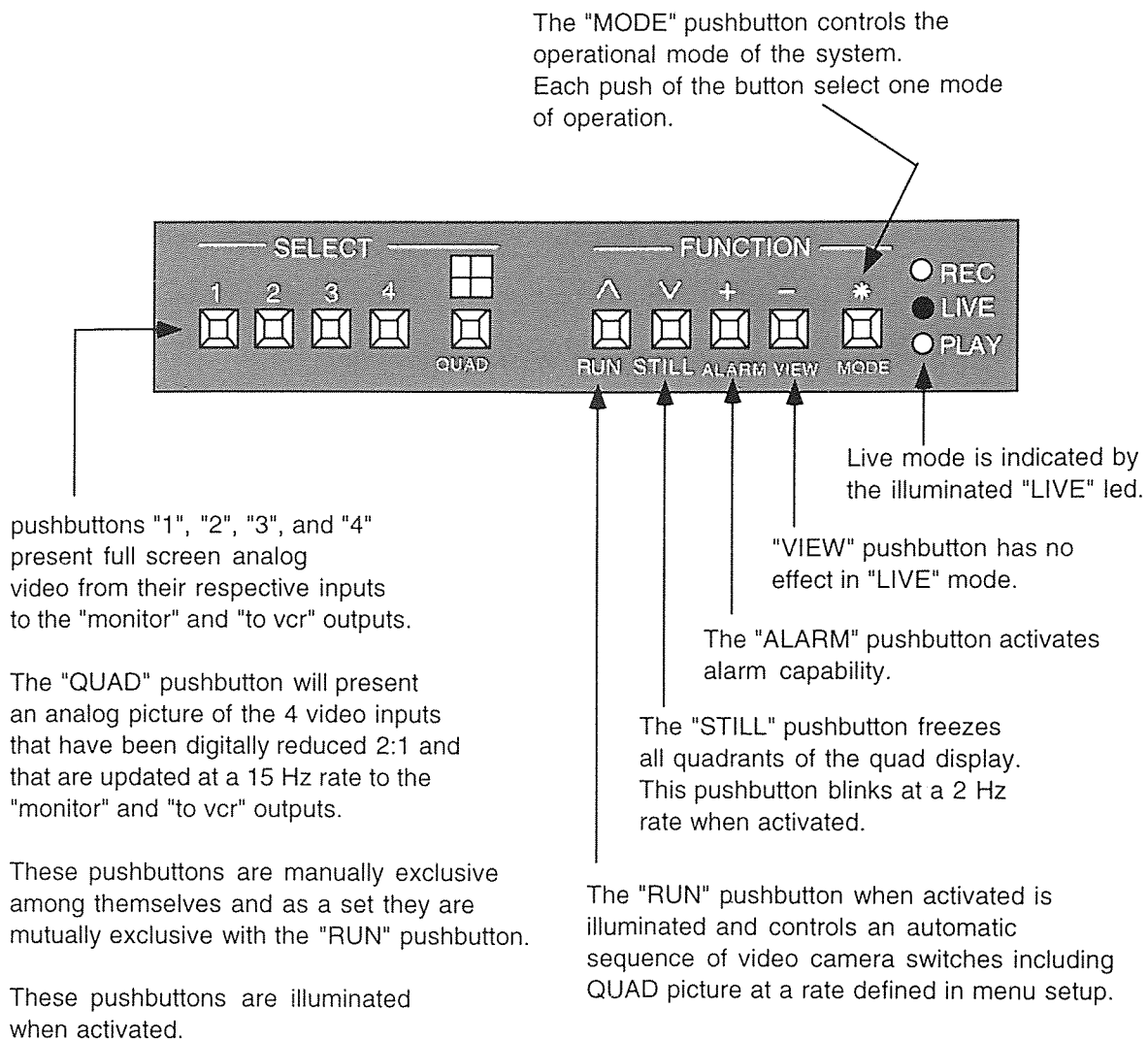


Figure 3.3 Front Panel in Live Mode

3.1.2 Play Mode

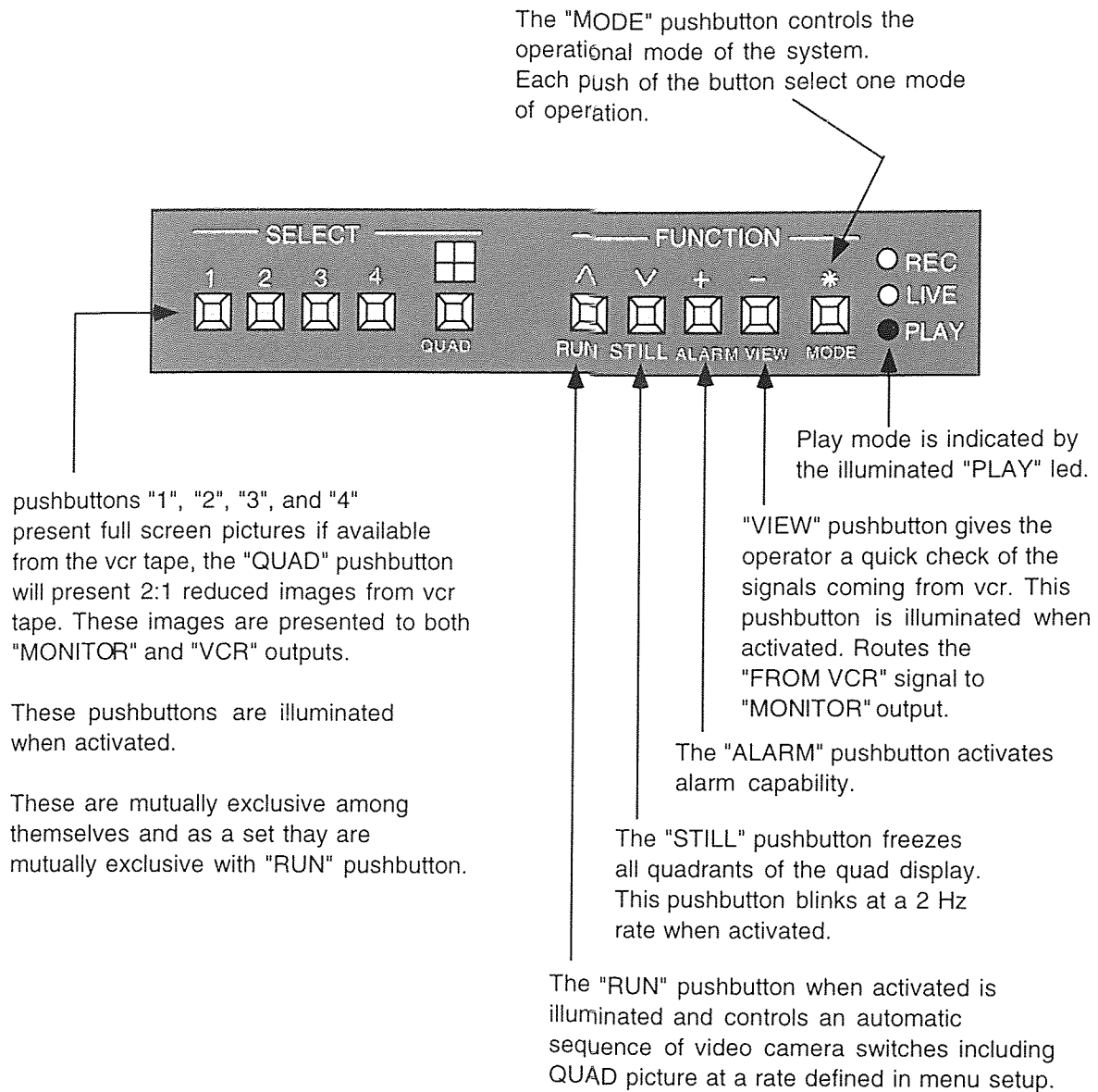


Figure 3.4 Front Panel in Play Mode

3.1.3 Record Mode

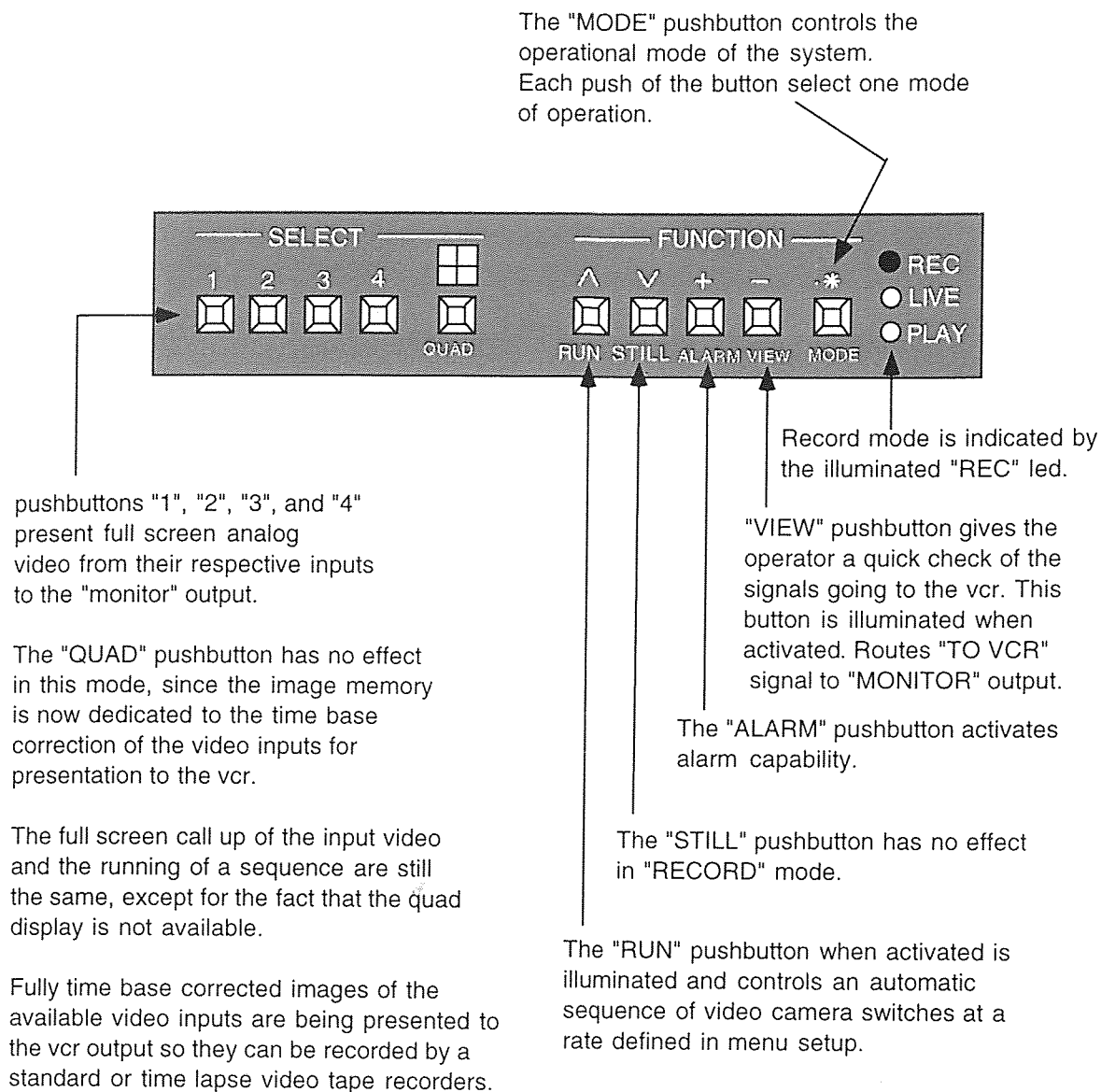


Figure 3.5 Front Panel in Record Mode

3.2 Power Loss

A number of system variables will have to be preserved to survive a power loss. These variables will all be grouped into a single structure, with a typedef declaring it as a data type called POWERLOSS. This POWERLOSS data structure will be written to EEPROM or read from EEPROM as required.

The elements of the POWERLOSS data structure will be :

```
enum SQUARETYPES { SQ_FULL, SQ_FOUR, SQ_NINE, SQ_SIXTEEN };  
  
enum OPERATINGMODES { OP_LIVE, OP_RECORD, OP_PLAYBACK };  
  
typedef struct {  
    unsigned running : 1;          /* Running Camera Sequence */  
    unsigned squares : 2;         /* assigned SQUARETYPES */  
    unsigned opmode : 2;          /* assigned OPERATINGMODES */  
    unsigned alarm_armed : 1;     /* boolean */  
    unsigned camera_number : 4; /* int */  
} POWERLOSS;
```

3.3 Factory Reset

The multiplexer can be returned to a condition where all programmable features of the machine can be returned to a default condition. This is called Factory Reset because it is the way the machine is programmed when it is packed for shipping.

A user can factory reset the multiplexer by holding the ALARM button down and cycling AC power. The user can release the ALARM button, 1 second after the power has been applied. The re-programming of the defaults may take longer than 1 second. The reason for this delay is the actual time required for the Factory Table be written to EEPROM in Hc11. As indicated below the actual size of this table is array of 397 bytes.

```
char const FactoryTable[397] = {
/* MENU 10 (0..1)      */ 0,1
/* MENU 0 (2..4)      */ 20,24,24
/* MENU 3 (5)         */ 21, /****** 3rd entey *****/
/* MENU 1 (6..7)      */ 2,3
/* MENU 2 (8..23)     */ 15,15,15,15,15,15,15,15,15,15,15,15,15,15,15
/* MENU 3 (24..25)    */ 8,11
/* MENU 4 (26)        */ 1
/* MENU 5 (27..40)    */ 'C','A','M','E','R','A',' ','1',' ',' ',' ',' ','4,6
/* MENU 6 (41..54)    */ 'C','A','M','E','R','A',' ','2',' ',' ',' ',' ','4,6
/* MENU 7 (55..68)    */ 'C','A','M','E','R','A',' ','3',' ',' ',' ',' ','4,6
/* MENU 8 (69..82)    */ 'C','A','M','E','R','A',' ','4',' ',' ',' ',' ','4,6
                      (83..96) */ 'C','A','M','E','R','A',' ','5',' ',' ',' ',' ','4,6
                      (97..110) */ 'C','A','M','E','R','A',' ','6',' ',' ',' ',' ','4,6
                      (111..124) */ 'C','A','M','E','R','A',' ','7',' ',' ',' ',' ','4,6
                      (125..138) */ 'C','A','M','E','R','A',' ','8',' ',' ',' ',' ','4,6
                      (139..152) */ 'C','A','M','E','R','A',' ','9',' ',' ',' ',' ','4,6
                      (153..166) */ 'C','A','M','E','R','A',' ','10',' ',' ',' ',' ','4,6
                      (167..180) */ 'C','A','M','E','R','A',' ','11',' ',' ',' ',' ','4,6
                      (181..194) */ 'C','A','M','E','R','A',' ','12',' ',' ',' ',' ','4,6
                      (195..208) */ 'C','A','M','E','R','A',' ','13',' ',' ',' ',' ','4,6
                      (209..222) */ 'C','A','M','E','R','A',' ','14',' ',' ',' ',' ','4,6
                      (223..236) */ 'C','A','M','E','R','A',' ','15',' ',' ',' ',' ','4,6
                      (237..250) */ 'C','A','M','E','R','A',' ','16',' ',' ',' ',' ','4,6

/* MENU 9 (251)      */ 18,
/* MENU 10 (252)     */ 3, /****** 3rd entry *****/
```


NOTE: This part of the table specify the location of log tables in EEPROM and possible values to store. In case of no entry the locations should have value of 0x20 (' '). The values from memory is copied line by line to dwell[0]..dwell[6], dwell[7] holds the value of pages[1..4] defined at top under MENU 5.

EEPROM start location for log tables = 253

Length of each line = 7 bytes

One line on each page might contain camera number, time and date.

offset from one page to other = $5 * 7 = 35$ bytes

PAGE 1:

(253..259) 0x20,0x20,0x20,0x20,0x20,0x20,0x20
 (260..266) 0x20,0x20,0x20,0x20,0x20,0x20,0x20
 (267..273) 0x20,0x20,0x20,0x20,0x20,0x20,0x20
 (274..280) 0x20,0x20,0x20,0x20,0x20,0x20,0x20
 (281..287) 0x20,0x20,0x20,0x20,0x20,0x20,0x20

PAGE 2:

(288..294) 0x20,0x20,0x20,0x20,0x20,0x20,0x20
 (295..301) 0x20,0x20,0x20,0x20,0x20,0x20,0x20,
 (302..308) 0x20,0x20,0x20,0x20,0x20,0x20,0x20,
 (309..315) 0x20,0x20,0x20,0x20,0x20,0x20,0x20,
 (316..322) 0x20,0x20,0x20,0x20,0x20,0x20,0x20,

PAGE 3:

(323..329) 0x20,0x20,0x20,0x20,0x20,0x20,0x20,
 (330..336) 0x20,0x20,0x20,0x20,0x20,0x20,0x20,
 (337..343) 0x20,0x20,0x20,0x20,0x20,0x20,0x20,
 (344..350) 0x20,0x20,0x20,0x20,0x20,0x20,0x20,
 (351..357) 0x20,0x20,0x20,0x20,0x20,0x20,0x20,

PAGE 4:

(358..364) 0x20,0x20,0x20,0x20,0x20,0x20,0x20,
 (365..371) 0x20,0x20,0x20,0x20,0x20,0x20,0x20,
 (372..378) 0x20,0x20,0x20,0x20,0x20,0x20,0x20,
 (379..385) 0x20,0x20,0x20,0x20,0x20,0x20,0x20,
 (386..392) 0x20,0x20,0x20,0x20,0x20,0x20,0x20,

PASSWD MENU (393..396) 17,17,17,17
};

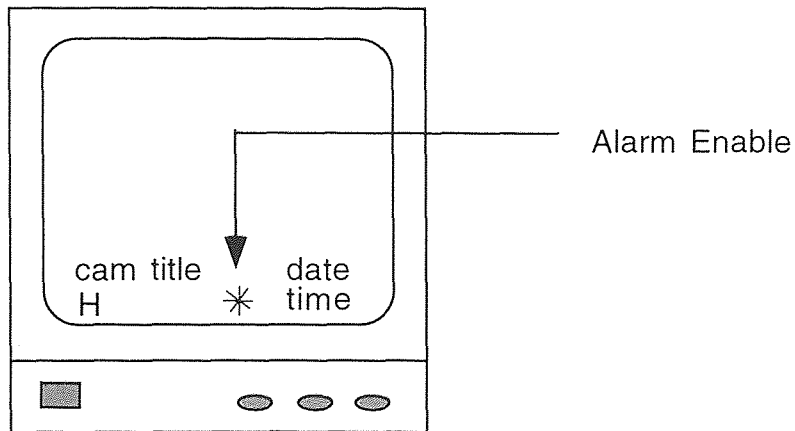
3.4 Alarm Section

3.4.1 Alarm Inputs

These inputs are from a latch based on address decoding, called alarm_latch.

3.4.2 Alarm Enable/ Disable

The ability of this multiplexer is to react to alarm conditions can be enabled or disabled by toggling the front panel alarm button. The LED associated with the front panel alarm button will be on when alarms are enabled, and will be off when alarms are ignored. This enabling indicated on the bottom screen by *



3.4.3 Alarm Package

This package is implemented based on American Dynamics main switcher alarm design, which used link list to implement the alarm algorithm. Let us explain this algorithm through examples.

Example 1: Imagine that three alarms read by scan routine and passed on to software alarm algorithm to place for further evaluation. This software routine first ask to see if alarm for particular camera exists or not. If alarm is new places the alarm in the SEQ (sequence) table following Link List algorithm in this manner;

If alarm 3, 4 and 6 activated,

example 1.1: alarm 3 activated; last alarm = &seq[3]; sequencer = &seq[3].

alarm 4 activated while 3 on; last alarm = &seq[4]; sequencer =
&seq[4]; seq[3] = 4; seq[4] = 3.

alarm 6 activated while sequencer = &seq[4]; last alarm = &seq[6];
sequencer = &seq[6]; seq[4] = 6; seq[6] = 3;

SEQ[8..16]:

```

0  1  2  3  4  5  6  7  8    <----- Alarm to display
-----
|  |  |  | 4 | 6 |  | 3 |  |  |    <----- Next alarm to display
-----

```

example 1.2: alarm 3 activated; last alarm = &seq[3]; sequencer = &seq[3].

alarm 4 activated while 3 on; last alarm = &seq[4]; sequencer =
&seq[4]; seq[3] = 4; seq[4] = 3.

alarm 6 activated while sequencer = &seq[3]; last alarm = &seq[6];
sequencer = &seq[6]; seq[3] = 6; seq[6] = 4;

SEQ[8..16]:

```

0  1  2  3  4  5  6  7  8    <----- Alarm to display
-----
|  |  |  | 3 | 6 |  | 4 |  |  |    <----- Next alarm to display
-----

```

These two examples showed that the property of Link List is maintained and the sequencing and displaying the current alarm is maintained as the new alarm forced into the sequence list.

This algorithm permits us to write separate modules or libraries for future products by simply writing the alarm scan routine part that is customized to individual

hardware, and reads individual alarms. In this product these alarms are maintained on an external input latch called Alarm_Latch.

3.4.4 Alarm List Algorithm

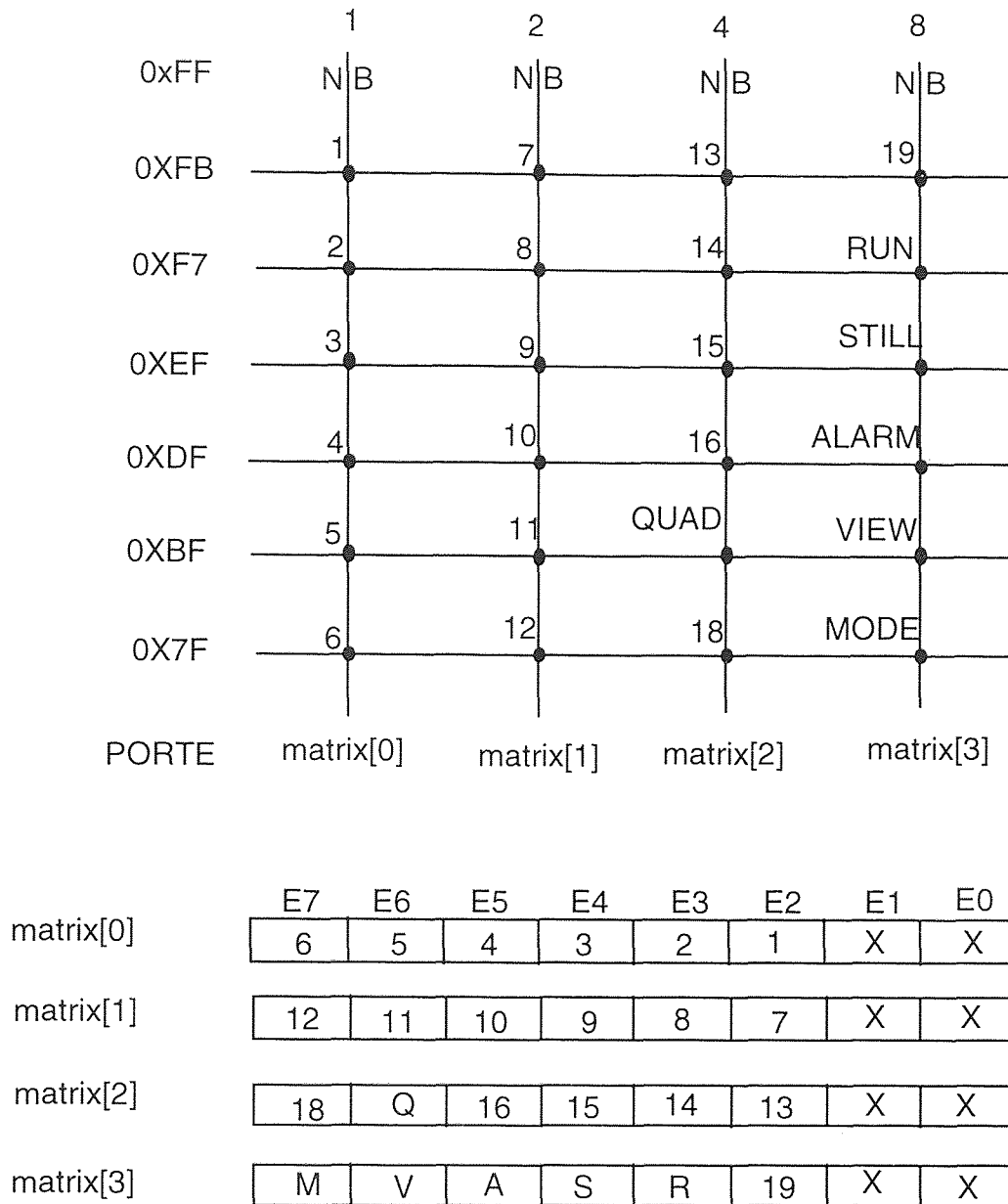
This multiplexer supports an **Alarm Log**. This alarm log is a list of the 20 alarms which have been detected by the machine. Each alarm log entry will be a 7 byte record containing 1 byte of camera number and 6 bytes which contain the packed BCD representation of the time and date of the alarm as read from the on-board time and date chip. This log list is viewable through the menu system. The alpha-numeric display in the multiplexer will allow up to 5 alarm logs per screen, so the alarm log menu will be divided into 4 pages. The next viewable log page can viewed if any data exists on that page, also each page indicates if user can go to next page. The last alarm log display includes an option to **Clear Alarm Log Pages**. This function is available only to last page of the log display. Choosing to clear the alarm list clears all 20 entries in the alarm log and adjust the screen to first alarm list and display empty screen.

3.5 Front Panel Input

The front panel of the 4 channel device has 10 pushbuttons and 10 LED's. The front panel of the 9 channel device has 16 buttons and 16 LED's, and the 16 channel device has 23 switches and 23 LED's. The software developed for this system will use a lookup table to map these actual switches to logical key legends which will always have the same index number no matter what device the software is for. The non-changing key legend values will be obtained from the front panel of the proposed 16-channel device, starting at the leftmost button, assigning it the value one, then from left to right, assigning ascending order to each button. This numbering system will then be applied to all the devices, so that for example the QUAD button will always be number 17, even in a device which has only 10 switches. This key number assignment is described in an ENUMerated data type declaration :

```
enum KEYCONSTANTS {  
    KCAM1 = 1, KCAM2, KCAM3, KCAM4,  
    KCAM5, KCAM6, KCAM7, KCAM8,  
    KCAM9, KCAM10, KCAM11, KCAM12,  
    KCAM13, KCAM14, KCAM15, KCAM16,  
    KQUAD, KNINE, KSIXTEEN, KRUN,  
    KSTILL, KALARM, KVIEW, KMODE  
};
```

Table 3.1 Key Pad Matrix Switches



The keyscanning routine will be responsible for returning values in the enumerated set.

3.6 Video Sequences and Switches

3.6.1 Mitel Switches and Memory Maps

The 4 channel device will be using the MITEL MT8806 8 X 4 Analog Switch Array. We will consider the 8 Y pins of the device to be inputs, and the 4 X pins of the device to be outputs. The AD1582 4-channel MUX will have 6 of the Y inputs connected to the D/A video converter, the VCR, and the 4 camera videos, and 3 of the 4 X outputs connected to the A/D video converter, the video loss Sampler, and the user monitor. We can think of the MT8806 as providing a 6 X 3 crosspoint for our purposes.

Memory Mapping: -

The lower 8-bits of the memory map for the Mitel are as follows:

xxxAAABB

Where AAA = Input Camera Number and BB = Output Channel Number. The base address is currently 0x3200 and is called /DECODE3. Combining the base address with the lower byte encoding produces the address of the switch required. To close a crosspoint, write a '1' to the address, to clear the crosspoint write a '0'.

Since the IC is a crosspoint switch, and the input and output assignments above are only logical concepts, we have to be careful in how the switch is used. The following rules apply when using this crosspoint switch.

1 - A single input can be connected to all 3 outputs. Example: Camera #1 video can be connected to the display monitor, to the videoloss sampler, and to the A/D video converter. 2 - No single output can have more than one input connected. Example:

Camera #1 and camera #2 cannot both be connected to the display monitor. This appears on the monitor as the sum of the two videos.

3 - All requests to connect an input Y to an output X must do it in steps:

- a) check to see if Y is already connected to X.
- b) If Y is not connected to X, the current connection to X must be broken and then the new connection can be made.
- c) If Y is connected already to X, then refuse the request.

4 - A bitmap of the current switch state must be maintained to support the requirements of #3 above.

3.6.2 Video Sequencing

Sequences are automatic camera switches executed by the cpu in the multiplexer based on a timing parameter called a DWELL time. The dwell time is programmed through the menu system. There is one dwell time, which is applied to all cameras in the SEQUENCE LIST. The sequence list in the programming menu is used to include or exclude cameras in the sequence. The sequence can also contain a MULTIVIEW picture. The selection of the type of multiview picture is not programmable, but is chosen by the multiplexer software using an algorithm called Largest_Viewable_Multiscreen. This inclusion of the multiview picture is programmed from the menu system.

3.7 Video Loss Detection / Automatic Gain Control

Video Loss (VL) and Automatic Gain Control (AGC) will be combined functions which both use data collected from a single source. The data source for these two functions is the A/D conversion of each of the camera video signals available to the machine. The A/D conversion is done in the HC11 using the on-board 8-bit converter. The V_{rh} of the system will be 5.0 V, and the V_{rl} of the system will be 0.0 V . The VL/AGC data collection routine will maintain an array of the digitized camera videos (8-bits) and use the data to interpret VL and AGC actions.

3.7.1 Video Loss

Video Loss is sampled on hc11 portE , channel 1. The rate of sampling is not critical, and once per second is satisfactory.

For each video channel, switch the desired video input to the Video Switch channel C. This connects the desired video to the video loss circuit. The Video Loss Circuit is a sync stripper and an RS flip-flop (RSFF). The microprocessor has an output to the Reset of the RSFF, and an analog input from the Q output of the RSFF.

The video loss algorithm is

- 1- Switch desired video to Video Switch channel 3 output.
- 2 - Write a zero to the RSFF Reset pin.
- 3 - Write a 1 to the RSFF output pin.
- 4 - Perform a A/D conversion on the Q output of the RSFF.
- 5 - Analyze: If conversion result is $> 1/2 V_{cc}$, then assume a video signal is present
Else assume a video signal is absent.

6 - Mark a bit in a bit array. Bits == 1 mean Video Is Present

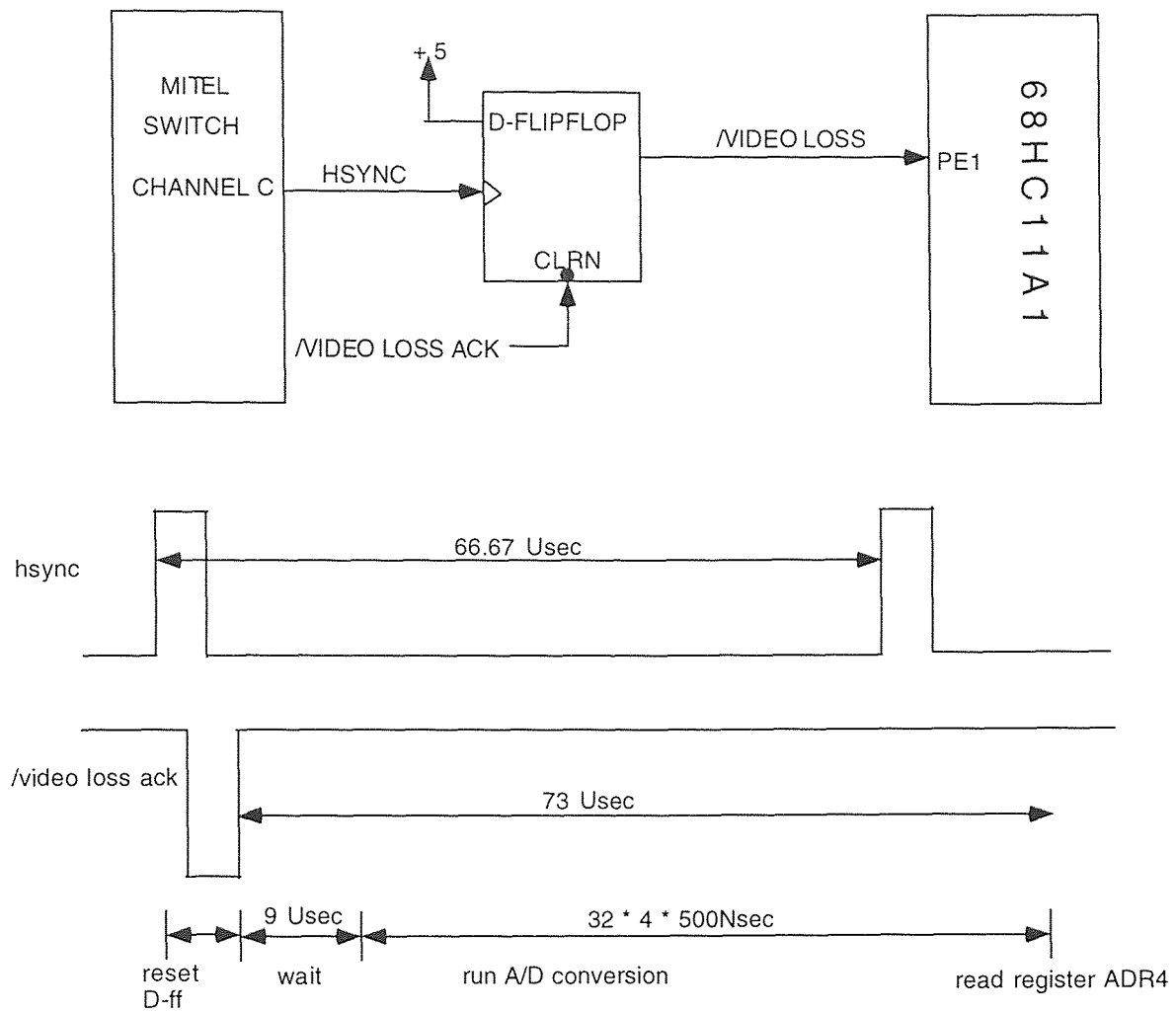


Figure 3.6 Video Loss Diagram

Specific Implementation:

The function for video loss will be called `boolean HasVideo(int channelnum)`

which will encapsulate this hardware sequence and return `TRUE` or `FALSE`.

The specific hardware implementation of this for the 4 channel device is

1- Clear all connections in Mitel switch (`/DECODE3 @ 3200`) . Set the connection for the channel number .

2 - `/DECODE12 (u103), D6 = 0;` (Hold Reset of FF down)

3 - `/DECODE12 (u103), D6 = 1;` (release Reset of FF)

4 - convert `hc11.porte` channel 1;

Report of video loss.

When a report is required,

- The internal raster to character generator will be switched on.
- The Mitel switch will be updated.
- The `VIDEOLOSS_MESSAGE` will be written to the display.

3.8 AGC Algorithm

The AGC routine will be to sample hc11 portE d0. For the moment, the answers will be stored in an array of 4 characters. To obtain the video, switch the video channel to be sampled to the Video switch output channel A. If you have done a normal switch then this has already been done.

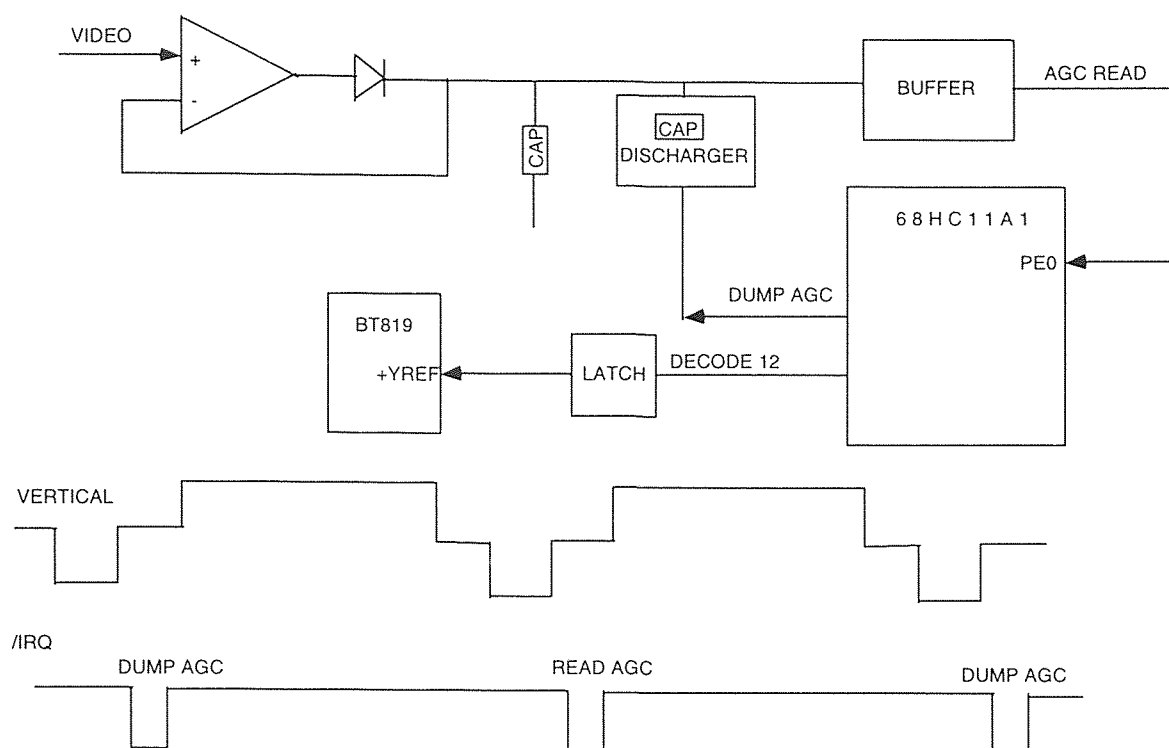


Figure 3.7 AGC Block Diagram

Experimental IRE values were run and recorded on the tables below. The IRE values are supplied by the signal generator and corresponding ADC and Q0-Q3 values at HC11 and Bt819 were measured.

Dump agc is implemented every 30 msec (every other vertical time) as well as AGC read as shown in the diagram above. Agc read is digitized value of incoming video peak and dump agc is the circuit that resets the peak detector circuit. Values are transferred to

Bt819 via an 8-bit latch to change the level of +YREF on Bt819 based on AGC read value & lookup tables (if-then-else statements).

Table 3.1 Bt819 Input Value vs DAC Output

Q0 - Q3 to BT819	STEP	DAC out	Delta V
0000	0	0.981	
0001	1	1.042	61 mv
0010	2	1.097	55 mv
0011	3	1.158	61 mv
0100	4	1.233	75 mv
0101	5	1.294	61 mv
0110	6	1.349	55 mv
0111	7	1.410	61 mv
1000	8	1.458	48 mv
1001	9	1.519	61 mv
1010	10	1.574	55 mv
1011	11	1.635	61 mv
1100	12	1.710	75 mv
1101	13	1.771	61 mv
1110	14	1.825	54 mv
1111	15	1.887	62 mv

Table 3. 2 IRE Level vs ADC Read at Main Processor

IRE LEVEL	AGC READ VOLTS	Delta V	ADC READ at HC11
0	0.584		11
10	0.653	69 mv	21
20	0.724	71 mv	30
30	0.795	71mv	40
40	0.866	71mv	49
50	0.936	70 mv	59
60	1.008	72mv	68
70	1.079	71 mv	77
80	1.150	71 mv	87
90	1.222	72 mv	96
100	1.293	71 mv	106
110	1.364	71 mv	115
120	1.435	71 mv	125
130	1.506	71 mv	134
140	1.577	71 mv	144
150	1.648	71 mv	153
160	1.719	71 mv	163
170	1.790	71 mv	172
180	1.861	71 mv	182

3.9 Time and Date Ic

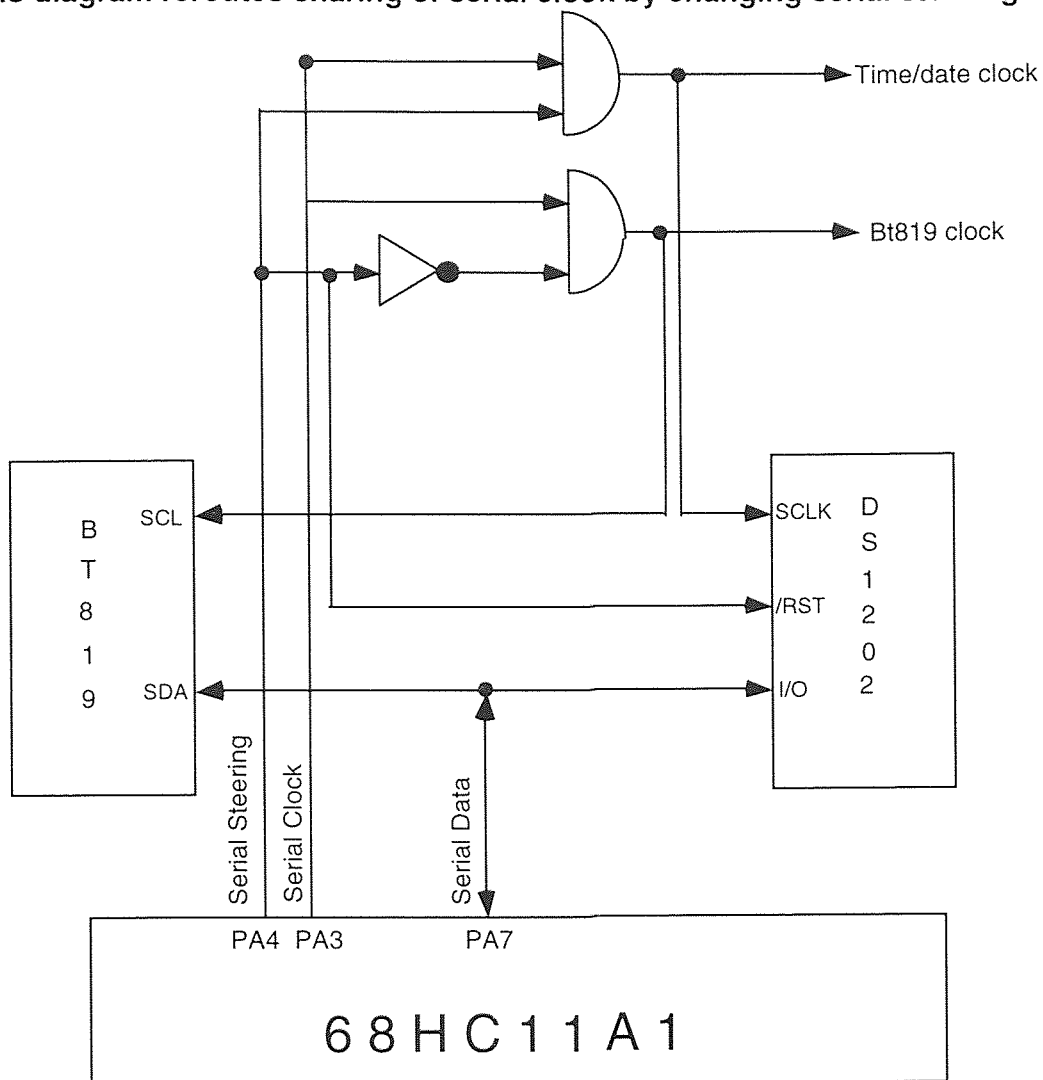
The IC chosen for maintaining time and date is the Dallas DS1202. This device has a bi-directional serial interface. There may be some conflict with other serial devices in the system. The DS1202 has been used in other American Dynamics line of products. The code is written in assembly and contains functions that can be called from C program. Three signals are required to communicate with DS1202; /RST, SCLK, and I/O. These are implemented in the AD1582 as :

/RST is	PA4
SCLK is	PA3
I/O is	PA7

When not communicating with the DS1202, you must hold the /RST signal low. This steers the I/O wire and the SCLK wire to the Brooktree Bt819.

According to Dallas Semiconductor the DS1202 has a software bug such that if the seconds register is initialized to 59, the minutes register will not increment until the seconds has counted through 60 seconds again.

This diagram reroutes sharing of serial clock by changing serial steering bit.



Note: To talk to DS1202 Serial Steering must be high.
To talk to BT819 Serial Steering must be low.

Figure 3.8 Serial Steering

OVERALL CLOCK PROGRAM

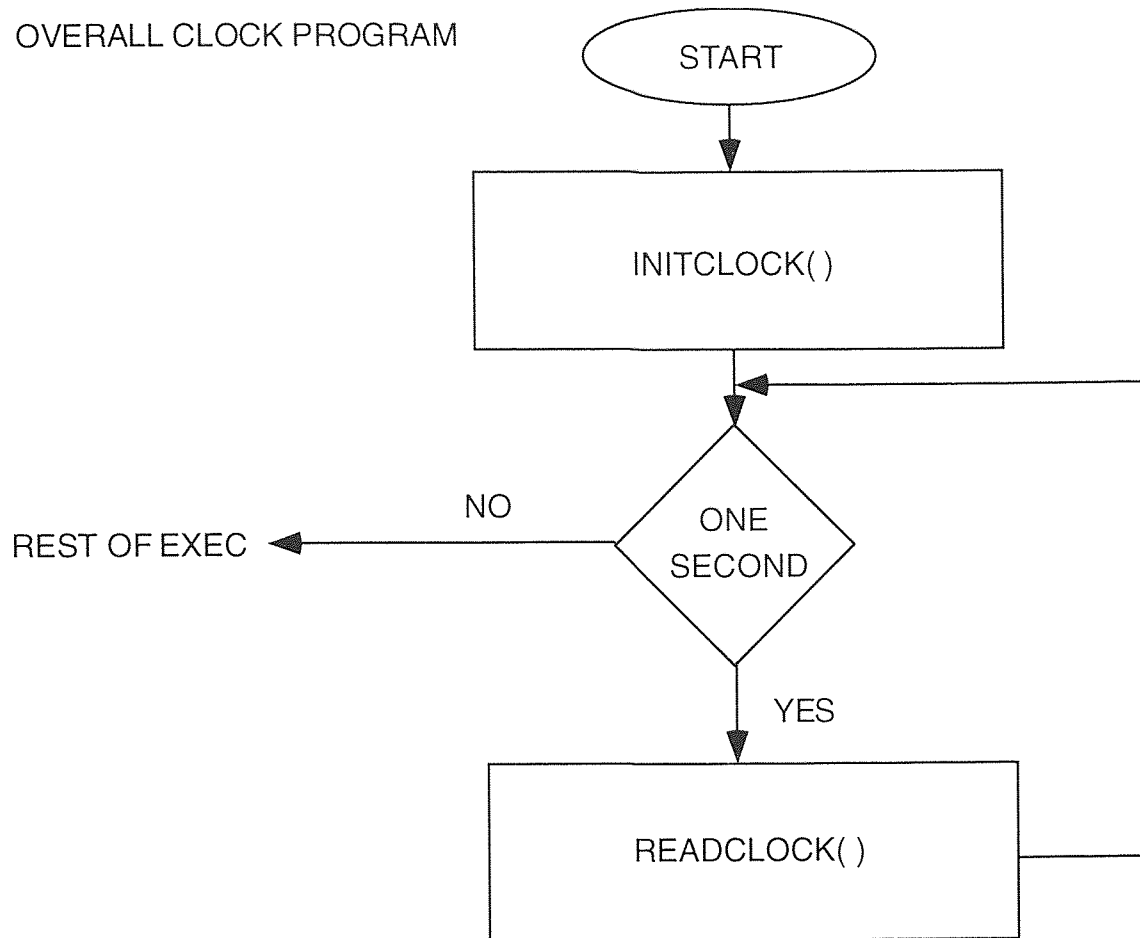


Figure 3.9 Clock Diagram

DS1202 INIT CODE
WRITTEN IN ASSEMBLY

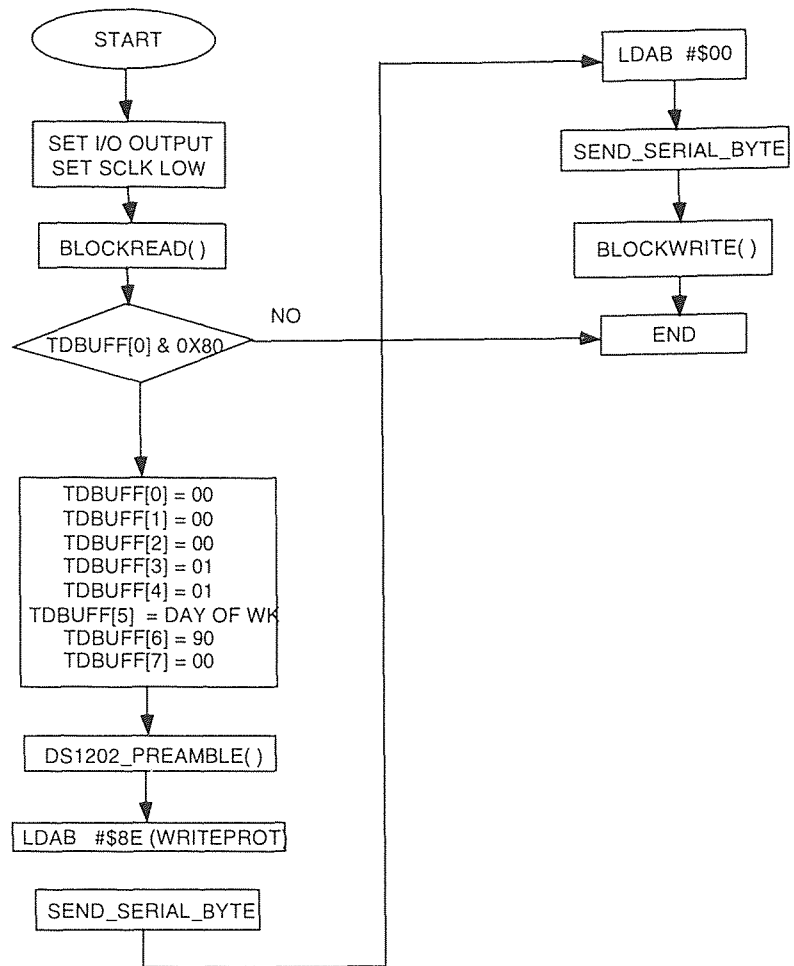


Figure 3.10 Initialization Clock Routine

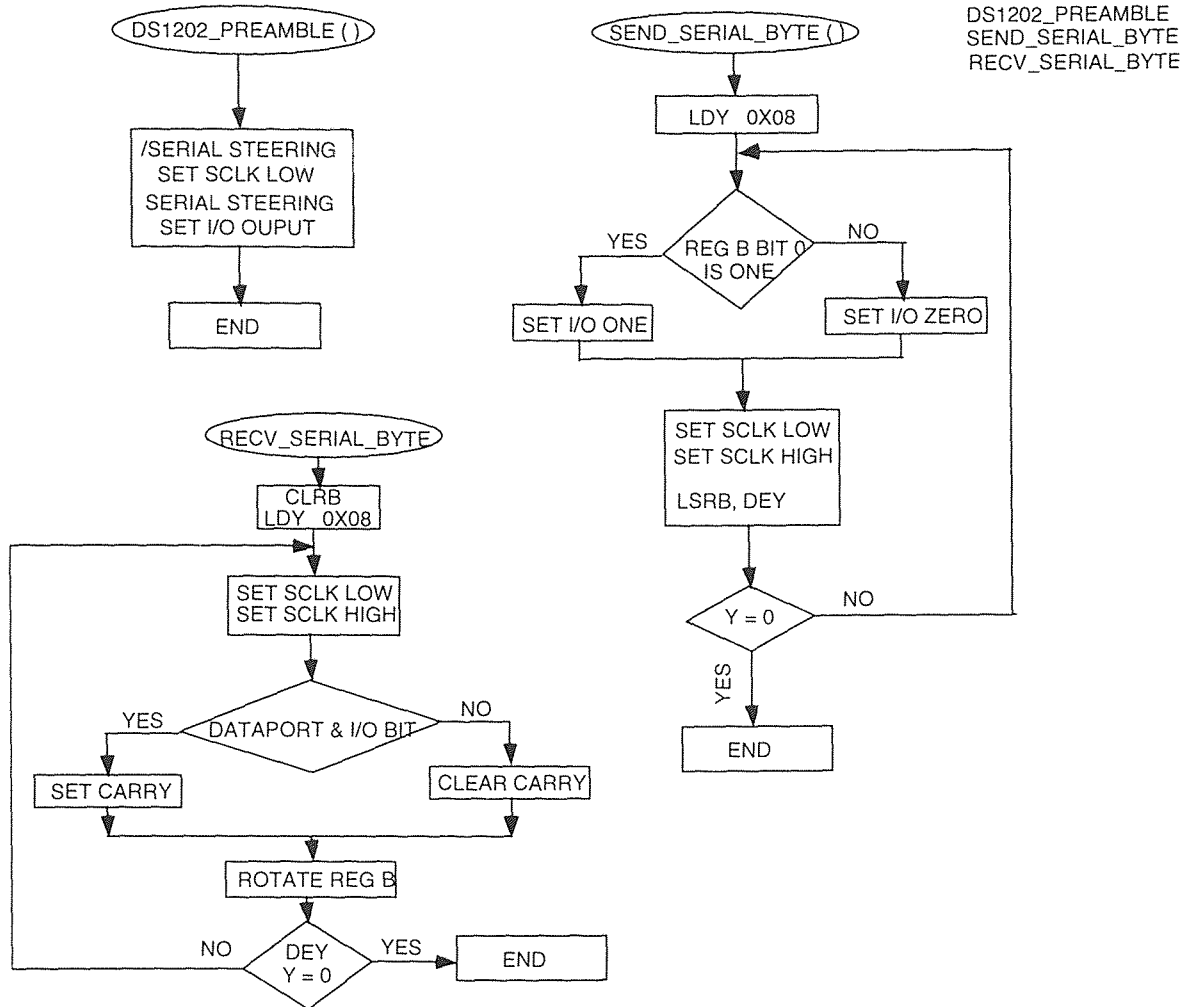


Figure 3.11 Send/Receive Real-time Clock Bytes

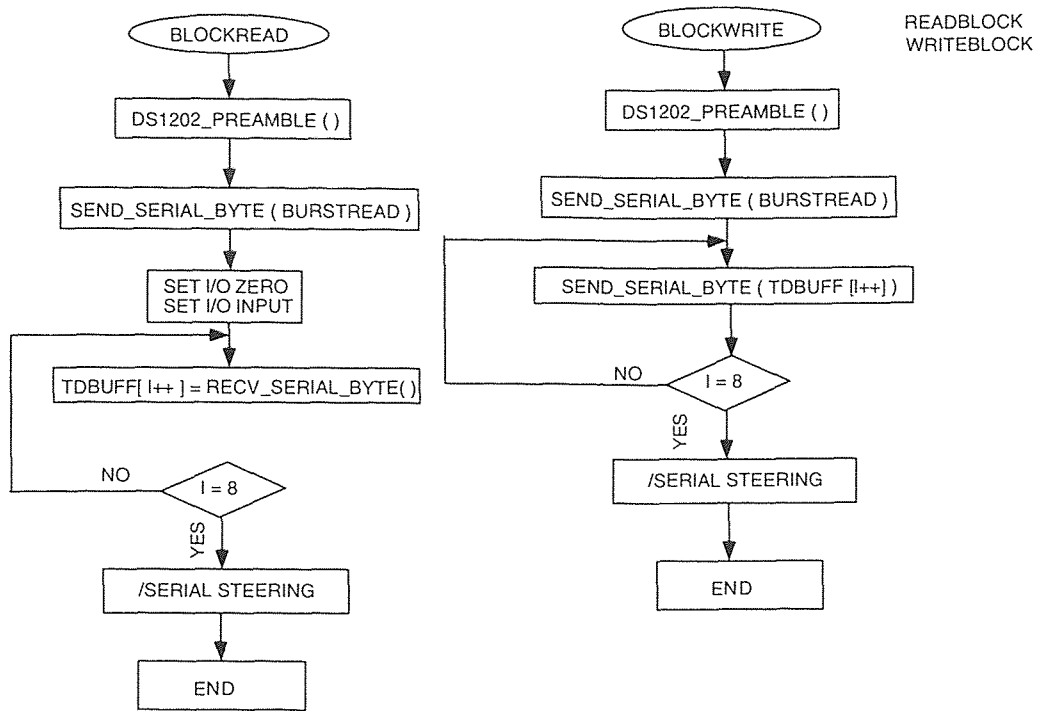


Figure 3.12 Read/Write Real-time Clock Bytes

3.10 Alphanumeric Output Ic

This device displays 12 lines of 24 characters , has a raster generator built into it, and is 75% compatible with the NEC 6145 which has been used in a number of projects at AD, but is now discontinued.. This part has an SPI serial connection , unlike the DS1202 and the BrookTree BT819 devices.

Title information for the cameras is 12 character positions. Camera number is not generated automatically. If a user wants a camera number in the title area, this value must be programmed within the 12 characters allocated.

The default programmed state of the title area is the camera number in the two leftmost positions of the 12 character area. Single digit numbers will be padded with 1 space so that the one's column of each camera number lines up as viewed when switching. This is not an issue with the 4 and 9 channel devices but generalizes the problem for 4,9 and 16 channel units.

3.11 On Screen Menu System

The menu system currently has 9 unique menus. Several of the 9 unique menus are 'paged' (i.e. alarm log menu is 4 pages). The system requirements for menu data and navigation software are currently in the 8K region.

Software menu structures are designed according to the navigation through each menu using front panel keys. Each front led keys represent separate menu functions. All led keys are illuminated during menu mode. Software structures for navigation through each menu are called MENUTASK and they are array of structures, or in another words two dimensional array in which, each array consists of navigation and pointer fields in this manner:

```
typedef struct{
    unsigned char txtcol;      /* Static string column position */
    unsigned char row;        /* Static string row position */
    int txtidx;               /* Index to static string */
    char edit;                /* Status of string (static, variable, etc.)*/
    unsigned char edcol;      /* Variable string column position */
    char fntn;                /* Numerical or character variable string */
    unsigned arg0;            /* RAM variable location */
    unsigned arg1;            /* RAM variable location */
    unsigned arg2;            /* RAM variable location */
}MENUTASK;
```

Every menu consists of two types of strings, strings that are not effected by the user (static strings) which always get painted on the screen and no need to save their changed values in the eeprom. Other strings (variable strings) which their contents needed to be changed by the user to setup the system based on their applications. Two major routines paints contents of menus to screen one for static strings and other for variable strings.

Variable string routine makes decisions on individual menus and accepts two parameters (current menu number, pointer to beginning of menu structure).

Each front panel key has one and only one function during menu mode as listed below:

- 1) Mode key (next page menu)
- 2) Minus key (decrement field or option)
- 3) Plus key (increment field or option)
- 4) Right key (move to next field or option)
- 5) Down key (move to next row or row option)
- 6) Quad key (quit menu)
- 7) 1 .. 4 keys used in camera setup menus to go from one camera setup to another.

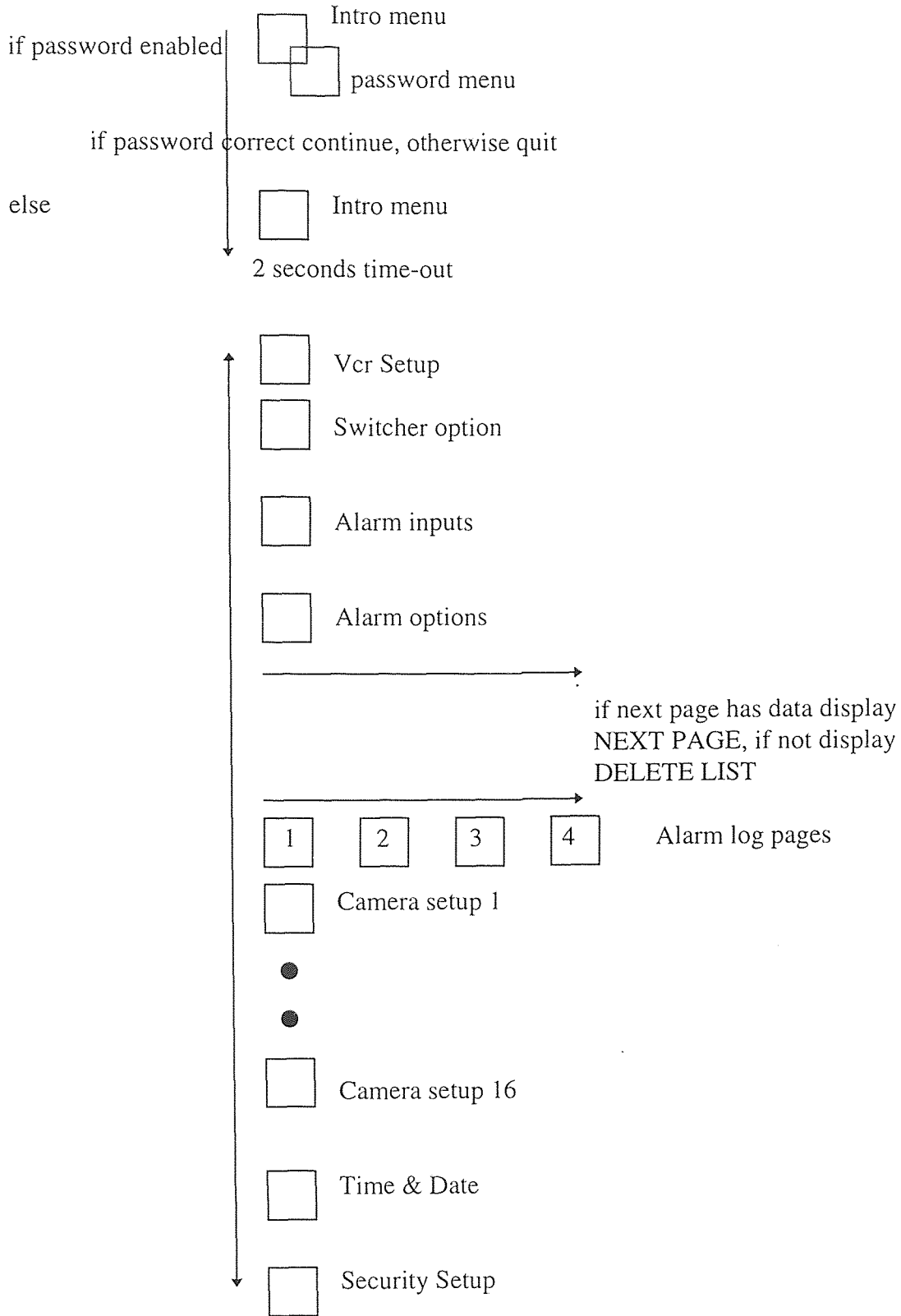
Menutasks are modified by the above keys and results saved to E²prom upon exit or going to next menu. In this fashion only six bytes allocated in ram for displaying variable strings in a menu. The below structure enables the programmer to maintain current menu number and menutask location.

```
typedef struct{
    char curmenu;          /* current menu number */
    MENUTASK *menucursor; /* pointer to menutasks */
}MENUCTRL;
```

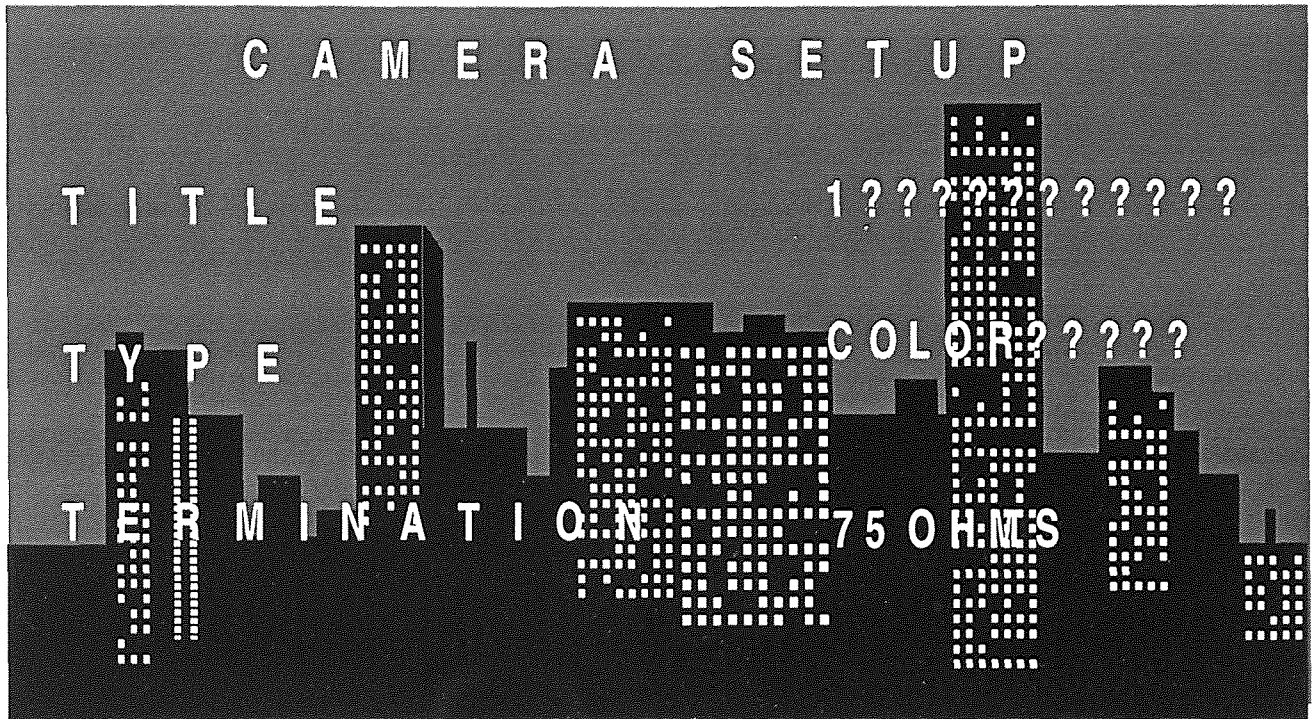
A typical menutasks for a typical menu is shown below:

```
MENUTASK const Switcher_Dwell[] = {
    {MSTRT,MSTRT,MSTRT, 0, 0, 0,      0, 0, 0},
    { 4, 1, 15,      0, 0, 0,      0, 0, 0},
    {13, 1, 28,      0, 0, 0,      0, 0, 0},
    { 1, 4, 15,      0, 0, 0,      0, 0, 0},
    {10, 4, 16,      2, 17, R_MLIST, 0, 1, 99},
    {20, 4, 17,      0, 0, 0,      0, 0, 0},
    { 1, 6, 18,      2, 17, R_SLIST, 1, 2, 3},
    {MEND,MEND,MEND, 0, 0, 0,      0, 0, 0} };
```

3.11.1 Order of Menu Appearance

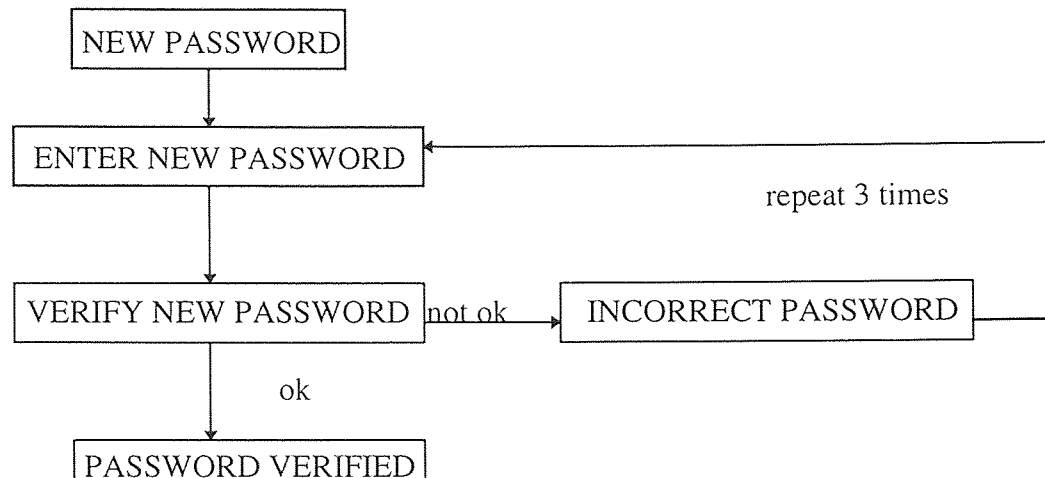


				A	L	A	R	M		L	O	G		P	A	G	E		4							
				C	A	M	E	R	A					A	L	A	R	M								
				N	U	M	B	E	R				T	I	M	E	/	D	A	T	E					
				?	?					?	?	:	?	?	:	?	?		?	?	/	?	?	/	?	?
				?	?					?	?	:	?	?	:	?	?		?	?	/	?	?	/	?	?
				?	?					?	?	:	?	?	:	?	?		?	?	/	?	?	/	?	?
				?	?					?	?	:	?	?	:	?	?		?	?	/	?	?	/	?	?
				?	?					?	?	:	?	?	:	?	?		?	?	/	?	?	/	?	?
				◀		D	E	L	E	T	E		L	I	S	T										



If verification is being correct then we get a message saying PASSWORD VERIFIED then 2 seconds delay and then NEW PASSWORD becomes NO.

If verification is being not correct then we get a message saying INCORRECT PASSWORD then 2 seconds delay and then display ENTER NEW PASSWORD again. If verification failed for the second time third time is given to the user, but after third time if verification still not correct then message PASSWORD NOT CHANGED will be displayed and then NEW PASSWORD becomes NO.



CHAPTER 4

VIDEO CAPTURE PROCESSOR

4.1 Brooktree Bt819

This part is a composite NTSC/PAL and S-video decoder, which essentially provides color video digitization services to other parts of this machine. The part should be considered as a co-processor which we have to query on a periodic basis. The part uses an Inter-Integrated Circuit bus (I^2C) to receive its initial operating parameters and to poll its status.

- Brooktree's VideoStream products (Bt819, Bt851, Bt817) are a family of single-chip, pin and register compatible solutions for processing of analog NTSC/PAL video into digital 4:2:2 YCrCb video. They provide a comprehensive choice of capabilities to enable the feature set and cost to be tailored to different system hardware configurations. All solutions are housed in a 100 QFP package.
- The feature set of the Bt819 supports a video/graphics system partitioning which optimizes the total cost of a system configured both with and without video capture capabilities. This enables system vendors to easily offer products with various levels of video support using single base-system design.

As graphics chip vendors move from graphics-only to video/graphics coprocessors and eventually to single chip video/graphics processor implementations, the ability to efficiently use silicon and package pins to support both graphics acceleration, video playback acceleration and video capture becomes critical. This problem becomes more acute as the race towards

higher performance graphics requires more and more package pins to be consumed for wide 64-bit memory interfaces and glueless local bus interfaces. The Bt819 minimizes the cost of the video capture function integration in a number of ways. Recognizing that YCrCb to RGB color space conversion is becoming a required feature of multimedia controllers for acceleration of digital video playback, the Bt819 avoids redundant functionality and allows the downstream controller to perform this task. Secondly, the Bt819 integrates the FIFO which would otherwise be dedicated to feeding a live video stream to the direct memory access engine (DMA) in video controller. Finally, the Bt819 can minimize the number of interface pins required by a downstream multimedia controller in order to keep package costs to a minimum.

Controller systems that are designed to take advantage of these features enable video capture capability to be added to the base system in a modular fashion using only single Integrated Circuit(IC).

- The Bt819 employ a proprietary technique known as UltraLock to lock to the incoming analog video signal. It will always generate the required number of pixels per line from an analog source in which the line length can vary by as much as a few microseconds. UltraLock's digital locking circuitry enables the VideoStream decoders to quickly and accurately lock on to video signals, regardless of their source. Since the technique is completely digital, UltraLock can recognize unstable signals caused by VCR headswitches or any other deviation and adapt the locking mechanism to accommodate the source. UltraLock uses non-linear techniques which are difficult, if not impossible, to

implement in genlock systems, and unlike linear techniques, it adapts the locking mechanism automatically.

- The Bt819 can reduce the video image size in both horizontal and vertical directions independently using arbitrarily selected scaling ratios. The X and Y dimensions can be scaled down to one_fourteenth of the full resolution. Horizontal scaling is implemented with a six-tap interpolation filter while two-tap interpolation is used for vertical scaling with a line store.

The video image can be arbitrarily cropped by programming the ACTIVE flag to reduce the number of active scan lines and active horizontal pixels per line.
- Analog video signals are input to the Bt819 via a two input multiplexer that can select between two composite source inputs or between a single composite and a single S-video input source.

The clock signal interface consists of two pairs of pins for crystal connection and two clock output pins. One pair of crystal pins is for connection to a 28.64 Mhz ($8 * \text{NTSC Fsc}$) crystal which is selected for NTSC operation. The other is for PAL operation with a 35.47 Mhz ($8 * \text{PAL Fsc}$) crystal. Either of the two crystal frequencies can be selected to generate CLKX1 and CLKX2 output signals. CLKX2 operates at the full crystal frequency ($8 * \text{Fsc}$) whereas CLKX1 operates at half the crystal frequency ($4 * \text{Fsc}$).
- The Bt819's outputs can support two different configurations: the Synchronous Pixel Interface (SPI) and the Asynchronous Pixel Interface (API).

Both SPI and API can support a YCrCb 4:2:2 data stream over a 16-bit wide path. The SPI also supports an 8-bit path.

In SPI mode, Bt819 outputs all horizontal and vertical blanking pixels in addition to the active pixels synchronous with CLKX1 (16-bit mode) or CLKX2 (8-bit mode). It is also possible to insert control codes into the pixel stream using chrominance and luminance values that are outside the allowable chroma and luma ranges. These control codes can be used to flag video events such as ACTIVE, HRESET, and VRESET. Decoding these video events downstream enables the video controller to do away with pins required for corresponding video control signals.

In the API mode, the Bt819 outputs only the active pixels at a rate asynchronous with the sample clock. A 40-pixel-deep FIFO buffers the pixel output port and enables the system to burst pixels out of the Bt819 at rates up to 35 Mpixels/sec.

An input clock must be provided on CLKIN for operation in this mode. The Bt819 outputs the DVALID, AEF and AFF flags to provide the system information on the status of the FIFO.

- The Bt819 registers are accessed via a two-wire Inter-Integrated Circuit (I²C) interface. The Bt819 operates as a slave device. Serial clock and data lines, SCL and SDA, are used to transfer data from the bus master at rate of 100Kbits/s. Chip select and reset signals are also available to select one of two possible Bt819 devices in the same system and to set the registers to their default values.

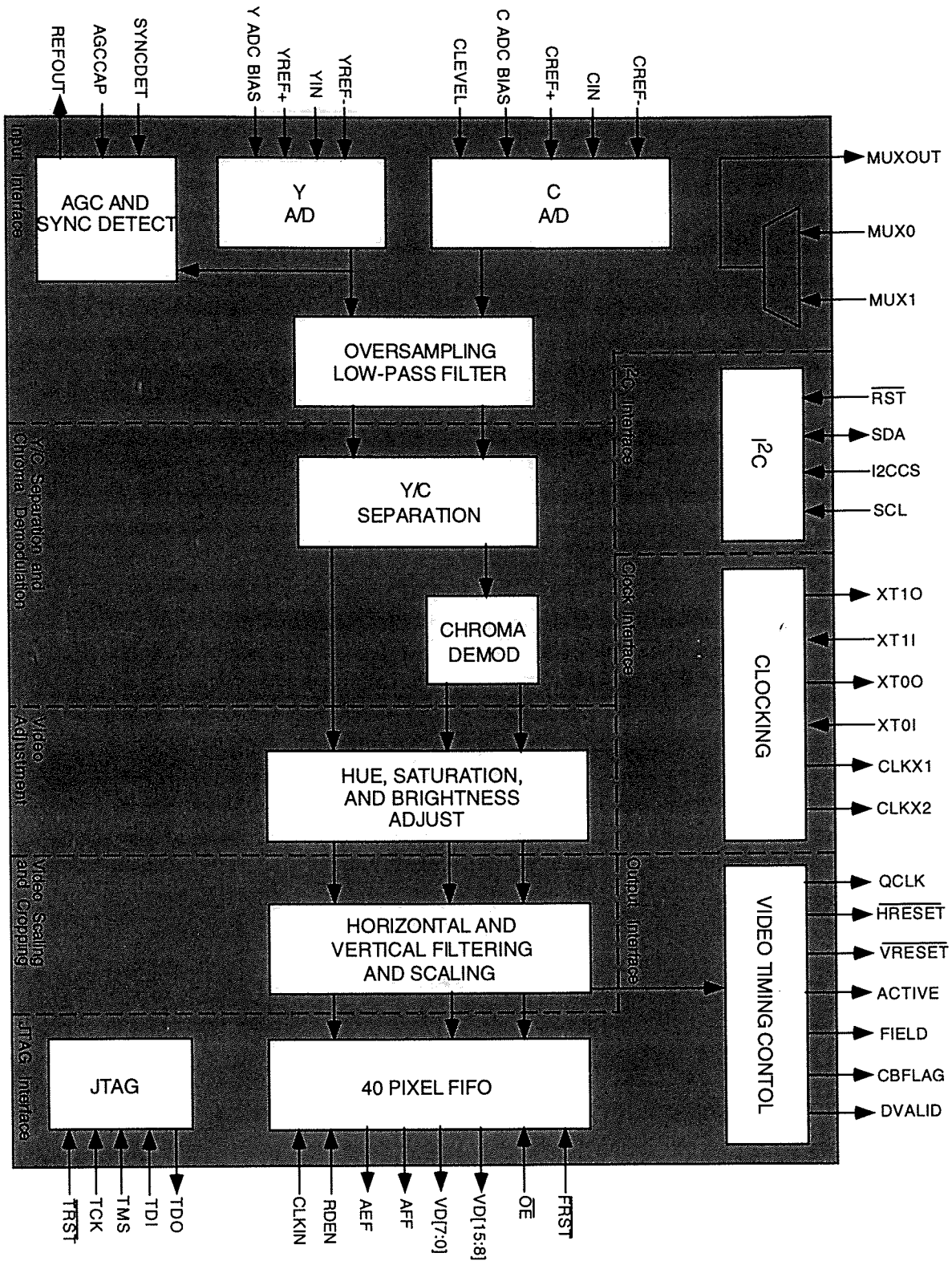


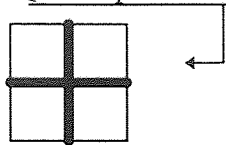
Figure 4.1 BT819 Block Diagram

CHAPTER 5

PIC PROCESSOR

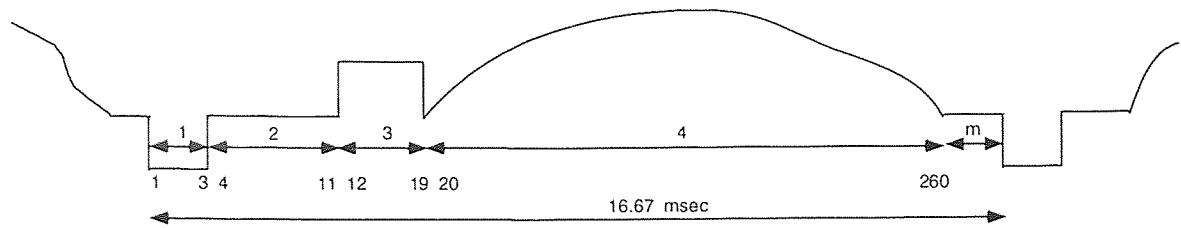
This processor produces necessary signals for this product hardware using Microchip assembly language and 13.5 Mhz clock. The signals that are shown in the next pages are:

- 1) Active Video: Blanking signal required for Bt851 Video Stream Encoder. This signal defines the active portion of video signal (live video lines 20-261).
- 2) Code Window: A window pulse to put code such as, camera ID, Alarm bit , Field bit and Q bit; which tells the hardware not to update the memory during playback mode.
- 3) Nsync1: Used to flag ASYC Ic to send clocks when digital video should be written to dual port ram.
- 4) CrossBar: Used to produce QUAD picture layout in 4 channel multiplexer.



- 5) Stop bit: This bit is set when end of each 63.5 μ sec is reached on every line. This flags the hardware to shut down PIC processor main clock (13.5 Mhz) until the next horizontal line.
- 6) Master bit: This bit is only set every 261 line which indicates one full NTSC frame passed by.
- 7) Active Pipeline: Digital information arrived at Bt851 must be pipelined before the data becomes a good data (NTSC/PAL). The time requirement is about 12 μ sec.

PIC IN VERTICAL TIME



note:

- 1 = type one, three horizontal lines
- 2 = type two, eight horizontal lines
- 3 = type three, seven horizontal lines
- 4 = type four, 241 horizontal lines
- m = 3 horizontal lines to reinitialize variables before master stop

Figure 5.1 Pic Vertical Time

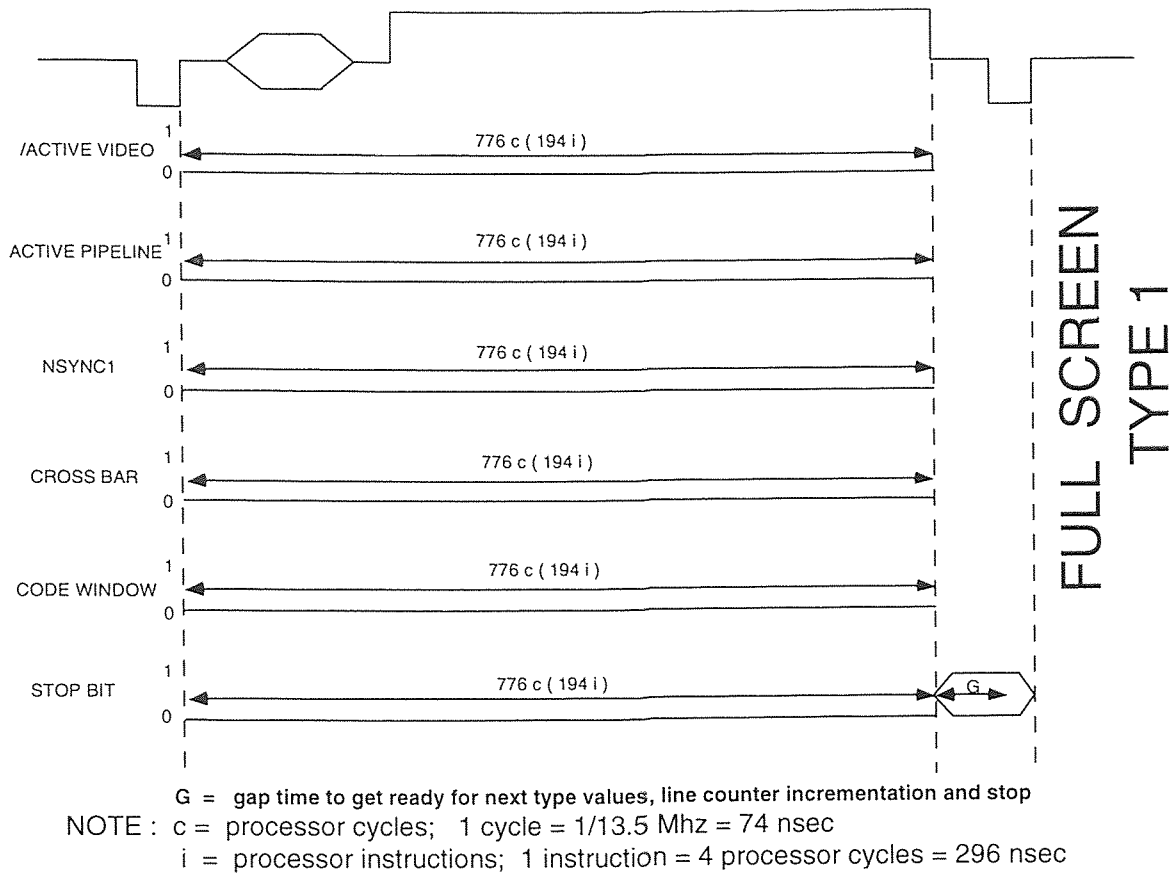


Figure 5.2 Pic Type1 Signal

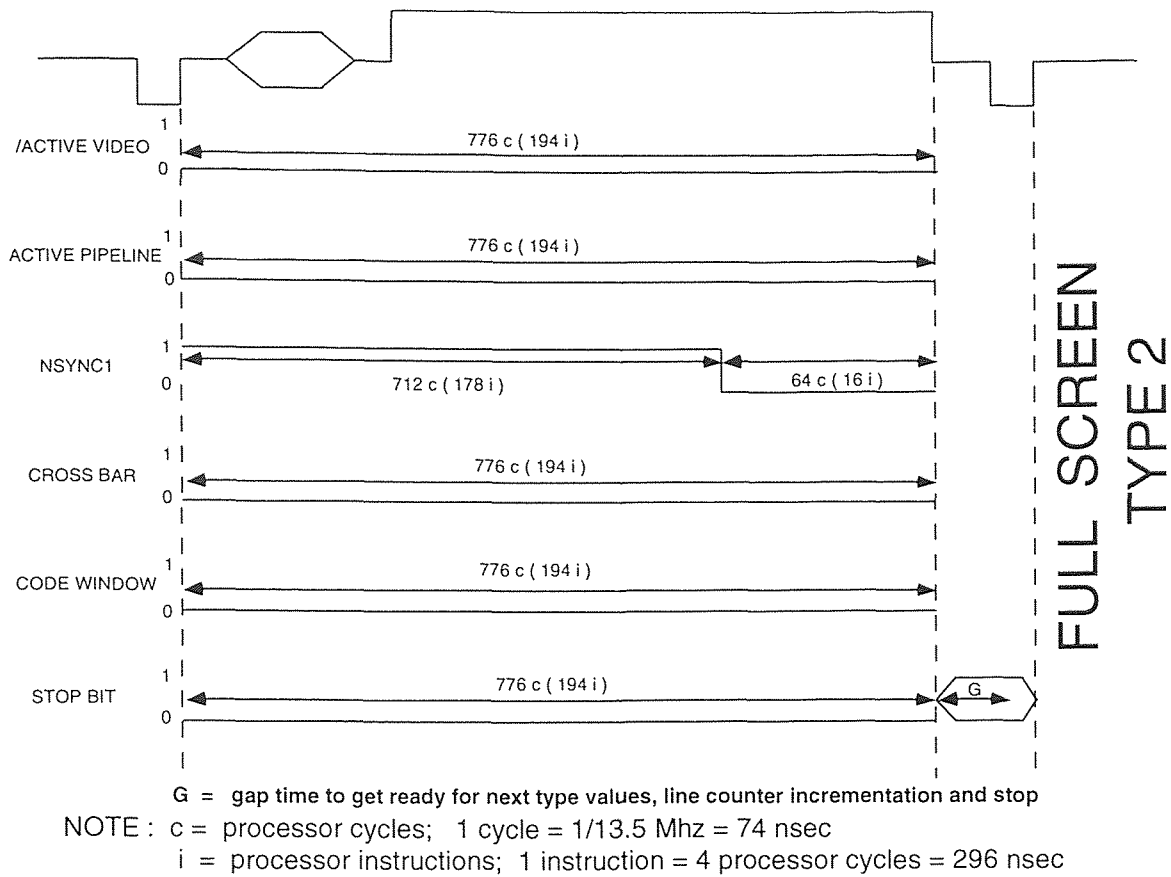


Figure 5.3 Pic Type2 Signal

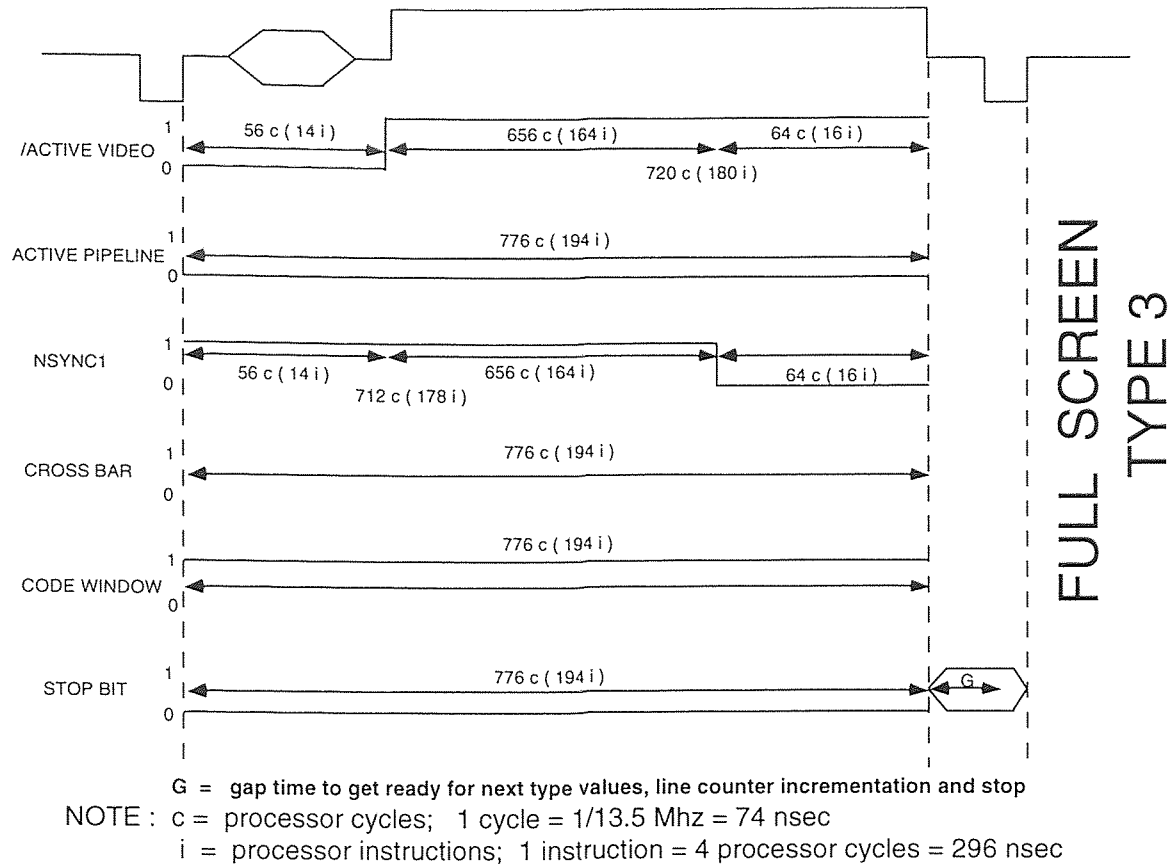


Figure 5.4 Pic Type3 Signal

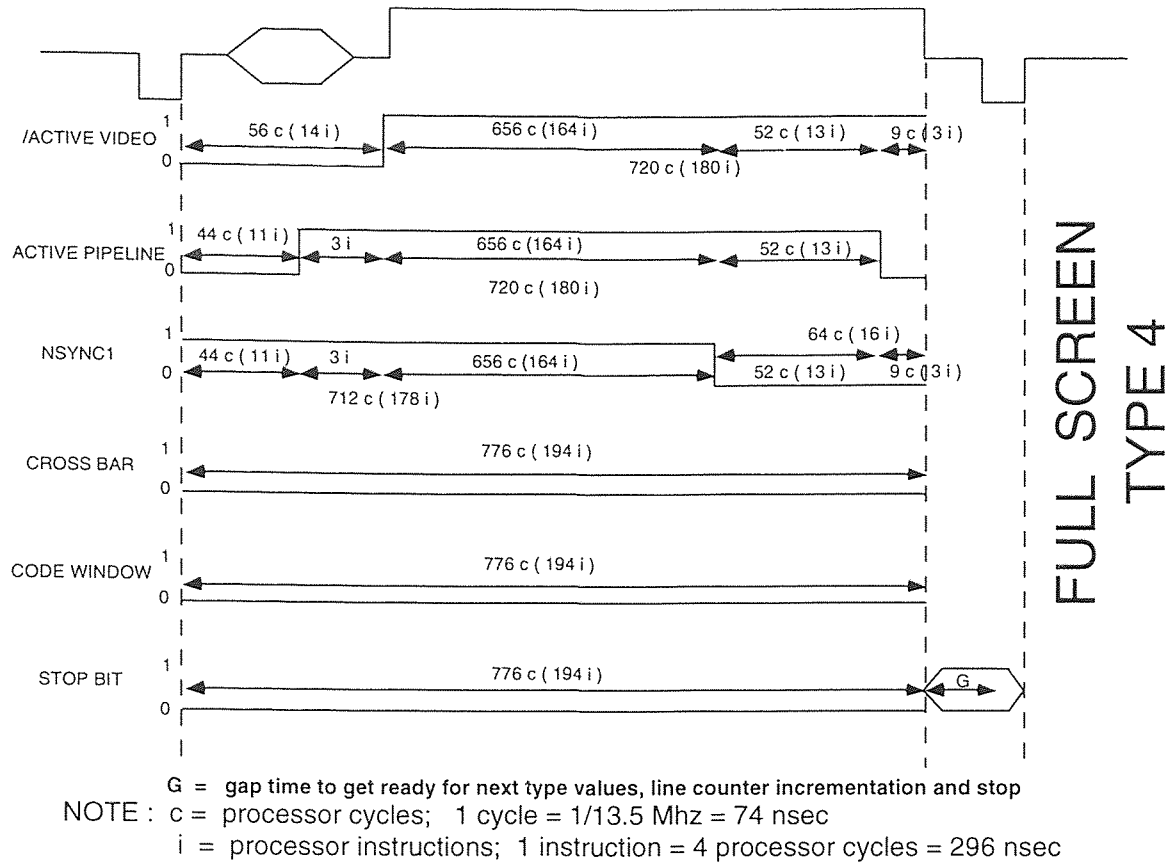


Figure 5.5 Pic Type 4 Signal

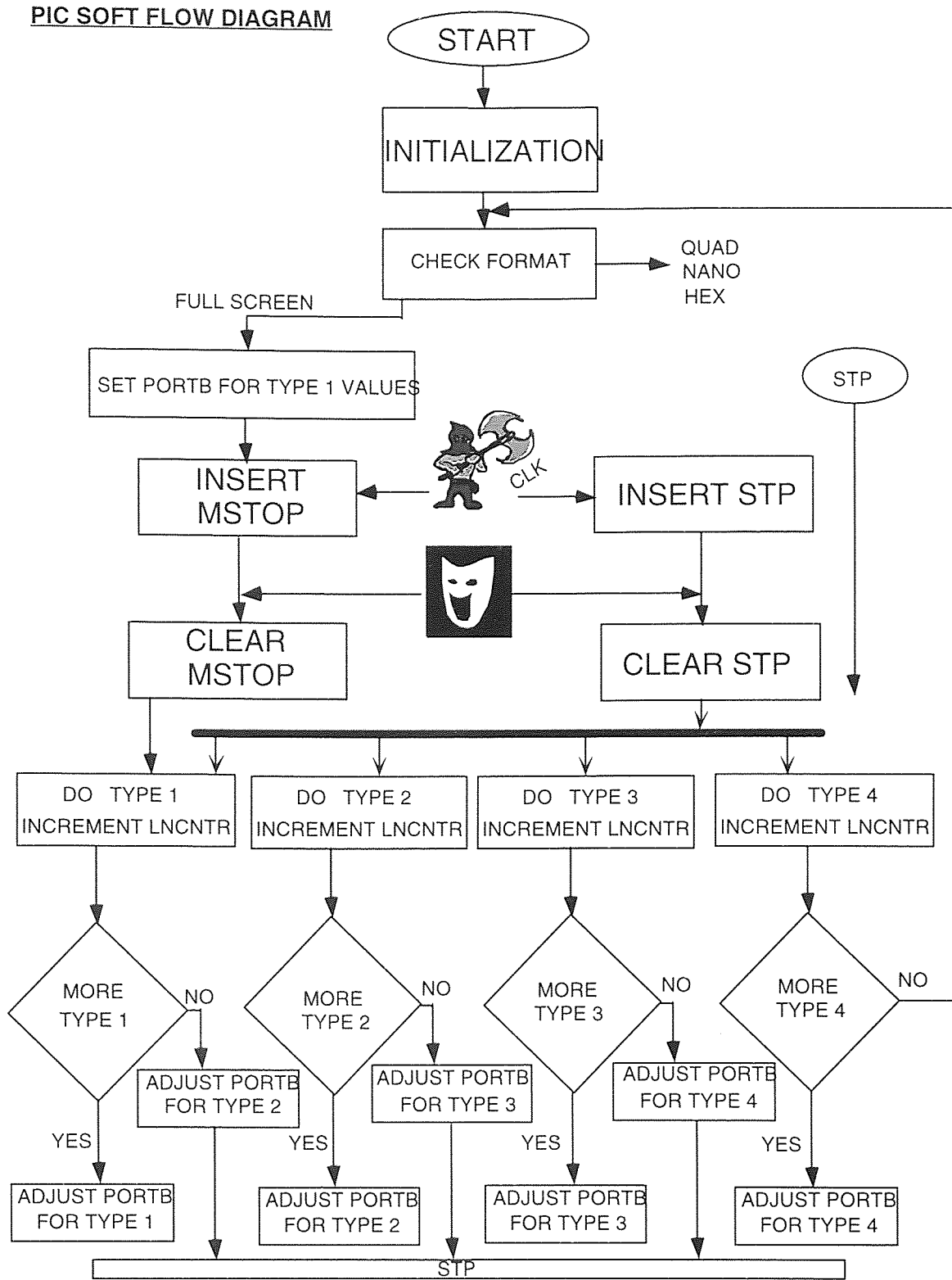


Figure 5.6 Pic Software Diagram

CHAPTER 6

INTERRUPTS

Interrupt routines have the biggest responsibilities in this product. There are two main interrupt routines, which service both the hardware and software sides. The two interrupts are one external IRQ interrupt and second is Vertical Sync pulse from Bt851. The IRQ interrupt is controlled by hardware and called Write Side Display. This interrupt service routine updates two ram locations called odd and even pages as well as character generator. Odd and Even ram locations are holding memory page address (0,1,2,3). As mentioned before Dram in this product has four pages. The Vertical Sync Interrupt takes the values of two ram locations and writes the data to memory locations. This method enables the product to update different locations of the memory. The reason for two ram locations is based on Even and Odd fields in video signals. Both interrupts are happening at 60 Hz rate asynchronously.

Head Switching Pulse (HS Pulse) - One frame of tape is written per Horizontal Sync Pulse. The frequency of this pulse varies with tape speed and could be as long as 1 hour and as short as 1 Nano seconds.

Code Capture - There is an 8-bit word (0x3D00 read) which is extracted by hardware from the Video Tape and contains camera # and alarm information.

$2 \text{ hours} * (60 \text{ minutes/hr}) * (60 \text{ sec/min}) * 60 \text{ verticals/sec} = 432,000 \text{ verticals.}$

Table 6.1 I/O Port Requirements for Both 4 and 9/16 Channel Multiplexes

Schematic Name	Decode Addr in Hex	AD1582/4	AD1582/9/16
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/DECODE1	0X3000	-	1-8 termination
/DECODE2	0X3100	-	9-16 termination
/DECODE3	0X3200	Mitel Switch	Mitel Switch
/DECODE4	0X3300	Front Panel LED	?????
/DECODE5	0X3400	Front Panel LED	Front Panel LED
/DECODE6	0X3500	-	Front Panel LED
/DECODE7	0X3600	-	Front Panel LED
/DECODE8	0X3700	Rear Panel Alarm	Rear Panel Alarm
/DECODE9	0X3800	1-4 termination	1-4 termination
/DECODE10	0X3900	-	Rear Panel Alarm
/DECODE11	0X3A00	-	Rear Panel Alarm
/DECODE12	0X3B00	AGC,DAC Video Control	AGC,DAC Video Control
/DECODE13	0X3C00	ASIC Control	ASIC Control
/DECODE14	0X3D00	Front Panel Keystroke	Front Panel Keystroke
/DECODE15	0X3E00	IRQ_ACK	IRQ_ACK
/DECODE16	0X3F00	Camera ID	Camera ID

CHAPTER 7

SUMMARY and CONCLUSION

This product started with research and development stage by American Dynamics multiplexer group to look into new encoding/decoding processor(s) to meet the recent digital video technology in the CCTV market. The research was limited to find a non-expensive digital video processors so the low end customers could afford owning a switcher with time base correcting with no need to expensive time lapse VCRs. The two processors developed by BrookTree Corporation met the criteria but the problem was these two processors were under Beta test phase, so in design of four channel multiplexer management had taken the possibility of not meeting the dead line for the final product.

The multiplexer team then started by getting samples and building hardware modules and software modules to test these two devices before any major design could happen. The modules were designed toward the final design to save time and man power. After testing modules then the cad and cabinet group designed the look of this product. In all these phases software group helped to write test procedures and documentation for this product.

Because of BrookTree Ics being in Beta phase bugs were discovered and solutions produced by both hardware and software group to push the product further in the design stage, rather than waiting for BrookTree to be fixed. For example one of the discoveries was that the Fifo buffer in BrookTree was not properly working as it was advertised. Therefore, a monostable was designed to lower the vertical frequency to let the digital video come out at reasonable rate for the dual ram memory to store the result.

This project was made this student to not only to realize the availability of technology but also the complication of video signal and its properties to time. Timing is one of the most important aspect of the design not only in terms of hardware but also in terms of software. Some of the routines in software had been translated to assembly from C/C++. The reason was that the cross compilers sometimes are not capable of optimizing a procedure as quick as pure assembly. Some of software software modules were used PC as a platform for simulation of final code and then the code translated to meet cross compiler parameters. This made the major portion of software to be debugged in less time and in more efficient way. This product can be number one multiplexer in terms of its sophistication in terms of digital video, software execution time, unique features built in and finally its low price with respect to other multiplexers in CCTV market.

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