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ABSTRACT

DESIGN, PROCESS AND PERFORMANCE SIMULATION OF A 360×360-ELEMENT VERY HIGH FRAME RATE BURST-IMAGE SENSOR

by
Guang Yang

A process was developed for fabrication of 360x360-element Very High Frame Rate (VHFR) burst-image sensor on the bases of one-dimensional (1-D) and two-dimensional (2-D) device and process simulations using SUPREM III, SUPREM IV, PISCES IIB and ISE-TCAD software, and the process data provided by the David Sarnoff Research Center. This process includes SiO_2-Si_3N_4 gate dielectric, four-levels of polysilicon, three-levels of metal, eight implants, and requires twenty-one mask levels. The imagers with a 2-cmx2-cm chip size were fabricated at the David Sarnoff Research Center. The VHFR burst-image sensor is capable of capturing images at frame rates up to 10^6 frames/sec. It stores continuously the last 30 image frames at the CCD pixel memory and reads out the detected frames at a slow rate.

1-D and 2-D simulation study is presented for optimization of the charge handling capacity of the buried-channel CCD (BCCD) pixel memory elements and simulation results are compared with the experimental data.

A new concept was developed and demonstrated for large high-speed photodetector with complete charge readout in less than 0.1 μsec. The high-speed photodetector is in the form of a graded three-potential-level pinned-buried BCCD structure. The simulation results of the 33-μm long photodetector of the VHFR burst-image sensor showed that a complete charge read out can be achieved in less than 0.1 μsec. Frame-to-frame image lag of less than 1.0% was demonstrated for operation of the imager with frame integration time of 1.0 μsec for optical test pattern illuminated by 0.4 μsec LED pluses.

DESIGN, PROCESS AND PERFORMANCE SIMULATION OF A 360×360-ELEMENT VERY HIGH FRAME RATE BURST-IMAGE SENSOR

by
Guang Yang

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DESIGN, PROCESS AND PERFORMANCE SIMULATION OF A 360×360-ELEMENT VERY HIGH FRAME RATE BURST-IMAGE SENSOR

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- Guang Yang, Chao Ye, and Walter F. Kosonocky, "Simulation of High Density CCD Image Structures." Presented in Dana Point, California, April, 1995, at the *1995 IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors*, Dana Point, California, USA, 1995.

- Walter F. Kosonocky and Guang Yang, "Multi-implant Pinned-buried High-Speed Zero-Lag Photodetector." Patent disclosure to be filed.

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Dedicated to my mom, my dad,
and my family

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As I sit in front of my computer and type the last "period" in my dissertation, my fond memories are with the people who influenced and helped me one way or another in the course of reaching at this point. They have contributed greatly to my evolution as a scientist, and to them I would like to express my warmest gratitude.

Especially, I would like to express my deepest appreciation to my advisor, Dr. Walter F. Kosonocky, for his guidance, constant support and encouragement throughout the four and half years of my Ph.D. studies. As a pioneer of CCD development, Walter's knowledge of CCD image sensor and semiconductor devices has contributed enormously to the completion of this dissertation. Walter deserves all the credits a thesis advisor can possibly get. It has been my great pleasure to work with Walter. I am very happy to become one of his Ph.D. students.

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CHAPTER 1

INTRODUCTION

The research described in this dissertation was performed at Image Sensor Design and Simulation Lab of Electronic Imaging Center in NJIT under the direction of Dr. Walter F. Kosonocky, Distinguished Professor of Electrical Engineering and NJIT Foundation Chair for Optoelectronics and Solid-State Circuits. This work was done with the support of an ONR SBIR Phase II program of Princeton Scientific Instruments, Inc. and 1993 Innovation Partnership grant of New Jersey Commission on Science and Technology.

In July 1991, Professor Walter F. Kosonocky and Mr. John L. Lowrance of Princeton Scientific Instruments, Inc. proposed a general architecture for a Very High Frame Rate (VHFR) burst-image sensor that should be capable of capturing a large number (N) of images at frame rates of up to 10^6 frames/sec [1]. The captured (detected and stored) N frames are read out at a slower rate during the imager readout cycle. The VHFR burst-image sensor was fabricated by David Sarnoff Research Center (Sarnoff) with a rather complex process that includes three-layers of metal, four-layers of polysilicon and eight implants process. The goal of the dissertation has been to simulate the expected device characteristics and performance and to define the process for construction of VHFR burst-image sensor. The simulation of the VHFR imager structure was based on the device dimensions obtained from the chip layout and the process data provided by Sarnoff where the imager was fabricated. The simulation study has been focused on the charge handling capacities of the BCCD channel, the design of the process and the photodetector readout characteristics of the imager.

Over the last eight years, previous research studies at Electronic Imaging Center of NJIT on the process and device simulation of the visible CCD structures and high-speed photodetector were done by be the following students of Professor Kosonocky:

Krishna M. Pillalamarri [2], Zengjing Wu [3], Mark Ratner [4], Elie I. Mourad [5], and Subramanyam V. Ayyagari [6].

The major objective of this dissertation was to optimize the charge handling capacities of the BCCD channel based on the process parameters used by Sarnoff using simulation tools. The resulting process definition and flow sequence was then used by Sarnoff for the fabrication of the VHFR burst-image sensor. The second major objective of this dissertation was to simulate the expected performance of high-speed photodetectors. The photodetector simulation study resulted in an optimized photodetector structure which can achieve a very high readout speed ($\geq$ 10 MHz) without image lag*.

At this point, it should be stated that, although the main thrust of the dissertation is represented by the process and device simulation study of the VHFR burst-image sensor, the author also participated and contributed to the design of the layout and the development of the detail operation of the burst-image sensor. Therefore, this work is also included in the dissertation.

The major contributions to the development of the layout of the imager were made by Liansheng Xie and Chao Ye. Initial work on the chip design of the imager was done by Liansheng Xie. However, the final chip design, layout and layout verification were done by Chao Ye who is expected to include this work in his Ph.D. dissertation at a later date. The major contributors to the testing of the VHFR burst-image sensor and the test devices is Rakesh Kabra and Chao Ye of NJIT, Vincent Mastrocola of Princeton Scientific Instrument (PSI), Inc., and Tom Villani of David Sarnoff Research Center. However, the author also participated in this effort, particularly, in the area of the evaluation of the performance of the test devices.

---

* Lag is defined as a fractional charge left behind in the photodetector during a readout of a very low intensity frame following a high intensity frame.

The second chapter of this dissertation describes the basic principles of the CCDs. After a short review of the surface-channel CCD (SCCD) and buried-channel CCD (BCCD) fundamentals, this chapter reviews the charge confinement and charge transfer mechanisms in CCD operation.

The third chapter gives an overview of the CCD modeling. It reviews the history of the CCD modeling, and describes the software tools used in this dissertation for the process and device simulation of the CCD structure. These software tools include SUPREM III, SUPREM IV, PISCES IIB, and ISE-TCAD package.

The forth chapter reviews the design, construction and operation of the VHFR burst-image sensor. This chapter also presents the experimental data that demonstrated the performance of the VHFR burst-image sensor.

The fifth chapter describes the process fabrication of the VHFR burst-image sensor. It includes the mask layers, fabrication sequence and process. The process specification was developed on the bases of the process data provided by Sarnoff and one dimensional (1-D) and two dimensional (2-D) simulations by SUPREM III, SUPREM IV, PISCES IIB which are presented in Chapters 6 and 7. Also presented in this chapter is a comparison of the SEM photographs of the processed imager chip with the 2-D topography simulation results by using ISE-TCAD tools.

The sixth chapter describes the process and device simulation by using SUPREM III and PISCES IIB for the optimization of the charge handling capacity of the BCCD channel, short gate effect in terms of gate length, channel width and channel-stop width, as well as determination of the BCCD channel potential as function of gate voltage. The optimization of the BCCD channel charge handling capacity includes the charge handling capacity as function of total BCCD implant dose, the ratio of arsenic implant dose to phosphorus implant dose, as well as the gate voltage swing. For a comparison, the experimental data on the BCCD channel potential as function of applied gate voltage and on the charge handling capacity of the BCCD elements are also presented in this chapter.

The seventh chapter describes the design of the high-speed pinned-buried lag-free photodetector. After introducing the construction of the photodetector, it shows the simulation results of the photodetector performance by using SUPREM III, SUPREM IV, PISCES IIB.

Finally, the conclusions of this dissertation are presented in the eighth chapter and the suggestions for further research are presented in the ninth chapter.

CHAPTER 2

CHARGE-COUPLED DEVICES

2.1 Introduction

In 1970, W. Boyle and G. Smith of Bell Labs, invented the Charge-Coupled Device (CCD) [7]. Since the CCD was invented, it has been considered for use in a wide variety of applications, ranging from high density VLSI memory circuits to visible and infrared imagers [8]-[19]. With the concurrent development of metal-oxide-semiconductor (MOS) technology in the early 1970's for integrated circuit applications, CCD performance continued to improve. As the first generation solid-state imaging device technology, CCDs have numerous performance advantages over most competing technologies for imaging. These include small pixel size, high fill-factor, large format, low readout noise and low dark current [19]-[24].

The CCD structures that include Surface-Channel CCD (SCCD) and Buried-Channel CCD (BCCD), that can be further divided into the two-, three-, and four-phase CCDs [23]-[26], the meander CCD [27]-[30], the virtual-phase CCD [31], [32], and other types [33]-[35]. A second generation of solid-state image sensors is expected to include on-chip timing and control electronics, signal processing and analog-to-digital conversion, in addition to high performance image acquisition[36]-[38]. On the other hand, with today's VLSI technologies which include the lager chip size and small CCD pixel size, the CCDs can be made in large area and high resolution [39], [40] for consumer market and scientific applications. Finally, the very high frame-rate burst-image sensor studied in this dissertation is of great interest for imaging applications with extremely fast time resolution (as low as 1.0 μsec or less).

2.2 CCD Concept

The basic concept of CCDs can be explained by a simple series connection of Metal-Oxide-Semiconductor capacitors (MOS capacitors) [20], [21], [41]-[43]. The individual capacitors are physically located very close to each other. The CCD is a unique device capable of charge storage and transfer: charge carriers are stored on the MOS capacitors and transferred between them under control of clock phases. Thus, charge packets can be transported from one capacitor to its neighbor capacitor. This transport of isolated charge packets can be accomplished in an almost perfect way, without any noticeable deterioration of the charge content. If the chain of MOS capacitors is terminated with an output node and an appropriate output amplifier, the charge signals will be converted into an output voltage.

The way the charge signals are introduced into the charge-coupled devices is application-dependent. In the case of filters, delay lines and memories, the CCD is provided with an electrical input stage. In the case of solid-state imagers, the impinging photons generate charge carriers which are collected and transported to the output amplifier.

2.3 SCCD and BCCD

In its simplest form the CCD consists of a semiconductor material covered by a thin insulator (usually silicon-dioxide or silicon-nitride) and an overlying conductor gate (usually polysilicon), as shown in Figure 2.1(a) for a p-type substrate. This device structure was introduced in 1970 by Boyle and Smith [7]. Since the signal (minority carriers) stored under the gates is located near the Si/SiO_2 interfaces, as shown in potential diagram of Figure 2.1(b), this device is referred to as a surface-channel CCD or just SCCD.

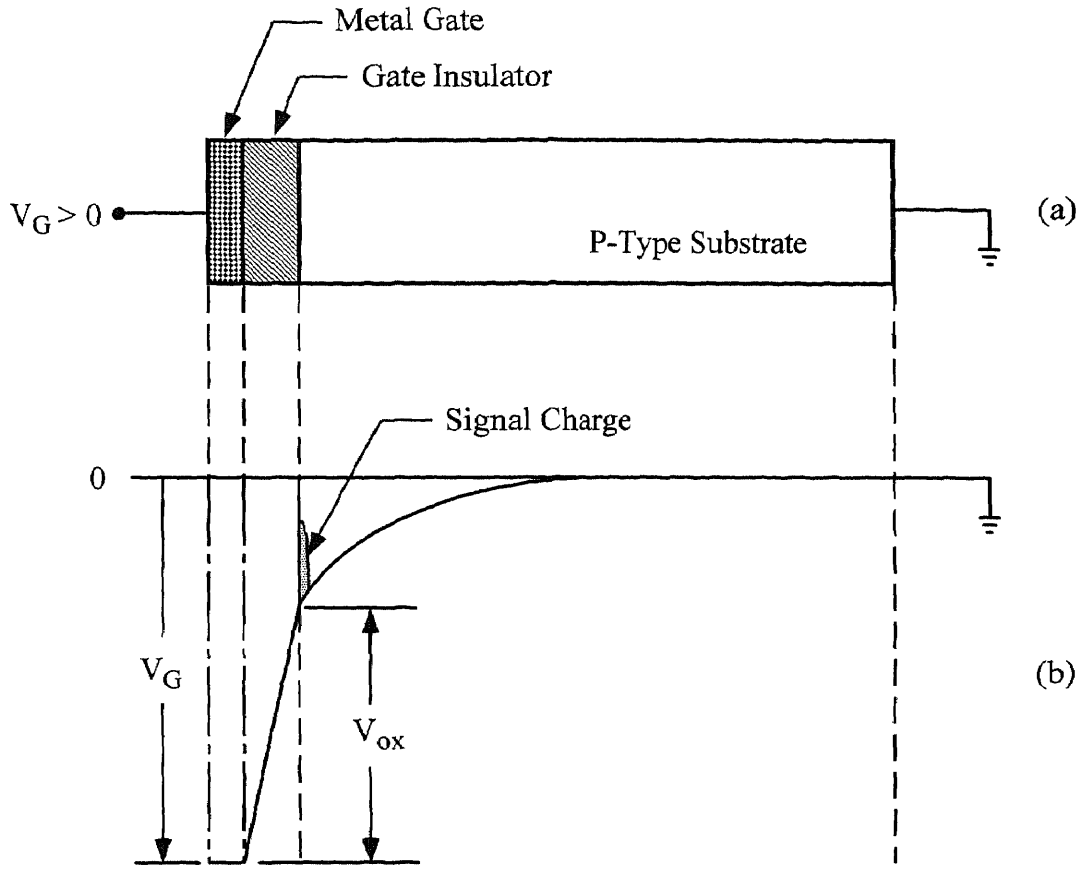


Figure 2.1 (a) *Surface-channel CCD structure for p-type substrate;*
(b) *Potential diagram of SCCD illustrating the principle of charge storage.*

In the SCCD, fast interface states play an important role in the charge transfer efficiency and operating speed of the device. Fast interface states trap charge as the charge signal is introduced to the well, but are reluctant to give them up and empty at a slower rate, which depends upon the energy difference between the interface states and the conduction band [41], [44]-[46]. The interaction of the charge signal with the fast interface states limits the speed of operation of the SCCD.

The first publications on a buried channel CCD (BCCD) appeared in 1972 [47], [48], only two years after the invention of the SCCD. The basic structure of the BCCD for a p-type substrate is shown in Figure 2.2(a), it consists of a shallow implanted region of

opposite conductivity to that of the substrate. The main advantage of the BCCD compared with the SCCD is that the signal (major carrier of the n-type implant region for the p-type substrate) is stored in the bulk of the semiconductor away from interface traps, as shown in Figure 2.2(b). By avoiding the problems associated with interface trapping, the BCCD can be operated at high clock rate with greater charge transfer efficiency than the SCCD. The advantages of the BCCD do not come without cost, while the BCCD can operator at higher clock rate than the SCCD, its maximum charge handling capacity is 1/4 to 1/3 of that of SCCD [45].

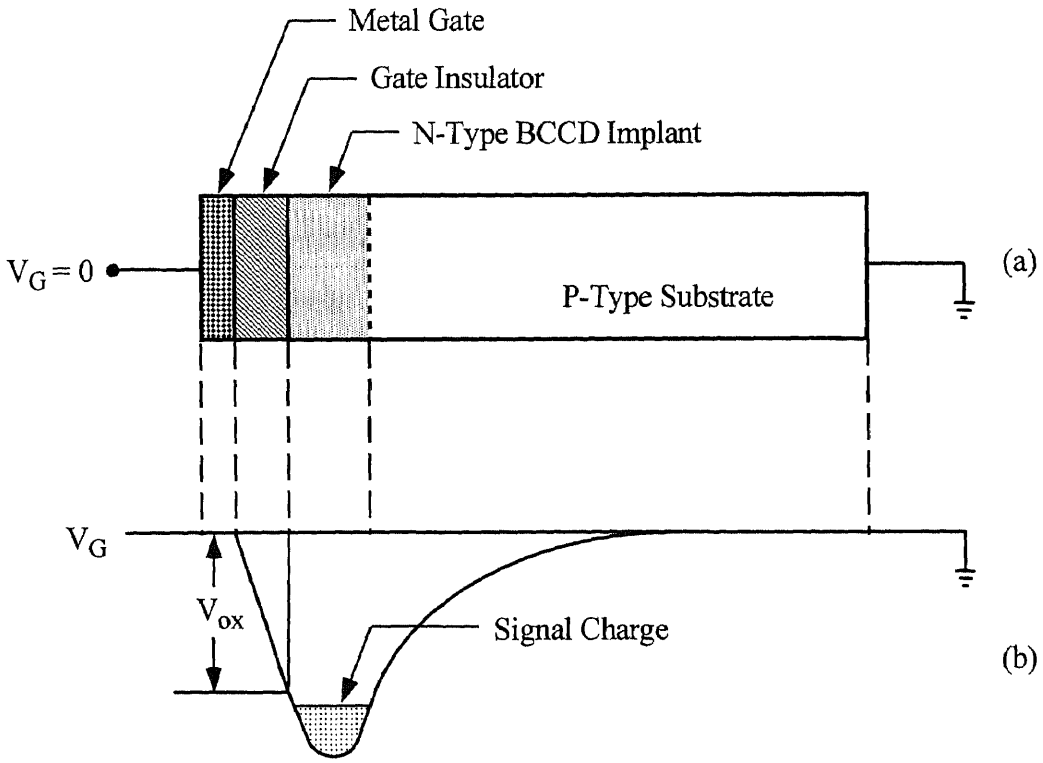


Figure 2.2 (a) *Buried-channel CCD structure for p-type substrate;*
(b) *Potential diagram of BCCD illustrating the principle of charge storage.*

2.4 Charge Storage in CCD

The charge storage in CCDs has been discussed in several books [20], [21], [42], [43], [44]. On the bases of a recent review given by A. J. P. Theuwissen [43], the charge storage in CCDs is briefly described in this section. It should be noted that, although the charge storage in CCD described in this section is using the SCCD structure, the general ideas is also applicable to the charge storage in the BCCD structure.

As mentioned before, the SCCD is a series connection of MOS capacitors. The threshold voltage V_T, needed to bring the MOS capacitance near to strong inversion is given by:

$$V_T = \Phi_{MS} + 2 \cdot \Phi_F - \frac{Q_{ox}}{C_{ox}} + \frac{Q_d}{C_{ox}}, \tag{2.1}$$

where, Φ_{MS} is the work-function difference between the metal and the silicon bulk, Q_{ox} is the sum of fixed oxide charges and mobile oxide charge, Q_d is the amount of fixed charge in depletion region, C_{ox} is the oxide capacitance per unit area, and Φ_F is the represents the Fermi potential of the bulk material, given by:

$$\Phi_F = \frac{kT}{q} \cdot \ln \frac{N_A}{n_i}, \tag{2.2}$$

with:

- k: Boltzmann's constant;
- T: Absolute temperature (°K);
- n_i: The intrinsic carrier concentration; and
- N_A: the doping concentration of p-type bulk.

To store signal charges in a CCD, the MOS capacitors are sequentially driven into deep depletion by digital pulses applied to the gate of the MOS structures. But when the CCD elements are forced into deep depletion, free electrons will be also supplied to the MOS capacitors — behaving in a non-equilibrium mode — through a process of thermal generation of minority carriers. Therefore, the charge signal can be stored in the CCD

elements only for a time much shorter than the time needed to build up the equilibrium inversion layer by thermal generation. Otherwise the thermally-generated minority carries would eventually saturate the charge handling capacity of the CCD elements. Under the condition of thermal non-equilibrium, an expression for the surface potential Φ_S as a function the minority-carrier charge density Q_n in deep depletion is given by:

$$\Phi_S = V_G - \Phi_{MS} + \frac{Q_{ox} + Q_n}{C_{ox}} - \frac{\varepsilon_{si} \cdot q \cdot N_A}{C_{ox}^2} \cdot \left[1 - \sqrt{1 - \frac{2 \cdot C_{ox}^2 \cdot \left(V_G - \Phi_{MS} + \frac{Q_{ox} + Q_n}{C_{ox}} \right)}{\varepsilon_{si} \cdot q \cdot N_A}} \right] \quad (2.3)$$

As can be seen from the above-mentioned expression, the surface potential Φ_S is a function of the gate voltage V_G, the oxide thickness t_{ox} (oxide capacitance per unit area C_{ox} is a function of t_{ox}), the doping concentration of the substrate N_A, and the number of free charge carriers Q_n. Figure 2.3 illustrates the influence of the above four parameters on the surface potential.

By defining two new parameters: Φ_{Sdd} — the surface potential in deep depletion (for $Q_n = 0$), and Φ_{Ssi} — the surface potential in strong inversion (for $Q_n = Q_{n,sat}$), the relation between the surface potential Φ_S and Q_n can be linearized by the following formula:

$$\Phi_S = \Phi_{Sdd} + (\Phi_{Ssi} - \Phi_{Sdd}) \cdot \frac{Q_n}{Q_{n,sat}} . \quad (2.4)$$

However, the maximum charge that can be handled by a CCD, i.e., the CCD charge handling capacity, is determined by the potential barrier of surface potentials under the adjacent gates. Considering the charge packet shown shaded in Figure 2.4(a), from Equation (2.3), we can obtained, the charge handling capacity of a CCD gate is given by:

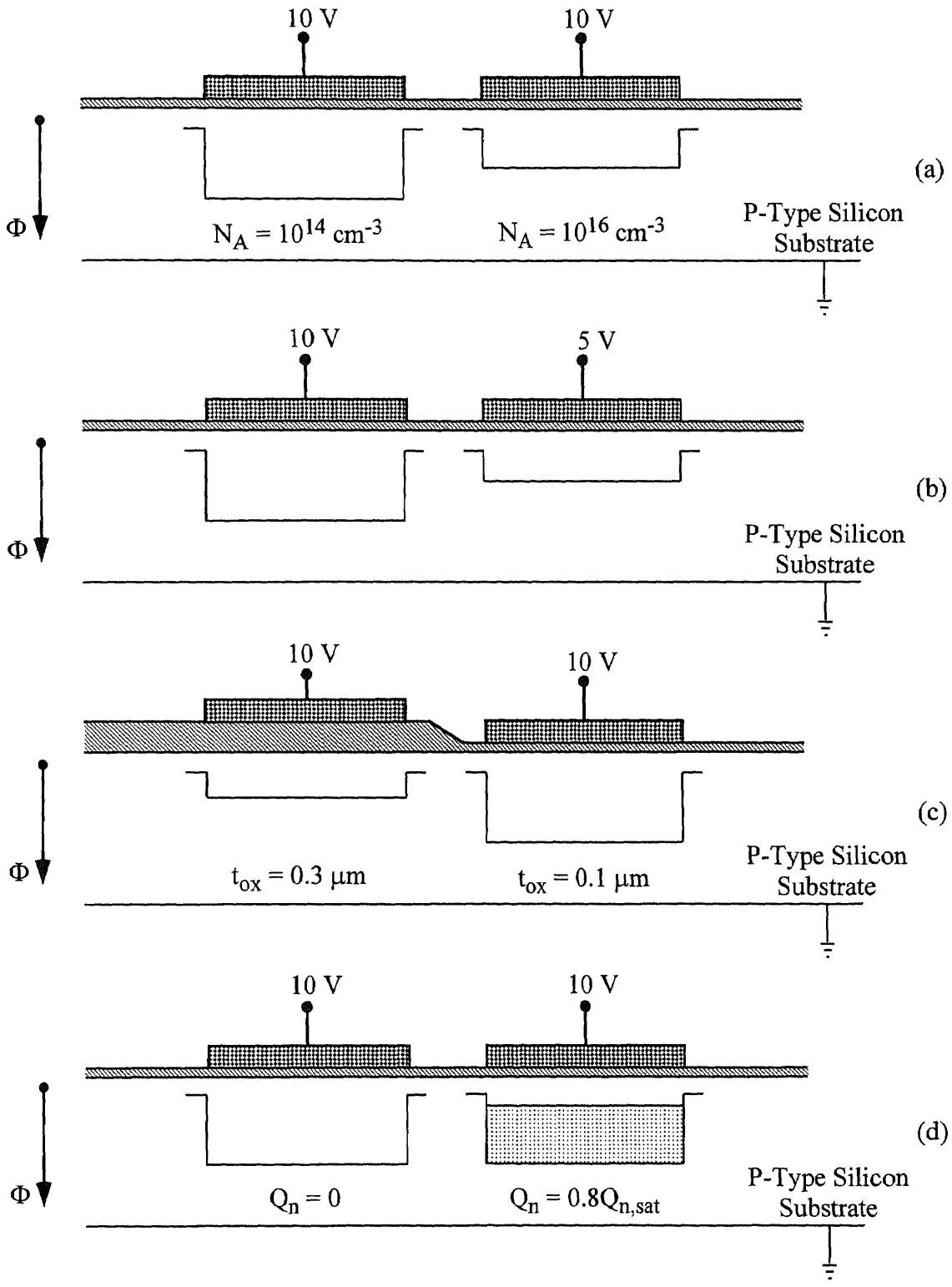


Figure 2.3 *Influence of different parameters on the surface potential:* (a) *the substrate doping;* (b) *the gate voltage;* (c) *the gate dielectric;* and (d) *the free-charge content.*

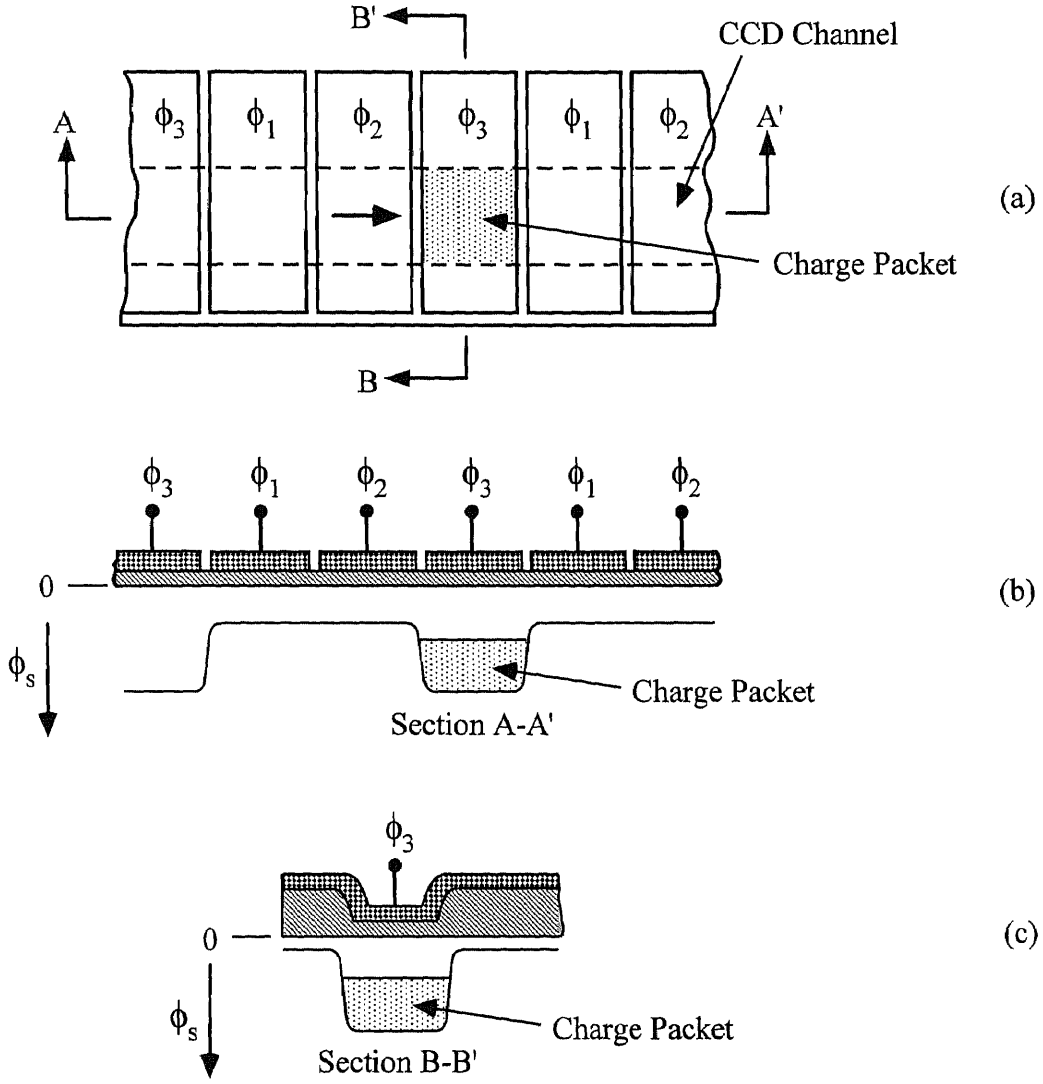


Figure 2.4 *Charge confinement in a CCD. The charge is the shaded region in* (a). *It is confined along A-A' by the gate potentials, with* $V_{G3} > V_{G1} = V_{G2}$, *in* (b), *and along B-B' by the two different oxide thickness in* (c).

$$Q_{n,max} = -A \cdot C_{ox} \cdot (V_{GS} - V_{GB}) \,, \tag{2.5}$$

where A is the area of the CCD gate, V_{GS} is the voltage applied to the storage gate, and V_{GB} is the voltage applied to the barrier gates on both sides of the storage gates. In the transfer direction, the charge is confined by the gate voltages, as shown in Figure 2.4(b).

On the other hand, in order for the charge to be confined to the channel, it is necessary for the surface potential of the channel to be higher than the surface potential of the lateral region adjacent to it, referred to the channel stop. An inspection of Figure 2.3 shows that either a thicker oxide or an increased doping concentration brings this about. The lateral charge confinement by a thicker oxide channel stop is shown in Figure 2.4(c).

As mentioned in the Section 2.2, the BCCD is formed by an extra n-type top doping of the p-type silicon substrate. If the doping concentration is chosen such that the n-type layer is fully depleted during operation of the BCCD, a potential minimum is created in the n-layer, away from the Si/SiO_2 interface. The signal charge is stored as majority carriers in the potential minimum, surrounded by depleted n-type regions.

Due to the fact that BCCD stores its charge in the bulk of the silicon, its charge handling capacity is smaller than that of SCCD. Figure 2.5 shows cross sections of CCD cells of a SCCD and BCCD register. In the case of a SCCD the signal charge resides at the node between the oxide capacitance C_{ox} and the depletion capacitance C_D, at the

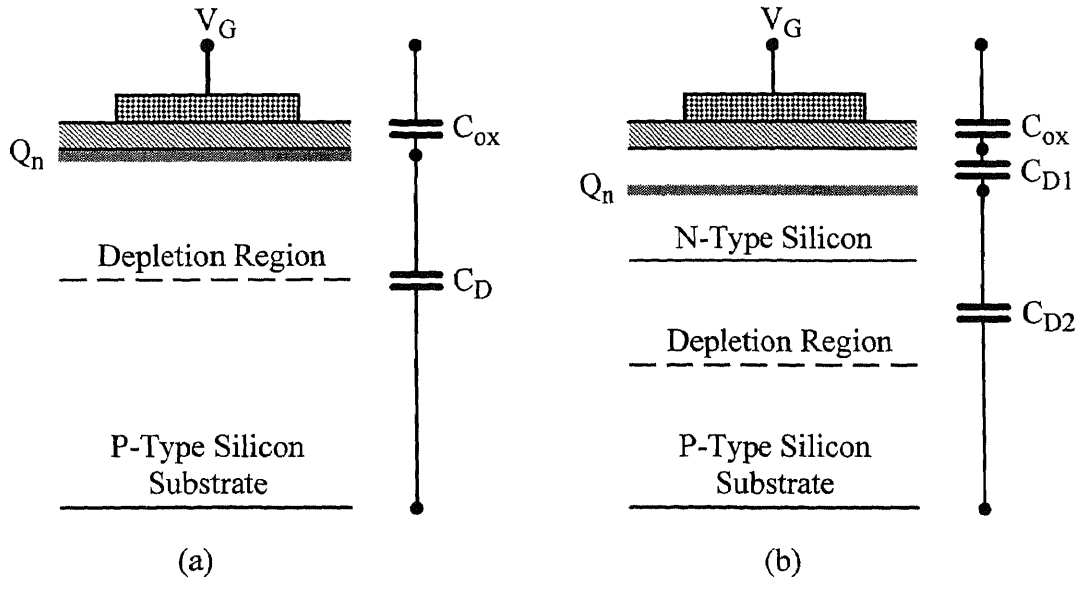


Figure 2.5 *Indication of the charge storage site in a CCD cell from a SCCD register in* (a) *and a BCCD register in* (b).

Si/SiO_2 interface. The maximum charge handling capacity is given by Equation (2.6). Whereas the capacitance above the charge packet is only C_{ox}, in a BCCD this capacitance is a serial combination of the oxide capacitance C_{ox} and the depletion capacitance C_{D1}, as shown in Figure 2.5(b). The maximum charge handling capacity for the BCCD is given by:

$$Q_{n,max} = -A \cdot \left(\frac{C_{ox} \cdot C_{D1}}{C_{ox} + C_{D1}} \right) \cdot (V_{G2} - V_{G1}) \, . \tag{2.6}$$

On the other hand, the channel stop for the BCCD can be formed by the p-doped SCCD in the lateral region adjacent to it.

2.5 Charge Transport in CCD

The charge packets stored in the CCD cell can be transferred through the silicon from one gate to another by shaping and reshaping the form of potential well. Figure 2.6 illustrates the transfer of a charge packet from one gate to another [42]. To start with, the gates are biased to 0 V, except the second gate is biased at 10 V. Electrons, if available, will gather in this potential well. This situation is depicted in Figure 2.6(a). At the onset of the charge transfer, shown in Figure 2.6(b), the third gate in the row is set to 10 V, and a new potential well is created underneath the third gate. If the two positive-biased gates are closely spaced, the individual potential wells under these gates will mix, forming just a single wide bucket. The electrons will flow to the deepest point in the buckets, and, in the enlarged bucket from Figure 2.6(b), the charge packet will be redistributed across the whole width of the potential well. The ultimate result is shown in Figure 2.6(c), where the packet of electrons is spread out across the second and third gates. The next step is to push the charge packet away from the second gate. In the next step of operation the charge packet is pushed away from the second gate. This is done in the way opposite to that used previously to attract the electrons. For the gate voltage on the second gate

lowered from 10 V to 5 V and then to 0 V, the transfer of charge signal from the potential well under the second gate is illustrated in Figures 2.6(d) and 2.6(e), respectively.

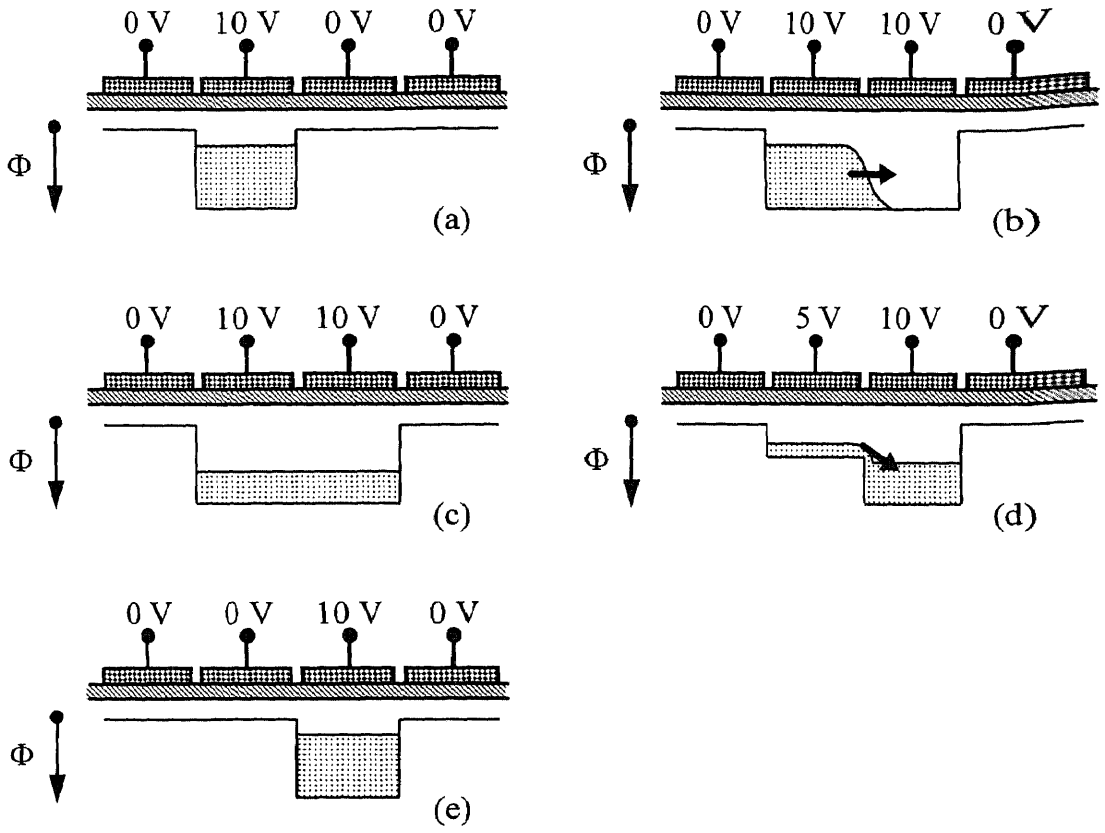


Figure 2.6 *Illustration of the charge transport in a CCD. The charge packet of electrons is moved through the silicon by means of digital pulses applied on the CCD gate.*

Note that, during this complete process of charge transport, the gate voltages on the first and forth gate did not change. This is quite important in order to keep the charge packet under consideration isolated from the other charge packets on its left and right side.

The movement of free carriers, in this case electrons, is driven by three mechanisms [49]: the thermal diffusion of charge carriers, self-induced fields, and fringing fields. From the analytical point of view, the charge transport of the electrons

through a CCD channel can be described by means of the current density and continuity equations. The current density equation can be written as:

$$\mathbf{J}(y,t) = \mathbf{J}_d + \mathbf{J}_s + \mathbf{J}_f \ , \tag{2.7}$$

where $\mathbf{J}(y,t)$ is the current density created by the movement of the charge packet, as a function of distance (y) and time (t). $\mathbf{J}_d$, $\mathbf{J}_s$, and $\mathbf{J}_f$ are the current densities of the thermal diffusion part, the part due to the self-induced fields, and the part resulting from the fringing fields, respectively. These three components are given by the classical expression for diffusion current and drift current generated through the action of an electrical field [50]:

$$\mathbf{J}_d = q \cdot D_n \cdot \nabla_{\mathbf{Y}} Q_n(y,t) \tag{2.8}$$

with D_n the diffusion constant of electrons and $Q_n(y,t)$ the charge distribution as a function of distance and time,

$$\mathbf{J}_s = Q_n \cdot \mu_n \cdot \mathbf{E}_s \tag{2.9}$$

with μ_n the mobility of electrons and $\mathbf{E}_s$ the self-induced electric field, and

$$\mathbf{J}_f = Q_n \cdot \mu_n \cdot \mathbf{E}_f \tag{2.10}$$

with $\mathbf{E}_f$ the fringing field.

Charge carriers transferred from one position to another define the current between these two positions. The continuity equation connects the amount of charge to be transferred with current density and is given by [49]:

$$\frac{\partial Q_n(y,t)}{\partial y} = \nabla_{\mathbf{Y}} \cdot \mathbf{J}(y,t) \ . \tag{2.11}$$

This relation is only valid if no extra charge carriers are added or subtracted from the original charge packet or the recombination and the generation of the charge carriers is not considered. If the transport of the charge packet is fast enough, the rate of total

amount of charge carrier generation and recombination is negligible relative to the total amount of charge of the charge carriers in the charge packet.

It is a rather complicate problem to solve the complete analytical solution for the charge transfer involving simultaneously thermal diffusion, self-induced drift, and fringing field. However, it is informative to consider the three mechanisms separately.

Thermal Diffusion

Even in the absence of any electric field, a charge packet which has the possibility to redistribute its local gradient toward an equilibrium situation will do so by means of thermal diffusion. This effect can be studied by introducing the current-density relation (2.8) into the continuity equation (2.11), and solving the partial differential equation. The solution is given by [49]:

$$Q_n(t) = \frac{8}{\pi^2} \cdot Q_n(0) \cdot e^{-\frac{\pi^2 \cdot D_n \cdot t}{4 \cdot L^2}} . \qquad (2.12)$$

In this expression the parameter L represents the length of a single gate, which is its dimension in the direction of charge transfer. The diffusion constant D_n can be related to the mobility of the charge carrier μ_n through:

$$D_n = \frac{kT}{q} \mu_n . \qquad (2.13)$$

As can be seen from Equation (2.12), the remaining charge packet $Q_n(t)$ decreases exponentially from its starting value $Q_n(0)$. The time constant of the process is inversely proportional to the diffusion constant D_n and proportional to L^2. With this exponential decay, only a first small part of the charge packet will move relatively fast, but the remaining packet needs some time to be transported to the next stage in the CCD. The transport mechanism based on thermal diffusion is enhanced if the diffusion constant D_n is increased and if the gate length is made as small.

Self-Induced Drift

In general, a gradient in charge concentration built up by charges of the same type will repel the charges to reshuffle their concentration so that the gradient will become zero. This reordering will take place through the electric field generated by the gradient in charge distribution. In case of the self-induced field alone, the continuity equation (2.11) can by written as:

$$\frac{\partial Q_n(y,t)}{\partial t} = \frac{\partial}{\partial y}(Q_n \cdot \mu_n \cdot E_s^y) \,. \tag{2.14}$$

As can be seen from Figure 2.6(b), the presence of a charge gradient underneath two neighboring gates at the same potential cause a change in surface potential Φ_S under the gates and consequently produces an electric field $\mathbf{E}_s$. The surface potential along the CCD channel $\Phi_S(y)$ as a function of $Q_n(y)$ can be determined sufficiently accurately using one dimensional Poisson equation. Compared to the transport of charges by thermal diffusion, the process involved in the self-induced fields looks similar. And both thermal-diffusion and self-induced drift processes can be combined using a single, effective diffusion constant D_{eff} given by [43]:

$$D_{eff} = \left(\frac{Q_n \cdot kT}{q(C_{ox} + C_D)} + 1 \right) \cdot D_n \,. \tag{2.15}$$

Due to the presence of self-induced fields, the total diffusion of charge carriers during the transport phase becomes much faster compared to the case of thermal diffusion only. Especially if the charge packet is greater than 1% of the saturation level. But in the case of a very small charge packet (e.g. $Q_n < 0.01\ Q_{n,sat}$), the net transport process is completely determined by the thermal diffusion of the carrier, and becomes slow again. So the self-induced drift current is important only during the initial period of the charge transfer as long as Q_n is sufficiently large and comparable to $Q_{n,sat}$.

Fringing Fields

A practical device can be operated much faster than described by the previous theory of thermal diffusion and self-induced drift. This can be accomplished by electric field generated by the voltages on the gates. These fringing fields, along the direction of charge flow, can arise from the two dimensional nature of the structure for the case of a short gate length.

The occurrence of the fringing fields is schematically shown in Figure 2.7. In Figure 2.7(a), the surface potential is depicted as a series of rectangular buckets but a more realistic curve for the surface potential is shown in Figure 2.7(b). The last situation is only valid if the spacing between two adjacent gates is small enough (e.g. comparable to the oxide thickness) and if the length L of the gates is not too long (e.g. less than 10 μm).

An empirical approximation for the minimum value of the fringing field $E_{f,min}$ at the middle of the transferring electrode in a CCD cell built with three gates is found to be equal to [42]:

$$E_{f,min} = A \cdot \frac{t_{ox}}{L^2} \cdot \frac{\Delta V}{2} \cdot \left[\frac{5 \cdot x_d / L}{(5 \cdot x_d / L) + 1} \right]^4, \tag{2.16}$$

where, A is a constant equal to 6.5, ΔV is the voltage swing on the gate during the charge transfer, and x_d is the width of the depletion layer. A smaller gate length gives a much higher fringing field and a significant improvement in transfer efficiency. The fringing field effect is very important in transferring the final 1% of the charges during the charge transport.

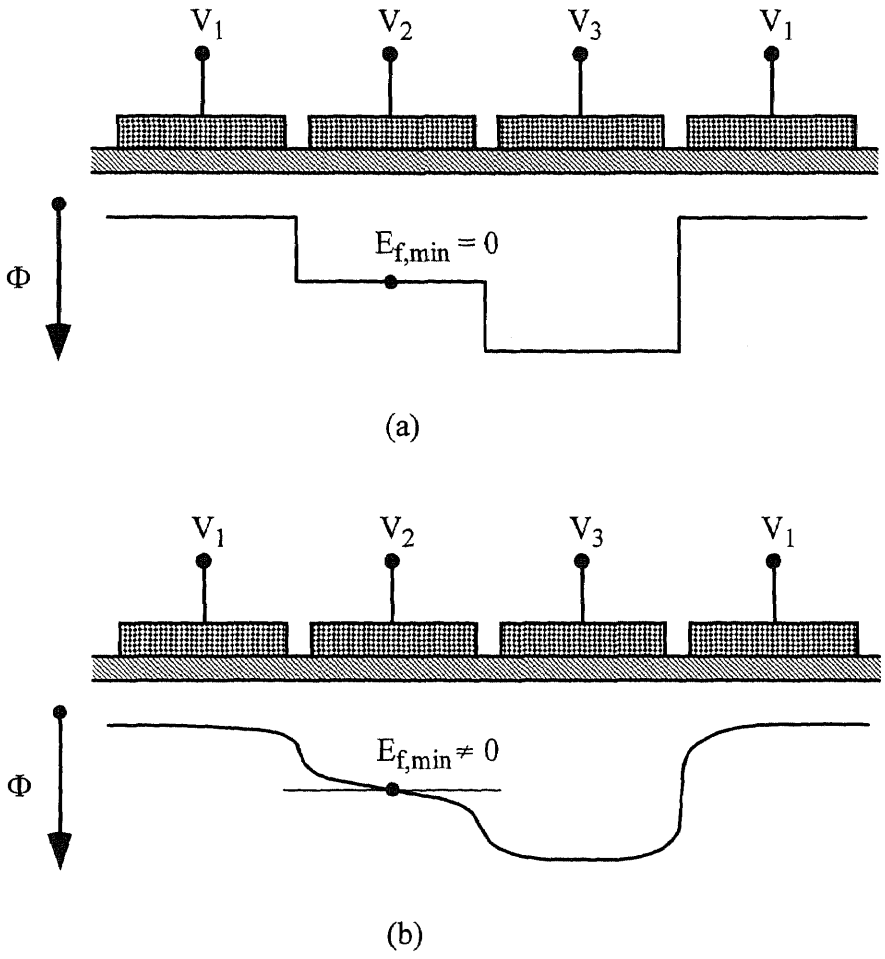


Figure 2.7 *Schematic illustration of the surface potential without* (a) *and with* (b) *fringing fields* ($V_1 < V_2 < V_3$).

Summary

In summary, the transport of a charge packet from one gate to another through a charge-coupled device is based on the three different mechanisms:

- self-induced drift to redistribute the charge content which is responsible for a fast transfer of the very first charge carriers, and
- thermal diffusion, which is characterized by a relatively slow charge transport, followed by

- fringing-field induced drift, which can be much faster than the thermal diffusion in sweeping up the remaining part of the charge packet.

Compared with the fringing field transfer, the self-induced drift followed by thermal diffusion results in a rather slow charge transfer process. Therefore, to operate charge-coupled devices at high speed, cares has to be taken during the design and operation of the devices to derive maximum benefit from the presence of the fringing field.

In this dissertation, a complete solution of the charge transport was obtained by numerical solutions described in Chapters 6 and 7.

CHAPTER 3

INTRODUCTION TO PROCESS AND DEVICE SIMULATION

3.1 Introduction

With the fast development of VLSI technologies, the performance of the CCD image sensors have been improved to meet the requirements of different applications. The use of computer-aided design tools has proven to be invaluable in the development of new technologies and in IC design (which also includes the CCD design). In general, a CCD process contains ten to twenty layers of masks and several hundred individual steps. Computer simulations have emerged as a very elegant way to aid us in our task of finding an optimum process to fabricate the CCD imager.

This chapter gives an introduction to the process and device modeling of the semiconductor IC design, especially in the CCD technology. After a brief review on CCD modeling, this chapter presents the general theoretical aspects of semiconductor process and device characterization analysis. Then, a general description is given on the process and device simulation software which were used in this dissertation for the design of VHFR burst-image sensor. However, it is beyond the scope of this dissertation to describe the numerical algorithms, or to explain the user interfaces, all of which are explained in the user's manual.

3.2 Review of CCD Modeling

During the development of CCDs, a number of theoretical studies has been done on the simulation of the CCD structures. The simulation of CCDs has been approached in two different ways: one is analytical and the other is using numerical methods.

The analytical approach to CCD simulation can be obtained using a closed form or a Fourier series which can be easily and efficiently computed. Once the solution is

identified, the parameters can be changed without having to re-work the problem. But such an approach requires many approximations or assumptions restricting its application to particular CCD structures.

The numerical approach is a general method to simulate the semiconductor devices (which also includes CCD structures) which solves the fundamental Poisson and sometimes the current continuity equation with the boundary conditions over a particular geometry. Since it is underlying physical phenomena that is being solved, one can predict quite accurately the operation of the device. CCD devices operate in the non-equilibrium regime, this added complication requires a good understanding of the quasi-Fermi levels and the techniques involved in controlling the CCDs. These levels are instrumental in controlling the size of the charge packet. The freedom in choosing arbitrary doping profiles makes this approach very attractive (especially for the 2-D simulation). However, such a flexibility comes with a cost in terms of the human effort put into describing the geometry and the computation time which risks to be quite high when solving the full two-carrier problem. Another problem (occasionally) is that of non convergent situations.

Both the analytical and numerical approaches of CCD modeling has been started in the early 1970's, the time of the invention of CCD concept. In analytical approaches, Boyle and Smith [7], the inventor of CCD, described the SCCD one-dimensional (1-D) model for a uniformly doped device with respect to charge packet size. Carnes et al [50] used the Fourier series and the zero space charge approximation to describe the two-dimensional (2-D) potential distribution in the oxide and in the silicon for an SCCD having a periodic arrangement of the electrode. In numerical approaches, Engeler et al [51], [52], Kim et al [53], [54] formulated the models for the charge transfer due to the self-induced drift field and the thermal diffusion for a SCCD and then numerically solved the 1-D model. Carnes et al [49], [50], modeled the lateral fringing field effects for SCCD. After then, a number of studies on modeling of CCD structures has been conducted during the later 1970's and 1980's.

The rapidly development of computer technology which includes the high computation speed and large calculation capacity, provided a powerful tools for obtaining the numerical solution of the complex mathematics expressions. More work on the numerical modeling of the CCD structures has been conducted recently. Banghart et al [55] performed modeling the CCD charge transfer at low temperature based on the Schockley-Read-Hall recombination-generation theory. The model simulated the general temperature, voltage swing, and signal level dependencies of the experimentally observed charge transfer efficiency in a BCCD. Using Gaussian doping profile with offset peaks, Washkurak et al [56] calculated the potential profile and charge including the effect of charge storage within the channel. On the other hand, the development of process and device simulators provided another useful tool for the modeling of the CCD structures.

SUPREM III (1-D process) [57], SUPREM IV (2-D process) [58], and PISCES IIB (2-D device) [59] are public domain simulators. By using these simulators, J. Pinter et al [60] and the author [61] calculated the maximum charge handling capacity, voltage swing, fringing field of the 1- and 2-D BCCD structures. Some internal simulation software were also used in the modeling of the CCD structures. Olympus Semiconductor Technology Center presented the operational mechanism of the charge modulation device image sensor by using TRINE [62], [63]. CCD group of Philips Imaging Technology using 3-D device simulator PADDY [64], [65] optimized the charge handling capacities and sensitivities of their imagers.

3.3 Process Modeling

The basic process steps used in the CCD fabrication are similar to that of IC fabrication. The process modeling used to predict the device structures includes ion implantation, diffusion, oxidation, deposition, etching, and etc. Some of the theoretical approaches are discussed by S. M. Sze et al [66], [67] are briefly described in this section.

3.3.1 Ion Implantation

The conduction properties of semiconductors can be changed by introducing small quantities of dopant atoms. Ion implantation is a method of introducing the dopant that is controllable, reproducible, and free from undesirable side effects. During ion implantation, dopant atoms are vaporized, accelerated, and directed at a silicon substrate. They enter the crystal lattice, collide with silicon atoms, and gradually lose energy, finally coming to rest at some depth within the lattice. The average depth can be controlled by adjusting the acceleration energy. The dopant dose can be controlled by monitoring the ion current during implantation. The principle side effect — disruption of the silicon lattice caused by the ion collisions — is removed by subsequent heat treatments.

Each implanted ion has a random path as it moves through the target, losing energy by nuclear and electronic stopping. We are considering an ion descending vertically and entering a horizontal silicon surface. The distribution of ions about the average depth of the implanted ions, the projected range R_p, can be approximated as Gaussian distribution with standard deviation σ_p. The lateral motion of the ions leads to a lateral Gaussian distribution with standard deviation $\sigma_\perp$.

Far from a mask edge, we can neglect the lateral motion and write the ion concentration $n(x)$ as:

$$n(x) = \frac{\Phi}{\sqrt{2\pi}\sigma_p} \cdot \exp\left[\frac{-(x-R_p)^2}{2\sigma_p^2}\right]. \tag{3.1}$$

In general, an arbitrary distribution $n(x)$ can be characterized in terms of its moments. The normalized first moment of an ion distribution is the projected range. The higher moments taken from R_p is given by:

$$m_i = \frac{1}{\Phi}\int_{-\infty}^{\infty}(x-R_p)^i \cdot n(x) \cdot dx \ . \tag{3.2}$$

The second, third, and forth moments are typically expressed in terms of the following parameters:

$$\text{(standard deviation)} \quad \sigma_p = \sqrt{\frac{m_2}{\Phi}} ,$$

$$\text{(stewness)} \quad \gamma = \frac{m_3}{\sigma_p^3} , \text{ and}$$

$$\text{(kurtosis)} \quad \beta = \frac{m_4}{\sigma_p^4} .$$

Gaussian distributions have a skewness of 0 and a kurtosis 3.

Several different distributions have been used to give a more accurate fit to the moments of an ion distribution than is possible using a Gaussian. The most popular of these is Pearson family of distributions, used in statistics, which is given by the solution of:

$$\frac{df(s)}{ds} = \frac{(s-a)\cdot f(s)}{b_0 + b_1 s + b_2 s^2} , \tag{3.3}$$

where $s = x - R_p$. The Pearson coefficients can be written in terms of the first four moments of the distribution:

$$a = -\gamma \cdot \sigma_p \cdot (\beta + 3) / A , \tag{3.4a}$$

$$b_0 = -\sigma_p^2 \cdot (4\beta - 3\gamma^2) / A , \tag{3.4b}$$

$$b_1 = a , \tag{3.4c}$$

$$b_2 = -(2\beta - 3\gamma^2 - 6) / A , \tag{3.4d}$$

where $A = 10\beta - 12\gamma^2 - 18$. There are seven different types of solution to Pearson's equation, depending on the values of the coefficients. For implantation profiles, the most commonly used is Pearson-IV, which applies when the coefficients satisfy $0 < b_1^2 / 4 b_0 b_2 < 1$. Integrating Equation (3.3) for a Pearson-IV solution gives,

$$\ln\left[\frac{f(s)}{f_0}\right]=\frac{1}{2b_2}\ln(b_0+b_1s+b_2s^2)-\frac{b_1/b_2+2b_1}{\sqrt{4b_0b_2-b_1^2}}\tan\left(\frac{2b_2s+b_1}{\sqrt{4b_0b_2-b_1^2}}\right). \quad (3.5)$$

The range data for different ion-target combinations have been derived and are available in the literature [68], [69]. In the CCD process, however, it is quite common to implant into a non-planar substrate that is covered by one or more thin layers of different materials. Typical examples are threshold-adjust implants, channel-stop, source/drain, and BCCD implants, into gate- and field-oxide regions, which may be covered by SiO_2 or Si_3N_4. The existence of multilayered structures results in implant profile discontinuities at the interface between layer. Additional, atoms from surface layers may be knocked into deeper layers by impinging ions. Considering the above effects, the Monte Carlo[70] and Boltzmann transport equation[71], [72] methods are widely used to simulate ion implantation phenomena in solids.

3.3.2 Diffusion

As the semiconductor undergoing a high temperature (usually in the range from 800 to 1200°C for silicon) process, the impurities are diffusing and being redistributed in the semiconductor. In full generality, impurity diffusion in silicon is described by the following set of equations:

- Flux equations for all charge particles:

$$\mathbf{J}_i=-D_i\cdot\nabla S_i+Z_i\mu_iS_i\mathbf{E}\,, \quad (3.6)$$

  where $\mathbf{J}_i$ is the particle flux, S_i stands for the concentration of diffusing species (donors, acceptor, interstitials, vacancies), S_i and μ_i are the corresponding diffusivities and mobilities, respectively, Z_i is the charge state, and $\mathbf{E}$ is the electric field.

- Continuity equations for all charged particles:

$$\frac{\partial S_i}{\partial t}+\nabla\cdot\mathbf{J}_i=G_i, \quad (3.7)$$

where G_i stands for the generation-recombination rate.

- Poisson's equation:

$$\nabla \cdot (\varepsilon \mathbf{E}) = q(p - n + N_D^+ - N_A^- + \text{other charged species}), \tag{3.8}$$

where n and p are the electron and hole density, respectively, ε is the dielectric premittivity, and N_D^+ and N_A^- are the ionized donor and acceptor concentration, respectively.

The diffusion of a substitutional impurity in silicon is governed by the local concentration of point defects [73], with diffusivity:

$$D = D_I^i \frac{C_I}{C_I^{eq}} + D_V^i \frac{C_V}{C_V^{eq}}, \tag{3.9}$$

where D_I^i and D_V^i are the intrinsic diffusivities of the impurity atoms, C_I and C_V are the concentrations of interstitials and vacancies, and C_I^{eq} and C_V^{eq} are the corresponding equilibrium values. This equation can be written as:

$$\frac{D}{D^i} = f_I \frac{C_I}{C_I^{eq}} + (1 - f_I) \frac{C_V}{C_V^{eq}}, \tag{3.10}$$

where $f_I = D_I / (D_I + D_V) = D_I^i / D^i$. Equation (3.10) assumes that the diffusivity of an impurity in silicon is proportional to the concentrations of vacancies and interstitials weight by the interstitialcy component f_I.

In most cases, Equation (3.8) can be eliminated by assuming local charge neutrality, $\nabla \cdot \mathbf{E} = 0$. For a two-dimensional problem, Equation (3.7) has to fulfill a set of initial and boundary conditions [74]:

Condition 1:

$$C_i(x, z, 0) = f(x, z); \tag{3.11a}$$

Condition 2:

$$C_i(x, \infty, t) = 0, \text{ or}$$
$$C_i(x, \infty, t) = C_B \text{ (= bulk concentration)}; \tag{3.11b}$$

Condition 3: No impurity flux is allowed along the lines of symmetry ($x = x_R$ and $x = x_L$),

$$\frac{\partial C_i}{\partial x} = 0 \text{ for } x = x_R \text{ and } x = x_L ; \tag{3.11c}$$

Condition 4: The boundary condition at the surface depends on whether the surface is being oxidized,

$$D_i \frac{\partial C_i}{\partial z}\bigg|_{z=0} = C_i\left(\frac{1}{m} - b\right)\cdot\frac{dz}{dt} \quad , \tag{3.11d}$$

or is exposed to an impurity gas source:

$$D_i \frac{\partial C_i}{\partial z}\bigg|_{z=0} = h\cdot(C_i - C_i^*). \tag{3.11e}$$

In Equation (3.11d), m is the segregation coefficient, given by the ratio of the dopant concentrations in silicon and SiO_2,

$$m = \frac{C_i^{\mathrm{Si}}}{C_i^{\mathrm{SiO_2}}} , \tag{3.12}$$

and b accounts for the volume change associated with the formation of SiO_2. Equation (3.11d) is valid under the assumption that the diffusion coefficient in the oxide is much smaller than in the silicon. If this is not true, Equation (3.11d) must be modified, and Equation (3.8) has to be solved also in the oxide. In Equation (3.11e), h is the mass transfer (or evaporation) coefficient and C^* is the dopant concentration in the gas phase.

The diffusion coefficient D_i in Equation (3.11d) is, in general, a function of the concentrations, of the impurities for high dopant concentrations. All process simulation programs reported include the concentration dependence of D_i obtained from the vacancy-diffusion model:

$$D_i = D_i^x + D_i^- f + D_i^= f^2 + \frac{D_i^+}{f} , \tag{3.13}$$

with $f = N/n_i$. The variables D_i^x, D_i^-, $D_i^=$, and D_i^+ are neutral, single negative, double

negative, and positive vacancy states in silicon, respectively. N is the electron concentration that depends on all C_i, and n_i is the intrinsic concentration at the diffusion temperature.

At low impurity concentrations, N is approximately equal to n_i and the diffusion coefficient reduces simply to the sum of the various vacancy states, independent of concentration:

$$D_i = D_i^x + D_i^- + D_i^= + D_i^+. \tag{3.14}$$

The individual diffusivities in Equation (3.13) or (3.14) are given by Arrhenius form:

$$D_i^* = D_{i0}^* \cdot \exp\left(-\frac{Q_i^*}{kT}\right), \tag{3.15}$$

with the prefactor D_{i0}^* and the active energy Q_i^*.

The electron concentration N can be approximated by:

$$N = \frac{C_{\text{net}} + \sqrt{C_{\text{net}}^2 + 4n_i^2}}{2}, \tag{3.16}$$

with

$$C_{net} = -\sum_{i=1}^{n} Z_i N_i, \tag{3.17}$$

where Z_i and N_i stand for the valence and concentration, respectively, of species i.

Diffusion of all important group III (Boron) and group V (Arsenic, Antimony) elements in silicon is described well by the above diffusion model. The diffusion of phosphorus, however, is governed by a rather complex diffusion behavior and is modeled by the three region model [75], which includes the high-concentration region, the transition region (often called the *kink* of the profile), and the low-concentration region (the tail region).

3.3.3 Oxidation and Segregation

In thermal oxidation, oxidant from the gas phase diffuses in the form of oxygen (dry oxidation) or water vapor (wet oxidation), through holes in the SiO_2 network toward the interface to form new SiO_2 material. This *growth* is accompanied by a large volume increase. At sufficient high temperature, the reaction is aided by viscoelastic flow of the oxide film towards the surface.

For one-dimensional problems, the growth rate of SiO_2 on top of Si can be obtained by integrating the oxygen flux that diffuses through an SiO_2 layer of thickness d_{ox} to react at the surface:

$$d_{ox}^2(t) + A \cdot d_{ox}(t) = B \cdot (t + \tau) \; . \tag{3.18}$$

where A and B are the rate constants and τ accounts for the initial oxide thickness at time t_0 (e.g. a natural oxide, etc.).

Whereas oxidation simulation in one dimension has been successful, no well-established theory is available at this point that would allow a first-principles solution of two-dimensional oxidation phenomena. Typical example would be the lateral oxidation near a mask edge, giving rise to the bird's beak phenomenon. Several numerical models, such as coordinate transformation method [74], viscous flow model [76], [77], and elastic model [78], are available that allow approximate numerical solutions in two dimensions.

3.3.4 Etching and Deposition

Etching and deposition are internal process steps in any modern silicon technology, such as the patterning of resist, polysilicon, deposition of polysilicon, dielectric, and metal layers. No basic physical theories exist that would allow first-principles solutions of etching and deposition processes. To circumvent this problem and to obtain some answers through simulation, the modeling of etching and deposition steps can be viewed as a purely geometric problem. The resulting shape of the surface is determined by an

initial profile which moves through the medium at a speed depending on the position and other variables such as etching and deposition rates, .

Etching

There are several etching methods in the semiconductor processes. Wet chemical etching is used extensively in semiconductor processing. The wet chemical etching processes for the amophrous layer (such as oxide, nitride and metal) and polysilicon are isotropic etches. Some etchants dissolve a given crystal plane of a semiconductor much fast than the other plane, this results in orientation-dependent etching. If the patterns are required a very small resolution, anisotropic etching must be used. Dry etching, such as plasma-assisted etching, are commonly used for high-fidelity transfer of the resist patterns.

To simulate the etching process, etching rates have to be defined explicitly. The rates are defined for etch material and separately for the isotrope and the ionic beam fraction. Etching simulation is done, assuming several ionic beams, having different incident angles. The shadow of each of the beams is computed. The etch rate in a point (x, y) in the direction ϕ (ϕ is the angle between the etching direction surface normal) is given by [79]:

$$r = \sum_{j=1}^{k} b_j(x,y) d_j \sum_{i=1}^{3} a_i(m) \cos^i(\alpha_j - \phi) + d \cdot i(m) \ . \qquad (3.19)$$

Here, m denotes the material of the point, k the number of the beam, $b_j(x, y)$ is 1, if the point is exposed by the beam j, otherwise is given be a shadow factor between 0 and 1. d_j define the dose, and α_j defined the incident direction of the beam j. $a_i(m)$ denote the (material dependent) rate coefficients, d is the isotropic dose and $i(m)$ the isotropic rate.

Deposition

There are four commonly used deposition methods: atmospheric-pressure chemical vapor deposition (CVD), low-pressure chemical vapor deposition (LPCVD), and plasma-assisted chemical vapor deposition (PCVD, or plasma deposition) and sputtering. Considerations in selecting a deposition process are the substrate temperature, the deposition rate and film uniformity, the morphology, the electrical and mechanical properties, and the chemical composition of the deposition film.

3.4 Device Modeling

The three governing equations for charge transport in semiconductor devices are the Poisson's equation and the continuity equations for electrons and holes. At the same time, a suitable value of the parameters (such as mobility, generation and recombination rate, intrinsic density, and boundary conditions) have to be carefully considered in order to simulate the performance of the semiconductor devices for different applications. The theoretical approach of the device modeling discussed by S. M. Sze et al [67], [80] and the consideration of the suitable parameter values discussed by M. Pinto et al [60] are briefly described in this section.

3.4.1 Transport Equations

The electrical behavior of semiconductor devices is governed by Poisson's equation:

$$\varepsilon \cdot \nabla^2 \psi = -q(p - n + N_D^+ - N_A^-) - \rho_F \,, \tag{3.20a}$$

and the continuity equations for electrons and holes:

$$\frac{\partial n}{\partial t} = \frac{1}{q} \nabla \cdot \mathbf{J}_n - R \,, \tag{3.20b}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q} \nabla \cdot \mathbf{J}_p - R \,. \tag{3.20c}$$

The primary function of device simulator (such as PISCES IIB) is to solve these three partial differential equations self-consistently for electric potential, ψ, and the electron and hole concentrations, n and p, respectively. In PISCES IIB, ψ is always defined as the intrinsic Fermi potential, i.e. $\psi = \psi_i$. N_D^+ and N_A^- are the ionized donor and acceptor concentrations, respectively, and ρ_F. $\mathbf{J}_n$ and $\mathbf{J}_p$ are the electron and hole current densities. G_n and G_p are the electron and hole generation rate, respectively, and R is the net electron-hole recombination rate.

The typical dimensions of silicon CCD gates and photodetectors are in the range of several micron to one hundred micron, and the charge transfer time in silicon CCDs is in the range of one nanosecond to several microseconds, thus, present-day silicon based CCD for imaging application can be well described by the drift-diffusion model.

The transport equations are used when modeling CCD charge transfer efficiency, photodetector readout, lateral and vertical antiblooming current, and CCD input and output. Figure 3.1 illustrates the first two situations.

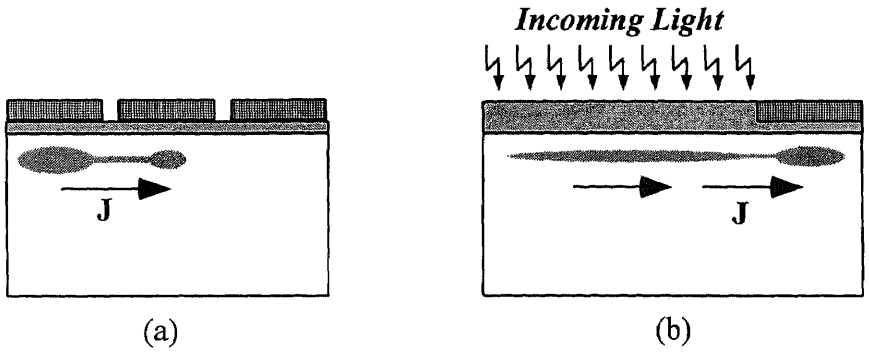


Figure 3.1 *Illustration of two typical CCD problems that require the solution of the transport equations in additional to Poisson's equation.* (a) *Charge transfer between electrodes which determines the charge transfer efficiency for CCDs;* (b) *Charge readout from photodetector to the electrode in determine the charge transfer time.*

From Boltzmann transport theory, the electron and hole currents can be written as functions of ψ, n and p, consisting of drift and diffusion components:

$$\mathbf{J}_n = -q\mu_n n\nabla\psi + qD_n\nabla n \,, \tag{3.21a}$$

$$\mathbf{J}_p = -q\mu_p p\nabla\psi - qD_p\nabla p \,, \tag{3.21b}$$

where μ_n and μ_p are the electron and hole mobilities, and D_n and D_p are the electron and hole diffusitivities.

If the temperature distribution in the device is not uniform, an extra term in the current equation must be included to take into account the flowing of current due to the gradient of the temperature:

$$\mathbf{J}_n = -q\mu_n n(\nabla\psi + P_n\nabla T) + qD_n\nabla n \,, \tag{3.22a}$$

$$\mathbf{J}_p = -q\mu_p p(\nabla\psi + P_p\nabla T) - qD_p\nabla p \,, \tag{3.22b}$$

where P_n and P_p are the absolute thermoelectric power and T is the temperature [81].

3.4.2 Carrier Statistics and Reference Potential

It is very important to have a clear understanding of carrier statistics in order to manipulate general purpose device simulators and solve for non-equilibrium CCD devices. The analysis in this section is valid for both equilibrium and non-equilibrium states.

The electron and hole concentrations in semiconductors are defined by Fermi-Dirac distributions and a parabolic density of states, which, when integrated, yield:

$$n = N_c \frac{2}{\sqrt{\pi}} F_{1/2}\left(\frac{E_{fn} - E_c}{kT}\right), \tag{3.23a}$$

$$p = N_v \frac{2}{\sqrt{\pi}} F_{1/2}\left(\frac{E_v - E_{fp}}{kT}\right), \tag{3.23b}$$

where N_c and N_v are effective density of states in the conduction and valence band, E_c

and E_v are the conduction and valence band energies, E_{fn} and E_{fp} are the are the electron and hole Fermi energies, k is the Boltzmann's constant, and T is the absolute temperature. The effective density of states are given by:

$$N_c = 2\left(\frac{2\pi\ kTm_n^*}{h^2}\right)^{\frac{3}{2}}, \tag{3.24a}$$

$$N_v = 2\left(\frac{2\pi\ kTm_p^*}{h^2}\right)^{\frac{3}{2}}, \tag{3.24b}$$

where m_n^* and m_p^* are the density-of-state effective masses for electron and hole, and h is the Planck's constant. $F_{1/2}(\eta_f)$ is the Fermi-Dirac integral which is defined by:

$$F_{1/2}(\eta_f) = \int_0^\infty \frac{\sqrt{\eta}}{1+\exp(\eta - \eta_f)} d\eta\ . \tag{3.25}$$

For the range of operation of most semiconductor devices, the Fermi energy of electron is several kT below E_c, and Fermi energy of hole is several kT over E_v, the electron and hole concentration can be defined by the simpler expressions, Boltzmann statistics, which are given by:

$$n = N_c \exp\left(-\frac{E_c - E_{fn}}{kT}\right), \tag{3.26a}$$

$$p = N_v \exp\left(-\frac{E_{fp} - E_v}{kT}\right), \tag{3.26b}$$

with $(E_c - E_{fn}) >> kT$ and $(E_{fp} - E_v) >> kT$.

The quasi-Fermi level in the neutral region of the semiconductor can be considered as the reference zero potential. We define the electron quasi-Fermi potential $\phi_n = E_{fn}/q$, and the hole quasi-Fermi potential $\phi_p = E_{fp}/q$. Using the reference zero potential, the electron and hole concentrations can be re-defined as follow:

$$n = n_{ie} \frac{2}{\sqrt{\pi}} F_{1/2}\left[\frac{q}{kT}(\psi - \phi_n)\right], \tag{3.27a}$$

$$n = n_{ie} \frac{2}{\sqrt{\pi}} F_{1/2}\left[\frac{q}{kT}(\phi_p - \psi)\right], \tag{3.27b}$$

for Fermi-Dirac statistics, and

$$n = n_{ie} \exp\left[\frac{q}{kT}(\psi - \phi_n)\right], \tag{3.28a}$$

$$n = n_{ie} \exp\left[\frac{q}{kT}(\phi_p - \psi)\right], \tag{3.28b}$$

for Boltzmann statistics. Neglecting the band-narrowing effect, the intrinsic carrier concentration n_{ie} is given by:

$$n_{ie}(T) = \sqrt{N_c(T)N_v(T)} \exp\left[-\frac{E_g(T)}{2kT}\right], \tag{3.29}$$

where E_g is the band-gap energy of the semiconductor.

Substituting the carrier concentration expressions for Boltzmann statistics, Equations (3.28a) and (3.28b), into the drift-diffusion current densities, Equations (3.21a) and (3.21b) yields:

$$\mathbf{J}_n = -q\mu_n n \nabla\phi_n , \tag{3.30a}$$

$$\mathbf{J}_p = -q\mu_p n \nabla\phi_p . \tag{3.30b}$$

In general, ϕ_n and ϕ_p are solved self-consistently with the current equations, however, they could be set artificially. From equations (3.30a) and (3.30b), we can see, a constant quasi-Fermi potential is equivalent $\mathbf{J}_n = \mathbf{J}_p = 0$. The setting of quasi-Fermi potential is often used in defining the initial non-equilibrium state of the semiconductor device. On the other hand, by artificially setting the quasi-Fermi level, it can introduce a charge package to the CCD without using the contact. For the simulation software do not have the capability of introducing charges by photo-generation, the method of artificially setting the quasi-Fermi level is used to introduce the charge package in the CCD. The

amount of charges under CCD gates can be controlled by varying the quasi-Fermi level, and the Poisson's equation is used to compute the potential profile and carrier distribution. This method is extensively used for the simulation of CCD charge handling capacity in this dissertation.

3.4.3 Boundary Conditions

Four type of boundary conditions are used in the simulation, ohmic contacts, gates contacts, Schottky contacts, and reflective boundaries.

Ohmic contacts can be implemented as simple Dirichlet boundary conditions. The minority and majority carrier quasi-Fermi potentials are equal to the applied bias of the electrode. The surface potential, ψ_s, is fixed at a value consistent with zero space charge, i.e.:

$$n_s - p_s = N_D^+ - N_A^- , \tag{3.31}$$

where n_s and p_s are the surface electron and hole concentrations. If the Boltzmann statistics are used, the surface potential and carrier concentrations are given by:

$$n_s = \sqrt{\frac{(N_D^+ - N_A^-)^2}{4} + {n_{ie}}^2} + \frac{N_D^+ - N_A^-}{2} , \tag{3.32a}$$

$$p_s = \sqrt{\frac{(N_D^+ - N_A^-)^2}{4} + {n_{ie}}^2} - \frac{N_D^+ - N_A^-}{2} , \tag{3.32b}$$

$$\psi_s = V_{applied} + \frac{kT}{q} \operatorname{asinh}\left(\frac{N_D^+ - N_A^-}{2n_{ie}}\right). \tag{3.32c}$$

For gate contacts, the electron and hole concentrations in the insulator and at the insulating contact are forced to zero, i.e. $n_s = p_s = 0$, and the electrostatic potential is simply taken as:

$$\psi_s = V_{applied} - (\Phi_m - \chi), \tag{3.33}$$

where Φ_m is the work function of the metal gate, and χ is the electron affinity of the semiconductor.

Schottky contacts to the semiconductor are defined by the work function of the electrode metal and an optional surface recombination velocity. The surface potential at a Schottky contact is defined by:

$$\psi_s = V_{applied} - (\Phi_m - \chi) + \frac{kT}{q}\ln\left(\frac{N_c}{n_{ie}}\right). \tag{3.34}$$

If a finite surface recombination velocity is imposed, the current boundary conditions are given by:

$$J_{sn} = qv_{sn}(n_s - n_0), \tag{3.35a}$$

$$J_{sp} = qv_{sp}(p_s - p_0), \tag{3.35b}$$

where J_{sn} and J_{sp} are the electron and hole currents at the contact, n_s and n_p are the actual surface electron and hole concentrations and n_0 and p_0 are the equilibrium electron and hole concentrations. v_{sn} and v_{sp} are the surface recombination velocities for electron and hole.

All other boundaries are treated with reflective boundary conditions (i.e. ideal Neumann) so that current only flows out of the device through the contact. It is given by:

$$\mathbf{n}\cdot\nabla\psi = 0, \tag{3.36a}$$

$$\mathbf{n}\cdot\mathbf{J}_n = 0, \tag{3.36b}$$

$$\mathbf{n}\cdot\mathbf{J}_p = 0. \tag{3.36c}$$

Here, $\mathbf{n}$ is the normal unit vector.

3.4.4 Some Other Models

Energy band gap as a function of temperature is given by:

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T+\beta} = E_g(300) + \alpha\left[\frac{300^2}{300+\beta} - \frac{T^2}{T+\beta}\right], \qquad (3.37)$$

where α and β are specified constants. Considering the band-gap narrowing effects due to the heavy doping, the decreasing of energy-gap can be written as:

$$\Delta E_g(x,y) = 9\times 10^{-3}\left[\ln\frac{N(x,y)}{10^{17}} + \sqrt{\left(\ln\frac{N(x,y)}{10^{17}}\right)^2 + \frac{1}{2}}\right](eV), \qquad (3.38)$$

where $N(x, y)$ is the local (total) impurity concentration. The effective intrinsic concentration which defined by Equation (3.29) varies with the changing of band-gap.

Recombination via deep levels in the gap is usually labeled Shockley-Read-Hall (SRH) recombination which is described as:

$$R^{SHR} = \frac{np - n_{ie}^2}{\tau_p\left\{n + n_{ie}\,exp\left[\frac{E_t - E_i}{kT}\right]\right\} + \tau_n\left\{p + n_{ie}\,exp\left[-\frac{E_t - E_i}{kT}\right]\right\}} . \qquad (3.39)$$

Here, E_i is the intrinsic Fermi Energy, E_t is the trap energy level and τ_n and τ_p are the electron and hole lifetime. The rate of band-to-band Auger recombination is given by:

$$R^{Auger} = (c_n n + c_p p)(np - n_{ie}^2) , \qquad (3.40)$$

where c_n and c_p are specified constants.

The other generation and recombination mechanisms include trap-assistant recombination, avalanche generation, and band to band tunneling. The net recombination rate is the summation of all the above effects.

The carrier mobilities μ_n and μ_p account for scattering mechanisms in electrical transport. It contains the bulk mobility μ_b, the surface contribution μ_{ac} and μ_{sr}, the carrier-carrier scattering μ_{eh}, and high field saturation in the following way:

$$\mu(E) = \frac{\mu_0}{\left[1 + \left(\frac{\mu_0 E}{v_{sat}}\right)^{\beta}\right]^{1/\beta}}, \tag{3.41}$$

with the low field mobility μ_0 defined by:

$$\frac{1}{\mu_0} = \frac{1}{\mu_b} + \left(\frac{1}{\mu_{ac}} + \frac{1}{\mu_{sr}}\right) + \frac{1}{\mu_{eh}}. \tag{3.42}$$

In the above, v_{sat} is the carrier saturation velocity, E is the electric field, and β is a constant (usually 1 or 2).

The simplest model of bulk mobility is a temperature dependent constant,

$$\mu_b = \mu_L \left(\frac{T}{300}\right)^{-\varsigma}, \tag{3.43}$$

with μ_L = 1417 cm^2/V·sec, ς = 2.5 for electron and μ_L = 470.5 cm^2/V·sec, ς = –2.5 for hole.

Mobility degradation at interface like in SCCD channels is accounted by the Lombardi *et al.* model [82]. It combines *surface ac-phonon scattering* (*ac*) and surface scattering (*sr*) with the bulk mobility by the Matthiessen rule:

$$\frac{1}{\mu[N(x,y),T,E_\perp]} = \frac{1}{\mu_b} + \frac{1}{\mu_{ac}} + \frac{1}{\mu_{sr}}. \tag{3.44}$$

The two surface contributions have the form:

$$\mu_{ac} = \frac{B}{E_\perp} + \frac{C[N(x,y)/N_0]^{\lambda}}{E_\perp^{1/3}(T/T_0)}, \tag{3.45}$$

$$\mu_{sr} = \frac{\delta}{E_\perp^{1/2}}. \tag{3.46}$$

For electron and hole mobility, $E_\perp$ is the electric field normal to electron and hole current, respectively, and B, C, N_0, λ and δ are specified constants.

Carrier-carrier scattering (electron-hole scattering *eh*) can be added by Matthiessen rule. The model given by Choo [83] which uses the Conwell-Weisskopf screening theory is shown as follow:

$$\mu_{eh} = \frac{D\left(\frac{T}{T_0}\right)^{3/2}}{\sqrt{(np)}}\left\{\ln\left[1+\xi\left(\frac{T}{T_0}\right)^2 (pn)^{-3}\right]\right\}^{-1}, \qquad (3.47)$$

with the specified constants D and ξ.

3.5 Simulation Tools

The application of software tools in the development of new processes and novel device structures has become a worthwhile, albeit challenging, alternative to the experimental route. Fabrication of one lot in a modern process can cost considerably more than 10,000 dollars, and consume weeks, months, or even years of efforts. The use of accurate simulation tools in the proper computing environment allows for comparatively inexpensive *computer experiments*.

Figure 3.2 gives a general description from chip design to the fabricated products. The chip design gives the layout, fabrication definition, terminal voltages and wave forms. The layout and process definition are used by chip fabrication. On the other hand, the layout, terminal voltages and waveforms, combining with the process information are used by the simulation route, which include process, device and circuit simulation.

A general description of the procedure from chip design to the fabricated products including the chip fabrication route and the simulation route is highlighted in Figure 3.2 The process and device simulation are the main thrust of this dissertation. A short description of the simulation tools used in this dissertation is described below. These tools include SUPREM, PISCES, and ISE-TCAD software package. SUPREM III, SUPREM IV and PISCES IIB have been developed at Stanford University Integrated

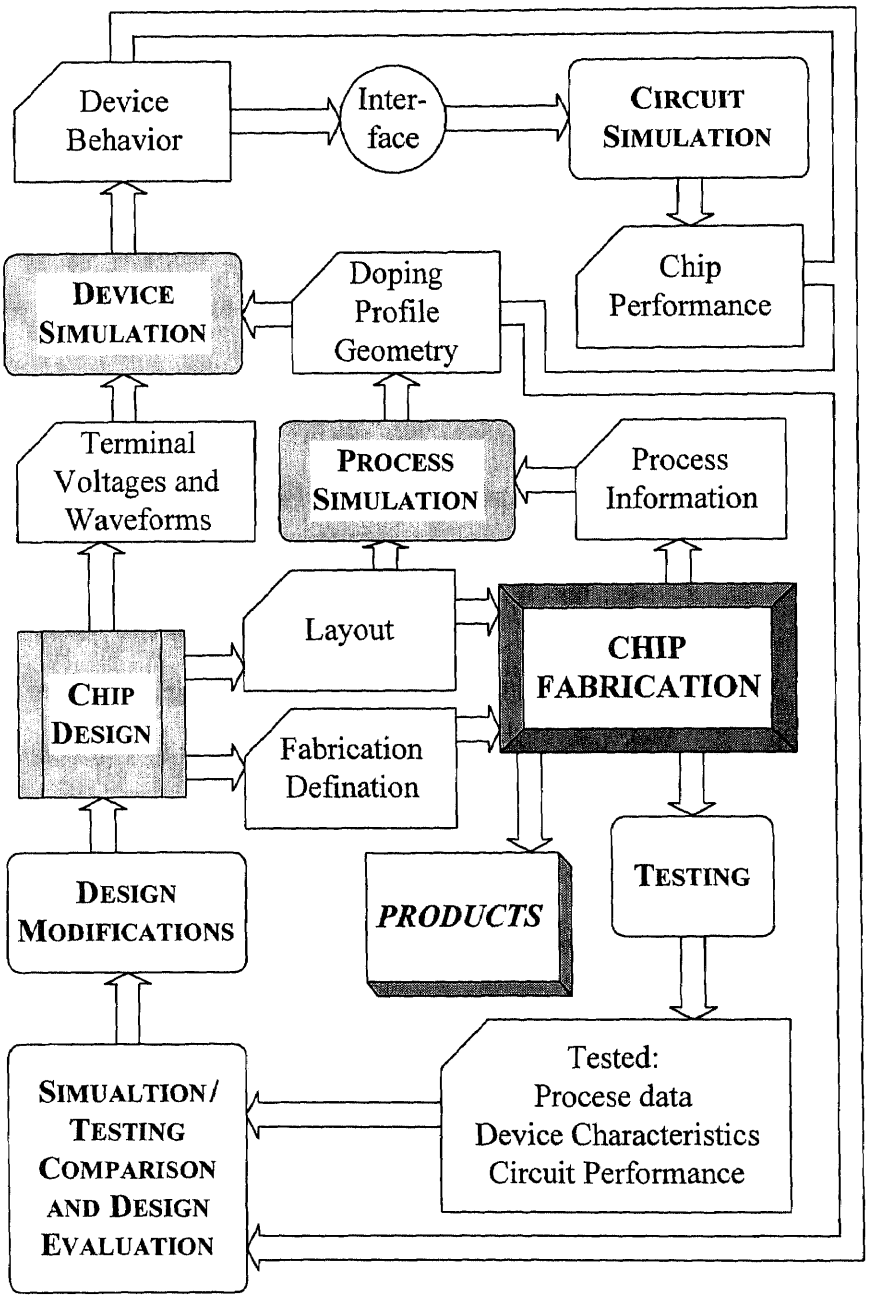


Figure 3.2 *A general description of the procedure from chip design to the fabricated products which includes the chip fabrication route and simulation route. It also shows the coupling between the various of simulation tools.*

Circuits Laboratory during the 1980's. A new simulation software package, ISE-TCAD tools (which includes LIGAMENT$_{-ISE}$, TEDIOS$_{-ISE}$, SIMUL$_{-ISE}$), was obtained from Integrated Systems Engineering (ISE) AG, ETH Zentrum which gave us additional tools for the modeling of CCD structures. The main limitation of the ISE software is that it does not allow to calculate the values of charge signal which plays an important role in the simulation of CCD structures.

SUPREM III

SUPREM III is a one dimensional process simulator capable of modeling semiconductor fabrication steps such as diffusion, ion implantation, deposition, etching, and oxidation. The doping profile obtained by the simulation can be exported to PISCES IIB to construct the device structure. On the other hand, by giving the gate and substrate voltages, and setting the electron and hole quasi-Fermi levels, it can simulate the one dimensional (1-D) potential profile and the charge handling capacity of a CCD structure. The typical simulation time of SUPREM III is in the range of several minutes on a SUN SPARC-10 workstation available at NJIT. Therefore, it is very useful for running a large number of simulations. However, since SUPREM III can only give the 1-D properties of the device, two dimensional (2-D) effects such as bird-beak effect, lateral diffusion and the fringing field caused by the adjacent CCD gates can not be simulated and that limits the applications of this software.

SUPREM IV

SUPREM IV is a 2-D process simulator. The doping profile and the device geometry obtained by the simulation can be exported to PISCES IIB. SUPREM IV can also be used for modeling the fabrication steps such as diffusion, ion implantation, deposition, etching, and oxidation. The 2-D effects such as bird beak effect, lateral diffusion and isotropic etching can be obtained by using SUPREM IV. Since the SUPREM IV installed in

VLSI/Simulation lab of NJIT is a comparatively older version, it dose not include the oxidation of polysilicon. The overlaps of polysilicon gates in a CCD structure can not be obtained by using SUPREM IV. The limitation by SUPREM IV is rather time intensive. The simulation time of SUPREM IV for our problems has been usually in the range of several hours to several days using the SUN SPARC-10 workstation.

PISCES IIB

PISCES IIB is a 2-D Poisson's and current continuity equations solver. It has the ability to determine the electrostatic potentials and carriers densities everywhere in a 2-D semiconductor structure. Doping profiles from either SUPREM III or SUPREM IV may be exported to PISCES IIB, which then be used to construct the device structure. By giving the gate voltages and setting the electron and hole quasi-Fermi level, PISCES IIB can be used to determine the charge handling capacity of the CCD wells including the effect of fringing field created by the adjacent gates. One the other hand, transient simulation by PISCES IIB can be used to model the charge transfer in the photodetector and under the CCD gates. The typical running time of PISCES IIB is about ten minutes using the SUN SPARC-10 workstation for static simulation and several hours for transient simulation. The limitation of PISCES IIB is its limited number of mesh points (3,000 for statistic and 1,600 for transient), regions (maximum of eight) and contacts (maximum of ten). It can not be used to simulate the charge transfer under a large number of serial CCD gates.

LIGAMENT$_{-ISE}$

LIGAMENT$_{-ISE}$ is a process simulation input file generator, the input files of which include process flow, process definition, and chip layout. LIGAMENT$_{-ISE}$ can be used to create the 1-D and 2-D process input files for the process simulator TEDIOS$_{-ISE}$. The

LIGAMENT$_{-ISE}$ process input file contains the effects of all the consequent mask layers to the selected region.

TEDIOS$_{-ISE}$

TEDIOS$_{-ISE}$ is a 1-D and 2-D process simulator. It has the capability to model the deposition, ion implantation, oxidation, diffusion, etching and glass reflowing. The bird beak effect is well predicated by TEDIOS$_{-ISE}$. 2-D doping profile and the device geometry can be exported to the device simulator SIMUL$_{-ISE}$. The simulation results of device topography can be used to compare with the SEM photographs of the fabricated device intersection. The typical running time of TEDIOS$_{-ISE}$ is several hours using the SUN SPARC-10 workstation for a 2-D simulation.

SIMUL$_{-ISE}$

SIMUL$_{-ISE}$ is a one-, two-, and three-dimensional (3-D) device simulator, which also solves the Poisson's and current continuity equations with the defined boundary conditions. In principle, unlimited mesh points, regions and contacts can by defined in SIMUL$_{-ISE}$. However, the more the mesh points used, the higher the time cost. Many days of simulation time is needed for a structure with mesh points of 20,000 on the SUN SPARC-10 workstation. The present version of SIMUL$_{-ISE}$ is not allowed to artificially set the electron and hole quasi-Fermi levels. On the other hand, SIMUL$_{-ISE}$ can solve the current densities and potential distributions. But it can not be used in the present form to solve for the carrier concentrations in the device. This limits its applications in the modeling of CCD structures.

3-D device simulation by SIMUL$_{-ISE}$ can be used to obtain the potential profile over the area of interesting in the CCD structure. However, the doping profile obtained by TEDIOS$_{-ISE}$ cannot be used to create the 3-D device structure of SIMUL$_{-ISE}$. Gaussian distribution approximation is used to create the 3-D device structure. However, since a

large number of mesh points has to be used to create a 3-D structure, the simulation will take a very long time (up to weeks or months) by using the SUN SPARC-10 workstation, and the precision of the results will be limited by the computational errors. Therefore, 3-D simulation using $SIMUL_{-ISE}$ was not attempted in this dissertation.

CHAPTER 4

VERY HIGH FRAME RATE BURST-IMAGE SENSOR

4.1 Introduction

The general architecture of the Very High Frame Rate (VHFR) burst-image sensor was proposed by Professor Walter F. Kosonocky and Mr. John L. Lowrance [1] in 1991. The application of the VHFR burst-image sensor is to capture images of rapid motion and transient photometric phenomena. In general, this imager is capable of capturing images at frame rates up to one million frames per second and storing the last 30 frames for subsequent readout at a slower rate.

The VHFR burst-image sensors described in this chapter contains 360x360 pixels, and it can capture and store 30 frames of image in a frame rate of up to 830,000 frames per second [84]. This imager has been constructed at the David Sarnoff Research Center (Sarnoff) with four-level-polysilicon three-level-metal BCCD technology in accordance with the process specification provided by NJIT that is described in Chapter 5.

The design and layout of this imager was developed at the NJIT Electronic Imaging Center by a team effort of Chao Ye, Liansheng Xie, Guang Yang, and Professor Kosonocky. The process definition and simulation for this imager were done as part of this dissertation by Guang Yang in collaboration with Dr. Frank Shallcross. Dr. Shallcross was also responsible for fabrication of a 20-wafer lot of these imagers at the David Sarnoff Research Center (Sarnoff). The VHFR burst-image sensors were tested and demonstrated at the Princeton Scientific Instruments (PSI), Inc. The test team of the imager included Rakesh Kabra, Guang Yang, Chao Ye and Processor Kosonocky of NJIT, and Vincent Mastrocola and John Lowrance of PSI. The test camera was designed and constructed by PSI. The voltage and timing specification of the clock waveforms for operation of this imager were by Guang Yang, Chao Ye, and later Rakesh Kabra of NJIT.

This Chapter contains a general description of the construction of the VHFR burst-image sensor, a discussion of the operation of the imager and the test results verifying the operation of the imager.

4.2 Construction of the VHFR Burst-Image Sensor

4.2.1 Chip Architecture

The functional block diagram of the VHFR burst-image sensor is shown in Figure 4.1. This imager contains 360x360 macropixels with a 13.5% fill factor (i.e., the ratio of the area of the photodetector to the area of the macropixel) and 30 micropixel per macropixel. The macropixels are defined as the imager resolution elements or just pixels, the micropixels represent the CCD storage elements at each pixel that corresponding to the number of frames that can be detected and stored on the focal plane array (FPA). The chip size of the imager is 2-cmx2-cm. In order to reduce transfer losses and to improve processing yield of usable device, this imager is organized into four quadrants; each quadrant contains 180x180 macropixels and the four OUTPUTs connected to each quadrant are reading the signal out simultaneously to reduce the number of the necessary CCD charge transfer stages.

4.2.2 Design of the Macropixels

Each macropixel of the imager has an overall dimension of 50-μmx50-μm. Each macropixel has an photodetector with a maximum vertical dimension of about 30 μm and a maximum horizontal dimension of about 10 μm, a photodetector charge read-out structure, an serial-parallel (SP) register, and a parallel (P) register.

The general architecture of the VHFR image burst-sensors is illustrated in Figure 4.2 for an array of 2x2 macropixels. Each macropixel consists of a photodetector (PD) with charge-collecting well under the G_1 gate, a blooming barrier gate G_2, a drain D, and the G_3 separating the charge-collecting well from 5-stage SP register. The drain D is used

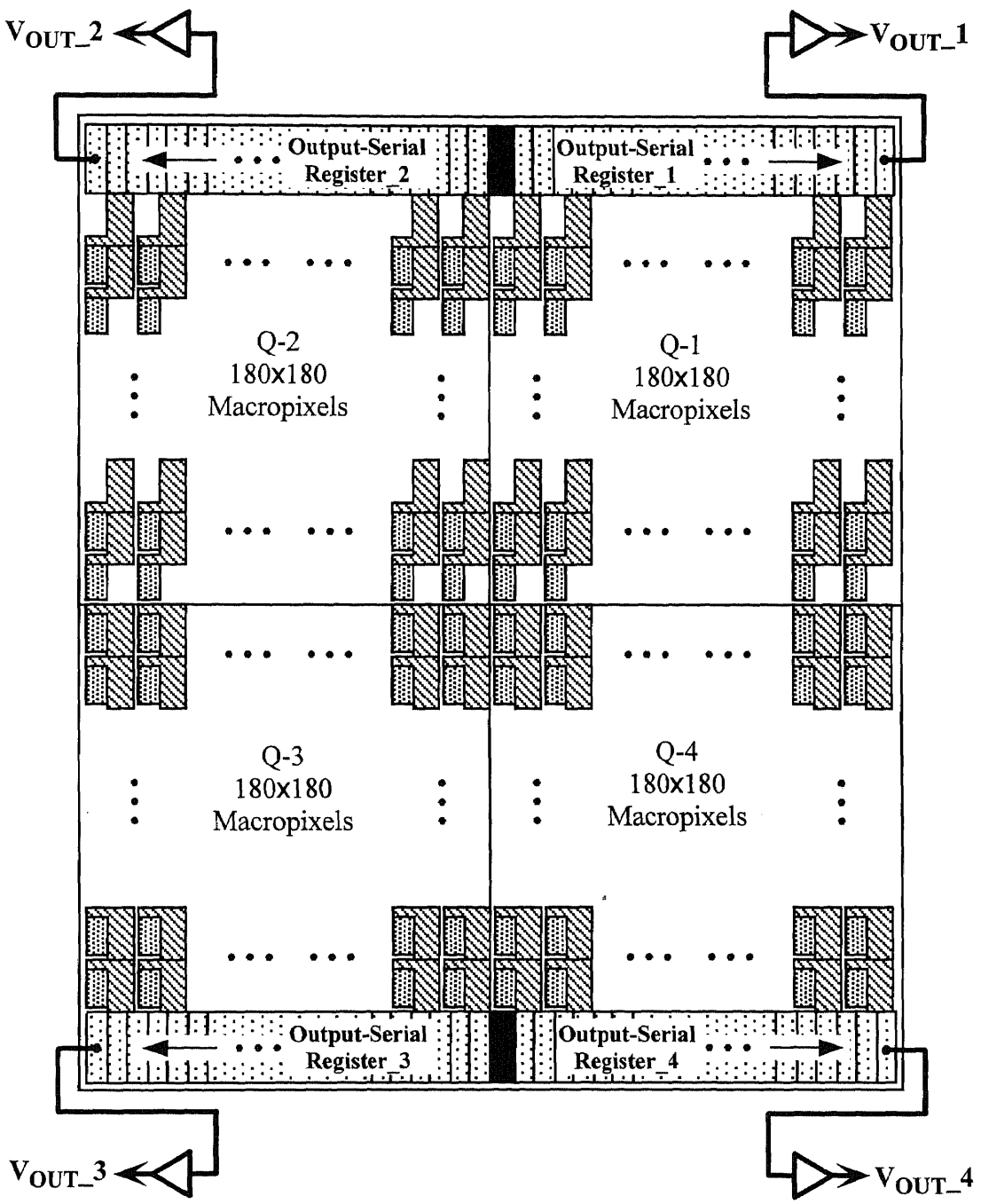


Figure 4.1 *Block diagram of the VHFR burst-image sensor with 360x360 resolution elements (macropixels) and 30 image frames storage capacity (micropixels).*

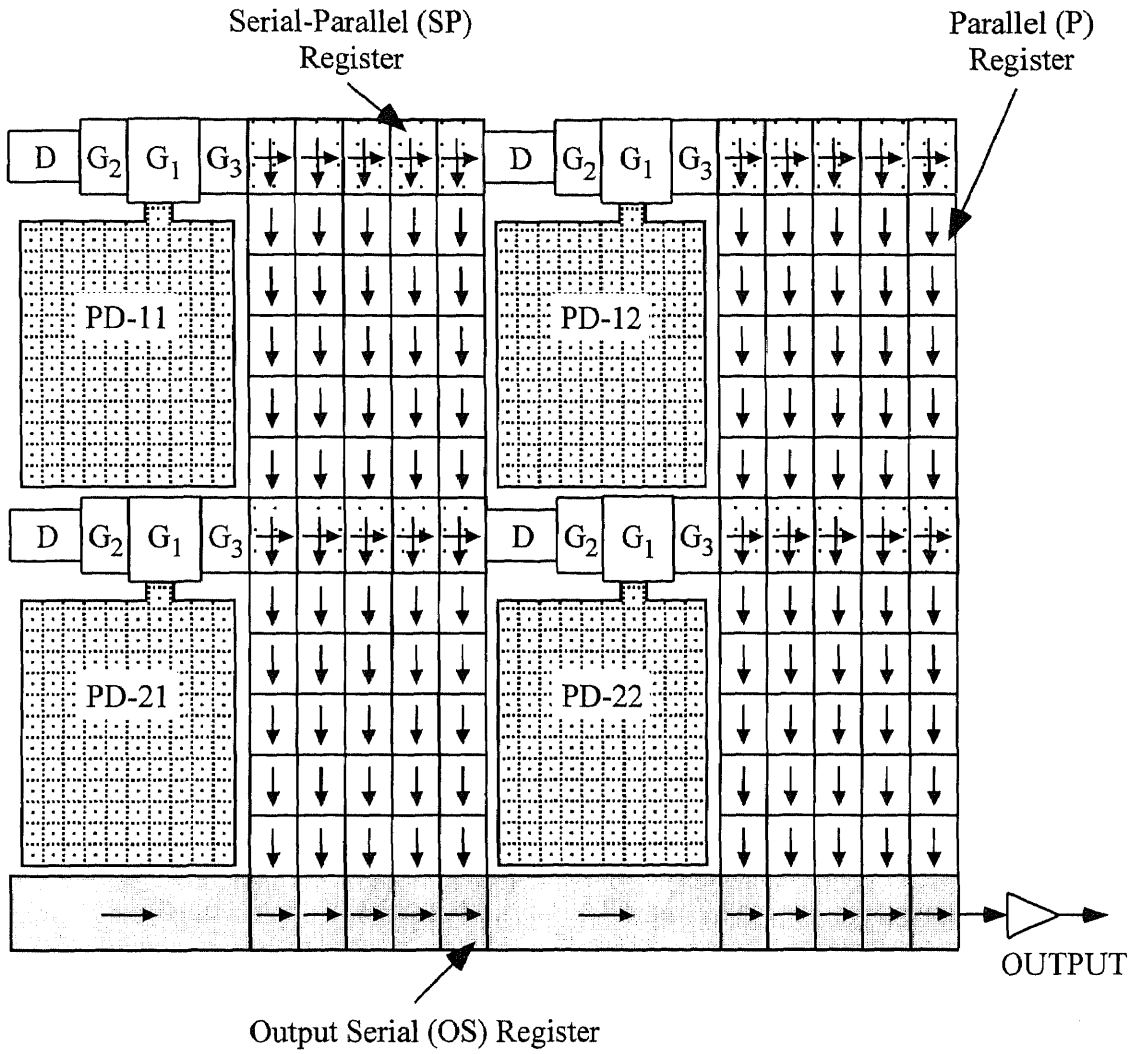


Figure 4.2 *Schematic diagram of architecture of the VHFR burst-image sensor.*

for control of blooming during optical (frame) integration and for dumping the excess charge signals (excess frames) from the SP register. However, this drain D could also facilitate the operation with the subframe optical integration time. The 5 stage SP register coupled to a 5x5 P register forms a 30-frame CCD storage at each macropixel.

To achieve an area-efficient layout, the design of the 3-phase CCD SP register uses four levels of polysilicon. Figure 4.3 shows the SP and P registers design with 3-phase CCD, four-level-polysilicon construction in the macropixels. The SP register

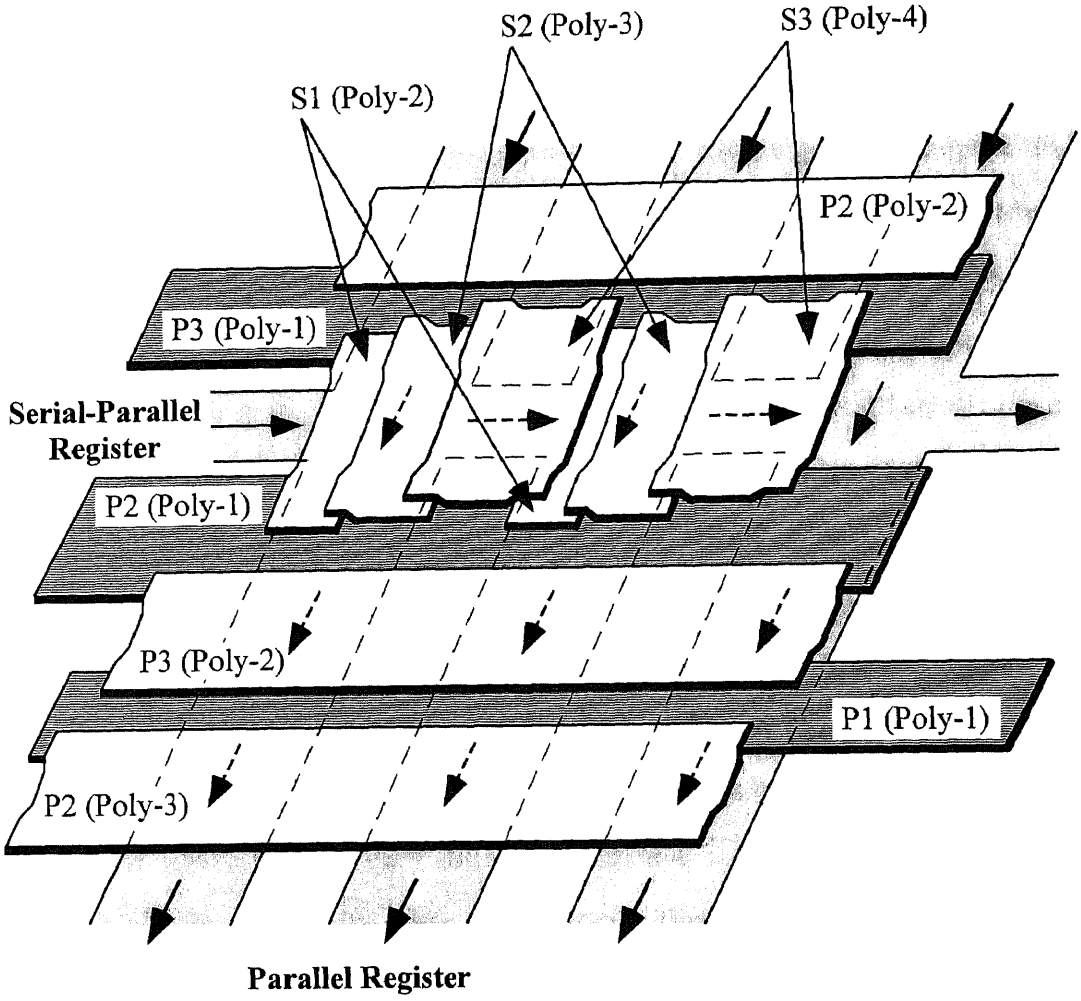


Figure 4.3 *SP and P registers design with 3-phase CCD, four-level-polysilicon construction.*

phases S1, S2, and S3 are constructed by poly-2, poly-3, and ploy-4, respectively. When the charge is transferring in P register, poly-4 gates (phase S3) act as the induced channel stop for vertical charge transfer, and poly-2 and poly-3 gates (phases S1 and S2) are clocked as phase P1 of P register. When the charge is transferring in P register, two poly-1 gates (shown as phases P2 and P3) act as induced channel stop for horizontal charge transfer.

In order to assure that the photodetector has the same size, shape and orientation in the upper- and lower-side of the imager as well as the symmetry of the signal storage sequence, the macropixel in upper- and lower-side of the imager are designed to be geometrically different. Figures 4.4 shows the layout of the lower-side macropixel. Inspection of this figure shows that, the charge storage elements are on the right side of the photodetector. Similarly, for the upper-side macropixel, the charge storage elements are on the right side of the upper photodetector. Figure 4.5 shows the schematic diagram and the charge transfer direction of the 2x2 macropixels in the center of the imager. S1A, S2A and S3A are the serial phase clocks of quadrant-1; S1B, S2B and S3B are the serial phase clocks of quadrant-2; S1C, S2C and S3C are the serial phase clocks of quadrant-3; and S1D, S2D and S3D are the serial phase clocks of quadrant-4. P1A, P2A and P3A are the parallel phase clocks of quadrant-1; P1B, P2B and P3B are the parallel phase clocks of quadrant-2; P1C, P2C and P3C are the parallel phase clocks of quadrant-3; and P1D, P2D and P3D are the parallel phase clock of quadrant-4. Inspection of Figure 4.5 shows that, the charge is transferring upwards for storage (loading) and readout (unloading) from the upper-side macropixels and transferring downwards for storage and read-out for lower-side macropixels. Therefore, the charge loading and unloading follows exactly the same pattern for both upper and lower parts.

Figures 4.6 is the schematic diagram of the two macropixels, the output serial (OS) register, and the output circuit of quadrant-4. Here, OS1, OS2 and OS3 are the phase clock of OS registers; FD is the read-out floating diffusion; OG_1 and OG_2 are the output control gates; RS is the reset gate; and G_4 is the connection gate between P register in the last row of each quadrants to the OS register. V_{rsd4} is the reset drains voltage, V_{dd4} is the drain voltage of output amplifier, and V_{OUT4} is the signal output of quadrant-4.

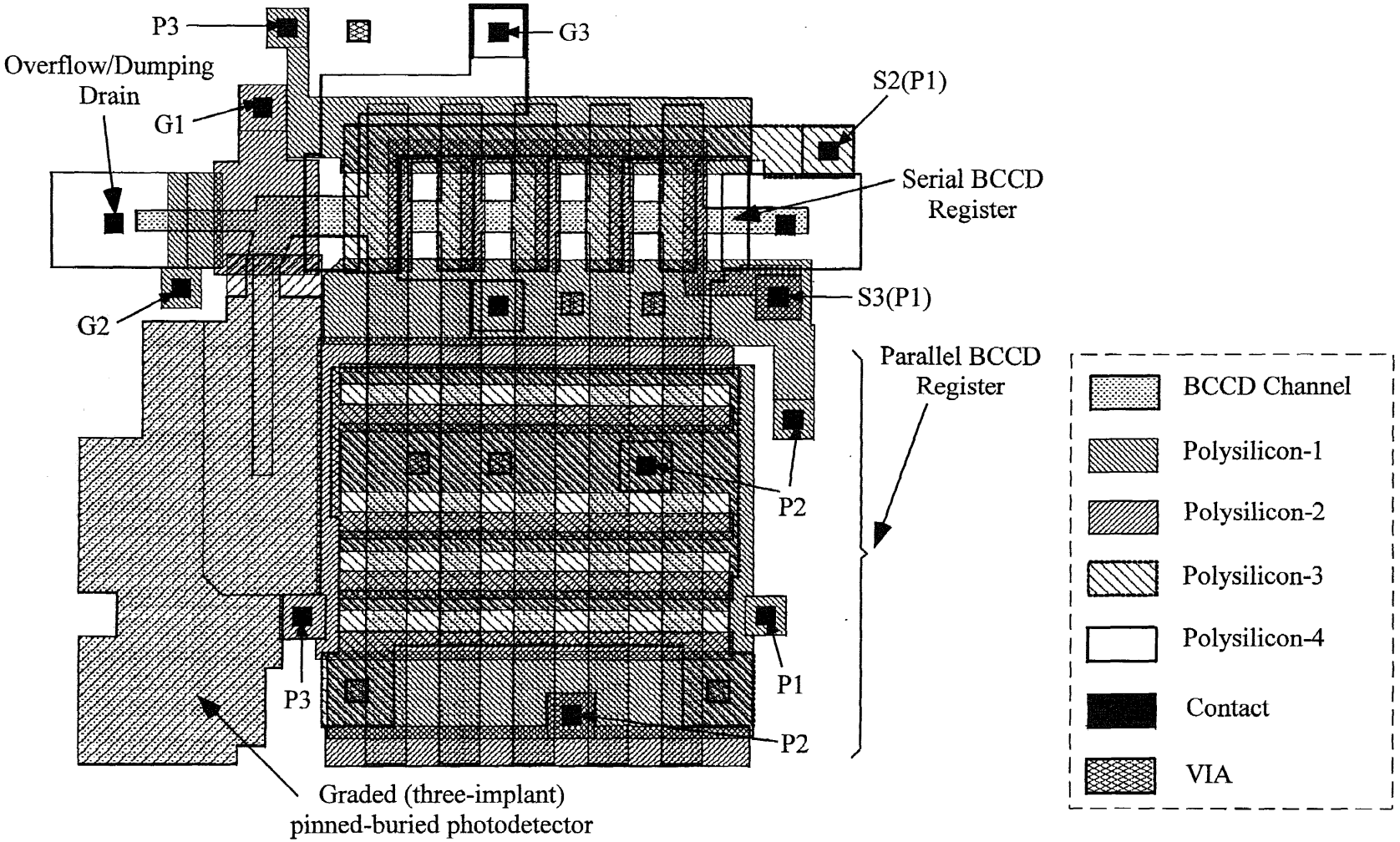


Figure 4.4 *Layout of the lower-side macropixel of the VHFR burst-image sensor.*

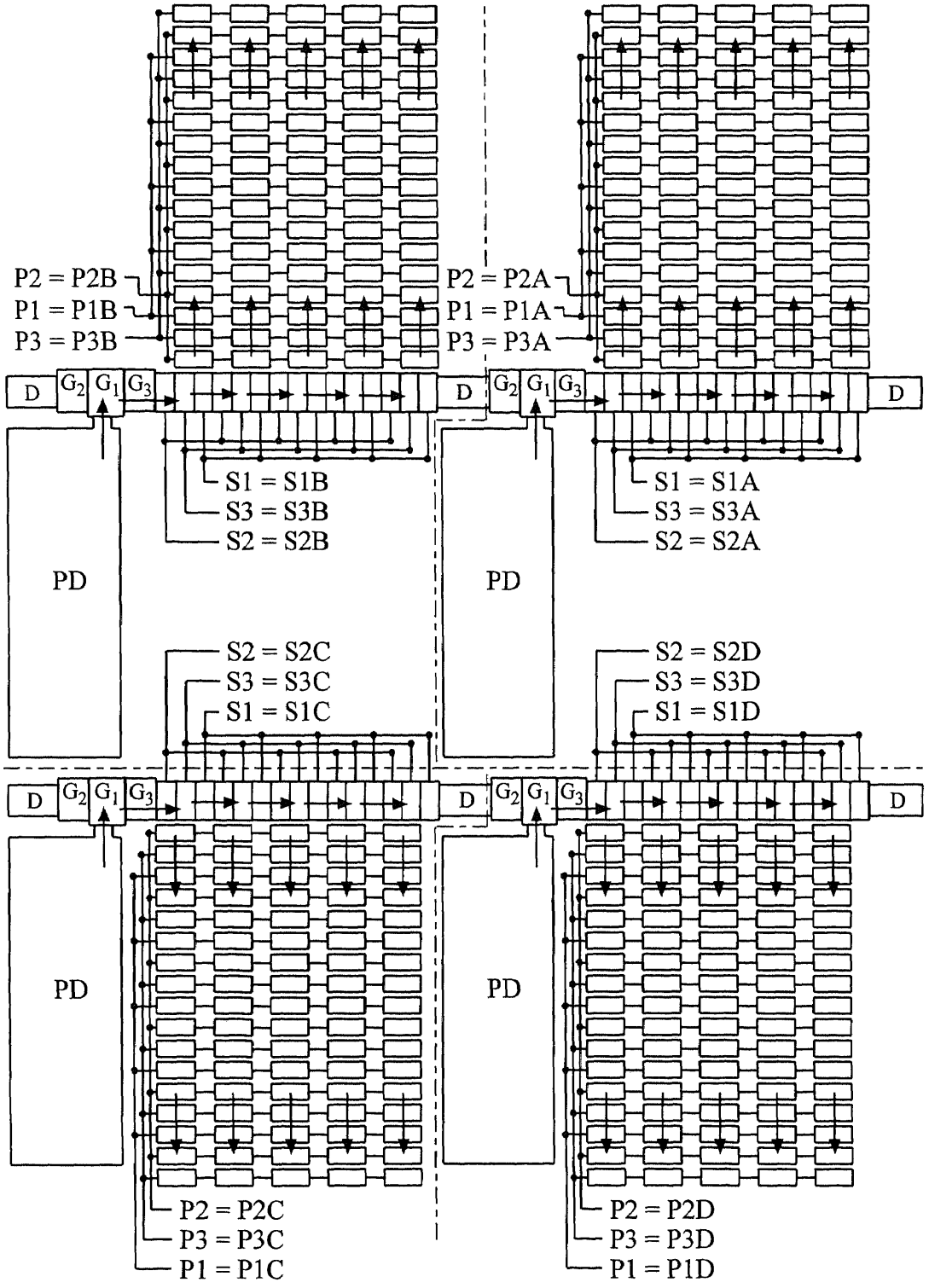


Figure 4.5 *Schematic diagram of 2x2 macropixels in the center of the VHFR burst-image sensor.*

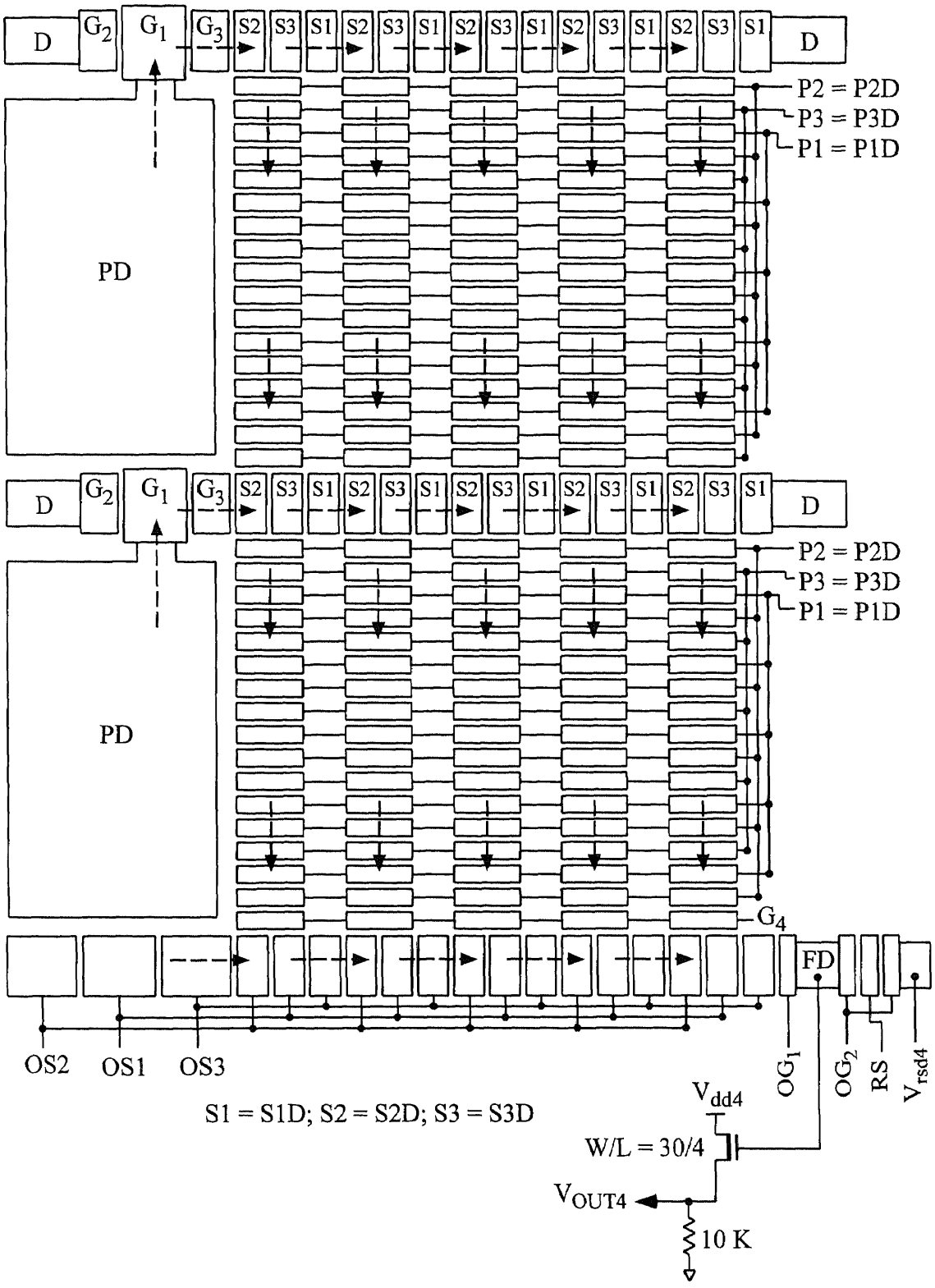


Figure 4.6 *Schematic diagram of two macropixels with output in the corner of quadrant-4.*

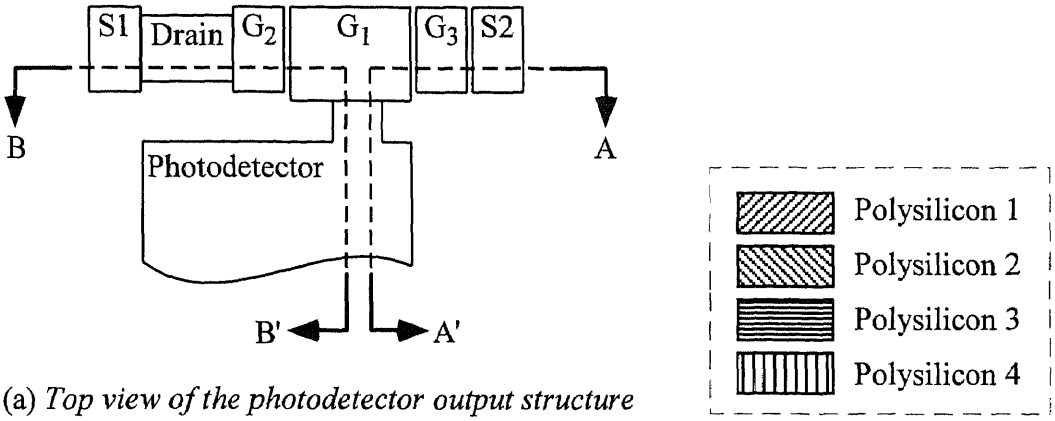
Using the minimum design rule of the four layers of polysilicon, the minimum size of the micropixels which is located in the P register is 6.0-μmx4.5-μm. The micropixel has a 2.5 μm channel stop region (p^--substrate) and a 3.0-μmx1.5-μm BCCD charge storage area. Considering the side-diffusion effect of the n-type BCCD implants, the effective charge storage area is somewhat bigger. The charge handling capacity of the charge storage area was simulated by using one-dimensional (1-D) and two-dimensional (2-D) simulators by SUPREM III, SUPREM IV and PISCES IIB for the different process options. The results of these simulations will be presented in Chapter 6.

4.2.3 Photodetector Readout

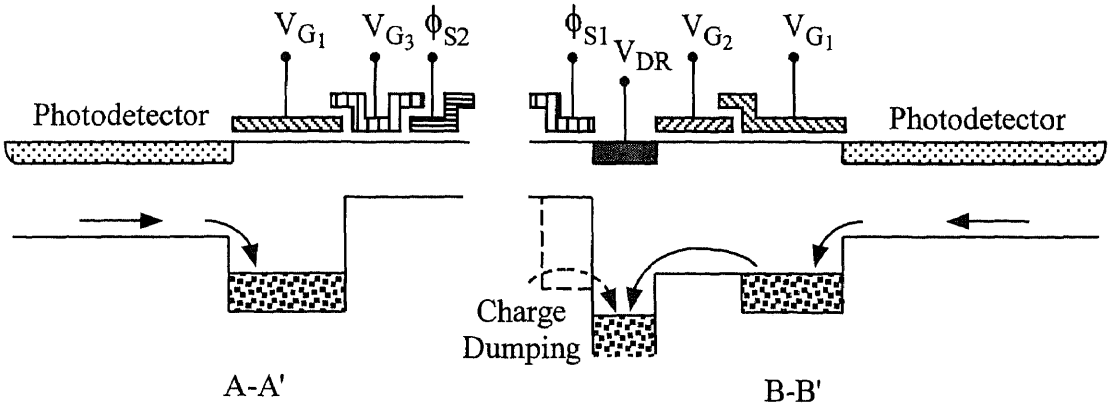
The VHFR burst-image sensor is constructed with the photodetector readout circuit illustrated in Figure 4.7. As shown in Figure 4.7(b), during the charge integration time, the potential well under the charge collecting gate G_1 acts as a sink for photodetector charge. The control of the blooming in the presence of a large optical overload is achieved by controlling the gate G_2 in conjunction with the blooming drain (V_{DR}). The channel potential G_2 is biased at a certain value (see Section 4.3) to keep the total charge collected by G_1 not exceeding the maximum charge handling capacity of the smallest BCCD storage element.

The readout of the collected charge signal is obtained by a periodical transfer of the charge from under gate G_1 to G_3.Then it is clocked out by the SP register clock phase S2. As illustrated in Figure 4.7(c), during the charge readout time, a potential well is formed under G_3 and potential barrier is formed under G_1. Thus, the charge under G_1 is pushed into G_3. In the mean time, the channel potential of G_2 forms a barrier to prevent the charge from flowing into the blooming drain.

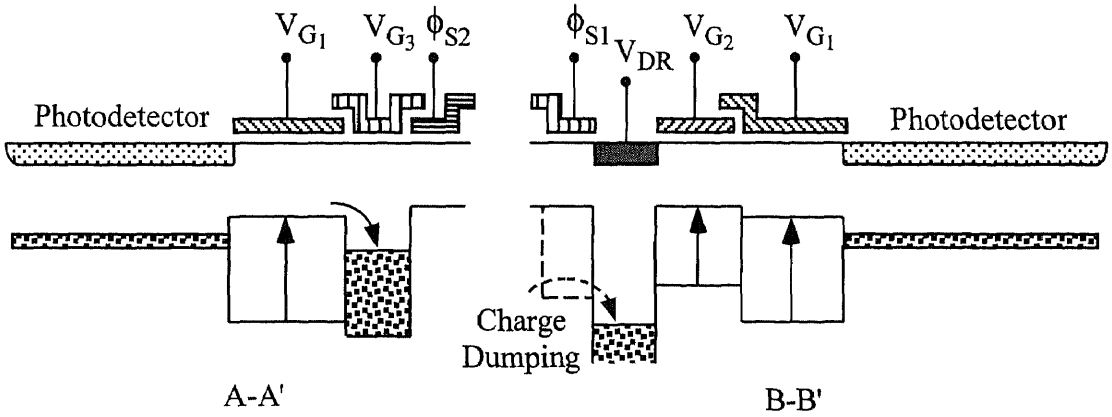
The blooming drain shown in Figure 4.7 is also used by the left-hand-side macropixel as a signal charge dumping drain when the storage capacity of the macropixel (i.e. 30 image frames or micropixels) is exceeded during the signal integration time.



(a) *Top view of the photodetector output structure*



(b) *Cross-section of A-A' and B-B' and potential profiles during the charge accumulation*



(c) *Cross-section of A-A' and B-B' and potential profiles during the charge readout*

Figure 4.7 *Construction and operation of photodetector readout.*

This charge dumping is shown as the dotted line in Figures 4.7(b) and (c). As the serial clock S1 is turned ON (i.e. at high voltage level), the charge signals clocked out by the SP register of the macropixels on left-hand-side are flowing into the blooming/dumping drain.

4.2.4 Output Serial Register and Output Circuit

As shown in Figure 4.6, the OS register is a 3-phase CCD register with 5+1 stages corresponding to each macropixel. The 5 stages correspond to the 5 horizontal micropixel and the 1 stage covers the space under the 10 μm wide photodetector. The voltage output of the OS register is detected by the floating diffusion amplifier. The floating diffusion signal voltage, V_{FD}, is pre-amplified by the on chip source follower is readout by an off-chip correlated double sampling. The output signal charge in the floating diffusion is reset after each read-out by the reset-voltage V_{RSD}. The buried-channel MOSFET of the on-chip source follower is formed by a polysilicon-1 gate over a BCCD channel.

Using the charge readout structures shown in Figures 4.6, the charge readout will involved up to 180x6x3 = 3,240 CCD transfers in a vertical direction and up to 180x(5+1)x3 = 3,240 CCD transfers in a horizontal direction. The resulting maximum number of CCD transfers of 6,480 is comparable to the largest state-of-the-art CCD imager.

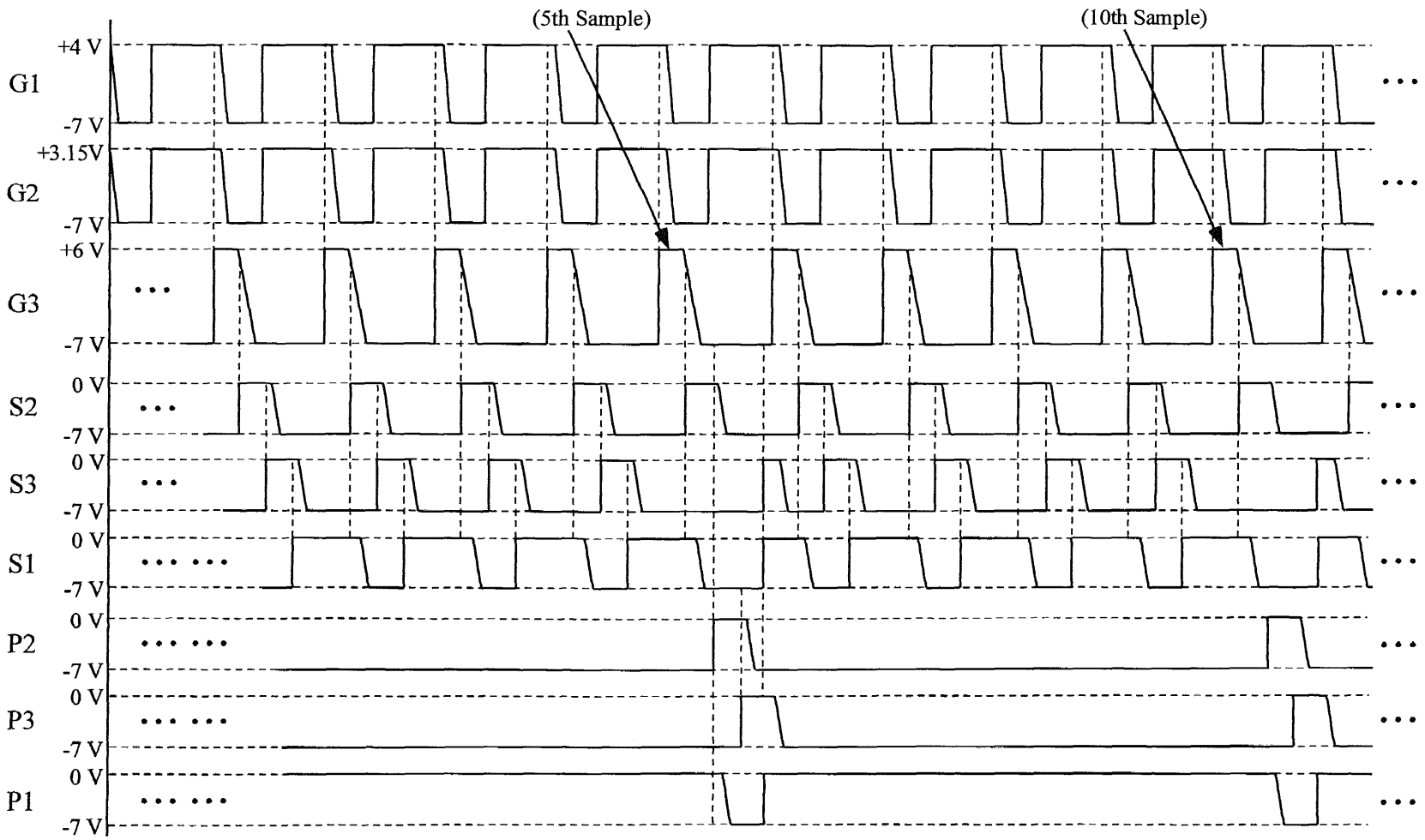
4.3 Operation of the VHFR Burst-Image Sensor

The operation of the VHFR imager consists of two periods: the frame collection or accumulation period and the frame readout period [84]. During the frame collection period, up to 30 frames are detected by the photodetectors of the macropixels and are continuously stored in the 5-stage SP register and 25-stage P register corresponding to 30 micropixels. As new image frames are accumulated, the micropixels corresponding to the excess frames are dumped into the blooming/dumping drain of the adjacent macropixels.

During the frame readout period, the frame collection operation is stopped, the photogenerated signal detected by the photodetector is transferred (drained) directly to the blooming drain, and the SP BCCD registers of the macropixel are reconfigured into large P registers (one of each quadrant) to be readout in parallel by four output serial (OS) registers.

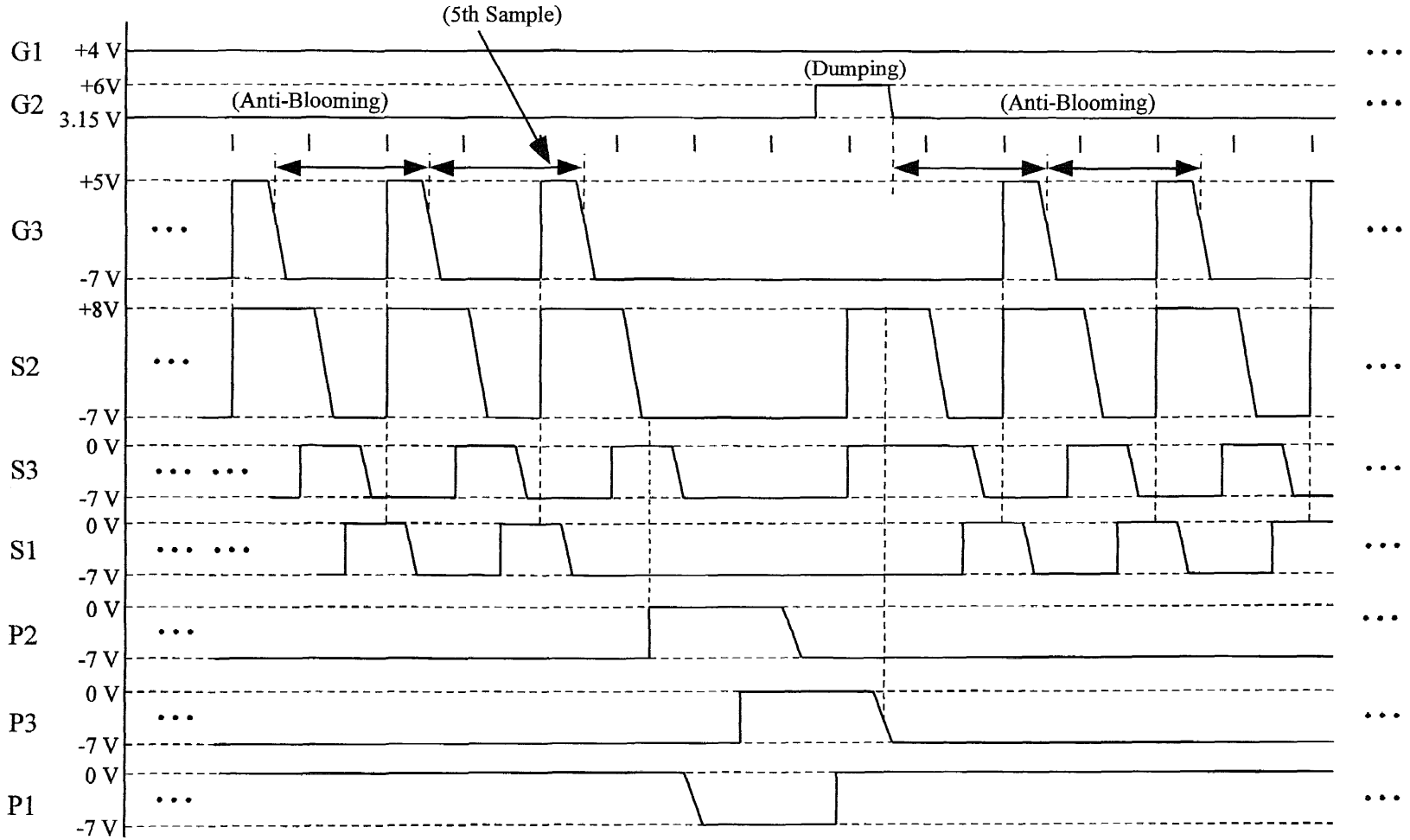
The clock wave forms of each clock phase for operating the VHFR burst-image sensor during the frame collection period and the frame readout period are illustrated in Figures 4.8 and 4.9, respectively. The applied gate voltages to each clock phase are chosen based on 1-D and 2-D simulations of charge handling capacity and simulation of the channel potential as function of gate voltage. According to the simulation results which will be described in Chapter 6, the applied voltages to the P, SP and OS registers are varied between 0V (ON) and -7V (OFF) for the low BCCD implant dose. However, the "ON" voltage of charge collecting gate (G1) has been chosen to be +4V (corresponding to channel potential of about 9.0 V) in order to remove the barrier at the edge of the photodetector (the simulation results will be given in Chapter 7). The area of G1 is approximately 25 μm^2 which is much bigger than the area of smallest CCD storage element. To keep the total charge collected not exceeding the maximum charge handling capacity of the smallest CCD storage element, the voltage applied on the blooming control gate G2 should be kept at +3.15V (corresponding to channel potential about 8.0 V) during the charge integration time.

There are several operating modes for the frame collection period. Figure 4.8(a) shows the clock waveforms in operation Mode-1. In this operating mode, the imager is continuously collecting the signals with a constant signal integration time, and the last 30 frames of signal will be stored in the macropixels and transferred to the output amplifiers during the frame readout period. The charge transfer under its associated gates in the macropixels during the frame collection period in Mode-1 is described in Appendix A, Section A.1. When the VHFR burst-image sensor is operated in this mode, as shown in



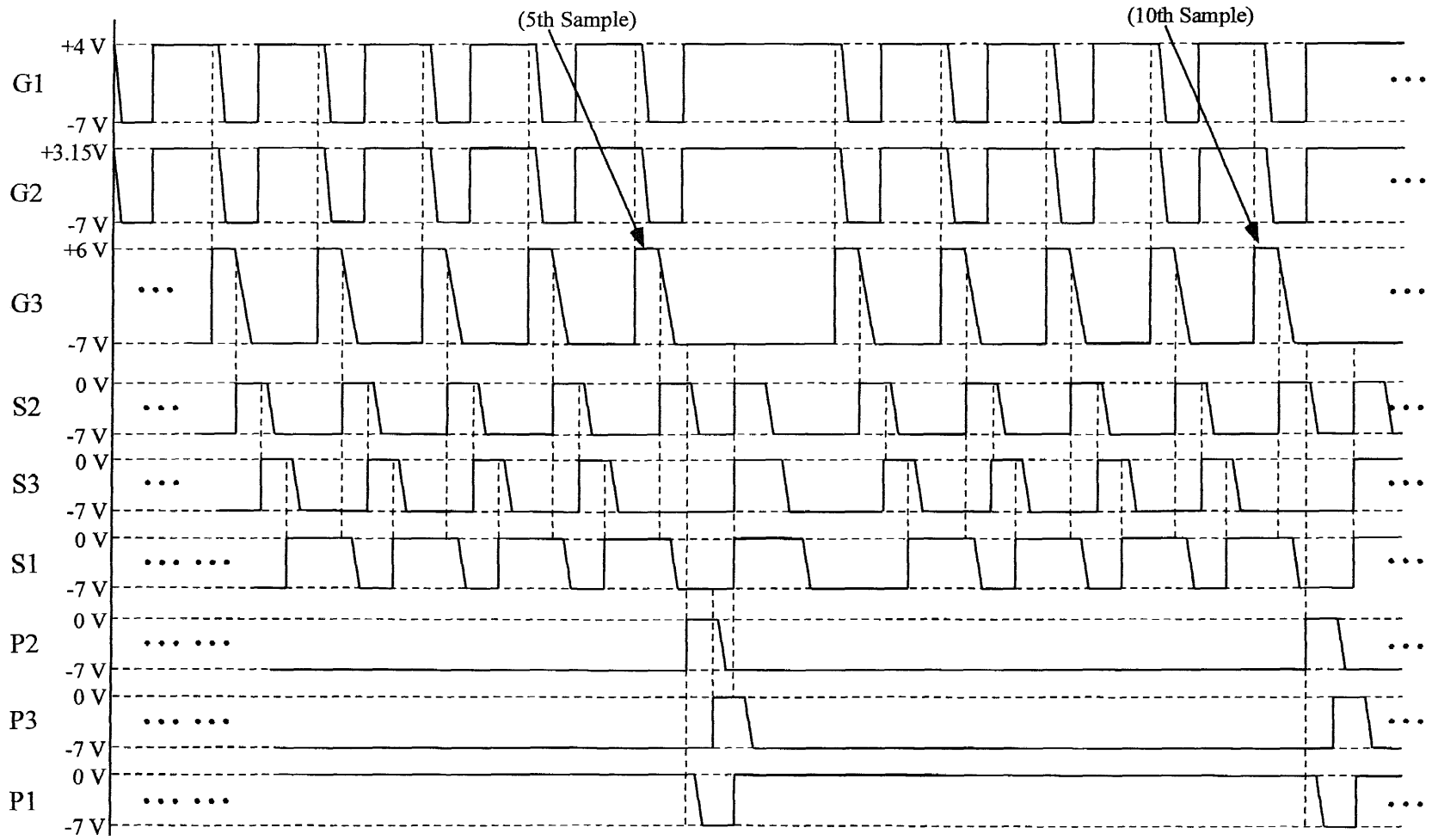
(a) *Mode-1*

Figure 4.8 *Driving waveform of VHFR burst-image sensor during the frame collection period.*



(b) *Mode-2*

Figure 4.8 *(Continued)*



(b) *Mode-3*

Figure 4.8 *(Continued)*

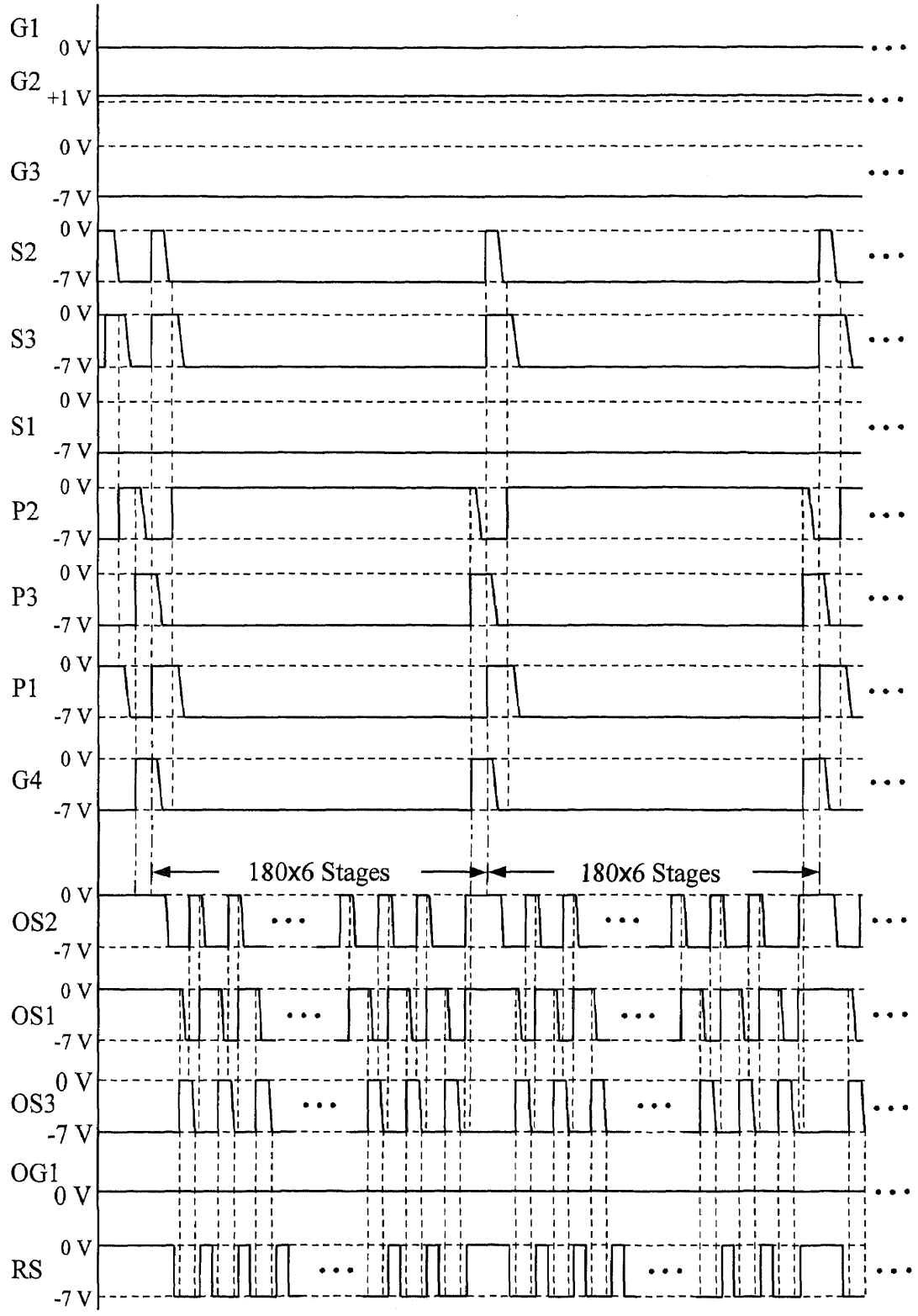


Figure 4.9 *Driving waveform of VHFR burst-image sensor during the frame readout period.*

Figure 4.8(a), during the time of collecting the signal charge of the first frame of each 5 frames, a higher frequency for clock phase S3 is needed. The charge transfers as the imager is collecting the signal charge of the first frame of each 5 frames of is illustrated in Figure 4.10. Inspection of this figure shows that, when the last row of charge (which can be either the residual charge in the imager or the signal charge of the excess frames) from the upper pixel (M, N-1) is transferred to SP register under S1 gates via S3 gates of pixel (M, N) and to be eventually dumped in the drain, the first frame signal charge for the next row of 5 frames is entering the SP register of pixel memory (M, N) via G3 gate. Thus, by operating the imager in this mode, clock phase S3 should have a very small RC time constant and the requirement on the timing of all the clock phases is very important.

In order to avoid the need for very short RC time constants of the clock phases in Mode-1, other modes are proposed for the operation of the imager. Figure 4.8(b) illustrated the clock waveforms in operation Mode-2. In this mode, the imager is continuously collecting the signals with the first frame of each 5 frames having twice as long integration time as the other frames. As a results, the 1^{st}, 6^{th}, 11^{th}, 16^{th}, 21^{st}, and 26^{th} frames have twice as much signal charges and they may exceed the charge handling capacity of the smallest charge storage element. The operation of photodetector readout in operating Mode-1 and Mode-2 was illustrated in Figure 4.7. Figure 4.8(c) illustrate the clock waveforms for operation of the imager in Mode-3. In this mode, the imager operates with a constant signal integration time, but an electronic shutter [see Figure 4.11(b)] is activated during the time needed for two parallel transfers of the pixel memory. In this case, as shown in Figure 4.8(c), after the SP register in each macropixel is loaded, two signal sampling have been skipped, while the detected charge signals are transferred from SP register to P register. As the results, the imager will collect (non-continuously) frames 1^{st} to 5^{th}, 8^{th} to 12^{th}, 15^{th} to 19^{th}, 22^{nd} to 26^{th}, 29^{th} to 33^{rd}, and 36^{th} to 40^{th}. The construction and operation of photodetector readout in operating Mode-3 is shown in Figure 4.11.

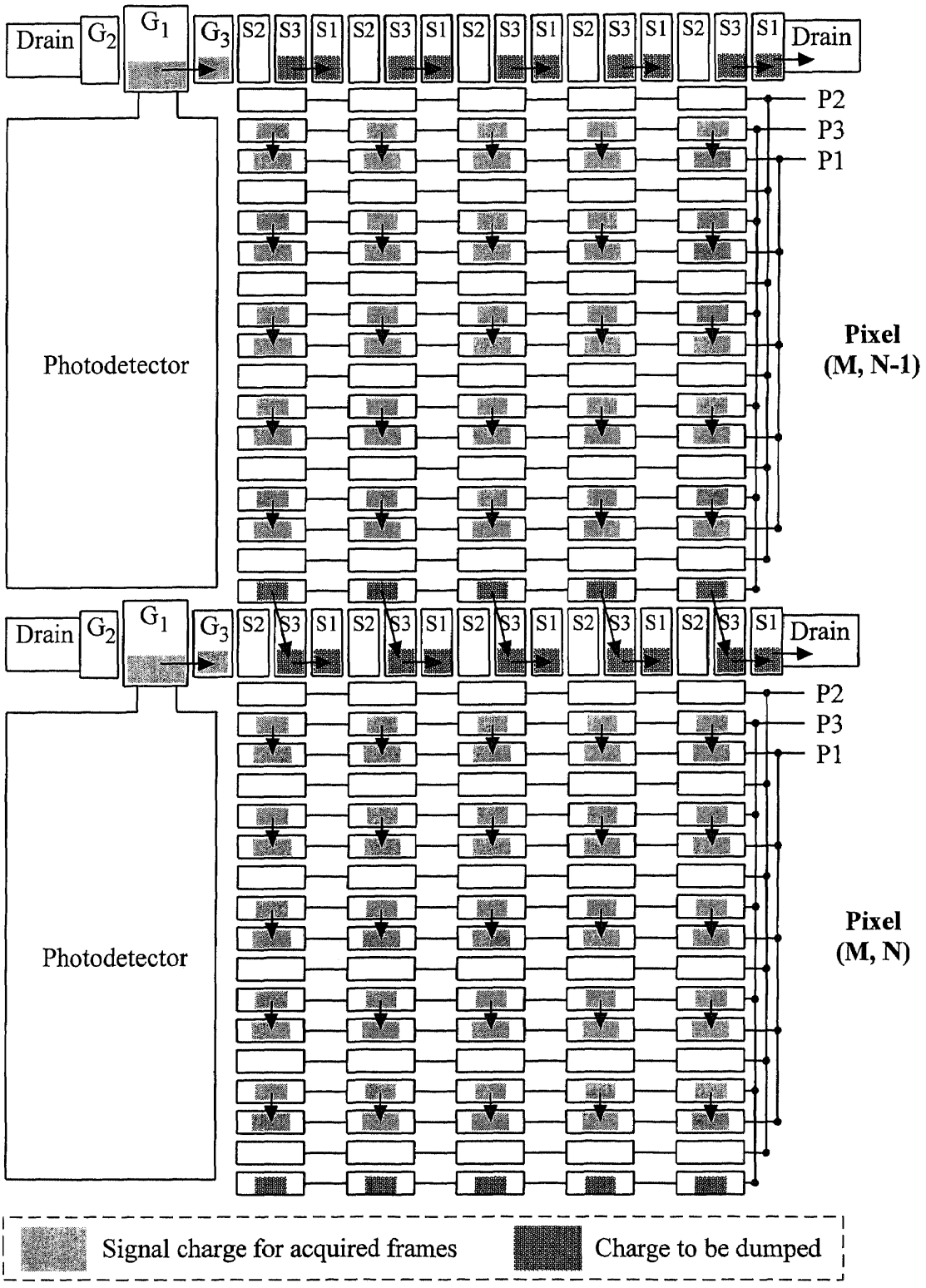
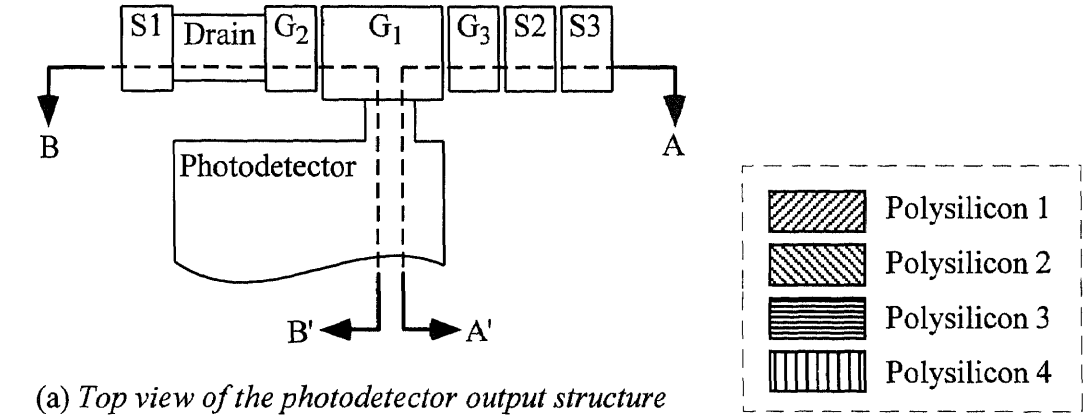
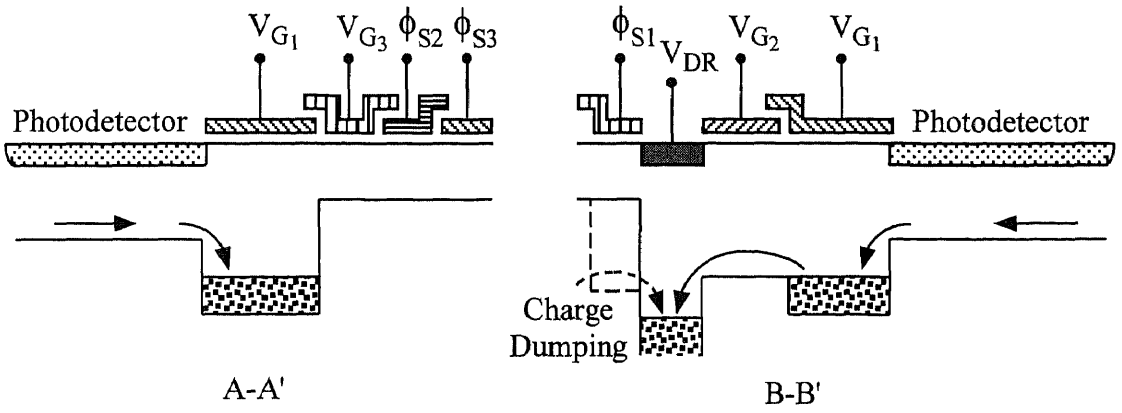


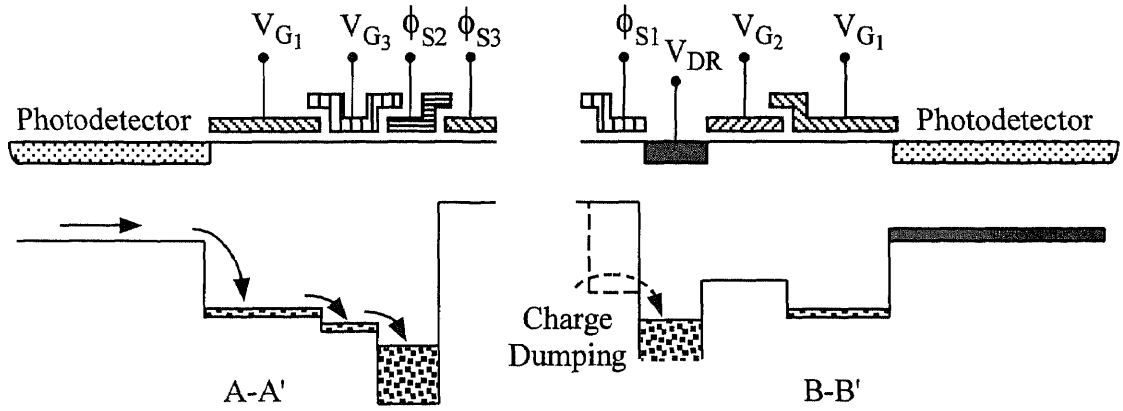
Figure 4.10 *Charge transfer diagram in macropixels when the VHFR burst-image sensor collecting the first frame charge signal of each 5 frames.*



(a) *Top view of the photodetector output structure*

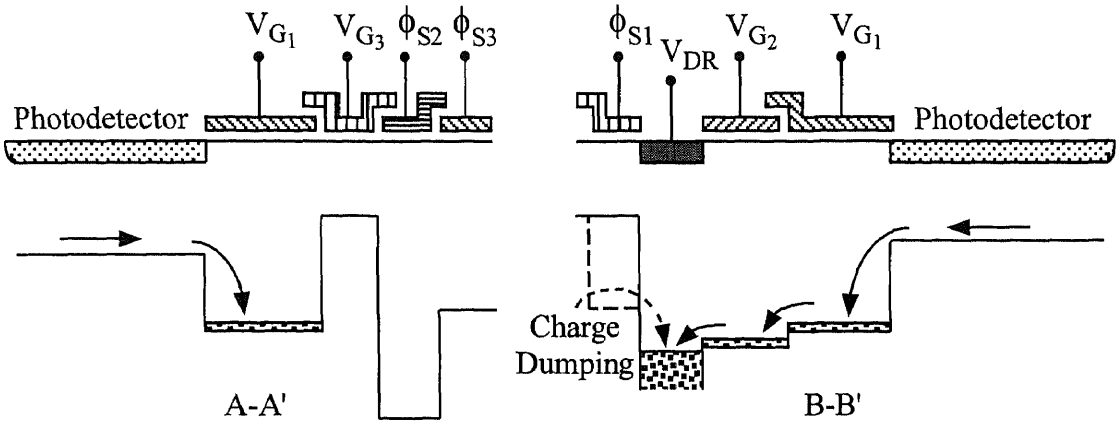


(b) *Cross-section of A-A' and B-B' and potential profiles during the charge accumulation*



(c) *Cross-section of A-A' and B-B' and potential profiles during the charge readout*

Figure 4.11 *Construction and operation of photodetector readout in non-continuous sampling mode.*



(d) *Cross-section of A-A' and B-B' and potential profiles when dumping the chage in skipping the samples*

Figure 4.11 *(Continued)*

Figure 4.9 illustrated the clock waveforms of each clock phase during the charge readout period. In this case, G1, G2, and G3 are kept at a fixed voltage required for dumping the charge collected by the photodetector to the blooming/dumping drain. During the frame readout period, the clock phase S1 is kept in the OFF state to form the induced channel stops for parallel transfer of the charge signals of the acquired frames to the OS registers. During the frame readout, the imager is reformatted into four [180x(5+1)]x[180x6] parallel registers, one for each quadrant. The charge transfers in the macropixels during the frame readout period are described in Appendix A, Section A.2.

4.4 Experimental Results of VHFR Burst-Image Sensor

4.4.1 VHFR Burst-Image Sensor Chip

Following the process specifications (see Chapter 5) based on simulation results described in Chapters 6 and 7, a wafer lot of VHFR burst-image sensors was fabricated at the David Sarnoff Research Center (Sarnoff). The operation of the VHFR burst-image sensors was demonstrated at the Princeton Scientific Instruments (PSI), Inc. using camera

electronics developed by PSI. The presently available data for analysis includes only operation of a single quadrant of the VHFR burst-image sensors with 180x180 pixels that were fabricated using the high BCCD implant dose option (see Chapter 5) [84]. The photograph of the 2-cmx2-cm VHFR burst-image sensor chip is shown in Figure 4.12.

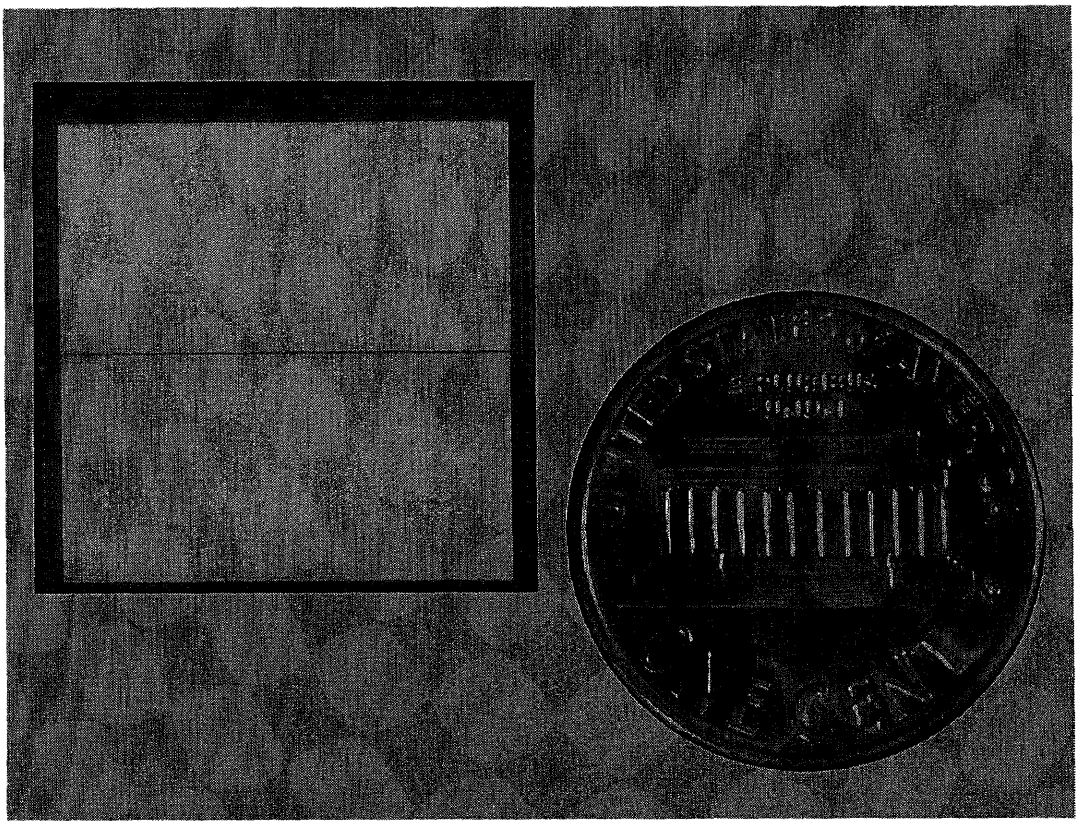


Figure 4.12 *Photograph of VHFR burst-image sensor.*

4.4.2 Display of Sequence of 30 Frames of Image

As described in Section 4.3, when the image acquicision is stopped, charge signals corresponding to 30 image frames are stored in the BCCD pixel memory of the imager as illustrated in Figure 4.13.

During the image readout, charge signals are transferred to the output amplifier and stored and reformatted in a external computer memory. A display of 30 image frames

in the form of mosaic is shown in Figure 4.14. Each image frame has 180x180 pixels for one imager quadrant.

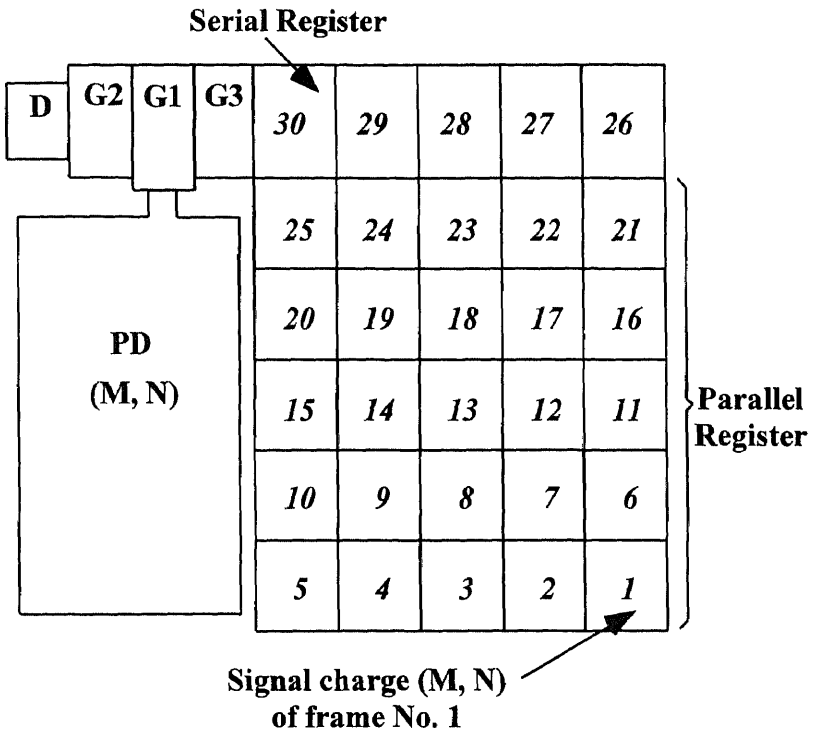


Figure 4.13 *Charge signals stored in the BCCD memory at one pixel location corresponding to 30 image frames.*

4.4.3 Test Set-up

The test set-up developed by PSI for operation of the VHFR burst-image sensors is illustrated in Figure 4.15. The optical test pattern is illuminated by a sequence of 0.4 μsec LED pulses. The LED pulse controlled by computer can be turned ON at any frame time. The optical pattern is detected by VHFR burst-image sensor at a frame rates up to 10^6 frames/sec. The output signal of VHFR burst-image sensor is readout by dual-slope correlated-double sampling to eliminate the reset noise. For clock frequency of the output serial BCCD register of 120 kHz, the readout noise was measured as 9 rms electrons/pixel [84]. After A-to-D conversion, the digital signal is read by a PC and is

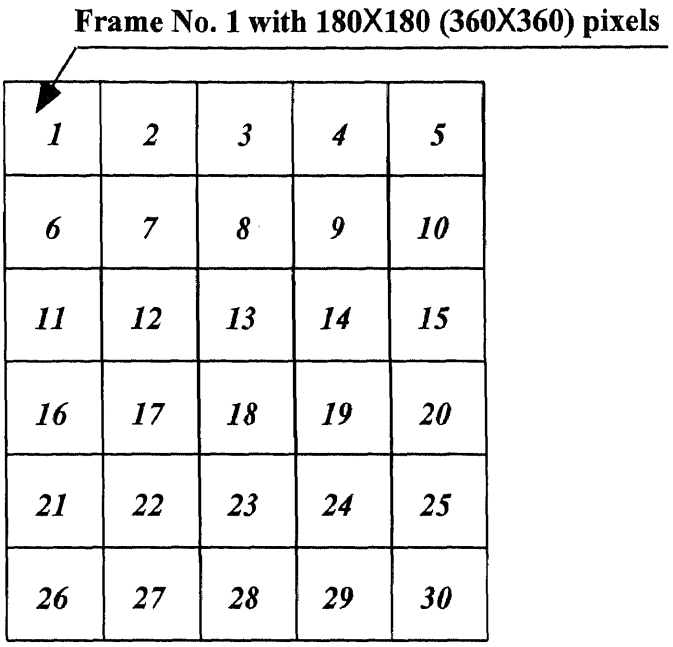


Figure 4.14 *Display of 30 image frames.*

stored in its memory. When the readout of the imager BCCD is completed, the computer (PC) reconstructs the data and displays a sequence of 30 reformatted image frames (see Figure 4.14). For the imager readout rate of 120 kHz, the total readout time for 30 image frames was about 8 seconds. To reduce the dark current, the VHFR burst-image sensor was TE cooled at -30 °C. The resulting dark current was found to be about 100 electrons/pixel for the pixel rows next to the output serial register and about 200 electrons/pixel for the last pixel rows in the frame. Furthermore, an optical shutter was employed to eliminate the optical smear during the 8 seconds readout time. The ON and OFF switching time of optical shutter was about 20 msec.

4.4.4 Test Results

For the following test results, the images were acquired with the integration time $T_i = 2.0$ μsec for the first frame, and $T_i = 1.0$ μsec for the next four frames of each 5-frame sequence.

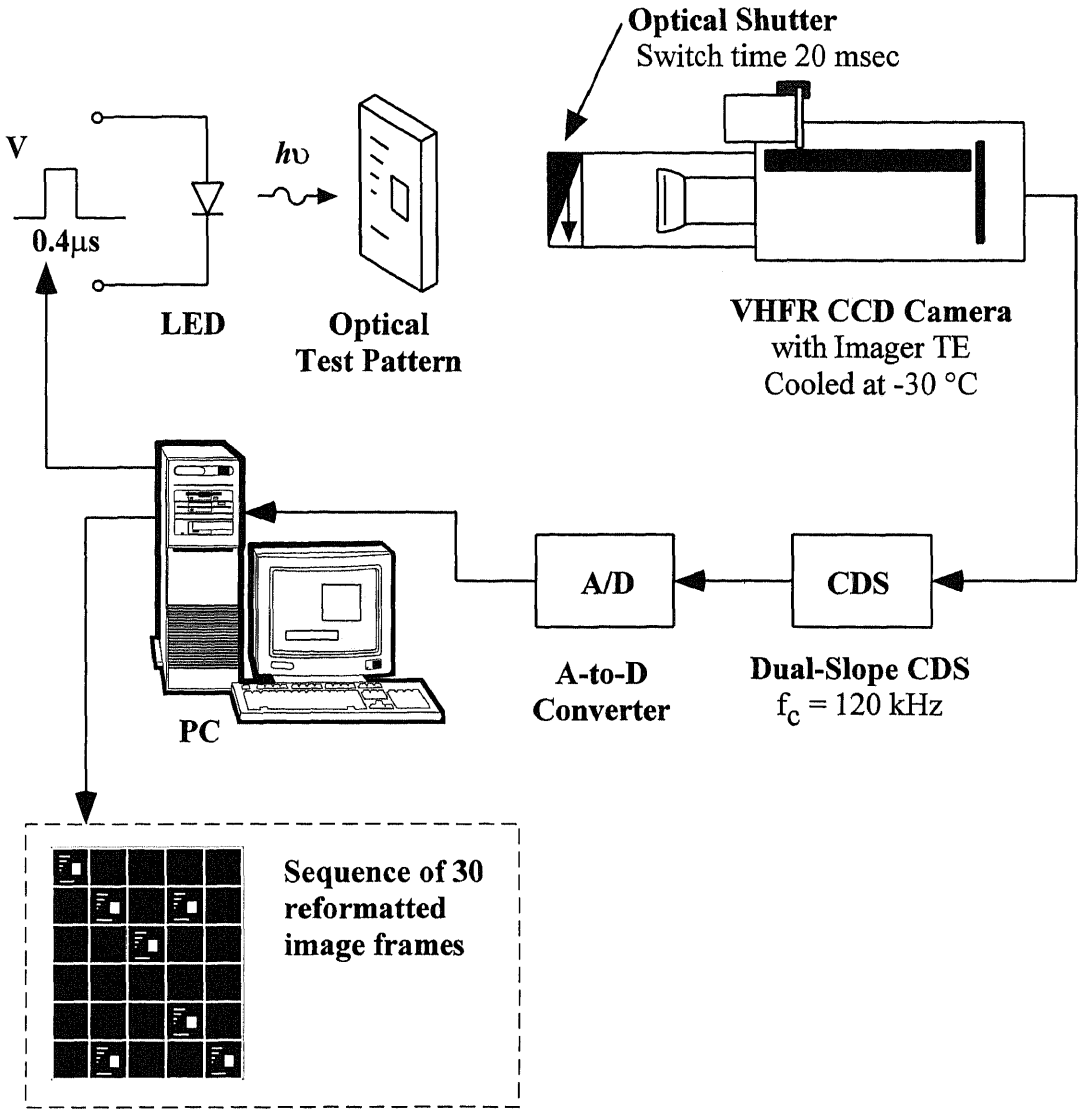


Figure 4.15 *Test set-up of image of optical test pattern.*

Figure 4.16 shows one frame of detected image of optical test pattern with 180x180 pixels. Figure 4.17 shows 30 sequential images of optical test pattern illuminated by 0.4 μsec LED pulses.

The maximum charge handling capacity of the BCCD pixel memory for proper operation of the VHFR burst-image sensor with the high BCCD implant dose was measured to be about 11,000 electrons/pixel. This was the maximum charge signal above which the BCCD memory started to show an increase in vertical transfer loss. However,

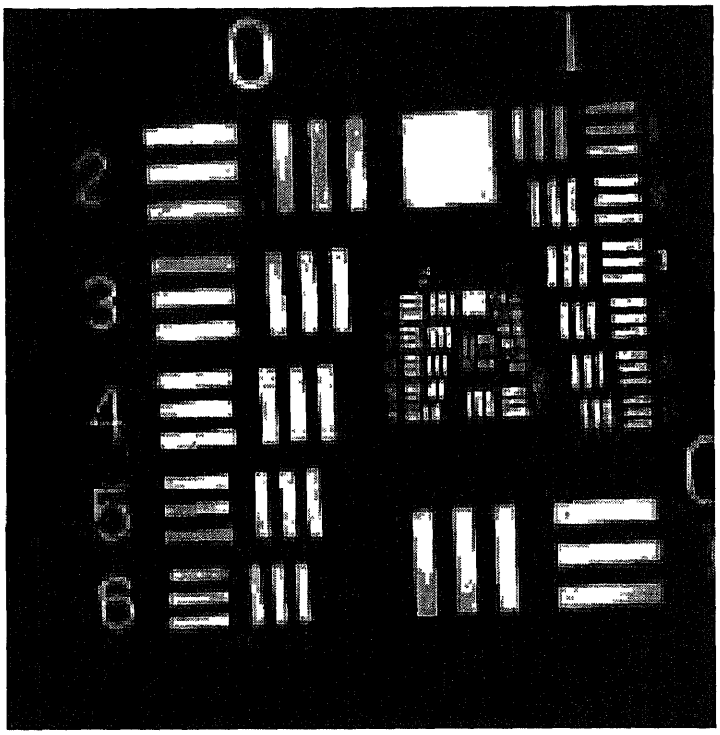


Figure 4.16 *One frame of detected image of optical test pattern with 180x180 pixels.*

for the test results illustrated in Figure 4.17, the maximum charge signal level was 8,000 electrons/pixel. Also in this experiment, the 0.4 μsec LED pulses were programmed to be turned ON at the time of 2, 6, 10, 22, 33, and 34 μsec, which are corresponding to frame numbers 1, 5, 8, 18, 27, and 29, respectively.

The BCCD transfer loss and frame-to-frame image lag were estimated by the comparison of the signal intensity of primary image and ghost image [84]. The measurements showed that the intensity of ghost images is less than 1% of that of the primary image. To transfer all of signal charges from BCCD storage memory to output amplifier, the charge signal is subjected to a maximum of 3,240 horizontal and 3,240 vertical transfers. Therefore, the horizontal BCCD transfer loss has been estimated to be about $3x10^{-6}$ per transfer, and the vertical BCCD transfer loss to be less than 10^{-6} per transfer, assuming that no frame-to-frame image lag is presented. At any rate, even with

zero horizontal BCCD transfer loss, the frame-to-frame lag would be only about 1.0%.

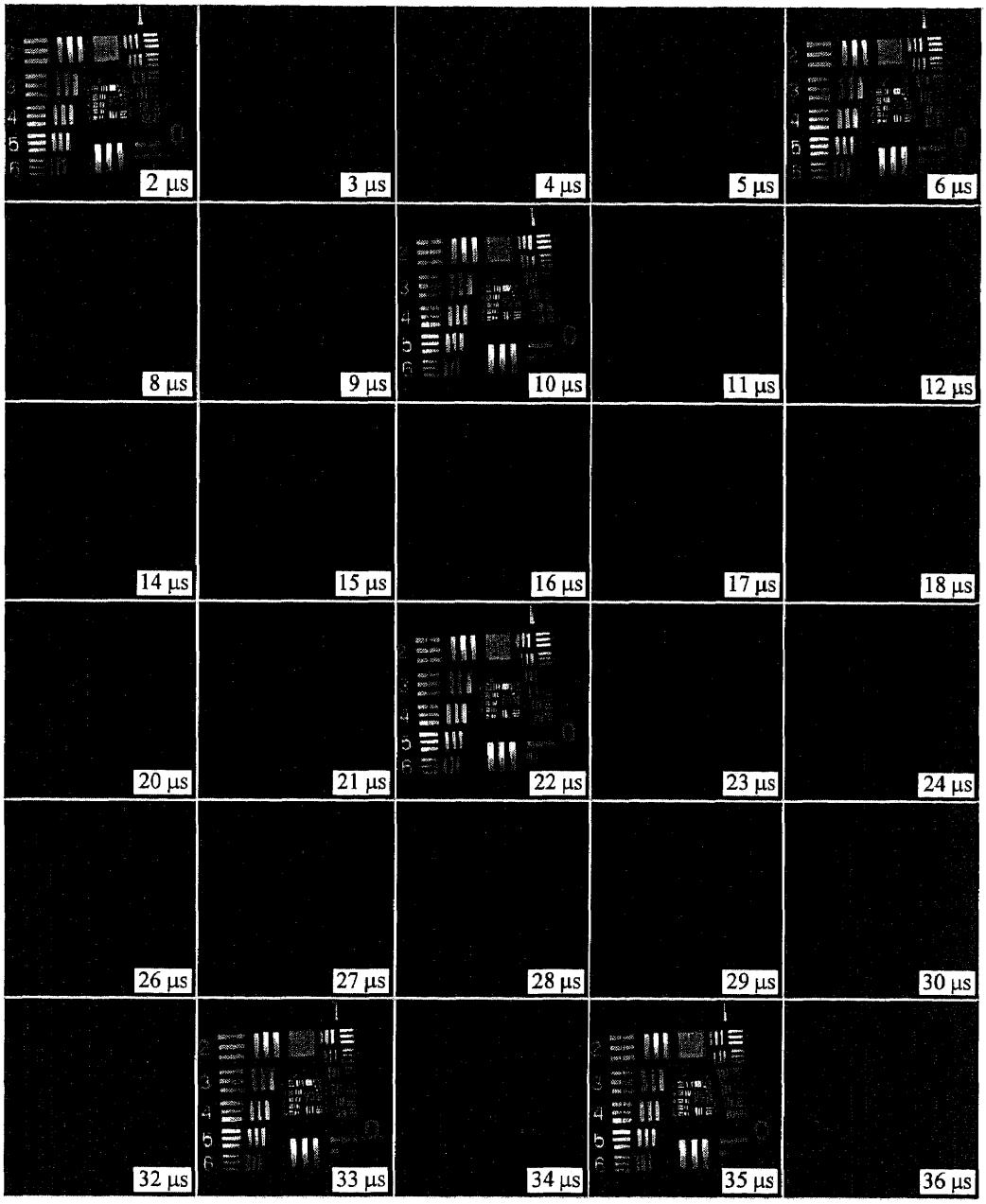


Figure 4.17 *A sequence of 30 images of optical test pattern illuminated by 0.4 µsec LED pulses for frames 1, 5, 8, 18, 27, and 29.*

CHAPTER 5

PROCESS DESIGN FOR THE VHFR BURST-IMAGE SENSOR

5.1 Introduction

The VHFR burst-image sensors were fabricated at the David Sarnoff Research Center (Sarnoff). This chapter presents the process definition for fabrication of these devices. The developed 4-layer polysilicon 3-layer metal BCCD process was based on BCCD and CMOS processes available at Sarnoff. Also included in this chapter are image topography simulations using ISE-TCAD tools with comparison to SEM photographs of the imager structure.

5.2 Fabrication Process

The VHFR burst-image sensor was fabricated by David Sarnoff Research Center using a three-phase buried-channel CCD technology with four-level-polysilicon and three levels of aluminum. This process has been based on the Sarnoff three-level-polysilicon one-level-metal CCD process and the Sarnoff one-level-polysilicon two-level-metal CMOS process. Minimum design rules of 1.5 μm were used for layout of the imager.

5.2.1 Process Technology

As indicated in Section 4.2.4 (see Figure 4.3), the use of an additional (forth) level of polysilicon allows a more efficient design of the serial-parallel register at the macropixels. Two levels of aluminum were used for metal interconnections and the third level of aluminum served as an optical shield over the BCCD memory regions. SiO_2/Si_3N_4 channel dielectric were used to improve the yield and to enhance charge transfer efficiency.

Arsenic and phosphorous dual-implantation was used to form the BCCD channels on p-type substrate to maximize the charge handling capacity and to achieve high fringing field for low transfer losses [85]. Since arsenic has a small diffusion coefficient, most of the implanted arsenic will stay near the silicon/silicon-dioxide interface and form a high concentration n-type layer. The arsenic contributes to the large charge handling capacity of the BCCD well. On the other hand, phosphorus has a large diffusion coefficient, therefore, the implanted phosphorus forms a deep diffusion responsible for large fringing field for a fast charge transfer to the adjacent BCCD well. A modified form of pinned-buried detector (described in Section 7.2) was introduced as high-speed photodetector [86] at each macropixel using a thin p^+ implant, the BCCD implants, and three additional n-type implants to achieve less than 0.1 μsec readout time.

The choice of BCCD implant doses for the fabrication of the VHFR burst-image was based on the 1-D simulation results that will be described in Chapter 6. The fabrication lot was split between two options for arsenic and phosphorus BCCD dual implants. In the lower BCCD implant dose option, the implant doses of arsenic and phosphorus were both chosen as 6.5×10^{11} cm^{-2}. The total implant dose in this case was the same as that presently used by Sarnoff. On the other hand, in order to achieve a larger charge handling capacity of the BCCD register, a higher BCCD implant dose option was chosen with arsenic implant dose of 1.2×10^{12} cm^{-2} and phosphorus implant dose of 1.0×10^{12} cm^{-2}. In this case, according to our 1-D simulation, the maximum BCCD electric field intensity at Si/SiO_2 interface is approaching the critical electric field strength of 3.0×10^5 V/cm [67], [80], as compare to the value of 2.0×10^5 V/cm for the lower BCCD implant dose option.

The BCCD dose is implanted to the p^- substrate in a very early stage of the fabrication, the thermal diffusion of the BCCD implant dose includes practically the full thermal cycle described below, for forming n^+ polysilicon layers, growth of inter-poly oxide, driving in of photodetector n-type implants, and reflowing of inter-metal glass.

The additional n-type photodetector implants have a thermal diffusion of 90 min at 1050 °C and the thermal cycle of inter-metal glass reflowing. However, the photodetector top p^+ (see Section 7.2) implant is only exposed to the thermal cycle associated with the reflow of the of inter-metal glass. Therefore, it will be confined to a shallow region near the Si/SiO_2 interface. The thickness of the SiO_2-Si_3N_4 channel dielectric, the doses and energies of the n-type buried-channel-CCD implant and photodetector implants were selected on the bases of simulations by SUPREM III, SUPREM IV and PISCES IIB. The results of these simulation are presented in Chapters 6 and 7.

In order to maintain high frame to frame fidelity, the detected signal charge must be physically transported to the output amplifier with nearly perfect charge transfer efficiency (CTE) is required. Since the maximum number of CCD transfer stages is 6,480, in order to achieve a total loss (εN) of 1% for entire imager, the transfer efficiency per transfer must by at least 0.999998. Therefore, The SiO_2-Si_3N_4 gate dielectric was used in order to prevent a possible transfer loss due to small potential wells between the gates caused by the lift-up of polysilicon edges that is expected in the case of SiO_2 channel dielectric.

5.2.2 Process Specification

The process specification for fabrication of the VHFR burst-image sensor is summarized below:

- The VHFR burst-image sensors are fabrication using nominally 17.5-μm thick p-type epi wafer with resistivity of 43 ohm-cm on <100> CZ p^+ substrate with resistivity in the range of 0.008 to 0.025 ohm-cm.
- Four levels of polysilicon are used for BCCD gates.
- Three levels of metal, two metal levels are used for interconnections and one for optical shield of the BCCD region not including the detectors.
- A dual channel dielectric of SiO_2/Si_3N_4 is used.

- Two BCCD implant doses have been chosen: low implant dose with $6.5x10^{11}$ cm^{-2} of arsenic and $6.5x10^{11}$ cm^{-2} of phosphorus, and high implant dose with $1.2x10^{12}$ cm^{-2} of arsenic and $1.0x10^{12}$ cm^{-2} of phosphorus with implant energy of 120 keV for arsenic and 180 keV for phosphorus.
- The channel stops for BCCD channels have been defined by SCCD regions in the form of the P-type substrate without the BCCD implant.
- The pinned-buried graded photodetector was constructed by BCCD implant with three additional n-type implants with phosphorus implant doses of $1.4x10^{12}$ cm^{-2}, $1.2x10^{12}$ cm^{-2}, and $1.0x10^{12}$ cm^{-2} and a top thin p^+ implant with BF2 dose of $2.5x10^{14}$ cm^{-2} for the low BCCD implant dose option and $3.0x10^{14}$ cm^{-2} for the high BCCD implant dose option. Implant energy was 120 keV for phosphorus n-type detector implants and 30 keV for the BF2 p^+ detector implant.
- The estimated total thermal diffusion of BCCD arsenic and phosphorus implants is about 330 min at 950 °C and 90 min at 1050 °C. Total thermal diffusion of the additional photodetector phosphorus implants is about 90 min at 1050 °C and 30 min at 950 °C. The total thermal diffusion for BF2 p^+ photodetector implant is about 30 min at 950 °C.
- The N^+ diffusions for blooming/dumping drain and source drains are defined by polysilicon gates on the channel side and thick-oxide regions formed as recessed oxide with a p-type implant. To avoid voltage breakdown of the N^+ diffusions, recessed thick oxide p-type implant was selected to be $3.0x10^{12}$ cm^{-2}.
- As a general design/layout procedure, the pinned-buried photodetector, the output amplifiers, and whenever possible the outside perimeter of the burst-image sensor were surrounded by a P^+ field implant corresponding to boron implant dose of $2.5x10^{15}$ cm^{-2} at 35 keV.

5.3 Fabrication Sequence

The process for fabrication of the VHFR burst-image sensor includes four levels of polysilicon, three levels of metal, eight implants, and requires a total of 21 mask levels.

Mask level 1: ***ACT***, defining the active area;

Mask level 2: ***VTFN***, P-type implant below the recessed thick oxide;

Mask level 3: ***THOX***, defining the thick oxide;

Mask level 4: ***BCCD***, BCCD implants;

Mask level 5: ***P+***, P^+ field implant surrounding the photodetector, output amplifiers, and the imager perimeter;

Mask level 6: ***POLY-1***, BCCD polysilicon-1 gates and output source follower MOSFET gates;

Mask level 7: ***POLY-2***, BCCD polysilicon-2 gates;

Mask level 8: ***POLY-3***, BCCD polysilicon-3 gates;

Mask level 9: ***POLY-4***, BCCD polysilicon-4 gates;

Mask level 10: ***DET-1***, first photodetector additional N-type implant, covering the whole photodetector region;

Mask level 11: ***DET-2***, second photodetector additional N-type implant, forming the first potential step in photodetector;

Mask level 12: ***DET-3***, third photodetector additional N-type implant, forming the second potential step in photodetector;

Mask level 13: ***DET***, photodetector P^+ implant, forming the pinned-buried BCCD channel photodetector;

Mask level 14: ***N+***, source and drain N^+ implants;

Mask level 15: ***C2PL***, defining contacts from metal-1 to polysilicon gates;

Mask level 16: ***AACT***, active area contacts, including contacts to source and drain, as well as to the substrate;

Mask level 17: ***MTL-1***, metal-1 interconnection lines;

Mask level 18: ***VIA***, VIAs between metal-1 and metal-2;

Mask level 19: ***MTL-2***, metal-2 interconnection lines;

Mask level 20: ***MTL-3***, metal-3 optical shield; and

Mask level 21: ***BPAD***, bonding pads.

The alignment of the 21 mask levels and fabrication sequence of the VHFR imager are illustrated in Figure 5.1, where the mask levels are denoted by the mask names described above, and the process sequence is given by number from 1 to 21.

A detailed process description is presented in the form of a flow chart in Appendix B. This process flow chart includes all processing steps that have been considered in the process and device simulation described in Chapters 6 and 7. Also illustrated on this flow chart are sketches of the cross-sectional view of the silicon wafer as it changes during the process steps. Finally, the results of all the process steps are illustrated as the schematic cross-sectional view of the silicon wafer in Figure 5.2.

5.4 Process Simulation by Using ISE-TCAD Software

The ISE-TCAD software obtained for the project from Integrated Systems Engineering (ISE) AG, ETH Zentrum, ETZ, CH-8092 Zürich, Switzerland, includes the following products:

- $LIGAMENT_{-ISE}$ Layout, process specification flow interface for 1-D and 2-D process simulation;
- $TESIM_{-ISE}$ 1-D process simulator;
- $DIOS_{-ISE}$ 2-D process simulator;
- $TEDIOS_{-ISE}$ 1-D and 2-D process simulator (a combination of $TESIM_{-ISE}$ and $DIOS_{-ISE}$);
- $MDRAW_{-ISE}$ 2-D mesh generator and structure modeling tool;
- $OMEGA_{-ISE}$ 3-D mesh generator;
- $DESSIS_{-ISE}$ 1-D, 2-D, and 3-D device simulator;

- PICASSO$_{-ISE}$ Visualization tool;
- MOVIE$_{-ISE}$ Visualization and animation tool.

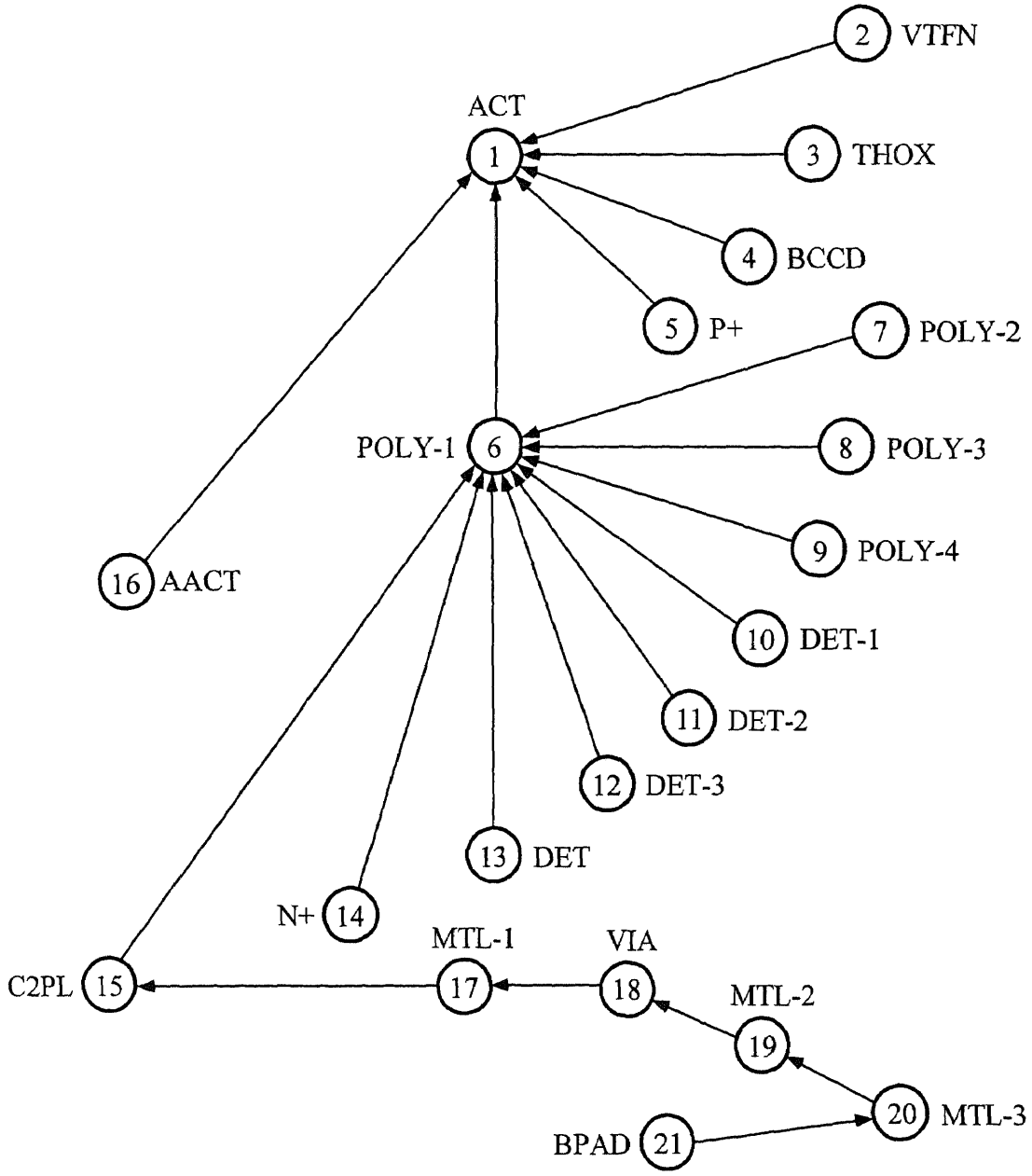


Figure 5.1 *Alignment of 21 mask levels and fabrication sequence of the VHFR burst-image sensor.*

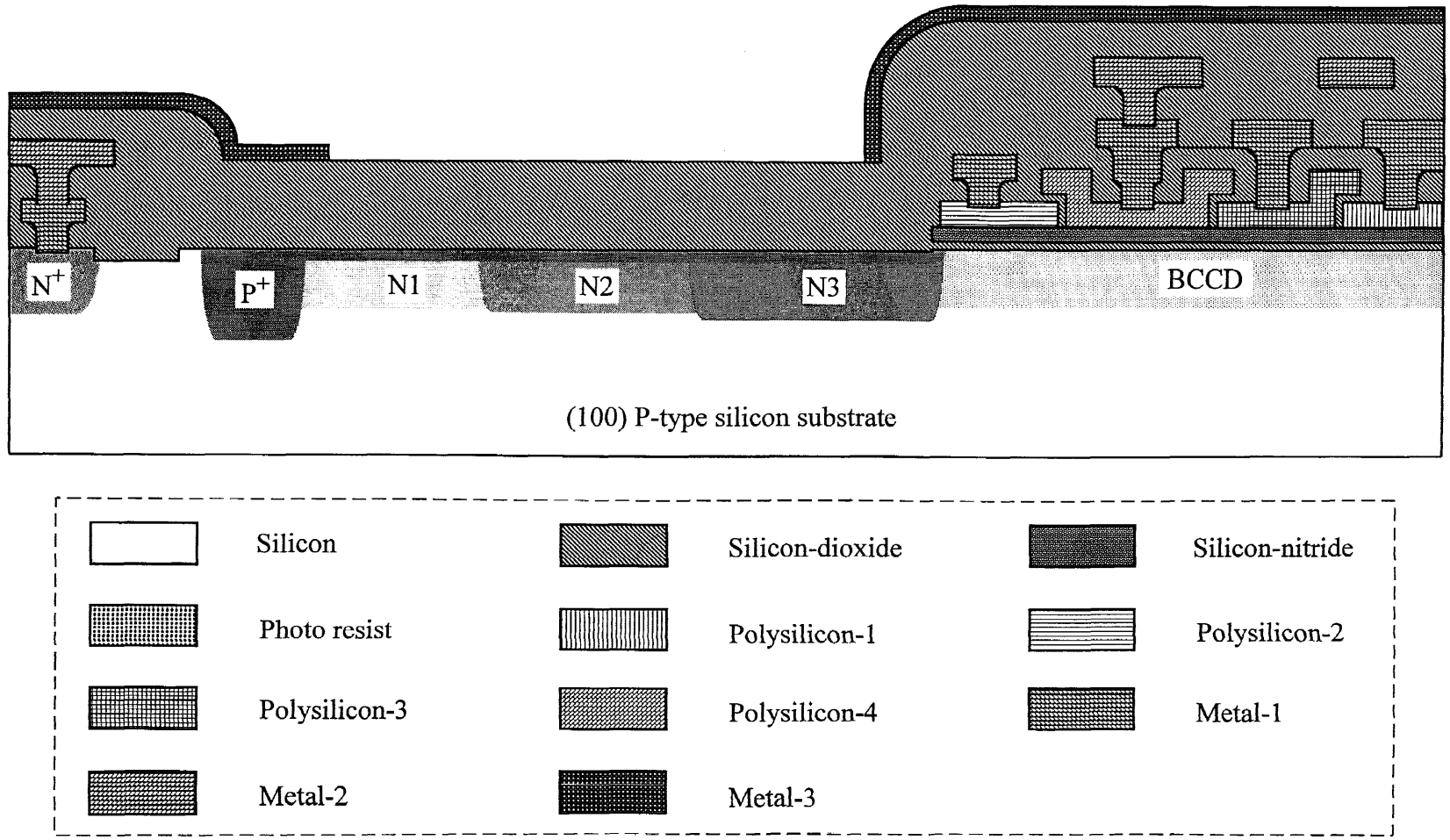


Figure 5.2 *Cross-sectional view of the imager silicon wafer after undergoing all the process steps.*

Figure 5.3 illustrates the capabilities of ISE-TCAD tools as a simulation package which can simulate the device characteristics on the bases of the chip layout and process specification. $DESSIS_{-ISE}$ reads the doping profile from the results of process simulators $TESIM_{-ISE}$, $DIOS_{-ISE}$, and $TEDIOS_{-ISE}$ for 1-D and 2-D device simulation. However, a Gaussian approximation of the doping profile is used for the 3-D device simulation by using $DESSIS_{-ISE}$.

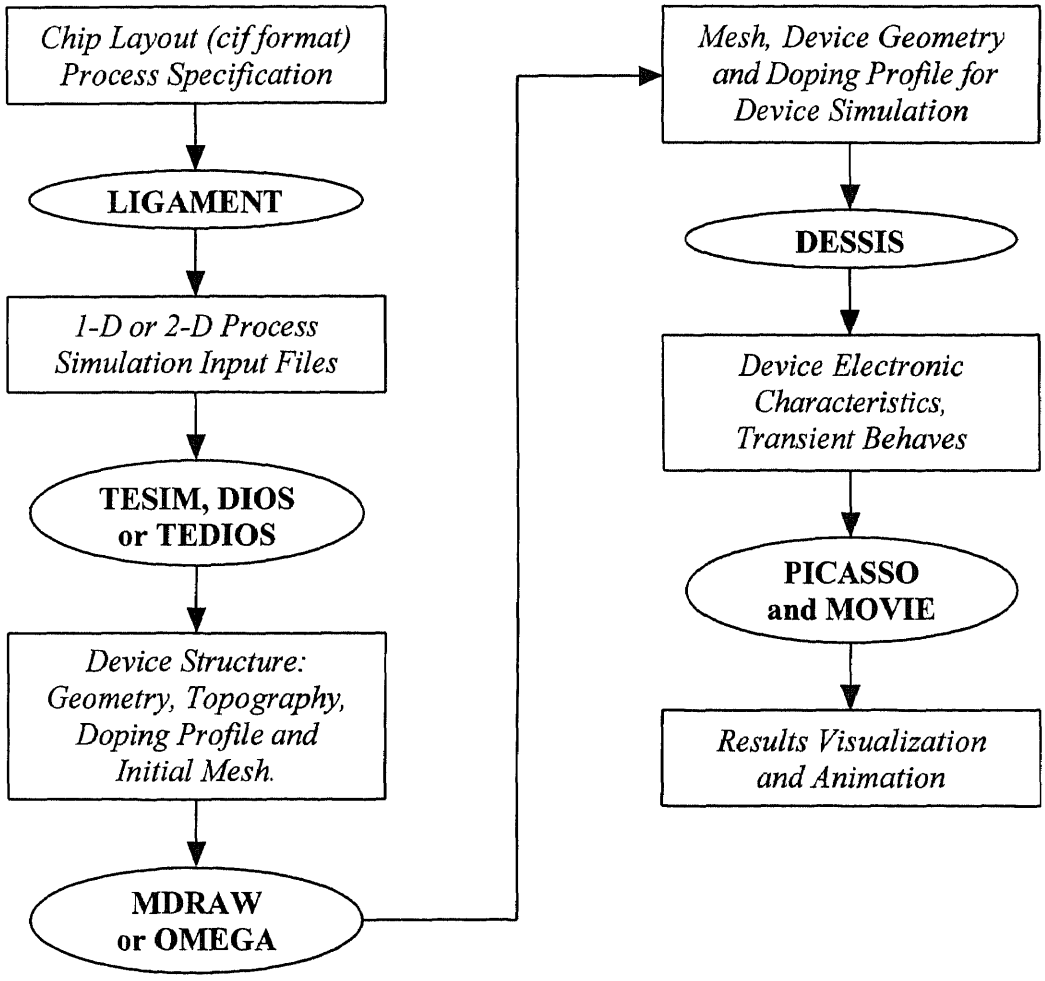


Figure 5.3 *Procedure of simulation by using ISE-TCAD package.*

In order to obtain the device characteristics of CCD imager (such as charge handling capacity of CCD well, charge transfer efficiency of CCD register, photodetector charge readout speed), the amount of electrons in a specified region is an important simulation parameter. However, as mentioned in Chapter 3, the device simulator $DESSIS_{-ISE}$ in the present version of ISE-TCAD package does not have the capability of integrating the amount of electrons for a specified region. This drawback of ISE-TCAD package limits its application in the simulation of the device characteristics of CCD imagers.

As mentioned before, the fabrication of the VHFR burst-image sensor has twenty-one levels of masks which include four levels of polysilicon and three levels of metal. The stack of four polysilicon and three metal layers will cause a large variation of the thickness on top of silicon substrate. In this dissertation, the process simulation by using $TEDIOS_{-ISE}$ of ISE-TCAD package was used to obtain the cross-sectional topography of the imager structure. The simulation results are shown in Figures 5.4, 5.5, and 5.6. Figure 5.4 shows a cross-sectional topography corresponding to cut-line along the parallel register, Figure 5.5 shows a cross-sectional topography corresponding to cut-line along the serial-parallel register, and Figure 5.6 shows the cross-sectional topography corresponding to cut-line across vertical BCCD channels.

After the imager chip has been fabricated, SEM photographs along different cross-sections of the chip were taken by David Sarnoff Research Center to investigate the possible shorts between different polysilicon layers and metal lines. Simulation of cross-sectional topography corresponding to the cut-lines of SEM pictures was done using $TEDIOS_{-ISE}$ to calibrate the existing process models. The SEM pictures and corresponding simulation results are shown in Figures 5.7 and 5.8. The SEM photograph of parallel BCCD gate structure is shown in Figure 5.7(a) and the corresponding simulation result, by $TEDIOS_{-ISE}$ is shown in Figure 5.7(b). It should be noted that, based on the device structure and parameters provided by the author, the simulation result

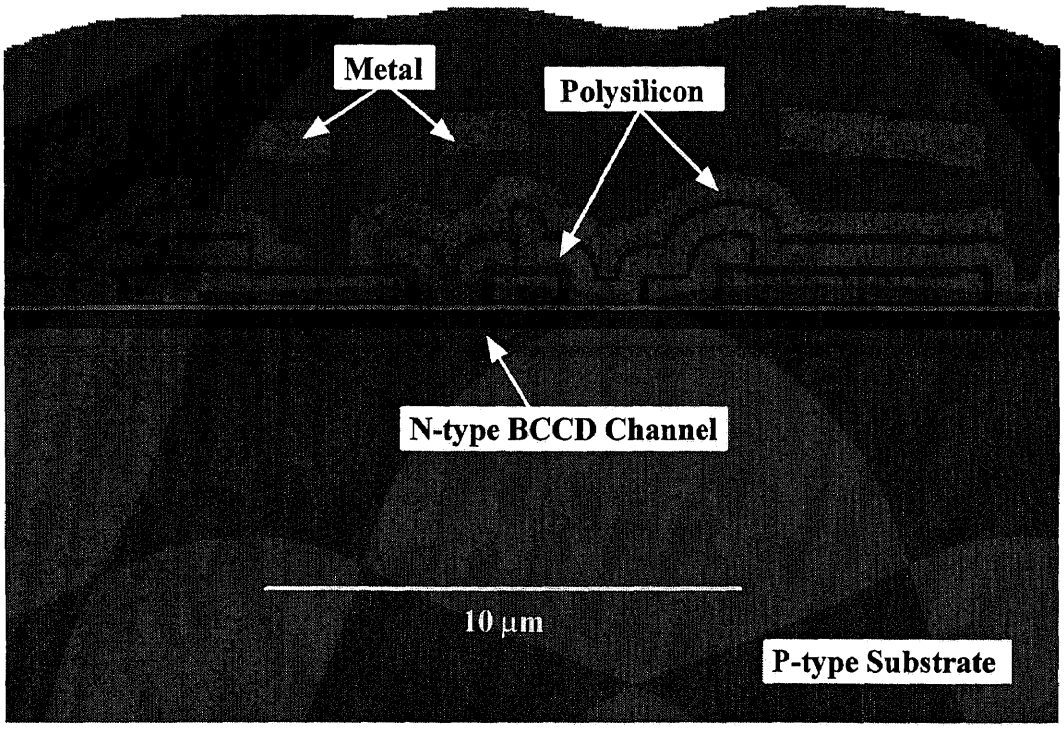


Figure 5.4 *Cross-sectional topography corresponding to cut-line along the parallel register.*

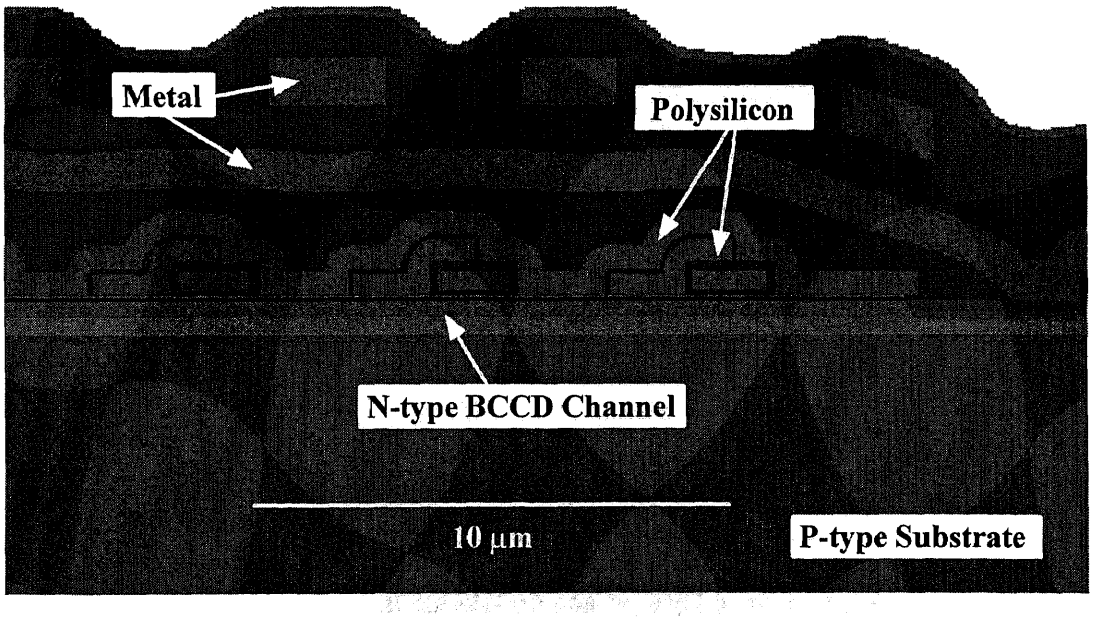


Figure 5.5 *Cross-sectional topography corresponding to cut-line along the serial-parallel register.*

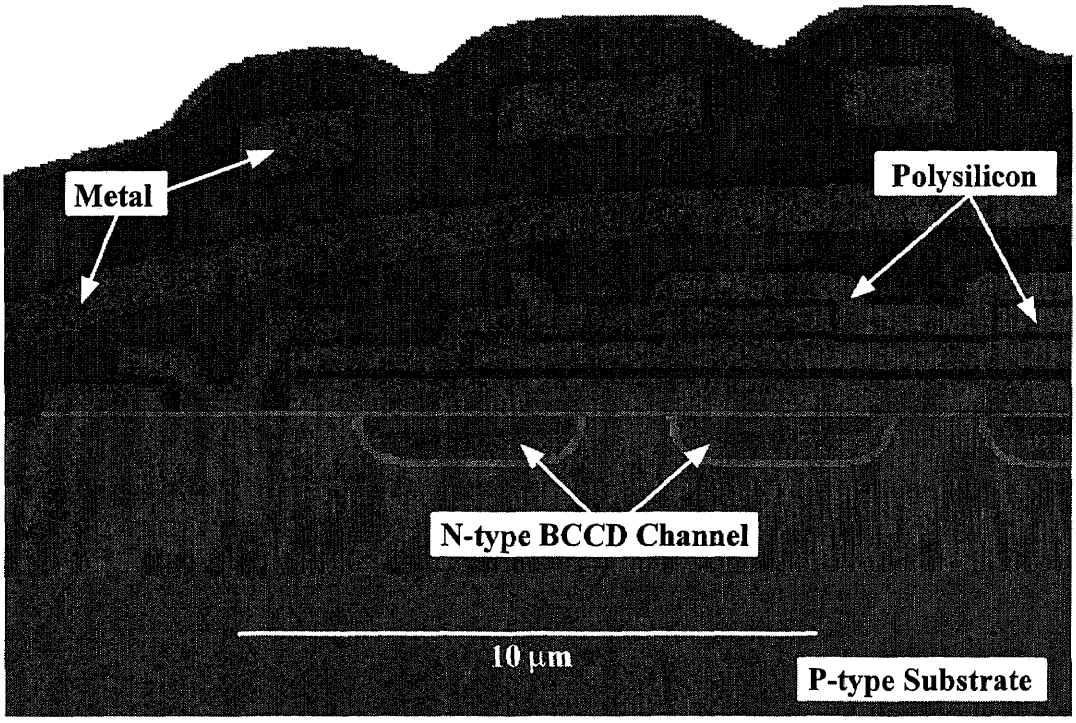
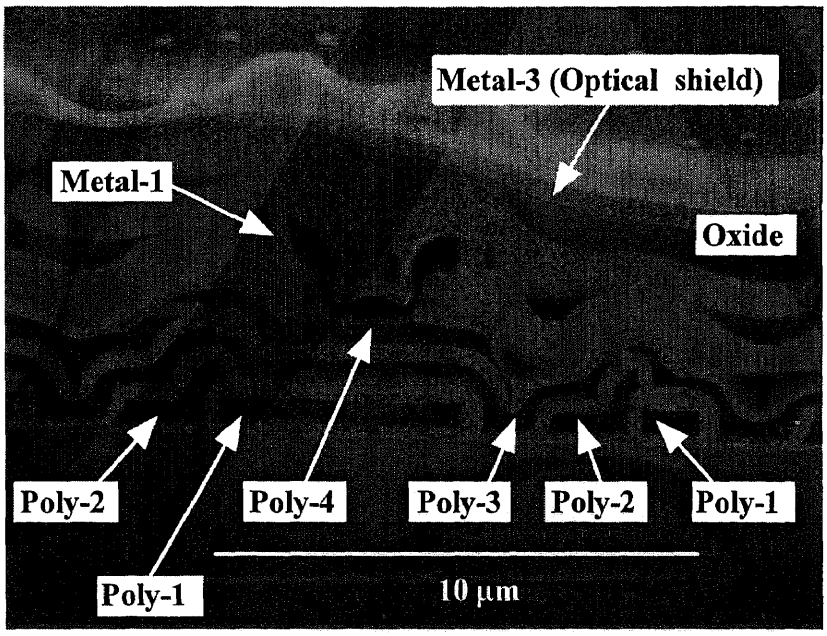


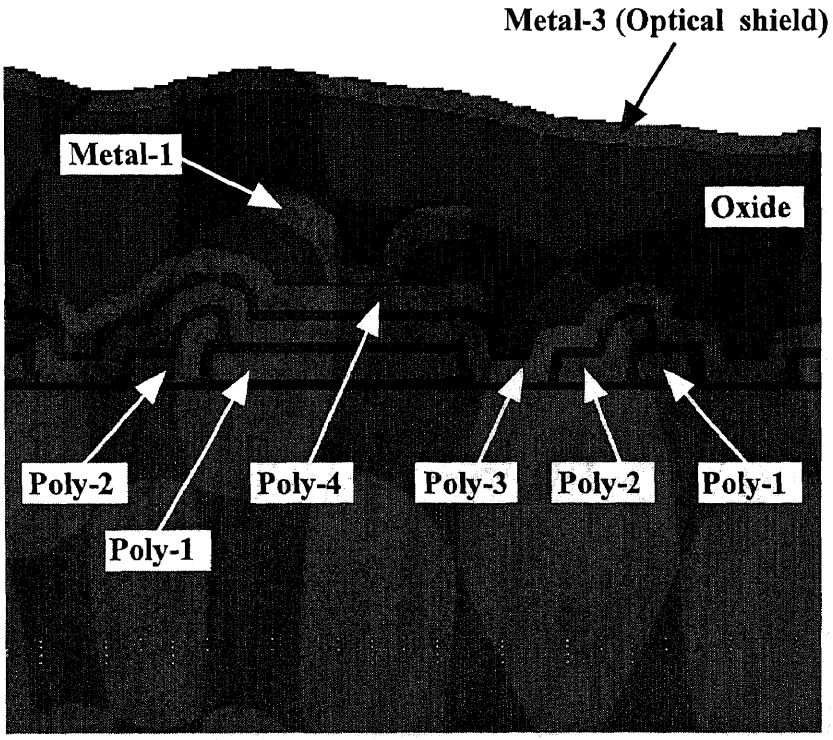
Figure 5.6 *Cross-sectional topography corresponding to cut-line across the vertical BCCD channels.*

shown in Figure 5.7(b) was performed by Zeynep Pektas of Electronic Imaging Center at NJIT who is expected to continue this work as part of her doctoral dissertation research with Professor Kosonocky. Inspection of Figures 5.7(a) and (b) shows that, after calibration the glass reflow parameter (by Zeynep Pektas), good agreement can be obtained between SEM and simulated device cross-section. The SEM photograph gate structure across serial BCCD channel is shown in Figure 5.8(a) and the corresponding simulation result, by $TEDIOS_{-ISE}$ is shown in Figure 5.8(b).

Inspection of Figures 5.7 and 5.8 shows that, the SEM photographs of the gate structures and their corresponded simulation result are quite similar. Thus, the process models which have been used in simulation can be used to predict the gate structures of the new chips and can be useful for defining layout design rules for a new process.

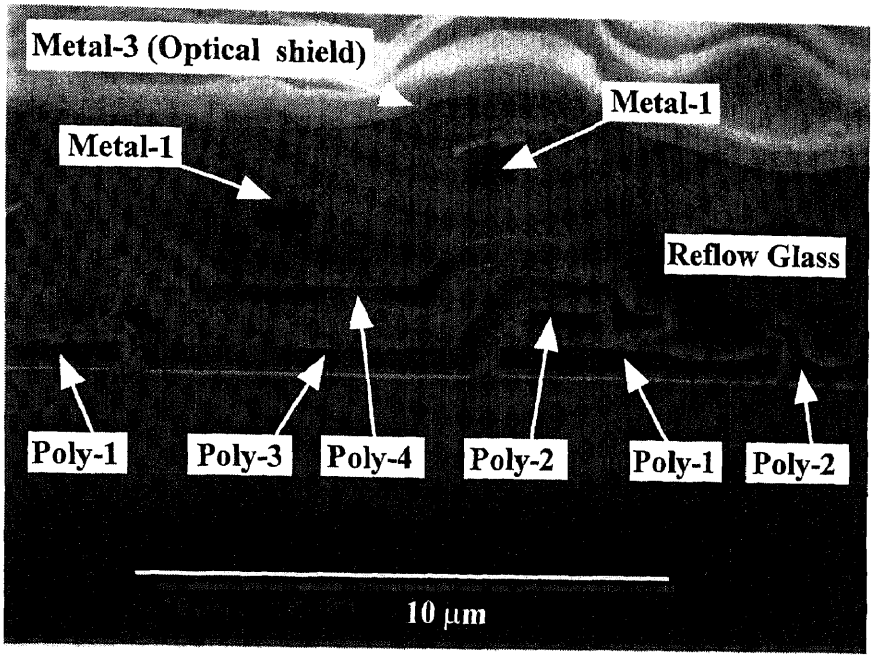


(a)

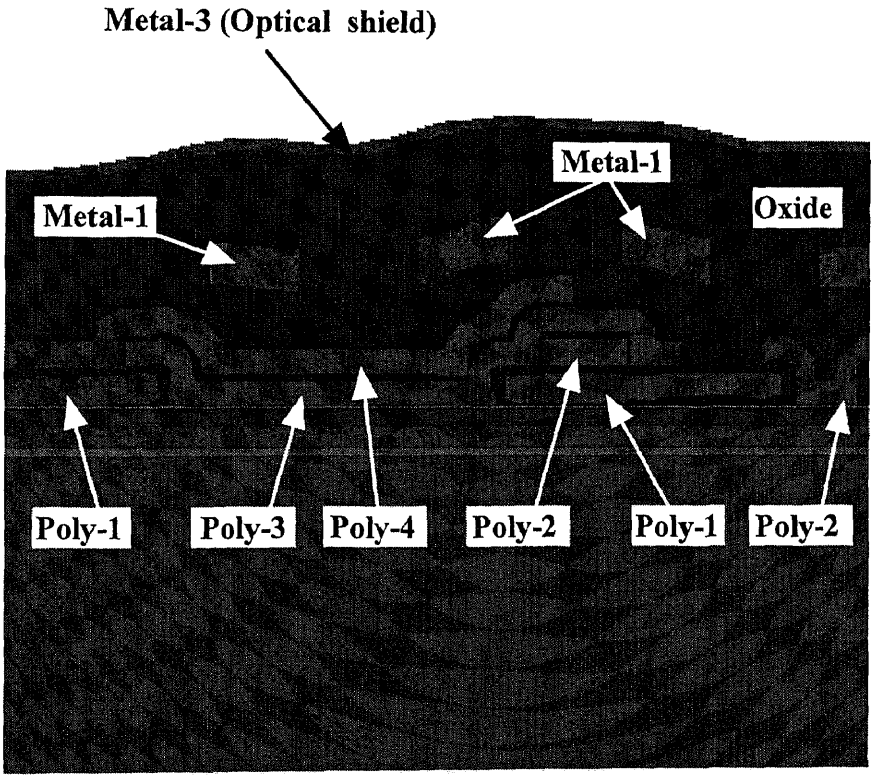


(b)

Figure 5.7 *Parallel BCCD gate structure, with SEM photograph in* (a), *and simulation result in* (b).



(a)



(b)

Figure 5.8 *Gate structure across serial BCCD channel, with SEM photograph in* (a), *and simulation result in* (b).

CHAPTER 6

PROCESS AND DEVICE SIMULATIONS OF THE BCCD STRUCTURES

6.1 Introduction

The two major objectives of the process design of the process and device simulations of the VHFR burst-image sensor BCCD structures presented in this chapter are to achieve (1) a high charge transfer efficiency and (2) a maximum charge handling capacity of the BCCD pixel memory elements. The process and device simulations presented in this chapter were used to define the imager process described in Chapter 5 and to predict the expected BCCD performance characteristics. After defining three different BCCD operation modes, one-dimensional (1-D) and two-dimensional (2-D) process and device simulation results are presented. These results include the 1-D simulation of BCCD charge handling capacity and BCCD channel potential as function of gate voltage, 2-D simulation of BCCD charge handling capacity as function of gate length, 2-D simulation of vertical BCCD channels with SCCD channel stops, and estimation of the charge-to-voltage conversion factor of the output amplifier. For comparison, the presently available corresponding test results are also presented in this chapter.

6.2 Process Definition for Simulations

As described in Section 4.2.2, the basic structure of the serial-parallel (SP) register and parallel (P) register is a three phase BCCD with three layers of polysilicon gates. The three phase CCD structure used for the simulation is shown in Figure 6.1. It contains three layer of polysilicon gates. As mentioned before, to assure a high charge transfer efficiency we have used a process with a dual gate dielectric having 350 Å SiO_2 layer covered with 650 Å Si_3N_4 layer. On the basis of the minimum design rules of 1.5 μm, the minimum size of the micropixel is 4.5 μm^2 (1.5-μmx3.0-μm).

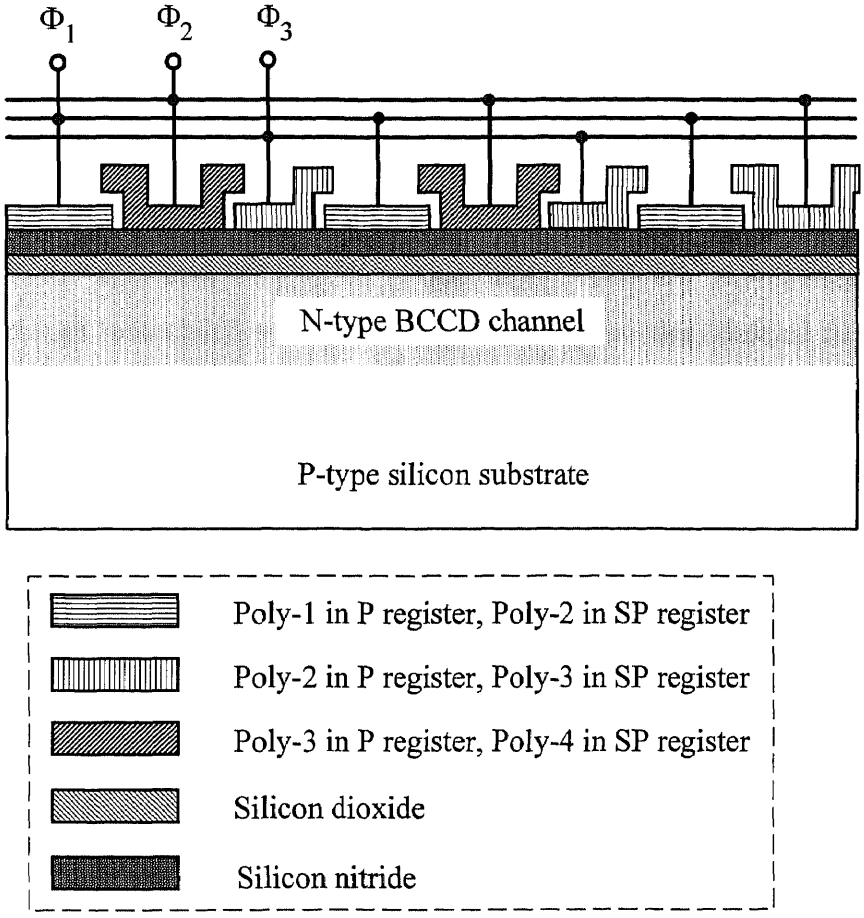


Figure 6.1 *Three phase CCD used for simulation.*

The VHFR burst-image sensors are fabricated using nominally 17.5-μm thick p-type epi wafer with resistivity of 43 ohm-cm on <100> CZ p^+ substrate with resistivity in the range of 0.008 to 0.025 ohm-cm. The silicon wafer thickness is specified as 500 to 550 μm. For the purpose of simulation, we have assumed that the p-type substrate has a doping concentration of 6.0×10^{14} cm^{-3}. In the simulation presented in this chapter, dual-implant of arsenic and phosphorus are used to form the BCCD channel on p-type substrate with SCCD regions forming channel stops.

6.3 BCCD Operation Modes

There are several ways in applying the clock voltage swing to the BCCD gates to operate a BCCD register. The gates with a high (positive) voltage form potential wells for storage of the charge signal, and the gates with a low voltage form the potential barriers to confine the charge signal under the storage gates between the barrier gates. Three operation modes (associated with different gate voltage swings) defined in this section have been used for the simulations presented in this chapter.

The basic structure of the n-channel BCCD element on a p-type substrate is shown in Figure 2.2(a). It consists of a shallow n-type implanted region covered by a thin insulator (SiO_2-Si_3N_4 layer) and an overlying polysilicon gate. The potential maxima occur in the implanted region, causing electron to be stored in the bulk. As described in Section 2.3, the main advantage of the BCCD is that the majority carrier is stored in the bulk of the semiconductor away from interface traps, as shown in Figure 2.2(b). By avoiding the problems associated with interface trapping, the BCCD can be operated at higher clock rates with greater charge transfer efficiency [41], [87].

As a negative voltage is applied to the gate of the BCCD, the peak potential in the channel as well as the potential in the silicon/insulator interface tends to decrease. The channel stops of the device which are physically adjacent to the channel are at ground potential; these channel stops are a potential source of holes for the valence band in the channel. Thus, the valence band in the channel can never move above ground without attracting an unlimited supply of holes from the channel stop. If the potential applied to the gate is allowed to become increasingly more negative, at some point the potential of the valence band at the silicon/insulator interface reaches the potential of the valence band in the bulk, assuming that the substrate is grounded, and no further reduction in channel potential occurs. The gate voltage at which this condition is reached is referred to as the pinning voltage [41]. When the device is operating with an applied gate voltage equal to or more negative (for a p-type substrate) than the pinning voltage, the device is

said to be operating in the pinning with a constant channel potential corresponding to the pinning condition.

As charge signal is generated either thermally, electrically or optically, the signal, electrons for an n-channel BCCD on a p-type substrate move to the potential maximum. The addition of negative charge causes the peak and surface potentials of the channel to become less positive. Eventually with the continued addition of the charge, a margin signal charge condition will be reached where the signal charge extends to the Si-SiO_2 interface. Another condition on the maximum signal charge is connected by charge confinement by the barrier gates along the channel. In this case the maximum barrier potential defining the BCCD wells is determined by the barrier gates in pinning condition. In other words, as the charge signal in a BCCD well is increased, the minimum channel potential is limited by the maximum channel potential under the barrier gates in the pinning condition. Therefore, to store and confine charge in BCCD for reliable operation, three constraints must be set on the full well conditions [5], [88]. The first condition requires that the peak potential of a full well should be at least 10 *kT/e* greater than the surface potential. This ensures that the signal will not reach the Si-SiO_2 interface and be trapped in fast interface states. To account for thermal emission and clock voltage drop across the chip associated to the a high clock rate [60], the second condition requires that the peak potential of the full well is at least 20 *kT/e* greater than the maximum potential of the pinned barrier gate along the BCCD channel. The third condition is determined by the clock voltage forming sufficient channel stop barrier potential under the gates across the BCCD channels.

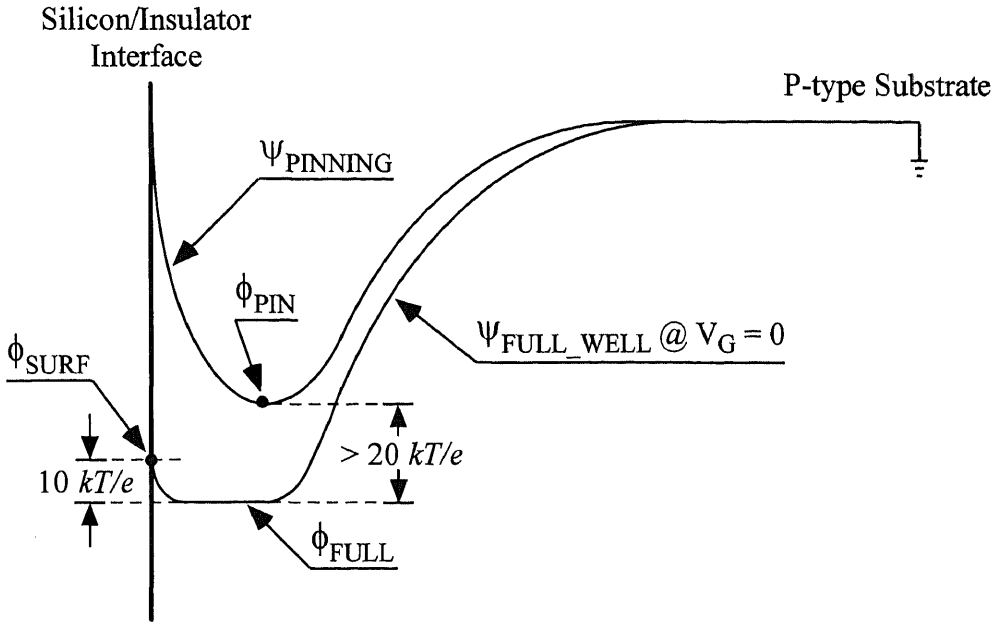
The maximum charge handling capacity per unit area of the BCCD well obtained from 1-D and 2-D simulation by using SUPREM, and PISCES were determined by the first and second constraints. As the BCCD potential barrier is formed under the gate biased at its pinning voltage, the full well potential is determined by the difference of the full well potential (ϕ_{FULL}) to the surface potential (ϕ_{SURF}) as well as by the full well

potential (ϕ_{FULL}) to the maximum pinning potential (ϕ_{PIN}) of the adjacent wells. The determination of the maximum full well condition is given by:

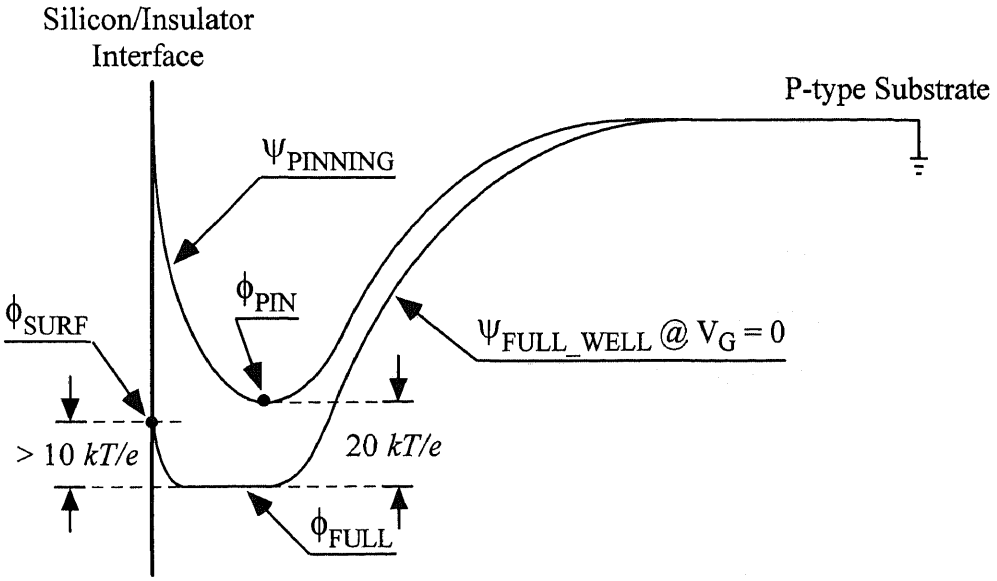
$$\phi_{FULL} \geq MAX(\phi_{PIN} + 20kT/e, \phi_{SURF} + 10kT/e). \quad (6.1)$$

Three following modes (A, B, and C) of BCCD operation were studied using 1-D and 2-D simulation. The full well condition of operation Modes A and B are determined by Equation (6.1). The potential barrier in operation Mode C is formed under the zero biased gate. The determination of maximum full well condition for operation mode C is defined later by Equation (6.2).

- ***Mode A:*** Operation with gate voltage swing, $\Delta V_G = 0 - V_{G(pinning)}$, where BCCD well is formed under zero biased gate, and the gate biased in pinning forms a barrier between the adjacent wells. The potential profile of operation Mode A is shown in Figure 6.2. As illustrated in this figure, the maximum full well is determined either a 10 *kT/e* difference of the full well potential to the surface potential shown in Figure 6.2(a), or a 20 *kT/e* difference of the full well potential to the maximum pinning potential of the adjacent wells shown in Figure 6.2(b).
- ***Mode B:*** Operation with gate voltage swing, $\Delta V_G = V_\sigma - V_{G(pinning)}$. In this case the maximum charge handling capacity is obtained by applying a optimized gate voltage (V_σ) to obtain the $\phi_{SURF} \cong \phi_{PIN}$ + 10 *KT/e*. At this time, the conditions of difference of the full well potential to the surface potential and to the maximum pinning potential of the adjacent wells are both satisfied. The potential profile of operation Mode B is shown in Figure 6.3.
- ***Mode C:*** Operation with gate voltage swing, $\Delta V_G = V_{G(+)} - 0$, where zero biased gates form the barrier between the wells, while the well is created under the gate with positive voltage $V_{G(+)}$. In this case, the maximum charge handling capacity is determined either for a 10 *kT/e* difference of the full well potential [$\phi_{FULL(+)}$] to the surface potential [$\phi_{SURF(+)}$] or for a 20 *kT/e* difference of the full well potential



(a)



(b)

Figure 6.2 *Potential profile of BCCD operation Mode A. The maximum full well determined by the difference of the full well potential to the surface potential in* (a), *and difference between the full well potential to the maximum pinning potential of the adjacent wells in* (b).

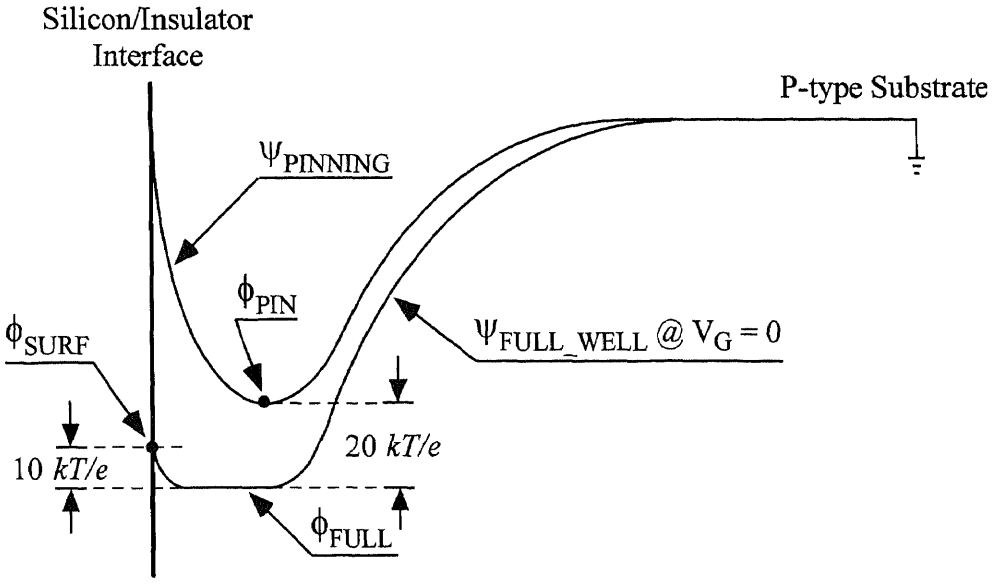


Figure 6.3 *Potential profile of BCCD operation Mode B.*

[$\phi_{FULL(+)}$] to the maximum barrier potential [$\phi_{MAX(0)}$] of the adjacent wells. Similarly to Equation (6.1), the determination of the full well condition is given by:

$$\phi_{FULL(+)} \geq MAX(\phi_{MAX(0)} + 20kT/e, \phi_{SURF(+)} + 10kT/e). \qquad (6.2)$$

Adjusting the applied positive voltage $V_{G(+)}$ carefully, we can always obtain the condition, $\phi_{SURF(+)} \cong \phi_{MAX(0)} + 10\ KT/e$, which gives the maximum charge handling capacity in operation Mode C. The potential profile of operation Mode C is shown in Figure 6.4.

6.4 1-D Process and Device Simulation to Maximize the BCCD Charge Handling Capacity

6.4.1 BCCD Doping Profile

As mentioned previously, in order to achieve a very high charge transfer efficiency and a maximum charge handling capacity, the BCCD channel is formed by arsenic and phosphorus dual-implantation on <100> p^- silicon wafer as the substrate. Figure 6.5 shows the simulation result of one example of doping profile of the BCCD implant used

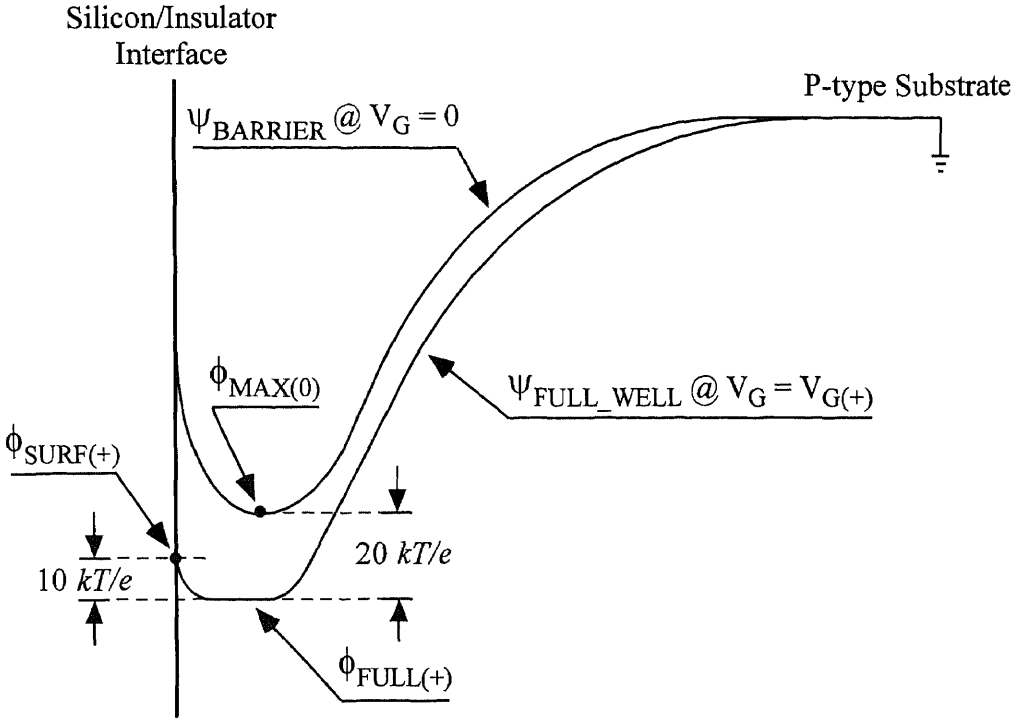


Figure 6.4 *Potential profile of BCCD operation Mode C.*

for the VHFR burst-image sensor simulation with the arsenic and phosphorus implant doses of 1.05×10^{12} cm^{-2} and 1.15×10^{12} cm^{-2}. An inspection of Figure 6.5 shows that, the implanted arsenic is located near the silicon/silicon-dioxide interface and the implanted phosphorus is diffused deeper into the bulk silicon.

6.4.2 Charge Handling Capacity

As will be illustrated by following simulation results, the charge handling capacity of the BCCD well, the gate voltage swing of different BCCD operation modes, and the maximum electric field intensity in silicon and insulator region are the function of the total implant dose as well as the ratio of the arsenic implant dose to the phosphorus implant dose.

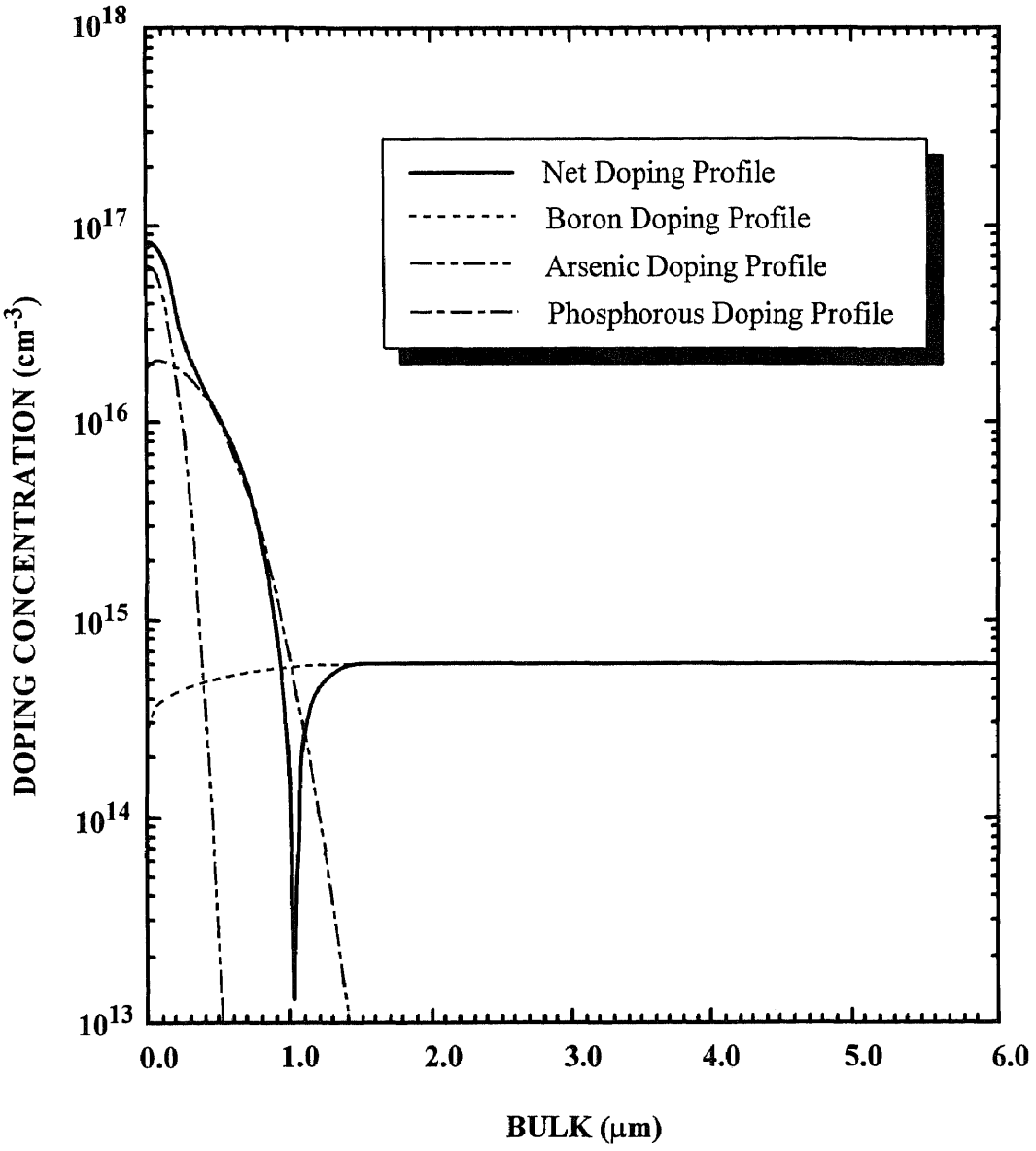


Figure 6.5 *Doping profile of BCCD implant (As = 1.05 x10^{12} cm^{-2} @120 keV, Phosphorus = 1.15 x10^{12} cm^{-2} @180 keV) on P-type substrate (B = 6.0x10^{14} cm^{-3}).*

As Function of Total Implant Dose

Charge handling capacity (in electrons/μm^2) and operating voltages are shown in Figures 6.6 and 6.7, respectively, for operation modes A, B, and C, as a function of total implant

dose for a fixed As implant dose of $1.0x10^{12}$ cm^{-2}. For a comparison, Figures 6.8 and 6.9 show the charge handling capacity and operating voltages, respectively, for operation modes A, B, and C, as a function of total implant dose for a fixed P implant dose of $1.0x10^{12}$ cm^{-2}.

As illustrated in Figures 6.6 and 6.8, charge handling capacity is proportional to the total BCCD implant dose for operation modes B and C. However, for operation mode A, the charge handling capacity increases at a considerable slower rate with the total BCCD implant dose, especially for the fixed As implant dose of $1.0x10^{12}$ cm^{-2}. Inspection of Figures 6.6, 6.7, 6.8, and 6.9 shows that, while mode C has charge handling capacity only 5 to 10% smaller than mode B, it requires about 30 to 40% smaller clock voltage swing ΔV_G.

Effect of the Gate Dielectric Thickness

The simulation results presented in Figures 6.6 to 6.9 were done for the 350Å-SiO_2 and 650Å-Si_3N_4 dual gate dielectric that was used for the fabrication of the VHFR burst-image sensors. Inspection of these figures shows that, as the total BCCD implant dose is increased above $3.0x10^{12}$ cm^{-2}, the gate voltage swing for operation modes A and B becomes bigger than 15 volts. Similarly, as the total BCCD implant dose is increased to above $4.0x10^{12}$ cm^{-2}, the gate voltage swing of operation Mode C becomes also bigger than 15 volts. The large gate voltage swings are caused by the high BCCD implant dose as well as the relative thick channel dielectric. Since SiO_2 has a dielectric constant of 3.9 and Si_3N_4 has a dielectric constant of 7.5, the effective channel dielectric for the above simulation corresponds to about 700 Å of SiO_2. In order to reduce the gate voltage swing for these higher BCCD implant doses, the thickness of channel dielectric has to be reduced.

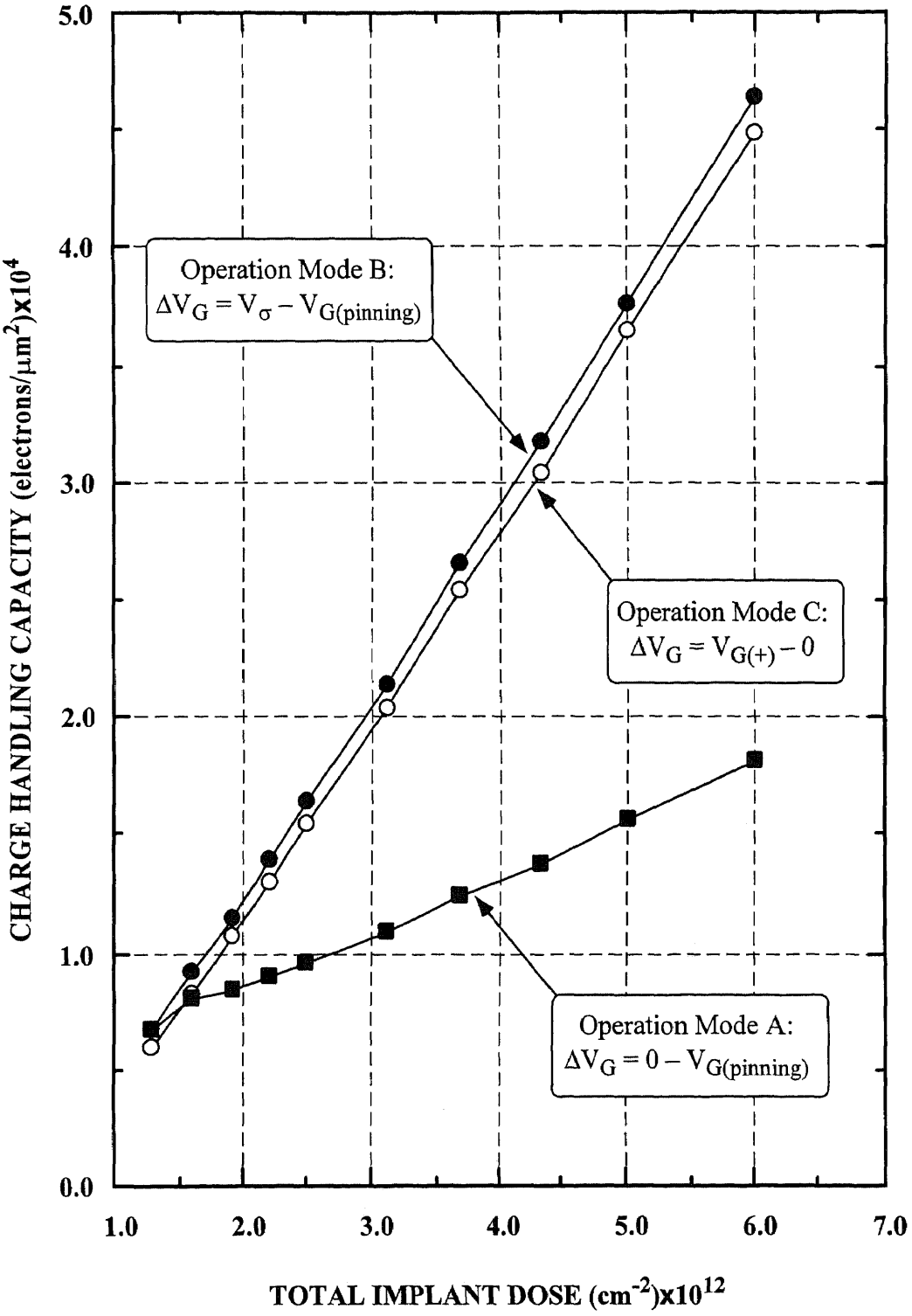


Figure 6.6 *Charge handling capacity as function of total implant dose (with As dose of $1.0x10^{12}$ cm^{-2}) for operation modes A, B, and C.*

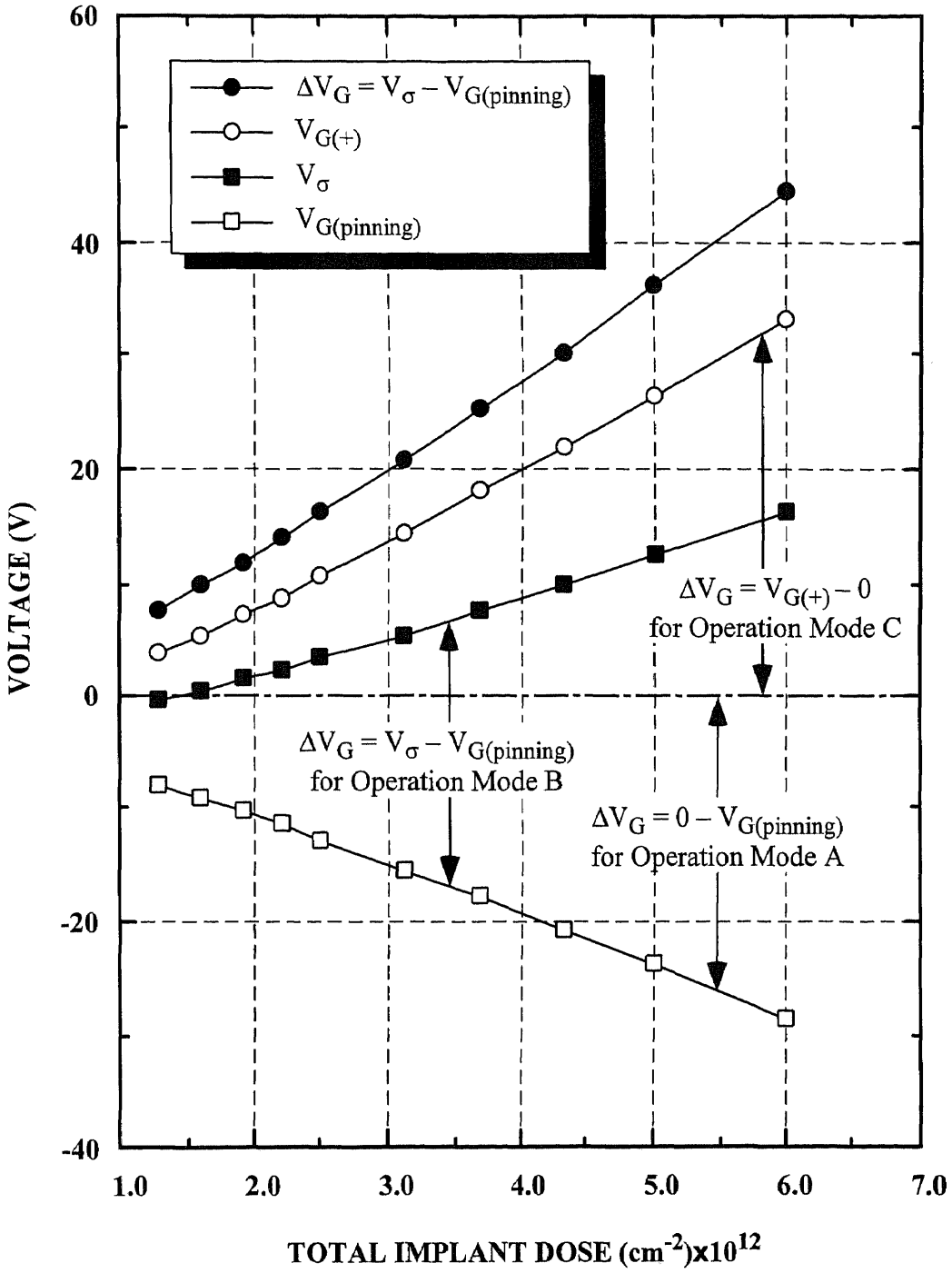


Figure 6.7 *Gate voltage swings, $\Delta V_G = 0 - V_{G(pinning)}$, $\Delta V_G = V_\sigma - V_{G(pinning)}$, and $\Delta V_G = V_{G(+)} - 0$, optimized gate voltage V_σ, positive gate voltage $V_{G(+)}$, and pinning gate voltage $V_{G(pinning)}$ as function of total dose for BCCD operations and implants described in Figure 6.6.*

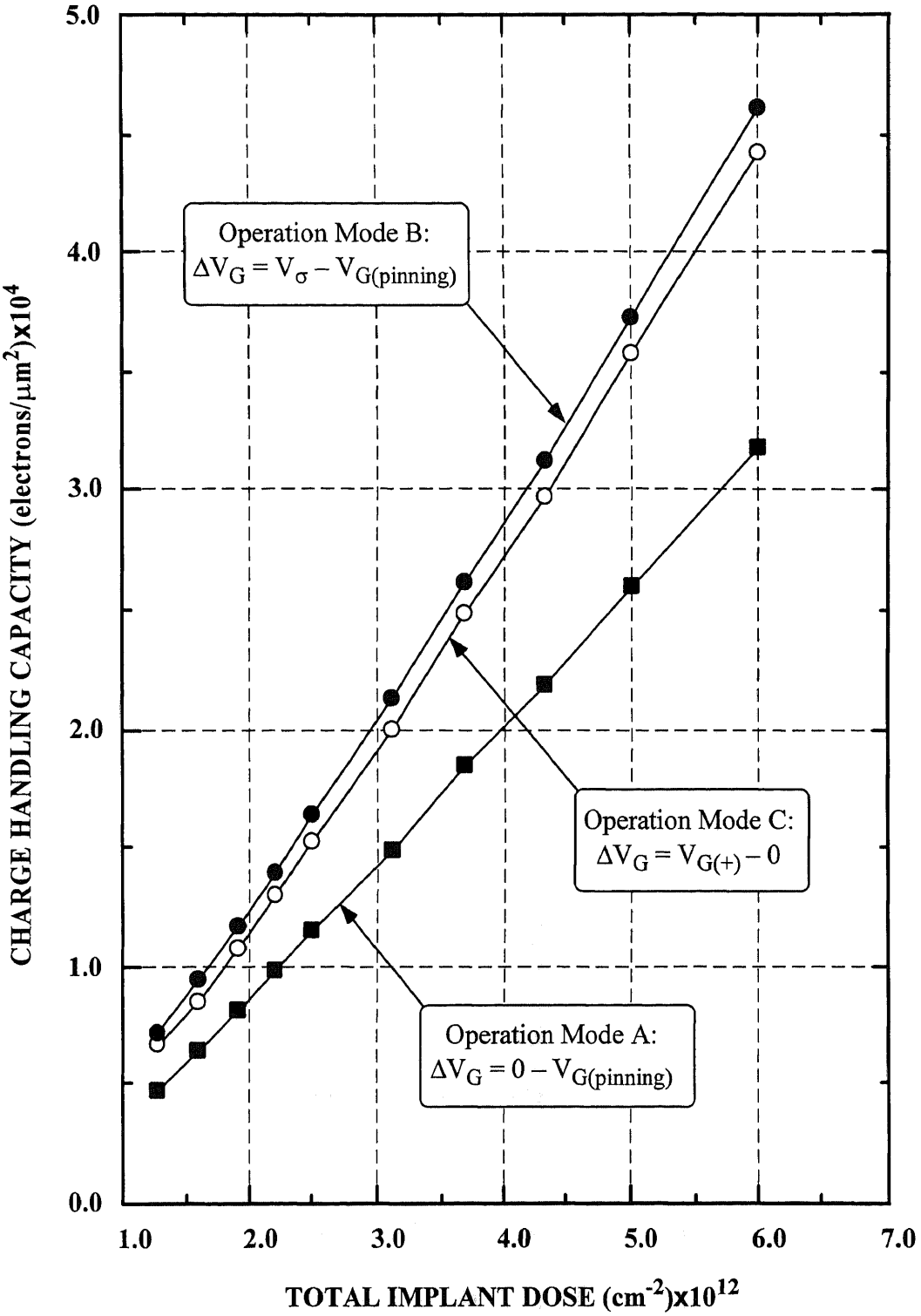


Figure 6.8 *Charge handling capacity as function of total implant dose (with P dose of $1.0x10^{12}$ cm^{-2}) for operation modes A, B, and C.*

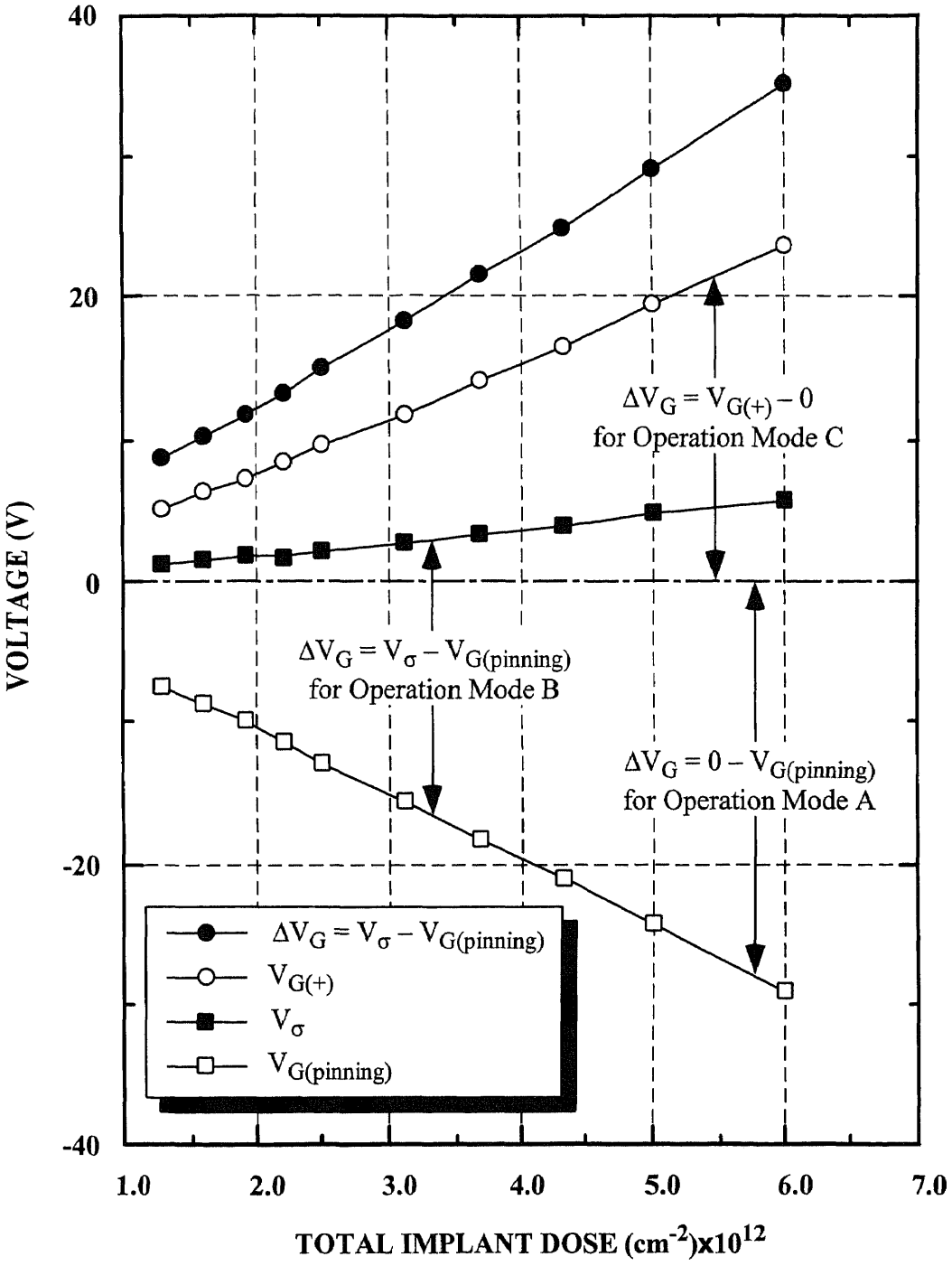


Figure 6.9 *Gate voltage swings, $\Delta V_G = 0 - V_{G(pinning)}$, $\Delta V_G = V_\sigma - V_{G(pinning)}$, and $\Delta V_G = V_{G(+)} - 0$, optimized gate voltage V_σ, positive gate voltage $V_{G(+)}$, and pinning gate voltage $V_{G(pinning)}$ as function of total dose for BCCD operations and implants described in Figure 6.8.*

Figure 6.10 shows the simulation results for the charge handling capacity of BCCD channel (with total BCCD implant dose of arsenic = $4.0x10^{12}$ cm^{-2}, and phosphorus = $1.0x10^{12}$ cm^{-2}) as function of effective channel oxide thickness for the operation modes A, B, and C, and Figure 6.11 shows the corresponding gate voltage swings. Inspection of Figure 6.10 shows that, as the effective channel oxide thickness is reduced from 700 Å to 100 Å, charge handling capacity of operation Mode A decreases from about 26,000 electrons/μm^2 to 5,000 electrons/μm^2, however, charge handling capacity of operation modes B and C remains almost unchanged. Inspection of Figure 6.11 shown that, gate voltage swing of the three operation modes is decreasing linearly with the reduction of the effective channel oxide thickness.

Comparison of simulation data in Figures 6.8 to 6.11 indicates that, for operation with a maximum gate voltage swing of 15 V, the following increases of charge handling capacity (CHC) can be achieved as the thickness of gate dielectric is reduced:

- For operation mode A, the CHC increases from 14,000 electrons/μm^2 to 17,000 electrons/μm^2 as the total BCCD implant dose is increased from $3.0x10^{12}$ cm^{-2} to $5.0x10^{12}$ cm^{-2} with the effective gate oxide thickness is reduced from 700Å to 400Å.
- In operation mode B, the CHC increases from 17,000 electrons/μm^2 to 38,000 electrons/μm^2 as the total BCCD implant dose is increased from $2.5x10^{12}$ cm^{-2} to $5.0x10^{12}$ cm^{-2} with the effective gate oxide thickness is reduced from 700Å to 200Å.
- In operation mode C, the CHC increases from 19,000 electrons/μm^2 to 37,000 electrons/μm^2 as the total BCCD implant dose is increased from $3.7x10^{12}$ cm^{-2} to $5.0x10^{12}$ cm^{-2} with the effective gate oxide thickness is reduced from 700Å to 400Å.

Therefore, it may be concluded that the operation mode C is most effective for achieving high charge handling capacity.

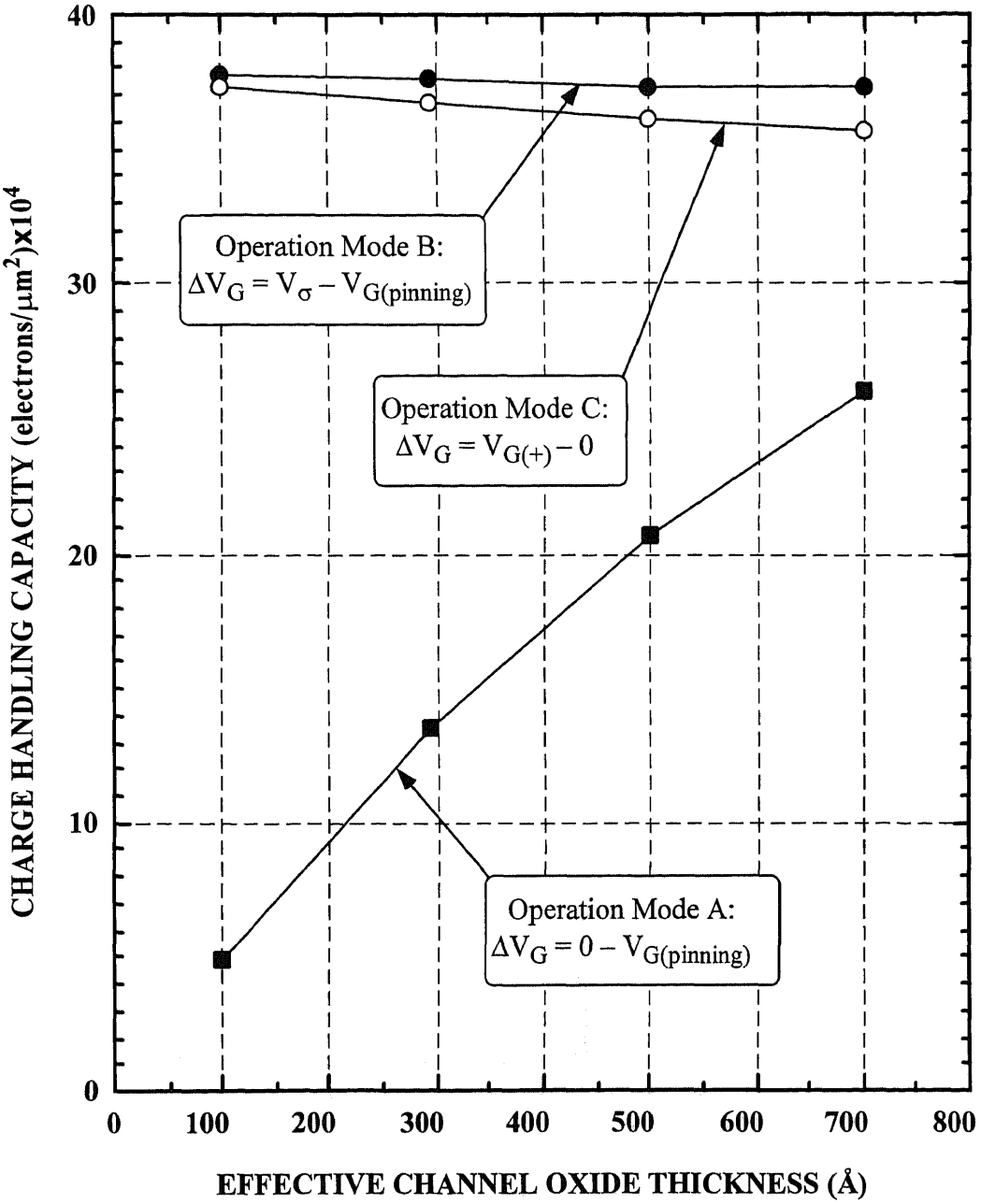
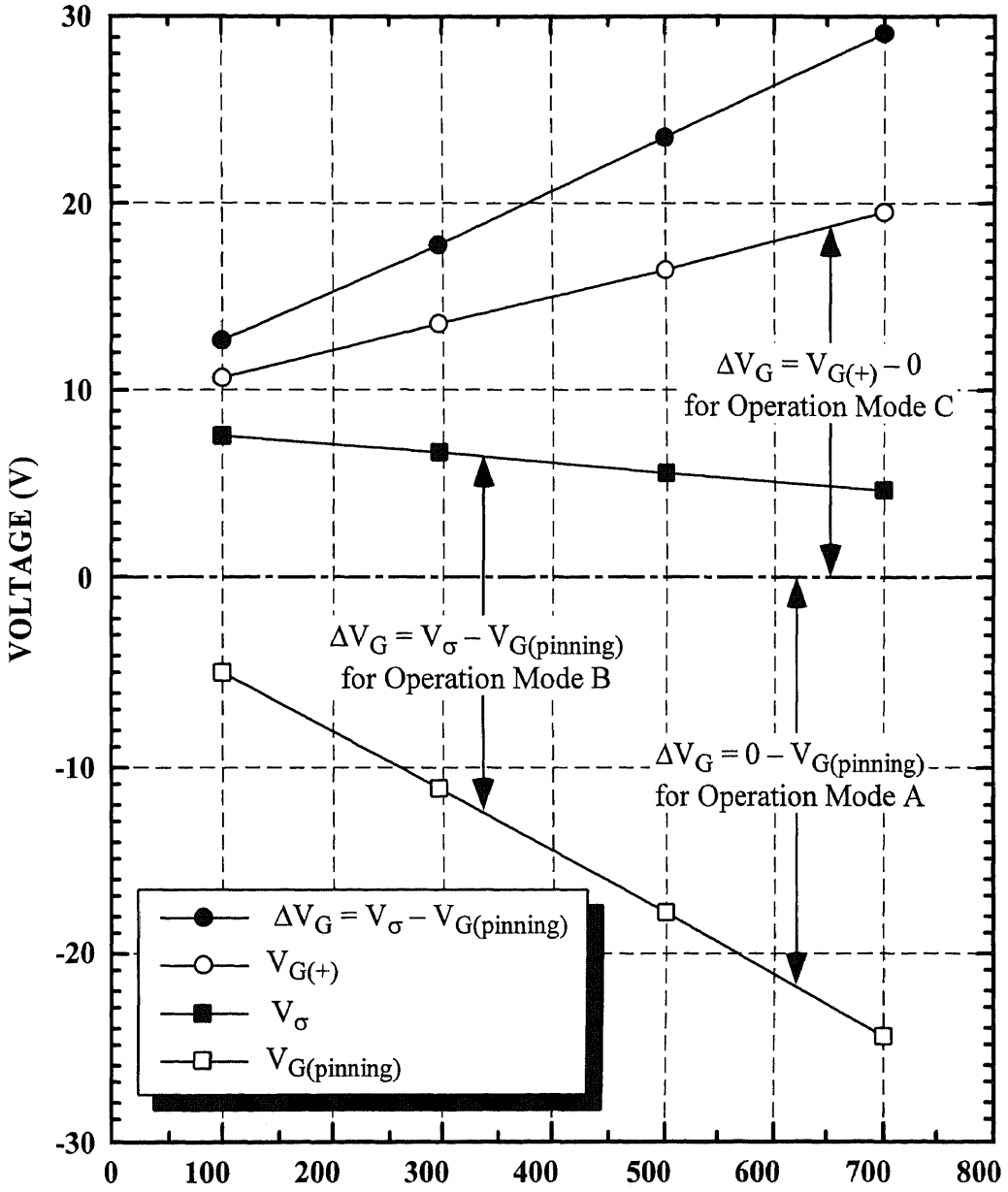


Figure 6.10 *Charge handling capacity of a fixed BCCD implant dose as function of effective channel oxide thickness for operation modes A, B, and C.*



(BCCD implant dose: Arsenic = 4.0×10^{12} cm^{-2},
Phosphorus = 1.0×10^{12} cm^{-2})

Figure 6.11 *Gate voltage swings, $\Delta V_G = 0 - V_{G(pinning)}$, $\Delta V_G = V_\sigma - V_{G(pinning)}$, and $\Delta V_G = V_{G(+)} - 0$, optimized gate voltage V_σ, positive gate voltage $V_{G(+)}$, and pinning gate voltage $V_{G(pinning)}$ as function of effective channel oxide thickness.*

Effect of The Ratio of As Implant Dose to P Implant Dose

The charge handling capacity of the three operation modes changes with the changing of the ratio of the arsenic implant dose to phosphorus implant dose. Optimization of the charge handling capacity in electrons/μm^2 as function of arsenic (x) and phosphorus (1-x) for total implant dose (1) of $1.3x10^{12}$ cm^{-2} is shown in Figure 6.12. Inspection of this figure shows that for operation in mode A the charge handling capacity increases with the increase of arsenic up to the dose of As = $8.5x10^{11}$ cm^{-2}. At this point, the condition of full well charge signal changes from being determined by PINNING (for 20 *kT/e* difference of the full well potential ϕ_{FULL} to the maximum pinning potential ϕ_{PIN} of the adjacent wells) to being determined by SURFACE (for 10 *kT/e* difference between the full well potential ϕ_{FULL} to the surface potential ϕ_{SURF}). Further increasing of arsenic results in reduction of charge handling capacity. However, operating in modes B and C results in increasing of charge handling capacity with the increasing of phosphorus.

Figure 6.13 shows the operating voltages for three operation modes and optimized gate voltage V_σ for operating mode B, as function of arsenic and phosphorus implant doses for a total implant dose of $1.3x10^{12}$ cm^{-2}. Inspection of this figure shows the following:

1. The pinning voltage is changed only from -7.2 V to -7.8 V as the arsenic implant dose changes from 0 to $1.\ 3x10^{12}$ cm^{-2}. Therefore, for operation mode A, the gate voltage swing, ΔV_G, is nearly a constant for different arsenic to phosphorus ratios.
2. For operating mode B, the optimized gate voltage $V_{G(B),Max} = V_\sigma$ is increased from about – 0.7 V to 2.1 V. And for operation in mode B, the gate voltage swing as well as the charge handling capacity increase with the increasing of phosphorus implant dose.

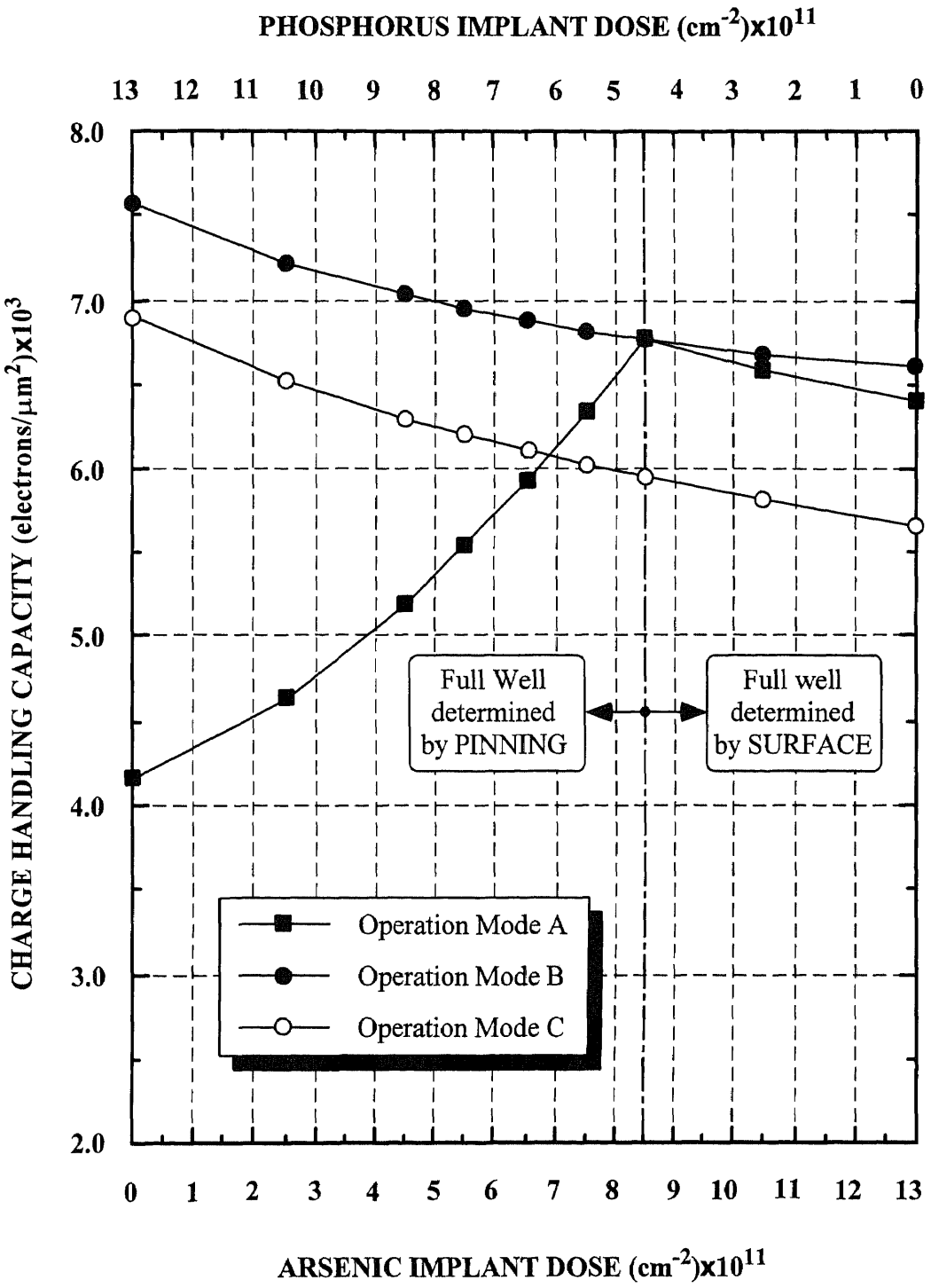


Figure 6.12 *Charge handling capacity of operation modes A, B, and C as function of arsenic and phosphorus implant doses for a total implant dose of* $1.3x10^{12}$ cm^{-2}.

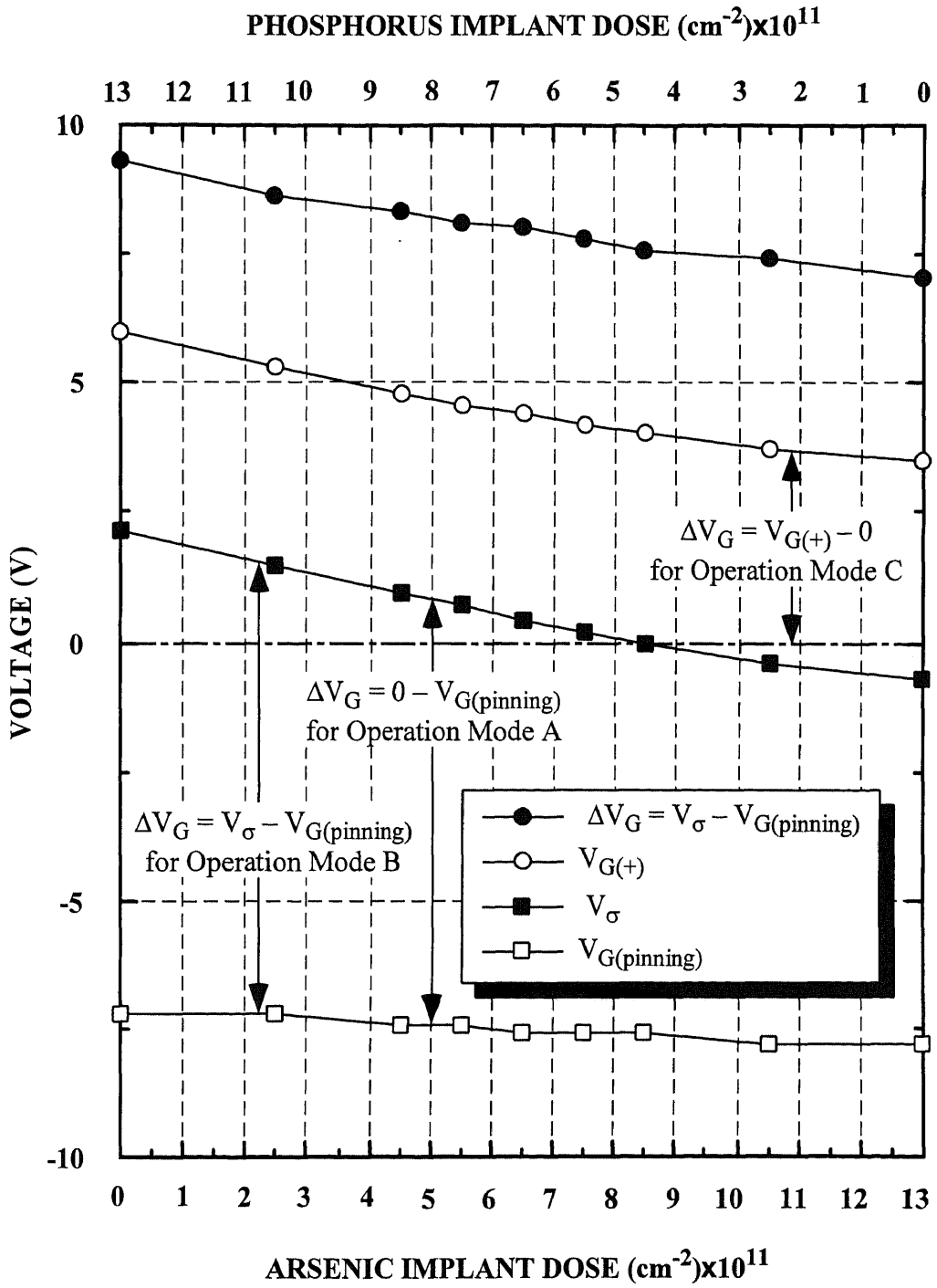


Figure 6.13 *Operating voltages for operation modes A, B, and C, and optimized gate voltage V_σ for operation mode B, as function of arsenic and phosphorus implant doses for a total implant dose of $1.3x10^{12}$ cm^{-2} described in Figure 6.12.*

3. The optimized gate voltage V_σ for operation in mode B changes from negative to positive as the condition of full well charge signal changes from being determined by PINNING to being determined by SURFACE. At the point that the arsenic implant dose equals to $8.5\text{x}10^{11}$ cm^{-2}, and $V_\sigma = 0$. In this case, the full well signal charge is determined by both of PINNING and SURFACE conditions.
4. For operation mode C, the gate voltage swing as well as the charge handling capacity increase with the increasing of phosphorus implant dose. For this case, the gate voltage swing is about 35 to 55% smaller than that for operation mode in B, however, as illustrated in Figure 6.13, the charge handling capacity for operation in mode C is only about 10 to 15% smaller than that of operation in mode B.

We have also simulated the charge handling capacity as a function of the ratio of arsenic implant dose to phosphorus dose in higher total implant doses. Figures 6.14 and 6.16 show the optimization of the charge handling capacity as function of arsenic (x) and phosphorus (1-x) for total implant dose (1) of $2.2\text{x}10^{12}$ cm^{-2} and $4.0\text{x}10^{12}$ cm^{-2}, respectively. Figures 6.15 and 6.17 show the operating voltages of the three operation modes and optimized gate voltage V_σ for operating mode B corresponding to the BCCD implants described in Figures 6.14 and 6.16, respectively.

Inspection of Figures 6.14 to 6.17 shows that, as the total BCCD implant dose increases to $2.2\text{x}10^{12}$ cm^{-2} and $4.0\text{x}10^{12}$ cm^{-2}, for operation in mode A, for the gate voltage swing kept nearly at a constant value for different arsenic to phosphorus ratios, the charge handling capacity increases with an increase of the arsenic implant dose. However, for operation modes B and C, the gate voltage swing as well as the charge handling capacity increase with the increasing of phosphorus implant dose. For the total BCCD implant dose of $2.2\text{x}10^{12}$ cm^{-2}, the gate voltage swing for operation in mode C is about 30 to 40% smaller than that of operation in mode B, however, the charge handling for operation in mode C is only about 5 to 10% smaller than that for operation in mode B. For the total BCCD implant dose of $4.0\text{x}10^{12}$ cm^{-2}, the gate voltage swing for operation

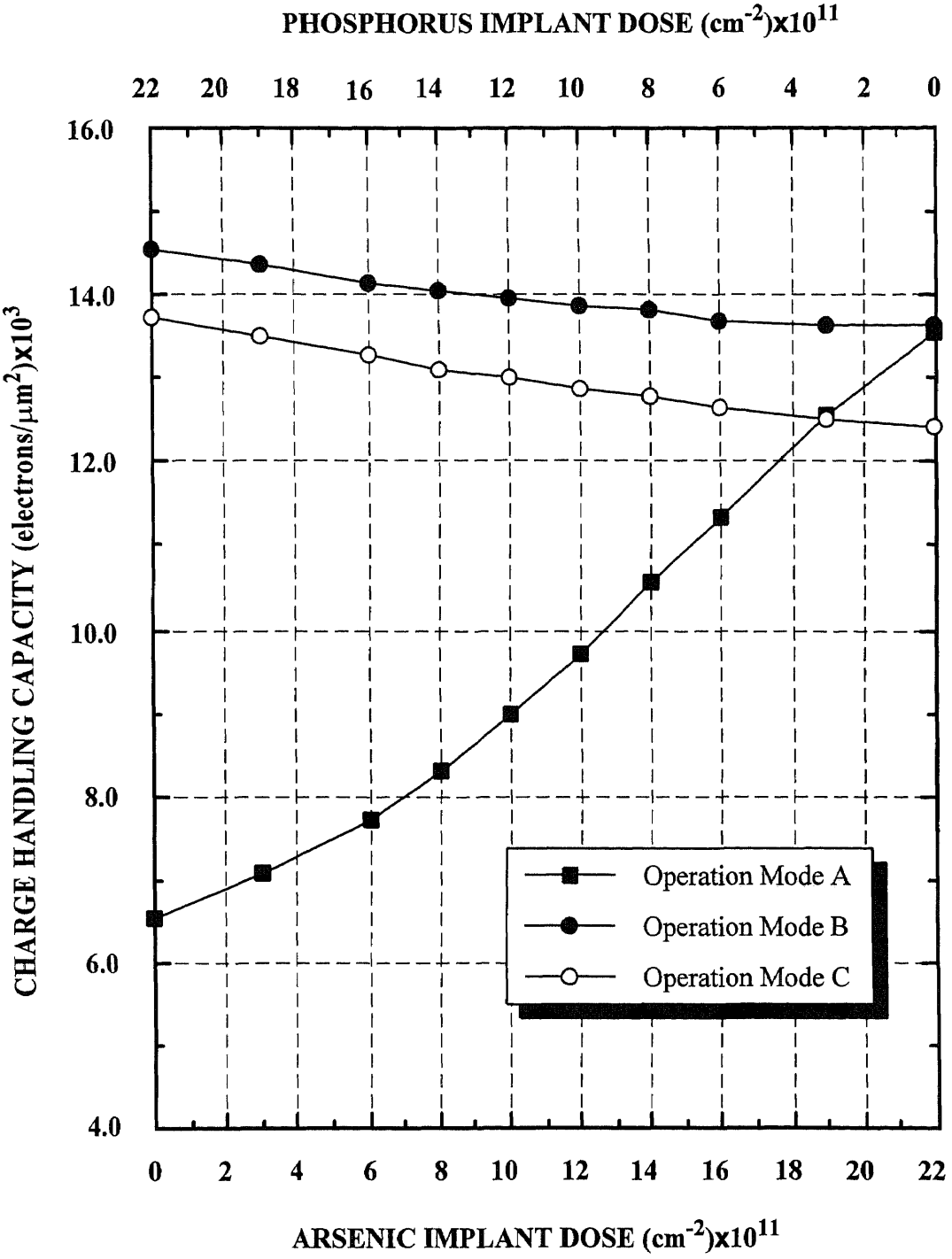


Figure 6.14 *Charge handling capacity of operation modes A, B, and C as function of arsenic and phosphorus implant doses for a total implant dose of* 2.2×10^{12} cm^{-2}.

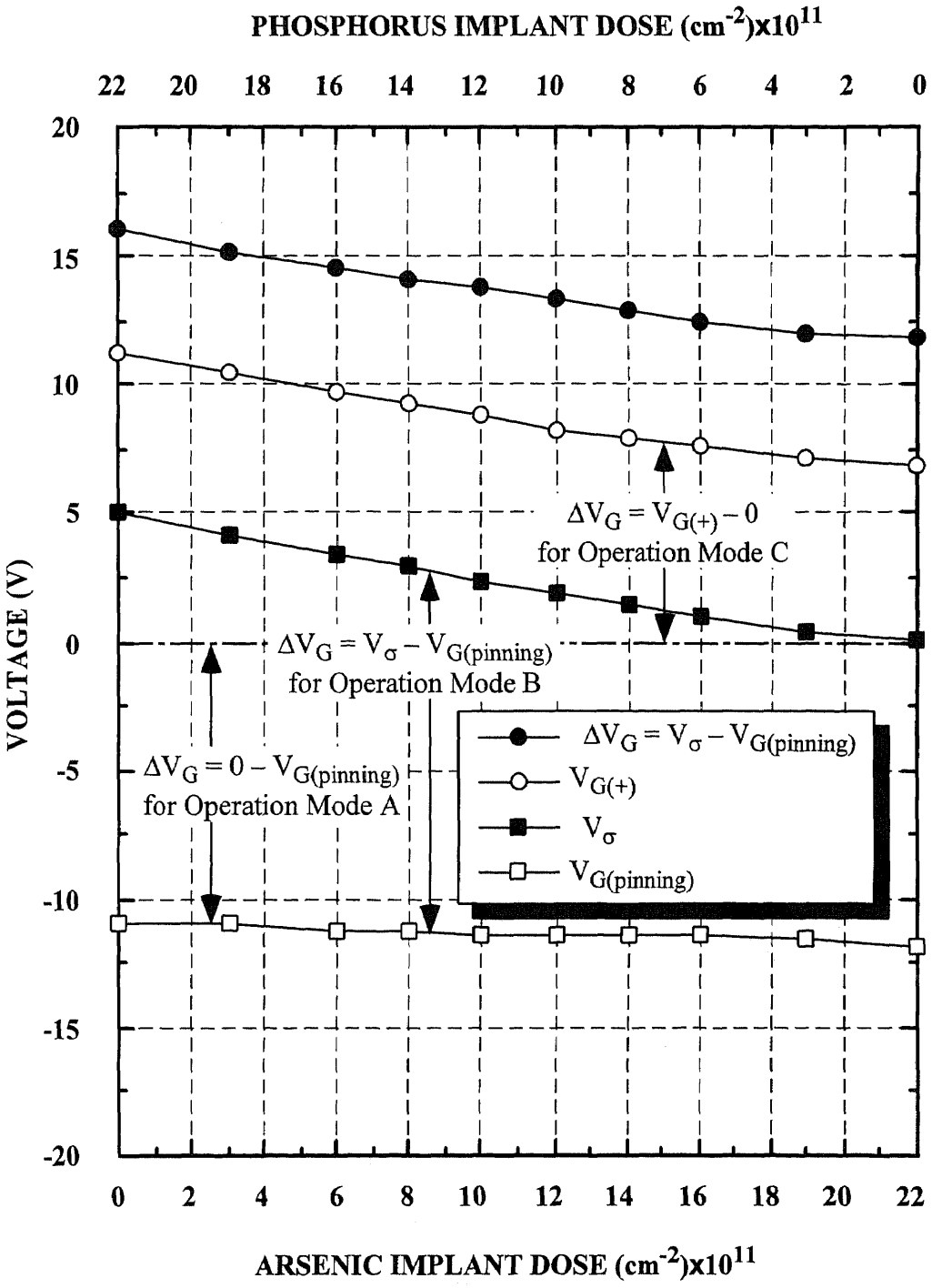


Figure 6.15 *Operating voltages for operation modes A, B, and C, and optimized gate voltage V_σ for operation mode B, as function of arsenic and phosphorus implant doses for a total implant dose of $2.2x10^{12}$ cm^{-2} described in Figure 6.14.*

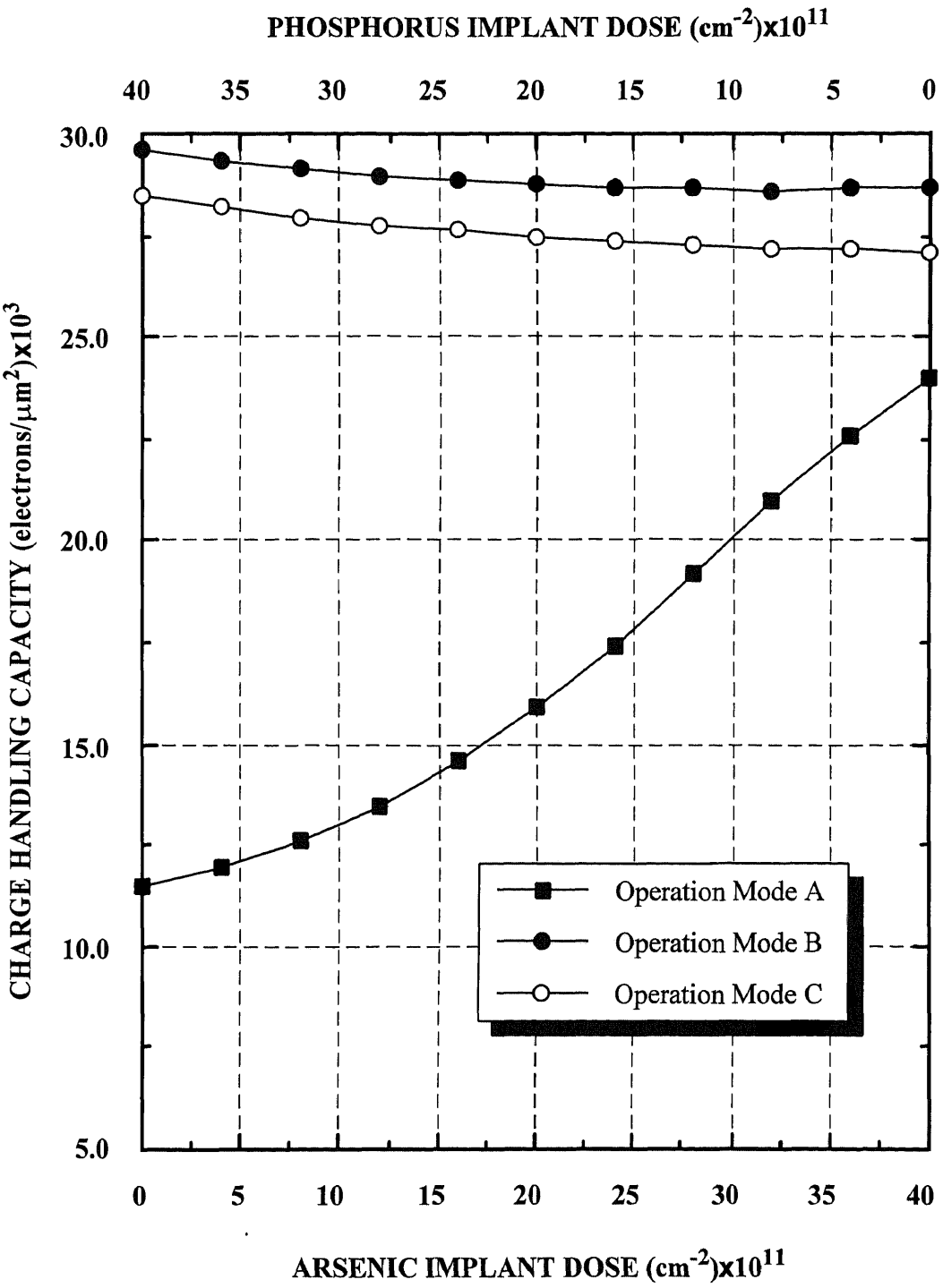


Figure 6.16 *Charge handling capacity of operation modes A, B, and C as function of arsenic and phosphorus implant doses for a total implant dose of 4.0x10^{12} cm^{-2}.*

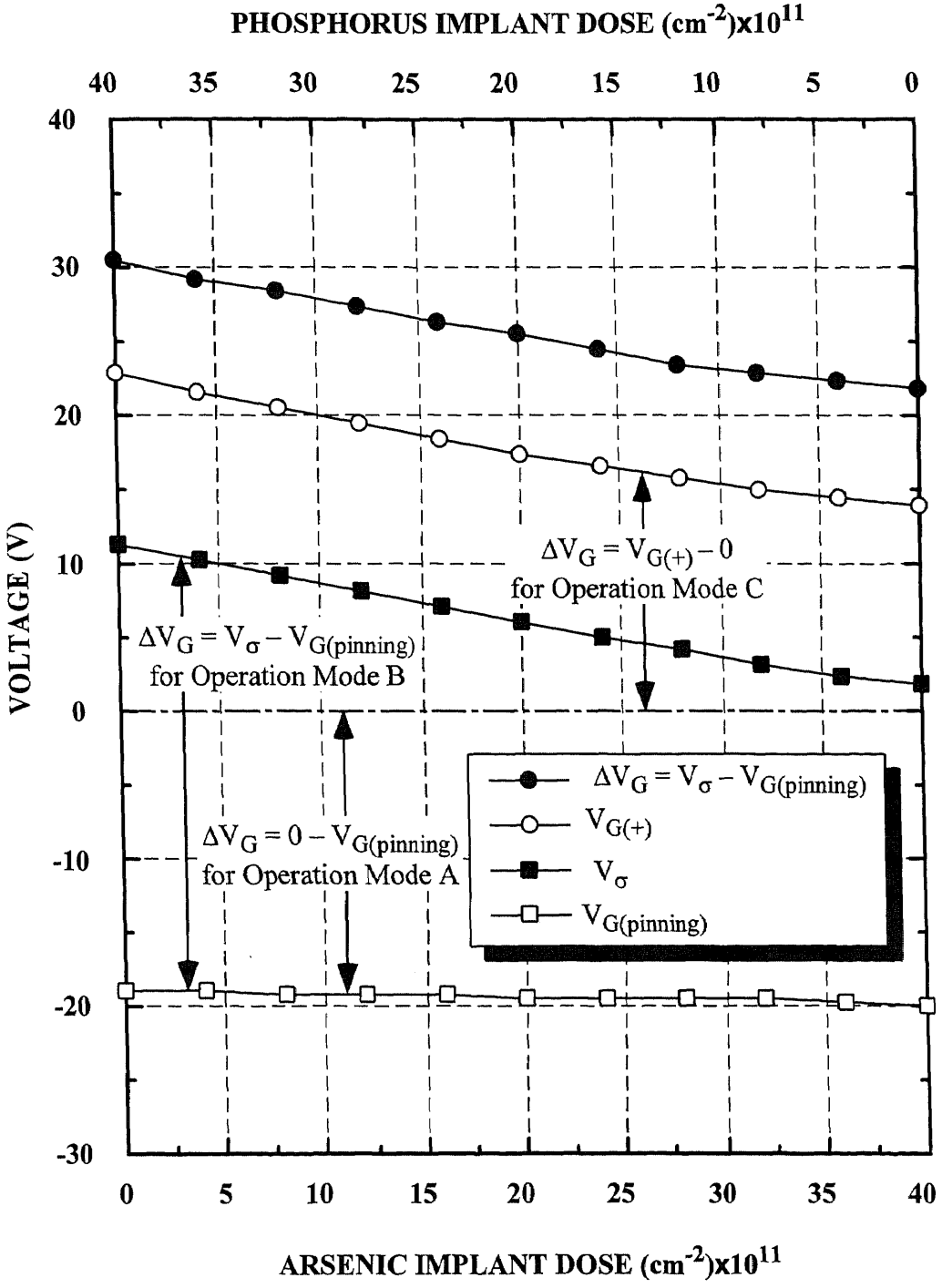


Figure 6.17 *Operating voltages for operation modes A, B, and C, and optimized gate voltage V_σ for operation mode B, as function of arsenic and phosphorus implant doses for a total implant dose of $4.0x10^{12}$ cm^{-2} described in Figure 6.16.*

in mode C is about 25 to 35% smaller than that for operation in mode B, however, the charge handling for operation in mode C is only about 4 to 5% smaller than that for operation in mode B.

6.4.3 Analytical Approximation for Charge Handling Capacity vs Gate Voltage Swing and BCCD Implant dose

As illustrated in Figures 6.14 and 6.16, as the total BCCD implant dose greater than $2.2\text{x}10^{12}$ cm^{-2}, the charge handling capacity for operation modes B and C increases with the increasing of the P implant dose for a fixed total implant dose, and simultaneously, the operating gate voltage also increases. However, the charge handling capacity of operation mode A decreases with an increase of the P implant dose for a fixed total implant dose and the operating gate voltage swing is nearly a constant. Therefore, it is interesting to examine how the charge handling capacity and the gate voltage swing vary with the BCCD implant dose.

From Figures 6.6 and 6.8, we can see that for the total implant does greater than $2.2\text{x}10^{12}$ cm^{-2} (in this case, the P implant dose is greater than the fixed As implant dose described in Figure 6.6, and As implant dose is greater than the fixed P implant dose described in Figure 6.8), the variation of the charge handling capacity of the three operation modes with the total implant dose can be considered as a linear function. Thus, the relation between the charge handling capacity CHC and the total implant dose N_{TOT} can be written as:

$$CHC = A_{CN} \cdot N_{TOT} + B_{CN}, \qquad (N_{TOT} \geq 2.2\times10^{12}\ \text{cm}^{-2}). \tag{6.3}$$

where, A_{CN} and B_{CN} are constants which can be estimated from Figures 6.6 and 6.8. Table 6.1 gives the constants A_{CN} and B_{CN} of the three operation modes for fixed As implant dose and fixed P implant dose.

Inspection of Figures 6.7 and 6.9 shows that, the operating gate voltage swing of the three operation modes is also a linear function for the total implant dose, as the total

implant dose greater than $2.2\text{x}10^{12}$ cm^{-2}. The relation between the gate voltage swing ΔV_G and the total implant dose N_{TOT} can be written as:

$$\Delta V_G = A_{VN} \cdot N_{TOT} + B_{VN}, \qquad (N_{TOT} \geq 2.2 \times 10^{12}\ \text{cm}^{-2}). \tag{6.4}$$

where A_{VN} and B_{VN} are constants which can be estimated from Figures 6.7 and 6.9. Table 6.2 gives the constants A_{VN} and B_{VN} of the three operation modes for fixed As implant dose and fixed P implant dose.

Table 6.1 *Linear constants for the relation between charge handling capacity and total implant dose of three operation modes.*

	Fixed As Implant Dose of $1.0\text{x}10^{12}$ cm^{-2}		**Fixed P Implant Dose of $1.0\text{x}10^{12}$ cm^{-2}**	
	A_{CN}	B_{CN} (μm^{-2})	A_{CN}	B_{CN} (μm^{-2})
Operation Mode A	0.2419	3649.1	0.5796	-3027.2
Operation Mode B	0.8387	-4331.4	0.8233	-3837.8
Operation Mode C	0.8275	-5019.7	0.8061	-4644.5

Table 6.2 *Linear constants for the relation between gate voltage swing and total implant dose of the three operation modes.*

	Fixed As Implant Dose of $1.0\text{x}10^{12}$ cm^{-2}		**Fixed As Implant Dose of $1.0\text{x}10^{12}$ cm^{-2}**	
	A_{VN} (10^{-12} $V \cdot cm^2$)	B_{VN} (V)	A_{VN} (10^{-12} $V \cdot cm^2$)	B_{VN} (V)
Operation Mode A	4.4878	1.6732	4.5955	1.4270
Operation Mode B	7.9700	-3.7400	5.7197	1.7366
Operation Mode C	6.4857	-5.6143	3.9643	-0.3214

From Equations (6.3) and (6.4), the variation of charge handling capacity with gate voltage swing can be approximated as a linear function for the total implant dose greater than $2.2\text{x}10^{12}$ cm^{-2}. The linear relation between the charge handling capacity and the gate voltage swing can be written as:

$$CHC = A_{CV} \cdot \Delta V_G + B_{CV}, \qquad (N_{TOT} \geq 2.2 \times 10^{12}\ \text{cm}^{-2}), \tag{6.5}$$

with the constants $A_{CV} = A_{CN}/A_{VN}$, and $B_{CV} = B_{CN} - (A_{CN}/A_{VN}) \cdot B_{VN}$. The calculated constants A_{CV} and B_{CV} are given in Table 6.3.

From Equation (6.5) and the data given in Table 6.3, the charge handling capacity variation with the gate voltage swing for operation modes A, B, and C are given in Figures 6.18, 6.19, and 6.20, respectively. Inspection of Figures 6.18, 6.19, 6.20 shows that, when the total implant dose is greater than $2.2\text{x}10^{12}$ cm^{-2}, with a fixed gate voltage swing, the charge handling capacity of fixed phosphorus implant dose of $1.0\text{x}10^{12}$ cm^{-2} is greater than that of fixed arsenic implant dose of $1.0\text{x}10^{12}$ cm^{-2} for all of the three operation modes. This is expected since arsenic implant is located closer to the interface of Si/SiO_2 and for the same implant dose requires less gate voltage swing than phosphorus implant.

Table 6.3 *Linear constants for the relation between charge handling capacity and gate voltage swing of three operation modes.*

	Fixed As Implant Dose of $1.0\text{x}10^{12}$ cm^{-2}		**Fixed P Implant Dose of $1.0\text{x}10^{12}$ cm^{-2}**	
	A_{CV} $(V^{-1} \cdot \mu m^{-2})$	B_{CV} (μm^{-2})	A_{CV} $(V^{-1} \cdot \mu m^{-2})$	B_{CV} (μm^{-2})
Operation Mode A	539.0	2747.2	1261.2	-4827.0
Operation Mode B	1053.6	-394.0	1437.7	-4896.8
Operation Mode C	1275.9	2143.5	2033.4	-3991.0

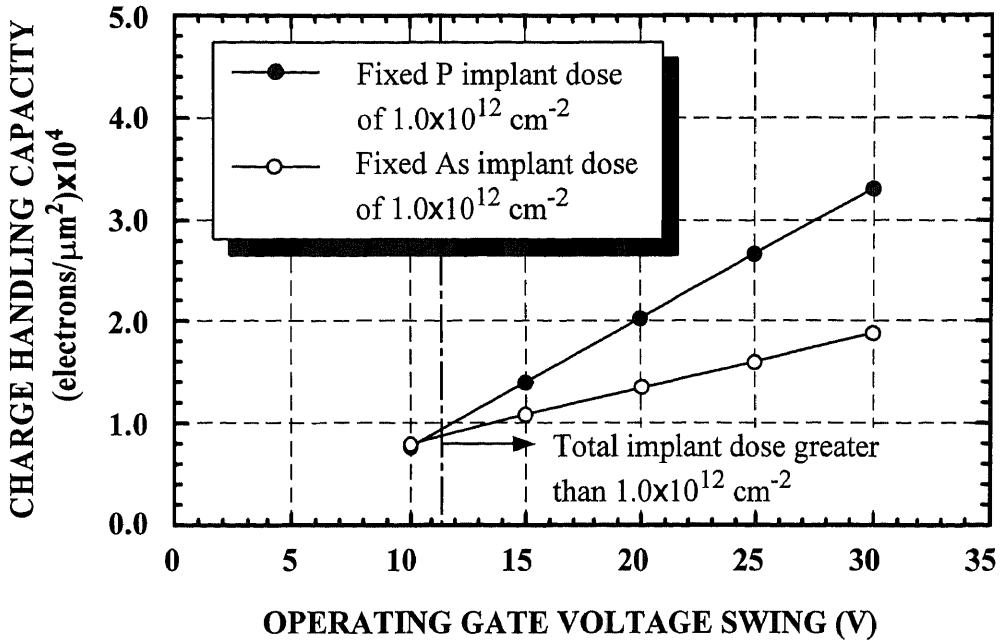


Figure 6.18 *Charge handling capacity as function of gate voltage swing for operation mode A.*

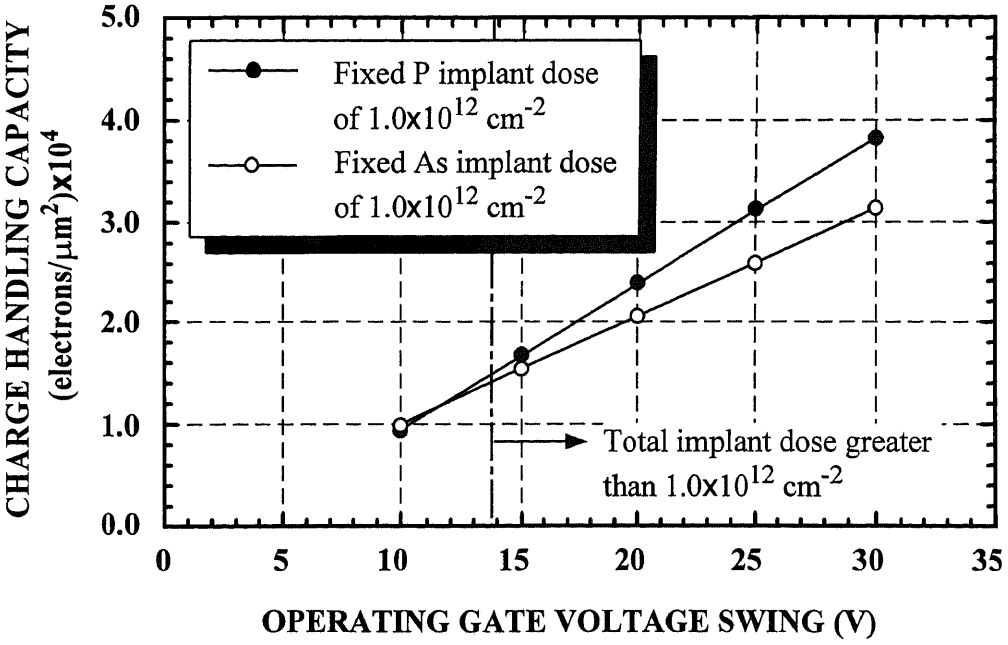


Figure 6.19 *Charge handling capacity as function of gate voltage swing for operation mode B.*

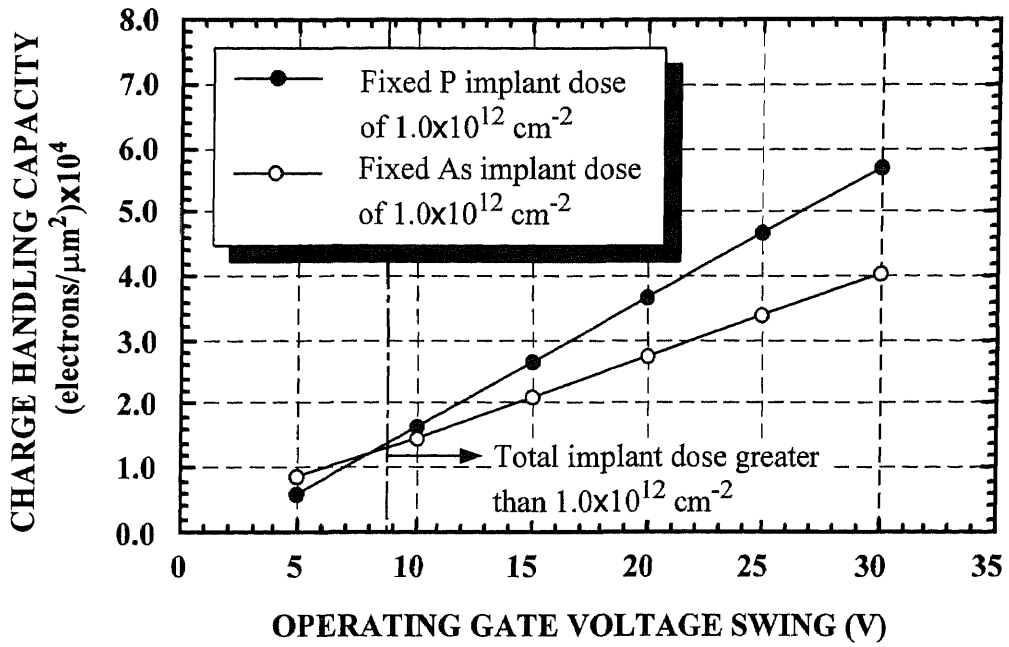


Figure 6.20 *Charge handling capacity as function of gate voltage swing for operation mode C.*

6.4.4 Electric Breakdown Voltage

The maximum allowed N-type doping of the BCCD channel is expected to be limited by the electric breakdown of the silicon [67], [80], [89]. According to the 1-D simulation, the maximum electric field occurs at the Si/SiO_2 interface. The calculated maximum electric field at the Si/SiO_2 interface for the three operating modes as function of total implant dose for a fixed As implant dose of $1.0x10^{12}$ cm^{-2} and a fixed P implant dose of $1.0x10^{12}$ cm^{-2} are shown in Figures 6.21 and 6.22, respectively. For lower dope silicon, the critical electric field strength, E_{BR}, is approximately $3.0x10^5$ V/cm [67], [80]. The simulation result shows that the ratio of As implant dose to P implant dose does not affect the electric field strength at the Si/SiO_2 interface. Inspection of Figures 6.21 and 6.22 shows that for E_{BR} = $3.0x10^5$ V/cm, the maximum allowed BCCD implant dose is approximately $2.2x10^{12}$ cm^{-2} for operation modes A and B, and $2.4x10^{12}$ cm^{-2} for operation mode C. However, published values of BCCD charge handling capacity imply

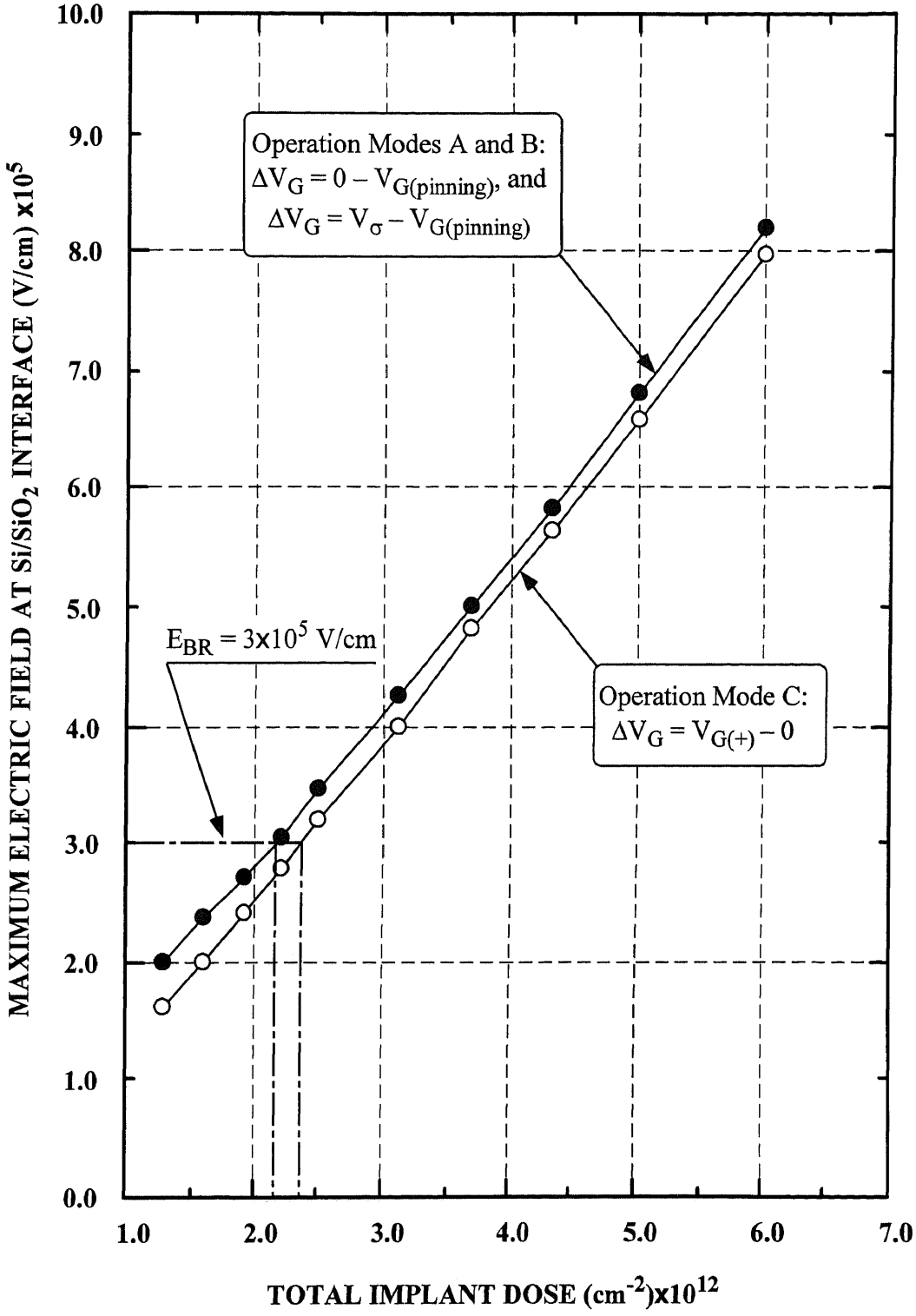


Figure 6.21 *Maximum electric field at the Si/SiO_2 interface as function of total dose for BCCD operations and implants described in Figure 6.6.*

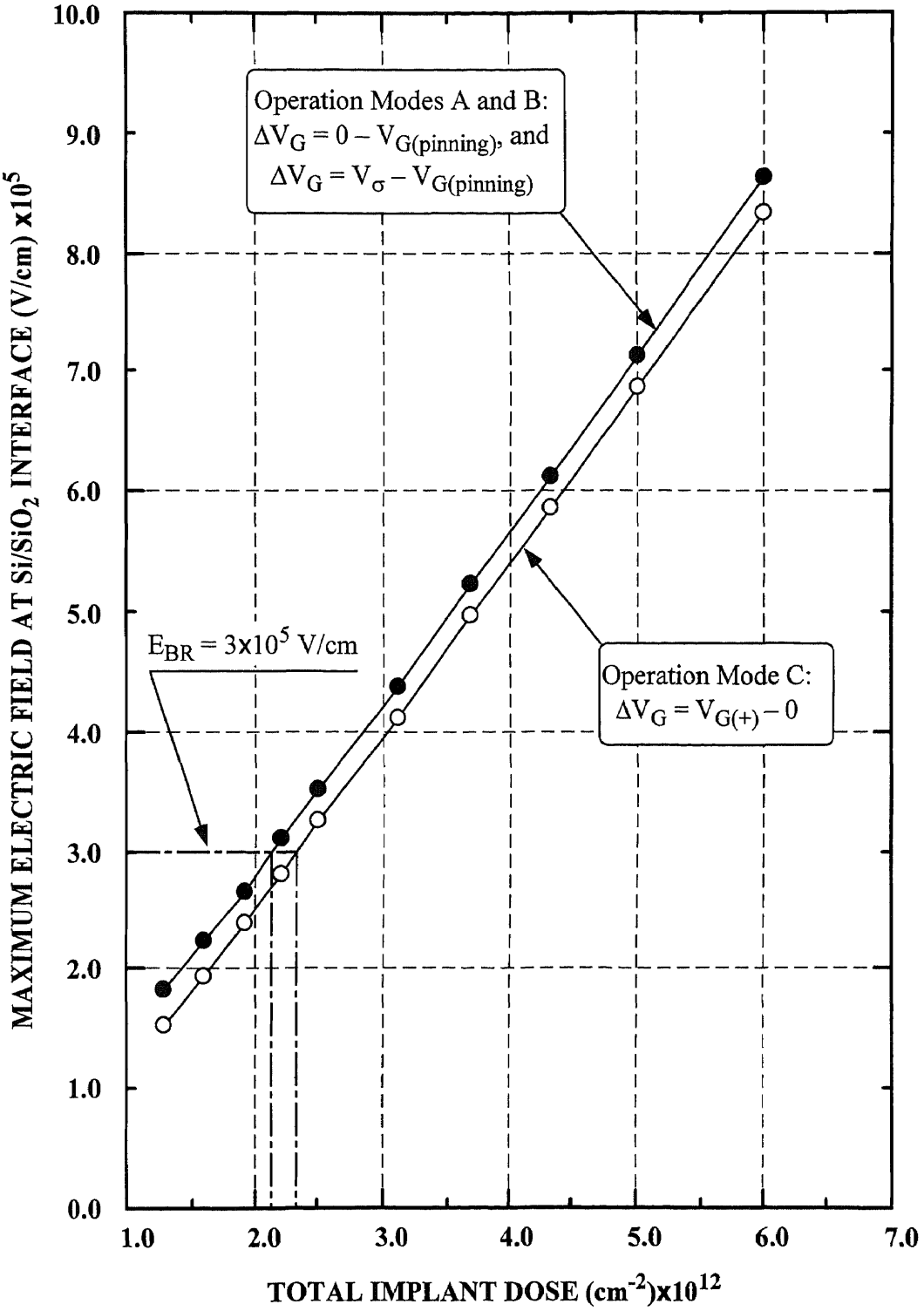


Figure 6.22 *Maximum electric field at the Si/SiO_2 interface as function of total dose for BCCD operations and implants described in Figure 6.8.*

that considerably higher electric field can be tolerated at Si/SiO_2 interface of highly doped BCCDs.

Normally, the critical field strength of $3.0x10^5$ V/cm is applicable to the breakdown caused by the avalanche multiplication process in a p-n junction with moderate dopings, such as a p^+-n one-sided abrupt junction with a doping concentration of $N_D \approx 10^{17}$ cm^{-3} or less under revered bias [67]. However, in the case of BCCD, there is no charge source at the Si/SiO_2 interface to cause the required avalanche multiplication process. Thus, the value of the critical field strength at the Si/SiO_2 interface of BCCD could be higher. However, we should also consider the lateral electric breakdown as a large voltage difference is applied to the adjacent gates.

The simulation result shows that the ratio of As implant dose to P implant dose does not affect the electric field strength in gate dielectric layer. In SiO_2 and Si_3N_4, the critical strength is depended on the quality of the material as well as its thickness. For thin oxide and nitride layer, the dielectric strength is approximately 10^7 V/cm [80], [89]. Our simulation showed that, the maximum electric field in SiO_2 and Si_3N_4 are lower than $2.5x10^6$ V/cm as the total implant dose reaches $6.0x10^{12}$ cm^{-2}.

6.4.5 Summary

According the three operation modes are defined in Section 6.3, the full well signal of operation modes A and B is determined by Equation (6.1), and the full well signal of operation mode C is determined by Equation (6.2). 1-D simulation shows that the charge handling capacity of the BCCD channel is determined by the total implant dose, the ratio of As implant dose to P implant dose, and the gate voltage swing associated with operating modes presented. In conclusion, 1-D simulation of the BCCD charge handling capacity gives the following results:

- The charge handling capacity for the three operation modes increases with the increase of total BCCD implant dose.

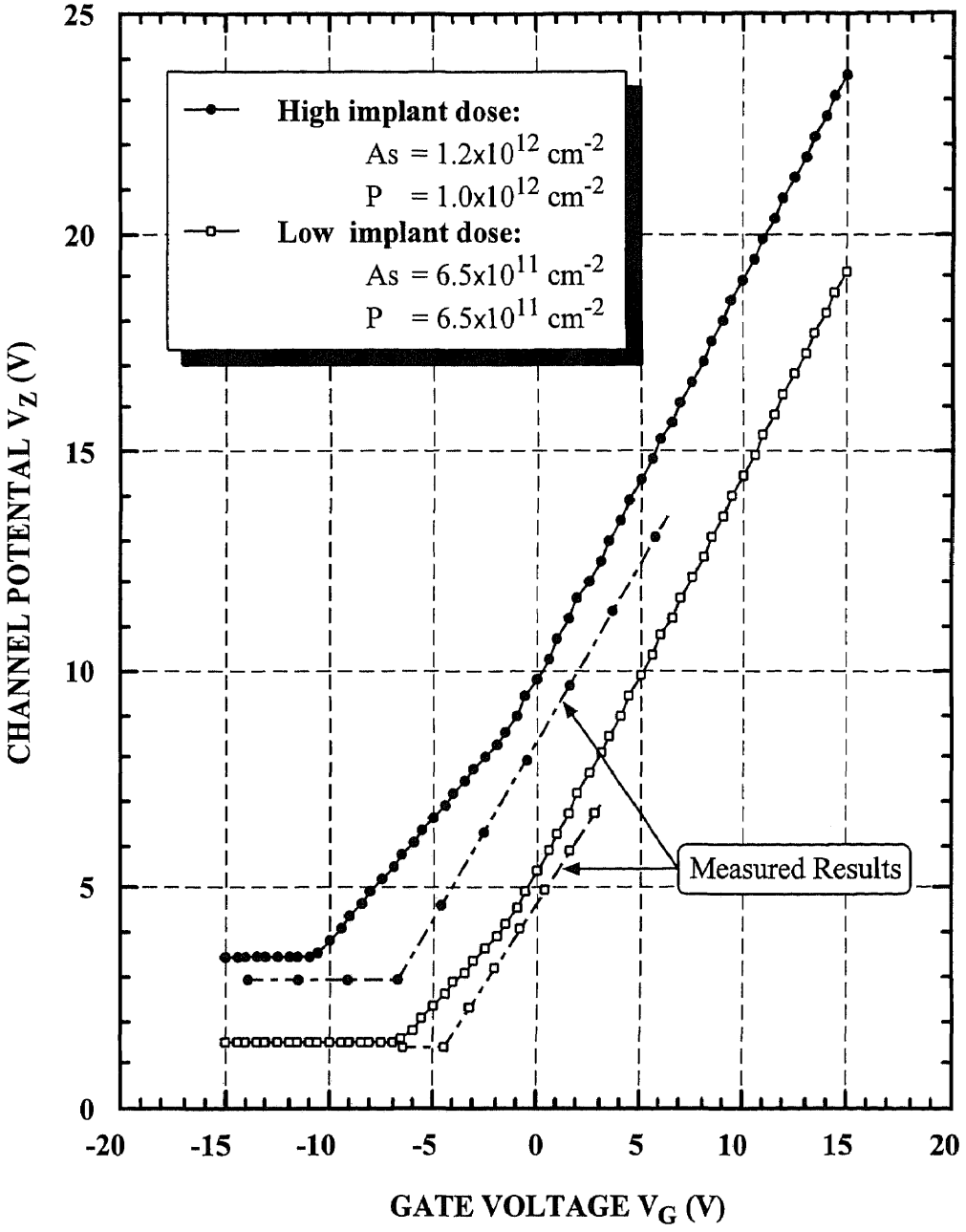
- The large gate voltage swing for all of the three operating modes associated with the high BCCD implant dose can be reduced for practical CCD operation by using a thin channel dielectric layer. The charge handling capacity for operation modes B and C remains almost unchanged as the thickness of channel dielectric layer reduced. However, the charge handling capacity for operation mode A is decreasing with the reducing of the thickness of channel dielectric layer.
- At a low total BCCD implant dose, such as 1.3×10^{12} cm^{-2}, for operation mode A, the charge handling capacity increases with the increasing of As implant dose, until the condition of full well charge signal changes from being determined by PINNING (the difference between the full well potential ϕ_{FULL} to the maximum pinning potential ϕ_{PIN} of the adjacent wells is 20 *kT/e*) to being determined by SURFACE (the difference between the full well potential ϕ_{FULL} to the surface potential ϕ_{SURF} is 10 *kT/e*). Further increasing of As implant dose results in reduction of charge handling capacity.
- At a high total BCCD implant dose (total implant greater than 2.2×10^{12} cm^{-2}), the full well charge signal is always determined by PINNING condition, and the charge handling capacity of operation mode A increases with the increasing of As implant.
- In general, for any As and P implant dose, the maximum charge handling capacity can be obtained by operating the BCCD in mode B, while operation in mode A results in the lowest charge handling capacity.
- Gate voltage swing of operation mode A, $\Delta V_G = 0 - V_{G(pinning)}$, is nearly a constant value only for a fixed value of total implant dose. However, the gate voltage swing of operation modes B and C increases with the decreasing of the ratio of As implant dose to P implant dose.
- Operation mode C has charge handling capacity only about 5 to 10% smaller than that of operation mode B, but it requires about 25 to 55% smaller gate voltage than operation mode B.

- The increasing of the ratio of As implant dose to P implant dose will increase the BCCD channel capacity. However, the gate voltage swing of operation modes B and C decreases with the increasing of the ratio of As implant dose to P implant dose. The increasing of the charge handling capacity with the increase of the P implant dose in operation modes B and C requires an increase of the gate voltage swing. However, for a fixed gate voltage swing, the charge handling capacity in all of the three operation modes will increase with the increasing of As implant dose.
- The maximum allowed As and P implant doses are limited by the electric breakdown of the silicon and the maximum gate voltage swing which is practical for the CCD imager operation.
- The maximum charge handling capacity of the BCCD channel is determined by the maximum allowed As and P implant doses, the maximum gate voltage swing, and the operation modes.

6.5 BCCD Channel Potential as Function of Gate Voltage

6.5.1 Simulation Results

BCCD channel potential as function of applied gate voltage were simulated by 1-D simulation for both lower BCCD implant dose (with both arsenic and phosphorus implant doses of 6.5×10^{11} cm^{-2}) and higher BCCD implant dose (with arsenic implant dose of 1.2×10^{12} cm^{-2} and phosphorus implant dose of 1.0×10^{12} cm^{-2}) options. Figure 6.23 illustrated the simulated BCCD channel voltage as function of applied gate voltage. Inspection of this figure shows that, the BCCD pinning gate voltage is about -7.0 V and the BCCD pinning channel potential is about 1.5 V for the lower BCCD implant dose option, and the BCCD pinning gate voltage is about -11.0 V and the BCCD pinning channel potential is about 3.5 V for the higher BCCD implant dose option. For comparison, the measured results are also illustrated by dash-line in Figure 6.23.



(Gate dielectric layer: 350 Å of silicon-dioxide, and
650 Å of silicon-nitride)

Figure 6.23 *Simulated result of variation of BCCD channel potential with applied gate voltage for two BCCD implant options.*

6.5.2 Test Results

The measured BCCD channel potential as function of applied gate voltage was obtained by measurements of the BCCD test device structures fabricated on the imager chip. The experimental test set-up is illustrated in Figure 6.24. As shown in this figure, the test BCCD device is constructed as a MOSFET with a BCCD channel having a gate length of 10 μm and a gate width of 20 μm. The drain of the BCCD MOSFET is biased at +20 V and a large load resistance (R_S = 10 MΩ) is connected to the source. By applying a sinusoidal voltage (V_G) to the gate, measurement of the source voltage, (V_S), for $I_S \cong 0$ gives a plot of channel potential ,ϕ_{CH}, as function of V_G, where $\phi_{CH} = V_S$.

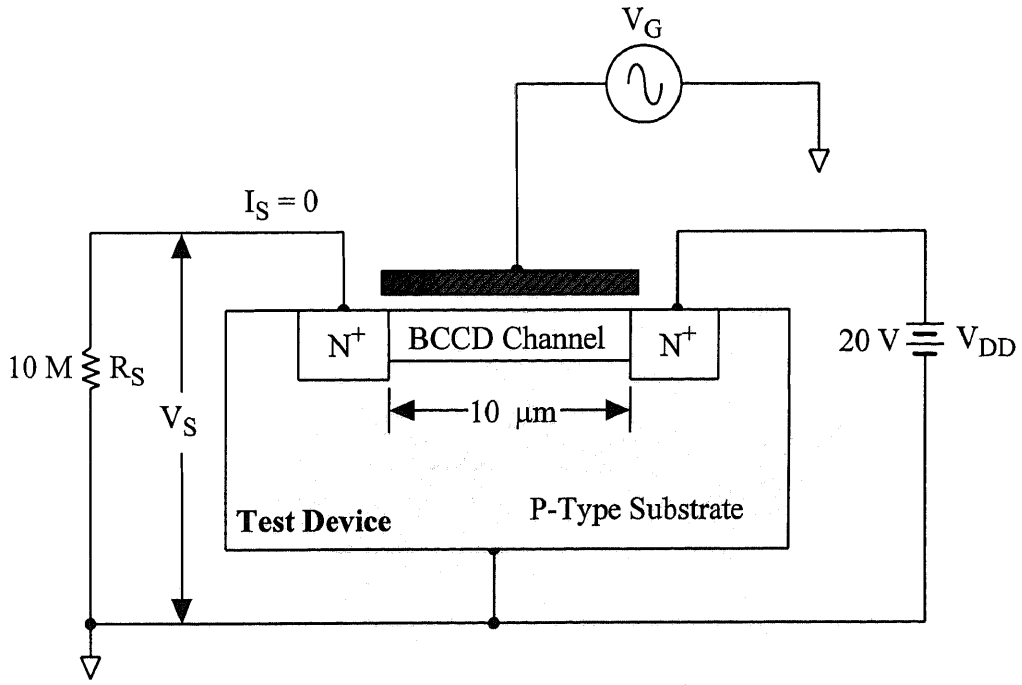


Figure 6.24 *Experimental set-up for measuring the BCCD channel potential varies with the applied gate voltage.*

During the imager chip fabrication, part of the silicon-nitride of the channel dielectric layer was etched during the process of polysilicon etching. Therefore, only the channel dielectric layer of BCCD poly-1 gate contains 350 Å of SiO_2 and 650 Å of Si_3N_4

which was used in simulations. The comparison of the simulation results with the tested results of the BCCD channel potential under poly-1 gate as function of the applied gate voltage for low BCCD implant dose option is shown in Figure 6.25 and for high BCCD implant dose option is shown in Figure 6.26.

Inspection of Figure 6.25 shows that, for lower BCCD implant dose, the pinning gate voltage is about -4.5 V and the corresponding BCCD channel voltage is about 1.45 V. Inspection of Figure 6.26 shows that, for higher BCCD implant dose, the pinning gate voltage is about -6.8 V and the corresponding BCCD channel voltage is about 3.0 V. Comparing with the simulation results described before, the measured value of the pinning gate voltage is about 35% less than that of simulation result, and the corresponding BCCD channel voltage is about 10% less than that of simulation result. The difference between above measured and simulated values may be affiliated to inaccuracy of implant doses and default simulation process parameters.

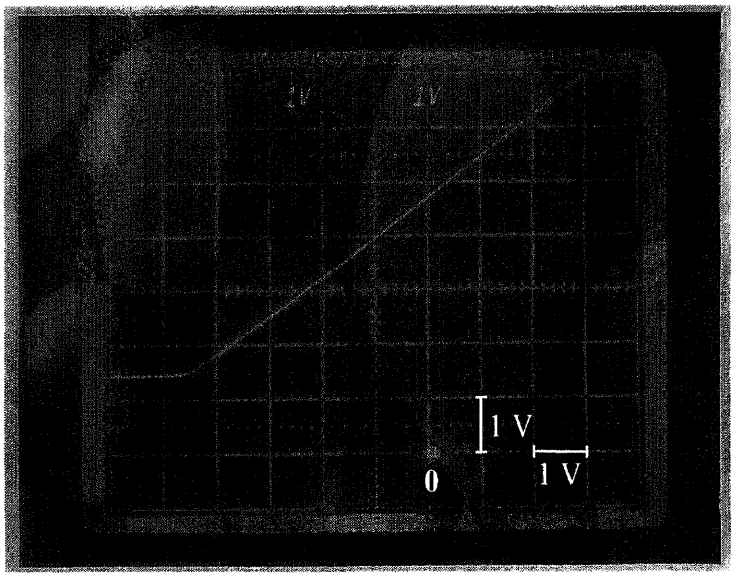


Figure 6.25 *Tested result of channel potential under poly-1 gate varies with applied gate voltage for low BCCD implant dose option.*

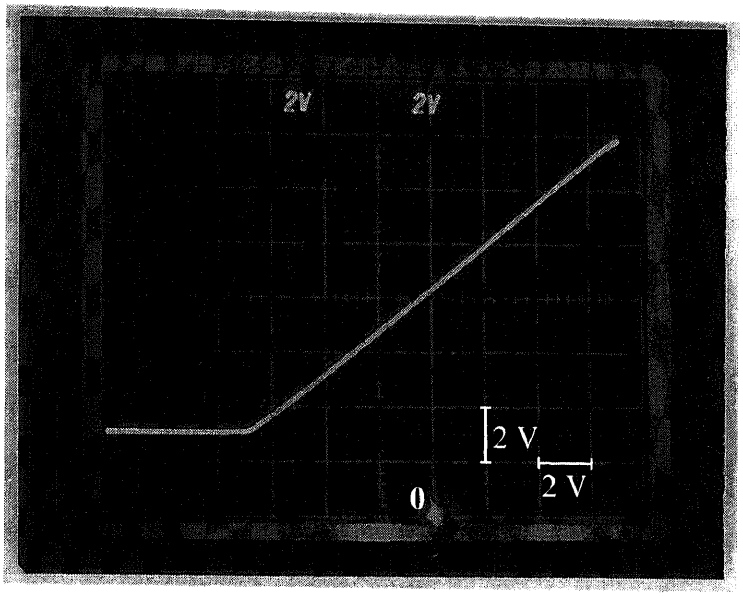


Figure 6.26 *Tested result of channel potential under poly-1 gate varies with applied gate voltage for high BCCD implant dose option.*

6.6 2-D Device Simulation

Two-dimensional simulations by PISCES IIB were performed to optimize the design of the BCCD storage area in the macropixel. The 2-D simulations formed the barrier for selecting the minimum width of the channel stop between the vertical BCCD channels and provided an estimation for the expected charge handling capacity due to the short channel effect. The doping profiles for the 2-D structure used by PISCES IIB were imported from the 1-D doping profiles obtained from SUPREM III with assumption of a 0.7 lateral diffusion ratio. Based on the 2-D structure and parameters provided by the author, part of the simulations described in this section were performed by Zeynep Pektas who is expected to continue this work as part of her doctoral dissertation research.

As indicated in Section 5.2.1, two dual BCCD implant doses were used for fabrication of the VHFR burst-image sensor. The lower BCCD implant dose consisted of 6.5×10^{11} cm^{-2} of arsenic and 6.5×10^{11} cm^{-2} of phosphorus, the higher BCCD implant

dose consisted of $1.2x10^{12}$ cm^{-2} of arsenic and $1.0x10^{12}$ cm^{-2} of phosphorus. The initial 2-D analysis of the short-channel effect on charge handling capacity and the effective channel stop width were performed for the lower dual BCCD implant dose. A 2-D simulation with the higher dual BCCD implant dose was done later to compare the maximum charge handling capacity of the BCCD register with the measured values.

6.6.1 Short Channel Effect on Charge Handling Capacity

Simulation Approach

The short channel effect results in lowering the charge handling capacity of a BCCD well and lowering the barrier potential between two adjacent BCCD wells. The BCCD channel structure and the potential profiles for empty and full wells are show in Figures 6.27(a) and 6.27(b), respectively. As mentioned in Chapter 3, PISCES IIB has its limitation on the number of mesh points, regions and contacts for the device structure to be simulated. Therefore, as shown in Figure 6.27(a), only five serial gates were used in the simulation of short channel effect. The thickness of oxide between the polysilicon gates δl_{ox} is about 1,400 Å which is obtained by 1-D process simulation as well as the process data provided by Sarnoff. The gates with an applied voltage of $V_{G,Max}$ form the BCCD wells, and the gates with an applied voltage of $V_{G,Min}$ create the potential barriers. $V_{G,Max}$ equals to 0, V_{σ}, and $V_{G(+)}$ for operation modes A, B, and C, respectively, and $V_{G,Min}$ equals to $V_{G(pinning)}$ for operation modes A and B, and 0 for operation mode C.

As previously defined in Section 6.3, the full well signal charge for the 1-D simulation is determined by two constrains: (1) the potential difference of 10 *kT/e* between the full well potential and the surface potential; (2) the potential difference of 20 *kT/e* between the full well potential and the barrier potential under the OFF-state gate. For 2-D simulation, the first constrain remains unchanged. However, the second constrain must be modified by the effect of the fringing field caused by the adjacent gates. Figure 6.27(b) illustrates (not to scale): (1) a potential profile of two full wells separated by a

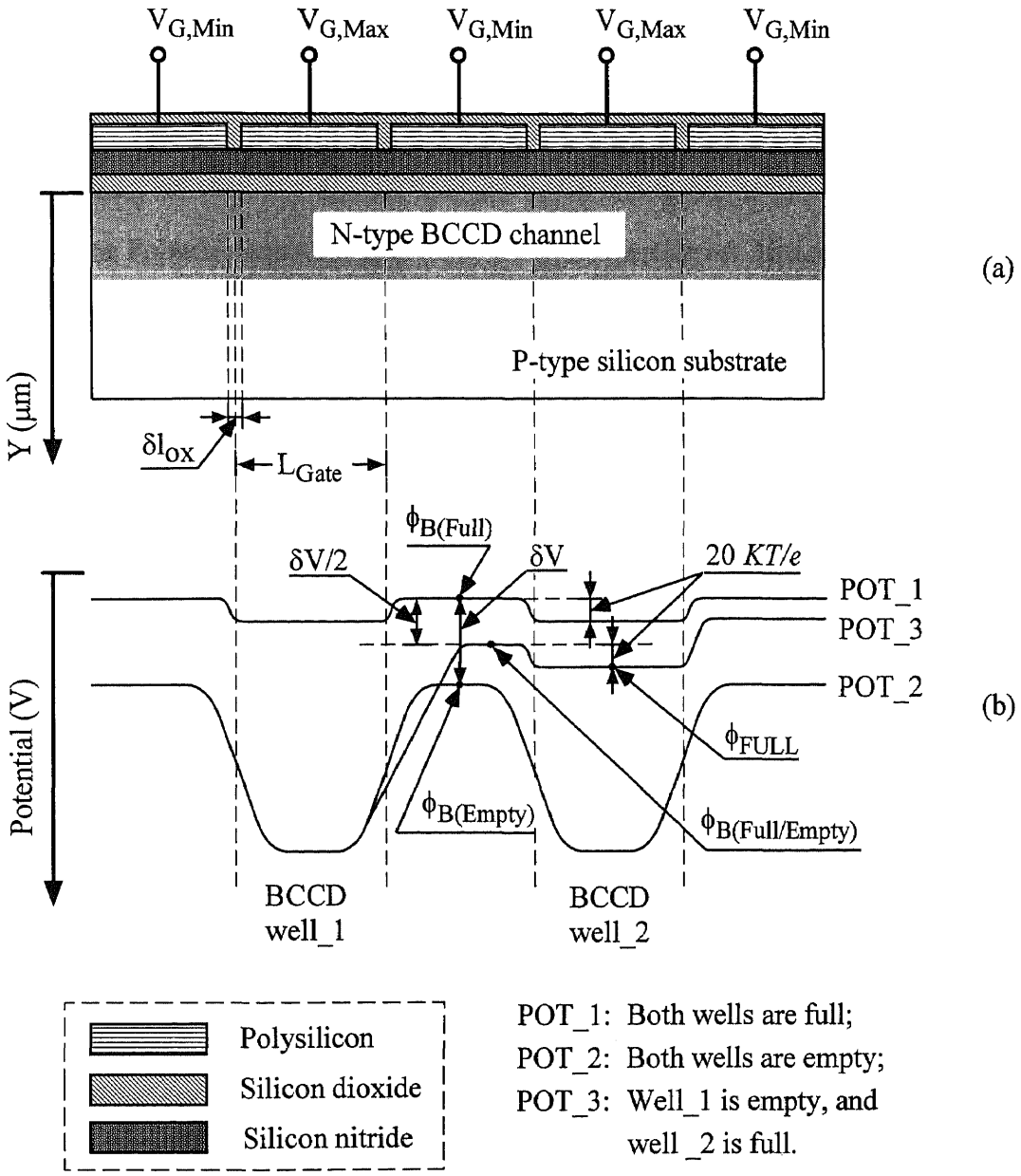


Figure 6.27 *The gate structure for 2-D simulation of charge handling capacity as function of gate length in* (a), *and the corresponding potential profiles in* (b) *for empty and full wells.*

barrier potential $\phi_{B(Full)}$ shown as POT_1; (2) a potential profile for two empty wells separated by a barrier potential $\phi_{B(Empty)}$ shown as POT_2; and (3) a potential profile for an empty well adjacent to a full well separated by an estimated barrier potential

$\phi_{B(Full/Empty)}$. The barrier potential for the empty and full well in POT_3 is estimated as:

$$\phi_{B(Full/Empty)} = \frac{1}{2}[\phi_{B(Empty)} - \phi_{B(Full)}] + \phi_{B(Full)} \cdot \quad (6.6)$$

Using PISCES IIB, the full well and empty well potential profiles are obtained by solving the Poisson's equation with a pre-set quasi Fermi level. However, the same quasi Fermi level must be set for the whole device structure. Therefore, a reasonable choice followed in this dissertation was to assume that the barrier potential for a full well adjacent to an empty well can be estimated by Equation (6.6). Thus, the full well potential in this case has been chosen to be 20 *kT/e* higher than the barrier potential $\phi_{B(Full/Empty)}$ is given by:

$$\phi_{FULL} \geq \phi_{B(Full)} + \frac{1}{2}[\phi_{B(Empty)} - \phi_{B(Full)}] + 20KT/e \, . \quad (6.7)$$

Simulation Results

The curves of simulated charge handling capacity of the BCCD channel for the three operation modes as function of the gate length are shown in Figure 6.28. Inspection of this figure shows that as the gate length is increased to about 5.0 μm, the charge handling capacity (Q_{Max}) saturates at about 6,200 electrons/μm^2 for operation mode B, 5,600 electrons/μm^2 for operation mode C, and 5,500 electrons/μm^2 for operation mode A. It should be noted that the above saturation values of Q_{Max} are about 10% lower than those obtained by 1-D simulation (see Figure 6.12). Figure 6.28 also shows that for the gate length of 1.5 μm (corresponding to the minimum gate length in the pixel memory of the VHFR burst-image sensor), the values of Q_{Max} are about 3,700 electrons/μm^2 for operation modes B and C and 2,600 electrons/μm^2 for operation mode A.

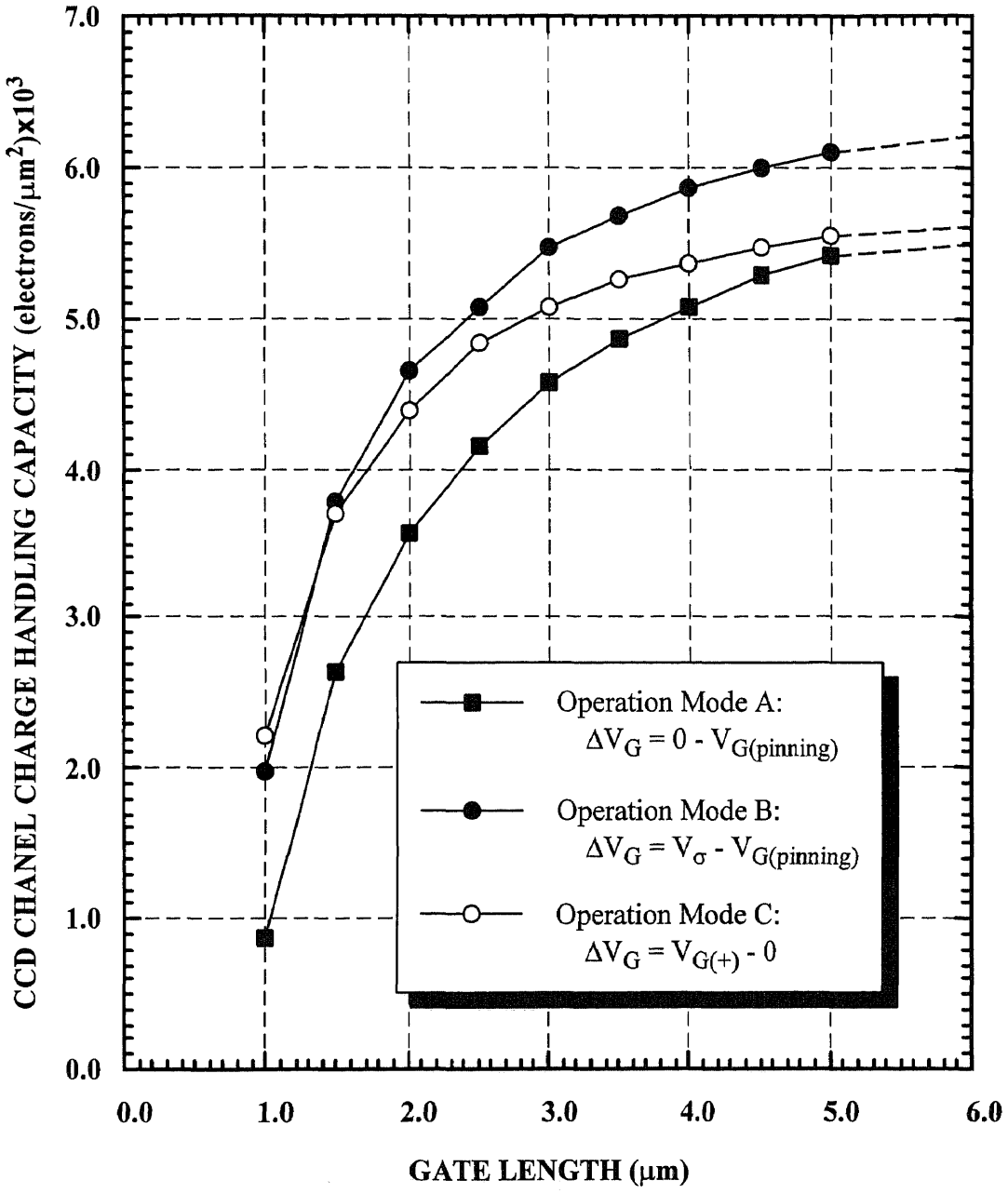


Figure 6.28 *CCD channel charge handling capacity as function of BCCD gate length for operation modes A, B, and C.*

Discussion of the Results

In the design of VHFR burst-image sensor, the area of the minimum CCD charge storage element is 1.5-μmx3.0-μm, and the imager has been operated in mode A. Thus, the charge handling capacity of the minimum CCD charge storage element is estimated as 11,800 electrons. However, for operation modes B and C, the estimated value of Q_{Max} is about 17,000 electrons.

Based on the presented simulation, the following suggestions can be made for the design and operation of the next imager chip:

1. Short gate length reduces the charge handling capacity of BCCD well significantly. In order to obtain a high charge handling capacity and to increase the dynamic range of the image signal, a larger CCD gate length should be used. On the other hand, with the shorter gate length, more frame storage can by achieved. In order to optimize the dynamic range and the resolution of the imager chip, the suggested CCD gate length should be at least 2.5 μm.
2. A higher CCD implant can be used to improve the CCD charge handling capacity.
3. Operating the imager in mode B can improve the CCD charge handling capacity by at least 20% in comparing with operating in mode A.

Comparison of Simulated and Measured Q_{Max}

At present time, test results are available only for the higher BCCD implant dose option. Therefore, in order to compare with the simulated and measured values of the charge handling capacity, charge handling capacity for a 1.5-μmx3.0-μm BCCD well of higher doping option (As = $1.2x10^{12}$ cm^{-2}, and P = $1.0x10^{12}$ cm^{-2}) has been simulated. According to 1-D simulation, the pinning voltage is -11.2 V for this option. In actual operation of this imager, the clock voltage had clock voltage swings, ΔV_G, in the range of 5.5 to 11.2 V. The results of the simulation are given in Table 5.4. This includes charge handling capacity (CHC) for BCCD channel in electrons/μm^2 and for a 1.5-μmx3.0-μm

BCCD well in electrons as function of gate voltage swing, ΔV_G, for 1-D and 2-D simulation.

Table 6.4 *Simulation results of charge handling capacity of minimum charge storage element with high doping option.*

	1-D simulation ΔV_G = 0 to -11.2 V	**2-D Simulation** ΔV_G =		
		0 to -11.2 V	0 to -7.4 V	0 to -5.5 V
CHC_CCD-Channel (electrons/μm^2)	9,722	3,818	3,796	2,442
CHC_Minimum-Well (electrons)	43,750	17,182	17,081	10,987

From Table 5.4, we can see that, for the high doped CCD channel with 1.5 μm gate length, the change of gate voltage swing from 7.4 volts to 11.2 volts gives no significant improvement on the charge handling capacity. The reason is that for such a short gate length, the fringing field reduces the potential barrier significantly under the adjacent gate.

The smallest BCCD storage well of the VHFR burst-image sensor (with the area of 1.5-μmx3.0-μm) is located in parallel register. During the operation of the imager, the minimum gate voltage swing of parallel register is 7.4 V. The measured saturation signal charge obtained during the operation of the imager was about 11,000 electrons which is 35% less than the simulated value of the Q_{Max} corresponding to the 1.5-μmx3.0-μm BCCD well with a 7.4 V gate voltage swing. However, this value is agree with the simulated value of the 1.5-μmx3.0-μm BCCD well with a 5.5 V gate voltage swing. However, since the clock voltage during operation was applied through a resistance of 25 Ω in series with imager clock phases, the actual operating voltage swing, ΔV_G, is

expected to be approximately 5.5 V. Thus, this gives a very good agreement between the measured value of Q_{Max} = 11,000 electrons and the simulated value of Q_{Max} = 10,987 electrons for ΔV_G, = 5.5 V.

6.6.2 Channel Stop Barrier Heights

Simulation Approach

As indicated before, the BCCD channels are formed by implanting arsenic and phosphorus on the p-type silicon substrate. The un-implanted p-type silicon SCCD region is used for channel stops between the BCCD channels. The structure of two BCCD channels separated by SCCD channel stop is shown in Figure 6.29(a), and the corresponding potential profiles (not to scale) of two full BCCD wells and two empty BCCD wells are illustrated as Ψ_{FULL} and Ψ_{EMPTY}, respectively, in Figure 6.29(b). The values of $V_{G,Max}$ for operation modes A, B, and C in Figure 6.29(b) have been defined to be the same as that described in Section 6.6.1.

In order to confine the charge within the BCCD channel, the potential barrier built by the SCCD channel stop should be greater than 20 *kT/e*. In general, the potential barrier of SCCD channel stop reaches its minimum in the case of one full BCCD well adjacent to an empty BCCD well. Similarly to the discussion in Section 6.6.1, since the same quasi Fermi level must be set up for the whole device structure, the worst case condition of one full well adjacent to an empty well could not be simulated using the available software in our lab. Therefore, a reasonable choice corresponding to the worst case in the operation is the difference between the full well potential and the minimum potential of SCCD channel stop of two empty BCCD wells should be greater than 20 *kT/e*. Since the minimum gate length of BCCD register is 1.5 μm in the design of the VHFR burst-image sensor, the values of quasi Fermi level of two full wells used in this simulation are chosen to be the same as those of full well quasi Fermi level used in Section 6.6.1 for the simulation of Q_{Max} of BCCD well with 1.5-μm gate length.

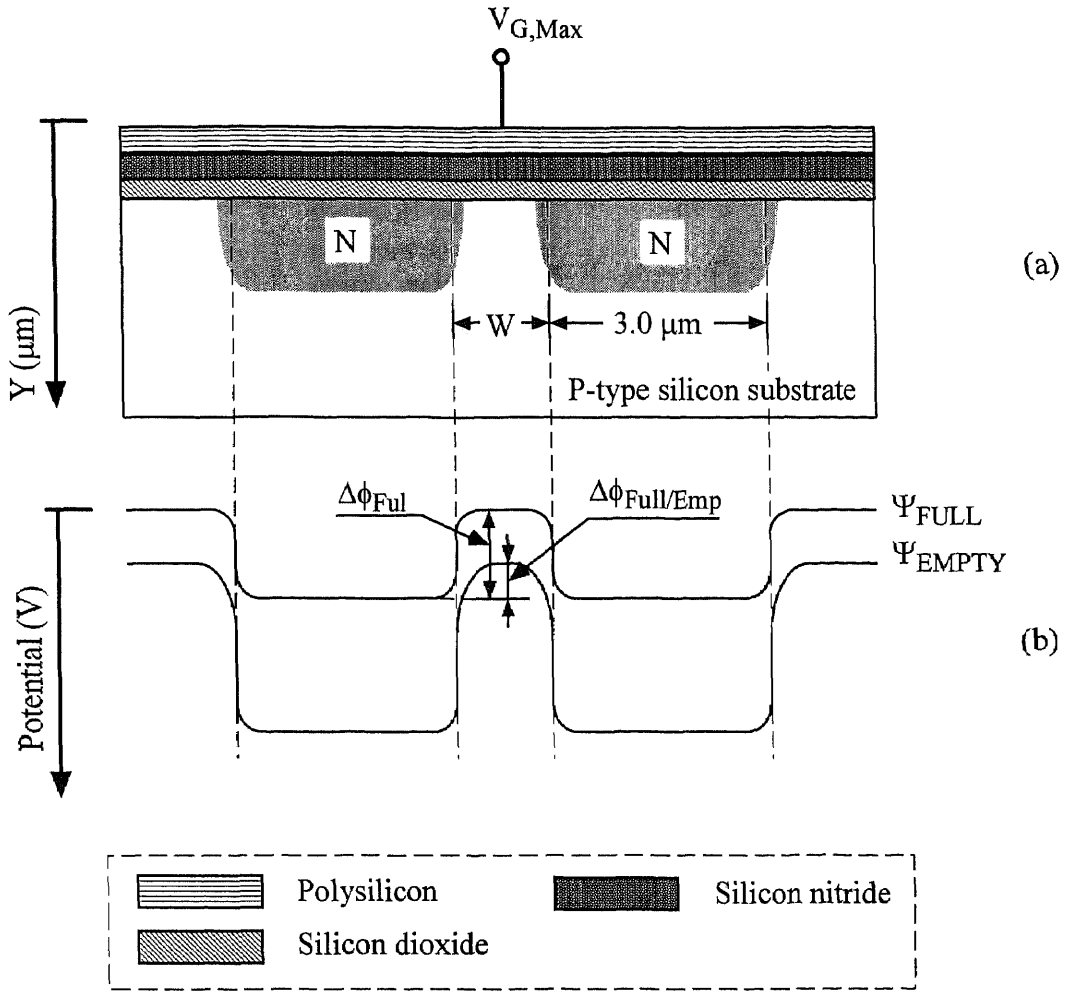


Figure 6.29 *Device structure employed for the simulation of channel stop barrier heights in* (a), *and the corresponding potential profile in* (b) *for empty and full wells.*

Simulation Results

Channel stop barrier heights for two full wells ($\Delta\phi_{Full}$) and for a full well adjacent to an empty well ($\Delta\phi_{Full/Emp}$) are function of the nominal channel stop width W and operation modes. The effectiveness of the SCCD region acting as a channel stop between two BCCD channels is illustrated in Figures 6.30 to 6.32. Figures 6.30, 6.31, and 6.32 illustrate the SCCD channel stop barrier heights of two full wells and a full well adjacent

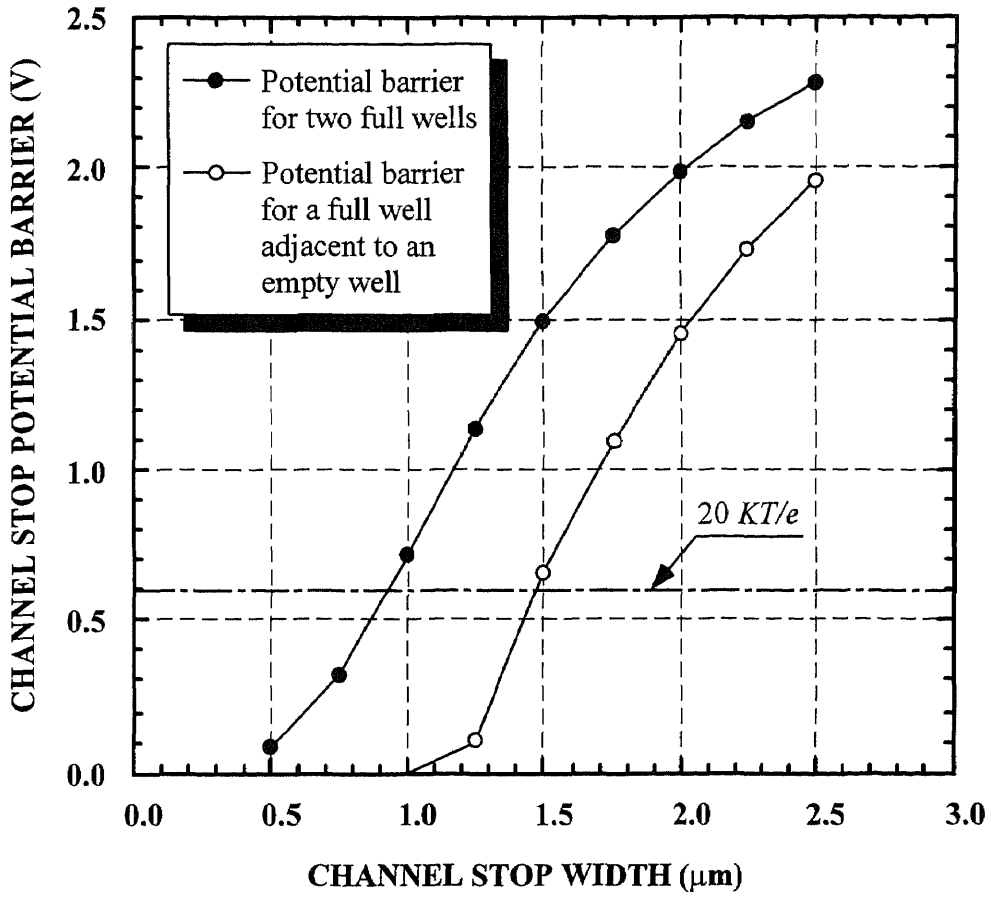


Figure 6.30 *SCCD channel stop potential barrier height as function of channel stop width (W) for two full BCCD wells and a full BCCD well adjacent to an empty BCCD well corresponding to 3.0-μm BCCD channels width and 1.5-μm gate length for operating in mode A.*

to an empty well as function of channel stop width (W) corresponding to 3.0-μm BCCD channel width and 1.5-μm gate length operating in modes A, B, and C, respectively.

Inspection of Figures 6.30, 6.31, and 6.32 shows that, as expected, the SCCD channel stop potential barrier for two full BCCD wells is higher than that of a full BCCD adjacent to an empty BCCD well. The SCCD channel stop potential barrier for a full BCCD well adjacent to an empty BCCD well becomes greater than 20 *kT/e* when the

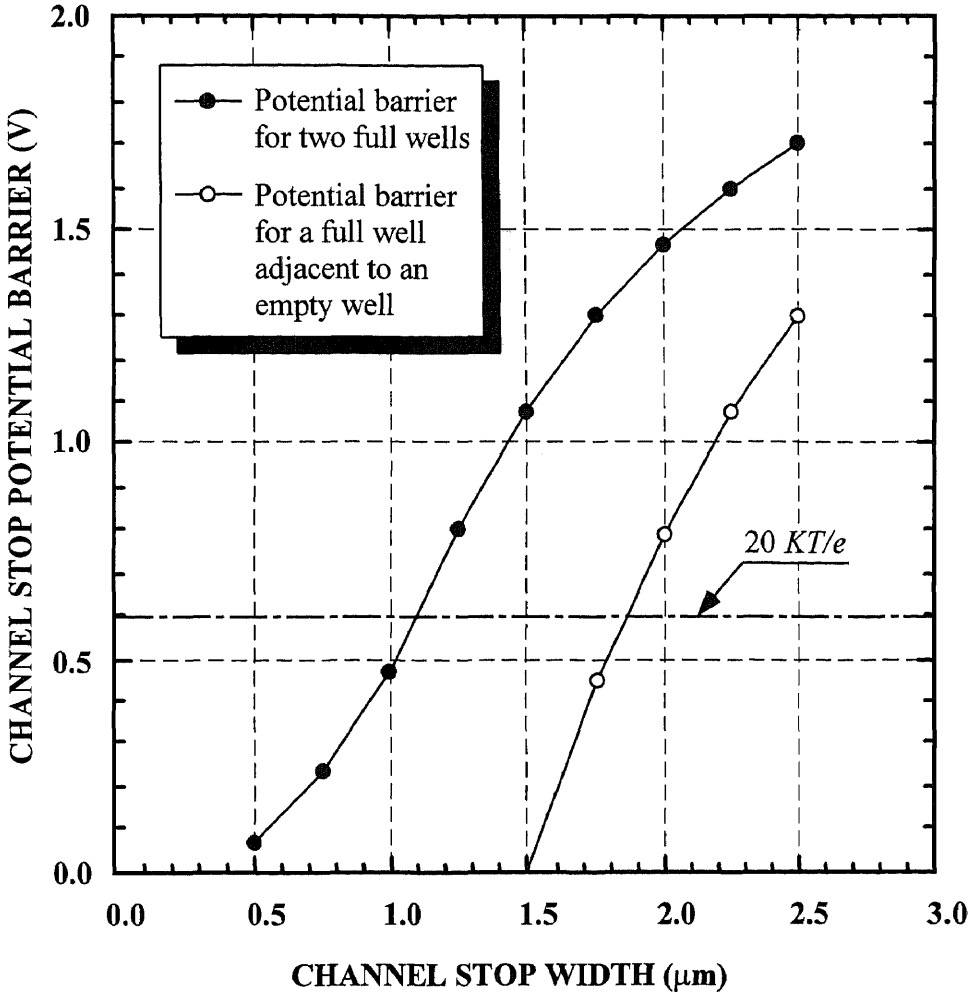


Figure 6.31 *SCCD channel stop potential barrier height as function of channel stop width (W) for two full BCCD wells and a full BCCD well adjacent to an empty BCCD well corresponding to 3.0-μm BCCD channels width and 1.5-μm gate length for operating in mode B.*

nominal channel stop width, W, is greater than 1.5 μm, 2.0 μm, and 1.75 μm for operation in modes A, B, and C, respectively. In the design of VHFR burst-image sensor, the minimum width of nominal SCCD channel stop between BCCD channels was selected to be 2.5 μm. As shown in Figures 6.30, 6.31, and 6.32, the minimum SCCD channel stop potential barrier height is higher than 1.5 V for operation in modes A and C,

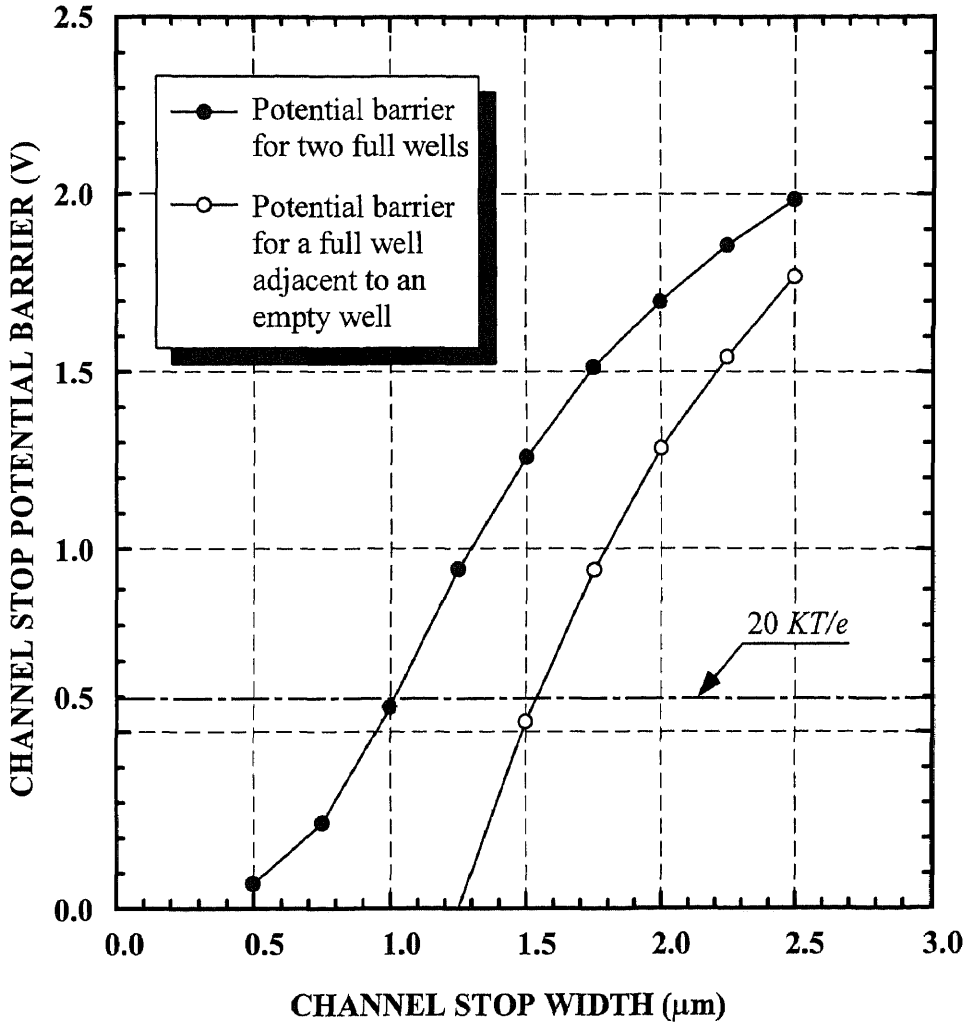


Figure 6.32 *SCCD channel stop potential barrier height as function of channel stop width (W) for two full BCCD wells and a full BCCD well adjacent to an empty BCCD well corresponding to 3.0-μm BCCD channels width and 1.5-μm gate length for operating in mode C.*

and higher than 1.0 V for operation in mode B. Thus, the charge signal can by properly confined within the BCCD channels for SCCD channel stop width of 2.5 μm.

Our 2-D simulation results also indicate that the effect of lateral diffusion of the BCCD implant does not affect charge handling capacity of the BCCD channels with 1.5

μm gate length and 3.0 μm channel width. In other words, the simulation results indicate that for the signal level limited by the 1.5 μm gate length, the possible increase in Q_{Max} due to BCCD implants side diffusion is compensated by the expected decrease of Q_{Max} due to fringing field of the channel stop edges.

6.7 Properties of BCCD Channels

Based on the 1-D and 2-D simulation results presented in this chapter, the properties of the BCCD channels operated in mode A for two implant options are summarized in Table 6.5. The values of the pinning gate voltage, maximum electric field, and the charge handling capacity per unit area were obtained by 1-D simulations. However, the charge handling capacity for the smallest BCCD well of the imager was obtained by 2-D simulation.

6.8 Output Amplifier Conversion Rate

The on-chip output amplifier shown in Figure 4.6 is a MOSFET source follower with a floating-diffusion charge input. No additional masks are used to construct the on-chip source follower. This enhancement buried-channel MOSFET is formed by a polysilicon-1 gate on the BCCD channel. As indicated in Figure 4.6, the gate width and length of the MOSFET are 30 μm and 4 μm, respectively. Since the capacitance of the floating diffusion and the metal interconnection is very low, the signal response of the MOSFET gate voltage to the detected signal can be obtained using the estimated gate capacitance. The capacitance per unit area of the MOSFET gate is given by:

$$\frac{1}{C} = \left(\frac{d_{oxide}}{\varepsilon_r^{oxide}} + \frac{d_{nitride}}{\varepsilon_r^{nitride}} + \frac{d_{Si}}{\varepsilon_r^{Si}} \right) \cdot \frac{1}{\varepsilon_0} \,. \tag{6.8}$$

However, the BCCD channel under the MOSFET gate may be filled with layer of electron that can extend close to the Si/SiO_2 interface. In this case, the thickness of

silicon layer in Equation (6.8), d_{Si}, can be ignored. According to the process specification, d_{oxide} = 350 Å, $d_{nitride}$ = 650 Å, and by assuming d_{Si} = 0, for the 30-μmx4-μm ploysilicon-1 gate, the capacitance of the MOSFET gate is about 60.23 fF. Thus, the estimated voltage conversion rate of the MOSFET gate voltage change to the detected charge signal is 2.66 μV/electron. The measured value of the floating diffusion amplifier conversion rate is 2.3 μV/electron, that is very close to the estimated value.

Table 6.5 *Properties of BCCD channel.*

BCCD Implant Doses	**As: $6.5x10^{11}$ cm^{-2} P: $6.5x10^{11}$ cm^{-2}**	**As: $1.2x10^{12}$ cm^{-2} P: $1.0x10^{12}$ cm^{-2}**
CCD Channel Dielectric	350 Å SiO_2 and 650 Å Si_3N_4	350 Å SiO_2 and 650 Å Si_3N_4
Pinning Gate Voltage *(Volts)*	-7.6	-11.2
Maximum Electric Field in Silicon *(V/cm)*	$1.81x10^5$	$3.12x10^5$
Maximum Electric Field in Silicon-dioxide *(V/cm)*	$6.21x10^5$	$9.79x10^5$
Maximum Electric Field in Silicon-nitride *(V/cm)*	$3.23x10^5$	$5.09x10^5$
Charge Handling Capacity per Unit Area* *(electrons/μm^2)*	5,938	9,722
Charge Handling Capacity of Smallest BCCD Well* *(electrons)*	11,833	17,182

† Simulation results are corresponding to gate voltage swing $\Delta V_G = 0 - V_{G(pinning)}$;

* 1-D simulation results by using SUPREM III;

** 2-D simulation results by using PISCES IIB.

CHAPTER 7

HIGH-SPEED PHOTODETECTOR

7.1 Introduction

The design goal of the VHFR burst-image sensor described in Chapter 4 was to capture images at frame rates up to 10^6 frames/sec with no image lag. To achieve no (zero) lag operation, a pinned-buried photodetector structure [86] was selected. However, since the imager has a rather large photodetector (approximately 30-μmx11-μm), to obtain an essentially complete charge readout in time much short than 1.0 μsec, a multi-implant (graded) pinned-buried photodetector structure was introduced [86]. A simulation study for this photodetector structure is presented in this chapter.

On the bases of the initial study, a decision was made to construct the macropixels of the 360x360 VHFR burst-image sensor with the 30-μmx11-μm photodetector using three implanted segments. However, for comparison, simulation results were also presented in the case of two implanted segments and one implant segment for the 30-μmx11-μm photodetector. The simulation results for the low and the high BCCD implant options (see Section 5.2.2) for fabrication of the VHFR burst-image sensor were found to be practically the same. Therefore, although the simulation results presented in this chapter were applied to the low BCCD implant option, they are also applicable for the high BCCD implant option. In addition, simulation study was also made for optimal construction of a large (about 65-μmx35-μm) photodetector that has been considered for a future burst-image sensor with large (100-μmx50-μm) macropixels to increase the fill factor from 13.5% to 45%. The details of this simulation study are presented in Appendix C. However, the results of this study are also summarized in this chapter.

On the basis of the results obtained from both studies of photodetector structures, a generalized method is presented for describing the readout of charge from the multi-implant (graded) pinned-buried photodetector structure.

7.2 Design and Operation of Photodetector

The layout (top view) and the BCCD charge readout structure of the photodetector of the 360x360-element VHFR burst-image sensor is shown in Figure 7.1. The fabrication of the photodetector structure with multiple implants along the cut-line A-A′ shown in Figure 7.1 is illustrated in Figure 7.2. The cut-line A-A′ represents the longest charge transfer distance in the photodetector. As shown in Figure 7.2, the fabrication of the high-speed photodetector includes a BCCD channel implant which is done before the deposition and definition of the polysilicon gates. Then after the polysilicon gates are formed, the first photodetector N-type implant is made to be self-aligned to the charge collecting gate (G_1). This is followed by the second and third N-type implants, and the detector structure is completed by a shallow P-type implant which is placed on the top of photodetector to form the pinned-buried detector structure.

The construction and operation of the multi-implant pinned-buried photodetector and BCCD readout is illustrated in Figure 7.3 by a cross-sectional view (along the cut-line A-A' in Figure 7.1) in part (a) and the corresponding potential profile in part (b). It may be noted that in Figure 7.3(a) the implants are shown with 70% lateral side diffusion. As illustrated in Figures 7.2 and 7.3, the maximum length of each of the three detector N-type implant levels is 11 μm. In this case, N1 includes BCCD implant plus the first photodetector implant, N2 includes N1 implants plus the second photodetector N-type implant, and N3 includes the N2 implants plus the third photodetector N-type implant. The graded potential along the photodetector is created by the variation of the doping concentration in the photodetector and the resulting fringing field.

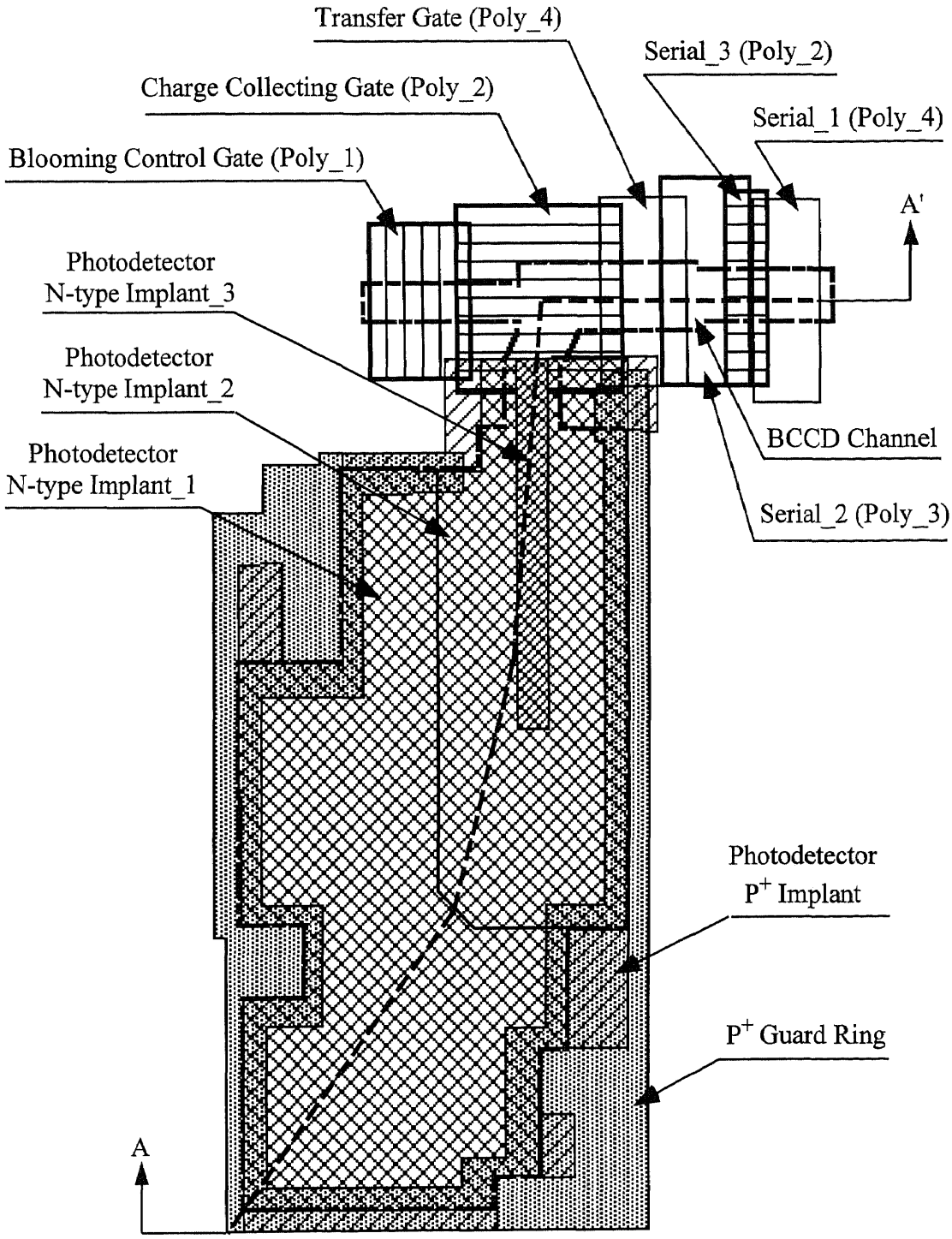


Figure 7.1 *Layout of the multi-implant (graded) pinned-buried high-speed photodetector.*

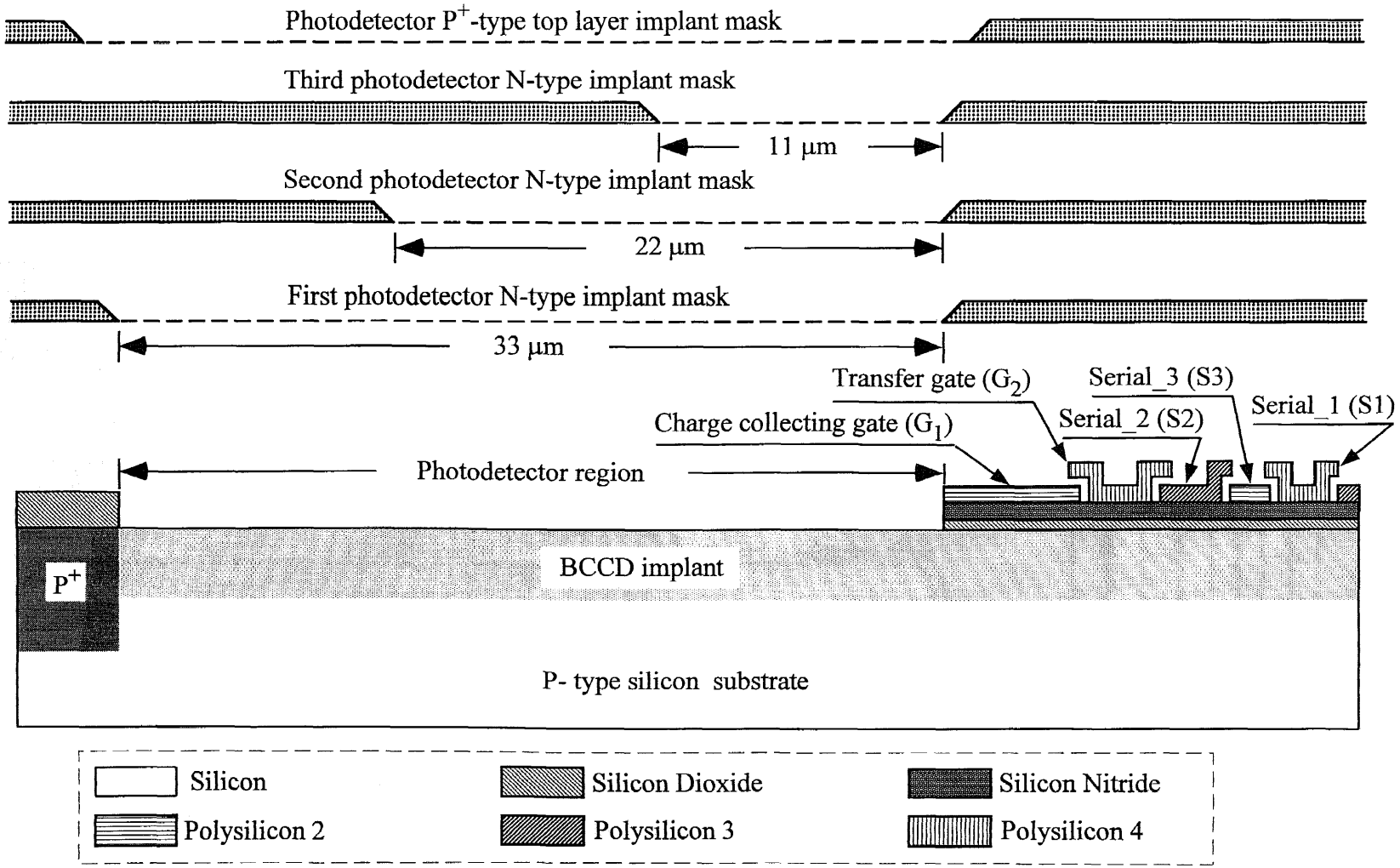


Figure 7.2 *Cross-sectional view of the implant masks and the corresponding photodetector regions.*

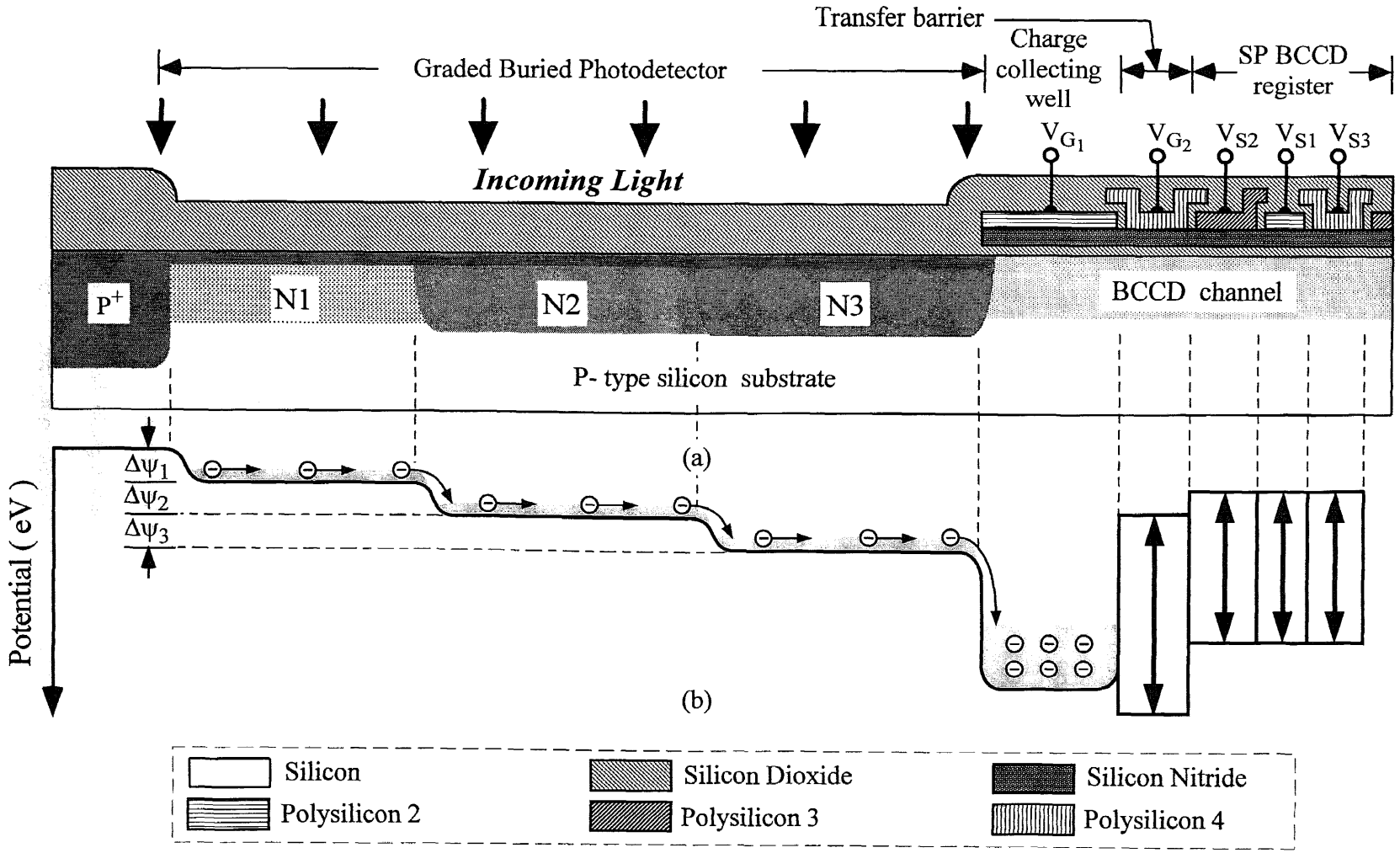


Figure 7.3 *Cross-sectional view illustrating of photodetector doping in* (a) *and the corresponding potential distrubution in* (b).

The high-speed photodetector was designed to have a potential difference between each step, $\Delta\Psi_1$, $\Delta\Psi_2$, and $\Delta\Psi_3$ shown in Figure 7.3(b) of approximately 0.5 eV. The values for the photodetector implants were selected on the bases of 2-D simulation by PISCES IIB. The resulting stair-case potential profile breaks up the photodetector structure into three about-equal-length regions where region-2 acts as a charge sink for region-1, and region-3 acts as a charge sink for region-2. Finally, the potential well under the charge collecting gate (G_1) acts as a sink for the charge collected by the photodetector during the optical integration time, T_{int}. At the end of the optical integration time, the signal charge accumulated in the charge collecting well is transferred (readout) to the BCCD register for temporary storage during the charge acquisition cycle of the imager operation. In other words, the charge signal detected by the photodetector is continuously accumulated by the charge collecting well that is periodically emptied into the BCCD readout register.

7.3 2-D Simulation of Detector Operation

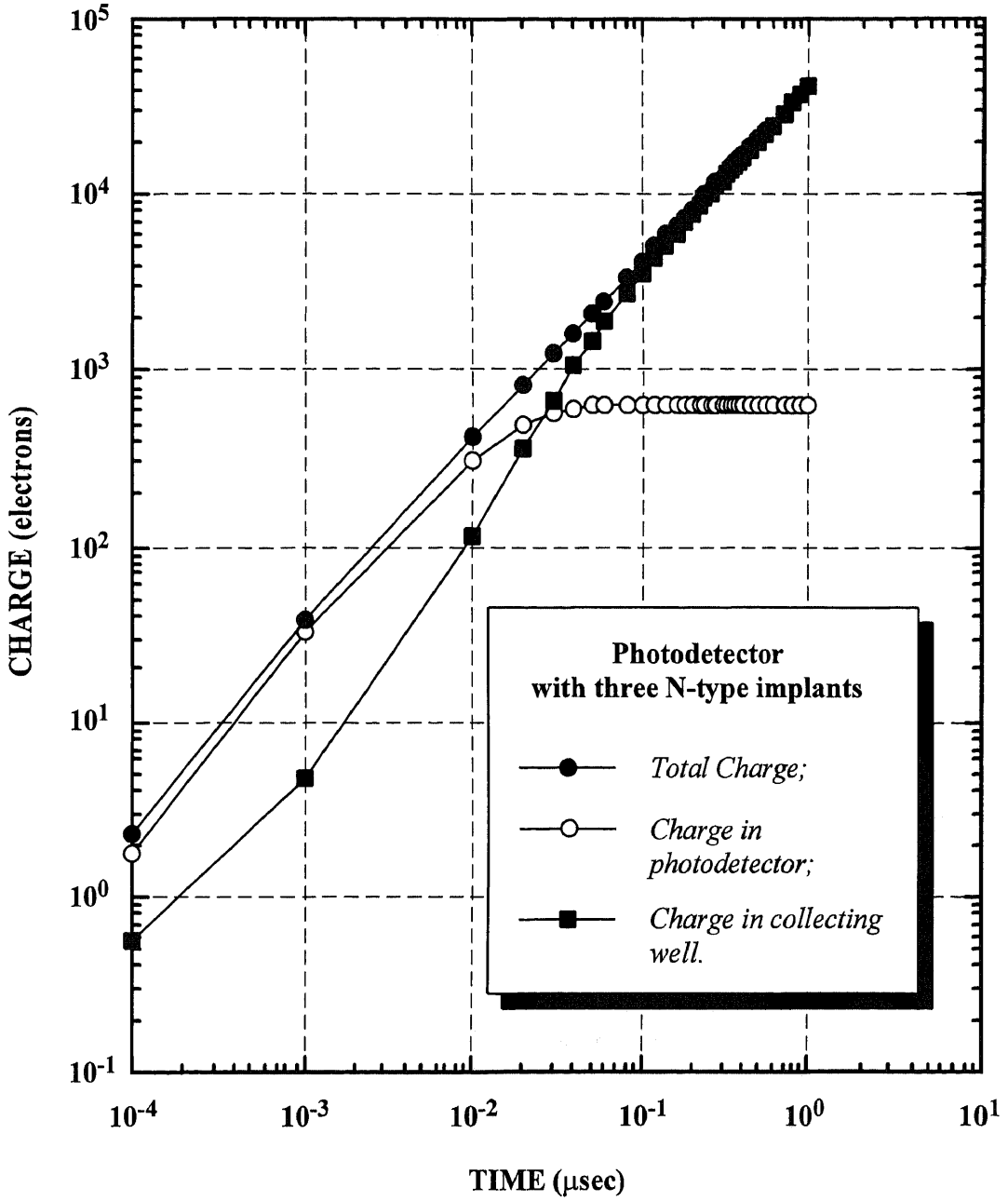
Initially the 2-D doping profiles of the photodetector were obtained by SUPREM IV. However, it was found that essentially the same results can be obtained by using 1-D SUPREM III simulation with 70% lateral side diffusion. The operation of the high-speed photodetector was studied by simulations using PISCES IIB. The simulation studies included the time response of the photodetector to a step illumination and the decay time of the accumulated photodetector channel charges after the illumination is turned off. For this simulation study, it was assumed that the total illumination corresponds to a detected charge of 20,000 electrons and the different illumination levels were obtained by using illumination time of 0.5, 1.0, 1.5, and 3.0 μsec.

As will be illustrated in Section 7.3.1, the magnitude of the steady-state accumulated photodetector channel charge due to step illumination was found to be directly proportional to the illumination intensity. The maximum useful signal is limited

by the charge handling capacity (Q_{Max}) of the BCCD storage registers at the pixel locations. The charge handling capacity indicated in Chapter 6 originally was estimated by 1-D simulation to be about 40,000 electrons for the high BCCD implant dose and 20,000 electrons for the low BCCD implant dose. Our later 2-D simulation (see section 6.6.1) showed that the Q_{Max} is about 17,200 electrons for the high BCCD implant option and 11,800 electrons for the low BCCD implant option. Finally, the recently available experimentally measured value of Q_{Max} for the high doping option is 11,000 electrons (also see Section 6.6.1). Therefore, in retrospect about 50% lower illumination would be preferable. However, this does not change the validity of the simulation results, since the charge handling capacity of the BCCD register is exceeded only for the case of optical integration time of 0.5 μsec. And even this case represents an operation for which the actual BCCD signal charge will be limited to about 11,000 electrons by the blooming drain structure coupled to the charge collection well.

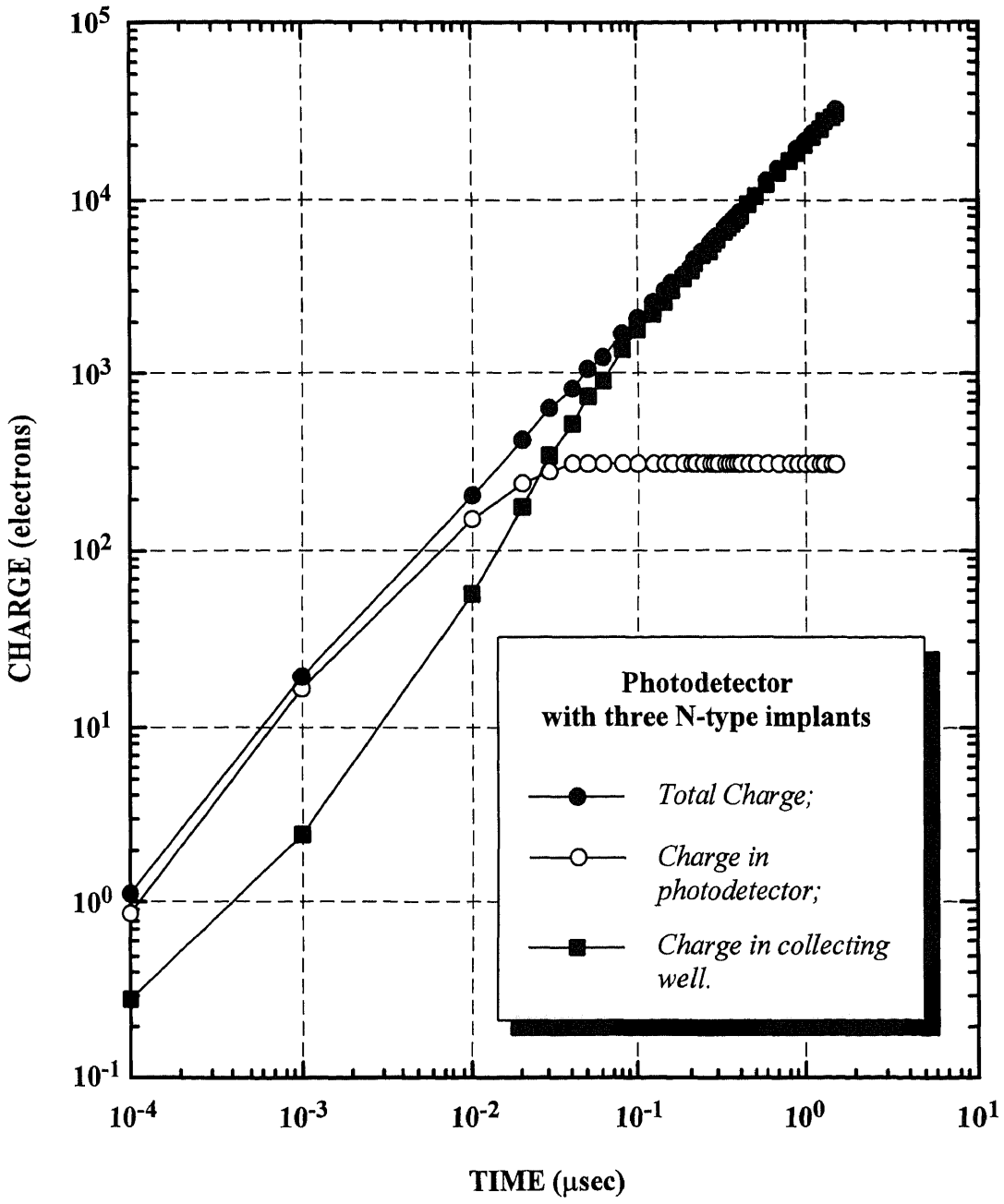
7.3.1 Time Response to Step Illumination Signal

The time response of the photodetector to a step illumination signals simulated for illumination intensities corresponding to the total detected signal of 20,000 electrons for optical illumination time of 0.5 μsec, 1.0 μsec, 1.5 μsec, and 3.0 μsec are shown in Figures 7.4, 7.5, 7.6, and 7.7, respectively. An inspection of these figures shows that for total charge increasing at a constant rate, the photodetector channel charge builds-up in the detector structure in about 0.05 μsec to a steady-state saturation level of about 630, 315, 210, and 105 electrons for the illumination intensities corresponding to optical illumination time of 0.5 μsec, 1.0 μsec, 1.5 μsec, and 3.0 μsec, respectively. After a response time, $t_{99\%}$, of about 0.05 μsec, the photodetector channel charge remains constant while the charge collecting well continues to integrate the detected charge until it reaches the value of 20,000 electrons minus the photodetector channel charge steady-



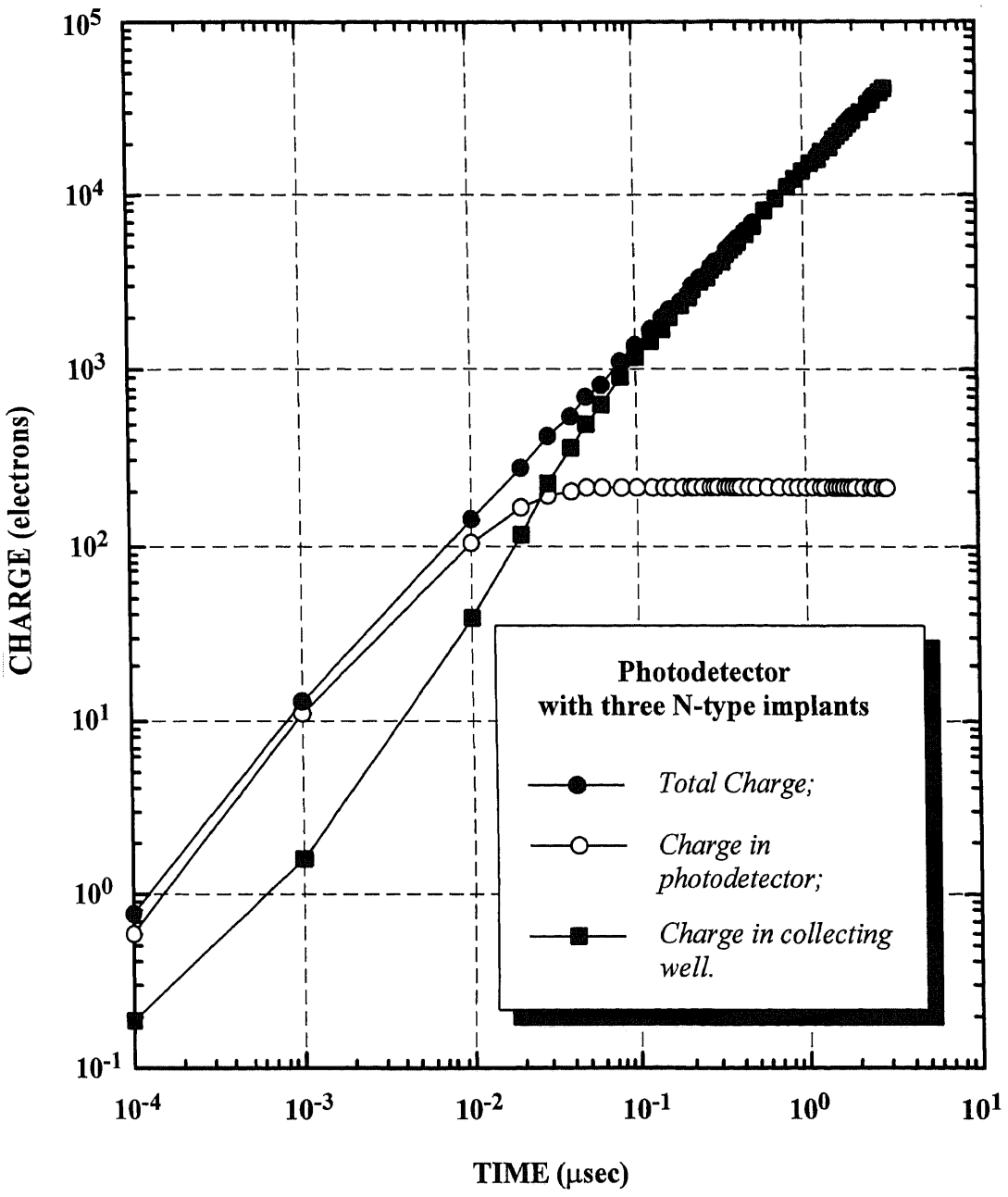
(Illumination intensity: 20,000 electrons in 0.5 μsec)

Figure 7.4 *Time response of the photodetector with three N-type implants to a step illumination corresponding to 20,000 electrons in 0.5 μsec.*



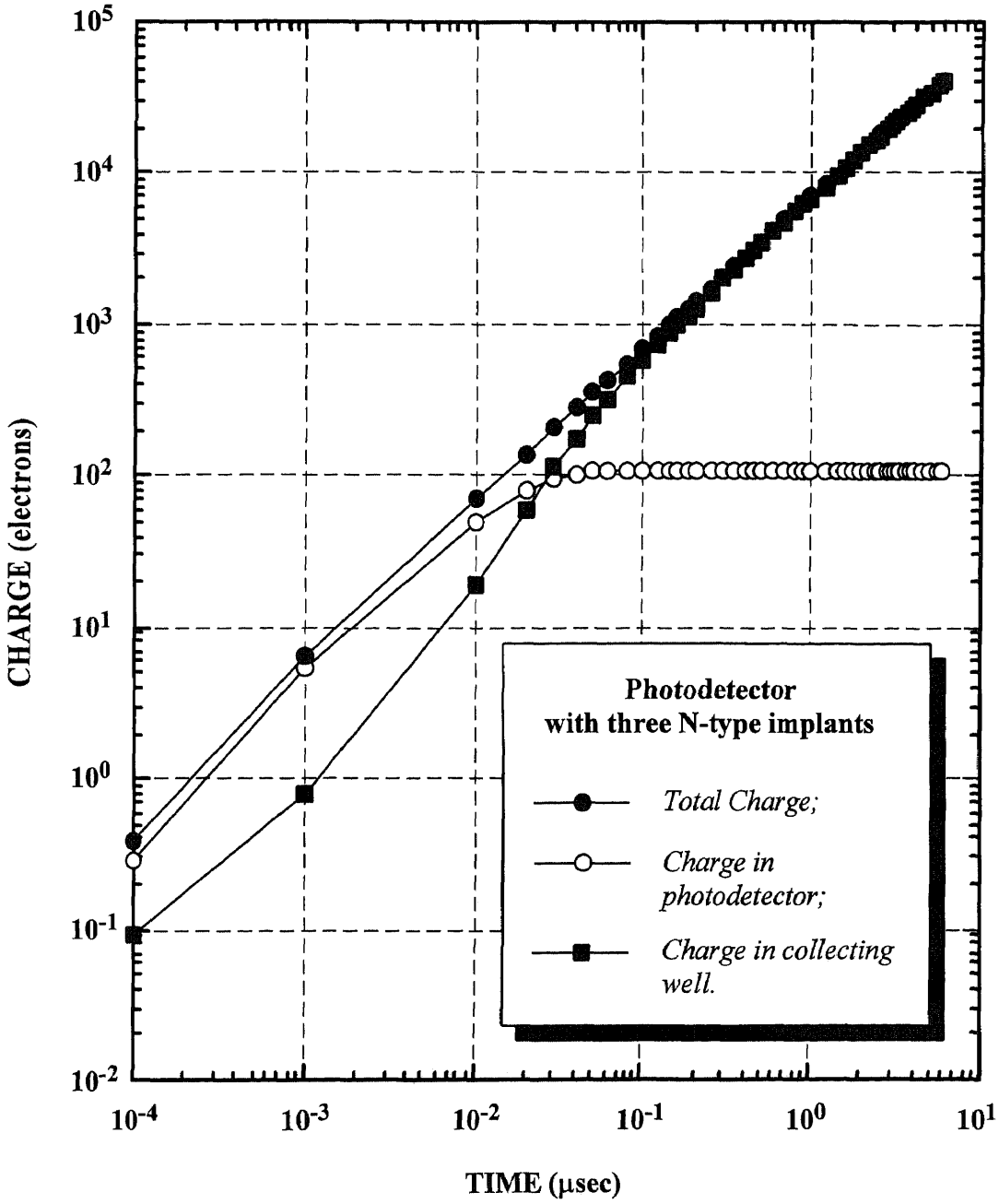
(Illumination intensity: 20,000 electrons in 1.0 μsec)

Figure 7.5 *Time response of the photodetector with three N-type implants to a step illumination corresponding to 20,000 electrons in 1.0 μsec.*



(Illumination intensity: 20,000 electrons in 1.5 μsec)

Figure 7.6 *Time response of the photodetector with three N-type implants to a step illumination corresponding to 20,000 electrons in 1.5 μsec.*



(Illumination intensity: 20,000 electrons in 3.0 μsec)

Figure 7.7 *Time response of the photodetector with three N-type implants to a step illumination corresponding to 20,000 electrons in 3.0 μsec.*

state saturation level. The response time $t_{99\%}$ is defined here as the time when the photodetector channel charge reaches 99% of its steady-state saturation value.

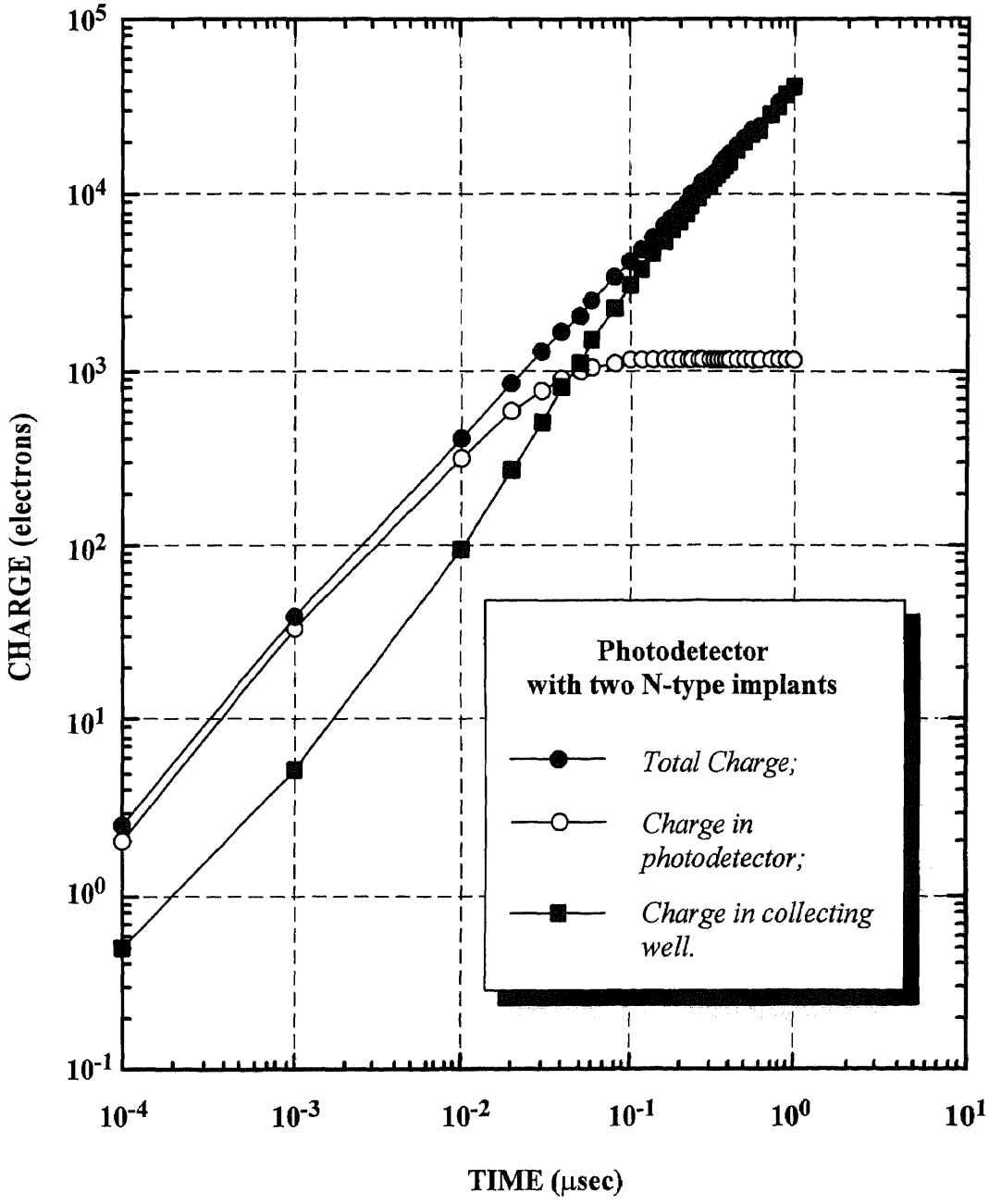
For comparison, the time response of the pinned-buried 30-μmx11-μm photodetector with two constant potential segments has been simulated and the results are shown in Figures 7.8, 7.9, 7.10, and 7.11. The simulation results of the photodetector with a single constant potential segment are shown in Figures 7.12, 7.13, 7.14, and 7.15. Inspection of Figures 7.8 to 7.15 shows that, the response time, $t_{99\%}$, is about 0.1 μsec and 0.4 μsec for photodetector with two and one photodetector implant, respectively.

It should also be added that the time response simulation data for a large (with the size of about 65-μmx35-μm) photodetector is also given in Appendix C, Section C.2.

7.3.2 Charge Decay in the Photodetector

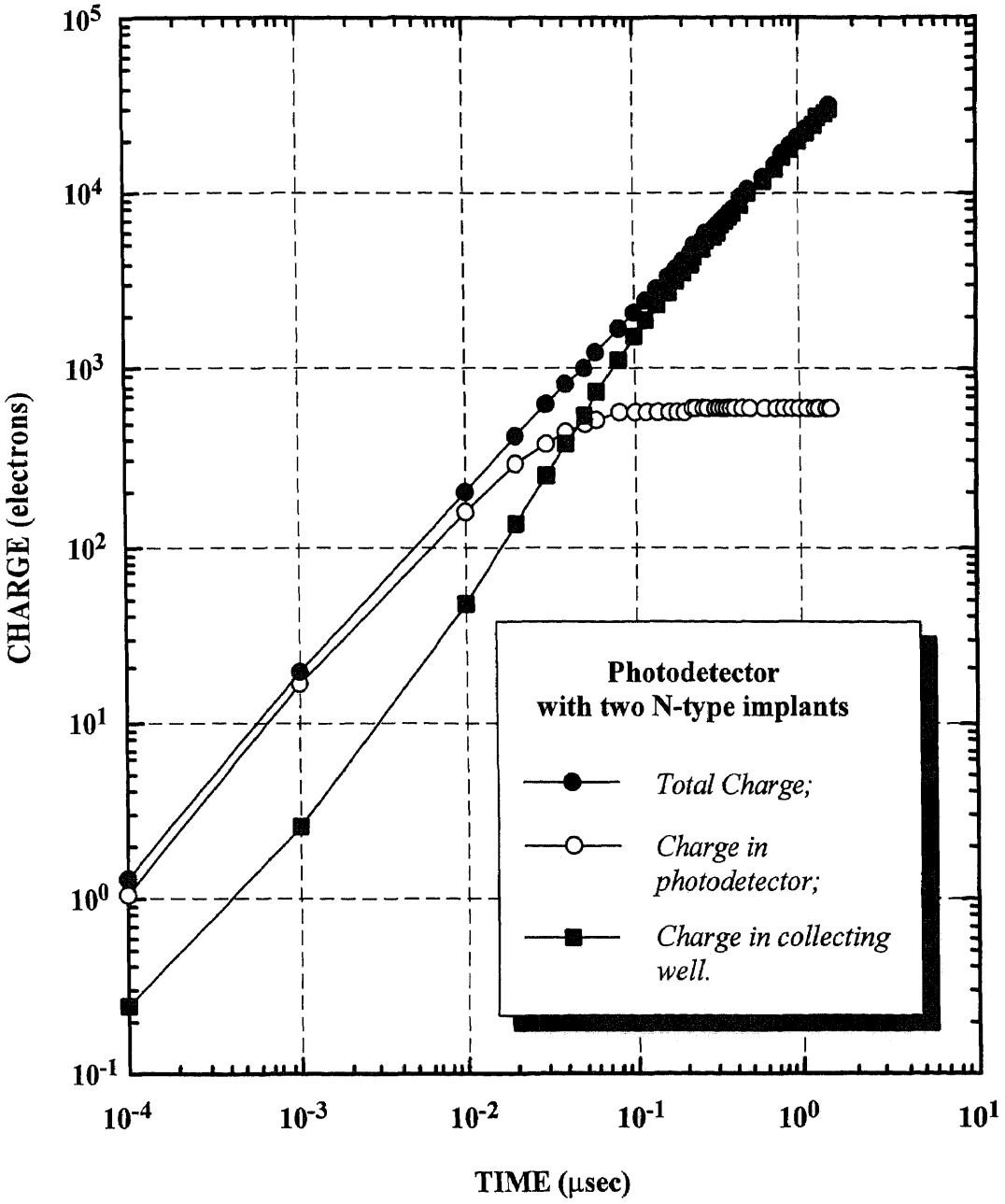
After the optical illumination is stopped, the photodetector channel charge is transferred to the charge collecting well which is operated at a more positive potential.

Figure 7.16 illustrates the decay of the channel charge in the photodetector with three N-type implants as a function of time after the optical illumination is stopped. The four curves correspond to four illumination intensities that result in integration of 20,000 electrons in 0.5 μsec, 1.0 μsec, 1.5 μsec, and 3.0 μsec, respectively. It should be noted that the minimum charge level in Figures 7.16 to 7.22 has no physical meaning and only represents a computational artifact. Figure 7.17 illustrates the decay as a function of time of the channel charge in the photodetector with two N-type implants. And, Figure 7.18 illustrates the decay as a function of time of the channel charge in the photodetector with single N-type implant. From Figures 7.16, 7.17, and 7.18 we can see that, the decay time, $t_{1.0\%}$, defined as the time when the photodetector channel charge decays to 1% of its original value (99% of the photodetector channel charge is transferred to BCCD charge collection well), is basically independent of the illumination level and depends only on the number of photodetector N-type implants.



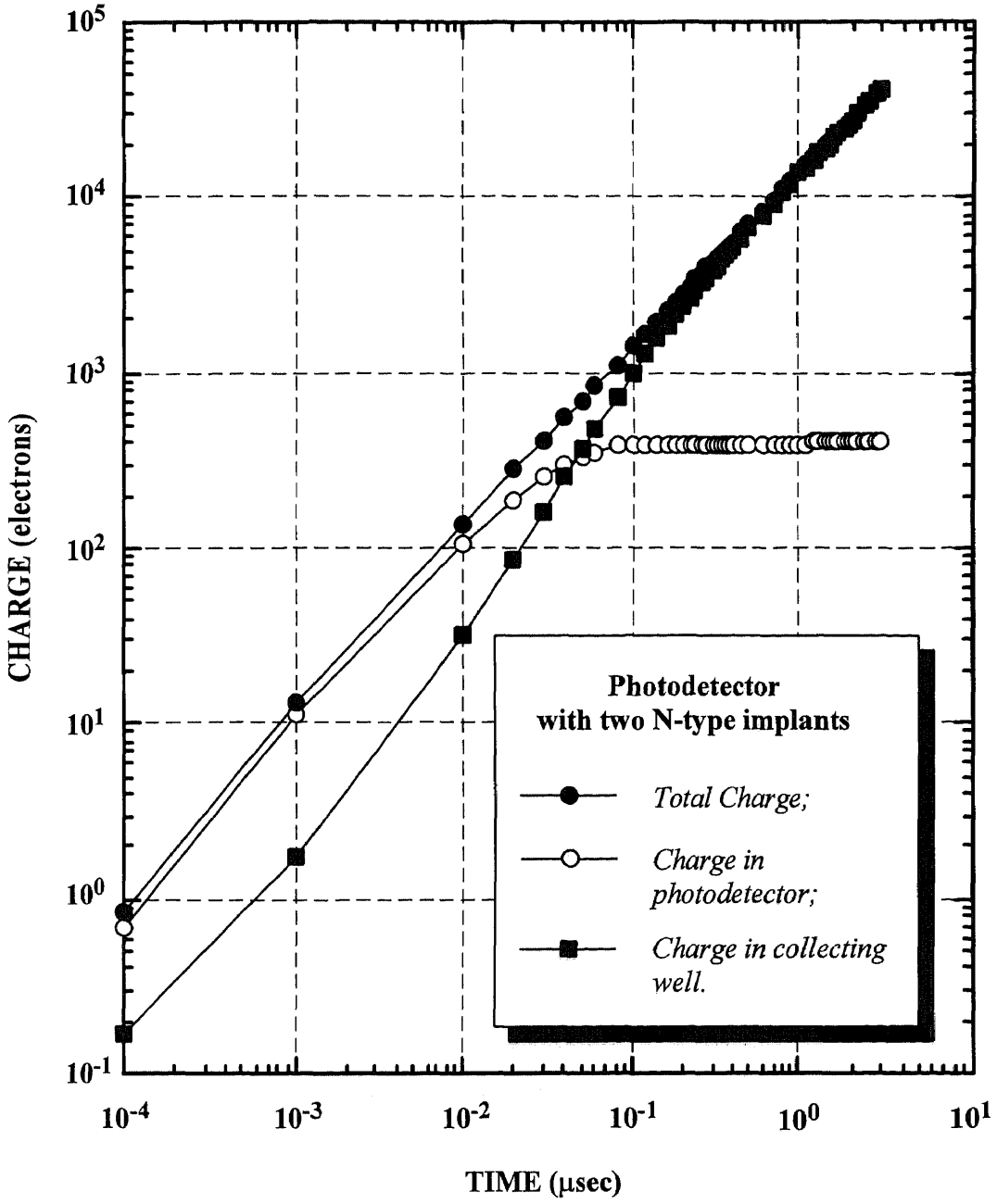
(Illumination intensity: 20,000 electrons in 0.5 μsec)

Figure 7.8 *Time response of the photodetector with two N-type implants to a step illumination corresponding to 20,000 electrons in 0.5 μsec.*



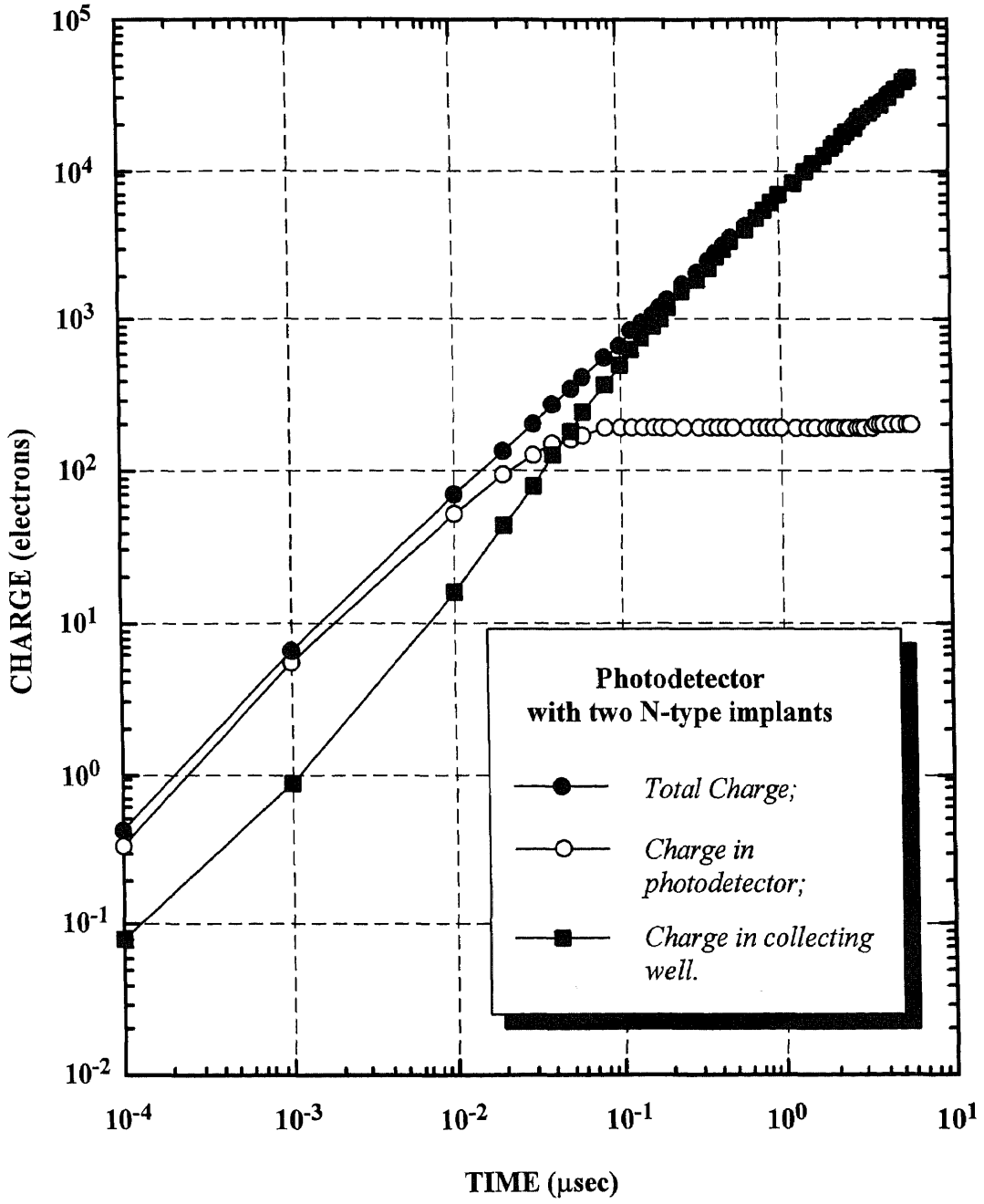
(Illumination intensity: 20,000 electrons in 1.0 μsec)

Figure 7.9 *Time response of the photodetector with two N-type implants to a step illumination corresponding to 20,000 electrons in 1.0 μsec.*



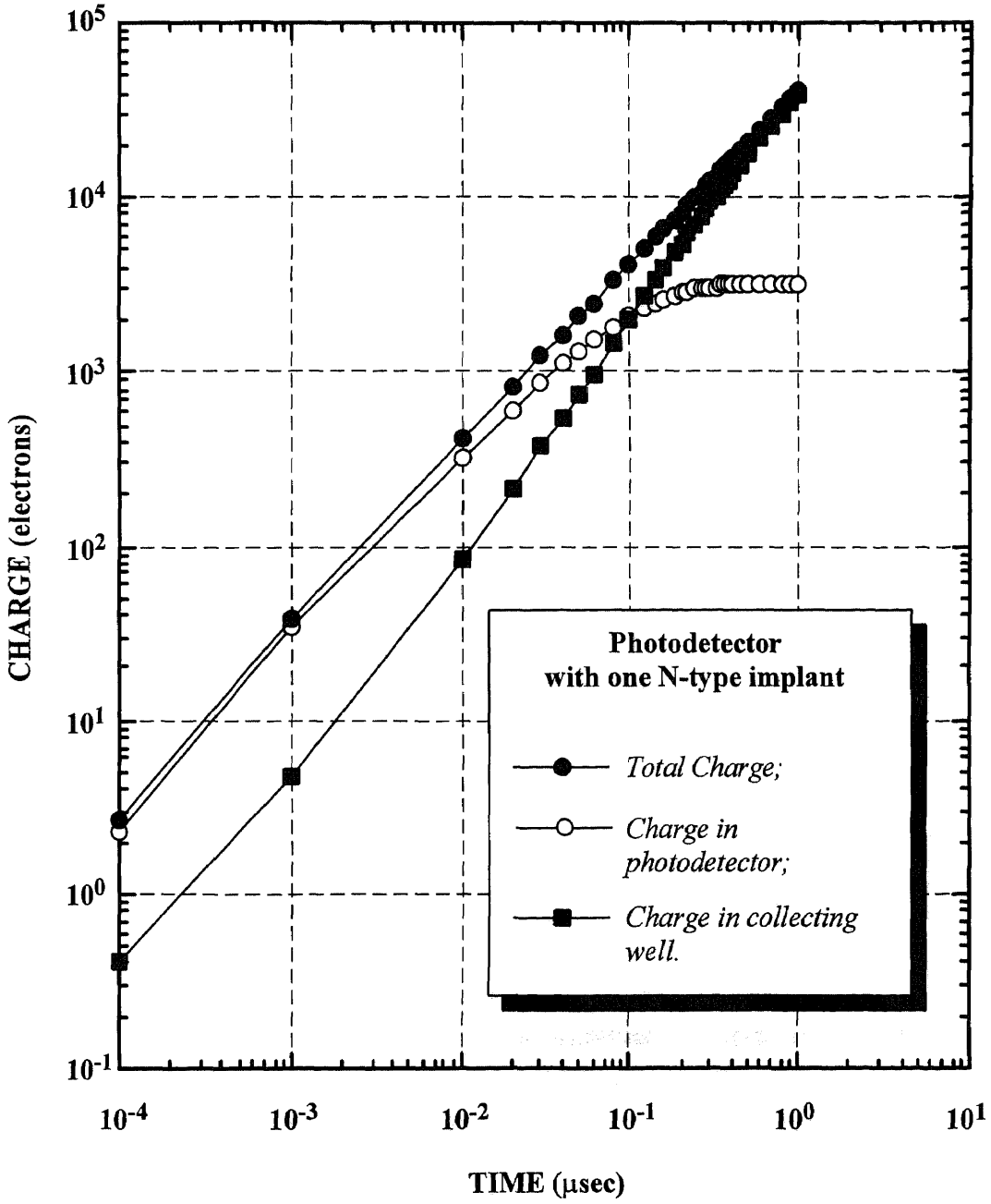
(Illumination intensity: 20,000 electrons in 1.5 μsec)

Figure 7.10 *Time response of the photodetector with two N-type implants to a step illumination corresponding to 20,000 electrons in 1.5 μsec.*



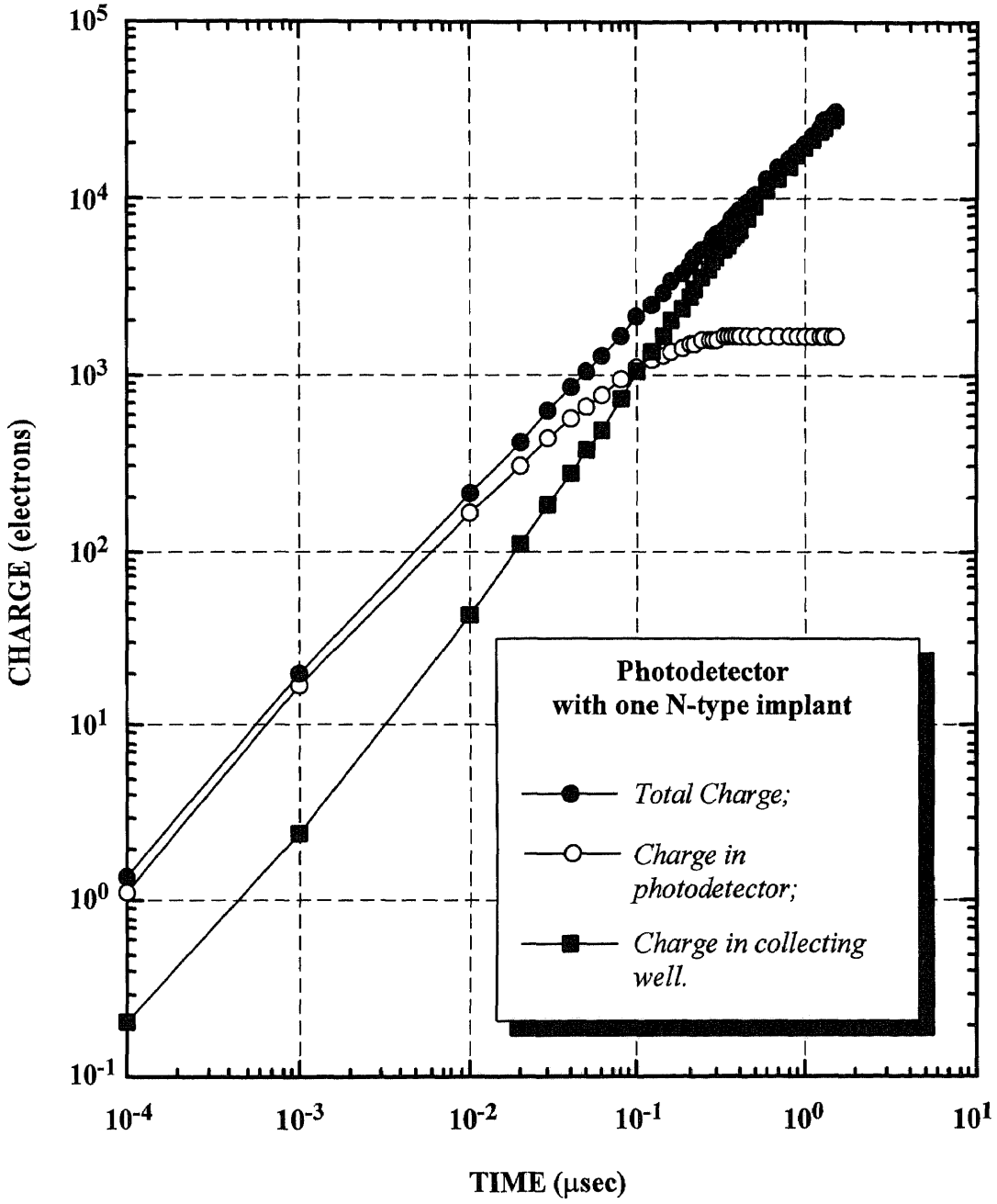
(Illumination intensity: 20,000 electrons in 3.0 μsec)

Figure 7.11 *Time response of the photodetector with two N-type implants to a step illumination corresponding to 20,000 electrons in 3.0* μsec.



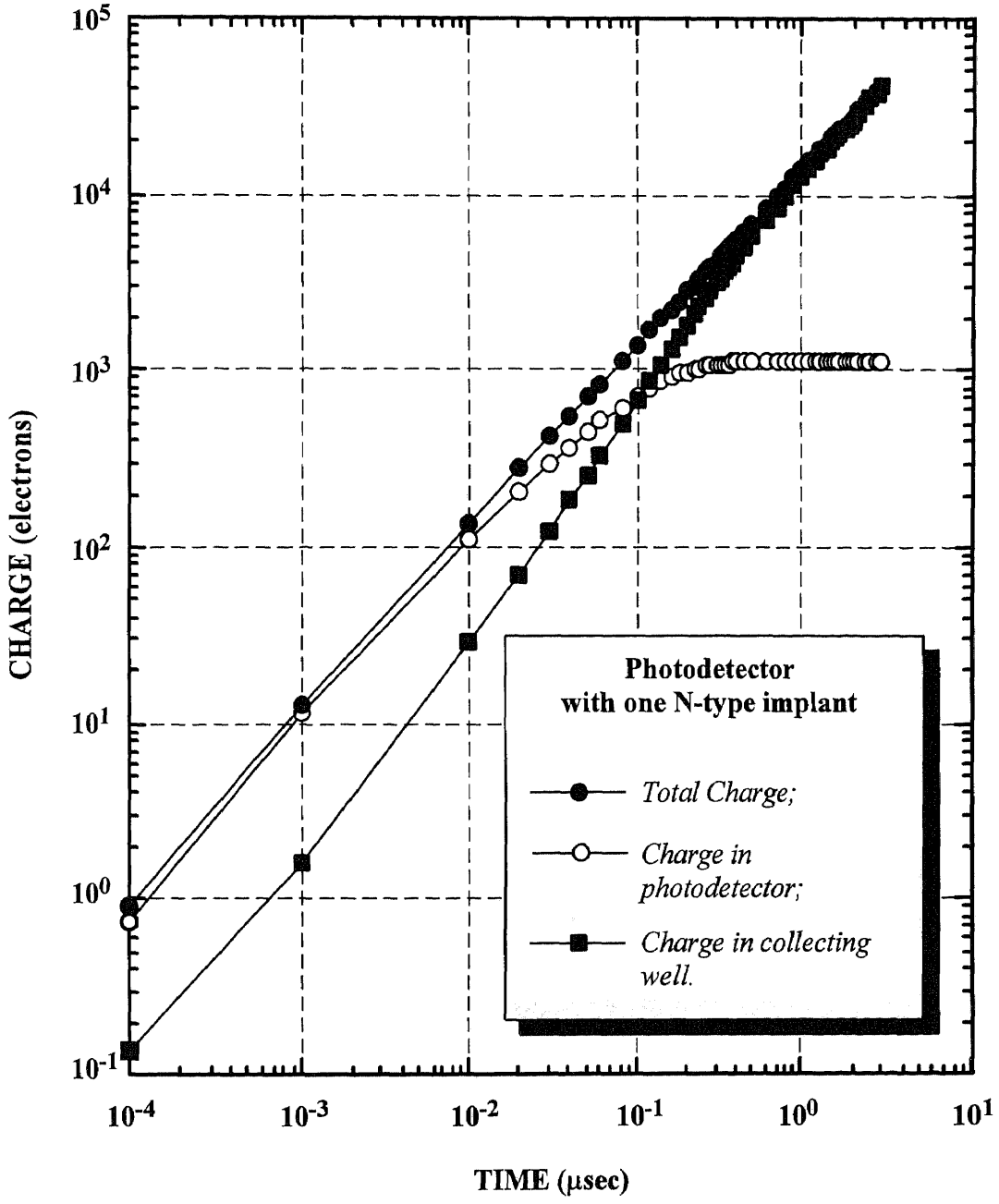
(Illumination intensity: 20,000 electrons in 0.5 μsec)

Figure 7.12 *Time response of the photodetector with single N-type implant to a step illumination corresponding to 20,000 electrons in 0.5 μsec.*



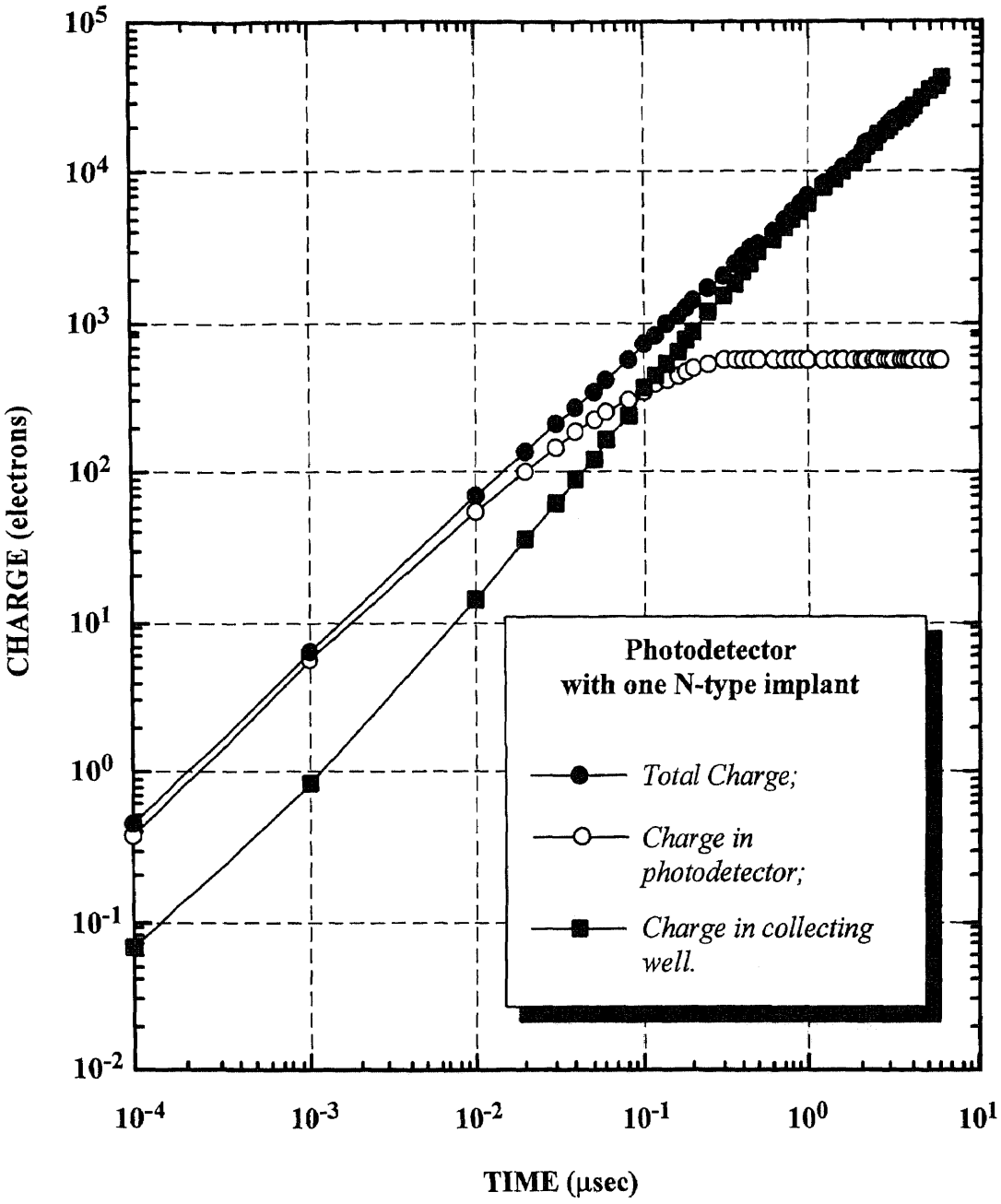
(Illumination intensity: 20,000 electrons in 1.0 μsec)

Figure 7.13 *Time response of the photodetector with single N-type implant to a step illumination corresponding to 20,000 electrons in 1.0 μsec.*



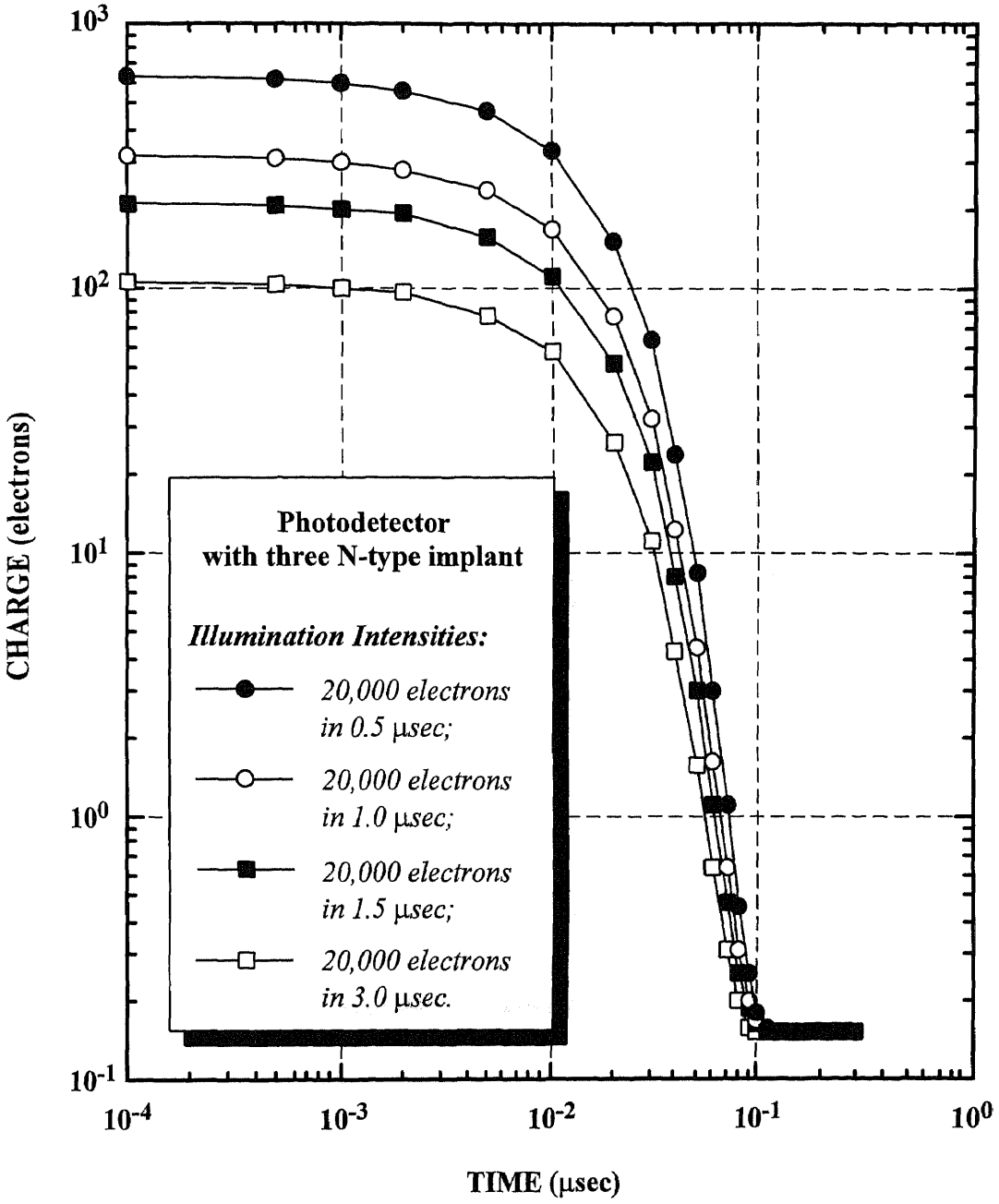
(Illumination intensity: 20,000 electrons in 1.5 μsec)

Figure 7.14 *Time response of the photodetector with single N-type implant to a step illumination corresponding to 20,000 electrons in 1.5 μsec.*



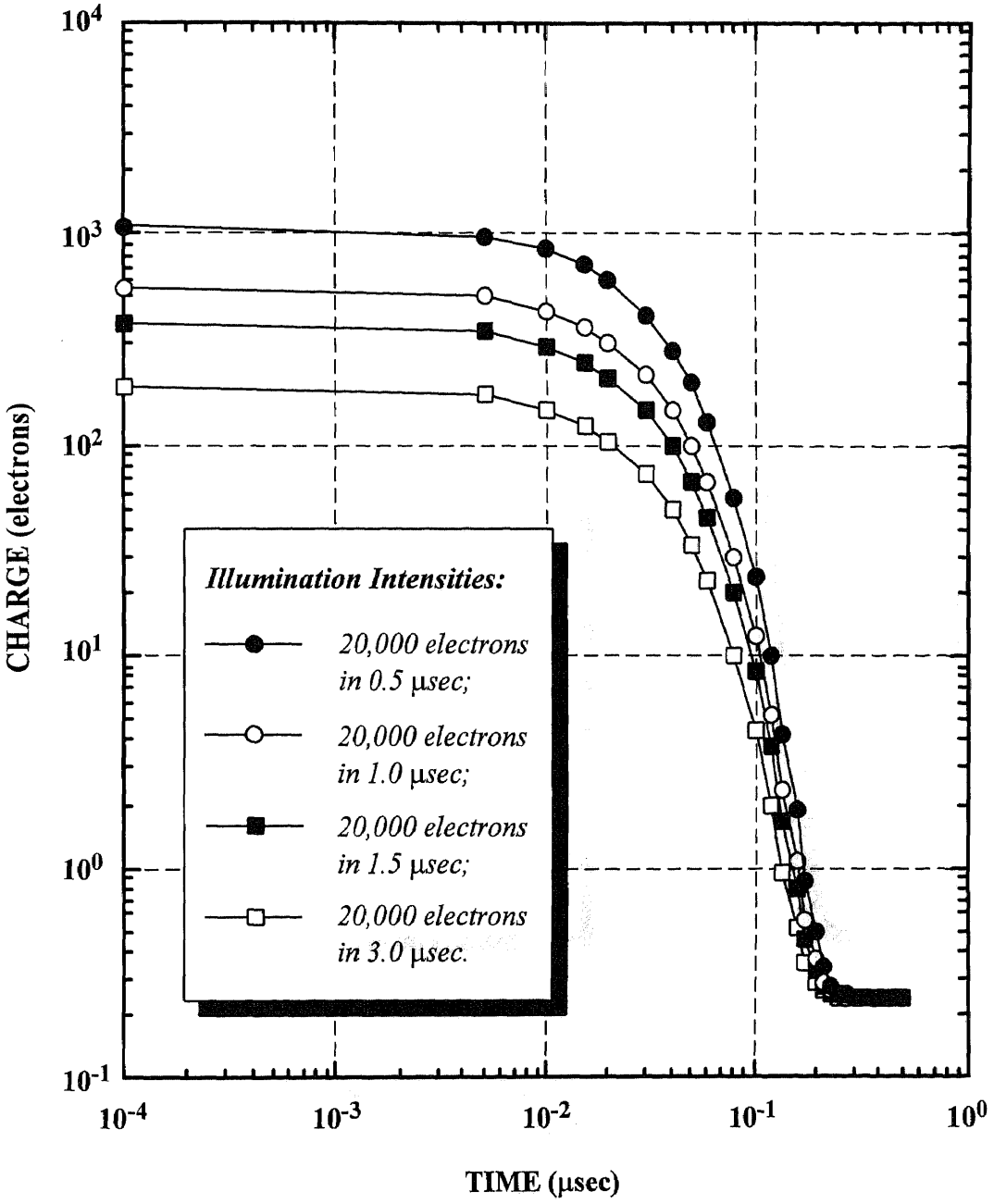
(Illumination intensity: 20,000 electrons in 3.0 μsec)

Figure 7.15 *Time response of the photodetector with single N-type implant to a step illumination corresponding to 20,000 electrons in 3.0 μsec.*



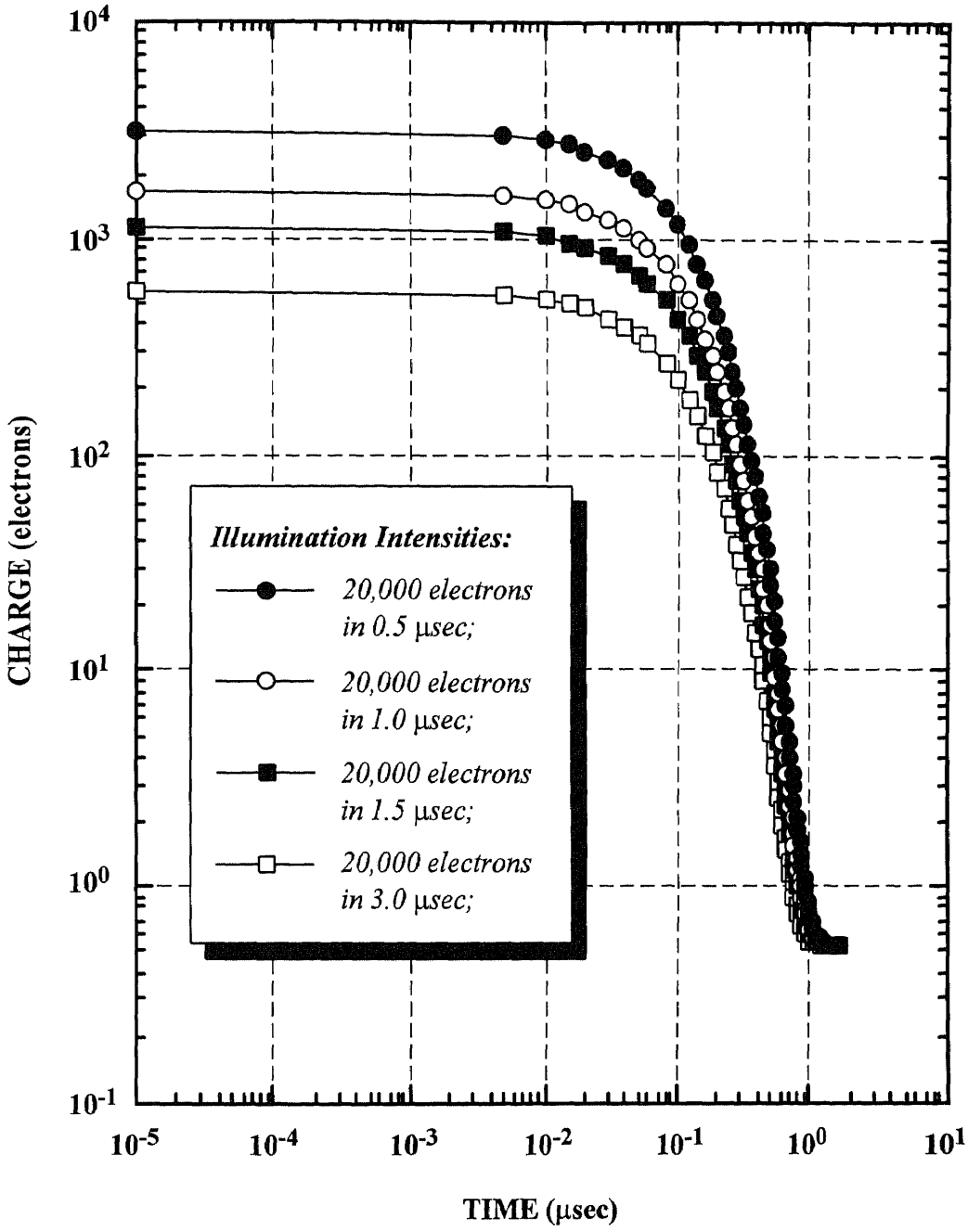
(Photodetector with three N-type implants)

Figure 7.16 *Decay of the channel charge in the photo-detector with three N-type implants for different illumination intensities after the illumination is cut off.*



(Photodetector with two N-type implants)

Figure 7.17 *Decay of the channel charge in the photo-detector with two N-type implants for different illumination intensities after the illumination is cut off.*



(Photodetector with single N-type implants)

Figure 7.18 *Decay of the channel charge in the photo-detector with single N-type implant for different illumination intensities after the illumination is cut off.*

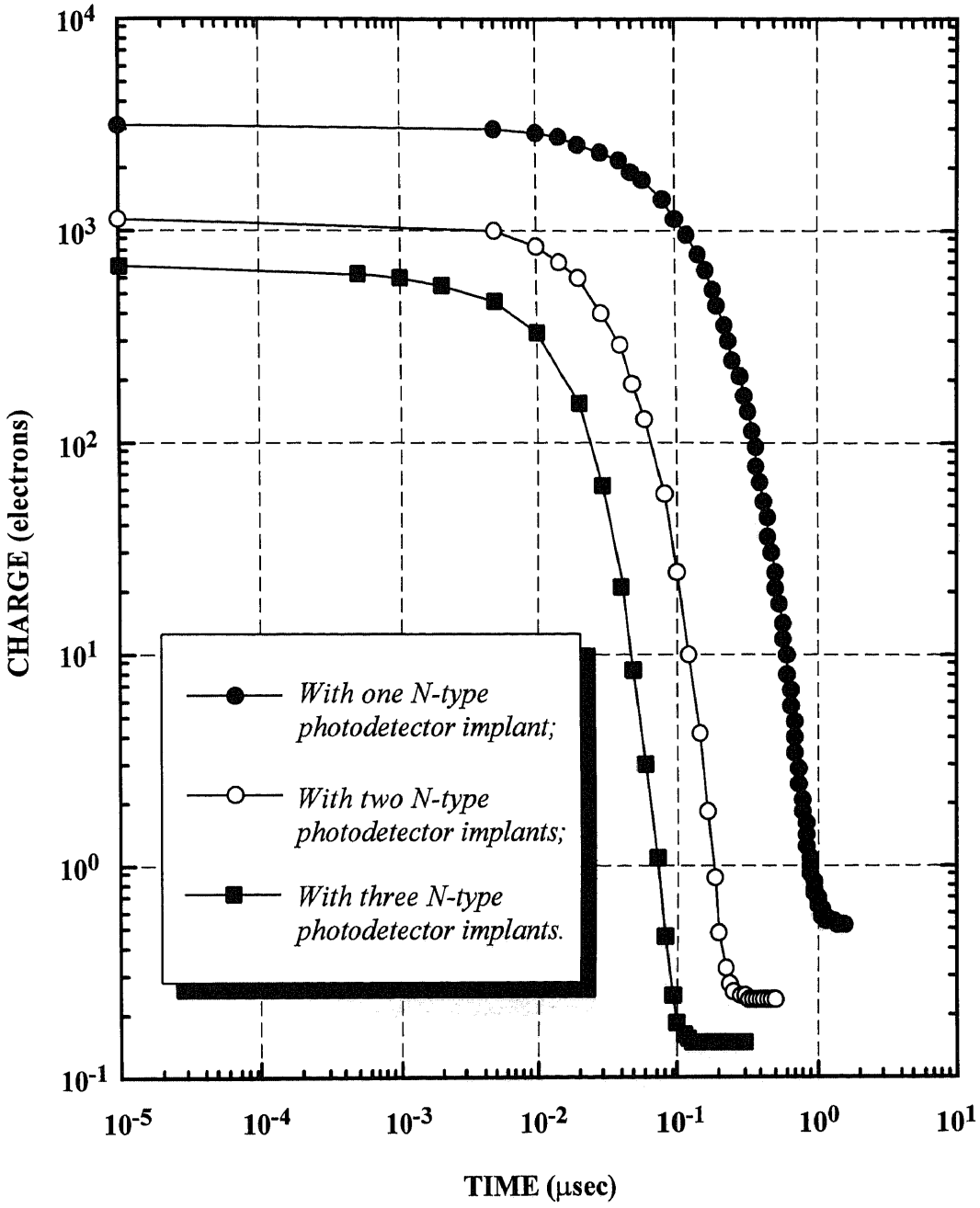
The comparison of the photodetector channel charge decay for fixed illumination intensity for photodetectors with one, two, and three N-type implants are shown in Figures 7.19, 7.20, 7.21, and 7.22 for illumination intensities that result in integration of 20,000 electrons in 0.5, 1.0, 1.5 and 3.0 μsec, respectively. An inspection of these figures also indicates that when photodetector with three N-type implants is capable of transferring 99% of its channel charge to BCCD charge collection well in about 0.055 μsec, the corresponding time for the photodetector with two and single N-type implants is about 0.12 μsec and 0.48 μsec, respectively.

7.4 Summary of Simulation Results

Table 7.1 summarizes the simulation results of the time response for the 30-μmx11-μm photodetector to step illumination corresponding to total detected signal charge of 20,000 electrons for illumination time of 0.5, 1.0, 1.5, and 3,0 μsec. This table shows the maximum length of the N-type implant, ΔL^{Max}, the response time, $t_{99\%}$ as function of the number of N-type photodetector implants, M. This table also shows the simulated values of the steady-state saturation photodetector channel charge, Q_{SS}, as function of the number of photodetector N-type implants (M) and illumination level corresponding to a detected signal charge of 20,000 electrons in 0.5, 1.0, 1.5, and 3.0 μsec.

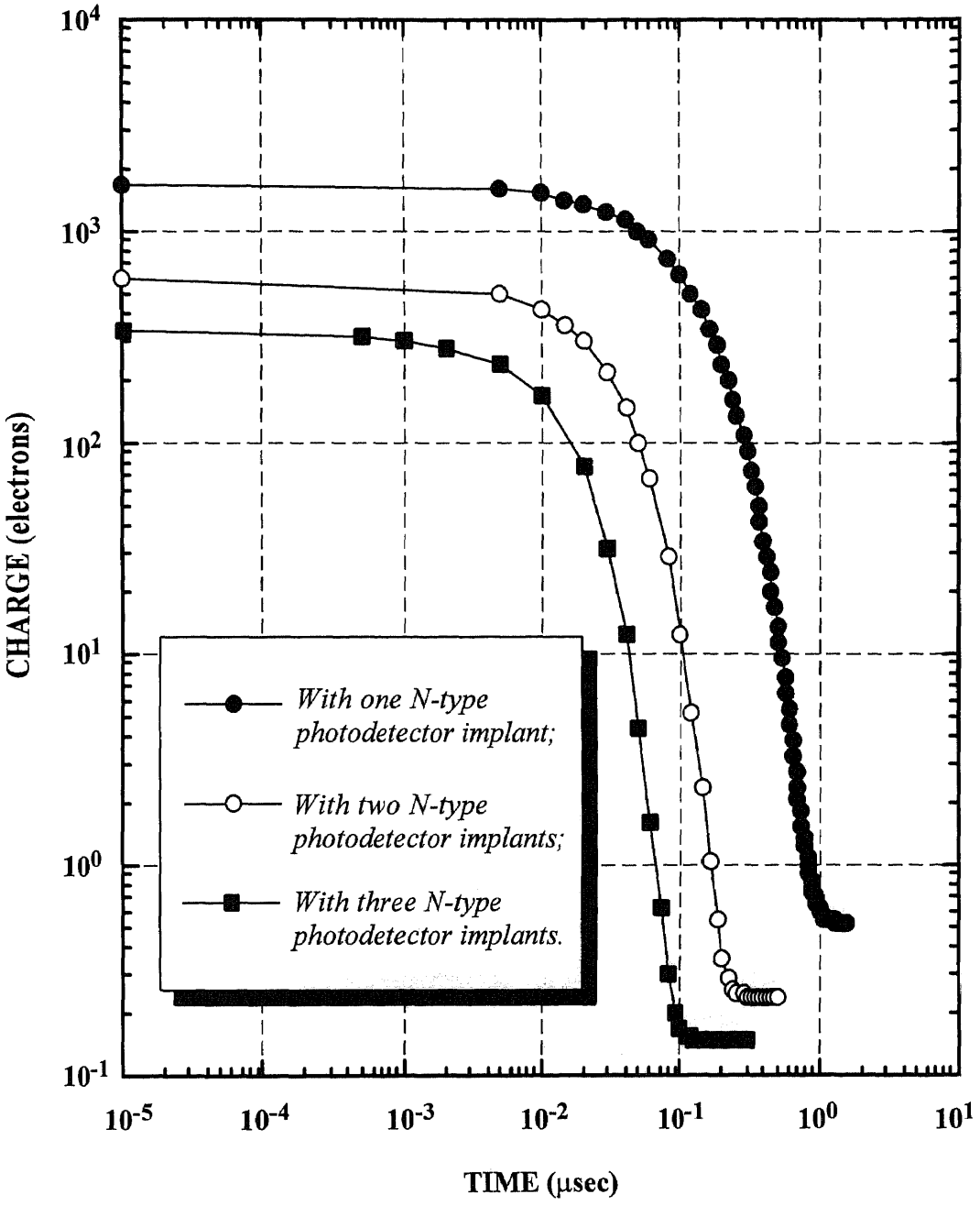
Similar simulation results for a large (about 65-μmx35-μm) photodetector described in Appendix C are shown in Table 7.2 for one (M = 1), two (M = 2), three (M = 3), four (M = 4), five (M = 5), six (M = 6), and seven (M = 7) photodetector N-type implants.

At this point, it should be noted that according to the simulation results presented in Section 7.3.1, the response time appears to be only a function of the detector structure (number of photodetector N-type implants M) and independent of the illumination intensities.



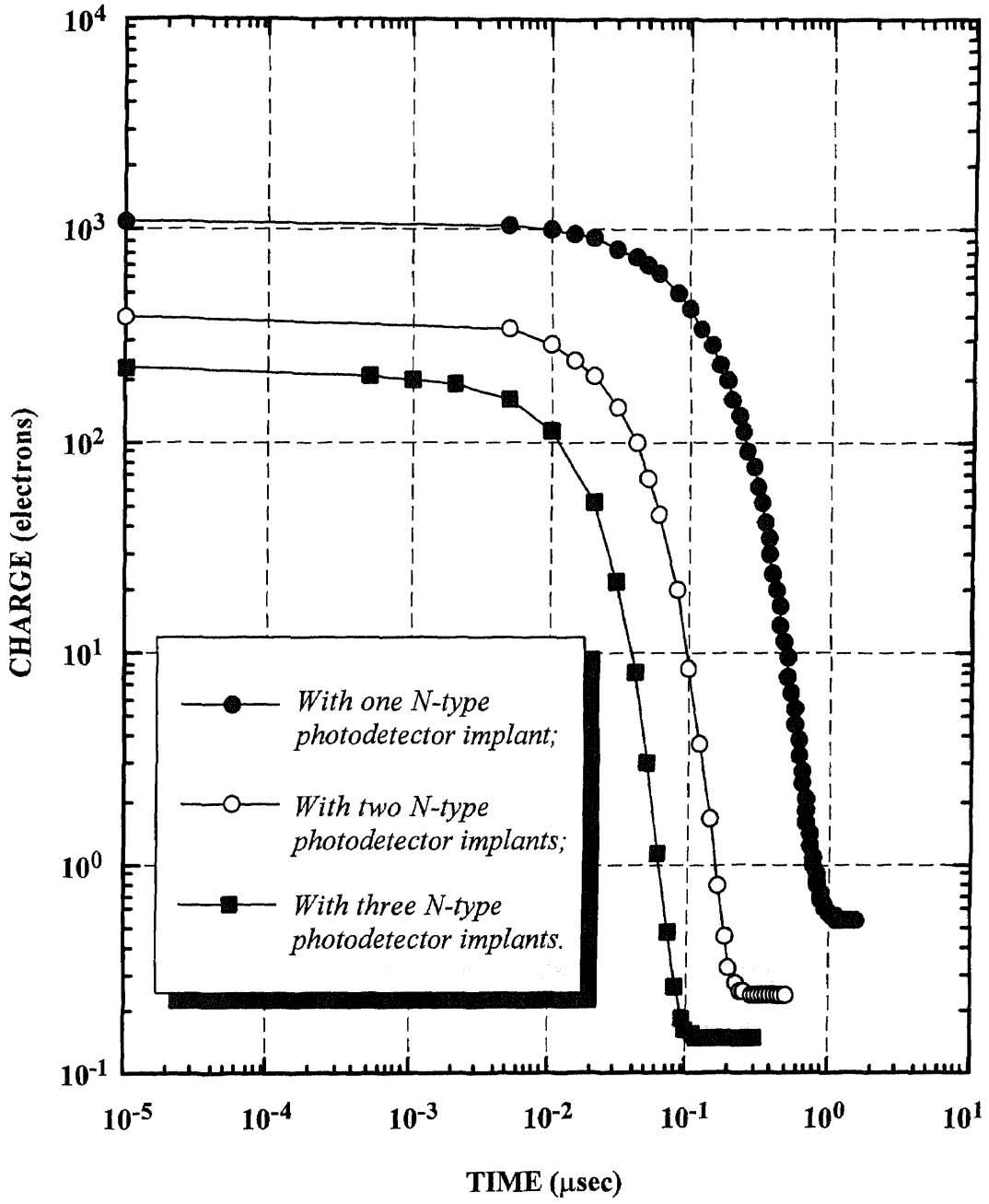
(Illumination intensity: 20,000 electrons in 0.5 μsec)

Figure 7.19 *Comparison of the decay of the channel charge in the photodetector with one, two, and three N-type implants after the illumination which is corresponding to 20,000 electrons in 0.5 μsec is cut off.*



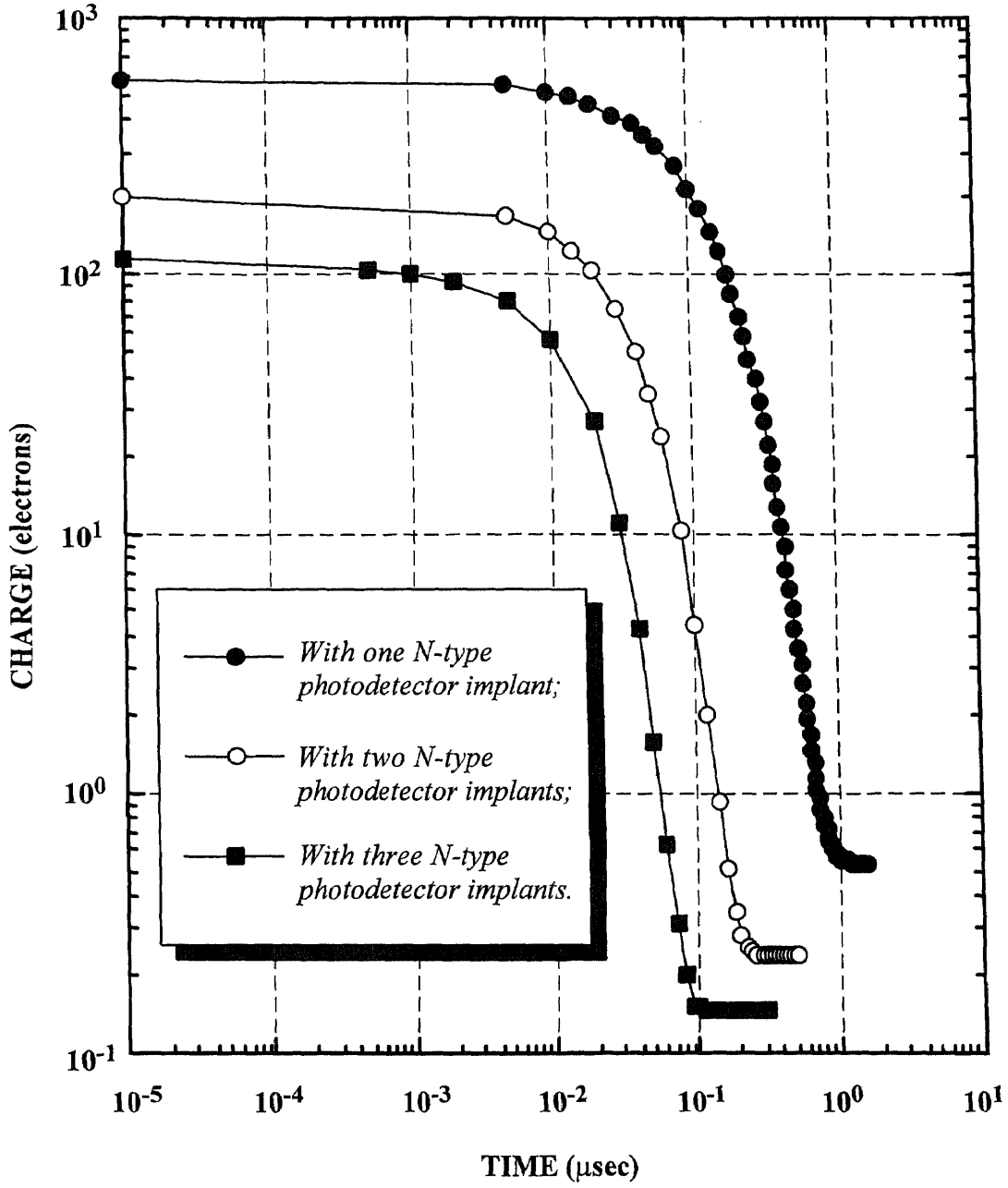
(Illumination intensity: 20,000 electrons in 1.0 μsec)

Figure 7.20 *Comparison of the decay of the channel charge in the photodetector with one, two, and three N-type implants after the illumination which is corresponding to 20,000 electrons in 1.0 μsec is cut off.*



(Illumination intensity: 20,000 electrons in 1.5 μsec)

Figure 7.21 *Comparison of the decay of the channel charge in the photodetector with one, two, and three N-type implants after the illumination which is corresponding to 20,000 electrons in 1.5 μsec is cut off.*



(Illumination intensity: 20,000 electrons in 3.0 μsec)

Figure 7.22 *Comparison of the decay of the channel charge in the photodetector with one, two, and three N-type implants after the illumination which is corresponding to 20,000 electrons in 3.0 μsec is cut off.*

Table 7.1 *Steady-state photodetector channel charge (Q_{SS}), photodetector response time ($t_{99\%}$), maximum length of photodetector segments (ΔL^{Max}), number of photodetector N-type implants (M) for illumination levels corresponding to 20,000 electrons in 0.5 μsec, 1.0 μsec, 1.5 μsec, and 3.0 μsec.*

M	ΔL^{Max} (μm)	$t_{99\%}$ (μsec)	Steady-State Photodetector Channel Charge Q_{SS} (electrons) for illumination intensities of 20,000 electrons in			
			0.5 μsec	1.0 μsec	1.5 μsec	3.0 μsec
1	33.0	0.4	3,220	1,670	1,130	580
2	16.5	0.1	1,160	590	400	200
3	11.0	0.05	630	320	210	110

The decay time of the photodetector channel charge as function of number of photodetector N-type implants (M) for the 30-μmx11-μm and 65-μmx35-μm photodetectors are shown in Table 7.3. This table also shows the maximum length of photodetector N-type implant, ΔL^{Max}, corresponding to number of photodetector implants. The decay time, $t_{1.0\%}$, represents the time for photodetector channel charge reaching 1.0% of its initial value. Similarly to the response time ($t_{99\%}$) shown in Tables 7.1 and 7.2, the decay time ($t_{1.0\%}$) in Table 7.3 is also independent of the illumination intensities. The fact that values of the corresponding decay time are about 20% larger than the response time implies a presence of some self-induced drift field at large signal levels during the response time.

Table 7.2 *Steady-state detector channel charge (Q_{SS}) in large photodetector, photodetector response time ($t_{99\%}$), maximum length of photodetector segments (ΔL^{Max}), number of photodetector N-type implants (M) for illumination levels corresponding to 20,000 electrons in 0.5 μsec, 1.0 μsec, and 2.0 μsec.*

M	ΔL^{Max} (μm)	$t_{99\%}$ (μsec)	Steady-State Photodetector Channel Charge Q_{SS} (electrons) for illumination intensities of 20,000 electrons in		
			0.5 μsec	1.0 μsec	2.0 μsec
1	78.0	3.0	23810	11,910	6,080
2	72.0	2.4	18,060	9,030	4,600
3	36.0	0.7	7,460	3,820	1,940
4	24.0	0.35	4,400	2,240	1,130
5	18.0	0.25	2,650	1,340	670
6	14.4	0.15	1,690	850	430
7	12.0	0.1	1,100	550	280

7.5 Channel Charge Decay Model

Analysis of the simulation results showed that the charge drift induced by fringing fields in the graded multi-implant high-speed photodetectors was sufficiently large in comparison to the thermal diffusion only in the vicinity of the multi-implant boundaries. Furthermore, the analysis of the simulation results summarized in Tables 7.1, 7.2, and 7.3 suggests that due to the fringing fields between the implanted regions of the photodetector, the effective length of the implanted regions, ΔL_{Eff}, should be approximately 3.4 μm shorter than the actual length, ΔL. The actual length of the implant region and corresponding effective length due to the fringing field are illustrated in Figure 7.23.

Table 7.3 *Charge decay time ($t_{1.0\%}$), maximum length of photodetector segments (ΔL^{Max}), number of photodetector N-type implants (M) for small and large photodetectors.*

	M	ΔL^{Max} (μm)	$t_{1.0\%}$ (μsec)
Small Photodetector (30-μmx11-μm)	1	33.0	0.48
	2	16.5	0.12
	3	11.0	0.055
Large Photodetector (65-μmx35-μm)	1	78.0	3.8
	2	72.0	3.0
	3	36.0	0.88
	4	24.0	0.46
	5	18.0	0.28
	6	14.4	0.18
	7	12.0	0.12

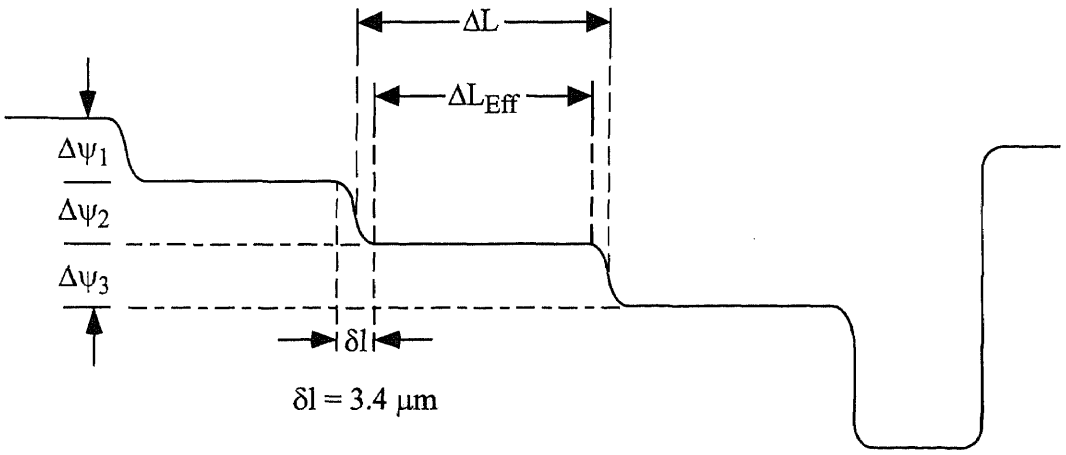


Figure 7.23 *Potential profile of empty photodetector with three N-type implants. The effective length of constant potential segments is about 3.4 μm shorter than the actual length of implant mask.*

To describe the photodetector channel charge decay, a thermal diffusion model is proposed. According to this model, the actual photodetector with M N-type detector implants is made up of M constant potential regions each with an effective length, ΔL_{Eff}, separated by a potential step of about 0.5 V. The more positive potential regions act as successive sinks for the less positive potential regions. Thus, the effective photodetector channel charge decay time can be estimated as the thermal diffusion decay time for the longest constant potential region (with effective length of ΔL_{Eff}^{Max}) plus an effective charge transfer time between these regions.

As shown by Equation (2.12), the photodetector charge decay in the longest constant potential region coupled to charge sink can be described as:

$$Q_n(t) = \frac{8}{\pi^2} \cdot Q_n(0) \cdot e^{-\frac{\pi^2 \cdot D_n \cdot t}{4 \cdot (\Delta L_{Eff}^{Max})^2}}, \tag{7.1}$$

where, $D_n = (kT/q) \cdot \mu_n$ is the electron diffusion constant and μ_n is the electron mobility. The electrons in the buried channel photodetector are moving in the N-region underneath the top P^+ layer, the doping level of the N-region is in the order of 10^{17} cm^{-3}. At room temperature, the default value of electron mobility in PISCES IIB is 1,000 $cm^2/V \cdot sec$. By using this value of electron mobility, the electron diffusion constant becomes 25.9 cm^2/sec. We can define the charge decay time constant, τ, due to the thermal diffusion as:

$$\tau = \frac{4(\Delta L_{Eff}^{Max})^2}{\pi^2 D_n}, \tag{7.2}$$

or

$$\tau = 1.565 \times 10^{-4} (\Delta L_{Eff}^{Max})^2 \quad \text{in } \mu\text{sec} \tag{7.3}$$

for ΔL_{Eff}^{Max} in μm.

According to Equation (7.1), the photodetector channel charge $Q_n(t)$ will decay to 1.0% of its initial value, i.e. $0.01 Q_n(0)$ in

$$t_{1.0\%}^{(Comp)} = 4.3952\tau \quad . \tag{7.4}$$

This, however, does not take into account the effective transport time of the charge between the constant potential regions. Therefore, the total calculated decay time, $t_{1.0\%}^{CT}$, can be expressed as:

$$t_{1.0\%}^{CT} = t_{1.0\%}^{(Comp)} + (M-1)\tau_t \ , \tag{7.5}$$

where τ_t is the effective charge transport time. As will be illustrated in Table 7.4, the value of τ_t can be approximated by the thermal diffusion time constant τ.

Table 7.4 compares the simulated charge decay time to 1.0% of the original photodetector channel charge, $t_{1.0\%}^{(Simul)}$, and the computed charge decay time to 1.0% of the original photodetector channel charge, $t_{1.0\%}^{(Comp)} = 4.3952\tau$, for effective length, ΔL_{Eff}^{Max}, of the longest constant potential region of the photodetector.

The effective maximum length, ΔL_{Eff}^{Max}, of the constant potential regions in the third column was used for calculations of the thermal diffusion time constant, τ, and charge decay time, $t_{1.0\%}^{(Comp)}$. The effective maximum lengths, ΔL_{Eff}^{Max}, for M = 1 in the case of small (30-μmx11-μm) photodetector, and M = 1 and M = 2 in the case of large (65-μmx35-μm) photodetector were estimated by assuming that the photodetector channel charge decay following Equation (7.1). In the above cases, the photodetector is represented by a single constant potential channel. It should be noted that because of detector construction for large photodetector with M = 2, the narrow constant potential region next to the charge collecting well is only 6.0 μm long. The effective maximum lengths, ΔL_{Eff}^{Max}, for M ≥ 2 for the small photodetector and for M ≥ 3 for the large photodetector were estimated as 3.4 μm shorter than the corresponding actual implant mask length, ΔL^{Max}.

The last column in Table 7.4 shows to what accuracy the total effective transport time, $(M-1)\tau_t$, [see Equation (7.5)], can be approximated by (M–1) times the thermal

Table 7.4 *Comparison of the simulated charge decay time, $t_{1.0\%}^{(Simul)}$, the computed charge decay time, $t_{1.0\%}^{(Comp)}$, for effective maximum length, ΔL_{Eff}^{Max}, of the photodetector constant potential region.*

	M	ΔL^{Max} (μm)	ΔL_{Eff}^{Max} (μm)	$t_{1.0\%}^{(Simul)}$ (μsec)	$t_{1.0\%}^{(Comp)}$ (μsec)	$M-1=\frac{t_{1.0\%}^{(Simul)}-t_{1.0\%}^{(Comp)}}{\tau}$
Small Photodetector (30-μmx11-μm)	1	33.0	26.4	0.48	0.48	0
	2	16.5	11.8	0.12	0.0958	1.11
	3	11.0	7.6	0.055	0.0397	1.69
Large Photodetector (65-μmx35-μm)	1	78.0	74.3	3.8	3.8	0
	2	72.0	66.0	3.0	3.0	0
	3	36.0	32.6	0.88	0.731	0.90
	4	24.0	20.6	0.46	0.292	2.53
	5	18.0	14.6	0.28	0.147	4.00
	6	14.4	11.0	0.18	0.0832	5.11
	7	12.0	8.6	0.12	0.0509	5.97

diffusion time constant τ. The last column in Table 7.4 estimates the value of M–1 from Equation (7.5) as:

$$M-1=\frac{t_{1.0\%}^{(Simul)}-t_{1.0\%}^{(Comp)}}{\tau}. \qquad (7.6)$$

Inspection of the last column in Table 7.4 shows, the above model is consistent with expected results for M = 5, 6, and 7 for the large photodetector. However, further requirements are needed to account for the edge effect in the case of small number of M regions.

7.6 Photodetector Readout

As described in Chapter 5, the construction of the VHFR burst-image sensor is using the gate dielectric in the form of Si_3N_4 layer on top of SiO_2 layer. In this case, the bird's beak effect associated with the lifting of the edge of the polysilicon during thermal oxidation to form inter polysilicon insulator oxide can be avoided in the BCCD register region and the CCD charge transfers can be obtained with very high charge transfer efficiency. However, the bird's beak effect can not be avoided in the region connecting the charge collecting well and the photodetector. It should be noted that, shallow P-type implant self-aligned to the charge collecting gate is placed on the top of photodetector to complete the pinned-buried photodetector structure. Considering the side diffusion of the boron and phosphorus, the photodetector N-type implants and the P^+ top layer are extended to under the edge to the charge collecting gate. According to our simulations, the combination of the lateral diffusion of photodetector N-type implants, the bird's beak effect, and the photodetector P^+ top layer extension result in a potential barrier for the charge transfer from photodetector to the charge collecting well.

As shown in Figure 7.24, the photodetector implants are processed after all the polysilicon gates are formed. During chip fabrication, in the photodetector region, the SiO_2-Si_3N_4 layer is etched to the silicon surface. Then a thin screen oxide layer (125Å) is grown for the additional phosphorous photodetector N-type implants. Then, the photodetector region is etched again to the silicon surface and another screen oxide layer is grown for the shallow boron implant. Thus, the growth of the screen oxides results in a lift-up of polysilicon at the edge of the charge collecting gate. The lateral diffusion of phosphorus photodetector N-type implants and the lift-up polysilicon at the edge of the collecting gate cause the Si-SiO_2 interface in the photodetector region to be lower than that under charge collecting gate. Finally, the shallow boron layer is self-aligned implanted to the charge collecting gate. After the thermal diffusion following the photodetector shallow P^+ implant, the boron will also diffuse laterally and be extended

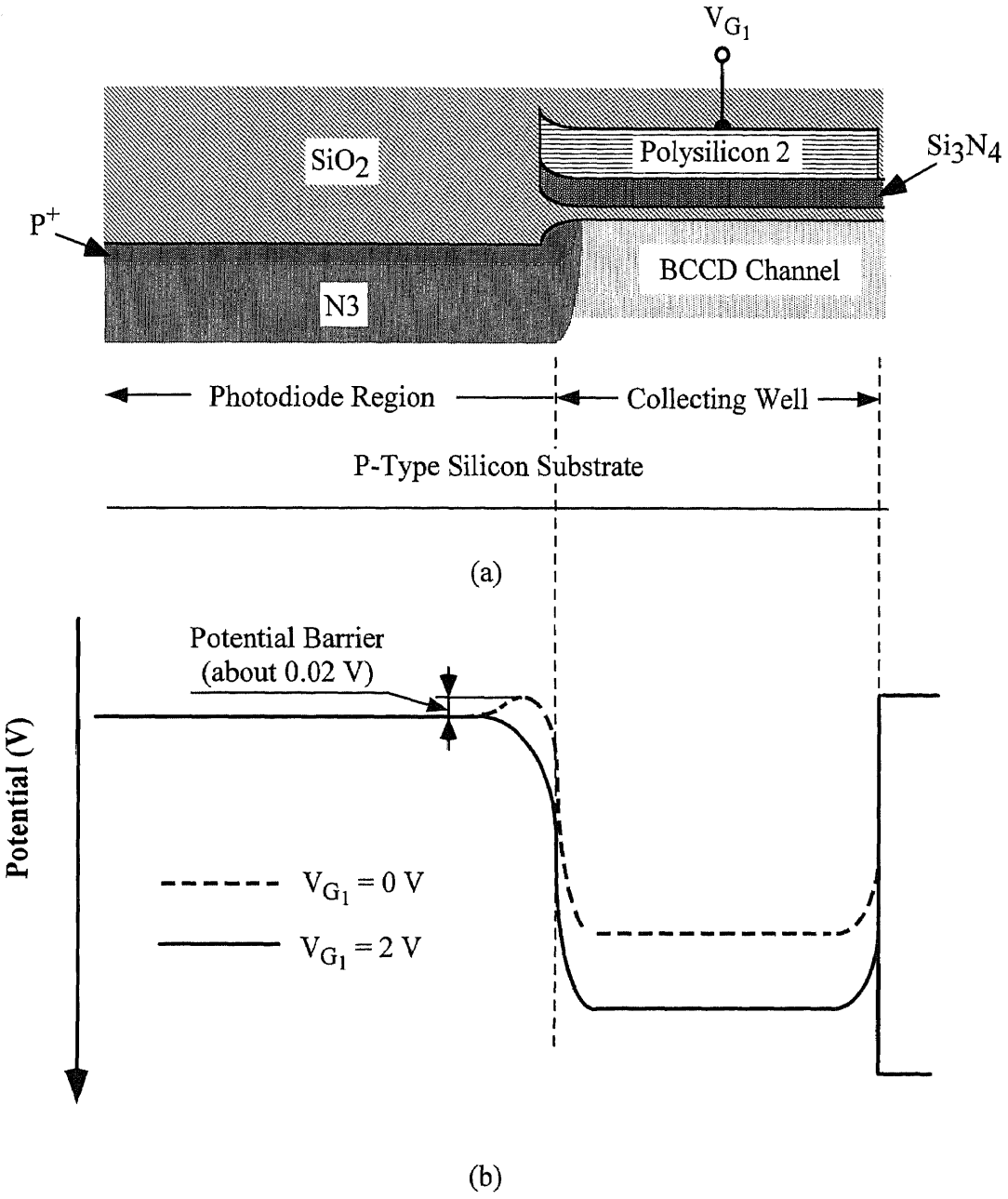


Figure 7.24 *The lift-up (bird's Beak) of silicon dioxide and lateral diffusion of photodetector phosphorus and boron implants in (a) and potential distribution in the edge of collecting gate in (b).*

under the edge of the charge collecting gate. The presence of the bird's beak effect and the lateral diffusion of the implanted phosphorus and boron have been demonstrated using 2-D process simulation by SUPREM IV. The cross-sectional view of the detector/collecting-gate structure and the corresponding potential diagram simulated by PISCES IIB are shown in Figures 7.24(a) and 7.24(b), respectively.

As shown in Figure 7.23(b), for the applied gate voltage of $V_{G_1} = 0$ (the ON operating voltage of the BCCD operated in mode A), a potential barrier about 0.02 V is expected in the edge of the charge collecting gate. This small potential is expected to block some of the generated photoelectrons from being transferred out of the photodetector region. Such incomplete transfer can result in a "lag" during the photodetector readout*.

The are two ways to remove the potential barrier in the edge of the collecting well and to eliminate the image lag.

1. As shown in Figure 7.23(b), when a positive voltage is applied to the collecting gate, the potential barrier will disappear due to the fringing field between the photodetector and the collecting gate. The simulation by PISCES IIB shows that, the minimum applied voltage needed to remove the potential barrier for charge collection is approximately +2.0 Volts.
2. As shown in Figure 7.2, the photodetector P^+ top layer is self-aligned to the polysilicon-2 charge collecting gate. If we move the edge of P^+ implant mask a into the photodetector region, the lateral diffusion of boron will be extended under the collecting gate to a less degree than that of a self-aligned P^+ top layer. On the other hand, if the edge of P^+ implant mask is moved further into the photodetector region, the top P^+ layer will not cover the whole photodetector. The simulation by SUPREM

* However, this potential barrier can also be useful isolating the charge collecting well from the photodetector during the readout of the signal charge from the charge collecting well.

IV and PISCES IIB shows that, there will be no potential barrier in the edge of charge collecting gate for the applied gate voltage of $V_{G_1} = 0$ if the edge of P^+ implant mask is moved 0.1 to 0.2 μm into the photodetector region.

CHAPTER 8

CONCLUSIONS

Process Development

A process (described in Chapter 5) was developed for fabrication of 360x360-element Very High Frame Rate (VHFR) burst-image sensor [84] on the bases of simulations of buried-channel CCD (BCCD) structures and high-speed zero-lag pinned-buried photodetectors.

- This imager fabrication process was based on a 3-phase three-level polysilicon one-level metal BCCD process and one-level polysilicon two-level metal 1.5 μm CMOS process available at the David Sarnoff Research Center (Sarnoff). The fabrication process for the VHFR burst-image sensor includes four-level of polysilicon, three-level of metal, eight implants, and requires a total of 21 mask levels.
- A dual dielectric in the form of SiO_2 thermal oxide covered by Si_3N_4 was chosen to avoid the possibility of a reduced charge transfer efficiency (CTE) due to small potential wells associated with the bird's beak effect at the edges of the overlapping polysilicon gates.
- To obtain maximum charge handling capacity with large electric fringing fields that are needed for high CTE operation, on the bases of one-dimensional (1-D) process and device simulations (described in Chapter 6), an Arsenic and Phosphorus dual-implant was selected for BCCD channels. The imager wafer lot was processed with two BCCD implant options. The low BCCD implant option has about the same total dose as the BCCD implants presently used by Sarnoff and the high level BCCD implant has about twice as large total implant dose.

- Simulations by ISE-TCAD software of the multi-layer imager chip topography was found helpful in processing of the dual-layer metal interconnections. After calibration of the glass reflow simulation parameter, good agreement was obtained between SEMs of finished imager wafers and the simulated device cross-sections.

VHFR Burst-Image Sensor Chip

The 360x360-element VHFR burst-image sensor (described in Chapter 4) is capable of capturing images at a frame rate up to 10^6 frames/sec, and continuously storing the last 30 image frames at the BCCD pixel memory. During the image readout, the BCCD pixel memory is reformatted into 4 quadrants of large parallel-serial CCD register with (180x5)x(180x6) storage elements.

- The final design of this imager format was based on one-dimensional (1-D) and two-dimensional (2-D) process and device simulations of BCCD registers (described in Chapter 6) and high-speed zero-lag photodetector (described in Chapter 7).
- The operation of the imager has been illustrated and the waveforms for several operating modes of the imager are described in Chapter 4 and Appendix A.
- Operation of one quadrant of the 360x360-element burst-image sensor was experimentally demonstrated. The experimental results showed that this imager can be operated at maximum frame rate of $1.0x10^6$ frames/sec. The BCCD transfer loss was estimated as less than $3x10^{-6}$ per horizontal transfer and less than $3x10^{-6}$ per vertical transfer.

Simulations of BCCD Performance

1-D and 2-D process and device simulations using SUPREM III and PISCES IIB were used for optimization of the design of the BCCD pixel memory elements of the VHFR burst-image sensor.

The design of the imager involved a trade-off between spatial resolution (number of pixels) and the number of image frames that can be continuously stored at the BCCD pixel memory. For this trade-off the key-element is the charge handling capacity of the BCCD channels representing the maximum charge that can be stored and transferred by the minimum size BCCD pixel memory element. Using 1.5-μm design rules, the minimum stage of the BCCD register was selected to correspond to 3-μm-wide BCCD channels separated by 2.5-μm channel stops and 1.5-μm gates for 3-phase BCCD registers. This results in a minimum BCCD charge storage area of 1.5-μmx3.0-μm and a minimum BCCD register area of 4.5-μmx5.5-μm.

The charge handling capacity of BCCD channel as function of total implant doses and as function of Arsenic-to-Phosphorus ratio was studied by 1-D and 2-D simulation.

- 1-D simulation showed that increasing of Arsenic-to-Phosphorus ratio will increase charge handling capacity of BCCD channel at a fixed gate voltage swing.
- 1-D simulation showed that for operation with 15 V clock voltage swing, the charge handling capacity can be increased by a factor of 2 by reduction of the effective gate oxide thickness from 700 Å to 200 Å to 400 Å depending on the operating mode.
- 2-D simulation showed that the maximum charge handling capacity is reduced by a factor larger than two due to electric fringing field associated with a short BCCD gate length of 1.5-μm.
- 2-D simulation showed that 2.5-μm channel stops which are created by an un-implanted p^- epi layer create a sufficient potential barrier to confine signal charge in the BCCD channels.
- The simulation results showed that the charge handling capacity of the minimum size BCCD storage stage is about 11,800 and 17,200 electrons/pixel for low BCCD implant dose option (arsenic implant dose of $6.5x10^{11}$ cm^{-2} and phosphorus implant dose of $6.5x10^{11}$ cm^{-2}) and high BCCD implant dose option (arsenic implant dose of $1.2x10^{12}$ cm^{-2} and phosphorus implant dose of $1.0x10^{12}$ cm^{-2}), respectively.

- The measured charge handling capacity of the BCCD pixel memory elements for high BCCD implant dose option was found to be 11,000 electrons/pixel for gate voltage swing of 7.4 V. This value is about 35% lower as compared to 17,000 electrons/pixel obtained by 2-D simulation.
- Comparison of measured and simulated channel potentials for polysilicon-1 BCCD elements as function of gate voltage for low and high BCCD implant options showed that the measured value of the pinning gate voltage is 35% lower than the simulated value, and the value of the corresponding measured channel potential is 10% lower than the simulated value.

High-Speed Photodetector

A new concept for large high-speed photodetector with complete charge readout in less than 0.1 μsec was developed and demonstrated.

- The large high-speed photodetector is in the form of a graded three-potential-level pinned-buried BCCD structure that is fabricated by a BCCD channel implant, additional three N-type implants, and a shallow p^+ implant.
- The response of this 33-μm-long high-speed photodetector to pulse illumination obtained by 2-D process and device simulations showed that this photodetector is expected to be applicable for operation essentially without lag (between successive frames) with detector readout time of less than 0.1 μsec.
- Demonstrated operation of one quadrant of the 360x360-element VHFR burst-image sensor with optical test pattern illuminated by 0.4 μsec LED pulses showed that for operation of the imager with frame integration time of 1.0 μsec, the photodetector lag is less than 1.0% assuming zero transfer losses for BCCD readout with 3,240 transfers.

- A model for operation of large high-speed photodetectors was developed on the basis of simulation study of 33-μm-long and 78-μm-long photodetectors with 1 to 3 and 1 to 7 constant potential segments, respectively.
- The decay of the charge stored in the BCCD channel of the high-speed photodetector when the illumination is turned off can be approximated by thermal diffusion decay of the channel charge corresponding to the longest constant potential segment and the effective charge transport time between the constant potential segments which is equal to the thermal diffusion time constant for these segments.
- 2-D process and device simulations showed that due to the electric fringing field, the effective length of the constant potential segments is about 3.4 μm shorter than the actual length of the implant masks.

CHAPTER 9

SUGGESTIONS FOR FUTURE RESEARCH

On the bases of this dissertation, the suggestions for future simulation work on the Very High Frame Rate (VHFR) burst-image sensor are as follows:

- On the bases of the measured BCCD gate breakdown voltage, the total dose of BCCD dual-implant can be increased up to 3.5×10^{12} $cm^{-2}$to improve the charge handling capacity of the BCCD channel. 1-D and 2-D process and device simulations should be done to optimized the arsenic-to-phosphorus ratio of the BCCD dual-implant to achieve the maximum charge handling capacity and a higher fringing field.
- The large fringing field caused by short gate length will limit the maximum potential of the BCCD well as well as the maximum charge handling capacity. 1-D and 2-D process and device simulations of the maximum charge handling capacity as function of gate length should be done to optimize the minimum gate length in the BCCD register.
- More studies on the charge transport model of the multi-implant pinned-buried photodetector are suggested to get a better understanding of the charge transfer mechanism in the photodetector.
- Commercial version of process and device simulators have the capability of optically generating electrons in a specified device region. The solutions of the SCCD channel stop barrier height and the potential barrier for separation of a full well adjacent to an empty well should be obtained by simulations.
- There are some critical regions that could not be analyzed by 2-D simulation in the designed VHFR burst-image sensor chip. 3-D process and device simulations are needed to fully understand the charge transfer in these regions. These critical regions include:

- whole photodetector region with multiple N-type implants and P^+ top implant;
- photodetector readout structure;
- blooming/dumping drain region; and
- serial-parallel register region.

APPENDIX A

OPERATION OF THE VHFR BURST-IMAGE SENSOR

The signal charge transfer in the macropixels during the frame collection period in Mode-1 and frame readout period is presented in this appendix.

A.1 Charge Collection Period in Mode-1

The clock wave forms of each clock phase for operating the VHFR imager during the frame collecion period in Mode-1 are given in Figure 4.19(a). Figures A.1(a) and (b) illustrute the clock waveforms of this mode during the whole frame colletion period. Figure A.2 shows the signal charge transfer in two vertically adjacent lower-side macropixels at different time which is defined in Figure A.1 during the charge collecting period. The signal charge transfer in upper-side macropixels is the same. The details are given as follows.

- At t = 0, imager start signal collecting.
- At, t = t1, as shown in Figure A.2(a), the 1st signal is being collected under gate G_1, and the blooming control may be achieved through G_2.
- At t = t2, as shown in Figure A.2(b), G_1 as well as G_2 turns OFF and the 1st signal charge transfers from G_1 to G_3.
- At t = t3, as shown in Figure A.2(c), the 1st signal charge transfers from G_3 to S2. During this transfer time, G_1 and G_2 are still kept OFF, until the 1st signal charge transfer in completed.
- At t = t4, as shown in Figure A.2(d), the 1st signal charge has been transferred to under gate S1 from S3, the 2nd signal charge starts transferring into G_3.
- At t = t5, as shown in Figure A.2(e), the first 4 signal charges are transferring from S1 to S2, and the 5th signal charge is transferring from G_3 to S2.

This completes the detection and collection of the first 5 image frames.

- At t = t6, as shown in Figure A.2(f), G_1 turns ON to collect the 6^{th} signal, and the first 5 signal charges are transferring vertically (in parallel) from S2 to P2. At this time, S3 is kept OFF.
- At t = t7, as shown in Figure A.2(g), the first 5 signal charges are transferring vertically from P3 to P1. S3 and S1 was turned ON simultaneously and S3 is turning OFF at this time, the residual charges from P3 of upper macropixel are transferring to gate S1 via S3 of lower macropixel.

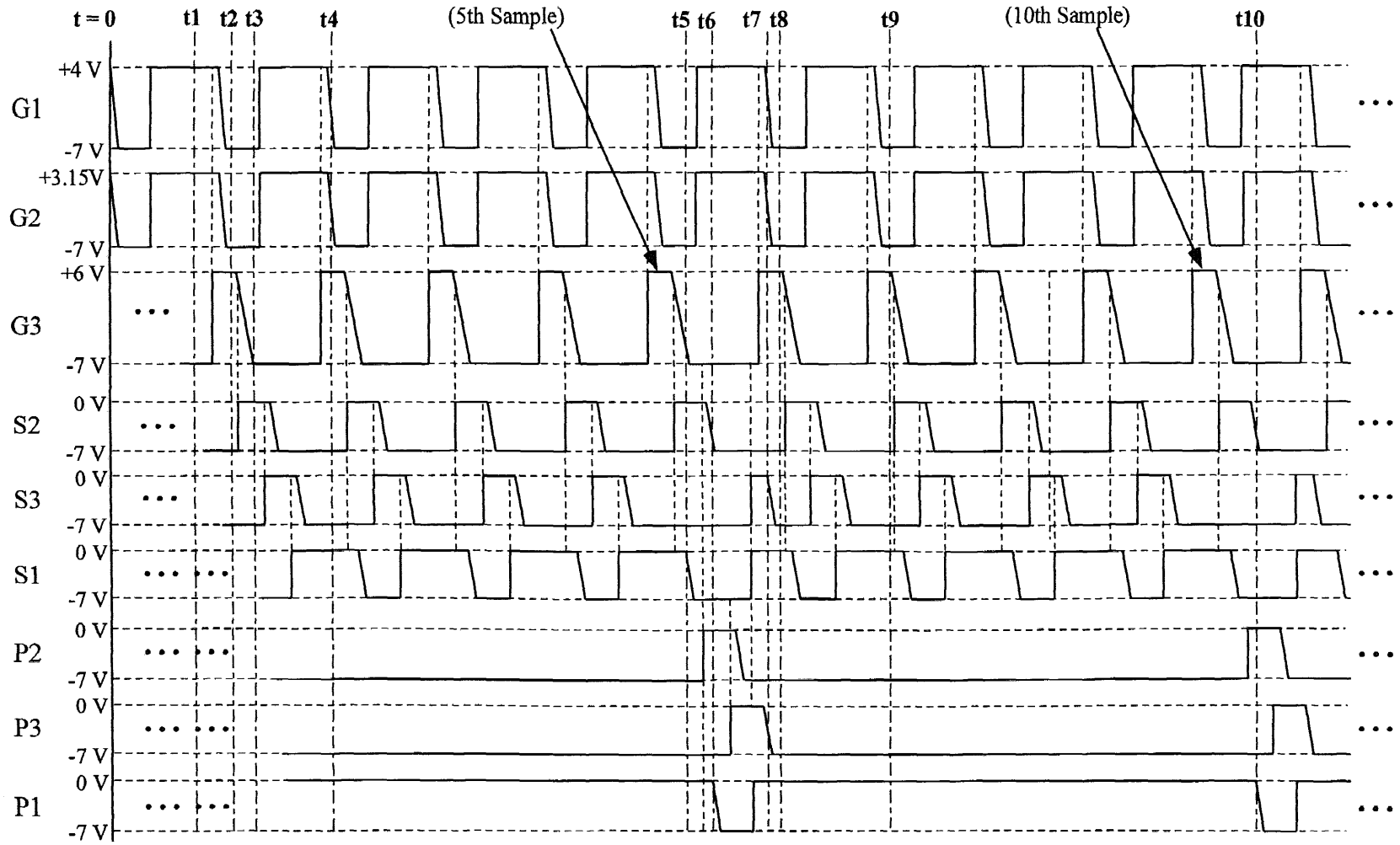
  In the last stage of S1, the residual charge from upper macropixel start to dump out into dumping drain.

  G_3 is turned ON and the 6^{th} signal charge collected under G_1 is transferring into G_3.
- At t = t8, as shown in Figure A.2(h), S3 turns OFF and S1 still keeps ON. all of the residual charges are transferred into S1 and eventually they will be transferred towards the dumping drain. The 6^{th} signal charge has been completely transferred from G_1 into G_3. The first 5 signal charges are completely transferred into P1.
- At t = t9, as shown in Figure A.2(i), the 6^{th} signal charge is transferred from S3 to the first stage of S1 and the 7^{th} signal charge is transferred from from G_1 to G_3.

  The residual charges have been transferred one more stage towards the dumping drain, and one more residual charge has been dumped out. After the 10^{th} signal charge has been transferred to S2, all the residual charges in the serial registers have been dumped out, and the 6^{th} to 10^{th} signal charges are stored under S2 in serial register.
- At t = t10, as shown in Figure A.2(j), the second parallel (vertically) charge transfer starts: the 1^{st} to 5^{th} signal charges are transferring from P1 to P2 and the 6^{th} to 10^{th} signal charges are transferring from S1 (acting as P1) to P2. The 6^{th} to 10^{th} signal charges transfer at this time is exactly same as the 1^{st} to 5^{th} signal charges transfer at t = t6.

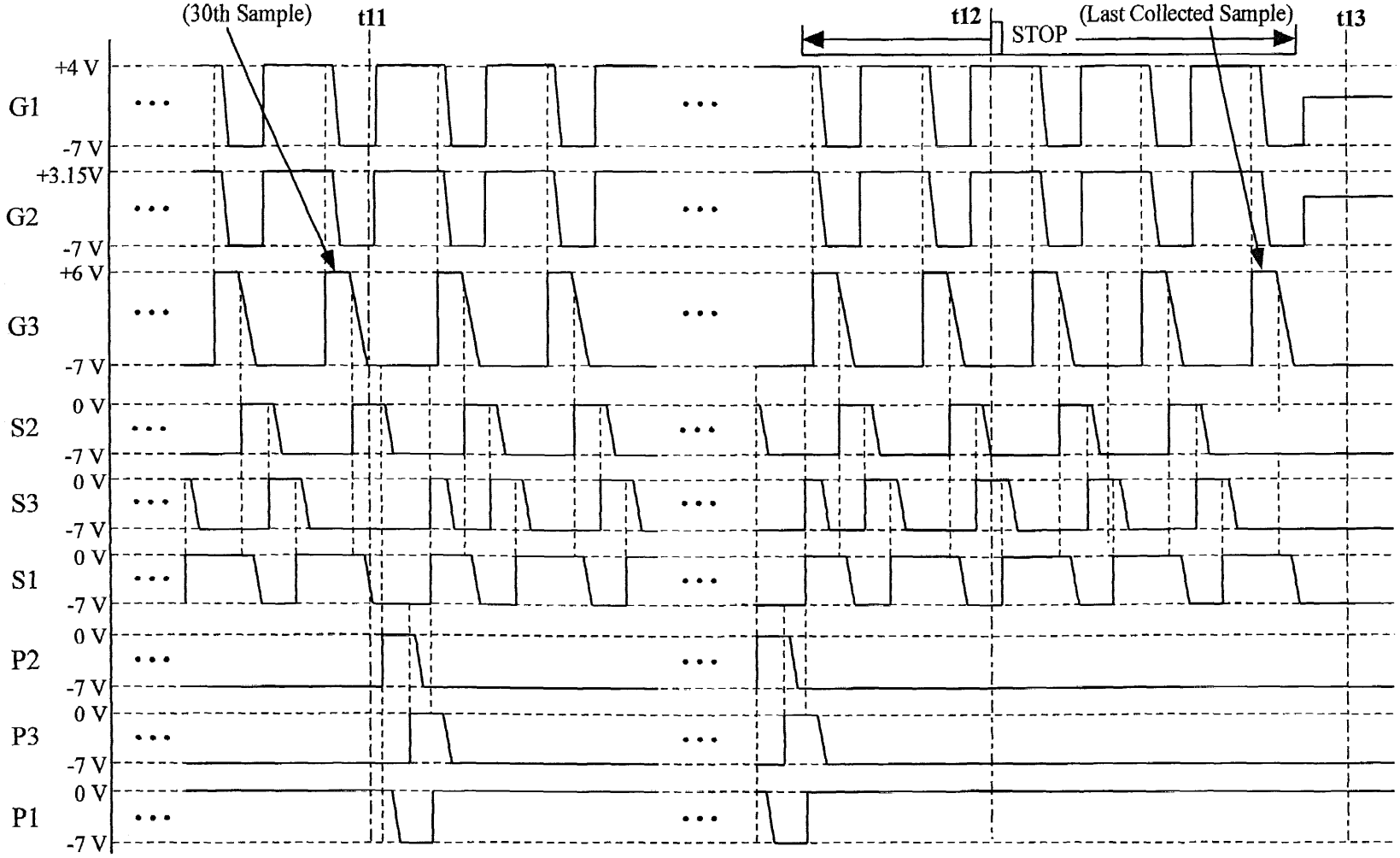
- At t = t11, as shown in Figure A.2(k), after 5 parallel (vertical) charge transfers in parallel registers and 5 additional serial (horizontal) charge transfers in serial registers, the macropixel contains 30 frames of signals. The 1^{st} to 25^{th} signals are stored in P1's, and the 26^{th} to 30^{th} signals are stored in S2's.
- Then, when the image keeps collecting signals (31^{th} to 35^{th}), the first 5 signals are being transferred into serial registers of the vertically adjacent macropixel and are dumped out, as were the residual signals. Therefore, the imager always maintains the most recent 30 frames of signal and keeps dumping older signals.
- At t = t12, imager receives an external "STOP" pulse, to stop the frame collection period and to initiate the frame readout period. AS shown in Figure A.2(l), as this moment, the 3 reight stages of the serial registers contain old (posible unwanted) signals coming from tje upper macropixel which should be dumped, while the left 2 stages of the serial registers contain the 2 newest signals. On option is for imager to continue collecting new signals and keep dumping the 3 old signals. This process will continue until t = t13, when all of the old (unwanted) signals have been dumped out, and the serial register have been filled up by all the new signals. At this point, the imager stops collecting signals and holds the most recent 30 signal frames for the readout. The signal charge distribution in the macropixel at t = t13 is given by Figure A.2(m).

Note that, during the signal collection, the gate G_4 next to the output serial registers operates exactly same as P3. It transfers charge from the parallel registers of the upper most and lower most row pixels to the output serial registers. And the output serial registers keep dumping all the unwanted signals towards the four outputs of imager.



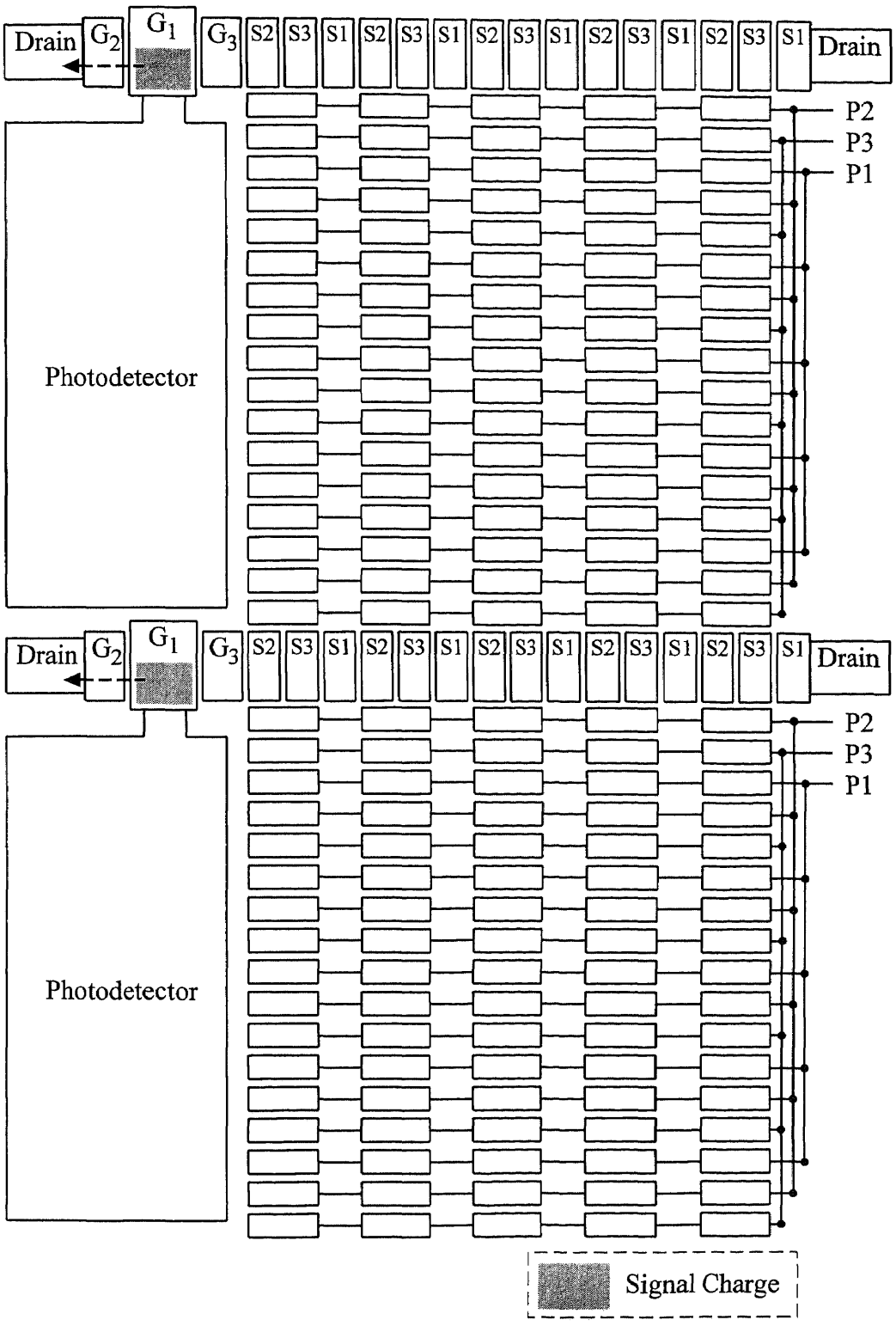
(a) *Beginning of the frame collection*

Figure A.1 *Driving waveform of the VHFR burst-image sensor during the frame collection period in Mode-1.*



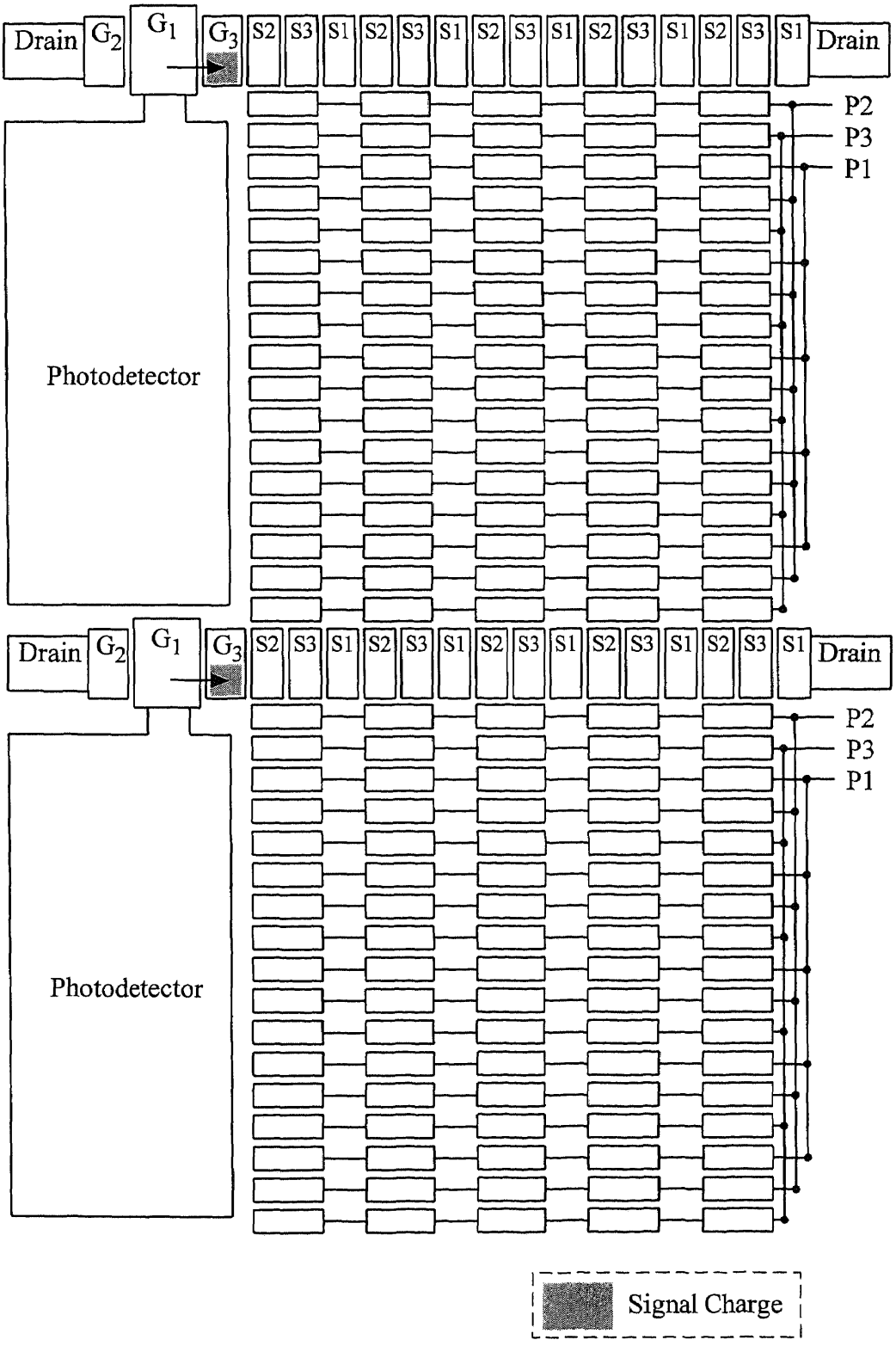
(b) *After 30 and more frames being collected and at the end of frame collecion*

Figure A.1 *(Continued)*



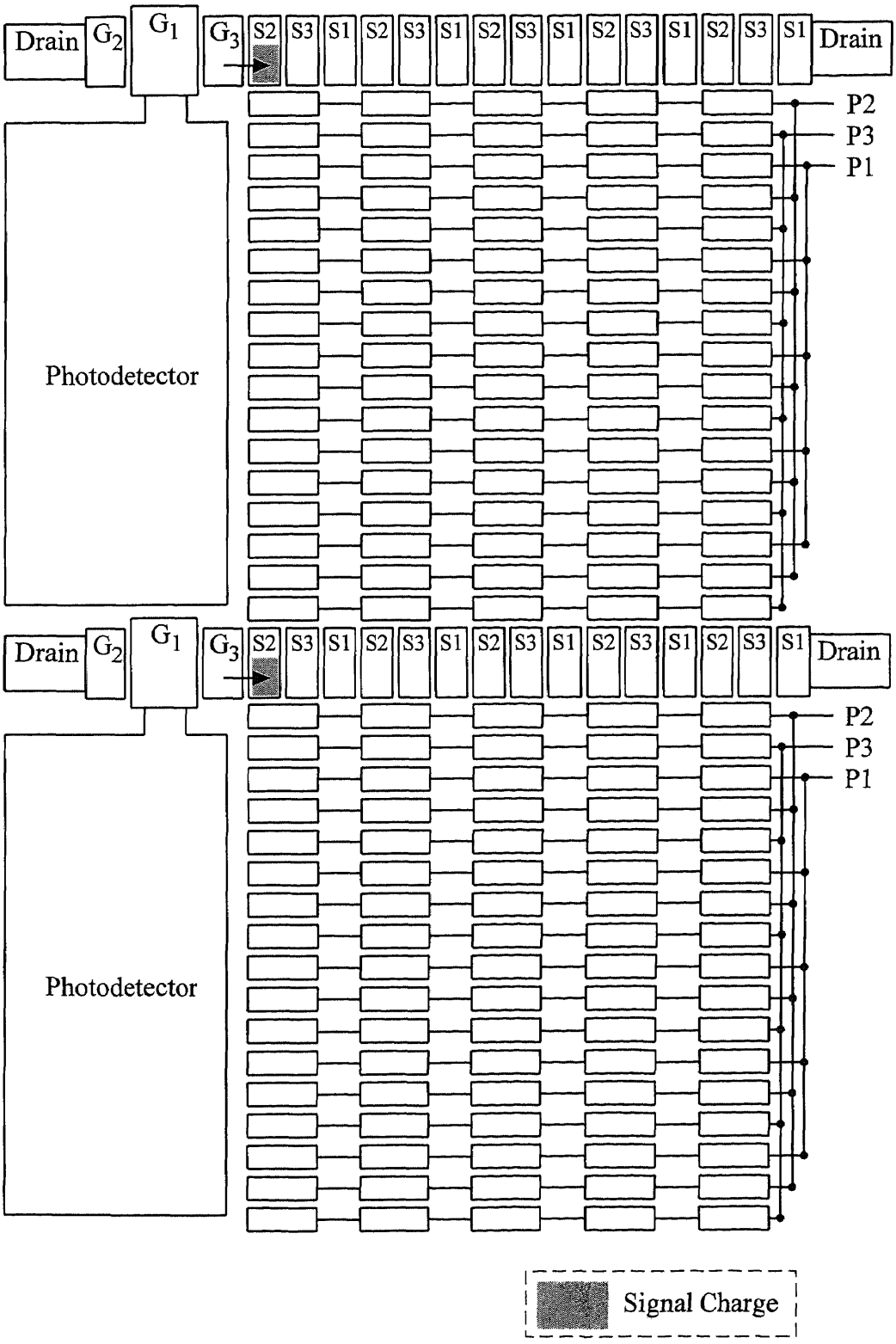
(a) $t = t1$

Figure A.2 *Signal charge transfer diagram in macropixels at different time during the frame collection period.*



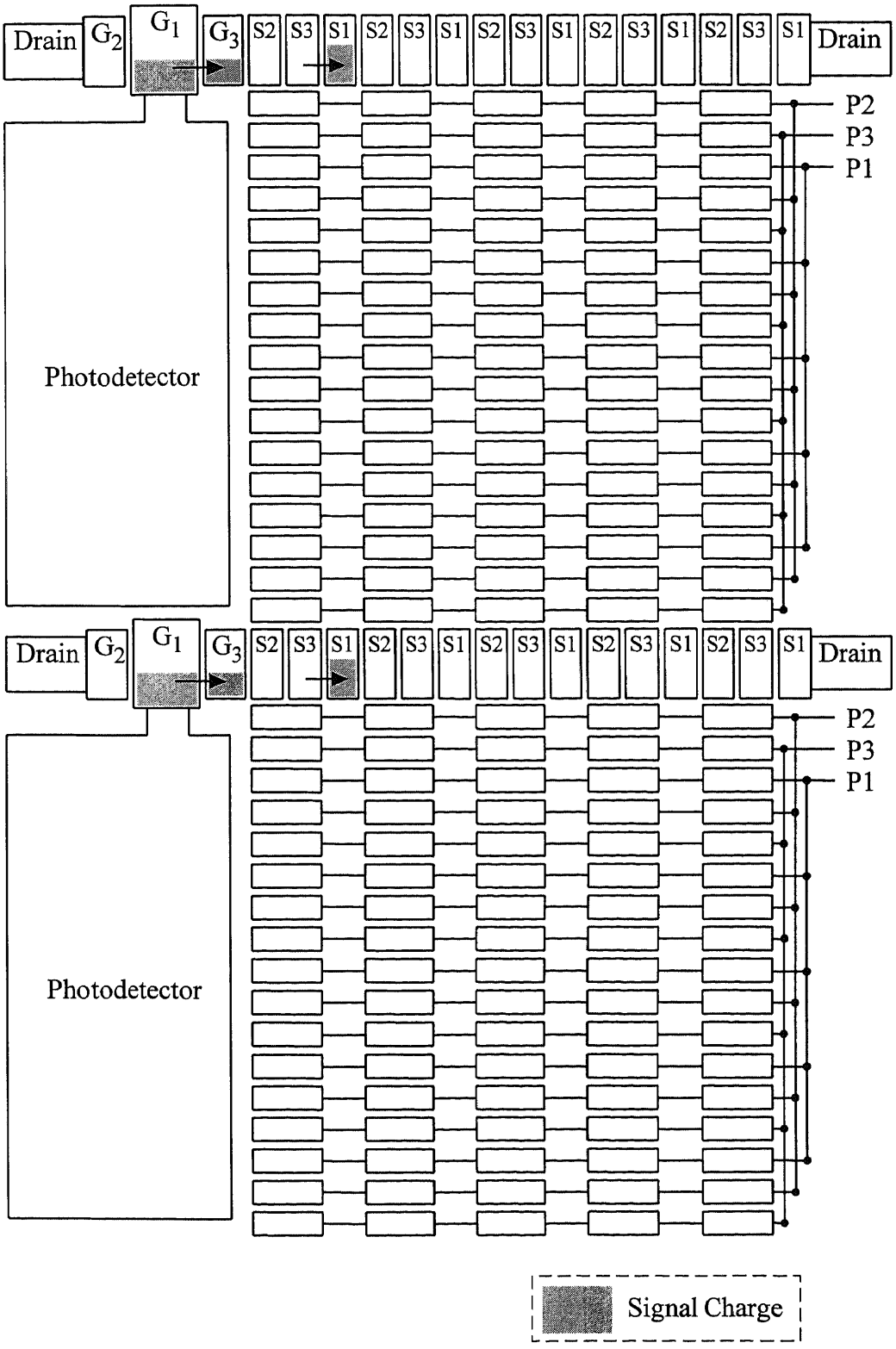
(b) $t = t2$

Figure A.2 *(Continued)*



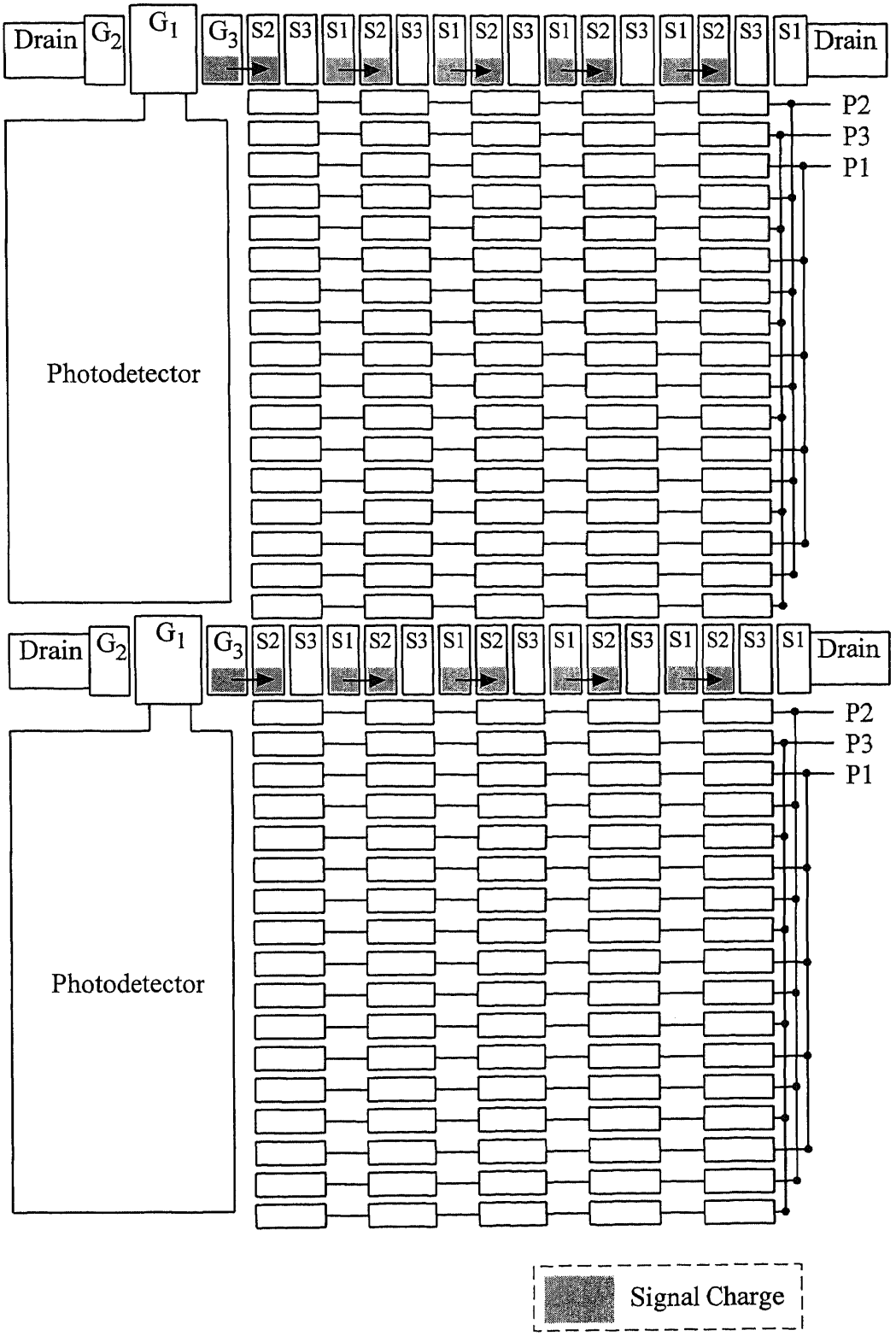
(c) $t = t3$

Figure A.2 *(Continued)*



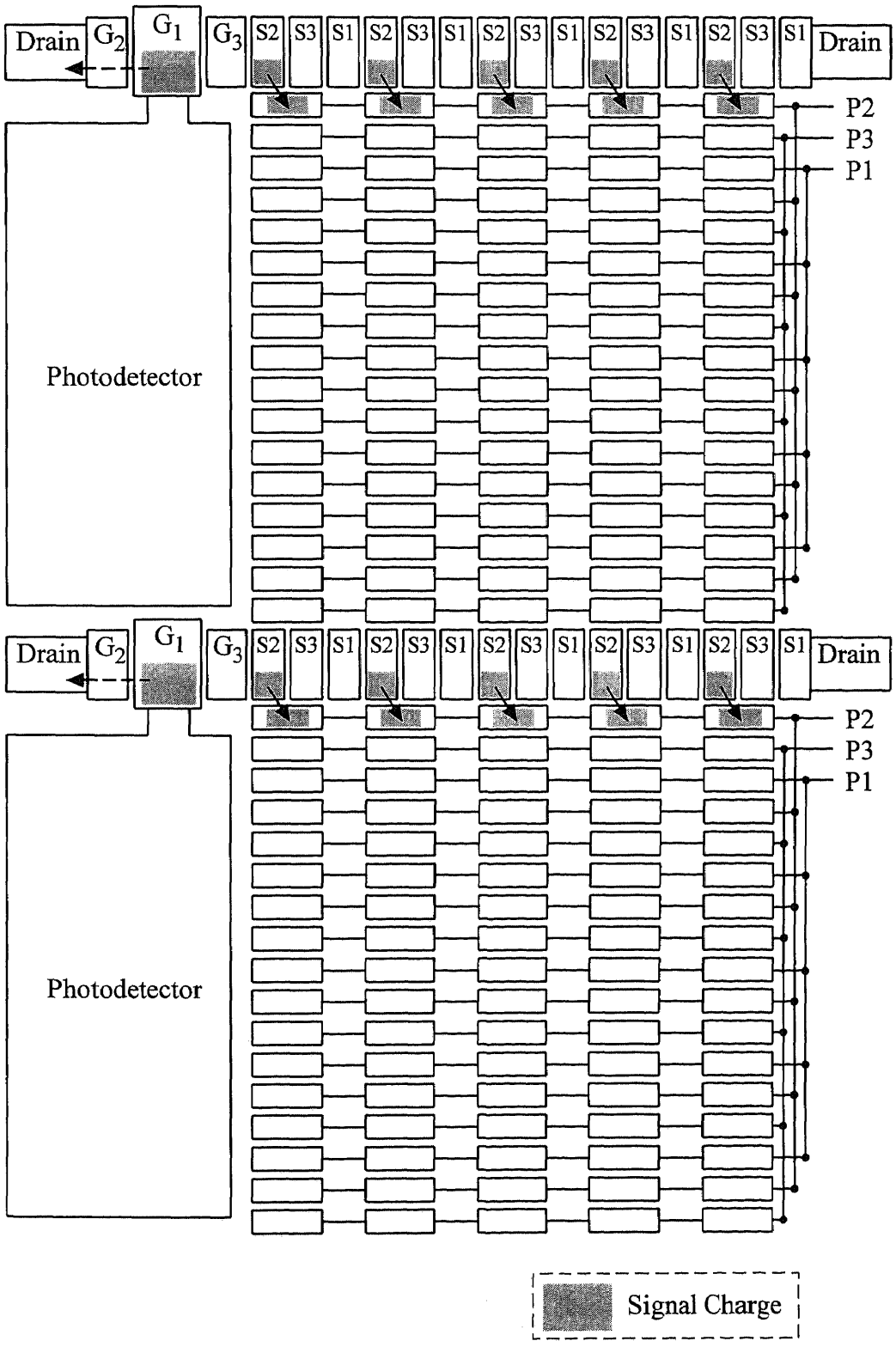
(d) $t = t4$

Figure A.2 *(Continued)*



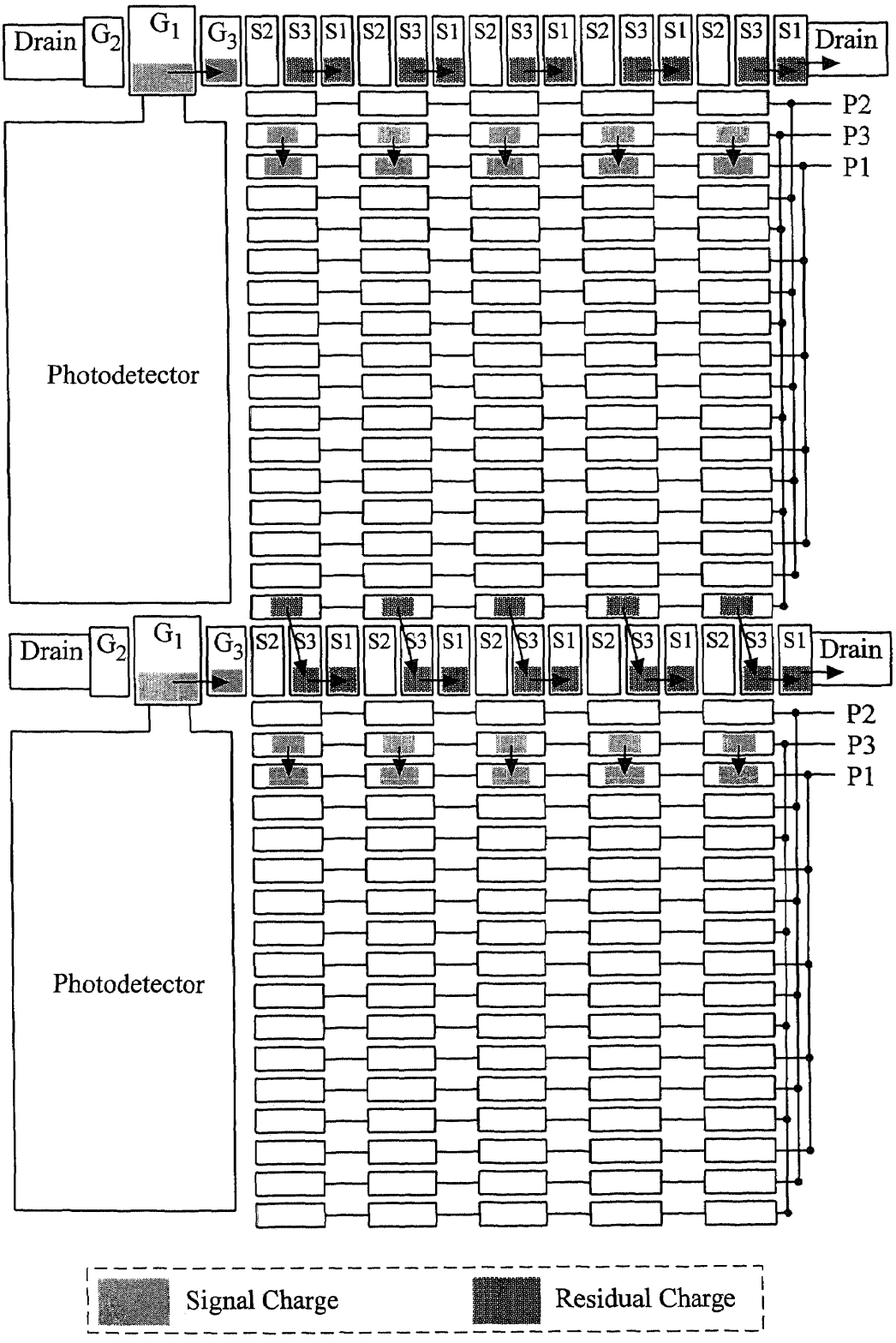
(e) $t = t5$

Figure A.2 *(Continued)*



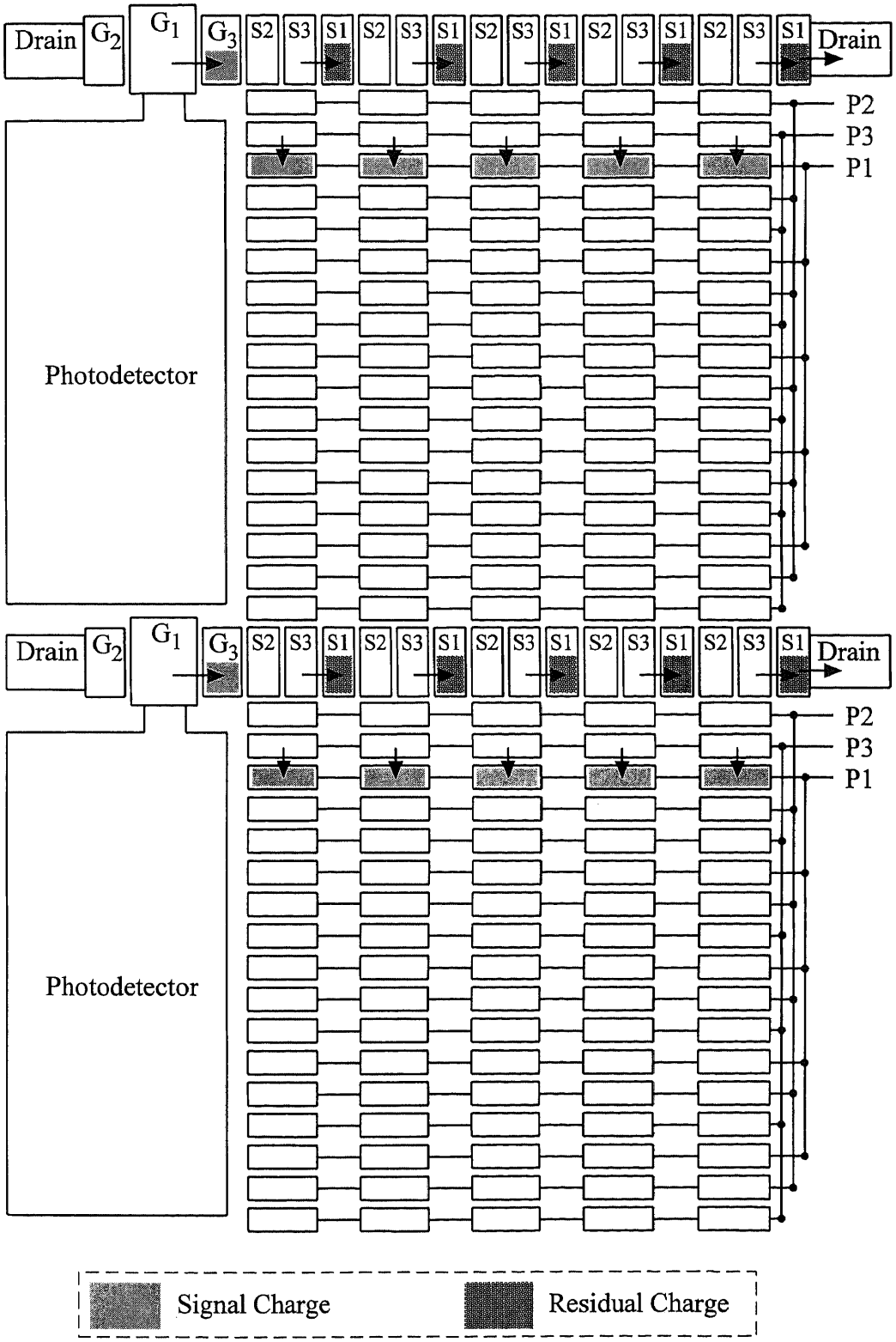
(f) $t = t6$

Figure A.2 *(Continued)*



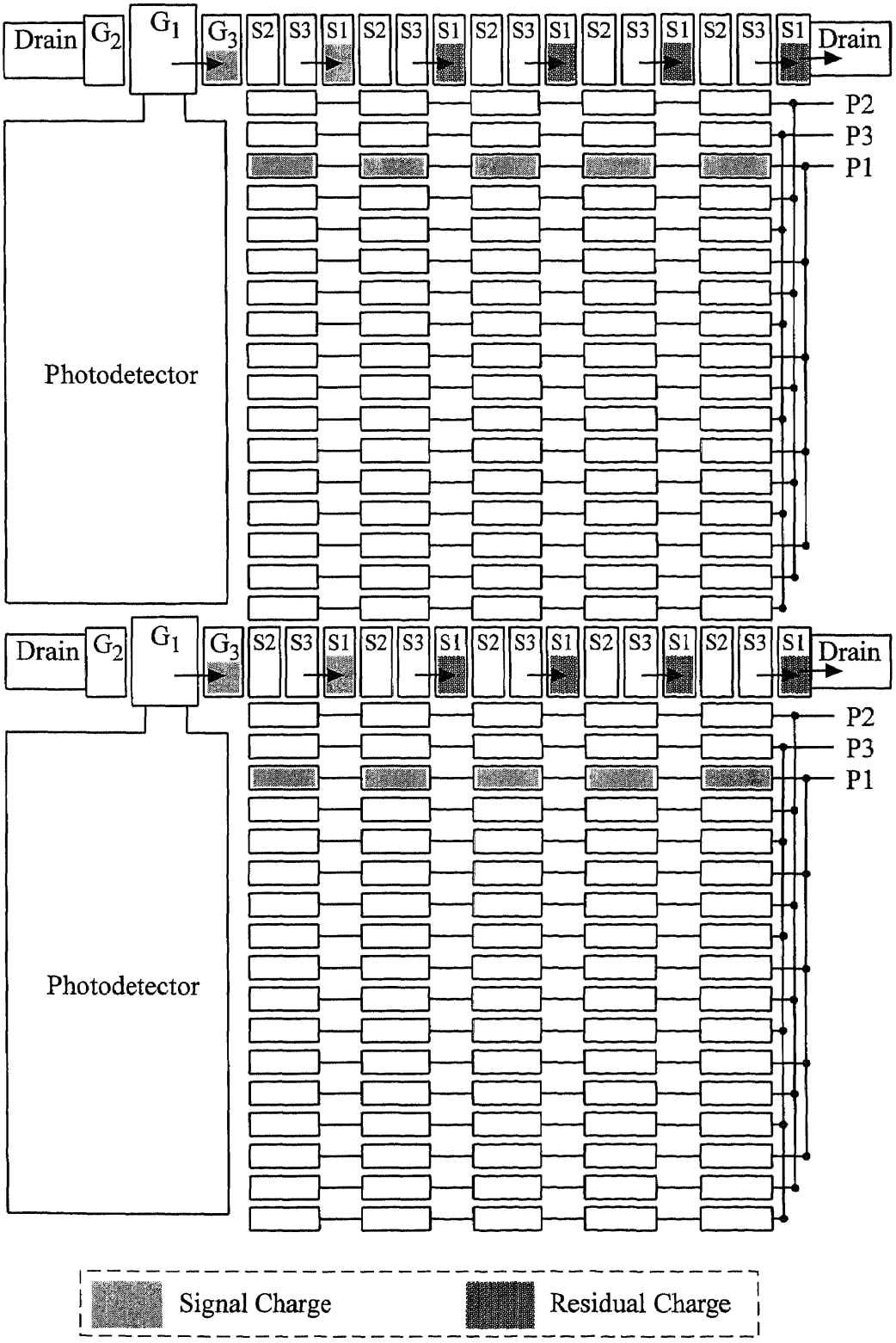
(g) $t = t7$

Figure A.2 *(Continued)*



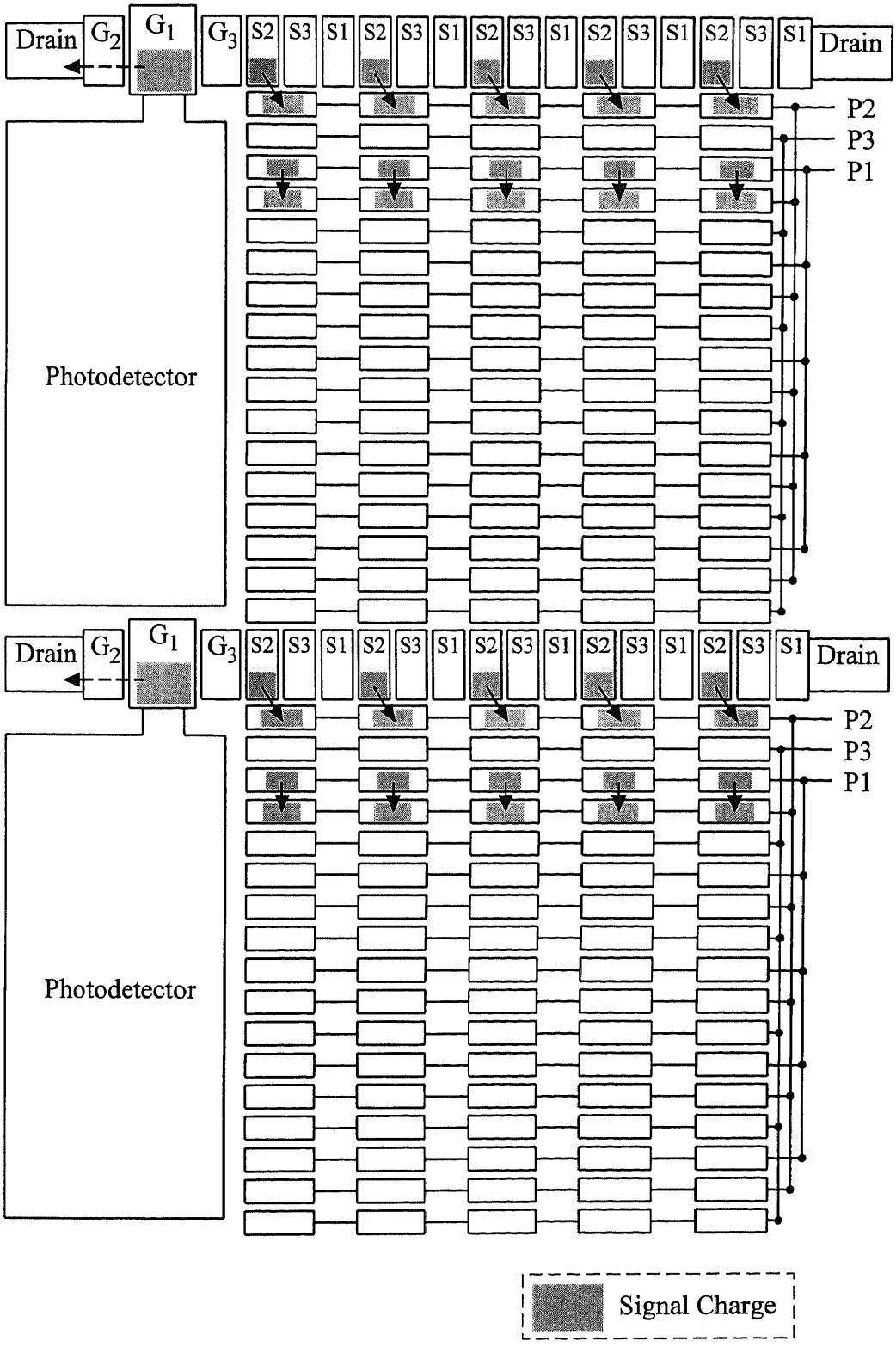
(h) $t = t8$

Figure A.2 *(Continued)*



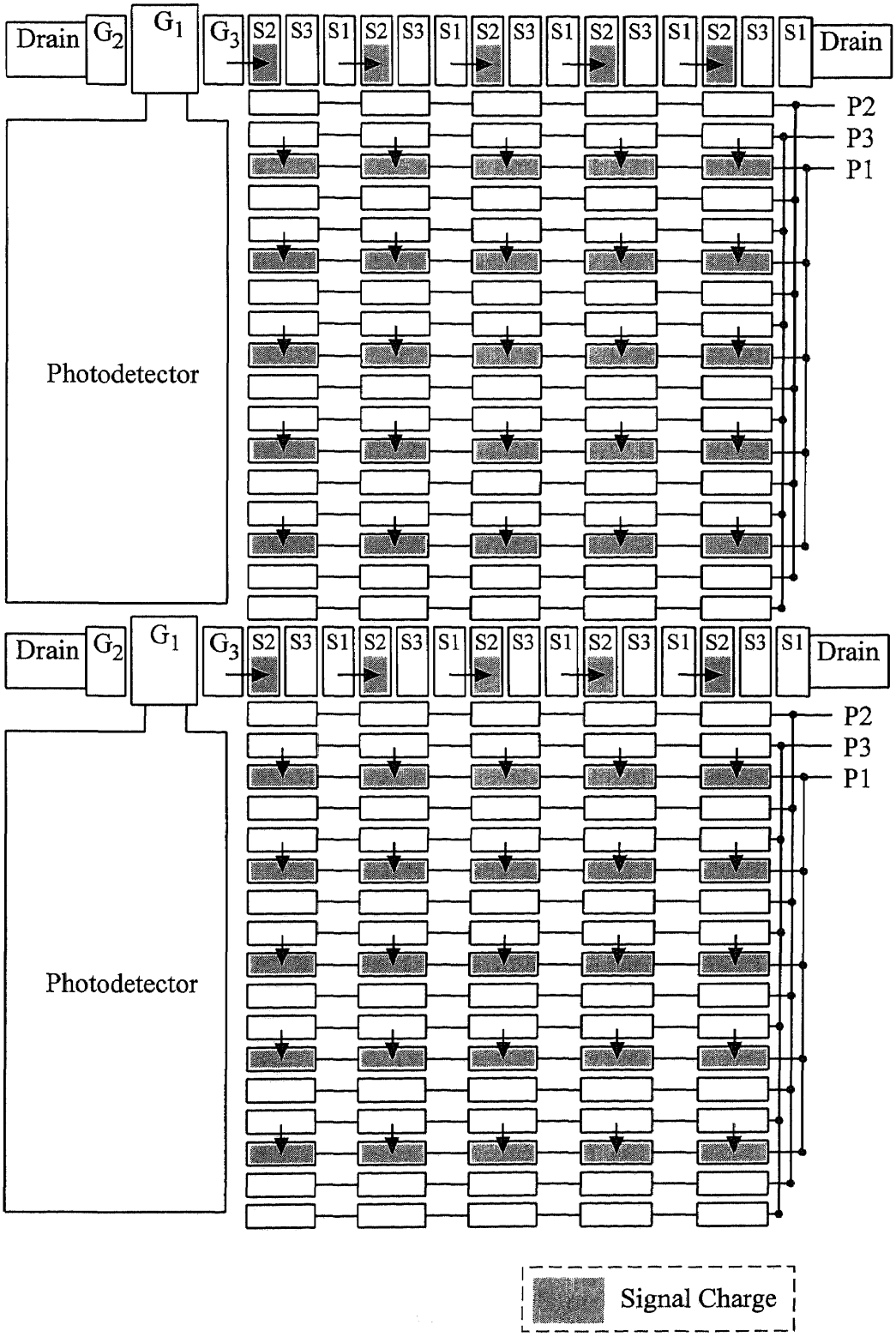
(i) $t = t9$

Figure A.2 *(Continued)*



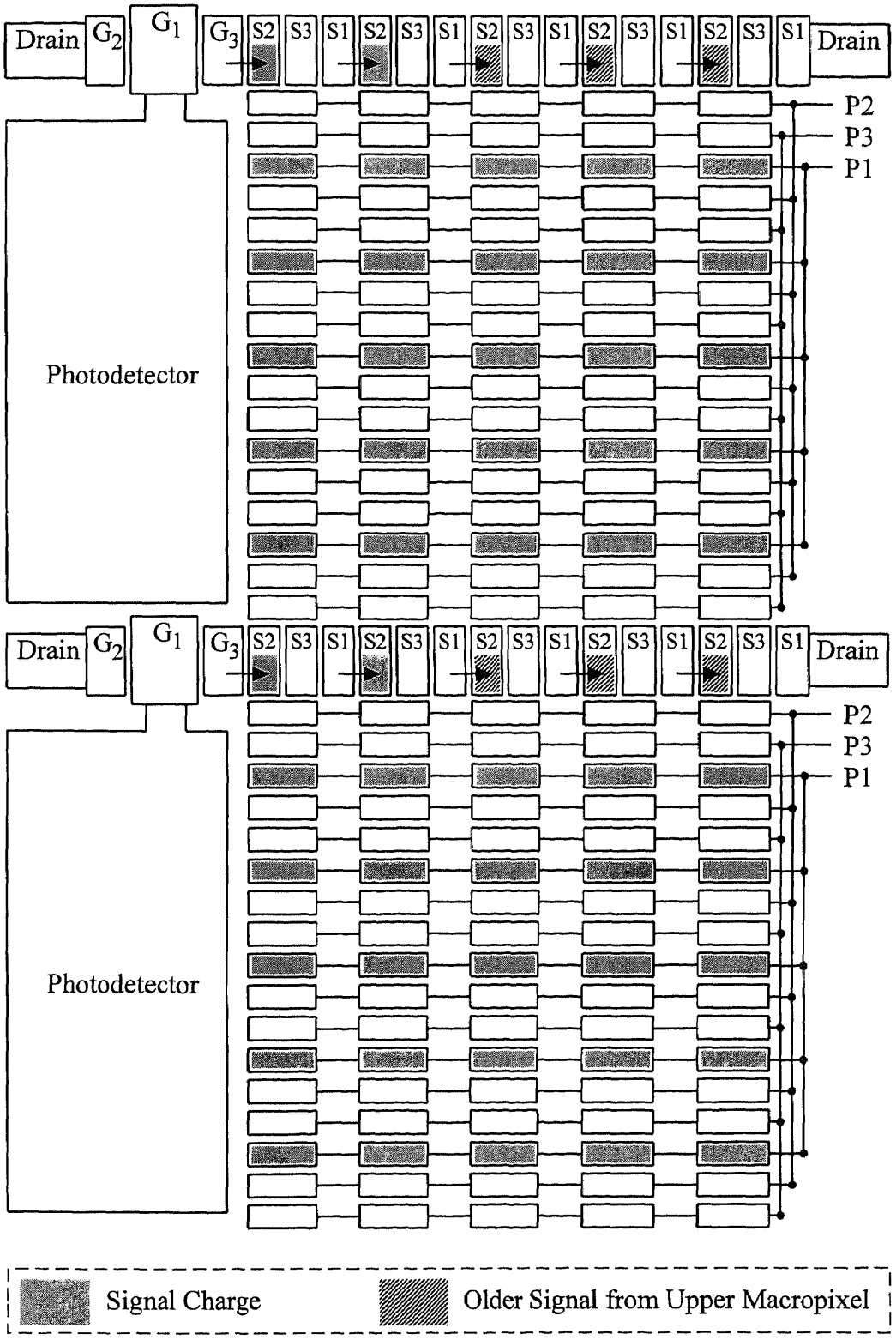
(j) $t = t10$

Figure A.2 *(Continued)*



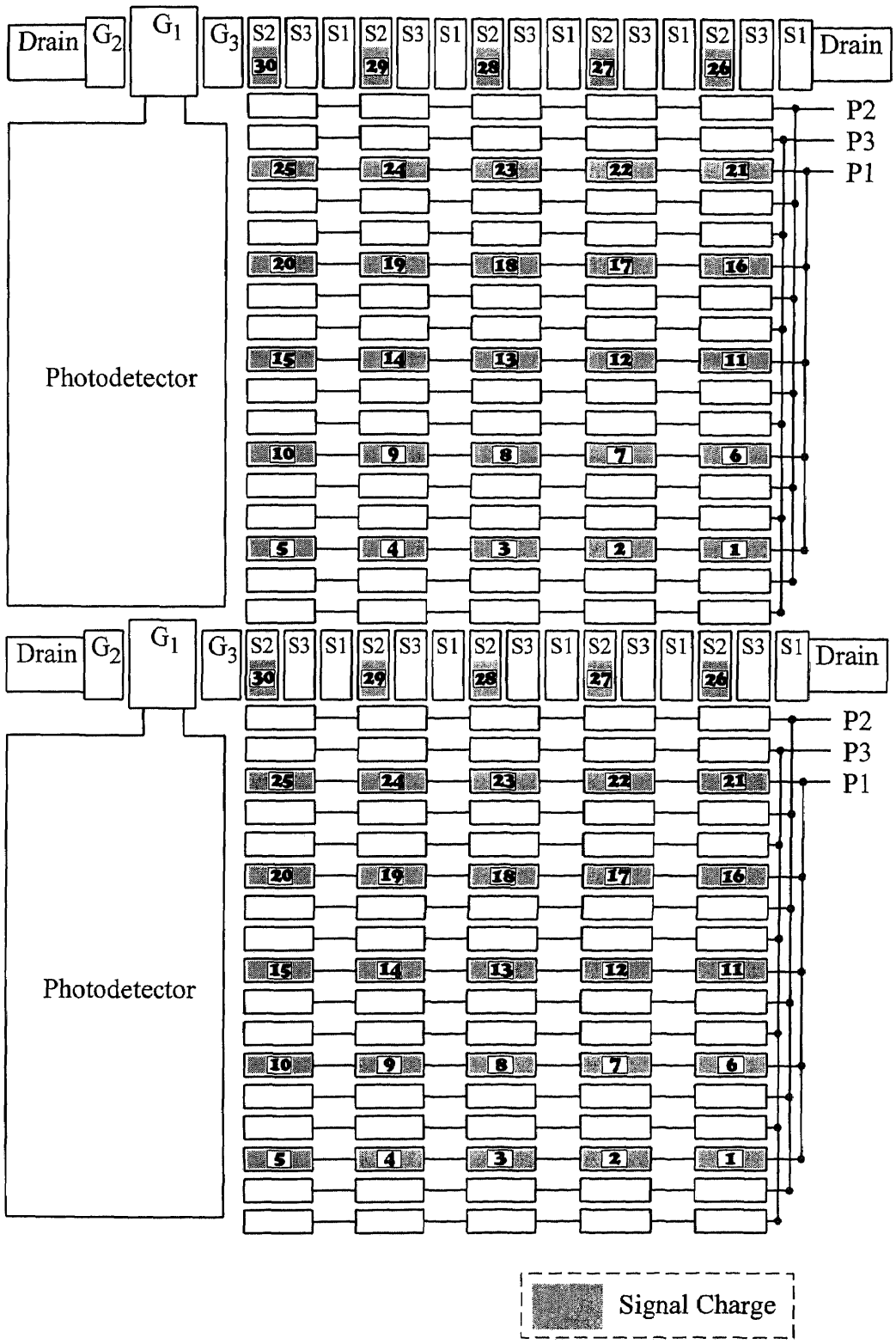
(k) $t = t11$

Figure A.2 *(Continued)*



(l) $t = t12$

Figure A.2 *(Continued)*



(m) $t = t13$

Figure A.2 *(Continued)*

A.2 Charge Readout Period

After the imager stops collecting signals and holds the most recent 30 frames signal, it can start to readout the collected signal charges. During the frame readout, the vertical (parallel) charge transfer is obtained by the parallel clock phases P1, P2, and P3. During this time, S2 and S3 act as P1 clock phase for vertical transfer the charge from one macropixel to the next one, while S1 is held in the low voltage stage to form channel stops for these parallel transfers. The clock wave formd fo each phase for operating the VHFR imager during the charge readout period are given by Figure 4.20. Figure A.3 redraws the wave forms with the definition of diferent time for the following discussion. Figure A.4 shows the signal charge transfer in four lower-side macropixels and the output serial registers in the lower-center of the imager at different time which is defined in Figure A.3 during the frame readout period.

- At t = t0, image starts signal readout. At this time, output serial register gates OS1 and OS2 are ON and OS3 is OFF.
- At t = t1, as shown in Figure A.4(a), S3 turns ON before S2 is turned OFF; P1 is kept ON. Signal charges are under S2 and S3 as well as P1.
- At t = t2, as shown in Figure A.4(b), S2 turns OFF, the signal charges in the serial registers are transferred into S3. P2 turns ON, the signal charges under S3 are transferring in parallel (vertical) to P2. In the mean time, in the parallel registers, signal charges in P1 are transferring to P2.
- At t = t3, as shown in Figure A.4(c), signal charges are transferring from P2 to P3 and from P2 to G_4, and to OS1 and OS2 gates of the output serial registers.
- At t = t4, as shown in Figure A.4(d), the parallel clocks P1, S2 and S3 are turned ON. Signal charges are transferring in parallel from P3 to P1 gates, and from G_4 to OS1 and OS2. The signal charges in the last P3 stage of the upper macropixel are transferring to S2 and S3.

- At t = t5, as shown in Figure 16(e), in the macropixels, all the signal charges in the serial registers of the macropixels are transferred into S3, and then transferred parallel into P2. The signal charges in the parallel register are transferred from P1 to P2. At this time, the first row of signals is completely transferred to the output serial registers and the signal charges in the macropixels are held under P2's pf the parallel registers. G_4 gate should be kept OFF at this time to allow the signal charges in the output serial registers to be clocked out to the OUTPUTs of each quadrant.
- At t = t6, also shown in Figure A.4(e), in the output serial registers, OS2 of the output serial registers is turned OFF and signal charges are transferred into OS1.
- At t = t7, as shown in Figure A.4(f), the signal charges in the output serial registers are transferred to the OUTPUTs of each quadrant in a sequence of OS1 to OS3, to OS2, to OS1, ...

  At this time, the remained signal charges in the macropixels are held under the phase P2 of the parallel register.
- After 180x6 transfers in output serial registers, the first row of signal is completely readout. The output serial register gates OS1 ans OS2 are turned ON to receive the next row of signals and OS3 in turned OFF. At t = t8, as shown in Figure A.4(g), the signal charges in the macropixels are transferring from P2 to P3 and P2 to G_4, and to OS1 and OS2 gates of the output serial register. At this time, the imager start to readout the second row of signal.

After the 180x6 rows of signal charge are transferred to the output serial register and then transferred to the output of each quadrant, all of the 30 frames of image have been read out and the whole operation of the image is completed.

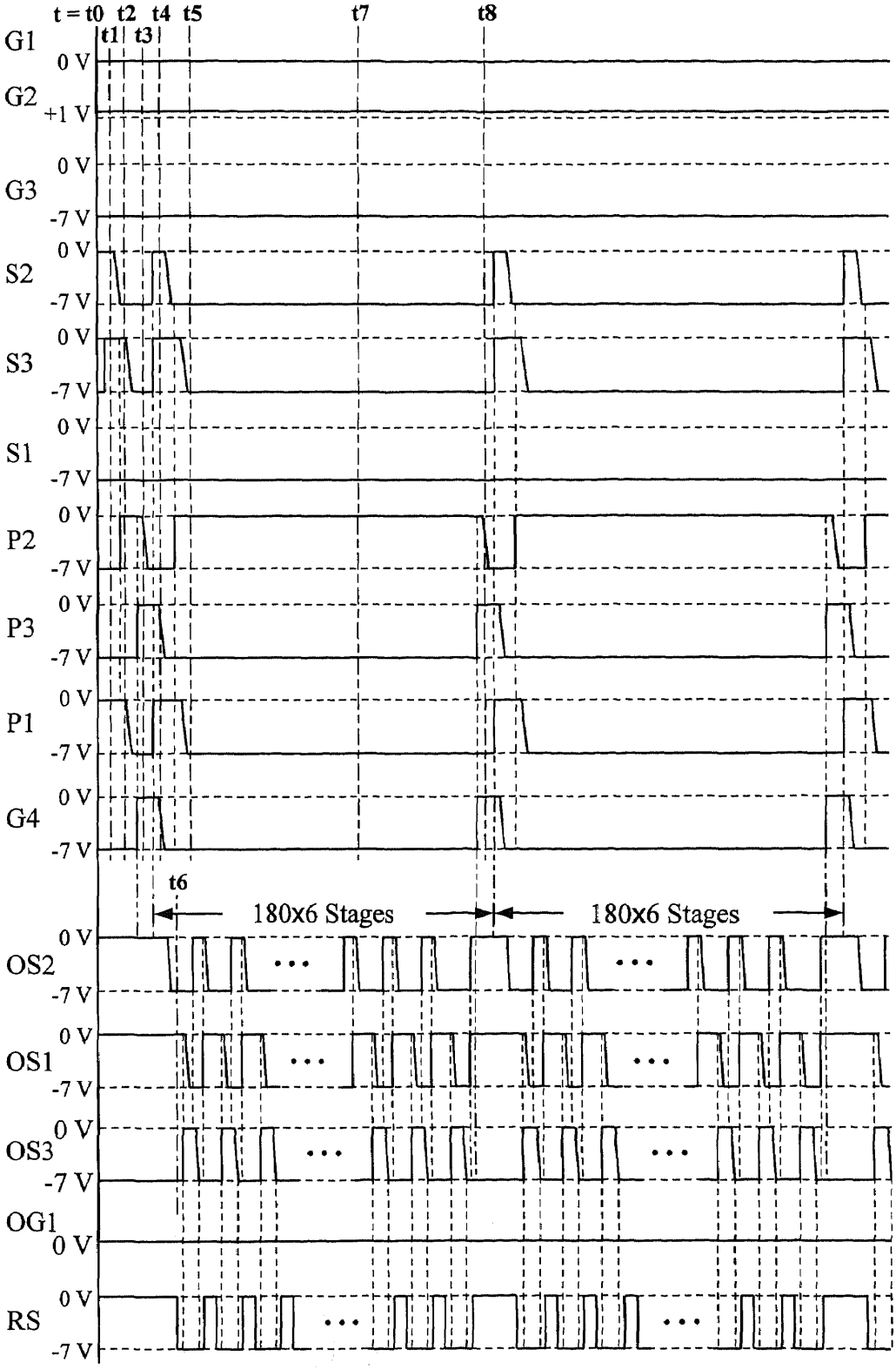
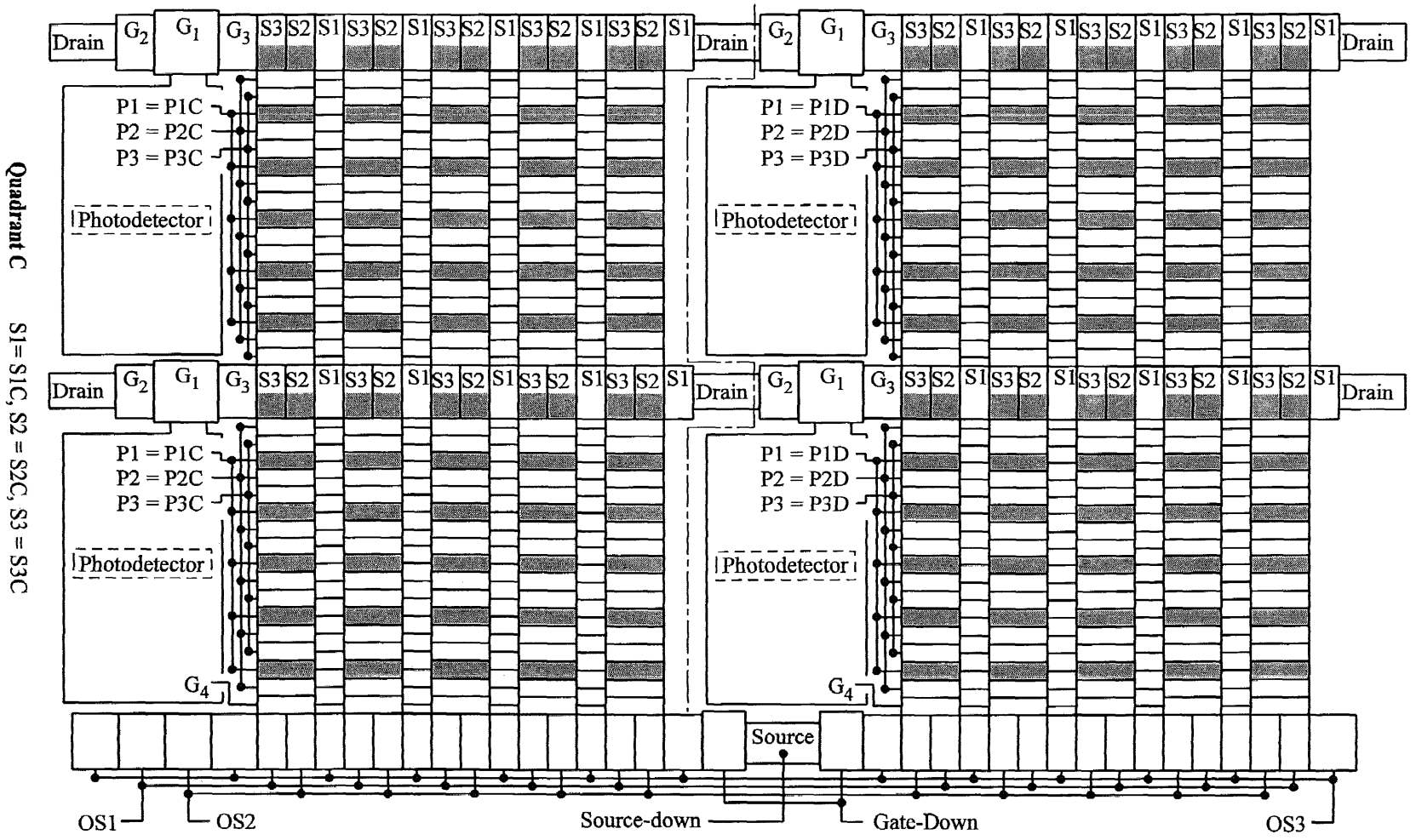


Figure A.3 *Clock wave form of VHFR burst-image sensor during the frame readout period.*

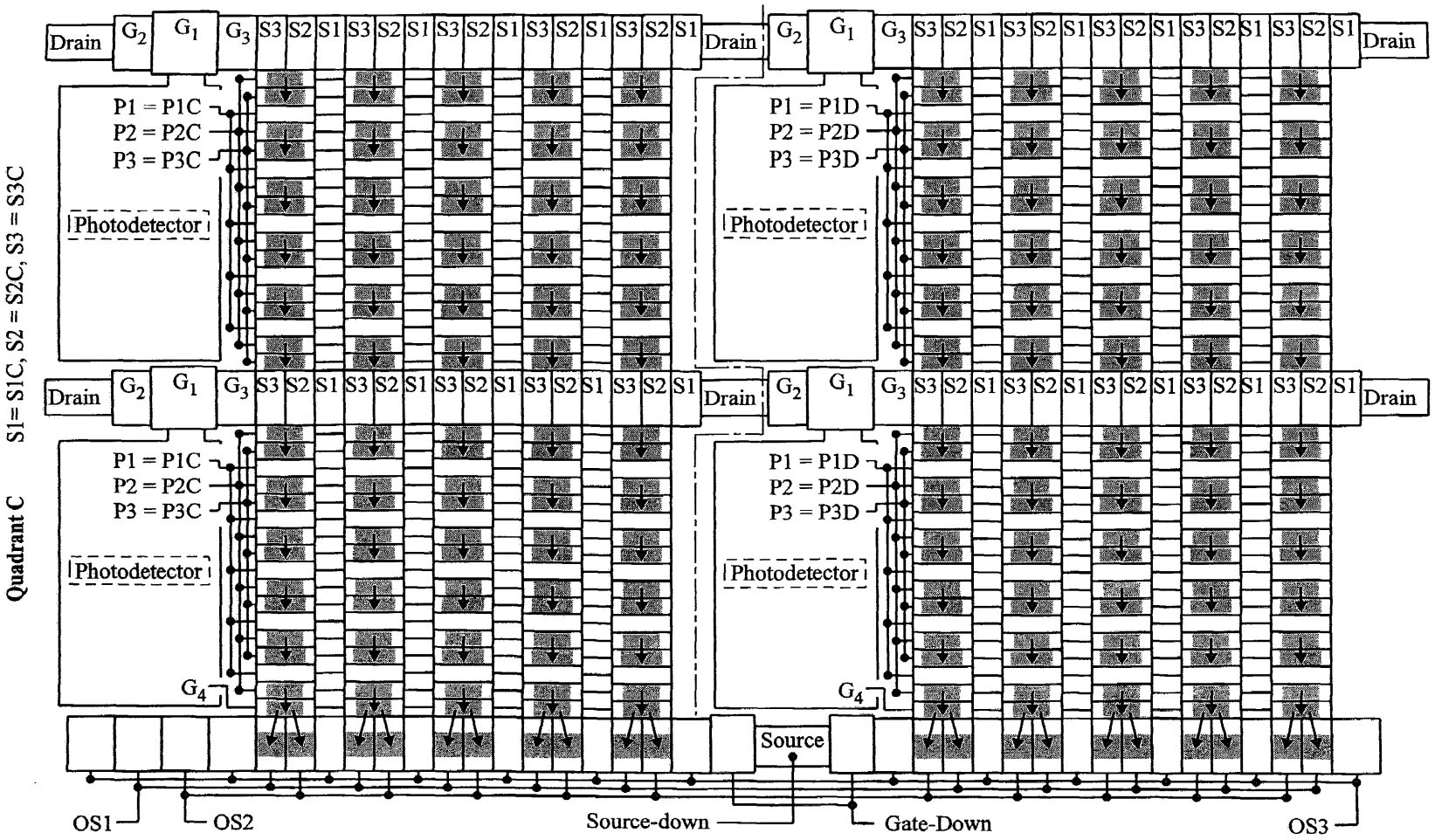


(a) $t = t1$

Figure A.4 *Signal charge transfer diagram at different time during the frame readout period.*

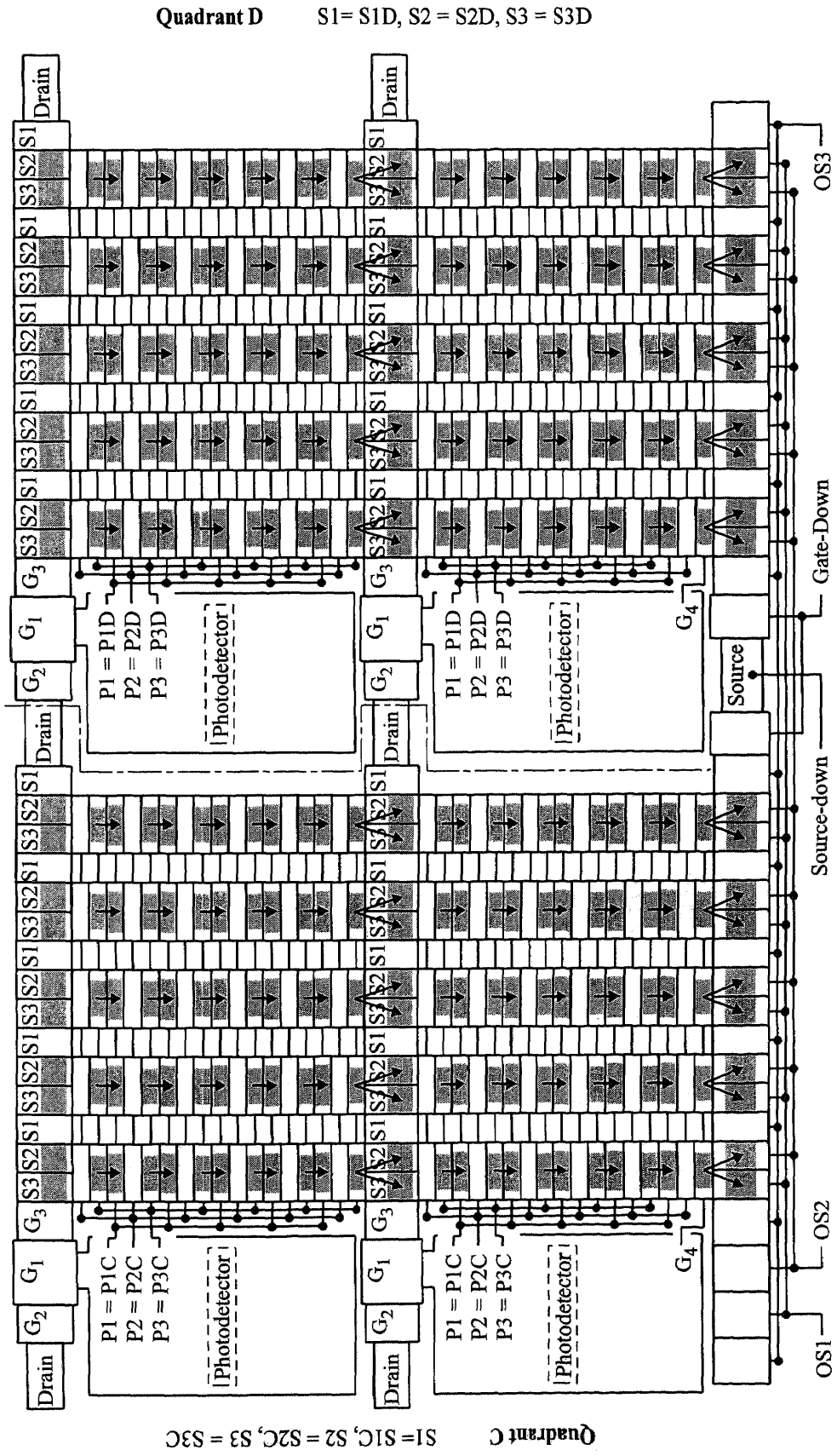
(b) $t = t2$

Figure A.4 *(Continued)*



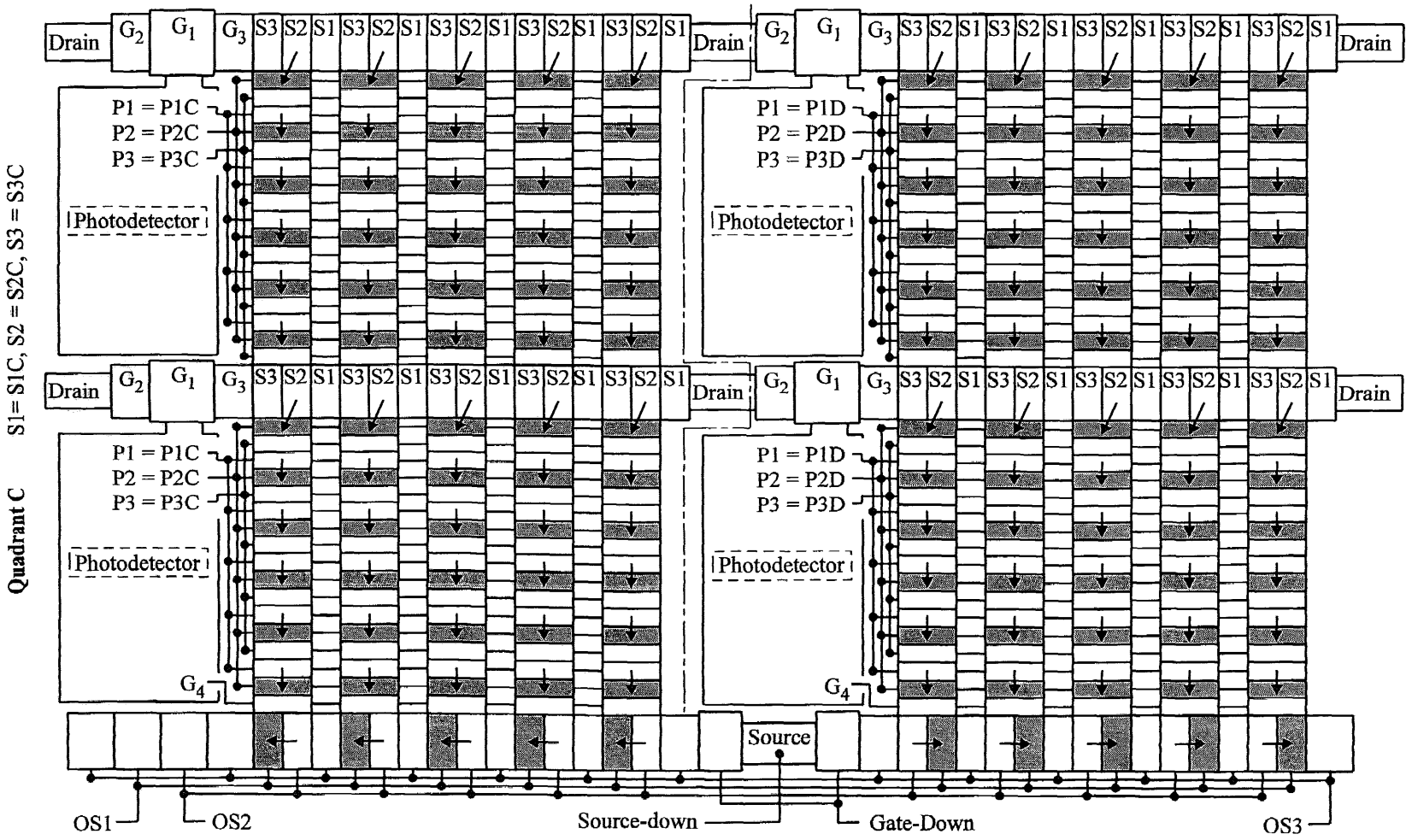
(c) $t = t3$

Figure A.4 *(Continued)*



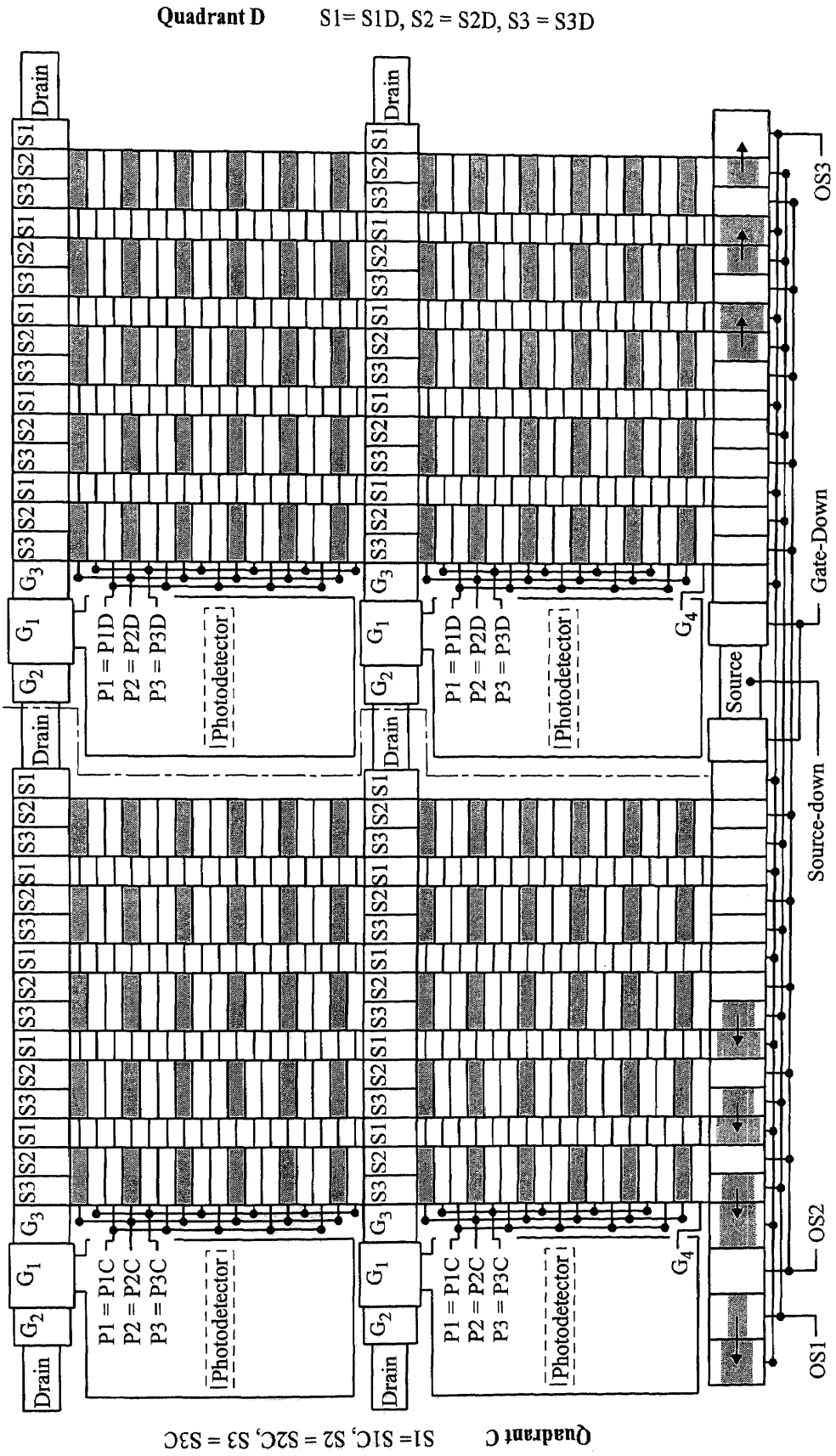
(d) $t = t4$

Figure A.4 *(Continued)*



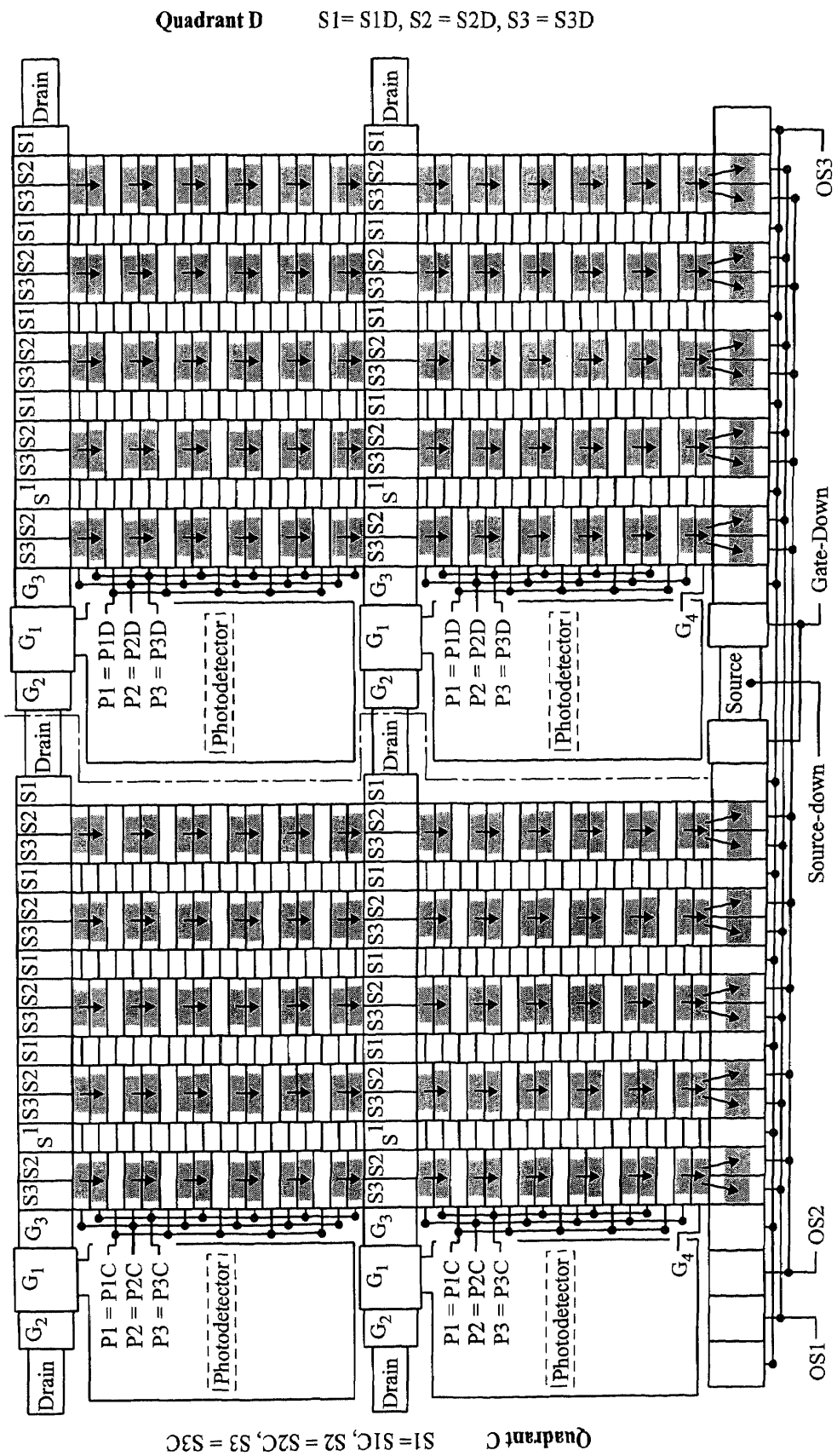
(e) *t = t5 in macropixels, and t = t6 in output serial registers*

Figure A.4 *(Continued)*



(f) $t = t7$

Figure A.4 *(Continued)*



(g) $t = t8$

Figure A.4 *(Continued)*

APPENDIX B

THE FLOW CHART OF THE FABRICATION PROCESS FOR THE VHFR BURST-IMAGE SENSOR

This appendix presents the process flow for fabrication of the VHFR burst-image sensors. The process flow illustrates the formation of the device structure by each process step described in Section 5.3. The device-structure patterns representing different layers and dopings as well as the photo resist are given in Figure B.1. It should be noted that this process description includes the specific process data that was developed as part of this dissertation. However, not included are the data of the Sarnoff process that are Sarnoff preparatory.

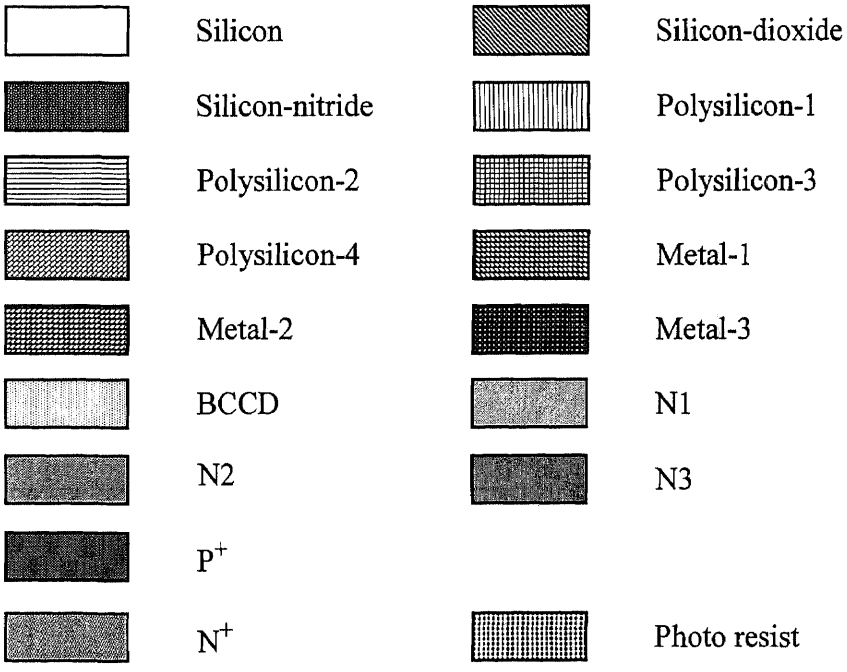
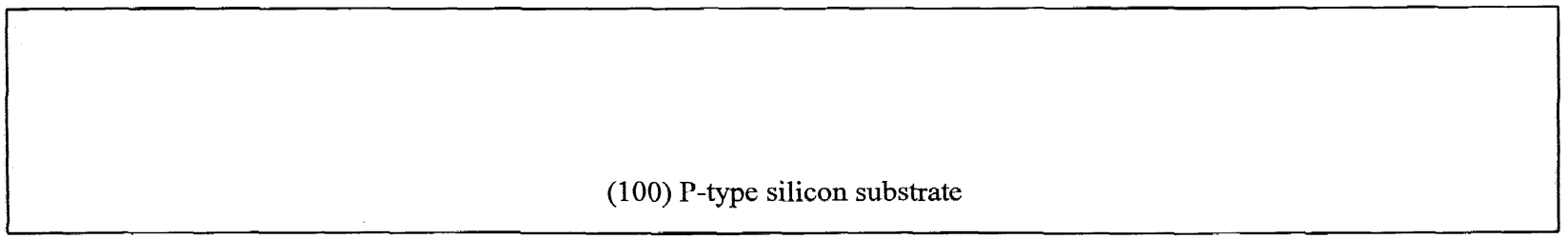
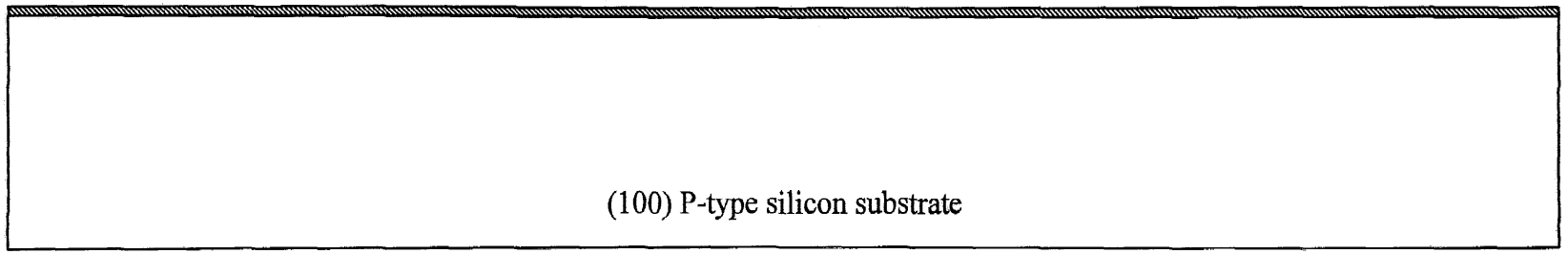


Figure B.1 *The device structure patterns which represent different materials and dopings in the process flow chart.*

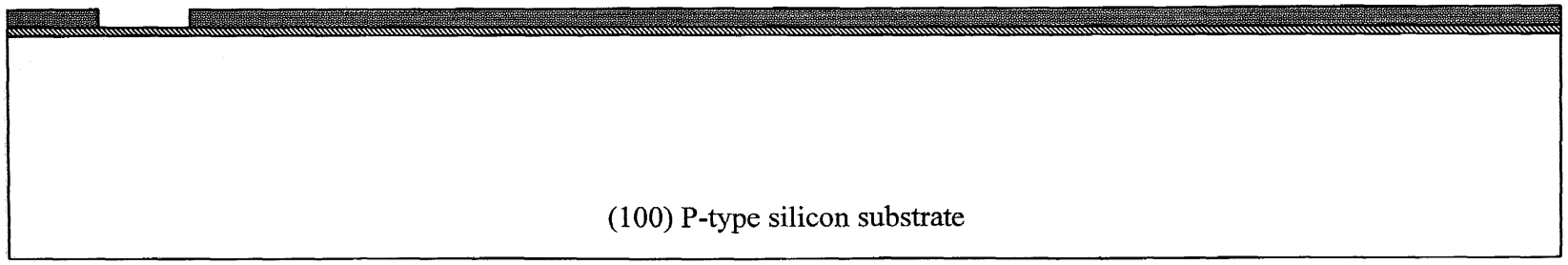
1. Substrate: Boron doped (100) P-type silicon epi wafer.
   - 17.5-μm p^- epi layer (resistivity of 43 ohm-cm) on <100> p^+ substrate.



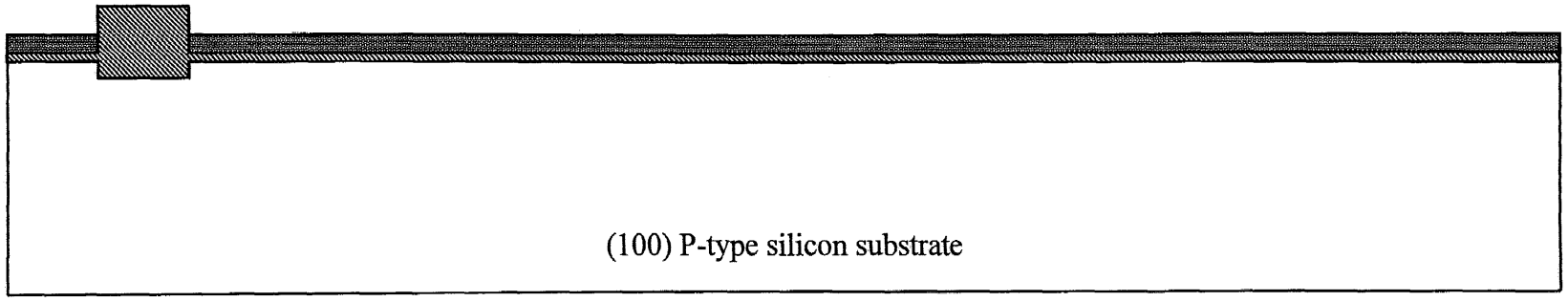
2. Growth of pad oxide for nitride.



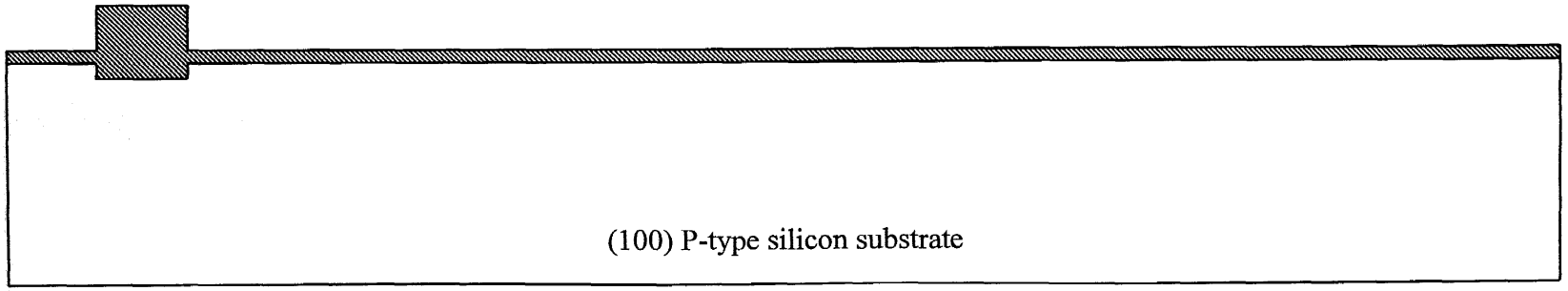
3. Deposit silicon-nitride, etch silicon-nitride in the region defined for growing field oxide.



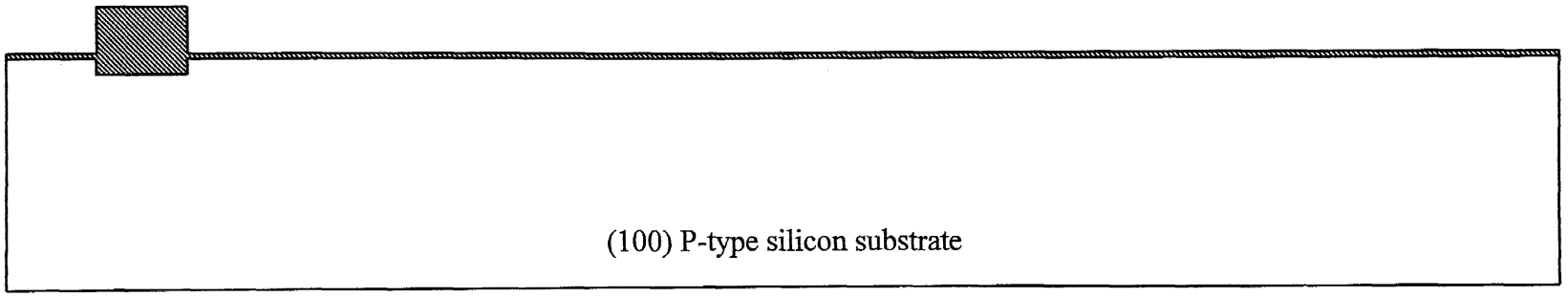
4. VTFN (boron implant dose of 3.0×10^{12} cm^{-2} at 50 keV) implantation followed by growth of field oxide.



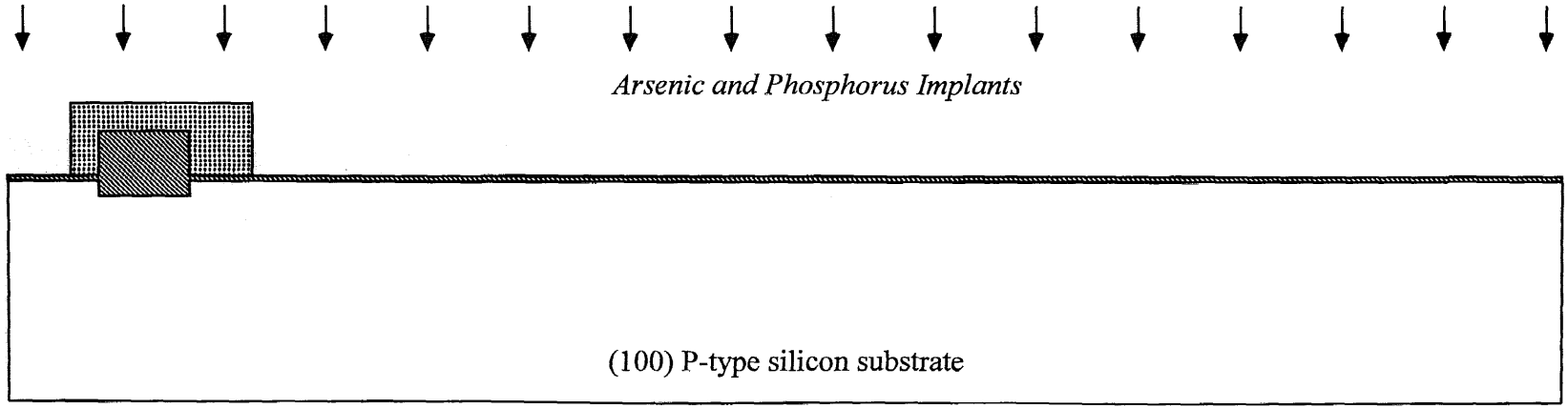
5. Etch silicon-nitride and growth of sacrifical oxide (in addition to the pad oxide in Step-2).



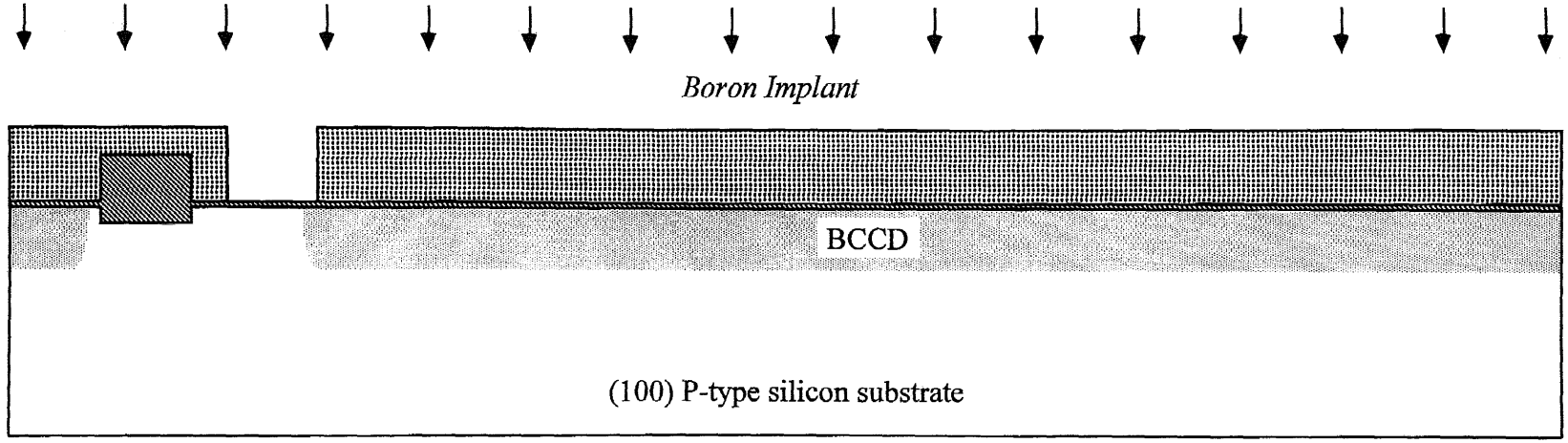
6. Etch oxide to silicon surface in the region without field oxide, grow screen oxide (about 125 Å) for BCCD implants.



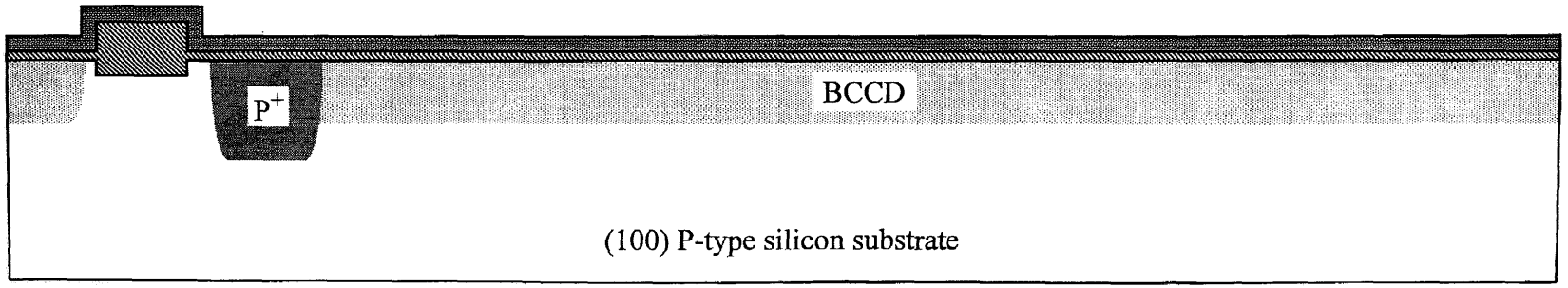
7. BCCD N-type implants
   - arsenic implant dose of 1.2×10^{12} cm^{-2} at 120 keV, and phosphorus implant dose of 1.0×10^{12} cm^{-2} at 180 keV



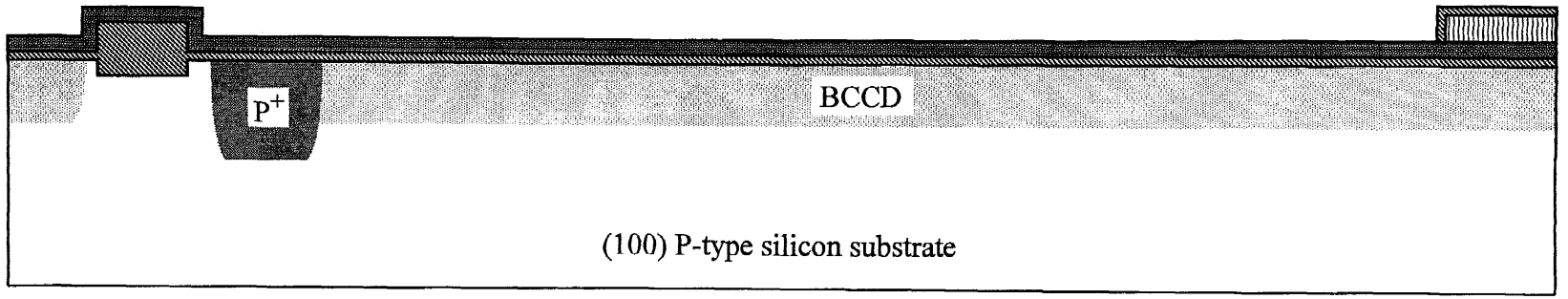
8. P^+ field implant (for P^+ region surrounded the photodetector and output amplifier) after initial BCCD implant drive-in.
   - boron implant dose of 2.5×10^{15} cm^{-2} at 35 keV.



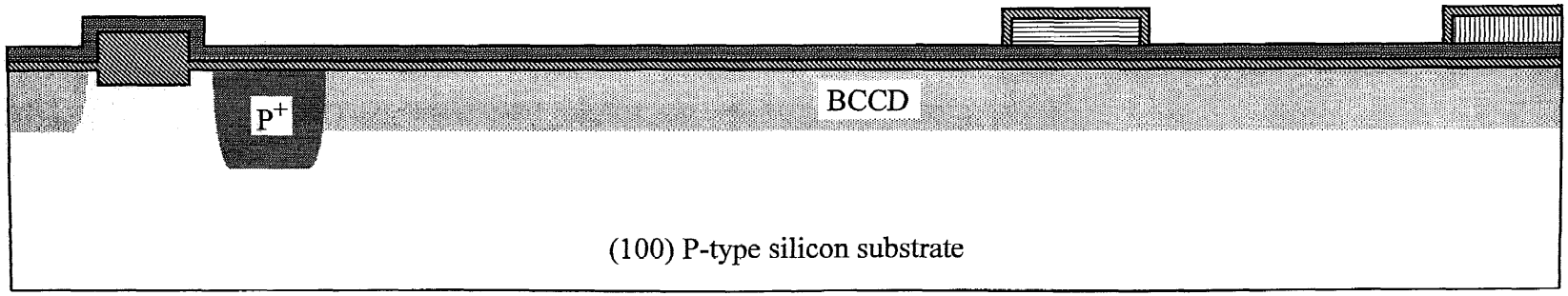
9. Etching oxide to the silicon surface in the region without field oxide.
10. Forming a gate oxide of 350 Å by thermal oxidation.
11. Deposit a gate nitride layer of 650 Å on top of oxide.



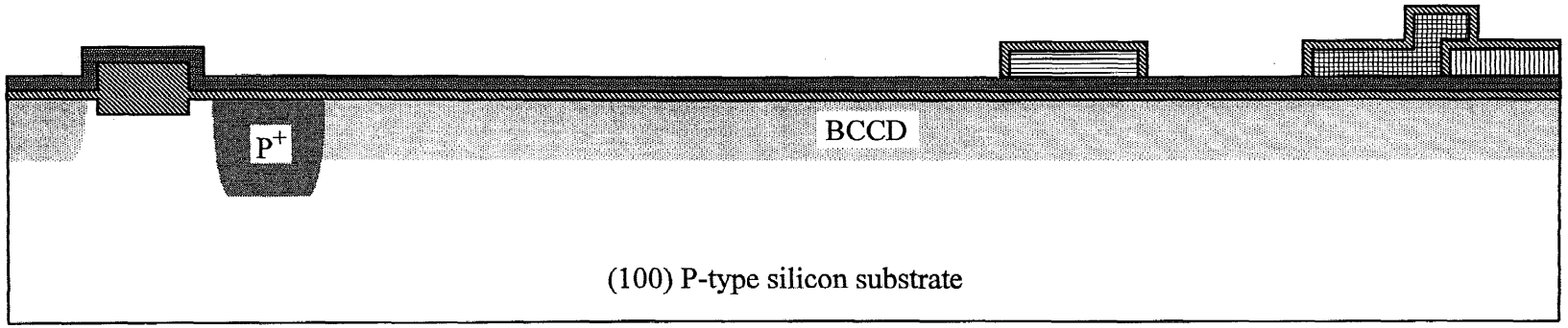
12. Deposit N^+ doped polysilicon (poly-1).
13. Etch poly-1 to gate insulator surface except the poly-1 gate regions defining poly-1 gates.
14. Grow the first inter-polysilicon oxide layer (about 1400 Å) by thermal oxidation for the deposition of second polysilicon layer.



15. Deposit N^+ doped polysilicon (poly-2).
16. Etch poly-2 to gate insulator surface except the poly-2 gate regions defining poly-2 gates.
17. Grow the second inter-polysilicon oxide layer (about 1400 Å) by thermal oxidation for the deposition of third polysilicon layer.



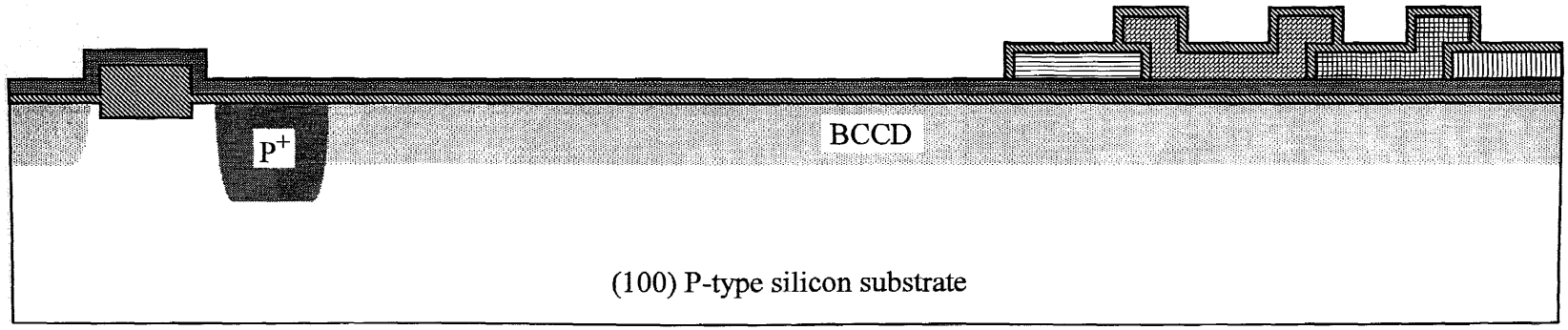
18. Deposit N^+ doped polysilicon (poly-3).
19. Etch poly-3 to gate insulator surface except the poly-3 gate regions defining poly-3 gates.
20. Grow the third inter-polysilicon oxide layer (about 1400 Å) by thermal oxidation for the deposition of forth polysilicon layer.



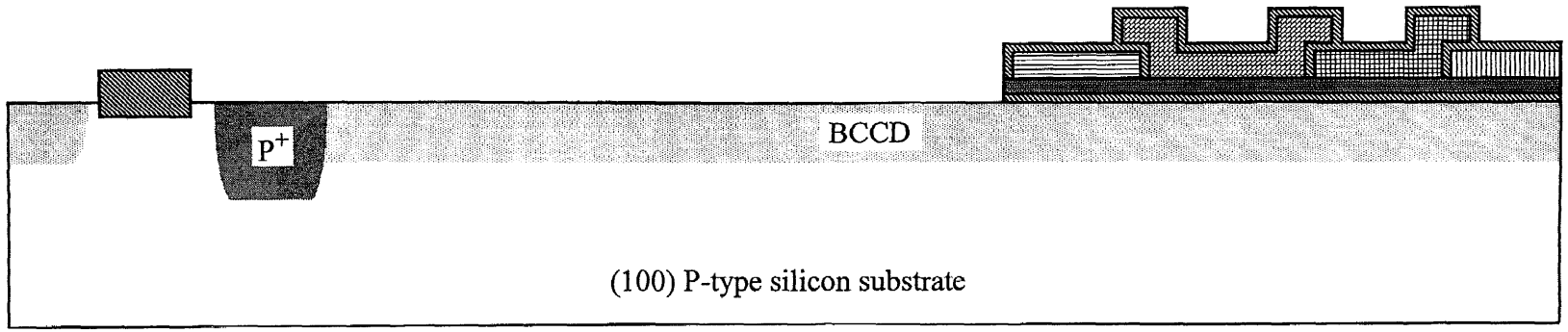
21. Deposit N^+ doped polysilicon (poly-4).

22. Etch poly-4 to gate insulator surface except the poly-4 gate regions defining poly-4 gates.

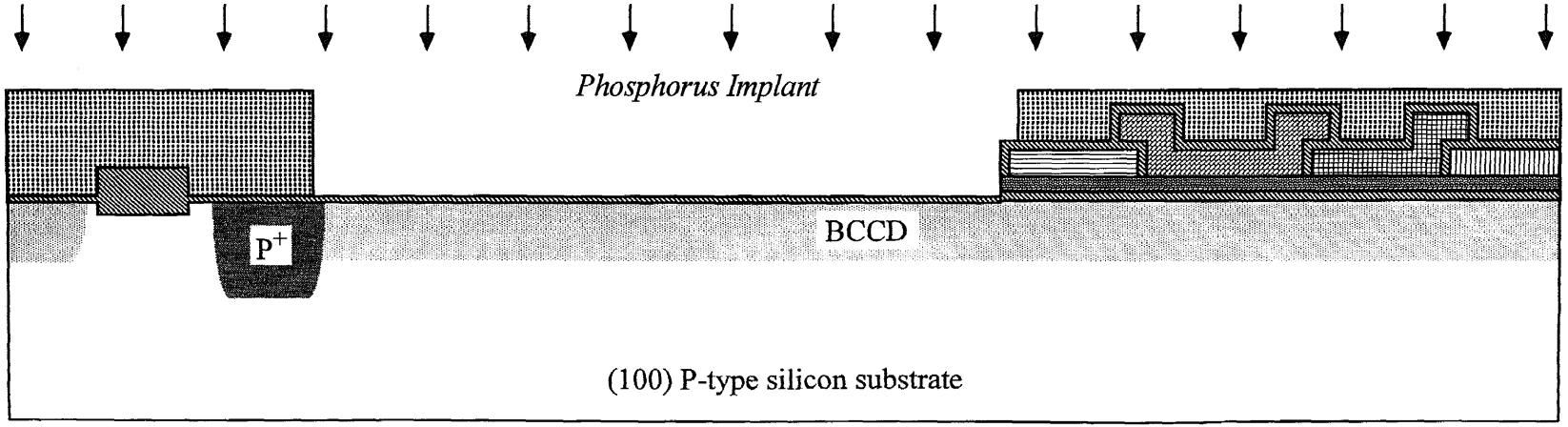
23. Reoxidation-one, nitride passivation and growing a oxide layer on top of poly-4.



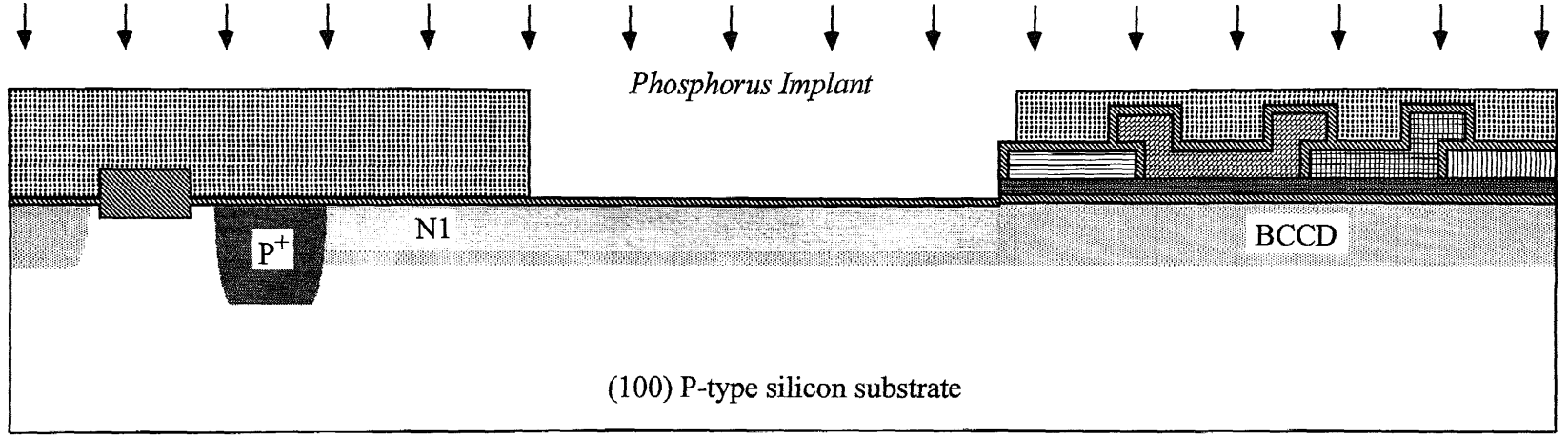
24. Etch nitride and oxide to silicon surface in the regions without polysilicon layers.



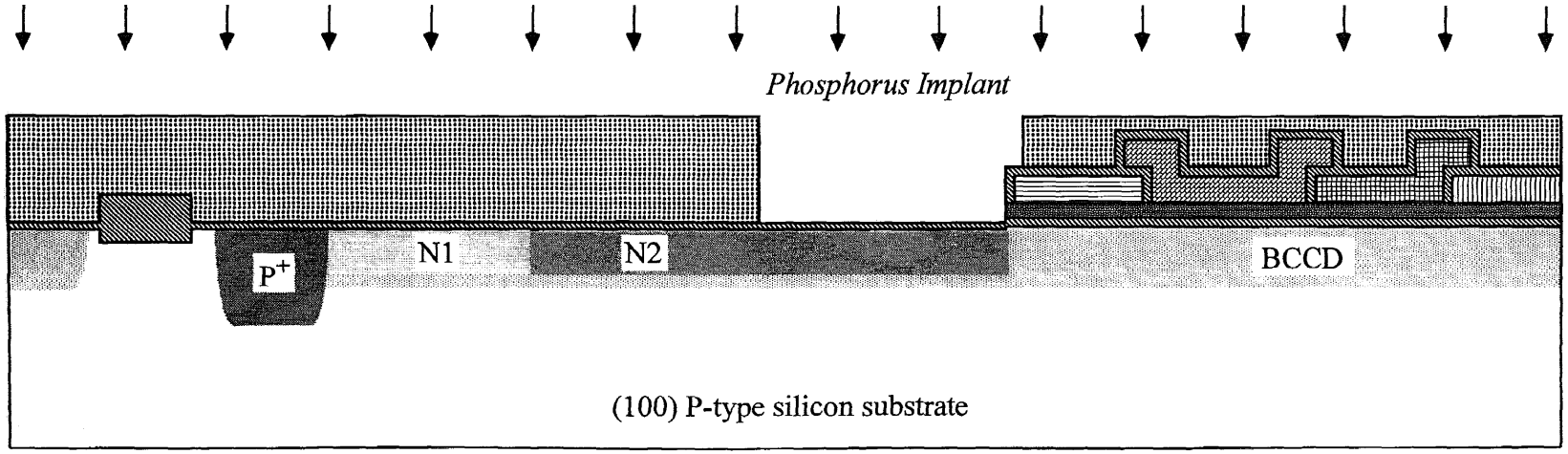
25. Grow screen oxide (about 125 Å) by thermal oxidation for photodetector additional N-type implants.
26. First photodetector N-type implant (phosphorus implant dose of 1.4×10^{12} cm^{-2} at 120 keV).



27. Second photodetector N-type implant (phosphorus implant dose of 1.2×10^{12} cm^{-2} at 120 keV).



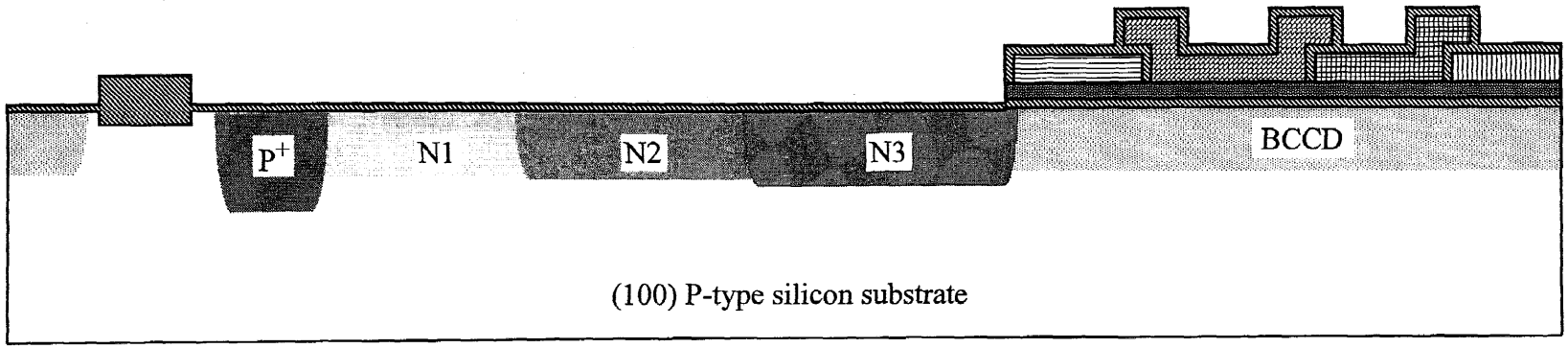
28. Third photodetector N-type implant (phosphorus implant dose of 1.0×10^{12} cm^{-2} at 120 keV).



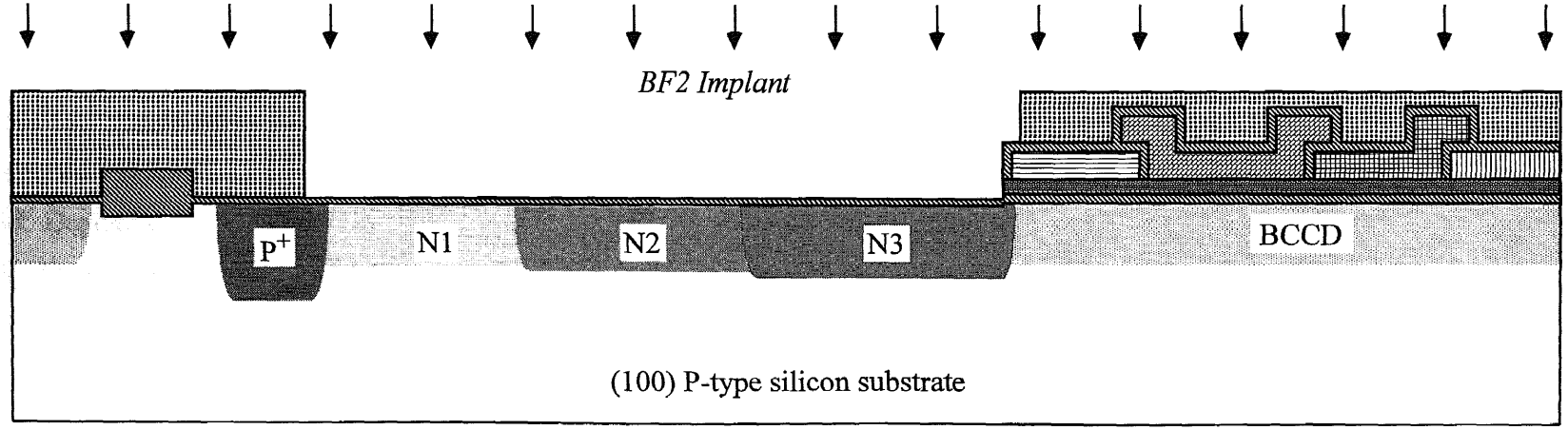
29. Drive-in the N-type photodetector implants and BCCD implant (the P^+ field implant is also diffused).

30. Remove screen oxide for the additional photodetector N-type implants.

31. Form a new screen oxide layer by thermal oxidation for photodetector P^+ implant.

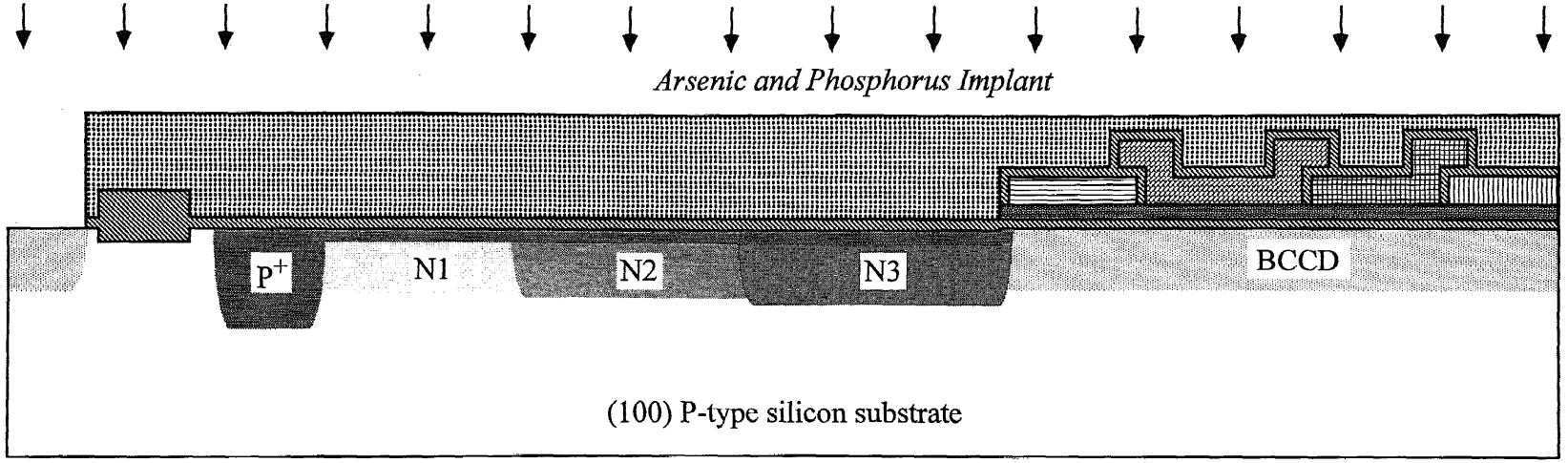


32. Photodetector P^+ implant (BF2 implant dose of $3.0x10^{14}$ cm^{-2} at 30 keV) to complete the pinned-buried photodetector..

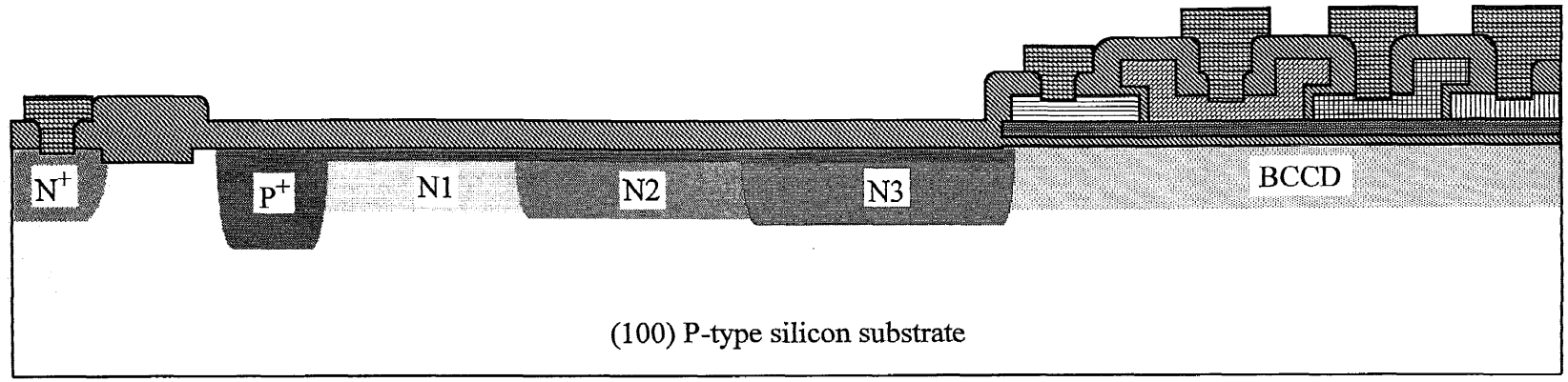


33. Reoxidation-two. An oxide layer is grown in the region without polysilicon.

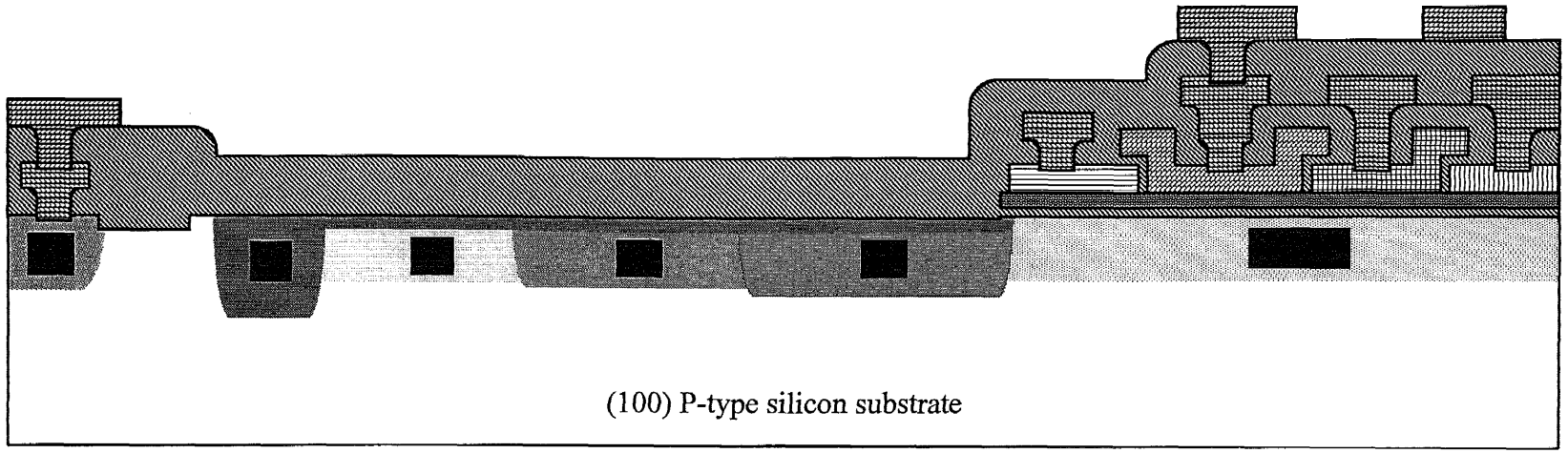
34. Etch oxide to silicon surface in source and drain region followed by source and drain N^+ implant.



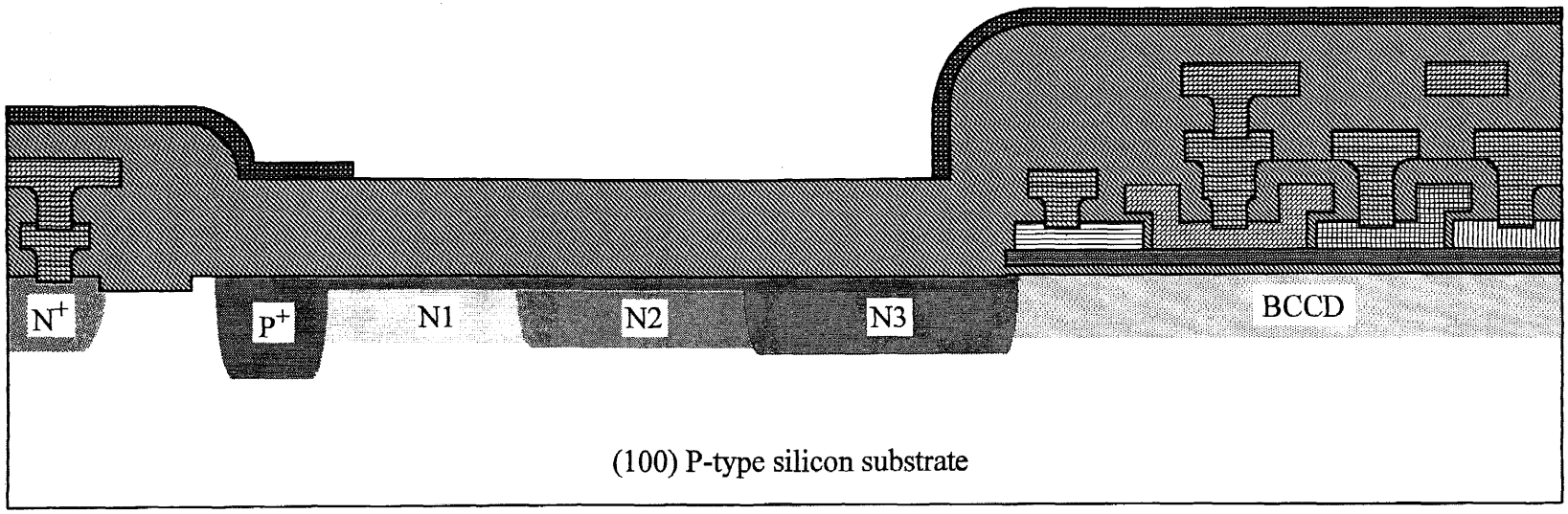
35. Deposit flow glass (BPSG: borosilica phosphorus glass).
36. Etch flow glass (oxide), open contacts (metal-1 to polysilicon gates and metal-1 to drains).
37. Glass reflow.
38. Deposit metal-1 layer.
39. Etch metal-1(form metal-1 lines).



40. Deposit interlevel-1 flow glass.
41. Etch flow glass, open VIAs (metal-2 to metal-1 interconnection).
42. Glass reflow.
43. Deposit metal-2 layer.
44. Etch metal-2 (form metal-2 lines).



45. Deposit interlevel-2 flow glass.
46. Glass reflow.
47. Deposit metal-3 layer.
48. Etch metal-3 (for optical shield).
49. Opening of bond pads by etched through interlevel-2 is not shown in drawing.



APPENDIX C

DESIGN AND SIMULATION OF LARGE HIGH-SPEED PHOTODETECTOR

C.1 Design of Large Photodetector

To achieve higher sensitivity for the available optical signal in wind-tunnel applications, development of VHFR burst-image sensor with larger macropixels allowing large fill factor were considered. The macropixels considered had areas of 100x50 μm^2 and 100x100 μm^2. For the macropixel with 100x50 μm^2 area, the size of the photodetector has been increased by reducing the horizontal direction resolution of the imager by a factor of 2 and keeping the vertical direction resolution of the imager unchanged, then the image sensor array contains with 180x360 pixels, and the number of storage units in each macropixel will remain unchanged (in other words, the design of the charge storage area in each macropixel remains unchanged).

Figure C.1 shows a layout of the 100x50 μm^2 macropixel with a large photodetector. In this design, the position of collecting gate related to the SP register remains unchanged. The photodetector of this macropixel has an area of 2,250 μm^2 and results in a fill factor of 45%. However, the maximum distance for charge transfer in the photodetector is about 78 μm, which is much longer than that of the photodetector design shown in Figure 7.1 (to be referred to *small photodetector*). Obviously, in order to obtain a short readout time, more N-type implants have to be used in the construction of the large photodetector.

A second choices for a layout of 100x50 μm^2 macropixel with a large photodetector is shown in Figure C.2. In this design, the charge collecting well is located in the middle portion of the photodetector, and the size of the photodetector is approximately 2,000 μm^2 with the length and width of approximately 65 μm and 33 μm, respectively. The fill factor in this case is 40%. The maximum charge transfer distance in

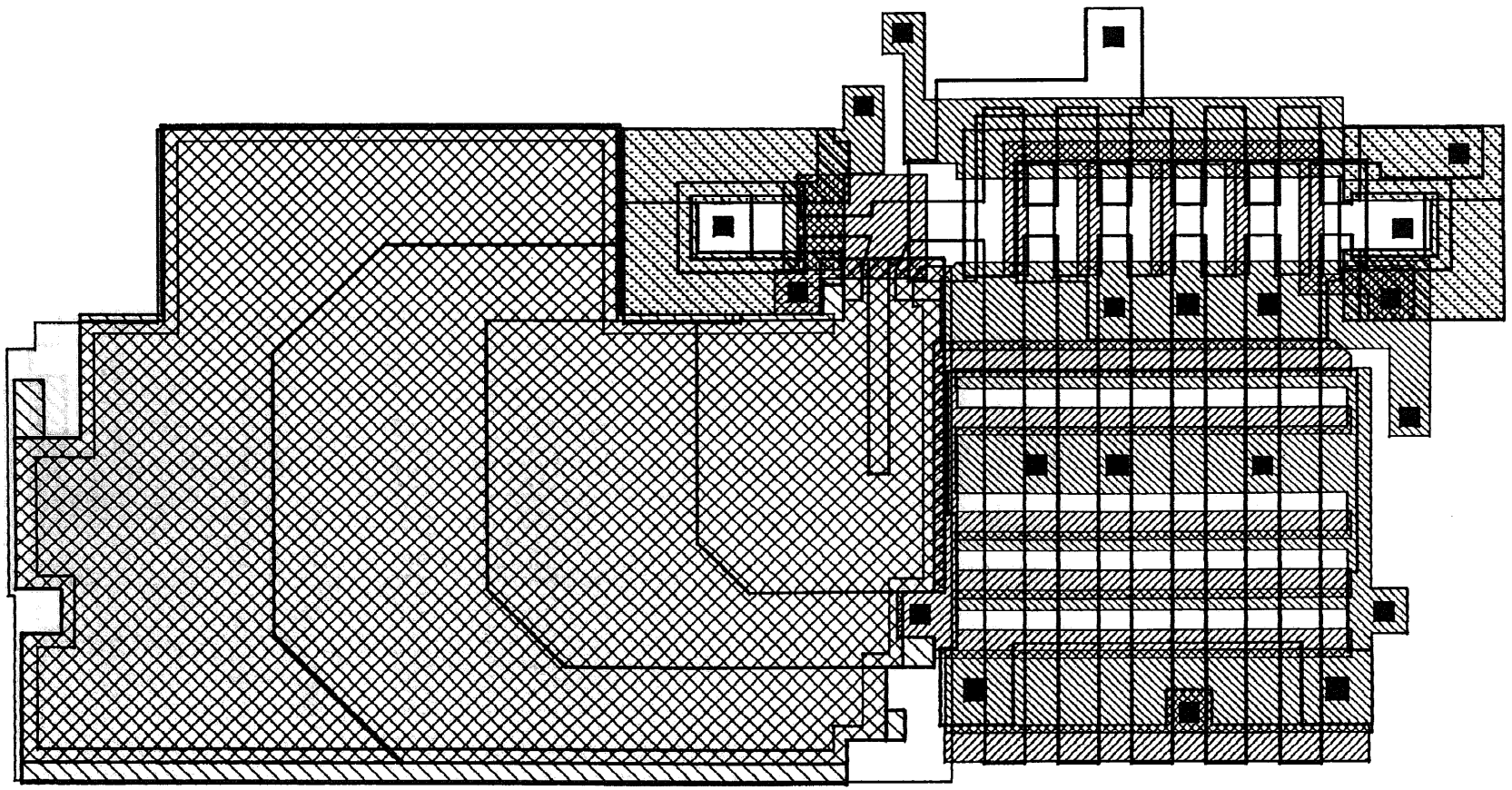


Figure C.1 *Checkplot of 100-μmx50-μm macropixel with fill factor of 45%.*

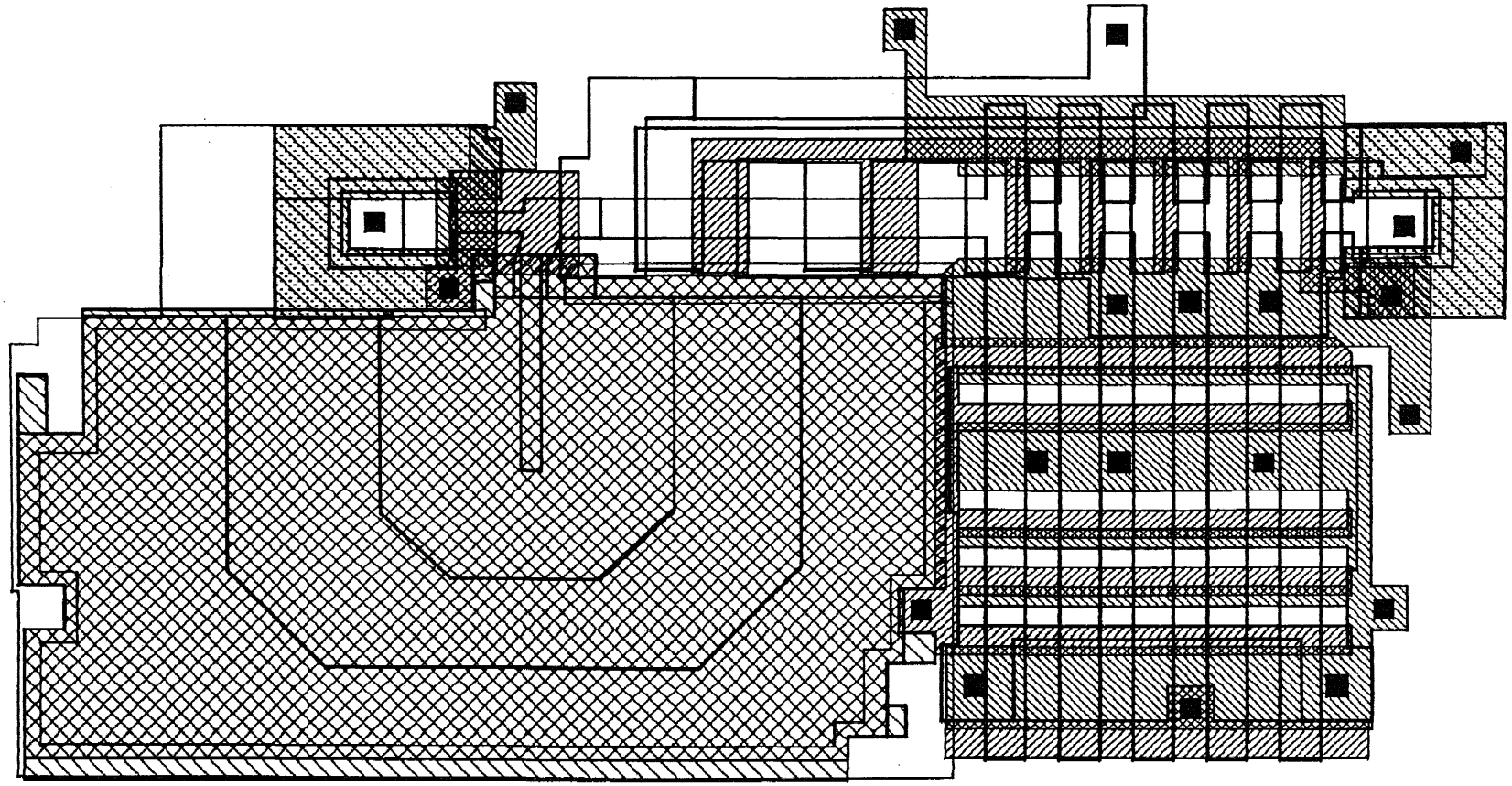


Figure C.2 *Checkplot of 100-μmx50-μm macropixel with fill factor of 40%.*

this photodetector is approximately 45 μm which is about 35% longer than that in the small photodetector.

C.2 2-D Simulation of the Large Photodetector

To investigate the effect of the N-type photodetector implants on the time response of the large photodetector to the step illuminations and the channel charge decay in the large photodetector after the illumination is cut off, different numbers of N-type implants have been considered for the large photodetector with the geometry shown in Figure C.1. We have simulated the time response to the step illuminations and the channel charge decay in the large photodetector after the illumination is cut off of the large photodetector with one (M = 1), two (M = 2), three (M = 3), four (M = 4), five (M = 5), six (M = 6), and seven M = 7) N-type implants.

For the large photodetector such as shown in Figures C1, the highest N-doped region of the photodetector is in the form of a narrow strip to allow a fast transfer of electrons from photodetector to charge collecting well. In the simulation of the large photodetector, the length of the maximum charge transferring path is about 78 μm. In the simulation of the large photodetector with single N-type implant, the photodetector is assumed to have a constant potential region which is equal to the maximum charge transfer distance in the photodetector. On the other hand, for the purpose of simulation of large photodetector with two to seven N-type implants, the first constant potential region next to the charge collecting well is assumed to be 1.5-μm wide with effective length of 6 μm. The remaining N-type implants are considered to correspond to optimally selected the charge transfer distances for the maximum length of the photodetector. That means the lengths of the constant potential segments in the photodetector are equal to 72 μm divided by 1, 2, 3, 4, 5, and 6 for the two, three, four, five, six, and seven N-type implants, respectively.

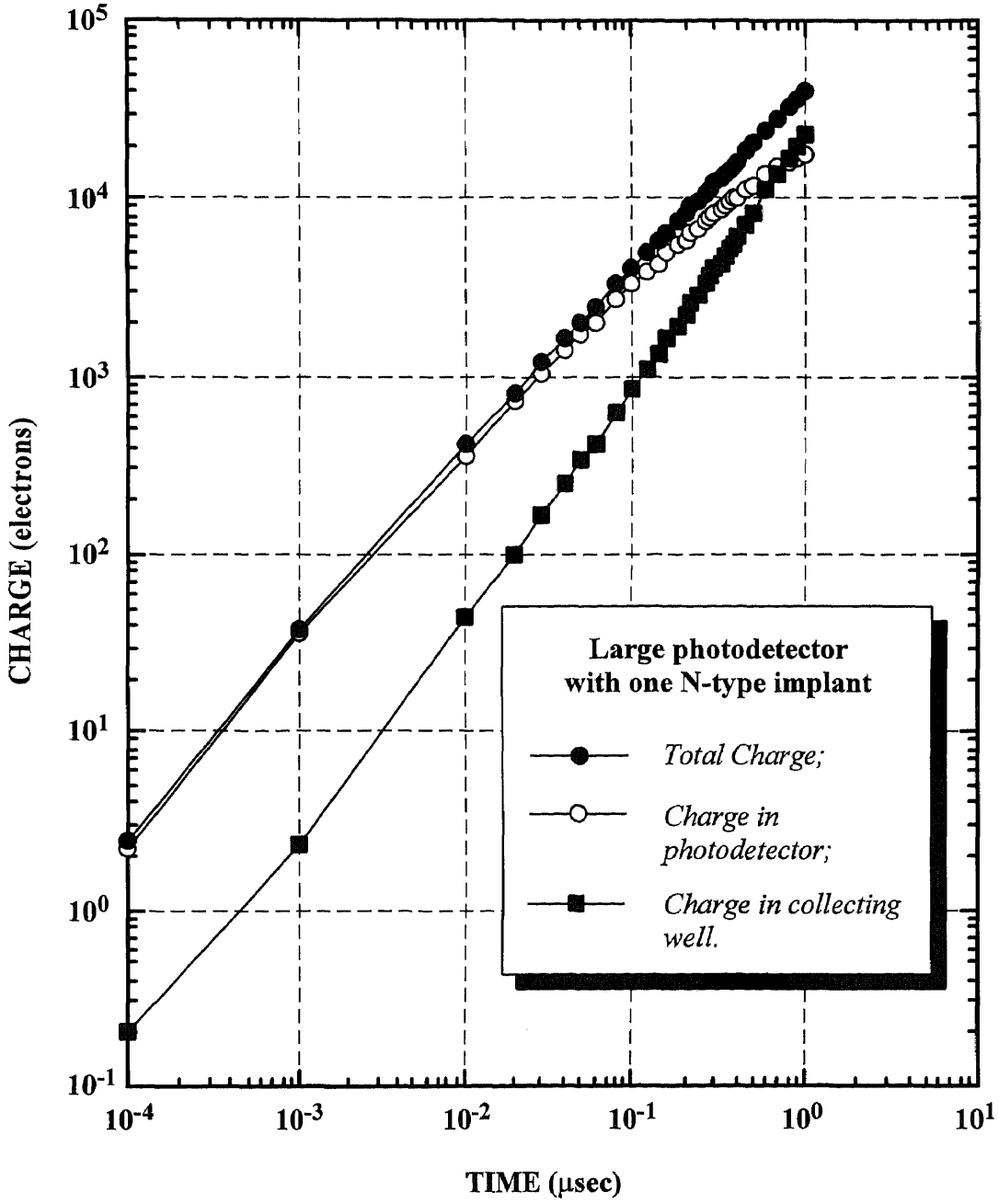
C.2.1 Time Response of the Large Photodetector to Step Illumination Signal

Large Photodetector with One and Two N-type Implants

The large photodetector with one N-type implant (photodetector-1) is assumed to be composed of a constant potential region about 78-μm long. Figures C.3, C.4, and C.5 illustrate the time response of the photodetector-1 to the illumination signals. The illumination intensities are assumed corresponded to a detected signal of 20,000 electrons for illumination time of 0.5 μsec, 1.0 μsec, and 2.0 μsec shown in Figures C.3, C.4, and C.5, respectively.

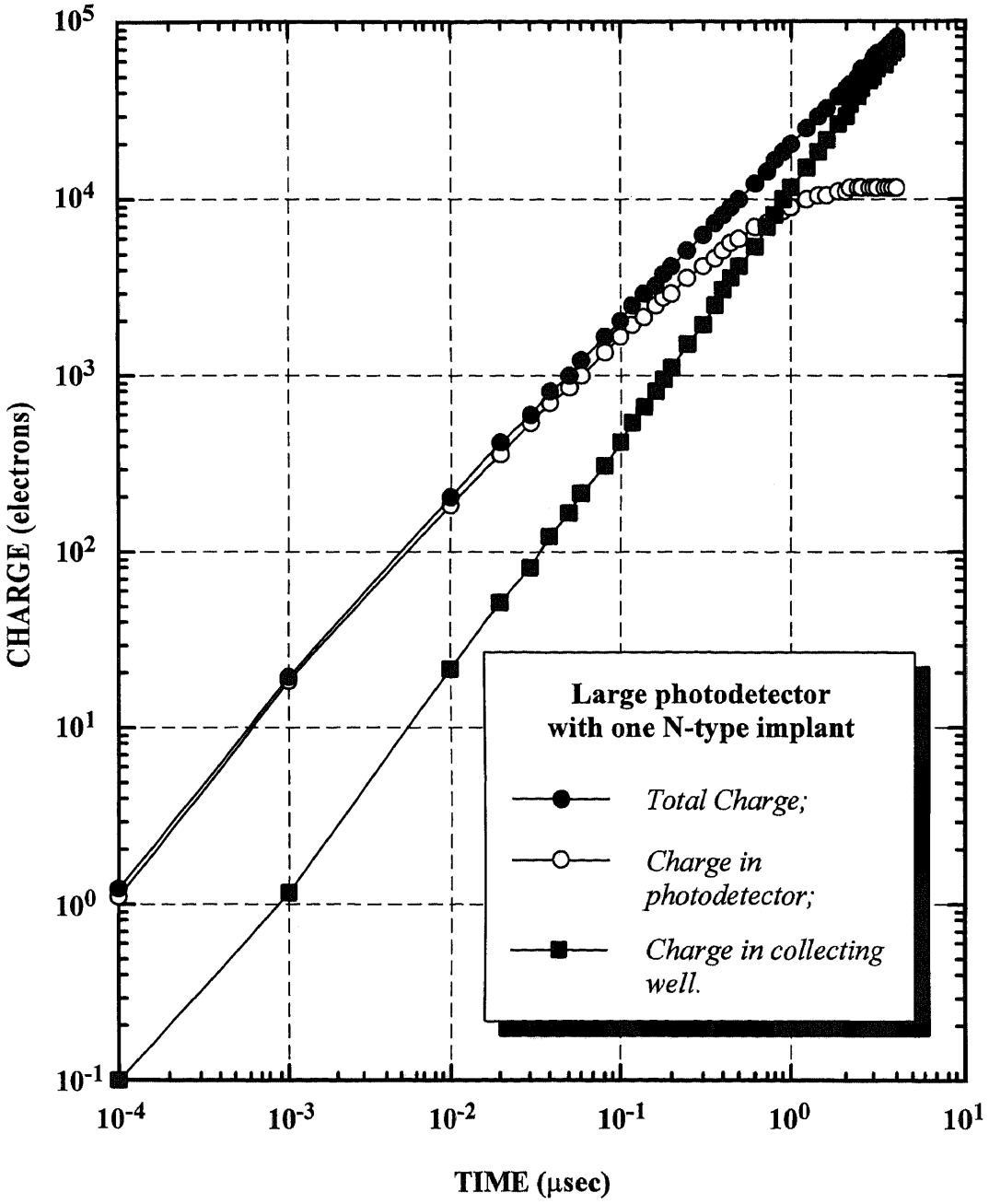
An inspection of Figures C.3, C.4, and C.5 indicated that the photodetector channel charges do not reached a steady-state saturation level when the optical integration time is completed. The photodetector channel charge reaches values about 12,000, 9,000, and 5,700 electrons for the illumination intensities corresponding to total detected signal charge of 20,000 electrons for the optical integration time of 0.5 μsec, 1.0 μsec, and 2.0 μsec, respectively. On the other hand, Figures C.4 and C.5 also shows that, the channel charge in the photodetector-1 will reach about 99% of its steady-state saturation level in about 3 μsec. However, the total detected signal charge in these cases will be more than 20,000 electrons for the considered illumination intensities and time.

Similar simulation results are presented in Figures C.6, C.7 and C.8 for large photodetector with two N-type implants (photodetector-2). As indicated before, in this case the second N-type implant is introduced in the form of 1.5-μm wide and about 15-μm long channel to assure a complete charge transfer out of photodetector without a barrier potential at the junction with the BCCD charge collecting well. The effective length of this narrow second implant for the purpose of simulation was assumed to be 6.0 μm and the other constant potential segment is assumed to be 72-μm long. Therefore, there is expected to be essentially no significant difference in the response time of the photodetectors with one and two N-type implants shown Figures C.6, C.7, and C.8.



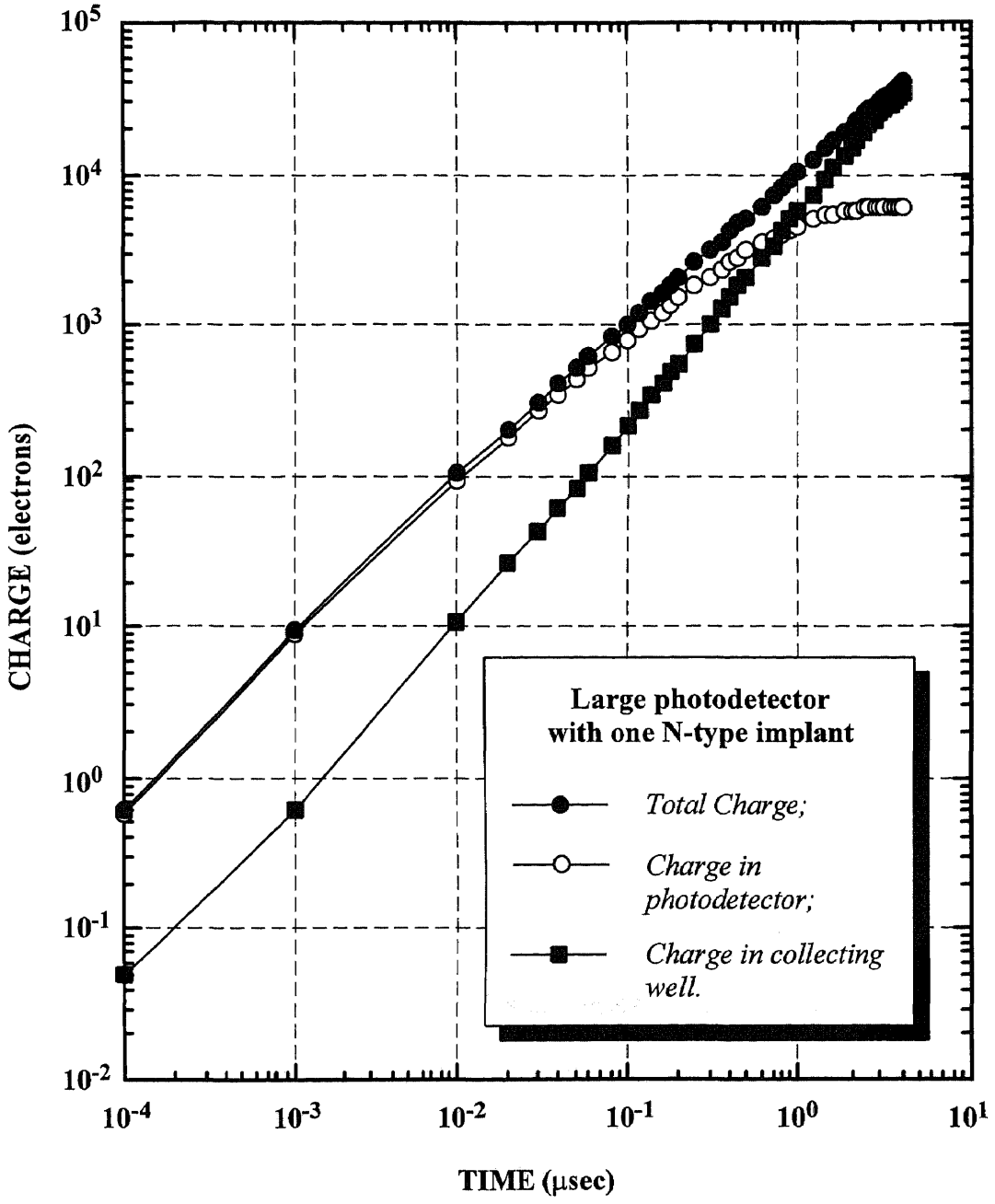
(Illumination intensity: 20,000 electrons in 0.5 μsec)

Figure C.3 *Time response of the large photodetector with single N-type implant to a step illumination corresponding to 20,000 electrons in 0.5 μsec.*



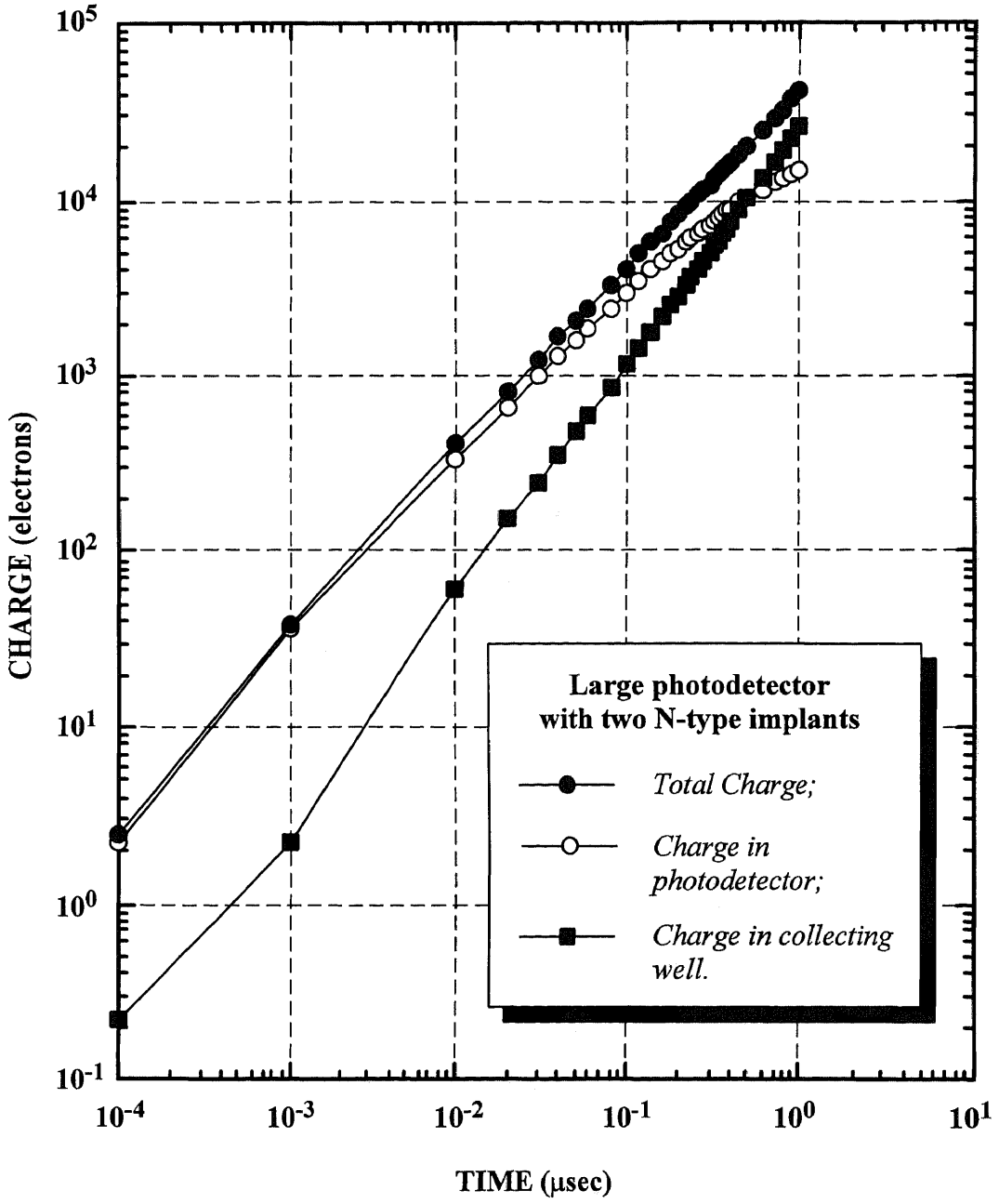
(Illumination intensity: 20,000 electrons in 1.0 μsec)

Figure C.4 *Time response of the large photodetector with single N-type implant to a step illumination corresponding to 20,000 electrons in 1.0 μsec.*



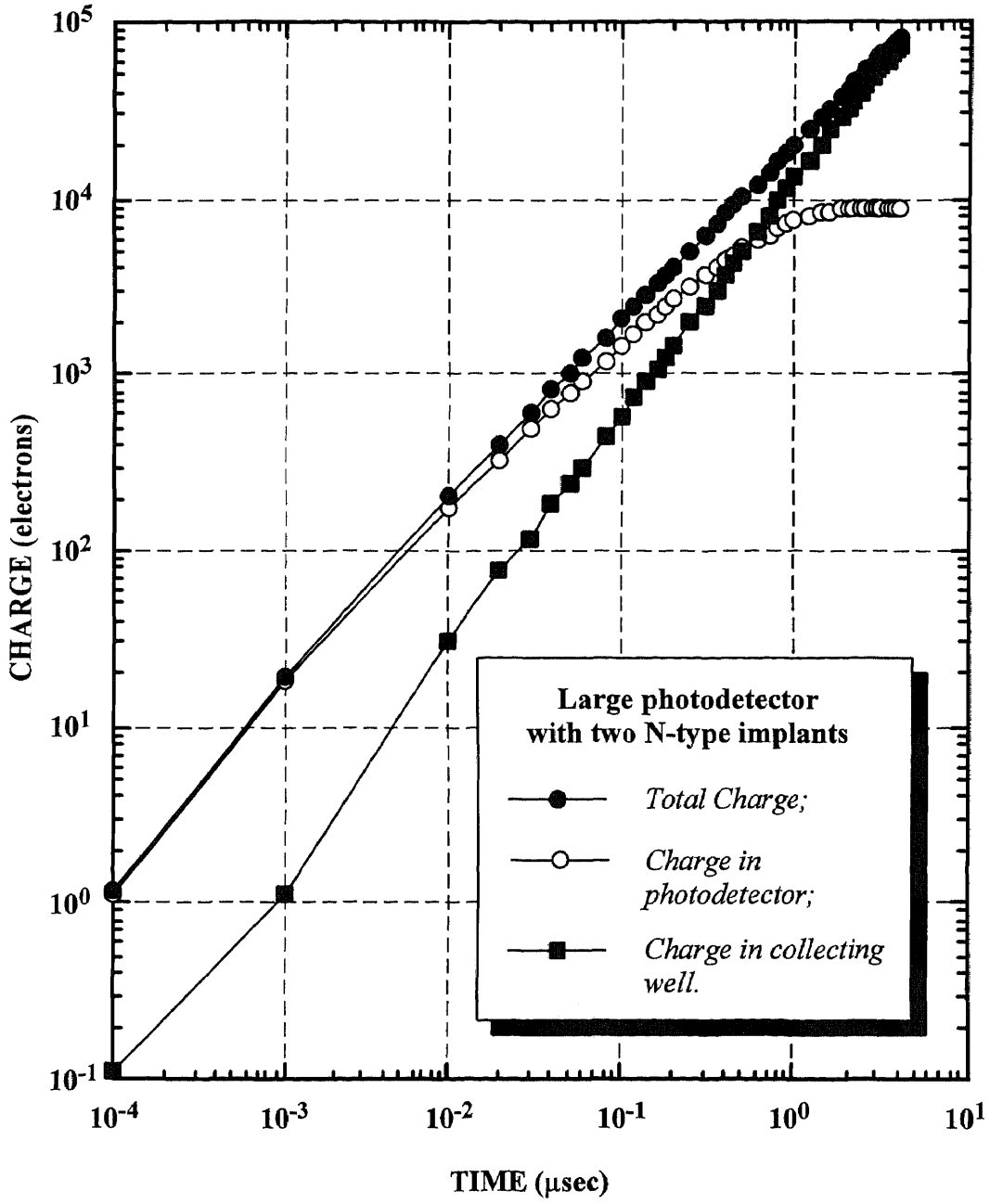
(Illumination intensity: 20,000 electrons in 2.0 μsec)

Figure C.5 *Time response of the large photodetector with single N-type implant to a step illumination corresponding to 20,000 electrons in 2.0 μsec.*



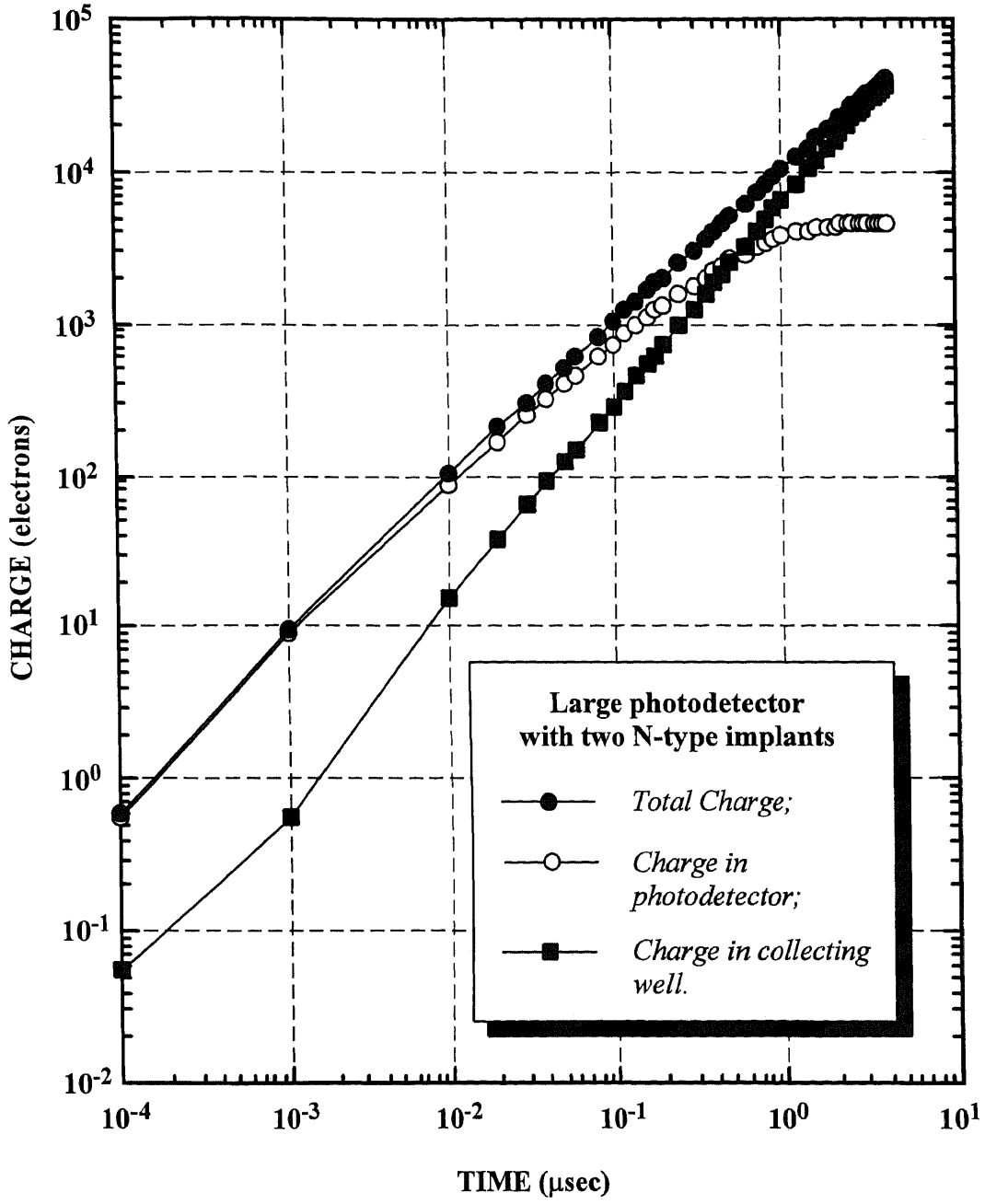
(Illumination intensity: 20,000 electrons in 0.5 μsec)

Figure C.6 *Time response of the large photodetector with two N-type implants to a step illumination corresponding to 20,000 electrons in 0.5 μsec.*



(Illumination intensity: 20,000 electrons in 1.0 μsec)

Figure C.7 *Time response of the large photodetector with two N-type implants to a step illumination corresponding to 20,000 electrons in 1.0 μsec.*



(Illumination intensity: 20,000 electrons in 2.0 μsec)

Figure C.8 *Time response of the large photodetector with two N-type implants to a step illumination corresponding to 20,000 electrons in 2.0 μsec.*

Large Photodetectors with Three-to-Seven N-Type Implants

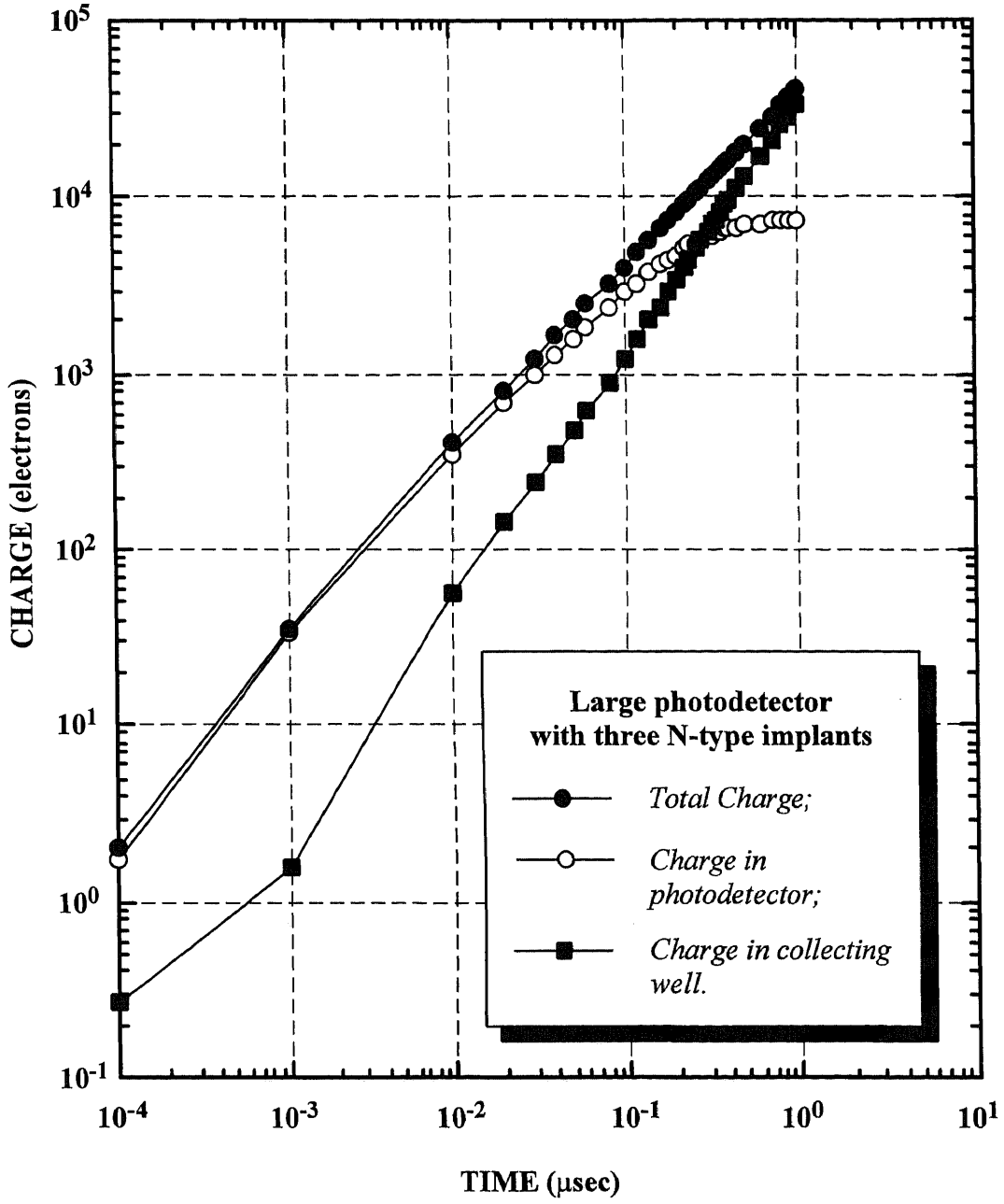
The simulation results for the response as function of time for large Photodetectors with three, four, five, six, and seven N-type implants to illumination intensities corresponding to total detected signal charge of 20,000 electrons in 0.5, 1.0, and 2.0 μsec are presented in Figures C.9 to C.11, C.12 to C.14, C.15 to C.17, C.18 to C.20, and C.21 to C.23, respectively.

Inspection of above figures indicated that the response time at which the photodetector channel charge reaches about 99% of its steady-state saturation level is about 0.7, 0.35, 0.25, 0.15, and 0.1 μsec for large photodetector with three, four, five, six, and seven N-type implants, respectively.

C.2.2 Charge Decay in the Large Photodetector

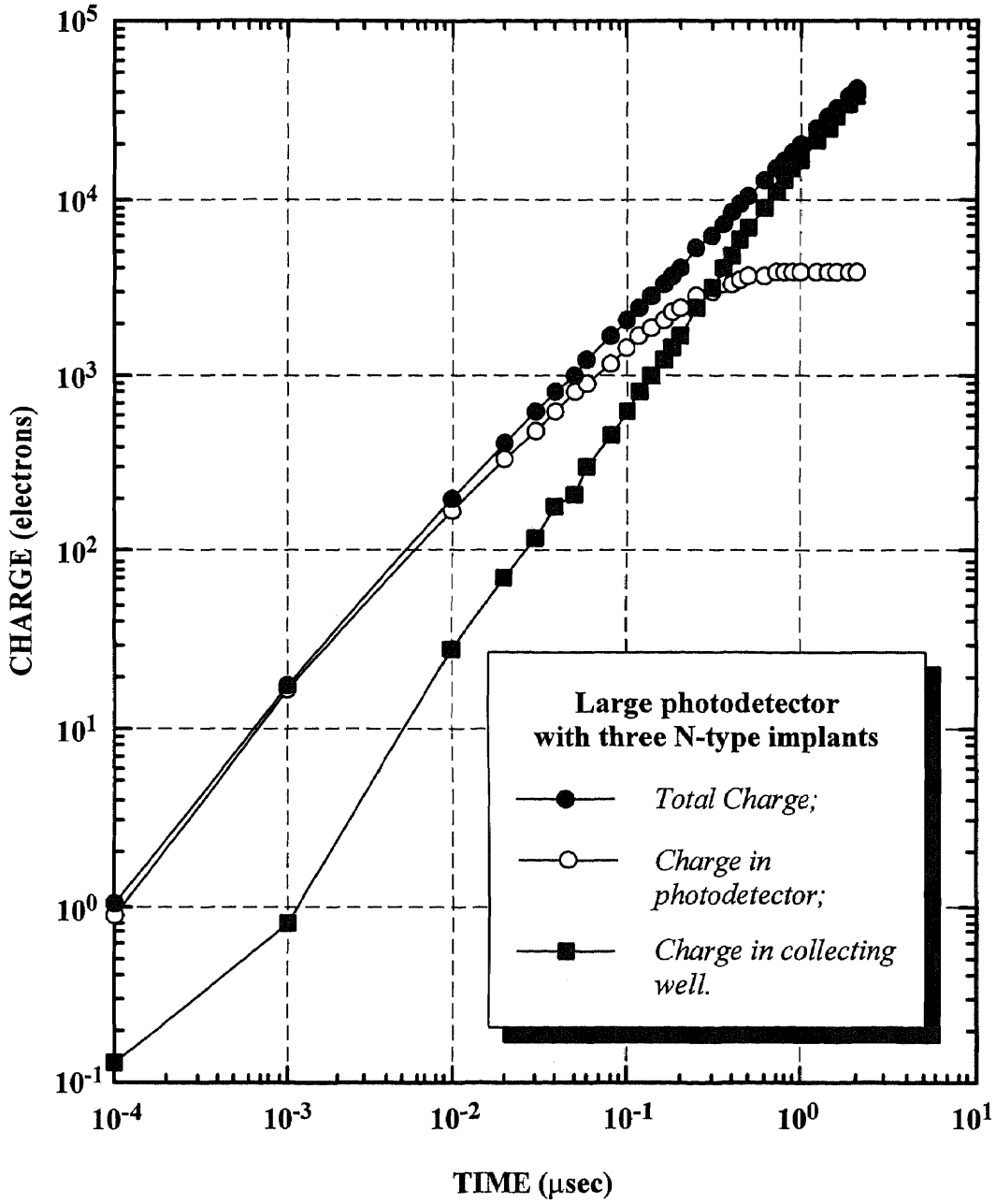
Similarly to the small photodetector, after the optical illumination is cut off, the channel charge in the large photodetector with one to seven N-type implants will be transferred to the charge collecting well which is operated at a more positive channel potential level. Simulation data presented in Figures C.24 to C.33 shows that the decay time ($t_{1.0\%}$) of the photodetector channel charge is dependent on the number of photodetector implants. The decay time is defined as the at which the photodetector channel charge decays to about less than 1% of its value at the end of optical illumination.

Figures C.24, C.25, C.26, C.27, C.28, C.29, and C.30 illustrate the decay of the photodetector channel charge in the large photodetector with one, two, three, four, five, six, and seven N-type implants, respectively, after the optical illumination is stopped. The three curves in Figures C.24 to C.30 correspond to three illumination intensities that result in integration of 20,000 electrons in 0.5 μsec, 1.0 μsec, and 2.0 μsec, respectively. As indicated before, after the optical illumination is stopped, the detector channel charges in photodetector-1 and photodetector-2 for all of the three illumination intensities, and the detector channel charge in the large photodetector with three N-type implants for the



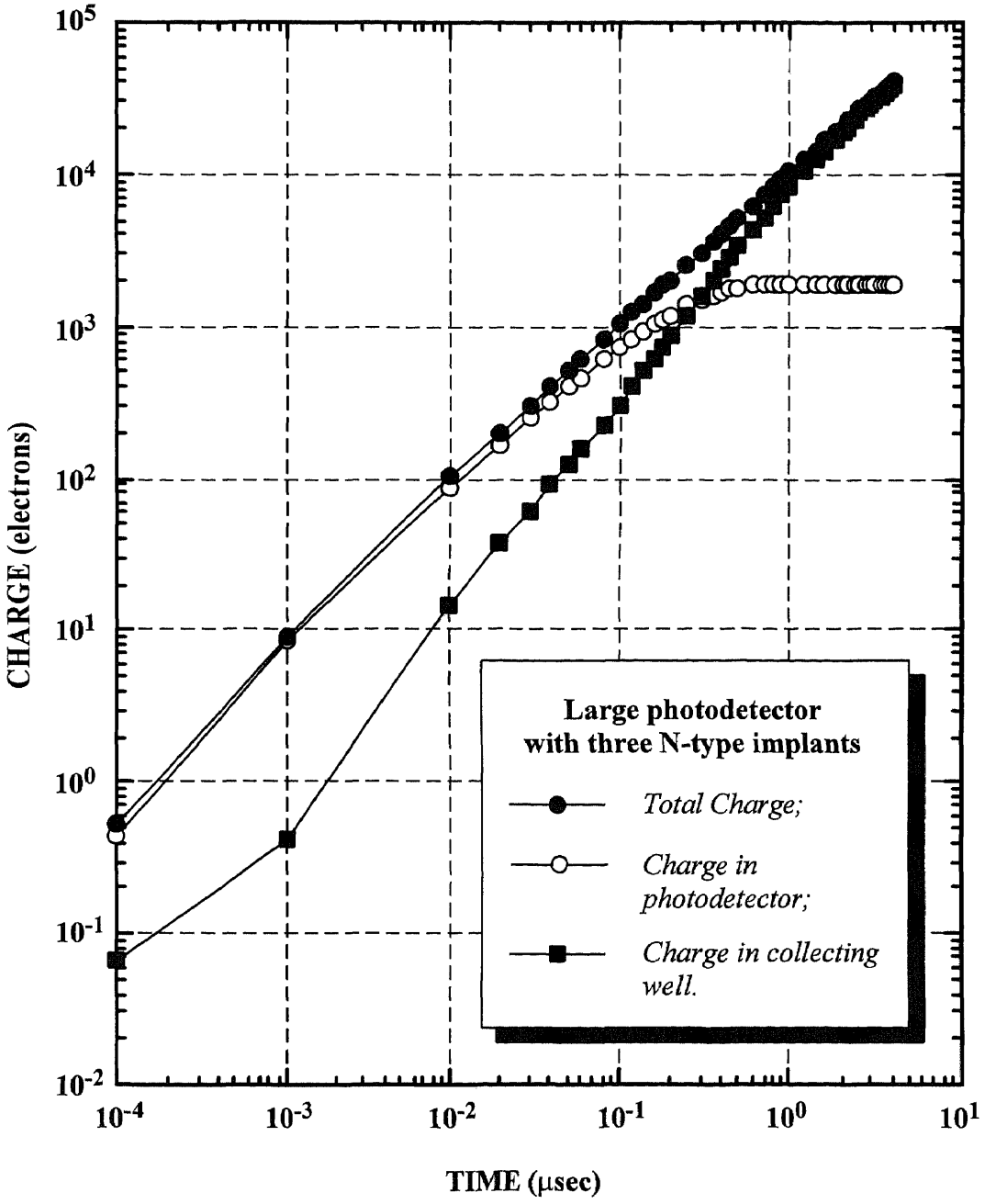
(Illumination intensity: 20,000 electrons in 0.5 μsec)

Figure C.9 *Time response of the large photodetector with three N-type implants to a step illumination corresponding to 20,000 electrons in 0.5 μsec.*



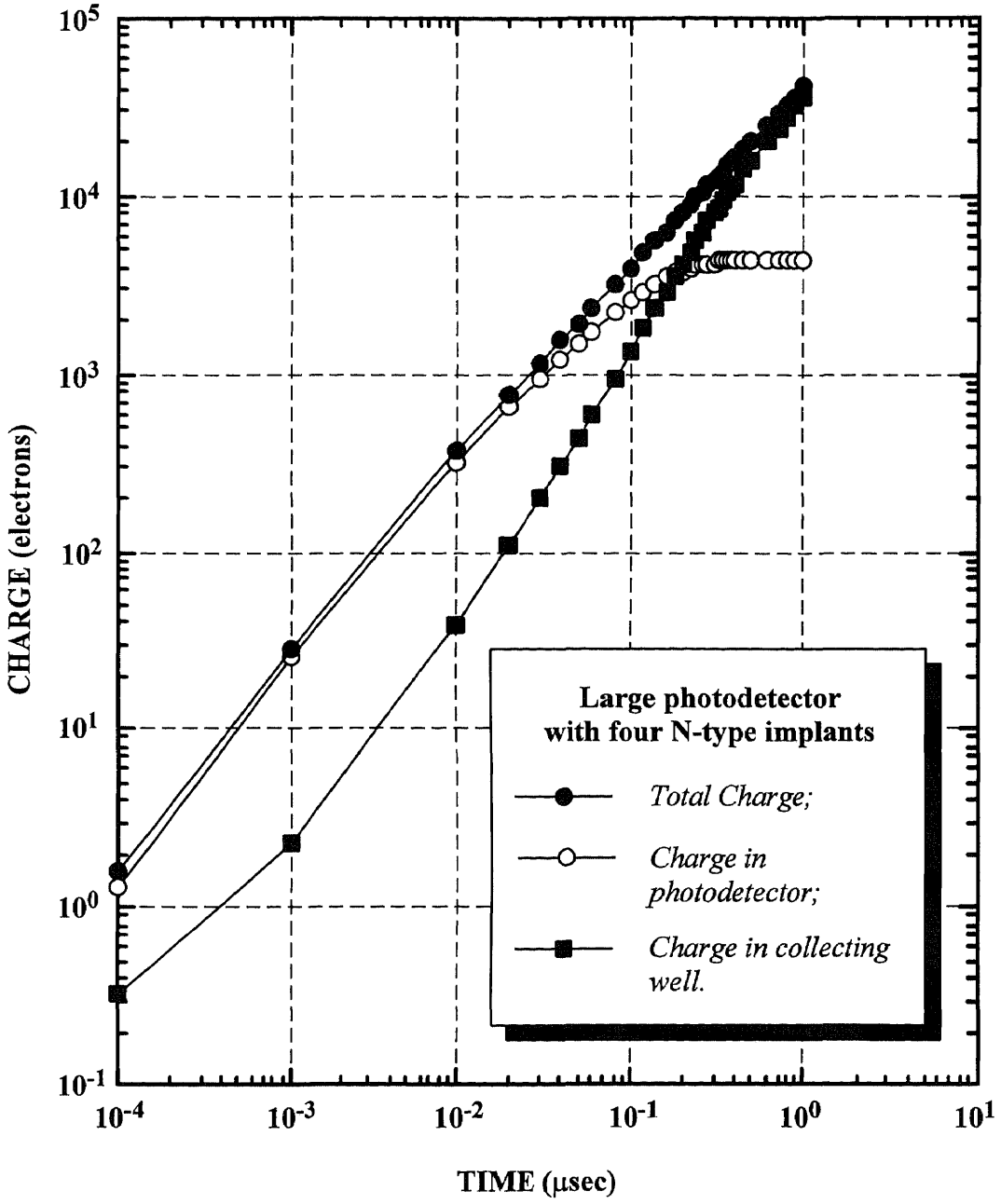
(Illumination intensity: 20,000 electrons in 1.0 μsec)

Figure C.10 *Time response of the large photodetector with three N-type implants to a step illumination corresponding to 20,000 electrons in 1.0 μsec.*



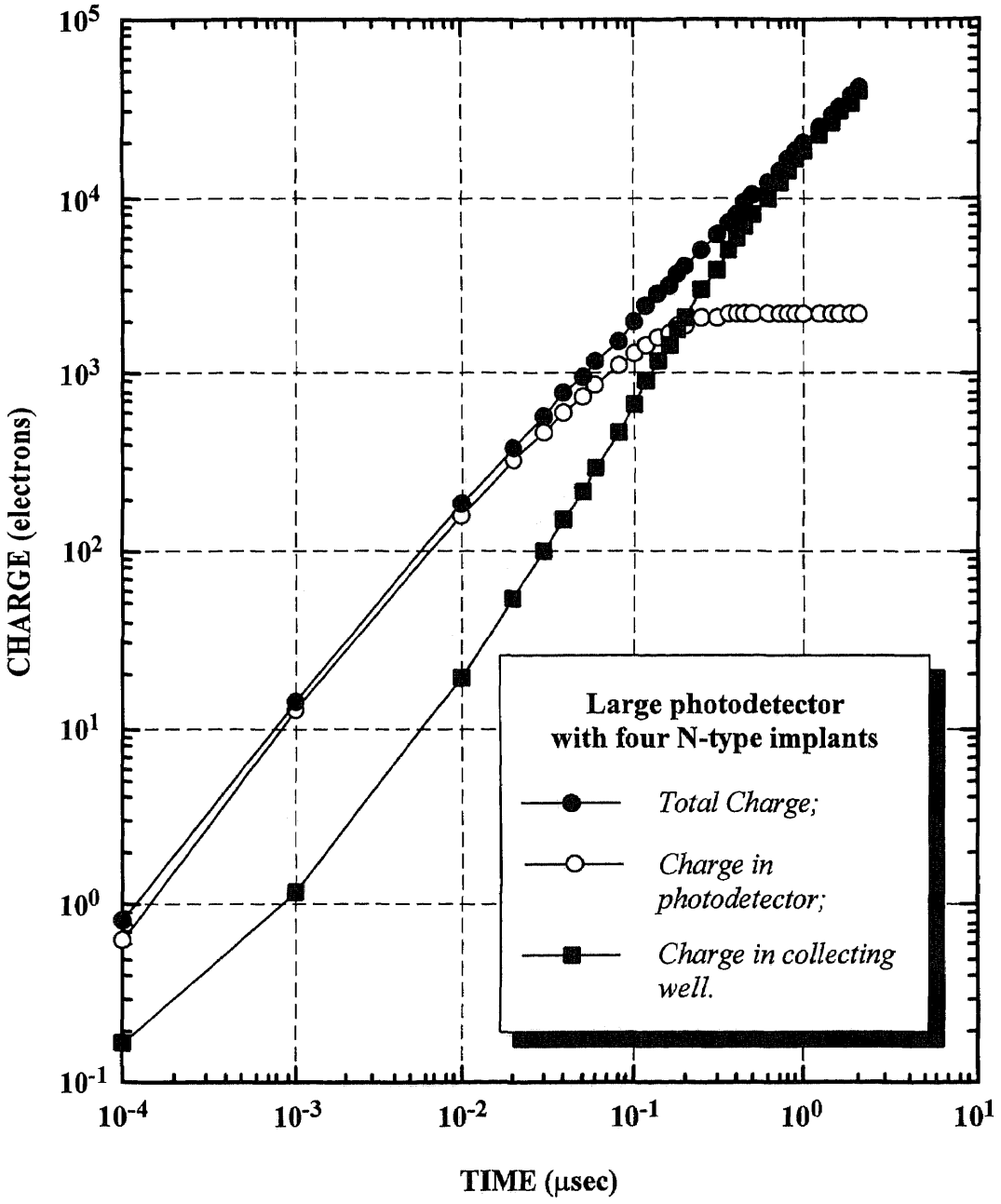
(Illumination intensity: 20,000 electrons in 2.0 μsec)

Figure C.11 *Time response of the large photodetector with three N-type implants to a step illumination corresponding to 20,000 electrons in 2.0* μsec.



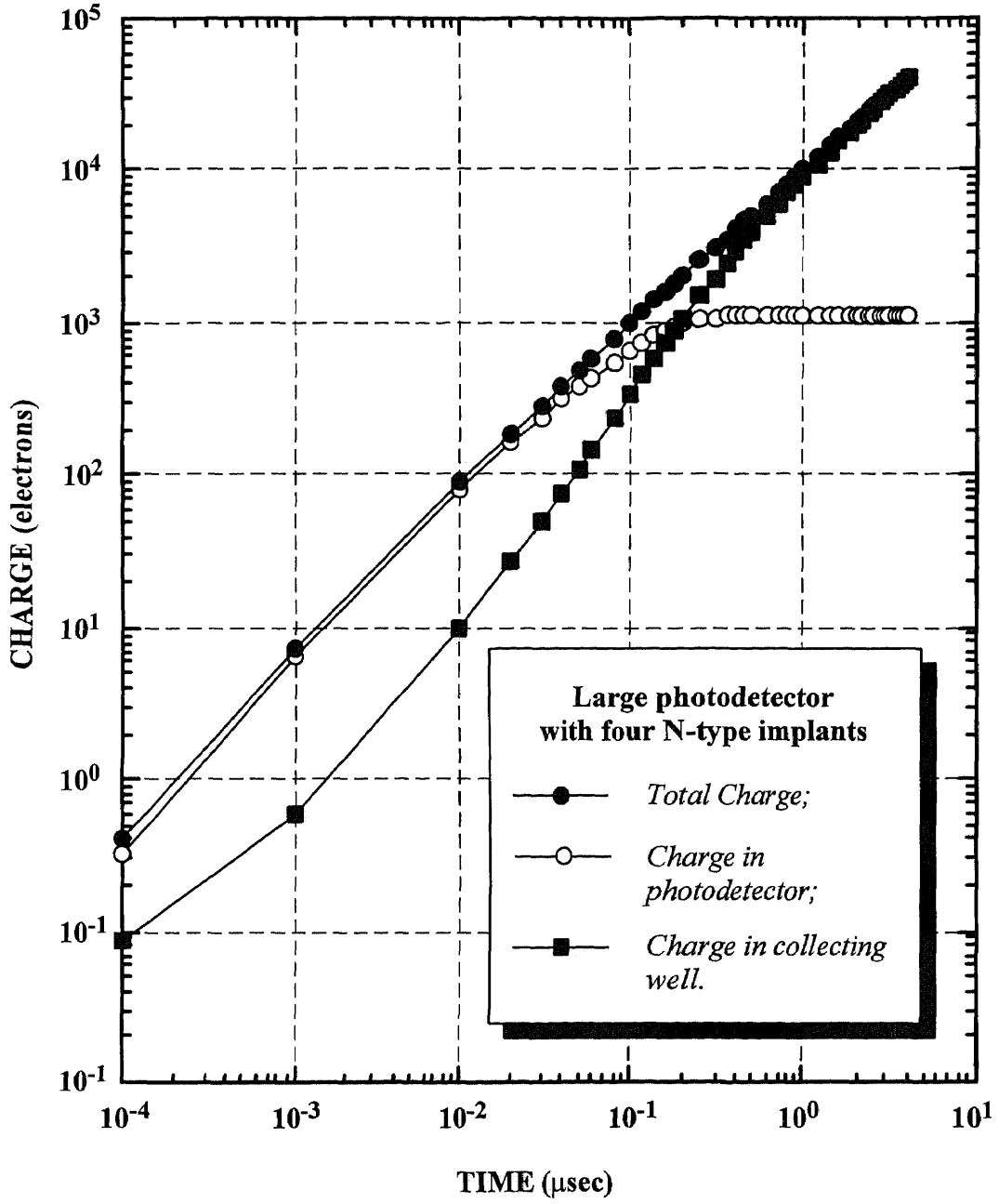
(Illumination intensity: 20,000 electrons in 0.5 μsec)

Figure C.12 *Time response of the large photodetector with four N-type implants to a step illumination corresponding to 20,000 electrons in 0.5 μsec.*



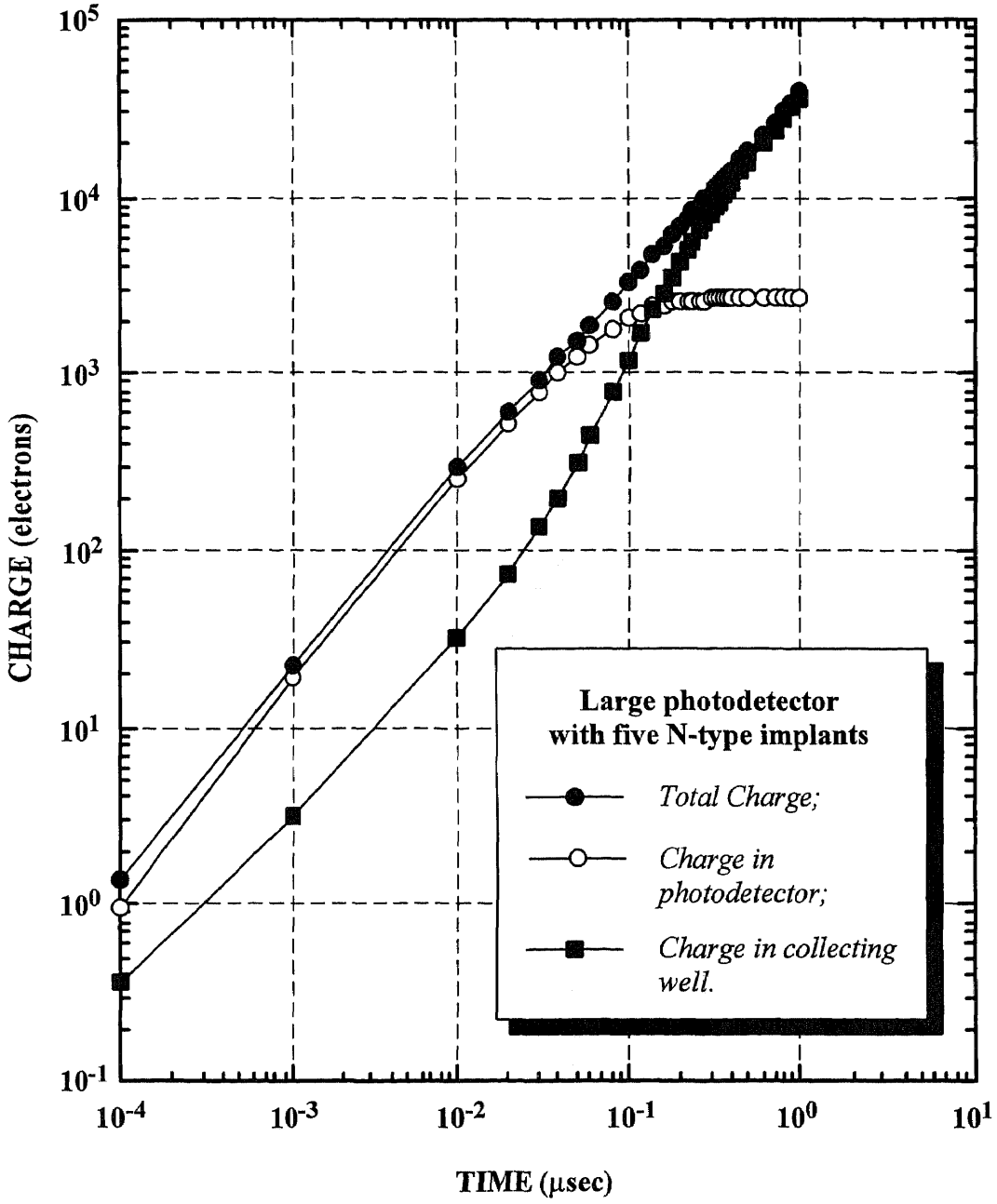
(Illumination intensity: 20,000 electrons in 1.0 μsec)

Figure C.13 *Time response of the large photodetector with four N-type implants to a step illumination corresponding to 20,000 electrons in 1.0 μsec.*



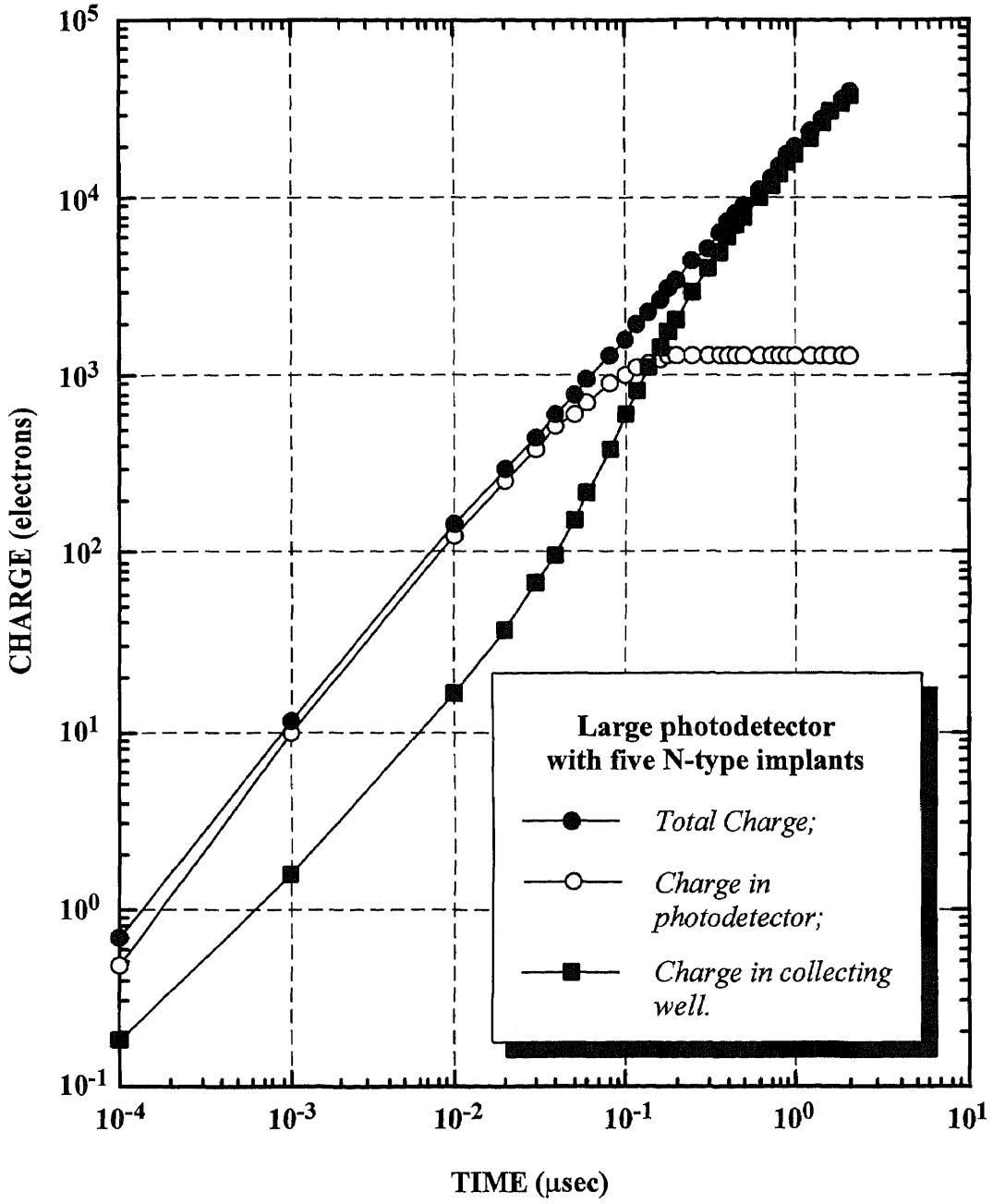
(Illumination intensity: 20,000 electrons in 2.0 μsec)

Figure C.14 *Time response of the large photodetector with four N-type implants to a step illumination corresponding to 20,000 electrons in 2.0 μsec.*



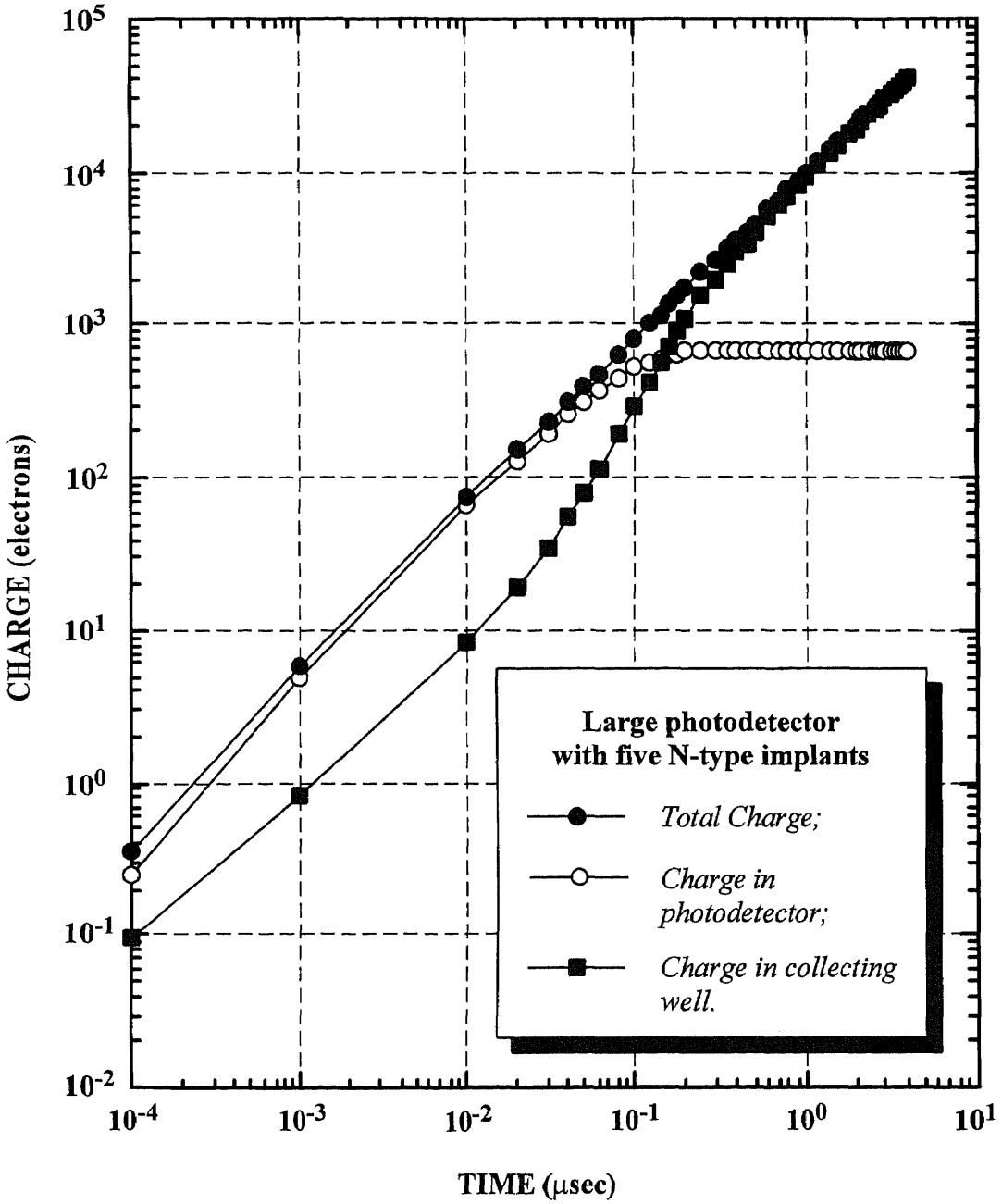
(Illumination intensity: 20,000 electrons in 0.5 μsec)

Figure C.15 *Time response of the large photodetector with five N-type implants to a step illumination corresponding to 20,000 electrons in 0.5 μsec.*



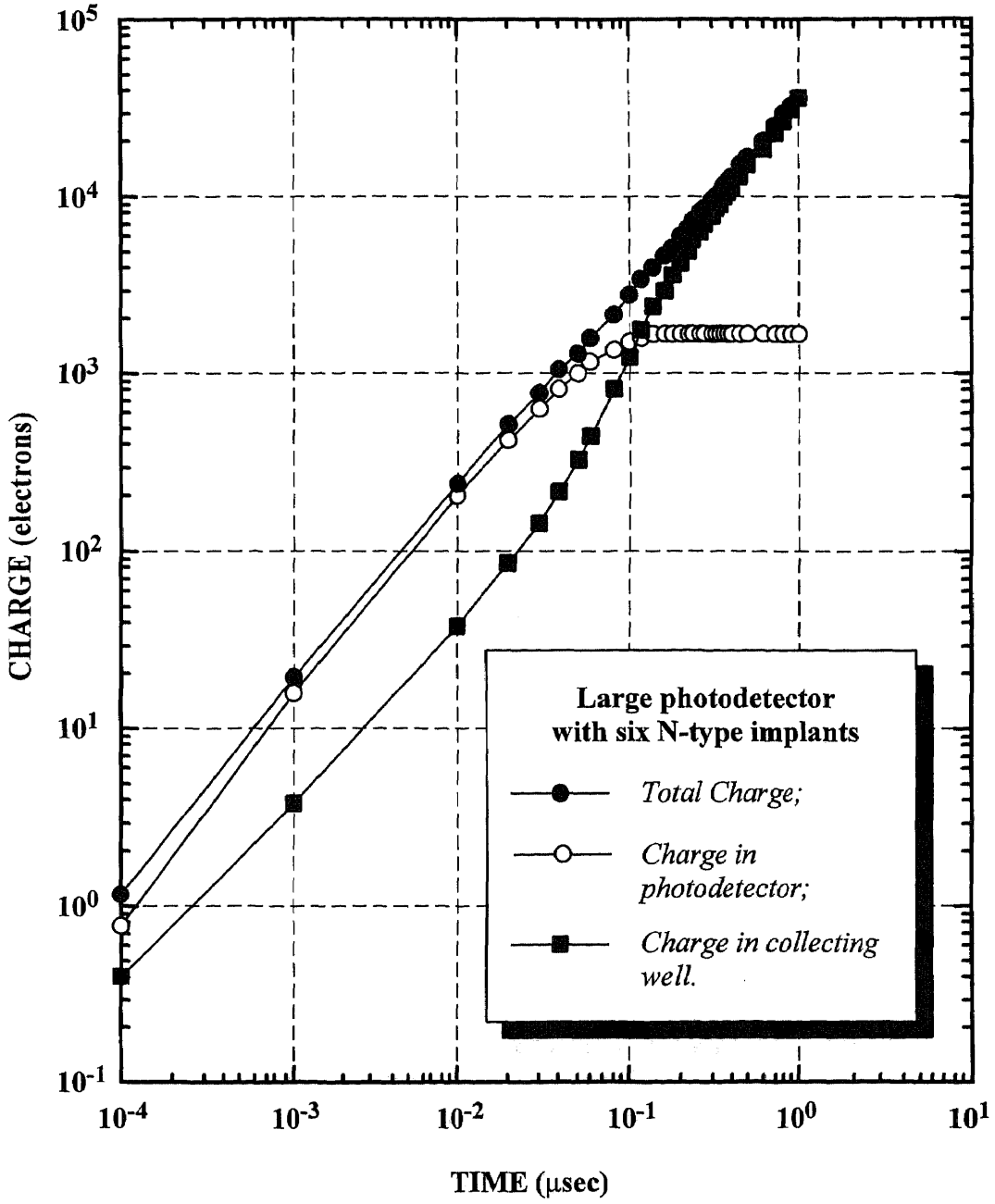
(Illumination intensity: 20,000 electrons in 1.0 μsec)

Figure C.16 *Time response of the large photodetector with five N-type implants to a step illumination corresponding to 20,000 electrons in 1.0 μsec.*



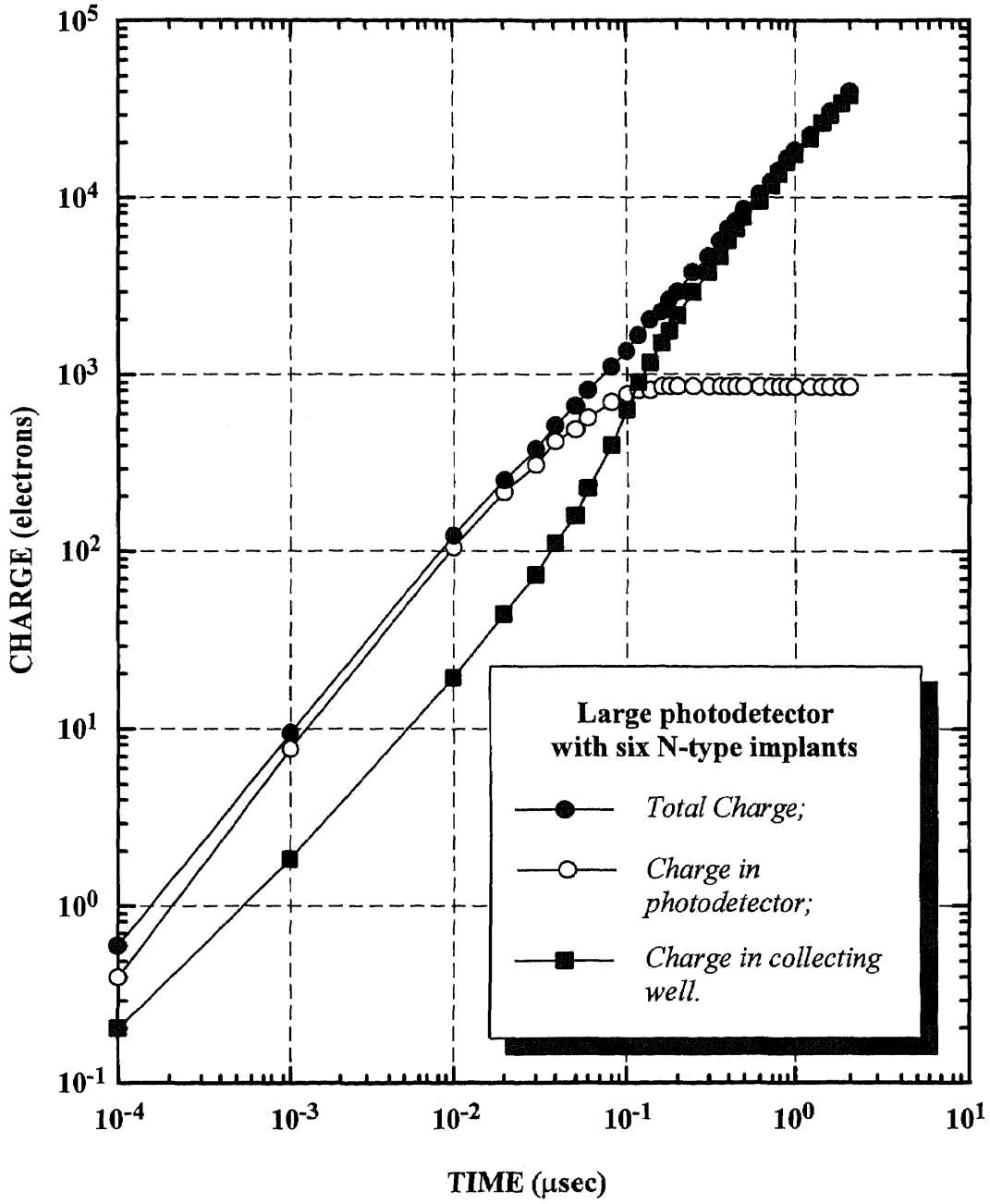
(Illumination intensity: 20,000 electrons in 2.0 μsec)

Figure C.17 *Time response of the large photodetector with five N-type implants to a step illumination corresponding to 20,000 electrons in 2.0 μsec.*



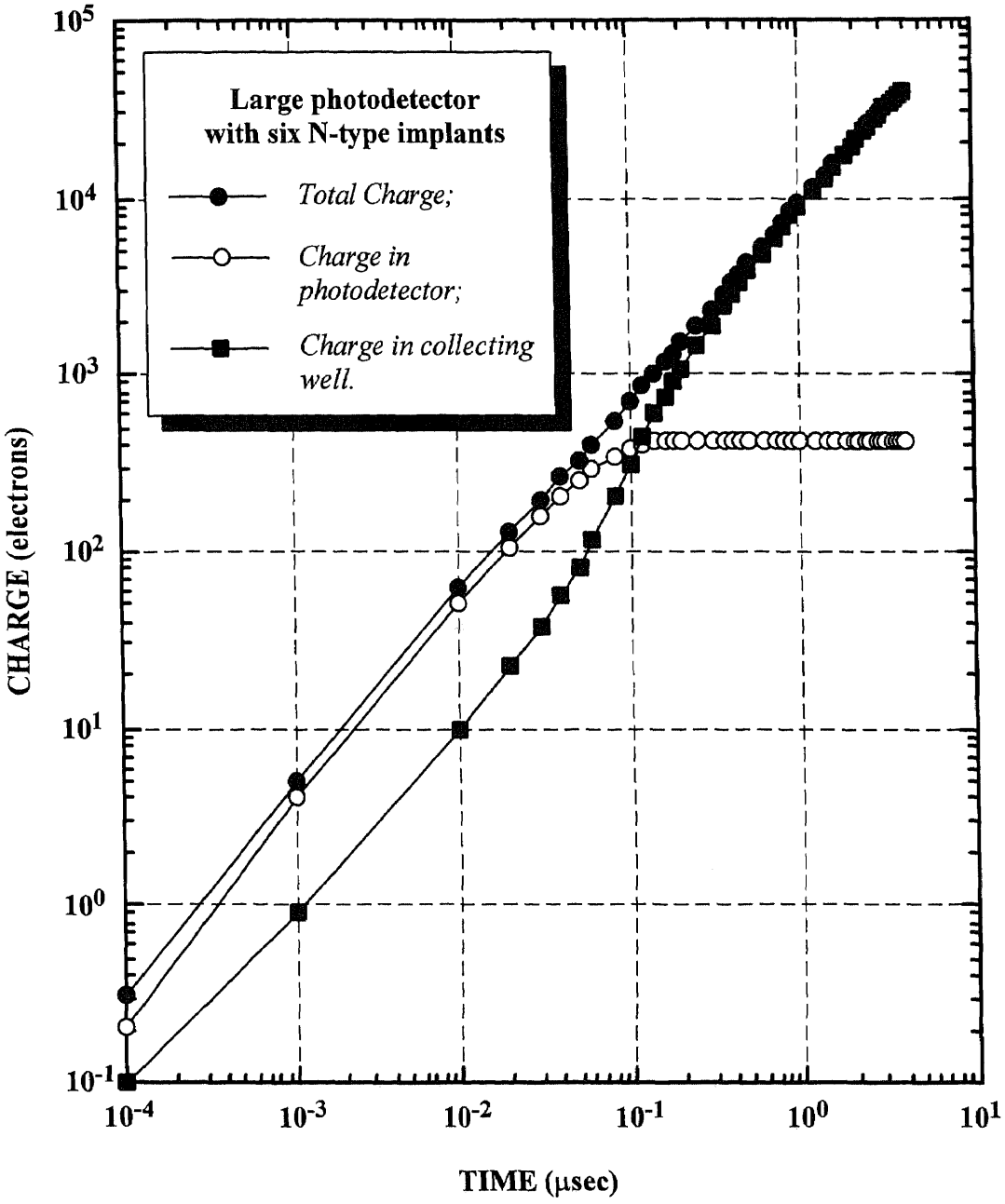
(Illumination intensity: 20,000 electrons in 0.5 μsec)

Figure C.18 *Time response of the large photodetector with six N-type implants to a step illumination corresponding to 20,000 electrons in 0.5 μsec.*



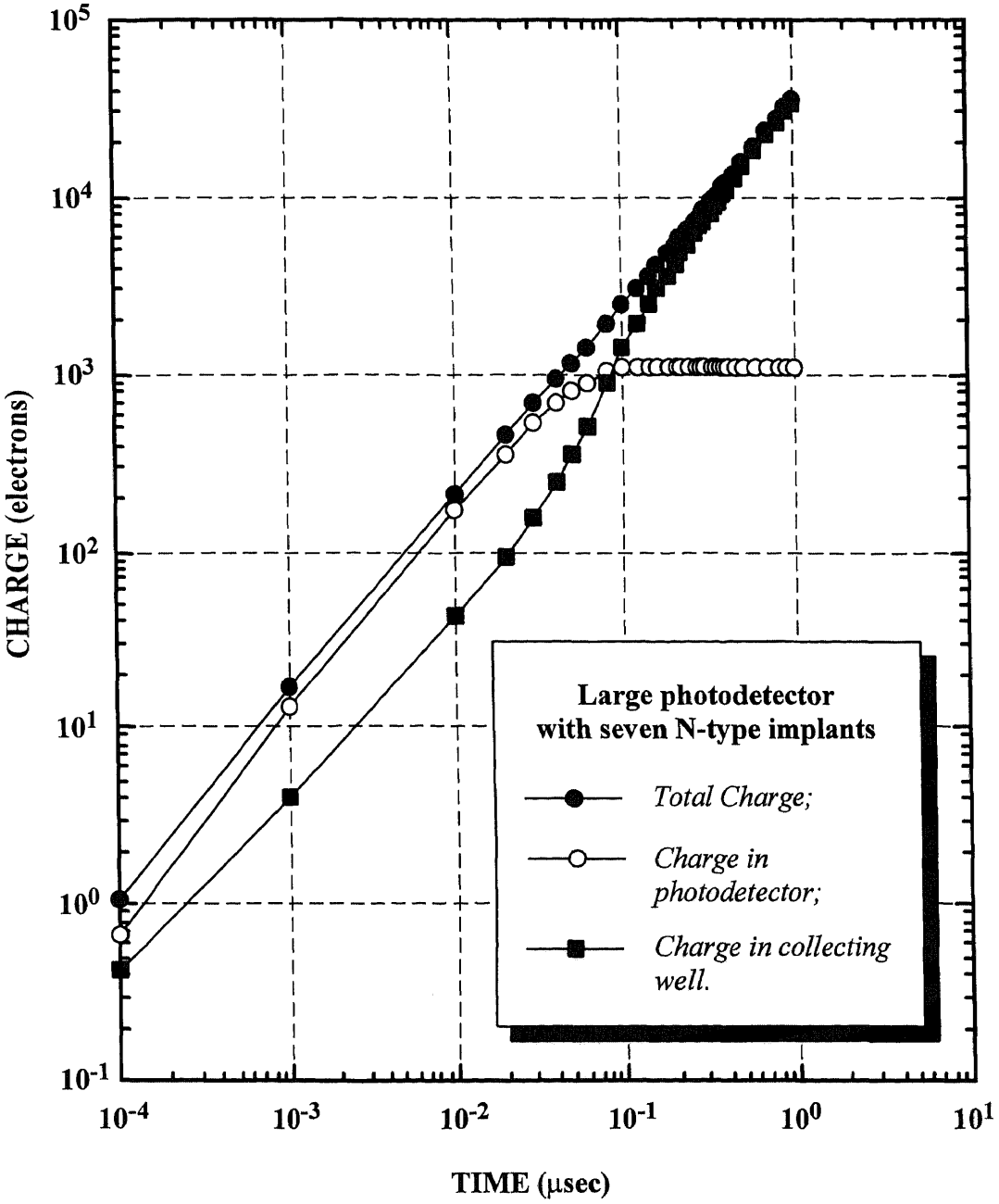
(Illumination intensity: 20,000 electrons in 1.0 μsec)

Figure C.19 *Time response of the large photodetector with six N-type implants to a step illumination corresponding to 20,000 electrons in 1.0 μsec.*



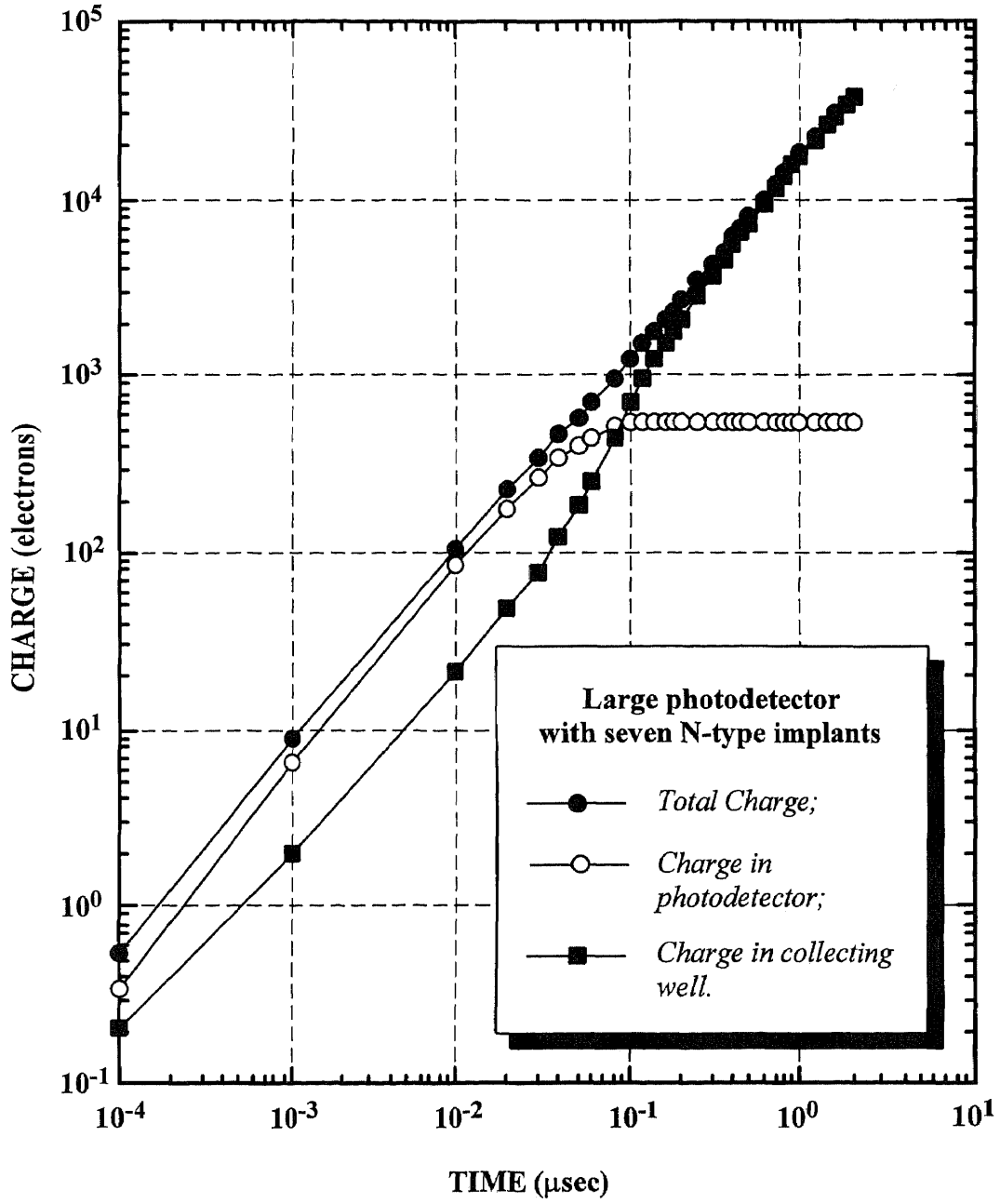
(Illumination intensity: 20,000 electrons in 2.0 μsec)

Figure C.20 *Time response of the large photodetector with six N-type implants to a step illumination corresponding to 20,000 electrons in 2.0 μsec.*



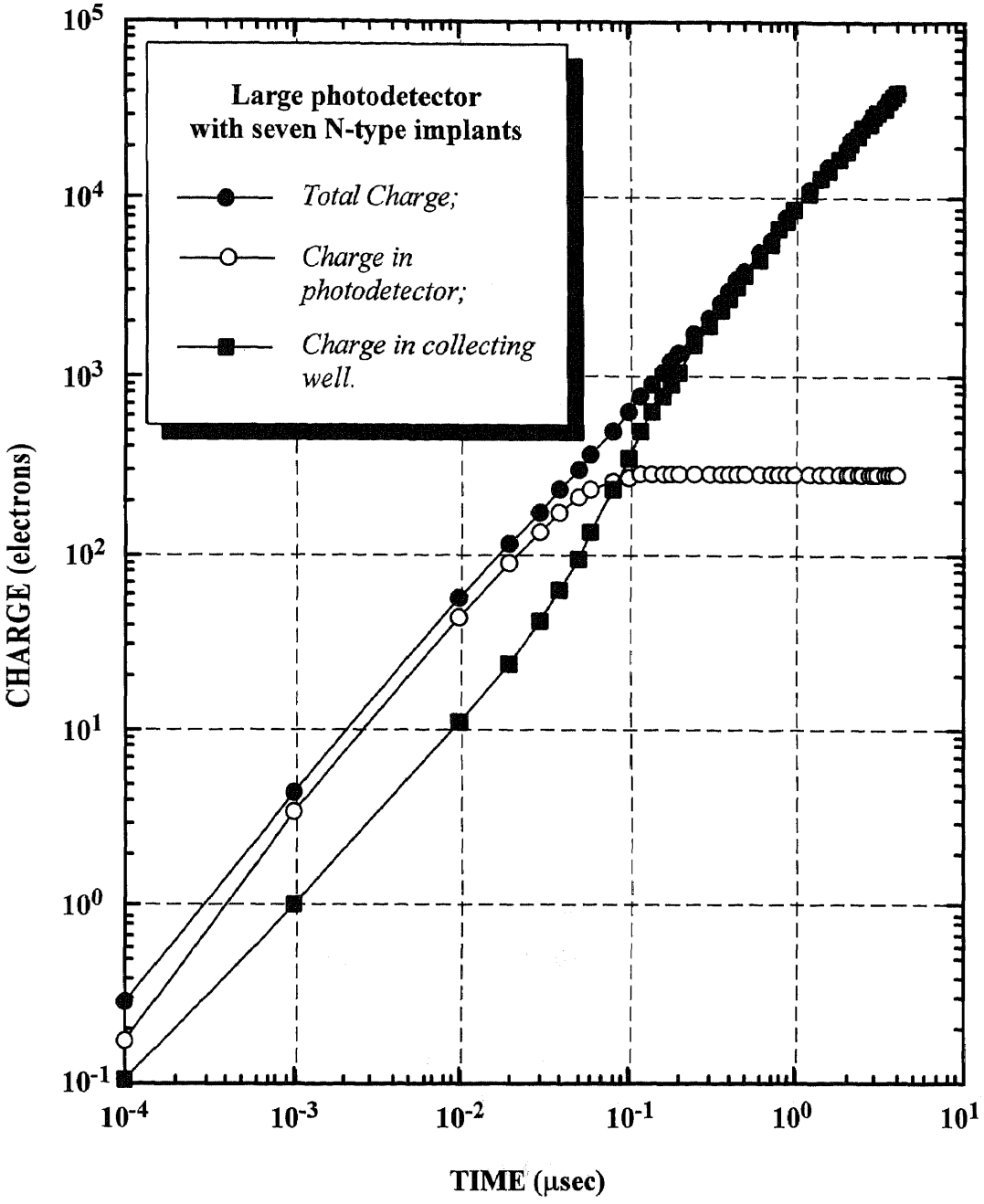
(Illumination intensity: 20,000 electrons in 0.5 μsec)

Figure C.21 *Time response of the large photodetector with seven N-type implants to a step illumination corresponding to 20,000 electrons in 0.5 μsec.*



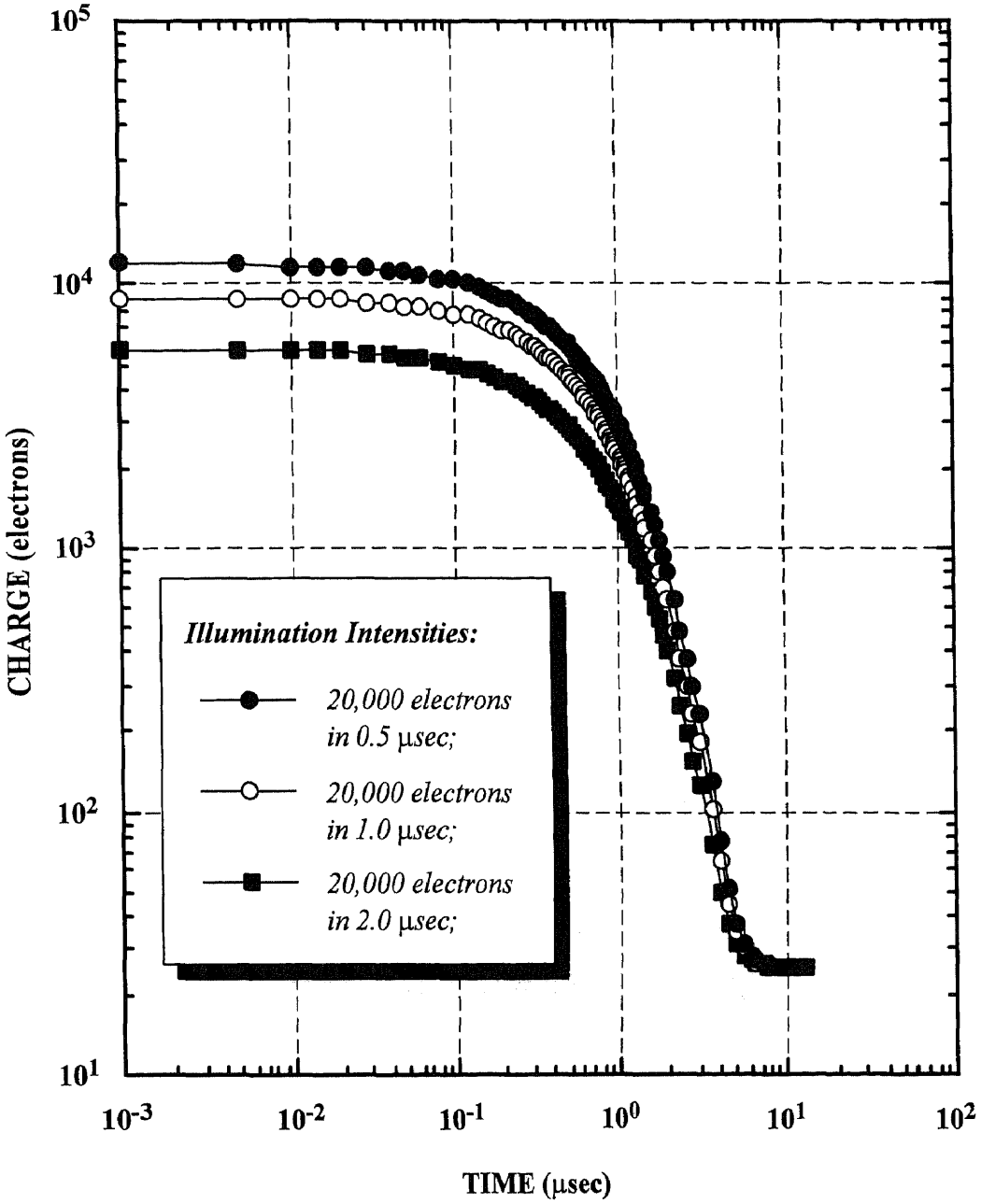
(Illumination intensity: 20,000 electrons in 1.0 μsec)

Figure C.22 *Time response of the large photodetector with seven N-type implants to a step illumination corresponding to 20,000 electrons in 1.0 μsec.*



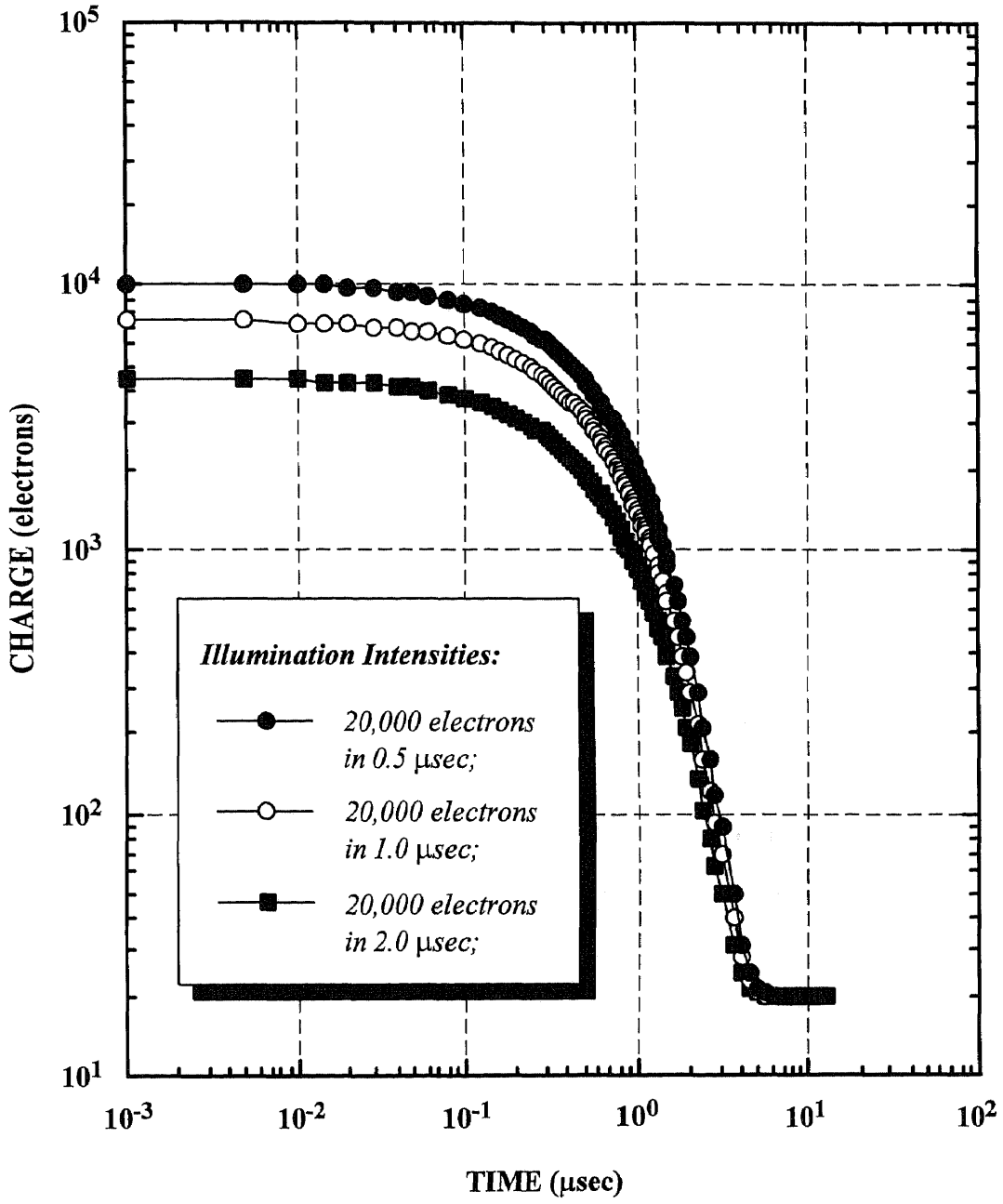
(Illumination intensity: 20,000 electrons in 2.0 μsec)

Figure C.23 *Time response of the large photodetector with seven N-type implants to a step illumination corresponding to 20,000 electrons in 2.0 μsec.*



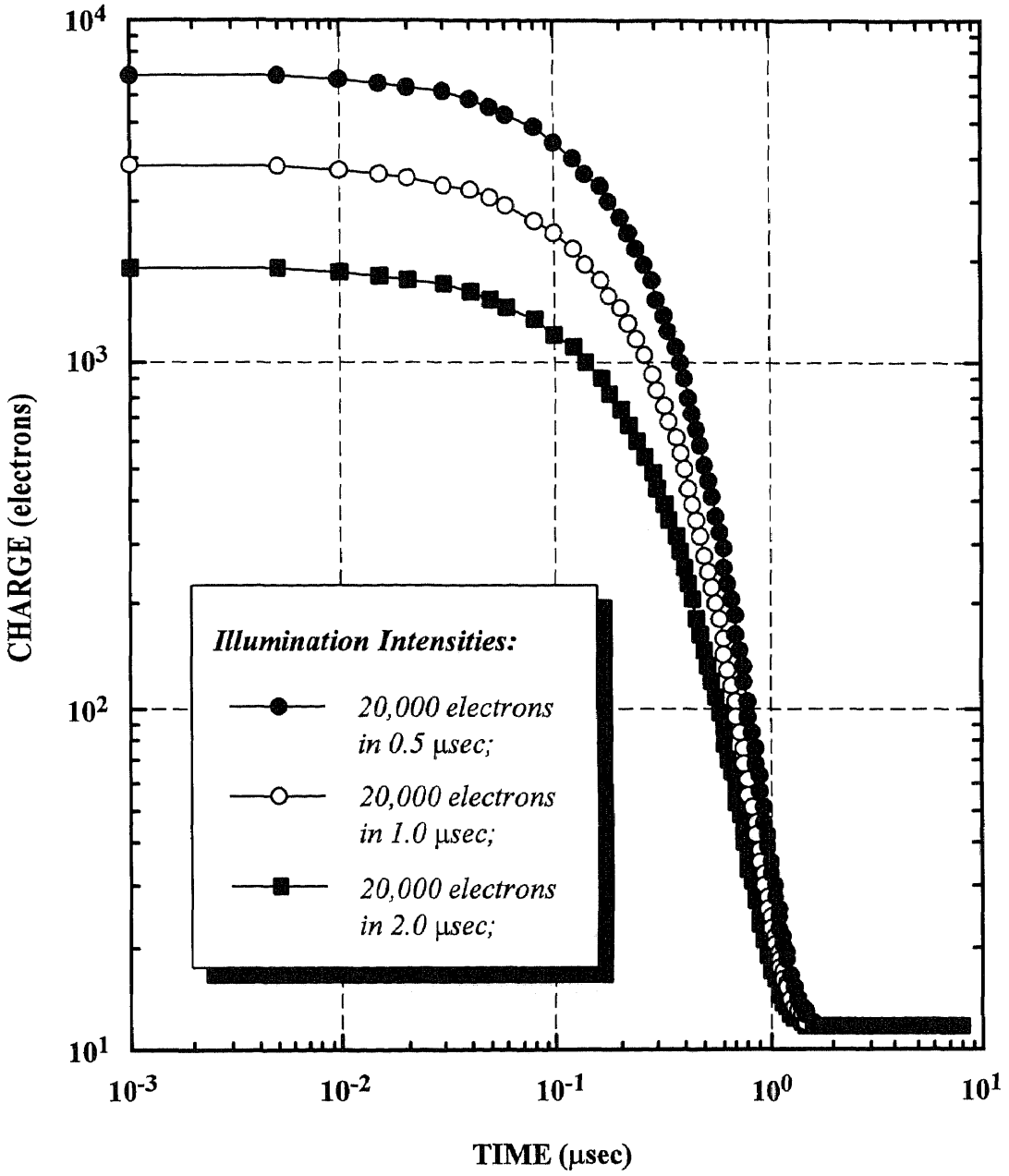
(Large photodetector with single N-type implant)

Figure C.24 *Decay of the channel charge in the large photodetector with single N-type implant for different illumination intensities after the illumination is cut off.*



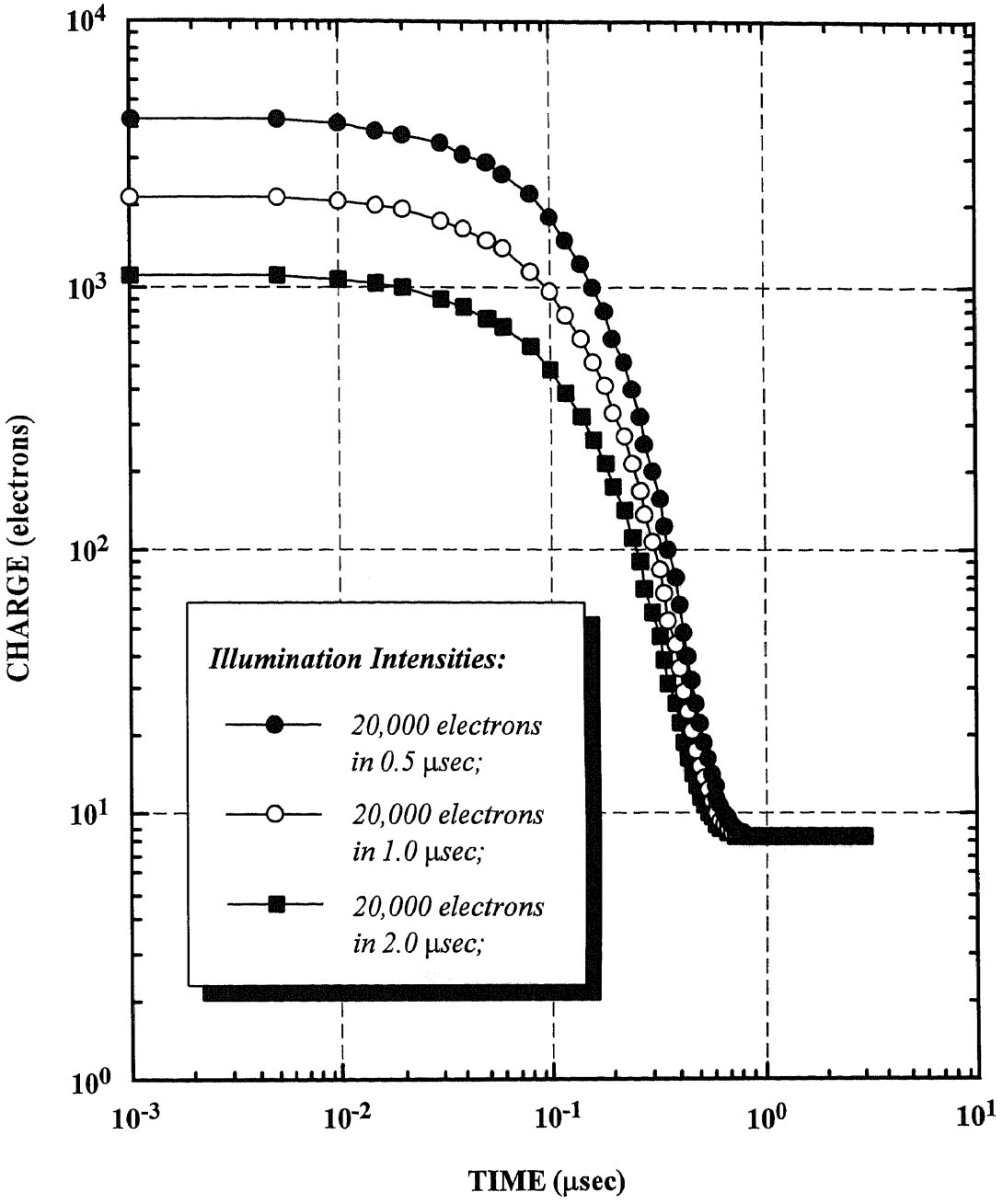
(Large photodetector with two N-type implants)

Figure C.25 *Decay of the channel charge in the large photodetector with two N-type implants for different illumination intensities after the illumination is cut off.*



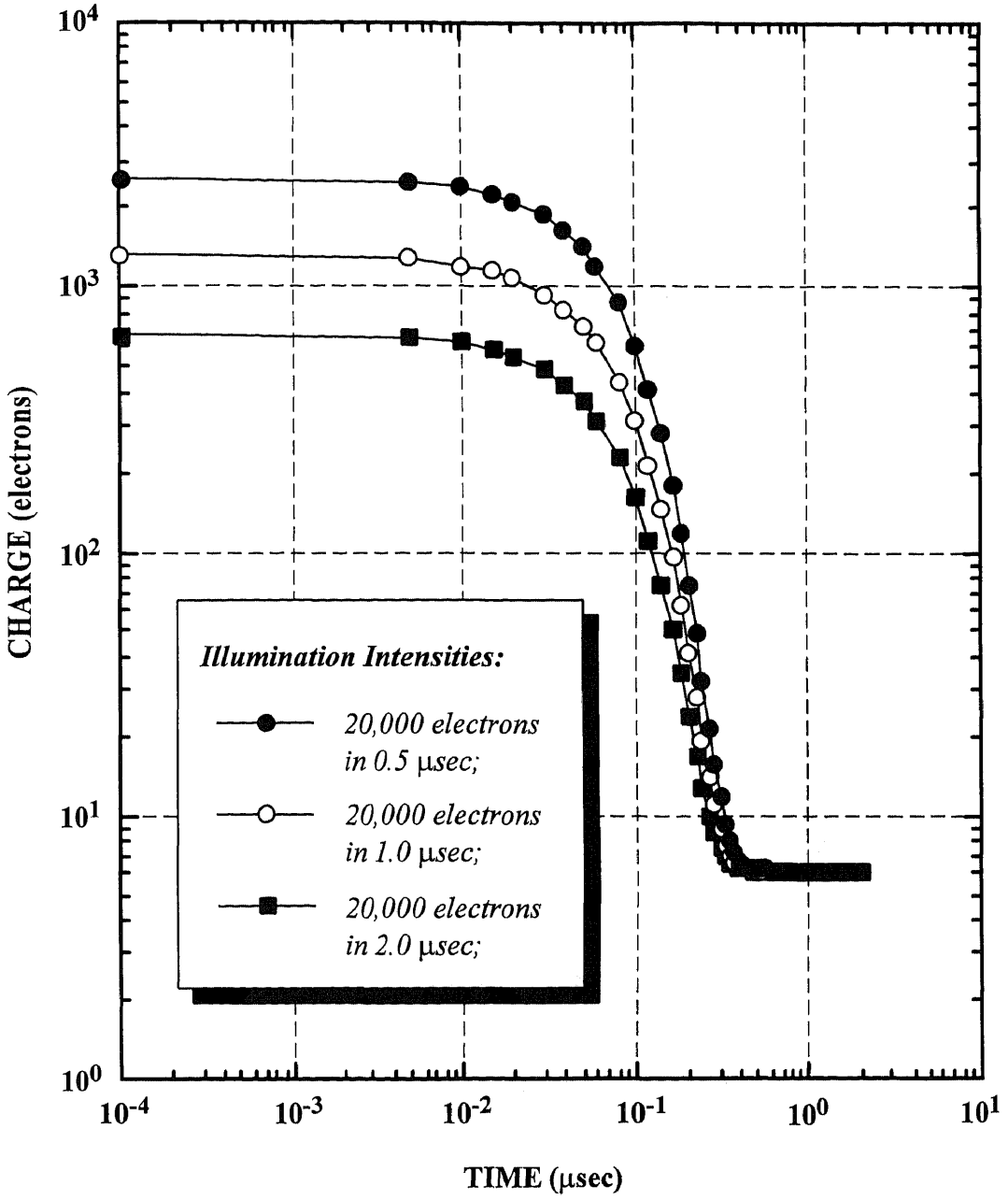
(Large photodetector with three N-type implants)

Figure C.26 *Decay of the channel charge in the large photodetector with three N-type implants for different illumination intensities after the illumination is cut off.*



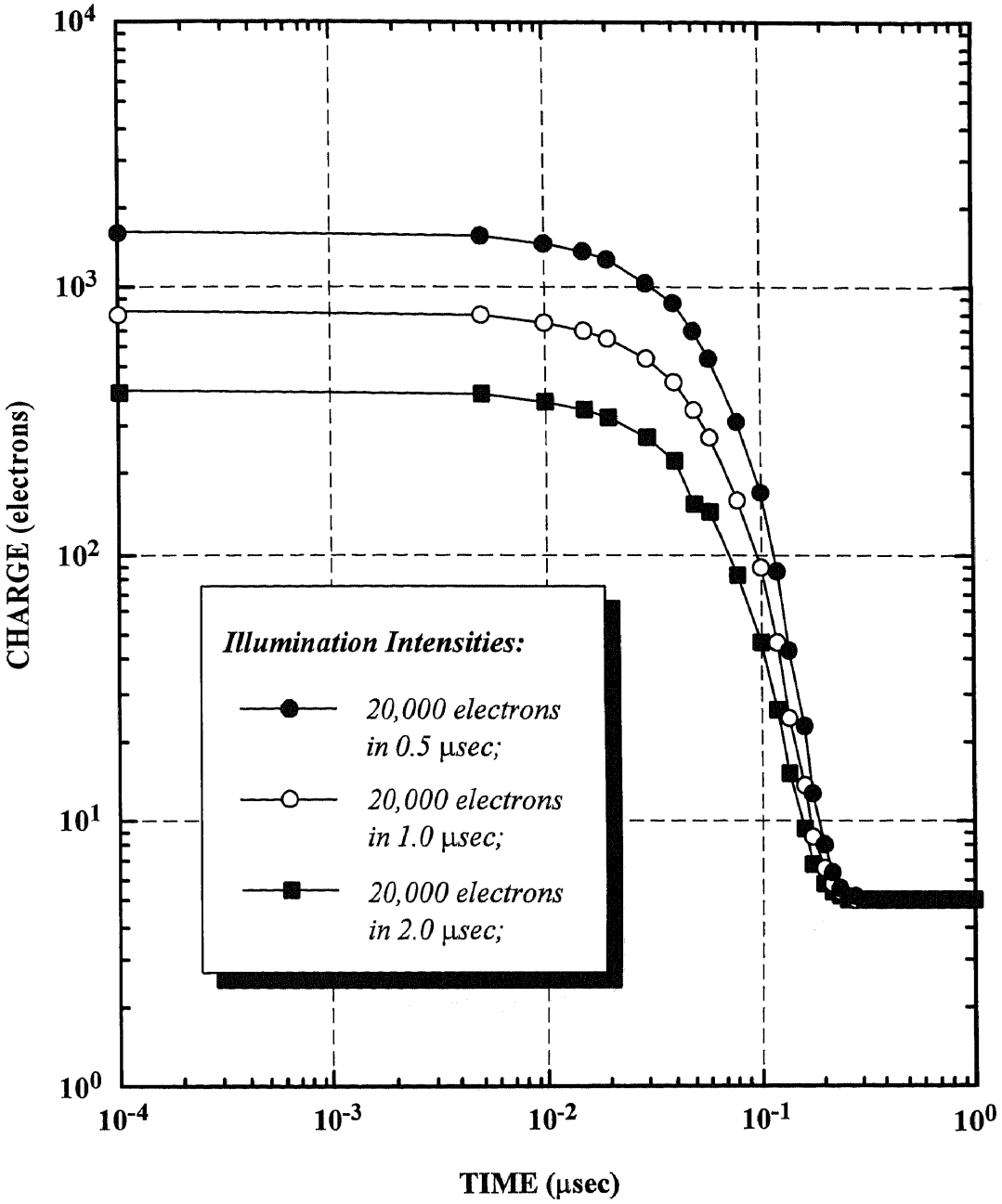
(Large photodetector with four N-type implants)

Figure C.27 *Decay of the channel charge in the large photodetector with four N-type implants for different illumination intensities after the illumination is cut off.*



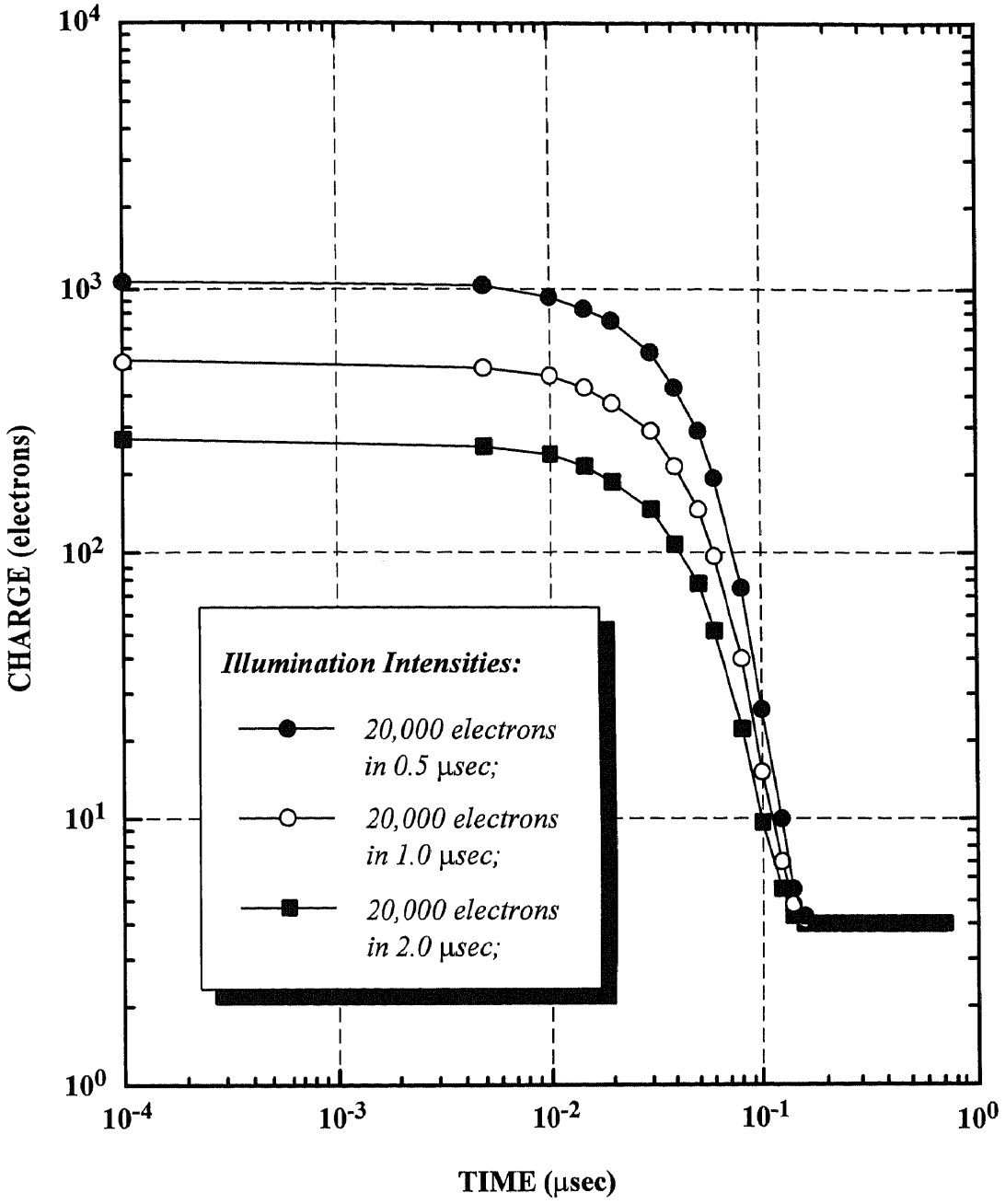
(Large photodetector with five N-type implants)

Figure C.28 *Decay of the channel charge in the large photodetector with five N-type implants for different illumination intensities after the illumination is cut off.*



(Large photodetector with six N-type implants)

Figure C.29 *Decay of the channel charge in the large photodetector with six N-type implants for different illumination intensities after the illumination is cut off.*



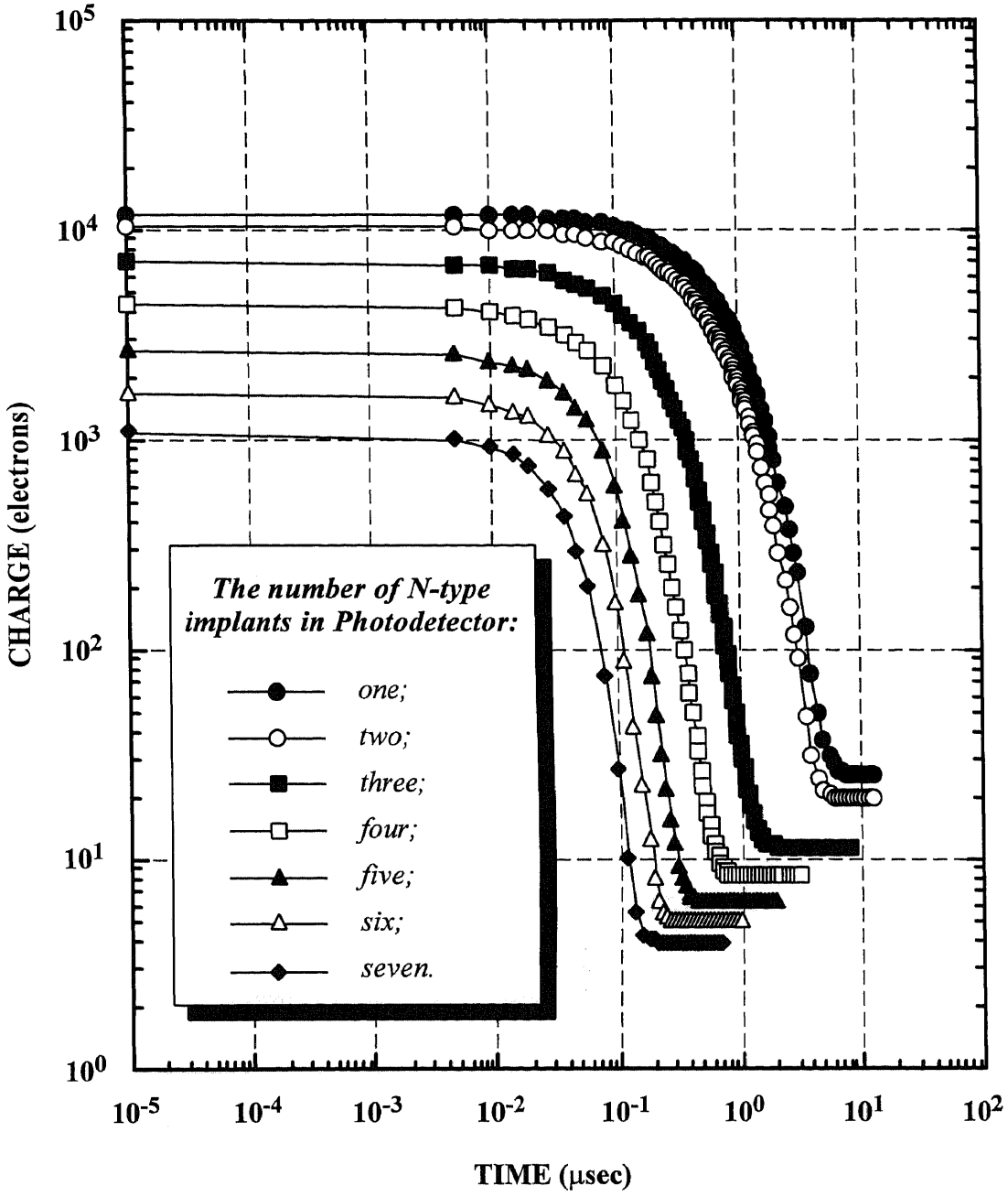
(Large photodetector with seven N-type implants)

Figure C.30 *Decay of the channel charge in the large photodetector with seven N-type implants for different illumination intensities after the illumination is cut off.*

illumination intensity corresponding to integration of 20,000 electrons in 0.5 μsec have not reached their steady-state saturation level. In these cases, the unsaturated photodetector channel charge levels corresponding to the optical illumination time are used as the starting photodetector channel charge for the simulation of the decay of the photodetector channel charge.

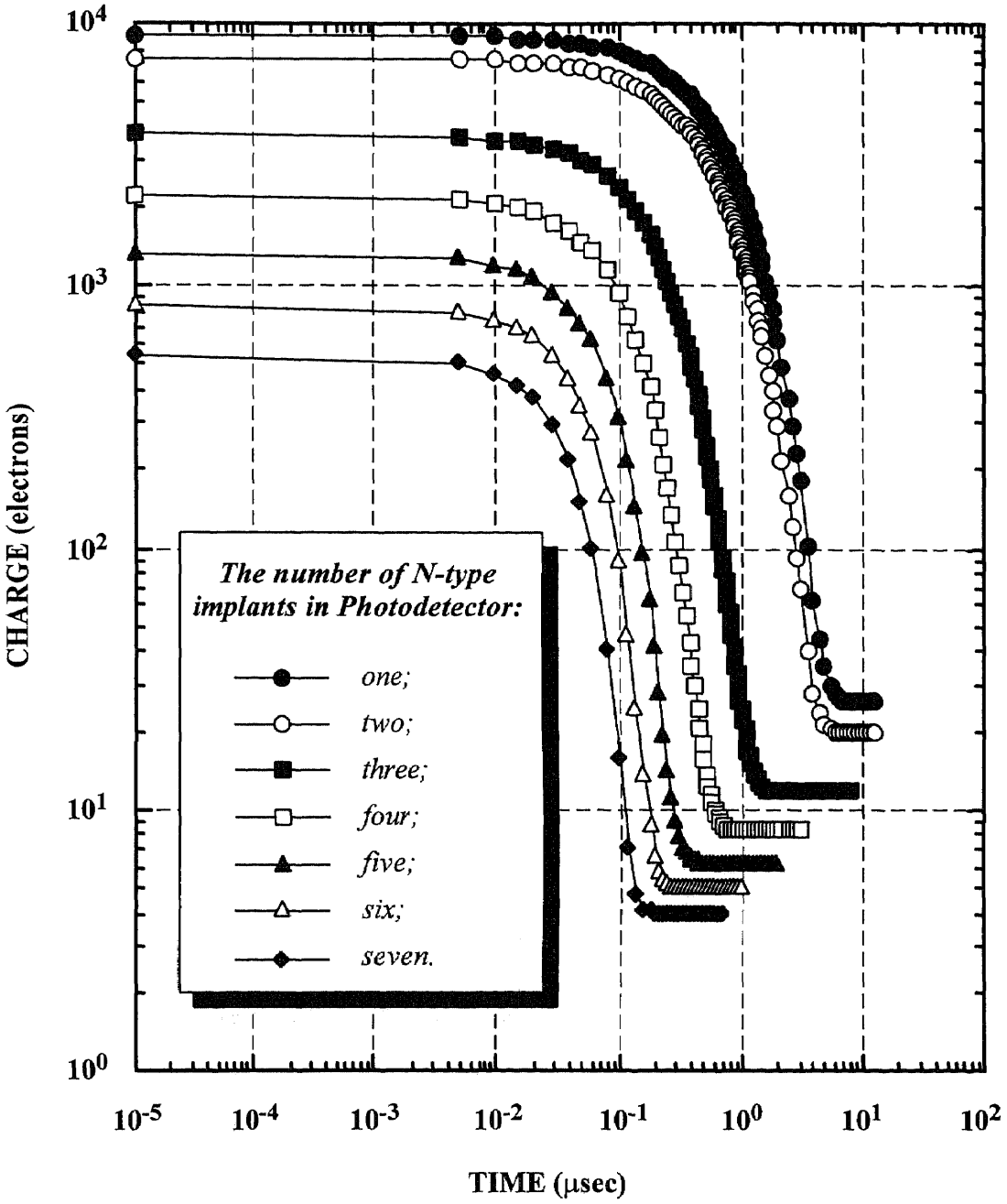
Inspection of Figures C.24, C.25, C.26, C.27, C.28, C.29, and C.30, shows that, after the optical illumination is stopped, although the photodetector channel charges are not the same for the different illumination intensities, the photodetectors with different numbers of N-type implants can transfer all the channel charges from photodetector to the BCCD collecting well in essentially the same decay time which is depended on the number of the N-type implants.

Figures C.31, C.32, and C.34 illustrate the comparison of the photodetector channel charge decay as function of time for the large photodetectors with one, two, three four, five, six, and seven N-type implants at the illumination intensities that results in integration of 20,000 electrons in 0.5 μsec, 1.0 msec, and 2.0 μsec, respectively. An inspection of Figures C.31, C.32, and C.33 indicates that when the large photodetector with seven N-type implants is capable of transferring 99% of its channel charge from photodetector to BCCD charge collecting well in about 0.12 μsec, the corresponding time for the large photodetector with one, two, three, four, five, and six N-type implants is about 0.18 μsec, 0.28 μsec, 0.46 μsec, 0.88 μsec, 3.0 μsec, and 3.8 μsec, respectively. It may be noted that, the residual charge in the photodetector region which represents the artifact of the computer and simulator also appears to be a function of the number of photodetector N-type implants.



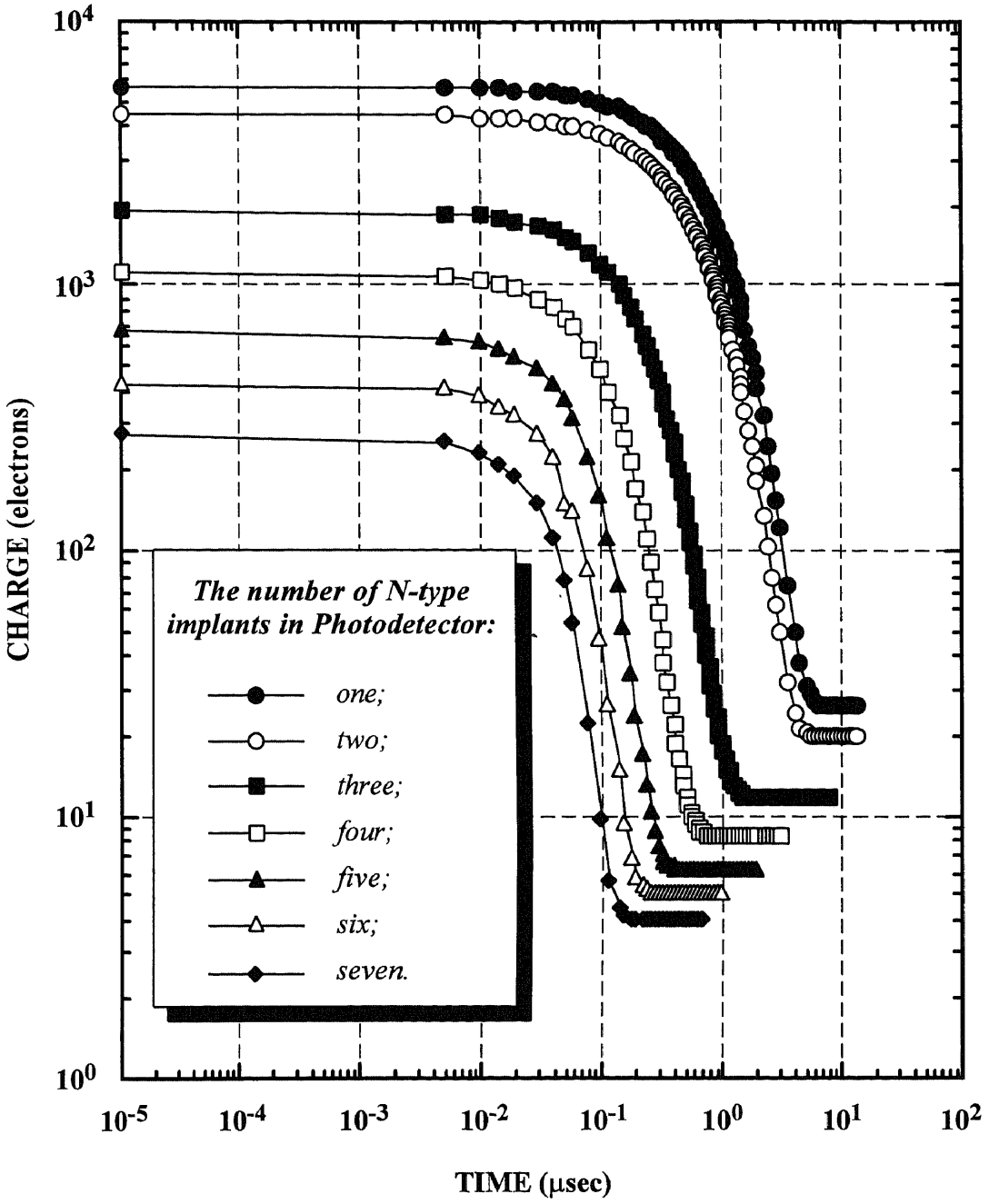
(Illumination intensity: 20,000 electrons in 0.5 μsec)

Figure C.31 *Comparison of the decay of the channel charge in the large photodetector with one to seven N-type implants after the illumination which is corresponding to 20,000 electrons in 0.5 μsec is cut off.*



(Illumination intensity: 20,000 electrons in 1.0 μsec)

Figure C.32 *Comparison of the decay of the channel charge in the large photodetector with one to seven N-type implants after the illumination which is corresponding to 20,000 electrons in 1.0 μsec is cut off.*



(Illumination intensity: 20,000 electrons in 2.0 μsec)

Figure C.33 *Comparison of the decay of the channel charge in the large photodetector with one to seven N-type implants after the illumination which is corresponding to 20,000 electrons in 2.0 μsec is cut off.*

C.3 Conclusions

The simulation study of the response time and decay time of large photodetector with up to seven N-type detector implants suggests that three or four N-type implants are sufficient for 78-μm long photodetector that can be used for the image sensor with frame acqucision rate up to 10^6 frames/sec.

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