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ABSTRACT

THE STUDY OF SiGe-CHANNEL HETEROJUNCTION MOS DEVICE

by
Yunchen Qiu

The advances in the growth of pseudomorphic silicon-germanium epitaxial layer combined with the strong need for high-speed CMOS VLSI circuit have led to increased interest in silicon-based heterojunction MOSFET's transistors. The high-performance heterostructure SiGe MOSFET exhibits higher channel mobility than its bulk Si counterpart. The most critical and challenging process for fabricating a SiGe MOSFET device is that for making a gate oxide with sufficient quality for useful conductivity modulation. PECVD methods was employed to deposit the gate oxide and C-V method was used to investigate the electrical characteristics of the film. For PECVD gate oxide, a film refractive index 1.47 were obtained using the deposition rate 125Å/min with a break-down voltage 4-5 MV/cm, which deposition conditions are optimized as flow rate of DES(12sccm), N2O(172sccm), Helium(850sccm), temperature 300°C, power density 0.09W/cm^2. The total interface trap and fixed charge density N_t = 5.4×10^{12} cm^{-2} and flatband voltage V_{fb} = -16V for non-annealing MOS capacitor and the total effect of interface trap and fixed charge density 6.4×10^{11} cm^{-2} and flatband voltage -4V were obtained at the oxide thickness d_{ox} = 1160Å using annealing at 650 °C for 30 minutes in the ambient of nitrogen. LPCVD silicon dioxide film was obtained at the deposition rate 14.5 Å/min and refractive index 1.46 while N_t = 3.9×10^{12} cm^{-2} and V_{fb} = -8V for non-annealing and N_t = 4.9×10^{11} cm^{-2} and V_{fb} = -2V for 650 °C annealed MOS capacitor.

THE STUDY OF SiGe-CHANNEL HETEROJUNCTION MOS DEVICE

by
Yunchen Qiu

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APPROVAL PAGE

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To my loving wife and newly expected baby

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CHAPTER 1

INTRODUCTION

1.1 Overview

Over the last ten years the significant progress in the application of SiGe layers is attributed to the rapid progress in techniques for the deposition of epitaxial layers of pseudomorphic SiGe epitaxial layers. This progress went through the following phases: material demonstrations, integration, feasibility, intrinsic profile optimization, structural integration and device parasites optimization[1]. Simple mesa structures were used to characterize the quality of the material set from 1983 - 1987[2][3]. This work led to the fabrication of the first SiGe devices in 1987[4]. The feasibility of integrated epitaxial Si and SiGe-base transistors was demonstrated from 1987 - 1989 and led to the generation of SiGe devices with ideal characteristics in 1989[5][6]. Then the sophisticated self-aligned devices[7][8][9] occurred in parallel through 1990 - 1992. The first significant commercial product of fully integrated SiGe bipolar transistors was made in 1994.

The SiGe material set also provides a path to heterojunction device physics and applications within the well established (CMOS dominated) silicon-based semiconductor industry.

The application of the film has became important in many electronics devices because of the ability of these techniques to tailor the band gap of the material. Due to the lattice mismatch between silicon and germanium, the films grown on silicon are strained up to a critical thickness. The narrow band gap of strained $Si_{1-X}Ge_X$ has been used to fabricate

heterojunction bipolar transistors (HBT's)[10][11], modulation-doped field effect transistors (MODFET's)[12][13], long wavelength optoelectronics devices, tunneling and superlattice devices[14], and field-effect transistors (such as MOSFET's). The SiGe HBT's have been demonstrated to have significant performance leverage over advanced bipolar transistors because they offer an enhanced mobility due to selective doping of that material component having the higher energy and edge[15]. In field-effect transistors (FET's), the strained SiGe offers enhanced carrier mobilities which largely improves the device transconductance. This improvement especially demonstrates in CMOS applications in which the interior performance of silicon P-MOSFET's is caused by the field-effect-hole mobility which is typically two to three times lower than the field-effect-electron mobility. Generally Si PMOSFET's are designed with wider gates to minimize asymmetric operation, which obviously affects improving packing density. Hence a high mobility SiGe-channel P-MOSFET's will improve both the circuit speed and the lever of integration.

1.2 Growth of Si/SiGe Structure

Making high mobility devices requires the high-quality SiGe films which have good crystalline property. A good quality SiGe films should have the following characteristics: (1) Can be n or p doped up to several orders of magnitude in doping concentration, (2) have a low contamination levels of oxygen, carbon and metals giving a long minority-carrier lifetimes, (3) contain low defect densities, (4) exhibit abrupt interfaces with neighboring layer, and (5) can be deposited selectively.

The most mature growth methods employed today are (1) molecular beam epitaxy (MBE)[16], (2) ultrahigh-vacuum/chemical vapor deposition UHV/CVD[17]. Both methods can be carried out at temperature of about 550°C and can get good quality SiGe layers.

The ability to control the band structure in semiconductors has much potential for the design of high-performance devices. The application of this concept is the heterojunction formed by using materials of differing bandgaps. The narrow-gap Si-Ge alloys shows special promise and is the subject of this thesis. Silicon and germanium are completely miscible over the entire compositional range and give rise to alloys with a diamond crystal structure. The lattice constant of the alloy at room temperature can be determined by Vegard's rule:

$$a_{Si_{(1-x)}Ge_x} = a_{Si} + x(a_{Ge} - a_{si}) \tag{1.1}$$

for low atomic concentration (x) of Ge. The lattice mismatch between Ge and Si is 4.17 percent at room temperature and increase only slightly with temperature. Figure 1.1 shows when such an alloy layer is deposited on a thick Si substrate, the mismatch can be in two different ways: 1) tetragonal distortion of the lattices, 2) generation of misfit dislocations at the interface. The distortion of the lattices results in cubic crystal and the films are under biaxial stress. The lattice constant in the plane of the substrate is determined by the substrate. Due to differences in lattices constant of Si, Ge and SiGe, the strain will be created at the surface. This strain is very fundamental property of the devices.

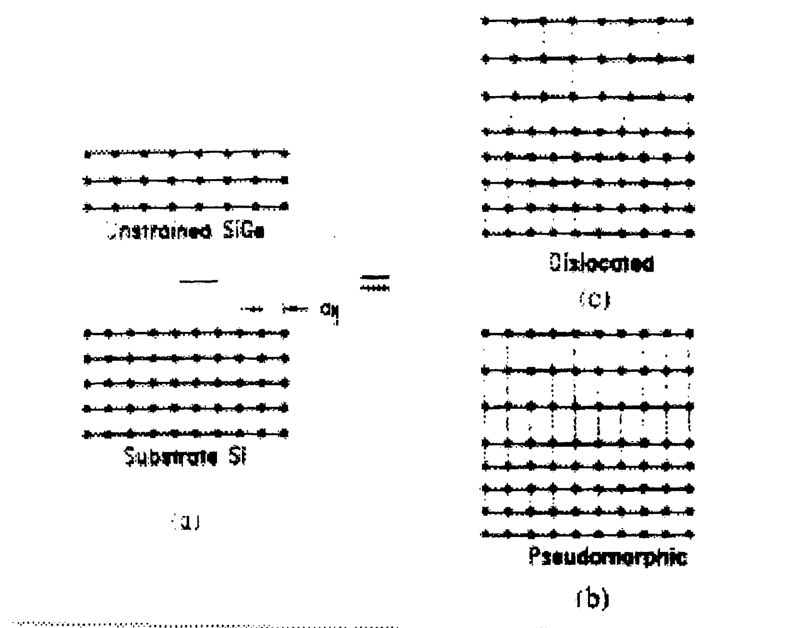


Figure 1.1 A two-dimensional representation of pseudomorphic growth. (a) An unstrained SiGe film is deposited on a silicon substrate. (b) Depending on growth parameter, the growth could be pseudomorphic, with the lattice constant difference accommodated by tetragonal strain or it could be dislocated.

Relaxed or unstrained growth occurs when misfit dislocation are permitted to nucleate. These dislocations may have pure edge components as shown in Figure 1(c) or they may thread through the layers.

It was investigated that the temperature ranges where the two- and three- dimensional growth modes persist using Rutherford Backscattering spectroscopy (RBS) and channeling and cross-sectional transmission microscopy. From this work it can be concluded that good quality layer by layer growth occurs only in the neighborhood of 550 °C for moderate Ge concentrations(up to 15%)[18].

The energy gap value as a function of Ge content is shown in Figure 1.2. The top solid curve shows the bandgap for a bulk alloy layer due to Braunstein et al[19]. The growth of

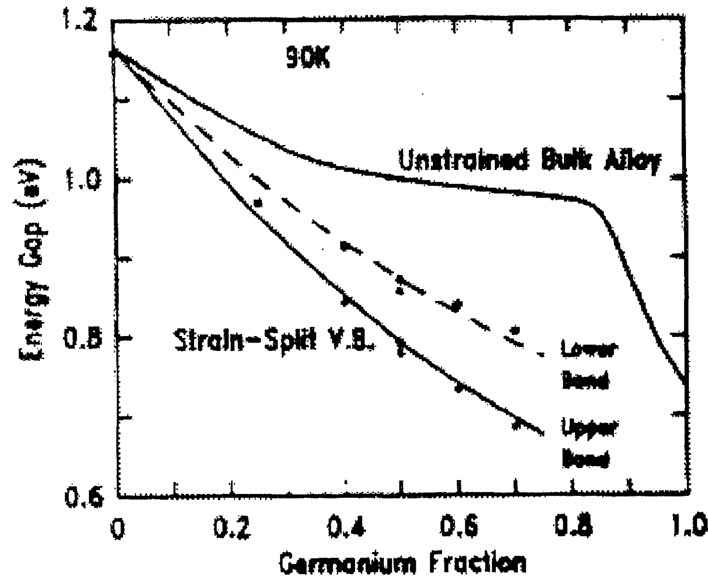
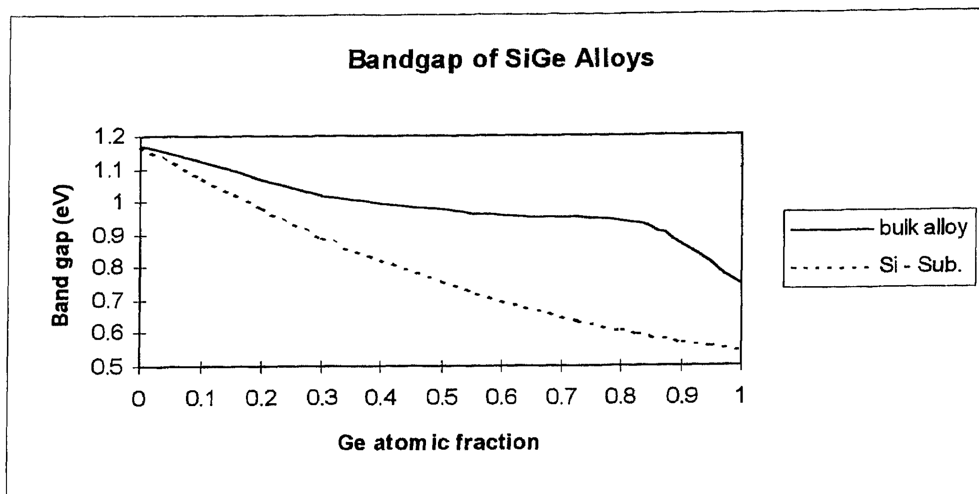


Figure 1.2 Bandgaps for unstrained bulk SiGe alloys and pseudomorphic SiGe alloys. Both the strain split light and heavy hole bands are shown along with the experimental optical absorption data.

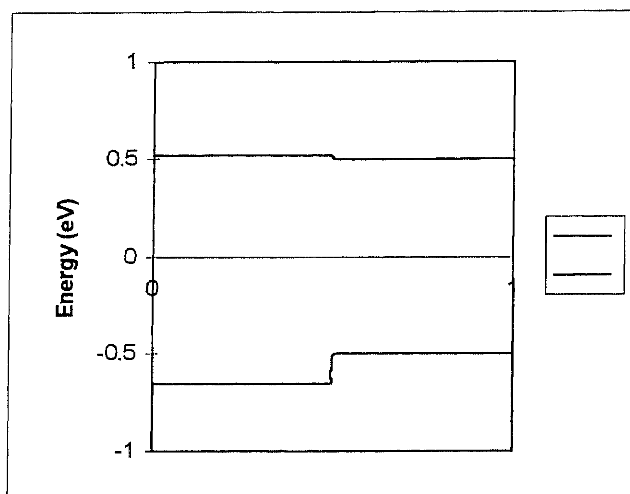
pseudomorphic Si_xGe_{1-x} on Si substrates causes an even greater shrinkage of the indirect gap as shown in the lower two curves of Figure 1.2. The bandgap shrinkage is significantly increased by the presence of tetragonal strain in the layers. Most of the bandgap difference manifests itself principally in the valence band. Figure 1.3 shows the band alignment for strained Si_xGe_{1-x} on Si. The gap energy of Si_xGe_{1-x} layers as a function of x is also summarized in Figure 1.3 for different substrates, which is based on theoretical calculations[4]. The effect of strain on the band structure of pseudomorphic structures provides for a wide range of control of the energy gap depending on the substrate chosen. Clearly, a greater degree of gap adjustment is possible for growth on substrate of different lattice constant. The band offsets are also sensitive to the relative strains in the constituents of the heterostructure.

The thickness of the Si_xGe_{1-x} layer is an important device design consideration. Critical thickness ("maximum thickness) for pseudomorphic growth of Si_xGe_{1-x} alloys is an important property of the system. The critical thickness h_c of an epilayer is a parameter introduced to explain the experimental observation that for an epilayer having a different lattice parameter than its substrate. There is an epilayer thickness below which coherency is preserved, and above which it is not. So if the misfit between substrate Si and growing epilayer Si_xGe_{1-x} is sufficiently small, the first atomic layers which are deposited will be strained such that the in-plane lattice constant of the film matches the substrate lattice parameter and hence a coherent interface will be formed. In this situation, defects could be avoided in growth of Si_xGe_{1-x} films on Si. The calculation of Mathews et al[21][22] determined the maximum (critical) thickness h_c of the strained epilayer as: 1) that thickness for which a grown in threading dislocation bows and elongates to form a segment of interfacial misfit dislocation line or 2) those conditions under which nucleation and subsequent growth of a dislocation half-loop would result in interfacial misfit dislocations. In particular, the above models give the following relation between critical thickness h_c and misfit between film and substrate f where b is the magnitude of the Burger's vector and ν is Poisson's ratio, f is the lattice mismatch. The critical thickness as defined either by theory or by experimental resolution does provides a frame of reference and this is summarized in Figure 1.4 for Si_xGe_{1-x} grown on Si (100) as a function of x.

$$h_c = \left(\frac{1}{f}\right)\left\{\frac{b}{4\pi(1+\nu)}\right\}\left[\ln\left(\frac{h_c}{b}\right)+1\right] \tag{1.2}$$



(a)



(b)

Figure 1.3 (a) Band gap of SiGe alloys (b) The band alignment on Si Substrate

One important property of covalent alloy semiconductors such as Si-Ge is that the onset of relaxation is graduate. This is different from that of pseudomorphic III-V layers in which relaxation is sudden and almost complete once the critical thickness is exceeded.

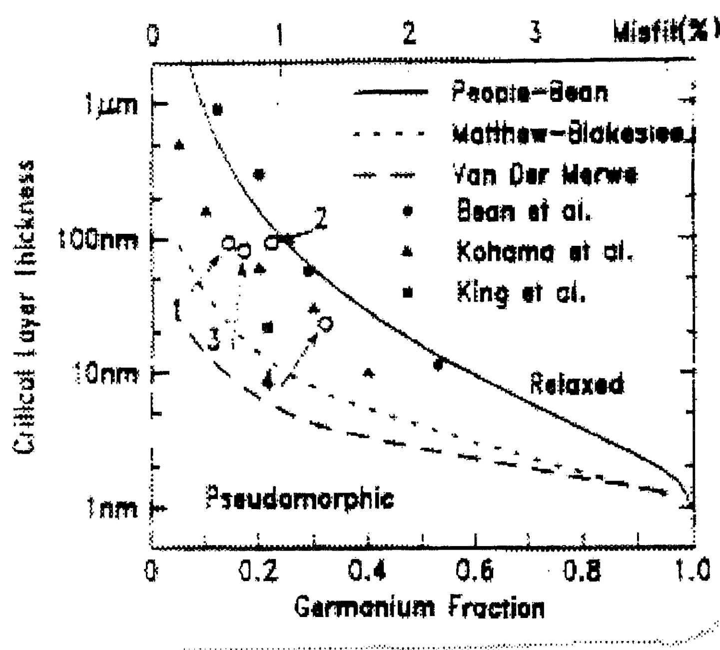


Figure 1.4 Critical thickness plotted as a function of Ge content.

1.3 Properties of SiGe Layers

1.3.1 Thermal Relaxation

A key challenge in fabrication of a SiGe HBT is maintenance of a nearly defect free SiGe strained layer on Si. Although Significant bandgap reduction is observed for unstrained SiGe on Si, the presence of an extensive misfit dislocation network in the material would preclude the fabrication of high quality devices. In order to process this material, several restriction are placed due to the metastable nature of pseudomorphic SiGe layers. During thermal annealing, the layers may relax. The mode of relaxation is either via intermixing or via additional misfit dislocation formation. The rapid increase in dislocation density above 850°C is caused by dislocation climb aided by Ge diffusion. It was proposed that

dislocation as a method of strain relaxation is operative only when a large number of them are initially present. Due to enhancement, the structure relaxes with a diffusion coefficient that is higher than normal when few dislocation is present[18]. Hull et al indicated that at low Ge concentration, annealing above 650°C causes significant strain relaxation, but that with large Ge concentration, the relaxation is far more gradual.

Furthermore, all the dislocations in device have electrical effect, this threading helps enhanced impurity diffusion to create a junction leakage. By limiting the processing temperature we can reduced this effect. The tendency of near perfect layers to relax via enhanced diffusion rather than dislocation formation is advantageous from the junction leakage point of view. In fact, relatively high-temperature annealing is also possible without junction degradation for high-quality heterojunctions[18].

1.3.2 Oxidation of SiGe Layers

The ability to oxidize exposed regions of silicon to create an insulator is obviously critical to all forms of Si integration and must be preserved when introducing the SiGe material system. The mechanisms of oxide growth on Si are complicated. Recent studies have found that small amounts of Ge could lead to dramatic enhancement in oxidation rates and Ge segregated to the growth interface during oxidation. Since local oxidation is generally used to provide electrical isolation, the Ge "pile-up" effect is likely to lead to high levels of leakage and potential reliability concerns under electrical stress. An general approach to control both of these effects is the use of an all-Si capping layer above the SiGe layer which serves as a sacrificial layer for oxide growth and isolation purposes.

1.3.3 Ion-Implantation of Si-Ge Layers

Strained $Si/Si_xGe_{1-x}/Si(100)$ heterostructure can offer great promise for making high-quality device. In such structures, it is imperative that strain-relieving misfit dislocations and/or threading dislocations be absent from the active device regions. The last thing one should consider doing to an ideal grown strained-layer is introducing significant amounts of lattice damage through implantation. Clearly, implantation damage could provide an ideal source of defect nucleation sites which in turn could lead to deleterious formation of an extensive misfit dislocation network upon annealing. Harame, et al [1] investigated two processes which are likely to cause problems: 1) moderate energy, low dose implants Phosphorous 100 kev, $1x10^{13}$ cm^{-2}; 2) high dose, low energy implants Boron 5 kev, $1x10^{15}$ cm^{-2}. The results show that the use of both types of implant have been found no significant yield impact for SiGe layers which are clearly within the Matthews and Blakeslee stability criterion. SiGe layer which are mechanically stable are able to undergo implantation and anneal cycles with no additional defect generation or motion beyond that.

1.3.4 Etching Effects of SiGe Layers

So far little is known about the dry etching behavior of SiGe alloy and how it differs from that of silicon. Dry etching techniques such as reactive ion etching (RIE), plasma etching (PE) and ion beam etching (IBE) can cause damage in materials. If these damages and contamination effect is not controlled, it can influence material properties and device performance[23]. Dry etching effects can change the surface properties, generation lifetimes, doping activation and diffusion lengths in etched silicon.

The simplest picture of the etching of SiGe is independent removal of Si and Ge atoms by the etchant atoms from the SiGe surface at rates of the species which is more slowly volatilized. The presence of several percent Ge in a SiGe alloy significantly increase the rate of Si atom volatilization of the alloy[24].

The major damages which are considered in dry etching are residues layer formation; impurity contamination, hydrogen permeation and bonding damage. The residue layer is present depends on the etching chemistry. For example, during the CF_4 + O_2 plasma etching, the residue formation maybe neglected. Some groups have detected impurities, particularly metallic impurities such as Fe, Ni, Al, Cr, K, and Zn, on the surface and near-surface region. The bonding damage that results from dry etching exposure has its roots in three distinctly different causes. One is the ion bombardment inherent in at least all current anisotropic dry etching, another is UV radiation, and the third is hydrogen. The effects of dry etching ion bombardment damage are easily seen by C-V characteristics of metal/semiconductor contact made on etching surface.

1.4 Application of SiGe Film

The application of silicon/SiGe heterostructures in device has focused on the bipolar and field-effect transistors. In bipolar transistors, the presence of germanium exponentially alters the device characteristics. The SiGe HBT's have been demonstrated to have significant performance leverage over advanced bipolar transistors[25] because they offer an enhanced mobility due to selective doping of that material component having the higher energy band edge [26]. The SiGe HBT offers three key advantages over conventional ion-

implanted bipolar transistor: 1) a reduction in base transit time resulting in higher frequency performance, 2) an increase in collector current density and hence current gain allowing high current gain with low intrinsic base resistance, and 3) an increase in Early voltage at a given cutoff frequency. The first commercial SiGe integrated circuit is the achievement of the application of SiGe technology to the fabrication of a high performance 12-bit DAC.

In the application of Metal-Oxide-Semiconductor field-effect transistor (MOSFET'S), the advantage of using SiGe MOSFET is that it can maximize the device transconductance because the strained SiGe offers enhanced carrier mobilities.

Since the bandgap difference between strained SiGe and unstrained Si appears mostly in valence band, there is large improvement in P-channel MOSFET's hole mobility. This result brings great advantage in CMOS applications because the field-effect hole mobility is typically two to three times lower than the field-effect electron mobility. Usually Si P-MOSFET's are designed with wider gates to minimize asymmetric operation, which affects packing density. Hence a high mobility p-channel FET will improve both the circuit speed and the level of integration.

1.5 Objectives of Thesis

The objective of this thesis was to develop a processing technique for fabricating SiGe-channel MOSFETs and to use these data as a guide for improving the processing approach. A further objective was to fabricate a SiGe-channel MOSFET and Si-channel MOSFET for comparing the electrical characteristics of the SiGe-channel MOSFET and

Si-channel MOSFET, which provides a new heterostructure MOSFET for improving the performance of CMOS VLSI circuit . For fabricating a SiGe-channel MOSFET, a low temperature processing (<650°C), which is a silicon-based heterostructure processing, was investigated because the SiGe layer tends to relax at high temperature(above 650°C). The most important step in this process comparing with the regular Si MOSFET process is how to obtain a good quality gate oxide. Thermal oxidation which is used in Si process (temperature 950°C) is not appropriate to SiGe films. The application of two methods for obtaining insulating gate oxide was investigated: 1) Plasma Enhanced Chemical Vapor Deposition (PECVD) method and 2) Low Pressure Chemical Vapor Deposition (LPCVD) method. The C - V analysis method was employed to study and compare the electrical characteristics of the films deposited by these two methods.

To study the SiGe device, SiGe-channel and Si-channel MOSFETs with different geometry were fabricated with the low-temperature process in NJIT cleanroom.

CHAPTER 2

EXPERIMENTAL I

2.1 Capacitor - Voltage Characteristics Technique

The capacitor-voltage characteristics of MOS capacitors have been found to be extremely useful in the evaluation of electrical properties of insulator-semiconductor interfaces. Uoinigescn shows that the Si/SiGe heterostructure MOS capacitor can become an excellent and thorough characterization vehicle for Si-based heterostructure technology.

There are two basic types of charge in the SiO_2 layer: (1) Interface trap charge; (2) Oxide charge. The feature that distinguishes interface trap charge from oxide charge is that interface trap charge varies with gate bias whereas oxide charge is independent of gate bias. There are three type of oxide charge Q_o, that are technologically important. (1) Oxide fixed charge Q_f, which is located at or very near the Si-SiO_2 interface. (2) Oxide trapped charge Q_{ot}, which is located either at the metal-SiO_2 interface or at the Si-SiO_2 interface. In some cases, Q_{ot} can be distributed within the oxide layer. (3) Mobile ionic charge Q_m, most commonly is caused by the presence of ionized alkali metal atoms such as sodium or potassium. This type of charge is located either at the metal-SiO_2 interface or at the Si-SiO_2 interface, where it has drifted under an applied field. Drift can occur because such ions are mobile in SiO_2 at relatively low temperatures.

Immobile oxide charge can be distinguished from mobile charge by a bias-temperature aging experiment.

2.1.1 Measurement of Oxide Charge

Oxide charge is an important parameter in devices. For example, it can alter the threshold voltage of a MOSFET; alter the silicon surface potential and thereby change reverse surface leakage current in a p-n junction; alter the avalanche breakdown voltage of a p-n junction. The simplest and most widely used method for measuring oxide charge density is to infer this density from the voltage shift of a C-V curve.

The presence of an oxide charge , interface states charge and work function differences are taken into account the flat-band voltage, the amount of gate to substrate voltage which is required to produce zero band-bending at the silicon surface is given by:

$$V_{fb} = \Phi_{ms} - Q_o/C_{ox} \tag{2.7}$$

This equation shows that the entire C-V curve is shifted along the voltage axis with respect to the ideal C-V curve by the amount V_{fb} - Φ_{ms}. Figure 2.1 illustrate the shift along the voltage axis of a high frequency C-V curve when positive or negative Q_o is present in the oxide.

2.1.2 Measurement of Mobile and Oxide Fixed Charge

Consider an experiment where the only oxide charge is oxide fixed charge. The initial high frequency C-V curve measurement is labeled (i) in Figure 2.2(a). After heating at 150°C for half an hour with a positive gate bias producing a field of a few million volts per centimeter across the oxide, and cooling back to room temperature, The curve labeled (f_+)

in figure 2.2(a) is obtained. Repeating the bias-temperature aging with negative gate bias yields curve (£) in figure 2.2(a). So the oxide fixed charge centers are immobile and is given by:

$$V_{fb} = Q_o/C_{ox} \tag{2.8}$$

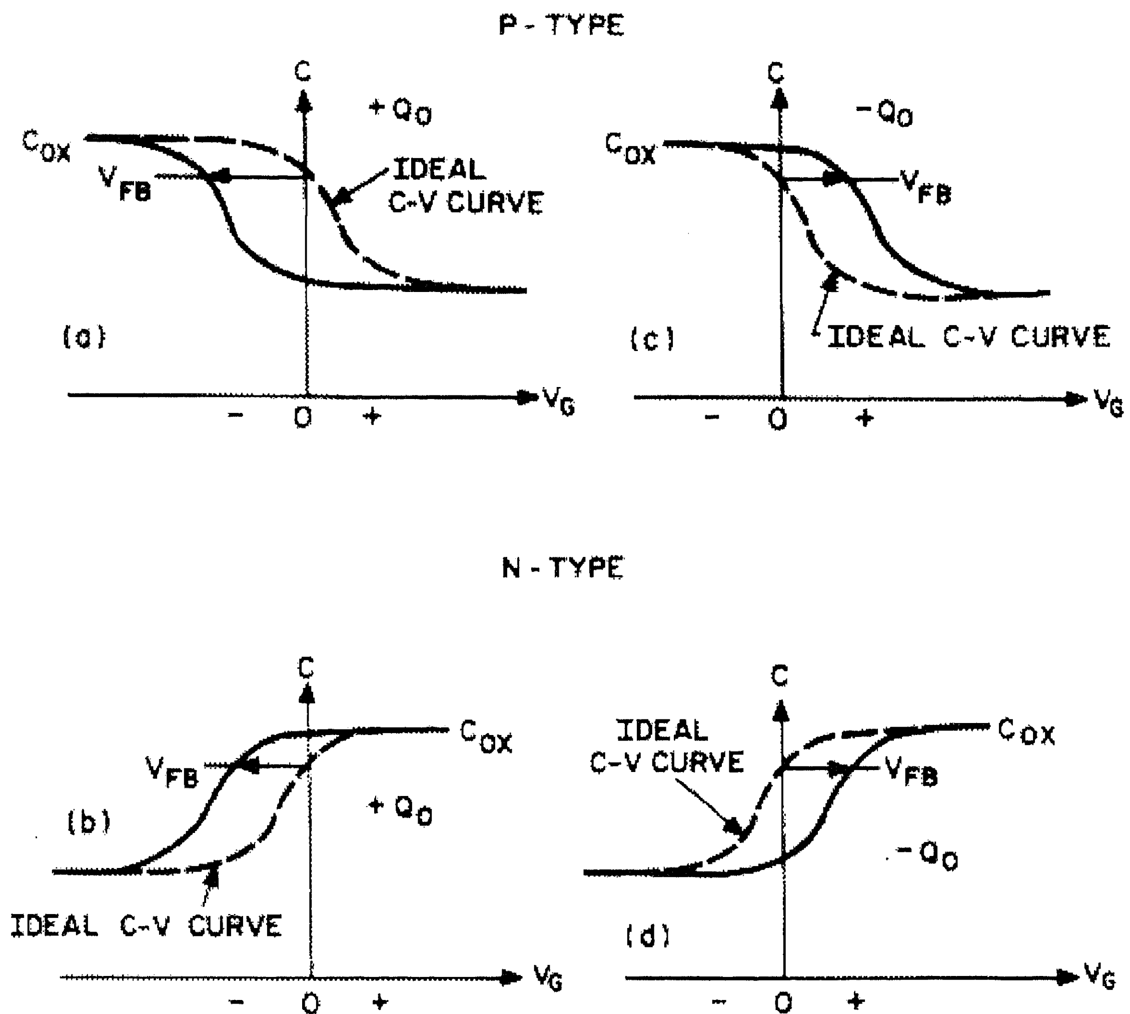


Figure 2.1 High frequency capacitance as a function of gate bias showing the effect of oxide charge. The C - V curves marked "ideal" have no oxide charge. (a) Positive oxide charge, p-type; (b) positive oxide charge, n-type; (c) negative oxide charge, p-type; (d) negative oxide charge, n-type.

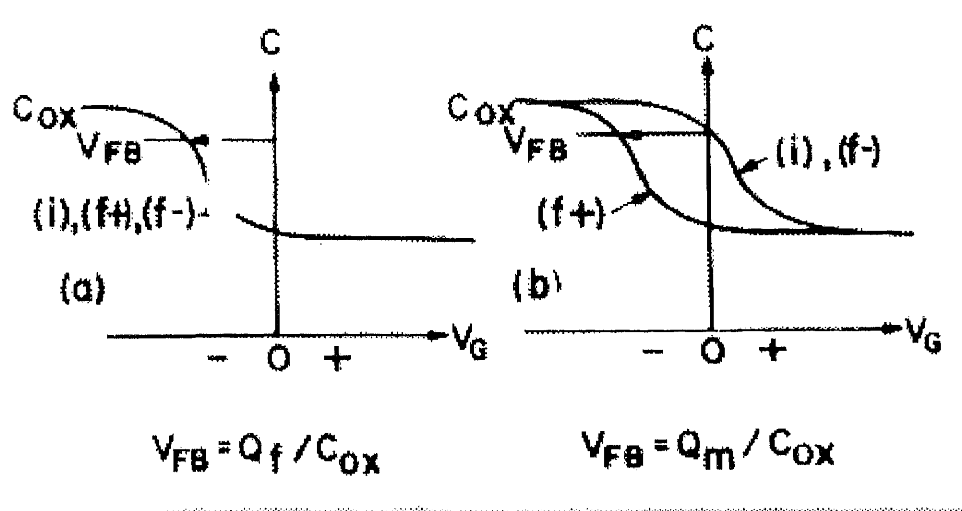


Figure 2.2 Diagram illustrating how oxide fixed charge, oxide trapped charge, and mobile ionic charge can be distinguished from a bias-temperature aging experiment. The Symbols (i) denotes the initial C - V curve; (f_+), after positive bias-temperature aging, and (f_-), after negative bias-temperature aging. (a) Oxide fixed charge; (b) mobile ionic charge.

Figure 2.2(b) shows the results of repeating this experiment on an oxide contaminated by mobile ions. Initially V_{fb} is low, and after positive bias aging it increases. With negative bias aging, V_{fb} return to its original value. The shift of flat-band voltage is resulted from the movement of mobile charges, which is given by

$$\Delta V_{fb} = Q_m/C_{ox} \tag{2.9}$$

2.1.3 Measurement of Interface Trap

The combined high-low frequency capacitance method is used to measure the interface traps. For lower frequencies, interface traps respond to ac gate voltage changes. Therefore

the low frequency equivalent circuit of the MOS capacitor contains an interface trap capacitance, which is not present if there are no interface traps. Figure 2.3 illustrates the equivalent circuit corresponding to equation (4):

$$C_{LF} = \frac{dQ_T}{dV_G} = (C_s + C_{it})\frac{C_{ox}}{C_{ox} + C_s + C_{it}} \quad (2.10)$$

C_{LF} is the capacitance at the low frequency.

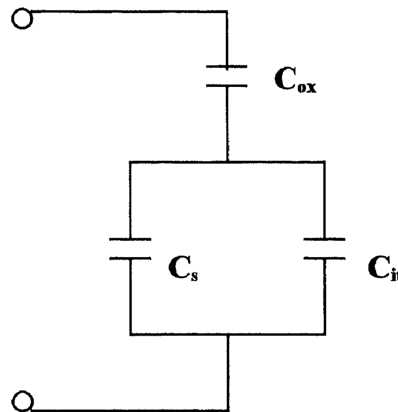


Figure 2.3 Low frequency equivalent circuit of the MOS capacitor.

For high frequency, the interface traps do not follow the ac gate voltage in a high frequency C-V measurement. They contribute no capacitance to the high frequency C-V curve. At high frequency the total capacitance is given by equation (5) with $C_{it}(\omega) = 0$ (because ω is too large for any ac response of interface traps). The capacitance at high frequency C_{HF} is given by

$$C_{HF} = \frac{C_s C_{ox}}{C_s + C_{ox}} \tag{2.11}$$

This capacitance corresponds to the equivalent circuit shown in figure 2.4.

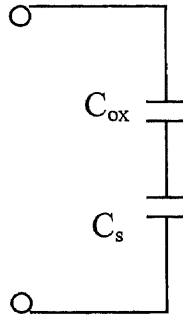


Figure 2.4 High frequency equivalent circuit of the MOS capacitor.

The circuit does not contain interface traps explicitly. Therefore, regardless of interface trap level density, the high frequency capacitance of an MOS capacitor will be the same as that of an ideal one without interface traps provided that C_s is the same.

Castangne and Vapaille were the first to combine high and low frequency C-V curves to obtain a measured C_s. The step eliminates the need for a theoretical computation of C_s and for measurement of the doping profile of the device. From equation (4) and (5), C_{it} is give by:

$$C_{it} = \left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}}\right)^{-1} \tag{2.12}$$

In this way C_{it} is obtained directly from the measured C-V curves without the uncertainty introduced by a theoretical C_s and without uncertainty as to whether C_s has been calculated for the correct band bending. If we let

$$\Delta C = C_{LF} - C_{HF} \tag{2.13}$$

Then

$$D_{it} = \frac{C_{it}}{q} = \frac{C_{ox}}{q}\left[\left(\frac{1}{\Delta C / C_{ox} + C_{HF} / C_{ox}} - 1\right)^{-1} - \left(\frac{1}{C_{HF} / C_{ox}} - 1\right)^{-1}\right]$$

$$= \frac{\Delta C}{q}\left(1 - \frac{C_{HF} + \Delta C}{C_{ox}}\right)^{-1}\left(1 - \frac{C_{HF}}{C_{ox}}\right)^{-1} \tag{2.14}$$

Hence, the interface density D_{it} can be calculated from equation (8).

2.1.4 C-V Measurement System

The C-V measurement system is designed to measure the low-frequency C-V, high-frequency C-V and bias-temperature C-V characteristics. This system uses personal computer to control HP4140B which is for quasi static parameter measurement and HP4145B which is used for measurement of high frequency C-V measurement. The components for the system are as follows:

1. Supercom 386 IBM/compatible PC
2. AT-G.P.I.B. interface card and software NI-488.2
3. HP4140B PA Meter / DC Voltage Source

4. HP4145B Semiconductor Parameter Analyzer
5. Boonton Capacitance Meter Model 72BD
6. Micromanipulator Hot Stage and Controller Model HSM
7. Micromanipulator Probe Station
8. Hewlett-Packard Colorpro Plotter
9. Software used: Microsoft Quick Basic Version 4.5 and National Instruments NI-DAQ DOS software version 4.4.

The diagram of Quasi static measurement system is shown in Figure 2.5, which system is designed to make C-V measurement. HP4140B is controlled by 4140 software from 386PC. It can supply desired voltage to DUT on the probe and measure the current or capacitance of the samples. 4140 is an interactive software and the measurement results are shown on the screen. The data are directly stored in a file.

The high frequency C-V measurement system is shown in figure 2.6. HP4145B which is controlled by PC386 software 4145 provides the needed voltage to DUT on the probe. The measurement range can be set through the interactive software. At the same time the HP4145B measures the voltages and currents of the samples and the datas are stored in a file.

2.2 NJIT Cleanroom

Most of our process work was done in NJIT clean-room. NJIT clean-room is a 1200-sq-ft and class 10 fabrication line. It was equipped with all necessary tools for processing wafers up to 150mm in diameter. These equipment include:

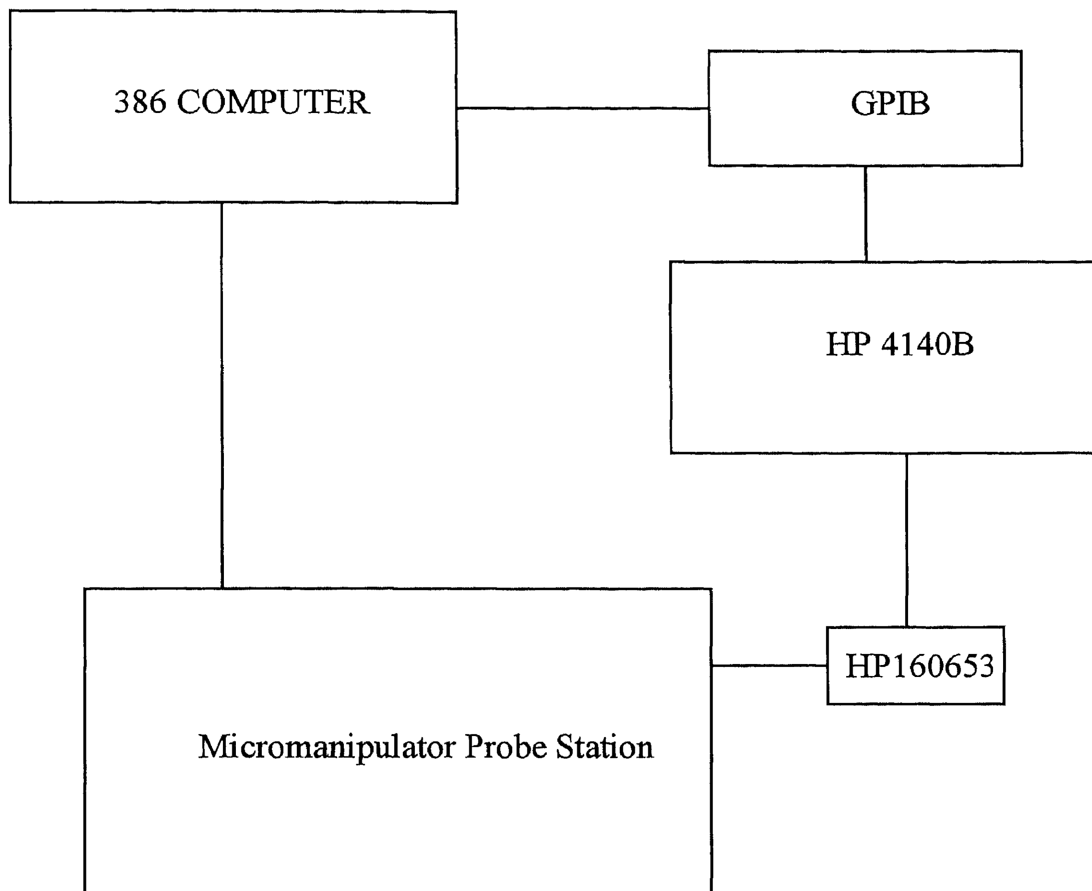


Figure 2.5 The diagram of Quasi static measurement system

1) Wafer inspection - microscope, Dektak profilometer

2) Nanometrics optical line width

3) Wet chemical station Ultratek mask/wafer scrub

4) Semitool spin/rinse dryers

5) Karl Suss exposure system

6) Nanometrics FTM

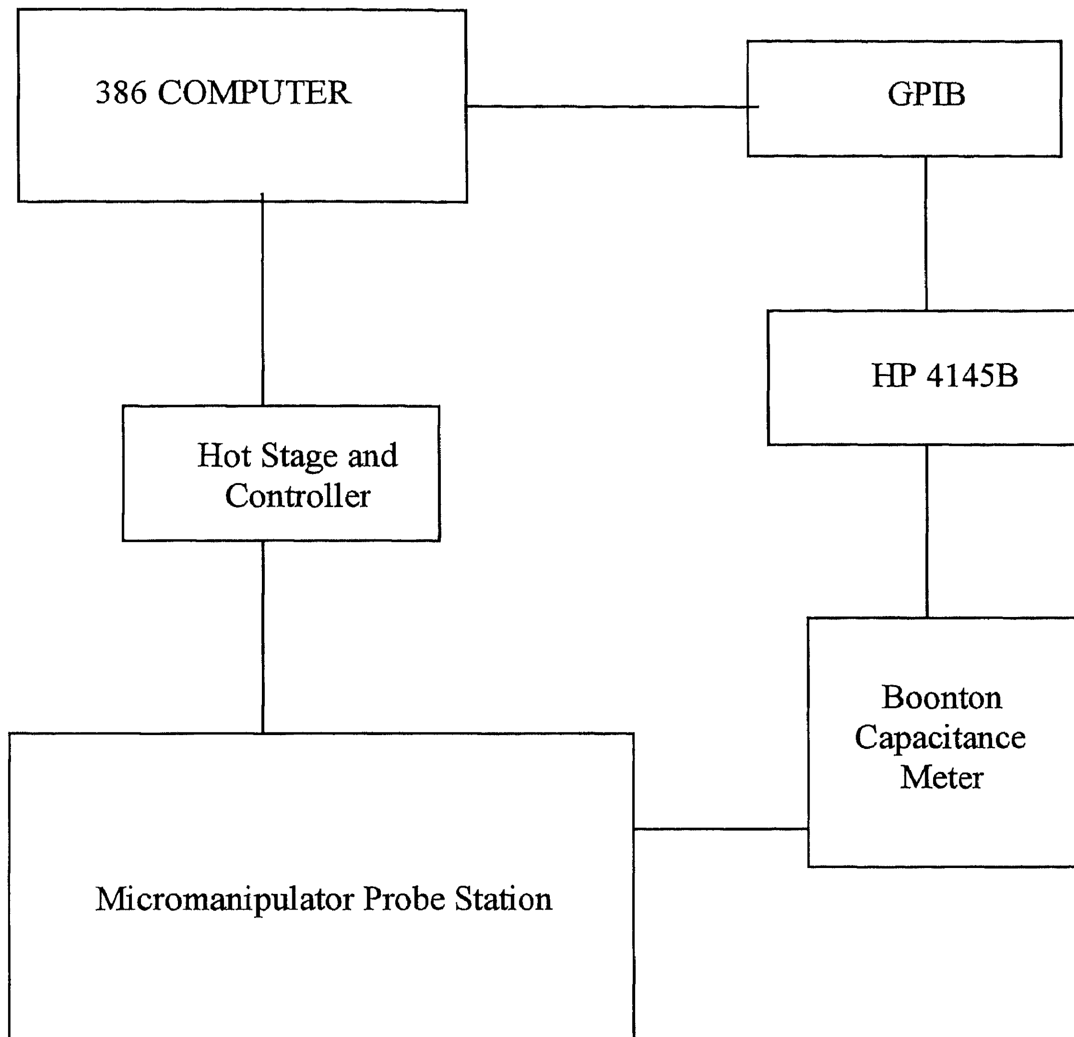


Figure 2.6 The diagram of high frequency C-V measurement system

7) Inspection microscope

8) MTI coat develop system

9) Drytek reactive ion etching system

10) Leitz MPV FTM

11) Varian sputtering system

12) BTU diffusion furnace

13) BTU LPCVD furnace

14) MDA toxic gas monitors

15) Tubewash station

16) MG Industries gas cabinets

2.3 Plasma Enhanced Chemical Vapor Deposition

2.3.1 Plasma-Enhanced CVD(PECVD)

Plasma deposition is a combination of a glow discharge process and low pressure chemical vapor deposition in which highly reactive chemical species are generated from gaseous reaction by a glow discharge and interact to form a thin solid film product on the substrate and electrode surface[29]. Since the plasma assists or enhances the CVD reaction, the process is denoted as Plasma-Enhanced CVD (PECVD).

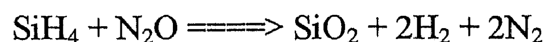
Plasma-enhancement offers an alternative to thermal energy for initiating chemical reactions leading to film deposition. Use of plasma frequently allows deposition at a much lower temperature than could otherwise be achieved, and/or it permits the use of source gases that would ordinarily be considered unreactive. This is the major advantage of PECVD. Radicals, which are predominant species in plasma field, tend to have high sticking coefficients, and also appear to migrate easily along the surface after adsorption. These two factors can lead to excellent film conformality. Desirable film properties such as good adhesion, low pinhole density, good step coverage, adequate chemical properties can

also be obtained by PECVD superior to those of APCVD or LPCVD films. Moreover, the mechanical strength of plasma deposited films is excellent due to their intrinsic compressive stress and high film density[30][31]. However, the complexity of reactions associated with PECVD makes the synthesis of stoichiometric composition difficult. And, as a consequence of the low temperature for film formation, gases are trapped in the films, which frequently causes thermal instability due to outgasing. Though sensitive MOS devices may be damaged by the radiation associated with the plasma discharge, the damage can usually be eliminated by a thermal annealing at the deposition temperature[32]. The main factors which affect the PECVD processes and the thin film properties include plasma power density, frequency as well as the substrate temperature and partial pressure of reactant gases, etc.

2.3.2 PECVD of SiO_2

The oxidation of silicon in an oxygen plasma allowed the controlled growth of thin, high-quality films of SiO_2 at temperature down to room temperature in a clean vacuum environment. The rate of oxidation and electrical properties may vary greatly depending upon the oxidation conditions. Plasma ion density and sample temperature are the two important factors affecting growth.

In PECVD SiO_2, siliane (SiH_4) and nitrous oxide (N_2O) are used. A typical reaction would be:



$$SiH_4 + N_2O \Longrightarrow SiO_2 + 2H_2 + 2N_2$$

The process can be carried out between 200 - 400°C. The PECVD SiO_2 films are known to contain hydrogen as well as nitrogen, and to have a high etch rate, high refractive index, low stress and to be oxygen deficient. Conformal coated, low pinhole count and excellent adhesion films were obtained by this technique.

Optimized gas composition of N_2O/ SiH_4 ratio 40/60 and rf power density 0.05W/cm^2 were employed to suppress gas phase reactions and enhance surface reactions. A typical deposition rate of 60 nm/min was readily obtained at 300°C. In our process, the PECVD is employed to deposit electronic quality SiO_2 .

2.3.3 PECVD Apparatus

The equipment used for thin film deposition is the Applied Materials AMP 3300IIA PECVD system with an external DES flow control equipment. The scheme of the reactor is given in figure 2.7. The reaction chamber is an aluminum cylinder with aluminum plates on both the top and the bottom, as upper electrode and susceptor, respectively. It has a conventional "radial flow" design and utilizes a mechanical pump/roots blower arrangement for the pumping system. The experimental procedures for deposition are:
1) Wafer loading. 2) Setting deposition conditions. 3) Film deposition.4) Post-deposition procedure. 5) Reactor etching

2.3.4 Helium-diluted PECVD

Thin films of high-quality silicon dioxide is deposited at low temperatures by Helium-diluted PECVD method, in which the deposition rate much lower than that used in

conventional plasma-enhanced processes is found to be crucial in obtaining material with reproducible, good properties. The controlled, slow deposition is achieved by using very low flow rates of reactive gases, together with a much higher flow of inert gas to ensure uniformity.

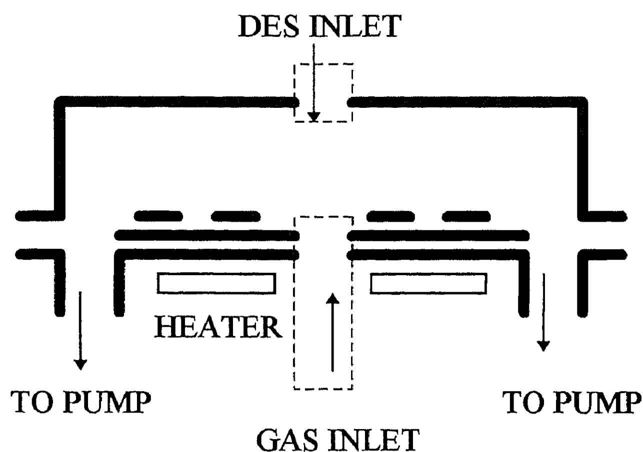


Figure 2.7 Schematic diagram of PECVD set-up

A typical PECVD reaction is a complex process, in which many variables must be monitored and/or controlled. Although each of these influences the end result to some degree, it is impractical to optimize each one in a given process. Some of these variables are constrained by equipment design, or by simple consideration of uniformity, etc. The most important factor in determining the electrical quality of the deposited material is found to be the rate of deposition. The more important variables which influence this are the total flow of reactive gases, chamber pressure, rf power, and the reactive gas ratio. This ratio of N_2O to SiH_4 is the primary factor in determining the stoichiometry of the film. To vary the deposition rate in a controlled fashion generally requires a change in

more than one parameter. Increasing the rf power increases the deposition rate but an increase in the reactive gas flow may be necessary to maintain uniformity. For a fixed power level, a decrease in the flow rate generally lowers the deposition rate but may require a decrease in chamber pressure for good uniformity. Moreover, the range of deposition which is possible using these conventional approaches is usually limited by design constraints. It proved difficult to obtain good control at low deposition rate. However, the approach adopted is to use a high flow of inert "carrier" gas (helium) to ensure uniformity and enable a wide range of deposition rate to be achieved simply by varying the reactive gas flow.

2.4 Low Pressure Chemical Vapor Deposition

2.4.1 Low Pressure CVD

The energy to activate and drive the chemical processes can be thermal, supplied by an electric glow discharge plasma, or attained by electromagnetic radiation. According to the type of energy supplied to initiate and sustain the reaction, CVD is classified into (1) Thermally activated reactions at various pressure range such as APCVD and LPCVD; (2) Plasma promoted reaction(PECVD).

In low pressure CVD processes, the reduced gas pressure enhances the mass transfer rate relative to the surface reaction rate, this makes it possible to deposit film uniformly in a relative highly economical close spaced positioning of the substrate wafers in a standup fashion.

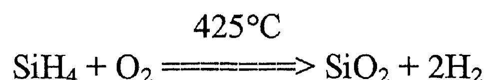
The outstanding advantage of LPCVD technique lies in the thickness uniformity of the films and the step coverage which are substantially improved over those obtained in conventional atmospheric pressure CVD reactors. The films have fewer defects, such as particulate contaminants and pinholes, because of the inherently cleaner hot wall operations and the vertical wafer positioning that minimize the formation and codeposition of homogeneously gas phase nucleated particles[33]. These considerations are especially important in VLSI processing where a very high device reliability and high product yield must be achieved.

2.4.2 LPCVD Apparatus

The equipment used in our cleanroom is computer-controlled BTU LPCVD furnace. The schematic of a LPCVD reaction chamber is shown in Figure 2.8. This is a front-end loading furnace commonly used for operational convenience.

The LPCVD system in our cleanroom is used to deposit the silicon dioxide in low temperature which is 425°C. The films are formed by reacting silane and oxygen.

The chemical reaction proceed as follows:



$$SiH_4 + O_2 \xrightarrow{425°C} SiO_2 + 2H_2$$

resulting in high-quality silicon dioxide films. The low deposition temperature of the silane-oxygen reaction makes it a suitable process for low-temperature requirement and also when films must be deposited over a layer of a aluminum.

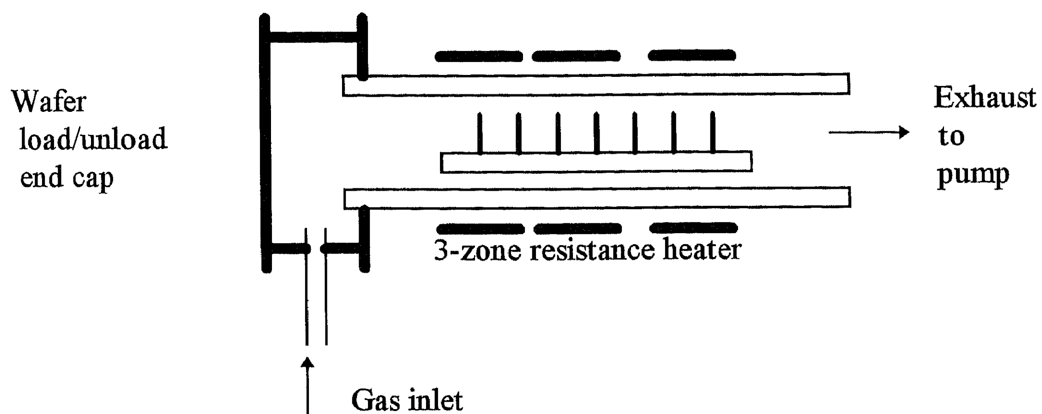


Figure 2.8 Schematic of LPCVD reaction chamber.

CHAPTER 3

EXPERIMENTAL II

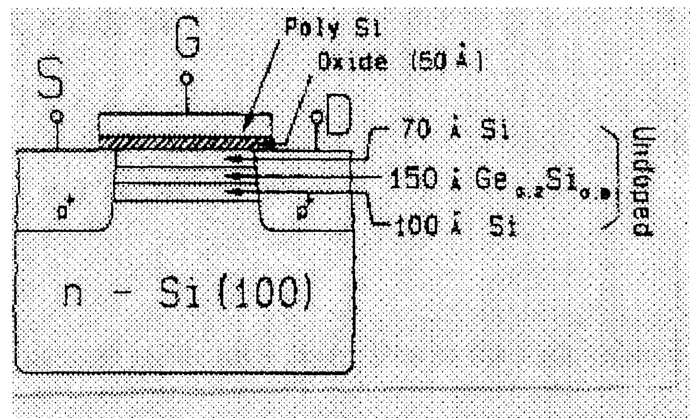
At present, the MOSFET is the dominant device used in VLSI circuits. MOSFET technology can be subdivided into NMOS (n-channel MOSFET) technology and CMOS (complementary MOSFET) technology, which provides n-channel and p-channel MOSFET's on the same chip. The performance of CMOS VLSI circuits is being improved steadily by aggressively scaling the device dimensions to the submicron regime. However, the scaling is becoming more and more difficult due to many technological and fundamental limitations. In order to circumvent these difficulties, new device structures and materials based on Si technology have been proposed. The high performance heterostructure SiGe p-MOSFET, which exhibits higher channel mobility than its bulk Si counterpart, was first proposed by Nayak et al[34][35]. The channel mobility in this device is improved by employing a strained $Si_{0.8}Ge_{0.2}$ layer as the conducting channel. The report[36] showed that high channel mobilities of 240 and 1500 $cm^2/V\ s$ at 300 and 77K, respectively, have been achieved for $Si_{0.5}Ge_{0.5}$ p-MOSFETs. For a short channel (0.25μm) $Si_{0.8}Ge_{0.2}$ device, a saturation transconductance of 167 mS/mm has been reported[37].

3.1 The SiGe MOSFET

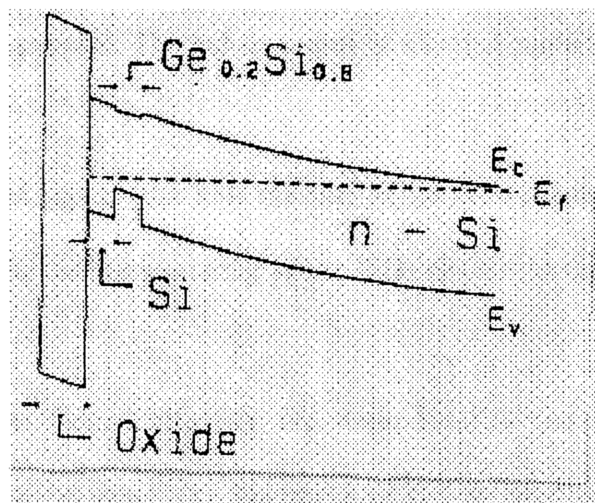
3.1.1 The Structure of SiGe MOSFET

The structure of SiGe device proposed by Nayak[34] is shown in Figure 3.1(a). The

structure is similar to a conventional Si p-MOSFET except that a pseudomorphic SiGe channel is used for channel conduction. Figure 3.1(b) gives the equilibrium band diagram of the above quantum-well structure which corresponds to the condition when the channel of the enhancement-mode p-channel device is inverted. The biaxial compressive stress in



(a)



(b)

Figure 3.1 (a) Schematic diagram of the layer composition of a p-type GeSi MOSFET. (b) Equilibrium band diagram of the structure shown in part (a).

SiGe lifts the degeneracy between heavy- and light-hole band, and the spin-orbit band is lowered in energy[38]. This results in a reduced bandgap and high in-plane hole mobility for the SiGe strained layer[39][40][41]. The reduction in bandgap of SiGe compared to bulk Si appears mostly as the valence band discontinuity at the Si/SiGe heterointerface

$$\Delta E_c = 0.02 \text{ eV} \tag{3.1}$$

$$\Delta E_v = 0.74x \text{ eV} \tag{3.2}$$

where x is the Ge content in the SiGe layer. Due to the high valance band discontinuity, the number of free holes in the buried SiGe channel (Figure 3.1(b)) will be higher than that in the adjacent Si layers. Therefore, the free carriers (holes in inversion) will be mostly confined in the SiGe channel. The enhancement in channel mobility is due to two main factors:

(1) Strained-induced high in-plan hole mobility of the SiGe channel.

(2) Reduced SiO_2/Si surface scattering as the SiGe channel is separated from gate SiO_2 by the Si cap layer.

There are two factors affecting the strain level in the SiGe channel: (1) Ge concentration, x, in the channel, (2) Thickness of the strained SiGe channel. High Ge content can improve the device performance because strain increases low-field hole mobility and high-field carrier saturation velocity. For a 1.6% strain, an enhancement

factor of 2.5 - 4.5 can be expected. Table 3.1 gives the theoretical calculation of in-plane hole mobility of strained SiGe layer on Si <100> substrate.

Furthermore, for fixed Si cap layer and SiGe channel thickness, hole confinement in the SiGe channel improves with increasing strain[35][43][44]. However, the thermodynamically stable critical thickness of strained SiGe on Si(100) decreases rapidly

Table 3.1 Theoretical calculation of in-plane hole mobility of strained SiGe layer on Si(100) substrate

Strain in SiGe (%)	**Hole mobility enhancement factor** ($\mu_{strained\text{-}SiGe}/\mu_{bulk\text{-}Si}$)
0.4	**1.2**
0.8	**1.4**
1.2	**1.8**
1.6	**2.4**
2.0	**3.6**
2.4	**5.1**

to practically unacceptable values with strain: 80, 40 and 25Å for $Si_{0.7}Ge_{0.3}$, $Si_{0.5}Ge_{0.5}$, $Si_{0.3}Ge_{0.7}$, respectively[45]. For a very thin SiGe channel (<40Å), Si/SiGe interface scattering may limit channel mobility[46]. Experimental results also showed that the channel mobility increases with increasing strain in SiGe which was summarized in Table 3.2. However, when the SiGe channel thickness considerably exceeds the thermodynamically stable critical thickness, degradation of mobility due to strain relaxation has been observed. Severe degradation of channel mobility has been reported for a 100Å channel with 1.6% strain[47] and a 70Å channel with 2.8% strain[36].

Table 3.2 Experimental low-field channel mobility of SiGe p- MOSFETs

Ref	Strain in SiGe channel (%)	SiGe Channel thickness (Å)	Temp. (T)	Bulk-Si p-MOS Channel mobility ($cm^2/V\ s$)	Strained-SiGe p-MOS channel mobility ($cm^2/V\ s$)	Improvement in mobility (%)
[34]	0.8	150	300	122	155	27
[47, 48]	0.8	100	300	120	166	38
	1.2	100			186	55
	0.8	100	90	372	573	54
	1.2	100			760	104
	0.8	125-300	300	95	150	57
[37]	0.8	125-300	82	250	400	60
	1.0	200	300	-	220	-
[49]	1.0	200	82	-	980	-
	2.0	70	300	141	240	70
[36]	2.8	70			160	13
	2.0	70	77	600	1500	150
	2.8	70			550	-8

3.1.2 SiGe-Channel MOSFET Design Parameters

The SiGe MOSFET design objective is to maximize the device transconductance. This can be achieved by confining high mobility holes in the SiGe channel while reducing the

density of low mobility holes which flow at the Si/SiO_2 interface. The following parameters are important for optimization of SiGe MOSFET performance:

(a) Choice of gate material.

(b) The method of threshold voltage adjustment.

(c) The SiGe profile in the channel.

(d) The Silicon-cap and gate-oxide thicknesses.

The following discussion is based on the investigation with the use of the one-dimensional Poisson simulator HETMOD (HeTerostructure MODeling)[50], which simulated the impact of each of these design parameter on device performance. All simulations assumed that SiGe channel widths exceeding 5nm, neglect of quantum effect, gate oxide 7nm, doping of the n-type substrate 5×10^{16} /cm^3, the Si/SiGe interface defect free, and the Si/SiO_2 interface density 5×10^{10} /cm^3.

A. Choice of Gate Material: n^+ - versus p^+ - doped Polysilicon

The type of gate material used in the SiGe p-MOSFET strongly influences the degree of the hole confinement to the SiGe channel[49]. HETMOD simulation results plotted in figure 3.2 show the hole densities in the SiGe channel and in the parasitic Si channel at the Si/SiO_2 interface as a function of gate voltage for both an n^+ - and a p^+ - gate SiGe p-MOSFET. The hole distribution in the SiGe p-MOSFET's is compared to the inversion holes present in a silicon n^+ - and a p^+ - gate p-MOSFET. This simulation considers that the vertical channel profile of the SiGe devices consists of a 5-nm Si cap layer and a 9-nm

wide 30% SiGe channel with a uniform n-type doping level of $1x10^{15}/cm^3$ throughout the Si and SiGe channel. The simulation shows that both SiGe MOSFET's exhibit that

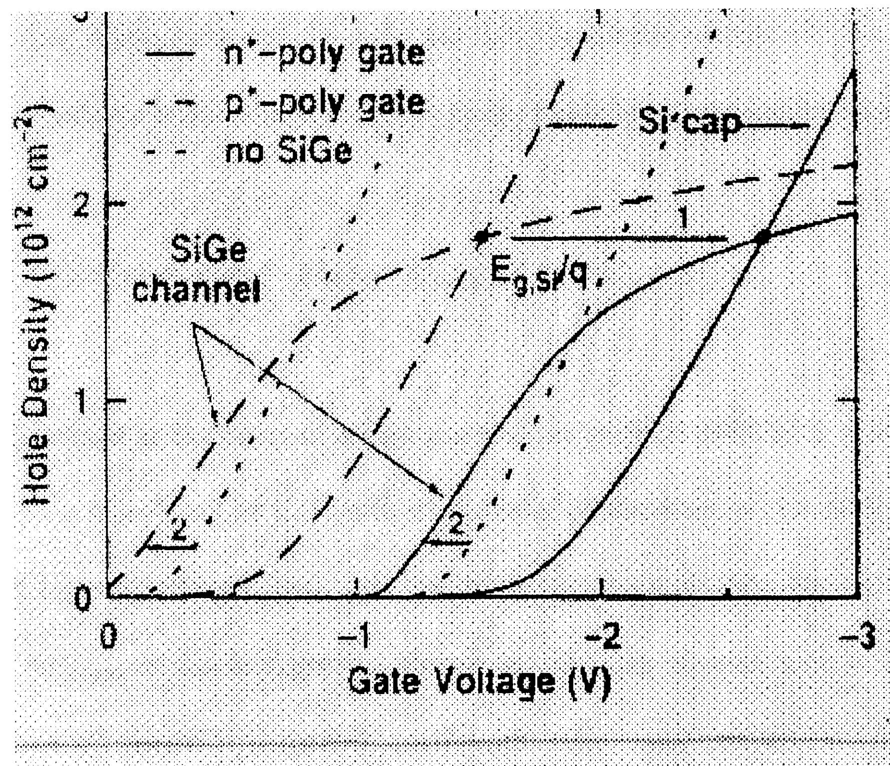


Figure 3.2 1-D Poisson simulation of the Si-cap and SiGe-channel charges for p^+- and n^+ gate SiGe MOSFET's without threshold voltage adjustment.

SiGe channel turns-on before the parasitic Si cap layer turns-on. The parasitic charge in the Si surface channel exceeds the SiGe-channel charge for gate voltage which is about 1.4 V higher than the turn-on voltage. The cross-over voltage is defined as the gate voltage at which the charges in the SiGe channel and in the Si cap are equal. The n^+ - and p^+ - gate SiGe p-MOSFET's show identical hole confinement, but the difference in workfunction of the gates results in a horizontal shift equal to the silicon bandgap.

The threshold voltage of a SiGe p-MOSFET is defined as the gate voltage at which the total concentration of holes in the Si and SiGe channel equals the concentration of

electrons in the n-type substrate[51]. The threshold voltage shift between the Si and SiGe MOSFET's is due to the energy band discontinuity at the Si/SiGe interface. The bandgap narrowing ΔEg is approximately 76 meV per 10% Ge introduced, and 97 % of this offset occurs in the valence band. Analytically, the SiGe threshold voltage can be expressed as:

$$V_t(SiGe) = V_t(Si) - \Delta E_v/q - Q_{channel}/C_{ox} + Q'_{channel}/C_{eq} \quad (3.3)$$

with $V_t(Si)$ defined as the onset of strong inversion in a silicon MOSFET. The gate-oxide capacitance C_{ox} is replaced by C_{eq} which is the series combination of the oxide capacitance and the Si cap capacitance. $Q_{channel}$ is the charge in the depletion region of a silicon MOSFET. $Q'_{channel}$ is the background charge in the SiGe channel and in the depleted region underneath the SiGe channel. From the simulation results plotted in Figure 3.2, the n^+ - gate p-MOSFET which has the threshold voltage of -1.2 V needs additional p-type dopants to move V_t to a lower value. But for the p^+ - gate p-MOSFET which has the threshold voltage of 0 V requires extra n-type dopants to increase V_t. When the flat channel doping profile is adjusted such that both the n^+ - and p^+ - gate p-MOSFET have identical threshold voltages of -0.6 V, the hole density is shown in Figure 3.3. The hole confinement to the SiGe channel for the n^+ - gate design is significantly better than that for the p^+ - gate design since the cross-over voltage for p^+ - gate is as low as -1.1 V and more than -3.0 V for n^+ - gate. Hence, Foe identical Si cap and SiGe channels, the n^+ polysilicon-gate SiGe p-MOSFET can be designed for operation at higher power supply voltages than the p^+ polysilicon-gate SiGe p-MOSFET.

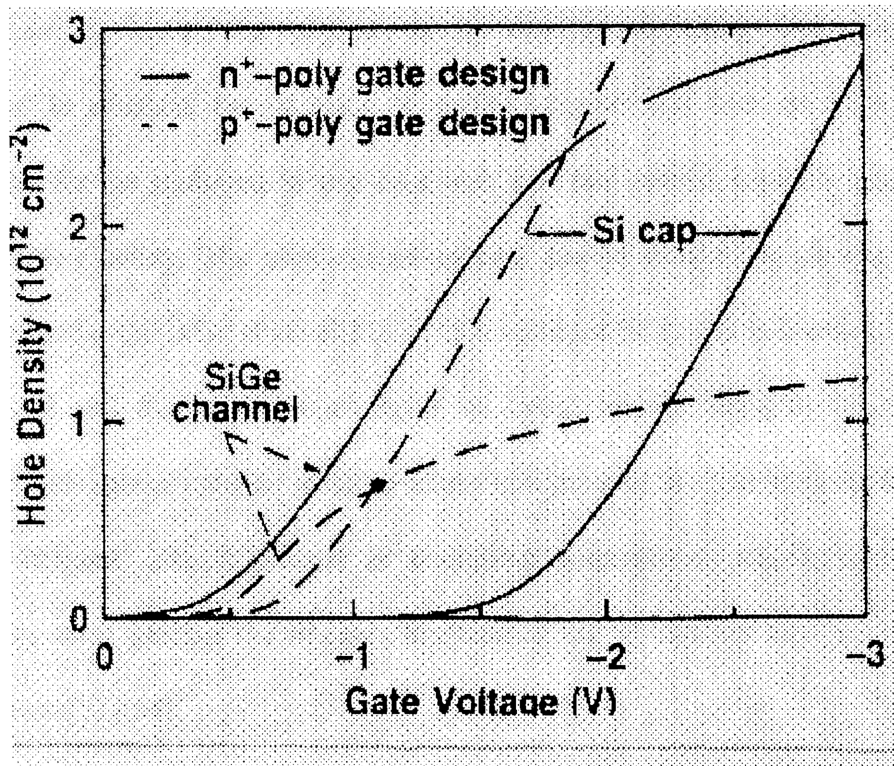


Figure 3.3 1-D Poisson simulation of the Si-cap and SiGe-channel charges for the p^+- and n^+- gate SiGe MOSFET's of figure 3.2 but with a -0.6 V threshold voltage.

B. The Method of Threshold Voltage Adjustment

HETMOD simulation show that shifting the threshold voltage of the n^+ - gate SiGe p-MOSFET to -0.6 V requires boron dose of $1.5 \times 10^{12}/cm^2$. But the high doping level in the SiGe channel leads to ionized impurity scattering which degrades the mobility. This problem can be avoided by using modulation-doping which locates the acceptor atoms outside the SiGe channel, physically separated from the mobile holes. The threshold voltage is independent of whether the boron-doped layer is located above or below the SiGe channel.

When the dopants are located above the SiGe channel, the thickness of the Si cap must increase to locate the dopants in it, therefore reducing the gate-to-channel capacitance. In addition, the parasitic Si surface-channel will turn on at a lower gate voltage than for the undoped Si cap case and also the ionized impurity scattering will affect the hole mobility. The above disadvantages can be avoided by placing the boron-doped layer under the SiGe channel[52]. A thin undoped Si spacer is located between the SiGe channel and the boron-doped layer to avoid ionized impurity scattering. The thickness of this spacer must be small to insure that most of the carriers are transferred to the SiGe channel. This technique is becoming common in state-of-the-art CMOS technologies since placing the dopants underneath the Si channel also improves short-channel effects[53][54].

C. The Germanium Profile Engineering

Hole confinement in the SiGe channel is largely dependent on the shape of the SiGe channel. To maximize the hole concentration in the SiGe channel and insure adequate confinement up to high gate voltages, a large valence band discontinuity at the top Si/SiGe films heterointerface is required. However, it is important to keep highly strained SiGe film stable throughout device fabrication. Matthews-Blakeslee gave the critical layer thickness limit on the SiGe thickness which is shown in Figure 3.4. From the results of simulation, the cross-over voltage is linearly proportional to the relative Ge concentration and more carriers flow in the Si cap layer as the gate voltage rises. In order to ensure that

the majority of holes flow in the SiGe channel for gate voltages equal to or more than -3.0 V, the Ge percentage must rise above 30%.

The results of 1-dimension Poisson simulations given in Figure 3.5, which compares a graded Ge profile to a uniform profile for the n^+- gate p-MOSFET design with identical integrated Ge doses, shows that grading the channel instead of keeping it flat results in a large current drive as the mobility of the holes in the SiGe channel is higher than that of the holes the Si cap layer. In addition, a built-in electric field created in the graded channel forces the holes towards the top surface which can maximize the gate-to-channel capacitance and guiding the holes away from the ionized acceptors.

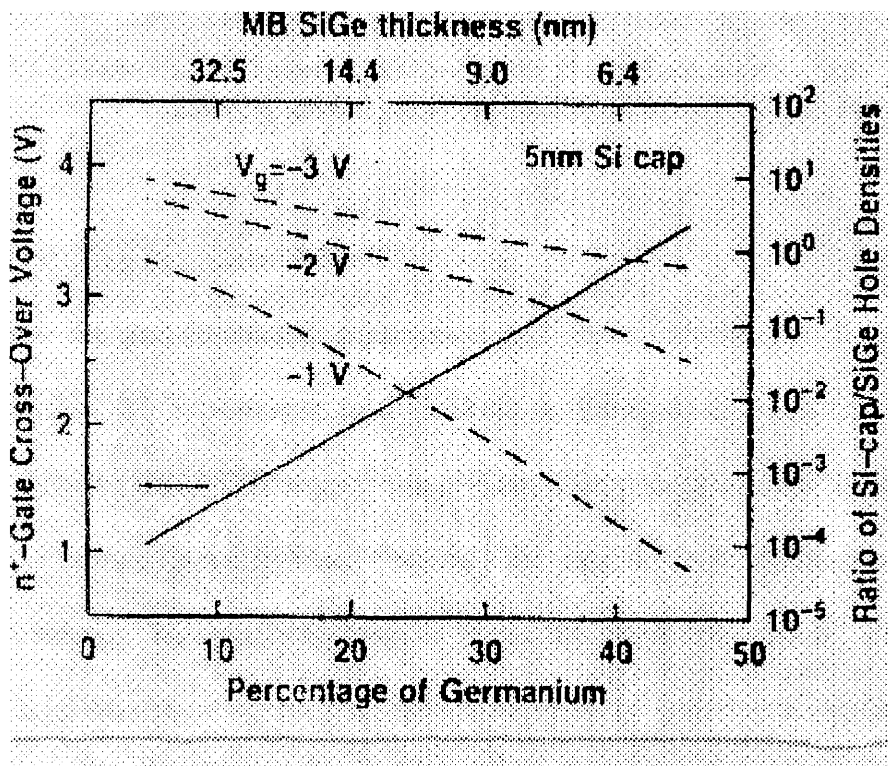


Figure 3.4 N^+-gate cross-over voltage versus %Ge in the SiGe channel for a flat Ge profile. The SiGe film thickness is adjusted such that it is stable following Matthews-Blakeslee (MB) stability criterion. No threshold voltage adjustment used in these device.

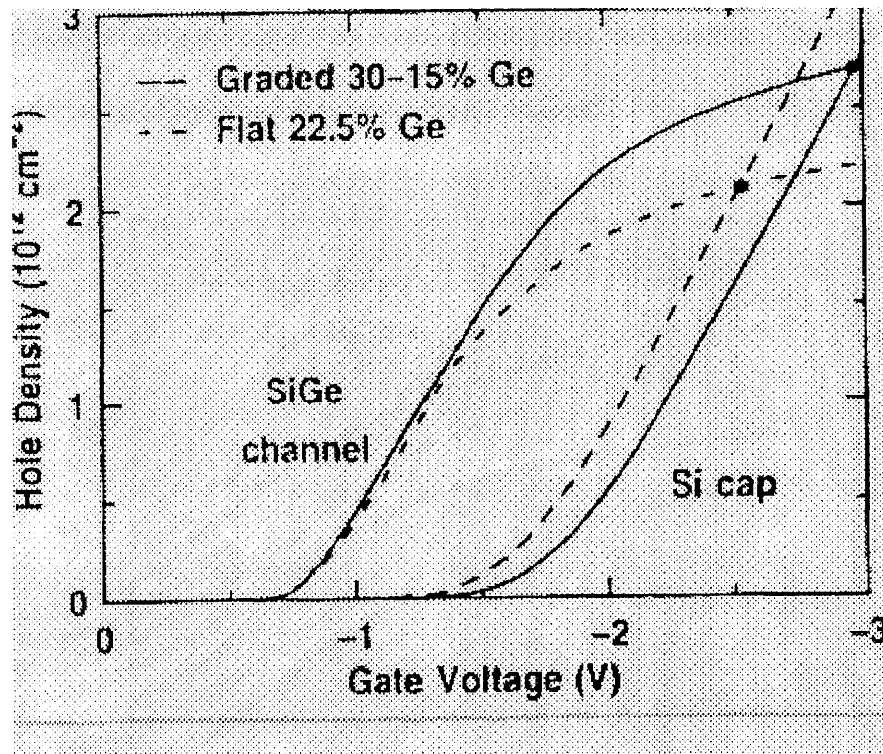


Figure 3.5 1-D Poisson simulation of the Si-cap and SiGe-channel charges in a n^+- gate SiGe p-MOSFET's, comparing graded versus uniform SiGe channels with identical total integrated Ge dose.

D. The Silicon Cap and Gate Oxide Thickness

To maximize the gate-to-channel capacitance and hence increase the SiGe MOSFET transconductance, it is important to minimize both the thickness of the silicon cap and that of the gate oxide. HETMOD simulations indicate that decreasing the Si cap thickness increases the cross-over voltage and reducing the gate oxide thickness decreases the cross-over voltage. This results is shown in Figure 3.6 where the ratio of holes present in the Si cap layer over those confined to the SiGe channel is plotted as a function of Si cap thickness for both the n^+ - and p^+ - gate designs and for two different gate thickness. If the Si cap is too thin, interface scattering will degrade the hole mobility but conversely

increase the channel-to-gate capacitance and hence transconductance. Therefore the Si cap thickness is determined by a mobility/capacitance tradeoff.

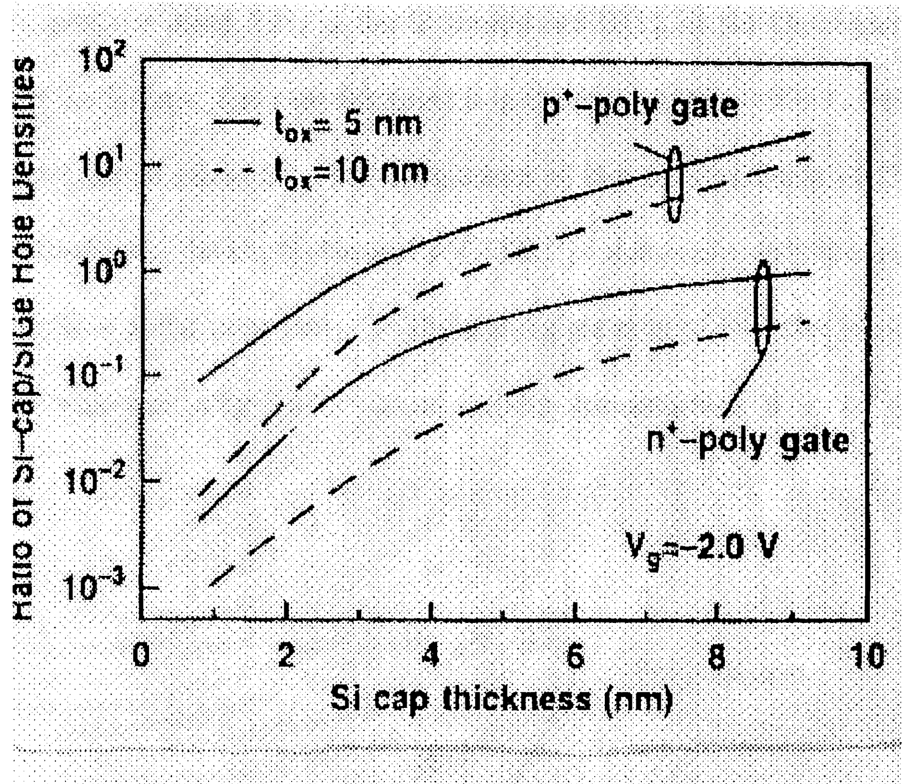


Figure 3.6 Ratio of holes flowing in the Si cap layer over those confined in the SiGe versus varying Si cap thickness (Vg = -2 V, T = 300K) for different n^+- and p^+-gate designs.

3.2 Fabrication of SiGe Channel MOSFET

The fabrication of SiGe MOSFET is carried out in NJIT cleanroom. The process design is based on NJIT cleanroom condition and the properties of SiGe material which is easy to relax in the high temperature procedure. Therefore, a series of low temperature processes are introduced to replace the high temperature processes used in Si MOSFET fabrication.

The device structure used in this work is shown in Figure 3.7. For making n-MOSFET, the starting material of SiGe wafer was grown by conventional CVD at atmospheric pressure using SiH_4 as the Si source and GeH_4 as the Ge source. SiH_4 was also used for the Si caps. The caps thickness is in the range 1500 - 1900 Å. Substrate is p-type <100> oriented si wafer. For comparison of the characteristics of SiGe-channel device and Si-channel device, Si-channel MOSFET is also made with the same process designed for SiGe at the same time. The starting material of Si wafer is p-type <100> Si-substrate with resistivity 14-21 Ω-cm(doping concentration $8 \times 10^{14}/cm^3$ - $1 \times 10^{15}/cm^3$).

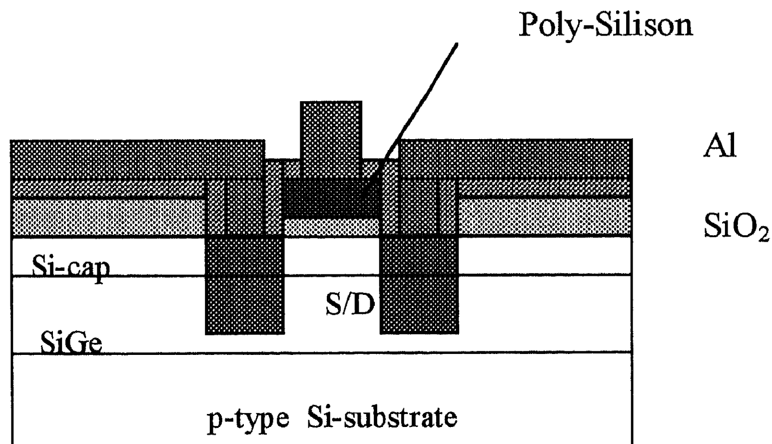


Figure 3.7 The structure of SiGe channel n-MOSFET

In this SiGe n-MOSFET process, there are four lithographic operations, four film-formation operations, two ion implantations and four etching operations.

3.2.1 Mask of Photolithograph

The masks used in SiGe n-MOSFET process were designed by Toros. These microelectronics test chip is composed of many device test structures for 2-micro process. Chip size is 3.58mm × 3.58mm. The MOSFET transistor structures include:

1) Four MOS transistors with L = 8 μm and W = 2 μm, 4 μm, 8 μm, 16 μm.

2) Four MOS transistors with W = 8 μm and L = 2 μm, 4 μm, 8 μm, 16 μm.

3) Four MOS transistors with L = W = 1.5 μm, L = W = 2 μm,

L = W = 3 μm, L = W = 4 μm.

There are four masks for this process which correspond to four different processes:

First mask(#1): Active device area definition.

Second mask(#2): Poly-silicon gate pattern definition.

Third mask(#3): Contact window definition.

Fourth mask(#4): Metal connection layer pattern definition.

3.2.2 Process Flow Procedure and Chart

The main procedures in this process include 18 steps:

1. Wafer clean
2. LTO SiO_2
3. Photolithograph - #1 Mask
4. Wet etching - Active area
5. LPCVD LTO Gate Oxide
6. Post - LTO Annealing

7. Threshold voltage adjustment ion implantation

8. Poly-Si deposition

9. Photolithograph -- #2 Mask

10. RIE Poly-Si

11. S/D implantation and Poly-Si doping

12. Post-annealing

13. LTO SiO_2

14. Photolithograph - #3 Mask

15. RIE LTO

16. Aluminum deposition

17. Photolithograph

18. Aluminum etching

19. Aluminum alloy annealing

3.2.3 SiGe-Channel MOSFET Process Traveler

In this section, the process is introduced step by step with calculation and explanation.

Step 1: Wafer clean

The first step for starting the process is always the wafer cleaning. The purpose is to remove the organic and inorganic contamination which exist on the surface of the wafer. The wafer clean used in NJIT cleanroom is p-clean followed by rinsing of deionized water. P-clean is consisted of three steps:

1) clean in the mixture of 5:1 H_2SO_4:H_2O_2 with 110°C and 10 minutes.

2) rinse with hot deionized water for 10 minutes.

3) rinse with cold deionized water for 5 minutes. Then spin the wafer dry.

Step 2: LPCVD LTO SiO_2 (field oxide)

This step is to form the oxide isolation region. The oxide is deposited by the LPCVD LTO method. Before the wafer is sent into the furnace, the furnace pre-clean procedure has to be done by 100:1 :: H_2O:HF for 1 minute. The deposition rate is about 15Å/min and the temperature is 425°C. The source is 300sccm SiH_4 and 75 sccm O_2 with pressure of 500m Torr. The film thickness is determined by many factors: (1) For 2 μm process, the thickness of field oxide is typically 0.5 to 1 μm.(2) serve as a mask for S/D ion implantation(120keV, $3 \times 10^{15}/cm^2$). Refer to Step 9 for detail. (3) the step of oxide. Since this is not the localized oxidation of silicon(LOCOS) process, after the formation of active area, the step is the same height of the oxide. If it is too high, the poly-silicon gate opening may occur at the corner of the step. (4) the oxide thickness loss during the process. Because the LPCVD LTO SiO_2 structure is loose and every furnace pre-clean will etch 530 Å approximately in 1 minute. Considering above factors, the film thickness is designed as 8000 Å in this process. Figure 3.9 show the cross-sectional view of SiGe MOSFET with formation of field oxide.

Step 3: Photolithograph - #1 Mask

This step defines the active device area which is patterned by mask #1. To do thephotolithograph, the first thing to do is to apply Photoresist which thickness is about 1.2μm determined by the revolution (4000 rpm) and time (20 seconds). Then bake the photoresist in bake box oven at temperature 115°C for 20 minutes. Third step is to do the

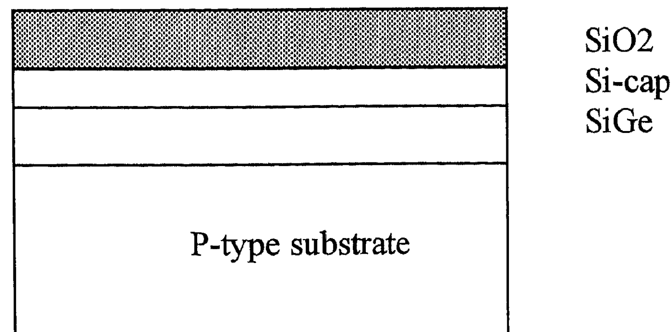


Figure 3.8 Cross-sectional SiGe MOSFET with field oxide

alignment and exposure, followed by developing. Finally, the film of photoresist has to be baked again to make it hard enough for etching. Figure 3.10

Step 4: Wet etching - Active area

The wet-etching of field oxide is done in the 7:1 BOE etchant with $HF:H_2O:NH_4F$. The

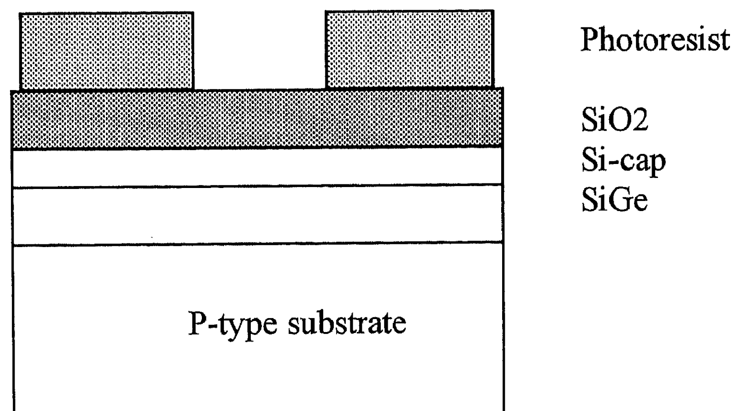


Figure 3.9 Cross-sectional SiGe MOSFET with photoresist

etching rate for LPCVD LTO SiO_2 is about 3300 Å/min. Since the wet chemical etching is isotropic, it should be very careful to control the ending time to avoid over-etching that will result in the larger active area than patterned area. After etching, photoresist is removed by p-strip solution (same as p-clean). Then clean the wafer for next step. Figure 3.11 is the cross-section of the formation of active area.

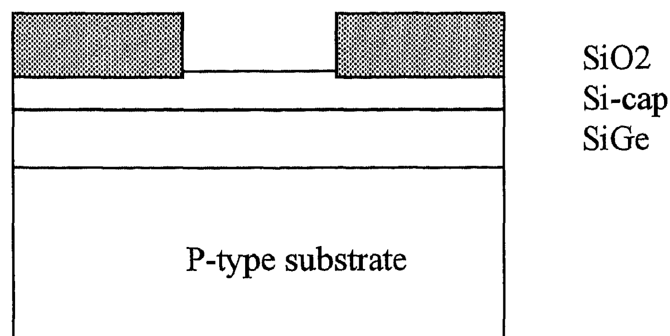


Figure 3.10 Cross-sectional SiGe MOSFET with etched field oxide

Step 5: LTCVD LTO gate oxide

In this process, the gate oxide is made by the deposition of LPCVD LTO which is introduced in step 2. The thickness of gate oxide is 435 Å according to 2-Micron process MOSIS parameters. This is a low temperature process, the quality of the oxide film is not as good as thermally grown oxide. Figure 3.12 shows cross-sectional SiGe MOSFET with gate oxide.

Step 6: Post-LTO annealing

Post-LTO annealing is necessary because it can reduce interface density which is brought by LPCVD deposition. Annealing is carried out in nitrogen at 600-650°C for 30 minutes.

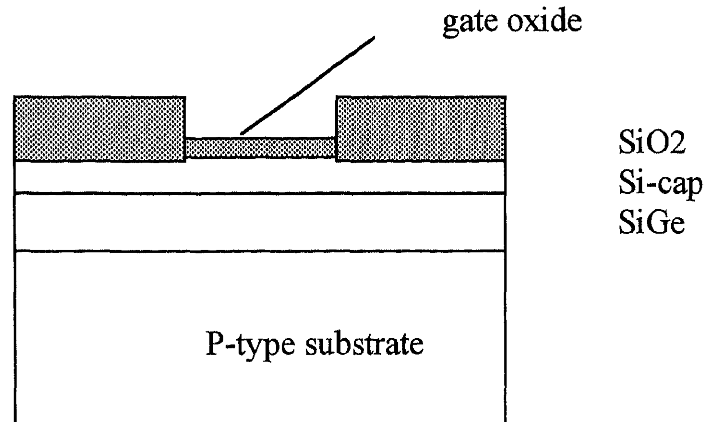


Figure 3.11 Cross-sectional SiGe MOSFET with etched field oxide

Step 7: Threshold voltage adjustment ion implantation

The experimental result shows that the flat-band voltage of Al-Si(p-type substrate) MOS structure is about -2 V after post-LTO annealing. But in this process, the gate material is poly-silicon. The difference of work function of poly-silicon and aluminum to p-type substrate is about -0.15 V. Hence the flat band voltage applied for poly-silicon to p-type substrate is about -2.15 V. The Threshold voltage is

$$ {}_t(Si) = V_{fb} + 2\Psi_B + \frac{\sqrt{2\varepsilon_s q N_A (2\Psi_B)}}{C_o} \qquad (3.4) $$

where

$$ \Psi_B = \frac{kT}{q}\ln\left[\frac{N_A}{n_i}\right] = 0.0259 \times \ln\left[\frac{1\times 10^{15}}{1.45\times 10^{10}}\right] = 0.29V \qquad (3.5) $$

$$C_o = \frac{\varepsilon_{ox}}{d} = \frac{3.9\times(8.85\times10^{-14})}{435\times10^{-8}} = 7.93\times10^{-8}\,F/cm^2 \quad (3.6)$$

Hence

$$V_t\,(Si) = -2.15 + 0.58 + 0.175 = -1.4\ V \quad (3.7)$$

From equation (2), $x = 0.2$, $\Delta Ev = 0.74x$ eV = 0.15 eV. So

$$V_t(SiGe) = V_t\,(Si) - \Delta Ev/q = -1.4 - 0.15 = -1.55\ V \quad (3.8)$$

To adjust the threshold voltage of the device to 0.9 V, $\Delta\ V_t(SiGe) = 2.45$ V and the p-type Boron ion implantation is required. The Boron charge causes a flat-band shift of

$$\Delta\ V_t(SiGe) = qF_B/C_o \quad (3.9)$$

$$F_B = C_o\,\Delta\ V_t(SiGe)/q = 1.21\times 10^{12}\ /cm^2 \quad (3.10)$$

Considering the thickness of gate oxide, the threshold voltage ion implantation can be done by p-type Boron $1.21 \times 10^{12}\ /cm^2$ at 20 keV.

Step 8: Poly-Silicon Deposition

The poly-silicon is deposited by LPCVD. The deposition parameters are 300sccm SiH_4, temperature 600°C, and pressure 400 mTorr. The deposition rate is 20Å/min. Since the

poly-silicon is gate material as well as the mask for ion implantation of S/D, so the thickness of poly-silicon is selected as 3600Å. It takes about 3 hours.

Step 9: Photolithograph - #2 Mask

This photolithograph defines the pattern of poly-silicon and forms the gate.

Step 10: Reactive-ion etching (RIE) Poly-Silicon

The RIE is done in DRIE-100. The plasma gases used in RIE are SF_6 50sccm and Freon - 115 50 sccm. The pressure is 150 mTorr and power is 400W. The etching rate is about 1000 Å/min. For 3600Å poly-silicon, etching time is about 3 minutes and 40 seconds. After etching, the photoresist is removed by p-strip. Figure 3.13 shows cross-sectional SiGe MOSFET with poly-silicon.

Step 11: S/D Ion Implantation and Poly-Silicon doping

To make a n-MOSFET device, the S/D is ion-implanted n-type dopant such as phosphorus. According to MOSIS 2-micron process requirement, the junction depth is

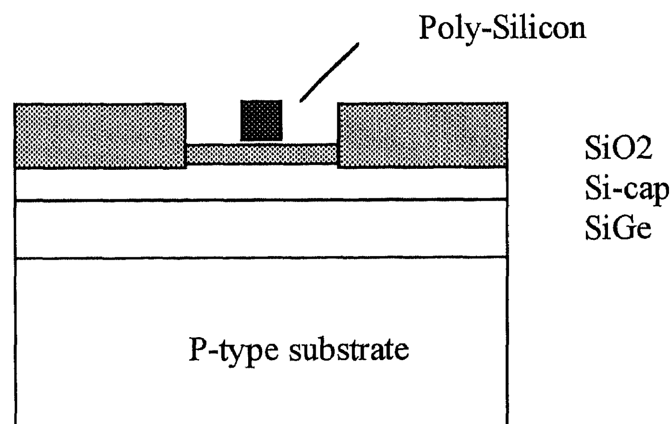


Figure 3.12 Cross-sectional SiGe MOSFET with poly-silicon

about 0.2 μm. In this process, the S/D is doped by ion-implantation phosphorus. At the same time, the poly-silicon is doped as well. From the figure 22 of chapter 10 of Semiconductor Device(S.M.SZE), if the ion-implantation energy is 120 keV, the corresponding projected range R_p is 0.15 μm and projected straggle ΔR_p 0.053 μm in Silicon while the R_p is 0.1215 μm and ΔR_p 0.038 μm in SiO_2. The calculation with equation(11) shows that if the substrate doping concentration is $1 \times 10^{15}/cm^3$ and ion dose is $3 \times 10^{15}/cm^2$, the junction depth is 0.2 μm. This satisfies the requirement of

$$n(x) = \frac{S}{\sqrt{2\pi}\Delta R_p} \exp\left[-\frac{\left(x - R_p\right)^2}{2\Delta R_p^2} \right] \qquad (3.11)$$

the device. On the other hand, the poly-silicon is doped at the same time of the formation of source/drain.

Step 12: Ion-Implantation Post-Annealing

Because of the damaged region and the disorder cluster that result from ion implantation, semiconductor parameters such as mobility and lifetime are severely degraded. In addition, most of the ions as implanted are not located in substitutional sites. To activate the implanted ions and to restore mobility and other material parameters, the post-annealing must be done at an appropriate combination of time and temperature. S.M.SZE book shows that if the doping dose of phosphorus is lager than $2 \times 10^{15}/cm^2$, 90% of the implanted ions are activated by a 30-min annealing at the temperature of 600 °C. This low temperature can not cause the implanted doping profile broadened by diffusion. Therefore,

in our process, the post annealing condition is chosen as temperature 600°C for 30 minutes.

Step 13: LPCVD LTO SiO_2

The next step is to open the contact windows. Before this, the oxide deposited for 3000Å by LPCVD LTO is employed as the insulator between poly-silicon and matal layer.

Step 14: Photolithograph - #3 Mask

This photolithograph defines the pattern of contact windows.

Step 15: Reactive-ion etching (RIE) LTO SiO_2

RIE LTO SiO_2 is done at the DRIE - 102. The conditions are: CF_4 50 sccm, Freon 23 50 sccm, Freon 116 100 sccm, pressure 300 m Torr and power 800 Watts for about 15 minutes. After RIE, the photoresist is removed by p-strip.

Step 16: Aluminum Deposition

The technique used for Aluminum deposition in our cleanroom is sputter deposition. In this system, deposition rate is 10 Å/sec. Base pressure is 8.0×10^{-7} Torr and temperature 300 °C. For the thickness of 3000 Å, the deposition time is about 5 minutes.

Step 17: Photolithograph - #4 Mask

This step defines the pattern of metal layer.

Step 18: Wet Etching Aluminum

The wet etching of Aluminum is carried out in the Aluminum Etch Solution. The etch solution is the mixture of Phosphoric Acid(85%) : Nitric Acid(70%) : Acetic Acid(99.7%) : Water :: 16 : 1 : 1 : 2 (Volumes). The etch rate increases with the increase of temperature. The relation between etching rate and temperature is shown in figure 3.14.

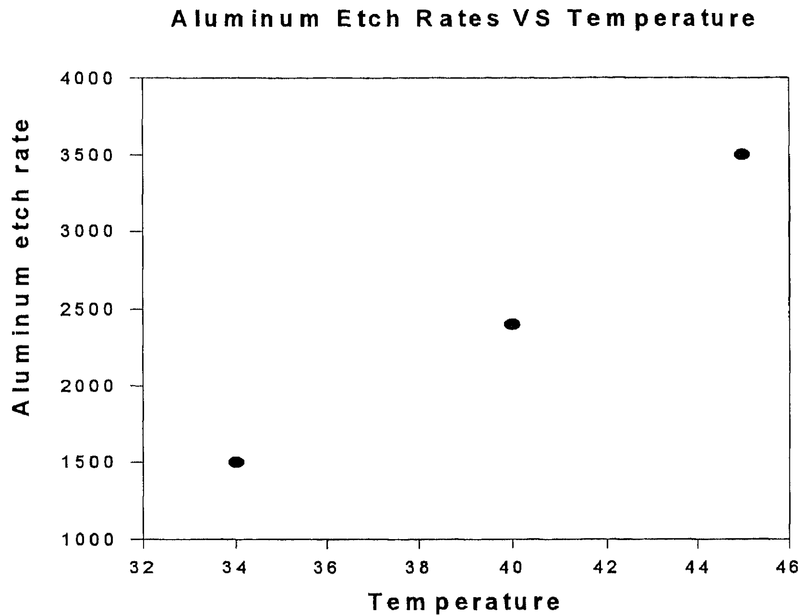


Figure 3.13 The relation between Aluminum etching rate and temperature

The above introduces the process of SiGe MOSFET in detail. Figure 3.7 gives the final cross-view of the MOSFET.

Step 18: Aluminum Alloy Annealing

This step is to form good ohm contact of aluminum with silicon source and drain and polysilicon. The process is T= 450°C, for 20 minutes in nitrogen.

CHAPTER 4

RESULTS AND DISCUSSIONS

4.1 PECVD SiO_2

Experimentally the PECVD silicon dioxide films were deposited in the Applied Materials AMP 3300IIA PECVD system with external DES flow control equipment. The starting material is 5 inch <100> p-substrate wafers which resistivity is 1 - 5 Ω-cm.

4.1.1 Deposition Rate With Distance

In this PECVD system, the gas inlet is at the center of susceptor. The deposition rate decreases with the increase of the distance from the center. Figure 4.1 shows the depletion effect of gas flow along the radius of the susceptor [62] . The results shows that the deposition rate in the outer zone was about 20% less than that in the center zone. The high flow rate of helium make the film much more uniform than there is not existence of helium which is about 50% less from center to outer zone.

4.1.2 Temperature Effect

Temperature effect on the growth rate and properties of the SiO_2 films was studied over a series of temperatures ranging from 200°C to 350°C. The flow rates of DES , nitrous oxide and Helium were set at 12 sccm, 172 sccm and 600 sccm respectively. Total pressure of the reactor was maintained at 0.3 Torr. Plasma power was kept at a constant level of 500W(0.15W/cm^2) and frequency was 100 kHz throughout the temperature series

study. The studies show that the deposition rate decreased as the substrate temperature increased. Figure 4.2 shows the deposition rate as a function of substrate temperature.

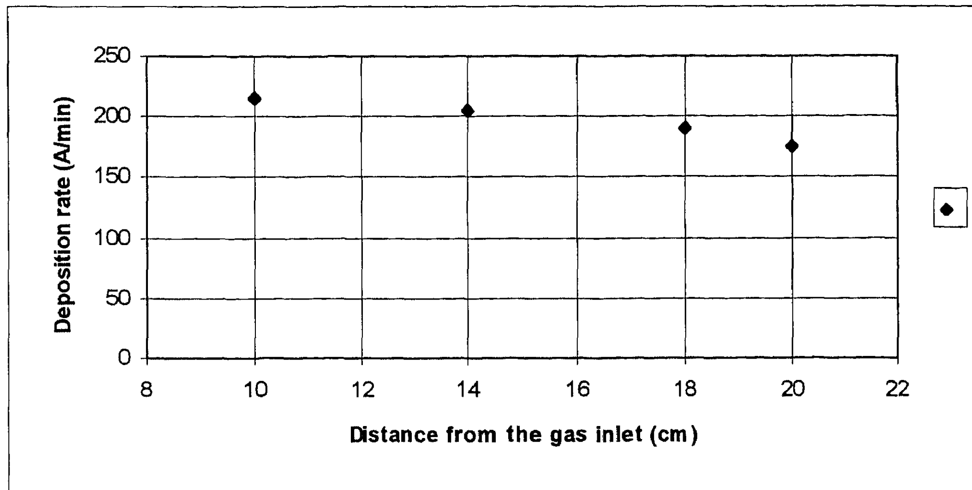


Figure 4.1 Deposition rate with the distance from the Gas inlet(cm). Deposition condition: 300°C, 0.3 Torr, Flow rate N_2O=172 sccm, DES=12sccm, He=600sccm, Plasma power 0.15W/cm^2, 100kHz

The decrease in growth rate with increasing temperature were also observed in the PECVD process of silicon dioxide from silane [55] and TEOS [56] and PECVD process of silicon nitride from DES [57]. This effect is contrary to the temperature dependence of LPCVD process. This difference between LPCVD and PECVD is possibly the reason that the thermal energy played the different roles in reactions. In LPCVD process, surface reaction includes thermal decomposition of the reactant gas molecules. Increasing temperature results in the increase of the reactants. Thus the deposition rate increases. In the PECVD process, the free radicals are produced by electron impact dissociation such as oxygen radical O^*. The increasing temperature increases the collision of reactive radicals. Thus the deposition rate is reduced.

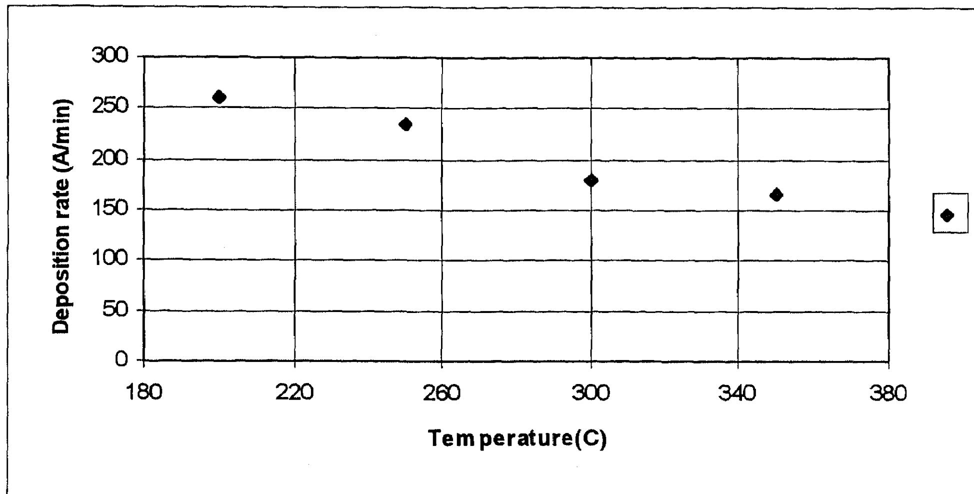


Figure 4.2 Deposition rate as a function of temperature. Deposition condition: 0.3 Torr, Flow rate N_2O=172 sccm, DES=12sccm, He=600 sccm, Plasma power 0.15W/cm^2, 100kHz

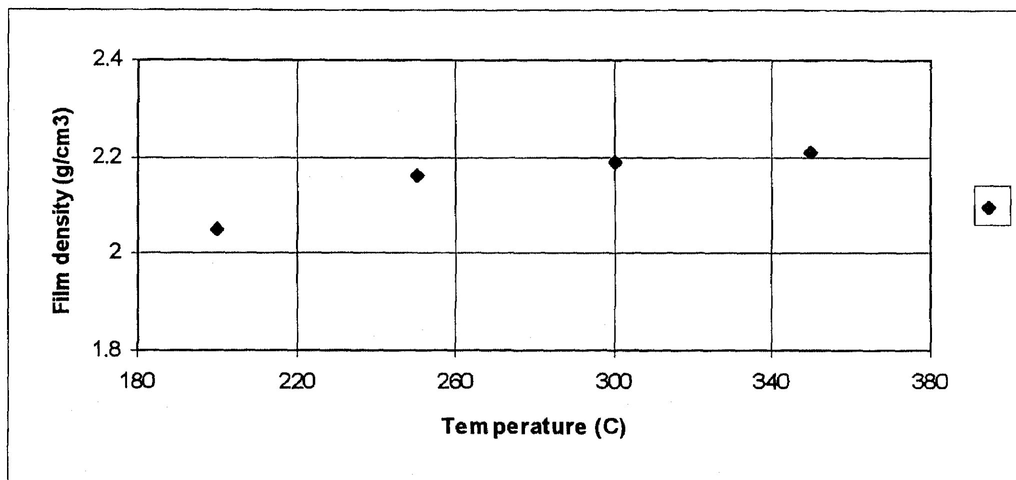


Figure 4.3 Film density as a function of temperature. Deposition condition: 300°C, 0.3 Torr, Flow rate N_2O=172 sccm, DES=12sccm, He=600 sccm, Plasma power 0.15W/cm^2, 100kHz

Figure 4.3 shows the relation of film density with the temperature. The oxide film density increases with increasing susceptor temperature. That means better film can be achieved at the higher temperature. But oxide density is still lower than that of thermally grown oxide ($2.27 g/cm^2$). This effect may be due to the reasons of loose structure of the amorphous deposit and the moisture and product gases trapped in the porous film. When the substrate temperature is higher, there is less moisture and other product gases absorbed by the film at the same time of deposition. Another reason is that at the higher temperature, the deposition rate is lower and the molecules have enough time to site themseves which make the film structure tight, hence increasing the film density. The third reason is that at the higher temperature, the film is difficult to absorb the impurities because the surface is less sticky.

The film refractive index of PECVD silicon dioxide is also affected by susceptor temperature and the ratio of N_2O/DES. The refractive index measured by ellipsometer can be use to detect deviations from stoichiometry in good quality oxide. The refractive index of the deposits is higher than that of thermally grown oxide (1.465) which is shown in figure 4.4. This must result from some differences in stoichiometry. This may be caused by the oxygen-deficient films which were generally observed in PECVD oxides [56][58] and more polar impurities such as water molecules and hydroxyl groups of the silanol [59] as well as carbon impurities. The oxygen radical O^* of reaction is coming from the N_2O. Increasing the ratio of N_2O/DES can increase the oxygen radical O^* in the reaction. Thus it can reduce the refractive index. Figure 4.5 shows the effects of changing the ratio of N_2O/DES to refractive index. In experiment, although there is a small but distinguishable

difference with the change of the ratio of N_2O/DES, it is still difficult to interpret what is the perfect ratio of N_2O/DES. However we do know that it is not silicon rich which can be confirmed by the result of refractive index by ellipsometry. Hence in practice, we set the ratio of N_2O/DES as 172/12 for which we obtained the relatively better results.

Some of the inferences can be confirmed by a typical FTIR spectrum of the PECVD SiO_2 film deposited from DES and N_2O according to the work done in reference [60][61][62] (Figure 4.6). The three absorption at 1080cm^{-1}, 800cm^{-1} and 600cm^{-1} characterized SiO_2. The broad absorption at about 3600^{-1} which was assigned to O-H

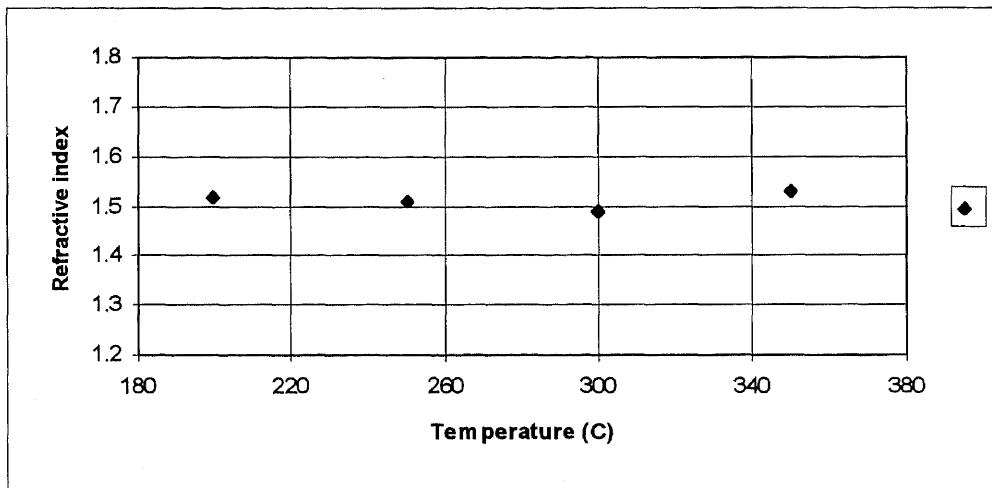


Figure 4.4 Refractive index as a function of temperature. Deposition condition: 300°C, 0.3 Torr, Flow rate N_2O=172 sccm, DES=12sccm, He=600 sccm, Plasma power 0.15W.cm^2, 100kHz

stretching may be attributed to the moisture trapped in the film or loosely bonded SiOH. The small absorption peak ("shoulder") at 880c m^{-1} was also due to this silanol bond. Unlike other work, no trend of the intensity of this 880 cm^{-1} peak associated with temperature variation was observed. The peak of 2270 cm^{-1} was characteristic of CO_2.

Due to the temperature effect in the range of temperature investigated, 300°C appears to be a best temperature for this system which not only yields good quality oxide deposit at a moderated growth rate, but also satisfies the low-temperature requirement of SiGe layer. Therefore, the system temperature was set up at the 300°C for the following experimental studies.

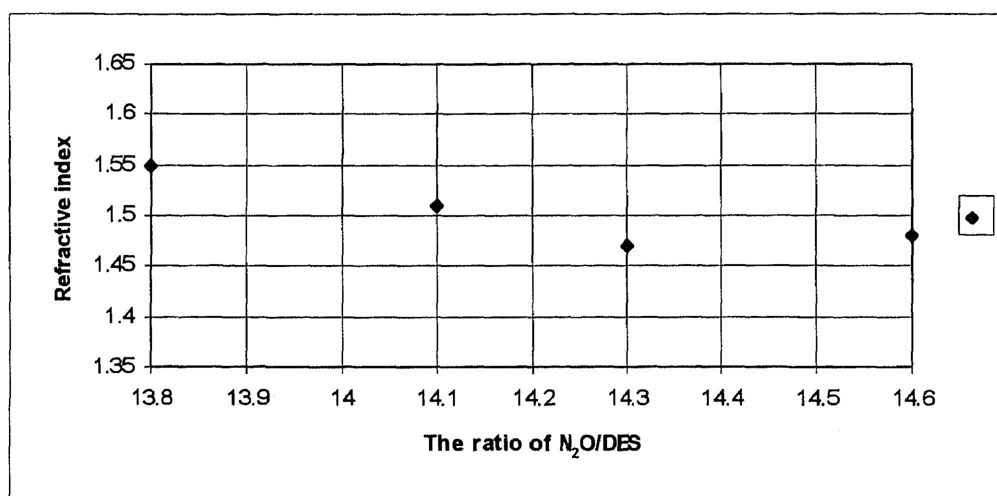


Figure 4.5 Refractive index versus the ratio of N_2O/DES (166/12 = 13.8, 169/12 = 14.1 172/12 = 14.3, 175/12 = 14.6). Deposition condition: 300°C, 0.3 Torr, He=600 sccm, Plasma power 0.15W/cm^2, 100kHz

4.1.3 Gas Composition Study

The gas composition study was done by L. Chen in the same deposition system. This study was very important for our experiment because it provided the basic information for us to choose the flow rate ratio of N_2O/DES.

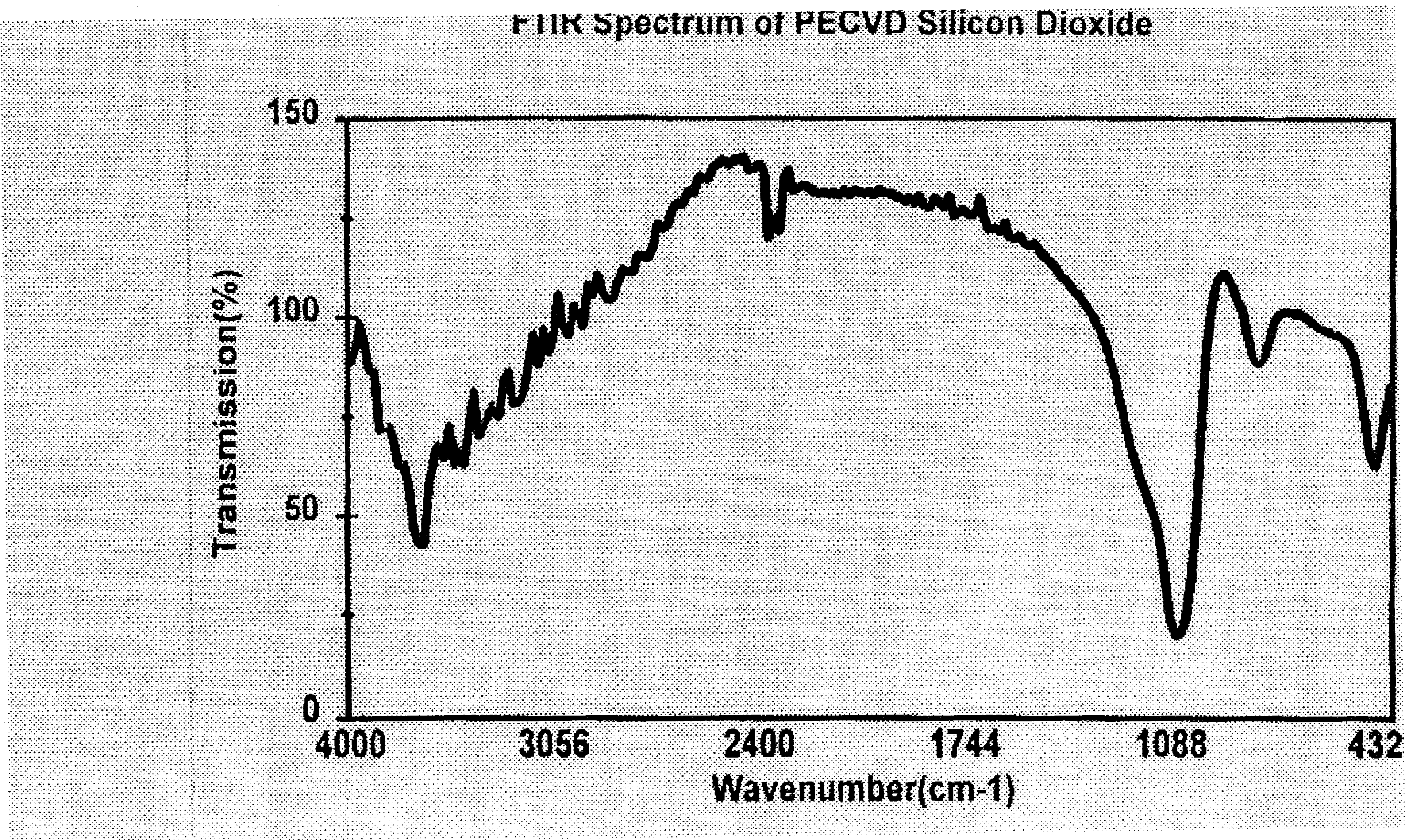


Figure 4.6 Typical FTIR Spectrum of PECVD Silicon Dioxide

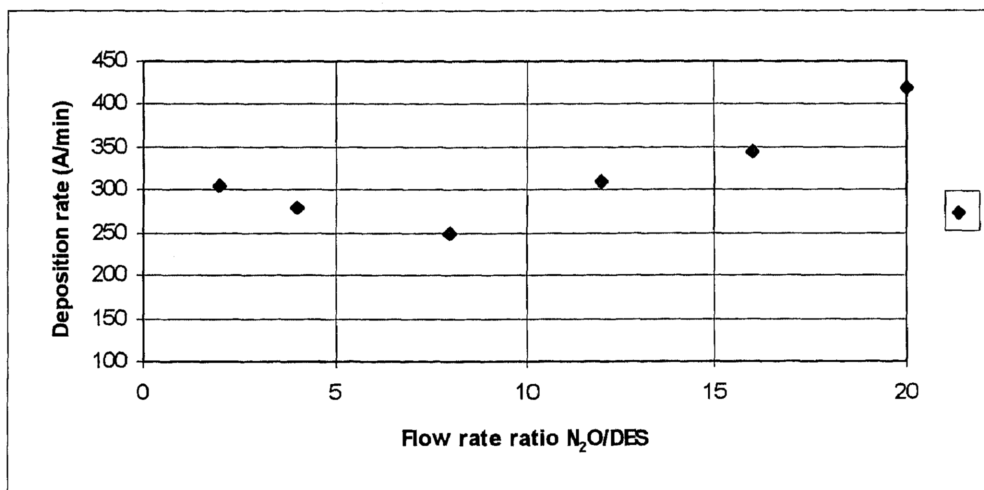


Figure 4.7 The deposition rate as a function of flow rate ratio N_2O/DES. Deposition condition: 300°C, 0.3 Torr, Plasma power 0.15W/cm^2, rf 100kHz

Figure 4.7 shows that the deposition rate increased with the increasing N_2O/DES ratio in the range 8 - 20, the DES flow rate is 15 sccm fixed and the N_2O flow rate changed. The total flow rate changed corresponding to that range is from 135 sccm to 315 sccm. The experimental result shows that when the N_2O/DES ratio were 2 - 4, total flow ratewere 45 - 95 sccm, the growth rate decreased as the flow rate ratio and total flow rate increased. While in the high ratio (>8), the deposition rate was large increase. The possible explanation for this phenomena may be that the flow rate was too low to remove the product gas molecules when it was lower than 135 sccm, thus films deposited under such conditions might trapped more gas molecules, showing high deposition rate. When the total flow rate as well as the N_2O flow rate became high enough, no further densification occurred. There might be two factors responsible for the significant increase in the deposition rate. 1) the increasing amount of the oxygen radical O* was available in the plasma, which dominated the plasma oxidation reaction and accelerated the deposition; 2)

the increasing reactant gases feed and increasing product removal favored the deposition reactions. L. Chen also investigated the other parameters affected by flow rate ratio such as film density, P-etch rate, mass variation, refractive index, Young's Modulus and film stress. Based on this series studies, N_2O/DES = 14 : 1 is an optimized flow rate ratio for good qualities such as refractive index (1.47) and film density (2.14 g/cm^2). The flow rate was set at N_2O flow rate = 172 sccm and DES flow rate = 12 sccm.

4.1.4 Uniformity of the Film

The use of high flow rate of helium helps us to get good uniform film and enable us to get relatively low deposition rate. In this part, we studied effect of the flow rate of helium to

Table 4.1 Uniformity of a 5" wafer versus the flow rate of helium

Flow rate of He (sccm)	Mean thickness of SiO_2 film d (Å)	Uniformity Δd (max-min) (Å)	Uniformity Δd/d (%)
None	1090	145	13
600	1078	85	8
750	1003	60	6
850	1032	55	5

the uniformity of a 5" wafer. The wafer is set at middle of radius. Table 4.1 shows the uniformity of the film in 5" wafer versus the flow rate of helium, which also compares the result with none-helium deposition. The results shows that the uniformity is indeed improved which is very important to the deposition of gate oxide because it is just 435Å. The flow rate of DES is 12 sccm and the flow rate of N_2O is 172 sccm. The power is 500W (0.15 W/cm^2).

4.1.5 The Deposition Rate

The most important factor in determining the electrical quality of the deposited material was found to be the rate of deposition. The more important variables which influence this are the total flow of reactive gases, chamber pressure, rf power and the reactive gas ratio. The ratio of N_2O/DES is also the primary factor in determining the stoichiometry of the film. In our experiment, the chamber pressure is set at 0.3 Torr according to Chen experimental results [62].The gas ratio can also not changed much because it will affect the stoichiometry of the film. Therefore, only two factors were studied here.

film. In our experiment, the chamber pressure is set at 0.3 Torr according to Chen experimental results [62].The gas ratio can also not changed much because it will affect the stoichiometry of the film. Therefore, only two factors were studied here.

Table 4.2 shows the effect of rf power to the deposition rate and also compared the deposition rate at same power but different flow rate of helium. The deposition rate decreases with the decreasing of the power. This is understandable since reducing the power would lower the concentration of the reactive species. Hence it reduced the

deposition rate. When the rf power is 250W (0.075W/cm^2), the system is unstable. There is no deposition on the surface of the wafer because the energy provided is not enough for reaction. But on the other hand, low power may reduce the defects caused by the plasma radiation which is very important to SiGe layer.

Table 4.2 The effect of rf power and the flow rate of helium to deposition rate

rf power (W)	Flow rate of He (sccm)	Deposition rate (Å/min)	Comment
500	600	195	
500	850	170	
300	850	125	
250	850	None	system unstable

4.1.6 Capacitor - Voltage Measurement

The electrical properties is measured here through high frequency (1MHz) capacitor-voltage method. The MOS capacitor was fabricated on 10 - 20 Ω-cm <100> silicon substrate. The deposition conditions are pressure 0.3 Torr, temperature 300°C, flow rate of DES 12 sccm, flow rate of N_2O 172 sccm, the flow rate of helium is 850 sccm. The rf powers are 500 W (0.15W/cm^2) and 300W (0.09 W/cm^2) for different samples. The radius of the circle capacitor dot is 300 μm and the area is 282600 μm^2. Aluminum contact dots were evaporated through a metal mask by thermal evaporation. Annealing temperature was 650°C for 30 minutes in the ambient of nitrogen.

The high frequency C-V measurement is carried out with HP4145B Semiconductor Parameter Analyzer. Through the high-frequency (1MHz) C - V measurement and the bias-temperature aging C -V measurement, the flat-band voltage (V_{fb}) and the change of flat-band voltage (ΔV_{fb}) due to the drift of mobile charges were measured, from which the interface density and the mobile charge density were deduced. Figure 4.8-4.11 give the C-V curves which measurement was taken at the room temperature. The applied gate bias voltage swept from inversion region to accumulation region for the safty of thermal equilibrium. The sample deposition conditions are the flow rate of DES 12 sccm, the flow rate of N_2O and the flow rate of He 850 sccm at the different power of 500W and 300W respectively. Figure 4.8 - 4.9 give the C-V curves of non-annealing samples. From that we can see the flat band voltages are too negative. Several reasons can cause this phenomenon. First, donor-type interface trap, which is filled with electrons. If interface trap density is too large, even at gate voltage $V_G = 0$ the surface layer is already depletion or inversion. Hence this makes the flat band voltage is too negative. Second, positive oxide charge density located near the surface of $Si\text{-}SiO_2$ is too large, which may be caused by plasma radiation-induced during the deposition

Figure 4.10 - 4.11 give the annealing sample C-V curve measured at the room temperature. The applied gate voltage swept from inversion region to accumulation region. The annealing is carried out at the temperature of 650°C in the ambient of N_2 which flow rate is 50sccm. For both C-V curves, annealing at temperature 650°C, the flat-band voltage decreased obviously. This might be that the interface trap density and oxide charge density can be reduced by annealing[63]. As we discussed above from the FTIR

spectroscopy, the PECVD SiO_2 film has higher OH content, which causes the stress to be compressive and cause large amount of interface trap charges. After annealing, the OH content is decreased and interface trap charge is also decreased[64].

Figure 4.8 - 4.11 show a common phenomenon that at the edge of the depletion region the C-V curve increases and then almost do not change with the voltage. This phenomenon might be the reason of the measurement frequency 1 MHz is not high enough and the generation-recombination rates in the surface depletion region are fast enough, then the minority carriers (electron) concentration can follow the ac gate signal and lead to charge exchange with the inversion layer in step with the measurement signal. Or the second reason might be that there are large amount of fast interface state at the surface of the Si, they can exchange the electrons with the inversion layer.

Figure 4.9 C-V curve which is a non-annealing sample deposited at the power of 500W showed more negative flatband voltage(-27) than C-V curve showed in figure 4.10 which is a non-annealing sample deposited at the power of 300W. It means that the sample deposited at the power of 300W had less interface trap density and fixed oxide charge because of less radiative damage.

Figure 4.12 - 4.15 give the bias-temerature(B-T) aging C-V curves. The procedures of B-T measurement for obtain a positive C-V curve(f_+)are 1) apply a positive bias gate voltage +10V and heat the substrate to the temperature of 150°C, 2) wait for 30 minutes, 3) cool down the substrate to room temperature, 4) take C-V measurement at the room temperature. The procedures of B-T measurement for obtain a negative C-V curve(f_-)are 1) apply a negative bias gate voltage -10V and heat the substrate to the temperature of

150°C, 2) wait for 30 minutes, 3) cool down the substrate to room temperature, 4) take C-V measurement at the room temperature. This method is used to measure the mobile charges in oxide layer. When a positive bias was applied to the MOS capacitor, the positive oxide mobile charges such as positive sodium ion was repelled to the interface of Si-SiO_2 which will make the flatband voltage shifts to the direction of negative. The curve labeled (f_+) was obtained. Repeating the B-T aging with negative voltage, the mobile charges was attracted to the surface of metal- SiO_2 surface, then the flatband voltage increases. Then the curve labeled (f_-) was obtained. The difference of the flatband voltage of the (f_+) and (f_-) C-V curve was used to calculate the mobile charge density.

Table 4.3 Experimental results of C - V measurement for PECVD

Power (W)	SiO_2 thickness (Å)	Annealing Temp. (°C)	V_{fb} (V)	ΔV_{fb} (V)	N_t* ($1/cm^2$)	N_m** ($1/cm^2$)
500	1050	none	-27	16	5.4×10^{12}	3.3×10^{12}
500	1050	650	-4	22	6.2×10^{11}	4.5×10^{12}
300	1160	none	-16	19	2.8×10^{12}	3.6×10^{12}
300	1160	650	-4.5	21	6.6×10^{11}	3.9×10^{12}

* N_t is the total effect of interface trap density N_{ss} and oxide charge density N_f.

Table 4.3 shows the experiment and calculation results for corresponding samples. The results of C-V measurement show that both interface state density and mobile charge density are greater than the requirement of MOSFET device which is generally at the order of 10^9-10^{10} cm-^{2}. The total effect of interface trap density and oxide charge density

is reduced by one decade by the post-deposition annealing but it is still much higher. The higher interface trap density maybe caused by surface damage, tensile stress, and surface contamination, which can change with the gate bias signal. Hence the device is unstable. The breakdown voltage of oxide film is about 4 - 5 MV / cm. For the high deposition rate oxide (330 Å/min) without helium, the depletion region of the C - V curve increased gradually. That means large leakage current (10^{-8}) and gradual charging of the oxide occurred before its break-down voltage, which may be caused by large amount of pinholes and gross defects. This would be a long-term stability problem. The C-V curve of low deposition rate oxide showed much better electrical characteristics. Considering the experimental results discussed above, high-quality silicon dioxide has been deposited at low substrate temperature by PECVD. The film properties were found to depend on the deposition rate. In our experiment, the deposition rate can be lowered less than 170 Å/min (power = 0.15 W/cm^2) and 125 Å/min (power = 0.15 W/cm^2) with the help of helium. According to J.Batey and E. Tierney[65], the high-quality silicon dioxide was achieved at the deposition rate 60 - 80 Å/min. But we can not reduce the deposition rate further in our PECVD system because 1) the flow rate of helium can not be increased more than 900 sccm; 2) power can not be reduces further. Also after B-T measurement(figure 4.12-4.15) the leakage current increased from 10^{-9} to 10^{-7} A. The C-V curve changed more gradually. This may be caused by large leakage current which means the pin-hole density increase after aging.

Figure 4.16 - 4.19 show the quasi static C-V curve of PECVD SiO_2 for non-annealing and 650°C annealing situation. The quasi static measurement was carried out at the room

temperature with HP 4140B PA Meter/DC Voltage Source. The sweeping ramp voltage is from negative to positive (from inversion to accumulation) because it is easy to produce non-equilibrium effect if sweep from accumulation to inversion). The sweep rate was 100mV/sec. The common phenomenon is that the C-V curve is skewed at different degree. The reason leads to the skewed C-V curve is caused by leakage current due to the leaky oxide. The leakage current is much greater than displacement current. This means that there are large amount of pin-hole in the oxide film. The second common phenomenon observed from the C-V curve is that there is a deviation in the weak inversion region. This kink point may be due to the following reason: 1) interface trap response, when the gate voltage increases, the energy band begins to bend toward the valence band. As the quasi-Fermi level passes through midgap at the silicon surface, the interface traps begin to emit the electrons to conduction band. The interface traps become positive and produce a electrical field due to the lack of electrons, which offsets part of the increased gate voltage and makes the flat band voltage shift toward right. Hence it produces the distortion of the C-V curve. 2) deep energy level, which may be the capture center of electrons produced by the heavy-metal impurities. The deep energy levelcapture centers begin to emit the electrons at the certain gate voltage which make the quasi-Fermi level pass through the deep energy level. In PECVD process, it may be happened due to heavy metal impurities, this may be come from the chamber. Because this instrument was also used as dry etching of alloy and other kind of material. So the cross contamination may happen. From the figure 4.17, there is a deviation in the depletion region. this may be also caused by the deep energy level.

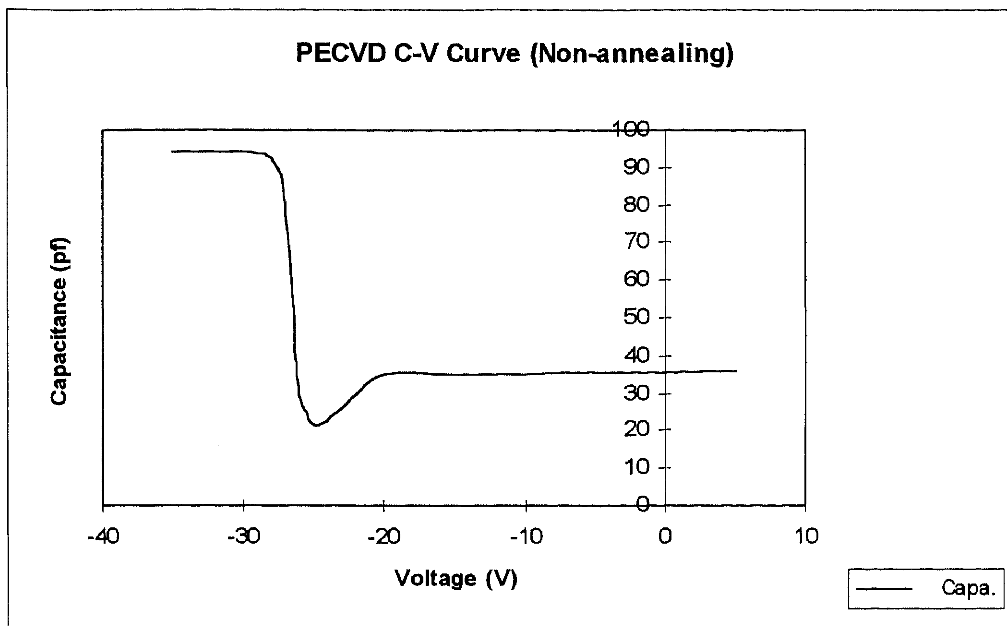


Figure 4.8 PECVD SiO_2 C-V curve. d_{ox} = 1050 Å, Non-annealing, $C_{ox} = 3.3\times10^{-8}$ F/cm^2, C_{ox} (total) =94pf, C_{fb} = 2.94×10^{-8}F/cm^2, C_{fb} (total)=83.7pf, $V_{fb}(C=C_{fb})$ = -27V, Power=500W, DES=12sccm, N_2O=172sccm, He=850sccm, deposition temp=300°C

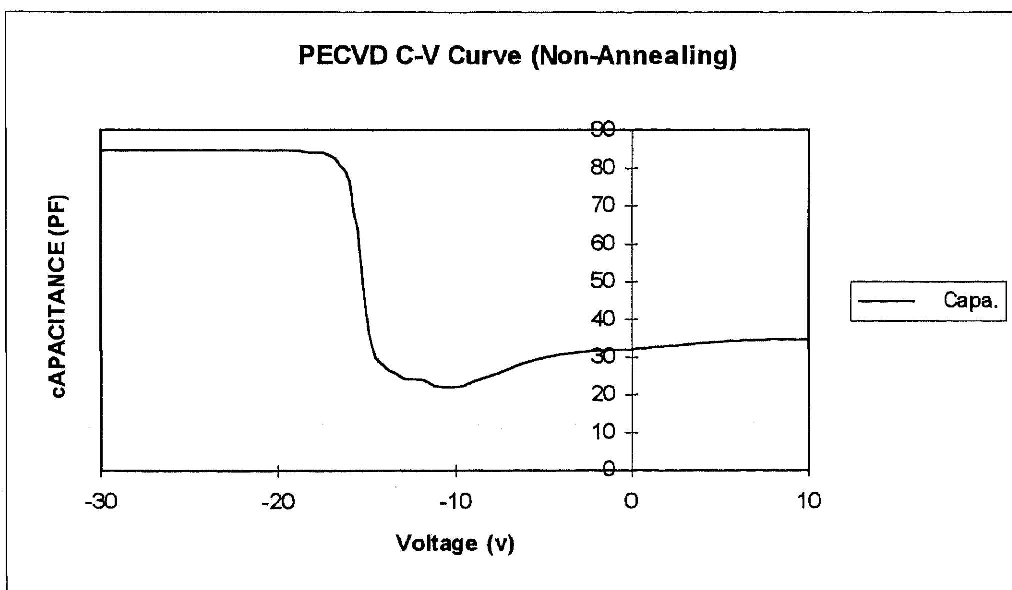


Figure 4.9 PECVD SiO_2 C-V curve. d_{ox} = 1160 Å, Non-annealing, $C_{ox} = 3.0\times10^{-8}$ F/cm^2, C_{ox} (total) =85pf, C_{fb} = 2.72×10^{-8}F/cm^2, C_{fb} (total)=76.5pf, $V_{fb}(C=C_{fb})$ = -16V, Power=300W, DES=12sccm, N_2O=172sccm, He=850sccm, deposition temp=300°C

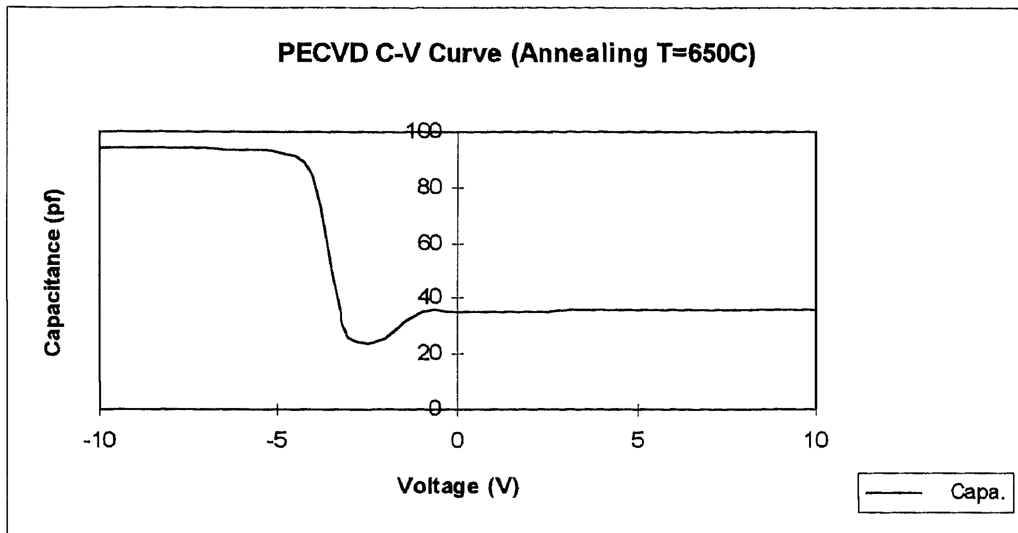


Figure 4.10 PECVD SiO_2 C-V curve. d_{ox} = 1050 Å, Annealing temp=650°C, C_{ox} = 3.3×10^{-8}F/cm², C_{ox} (total) =94pf, C_{fb} = 2.94×10^{-8}F/cm², C_{fb} (total)=83.7pf, $V_{fb}(C=C_{fb})$ = -4V, Power=500W, DES=12sccm, N_2O=172sccm, He=850sccm, deposition temp=300°C

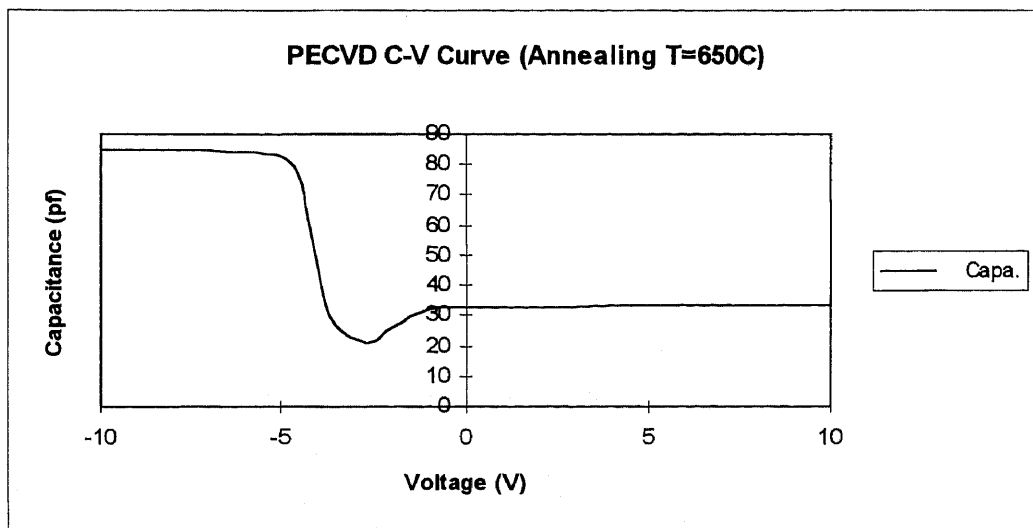


Figure 4.11 PECVD SiO_2 C-V curve. d_{ox} = 1160 Å, Annealing temp=650°C, C_{ox} = 3.0×10^{-8}F/cm², C_{ox} (total) =85pf, C_{fb} = 2.72×10^{-8}F/cm², C_{fb} (total)=76.5pf, $V_{fb}(C=C_{fb})$ = -4.5V, Power=300W, DES=12sccm, N_2O=172sccm, He=850sccm, deposition temp=300°C

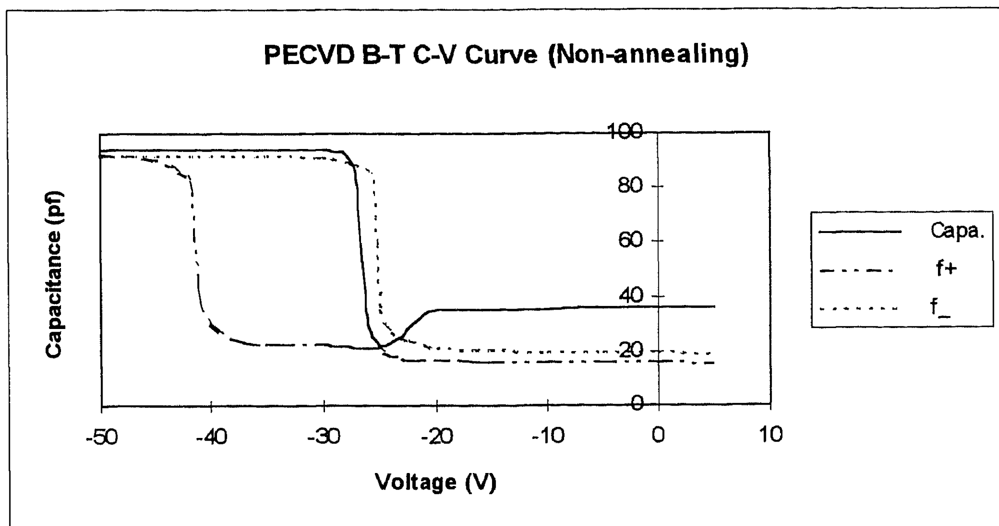


Figure 4.12 PECVD SiO_2 Bias-temperature C-V curve. d_{ox} = 1050 Å, C_{ox} = 3.3×10^{-8}F/cm^2, C_{ox} (total) =94pf, C_{fb} = 2.94×10^{-8}F/cm^2, C_{fb} (total)=83.7pf, V_{fb}(C=C_{fb}) = -4V, Power=500W, DES=12sccm, N_2O=172sccm, He=850sccm, deposition temp=300°C, T(B-T)=150°C, V_{Bias}(f+)=+10V for t=30min, V_{Bias}(f-)=-10V for t=30min,

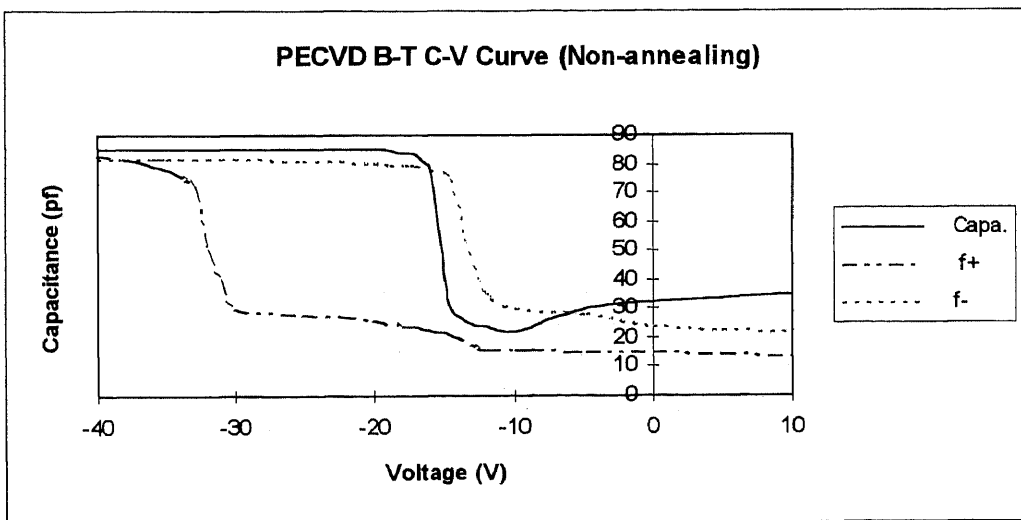


Figure 4.13 PECVD SiO_2 Bias-temperature C-V curve. d_{ox} = 1160 Å, C_{ox} = 3.0×10^{-8}F/cm^2, C_{ox} (total) =85pf, C_{fb} = 2.72×10^{-8}F/cm^2, C_{fb} (total)=76.5pf, V_{fb}(C=C_{fb}) = -4.5V, Power=300W, DES=12sccm, N_2O=172sccm, He=850sccm, deposition temp=300°C T(B-T)=150°C, V_{Bias}(f+)=+10V for t=30min, V_{Bias}(f-)=-10V for t=30min,

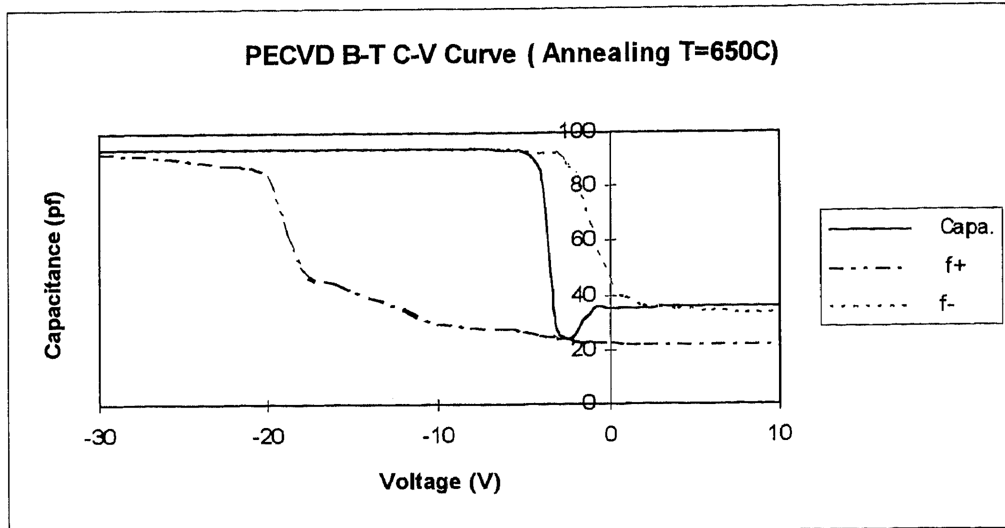


Figure 4.14 PECVD SiO_2 Bias-temperature C-V curve. d_{ox} = 1050 Å, Annealing temp=650°C, C_{ox} = 3.3×10^{-8}F/cm^2, C_{ox} (total) =94pf, C_{fb} = 2.94×10^{-8}F/cm^2, C_{fb} (total)=83.7pf, $V_{fb}(C=C_{fb})$ = -4V, Power=500W, DES=12sccm, N_2O=172sccm, He=850sccm, deposition temp=300°C, T(B-T)=150°C, V_{Bias}(f+)=+10V for t=30min, V_{Bias}(f-)=-10V for t=30min,

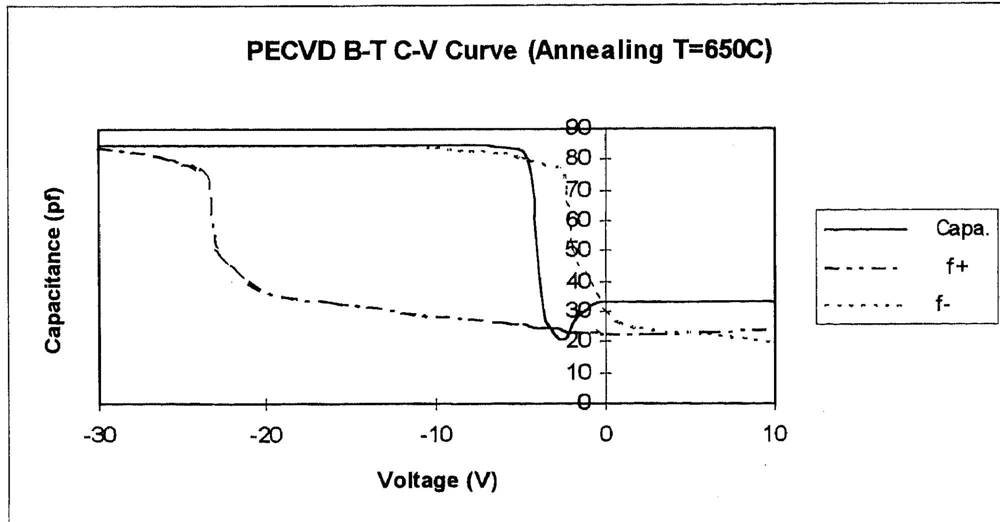


Figure 4.15 PECVD SiO_2 Bias-temperature C-V curve. d_{ox} = 1160 Å, Annealing temp=650°C, C_{ox} = 3.0×10^{-8}F/cm^2, C_{ox} (total) =85pf, C_{fb} = 2.72×10^{-8}F/cm^2, C_{fb} (total)=76.5pf, $V_{fb}(C=C_{fb})$ = -4.5V, Power=300W, DES=12sccm, N_2O=172sccm, He=850sccm, deposition temp=300°C, T(B-T)=150°C, V_{Bias}(f+)=+10V for t=30min, V_{Bias}(f-)=-10V for t=30min,

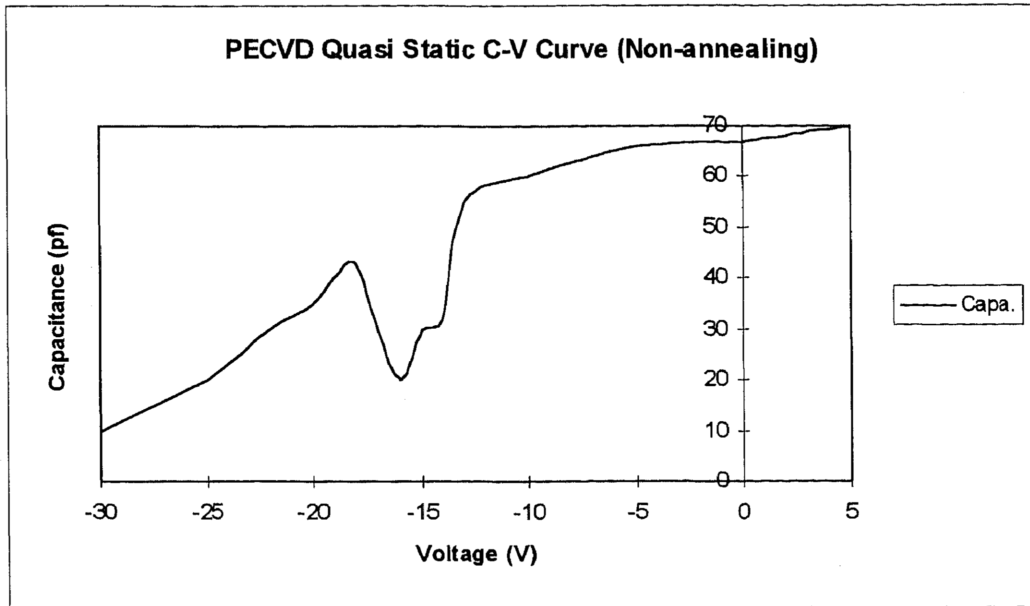


Figure 4.16 PECVD SiO_2 Quasi Static C-V curve. d_{ox} = 1050 Å, Non-annealing, C_{ox} = 3.3×10^{-8} F/cm^2, C_{ox} (total) =94pf, $C_{fb} = 2.94\times10^{-8}$F/cm^2, C_{fb} (total)=83.7pf,Power=500W, DES=12sccm, N_2O=172sccm, He=850sccm, deposition temp=300°C

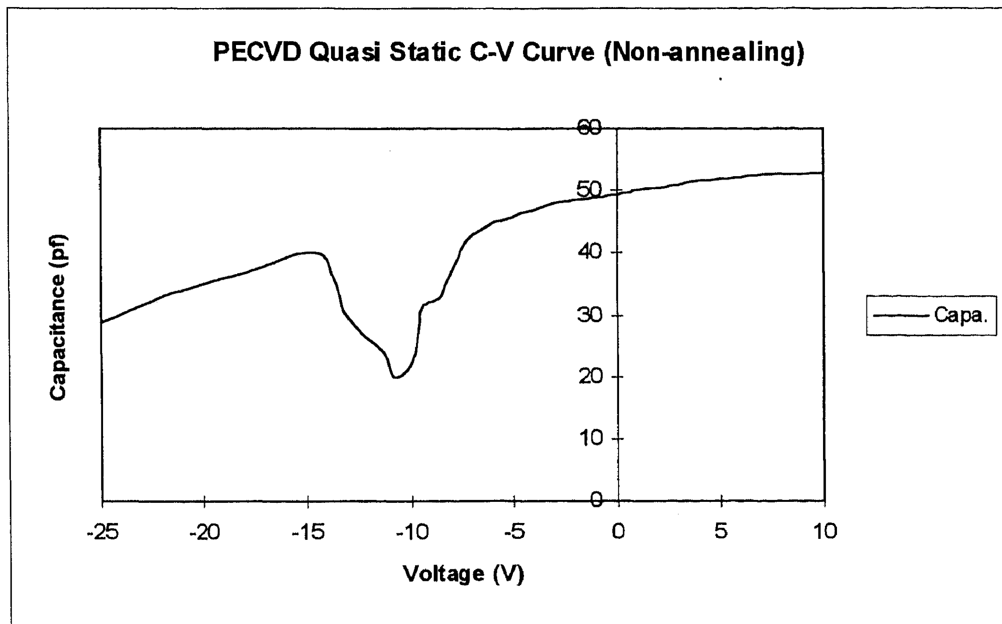


Figure 4.17 PECVD SiO_2 Quasi Static C-V curve. d_{ox} = 1160 Å, Non-annealing, C_{ox} = 3.0×10^{-8} F/cm^2, C_{ox} (total) =85pf, $C_{fb} = 2.72\times10^{-8}$F/cm^2, C_{fb} (total)=76.5pf, Power=300W, DES=12sccm, N_2O=172sccm, He=850sccm, deposition temp=300°C

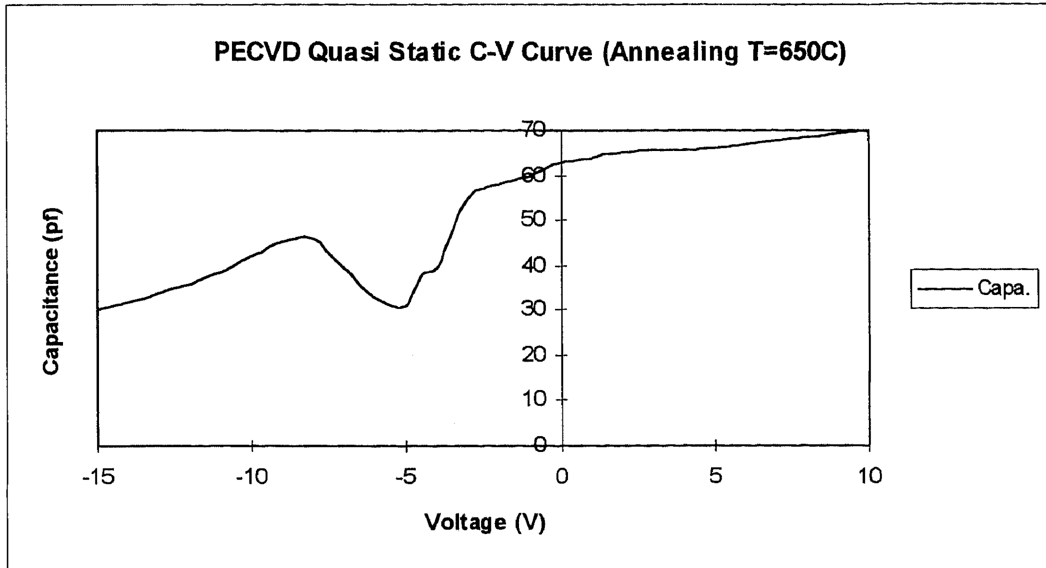


Figure 4.18 PECVD SiO_2 C-V curve. d_{ox} = 1050 Å, Annealing temp=650°C, C_{ox} = 3.3×10^{-8}F/cm^2, C_{ox} (total) =94pf, C_{fb} = 2.94×10^{-8}F/cm^2, C_{fb} (total)=83.7pf, $V_{fb}(C=C_{fb})$ = -4V, Power=500W, DES=12sccm, N_2O=172sccm, He=850sccm, deposition temp=300°C

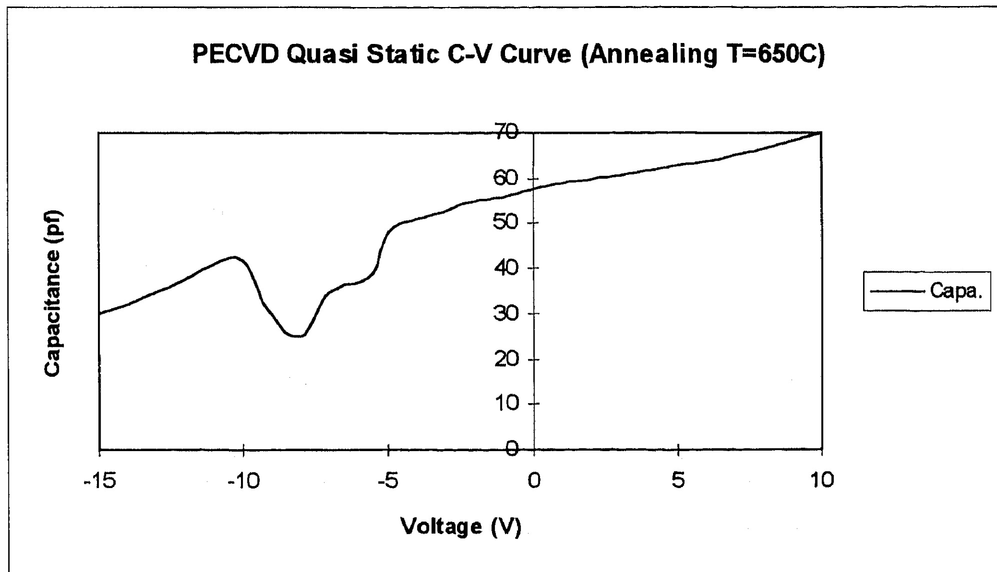


Figure 4.19 PECVD SiO_2 C-V curve. d_{ox} = 1160Å, Annealing temp=650°C, C_{ox} = 3.0×10^{-8}F/cm^2, C_{ox} (total) =85pf, C_{fb} = 2.72×10^{-8}F/cm^2, C_{fb} (total)=76.5pf, $V_{fb}(C=C_{fb})$ = -4.5V, Power=300W, DES=12sccm, N_2O=172sccm, He=850sccm, deposition temp=300°C

4.2 LPCVD SiO_2

The LPCVD low temperature silicon dioxide films were deposited in BTU computer controlled LPCVD system in NJIT cleanroom. This system is for production and research and the deposition condition is quite mature. So the purposes of this experiment are 1) measure the deposition rate and uniformity at the different depositing position; 2) measure the electrical properties of the oxide films; 3) compare it with PECVD silicon dioxide.

The starting material is 10 - 20 Ω-cm <100> p-substrate silicon wafers. Figure 2.11 shows the reaction furnace. There are two ways to put the wafer inside the furnace: 1) vertical position; 2) horizontal position. Table 4.4 gives the three runs average deposition rate and uniformity. The deposition conditions are flow rate of SiH_4 300 sccm, O_2 75 sccm, temperature 425°C and pressure 500 mTorr. Obviously the horizontal deposition position is not a good choice. The deposition rate is too high and the film uniformity is low. This would make the film structure loose. The vertical deposition position has lower deposition rate and better uniformity, which, therefore, is adopted as usual deposition position for production and research.

Table 4.4 Deposition rate and uniformity of LPCVD SiO_2

Position	Average deposition rate (Å/min)	Average uniformity (Max-Min)/Mean (%)
vertical	14.5	8
horizontal	140	17

Figure 4.20-4.21 give the C-V curves of the LPCVD SiO_2 non-annealing samples for room-temperature C-V. From Fig. 4.20, there is also deep curve at the edge of depletion region. But the C-V curve of Fig 4.21 do not have that. Comparing these curve with non-annealing PECVD C-V curve, they are much better. The flatband voltage is also less negative comparing with non-annealing PECVD samples. After annealing which is carried out at the temperature of 650°C in the N_2 ambient, the C-V which is given by Figure 4.22 - 4.23 showed better C-V curves. The flatband voltage was around -2V. Frome these curves, the results showed that the interface traps on the interface of Si-SiO_2 of LPCVD samples is less and have less effect. Hence the interface of Si-SiO_2 of LPCVD samples was obviously improved. This result can also be seen in the quasi static C-V curves afterwards.

Figure 4.24 - 4.27 give the bias-temperature aging C-V curves. Bias-temperature aging C-V curves. The system and measurement condition and methods are the same as the measurement of PECVD samples which was discussed in 4.1.6. Table 4.5 gives the C-V measurement and calculation results which were obtained by high frequency (1MHz) capacitor-voltage method. The MOS capacitor use LPCVD SiO_2 as gate oxide. The radius of the circle capacitor dot is 300 μm and the area is 282600 μm^2. Aluminum contact dots were evaporated through a metal mask by thermal evaporation. Annealing temperature was 650°C for 30 minutes in the ambient of nitrogen.

Through the high-frequency (1MHz) C - V measurement and the bias-temperature aging C -V measurement, the flat-band voltage (V_{fb}) and the change of flat-band voltage

(ΔV_{fb}) due to the drift of mobile charges were obtained, also from which the interface density and fixed charge density and the mobile charge density were deduced.

The experiment results showed that the interface trap density, fixed charge density and the mobile charge density of LPCVD SiO_2 has the same order of PECVD SiO_2 but it is less than corresponding PECVD samples. The break-down voltage of LPCVD oxide film is about 5 - 6 MV/cm. The post-LTO annealing can reduce the interface trap density about a decade. The refractive index of LPCVD SiO_2 is quite stable for each run which is about 1.45 - 1.46. But the high etch rate (3300Å/min) comparing with thermal oxide (1000Å/min) means that LPCVD SiO_2 has loose structure. The leakage current during C-V measurement is about 10^{-9} A.

Although Figure 4.20 - 4.21 showed that for the non-annealing samples C-V curve has less negative flatband voltage comparing with the corresponding PECVD samples, the flatband voltage was still too negative for the MOS device. This can be explained as follows: 1) donor-type interface trap. If interface trap density is very large, it can makes

Table 4.5 Experimental results of C - V measurement for LPCVD

SiO_2 thickness (Å)	Annealing Temp. (°C)	V_{fb} (V)	ΔV_{fb} (V)	N_t* ($1/cm^2$)	N_m** ($1/cm^2$)
392	none	-8	11	3.9×10^{12}	6.1×10^{12}
510	none	-13	16	5.1×10^{12}	6.8×10^{12}
406	650	-2.2	7	6.4×10^{11}	3.7×10^{12}
440	650	-2	12	4.9×10^{11}	5.8×10^{12}

* N_t is the total effect of interface state density N_{ss} and oxide fixed charge N_f.

** N_m is the oxide mobile charge.

the flat band voltage is too negative compared with the ideal situation. 2) positive oxide charge density located near the surface of $Si-SiO_2$ is large. Hence it need to be improved. For both C-V curves, annealing at temperature 650°C in the ambient of nitrogen, the flat-band voltage increased obviously (Figure 4.10-4.11), which is much better than corresponding PECVD C-V curves. This might be that the interface trap density and oxide charge density can be reduced by annealing[63]. Traps in LPCVD grown oxide are also linked to OH incorporation in the film. After annealing, the OH content is decreased and interface trap charge is also decreased[64]. The total effect of interface trap density and oxide charge density is reduced by one decade by the post-deposition annealing. More explanation can be referred in the section 4.16. Therefore, post-LTO annealing is very helpful for improving the interface quality of $Si-SiO_2$.

Figure 4.28 - 4.31 give the LPCVD quasi static C-V curve which used the same system and method as the measurement of PECVD samples introduced above. From the quasi static C-V curves for non-annealing C-V curves, we can see the deviation still exists in the weak reversion region for the samples of non-annealing LPCVD SiO_2. This may be caused by the interface traps. For LPCVD oxide, the deviation may not be caused by heavy metal impurities because all processes were completed in the cleanroom. The skewed C-V curves is attributed to the leakage current which is a common disadvantage for LPCVD and PECVD oxide. This means both oxide structure is loose and both films have lot of pinholes which deteriorate the quality of the films. The fast etching rate can also explain the loose structure of the PECVD and LPCVD films.

Figure 4.28 - 4.29 show the quasi static C-V curve for samples which were annealed at the temperature of 650°C in the ambient of nitrogen.. There is no obvious kink point in the curve of Figure 4.30 and no kink point in figure 4.31. This means that after the interface of Si-SiO_2 was largely improved by annealing, which was much better than the corresponding PECVD samples. Therefore, post-annealing is indeed providing a method to improve the quality of LPCVD and PECVD SiO_2.

Comparing both PECVD oxide film and LPCVD oxide film in our experiments, we choose LPCVD oxide film as gate oxide to fabricate the MOS device. Because from the above analysis, the quality of LPCVD oxide film is better than the PECVD oxide film. The second reason is LPCVD system is in the cleanroom that can avoid cross contamination which is important to device characteristics. The third is LPCVD system is quite stable. A lot of work has to done to improve the quality of PECVD oxide film in our experiment.

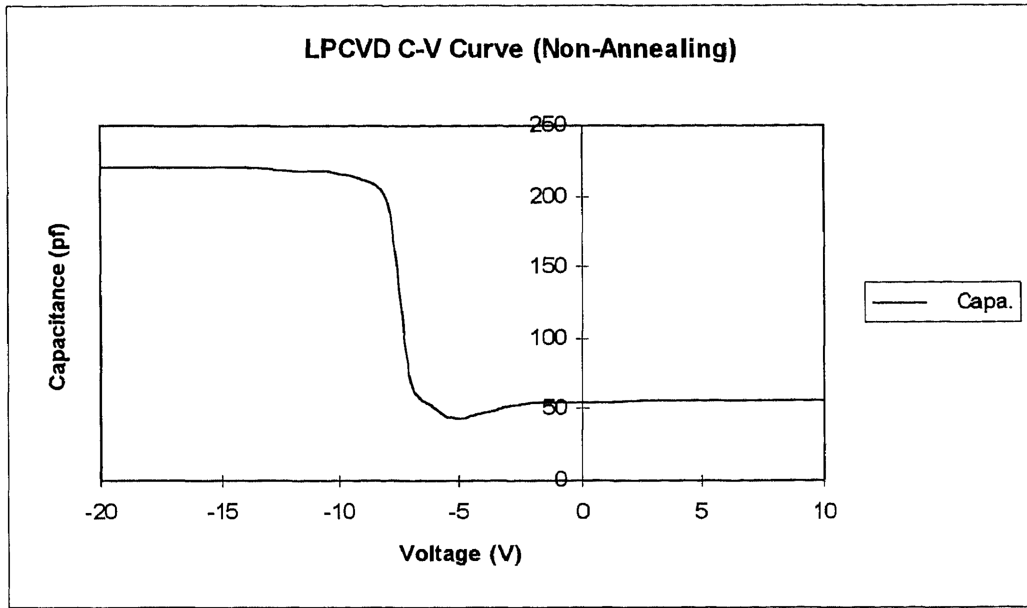


Figure 4.20 LPCVD SiO_2 C-V curve. d_{ox} = 392 Å, non-annealing, $C_{ox} = 8.8\times10^{-8}$F/cm^2, C_{ox} (total) =248pf, C_{fb} = 7.9×10^{-8}F/cm^2, C_{fb} (total)=220pf, $V_{fb}(C=C_{fb})$ = -8V, SiH_4=300sccm, O_2=75sccm, deposition temp.=425°C

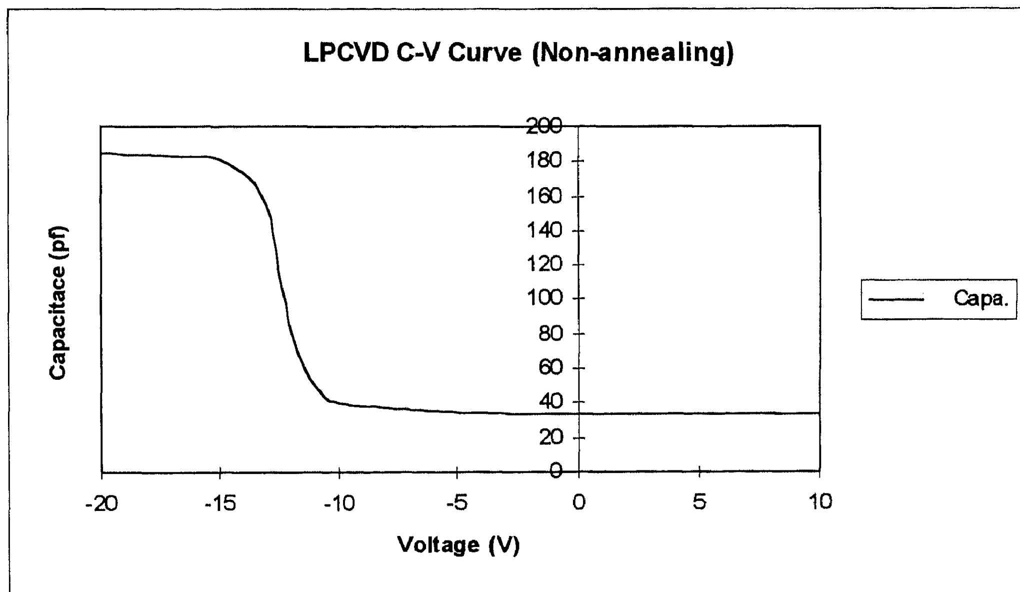


Figure 4.21 LPCVD SiO_2 C-V curve. d_{ox} = 510 Å, non-annealing, $C_{ox} = 6.77\times10^{-8}$F/cm^2, C_{ox} (total) =188pf, C_{fb} = 6.22×10^{-8}F/cm^2, C_{fb} (total)=173pf, $V_{fb}(C=C_{fb})$ = -13V, SiH_4=300sccm, O_2=75sccm, deposition temp.=425°C

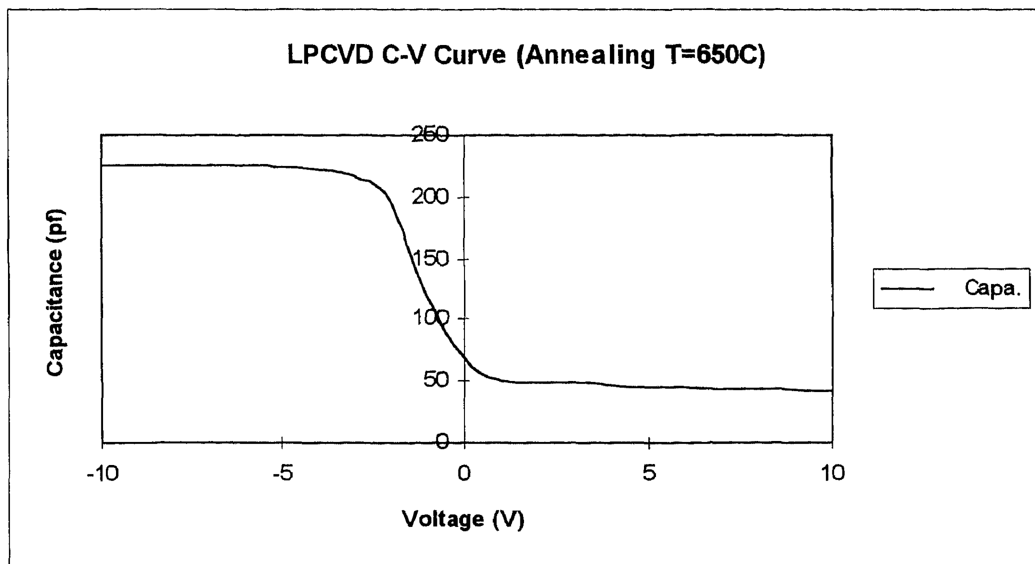


Figure 4.22 LPCVD SiO_2 C-V curve. d_{ox} = 406 Å, Annealing Temp = 650°C, C_{ox} = 8.5×10^{-8}F/cm^2, C_{ox} (total) =240pf, C_{fb} =7.7×10^{-8}F/cm^2, C_{fb} (total)=218pf, $V_{fb}(C=C_{fb})$ = -2.2V, SiH_4=300sccm, O_2=75sccm, deposition temp.=425°C

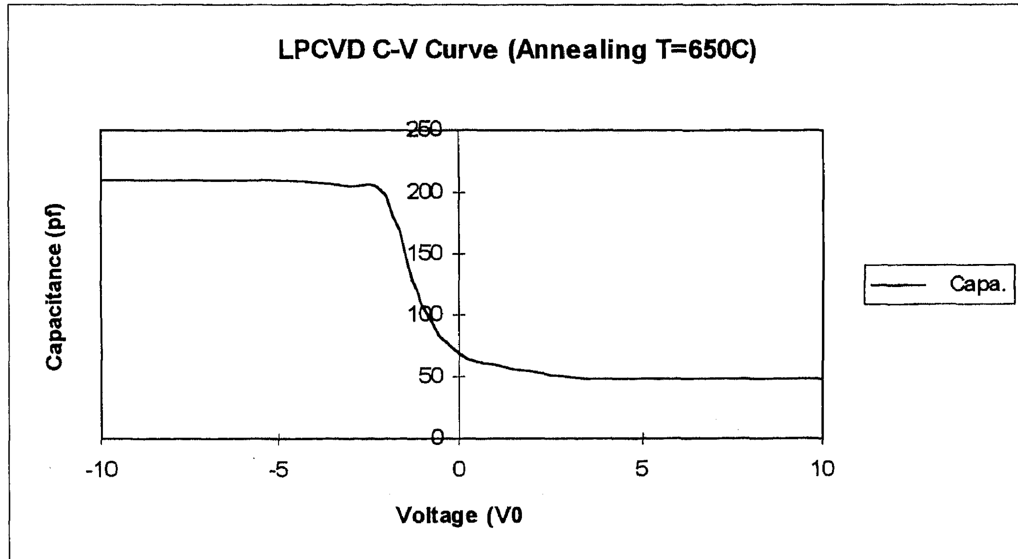


Figure 4.23 LPCVD SiO_2 C-V curve. d_{ox} = 440 Å, Annealing Temp = 650°C, C_{ox} = 7.8×10^{-8}F/cm^2, C_{ox} (total) =220pf, C_{fb} = 7.2×10^{-8}F/cm^2, C_{fb} (total)=204pf, $V_{fb}(C=C_{fb})$ = -2V, SiH_4=300sccm, O_2=75sccm, deposition temp.=425°C

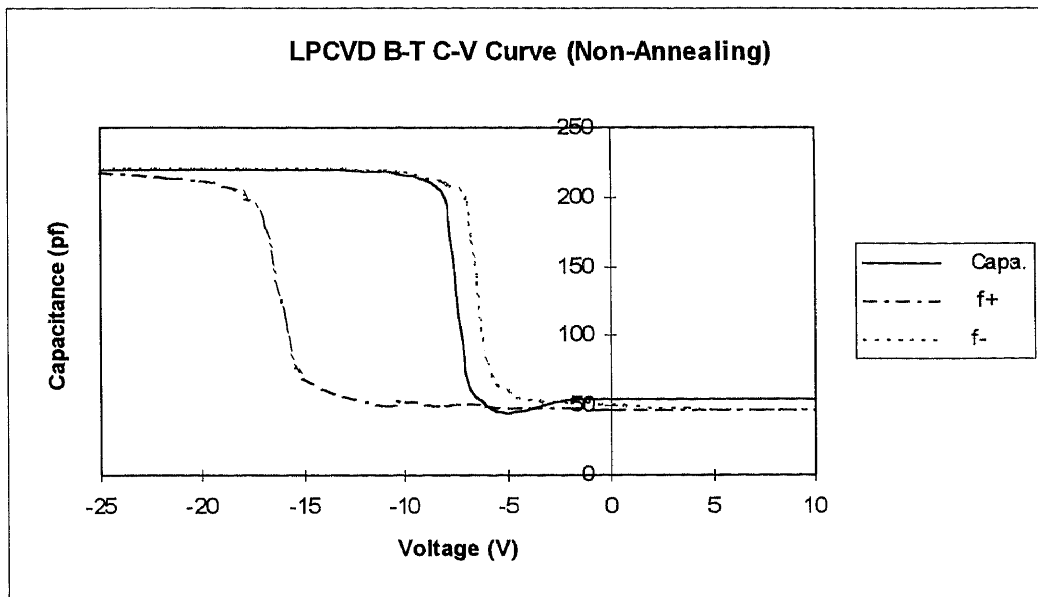


Figure 4.24 LPCVD SiO_2 Bias-Temperature C-V curve. d_{ox} = 392 Å, non-annealing, C_{ox} = 8.8×10^{-8}F/cm^2, C_{ox} (total) =248pf, C_{fb} = 7.9×10^{-8}F/cm^2, C_{fb} (total)=220pf, $V_{fb}(C=C_{fb})$ = -8V, Temp(B-T)=150°C, V_{Bias}(f+) = + 10V, V_{Bias}(f-) = - 10V, time = 30 minuts, SiH_4=300sccm, O_2=75sccm, deposition temp.=425°C

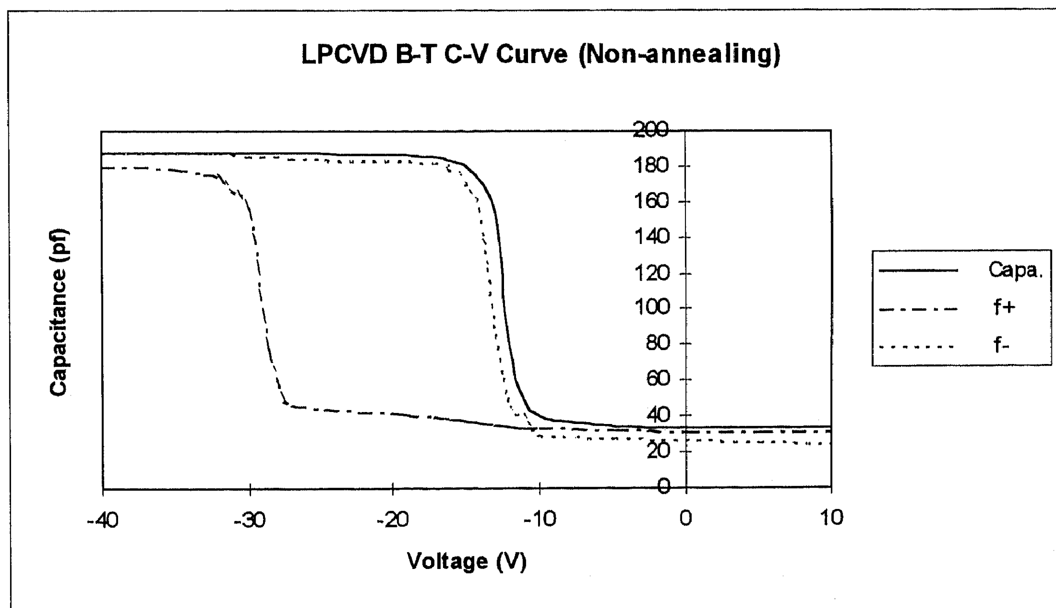


Figure 4.25 LPCVD SiO_2 Bias-Temperature C-V curve. d_{ox} = 510 Å, non-annealing, C_{ox} = 6.77×10^{-8}F/cm^2, C_{ox} (total) =188pf, C_{fb} = 6.22×10^{-8}F/cm^2, C_{fb} (total)=173pf, $V_{fb}(C=C_{fb})$ = -13V, Temp(B-T)=150°C, V_{Bias}(f+) = + 10V, V_{Bias}(f-) = - 10V, time = 30 minuts, SiH_4=300sccm, O_2=75sccm, deposition temp.=425°C

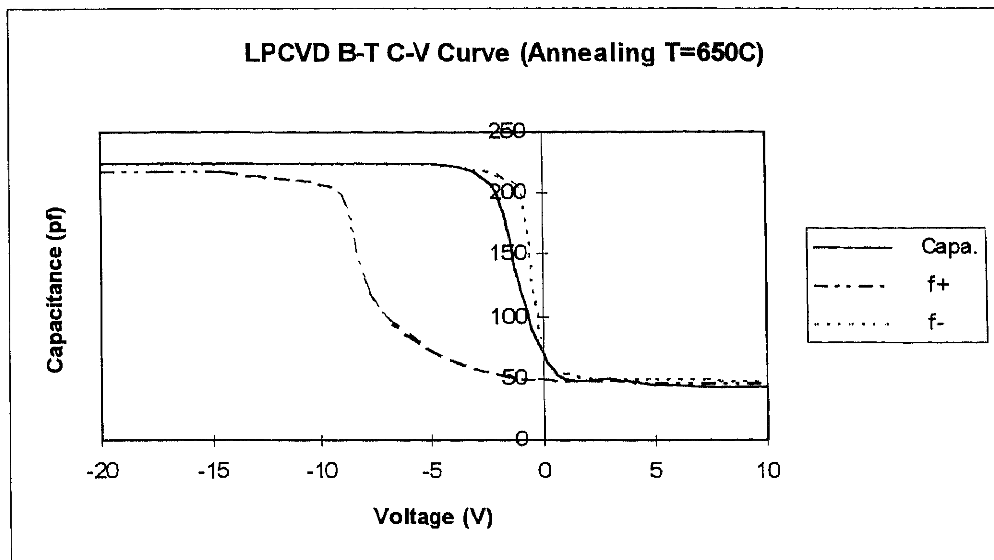


Figure 4.26 LPCVD SiO_2 Bias-Temperature C-V curve. d_{ox} = 406 Å, Annealing Temp = 650°C, C_{ox} = 8.5×10^{-8}F/cm^2, C_{ox} (total) =240pf, C_{fb} =7.7×10^{-8}F/cm^2, C_{fb} (total)=218pf, $V_{fb}(C=C_{fb})$ = -2.2V, Temp(B-T)=150°C, V_{Bias}(f+) = + 10V, V_{Bias}(f-) = - 10V, time = 30 minuts ,SiH_4=300sccm, O_2=75sccm, deposition temp.=425°C

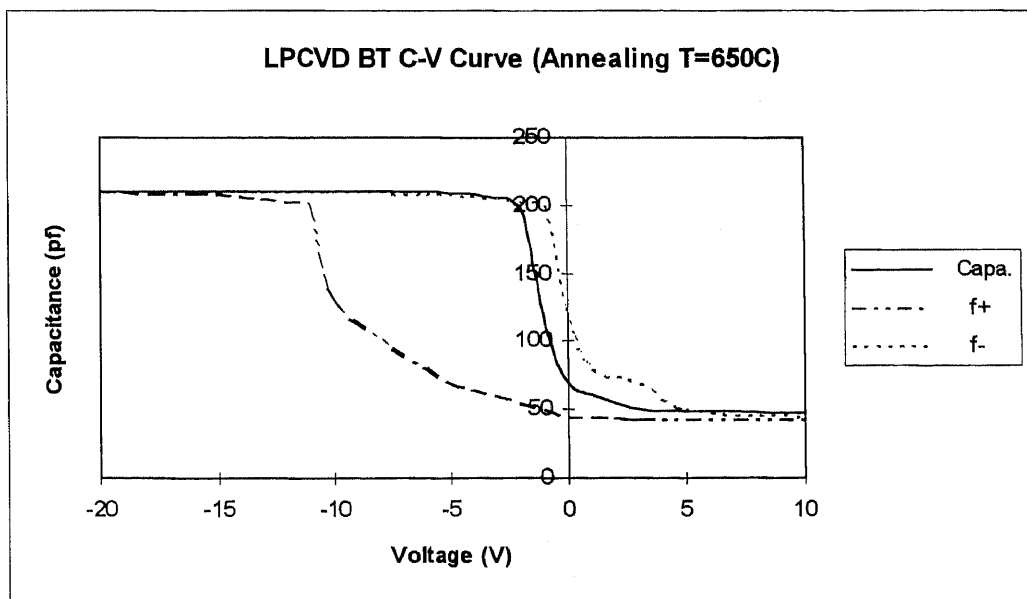


Figure 4.27 LPCVD SiO_2 Bias-Temperature C-V curve. d_{ox} = 440 Å, Annealing Temp = 650°C, C_{ox} = 7.8×10^{-8}F/cm^2, C_{ox} (total) =220pf, C_{fb} = 7.2×10^{-8}F/cm^2, C_{fb} (total)=204pf, $V_{fb}(C=C_{fb})$ = -2V, Temp(B-T)=150°C, V_{Bias}(f+) = + 10V, V_{Bias}(f-) = - 10V, time = 30 minuts ,SiH_4=300sccm, O_2=75sccm, deposition temp.=425°C

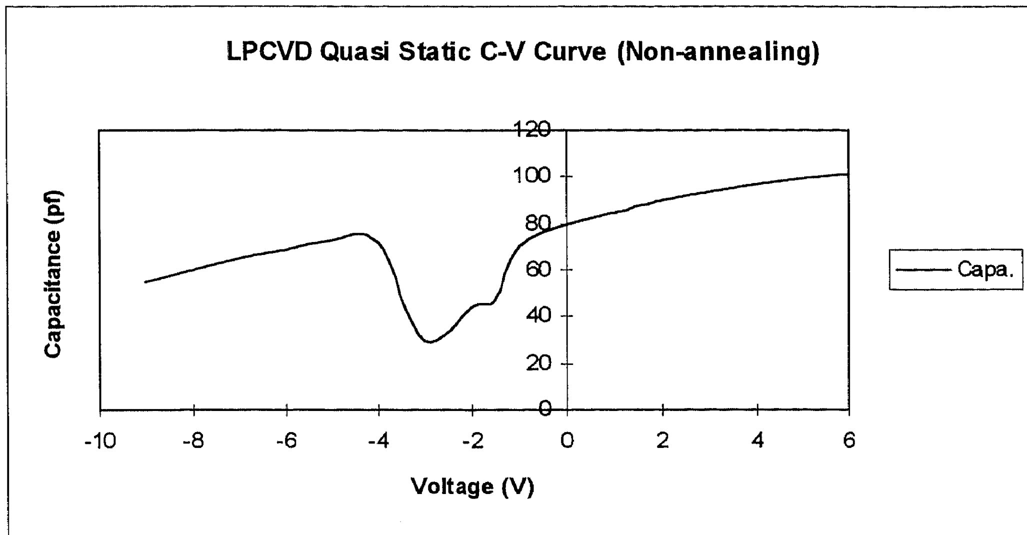


Figure 4.28 LPCVD SiO_2 Quasi Static C-V curve. d_{ox} = 392 Å, non-annealing, C_{ox} = 8.8×10^{-8}F/cm^2, C_{ox} (total) =248pf, C_{fb} = 7.9×10^{-8}F/cm^2, C_{fb} (total)=220pf, SiH_4=300sccm, O_2=75sccm, deposition temp.=425°C

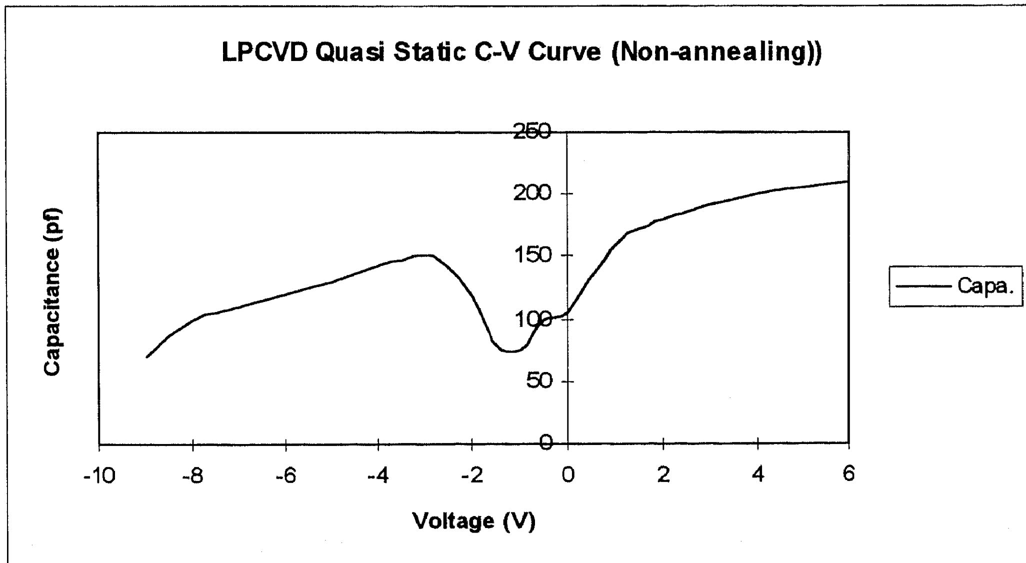


Figure 4.29 LPCVD SiO_2 Quasi Static C-V curve. d_{ox} = 510 Å, non-annealing, C_{ox} = 6.77×10^{-8}F/cm^2, C_{ox} (total) =188pf, C_{fb} = 6.22×10^{-8}F/cm^2, C_{fb} (total)=173pf , SiH_4=300sccm, O_2=75sccm, deposition temp.=425°C

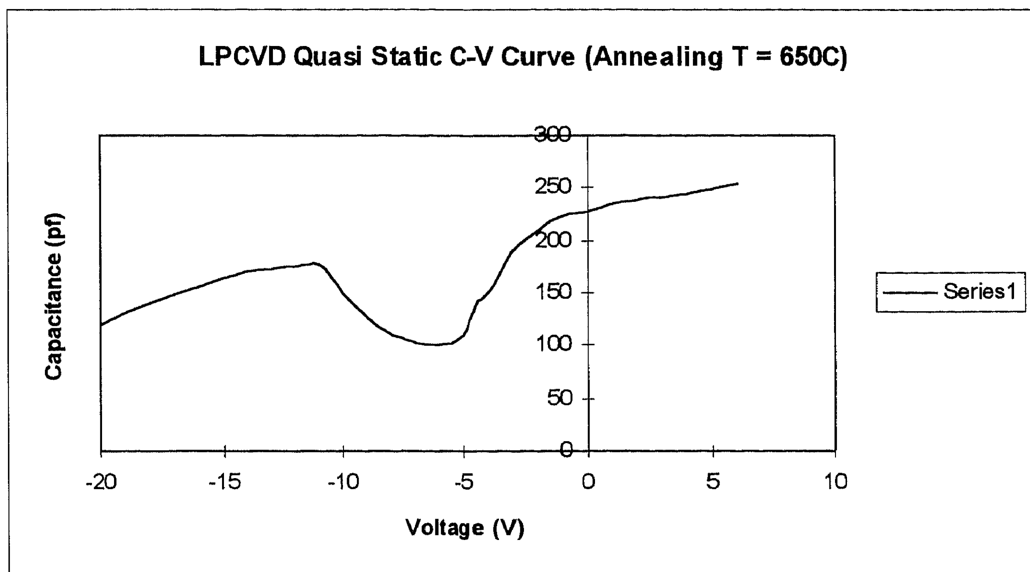


Figure 4.30 LPCVD SiO_2 Quasi Static C-V curve. d_{ox} = 406 Å, Annealing Temp = 650°C, C_{ox} = 8.5×10^{-8}F/cm^2, C_{ox} (total) =240pf, C_{fb} =7.7×10^{-8}F/cm^2, C_{fb} (total)=218pf, SiH_4=300sccm, O_2=75sccm, deposition temp.=425°C

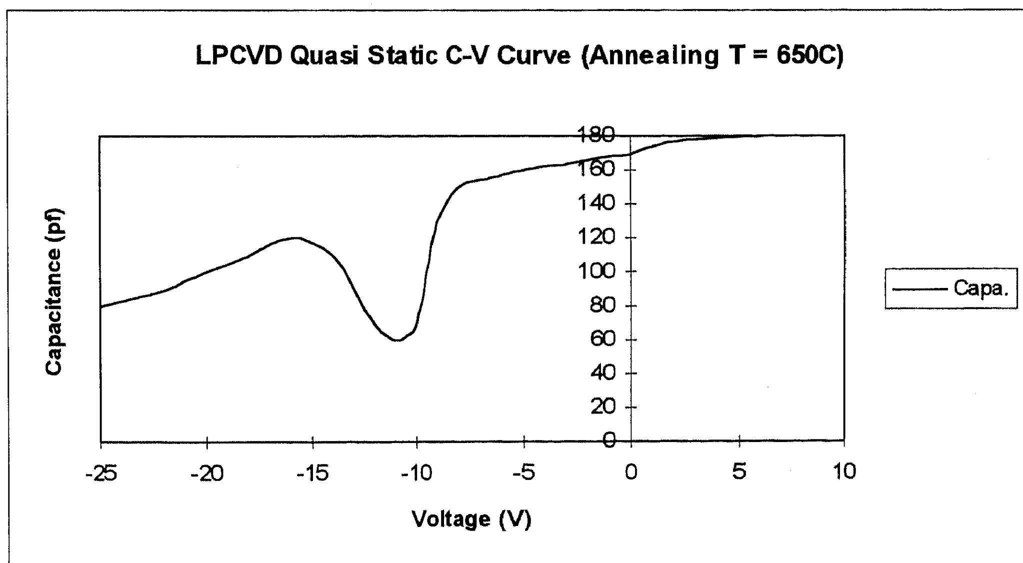


Figure 4.31 LPCVD SiO_2 Quasi Static C-V curve. d_{ox} = 440 Å, Annealing Temp = 650°C, C_{ox} = 7.8×10^{-8}F/cm^2, C_{ox} (total) =220pf, C_{fb} = 7.2×10^{-8}F/cm^2, C_{fb} (total)=204pf, SiH_4=300sccm, O_2=75sccm, deposition temp.=425°C

CHAPTER 5

CONCLUSIONS

Good-quality silicon dioxide films were deposited on Si substrate at a substrate temperature 300°C by PECVD and 425°C by LPCVD methods. The silicon dioxide films were found to depend on the deposition rate. In PECVD method, deposition rate 125 Å/min was achieved at the condition of reactive flow rate DES 12sccm, N_2O 172sccm helium 850sccm, rf power 300W(0.09W/cm^2); and deposition rate 190 Å/min at the condition of reactive flow rate DES 12sccm, N_2O 172sccm helium 850sccm, rf power 500W(0.15W/cm^2). The SiO_2 films showed relatively good quality silicon dioxide film which had refractive index 1.47, breakdown voltage 4-5 MV/cm, less pin-hole, measurement leakage current 10^{-9}A. Control over the rate of deposition was achieved by reducing total reactive gas flow(mimimun 184 sccm) and rf power (from 0.15W/cm^{-2} to 0.09W/cm^{-2}), together with a large flow of inert carrier gas helium(850 sccm) to ensure film uniformity. The investigation of electrical characteristics of the films showed that the total effect of interface trap and fixed charge density $N_t = 5.4\times10^{12}$ cm^{-2} and flatband voltage V_{fb} = -16V for non-annealing MOS capacitor and the total effect of interface trap density 6.4×10^{11} cm^{-2} and flatband voltage -4V was obtained at the oxide thickness d_{ox} = 1160Å by using annealing at temperature 650 °C for 30 minutes in the ambient of nitrogen. The experiment results shows post deposition annealing can improve the quality of the oxide film. Films deposited at conventional high rates (> 330 Å/min) are of a relative poor quality which has refractive index >1.47, breakdown voltage <2 MV/cm.

LPCVD silicon dioxide exhibit good quality and better electrical properties with the deposition rate 14.5 Å/min. The deposition parameters were: ambient temperature 425°C; furnace pressure 0.5 Torr; SiH_4 flow rate, 300 sccm; O_2 flow rate, 75 sccm. The investigation of electrical characteristics of the films showed that the total effect of interface trap and fixed charge density $N_t = 3.9\times10^{12}$ cm^{-2} and V_{fb} = -8V (d_{ox} = 392Å) for non-annealing and $N_t = 4.9\times10^{11}$ cm^{-2} and V_{fb} = -2V (d_{ox} = 440Å) by using annealing at temperature 650 °C for 30 minutes in the ambient of nitrogen. The film refractive index was 1.46, breakdown voltage 5-6 MV/cm, measurement leakage current (10^{-9}A). Post deposition annealing was thought very helpful for reducing the interface trap density and improve the quality of the oxide film. Finally, the LPCVD oxide film is chosen as gate oxide for fabrication of the SiGe-channel MOS device.

This investigation showed that LPCVD processing to grow insulating gate oxide for SiGe MOSFET is a primary method at the present period. However, further research in PECVD method, which has large potential to improve the quality of the oxide film, including reducing deposition rate, reducing refractive index to 1.46, improving uniformity and density, reducing interface trap density and minimize contamination should be done in the near future.

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