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ABSTRACT

ULTRA-THIN SILICON WAFER BONDING

by
Diyu Yan

In this thesis the history and recent developments on the silicon direct bonding technique are reviewed. The growing applications of this technique in SOI, SOS and MEMS areas, difficulties and disadvantages of various bonding processes are discussed. A direct bonding procedure for attaching ultra-thin wafers less than 200 μm thick to substrate wafers is developed and described in detail. Difficulties in handling, aligning and annealing ultra-thin wafers are reported. Wafers of different doping concentration, thickness, surface roughness and chemical characteristics are tested for bondability. Methods to minimize voids and other failure mechanisms are proposed. A photodetector is designed based on ultra-thin wafer bonding. The essential fabrication details of this detector are carried out to demonstrate the feasibility of using ultra-thin silicon wafer bonding to make an optically sensitive device.

ULTRA-THIN SILICON WAFER BONDING

by
Diyu Yan

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Submitted to the Faculty of
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Master of Science in Applied Physics

Department of Physics

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APPROVAL PAGE

ULTRA-THIN SILICON WAFER BONDING

Diyu Yan

Dr. Kenneth R. Farmer, Thesis Advisor — Date
Asst. Professor, Federated Department of Physics, NJIT and Rutgers-Newark

Dr. Ken Chin, Committee Member — Date
Professor, Federated Department of Physics, NJIT and Rutgers-Newark

Dr. William N. Carr, Committee Member — Date
Professor, Department of Electrical and Computer Engineering, NJIT
Professor, Federated Department of Physics, NJIT and Rutgers-Newark

BIOGRAPHICAL SKETCH

Author: Diyu Yan

Degree: Master of Science in Applied Physics

Date: January, 1996

Undergraduate and Graduate Education:

- Master of Science in Applied Physics,
  New Jersey Institute of Technology,
  Newark, New Jersey, 1996

- Bachelor of Engineering in Engineering Physics,
  Tsinghua University, Beijing, P.R. China, 1993

Major: Applied Physics

This thesis is dedicated to
my dear parents

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CHAPTER 1

INTRODUCTION AND MOTIVATION

Since the creation of the first bipolar transistor in 1947, there has been an ever increasing number of devices manufacturable on semiconductor substrates. Silicon is presently the most important semiconductor for the electronics industry, and is likely to retain this position for the foreseeable future. Within this setting, silicon wafer bonding has attracted increased attention. Its applications in silicon-on-insulator materials, silicon-on-silicon materials, micromachining, microelectromechanical systems (MEMS) are very promising.

1.1 Method for Obtaining Thin Silicon Film in SOI, SOS and MEMS

Generally there are two ways to accomplish silicon wafer bonding:

1. Anodic bonding, or field-assisted bonding [1], was introduced in the 1960's based on electrostatic forces pulling the materials together. A top wafer is brought into mechanical contact with the substrate, then both wafers are heated to an elevated temperature and an electric field is applied across the boundary.

2. Direct or fusion bonding is a process in which a top wafer is brought into contact with a substrate, then annealed to promote adhesion.

polish" or "bond and etch".

In many applications, the ultimate goal for these methods is to obtain a thin

silicon film after bonding. Conventionally, this goal is achieved through "bond and polish" or "bond and etch"

"Bond and polish" [2] is currently used widely to form thin SOI layers. After a top silicon wafer of general thickness is bonded to an oxidized substrate, it is polished to the required thickness. The major disadvantage of the "bond and polish" technique is that polishing after bonding detracts from device yield, because the bonded interfaces are never as strong as the bulk material. Meanwhile, SOI layers less than 5 micrometers thick is difficult to obtain in this process, especially when a good uniformity is required. In the past, a technique called chemical-mechanical polishing, also called tribochemical, was introduced. This technique combines chemical attack of the material and abrasive grinding/polishing, resulting in a damage-free surface and subsurface. High-level geometrical precision, however, is sacrificed by this method.

"Bond and etch" [3] is another technique used for SOI materials. The yield detractor of polishing is avoided here by forming an etch-stop layer on a silicon wafer through ion implanting, the unwanted silicon is then removed by etching to the etch-stop layer. This process gives a much better thickness uniformity. Figure 1.1 is a schematic illustration for the fabrication of bond and etch-back silicon on insulator using a strain-sensitive etch and etch stop [4]. The etch-stop layer is formed often by ion implanting or dopant deposition or epitaxial growth. In recent years, many new and improved bond-and-etchback techniques have been introduced. However, problems still remain. Single selective etchstop cannot achieve high film thickness uniformity. Double etchstop technique has a high surface roughness related to the P^{++} implant damage. Drawbacks

associated with an MBE grown layer as an etchstop are low etch selectivity, high expense and misfit dislocations. An electrochemical etchback has been proposed where a reverse-biased p-n junction serves as an etchstop, but an elaborate wafer preparation scheme to provide bias through the SOI oxide, and a final orange-peel type of roughness renders this technique less attractive [3].

For MEMS applications, planar technology is used to form thin mechanical membranes. The membrane material is deposited over another material which is dissolved later from under portions of the membrane, freeing it to move. Unless complex and unreliable recrystallization methods are employed, this technique generally precludes the use of crystalline silicon as the membrane material. Both bond-and-polish and bond-and-etch technology are used for MEMS applications. In the bond-and-polish approach, the same disadvantage in SOI, low yield, cannot be eliminated; it is even worse because polishing over the delicate micromachined structures is much more complicated than polishing merely over bonded silicon. The thickness tolerance of polishing in some cases is not acceptable for thin membrane structures. The pressures of polishing may also cause damage to thin membranes. In the bond-and-etch technique for MEMS, an etch-stop layer is formed to a depth equal to the desired membrane thickness. After this layer is buried by bonding to a micromachined substrate, unwanted silicon is removed by selective etching and membranes over the micromachined features are obtained. The lack of control over doping profile and uniformity leads to variations in membrane uniformity. The process for etch and doping steps also add complexity. Furthermore, the heavily doped etch-stop layer limits electrical applications using the silicon membrane material.

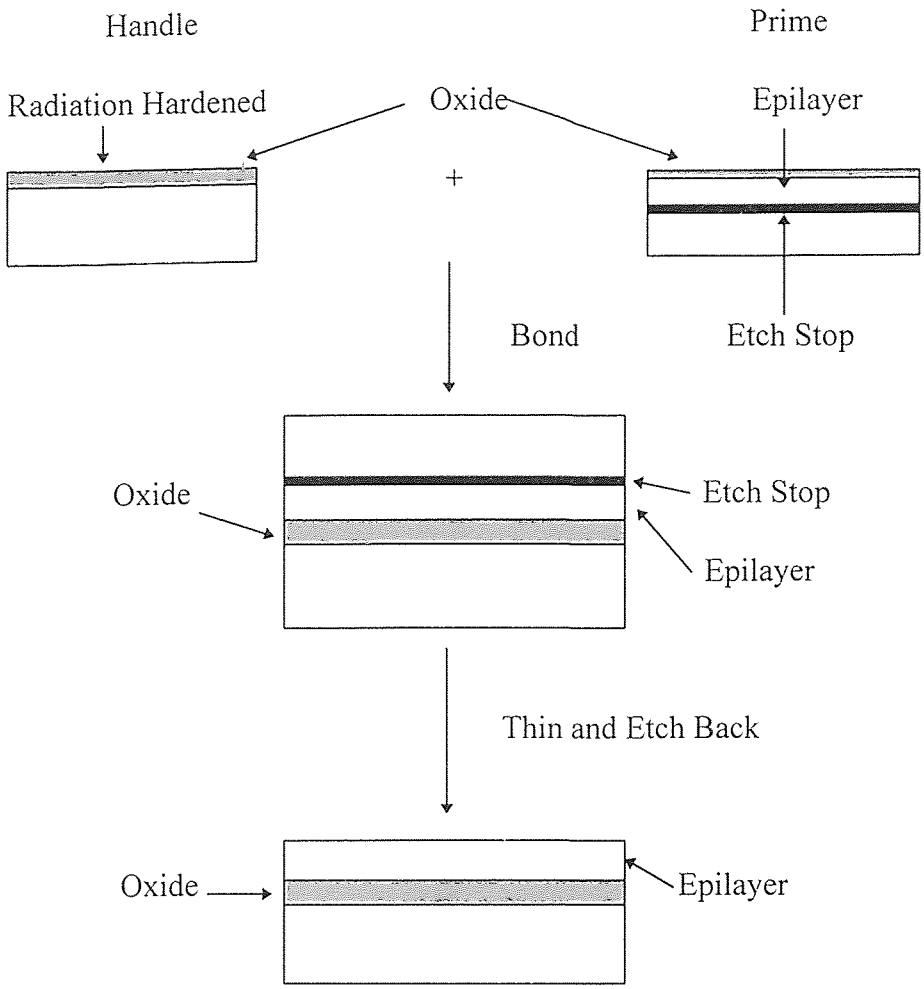


Figure 1.1 Fabrication of bond and etch-back silicon on insulator [4]. Top: handle wafer and prime wafer containing etch stop and epilayer are prepared with suitable oxides. Middle: After bonding the wafers through their oxides. Bottom: After thinning through the back side of the prime wafer to the silicon epilayer.

For SOS applications, the thin crystalline silicon film is usually formed by epitaxial growth on silicon substrates. This technique , whether vapor phase epitaxy or molecular beam epitaxy, is costly and relatively slow. Substrate materials are also limited to crystalline silicon if complex recrystallization techniques are not used.

As can be seen, in each of these application areas methods exist to produce devices which incorporate a thin film of silicon. But there are certain drawbacks accompanying each of these methods which makes device characteristics less than ideal.

1.2 Ultra-thin Silicon Wafers - A New Alternative

In this thesis, the term " ultra-thin silicon wafer" refers to the material manufactured by Virginia Semiconductor Inc., Fredericksburg, VA, which is less than 200 micrometers thick, beyond the limits of ordinary wafer polishing technology[5]. The ultra-thin silicon wafer provides a new alternative to obtain thin bonded structures. Ultra-thin wafers can be bonded to the substrate directly. Compared with other methods, the procedure for direct bonding is relatively simple and the quality of the bonded interfaces is sufficiently high. Both advantages are attractive to microelectronic device processing.

The bonding method in brief is to place a pair of mirror-polished silicon surfaces into contact with each other in a clean atmosphere, a weak bond in the form of a "contact wave" develops between the surfaces. The bonding is completed with a subsequent annealing, strengthening the interface bond energy. In Figure 1.2 three broad applications are represented in the sketches: a) a SOS structure formed by bonding a heavily doped p-type thin silicon film to a lightly doped n-type silicon substrate for

optical and electrical uses, such as a photodetector; b) a SOI structure formed by bonding an n-type thin silicon film on an oxidized n-type silicon substrate for power devices; c) a thin silicon film bonded to a micromachined substrate for use in MEMS systems. With the use of ultra-thin wafers, many disadvantages in the bonded wafer application areas, MEMS, SOI and SOS, are eliminated. In addition, new applications which are not possible due to the limitations of existing technology can be developed. For SOI and MEMS applications, ultra-thin silicon wafer direct bonding provides controllable thickness, uniformity and doping concentration. Complex doping, etching or polishing steps are no longer needed. In SOS applications, wafer bonding is a replacement to thick epitaxial growth or time-consuming deep impurity diffusion. Type p-p, n-n and p-n junctions can be made by directly bonding two silicon wafers with different types and concentrations of doping impurities. Complex devices can be manufactured from these basic junctions. Thus, high performance microwave and photodetector devices may be achieved. As will be discussed later in this thesis, an IR detector is made to show one of its applications. The main structure of the detector is similar to part (a) in Figure 1.2. The structure can be obtained easily from direct wafer bonding.

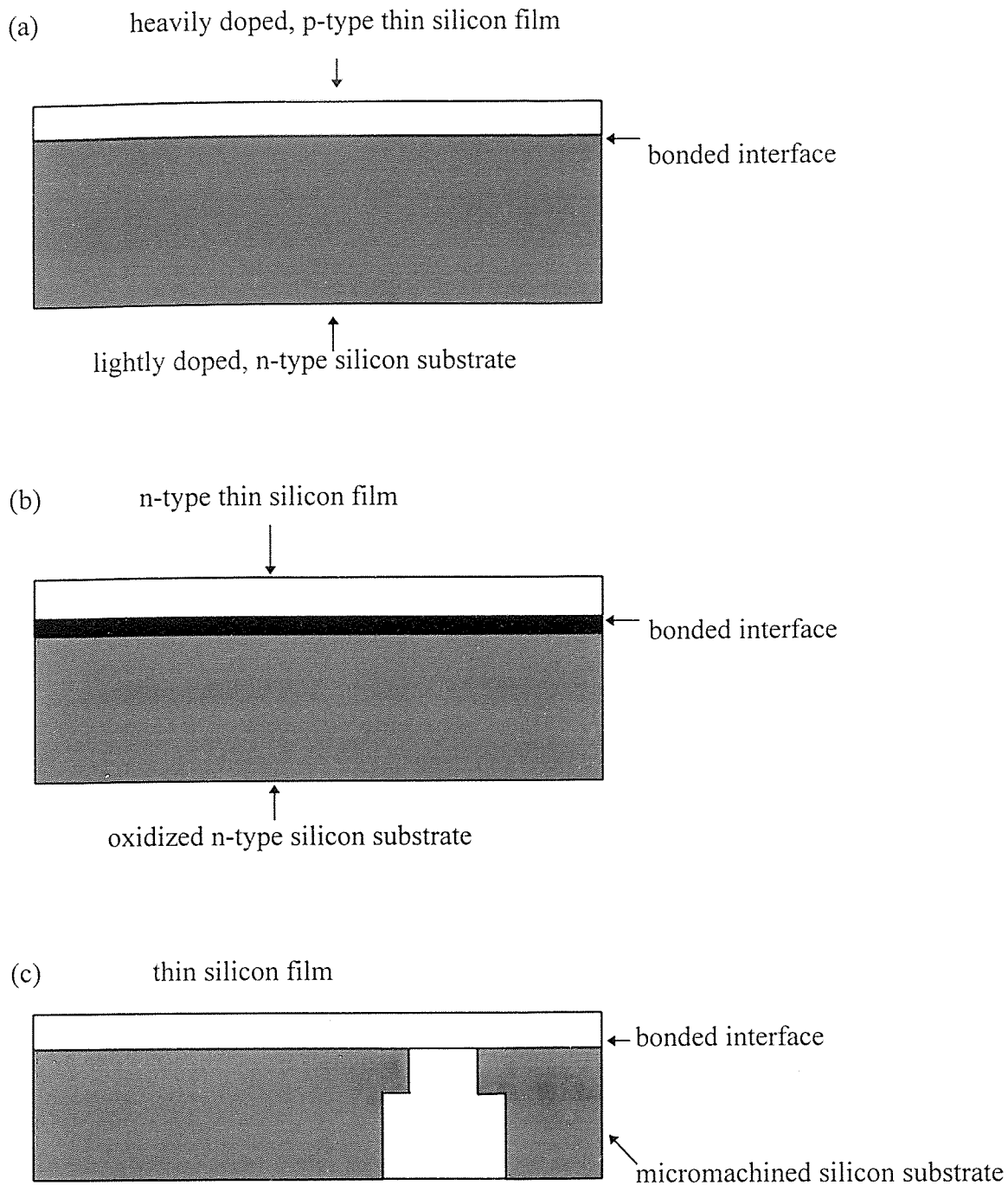


Figure 1.2 Bonded wafer product in three broad application areas: a) thin film SOS b) thin film SOI c) thin film silicon on a micromachined substrate

CHAPTER 2

MECHANISMS OF WAFER BONDING

2.1 Conventional Bonding Method

In 1969, George Wallis and Daniel I. Pomerantz [1] introduced a new process which permits the sealing of metals to glass and other insulators at temperatures well below the softening point of the glass. The experimental equipment consists simply of a furnace in which the parts are heated, and a dc power supply to apply a potential difference between the metal and glass parts. The faces of the glass and metal are first polished to a smooth, flat surface finish, then assembled and heated to a temperature well below the softening point of the glass. The power is connected to make the metal biased positive with respect to the glass. When a voltage in excess of a few hundred volts is applied for a time of the order of a minute, the glass and the metal are found to form a strong hermetic seal. This method is often called anodic bonding, or field assisted bonding.

In field assisted bonding, at first only a few points of the flat surfaces placed on top of each other contact, as shown in Figure 2.1. The two materials, though optically polished, are separated over almost their entire area by a gap of the order of a micron. Physical contact is accomplished by electrostatic attraction. An electrostatic field in the gap is set up by the applied voltage, and the field in turn generates the electrostatic force that pulls the parts together. Bonding spreads from the points of contact. Whether a bond will form subsequent to contacting appears to depend largely on temperature and on the

amount of time the materials remain in contact, as well as the type of mateirals bring bonded.

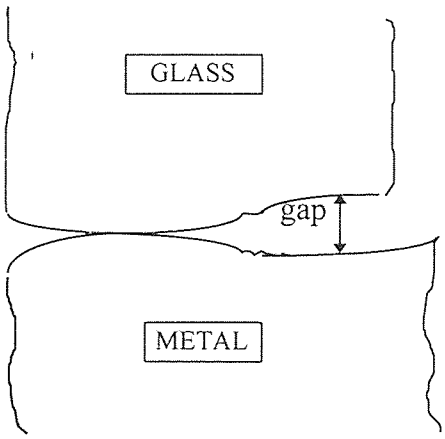


Figure 2.1 Cross section of glass-metal interface prior to sealing in field assisted bonding [1]

Another way to bond wafers is to deposit an adhesive layer on the wafer surfaces. A variety of materials can be used as adhesive layers. For example, many low melting temperature glasses, such as boron glass[6] and BPSG glass[7] can produce good bonding. The bonding is completed with an anneal step. Wafers were also joined by Si-B-O particles[8], even thin metallic films[9].

2.2 Direct Bonding

Field assisted bonding is only applicable if at least one of the materials is insulating or covered with an insulator. Although the field method has been known for a long time, an

alternative method has become popular only recently. This method, direct bonding, exploits the fact that oxidized and unoxidized silicon wafers can stick together at room temperature without any additional force applied. Direct bonding of silicon wafers does not need the help of electrostatic fields or intermediate adhesives deposited on the surfaces. The bond materials can be metals, semiconductors and insulators.

In our direct bonding experiments, two pre-processed clean silicon wafers with high flatness and smoothness are brought into contact at room temperature in a dust-free environment. One of them is of conventional thickness, the other one is ultra-thin, that is less than 200 micrometers thick. A weak bond develops due to weak attraction force between the surfaces. The bonding spreads out over the entire area of the wafer in the form of a "contact wave". The speed of the contact wave can be on the order of several cm/s [10] [11] . Faster speed can be obtained when the surface is smoother. The bonded pair is then annealed at an elevated temperature to increase the bonding strength.

W.P.Maszara [10] developed a simple method to quantitatively measure the strength of the bond created during contacting at room temperature or by annealing at elevated temperatures. The procedure is to measure the surface energy of the bond. Using the theoretical analysis of crack propagation in a cleaved bulk sample of a linearly elastic solid [12], the relationship between the surface energy and the geometry of a crack was derived. Figure 2.2 is a schematic diagram of the measurement. The crack length L is measure by inserting a thin metal blade. The relation between the thickness of the blade 2y, the crack propagation distance L, the thickness of the wafers t, and the surface energy γ is [12]

$$\gamma = 3Et^3y^2/(8L^4) \qquad (2.1)$$

where E is Young's modulus of elasticity. The distance L is measured using an infrared image converter.

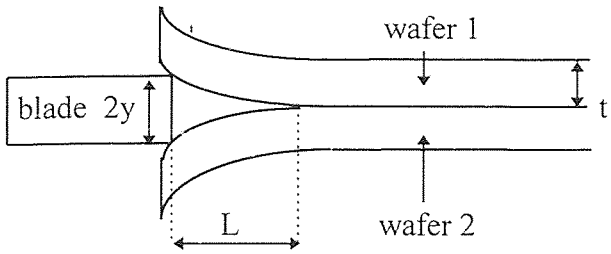


Figure 2.2 Schematic diagram showing the method of surface energy measurement of two bonded wafers by separation with a blade. [10]

The surface energy of Si - Si interfaces is illustrated in Fig 2.3[13]. Obviously the surface energy increased considerably after annealing.

The bonding mechanism has been explained in the following ways. One model that has been jproposed is based on the structure of the adsorbed molecules at the SiO2 surface[14]. For a silicon or SiO2 surface exposed to air, there are a few monolayers of organic contaminants, mainly hydrocarbons, physically adsorbed water vapor, and silanol groups (≡SiOH) present at the bonding interface. It is thought that at room temperature, adhesion takes place between the thin adsorbed layers on the wafer surfaces as illustrated in Figure 2.4. Lasky et al.[15] proposed that the attraction force at room temperature is caused by hydrogen bonds between hydroxyl groups and water molecules adsorbed on the two wafer surfaces. Van der Waals forces between atoms and molecules in the

adsorbed layers may also contribute to the attraction between two mirror-polished surfaces [14].

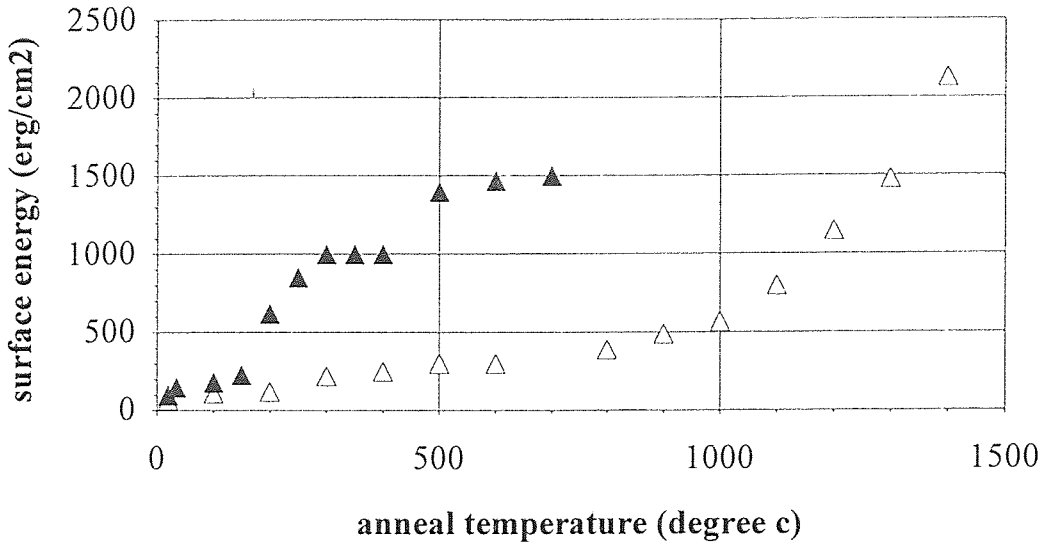


Figure 2.3 The surface energy of SiO_2-SiO_2, open symbols, and Si-Si, filled symbols, interface vs. annealing temperature. The annealing was carried out for 10 minutes (SiO_2) and 15 minutes (Si).[13]

When this pair of weakly bonded wafers is annealed by raising the temperature to 1100°C, several chemical reactions occur. At first, when the wafers are brought into intimate contact at room temperature hydrogen bonds develop between the oxygen and hydrogen atoms of the adsorbed water molecules. Four of these water molecules can form a water cluster (cyclic tetramer) [15]. As the temperature of the bonded pair is increased, it becomes energetically favorable for the water clusters to separate from the SiOH-groups and form rings around the now developing SiOH:OHSi bonds, as demonstrated in Figure 2.5 [14]. Since the tetramers have a diameter of about 4Å they cannot easily

diffuse away from the bonding interface through the SiO_2 network. The increased surface mobility of adsorbed species causes an increased number of bonds to bridge the gap between the wafers. Elastic deformation of wafers may also contribute to an increase in the density of bonds.

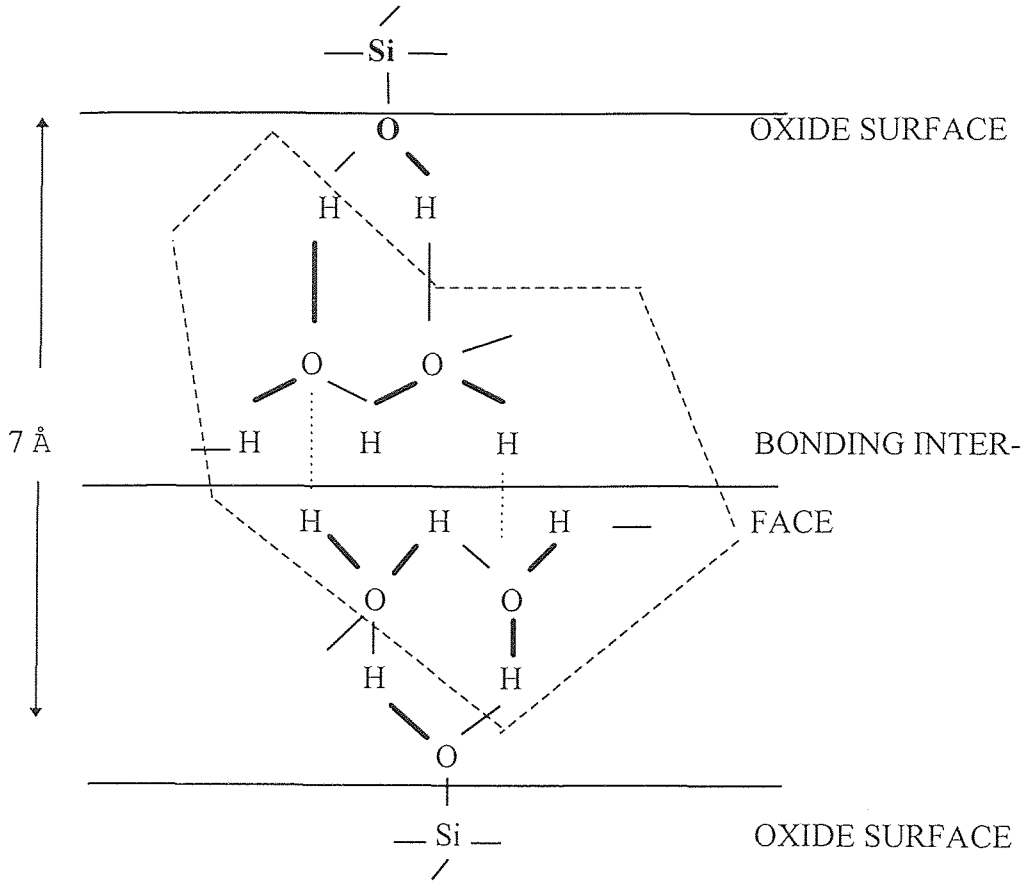


Figure 2.4 $SiOH:(OH_2)_2:(OH_2)_2:HOSi$ [14]

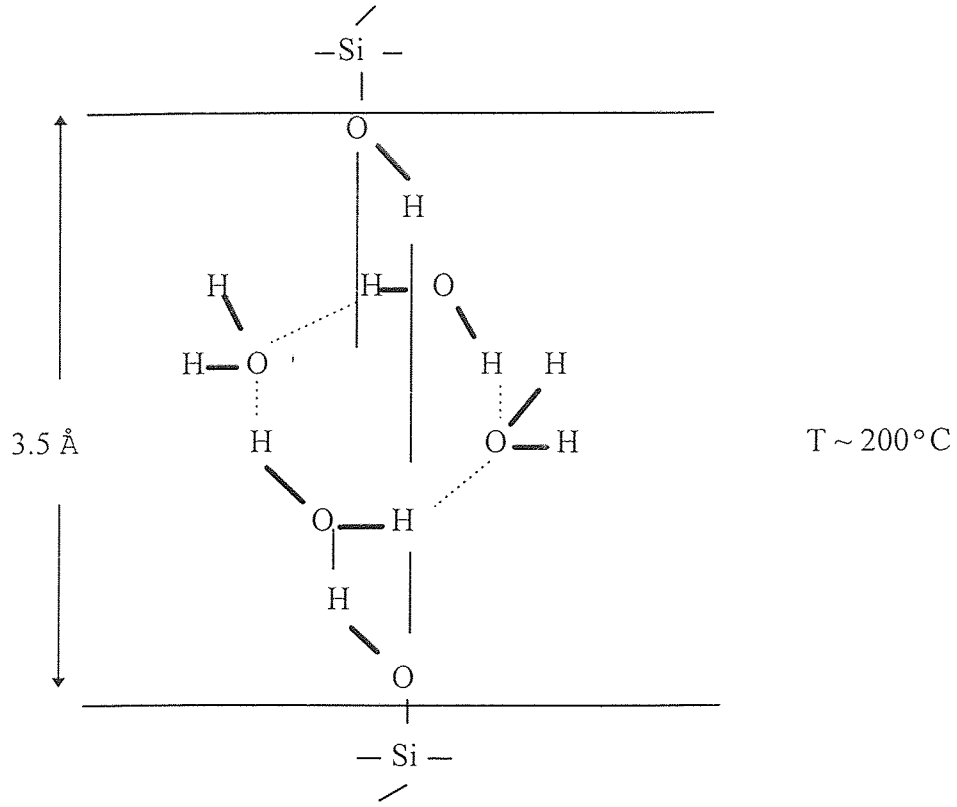


Figure 2.5 SiOH:OHSi + (H_2O)$_4$ [14]

As the temperature goes higher to above 700°C, the water clusters decay and diffuse away from the interface. The single silanol bonds may now form Si-O-Si bonds accompanied by the release of a water monomer. The reaction is [15]

$$\equiv SiOH + HOSi \equiv \rightarrow \equiv Si - O - Si \equiv + H_2O$$

The symbol ≡ represents the three satisfied valence electron bonds of the silicon surface atoms. Thus, the initial weak bonding is replaced by a much stronger bonding. If the temperature is raised up to 1100°C, additional bonds are formed near those which already exist. Oxygen diffuses from the interface to the silicon bulk, forming Si - Si bonds together with excellent electrical contact. [16].

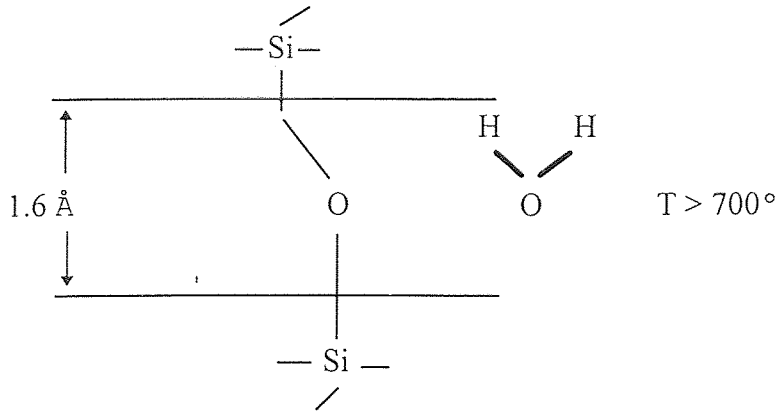


Figure 2.6 SiOSi + H2O [14]

In some applications, hydrophobic surfaces are desired due to the need for interface electrical properties. Though water and hydroxyl groups adsorbed on the wafer surfaces are believed to be important for the weak bonding at room temperature, which means wafer surfaces must be hydrophilic, it is not necessary in order for room temperature bonding to occur. Van der Waals interaction between adsorbed layers of molecules other than water and hydroxyl groups may take place as well. To achieve hydrophobic surface properties, the wafers are dipped in hydrofluoric acid (HF) prior to the final water rinsing and drying, thus dissolving the native oxides. Bonding of these wafers is also successful. Hydrophobic wafers do not show immediate bonding when laid on top of each other, however the bonding can be initiated by slightly pressing them together. The attractions they show are much weaker than hydrophilic ones. In our experiments, we found a hydrophobic pair is more easily to be separated than a hydrophilic pair after room temperature contacting. According to the experiments of

Y.Bäcklund[17], the surface energy of an interface between hydrophobic silicon wafers was measured to be approximately 2-4 times lower than the surface energy of an interface prepared with hydrophilic wafers. The successful bonding of hydrophobic surfaces is also due to the interaction between adsorbed layers on the wafer surfaces. The composition of adsorbed layers on hydrophilic and hydrophobic wafers is different. Surface atoms on an HF-dipped silicon surface are terminated with hydrogen, and the density of hydroxyl groups is also lower. Adsorbed water molecules are scarce since it is hydrophobic. Attractive Van der Waals forces between layers of hydrocarbons gives adhesion energies which are 2 - 3 times smaller as compared to the case of layers of water molecules[18]. However, in our experiments the bonded interface between two hydrophobic wafers is unbreakable after a high temperature anneal. Y.Bäcklund's experiments also showed that after an anneal at 800°C for one hour in oxygen, the interfaces of hydrophobic wafer pairs exhibited higher surface energies than the hydrophilic samples.

CHAPTER 3

BONDING PROCEDURE AND EXPERIMENTAL RESUTS

3.1 Fabrication Procedure

Raw materials for all the experiments are supplied by Virginia Semiconductor Inc.. In Table 3.1, different types of wafers that have been tested are included.

Table 3.1. Specification of wafers used for the preparation of bonded silicon - silicon interfaces.

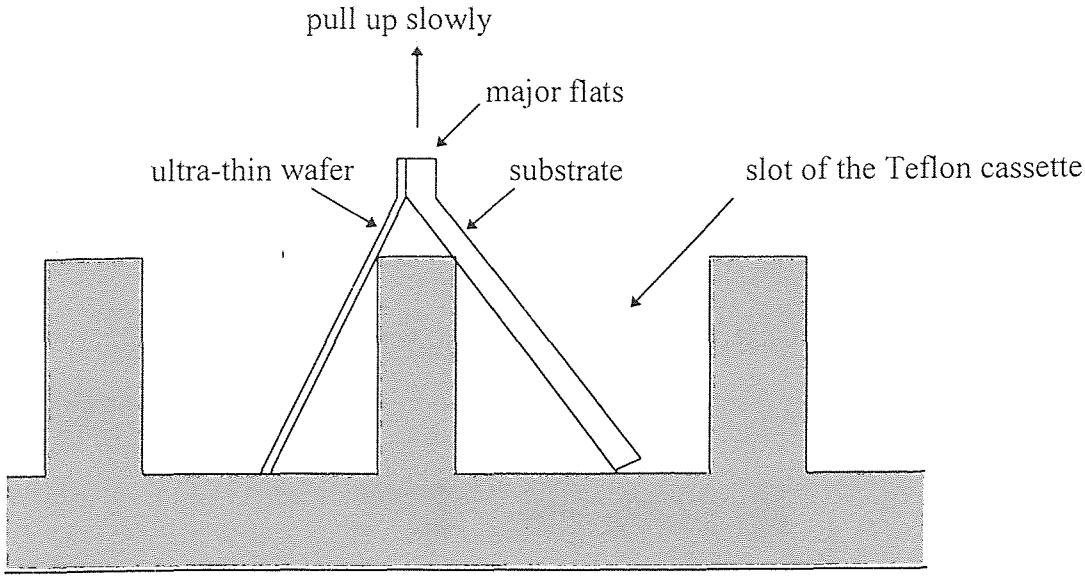
	Substrate	Substrate	Substrate	Handle	Handle	Handle
Doping Type	n	n	p	p	p	p
Cz/Fz	Cz	Fz	Cz	Cz	Fz	Fz
Orientation	<100>±0.50°	<100>±0.25°	<100>±0.50°	<100>±0.50°	<100>±0.25°	<100>±0.50°
Resistivity (ohm-cm)	2.0-6.0	0.00295-0.0037	<=0.02	0.015-0.016	>=1000.0	>=1000.0
Diameter (inch)	2.988-3.012	2.990-3.010	3.917-3.957	2.988-3.012	3.00±0.010	3.917-3.957
Thickness (mil)	0.0146-0.0150	0.0145-0.0155	0.01493-0.01772	0.0010-0.0014	0.0015±0.001	0.0037-0.0041
Sides Polished	single	double	single	double	double	double

All the experiments were carried out in the class 10 silicon processing facility at New Jersey Institute of Technology. The fabrication sequence is as follows:

1. Load wafers vertically into adjacent slots of a Teflon cassette suitable for chemical bathing.
2. "P-Clean" cassette in an aqueous, electronic grade solution of 80%-H_2SO_4 mixed nominally 50:1 with 20% H_2O_2, 10 minutes at 110°C [19].
3. Rinse cassette in warm de-ionized water, 10 minutes, 60 - 70°C.
4. Rinse cassette in cool deionized water, 5 minutes, ~ 20°C.
5. While preventing contact between the thin and substrate wafers, blow the wafers and cassette dry carefully in a gentle stream of nitrogen gas. This is a non-standard step; wafers are usually spun dry in a commercial spinner. In our case, the ultra-thin wafer cannot survive such rough handling. Drying the wafers completely is critical for achieving successful bonding. Evaporation of water trapped at the bonded interface can blow the wafers apart, shattering the thin wafer during annealing at high temperature. Attempts to bond wet wafers have been made. We managed to bond a 25μm ultra-thin wafer to a substrate when they were completely wet. The bonded pair was then kept carefully in an oven at 80°C for 21 hours and annealed later. After anneal, only a few small pieces of the thin wafer remained on the interface. Most of the parts were blown away. Small, almost invisible water drops can also contaminate the bonded surface.
6. Visually align the major flats of the two silicon wafers by rotating the wafers in their slots in the cassette. With care, this can achieve reasonable crystallographic alignment to ±1°.

7. Mate the wafers by slowly and simultaneously removing them from their adjacent slots in the cassette as illustrated in Figure 3.1(a). Allow the flats to come into contact first. This will initiate a contact wave whose propagation will be stopped by the Teflon divider between adjacent slots if the speed with which the wafers are pulled from the cassette is slower than the contact wave propagation speed. Typical contact wave speeds are on the order of 1 cm/sec, with maximum speeds for hydrophilic surfaces being reported to be 2 cm/sec. [20] For hydrophobic surfaces, slight pressure is needed to initiate and continue the contact wave. This is a non-standard step. For thick samples, as in Figure 3.2(b), the wafers to be bonded are often held in place on parallel chucks using a vacuum applied to the backside of each wafer. The wafers are then aligned, and brought into contact by removing air from the space between the surfaces to be mated. Vacuum mounting would be unsatisfactory for ultra-thin silicon films because they are easily deformed by the resulting forces.
8. Inspect the wafer pair to insure that there are no obvious voids at the interface. Such voids are easily observed as ripples on the thin silicon film, and are not easily removed by, for example, pressure applied to wafer pair. Upon annealing, the voids tend locally to rupture the thin silicon film and therefore are to be avoided.
9. Load the wafer pair into a suitable size quartz boat for automatic insertion into a 6 foot long, 7 inch diameter, quartz annealing tube.
10. Gradually insert the boat into the center of the furnace, pushing at a rate of ~ 0.5 mm/sec in N_2, flowing at 7.5 l/min, at 300°C. The slow push at relatively low temperature is critical to achieve successful bonding. Since the wafers are of different

(a)



(b)

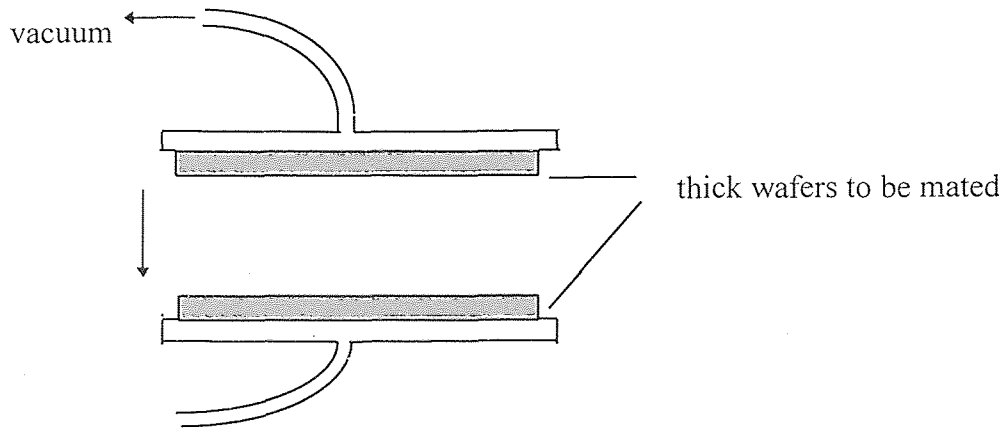


Figure 3.1 Wafer mating (a) Special procedure for mating ultra-thin wafer to a substrate. Initiate contact at aligned major flats, then slowly and simultaneously remove wafers from their adjacent slots in the cassette. Wafer deformation is exaggerated. (b) Conventional mating of thick wafers.

thickness and doping concentration, thermally induced differential interfacial stress caused by faster pushes at higher temperatures may be minimized or even eliminated when the slow, low temperature push is used.

11. Once the samples are loaded (which takes roughly 30 minutes), increase the temperature slowly, at a rate of 5 degrees per minute, to 1100°C, in the same flowing N_2 environment. This anneal is known to strengthen the bond at the interface[21]. At 1100°C, add 2.5 l/min of flowing O_2 to the annealing environment. It has been reported that O_2 leads to increased bond strength[22], but this claim has been disputed [3].
12. Anneal for one hour.
13. Turn off the flow of O_2, and ramp the furnace temperature to 300°C at the rate of 5 degrees per minute.
14. Pull the boat from the furnace at ~0.5 mm/sec in the flowing N_2. This slow pull rate continues to minimize the risk of the thermal stress related bond failure.
15. Allow boat to cool and remove bonded sample.

This fabrication sequence leads to the production of a bonded pair that can withstand the misorientation-induced stress caused by cleaving along one of the substrate's crystallographic axes. This is a minimum requirement for future device applications. In contrast, without the anneal, attempts to cleave pop the thin silicon film from the substrate.

3.2 Special Difficulties in Handling Ultra-thin Wafers

In general, ultra-thin wafers are difficult to handle. In Table 3.2, we include the special treatments of ultra-thin wafers as compared to wafers of regular thickness more than 500 microns.

Table 3.2 Different treatment for ultra-thin wafers and regular wafers.

Treatment	Ultra-thin Wafers	Regular Wafers
P-strip and p-clean	Pay special attention when putting the wafers under the liquid and taking them out. Each movement must be very slow. Wafers less than 25 μms thick tend to float up. Make sure the wafers stay in the cassette during the whole procedure.	No special attention is needed.
Oxide pre-clean	Generally not possible for wafers with thickness less than 100μm because the wafers tend to break while in the quartz oxidation boat.	Available.

Table 3.2 (Continued)

Treatment	Ultra-thin Wafers	Regular Wafers
Drying	Carefully blow dry. Do not leave any small water drops.	Spin dry.
Mounting	Mate by slowly and simultaneously removing wafers from adjacent slots.	Vacuum mounting.
Loading for anneal	Put bonded wafers on the quartz boat for anneal horizontally with thin ones on top if possible. Thin wafers are easy to crack when vertically put on the boat.	Put wafers vertically on the quartz boat to save space.
Inserting into the furnace	Pushing rate is as slow as 0.5 mm/sec	Regular pushing rate.

3.3 Voids

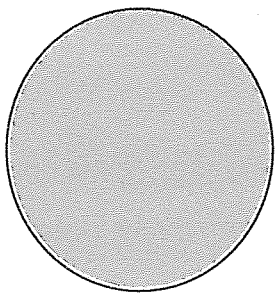
The points and areas where bonding has failed are named "voids", or "bubbles". Voids probably constitute a major obstacle for silicon wafer bonding. Basically there are two different types of voids, extrinsic and intrinsic voids. Extrinsic voids are formed during

the initial contacting of the wafers at room temperature. Intrinsic voids are formed during the procedure of annealing.

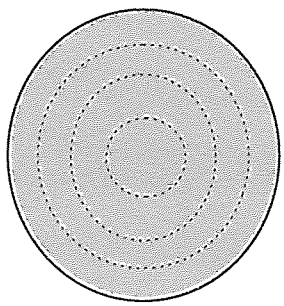
During LSI fabrication steps, silicon wafer surfaces are exposed to many kinds of contaminants. The main cause for extrinsic voids are dust particles, gas, insufficient flatness, local surface contamination of the wafers or air trapped in pockets when the mating of the wafers at room temperature has caused contact waves to originate from two or more points simultaneously. Basically all the voids introduced during the bonding process at room temperature remain during the annealing step.[11] Any dust particle, particularly those > 0.5 μm, on either bonding surface can hold apart the wafer surfaces and cause a void. [23] This is particularly true if hydrophlic surfaces are to be mated, because such surfaces 'attract' dust. It seems to be difficult to realize totally dust-free wafer surfaces prior to the bonding procedure. R. Stengl introduced a bubble-free silicon wafer bonding method [11]. The wafers are separated in the rack by Teflon spacers introduced at the wafer edges. After drying the wafers by a spin dryer, the spacers are removed and bonding occurs. However, this is not applicable in our experiments since our wafers are ultra-thin. A thorough cleaning procedure immediately prior to wafer contacting is crucial for reducing the density of voids. Our use of class 10 cleanroom, and our procedure of maintaining wafer surfaces vertical and in close proximity prior to bounding seems to minimize the presence of particles. An additional cleaning procedure of steam oxidation followed by oxide strip can also reduce dust particles considerably. This method is limited to wafers that are more than 100 micrometers thick, otherwise the wafers are too thin to survive the contact with the boat for oxidation. Usually we grow

1000Å SiO_2 by wet oxidation, then bond the wafers immediately after oxide strip. These wafers show better contact wave than the ones not treated with this clean step.

Surface roughness is discovered to be very important for bonding perfection. The surface roughness of the silicon surface is considerably influenced by the cleaning procedures. Wafers are also made rougher by processing steps such as doping or etching. Different suppliers, or even the same supplier with different final polishing and cleaning procedures can make the characteristic surface features differ greatly. Bonding with the rougher surface leaves many voids,[23] and it is extremely difficult to bond rough hydrophobic surfaces. Two types of ultra-thin wafers manufactured by Virginia Semiconductor Inc. have been experimented on to find out the relationship between surface roughness and bondability. They are of the same thickness but treated with different final thinning procedures. One type is polished and the other type is etched. The polished ones have mirror-like surfaces while the etched ones have tiny visible rings on them as shown in Figure 3.2. Both wafers were made hydrophobic before bonding. Good



ultra-thin wafer surface with final polish



ultra-thin wafer surface with final etch

Figure 3.2 Wafers with different surface roughness supplied by the same manufacturer

contact wave was formed when the polished ones were bonded. On the contrary, there was no contact wave at all for the etched ones. Applied pressure is required to form wafer bonds in this case. Even so, one of the three wafers of this type was not bonded after annealing.

Extrinsic voids have been reported in all types of silicon based, Si-Si, Si-SiO_2 and SiO_2-SiO_2 interfaces, while intrinsic voids have only been reported for Si-Si bonding. It is because large amounts of H, OH and H_2O exist on the bare silicon surfaces, irrespective of whether or not there is a thin layer of native oxide on it. However, very little of these species exists on the thermal oxide surface. From the experiments reported[24], the bare silicon surface and the natural oxide correspond to HF dipping and HCL/H_2O_2 cleaning, respectively. It was confirmed that the behavior of void formation was almost the same for both surface conditions in the lower temperature ranges. In the Si/Si structure, strong hydrogen bonding takes place and excess OH and H_2O fill in the microscopic variations in the wafer surface. The H_2O on the silicon surface is vaporized at over 100°C, and as a result, voids are formed. According to the reaction:

$$Si - OH + OH - Si \rightarrow H_2O + Si - O - Si$$

water molecules adsorbed on the siloxane network are released at the interface during the formation of Si - O - Si bonds. The onset of this reaction is at 200°C to 300°C and the water collects in pockets, causing voids. At higher temperatures the interfacial water is consumed by an oxidation process and the voids close. Conclusively, intrinsic voids are caused by water vapor released from the wafer surfaces.

Another explanation of the forming of intrinsic voids was proposed by V. Lehmann[22]. He found out that the phenomenon depend on the wafer source (i.e., the manufacturer) and the storage conditions. It was attributed to the deposition of organics on the wafer surfaces, especially since hydrocarbons have recently been identified as a possible major source of wafer contamination. The commonly used cleaning procedures prior to wafer bonding cannot sufficiently remove the hydrocarbons. Hydrophobic silicon surfaces are covered mainly with Si-H and Si-CHx groups. After annealing at 400°C, indications of the Chx groups nearly disappeared whereas even after annealing at 1220°C Si-C bonds were detectable. So most of the hydrocarbons evaporate during annealing, thus producing bubbles, while the carbon directly bonded to the silicon surface remains at the surface in some form of silicon carbide. This explains why generally treated hydrophobic bonded silicon wafers have more bubbles than hydrophilic ones do. Though they have a considerably lower density of water adsorbed on the surfaces, they have a higher density of hydrocarbons compared to wafers covered with native oxides, thus more voids are generated. However, if the hydrophobic wafers are treated with steam oxidation and oxide strip, the number of voids can be reduced to the same level as the hydrophilic ones due to the greatly reduced particles on the wafer surface. This is an additional value of the oxidation pre-clean.

CHAPTER 4

DESIGN OF PHOTODETECTOR

As discussed before, n-n_+, p-p and n-p type junctions can be prepared by direct silicon wafer bonding. Complex devices can be fabricated based on these junctions. In this chapter, a photodetector is designed based on n-p silicon-silicon wafer bonding.

4.1 Photodetector Mechanism

A photodetector is an electronic device that absorbs optical energy and converts it to electrical energy. Photodetectors demodulate optical signals, that is, convert the optical variations into electrical variations that are subsequently amplified and further processed. The primary mechanism is dependent on the concept of semiconductor band gaps, as shown in Fig. 4.1[25]. Semiconductor detectors that rely on that gap for their operation are called intrinsic detectors. An intrinsic photodetector usually detects light of wavelength close to the bandgap of the semiconductor. Additional energy levels can be created by deliberately adding impurities; this is referred to as doping the material, and the resulting detectors are called extrinsic detectors. An extrinsic photodetector detects light of energy smaller than the bandgap energy. In these devices the transition corresponding to the absorption of photons involves deep impurity and defect levels within the bandgap. Carriers can be given enough energy to cross the gap into the

conduction bands if they collide with an incoming packet of electromagnetic radiation - a photon. Energy of a photon in electron volts is[25]

$$E = hc/e\lambda \cong 1.24\ eV\mu m / \lambda \qquad (4.1)$$

If a photon does not have enough energy to promote an electron across the band gap, the electron cannot absorb any energy from the photon, and the photon will pass through the material undetected. Our experimental material is Si, which has a band gap of 1.12 eV, photons of wavelength 1.1μm have just barely enough energy to generate a

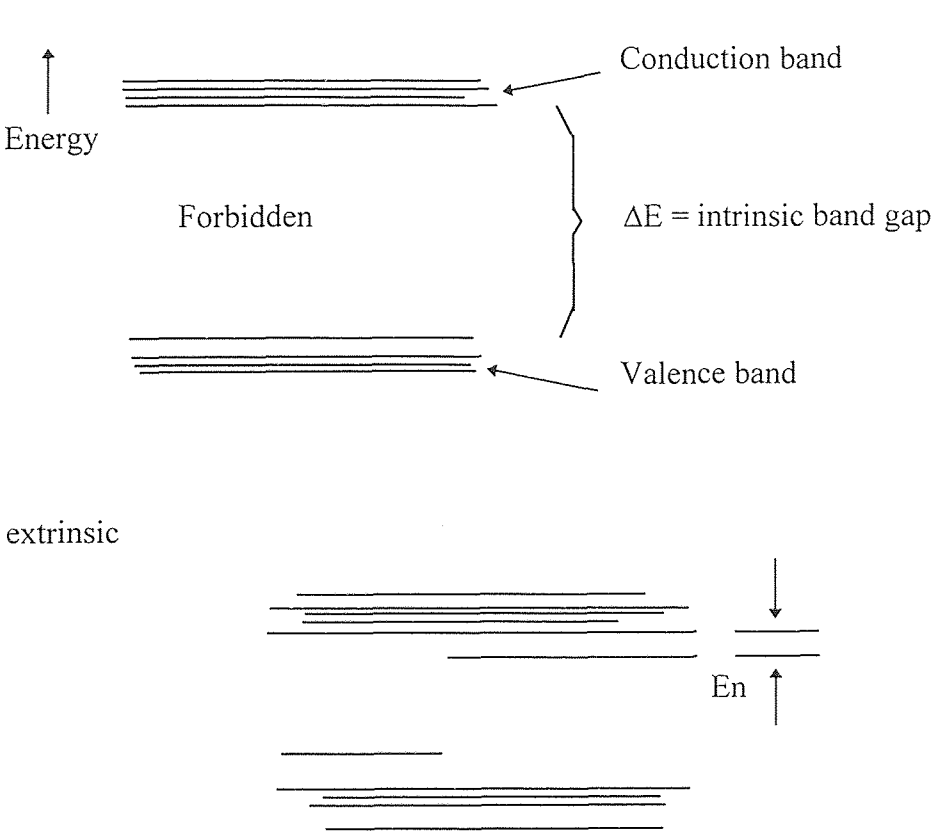


Figure 4.1 Photodetectors: energy levels.

conduction electron in Si. To photons with longer wavelength, Si is transparent. So in our experiment, the cutoff wavelength is 1.1μm.

A general photodetector has basically three processes: (1) carrier generation by incident light, (2) transportation of the photogenerated carriers across the absorption and/or transit region, with or without gain, and (3) interaction of current with the external circuit to provide the output signal.

There are mainly three types of photodetectors. Photoconductors, photovoltaic detectors and photodiodes. The junction photodiode is the most common photo detection device that is used in a multitude of ordinary and specialized applications. A semiconductor diode is made by joining two pieces of semiconductor material. One side is n-type material the other side is p-type material. As infrared radiation passes near the junction, it is absorbed and gives an electron enough energy to reach the conduction band. This generates an electron in the conduction band and leaves behind a hole that can also contribute to conduction. The presence of an electron-hole pair changes the current-voltage relationship of the diode. That change can be monitored to provide infrared detection.

4.2 Design Of Photo Diode

After an electron-hole pair is created in the depletion region of a reverse biased p-n junction, the charges are quickly separated by the field at the junction and flow around the external bias circuit, contributing to the reverse leakage current. The absorption must take place in the depletion region. This condition is difficult to meet because several tens

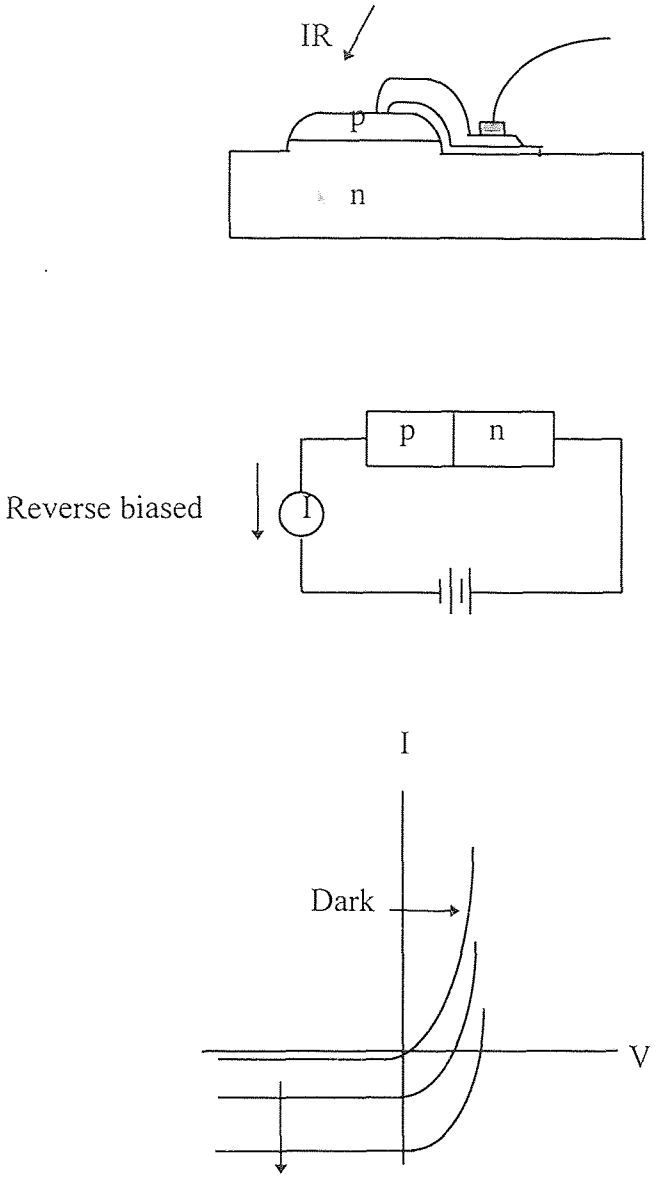


Figure 4.2 Diodes and photodetectors [25][26]

of microns are often needed to absorb light [27]; but depletion region widths are usually no bigger than a micron. The solution is to tailor the doping to stretch out the depletion region. As illustrated in Fig 4.3[27], a p^+n^{--} diode can be constructed so that the depletion region would extend a long way into the lightly doped n-side.

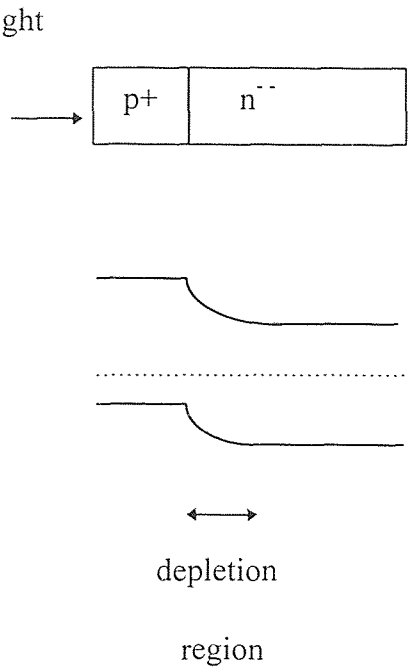


Figure 4.3 Extending the depletion region [27]

Our method to construct this p-n junction is to bond a low-impurity n-type silicon to a high impurity p-type silicon and then etch the p layer to desired thickness. Conventionally, this thin p silicon layer is often formed by epitaxial growth on silicon substrates at elevated temperatures in a high vacuum environment or by ion implantation. The process for epitaxial growth is both slow and expensive. The thin layer is grown

atomic layer by atomic layer in costly reaction chambers. The biggest drawbacks of thin silicon films formed by epitaxy on silicon substrates are the breadth of the interface, which can be several micrometers, and the uniformity of doping concentration within the thin film. For a photo diode, an abrupt transition is desired from one uniform doping

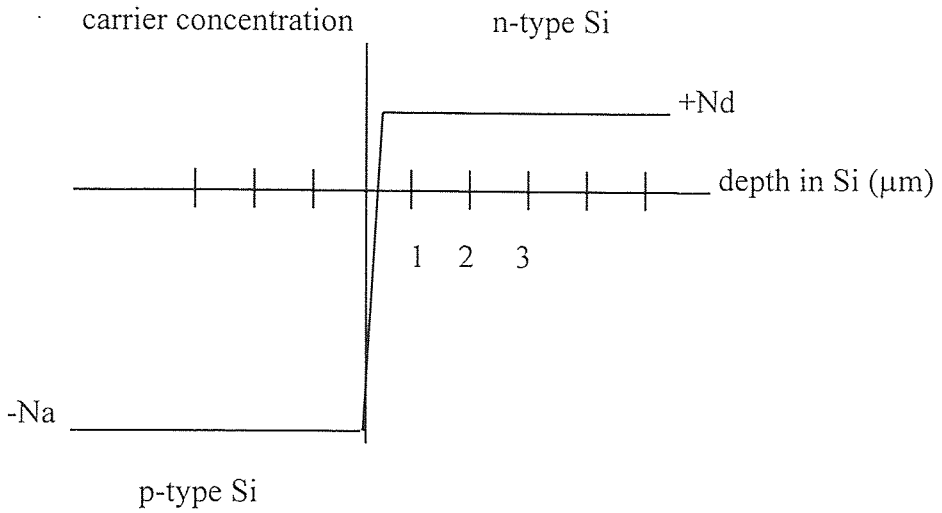


Figure 4.4 Schematic plot of carrier concentration as a function of silicon depth for an abrupt p-n junction. [28]

concentration to another, as illustrated in Figure 4.4 [28]. It is impossible to produce such structures by using epitaxy because the high temperatures and long times required for the thin film growth lead to dopant diffusion and junction broadening.

A relevant experiment has been done showing the carrier concentration as determined from a spreading resistance profile (SRP) measurement on a typical junction formed using epitaxy. Figure 4.5 [28] clearly illustrates one solution that minimizes the effects of dopant diffusion during growth: the n-type dopant concentration is gradually

decreased from the initial heavy concentration, then switched to the desired light p-type doping. Notice that the transition from heavy n to light n, then to light p occurs over more than 20 micrometers of sample depth, far from being abrupt.

Direct wafer bonding makes a new approach possible. In the same SRP measurement, a lightly doped, p-type ultra-thin wafer is bonded to a heavily doped, n-type substrate. The resulting carrier concentration profile is shown in Figure 4.6[28]. There are two important features to notice. One is the comparatively abrupt transition from heavy n to light p, even more abrupt than the transition from heavy n to light n in

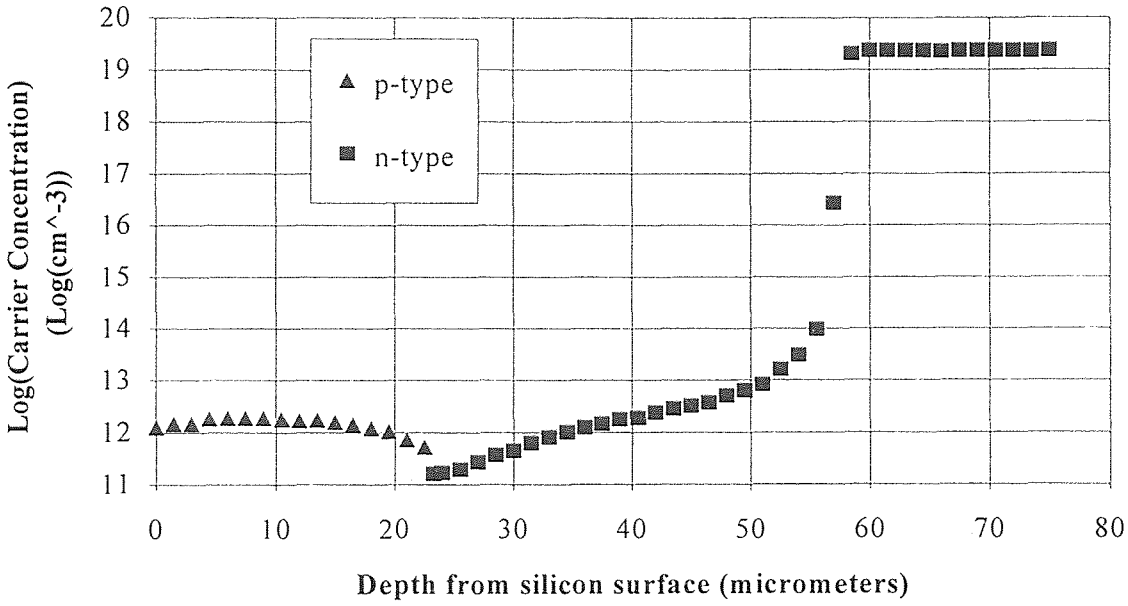


Figure 4.5 Carrier concentration as a function of silicon depth for a typical device formed using epitaxy. The "active" junction is the transition from heavily doped n-type silicon to lightly doped n-type silicon. The lightly doped top p-type silicon is an "ohmic" contact to the active device. [28]

ϕ = 0.69 V where k is the Boltzmann's constant, T is 300°K, q is elementary charge, ni is the intrinsic carrier concentration of 1.5 x 10^{16} /cm^3 , and carrier concentration N_A = 1x10^{19} /cm^3, N_D = 1x10^{13} /cm^3 for n-type and p-type respectively. The width of the depletion region at zero bias is then calculated as

$$W_p = [\, 2\, \varepsilon\, \phi\, N_D / q\, N_A\, (N_A + N_D)\,]^{1/2} \qquad (4.3)$$

where ε is the delectric constant. Wp = 5.5 μm in this case which proves that this is an electrical effect in the region 35 to 40 μm from the thin film's top surface.

However, if the annealing for bonding is carried out at very high temperatures for long time, the advantageous thermal budget of wafer bonding as compared to epitaxial growth is lost. We choose anneal at 1100°C to achieve highest strength while limiting deleterious diffusion. For example, to make a photodetector, we use an n-type substrate with a doping level of 1x 10^{15} atoms/cm^3, a p-type ultra-thin handle with doping level of 1x10^{18}. Assume there is a constant concentration Cs of boron diffusant at the p-n interface, then the boron concentration profile in the lightly doped n region, as a function of the distance x from the interface after t seconds at temperature T, is given by

$$C\,(x, t) = C_s\, \mathrm{erfc}\, [x / 2\, D^{1/2}\, t^{1/2}\,] \qquad (4.4)$$

where D is the diffusion coefficient of boron in silicon. At temperature T, D is given by

$$D = 0.76 \exp (-3.46 / kT) \qquad (4.5)$$

where k is Boltzmann's constant. For T = 1100°C and t = 3600 s, the junction depth is about 2.4 x 2 $D^{1/2}$ $t^{1/2}$ = 1.1 μm.[29] This is the position where the concentration of the diffusion profile equals the substrate doping.

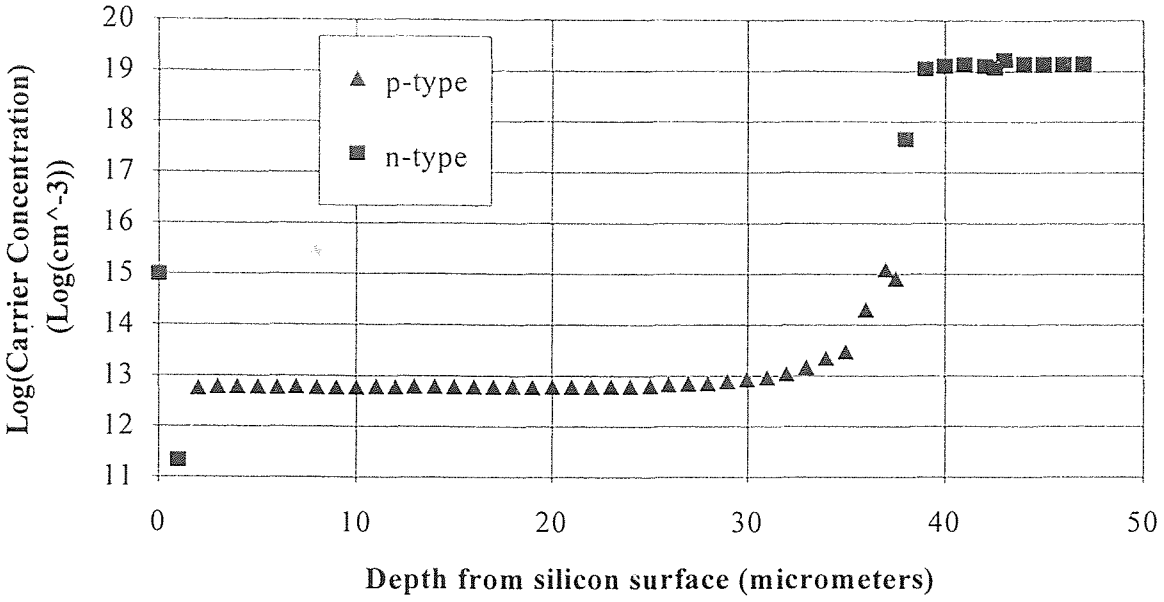


Figure 4.6 Carrier concentration as a function of silicon depth for a thin film bonded wafer structure. [28]

Figure 4.5, and the flatness of the p profile. These are the key achievements of this bonding process. Neither of these desirable characteristics are possible with existing technology, but are easily achieved with the bonded structure. The p layer can then be etched thinner to meet the requirement of a photo diode. There are other features to be noted. There is a less than 1μm thick n layer on the surface of the p layer. This was formed during the annealing step by out-diffusion of arsenic from the n-type substrate, followed by diffusion into the top p-type membrane. This unwanted layer can be easily etched off. The depletion region of this p-n junction can be caculated. The built-in voltage is:

$$\phi = \frac{kT}{q} \ln \frac{N_A N_D}{ni^2} \qquad (4.2)$$

If the thin layer is formed by ion implantation, there are also some problems. Ion implantation causes damage to the material structure of the target. In crystalline targets (e.g. single-crystal Si wafers), crystal defects and even amorphous layers are formed. To restore the target material to its pre-implantation condition, thermal processing after implantation must be performed. In some cases, significant implantation damage cannot be removed[30]. Ion implanters are complex machines, among the most sophisticated systems in wafer manufacturing. Thus also costly.

In conclusion, the direct bonding technique provides a high-purity defectless single crystalline layer formation by replacing silicon epitaxial growth or ion implantation. The cost for the complicated equipment is greatly reduced. The electrical properties are also improved.

CHAPTER 5

DEVICE PROCESSING AND TESTING

In this chapter the wafer level fabrication processing of a photodetector is discussed. The purpose of this work is to demonstrate the feasibility for making a photodetector using the direct bonding of ultra-thin silicon wafers. Junction formation includes two processing steps, wafer bonding and etching. The result of visible to IR transmittance measurement of the membrane is included in this chapter. Finally, the procedures are discussed for testing a photodetector made using this process.

5.1 Wafer Preparation And Bonding

The wafers chosen to make the photo detector are:

Table 5.1 Specification of wafers used for photodetector.

	Substrate	Handle
Material	Cz	Cz
Surface	Single side polished	Double side polished
Orientation	<100> +/- 0.50°	<100> +/- 0.50°
Dopant	Phosphorus, n-type	Boron, p-type
Diameter	2.988" - 3.012"	2.988" - 3.012"
Thickness	0.0146" - 0.0150"	0.0010" - 0.0014"
Resistivity	2.0 - 6.0 ohm-cm	0.015 - 0.016 ohm-cm

The n type substrate is lightly doped with concentration of 1 x 10^{15} atoms/cm^3 and thickness over 370μm, the p type membrane is heavily doped with concentration of 1 x 10^{19} atoms/cm^3 and thickness about 25 μm. We choose 25 μm wafers because they are easier to handle compare with 5 or 10 μm ones.

Three standard bonding steps were taken: hydrophylic wafer cleaning, manual bond and anneal. The detailed fabrication sequence is as described in Chapter 3.

5.2 Transmittance Measurement of Membrane Material

It is important that the membrane material, the 25μm p type silicon wafer in our case, should be made to be IR-transparent, otherwise incident light cannot even reach the p-n junction. This means the membrane should be thinned to be more transparent. We have measured the transmittance of 3 μm and 25 μm thick wafers for light of wavelength between 600 and 1200 nm. The 3μm thickness is made through TMAH etching, which is described below. The appropriateness of the thickness of ultra-thin silicon as an IR-transparent membrane is illustrated in Figure 5.1~ 5.6.

Two detectors with different bandwidth were used in the measurement. One is visible light detector and the other is for infrared. Figure 5.1 and 5.4 showed the output of these detectors without membrane samples. These curves are used as calibration.

Figure 5.2 and 5.5 show the output of the two detectors with the membranes in place. The drop of the curves after 900 nm in Figure 5.1 and 5.2 is due to the quantum efficiency drop off of the detector, it does not mean that the real transmittance of the

membrane is low for light of wavelength between 900 and 1000 nm. Figures 5.3 and 5.6 showed the % transmittance of the membranes as measured using the two detectors.

For the 3 μm sample, the measurements reveal that beginning at about 780 nm, 10% of the incident light is detected. This percentage increases with the wavelength to about 45%. The 25 μm sample has a much lower transmittance when the wavelength is relatively short, but only slightly less transmittance than the 3 μm sample in the region of infrrared light, which is about 50%.

5.3 Silicon Etching in TMAH

From the previous bonded wafer pair, we could make a photodetector by etching the 25 μm p layer to less than 3μm thick. Up to now, many kinds of etchants have been proposed. The important properties of anisotropic silicon echants are anisotropy, selectivity and process compatibility. Detailed characteristics of tetramethyl ammonium hydroxide (TMAH, $(CH_3)_4NOH$) as silicon anisotropic etching solutions with various concentrations from 5 to 40 wt.% have been studied by O.Tabata [31]. According to his experiments, very smooth surfaces can be obtained above 22 wt.%. TMAH is a promising solution for silicon micromaching as one of the useful etchants having good LSI process compatibility .

The etch rate depends on temperature, concentration and crystal orientation. Experiments were carried out to find out the etch rate of our ultra-thin silicon wafers. The TMAH solution we used is 25 wt.%, 99.9999% electronic grade. The temperature of the

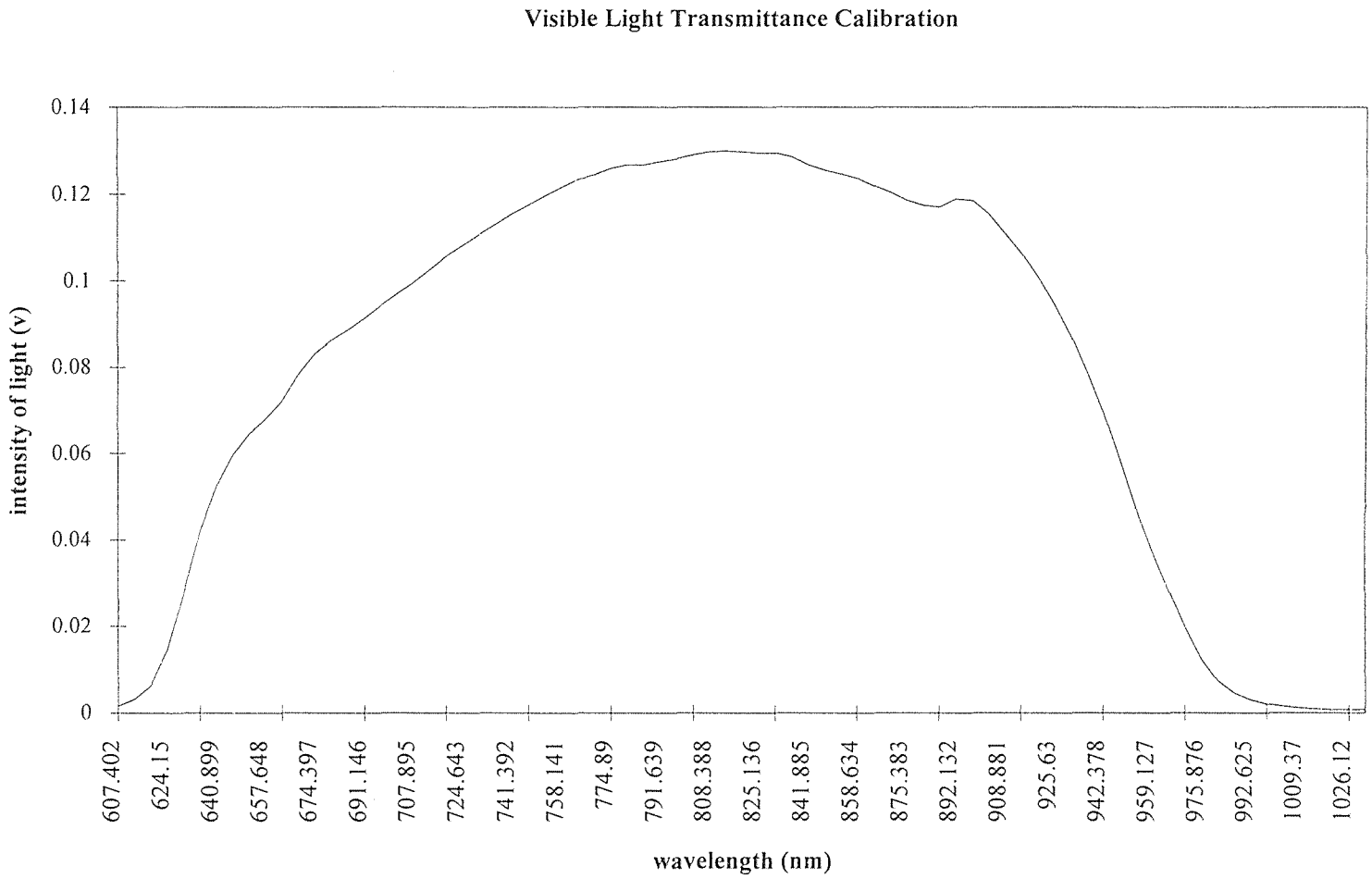


Figure 5.1 Visible light transmittance calibration

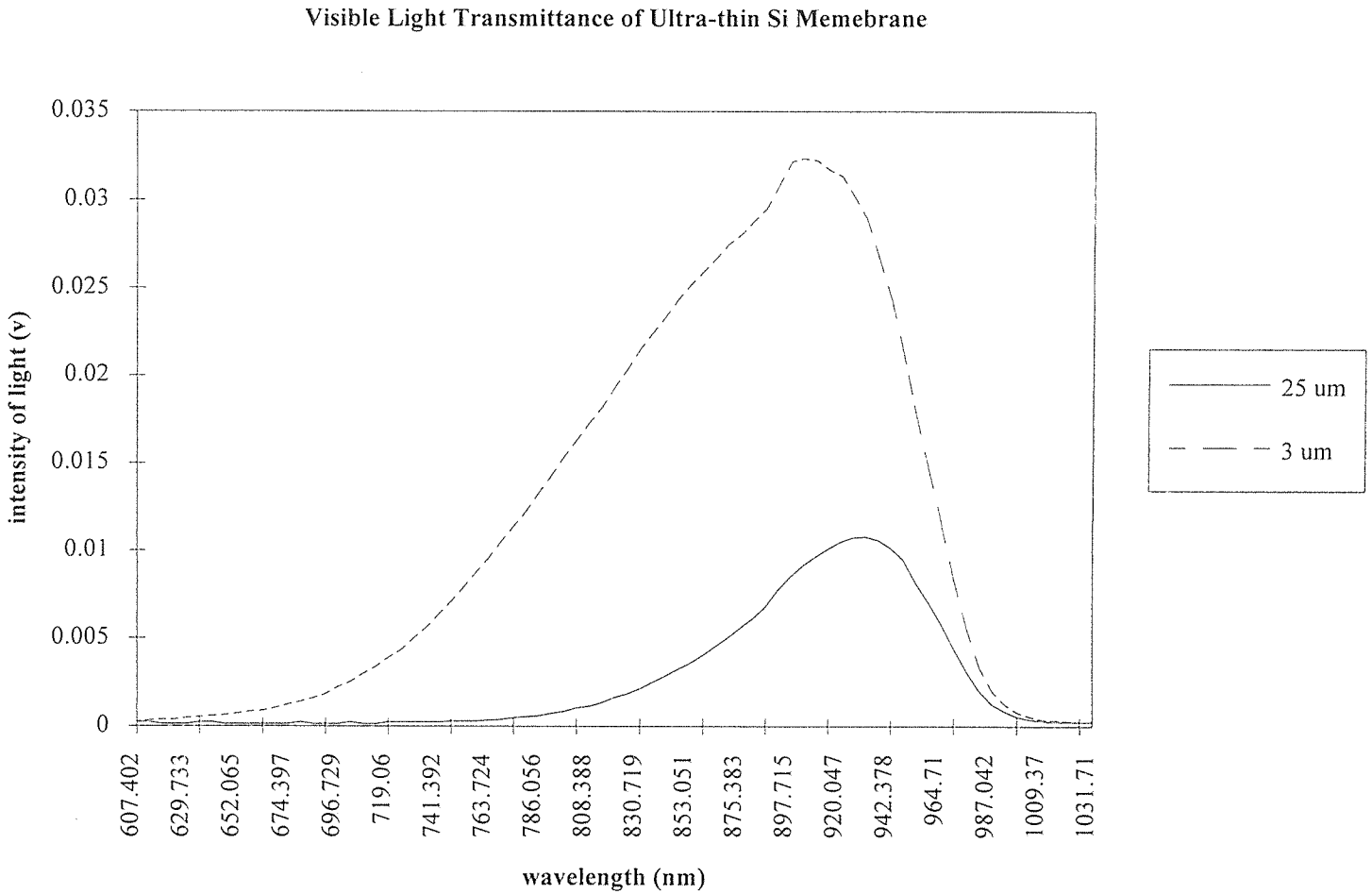


Figure 5.2 Visible light transmittace of ultra-thin Si membrane

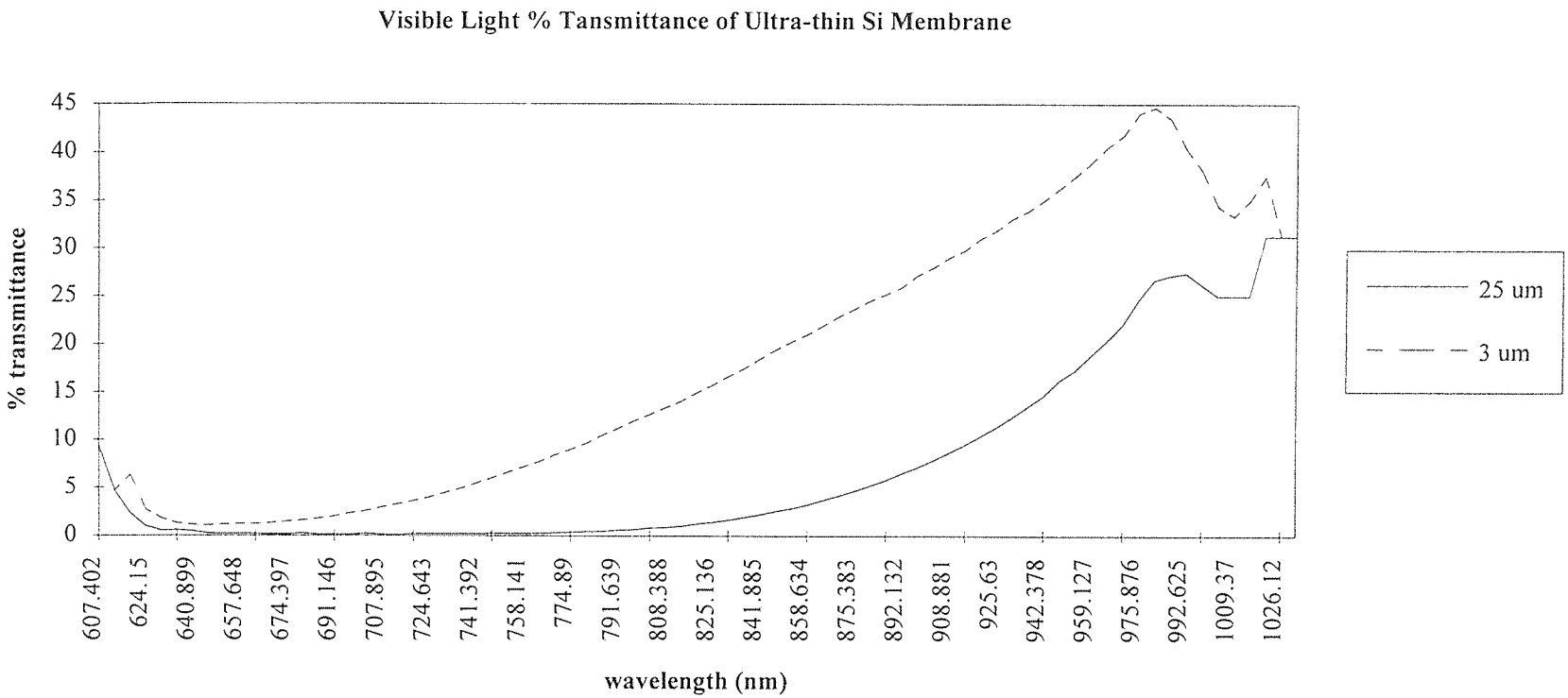


Figure 5.3 Visible light % transmittance of ultra-thin Si membrane

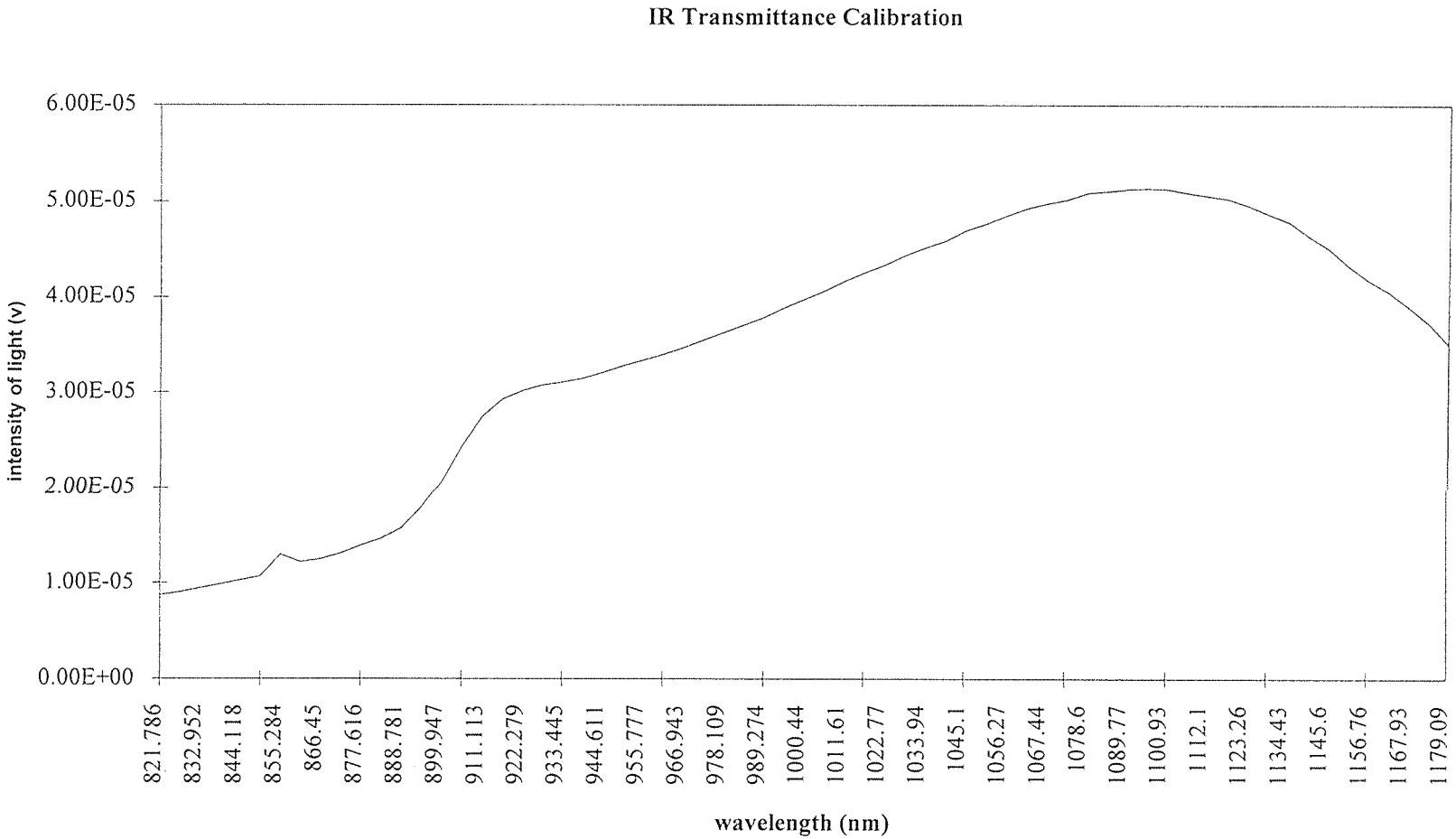


Figure 5.4 IR transmittance calibration

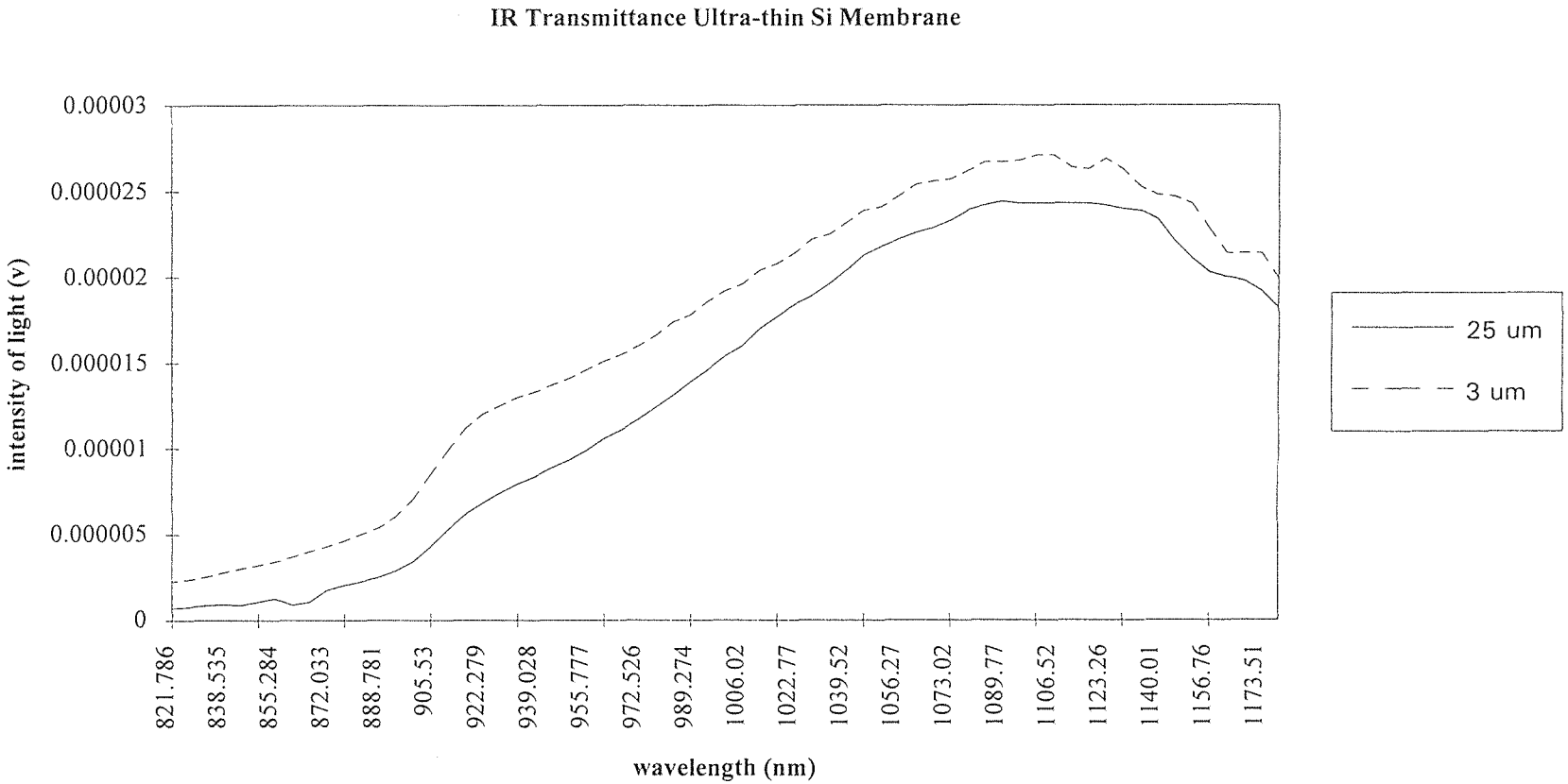


Figure 5.5 IR transmittance of ultra-thin Si membrane

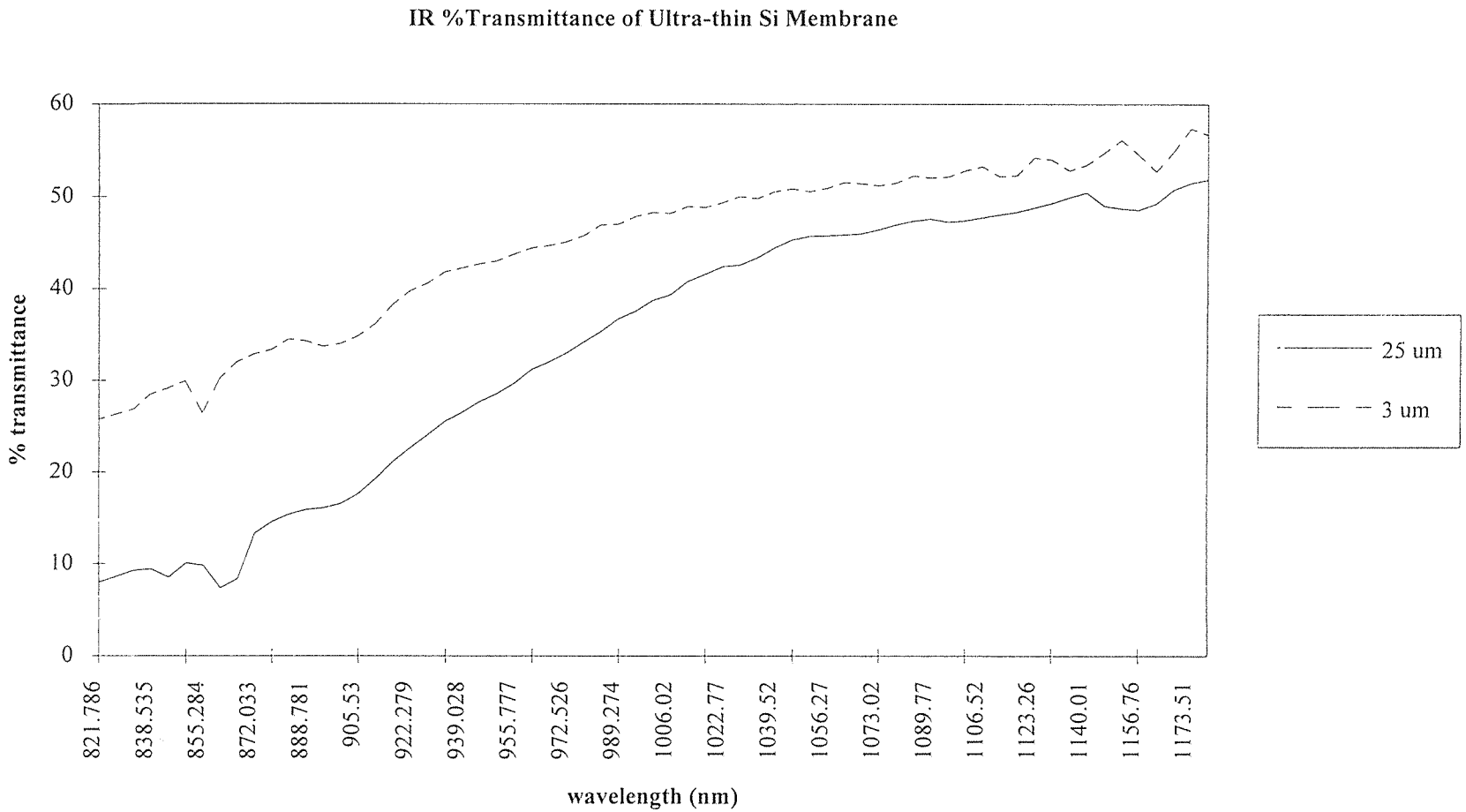


Figure 5.6 IR % transmittance of ultra-thin Si membrane

solution was kept at 80°C during the whole etching process. Our results show that etch rate decreases with time at fixed temperature, which may be due to the slight change of components of the solution as silicon dissolves. Whether the swirl function of the heater is set or not has influence on the etch rate as well, probably for the same reason since the swirl diminishes this effect. Different doping concentrations of the wafers have little effect on etch rate. Figure 5.7 shows the dependence of the etch rate on time and the comparison between two experimental cases.

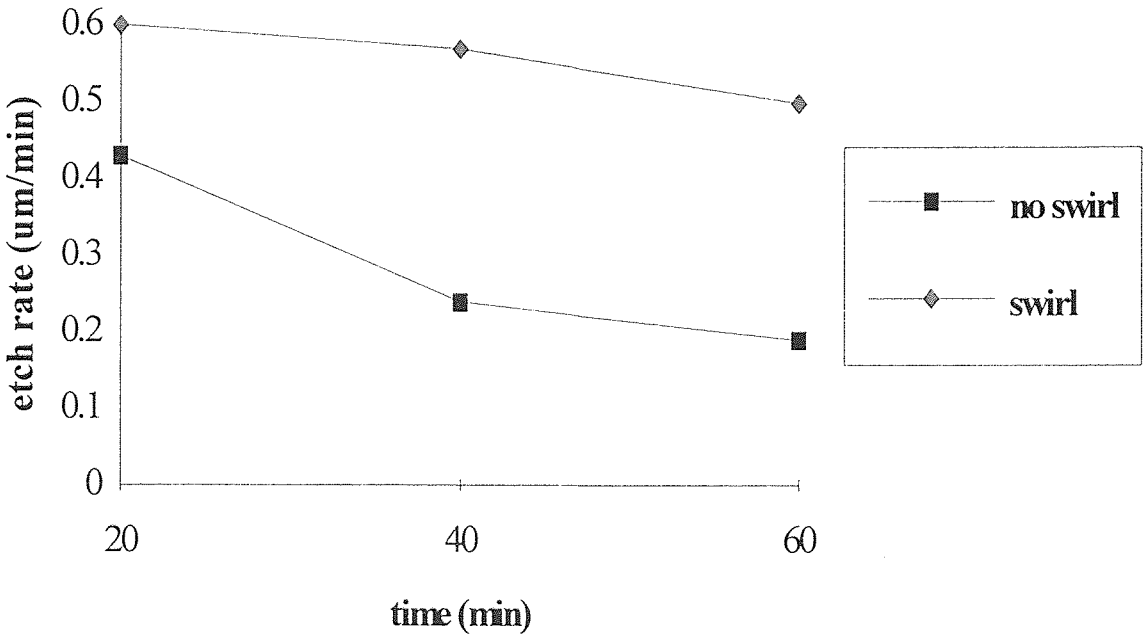


Figure 5.7 Silicon etch rate in TMAH at 80°C

With swirl on, it takes 40 minutes to etch the ultra-thin wafer from 25 μm to 3 μm. The thickness of the 3 μm membrane was measured by profilometer at 3 points of the surface. The results are 3.3544μm, 3.4614 μm and 3.4170 μm.

5.4 Device Testing

Although we have met our goal of demonstrating the feasibility of making a photodetector using the bonded ultra-thin silicon, one could complete the fabrication of such a device. In this case, the photo detector can be made using the bonded wafer with ohmic contacts affixed to opposite ends and connected to reverse biased voltage as illustrated in Figure 4.2. The reverse voltage reduces the carrier transit time and lowers the diode capacitance.

The performance of a photodetector is measured in terms of quantum efficiency and frequency reponse. The quantum efficiency η is the number of electron-hole pairs generated per incident photon

$$\eta = (I_p / q) / (P_{opt} / h\nu) \qquad (5.1)$$

where I_p is the photogenerated current by the absorption of incident optical power P_{opt} at a wavelength λ (corresponding to a photon energy $h\nu$). [32] For an ideal photodiode , η = 1. Absorption coefficient of the material is one of the key factors that determines the quantum efficiency.

The frequency response of the photodetector can be measured by gradually changing the wavelength of the incident light as did in the transmittance experiment. Specific wavelength range that appreciable photocurrent can be generated can be found

out this way. Usually in the near infrared region, silicon photodiodes show good quantum efficiencies.

CHAPTER 6

CONCLUSIONS AND SUMMARY

Rapid developments on the silicon direct bonding technique in the areas of silicon on insulator, silicon on silicon and microelectromechanical areas show that this is a very promising field. Various approaches have been made to ultimately obtain a thin silicon film, each having its own advantages and drawbacks. With the ultra-thin wafer bonding technique developed in this thesis, processing can be made simple, high quality interfaces can be obtained and the cost is low. The attraction force at room temperature is caused by hydrogen bonds between hydroxyl groups and water molecules adsorbed on the two wafer surfaces. The bond is enhanced after annealing through several chemical reactions. Based on bonding experiments in the class 10 cleanroom at NJIT, the current fabrication procedure for ultra-thin wafer bonding has proved to be successful and reproducable. Special treatment is needed in handling ultra-thin wafers throughout the procedure. Experiments show that bondability depends on surface roughness, chemical characteristics and other factors. Number of dust particles, roughness and chemical characteristics of the surface, time and temperature for annealing all affect the formation of voids. Most of the voids can be eliminated through oxidation pre-cleaning, appropriate annealing temperature and improvement on surface smoothness. Measurements show that it is feasible to make a photodetector from a bonded ultra-thin wafer pair with different

doping type and concentration to form a p-n junction. Only a few processing steps are needed.

REFERENCES

[1] George Wallis and Daniel.I.Pomerantz, *J.Appl.Phys.* **40**, 3946(1969)

[2] J.Haisma *et al., Jpn. J.Appl. Phys.* **28**, L725 (1989)

[3] W.P.Maszara, *J.Electrochem. Soc.* **138** 341 (1991)

[4] D.J. Godbey, M.E.Twigg and H.L.Hughes, *J.Electrochem Soc.*, **137** 3219 (1990)

[5] It is commonly known that silicon wafers can not be polished successfully to thickness less than ~200 micrometers using conventional methods. Below this thickness, it is difficult to maintain uniformity. In addition, yield decreases significantly due to wafer cracking. To our knowledge, VSI is the only company which can routinely produce wafers substantially thinner thatn 200 micrometers. Personal conmmunication with Dr. K.R.Farmer, New Jersey Institue of Technology.

[6] M.Kimura,K.Egami, M.Kanamori and T.Hamaguchi, *Appl.Phys.Lett.* **43**, 263 (1983)

[7] J.Tiren, K.E.Bohlin and G.Alestig, *Extended Abstracts Electrochem. Soc. Fall Meeting*, Vol **91-2**, Phoenix, 695 (1991)

[8] R.Sawada, J.Watanabe, H.Nakada and K. Koyabu, *J. Electrochem. Soc.* **138**, 184 (1991)

[9] J.K.Bhagat and D.B.Hicks, *J.Appl.Phys.* **61**, 3118 (1987)

[10] W.P.Maszara, G.Goetz, A Caviglia and J.B.McKitterick, *J. Appl. Phys.* **64**, 4943 (1988)

[11] R.Stengl, K.Y.Ahn and U.Goesele, *Jpn.J.Appl.Phys.* **27**, L2364 (1988)

[12] P.P.Gillis and J.J.Gilman, *J.Appl.Phys.* **35**, 647 (1964)

[13] S.Bengtsson, Ph.D.Dissertation, Dept. of Solid State Electronics, Chalmers University of Technology, Sweden (1991)

[14] R.Stengl, T.Tan and U.Goesel, *Jpn.J.Appl.Phys.* **28**, 1735 (1989)

[15] J.B.Lasky, *Appl.Phys.Lett.* **48**, 78 (1986)

[16] M.Shimbo, K.Furukawa, K.Fukuda and K.Tanzawa, *J.Appl.Phys*, **60**, 2987 (1986)

[17] Y.Bäcklund, K.Hermansson, L.Smith and Ul Lindberg,*in Extended Abstracts Electrochem.Soc.Fall Meeting*, Vol.**91-2**, Phoenix, 682 (1991)

[18] J.Israelachvili, P.McGuiggan and R.Horn, in *Extended Abstracts Electrochem. Soc.Fall Metting*, Vol.**91-2**, Phoenix, 458 (1991)

[19] K.Lungberg, et al, *J.Electrochem.Soc.* **141**, 562 (1994)

[20] G.A.C.M. Spierings and J.Haisma, *Semiconductor Wafer Bonding: Sicence, Technology and Applications*, W.Gosele et al, editors **PV 92-7**, 18, (The Electrochemical Society Proceedings Series, Pennington, NJ, 1992)

[21] According to the bonding mechanism mentined before, additional bonds are added at the interface above 1100°C, leading to stronger bond. On the other hand, high temperature annealing will lead to longer diffusion lenghth, which will limit many applications. We choose anneal at 1100°C to achieve highest strength while limiting deleterious diffusion and tube deterioration effects. The temperature may be varied for different requiement. Personnal communication with Dr. K.R.Farmer, New Jersey Institute of Technology.

[22] V.Lehmann, et al, *Solid State Technology*, **33**, 91 (Apr 1990)

[23] Takao Abe, *Solid State Technology*, **33**, 39 (Nov 1990)

[24] Takao Abe, T.Takei, A.Uchiyama, K.Yoshizawa and Y.Nakazato, *Jpn.J.Appl.Phys.* **29**, L2311 (1990)

[25] John David Vincent, *Fundamentals of Infrared Detector Operation And Testing*, Chap 1, Wiley, New York, 1990

[26] Pallab Bhattacharya, *Semiconductor Optoelectronic Devices*, Chap 8, Prentice Hall, Michigan,1994

[27] M.J.Cooke, *Semiconductor Devices*, Chap 6, Prentice Hall, Britian, 1990

[28] Experimental results provided by Prof. K.R. Farmer, New Jersey Institute of Technology, and N.Perry Cook, Virginia Semiconductor Inc..

[30] S.Wolf and R.N.Tauber, *Silicon Processing for the VLSI Era, Vol 1- Process Technology*,Chap 8, Lattice Press, California, 1986

[31] S.Wolf and R.N.Tauber, *Silicon Processing for the VLSI Era, Vol 1- Process Technology*,Chap 9, Lattice Press, California, 1986

[32] S.M.Sze, *Physics of Semiconductor Devices*,Chapter 13, Wiley, New york, 1981