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ABSTRACT

MBE GROWTH OF $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}/\text{Si}$ HETEROSTRUCTURE SYSTEM

by
JUN LIU

In this work, we grew the $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}/\text{Si}$ (GaAs as buffer layer) by MBE technique. The surface of the buffer layer became microscopically rough as the thickness of the buffer layer increased and the growth mode of GaAs on Si underwent a change from three-dimensional to two-dimensional during the initial growth stage as indicated on the Reflection High Energy Electron Diffraction (RHEED) screen. The Scattering Electron Microscopy (SEM) observation of the etched surface of GaAs on Si showed that the structure of the buffer layer tended to be poly-crystalline and it was possible that a predominant orientation occurred at next step of the epitaxy of $\text{In}_x\text{Ga}_{1-x}\text{As}$. The role of contaminations such as C and SiO_2 as crystallization centers was revealed by Photoluminescence (PL).

SEM study of interfaces of $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}/\text{Si}$ showed that most of the threading dislocations propagated through the growing layer without changing their running direction which was close to the normal to the plane of the layer-by-layer growth for the large lattice mismatched system. From cross-hatch, we also obtained the linear dislocation densities along two $\langle 110 \rangle$ directions, 200cm^{-1} and 1200cm^{-1} respectively. In addition, the SEM topographies of the epitaxial growth of $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$ on tilted and untilted Si substrates indicated that in the case of using tilted substrates, the island growth would not be isotropic and the islands tend to be elongated running parallel to the steps.

**MBE GROWTH OF $\text{In}_x\text{Ga}_{1-x}\text{As}$ / GaAs/ Si
HETEROSTRUCTURE SYSTEM**

by
Jun Liu

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A Thesis
Submitted to the Faculty of
New Jersey Institute of Technology
in Partial Fulfillment of the Requirements for the Degree of
Master of Science in Applied Physics

Department of Physics

October 1994

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APPROVAL PAGE

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This thesis is dedicated to
my wife and daughter

ACKNOWLEDGMENT

The author wishes to express his sincere gratitude to his advisor, Professor Ken K. Chin, for his guidance, support and encouragement throughout this research.

Special thanks to Professor Guanhua Feng , the thesis work would not be completed without his idea, his help and guidance in the experiment and analyses.

The author would like to thank Mr. Abhay Joshi for his support on this project.

The author appreciates Professor Yuan Yan in PL data acquisition.

Finally, the author likes to thank all his friends in the Physics Department for their kindness and support.

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CHAPTER 1

INTRODUCTION

1.1 The Growth of Heterostructure System

Molecular beam epitaxial (MBE) growth of various lattice-mismatched semiconductor materials such as InSb/ GaAs, GaAs/ Si and InGaAs/GaAs/Si has been well developed [1-4]. These developments have created new dimensions in the field of material sciences, solid state electronics and monolithic integration of optoelectronic integrated circuits(OPICs). Among those, the lattice mismatched $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}/\text{Si}$ with x from 0 to 1 may be one of the most attractive material systems.

The $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ can cover a wide range of lattice mismatch up to 7% with respect to the GaAs substrate, offering a good material system for the study of heteroepitaxy. In addition the growth technique[5-6] of $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ has improved. The results on formation, interaction and propagation of misfit dislocations[7-8] in the heterointerfaces have been reported. It is known that there is lattice constant difference between $\text{In}_x\text{Ga}_{1-x}\text{As}$ and GaAs above which there will result a lot of dislocations on the surface of the growth film. In this lattice-mismatched system, high quality strained layers can be grown provided that their thickness are below the critical layer thickness (CLT). Above this thickness the strain is relieved by the formation of the misfit dislocations. For thickness above CLT, The quality of the epilayers is degraded, affecting the device performance. Generally speaking, dislocations are related to strain relaxation. Traditional methods to treat the strain relaxation process of the heteroepitaxy are based on a two-dimensional growth mode [9-10], that is, during the initial growth stage, the lattice constant of epilayer parallel to the growth surface is forced to follow the

substrate until reaching a CLT. Beyond this, the layer is relaxed by the generation of misfit dislocations at the interface and the cross-hatch patterns at the free surface can be directly observed by optical microscopy [5]. But, the two-dimensional mode is suitable only for small x ($\varepsilon < 2\%$). For large lattice-mismatched system, particularly $x > 0.28$ ($\varepsilon > 2\%$), $\text{In}_x\text{Ga}_{1-x}\text{As}$ undergoes a transition from a two-dimension to three-dimension island growth mode [11-13] before the generation of dislocation. The coalescence of the islands during the epitaxy has led to the introduction of undesired threading dislocations which transmit through the $\text{In}_x\text{Ga}_{1-x}\text{As}$ epilayer up to free surface. The 3D strain relaxation mode is very complicated. Theoretical curves [6] were calculated using the heterogeneous force equilibrium mode of Matthews and Blakeslee for a single heterointerface and homogeneous energy equilibrium mode of People and Bean.

Many experiments from X-ray diffraction (XRD) and transmission electron microscopy (TEM) have showed that the $\text{In}_x\text{Ga}_{1-x}\text{As}$ material quality degraded as x increased from 0 to 0.5, whereas increased from 0.5 to 1, the materials recovered in spite of more lattice mismatch [14]. So, it has been suggested that the lattice mismatch is not only the factor that determined the epilayer qualities. Compound and alloy materials also played an important role.

As regards growth conditions, substrate temperature is generally considered an important factor to get high quality epilayer. Since the In-As binding energy is lower than that of Ga-As, the $\text{In}_x\text{Ga}_{1-x}\text{As}$ with large X required a lower growth temperature and is always kept below 550°C or indium atoms tend to aggregate and desorb [15-16].

The growth of GaAs/ Si, compared to $\text{In}_x\text{Ga}_{1-x}\text{As}/ \text{GaAs}$, is more difficult because of three reasons as below: (1).anti-phase domain; (2).lattice mismatch; (3).different thermal expansion coefficient. A few novel techniques such as choosing tilted, or porous, or sawtooth-patterned Si substrates were used to obtain

improved quality of growth films.

So, the structure of $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}/\text{Si}$ system needs further studying due to the potential application of heterostructure devices.

1.2 Application of $\text{In}_x\text{Ga}_{1-x}\text{As}$ System

OEICs that combine photodetectors with amplifier and signal processing circuits on the same substrate have the advantage of reducing the parasitic reactance between the optical detecting element and the electronic signal processing circuit thus improving both performance and reliability[17,20,21]. Of particular interest is the monolithic integration of silicon advanced electronics with $\text{In}_x\text{Ga}_{1-x}\text{As}$ optoelectronic modules for broad-band fiber-optic communications and optical processing in the 1.3 to 1.6 μm optical wavelength range where the transmission of the most widely used quartz optical fiber peaks. InGaAs photodiodes have already been demonstrated on bulk GaAs substrates as well as on GaAs/ Si structure[18]. High quantum efficiency InGaAs p-i-n photodetectors with an InP barrier-enhancement layer have also been fabricated using the low -pressure metalorganic chemical vapor deposition (LPMOCVD) technique[19].

In order to realize the integration of InGaAs optoelectronic devices with silicon technology, high quality InGaAs layers epitaxially grown on silicon substrates are required. However, due to the large lattice mismatch between $\text{In}_x\text{Ga}_{1-x}\text{As}$ and supporting silicon substrate and the differences in thermal expansion coefficients between silicon and the Group III-IV compounds, high quality InGaAs/ Si structures with low defect density and low levels of threading dislocations are very difficult to obtain. On the other hand, GaAs has only 4% lattice mismatch with silicon, and, by using two-dimensional growth techniques, threading dislocations, stacking faults, and antiphase domain boundaries in MBE-grown GaAs/ Si structures can be greatly reduced.

1.3 The Objective of the Thesis

In this thesis, we grew the $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}/\text{Si}$ (GaAs as buffer layer) by MBE technique. The initial stage of the buffer layer growth was studied by Reflection High Energy Electron Diffraction (RHEED). The Scanning Electron Microscopy (SEM) image of (Etch Pit Density)EPD showed the quality and the structure of GaAs buffer layer. Photoluminescence (PL) spectrum were used to reveal the effects of contaminations such as C and SiO_2 on the surface of the substrates during the growth of the buffer layers. The SEM studies of cross-hatches and interfaces of $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}/\text{Si}$ with $X=0.5, 1.0$ would show the generation of the strain, the density and formation of the dislocation, and the link of the epilayer quality and the initial strain relaxation process. In addition, I investigate the quality difference of growth on untilted and tilted Si substrates from SEM topographies. In a later chapter, we present a theoretical explanation of generation mechanism of dislocations by simple modes.

CHAPTER 2

EXPERIMENT

2.1 Substrate Preparation

All substrates have to be cleaned before MBE growth. The substrates were initially solvent degreased in acetone. (1). GaAs substrates: Surface oxides on the substrates were removed by a quick etching in concentrated HCl (1:1 with water). Mechanical damage resulting from polishing was removed by etching in a mixture of H_2SO_4 : H_2O : H_2O_2 (4:1:1). The substrates were then rinsed in deionized water and blown dry with nitrogen gas. We mounted substrates on molybdenum sample holder with indium. Prior to growth, oxides had been desorbed at 600°C under an As flux until the diffraction patterns on the screen of RHEED showed only the main lines and additional lines between them; (2). Si substrates: We used two kinds of silicon substrates, tilted and untilted. The former does not need cleaning because they have been prepared by manufacturer. The others were put in concentrated HF (1:1 with water) for several seconds to remove oxides on the surface. Then, they were dried, and oxide residues were desorbed at 850°C under Ga flux.

2.2 The Growth of $\text{In}_x\text{Ga}_{1-x}\text{As}$ / GaAs/ Si by MBE

2.2.1 Flux Calibration

The flux calibration which determines X (ratio of In to Ga in growth films) during the growth of the epi-heterostructure system should be measured at first. The fluxes of Ga and In were respectively measured at substrate position as a function of the temperature of the cells holding solid sources. Meanwhile, the manipulator was placed at its epitaxy position, by mechanically adjusting the X, Y and Z

vernier knobs. The position was checked by looking through the viewport located on the evaporation flange and corrected (rotated) by using the manipulator handle. This position results in the best uniformity epi-films. The fluxes of Ga and As were recorded one after the other by the Bayard-Alpert gauge in epi-position. The measured curves of Ga and As were showed as Figure 2.1.

2.2.2 The Growth Rate of Epilayer

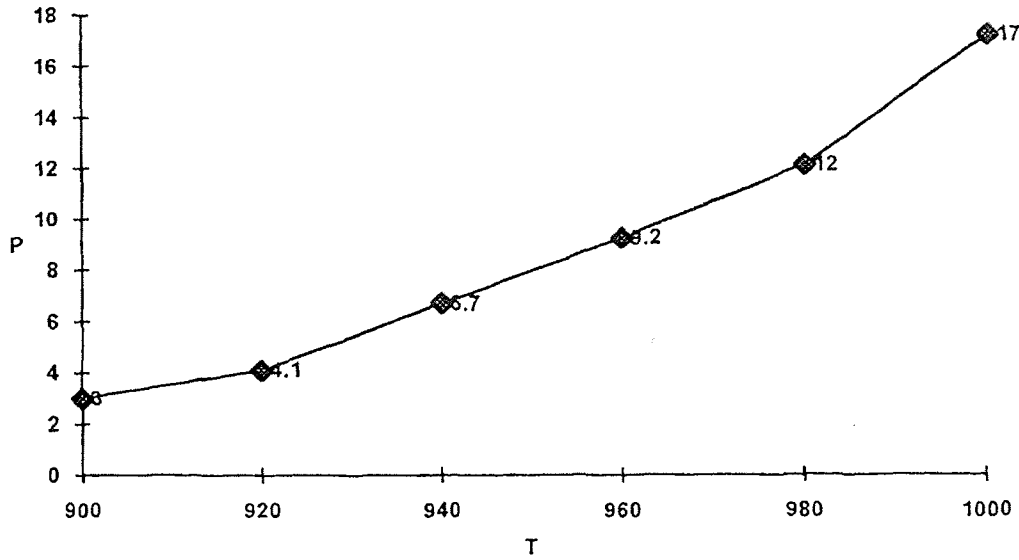
The growth rate of epilayer is one of the most important growth conditions. It was measured by RHEED during the initial growth stage. The frequency of the intensity oscillation of the main line centered on the screen of RHEED indicates how many molecular layers (ML) per unit time are deposited on substrate. The initial growth rate from RHEED is 0.7ML/sec.. The average growth rate of $\text{In}_x\text{Ga}_{1-x}\text{As}$ for whole growth process was obtained by α -step instrument and it is about $1\mu\text{m}$ per hour.

2.2.3 The Substrate Temperature

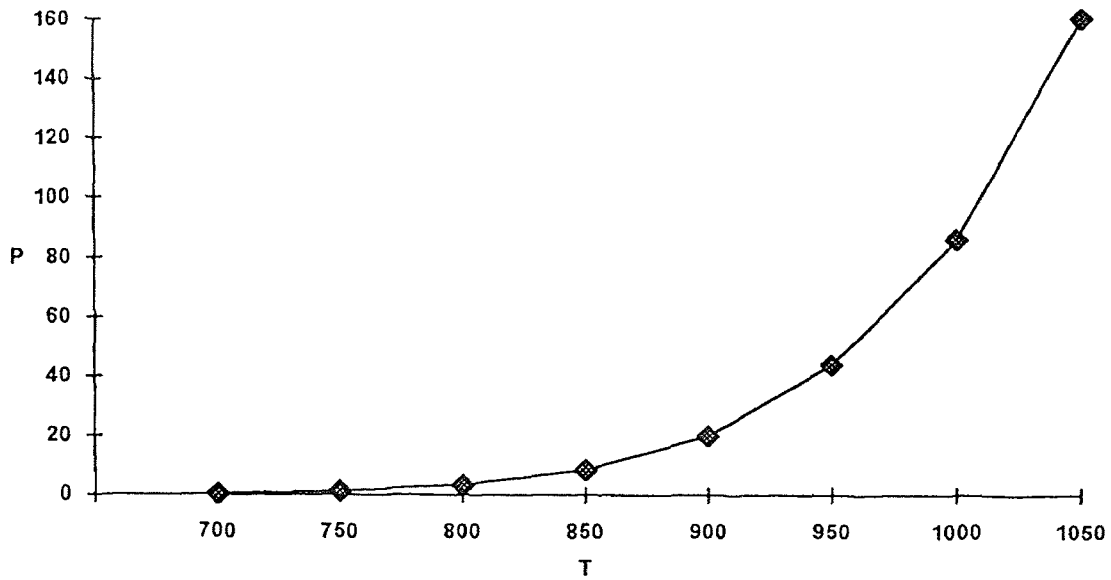
The substrate temperature T_s is a critical parameter in the lattice relaxation mechanism. It must be optimized. Temperatures measured with the thermocouple can be somewhat different due to the position of substrates, the nature of the bonding and the inner surface of the well on the molybdenum block. It is necessary to wait for the temperature to stabilize ($\pm 1^\circ\text{C}$ around the displayed temperature) before starting with the epitaxial growth.

2.2.4 The Growth Procedure of $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}/\text{Si}$

The cleaned wafers were mounted on a molybdenum substrate holder with indium, and loaded into MBE chamber. The background pressure was lowered to less than 10^{-10} torr. Before the starting of the growth, the substrates were heated to a

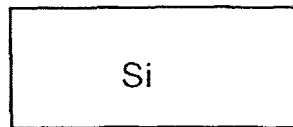


(a). The Pressure at Epitaxial Position as a Function of Source Temperature for Ga ($P \times 10^{-7}$ Torr, $T \times 1K$)

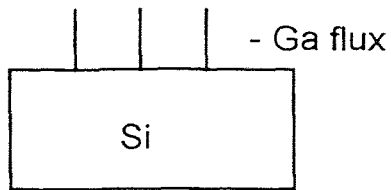


(b). The Pressure at Epitaxial Position a Function of the Source Temperature for In ($P \times 10^{-7}$ Torr, $T \times 1K$)

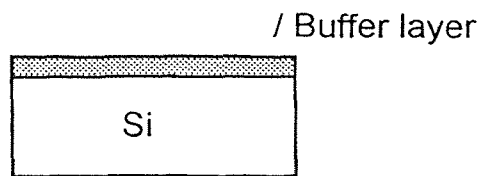
Figure 2.1 Calibration of Fluxes of Ga and In



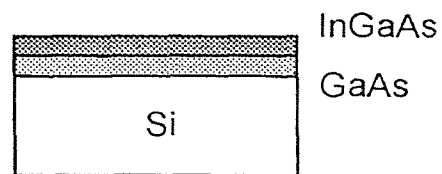
(1). Chemical cleaning



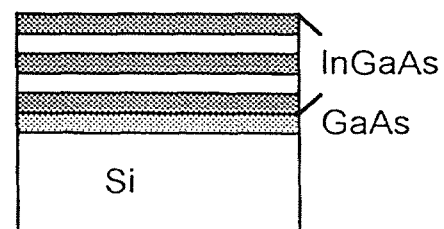
(2). Desorbing oxides



(3). Growth of buffer layer



(4). Growth of InGaAs



(5). Gradient InGaAs heterostructure
with x ranging from 0 to 0.53

Figure 2.2 The Flow Chart of the Growth of $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}/\text{Si}$

temperature of 850⁰C and kept there under Ga flux for 10 min so that the passivating oxide layer on substrate surface was desorbed as indicated on the screen of the RHEED. The substrate temperature was decreased to 350-380⁰C to accelerate nucleation on the surface of the substrate. Finally, the temperature was lowered to the desired growth temperature in the range between 550⁰C and 580⁰C. We fixed source temperatures of Ga and As at 940⁰C and 240⁰C respectively and changed the source temperature of In to get the samples with different x values.

2.3 MBE System and Analysis Instruments

The standard RIBER MBE 32 system as shown in Figure 2.3 which was used to fabricate single crystal III-V thin film samples combines chambers for substrate loading, epitaxy and RHEED analysis during epitaxial growth stage. It consists of an epitaxy chamber, a loading module, a heat treatment module, a transfer module and their related pumping system including rough pumping (a dry diaphragm pump of Model PSM2 and three sorption pumps of Model PA 10L) and secondary pumping system (ion pumps of Model PI and titanium sublimators of Model PF 6). Bayard-Alpert triode gauges (Model JBA) permit pressure readings in each section.

The epitaxy chamber, where the growth is carried out, consists of three main parts: (1) The evaporation flange bears the various cells housing the materials to be evaporated, and is equipped with two liquid nitrogen-cooled panels. Each cell has its own heating power supply (temperature) with computer-controlled regulation. The cell shutter motors can also be computer-controlled; (2) The manipulator that houses the substrates permits its orientation and continuously rotates during epitaxy to improve uniformity. It features an inner fixed furnace to heat the substrates and a Bayard-Albert triode gauge to measure fluxes; (3) The

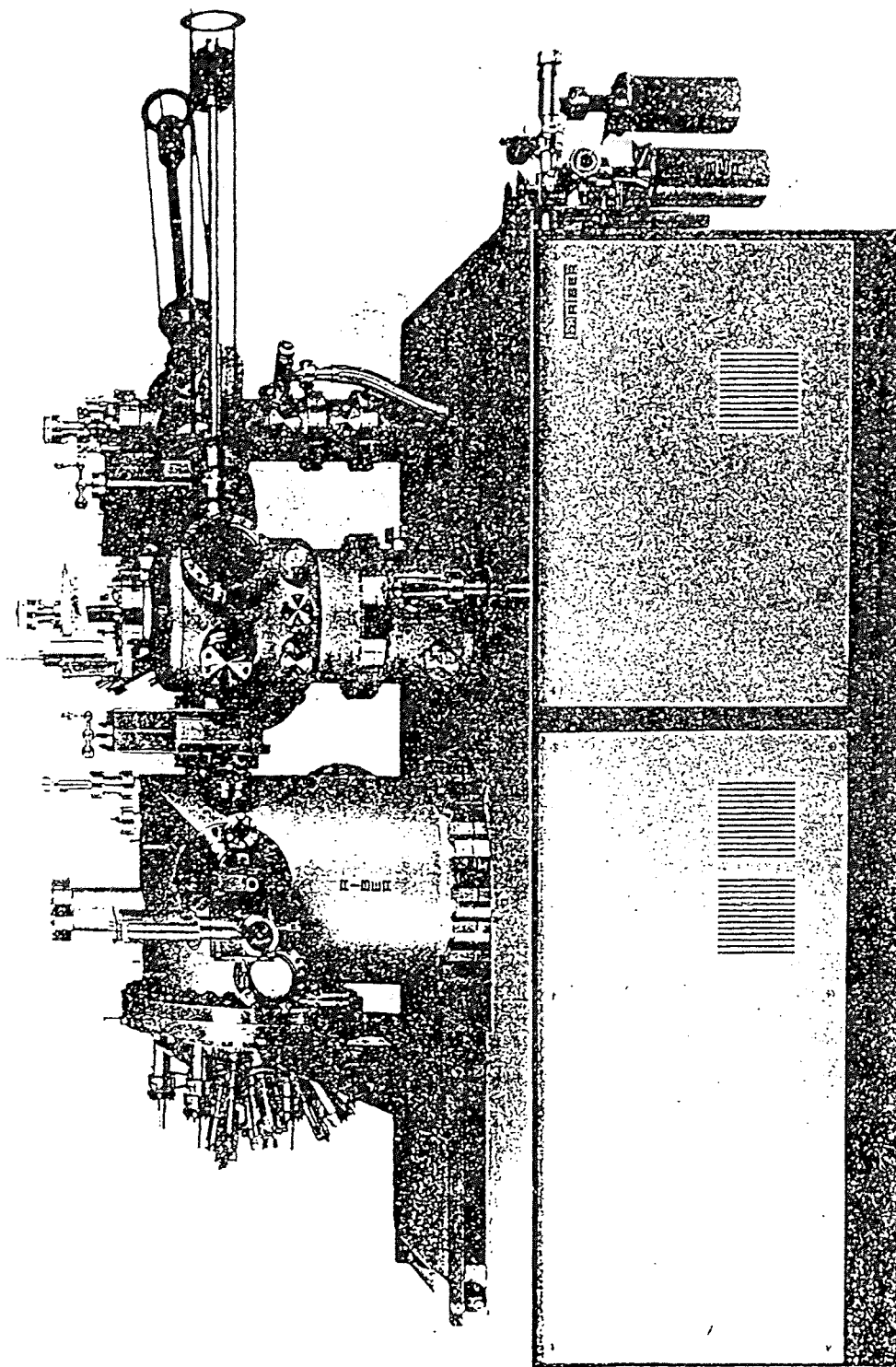


Figure 2.3 RIBER MBE System

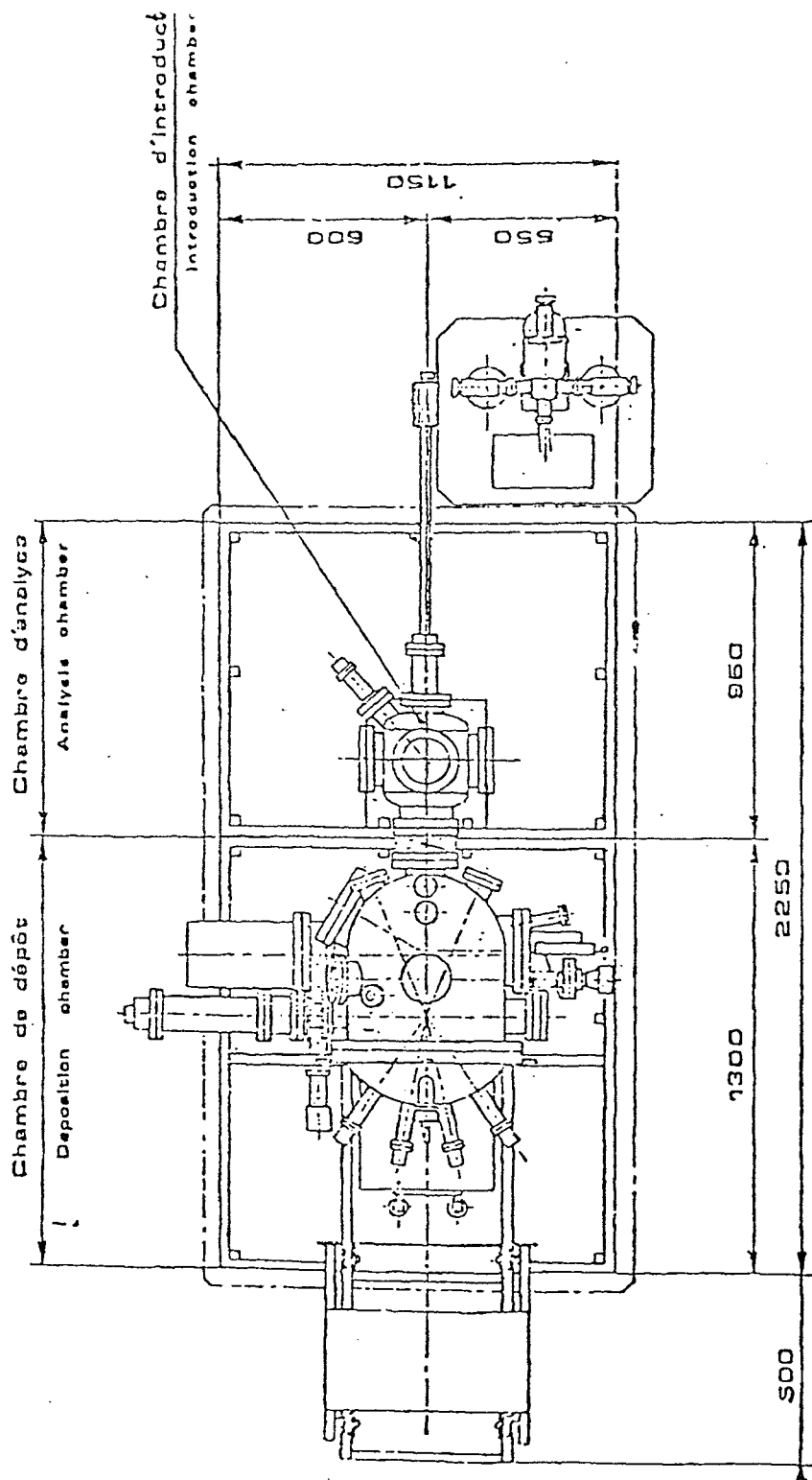


Figure 2.4 Dimension of RIBER MBE System

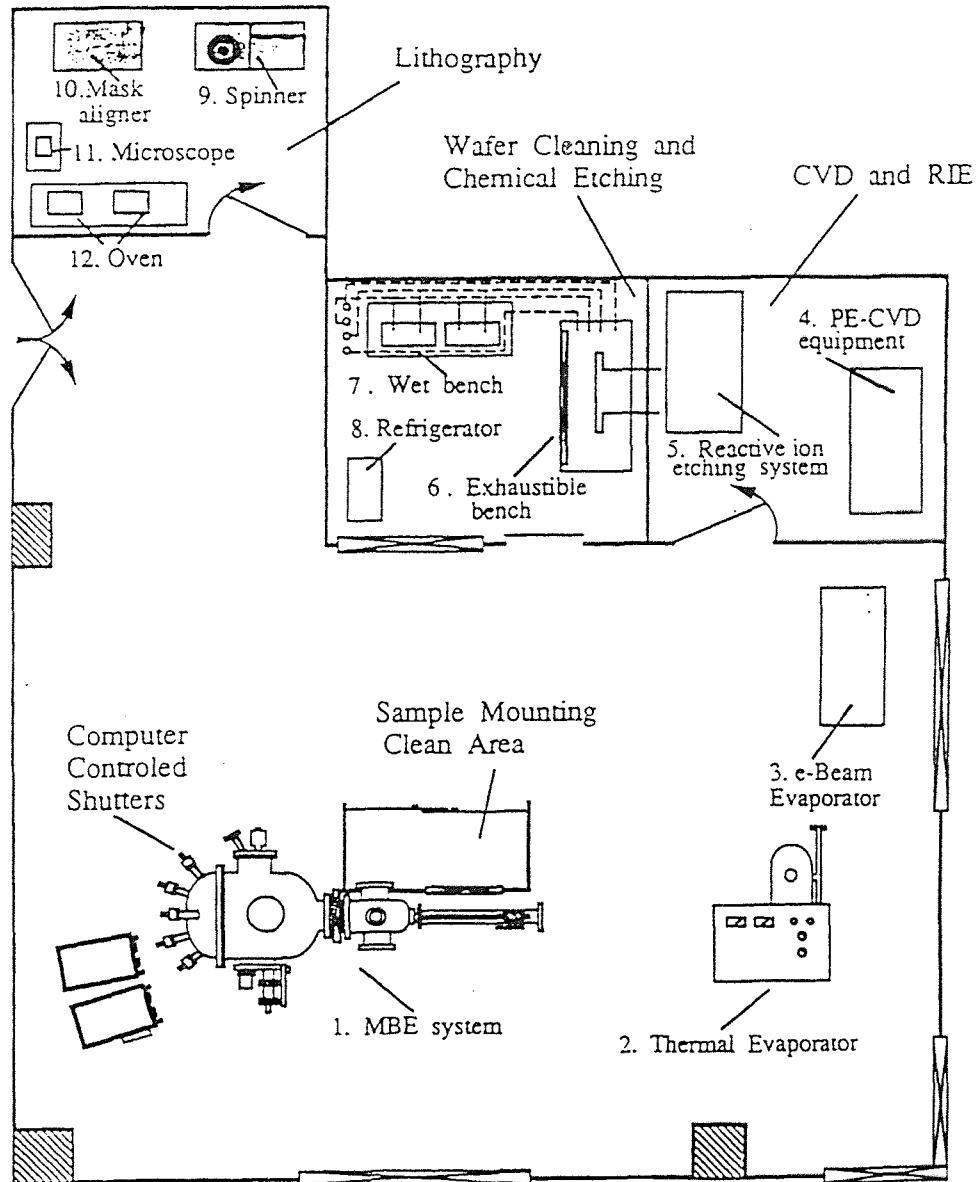


Figure 2.5 III-V Device Process Laboratory in Which the Samples Were Prepared

analysis instrument of this MBE system is a RHEED electron gun (Model CER606) to display on a fluorescent screen the crystallographic correctness when starting the growth. Figure 2.3, Figure 2.4 and Figure 2.5 show MBE system and III-V Device Process Laboratory.

For PL measurements, an Argon laser pump source and a photomultiplier detector were used. The PL spectra were recorded with a computer-controlled data-acquisition system

which included a grating spectrometer and a lockin amplifier. The topographies and cross-hatches were obtained by a SEM AMRAY 1600 TURBO system.

CHAPTER 3

EXPERIMENTAL RESULTS AND DISCUSSIONS

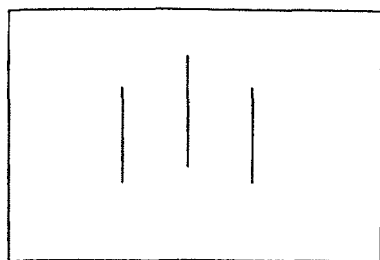
3.1 Investigation of GaAs Buffer Layer in InGaAs/GaAs/Si

3.1.1 RHEED Analysis of GaAs Buffer Layer

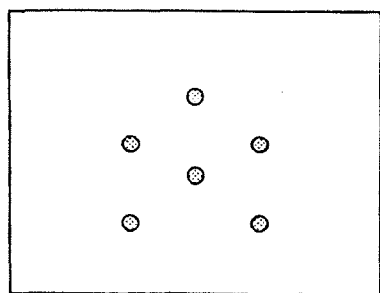
RHEED patterns generated by GaAs grown on the Si substrate were observed during the initial growth stage of the GaAs buffer layer. During the first ten minutes when substrate temperature was kept at 350°C under the fluxes of Ga and As, the RHEED pattern of the Si substrate surface reconstruction disappeared. This indicated a three-dimensional nucleation of GaAs on the surface of the Si substrate. With increased substrate temperature, island growth with small grain size would occur. When substrate temperature was raised to 610°C while exposed to the arsenic beam, half-order streaks appeared between main streaks. This indicated that the GaAs growth mode was changed from three-dimensional nucleation to two-dimensional growth epitaxy. Meanwhile, an oscillation of the main line centered on the screen of RHEED occurred and its frequency indicated a growth rate of about 0.7ML/sec during the initial growth stage when the source temperatures of Ga and As were 940°C and 240°C respectively. As the thickness of GaAs buffer layer continued to increase to 2000Å, the main streaks and half-order streaks became indistinct and disappeared finally. We may consider that the surface of buffer layer was microscopically rough at that time, and a lot of dislocations on the surface of GaAs were formed due to release of elastic energy above CLT. The quality of the buffer layer was improved when it was kept at 610°C under As flux for 10 minutes.

In our work, tilted Si substrates were used to improve the quality of buffer

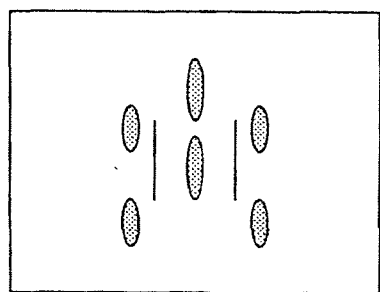
layers and epilayers . From the 4% lattice mismatch between buffer layer GaAs and Si , one dislocation with Burgers vectors which lie in the substrate plane for every 25 atomic planes is required to accommodate the misfit. The steps occur in the surface due to the discrete atomic nature of the crystal [31]. The steps in tilted orientations of Si run along $\langle 011 \rangle$ directions preferentially, and thus in orientations tilted off toward $\langle 011 \rangle$, the dislocations mentioned above are only preferentially nucleated along one direction. This will reduce the dislocation density.



After desorbing oxides under Ga flux at 850C for 10 min



Nucleation at 380C



During the initial growth of the buffer layer at 610C

Figure 3.1 RHEED Observation During Growth of GaAs on Si

3.1.2 Microscopic Observation of Etched Surface of GaAs/Si

The surface morphology of etched GaAs/Si was observed by microscopy. A+B etched GaAs on Si was shown in Figure 3.2. The etch pit density (EPD) was counted based on a photograph taken under optical microscope. It was about $0.6 \times 10^6 \text{ cm}^{-2}$. We know the quality of GaAs buffer layer is extremely sensitive to the microstructure of the substrate Si. The tilted Si wafer was used to decrease mismatch between GaAs and Si so that the dislocation density on the surface of the buffer layer was reduced greatly. The shapes of etch pits included triangle and square which were characterized on (111) plane and (110) plane. The co-existence of two shapes of etch pits indicated that the buffer layer tended to become polycrystal as the thickness of the GaAs buffer layer increased.

3.1.3 PL Study of GaAs on Si

It is well known that there a layer about 20\AA thick of natural SiO_2 on Si. Oxides and other contaminants tend to induce polycrystalline and/or amorphous growth of the GaAs buffer layer because the impurities can produce crystallization centers. On the other hand, the average size of crystal grains will be small if there are a lot of oxides on the surface of Si substrates. This will make the growth of high quality $\text{In}_x\text{Ga}_{1-x}\text{As}$ epilayer impossible in next step.

The PL spectrum at 10K obtained from the buffer layer GaAs on untilted Si is shown in Figure 3.3. In the spectrum, it reveals a wide and weak peak of 1.48eV. It is well known that the GaAs is under biaxial tension generated during cooling from the growth temperature due to the different thermal expansion coefficient between GaAs and Si. Therefore, for the appearance of the peak in this buffer layer, one should consider a possible strain-induced shift of the PL peak. Furthermore, the nature of observed peak must be understood. The peak becomes

wider due to misfit dislocations formed during the growth of epilayer the surface effect of contamination. To improve the quality of the buffer layer, we can use the following methods: (1) complete removal of oxides and other contaminations on substrate surface by heating up the Si substrate under UHV (ultrahigh vacuum) condition in the MBE chamber up to 850⁰C; (2) annihilation of dislocations by increasing the growth rate and accelerating the formation of single domains during the growth; (3) enhancement of surface migration of adatoms on the growth front [4].

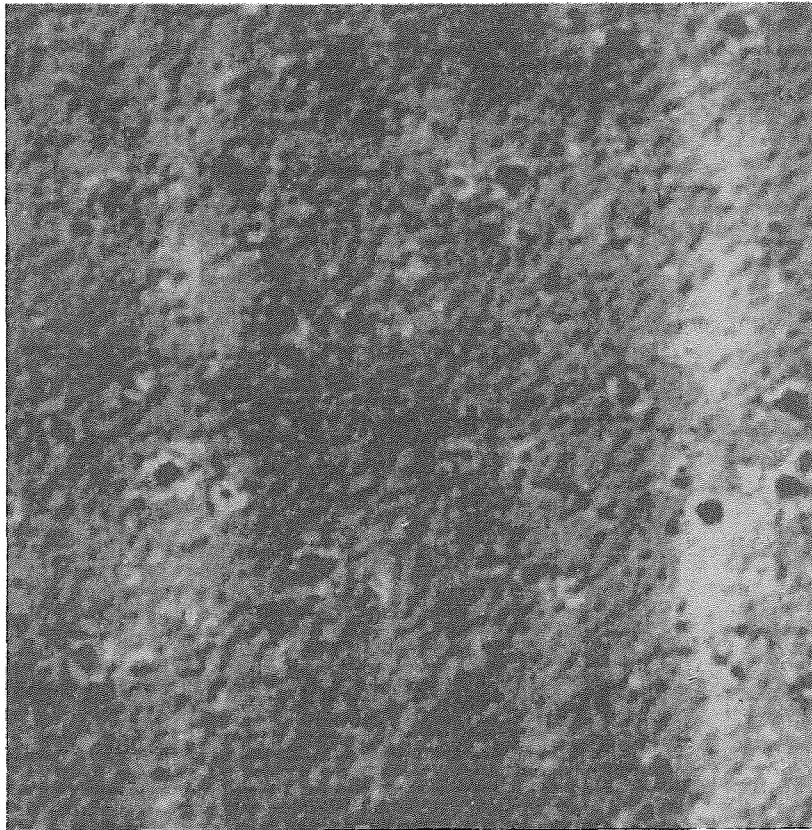


Figure 3.2 Surface Morphology of Etched GaAs on Si

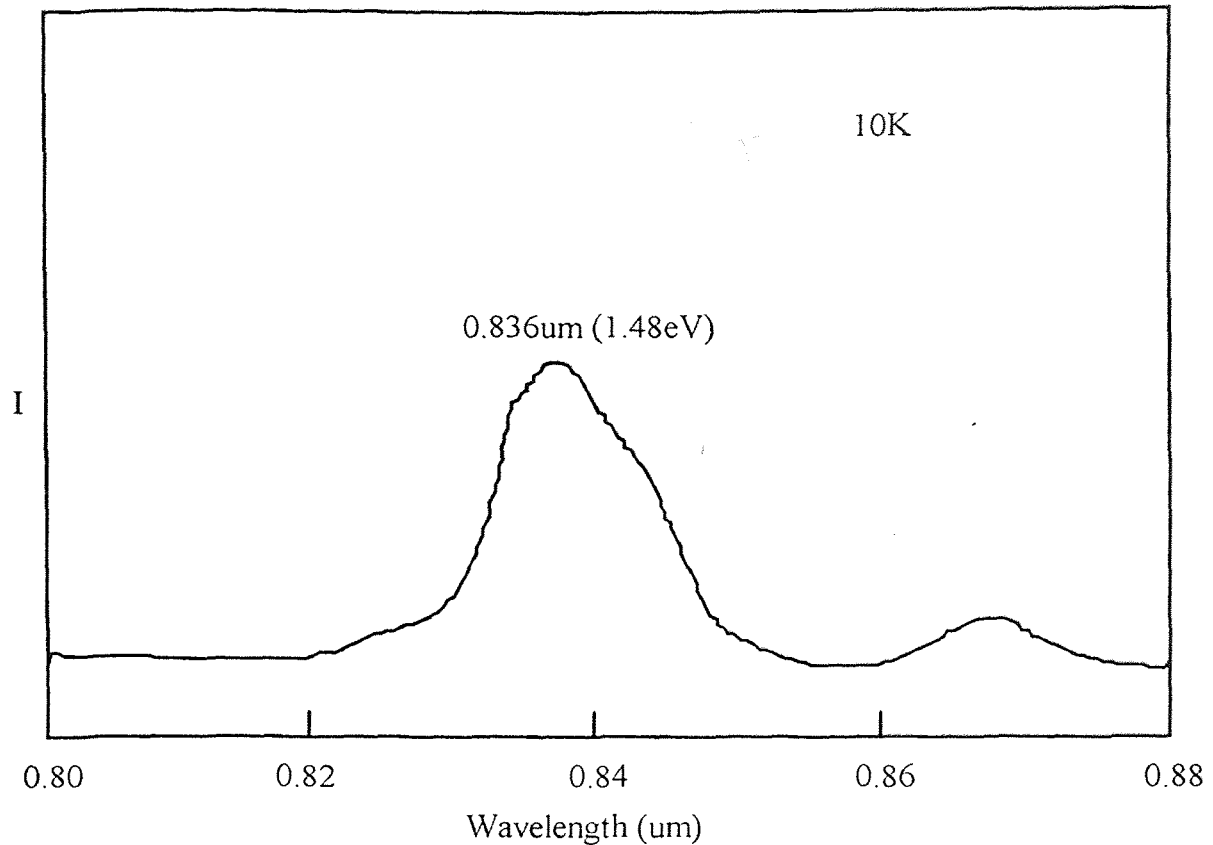
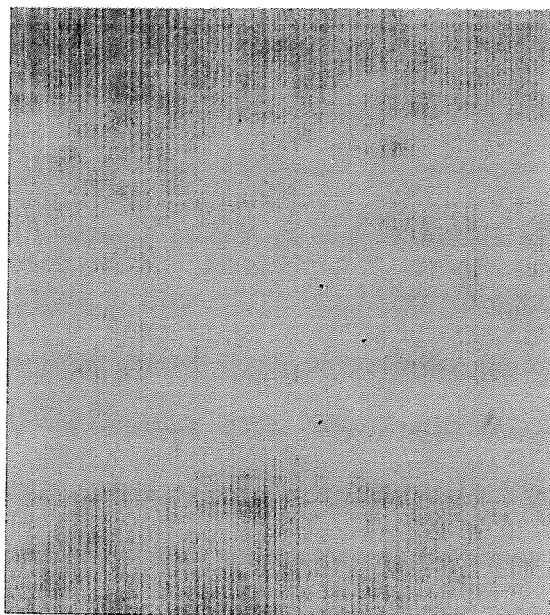


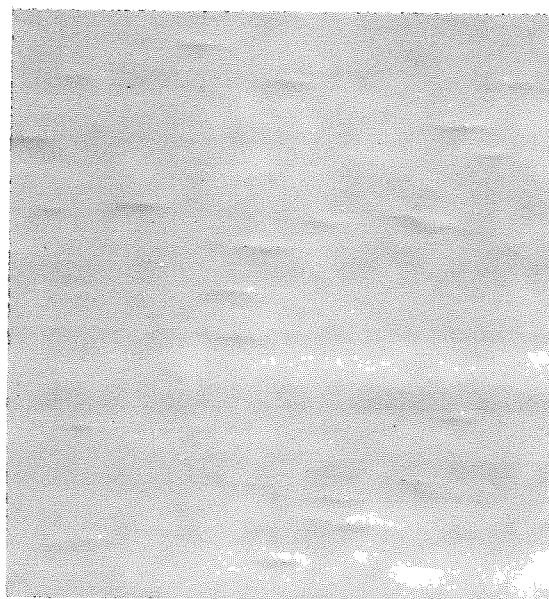
Figure. 3.3 Low Temperature PL Spectrum of GaAs/Si

3.2 Microscopic Cross-hatch Analysis of $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}/\text{Si}$

Figures 3.4(a) and 3.4(b) were the results of microscopic cross-hatch image and topograph obtained from 5000\AA thick $\text{In}_{0.3}\text{Ga}_{0.7}\text{As}$ and InAs epilayers which were grown on the large area Si substrates at 560°C and from a 2000\AA thick GaAs buffer layer which was grown between the InGaAs (or InAs) and Si at 610°C . The epilayer thickness exceeded the critical layer thickness so the density of dislocations at the interface in these samples was high. The effect of the growth area will be discussed later in this Chapter and Chapter 4. The linear interface dislocation density was defined as the average number of misfit dislocations crossed by a 1cm long line drawn perpendicular to the line direction of a set of parallel interface dislocations [18]. In other words, the linear interface dislocation



(a)



(b)

Figure 3.4 (a) Microscopic Cross-hatch of $\text{In}_{0.3}\text{Ga}_{0.7}\text{As}$;
(b) Microscopic Topography of InAs

density is the inverse of the dislocation spacing and has units of cm^{-1} . The features observed from Figure 3.4(a) were the following: (1) There was a difference in linear interface dislocation densities along the two $\langle 110 \rangle$ directions; (2) The values were 200cm^{-1} and 1200cm^{-1} respectively, which is better than reported values[18]. A sample grown on a microscopically unlimited large area with such low linear interface dislocation densities was considered high quality.

Surface ridges on mismatched epitaxial material are frequently observed, but their origin is poorly understood [32]. We found many ridges along $\langle 110 \rangle$ directions on the surface of InAs/GaAs/Si indicated in Figure 3.4(b). No parallel dislocation lines like Figure 3.4(a) existed on the surface of the heterostructure system. The bigger x value (atomic ratio of In to Ga), the more mismatched the lattices of the $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}/\text{Si}$ should be. The quality of $\text{In}_x\text{Ga}_{1-x}\text{As}$ with a big x or $x=1$ should have degraded. To explain this contradiction, consider that defects at internal interface can affect the epilayer in two ways. First, the dislocations that glide to the interface leave surface steps behind. These steps can act as preferred nucleation sites during epitaxial growth. Second, it has been shown that dislocations with Burgers vectors completely in the interface plane can still act as preferred nucleation sites, presumably because of the compressive and tensile stresses present around the dislocation. On the other hand, bonding energy of In-As is lower than that of Ga-As. It is reasonable to assume that more broken bonds were formed for InAs/GaAs/Si because of lattice vibrations from thermal energy during growth. Therefore the quality of $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}/\text{Si}$ was improved as x increased. But, we are still not sure that all of the strain is relieved by dislocations and maybe elastic strain effects are still present in the epilayer. This will result in poor electrical properties if $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}/\text{Si}$ with big x is used for devices.

3.3 SEM Topographies of Epilayers on Tilted and Untilted Si Substrates

Figure 3.5 and 3.6 show SEM topographies of the epitaxial growth of $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$ on tilted and untilted Si substrates. The thicknesses of the epilayer and the buffer layer are $1\mu\text{m}$ and 2000\AA respectively. The appearance of valleys was observed from the SEM surface morphologies shown in Figure 3.6. In earlier studies, the valleys appeared where clusters of threading dislocations had reached the surface of the film. As can be seen in Figure 3.5 and 3.6, epilayers grown on (100) Si untilted and 3.5° tilted toward [110] have different appearance. In the surface of the latter, the valleys are more elongated.

Studies of initial phases of the buffer layer on Si have shown that initially, at growth temperatures between $350 - 380^\circ\text{C}$, the growth is three-dimensional. Steps in the substrate surface will influence the size of nuclei. The dislocations with Burgers vector which lie in the substrate plane are generated at the edges of these nuclei such that when they coalesce, clusters of dislocations may be formed. Most likely, this explains the morphological features observed in these films. The appearance of a valley along with a dislocation cluster is evidence of a point where two or more islands coalesced. The valley arises from the fact that the growth is not planar initially.

In the presence of steps, the atomic diffusivity will be lower. Therefore with steps, there would be a large number of small islands, whereas without steps, the islands would tend to be larger and fewer. In the case of a tilt toward [110], where steps occur in one direction, the islands would not grow isotropically. The islands tend to be elongated, with the elongation running parallel to the steps. However, in the case of untilt, the islands would grow isotropically. This is exactly what is observed in Figure 3.5 and 3.6.

It was also found from Figure 3.5 and 3.6 that the surface morphologies of

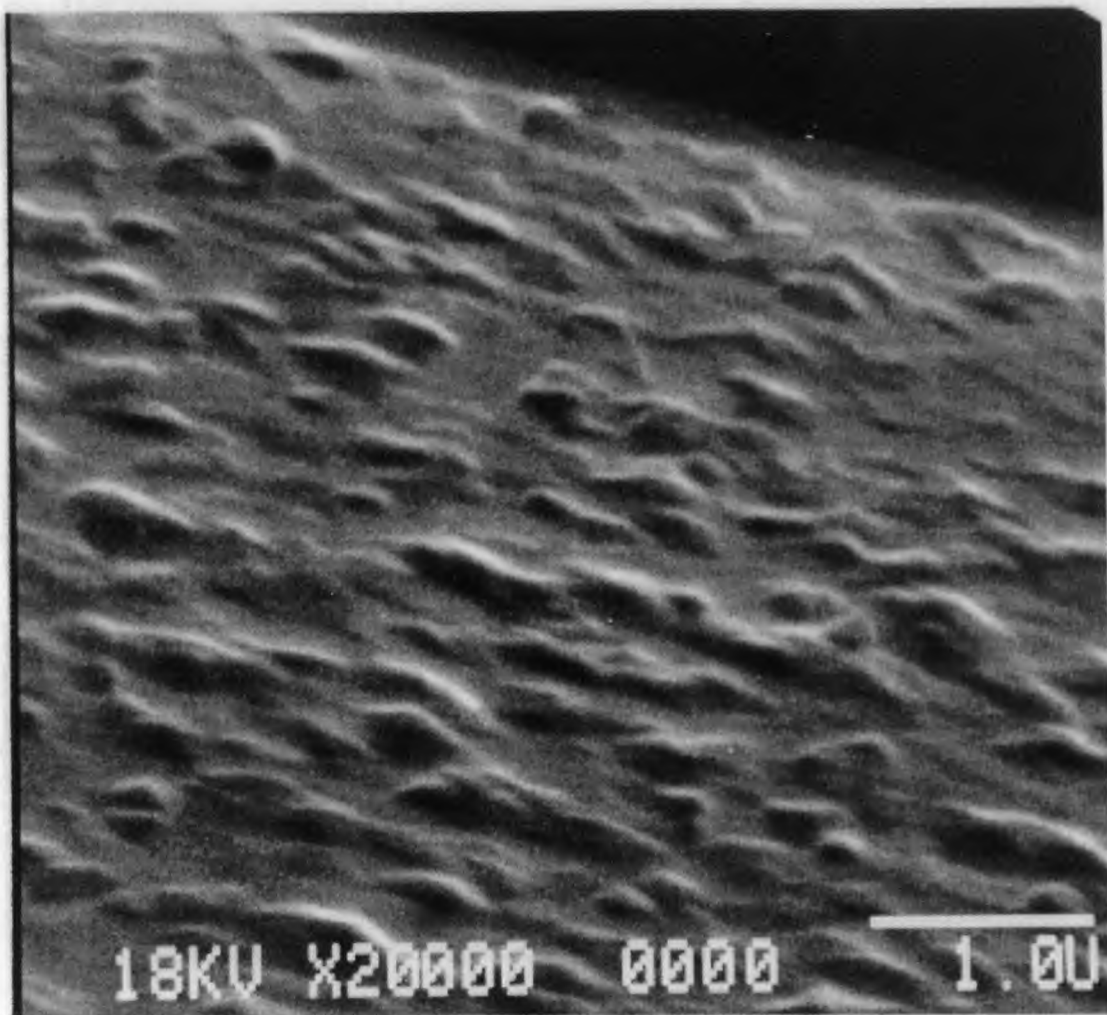


Figure 3.5 SEM Topography of the Epilayer In_{0.5}Ga_{0.5}As on Tilted Si

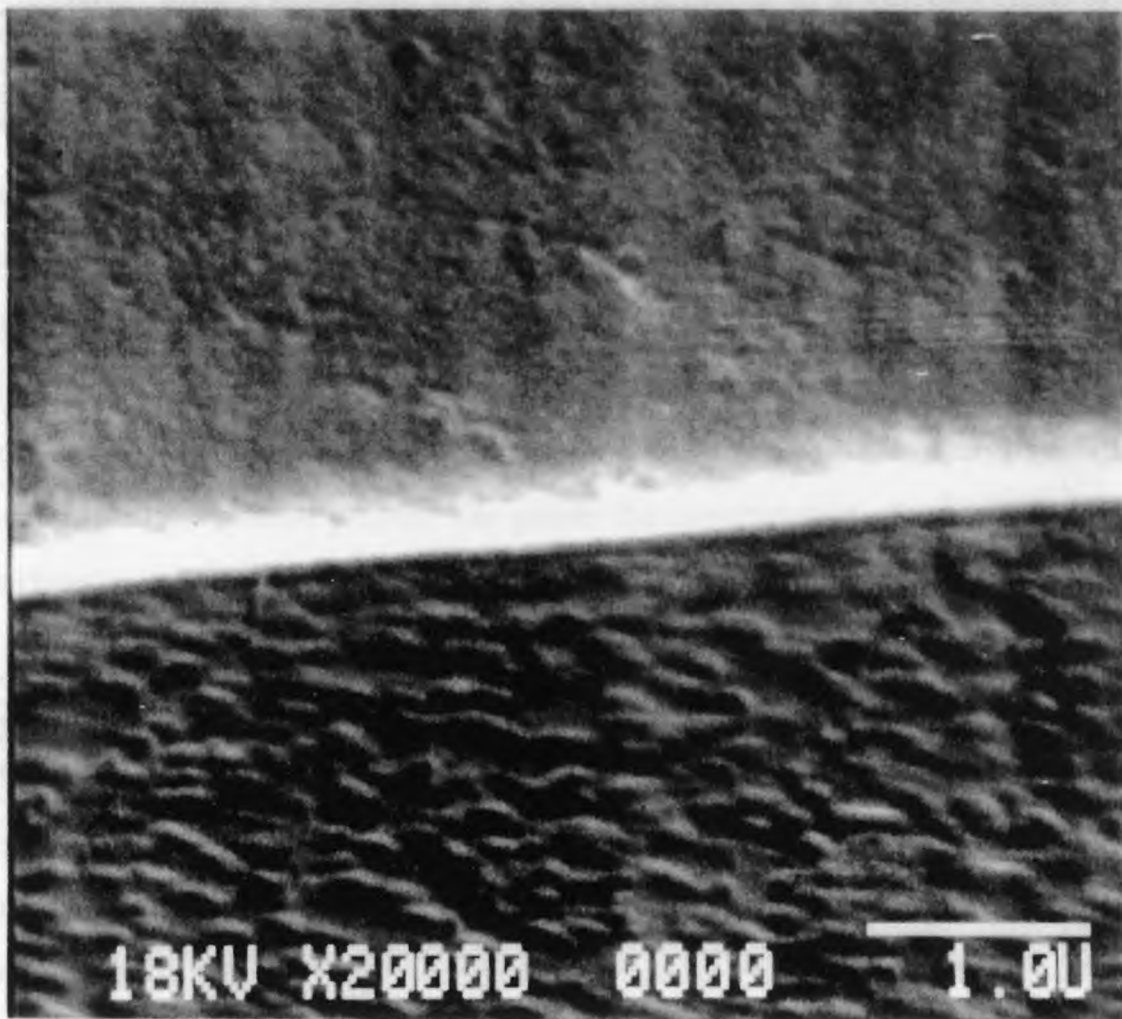


Figure 3.6 SEM Topography of Epilayer $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$ on Untilted Si

epilayers on Si have a slight texture. We estimate that the surface roughness has been typically about 100\AA . If further improvement is necessary for semiconductor processing, growth techniques such as the deposition of an amorphous GaAs layer on the buffer layer could be used to provide a much smoother surface.

In addition, we have investigated the effect of natural SiO_2 on the growth of $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$ and buffer layer. A smoother surface of epilayer was observed if the natural SiO_2 and other contamination such as carbon on the surface of the substrates had not been removed before the MBE epitaxial growth. The roughness difference of epilayers on cleaned and uncleaned surfaces of the substrates is due to that the oxide and the other contamination will produce a lot of crystallization centers during epitaxial growth. The greater the concentration of impurities on the surface and in the growth films, the smaller the size of the crystal grain.

3.4 SEM Study of Interfaces of $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}/\text{Si}$

Figure 3.7 and 3.8 show the interfaces of $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}/\text{GaAs}/\text{Si}$ (Epilayer thickness is about 7000\AA). The nature and characters of threading dislocations generated in $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}/\text{GaAs}/\text{Si}(100)$ tilted off 3.5° toward $[110]$ orientation have also been investigated using the SEM micrographs. Because of the limitation of the SEM system, more details will be obtained in the future study.

From the micrographs, we can see that almost all of the threading dislocations propagate through the growing layer without changing their running direction, not only in InGaAs epilayer, but also in GaAs buffer layer. Most of these threading dislocations are screw type or 60° dislocations and the propagating directions are found to be close the normal to the favored over layer-by-layer growth for large lattice mismatched systems.

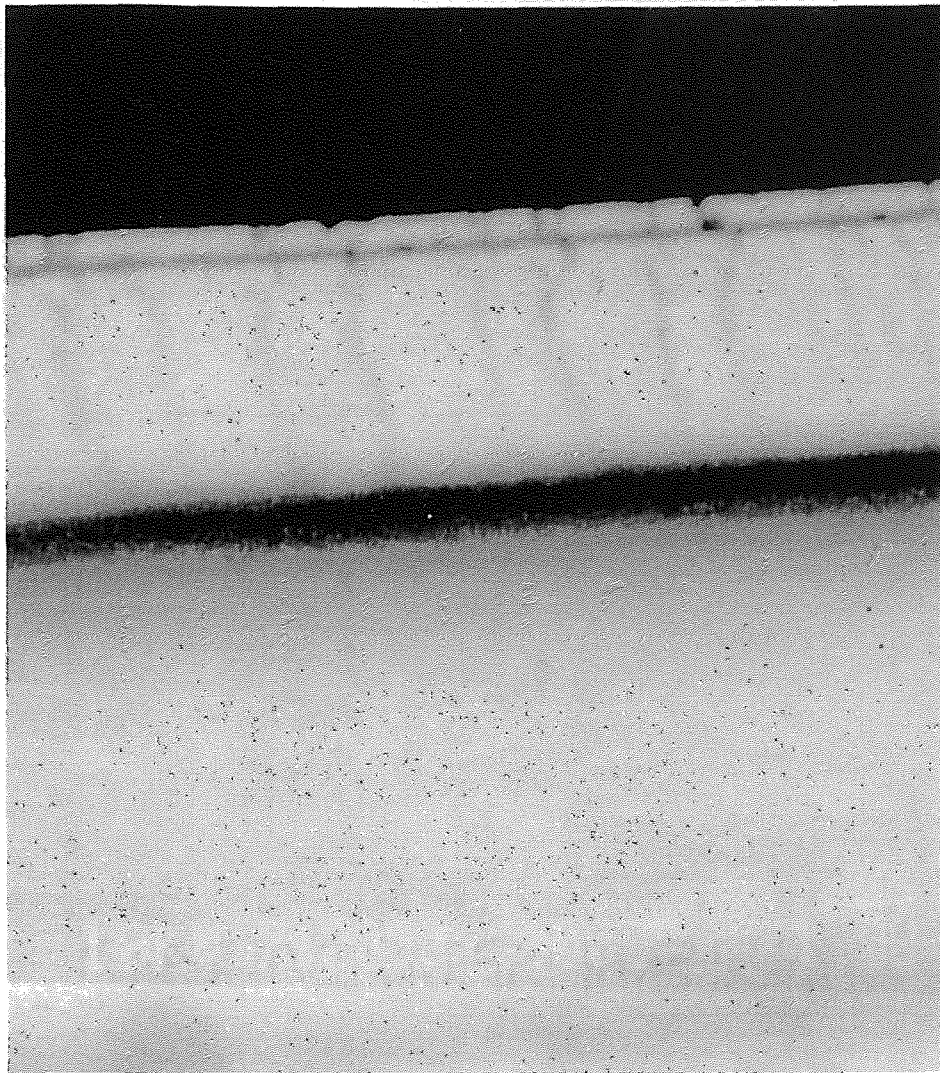


Figure 3.7 SEM Image of the Interfaces of $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}/\text{GaAs}/\text{Si}$

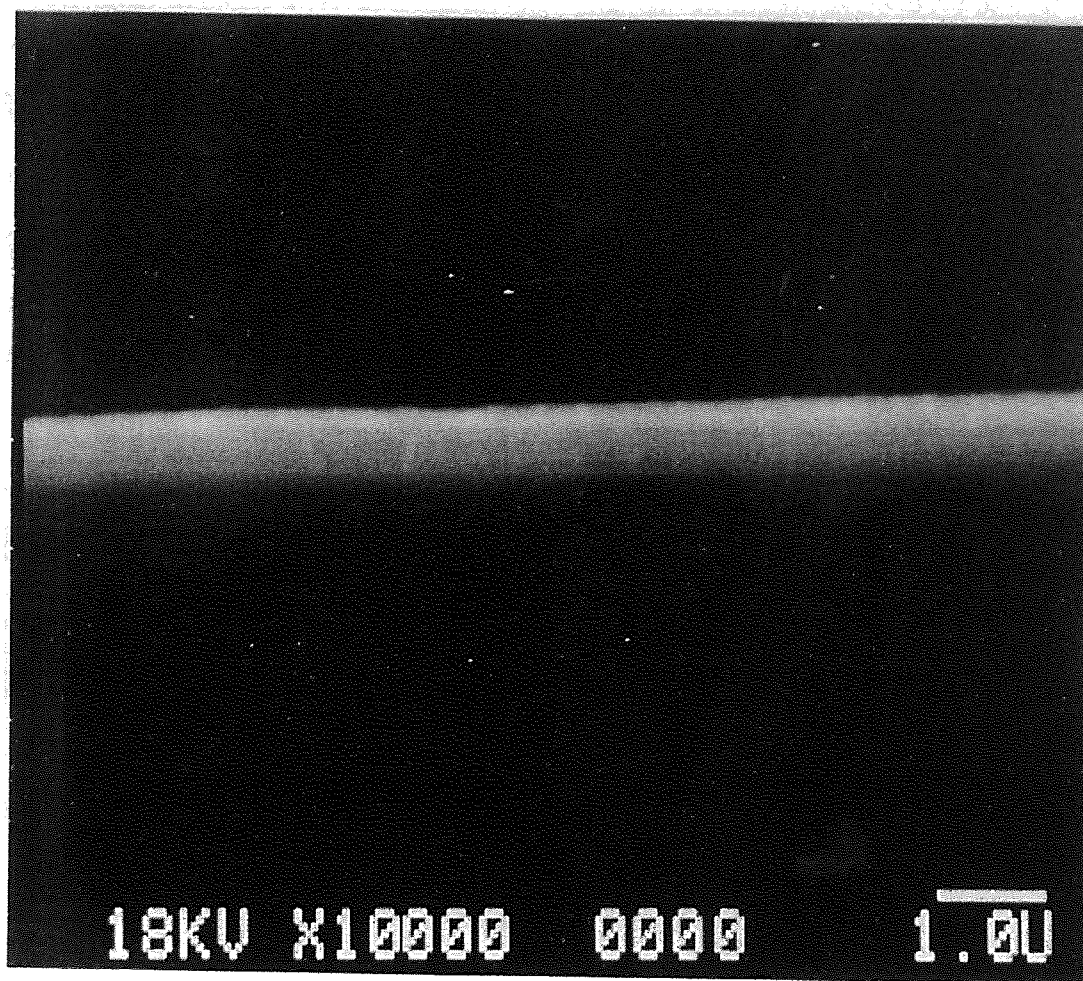


Figure 3.8 Enlarged SEM Image of the Interfaces of In_{0.5}Ga_{0.5}As/GaAs/Si

We use a schematic representation of examples of threading dislocation natures (Figure 3.9) to explain the generation of threading dislocations[33]. The Burgers vector for each dislocation is shown by short lines for the corresponding dislocations. We now consider typical examples of the generation of these threading dislocations. First, two sets of orthogonal arrays of misfit dislocations lying along two $\langle 110 \rangle$ orientations are generated at the (001) interfaces of InGaAs/GaAs/Si. These misfit dislocations are composed of both pure-edge dislocations and 60° -type ones with $\langle 110 \rangle$ Burgers vectors inclined to the (001) plane. It is anticipated that 60° -type misfit dislocations easily change their slip planes without interactions due to a strong strain field induced by a large misfit between the epilayer and Si and turn into threading dislocations. In this case, $\langle 110 \rangle$ -directed 60° misfit dislocations on the (100) interface are considered to be naturally changed into $\langle 211 \rangle$ -directed threading dislocations on the inclined $\{111\}$ planes. Namely, a larger number of $\langle 211 \rangle$ threading dislocations will be

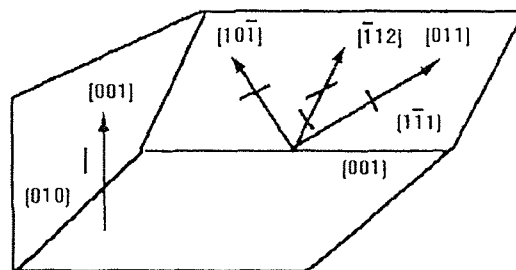


Figure 3.9 Schematic Representation of Threading Dislocation Natures

generated than $\langle 110 \rangle$ threading dislocations. This is consistent with the experimental results.

On the other hand, an asymmetric orthogonal array of misfit dislocations has already been observed, particularly at the $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ interface [23,34]. This asymmetry was first discussed on the basis of the absence of an inversion symmetry in the zinc-blende lattice[35]. Recently, Fox and Jesser have determined the asymmetry to be due to the differences in the Peierls barriers of the two types of dislocations[36]. This asymmetric misfit dislocation array may result in a preferential generation of $[112]$ or $[\bar{1}1\bar{2}]$ -directed threading dislocations in epitaxial GaAs films, if we consider the threading dislocation generation mentioned above. Such a dislocation asymmetry may also be related to another fact that the substrate orientation was tilted away from the $[100]$ to $[110]$.

The generation of threading dislocations will also be discussed in Chapter 4.

CHAPTER 4

FORMATION MECHANISMS OF MISFIT DISLOCATIONS

4.1 Critical Thickness

The critical thickness h_c of an epilayer is a parameter introduced to explain the experimental observation that for an epilayer having a different lattice parameter than its substrate. There is an epilayer thickness below which coherency is preserved, and above which it is not. The simplest model[8] to calculate h_c assumes that threading dislocations glide in the interface when the force F_ε due to the misfit strain is sufficient to overcome line tension F_l . Equating the two gives

$$h_c = \frac{b(1 - \cos^2 \theta)}{8\pi(1 + \nu) \cos \theta_1 f} \left(\ln \frac{h_c}{b} + 1 \right) \quad (4.1)$$

where b is the magnitude of the Burgers vector, ν is Poisson's ratio, θ is the angle between the misfit dislocation line and its Burgers vector, θ_1 is the angle between the slip direction and that direction in the interface which is perpendicular to the line of intersection of slip plan and the specimen surface, and f is the lattice mismatch.

Equation (4.1) can be refined [22] by including the resistance force F_p due to the Peierls stress. Then equating $F_\varepsilon = F_l + F_p$ gives

$$h_c = \frac{b(1 - \nu \cos^2 \theta)}{8\pi(1 + \nu) \cos \theta_1 (f - \varepsilon_p)} \left(\ln \frac{h_c}{b} + 1 \right) \quad (4.2)$$

with

$$\varepsilon_p = \frac{\sqrt{3}(1 - \nu)}{\sqrt{2}\mu(1 + \nu)} \tau_p$$

where τ_p is the Peierls stress, which can be expressed as

$$\tau_p = \frac{2\mu(1-\nu\cos^2\theta)}{(1-\nu)} \psi \exp\left[-\frac{2\pi\Gamma_d(1-\nu\cos^2\theta)}{b(1-\nu)} \psi\right] \quad (4.3)$$

with

$$\Gamma_d = \frac{a}{\sqrt{3}} \quad \text{and} \quad \psi = \exp\left(\frac{4\pi^2 n_\alpha kT}{5\mu a_e^3}\right)$$

where a and a_e are the lattice constants of the substrate and the strained layer respectively, n_α is the number of atoms in one unit cell, θ' is the angle between the dislocation line in the epilayer and its Burgers vector, and μ is the shear modulus.

4.2 Misfit Dislocation Sources [18]

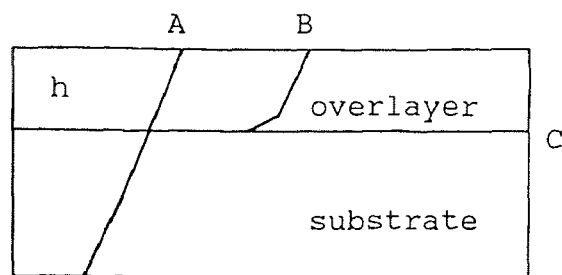
It is necessary for the study of a heterostructure system to investigate the formation of misfit dislocations focused on the energy (or force) balance between the creation of misfit dislocations (considered to occur at the the interface only) and strain relief by misfit dislocation formation [23]. We must discuss the three general categories of misfit dislocation nucleation: fixed sources, dislocation multiplication, and surface half-loop nucleation.

4.2.1 Fixed Nucleation Sources

The fixed nucleation sources are defined as those sources which decrease linearly in number with a decrease in growth area. Consider a substrate material which has a certain density of substrate dislocations which intercept the substrate surface. The dislocation like this is shown as Fig.4.1. As mismatched material is deposited, eventually the strain in the overlayer causes the force on A to become greater than zero, and the threading dislocation segment in the overlayer glides laterally,

creating a misfit dislocation at the interface. This also defines the CLT, the point where the energy to create the misfit dislocation at the interface balances the elastic energy released by the glide of the threading dislocation.

We expect fixed sources to have low activation energy for misfit dislocation nucleation since: (1) threading dislocations already exist in the epilayer as continuations of substrate dislocations, so that nucleation requires only the energy needed to extend the existing misfit dislocation along the interface. (2) Substrate surface inhomogeneities create large stress concentrations at the heterointerface during growth, thereby drastically reducing the activation energy necessary to heretogeneously nucleate misfit dislocation.



A: $h < h_c$ B&C: $h > h_c$

Figure 4.1 A Schematic Diagram Showing the Generation of a Misfit Dislocation from a Threading Dislocation. (The Dislocation in the Epilayer Glides from A to B and C after the CLT)

Because of the low activation barriers, we expect that substrate dislocations and substrate inhomogeneities are the first nucleation sources to be activated. therefore, the experimental CLT, or the point where misfit dislocations first appear, is usually determined by the fixed nucleation source density. However, films grown on dislocation-free substrates with a low density of surface inhomogeneities will exhibit a critical thickness much larger than expected since it is unlikely that another low-stress source exists in these films. Therefore, the

observed CLT will be greater and will occur at the stress level corresponding to the next lowest activation energy source (e.g., heterogeneous surface loop nucleation).

4.2.2 Dislocation Multiplication and Interaction

Once misfit dislocation sources become active, long lengths of misfit dislocations are created. Eventually the misfit dislocations become long enough to ensure a high probability of dislocation interactions.

The dislocation multiplication mechanism that is one type of dislocation interaction was first described by Hagen and Strunk [24]. This multiplication is shown schematically in Figure 4.2. Figure 4.2(a) depicts a plan view of a $[001]$ interface, with misfit dislocations lying along the $[110]$ and $[\bar{1}\bar{1}0]$ directions. If the directions have the same Burgers vector, a repulsive interaction occurs, forming a right-angle segment in the interface and a rounded right-angle segment which lies on a $\{111\}$ plane above the interface plane (Figure 4.2(b)). The $\{111\}$ segment can reach the surface because it is repelled by the junction and because it is attracted to the surface by the surface image force. This mechanism is effective in thin films where the $\{111\}$ segment can reach the surface, creating two new free-ended dislocations (Figure 4.2(c)). These dislocations can now glide and extend the two misfit dislocations to the wafer edge. The remnants of such a reaction produce an intersection as shown in Figure 4.2(d).

Dislocation multiplication is expected to increase the misfit dislocation density dramatically since two new misfit dislocations are produced for every multiplication event. However, it is unlikely that dislocation multiplication by the Hagen-Strunk mechanism will occur for thick overlayers, since the driving force for the $\{111\}$ segment to reach the specimen surface becomes low as the film

thickness increases. therefore, if Hagen-Strunk multiplication does not occur when the overlayer is thin, a thicker film will not possess interface dislocations generated by this form of multiplication.

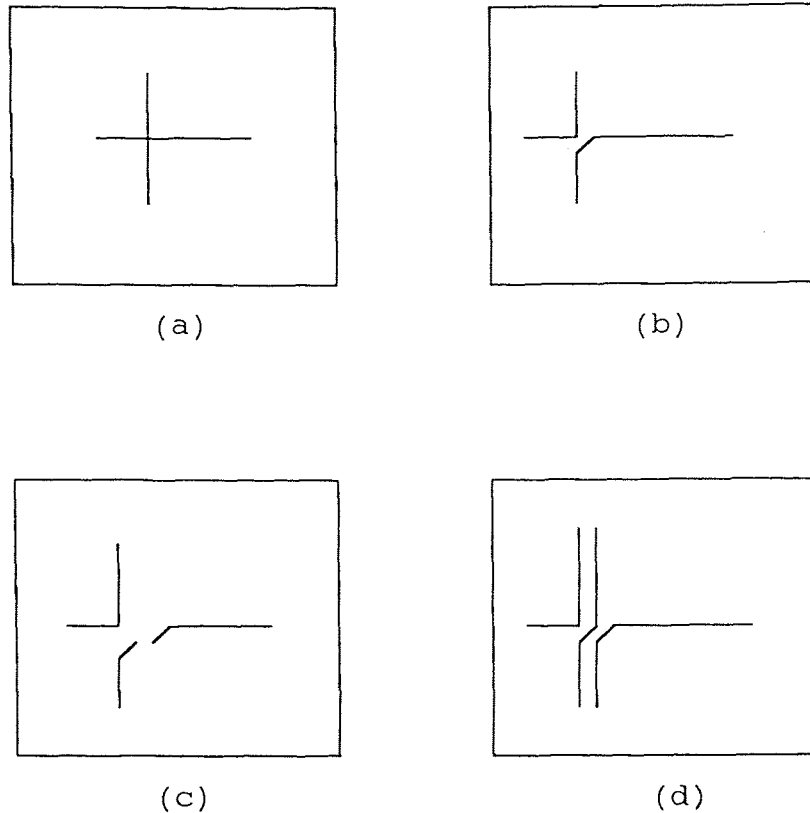


Figure 4.2 A Schematic Diagram of Dislocation Multiplication by Hagen-Strunk Mechanism

We note that other multiplication mechanisms may be active besides that described by Hagen and Strunk. For example, as a misfit dislocation is forming, the dislocation segment extending to the surface may cross other threading segments above the interface plane, i.e., in the epilayer. If the dislocations have the same Burgers vectors, a repulsive reaction will result in a surface half-loop and a segment on a $\{111\}$ plane extending up from the two misfit dislocations in the

interface plane. The surface half-loop can grow to form a misfit dislocation at the interface, and the $\{111\}$ segment may glide to the interface region or remain out of the interface plane. It is conceivable that this variation of the Hagen-Strunk multiplication mechanism could occur in thick films when many misfit dislocations are forming.

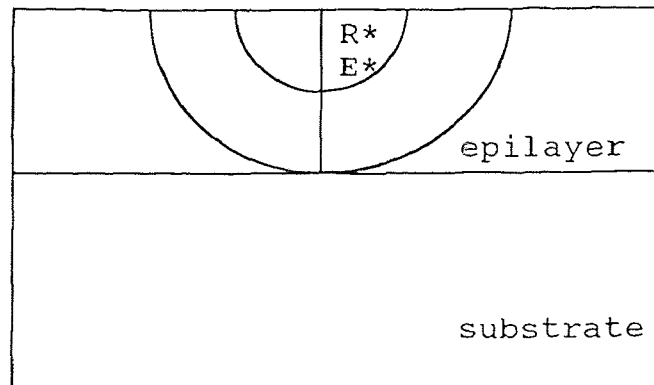
Dislocation interactions can also lead to an increase in the number of threading dislocations. When active, dislocation multiplication will continually produce large numbers of new gliding threading segments. Many of the threading 60° dislocations will not reach a free edge due to encounters with other dislocations. Some TEM observations of misfit dislocation formation show that threading 60° dislocations may be prevented from gliding further due to dislocation interactions at the interface, thereby increasing the density of threading 60° dislocations. Also, threading 60° dislocations with appropriate Burgers vectors can react in the epilayer to form a threading sessile edge dislocation. Subsequent strained layers cannot be used to reduce the threading edge dislocation density since the strain cannot move the sessile edge dislocation through the epilayer. The threading edge dislocation is therefore a permanent threading dislocation.

The ideal arrangement of 60° dislocation (in which the screw and tilt components cancel locally) results in the minimum number of dislocations needed to relieve strain. However, because Hagen-Strunk multiplication generates bundles of 60° dislocations with identical Burgers vectors, it is unlikely that the ideal arrangement will form and more 60° dislocations may be present at the interface than the number required for the ideal 60° dislocation distribution.

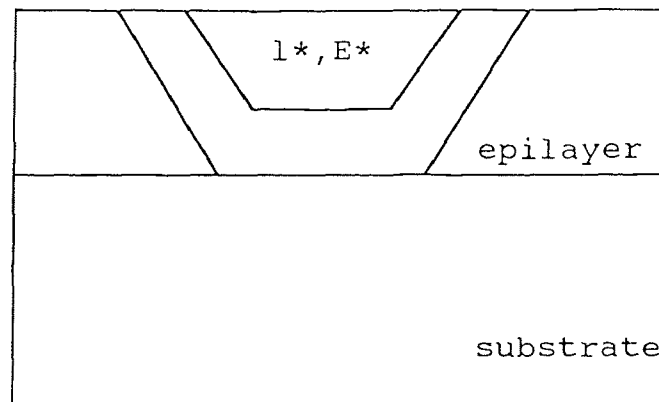
From the above discussion, it is clearly important to allow misfit dislocations to escape at the edges of the growth area and to limit the glide of dislocations during layer growth in order to prevent dislocation interactions.

4.2.3 Surface Half-loop Nucleation

If the overlayer and substrate have a large lattice mismatch, surface nucleation may occur. As we will show, homogeneous surface nucleation has a large activation energy and the strain required to activate this mechanism is high.



(a)



(b)

Figure 4.3 Misfit Dislocation Formation by Surface Half-loop Nucleation:(a) Semicircular Loop Nucleation; (b) Semi-hexagonal Loop Nucleation.

Figure 4.3(a) depicts the semicircular surface loop nucleation as described by Matthews [25]. In (001) zinc-blende or diamond heterostructures, surface half-loops nucleate on $\{111\}$ planes. The activation energy for the formation of this

half-loop will be dependent on the strain and surface energy released by the half-loop, as well as the energy needed to create the half-loop. We can approximate the creation energy as one-half the self-energy of a complete circular dislocation loop in an isotropic material [26]:

$$E = \frac{Gb^2R}{8} \left(\frac{2-\nu}{1-\nu} \right) \ln \left(\frac{8\alpha R}{e^2b} \right) \quad (4.4)$$

where G is the shear modulus in the $\{111\}$ plane, b is the magnitude of Burgers vector (which is coplanar with the loop), R is the radius of the loop, ν is Poisson's ratio, and α is the core energy factor (≈ 4 for the diamond cubic lattice).

The elastic energy released by the half-loop is found by integrating the force on the dislocation loop over the distance the half-loop has glided:

$$E_\varepsilon = \int F_\varepsilon dR \quad (4.5)$$

$$F_\varepsilon = \frac{2G(1+\nu)}{(1-\nu)} \pi R b \varepsilon \cos \lambda \cos \phi \quad (4.6)$$

where ε is the elastic strain in the overlayer, and $\cos \lambda \cos \phi$ resolves the biaxial stress into the glide plane perpendicular to the dislocation line direction. $\cos \lambda$ and $\cos \phi$ are defined by Matthews [27] and have values of $1/2$ and $\sqrt{2/3}$, respectively [28], for 60° dislocations in zinc-blende or diamond crystal structures. Combining equations (4.5) and (4.6) gives the strain energy released by the half-loop:

$$E_\varepsilon = \pi R^2 \left[\frac{Gb(1+\nu)}{(1-\nu)} \right] \varepsilon \cos \lambda \cos \phi \quad (4.7)$$

If we assume a planar growth mode, one atomic layer steps exist on surface. A surface dislocation half-loop will remove a fraction of the surface steps, thereby releasing surface energy:

$$E_s = 2 \gamma b \sin \beta = \left(\frac{Gb^2}{4} \right) \sin \beta \quad (4.8)$$

where γ is the surface energy per unit area and β is the angle between the Burgers vector and the dislocation line. The right-hand term in equation (4.8) was derived assuming $\gamma = Gb/8$ [25].

The total energy difference of the system due to the formation of the semicircular loop is $E = E_1 + (E_\epsilon + E_s)$:

$$E = \frac{GbR}{8(1-\nu)} \left[b(2-\nu) \ln \left(\frac{8\alpha R}{e^2 b} \right) - 8\pi R \epsilon (1+\nu) \cos \lambda \cos \phi - 2b(1-\nu) \sin \beta \right] \quad (4.9)$$

The critical loop radius for surface nucleation, R^* , can be derived by maximizing equation (4.9) with respect to R :

$$R^* = \frac{b(2-\nu) \left[\ln \left(\frac{8\alpha R^*}{e^2 b} \right) + 1 \right] - 2b(1-\nu) \sin \beta}{16\pi \epsilon (1+\nu) \cos \lambda \cos \phi} \quad (4.10)$$

If the half-loop grows beyond this critical radius, it will spontaneously grow and reach the interface, eventually forming a misfit dislocation. The activation energy to reach critical radius size is obtained by inserting R^* in equation (4.9) $E^* = E^*(R)$.

The above calculations are for a semicircular loop. However, recent observations suggest a prismatic or semihexagonal geometry for larger loops [29]. Using an analogous derivation for the semihexagonal loop shown in Figure 4.3(b), we arrive at

$$l^* = \frac{3(2-\nu)b \left[\ln \left(\frac{4\alpha l^*}{c\sqrt{3}b} \right) + 1 \right] - 2\pi b(1-\nu) \sin \beta}{32\pi \epsilon (1+\nu) \cos \lambda \cos \phi} \quad (4.11)$$

$$E^* = \frac{\sqrt{3}Gb l^*}{(1-\nu)} \left[\frac{1}{4\pi} (2-\nu)b \ln \left(\frac{4\alpha l^*}{c\sqrt{3}b} \right) - \frac{4}{3} l^* (1+\nu) \epsilon \cos \lambda \cos \phi - \frac{(1-\nu)}{6} b \sin \beta \right] \quad (4.12)$$

where $c=e^{0.84}$ [30], and l^* , the edge length of the hexagon, is analogous to R^* for semicircular geometry.

4.3 The Effect of Growth Area [18]

We now discuss the effect of limiting growth area on the dislocation nucleation sources described above. Figure 4.4 schematically illustrates the advantages of growth on small areas versus large areas. The black dots represent fixed sources (substrate dislocations and substrate surface inhomogeneties). As mismatched overlayer is grown on a large area [Figure 4.4(a)], misfit dislocations start to nucleate at the many fixed nucleation sites found within the large area, since these

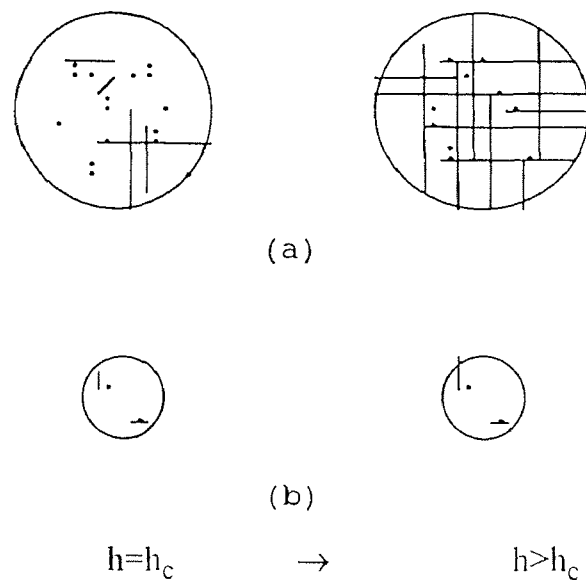


Figure 4.4 The Formation of Interface Dislocations for (a) Large Growth Area and Small Growth Area

have the lowest activation energy of the sources discussed previously. Each of these many nucleation sources can initially form a long misfit dislocation segment since the lateral glide of the dislocation is not inhibited. Long glide and long misfit

dislocation lengths result in many dislocation interactions, leading to dislocation multiplication and an increased number of threading dislocations. The new dislocations created by dislocation multiplication can now glide to create even more misfit dislocation length in the interface and more dislocation interactions. The final result is a heterostructure with many threading and interface dislocations.

Now consider growth on small areas, as depicted in Figure 4.4(b). As first theorized by Matthews [27], a reduction in growth area will reduce the number of threading dislocations available for misfit dislocation formation in that area. This can be shown by considering the definition of linear interface-dislocation density:

$$\rho_1 = 1/S_{110} = \delta/b_{\text{eff}} = 2\delta/b \quad (4.13)$$

where ρ_1 is the linear interface dislocation density, S_{110} is the dislocation spacing along a $\langle 110 \rangle$ direction, δ is the plastic deformation, b is the Burgers vector, and b_{eff} is the strain relief component of the Burgers vector along one $\langle 110 \rangle$ direction, which is equal to $b/2$ for 60° dislocations. The plastic deformation is

$$\delta = j\rho_f \left(\frac{L}{2} \right) \left(\frac{b}{2} \right) = j\rho_f L \frac{b}{4} \quad (4.14)$$

where $(b/2)$ is the effective Burgers vector for 60° dislocations for one $\langle 110 \rangle$ direction, ρ_f is the density of fixed nucleation site (cm^{-2}), $(L/2)$ is an average length of misfit dislocation line in a square growth area of side L , and j is the fraction of fixed nucleation sites which generate misfit dislocation along that $\langle 110 \rangle$ direction. If there is not a difference in $\langle 110 \rangle$ interface-dislocation densities and every fixed nucleation site creates a misfit dislocation, then $j=1/2$. If 75% of the nucleation sites produce misfit dislocations along a $\langle 110 \rangle$ direction in an asymmetric interface, then $j=3/4$ for that direction.

Combining equations (4.13) and (4.14) yields

$$\rho_1 = j\rho_f L/2 \quad (4.15)$$

Therefore, if fixed nucleation sources are responsible for all misfit dislocations, the linear interface-dislocation density is proportional to the fixed nucleation site density (ρ_f) and mesa size (L).

For a circular mesa, the derivation is identical, except the average length of a misfit dislocation line in a circular mesa of diameter L is $\left(\frac{\pi}{8}\right)L$, giving

$$\rho = j\rho_f L \frac{\pi}{8} \quad (4.16)$$

Thus, the number of low activation energy nucleation sites can be reduced by using high-quality substrates and by limiting the size of the growth area. In addition, an operating fixed source cannot generate long lengths of misfit dislocations in the interface due to the escape of the dislocation at the edge of the small growth area. Dislocation interactions are virtually eliminated as well since the average length and lateral glide of misfit dislocations is small, and the probability of dislocation interaction is sharply reduced.

However, homogeneous surface half-loop nucleation will not be affected by a reduction in growth area, since homogeneous surface half-loop nucleation is a function of elastic strain only. As shown above, a high strain is needed for this process. therefore, if the growth area is reduced and the elastic strain is below (about 2%-6%), very few misfit dislocations will be able to form.

CHAPTER 5

CONCLUSION

In summary, we demonstrate that we have grown a high quality $\text{In}_x\text{Ga}_{1-x}\text{As}$ epilayer on Si (with a buffer layer of GaAs) by MBE technique. A great number of dislocations were formed and the surface of buffer layer became microscopically rough as the thickness of buffer layer increased as indicated in observation from RHEED. Combination of SEM observation of the etched surface of GaAs on Si and the study of PL showed that the structures of GaAs buffer layer tended to be poly-crystalline even though the crystallization centers due to silicon oxides and other contaminations were greatly reduced. The predominant orientation probably occurred during following epitaxy of $\text{In}_x\text{Ga}_{1-x}\text{As}$.

SEM study of interfaces of $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}/\text{Si}$ revealed that most of the threading dislocations were screw type or 60° dislocations and all of them propagated through the growing layer without changing their running direction which was close to the normal to the plane of layer-by-layer growth for this large lattice mismatched system. The linear dislocation densities along two $\langle 110 \rangle$ directions, 200cm^{-1} and 1200cm^{-1} respectively, were obtained from microscopic observation of cross-hatch. The SEM topographies of the epitaxial growth of $\text{In}_{0.5}\text{Ga}_{0.5}\text{As}$ on tilted and untilted Si substrates showed that in the case of tilted substrates, the island growth would not be isotropic and the islands tend to be elongated running parallel to the steps. On the other hand, the SiO_2 and other contaminations on the surface of substrates will greatly affect the quality of the epilayer. The mechanism of dislocation sources and interactions was also summarized using simple models.

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