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ABSTRACT

FABRICATION AND CHARACTERIZATION OF WSi_2 /p-si AND $TaSi_2$ /p-si DEVICES

by
Anitha Kodali

Thin films Silicides of Tungsten and Tantalum have become very important for IC manufacturing. W and $TaSi_2$ films were deposited on silicon substrates by CVD and Co-sputtering techniques respectively. These films have been characterized using current-voltage technique. The analysis of the obtained experimental measurements has been performed in the light of Schottky-Mott theory. The effects of annealing were studied using Rapid Thermal Processing technique in the temperature range of 500 to 700°C, in nitrogen atmosphere at a constant pressure of $5x10^{-6}$ torr for a duration of 30 seconds.The increase in annealing temperature resulted in the formation of ohmic contact evidenced by current-voltage and sheet-resistance measurements. Typical sheet -resistances were found to be in the order of 6-12Ω /square for tungsten silicide and 2-7Ω /square for tantalum silicide. The RTP technique,as concluded from the results, was found to be very effective in the formation of ohmic contacts.

FABRICATION AND CHARACTERIZATION OF WSi_2 /p-si AND $TaSi_2$ /p-si DEVICES

by
Anitha Kodali

A Thesis
Submitted to the Faculty of
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in Partial Fulfillment of the Requirements for the Degree of
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Department of Electrical and Computer Engineering

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APPROVAL PAGE

FABRICATION AND CHARACTERIZATION OF WSi_2/p-si AND $TaSi_2$/p-si DEVICES

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This thesis is dedicated to
my Grandmother

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CHAPTER 1

INTRODUCTION

1.1 An Overview

The primary thrust of very large scale integration (VLSI) has been the miniaturization of devices to increase packing density, achieve higher speed and consume less power[1]. The continued evolution of smaller and smaller devices has aroused a renewed interest in the development of new metallization schemes for low resistivity gates, interconnection and Ohmic contacts. This interest in new metallization sehemes has been aroused by the fact that with the scaling down of the device sizes, the line width gets narrower and sheet resistance contributing to RC delay increases.

Aluminum and its alloys are used extensively for metallization in integrated circuits because of their low resistivities(i.e., 2.7μΩ-cm for Al and upto 3.5 μΩ-cm for its alloys). However the use of aluminum in integrated circuits for shallow junctions often creates problems such as spiking and electromigration[2]. It also requires all post gate processing of the devices to be limited to very low temperatures preferably below 500°C. Aluminum on silicon leads to metallurgical interactions causing serious instabilities. Annealing of aluminum on silicon (typically at 450°C) causes dissolution of silicon by diffusion into the metal and leads to pit formation[3]. The pits in silicon become visible after selectively removing Al from the surface. In actual devices, diffused aluminum is present in silicon below the Al/Si interface. If the penetration is deep, it leads to contact and junction failure. Electromigration causes considerable materials transport in Al because of the enhanced and directional mobility of atoms which lead to momentum transfer. Aluminum gathers in the direction of electron flow, leading to

a discontinuity in the current-carrying lines. This type of device failure seriously affects the reliability of silicon integrated circuits [4].

We can use polysilicon as gate metal and interconnect. The structure of polysilicon is strongly influenced by dopants, impurities, deposition temperature and post deposition cycles[5]. Films deposited for temperatures below 575°C, are amorphous with no detectable structure. Poly, deposited above 625°C are polycrystalline and has a columnar structure, which leads to higher resistivity.

The undoped polysilicon films can be highly resistive (400-700Ω-cm). However, their resistivity can be decreased by doping them with appropriate dopant gases introduced during the deposition process.The major disadvantage of polysilicon as a gate metal is its high resistivity. With the increasing complexity and density of IC's, the width and spacing of the polysilicon runners have to be reduced. With desired improvements in speed-power product, the RC delays introduced by the polysilicon films becomes unacceptable..

Refractory metals were investigated for applications in VLSI technology in the 1970's. The two most commonly investigated materials were tungsten and molybdenum[6,7]. These materials have much higher melting points than silicon, and their thermal expansion co-efficients are similar to that of silicon.But the use of refractory metals requires complete passivation of these metals from oxidizing ambient and they may form silicides at temperatures above 900°C when they are in contact with silicon.The formation of silicides is accompanied by a volume shrinkage which can result in development of cracks. These cracks pose functional and reliability problems in IC's. Among many problems of refractory metals are those of cleanliness, contact to other conductors and deposition and etching of the metals for pattern generation. The uncertainties associated with the stability of these metal films have led to search for alternative materials.

The silicides have attracted attention because of their low resistivities and high temperature stability. The use of silicides, with resistivity values one tenth those of polysilicon, is certain to improve the speed of ICs. Expected higher electromigration resistance and the possibility of forming silicides directly on polysilicon, thus preserving the basic polysilicon MOS gate while decreasing the resistance, make these silicides attractive for gate and interconnect metallization[8,9].

Scaling down in the size also means reduced junction depths. This could lead to contact problems. In particular, shallow junctions limit the use of aluminum due to its known penetration in silicon. Forming silicides in the contact windows by reaction between the silicon substrate and a thin metal layer offers a possibility of forming contacts with lower contact resistances. The possibility of using deposited silicides directly into contact windows offers the advantage of preserving shallow junctions which may be penetrated by a conventional silicide formed by reacting a metal with silicon.

Silicides such as WSi_2, $TaSi_2$ and $TiSi_2$ have reasonably low resistivities ($<50\mu\Omega$-cm) and are generally compatible with integrated-circuit processing. WSi_2 in particular has attracted attention because of good adhesion properties, good resistivity, high temperature stability, and the feasibility of forming an insulating layer on top [10].

1.2 Objectives of the Current Work

This study focuses on the formation and characterization of the silicides.The samples used for experimental studies are W on p-Si and $TaSi_2$./p-Si The thesis gives an overview of the methodology of formation of metal thin films. Post annealing of these metal films using RTP techniques at different temperatures results in a) formation of Tungsten silicide b) improved contact of $TaSi_2$ on p-si.

These silicides are characterized by current-voltage and sheet resistance techniques.

1.3 Organization of the Thesis

This thesis is a study of Fabrication and Characterization of WSi_2/p-Si and $TaSi_2$/p-Si devices. Chapter 2 gives an overview of the different processing techniques for silicides.We discuss the advantages and disadvantages of each of the processing techniques. Chapter 3 throws light on the physical and electrical properties of silicides. Chapter 4 is concerned with Rapid Thermal Processing and Chapter 5 is devoted to experimental results. Conclusions inferred from experimental data are presented in the chapter 6.

The various process recipies used for silicide formation, and the software programs used for the analysis of electrical properties are included in the Appendix.

CHAPTER 2

FORMATION OF SILICIDES

2.1 Introduction

In most case, silicides are formed by a diffusion-limited growth process. In some cases, a linear dependence on time, indicating an interface rate controlled interaction, has been reported[11,12]. The inter metallic formation and kinetics of the metal-silicon interaction also strongly depend on the nature of the metal film (its thickness, grain size, purity, and defects), the substrate preparation, the interfacial oxide thickness, and the film deposition parameters (such as energy, temperature, and ambient pressure). The most important factors that control the silicide nucleation and growth are: the cleanliness of the metal-silicon interface, the purity of the film and substrate materials, the diffusivity of metal atoms in silicon and vice versa, the realtive free energy formation of various phases and the temperature of interaction.

2.2 Methods of Silicides Formation

Silicides of interest can be formed by, basically, three techniques, each of which involve a metal deposition followed by a thermal step to form the silicide:

- Direct Metallurgical Reaction: Deposition of the pure metal on silicon (i.e. onto single crystal / polycrystalline silicon).
- Co-evaporation: Simultaneous evaporation of the silicon and the refractory metal from two sources.
- Sputtering: Sputter deposition of the silicide, either from a composite target, or by cosputtering or layering.

• Chemical Vapor Deposition: Formation of a thin metal film on Si by the reaction of vapor phase chemicals(reactants) that contain the required constituents.

2.2.1 Direct Metallurgical Reaction

In this technique, a refractory metal film is deposited directly on a silicon surface, and the wafer is annealed at relatively low temperatures, Metal rich silicides are initially formed, and continue to grow until the metal is consumed[13]. Typically at that point, the next silicon rich phase begins to grow. For example the figure 2.1 shows the effect of temperature on the formation of WSi_2 and W_5Si_3. W_5Si_3 has the highest melting point and WSi_2 has the least.This temperature dependence has been observed for most silicide formation,and is an indication of a diffusion limited process. In this WSi_2 reaction, for each angstrom of tungsten thickness consumed, 2.53A of silicon are consumed, resulting in 2.58A of WSi_2 being formed. An important care must be taken that sufficient silicon should be available when using this technique.

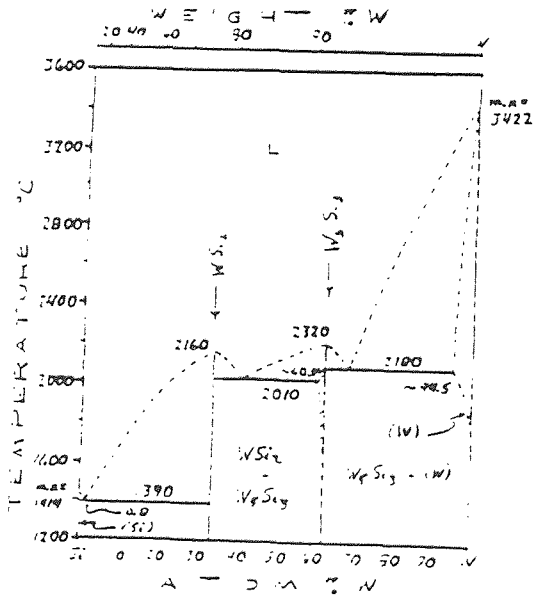

Figure 2.1 Phase diagram of tungsten-silicon system

2.2.2 Co-Evaporation

The evaporation method utilizes the simultaneous deposition of the metal and Si under high vacuum conditions. The metal and Si can be vaporized by electron beam, rf induction, laser, or resistive heating. Since the refractory metals like W, Ta, Ti, Mo have very high melting points (1670°C to 2996°C), and silicon has a low vapor pressure, e-beam evaporation is chosen as one of the best choice. In e-beam evaporation, a stream of electrons is accelerated to high kinetic energy, and the beam is directed at the material to be evaporated, and the kinetic energy is transformed to thermal energy upon impact. This electron stream can melt and evaporate any material, provided the beam can supply energy to the evaporant at an equal rate at which heat is lost, as the material is held at high temperature. Electron beam guns are built to supply up to 1200KW of highly concentrated

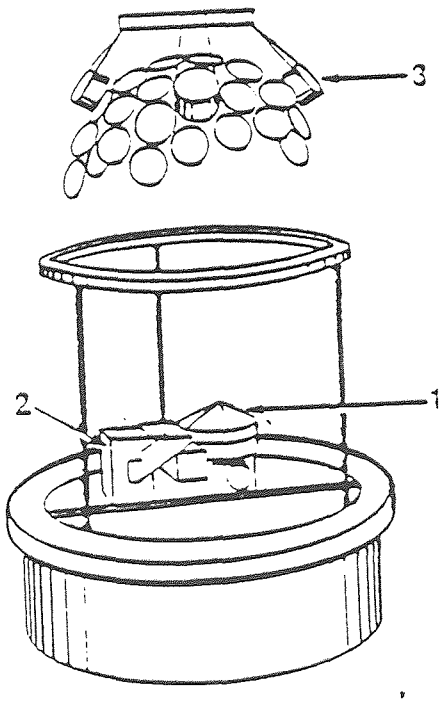

Figure 2.2 Typical arrangement of electron beam evaporator. (1) of 270°C electron gun (2) centrally located relative to the planetary substrate holder(3).

electron beam power for evaporation applications. Very high film deposition rates can thereby be obtained as a result of high power available. Typically two guns are employed with separate power supplies. Careful determination of the evaporation rate as a function of power for both metal and Si must be determined. The correct amount of power is supplied to each gun to provide the proper M/Si ratio where M denotes metal. X-ray damage from e-beam evaporation is generally annealed out during the high temperature sinter operation. A typical configuration for deposition is shown in the Figure 2.2.

2.2.3 Co-Sputtering

Sputtering using one Silicide Alloy Target : In this technique, a sputtering chamber has a single powered sputtering target. The Si:M ratio, in the film is tied to that of the target, and only small variations can be effected by changing the sputtering parameters. Figure 2.3 shows the Si:Ta ratio of the Ta-Si films deposited using various sputtering pressures for the same sputtering target[15]. Thus, to obtain

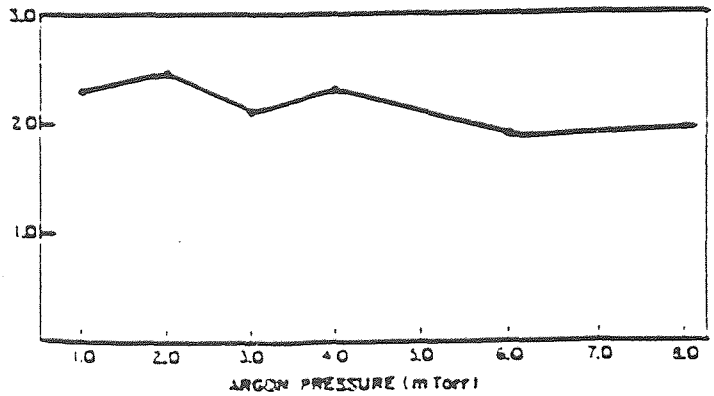

Figure 2.3 Si:Ta ratio as a function of sputtering pressure in films with Si:Ta ratio of 2.6.

significant Si:M ratio variations, one must have several targets with Si:M ratios spanning the desired range.

There are two different techniques of Sputtering, (1) using single target and (2) Two or more targets. These two different techniques are described below:

Sputtering using two or more Targets: In this technique, a sputtering chamber can have two or more independently powered sputtering targets.. The deposition rate is established from the individual metal and silicon targets for a given condition of sputtering. These rates are used to determine the desired Si:M atomic ratio in the deposited silicide film. Figure 2.4 shows calibration curves, for tantalum and silicon determined in a dual-target d.c.magnetron sputtering system. The sputtering rate of silicon should be noted.Target power is varied according to the metal-silicon system desired.

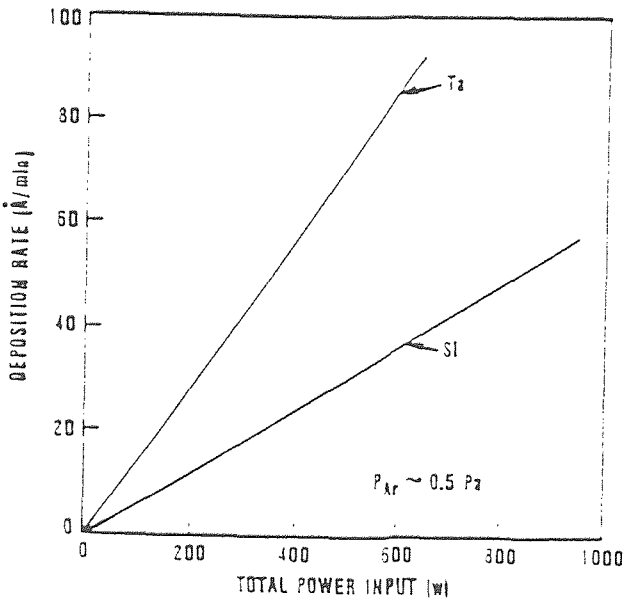

Figure 2.4 Deposition rates Vs Power for Ta and Si

2.2.4 Chemical Vapor Deposition

In this technique, the material which forms a thin film on the substrate is produced by a chemical reaction in the vapor phase or by a reaction that occurs on the substrate. The reaction is generally induced by heat, which causes either a decomposition of vapor or a reaction between different gaseous species in the ambient. Such depositions are limited only by the availability of the reactants that are in the gas phase or that will easily vaporize. The reactants must decompose or react to produce the desired film at usable temperatures. The process is usable as long as the temperatures are low enough so that they do not effect the characteristics of the processed substrates.

Tungsten and Molybdenum which are common metals for forming the metal-semiconductor contacts have been very successfully deposited using LPCVD(low-pressure chemical vapor deposition). CVD of tungsten is generally performed in either hot-wall low pressure system or a cold wall, low pressure temperature system figure 2.5. Tungsten hexaflouride, WF_6, is well suited as the W source gas, since it can be either reduced by hydrogen or silicon. The silicon reduction is given by:

$$2WF_6(\text{vapor}) + 3Si\ (\text{solid}) \rightarrow\ 2W(\text{solid}) + 3SiF_4\ (\text{vapor})$$

while the hydrogen reduction is given by:

$$WF_6(\text{vapor}) + 3H_2(\text{vapor}) \rightarrow\ W(\text{solid}) + 6HF\ (\text{vapor})$$

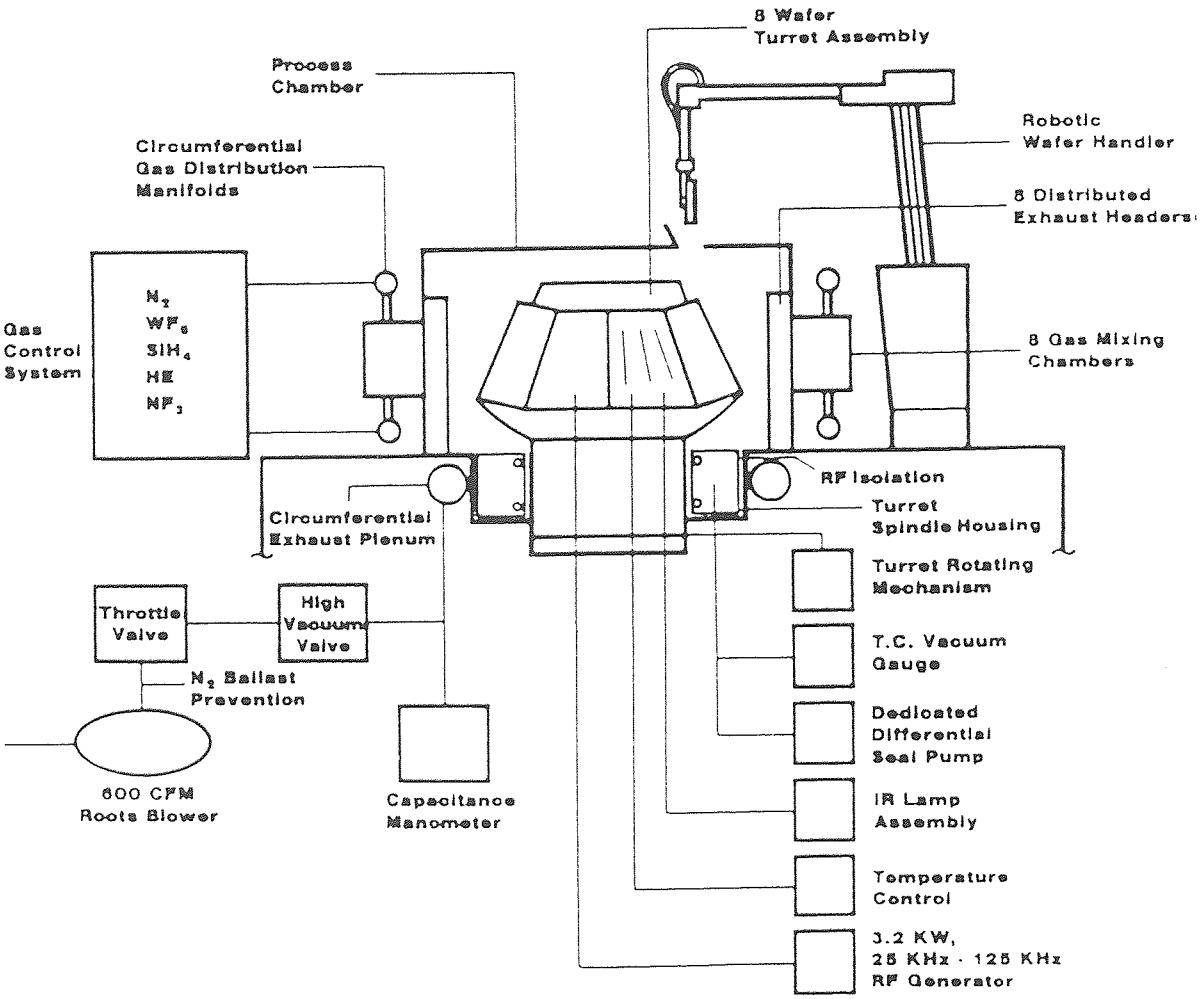

Figure 2.5 Schematic of the cold-wall reactor for CVD of WSi_2

other source gases such as WCl_6 have also been employed in the hydrogen reduction, and the other refractory metals are generally reduced by hydrogen from their respective chlorides. The hydrogen reduction may result in the selective deposition of W. However, the reaction requires good nucleating surfaces[16]. Silicon, metal, and silicide surfaces provide good sites, while SiO_2 and Si_3N_4 (especially at low temperatures), do not. On the silicon surface, the deposition starts by the Si reduction, but after the reaction becomes self-limiting, the H_2 reduction takes over. At the outset of the deposition, the carrier gas is Ar. After the Si reduces WF_6, H_2 is added to the gas flow, and the Ar flow is stopped. The silicon reduction of WF_6 can be used to produce thin films of selectively deposited W. These films have excellent surfaces and sheet resistances of 10-15Ω / sq.- cm..

2.3 Advantages and Disadvantages of Each of the Techniques

The technique discussed in section 2.2.1 has one main advantage; the silicide growth usually yields a lower resistivity when compared to the other methods. Both polycide and salicide structures can be formed using this technique. Selective etching is possible. The disadvantage of this technique is that M/Si ratio depends on the phase formed. The silicide formed is sensitive to sintering environment. After sintering the surface formed is rough.

The technique discussed in section 2.2.2 have these advantages; the purity of the silicide formed is good when compared to the other methods. Sintering environment is not as critical when compared to other techniques. The surface formed after sintering is quite smooth. The disadvantage is that the M/Si ratio is theoretically possible but practically difficult. No selective etching is possible. Step coverage is poor.

The technique discussed in section 2.2.3 have these advantages; good control of M/Si ratio, the films formed are smooth, sintering environment is not as

critical and good step coverage. It has the ability to deposit sandwich of metal and silicon. This technique always leads to the silicides that are relatively free of oxygen. The disadvantages are contamination from target and no selective etching of the metal after sintering.

The technique discussed in section 2.2.4 offers several advantages , the most important of which are excellent step coverage and high throughput, higher purity films (low O_2 content) and improved uniformity on large area silicon wafers. Possible poor adhesion is the disadvantage.

CHAPTER 3

PROPERTIES OF SILICIDES

3.1 Introduction

The desired properties of silicides to be used in IC fabrication are listed below :

- Low resistivity
- Ease of fabrication
- Patterning suitability
- Stability in oxidizing ambients; oxidizability
- Mechanical integrity; good adherence, low stress
- Surface smoothness
- Stability throughout processing, including high temperature sinter, dry or wet oxidation, gettering, passivation, metallization etc.
- Lack of reactivity with final metal, aluminum
- Not a contamination source of devices, wafers or working apparatus
- Good device characteristics and lifetimes
- For window contacts- low contact resistance, minimal junction penetration

3.2 General Physical Properties

More than half of the elements in the periodic table react with silicon to form one or more silicides. Of all silicides, silicides of group IVA, VA and VIA which are called refractory metal silicides are of particular interest to us. Although the list of all these silicides is long, the number is further reduced by noting that not all these are known to form silicides[17] when a thin metallic film reacts with silicon or polysilicon substrates. Finally, we must consider the fact that the availability of silicon is unlimited and, for the present device processing temperatures of 900°C

or more only silicon rich silicides are stable. Table 3.1 lists all such silicides of interest to us together with their melting points. Also listed in Table 3.1 are lowest eutectic temperatures in these metal-silicon systems[18,19]. As is apparent, silicides of Pd,Pt and Ni are not suitable for processes where temperatures may exceed 700°, 800° and 900°C respectively.

Table 3.1 Lowest eutectic temperatures of some silicides of interest

Silicide	Temperature(°C)	Composition(%Si)
WSi_2	1440	99.2
$TiSi_2$	1330	86
$HFSi_2$	1300	91.8
VSi_2	1385	97
$TaSi_2$	1385	99
$CrSi_2$	1300	87
$MoSi_2$	1410	97
$NbSi_2$	1295	95
$FeSi_2$	1208	73
PtSi	830	23
$CoSi_2$	1195	23
$ReSi_2$	1125	90
Pd_2Si	720	45
Ru_2Si_3	1370	83
$NiSi_2$	966	46

3.2.1 Schottky Barrier Height

When a metal is deposited or a silicide is formed on a semiconductor(i.e.,silicon), a potential barrier to charge transfer results because the Fermi levels are required to match up. Such a barrier is commonly referred to as the Schottky barrier,which arises from the difference in the work functions of the metal and the semiconductor. The height Φb of this barrier predicts the current flow characteristics of the metal on semiconductor devices. Figure 3.1 lists the best known values of the Schottky barrier heights of various silicides on n-silicon. The barrier heights of silicides are controlled by four apparent variables:1) The work function Φ_M of the metal, 2) The ability of the metal atoms, which may have diffused (across the interface)into silicon, to act as traps for electrons or holes and thus participate in the current carrying process, 3) the crystalline or amorphous structure at the metal-silicon interface and 4) the outermost electronic configuration of the metal.

The barrier height is a property of the given metal on silicon system and is independent of the silicide phase formed.[20,21]. The experiments carried out in ultra high vacuum systems indicate that the barrier height is pinned down as soon as a monolayer of the metal is deposited on a clean silicon surface[22].In some cases, the barrier height of the metal is found to be different from that of its silicide. The difference is attributed to the diffusion of metal atoms, which create traps for electrons and holes and thus participate in the current-conduction processes, into the semiconductor[23]. For n-silicon, the barrier height decreases for higher doping levels leading to lower contact resistances. At high enough doping ($>10e^{19}cm^{-3}$), current flow due to tunneling across the metal-semiconductor barrier dominates and contact resistance is very low.

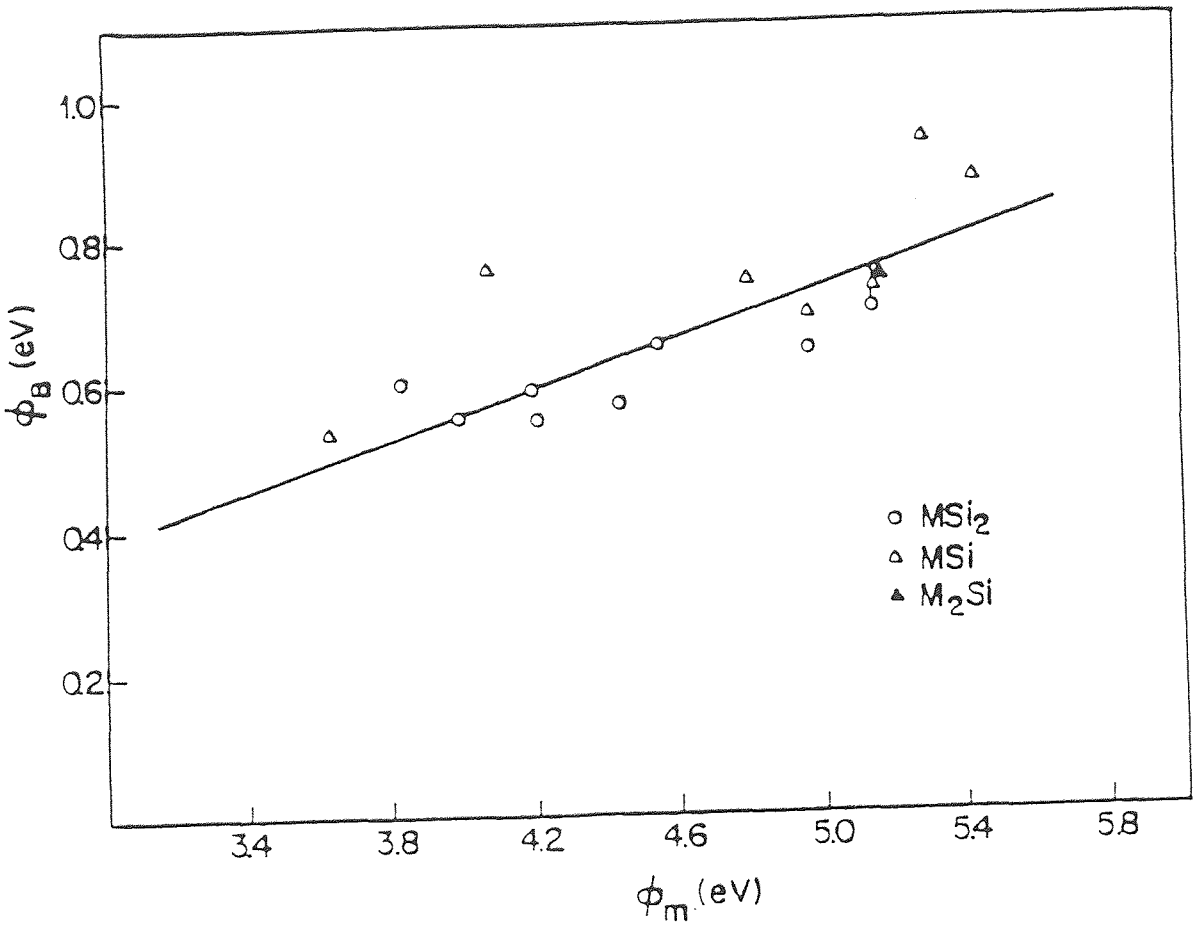

Figure 3.1 Schottky barrier heights of various silicides on n-silicon as a function of the metal work function.

3.2.2 Resistivity

The resistivity of silicides is the single most important factor in considering them for use as metallization in integrated circuits. Table 3.2 lists the resistivities of silicon-rich silicides for the refractory and near noble metals.

Table 3.2 Resistivities of various silicides

Silicide	Formed by Starting from	Sintering Temperature (°C)	Resultant Resistivity ($\mu\Omega$-cm)
$TiSi_2$	Metal on Polysilicon	900	13-16
	Cosputtered	900	25
$ZrSi_2$	Metal on Polysilicon	900	35-40
$HfSi_2$	Metal on Polysilicon	900	45-50
	Cosputtered Alloy		60-70
VSi_2	Metal on Polysilicon	900	50-55
$NbSi_2$	Metal on Polysilicon	900	50
$TaSi_2$	Metal on Polysilicon	1000	35-45
	Cosputtered Alloy	1000	50-55
$CrSi_2$	Metal on Polysilicon	700	~600
$MoSi_2$	Metal on Polysilicon	1100	~90
	Cosputtered Alloy	1000	~100
WSi_2	Cosputtered Alloy	1000	~70
$FeSi_2$	Metal on Polysilicon	700	>1000
$CoSi_2$	Metal on Polysilicon	900	10-18
	Cosputtered Alloy	900	25
$NiSi_2$	Metal on Polysilicon	900	~50
	Cosputtered Alloy	900	50-60
PtSi	Metal on Polysilicon	600-800	28-35
	Cosputtered Alloy		
Pd_2Si	Metal on Polysilicon	400	30-35

The variation in the resistivities is the result of variability in preparation of the silicides. The variability is caused by purity(especially oxygen contamination) and crystallinity. Oxygen, due to its prevalent presence in the environment increases the resistivity significantly.

Oxygen, due to its prevalent presence in the environment increases the resistivity significantly.

The most commonly used method for measuring the resistivity ρ of a film is the Four-point probe method. In this method, a constant current is passed between two outer probes and voltage drop across the two middle probes is measured. By proper selection of the probes, probe separations and current, the voltmeter reading can directly give the sheet resistance Rs. The resistivity ρ and Rs are related by

$$Rs = \rho / d$$

where, d is the thickness of the film. The quantity Rs is given in ohms per square and is, in fact the resistance of a square of the film. In using this method to obtain film Rs and ρ, the contribution from the substrate must be taken into account. If the substrate is not an insulator, it will contribute to the conduction.

The other technique that can used to measure the resistivity(or sheet resistance) is the contactless method[24]. The biggest advantage of such a measurement is that the conductivity of the films, which are protected by insulating encapsulants, can be easily measured without removing the insulating layer. In this method, the currents that are magnetically induced in the conducting sample are measured by means of the magnetic fields they produce. A sample is inserted between two coils, a primary coil that produces a time-varying driving magnetic field and an identical secondary coil that acts as the detector. The voltage induced in this secondary coil is caused by the driving magnetic field in the primary coil and the magnetic field of the current induced in the sample. Since these two magnetic fields are 90 degrees out of phase, the signal caused by the sample alone can be measured by use of electronics. The resistivity can be easily calculated if the contribution from the various layers that make up the sample are known. Figure 3.2 shows a plot of the sheet resistance of W-Si as a function of sintering temperature.

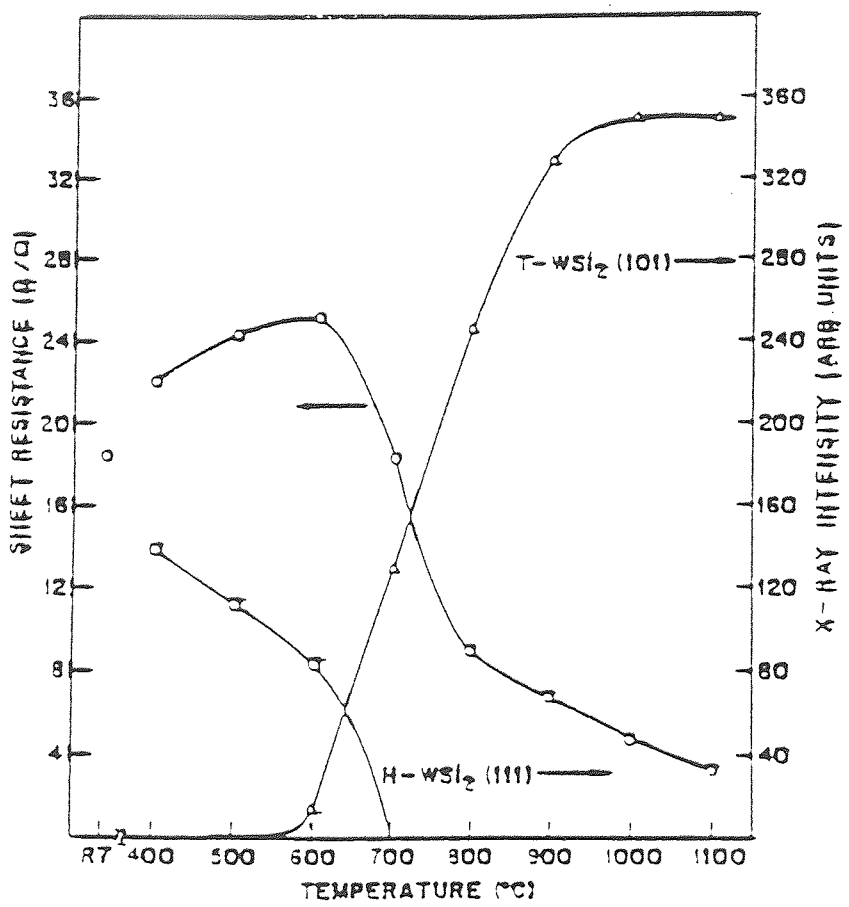

Figure 3.2 Sheet resistance as a function of sintering temperature for WSi_2

3.2.3 Stress in the Silicide Films

The silicide formation results in a net volume shrinkage. This could cause a large tensile stress in the silicon films leading to a concern about the mechanical stability of the structures at the siliciding temperatures or later during further processing. A measure of the stress in the film is therefore necessary. The behavior of the room temperature stress, resulting from high temperature sintering of metal on polysilicon films, is different for different metals. For titanium and tantalum,

the stress tends to be compressive after low temperature sintering. This type of behavior has been attributed to the interstitial silicon and or/oxygen diffusion in the metal[25]. In purer ambients tantalum films show much less stress. At high temperatures, stress increases and finally becomes tensile and is independent of sintering temperature. One way to lower the stress is to cosputter disilicides in the Si/Metal ratio of 2 or slightly greater than 2. It has been found that this leads to comparatively lower stress.The following observations are made for CVD tungsten silicide[26]:

1) The stress of CVD tungsten silicide film is a tensile stress of the order of 10^9 dynes/cm.

2) The stress of CVD tungsten silicide film decreases when the Si/W composition ratio increases.

3) The residual stress after nitrogen annealing reaches a maximum value at 500°C, starts decreasing at 600°C or higher and reaches a minimum value at 800°C.

3.3. Electrical Properties of Schottky Barrier Contacts

The first practical semiconductor device was the metal-semiconductor contact in the form of a point contact rectifier, that is, a metallic whisker pressed against a semiconductor surface. In 1938, Schottky suggested that the rectifying behavior could arise from a potential barrier as a result of stable space charges in the semiconductor. The model arising from this consideration is known as the Schottky barrier. We discuss briefly in sections 3.3.2 and 3.3.3, about the energy-band diagrams and the current transport mechanisms in the Schottky barrier contacts.

3.3.1 Energy Band Diagrams for Schottky Barrier

The surface parameters in the energy-band diagram are work function Φm of a metal and the electron affinity χ of a semiconductor. The work function is the energy difference between the Fermi energy and the ionization energy , and the electron affinity is measured from the bottom of conduction band to the vacuum level. Typical values of ϕ for very clean surfaces are 4.55eV and 3.8eV for W and Ta respectively[27]. These values may have different values due to surface dipoles of unequal magnitudes and other related reasons.

When a metal with work function qΦm is brought in contact with a semiconductor having a work function qΦs, charge transfer occurs until the Fermi levels align at equilibrium figure 3.3. When Φm> Φs, the semiconductor Fermi level is initially higher than that of the metal before contact is made. To align the two fermi levels, the electrostatic potential of the semiconductor must be raised(i.e., the electron energies must be lowered) relative to that of the metal. In the n-type semiconductor of Figure 3.3a, a depletion region W is formed near the junction. The positive charge due to uncompensated donor ions within W matches the negative charge on the metal[28]. The electric field and the bending of the bands within W are similar to effects of the p-n junction. Figure 3.4 rates a Schottky barrier on a p-type semiconductor, with Φm<Φs. In this case, aligning the Fermi levels at equilibrium requires a positive charge. The Fermi level is initially higher than that of the metal before contact is made. To align the two fermi levels, the electrostatic potential of the semiconductor must be raised(i.e., the electron energies must be lowered) relative to that of the metal. In the n-type semiconductor of Figure 3.3a a depletion region W is formed near the junction. The positive charge due to uncompensated donor ions within W matches the negative charge on the metal[28]. The electric field and the bending of the bands

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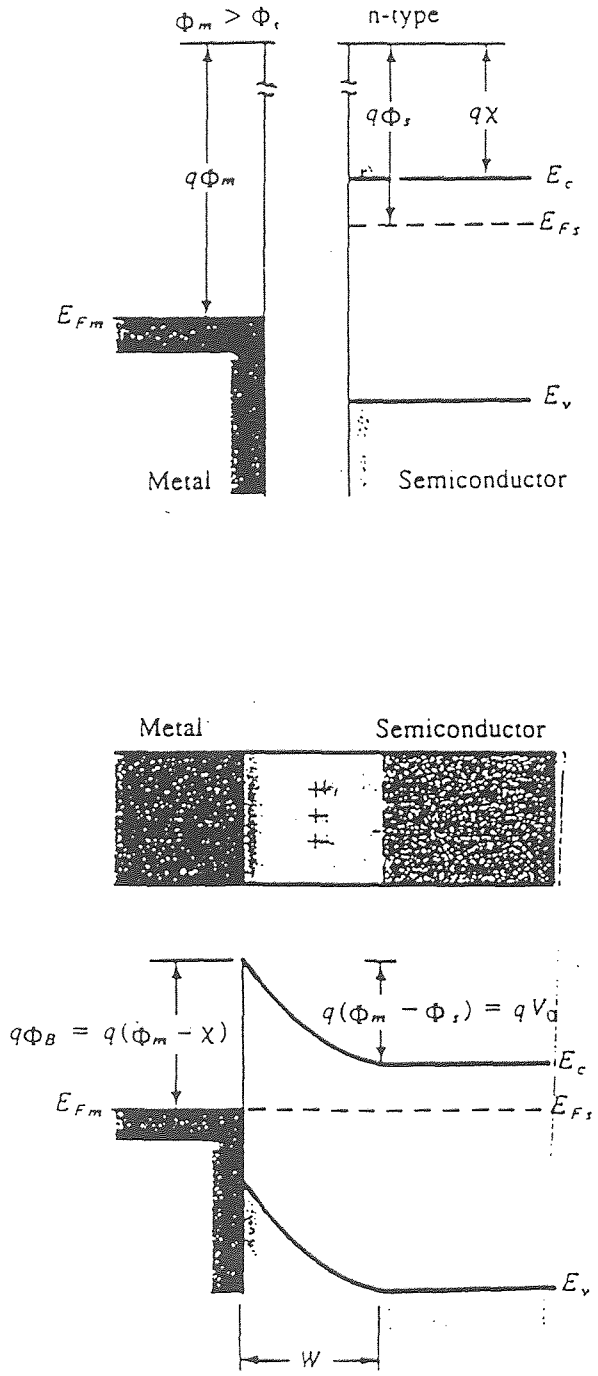

Figure 3.3 Schottky barrier formed by contacting an n-type semiconductor with a metal having large work function:(a) band diagrams for the metal and the semiconductor before contact; (b) equilibrium band diagram after contact.

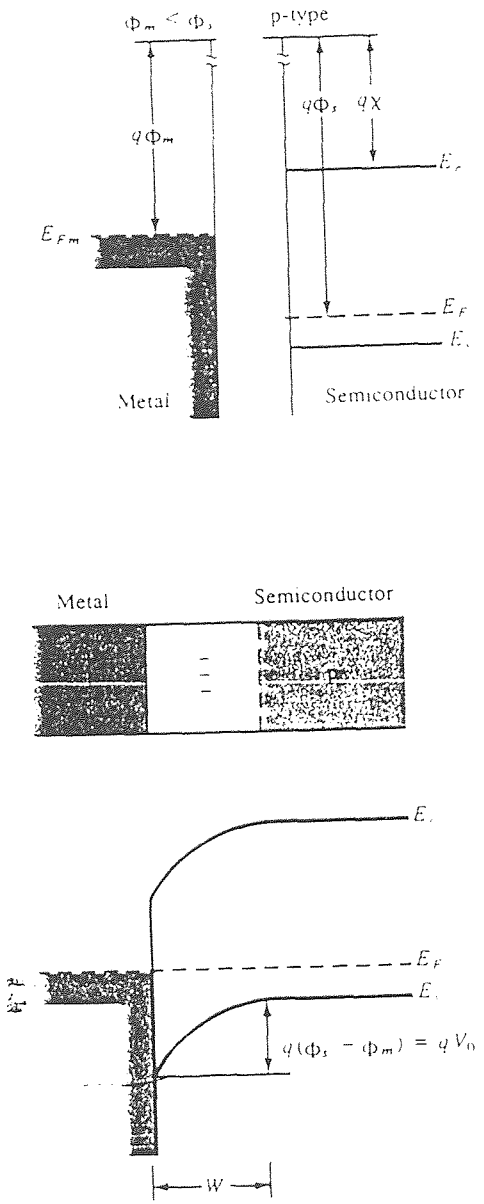

Figure 3.4 Schottky barrier between p-type semi-conductor and a ,metal having a smaller work function:(a) band diagrams before contact; (b) band diagram after contact at equilibrium.

on the metal side and a negative charge on the semiconductor side of the junction. The negative charge is accommodated by a depletion region W in which ionized acceptors(Na^-) are left uncompensated by holes. The potential barrier Vo retarding

hole diffusion from the semiconductor to the metal is Φs-Φm, and this barrier can be raised or lowered by the application of the voltage.

When a forward-bias voltage V is applied to the Schottky barrier of figure 3.3a, the contact potential is reduced from Vo to Vo-V (figure 3.5a). As a result, the electrons in the semiconductor conduction band can diffuse across the depletion region to the metal. This give rise to a forward current through the junction. Conversely, a reverse bias increases the barrier to Vo+Vr, and electron flow from semiconductor to metal becomes negligible. In either case, flow of electrons from the metal to the semiconductor is retarded by the barrier Φm -χ.

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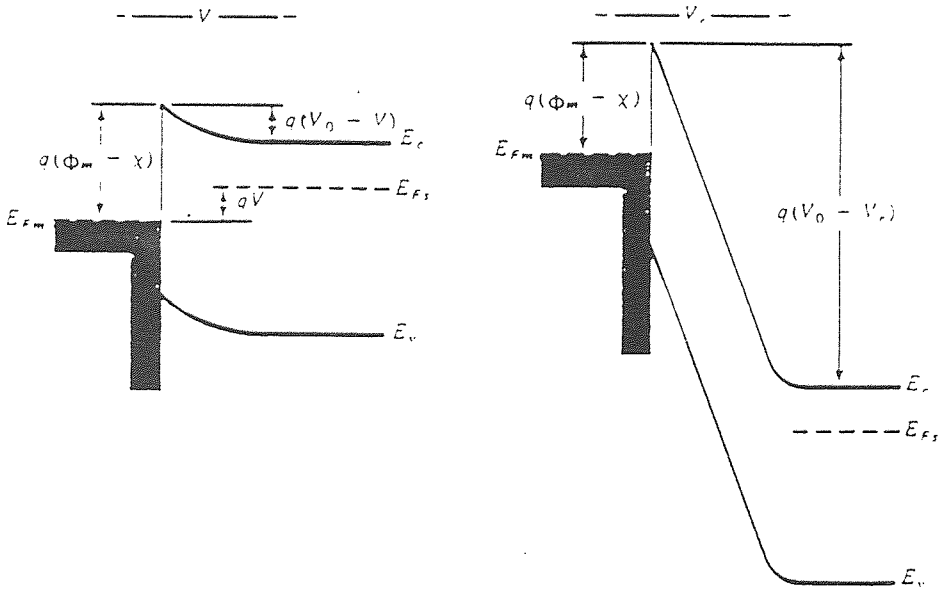


Figure 3.5 Effects of forward and reverse bias on the junction of fig3.3 (a) forward bias; (b) reverse bias.

Assuming that there is no interfacial layer existing between a metal and semiconductor, when an electron approaches a metal, the requirement that the electric field must be perpendicular to the surface enables the electric field to be considered as if there were a positive charge located at the mirror image of the electron with respect to the surface of the metal. When this sort of image force is combined with an applied electric field, the effective metal work function is somewhat reduced. This phenomenon has been described as Schottky effect which is the image force induced lowering of the potential energy for charge carrier emission when an electric field is applied. The image potential energy has to be added to the potential energy due to the Schottky barrier. If there is an insulating layer between the metal and semiconductor, the potential due to the image force will be much more complicated. Because the image force lowering contributes to modification to the barrier height of the Schottky structure, even in a perfect contact without interfacial layer, the barrier height is still reduced as a result of the image force by an amount of $\Delta\Phi$[29].

3.3.2 Surface Effects and Recombination-Generation Phenomena on Metal-Semiconductor Contacts

The surface effects are indeed of great importance in determining the I-V characteristics of metal-semiconductor contacts because the current-voltage characteristics of metal-semiconductor contacts usually deviate from the ideal case. Many of the non-ideal characteristics of metal-semiconductor contacts can be understood in terms of the properties of the space-charge region at the edge of the contacts.

We have considered the basic energy band diagrams of metal-semiconductor contacts in section 3.3.2. The Schottky-Mott model, described in 3.3.2, is based on the Schottky-Mott theory which is an ideal case. In most

practical metal-semiconductor contacts, the ideal situation is never reached because there is a thin insulating layer of oxide on the surface of the semiconductor. Such an insulating film is often referred to as an interfacial layer. The Bardeen model[30] represents a good insight into the general features of the interface state behavior. It supposes that there are localized states at the insulator-semiconductor interface. It has the merits of being easy to analyze and corresponds to the real situations of metal-semiconductor contacts. A detailed energy-band diagram of a metal n-type semiconductor contact is therefore more like that as shown in the figure 3.6.

In the presence of surface states, the neutrality condition becomes $Q_M = -(Q_{SS} + Q_{SC})$. There are three distinct sources of charge in the system: Q_M resides on the surface of the metal, Q_{SC} is due to the uncompensated donor ions in the depletion region and Q_{SS} is due to the electrons in the surface states. Q_m is determined by the electric-field strength in the insulating layer, Q_{SC} by the width of the depletion region and the density of donors, and probability. These three charge densities are the important factors describing the phenomena on surface effects.Q_{SS} is determined by the density of interface states and by their occupation probability. These three charge densities are the important factors describing the phenomena of surface effects.

The depletion regions and the corresponding energy-band diagrams are different for various bias conditions. The flat-band voltage can be considered as a voltage which is just sufficient to overcome the "built-in" voltage due to the metal-semiconductor work-function difference and surface state charge Q_{SS}. The energy band comes up flat to the surface and the potential barrier at the edge of the metal contact looks the same along the surface. When a bias, is more negative than

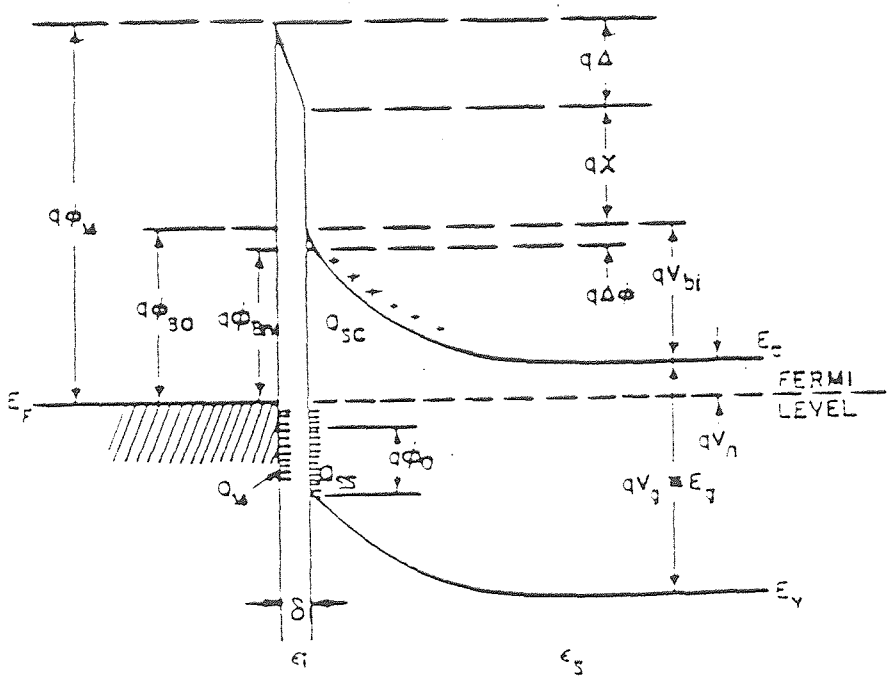


Figure 3.6 Detailed energy band diagram of a metal n-type semiconductor contact with an interfacial layer of the order of atomic distance(all symbols have their usual meanings)[31].

the flat-band voltage is applied, a surface depletion layer is formed. It is continuos with the depletion layer of the metal-semiconductor contact. If a bias, further more negative than the flat band voltage is applied, the surface depletion region is widened and a layer of strong inversion is formed. If a bias more positive than flat-band voltage is applied, the energy band is bent down at the surface, forming an accumulation layer and causing the potential barrier of the metal-semiconductor contact to be narrower in the direction along the surface. The forward as well as the reverse I-V characteristics of metal-semiconductor contacts can be substantially modified by varying the applied voltage and, consequently,change the condition of the space charge region where it intersects the surface.

In earlier studies about Schottky barrier-contacts have represented the experimental results of the current components in the metal-semiconductor contacts. The phenomena and the importance of recombination in the space-charge region have been demonstrated by Yu and Snow[32]. They showed that both forward and reverse currents of a metal-semiconductor contact increase to a higher level when the surface around the contact is inverted. This increase is due to generation-recombination currents associated with the field-induced junction. When the positive bias is applied and the surface is accumulated, excess current will appear. The forward excess current will be relatively less important as the forward bias is increased. The surface may be accumulated by the positive interface charge Q_{SS} or by positive ions in the oxide or on the oxide surface. Depending on the surface conditions, a given metal-semiconductor contact may have widely different I-V characteristics. The surface condition is determined by the amount of charge on or near the surface. Because of the presence of positive surface state charge at the interface and positive ions in or on the oxide, the surface of n-type Si is usually accumulated. The mechanism such as recombination current in the depletion region can be well understood after considering the phenomena of surface effects on metal-semiconductor contacts.

3.3.3 Current Transport Mechanisms in Schottky Structure

In this section, we discuss the transport mechanisms that determine the conduction properties of Schottky barriers. Here, it is assumed that a barrier has been established and we assume nothing about the factors which determine the height of this barrier. Because of their importance in direct current and microwave applications and as tools in the analysis of important fundamental physical parameters such as the magnitude of the barrier heights, metal-semiconductor contacts and the mechanisms of current transport through the contacts have been

studied extensively. The current transport in metal-semiconductor contacts is mainly due to majority carriers. Many theories that describe the role of metal-semiconductor interface have been developed. The various ways in which electrons can be transported across a metal-semiconductor junction under forward bias, are shown schematically for an n-type semiconductor in figure.3.7. The inverse processes occur under reverse bias. The four mechanisms are:

(1) Emission of electrons from the semiconductor over the top of the barrier into the metal (this process is dominant for Schottky contacts with moderately doped semiconductors operated at 300 K);

(2) Quantum-mechanical tunneling through the barrier;

(3) Recombination in the space-charge region;

(4) Recombination in the neutral region('hole injection' from metal to semiconductor).

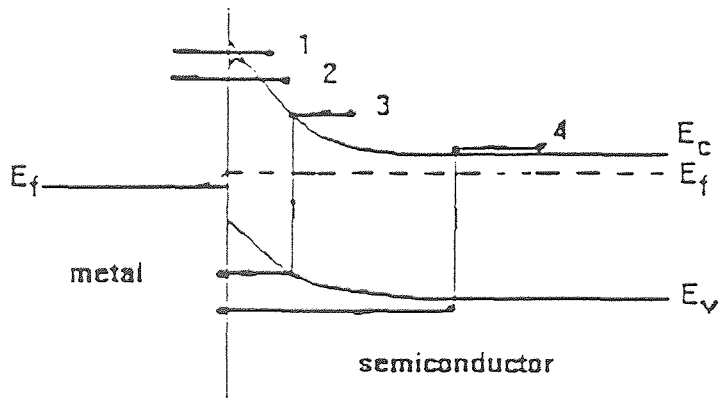


Figure 3.7 Four basic transport processes under forward bias[31].

The main question is to solve these fundamental issues whether the current is limited by the process of thermionic emission of electrons from the semiconductor into the metal, as was considered by Bethe, or whether it is limited by drift and diffusion of electrons through the space charge region, as was suggested in the original works of Schottky and Spenke or Mott. It is possible to make practical Schottky-barrier contacts in which process (1) was the most important and such contacts are generally referred to as "nearly ideal". The I-V characteristics of metal-semiconductor contacts are often termed "ideal" if they can be described in the process of thermionic emission of conduction electrons over the interfacial potential barrier alone. Processes (2), (3), and (4) (see page 30) usually are the important factors causing the departures from the so called ideal behavior.

For Schottky contacts with moderately doped semiconductors operated at moderate temperatures, the dominant mechanism is thermionic emission of majority carriers from the semiconductor over the potential barrier into the metal. Figure 3.8 illustrates the thermionic emission process. At thermal equilibrium , the current density is balanced by two equal and opposite flows of carriers, thus there is zero net current. Electrons in the semiconductor tendto flow (or emit) into the metal, and there is an opposing balanced flow of electrons from the metal into the semiconductor. These current components are proportional to the density of electrons at the boundary. At the semiconductor surface, the electron density n_S is

$$ns = N_D \exp\left[\frac{-qV_{Bi}}{KT}\right] = N_D \exp\left[\frac{-q(\Phi_{Bn} - Vn)}{KT}\right]$$

$$= N_c \exp\left[\frac{-q\Phi_{Bn}}{KT}\right]$$

where Nc is the density of states in the conduction band. At thermal equilibrium we have

$$|Jm \rightarrow s| = |Js \rightarrow m|\alpha n_s$$

$$|Jm \rightarrow s| = |Js \rightarrow m| = C_1 Nc \exp\left[\frac{-q\Phi bn}{KT}\right]$$

or

$$|Jm \rightarrow s| = |Js \rightarrow m| = C_1 Nc \exp\left[\frac{-q\Phi bn}{KT}\right]$$

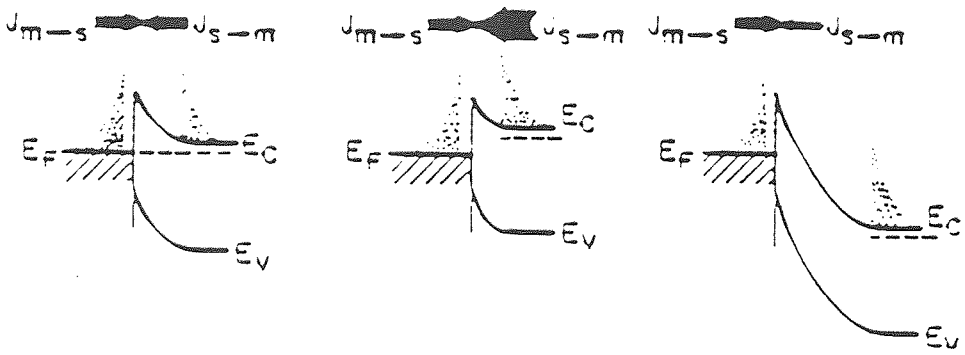


Figure 3.8 Current transport by thermionic emission process. (a) thermal equilibrium (b) forward bias (c) reverse bias.

where $J_{m \rightarrow s}$ is the current from the metal to the semiconductor, Js→m is the current from the semiconductor to the metal, and C1 is a proportionality constant.

When a forward bias VF is applied to the contact, the electrostatic potential difference across the barrier is reduced, and the electron density at the surface increases to

$$n_s \cong N_D \exp\left[\frac{-q(V_{bi} - V_F)}{KT}\right] = N_c \exp\left[\frac{-q(\Phi_{Bn} - V_F)}{KT}\right]$$

The current Js→m that results from the electron flow out of the semiconductor is therefore altered by the same factor. The flux of electrons from the metal to the semiconductor, however remains the same because the barrierΦbn remains at its equilibrium value. The net current under forward bias is then

$$J = J_{s \to m} - J_{m \to s}$$

$$= C_1 N_c \exp\left[\frac{-q(\Phi_{Bn} - V_F)}{KT}\right] - C_1 N_c \exp\left[\frac{-q\Phi_{Bn}}{KT}\right]$$

$$= C_1 N_c \exp\left[\frac{-q\Phi_{Bn}}{KT}\right] \left(e^{qV_F / KT} - 1\right).$$

Using the same argument for the reverse bias conditions, the expression for the net current is identical to equation except that V_F is replaced by $-V_R$. The coefficient C_1N_c is found to be equal to A^*T^2, where A* is called the effective Richardson Constant (in units of $A/K^2\text{-}cm^2$), and T is the absolute temperature. The values of A* depend on the effective mass and are equal to 110 and 32 for n- and p- type

silicon, respectively. The current voltage characteristic of a metal-semiconductor contact under thermionic emission condition, is therefore, is given by

$$J = Js\ (\exp\ qv/KT\ -\ 1)$$

and

$$Js = A^*\ T^2\ \exp(-q\ bn/KT)$$

where Js is the saturation current density and the applied voltage V is positive for forward bias and negative for reverse bias. The obtained experimental I-V curves for samples studied here are presented in chapter 5.

CHAPTER 4

RAPID THERMAL PROCESSING

4.1 Introduction

In recent years, there has been two major trends in semiconductor processing : The reduction in device dimensions to increase speed and packing density and larger wafer sizes to increase the number of circuits per wafer and thus reduce processing costs Both of these trends have begun to put constraints on (a) batch mode processing and (b) thermal budget (product of temperature and time) that a wafer can be subjected to. As device dimensions are reduced, junction depths must also shrink and dopant diffusion must be precisely controlled. This demands that the thermal processing, during and subsequent to the doping steps, minimize dopant diffusion. This can be done by reducing the temperature of a particular step or minimizing the time at temperature. In a conventional furnace, it is difficult to reduce the time accurately because of the thermal stresses, the effects of radial heating and cooling and the large thermal mass of a boat load of wafers. Lowering the temperature can result in excessive process times or, if the activation energy of a particular step is large, the desired result(low sheet resistance, damage annealing,etc) will not be achieved.

The trend towards larger wafers will require more uniform heat treatments across a wafer. Due to edge heating and cooling in a standard furnace, uniform heat treatments will be more difficult. Also as wafers get larger, the value of a wafer at any step will be greatly increased. Serial and real time feedback of a thermal step could prevent a devastating process mistake from ruining an entire lot of wafers.

RTP was developed to overcome all these problems. In this case, a single wafer is heated to temperatures of 400 to 1440°C (depending on the process desired) for times of the order of 1 to 120sec. In this process, the wafers are thermally isolated from the chamber and the heating and cooling are by radiation. The temperature and time can be well controlled on a given wafer and wafer-to wafer.

4.2 An Ideal RTP Unit

An illustration of RTP model for this experimental work is shown in figure 4.1. The model RTM-2016-M-2F-VAC-FC-TU-SP(208) is designed to process two(2), three(3), or four(4) inch diameter samples, one at a time. It is capable of providing temperature excursions from room temperature to 1250° at heating rates of upto 300°C/sec and cooling rates of approximately 100°C/sec. The specimen can be held at constant temperatures accurately within +/-2.5°. Two process gas flow paths are provided:- one designed for nitrogen gas at upto four(4) standard liters per minute, and one designed for forming gas at upto one(1) standard liter per minute. Specimen temperature and gas flow paths are automatically controlled by a built in programmable controller. Gas flow rates are controlled by setting rotameters on the front of the process chassis. A turbo molecular pump and roughing pump provide vacuum in the chamber to approximately $1x10^{-6}$ torr.

The Model RTM-2016-M-2F-VAC-FC-SP(208) consists of:

- Quartz process chamber with a manually operated door
- Process gas plumbing system
- Specimen heating system
- Specimen water cooling system
- Lamp cool system

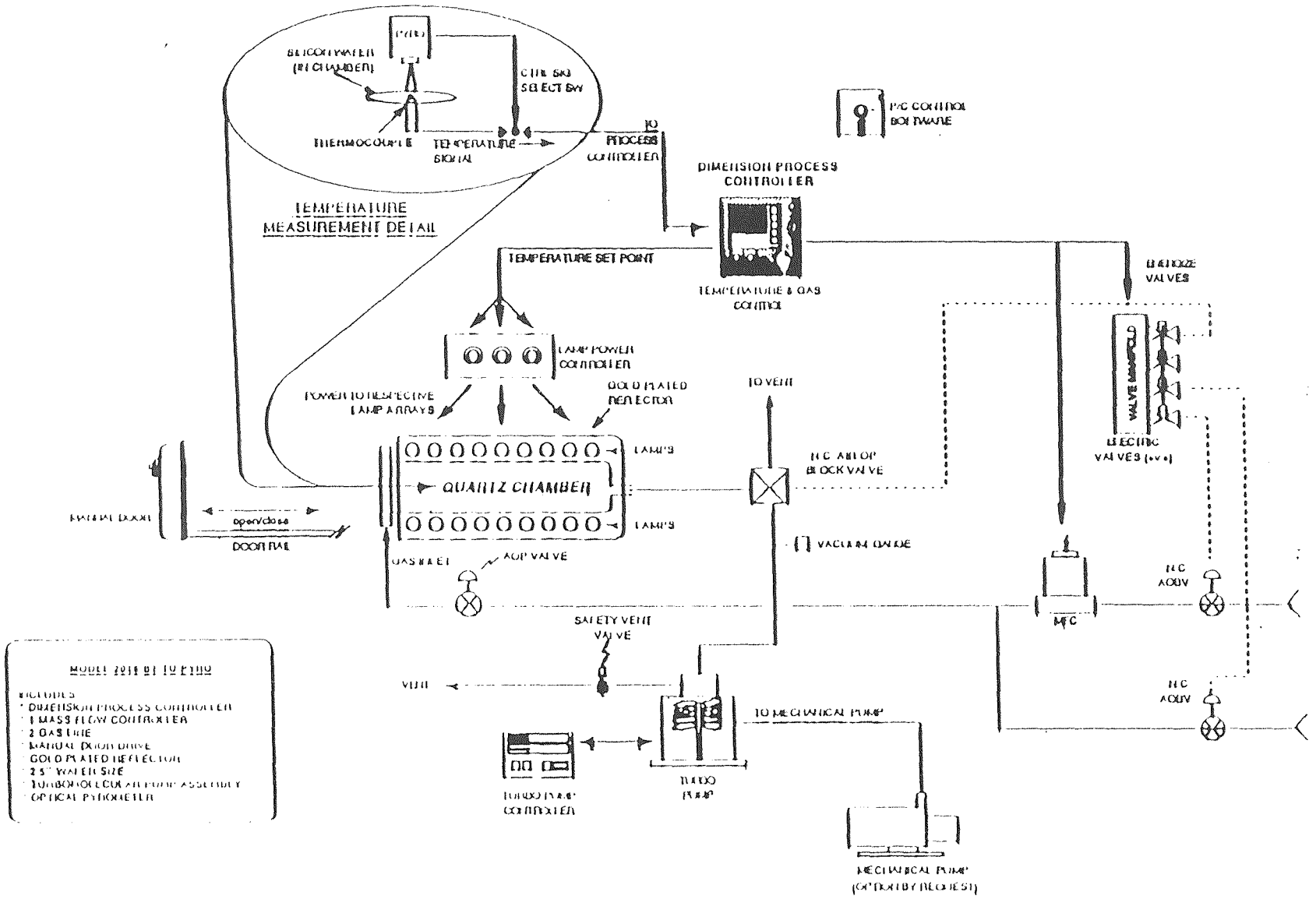


Figure 4.1 Process Controller RTM-2016-M-2F-VAC-FC-TU-SP

- Control panel with a programmable MICRISTAR controller.
- A.C. power system
- Automatic process controller
- Vacuum option(valve and piping,connected to a turbo molecular pump with roughing pump including an ion gauge controller with integral thermocouple gauge control.
- "Emergency off" switch
- Two "monitor-only" thermocouples, with separate jacks on the rear of the process chassis.
- Cabinet to house all other components.(Except the roughing pump)

4.2.1 Principle of Operation

RTP is an Isothermal Process. A specimen is placed in the process chamber and provided with a non-oxidizing atmosphere(nitrogen or forming gas) or, using a turbo molecular pump with roughing pump, provided with a reduced pressure atmosphere. The Process Product Corporation Rapid Thermal Module has a Research Incorporated "Micristar" controller for its control unit. The specimen placed onto specimen holder extends from the chamber door toward the chamber. There are three thermocouples extending through the door. The center thermocouple is the control thermocouple,and must be positioned properly before the system is operated. The two thermocouples adjacent to the center position are provided for remote monitoring only. When the door is closed, a micro-switch closes which enables the system. The system provides the specimen with a non-oxidizing atmosphere while the specimen is heated or cooled as required for the process. The system also includes a vacuum valve which provides connection to the vacuum pump for reduced pressure processing. The valve is automatically controlled by the Micristar controller. The vacuum valve works in conjunction with a vent valve, so that one or the other is open. The Micristar controller is used

to control the temperature of a specimen by providing an analog "set point" output to a Control Concepts S.C.R. power controller. The power controller provides power to tungsten halogen lamps arranged on the top and bottom of the quartz chamber. The lamps are designed to provide infra red(I.R) energy which is passed through the quartz chamber, either directly or after being reflected by the reflector, onto the specimens being processed. Various safety locks are provided with the system to inhibit operation in the event of an undesirable situation.

Table 4.1 Comparison of furnace and RTP features

Feature	**RTP**	**Furnace**
Thermal Mass	Low	High
Batch Size	Single Wafer	Large Batch
Cluster Applications	Natural	Difficult
Turn-Around Time	Short	Long
Test Wafers	Practical	Impractical
Throughput & Cost	Can be O.K.	Advantage
Risk	Low	High
Familiarity	More needed	Excellent
Submicron Production	Compatible	Some Limits
Rapid Start & Stop	Key Capability	Unsuited
Vacuum & Gas Flow	Easy	Suited
Contamination	Minimum	Difficult
Radiation Hardening	Weakened	Less Affected

4.3 Applications of RTP

RTP has been applied to a variety of thermal processing steps:

(a)Metallization/Silicidation: Formation of self-aligned silicide films, formation of refractory metal nitrides, aluminum-silicon alloy, reduction of contact resistance, Ohmic contact anneal, CVD deposition/alloy, reduction of junction leakage. The short anneal cycle associated with RTP eliminates the unwanted lateral silicidation that results in poor line width control, a common occurrence in furnace processing. RTP contact alloying, due in large part to the short time and high temperatures of the process, reduces hillocks, spikes, and epitaxial silicon re- growth in the contact areas.

(b)Ion Implantation: Removes damage, shallow junction formation, lower sheet resistance, lower sheet resistance uniformity, dopant activation, process control. The short time cycle of RTP minimizes the diffusion of dopants, which preserves the junction depth defined by ion implantation. The capability to produce temperatures higher than a furnace effectively removes most of the crystal damage caused by implantation, thereby reducing junction leakage.

(c)Thin gate Dielectrics: Rapid thermal growth of oxides,nitrides, and oxynitrides, improvement of chemical, mechanical and electrical properties, annealing of gate insulator charges, reduction of carrier trapping, annealing of process-induced radiation damage, and increase of breakdown voltage.

To grow silicon dielectrics in the 20-150 Angstroms range, at temperatures in excess of 1000^{o}C requires the short,precise time cycles available only with RTP. RTP dielectrics demonstrate better electrical characteristics than furnace-assisted dielectrics. Since the chamber is quartz and isolates the wafer from the metal chamber walls, metallic ion contaminants are eliminated.

(d)Devices: Increased device speed, reduced leakage current, improvement of avalanche breakdown voltage

(e)Polysilicon/Thin glass films: Activation of implanted species, reduction of sheet resistance, oxidation, in-situ doping, controlled dopant diffusion, shallow junction formation using doped surfaces.

(f)Bulk silicon: Thermal donor annihilation, annealing of RIE-induced defects, oxygen precipitation, lattice damage repair, gettering.

CHAPTER 5

RESULTS AND DISCUSSION

5.1 Introduction

This chapter presents the details of the present experimental work. These include the current-voltage measurements of samples W on p-Si and $TaSi_2$./p-si. These samples are then annealed using RTP techniques leading to the formation of WSi_2 and $TaSi_2$ on silicon. Current-voltage measurements are performed on these annealed samples at different temperatures and are analyzed with the conventional Schottky-Mott theory. A computer model for calculation of current-voltage characteristics is developed with a view to interpret the experimental results. The programs for different measurement temperatures are given in the Appendix. The sheet resistance measurements are also performed on these samples, using the Four-point probe method.

5.1.1 Experimental Process Details for WSi_2

Tungsten Silicide films have been prepared on p-type (100) Si wafers with 5-10Ω cm resistivity. Prior to the metal deposition, the samples were RCA cleaned, dipped in HF solution and rinsed in deionized water. Tungsten film is deposited using CVD techniques. This process is carried out in a LPCVD reactor at 0.1 to 0.2 torr for a temperature of 500 to 600°C by reduction of WF_6. Thickness of the films deposited is found to be 7000A. These samples are then patterned by photolithography using self designed mask and the samples are then annealed using RTP at 5x10-5 torr for 30seconds for temperatures ranging from 500°C to 700°C.The process travellers sheets are given in appendix.

5.1.2 Experimental Process Details for $TaSi_2$ /p-si

$TaSi_2$ films were prepared on p-type (100) Si wafers with resistivity of 5-10Ωcm . The samples are RCA cleaned prior to the metal deposition. $TaSi_2$/p-si is deposited using Sputtering techniques. The thinckness of the metal film is found to be 3000A. The samples are then annealed in RTA to form a proper contact with the Si. The process details are given in the appendix. In both cases WSi2/p-si and TaSi2/p-si. The devices are circular in geometry with diameter of 2mm.

5.1.3 Current-Voltage Measurements

Each of the samples used for the measurements contain approximately 100 devices. The results in this study represent an average of 20 measurements per sample. Current-Voltage measurements for these devices are performed using a Keithley 236/237 source Measurement Unit(SMU) with a sophisticated computer data acquisit software Model251. The setup consists of a computer configured through an IEEE interface to Keithley hardware which supplies voltage in steps to the samples placed in the probe station. The voltage sweep was carried out in steps of 10mv and the compliance value of 10mA was fixed to protect the devices. Extreme care was taken during the I-V measurements so that the devices were not excited or disturbed by light in the probe station to obtain accurate results. Maximum voltage of 1V was applied to test the devices.Both forward and reverse bias voltages ranging from -0.3V to 0.3V were applied..

5.1.4 Sheet Resistance Measurements

Sheet resistance measurements were done using Four-point probe method.The measured sheet resistances values are plotted as a function of annealing temperatures.

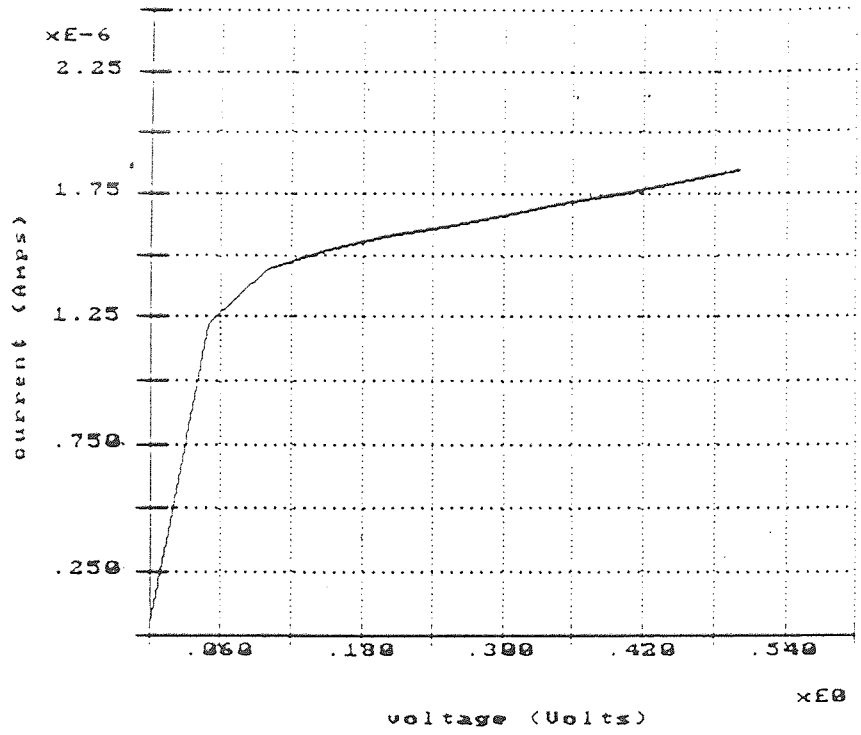


Figure 5.1 Experimental result of I-V characteristics for $TaSi_2$ /p-si before annealing.

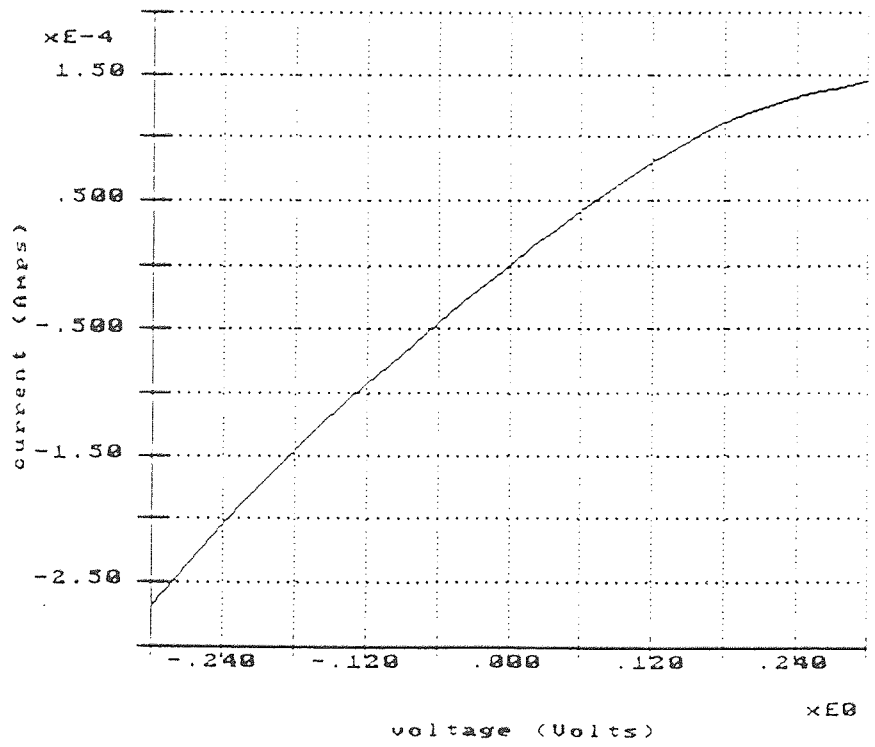


Figure 5.2 Experimental result of I-V characteristics for $TaSi_2$ /p-si after 500°C. anneal for 30sec.

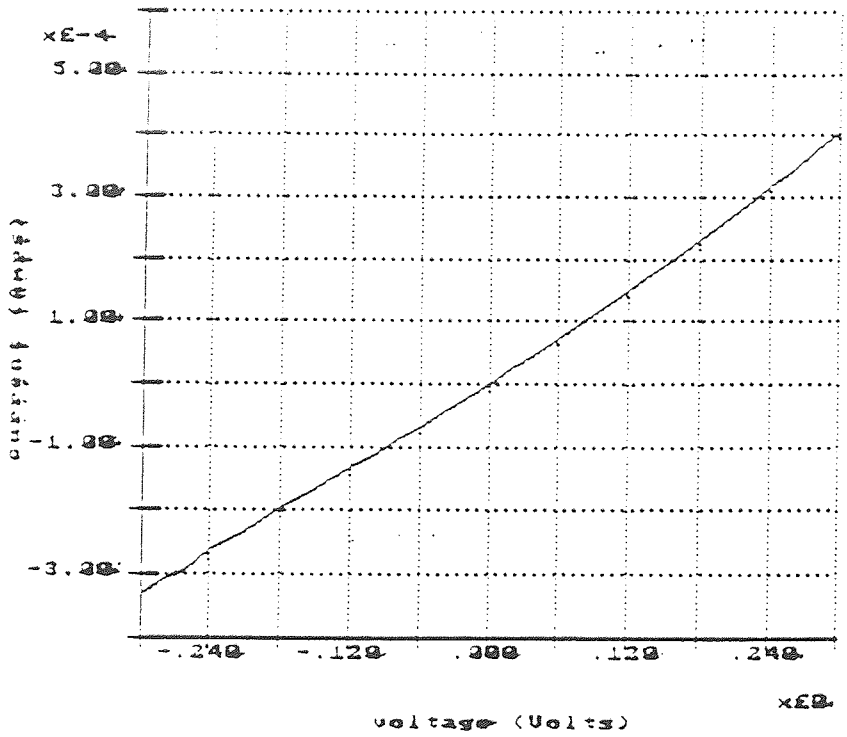


Figure 5.3 Experimental result of I-V characteristics for $TaSi_2$ /p-si after 600°C anneal for 30sec.

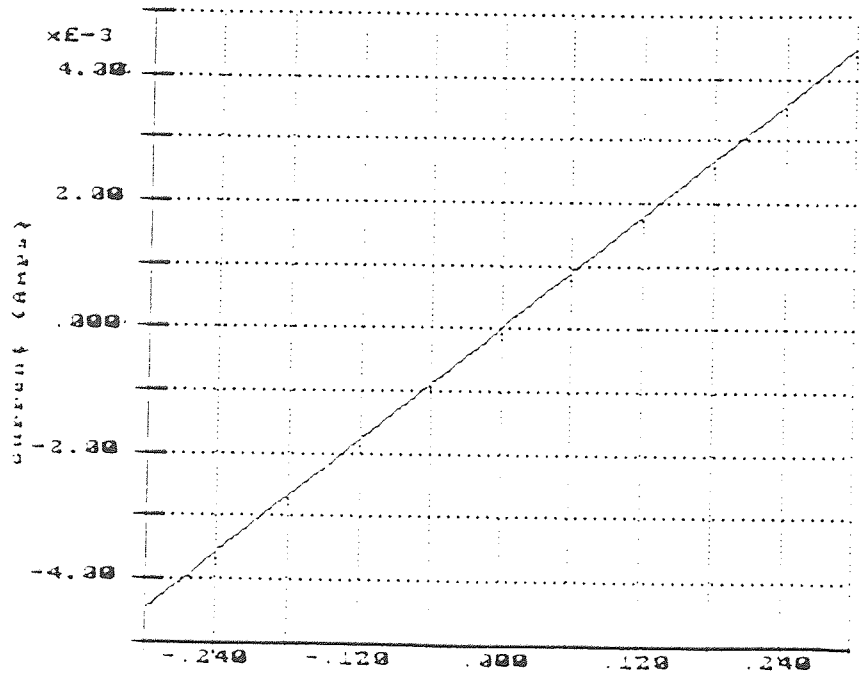


Figure 5.4 Experimental result of I-V characteristics for $TaSi_2$ /p-si after 700°C anneal for 30sec.

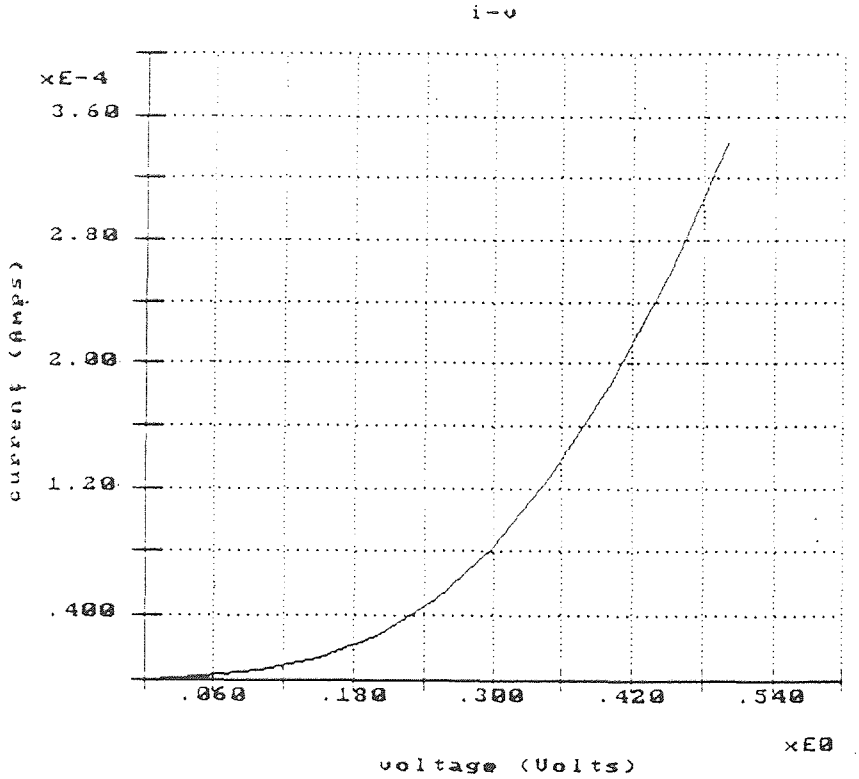


Figure 5.5 Experimental result of I-V for WSi_2 /p-si before anneal

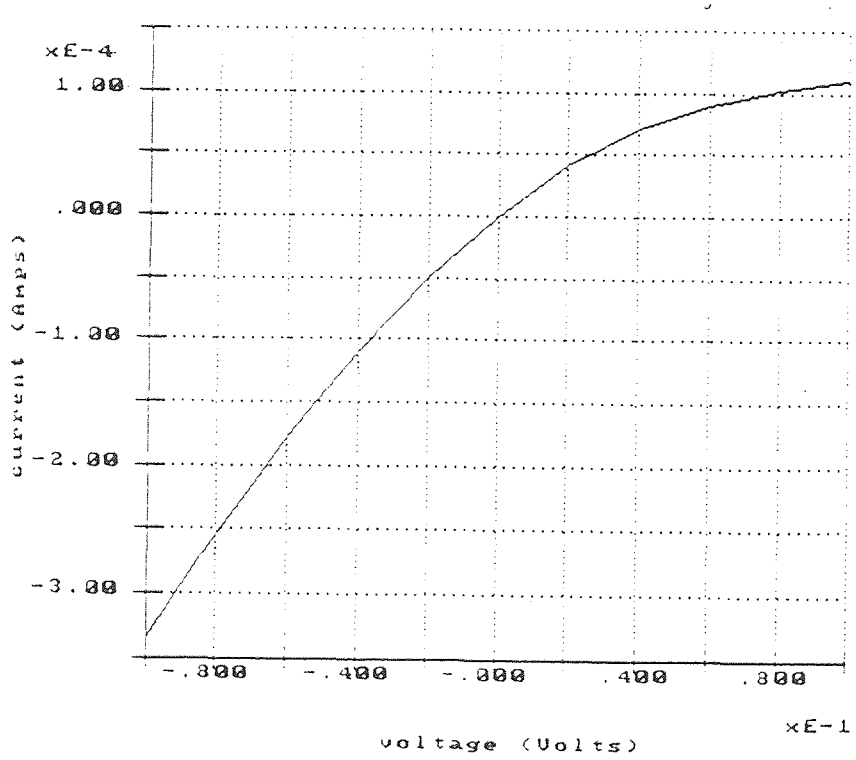


Figure 5.6 Experimental I-V characteristics for WSi_2 /p-si after 500°C anneal for 30sec.

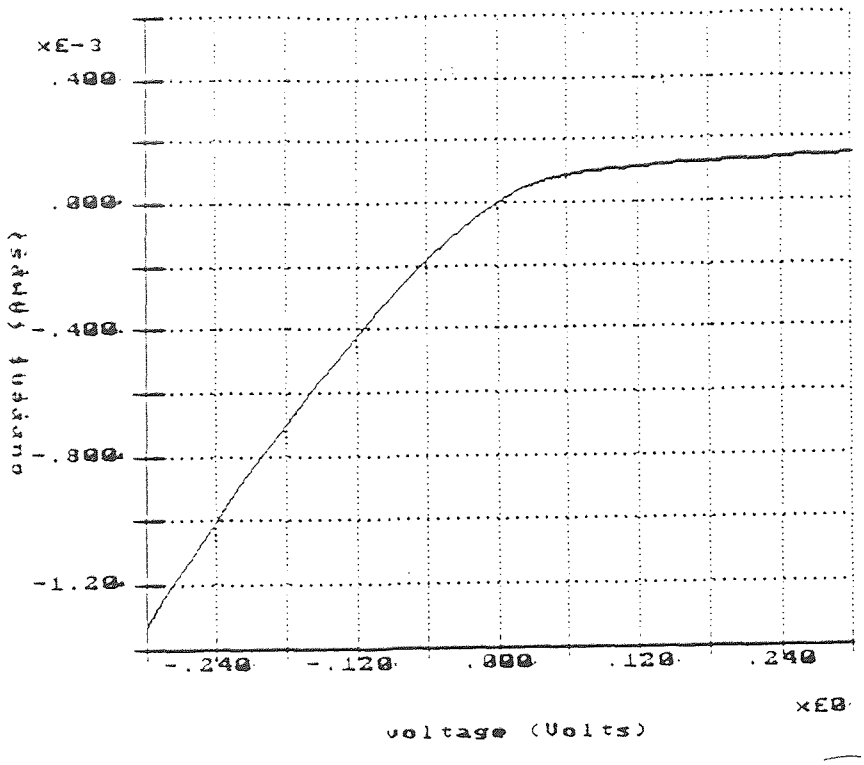


Figure 5.7 Experimental I-V characteristics for WSi_2 /p-si after 600°C anneal for 30sec.

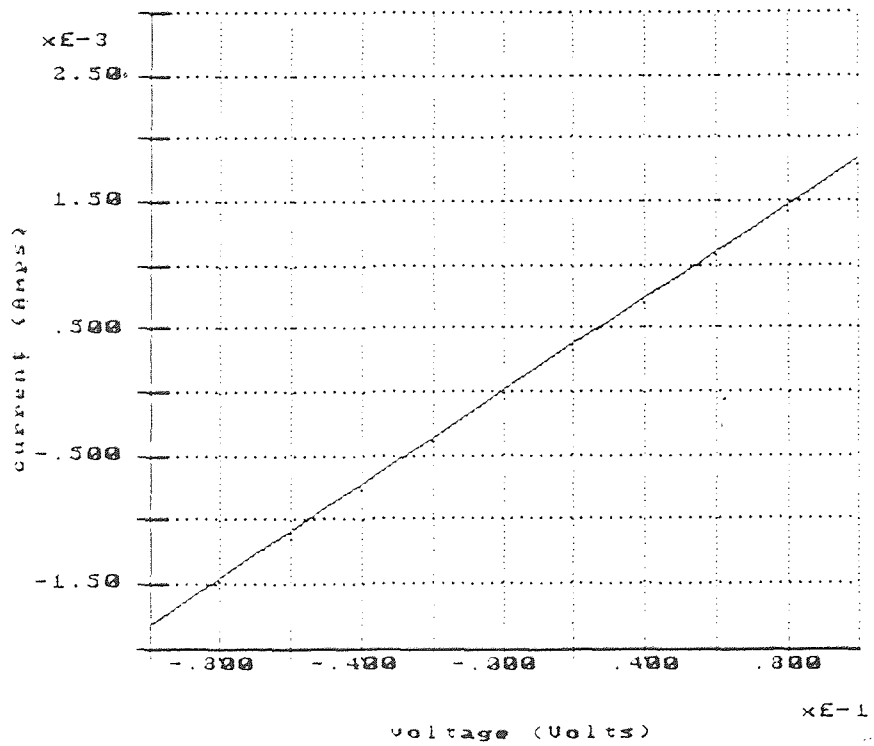


Figure 5.8 Experimental I-V characteristics for WSi_2 /p-si after 700°C anneal for 30sec.

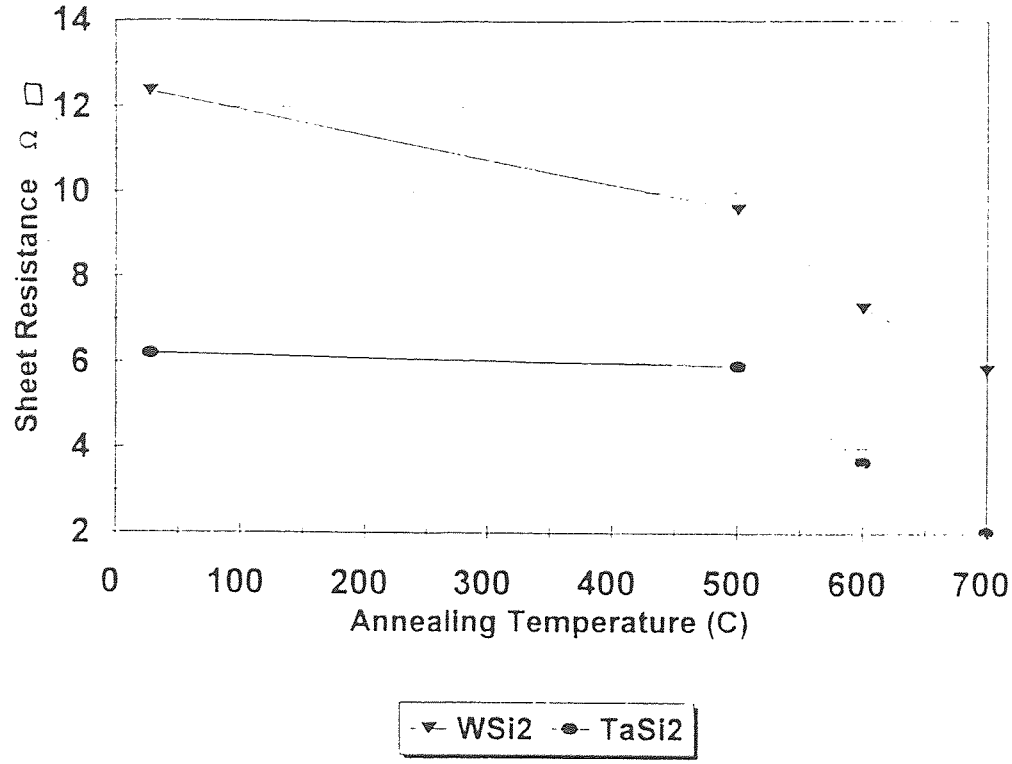


Figure 5.9 Sheet resistance Vs annealing temperature for WSi_2 /p-siand $TaSi_2$/p-si.

5.2 Discussion

As can be seen from figures 5.5 through 5.8, for W/p-si contacts, as the annealing temperature is increased, the I-V characteristics tend to be ohmic and linear. Such results are also reflected for the $TaSi_2$/p-si devices in figures 5.1 through 5.4.

Such a transition from diode like behavior to ohmic like behavior, for W on p-si, can be attributed to interaction between W and Si resulting in the formation of WSi_2. Similar studies have also been reported in the literature as shown in the figure 5.10 and the formation of WSi_2 is expected to occur at temperatures of 600° C or higher.

Figure 5.9 shows the shows the decreasing sheet resistance values with increasing anneal temperatures. This can also be evidenced from the literature as shown in the figure 5.11.

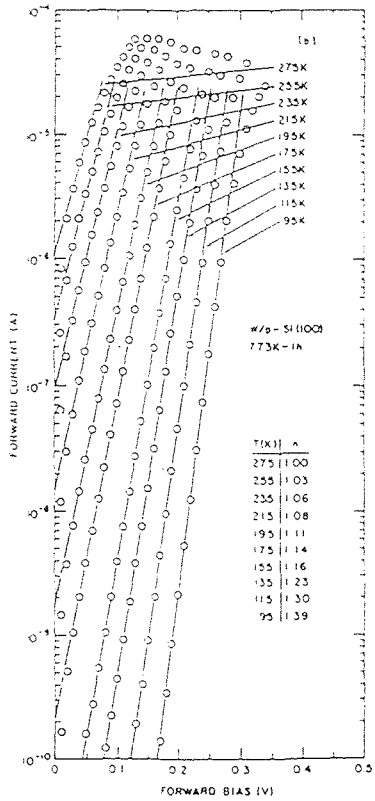


Figure 5.10 current-voltage characteristics of W on p-type si annealed at 1000°C.

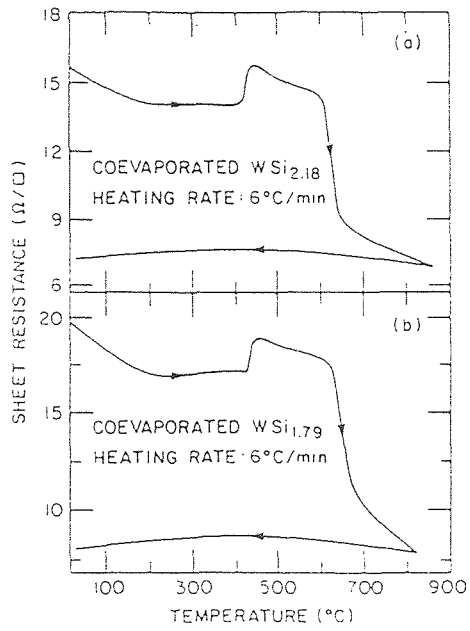


Figure 5.11 Sheet resistance curves obtained insitu from the co-evaporated WSi_2

CHAPTER 6

CONCLUSIONS

An investigation of the fabrication and characterization of (a) W on p-si and (b)$TaSi_2$ on p-si devices, and the influence of rapid thermal anneals has been presented in this study. For (a) i.e. W on si the current-voltage characteristics before anneal indicate a non-linear behavior. RTA at 500, 600 and 700°C for 30seconds yields devices whose current-voltage characteristics become linear. This can be attributed to the formation of WSi_2 on p-Si. For $TaSi_2$ on p-si, rapid thermal anneals at 500, 600, 700°C for 30seconds results in the reduction of the interface states, which further resulted in better contact formation between $TaSi_2$ and p-si as is evidenced by electrical measurements. Sheet resistance values, as function of annealing temperature, reach acceptable values. Further work is in progress to establish the chemical composition of the metal layers.

APPENDIX 1

Process Steps For Samples

Process steps for $TaSi_2$ / WSi_2

Oxide Strip

1. Add control wafer if needed
2. P-clean 5:1 H_2So_4:H_2O_2 110°C ,10 minutes.
3. Rinse hot DI water, 10min.
4. Rinse cold DI water, 5min.
5. Spin dry.
6. Oxide strip, BOE, 10min.
7. Rinse DI water, 10min.
8. Spin dry.

Sputter

1. Add control wafer.
2. Sputter pre-clean, 100:1 H_2O:HF, 1 min.
3. Rinse and spin dry.
4. Sputter $TaSi_2$, 3000A° at 3A /sec.
5. Measure the Thickness

Photo Mask 1

1. Apply photoresist.
   Program #: 1
   Resist: 53813

2. Expose.
   Mask:
   Time: 15sec.

3. Develop PR.

4. Hard bake PR at 115°C for 60seconds.

RIE - $TaSi_2$

1. Reactive Ion Etch $TaSi_2$:
   SF6: 25 sccm
   Freon 115: 75sccm
   Pressure: 150 mtorr
   Power: 600 Watts
   Time /over-etch: 10min

2. Inspect.

3. Strip PR, P-strip at 110°C for 10 min.

4. Rinse and spin dry

5. Inspect.

6. RTP at 500, 600 and 700°C.

APPENDIX 2

Keithley Instruments

Model 251 I-V Test Software

Model 251 is an sophisticated software which controls model 236/237/238 Source Measure Units (SMU).

Model 251 performs the following tests:

-FET TEST: Curve family, Threshold Voltage, Transcounductance, Breakdown and Leakage.

-BIPOLAR TEST: Curve family, Gummel Plot, Current gain, Breakdown and Leakage.

-DIODE TESTS: I-V Curve, Reverse Breakdown, Zener Voltage.

-COMPONENT TESTS: Capacitor Leakage, Resistor voltage Coefficient.

In the recent work I-V curves were obtained performing diode test, sweeping voltages Upto 3Volts. Maximum compliance value was kept at 10mA. The voltage sweep was supplied through the software model 251 which controls Model 2361(Trigger Controller). This Trigger Controller controls the amplitude and frequency of voltage, which is supplied to the text fixture. The test fixture consists of thin probes which are placed on the metallized part of the wafer while the bulk silicon part is given a low voltage. The source measure unit senses the current generated by voltage sweep which is sent to the computer through IEEE-488 interface back to computer where a I-V curve is generated.

APPENDIX 3

Programs

```
C           Programmed by:  Anitha Kodali
C           File Name       :  Thesis.c
C       To solve for current in metal-semiconductor contact (Schottky diode)
C       ************************************************************

            #include<stdio.h>
            #include<math.h>
            #define A 32
            #define Φb  0.47
            #define K  1.38e-23
            #define q  1.602e-19
            #define  n  1
            main( )
            {
            float V;
            float i;
            int T;
            for(V=0; V<=1; V+=0.05)
            {
```

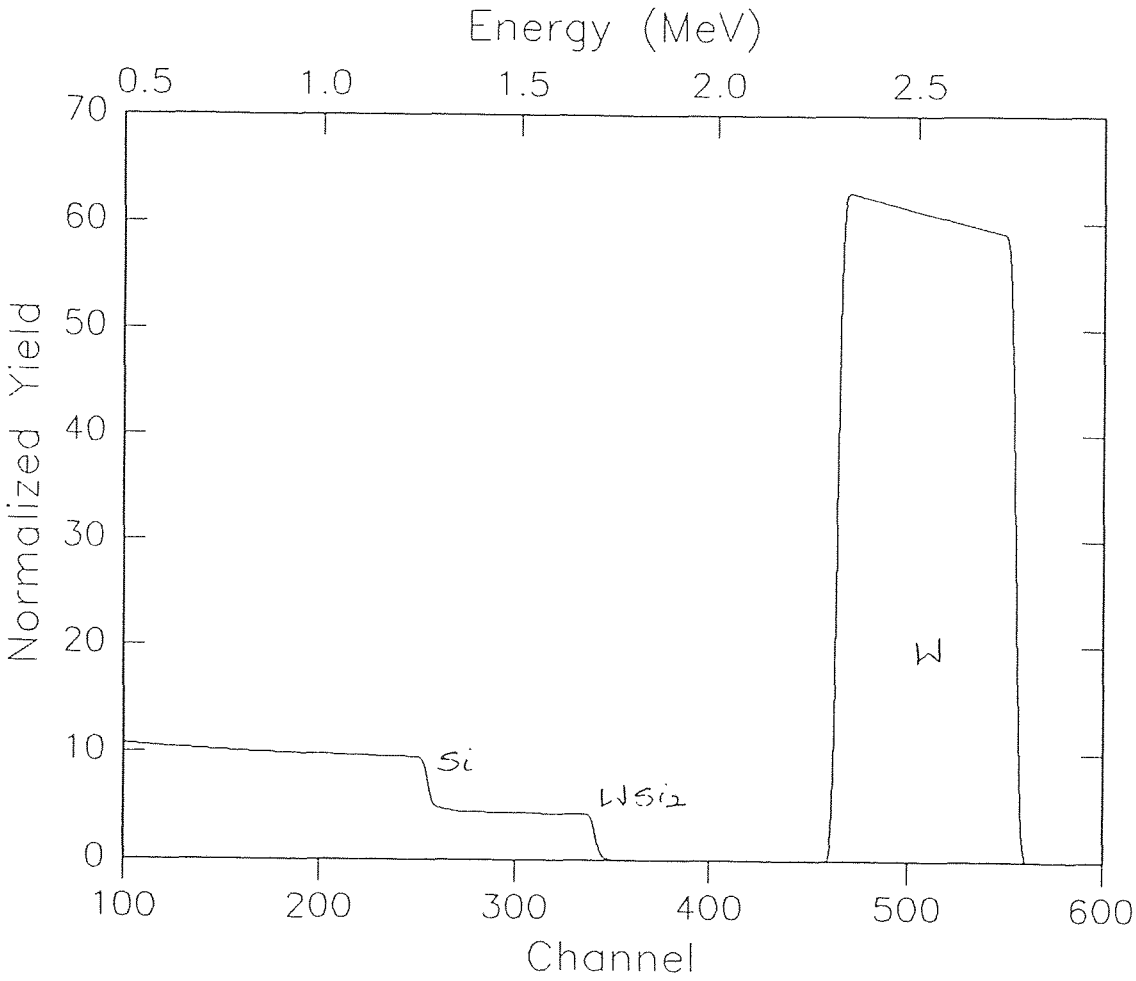
```
for(T=300; T<=500; T+=50)
{

i=A*T*T*exp((double)(qob/K*T)))*(exp((double)((q*V)/(n*K*T)))-1);
printf("\tV\t\ti\n");
printf("%f\t\t %f", V, i);
}
printf("\n-------------------------------\n");
}
}
```

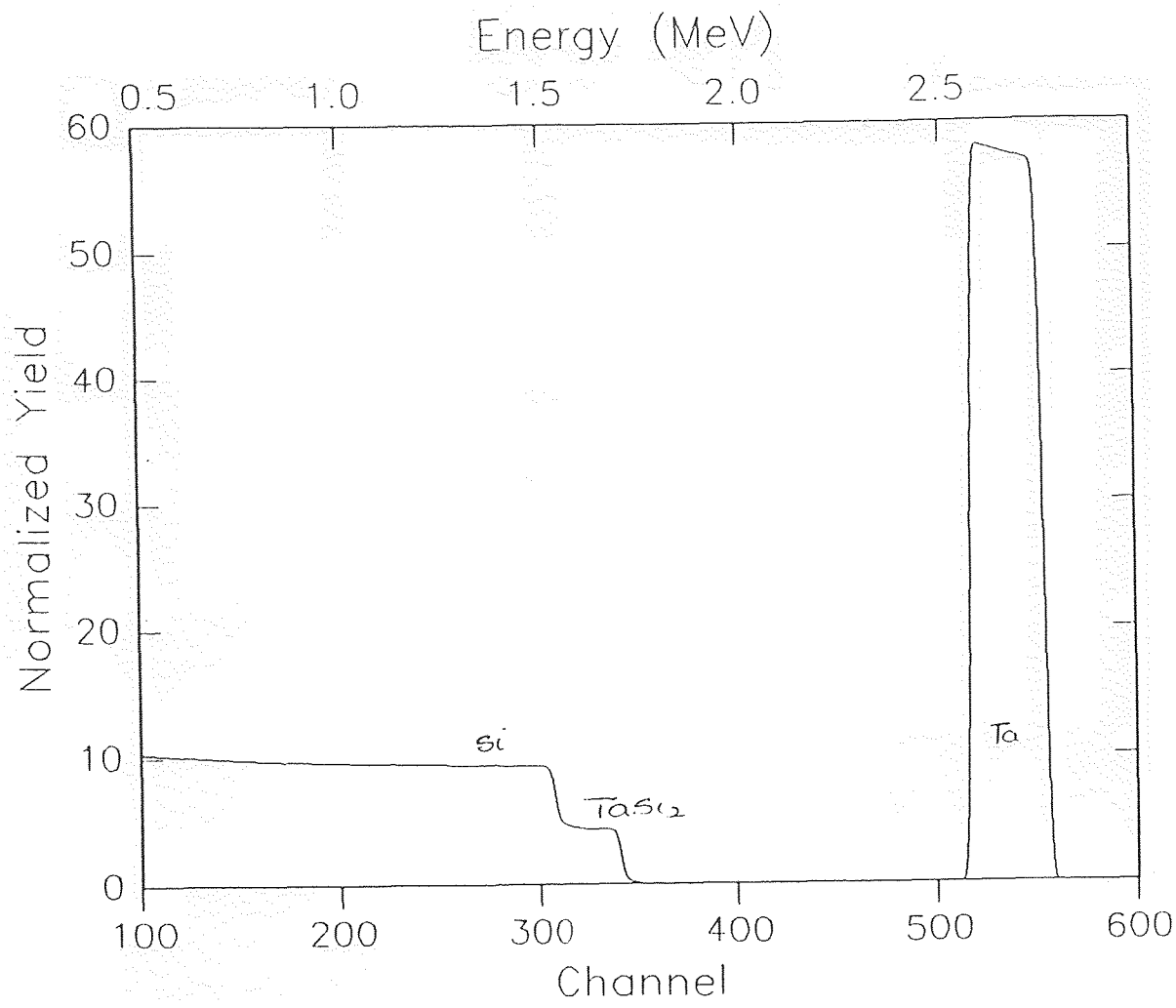
APPENDIX 4

Rutherford's Universal Manipulation Program

As part of our efforts in attempting to analyze the chemical composition of the samples, we performed initial studies using Rutherford's universal manipulation program. Results of this study are shown. Further analysis using Rutherford's Backscattering spectrometer is in progress.



RUMP simulation for WSi_2/p-si.



RUMP simulation for $TaSi_2$/p-si.

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