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ABSTRACT

LOW TEMPERATURE PERFORMANCE OF FIELD EFFECT TRANSISTORS

by
Wei Zhu

The low temperature static characteristics of silicon junction field-effect transistors (JFETs) have been investigated and analysed. The following changes were observed after cooling down the transistors: pinch-off voltage and transconductance increases; and drain current is changed as a function of the drain-source voltage. It was found that there was an increase in the amplifying properties and a reduction in noise voltage of cooled transistors. In addition, the temperature and voltage dependence of leakage current have been studied. Temperatures below 77K are of interest in evaluating effects of impurity freezeout and temperature above 77K are important since actual device temperature will be about the ambient. Operation of FET circuits at liquid nitrogen temperature has been suggested as a means of improving circuit and system performance.

LOW TEMPERATURE PERFORMANCE OF FIELD EFFECT TRANSISTORS

by
Wei Zhu

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APPROVAL PAGE

LOW TEMPERATURE PERFORMANCE OF FIELD EFFECT TRANSISTORS

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This thesis is dedicated to my parents

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CHAPTER 1

INTRODUCTION

In recent years there has been a need for the study of the field-effect transistor (FET) operating at low and very low temperature[1]. Here we define the temperature range as, commercial range: –50°C ~ 70°C; industrial range: –60°C ~ 90°C; military range: –70°C ~ 120°C. The device operation at liquid-nitrogen or liquid-helium temperatures is of considerable interest for low temperatures provide substantial improvement of the circuit performances. In particular, it is well known that in such conditions the carrier mobility, the subthreshold slope, and the latch-up immunity are greatly enhanced while the leakage currents and the power consumption are reduced[1].

Certain electronic equipment, such as infrared focal plane array (FPA) detectors, requires that the electronic devices involved operate at liquid-nitrogen or liquid-helium temperatures. It would be desirable to use the amplifiers placed in the low temperature environment near the signal source, in order to minimize microphonic noise and electromagnetic pickup in the long leads normally needed between the source and the first stage amplifier. The low-noise, low-power amplifiers with sufficient voltage gain and a complete line of electronic parts suitable for operation at cryogenic temperature would improve the signal-to-noise ratio and preserve the frequency response of the detector. Such devices are needed for space astronomy, astrophysics, geophysics and atmospheric studies of x-rays, ultraviolet, and visible wavelengths. They are also needed for many experiments in low temperature physics which require the detection of very low level electrical signals. At present the field-effect transistor seems to be the only device capable of broad band amplification at cryogenic temperature.

Within the family of FETs, as shown in Figure 1.1, we have three main types: the junction FET, more commonly known as the JFET, the metal-semiconductor FET, more commonly known as MESFET, and the metal-oxide-semiconductor FET, more commonly known as the MOSFET[2]. Despite the plethora of both small-signal and power FETs, there are only two basic modes of operation, the depletion mode and the enhancement mode. Depletion-mode FETs are normally on devices. Their drain current is reduced, or depleted, by the application of a gate potential whose polarity is opposite that of the drain voltage. On the other hand, the enhancement-mode FET is normally off device. Its drain current increases when the polarity of the gate potential matches that of the drain voltage. The JFET is classified as a depletion-mode FET, where as the MESFET and MOSFET can be designed to operate as either a depletion-mode or an enhancement-mode FET.

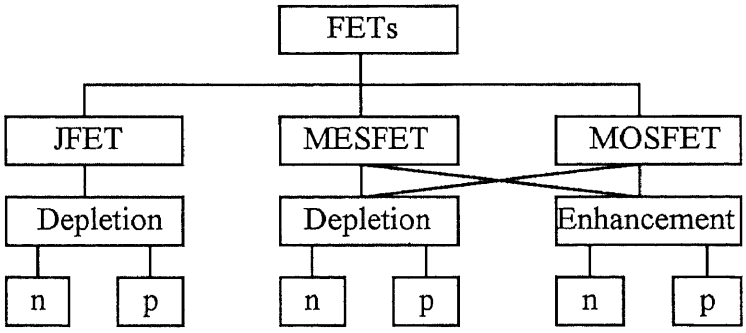


Figure 1.1 The family of FETs showing the three main types.

There are several semiconductor materials suitable for the manufacture of FETs, among which silicon and gallium arsenide are the most important ones.

The field-effect transistors are widely used in digital and analog electronics. They offer many attractive features for applications in analog switching, high-

input-impedance amplifiers, microwave amplification, and integrated circuits[3]. Compared with bipolar transistors, the FETs have considerable higher input impedance, which allows the input of an FET to be more readily matched to the standard microwave system. The FET has a negative temperature coefficient at high current levels; namely the current decreases as temperature increases. This characteristic leads to a more uniform temperature distribution over the devices area and prevents the FET from thermal runaway or second breakdown, which occurs in the bipolar transistor. The FET device is thermally stable, even when the active area is large or when many devices are connected in parallel. Because FETs are unipolar devices, they do not suffer from minority-carrier storage effects, and consequently, have higher switching speeds and higher cutoff frequencies. In addition, the FETs are basically linear devices; intermodulation and cross-modulation products are much smaller than those of bipolar transistors.

Most of the research done on FETs is referred to their room temperature behavior. The understanding and, therefore, the modeling of FET operation at low temperature is not so widely developed. In this work, current-voltage characteristics of FETs are investigated in detail in the temperature range 10-300K with special emphasis on the role of leakage current.

CHAPTER 2

TEMPERATURE DEPENDENCE OF FET'S BEHAVIOR

2.1 Structure and Operation of FET

The FET is a three-terminal device in which the current passing through two terminals is controlled by a voltage applied at the third terminal[4]. Compared to bipolar transistors, the FET is a unipolar device, namely the current involves only carriers of one kind.

In a JFET the depletion region width of a junction, or the effective cross-sectional area of a conducting channel is dependent on the bias voltage of the junction. In the device of Fig. 2.1, the current I_D flows through an n-type channel between two p^+ regions. A reverse bias between these p^+ regions and the channel causes the depletion regions to intrude into the n material, and therefore the effective width of the channel can be restricted. Since the resistivity of the channel region is determined by its doping, the channel resistance varies with changes in the effective cross-sectional area. By analogy, the variable depletion regions serves as the two doors of a gate, which open and close on the conducting channel. The end of the channel from which electrons flow is called the source, and the end toward which they flow is called the drain. The p^+ regions are called gates. It is common practice to connect the two gate regions electrically; therefore the voltage V_G refers to the potential from each gate regions G to the source S. As V_G is varied, a family of curves is obtained for the I-V characteristic of the channel, as shown in Fig. 2.1(c).

The operation of a MESFET is identical to that of a JFET. In the MESFET, however, a metal-semiconductor rectifying contact instead of a p-n junction is used for the gate electrode.

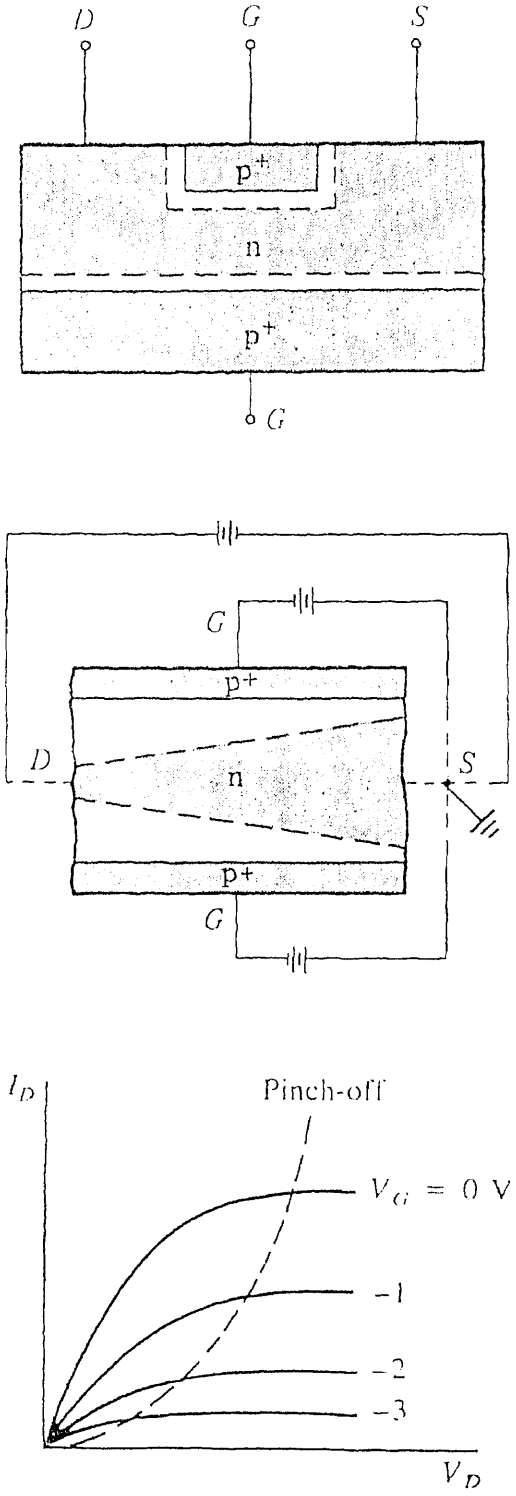


Figure 2.1 An n-channel JFET: (a) cross section of the device; (b) increase of depletion region width with V_G negative; (c) family of current-voltage curves for the channel as V_G varied.

The basic MOSFET transistor is illustrated in Fig. 2.2 for the case of an n-type channel formed on a p-type Si substrate. The n^+ source and drain ohmic contact regions are diffused or implanted into a relatively lightly doped p-type substrate, and a thin oxide layer separates the Al metal gate from the Si surface. No current flows from drain to source without a conducting n channel between them, since the drain-substrate-source combination includes oppositely directed p-n junctions in series. When a positive voltage is applied to the gate relative to the substrate (which is connected to the source in this case), positive charges are in effect deposited on the gate metal. In response, negative charges are induced in the underlying Si, by the formation of a depletion region and a thin surface region containing mobile electrons, these induced electrons form the channel of the FET, and allow current to flow from drain to source. As Fig. 2.2(c) suggests, the effect of the gate voltage is to vary the conductance of this induced channel for low drain-to-source voltage, analogous to the JFET case. For a given value of V_G there will be some drain voltage V_D for which the current becomes saturated, after which it remains essentially constant.

2.2 Current-Voltage Characteristics

In Section 2.2 and 2.3 we discuss the theory of the JFET only. The characteristics of the MESFET and MOSFET has similar as well as different features as that of the JFET. The theories of the MESFET and MOSFET have also been well studied.

2.2.1 Drain Current

Consider the FET structure shown in Figure 2.3 with the uniform doping profile of Figure 2.4[5]. The drain current density J_D, is given by

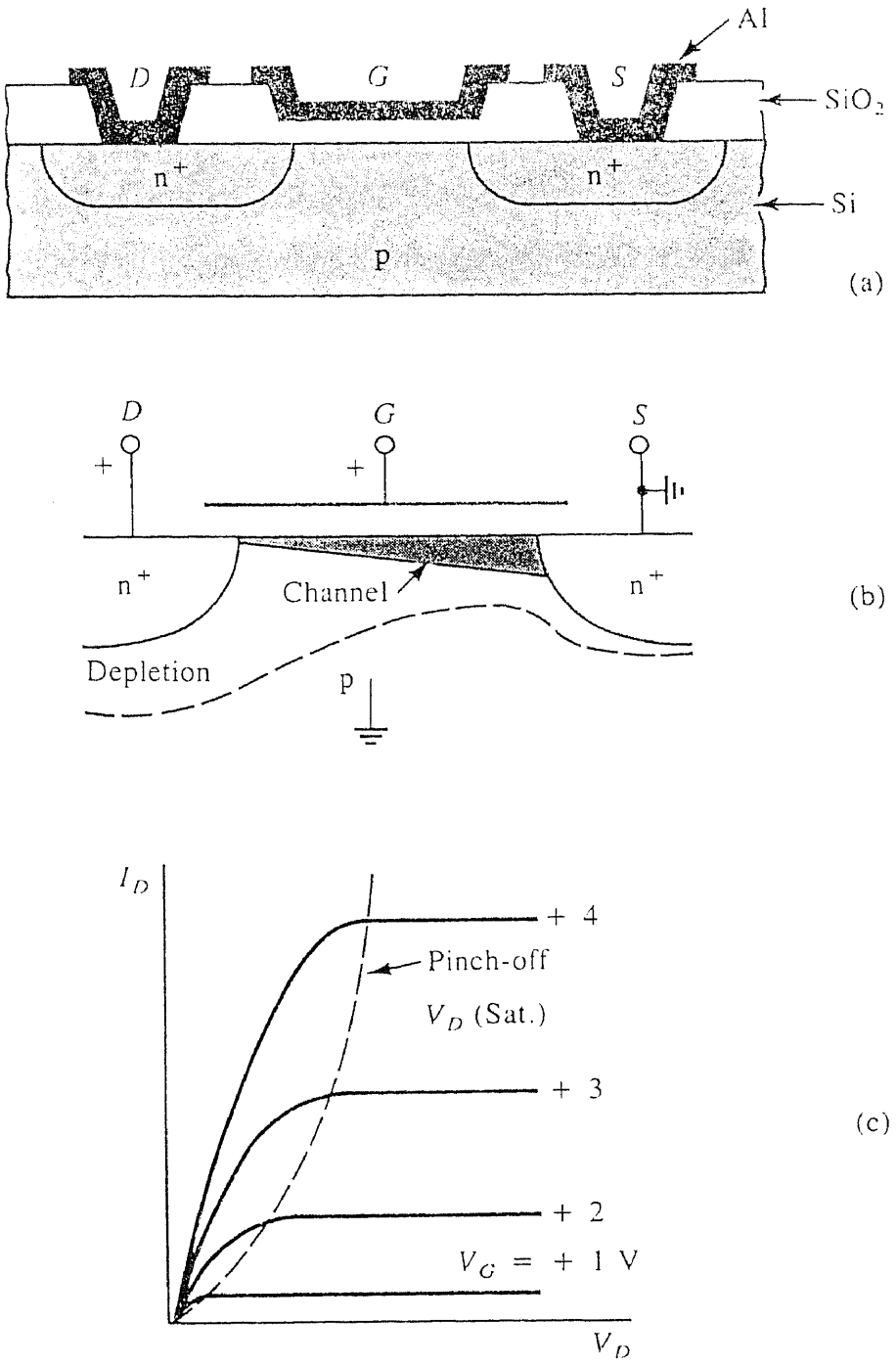


Figure 2.2 An enhancement-mode n-channel MOSFET: (a) cross section of the device; (b) schematic illustration of the induced n-channel and the depletion region; (c) drain current-voltage characteristics as a function of gate voltage.

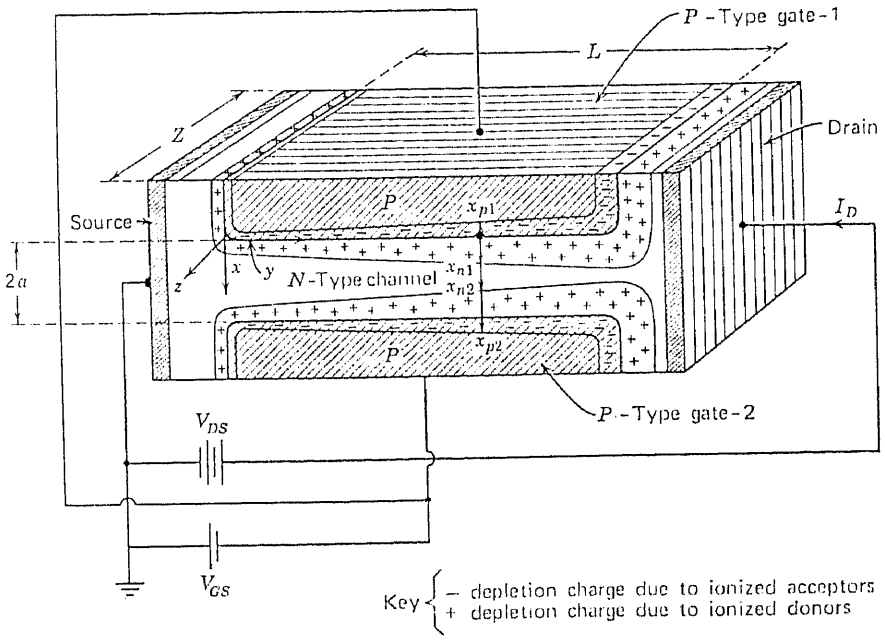


Figure 2.3 Sketch of an n-channel JFET showing coordinate system and dimensions used in the analysis.

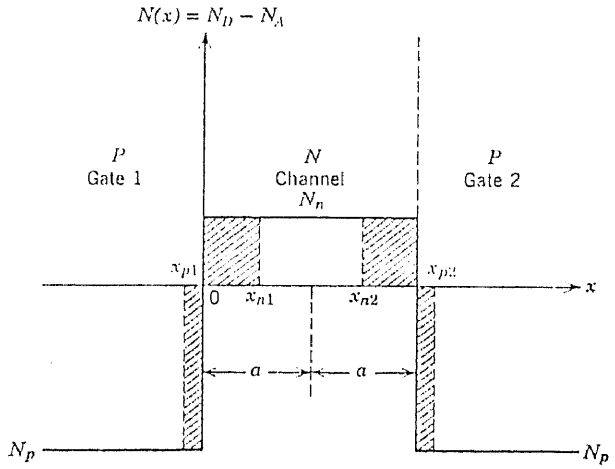


Figure 2.4 Idealized impurity distribution for an abrupt JFET. The space-charge regions are shown crosshatched.

$$J_D = \sigma(x)E_y = q\mu_n N(x)\frac{dW(y)}{dy} \tag{2.1}$$

where E_y is the electric field component along the channel and W(y) is the gate-channel potential. In general the electron bulk mobility μ_n depends on both the doping and electric field and so may vary in both the x and y directions. For the present we shall assume that μ_n is independent of E_y and the dependence on doping can be accounted for by suitably averaging μ_n across the channel.

If the *gradual approximation* is valid then the electric field in the undepleted portions of the channel can be assumed to lie only along the channel[6]. For a channel width Z the drain current becomes

$$I_D = -Z\int_{x_{n1}}^{x_{n2}} J_D dx = -Z\frac{dW(y)}{dy}\int_{x_{n1}}^{x_{n2}} q\mu_n N(x)dx \tag{2.2}$$

From Figure 2.3 it will be noted that $x_{n2}=2a-x_{n1}$ so that if the channel doping is constant and equal to N_n, (2.2) reduces to

$$I_D = -2Z(a-x_{n1})q\mu_n N_n \frac{dW(y)}{dy} \tag{2.3}$$

In the gradual approximation, we have

$$\left(\frac{W(y)}{W_O}\right)^{1/2} = \frac{x_{n1}}{a} \tag{2.4}$$

where W_o is the gate-source potential required to produce channel pinch-off. Substituting for x_{n1}, as given by (2.4), and integrating from y=0 to L, I_D becomes

$$I_D = \frac{-2q\mu_n N_n Za}{L}\int_{W_{GS}}^{W_{GD}}\left[1-\left(\frac{W(y)}{W_O}\right)^{1/2}\right]dW(y) \tag{2.5}$$

where the integration limits are the values of W(y) at the source and drain ends of the channel. Performing the integration we obtain

$$\frac{I_D}{I_O} = 3\left(\frac{W_{GD}}{W_O} - \frac{W_{GS}}{W_O}\right) - 2\left[\left(\frac{W_{GD}}{W_O}\right)^{3/2} - \left(\frac{W_{GS}}{W_O}\right)^{3/2}\right] \tag{2.6}$$

where

$$I_O = -\frac{2aZq\mu_n N_n W_O}{3L} \tag{2.7}$$

is the drain current for $W_{GS}=0$, and $W_{GD}=W_O$. Equation (2.6) can be written in terms of the applied voltage and the barrier potential

$$W_{GD} = V_{GS} - V_{DS} + \psi \tag{2.8}$$

$$W_{GS} = V_{GS} + \psi \tag{2.9}$$

The range of validity of (2.6) extends up to $W_{GD}=W_O$, at which point, pinch-off occurs at the drain end, and both the abrupt and gradual approximations fail. A more practical expression for the pinchoff point can be obtained by defining V_P to be the gate-drain voltage required to produce pinch-off, that is

$$V_P = W_O - \psi \tag{2.10}$$

From (2.9) it follows that the drain-source voltage at which pinchoff occurs is given by

$$V_{DS} = V_{GS} - V_P \tag{2.11}$$

Since $I_D=0$ when $V_{DS}=0$, V_P is also the gate-source cutoff voltage.

For the present we assume that for $V_{DS} \geq V_{GS}-V_P$, the drain current saturates at a value obtained by substituting $W_{GD}=W_O$ into (2.6). Denoting the saturation value of a quantity with a prime, we obtain

$$\frac{I'_D}{I_O} = 1 - 3\frac{W_{GS}}{W_O} + 2\left(\frac{W_{GS}}{W_O}\right)^{3/2} \qquad (2.12)$$
$$(V_{DS} \geq V_{GS} - V_P)$$

2.2.2 Transconductance and Output Conductance

An expression for the transconductance g_m be readily obtained from (2.5) by noting that $I_D=I_D(W_{GS}, W_{GD})$, so that

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{\partial I_D}{\partial W_{GS}}\frac{\partial W_{GS}}{\partial V_{GS}} + \frac{\partial I_D}{\partial W_{GD}}\frac{\partial W_{GD}}{\partial V_{GS}} \qquad (2.13)$$

From (2.8) and (2.9)

$$\frac{\partial W_{GS}}{\partial V_{GS}} = \frac{\partial W_{GD}}{\partial V_{GS}} = 1 \qquad (2.14)$$

and the remaining two terms can be obtained directly from (2.5) by differentiation yielding

$$\frac{g_m}{g_o} = \left(\frac{W_{GD}}{W_O}\right)^{1/2} - \left(\frac{W_{GS}}{W_O}\right)^{1/2} \qquad (2.15)$$

where

$$g_o = \frac{2aZq\mu_n N_n}{L} \qquad (2.16)$$

is the maximum value of g_m, which occurs when $W_{GS}=0$ and $W_{GD}=0$. It is also the conductance of a channel of thickness 2a, length L and width Z. Equation (2.15) can be expressed in the form

$$g_m = g(W_{GS}) - g(W_{GD}) \qquad (2.17)$$

where

$$g(W)=\frac{2aZq\mu_n N_n}{L}\left[1-\left(\frac{W}{W_O}\right)^{1/2}\right] \tag{2.18}$$

From (2.18) it can be readily seen that for $V_{DS} \geq V_{GS}-V_P$, $g(W_{DS})=0$ and g_m is determined solely by the undepleted channel thickness at the source (y=0). The saturation value of transconductance, from (2.15) and (2.17), becomes

$$\frac{g'_m}{g_o}=1-\left(\frac{W_{GS}}{W_O}\right)^{1/2} \tag{2.19}$$

The output conductance g_{ds} defined by

$$g_{ds}=\frac{\partial I_D}{\partial V_{DS}}=\frac{\partial I_D}{\partial W_{GD}}\frac{\partial W_{GD}}{\partial V_{DS}} \tag{2.20}$$

can also, with the aid of (2.5) and (2.8), be expressed in the form

$$g_{ds}=g(W_{GD}) \tag{2.21}$$

where $g(W_{GD})$ is given by (2.18). Thus the output conductance can be written as

$$g_{ds}=g_o\left[1-\left(\frac{W_{GS}-V_{DS}}{W_O}\right)^{1/2}\right] \tag{2.22}$$

Under saturation conditions $g_{ds}=0$. However, in practice it remains finite, and depends on the channel shortening effect.

The current-voltage characteristics of other doping profiles can be calculated [3]. It is found that the ratio I'_D/g'_m varies almost linearly with V_{GS}, with an intercept of V_P on the gate-source voltage axis. Hence

$$\frac{I'_D}{g'_m}=\frac{1}{n}(V_P-V_{GS}) \tag{2.23}$$

where n varies between 2 and 2.25[5]. Equation (2.23) also enables a very useful and simple relationship to be derived for the saturation drain current. Rewriting (2.23) as

$$\frac{dV_{GS}}{V_P - V_{GS}} = \frac{dI'_D}{I'_D} \tag{2.24}$$

and integrating from V_P to 0, we obtain Shockley's equation

$$I'_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^n \tag{2.25}$$

where I_{DSS} is the saturated drain current with V_{GS}=0.

2.3 Temperature Effects

There are three fundamental parameters which affect the temperature dependence of junction FET's behaviour:

1. Variation of the space-charge region carrier recombination and generation.
2. Variation of the channel conductivity.
3. Variation of the p-n junction barrier potential.

2.3.1 Effects of Temperature on the Channel

It was first pointed out by Hoerni and Weir[7] that the major effects of temperature on a FET are to alter the average channel conductivity σ and the gate-channel junction barrier potential ψ. Since σ decreases with increasing temperature, the effect of this is to decrease the drain current as the temperature rises. On the other hand, $|\psi|$ decreases with increasing temperature, causing the magnitude of the total gate-source potential to be reduced, hence increasing the drain current. By suitably choosing the operating point, it is possible to make

these effects cancel, producing what is essentially a zero temperature coefficient operating point.

To study this, we consider a three terminal FET biased in the saturation region with a constant gate-source emf. From (2.6) it is evident that I'_D can be written as

$$I'_D = I'_D(\psi, \sigma) \tag{2.26}$$

which, on differentiation yields

$$\frac{dI'_D}{dT} = \frac{\partial I'_D}{\partial \psi}\frac{d\psi}{dT} + \frac{\partial I'_D}{\partial \sigma}\frac{d\sigma}{dT} \tag{2.27}$$

Now $\partial I'_D/\partial\psi = g'_m$ and, since $I'_D \propto \sigma$, (2.27) becomes

$$\frac{dI'_D}{dT} = g'_m\frac{d\psi}{dT} + \frac{I'_D}{\sigma}\frac{d\sigma}{dT} \tag{2.28}$$

If I_{DZ} and g'_{mZ} are, respectively, the drain current and transconductance for zero temperature coefficient, then the condition for dI'_D/dT to be zero becomes

$$\frac{I'_{DZ}}{g'_{mz}} = -\frac{d\psi/dT}{\left(1/\sigma\right)\left(d\sigma/dT\right)} \tag{2.29}$$

In practice, one is often concerned with the equivalent input drift dV_{GS}/dT at a particular operating point (I'_D, g'_m). This can be obtained by dividing (2.28) by g'_m, noting that $g'_m = \partial I'_D/\partial V_{GS}$ and substituting (2.29), yielding

$$\frac{dV_{GS}}{dT} = \frac{d\psi}{dT}\left[1 - \left(\frac{I'_D/g'_m}{I'_{DZ}/g'_{mz}}\right)\right] \tag{2.30}$$

In terms of the power law exponent n, (2.30) with the aid of (2.23) and (2.25) becomes

$$\frac{dV_{GS}}{dT} = \frac{d\psi}{dT}\left[1 - \left(\frac{I'_D}{I'_{DZ}}\right)^{1/n}\right] \tag{2.31}$$

This equation gives the gate-source voltage change with temperature when the drain current is kept constant. The gate-source voltage for zero drift can be found from (2.23) and (2.29)

$$|V_{GSZ}| = |V_P| - \frac{nI'_{DZ}}{g'_{mz}} \tag{2.32}$$

The temperature coefficients of ψ for silicon linear graded and abrupt junctions are given by[5]

GRADED

$$\frac{d\psi}{dT} = -(4.49 - 3.525\psi_{300}) \qquad \text{mV/K} \tag{2.33}$$

ABRUPT

$$\frac{d\psi}{dT} = -(4.29 - 3.33\psi_{300}) \qquad \text{mV/K} \tag{2.34}$$

where ψ_{300} is the value of ψ at 300K.

For both n-type and p-type silicon, the variation of conductivity with temperature can be computed[3]. It will be note that $(1/\sigma)(d\sigma/dT)$ is a function of temperature, so that dI'_D/dT will be zero only at one temperature. However, since $(1/\sigma)(d\sigma/dT)$ is not a rapidly varying function, ΔV_{GS} can be quite small for wide fluctuations in T.

If the gate-source voltage is held constant, then the drain current temperature coefficient can, with the aid of (2.28), (2.29) and (2.23) be expressed as

$$\frac{1}{I'_D}\frac{dI'_D}{dT} = n\frac{d\psi}{dT}\left(\frac{1}{V_P - V_{GS}} - \frac{1}{V_P - V_{GSZ}}\right) \tag{2.35}$$

Next we turn to the temperature dependence of the pinch-off voltage V_P. From (2.10), since W_O is independent of temperature, hence

$$\frac{dV_P}{dT} = -\frac{d\psi}{dT} \tag{2.36}$$

The magnitude of the pinch-off voltage increases with increasing temperature. For a temperature change of 150K this amounts to approximately 0.3V.

2.3.2 Effects of Temperature on the Leakage Current

Leakage currents for low-voltage FETs closely obey the simple Shockley diode model that predicts[2]

$$I = I_0\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \tag{2.37}$$

where I_0, the reverse saturation current, also exhibits a temperature dependency:

$$I_0 = AT\exp\left(-\frac{qE_a}{kT}\right) \tag{2.38}$$

where

E_a = activation energy

T = temperature in degrees K

q = electronic charge (1.602×10^{-19}C)

k = Boltzmann's constant (1.38×10^{-23}J/K)

A = a constant

Equation (2.38) indicates that I_0 doubles for approximately every 10K. The leakage current phenomenon becomes more complicated as the voltage rises.

CHAPTER 3

EXPERIMENTAL METHODS

3.1 Test System

In order to measure the low temperature characteristics of FET, a special test system was designed. A Keithley 236 Source Measure Unit, which can measure current as small as 10 fA (10^{-14}A) DC was used as the voltage source and current measurement equipment during testing. Measurements have been performed in a closed cycle refrigerator with helium gas as the coolant. The samples were mounted on a heater, and a temperature controller (Model: 4025 Cryogenic Temperature Controller) has been used for the temperature control. The connections between the Keithley 236 and the test samples were via triax connectors and triax cables which provided double shielding for the test signals.

The measurement was under the control of an IBM 386 AT personal computer via an IEEE 488 communication port. Data obtained by the Keithley 236 were sent to the PC, and then processed, plotted and printed. The system control and data processing program were written in Quick Basic Language (See Appendix).

The system schematic diagram is shown in Figure 3.1.

3.2 Description of Apparatus

3.2.1 Source Measure Unit

The fundamental model of the Source Measure Units are shown in Figure 3.2. When programmed to source voltage, the I_{METER} is connected in series with the V_{SOURCE} and output. When programmed to source current, the V_{METER} is connected across (in parallel to) the I_{SOURCE} and output.

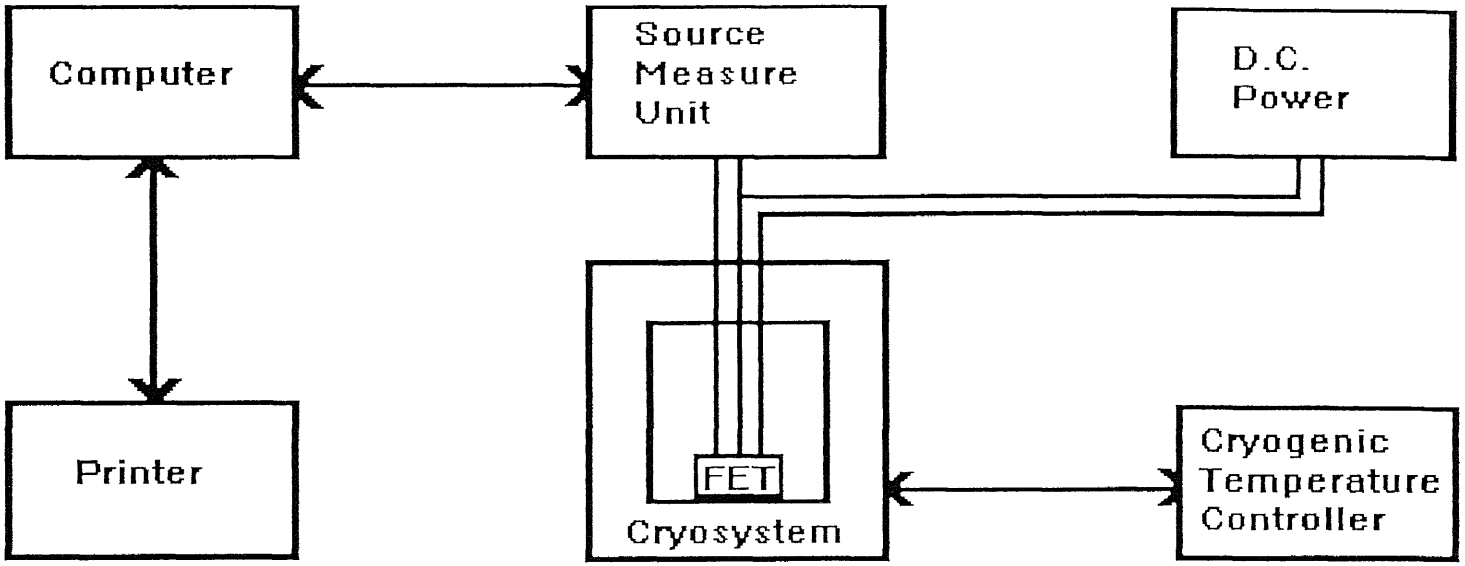


Figure 3.1 Test system schematic diagram.

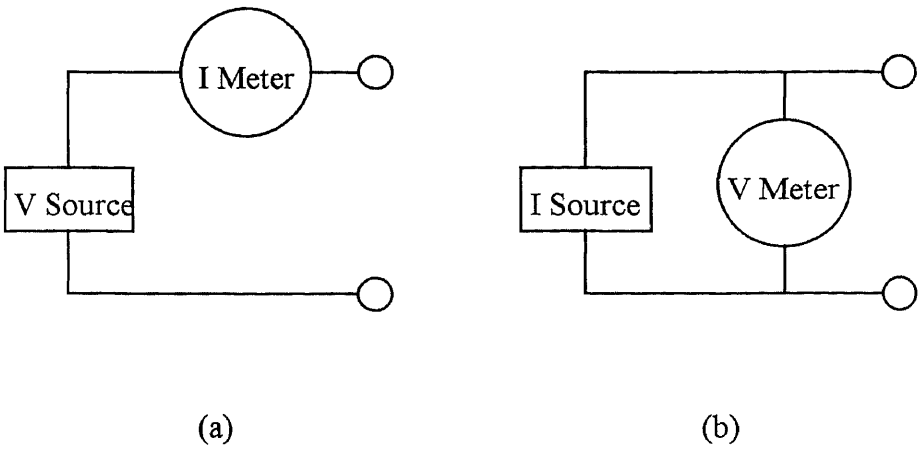


Figure 3.2 Fundamental model of the source measure units:
(a) source V measure I; (b) source I measure V.

As a voltage source, the Model 236 can supply from ±100μV to±110V with a programmable compliance limit of up to 100mA. Compliance limits are used to protect external circuitry or DUT (Device Under Test). Setting an appropriate current compliance (I-limit) can prevent excessive power dissipation in a device. The Source Measure Unit will never exceed the user programmed compliance limit.

When configured to measure current, the Model 236 can measure from ±10fA to ±100mA. The selected compliance range is also the maximum measurement range. However, if autorange is enabled, the Source Measure Unit will always go to the lowest (most sensitive) possible range to make the measurement.

The basic circuit configuration of Source Measure Unit is shown in Figure 3.3. When the Model 236 is operated as the voltage source and current measure, an ammeter (I_{METER}) is connected between the voltage source (V_{SOURCE}) and output HI. In this configuration, the Source Measure Unit will function as a low-impedance voltage source with current measure (and limit) capability. Sense

circuitry is used to constantly monitor the output voltage and make adjustments to V_{SOURCE} as needed. V_{METER} measures the voltage at the output (local sense) or at the DUT (remote sense) and compares it to the programmed voltage level. If the sensed (measured) level and the programmed value are not the same, V_{SOURCE} is adjusted accordingly. Here again, remote sense eliminates the effect of voltage drops in the test leads ensuring that the exact programmed voltage appears at the DUT. The driven guard needed to accurately measure low current is provided by the buffer circuit. Guard and output HI will always be at the same potential. When the Source Measure Unit is properly connected to a test fixture, guard is extended to that test fixture. Thus, leakage in the connecting triax cables is virtually eliminated. Inside the test fixture, coaxial cables are used to extend the guard all the way to the DUT. Guard should always be used when sourcing or measuring low current (<1μA) or for high speed measurements.

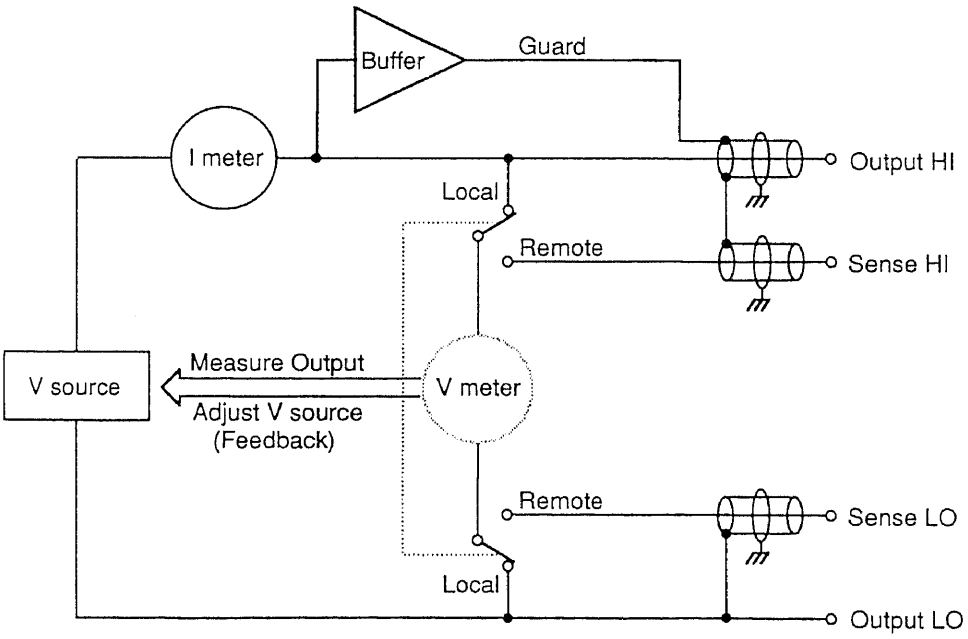


Figure 3.3 Basic circuit configuration of the source measure unit.

Shielding for the DUT must be provided. Figure 3.4 shows the basic shield configurations. Without proper shielding, surrounding electric fields can induce noise into the test circuit resulting in erratic and noisy measurements. Optimum shielding is achieved only when the output LO to chassis ground link on the rear panel is installed. When properly connected to the Source Measure Unit, the metal chassis of the test fixture function as a shield since it is connected to chassis ground via the outer shields of the triax cable. The inner panel of the test fixture, which is insulated from the chassis, provides additional shielding when it is connected to circuit low or the chassis. In most cases, best results are achieved by connecting the inner panel to circuit low. However, trial and error may prove that connecting the inner panel to the chassis provides better shielding. Figure 3.4 shows the basic shield configurations.

As shown in Figure 3.3 and Figure 3.4, the triax cable provides the chassis of the Source Measure Unit and the test fixture with a common floating voltage level, which is grounded outer cable. This double shielding reduce the noise level substantially.

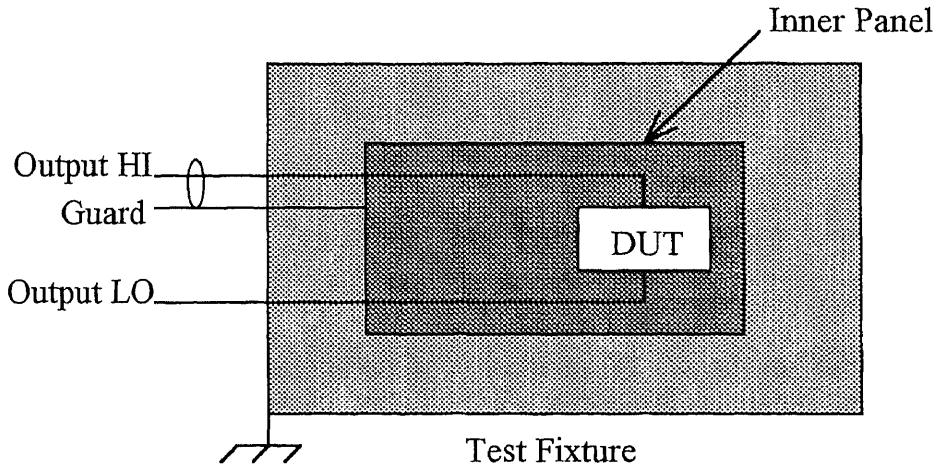


Figure 3.4 Basic shield configuration.

3.2.2 Closed Cycle Refrigerator System

The LTS-22 Closed Cycle Cryogenic Refrigerator System is designed to provide a simple, reliable source of variable cryogenic temperature for a wide range of experimental applications. This system, utilizing closed cycle refrigeration as the source of cooling, generates low temperatures without the consumption of cryogens such as liquid nitrogen or liquid helium. Because of this, the expense, difficulties, and dangers of transferring and storing these liquefied gases is avoided.

The refrigerator system consists of three primary components: the compressor unit, the cold head/vacuum shroud assembly, and the temperature controller. A component interconnection diagram is shown in Figure 3.5.

The compressor unit of the closed cycle refrigerator system is designed to compress the low pressure expanded helium gas from the cold head, remove the resultant heat of compression, and pass the high pressure helium gas to the cold head for re-expansion. The gas flow portion of the compressor contains the compressor pump, oil injection system, heat exchanger, oil separation system, and adsorber. In addition, the compressor contains the electronics required for the control of the compressor and the cold head power.

The cold head /vacuum shroud assembly functions to expand the high pressure helium gas provided by the compressor to produce the refrigeration required for cryogenic temperatures. This expansion takes place in two stages, providing concurrent refrigeration at two different temperatures. The first stage of the cold head provides refrigeration at a nominal 77 K, while the second stage, where the sample stage is normally mounted, provides refrigeration at a nominal 10 K. The cooling power available at 77 K is normally used to dissipate heat from a radiation shield, thus minimizing the black body radiation heat load experienced by the 10 K stage. The vacuum shroud assembly attached to the cold head

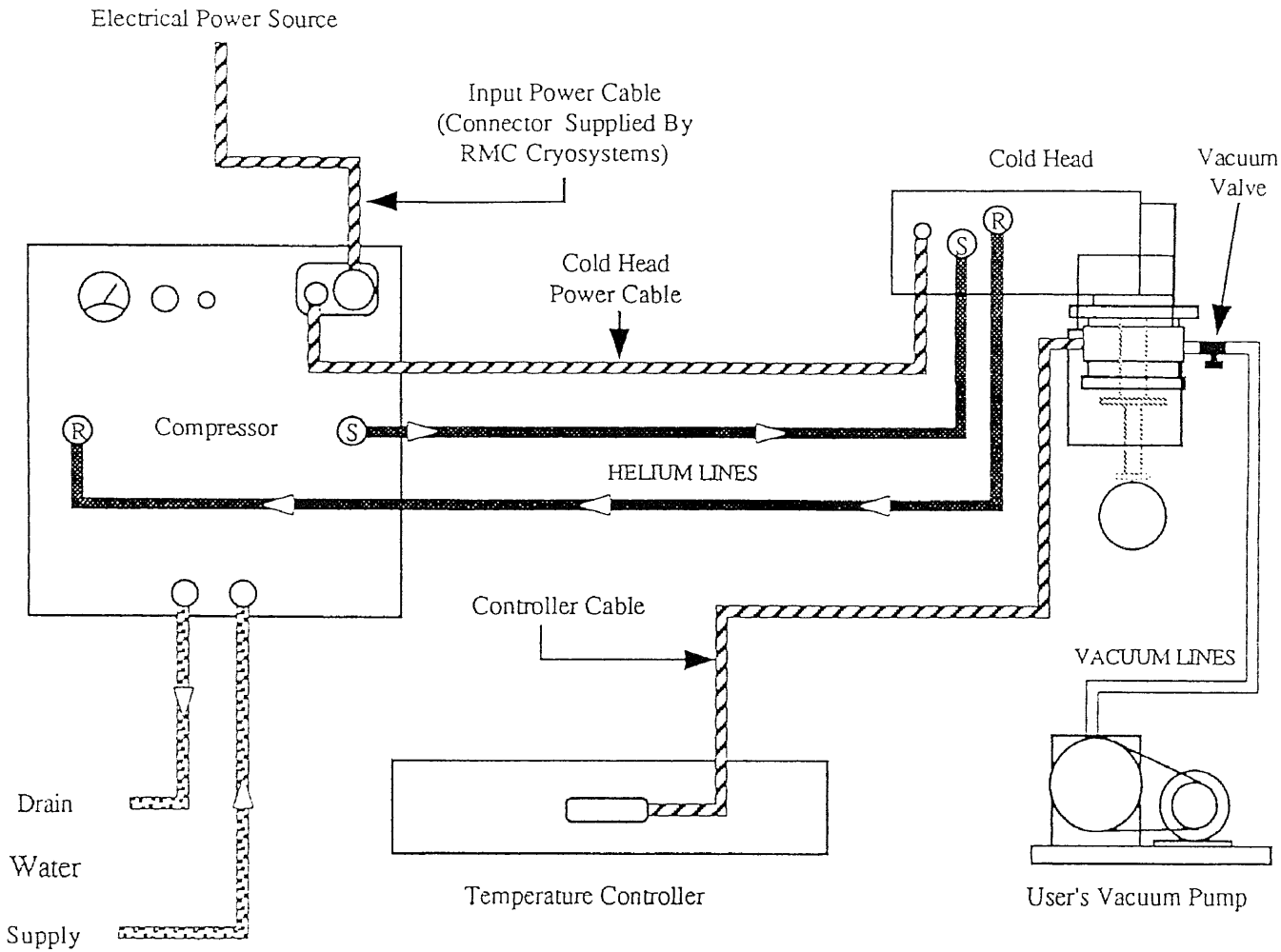


Figure 3.5 Component interconnection diagram of cryosystem.

provides the ability to insulate the cold finger of the cold head from ambient conditions. Due to the extremely low operating temperatures provided by the cold head, high vacuum insulation is required to minimize the convective heat conduction which would take place without the vacuum shroud. Such a heat load on the cold finger will not allow it to reach these cryogenic temperatures.

The cryogenic temperature controller supplied with the refrigerator system provides the capability of obtaining sample temperatures over the entire operating range of the system, rather than just the lowest attainable temperature.

In order to achieve cryogenic temperatures with this system, it is necessary that the cold portions of the system be vacuum insulated to prevent unwanted convective heat loss. For this purpose, a vacuum of better than 1×10^{-3} torr must be achieved in the vacuum chamber. Once system cool down begins, the cold surfaces will cryopump the residual gases in the vacuum chamber, resulting in a high vacuum environment. Typical cool down time to 10 K for a refrigerator system under no load conditions is approximately 50 minutes. However, typical cool down time varies by the mass of the sample and sample holders employed. In addition, instrumentation wiring incorporated into the system may add to the cool down time required.

The system may be allowed to warm with no additional heat load to the system and the refrigerator turned off. However, this method of warmup will take several hours. Another method of warm up involves the use of the temperature controller and temperature control heater. With the compressor and cold head running, enter a temperature set point near room temperature. The temperature controller will rapidly heat the cold finger up to the required temperature. The rate of warmup of the radiation shield may be increased by introducing dry nitrogen gas to the vacuum chamber. This will provide a convective heat transfer path between the radiation shield and the vacuum chamber walls.

3.3 Test Configuration for FET Tests

3.3.1 Common-Source Test

One of the more common FET tests involving family of curves are common-source characteristics. Figure 3.6 shows the test configuration for the common-source test. Source Measure Unit sweeps V_{DS}, and the instrument also measures I_D.

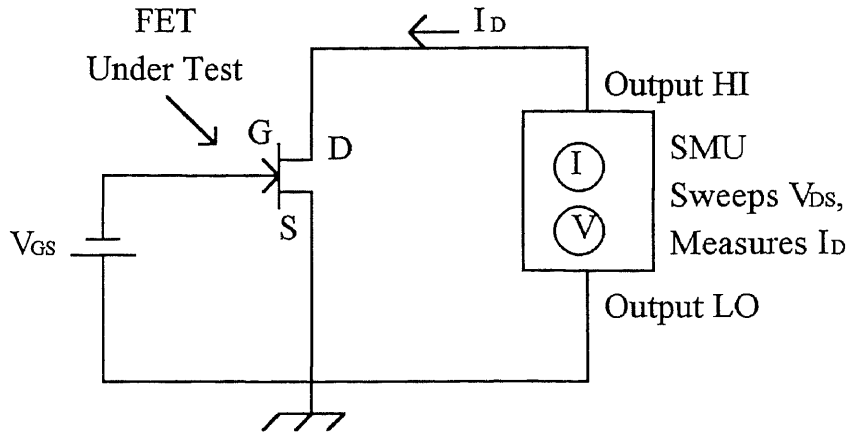


Figure 3.6 Test configuration for common-source tests.

3.3.2 Drain Leakage Test

One important parameter associated with FET is leakage current. As the gate is biased beyond cutoff, that is, the gate-source voltage V_{GS} is greater than the gate-source cutoff voltage $V_{GS}(off)$, the drain current I_D becomes $I_D(off)$—the drain leakage current. The Source Measure Unit sources the drain-source voltage V_{DS}, and it measures the resulting leakage current through the device. The resistor, R, is included for current limiting, and it also helps to reduce noise.

Once the leakage current is known, the leakage resistance can easily be calculated from the applied voltage and leakage current value as follows:

$$R = \frac{V}{I} \tag{3.1}$$

3.3.3 Gate Leakage Test

Figure 3.7 shows the basic test configuration for gate leakage current. The Source Measure Unit sources the gate-source voltage V_{GS}, and the instrument also measures the gate reverse current I_{GS}. Often, V_{GS} is swept across the desired range of values, and the resulting I_{GS} values are plotted against V_{GS}. When drain is shorted to source (V_{DS}=0), the gate reverse current refers to the gate leakage current I_{GSS}.

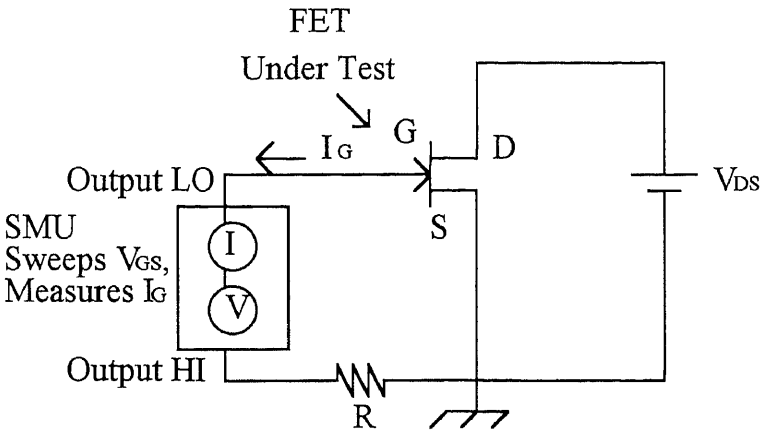


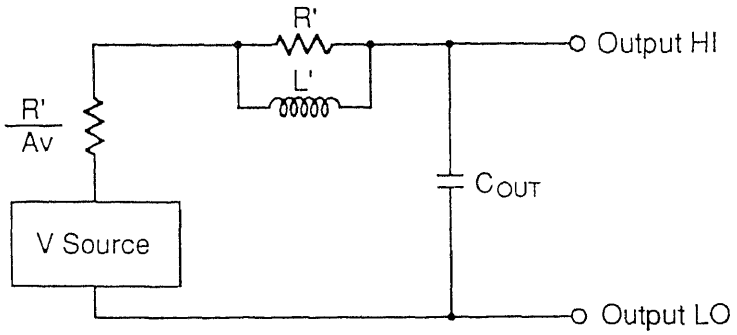
Figure 3.7 Test configuration for gate leakage test

3.4 Experimental Techniques of Measurement

3.4.1 Making Stable Measurements

The output impedance models of the Source Measure Unit are shown in Figure 3.8. When sourcing voltage, the output looks inductive. As a result, capacitive loads will degrade phase margin. The Source Measure Unit is designed for a 45° phase margin into 3000pF and as a result will handle much higher capacitances without oscillating. In addition, the effective series resistance (ESR) of the capacitor (especially large value electrolytic types) helps limits the Q of the

resonant circuit. Adding an external series resistor (100 Ω) will help decouple large capacitive loads.



R' = Current range resistor
Av = Loop gain (10^6)

$L' = \frac{R'}{2\pi BW'}$ BW = 40 kHz for 1.1V, 11V and 110V ranges
= 4 kHz for 1100V range

C_{OUT} = Fixed capacitor (depends on selected current range)

Figure 3.8 V-source output impedance model.

3.4.2 Guarding Technique

The purpose of guarding is to eliminate the effects of leakage current (and capacitance) that exists between output high and output low. In the absence of a driven guard, leakage could be enough to adversely affect the performance of the Source Measure Unit. The guard potential (equal to the potential of output HI) is connected to the inner shell of the triax connectors that surround output HI and sense HI. Since the voltage potential on the inner shells (guard) and center conductor (output HI and sense HI) are the same, virtually no leakage current can flow from output HI or sense HI to output LO (or chassis), and the capacitance effects of the triax cable are reduced. Figure 3.9 and Figure 3.10 is used to help explain the principles of guarding. Both illustrations show LO being connected to chassis ground. On the Source Measure Unit, output LO can be connected to

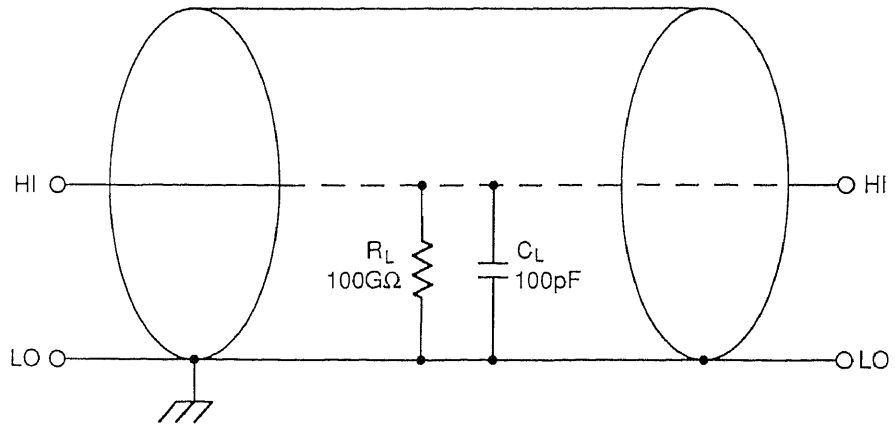


Figure 3.9 Unguarded coaxial cable.

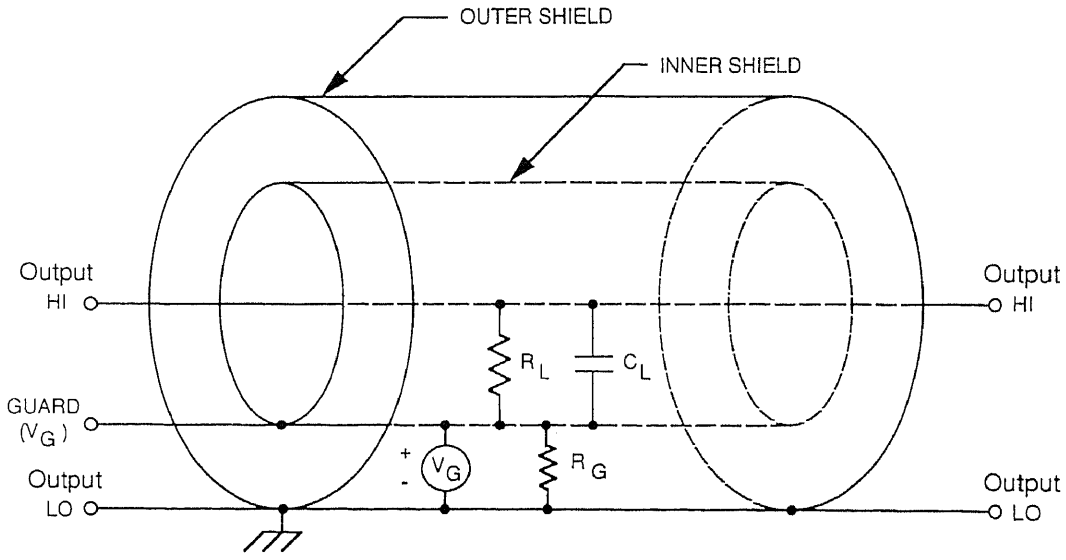


Figure 3.10 Guarded triax cable.

chassis ground by installing the ground link on the rear panel. Even with the ground link removed, the resistance between output LO and chassis ground (10GΩ) is relatively low when compared to the insulation resistance of the cable (100GΩ). Thus, for the following discussion on low level leakage currents, the outer shield of the cables (chassis ground) can be considered to be output LO.

Typically, insulation resistance between conductors in a coaxial or triaxial cable is 100GΩ. In the unguarded configuration, shown in Figure 3.9, leakage current will flow through the insulator (represented by R_L and C_L) separating HI from LO. Leakage current is a problem in an unguarded circuit when sourcing or measuring current for a high impedance load. Figure 3.10 shows the general guarding technique using a triax cable. Guard (V_G) is connected to the inner shield of the cable and surrounds output HI. Since the guard voltage is at virtually the same potential as output HI, leakage current through the insulator will be almost zero. In reality, guard and output HI differ by a small offset voltage (±2mV). The actual maximum leakage current (I_L) would be:

$$I_L = \frac{2mV}{100G\Omega} = 20fA \tag{3.2}$$

Leakage current will flow from the inner shield to the outer shield (through R_G), but it does not matter since the current is supplied by buffered guard source(V_G) and not output HI.

3.4.3 Electrostatic Interference

Electrostatic interference occurs when an electrically charged object is brought near an uncharged object, thus inducing a charge on the previously uncharged object. Usually, the effects of such electrostatic action are not noticeable because low impedance levels allow the induced charge to dissipate quickly. However, high impedance levels of many Source Measure Unit measurements do not allow

these charges to decay rapidly, and erroneous or unstable readings may be caused in the following ways:

1. DC electrostatic fields can cause undetected errors or noise in the reading.

2. AC electrostatic fields can cause errors by driving the amplifier into saturation, or through rectification that produces DC errors.

Electrostatic interference is first recognizable when hand or body movements near the experiment cause fluctuations in the reading. Pick up from ac fields can also be detected by observing the output on an oscilloscope. Line frequency signals on the output are an indication that electrostatic interference is present.

Means of minimizing electrostatic interference include:

1. Shielding. Possibilities include a shielded room, a shielded booth, shielding the sensitive circuit (test fixture), and using shielded cable. The shield should always be connected to a solid connector that is connected to signal low. Note, however, that shielding can increase capacitance, possibly slowing down response time.

2. Reduction of electrostatic fields. Moving power lines or other sources away from the experiment reduces the amount of electrostatic interference.

3.4.4 Radio Frequency Interference

Radio frequency interference (RFI) is a general term frequently used to describe electromagnetic interference over a wide range of frequencies across the spectrum. RFI can be especially troublesome at low signal levels, but it may also affect higher level measurements in extreme cases.

RFI can be caused by steady-state sources such as TV or radio broadcast signals, or it can result from impulse sources, as in the case of arcing in high

voltage environments. In either case, the effect on instrument performance can be considerable, if enough of the unwanted signal is present. The effects of RFI can often be seen as an unusually large offset, or, in the case of impulse source, sudden, erratic variations in the reading.

The most convenient method to minimize the effects of RFI is to use the filter feature of the Source Measure Unit. Up to 32 readings can be averaged with this filter. A detrimental affect of filtering of overall Source Measure Unit speed is decreased.

Other methods can be used to minimize the effects of RFI. The most obvious method is to keep the instrument and experiment as far away from the RFI source as possible. Shielding the instrument, experiment, and test leads will often reduce RFI to an acceptable level. In extreme cases, a specially constructed screen room may be necessary to sufficient attenuate the troublesome signal.

CHAPTER 4

RESULTS AND DISCUSSIONS

4.1 Static Current-Voltage Characteristics

The samples used are silicon n-channel junction FETs fabricated by Siliconix (reference number: 2N4392). Static characteristics of this type of FETs were measured from 10K to 300K. A number of transistors has been tested and results are confirmed in all cases.

After cooling down the transistors from 300K to 10K, changes in their parameters were observed. The drain current of the FET increases with decreasing temperature, as shown by the drain characteristics of Figure 4.1, Figure 4.2 and Figure 4.3. These pictures show an increase in the separation of the I-V curves with decreasing temperature. For a given gate voltage, the drain current saturates at a larger current with decreasing temperature. A decrease in temperature increases the channel conductivity, owing to increased carrier mobility, but decreases the channel height because of the increase in the depletion-region thickness (junction-barrier height) that occurs as a result of Fermi-level shifts with temperature[3]. These are opposing effects, as far as drain current is concerned, but these figures suggests that the effect on channel conductivity predominates.

The forward transfer characteristics, $I_D = f(V_{GS})$ of transistors were measured and plotted in Figure 4.4. With the drop in temperature of the FETs to below room temperature, their transconductance, g_m, increases as

$$g_m = \frac{dI_D}{dV_{GS}} \tag{4.1}$$

The transconductance of silicon JFETs reaches its maximum in the temperature range 100–150K. This is because the carrier mobility is at its greatest in this

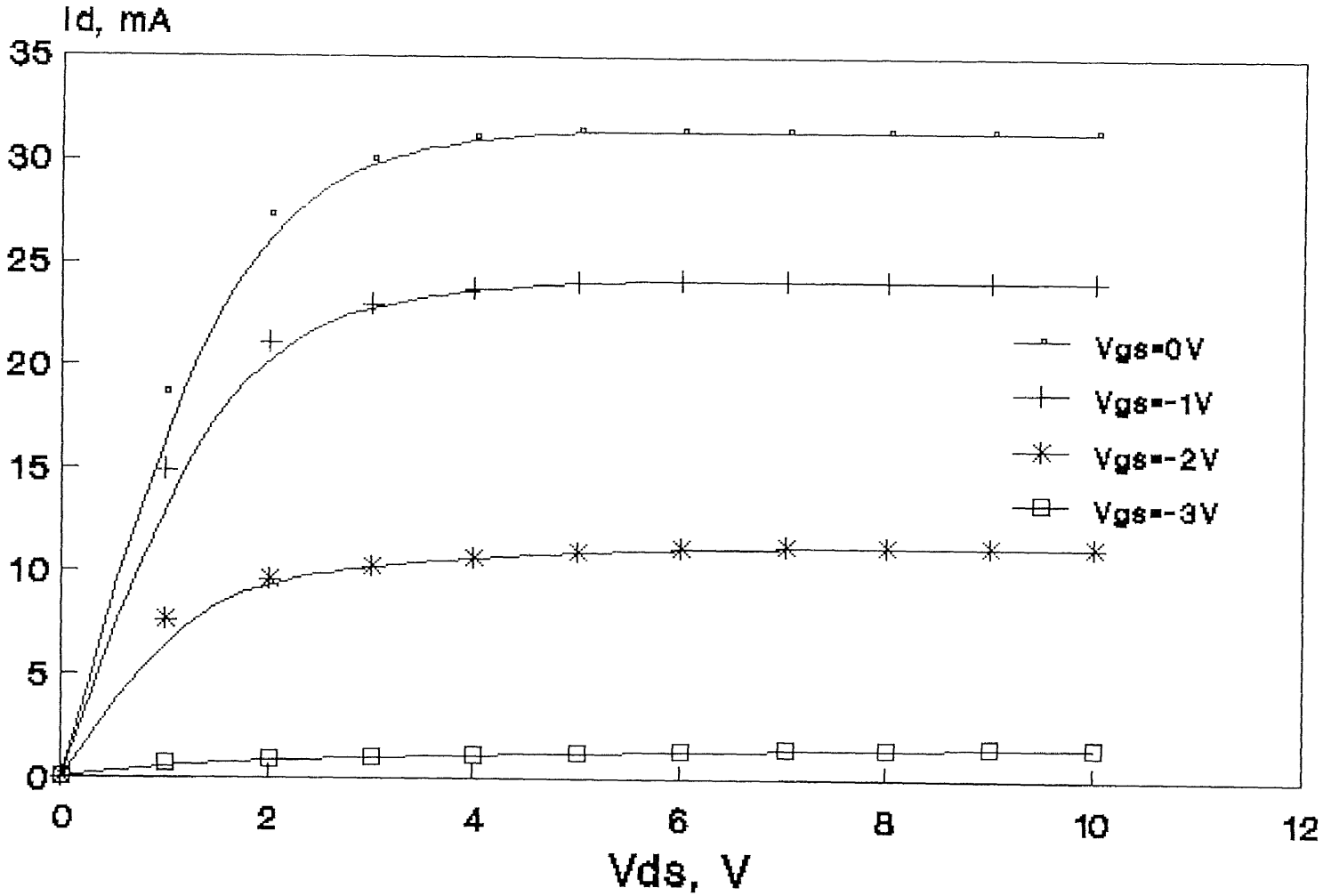


Figure 4.1 Drain current-voltage characteristics at T = 300K.

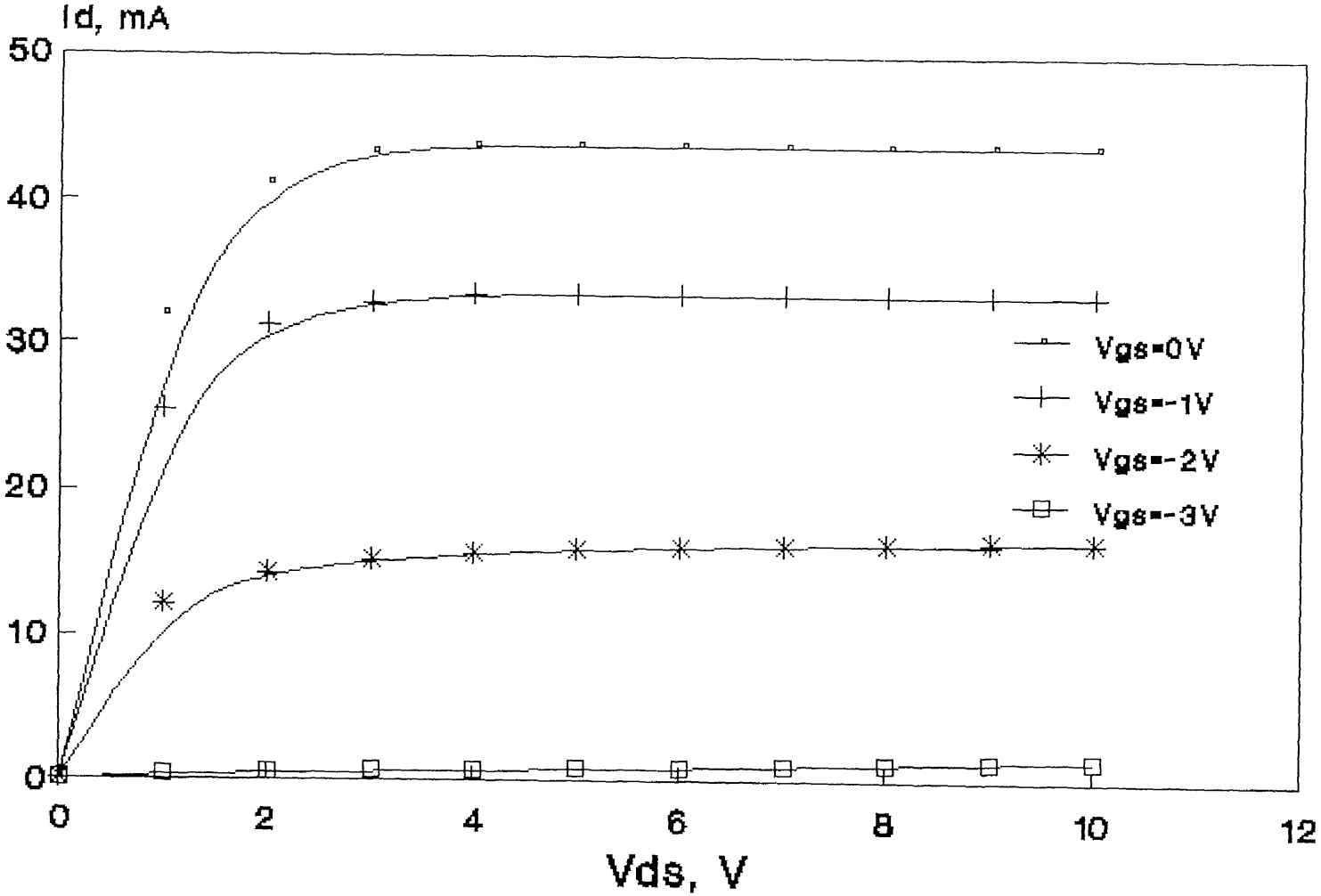


Figure 4.2 Drain current-voltage characteristics at T = 200K.

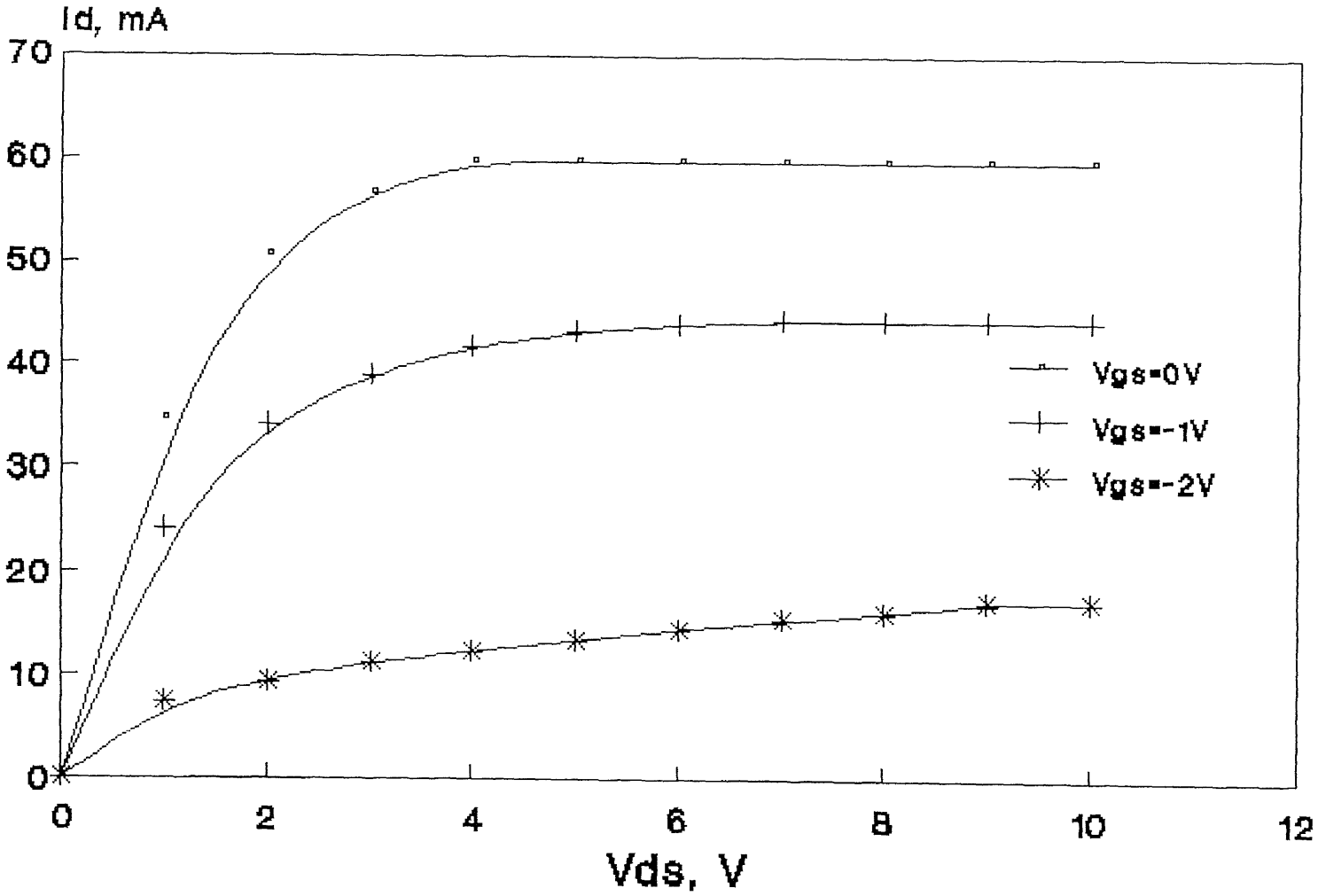


Figure 4.3 Drain current-voltage characteristics at T = 77K.

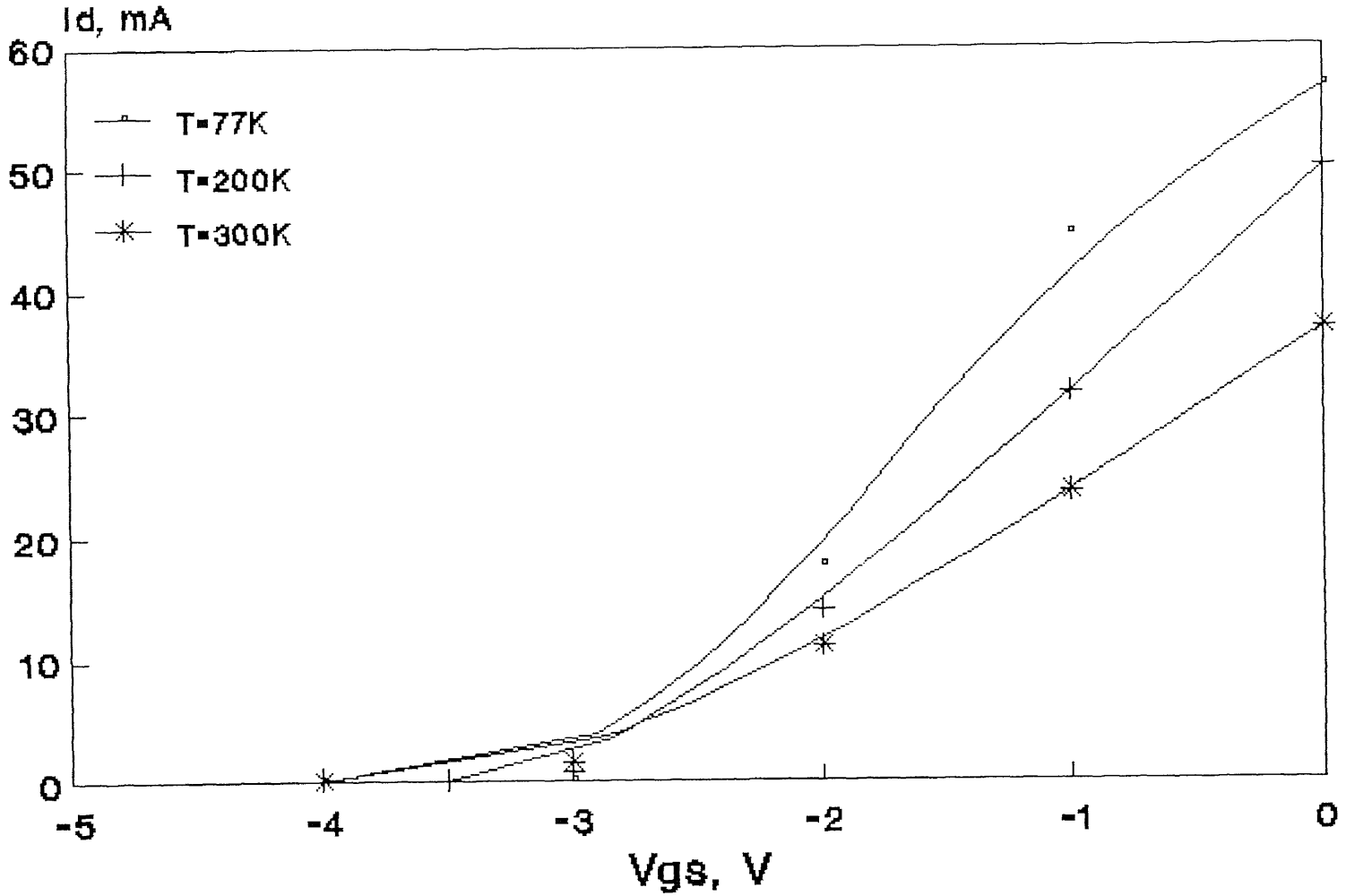


Figure 4.4 Variation of forward transfer characteristics with temperature for $V_{DS} = 10V$.

range. The g_m transconductance is generally greater at 77K than at 300K and is dependent, as the I_{DSS} current, on V_{DS}.

The pinch-off voltage V_p is the critical gate voltage at which free carriers appear or disappear in the channel. The importance of knowing the pinch-off voltage at low temperatures is that a possible decrease of $|V_p|$ with temperature might result in a shifting of the quiescent operating point beyond the drain current cut-off point if the same gate bias voltage is retained. The relation between I'_D, V_{GS} and V_p is given by Equation (2.25)

$$I'_D = I_{DSS}(1-\frac{V_{GS}}{V_p})^2 \tag{4.2}$$

thereby defining V_p to be equal to V_{GS} when I'_D just becomes equal to zero. For all the transistors investigated, an increase in the value of the pinch-off voltage V_p followed the decrease of temperature and because V_p is a negative voltage, there was a drop in the absolute value of V_p. For these transistors, the V_p voltage was a factor of 1.0 larger at 77K than at 300K and the mean ratio V_{p300}/V_{p77} amounted to 1.3.

A more detailed I_D vs. V_{GS} characteristics for T = 77K is shown in Figure 4.5, in which the data are plotted on logarithmic paper to show the current magnitude near "cutoff". This is also the "deep cutoff " behavior of the transistors. Because I_D does not go to zero, the error of Equation (4.2) increases as V_{GS} approaches V_{GS}(off). From a practical measurement standpoint, V_{GS}(off) is usually specified at an I_D value just above the minimum value. The symbol I_D(off) is used for the approximate minimum value of I_D.

Figure 4.6 illustrates the saturated drain current, measured at V_{GS}=0, V_{DS}=10V, as a function of temperature. A drop in the I_{DSS} value of the transistors was observed after cooling down below 40K. The mean ratio of I_{DSS} at 300K to

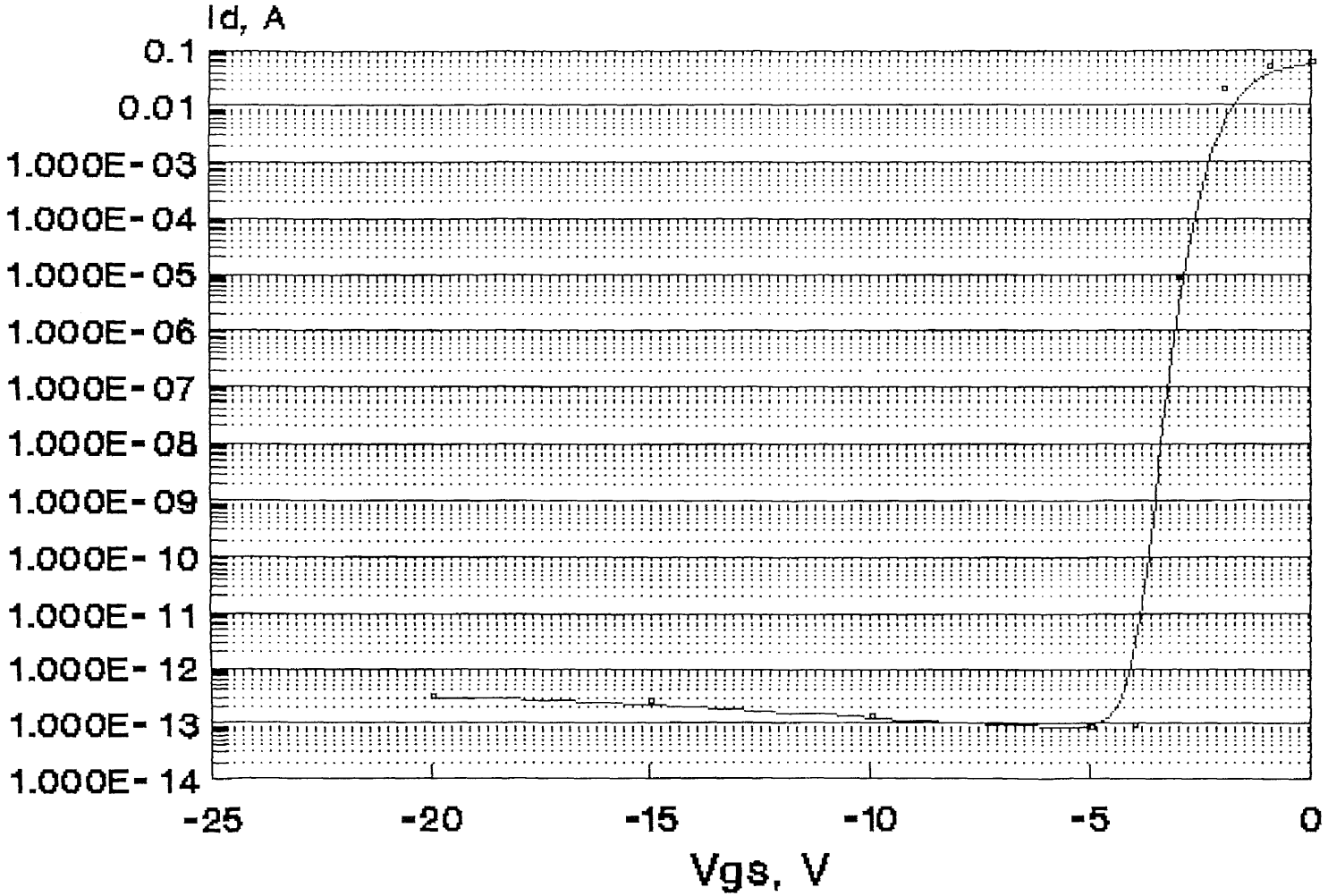


Figure 4.5 The effect of gate-source voltage on drain leakage current at T = 77K, V_{DS} = 10V.

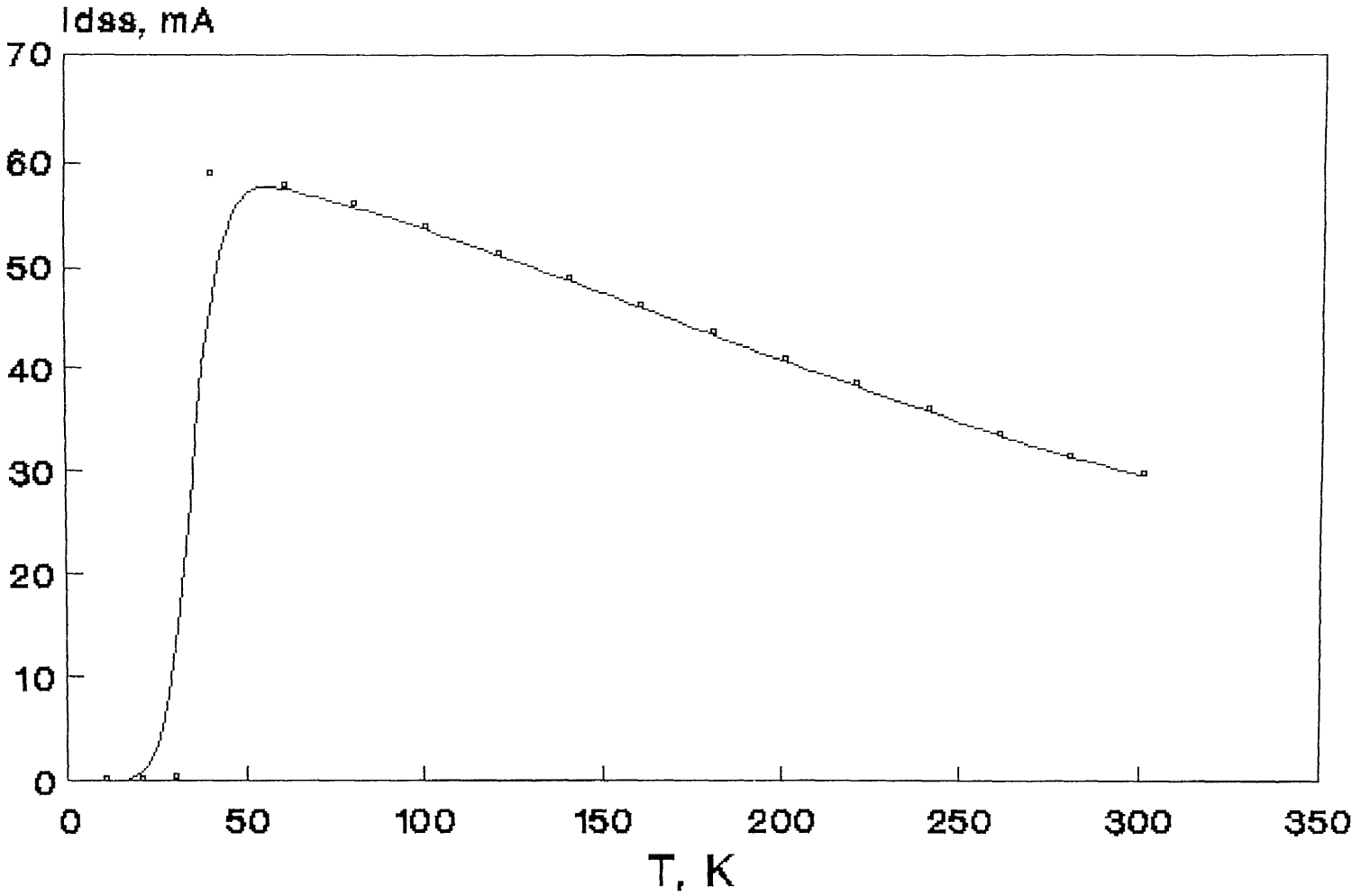


Figure 4.6 Temperature dependence of saturated drain current for $V_{GS} = 0$, $V_{DS} = 10$ V.

I_{DSS} at 40K amounted to I_{300}/I_{40}=2.0. The I_{DSS} decreases by eight orders of magnitude when the temperature decreases from 40K down to 10K, which affects the operation of the transistor. Apparently, the transistors do not conduct below 40K and therefore cannot operate. At very low temperatures, donor or acceptor impurities currently used to dope the semiconductor are fully frozen-out and the density of free carriers in the channel is very close to zero[8]. Therefore, the channel resistance has obtained its maximum value and a decrease of temperature cannot further change the number of ionized impurities. At these temperatures the thermal energy kT is not sufficient to excite carriers out of their dopent sites. With increasing temperature, the number of majority carriers emitted from the frozen-out impurities increases, thus the I_{DSS} rises.

The temperature dependence of gate leakage current is given in Figure 4.7. As referred to in the previous chapter,

$$I_{GSS} \propto e^{-\frac{qE_a}{kT}} \tag{4.3}$$

that is, I_{GSS} should vary exponentially with T^{-1}, and this is experimentally observed. We can divide I_{GSS} into two components; one arising from the intrinsic structure, the other from the extrinsic structure. Concerning the voltage dependence of I_{GSS}, it will be noted that the intrinsic component will increase until saturation is reached, at which point (neglecting the change in effective channel length) no further increase should be observed. This is shown in Figure 4.8, where the device with T=10K exhibits a rapid increase of I_{GSS} up to the saturation point, beyond which the less rapid change can probably be ascribed to the voltage dependence of the extrinsic leakage components.

The effects of temperature and voltage on the drain leakage current are shown in Figure 4.9 and Figure 4.10 separately. The temperature and voltage dependences of drain leakage current are similar to that of gate leakage current.

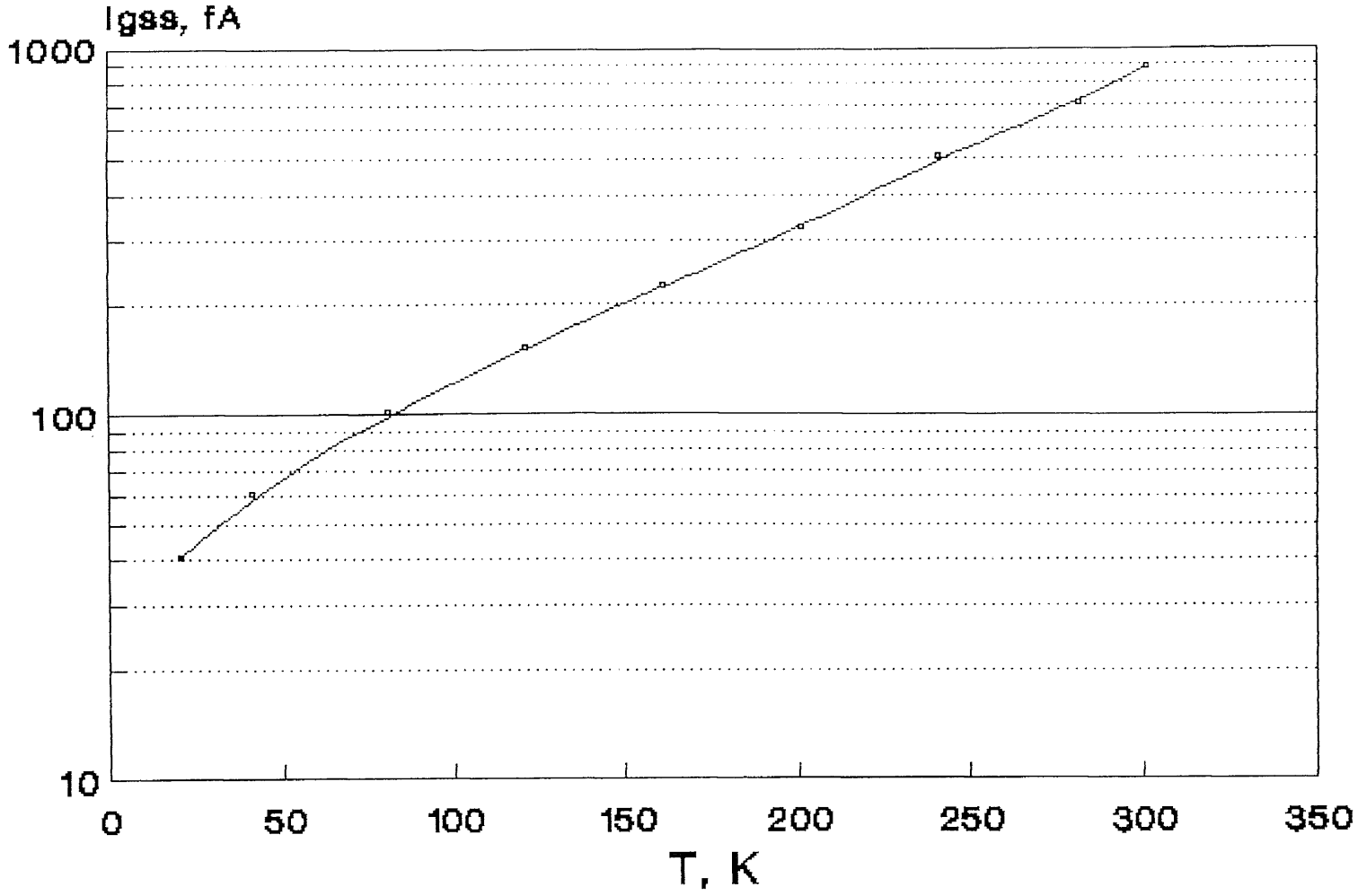


Figure 4.7 Temperature dependence of the gate leakage current for $V_{DS} = 0$, $V_{GS} = 20V$.

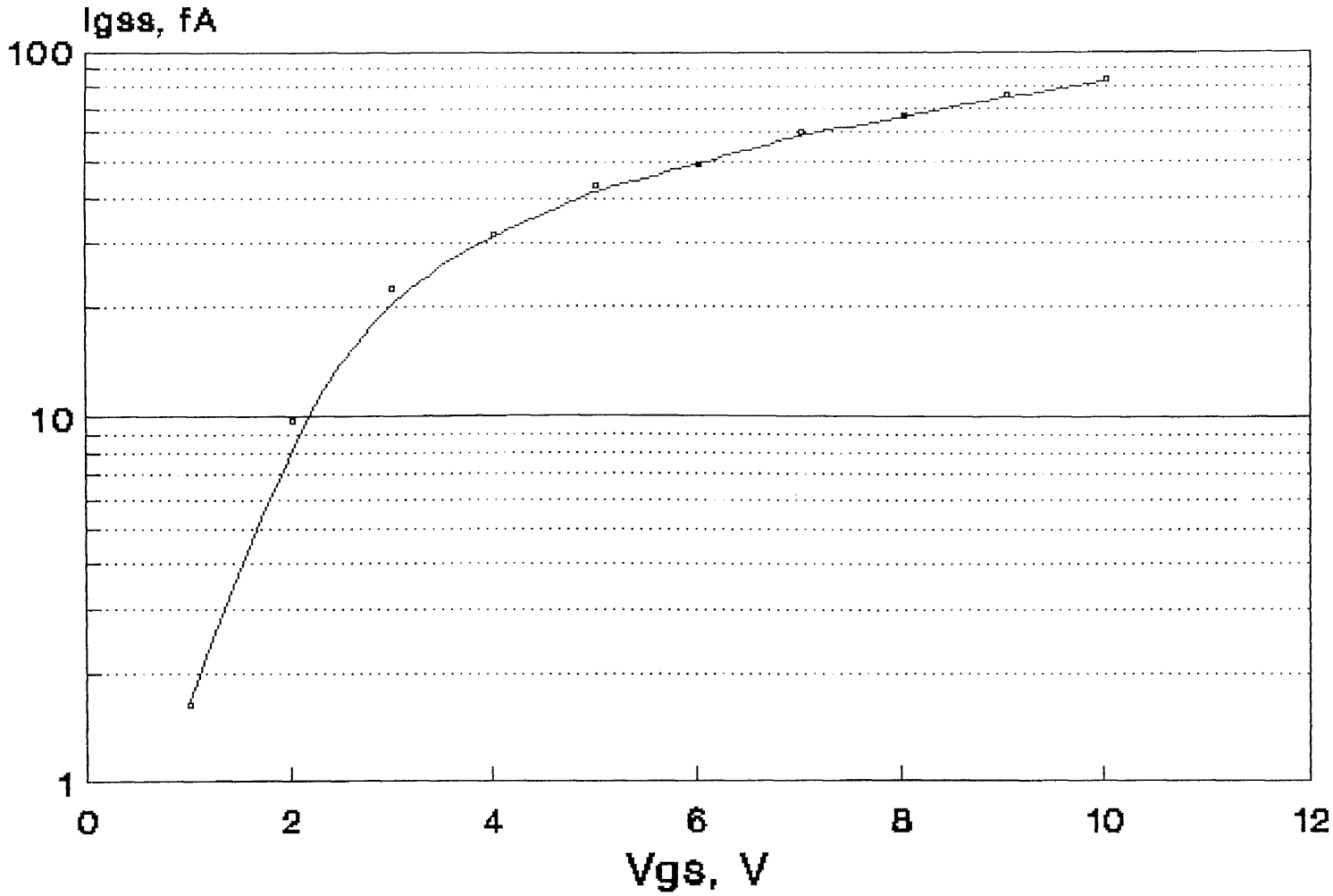


Figure 4.8 Dependence of the gate leakage current on voltage at 10K, $V_{DS} = 0$.

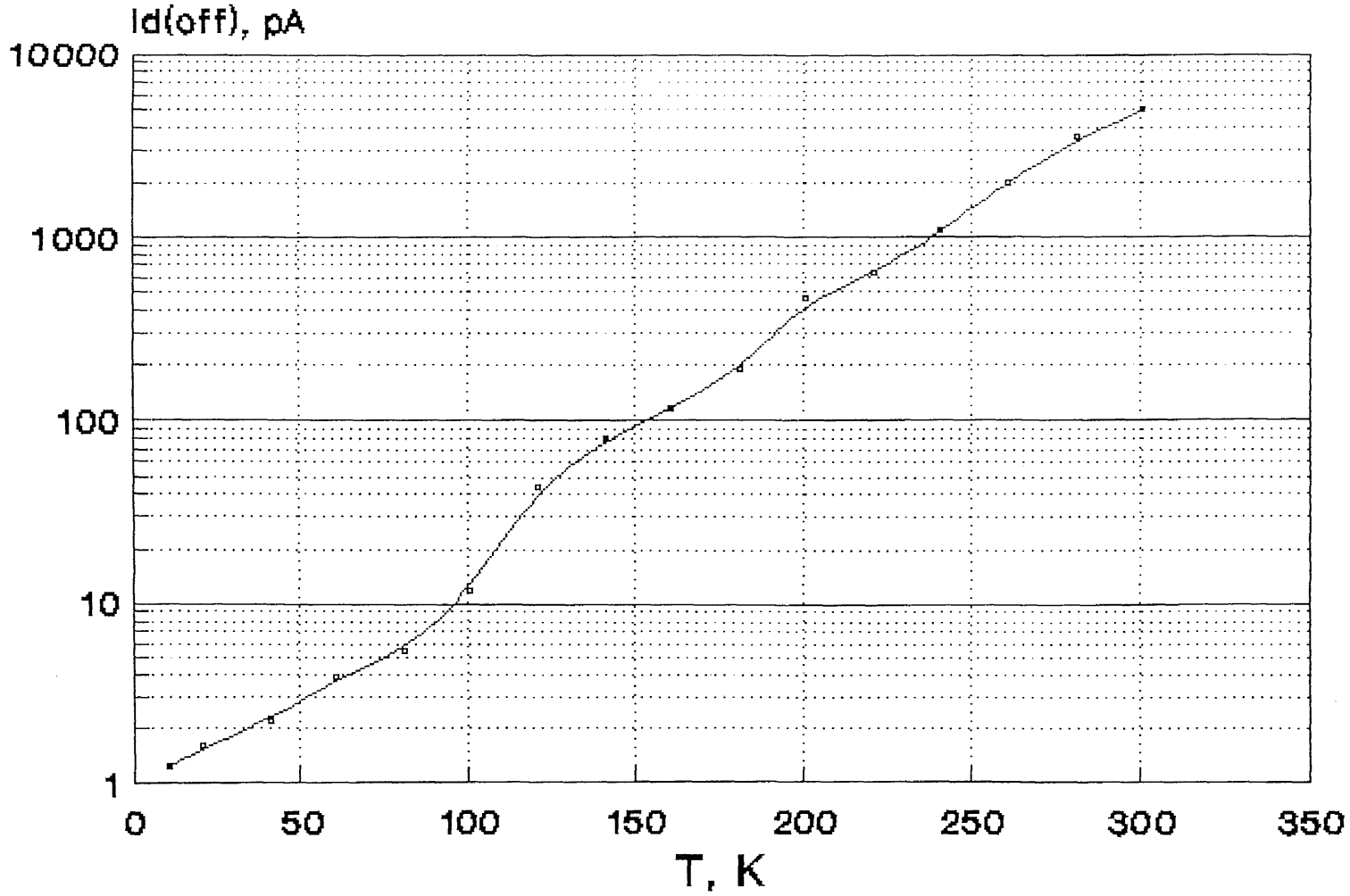


Figure 4.9 Temperature dependence of the drain leakage current for $V_{GS} = -5V$, $V_{DS} = 5V$.

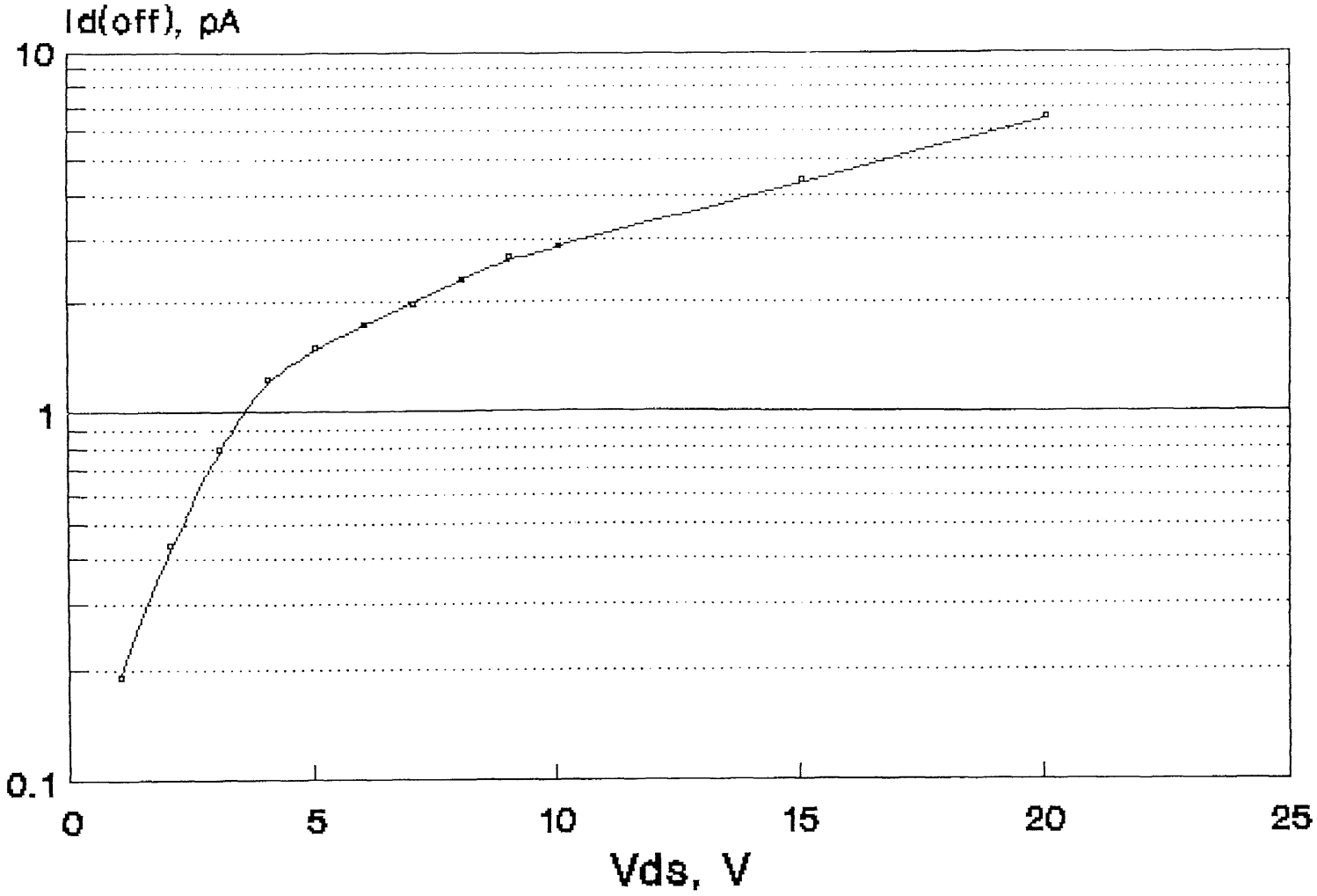


Figure 4.10 Dependence of the drain leakage current on voltage at 10K, V_{GS} = –5V.

4.2 Amplifying and Noise Properties

An increase in transconductance after cooling the transistors to 40K influences the improvement of their amplifying and noise properties. Amplification of a one-stage amplifier with a JFET in the configuration "common source" is proportional to g_m

$$k_u = -g_m Z_o \tag{4.4}$$

where k_u is the coefficient of voltage amplification, Z_O is the impedance of transistor loading and g_m is the transconductance of the transistor. The frequency bandwidth of the amplifier is defined by the cut-off frequency of the transistor and this is also proportional to g_m[9]

$$f_{\max} = \frac{g_m}{C_{11}} \tag{4.5}$$

where f_{max} is the cut-off frequency of the JFET, and C_{11} is the parasitic gate-channel capacitance. Therefore transistor cooling causes an increase in amplification and an increase in the cut-off frequency of the transistor. This has been verified experimentally[9].

The thermal noise of the channel and the *1/f* noise are the principle components of noise in the JFETs. The latter noise can be neglected for frequency >1kH$_Z$. The minimum of transistor noise occurs in the frequency range from 1 to 50 kH$_Z$. Thus, the thermal noise of the channel defines the level of noise, according to the relation given by Van der Ziel[10]

$$\overline{U_n^2} = \frac{8kT\Delta f}{3g_{ms}} \tag{4.6}$$

where

$\overline{U_n^2}$ = mean square noise voltage

k = Boltzmann's constant

T = absolute temperature

Δf = measurement bandwidth

g_{ms} = transconductance of the JFET for V_{GS} = 0V

The drop in temperature of the transistor from 300 to 40K and the increase in transconductance g_{ms} cause a total decrease in the level of noise.

CHAPTER 5
CONCLUSIONS

The current-voltage characteristics of silicon n-channel JFETs have been investigated in the temperature range 10 – 300K. Mobility and pinch-off variations dominate the temperature dependence of the characteristics over this temperature range. Bulk impurity freezeout also affects the *I–V* characteristics. Despite the great variation in temperature, the static device characteristics continue to have familiar behavior, even down to 40K.

After cooling down the transistors, their parameters change: pinch-off voltage and transconductance increase, and drain current is changed as a function of the drain-source voltage. The leakage current decreases exponentially with decreasing temperature and also exhibits a voltage dependence. The transistors work satisfactorily at the liquid nitrogen temperature (77K) but do not operate below 40K. So operation of silicon JFET circuits at 77K has been suggested as a means of improving circuit and system performance.

It was found that there was an improvement in the amplifying properties and a reduction in noise voltage of cooled transistors. This improvement in the parameters of the JFETs enables them to be used in cryogenic amplifiers and resulting in better parameters than for amplifiers at room temperature.

APPENDIX

PROGRAM FOR FET LEAKAGE TEST

```
'FET LEAKAGE TEST, QUICKBASIC VERSION. REV. 1.3
OPEN "\DEV\IEEEOUT" FOR OUTPUT AS #1    ' Open IEEE-488 output path.
OPEN "\DEV\IEEEIN" FOR INPUT AS #2      ' Open IEEE-488 input path.
IOCTL #1, "BREAK"                       ' Reset interface.
PRINT #1, "RESET"                       ' Warm start interface
PRINT #1, "CLEAR"                       ' Send device clear.
PRINT #1, "REMOTE 16"                   ' Put unit in remote.
CLS                                     ' Clear CRT.
OPTION BASE 1
DIM RX(101), RY(101)                    ' Dimension reading arrays.
PRINT #1, "OUTPUT 16;F0,1X"             ' Source V, sweep mode.
PRINT #1, "OUTPUT 16;O0T1,0,0,0X"       ' Local sense, trigger on GET.
PRINT #1, "OUTPUT 16;L1E-3,0X"          ' 1mA compliance,autorange measure.
PRINT #1, "OUTPUT 16;G5,2,1X"           ' Source, measure, no prefix, sweep.
PRINT #1, "OUTPUT 16;M2,X"              ' SRQ on sweep done.
PRINT #1, "OUTPUT 16;S2X"               ' Line cycle integration.
PRINT #1, "OUTPUT 16;B0,0,0X"           ' Program 0 bias value.
PRINT #1, "OUTPUT 16;Z1X"               ' Enable suppress.
Vstart = 0: Vstop = 10: Vstep = .1      ' Define voltage sweep parameters.
Delay = 100                             ' Define 100msec delay.
PRINT #1, "OUTPUT 16;Q1,"; Vstart; ","; Vstop; ","; Vstep; ",0,"; Delay; "X"
PRINT "Close lid, press any key to begin."
DO WHILE INKEY$ = "": LOOP              ' Wait for keypress.
```

```
PRINT #1, "OUTPUT 16;R1N1X"          ' Arm sweep, turn on 236 output.
PRINT #1, "TRIGGER 16"                ' Trigger sweep.
WaitForSRQ: PRINT #1, "STATUS"        ' Get bus status.
INPUT #2, ST$                         ' Input status string.
IF MID$(ST$, 11, 2) = "S0" THEN GOTO WaitForSRQ ' Wait for SRQ.
PRINT #1, "SPOLL 16"                  ' Serial poll 236 to clear
SRQ.
INPUT #2, SB
PRINT #1, "OUTPUT 16;N0X"             ' Turn off 236 output.
FOR I = 1 TO 101                      ' Loop for all 101 readings.
PRINT #1, "ENTER 16"                  ' Address 236 to talk.
INPUT #2, RX(I), RY(I)                ' Input voltage and current readings.
NEXT I                                ' Loop back for next reading.
CLOSE 1: CLOSE 2                      ' Close I/O files.
PRINT "Press key to display graph."
PRINT "Press key while in graph to end program."
DO WHILE INKEY$ = "": LOOP            ' Wait for keypress.
title$ = "Id(off) vs. Vds": xaxis$ = "Vds": yaxis$ = "Id(off)"'Plot data
X% = 1: Y% = 1: SYMBOL% = 0: NUM% = 101: PEN.NUM% = 2: LIN% = 1:
MODE% = 16
CALL GRID(1)
CALL SCREENMODE(MODE%)
SCREEN 9
CALL GRAPHXY(SEG RX(1), SEG RY(1), NUM%, X%, xaxis$, Y%, yaxis$,
title$, LIN%, SYMBOL%, PEN.NUM%)
DO WHILE INKEY$ = "": LOOP
END
```

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