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ABSTRACT

A PROGRAMMABLE INTEGRATED POWER SUPPLY FOR ELECTROSTATIC-DRIVE MICROMOTOR

by
Chao Ye

A 6-phase bipolarized, high-voltage power supply with rectangular pulse shape has been designed to study the special operational characteristics of various electrostatic-drive micromotors. In particular the design powers the variable-capacitance side-drive micromotor. This power supply provides variable frequency, variable voltage, and variable duty-cycle control. Simulation has been used extensively in the design and design verification.

The bipolarization (dual voltage polarity) of each pair of the phases reduces physical clamping of the rotor to the electrical shield beneath it. Thus, bipolarization of the voltage supplied to the stator nodes reduces charge build-up on the rotor.

The output frequency range varying from 1Hz to 40KHz has been achieved. This supply frequency range corresponds to motor rotational speed range of 5rpm to 200Krpm, for a micromotor with 12 stator poles and 8 rotor poles (3:2 architecture). The voltage amplitudes of all six phases can be varied from 20 to 200Volts.

The duty cycle of each phase can be changed by means of a parallel register. The output with variable duty cycle has been obtained, changing from 50% non-overlapping to 33% overlapping.

The power supply with 6-phase bipolarized output, variable frequency, and variable voltage output has been constructed with prototyping wire wrap boards, and assembled in a card cage. The power supply is shown to meet the design specification.

A PROGRAMMABLE INTEGRATED POWER SUPPLY FOR THE ELECTROSTATIC-DRIVE MICROMOTOR

by
Chao Ye

A Thesis
Submitted to the Faculty of
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Master of Science

Department of Electrical and Computer Engineering

January, 1993

APPROVAL PAGE

A Programmable Integrated
Power Supply for
The Electrostatic-drive Micromotor

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This thesis is dedicated to
my dear parents, my sister,
and all my close friends

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CHAPTER 1

INTRODUCTION

Silicon micromachining has been developed over the last decade as a means of accurately fabricating very small structures in situ without the assembly of discrete components. Recently, silicon micromachining technology has been extended to provide rotary or linear bearings, thereby allowing unrestricted motion of the moving component in one degree of freedom These bearings permitted the demonstration of electrically-driven motors, referred to here as micromotors.

Micromotors have a planar geometry with a gap separation in the order of 1 ~ 2 μm and lateral dimensions on the order of 100 μm or more. Their very small size, particularly their micro-scale gap separation, and the characteristics of silicon micromachining combine to provide micromotors with important electromechanical characteristics which are significantly different from those of conventional motors.

Recently there has been a slight decline in micromotor research, because the application of micromotors has been delayed by limitations of their characteristics such as difficulty in coupling power out. However, the study of various electrostatic-drive micromotors still has a lot of academic attraction and remains an active field in silicon micromachining after almost four years of research by scientists. Researchers are still trying to understand the failure mechanism of the operation of the micromotors, and more are working on novel designs of various micromotors.

Figure 1.1 shows a electrostatic micromotor in top and side view. Figure 1.2 is the SEM photograph of the variable-capacitance side-drive micromotor first fabricated by Fan, Tai, and Muller (UC Berkely) in 1988 [1]. At almost the same time Mehregany, Nagarkar, Senturia and Lang (MIT) fabricated their first electrostatic-drive micromotor [2]. This structure comprises a rotor which is pinned to a substrate

or stator by a central bearing which restricts the lateral and axial motion of the rotor. The rotor is shown suspended above the substrate to illustrate its freedom to rotate about the bearing Silicon micromachining is ideally suited to the fabrication of a controlled micro-scale gap between the rotor and stator of a micromotor. This is essential if substantial torques or force are to be produced by an electrostatic, rather than magnetic induction, micromotor.

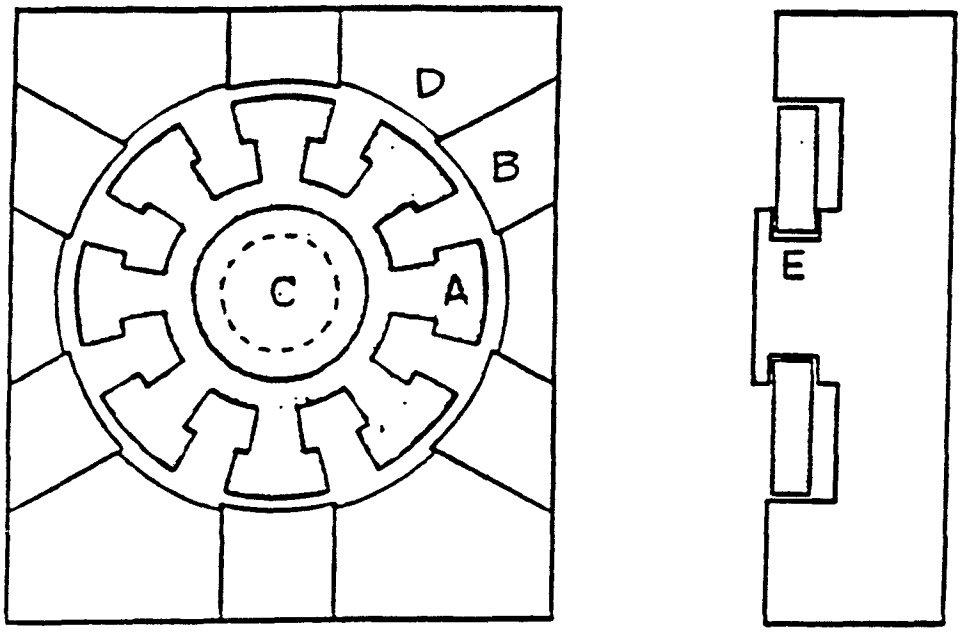


Figure 1.1 Electrostatic micromotor system.
(a) Top view. (b) Side view [1]

In order to study the special characteristics of various micromotors, we need to operate them under different conditions, e.g., varying rotating speed, varying power supply voltage, varying duty cycle of the power pulses, etc. These requirements constitute the specification for the power supply design of this thesis. This supply is basically a 6-phase bipolarized, high-voltage square-wave power supply with varying frequency (1Hz to 40KHz), varying voltage (20volts to 200volts), and varying duty

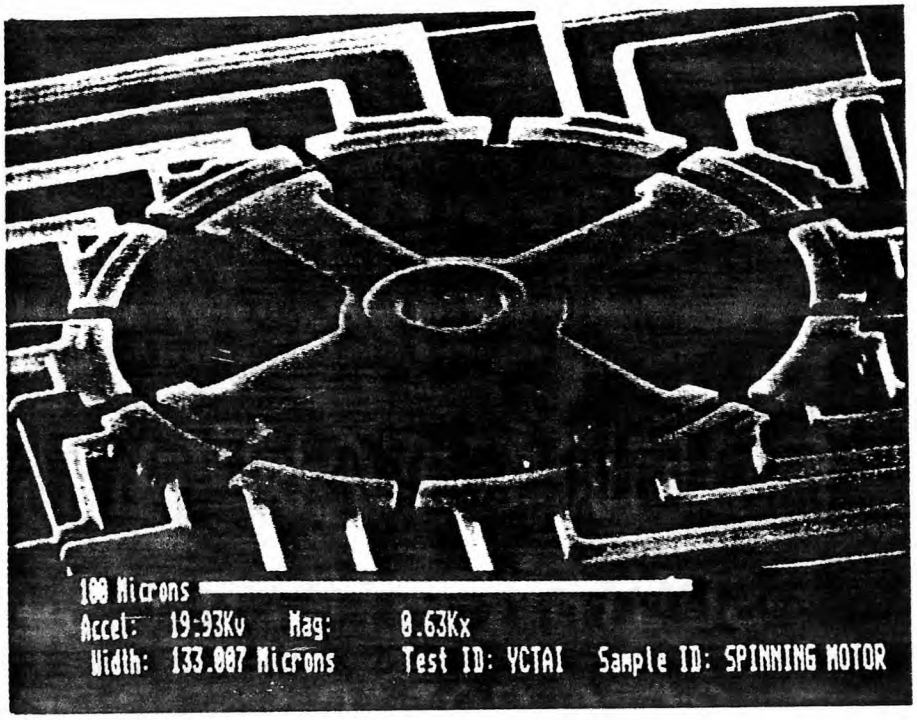


Figure 1.2 SEM photograph of a fabricated micromotor [1]

cycle (either non-overlapping or overlapping). Figure 1.3 shows a functional diagram of the power supply for micromotors

Chapter 2 presents the fundamental principles of micromotor operation, its testing requirement and some of its basic characteristics, focusing on normal variable-capacitance side-drive micromotor.

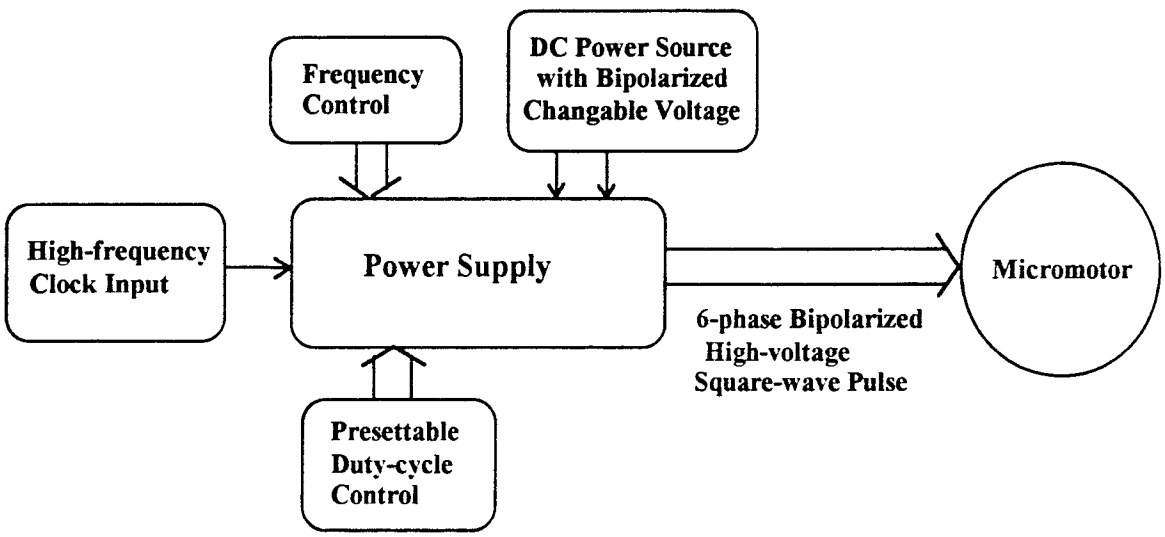


Figure 1.3 Functional Diagram of the Power Supply for Micromotors

The electrical design specification of the entire power supply including the digital circuit and the analog high-voltage drivers is presented in Chapter 3.

The detail circuit design, analysis, simulation and layout of the programmable integrated digital circuit of the power supply are presented in Chapter 4, using VLSI design tools, Mentor Graphics' Design Architecture, QuickSim II and ICgraph (layout). Also, the MOSIS database in CIF format is extracted from the physical layout for IC chip fabrication.

Chapter 5 discusses the design and analysis of the analog high-voltage drivers circuit , in which power transistors work in a switching mode to generate high-

voltage, bipolarized square-wave pulses Circuit simulation has been done with PSPICE.

Chapter 6 describes the digital and analog circuits which have been implemented on Plugbord prototyping boards using the wirewrap prototyping technique. Engineering acceptance testing of the power supply indicates acceptable performance with up to 40KHz output frequency

Finally, the summary and conclusions of this work are presented in Chapter 7

CHAPTER 2

PRINCIPLES OF MICROMOTOR OPERATION AND TESTING REQUIREMENTS

2.1 Operation of Electrostatic-drive Micromotor

In 1988 operation of the first electrostatic-drive micromotor were described by Fan, Tai, and Muller [1], and by Mehregany, Nagarkar, Senturia and Lang [2] These were electrostatic, normal side-drive micromotors. Since then a second type of micromotor has been described, the variable-capacitance harmonic side-drive (wobble) micromotor. Although the variable-capacitance wobble micromotor has potentially important characteristics, some novel designs, and some attractive advantages [2], the task of the present thesis is to design and test a power supply for the normal variable-capacitance side-drive micromotor

2.1.1 Basic Structure of VC Side-Drive Micromotor

Figure 2.1 shows an SEM photograph of a variable-capacitance side-drive micromotor, with 12 stator- and 4 rotor-poles. This micromotor was fabricated using a three-layer polysilicon process [1] Figure 2.2 is the cross section schematic for this same micromotor. The SEM close-up of the coplanar rotor-stator structure and the motor hub are shown in Figure 2.3 and 2.4 from Reference [1].

The processing of the micromotors from Reference [3] is simplified into 5 steps showing the cross-section of the device in Figure 2.5.

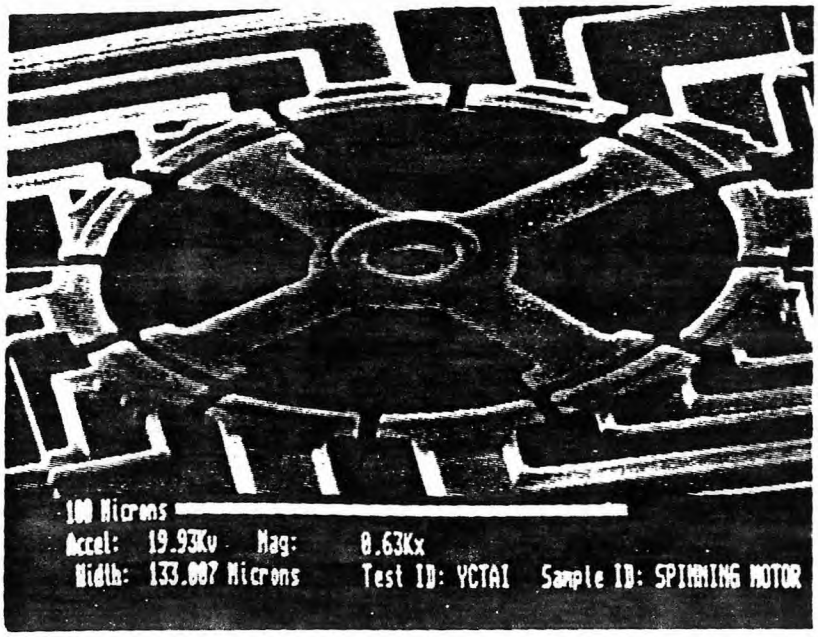


Figure 2.1 SEM photograph of a fabricated micromotor; rotor diameter = 120 μm. [1]

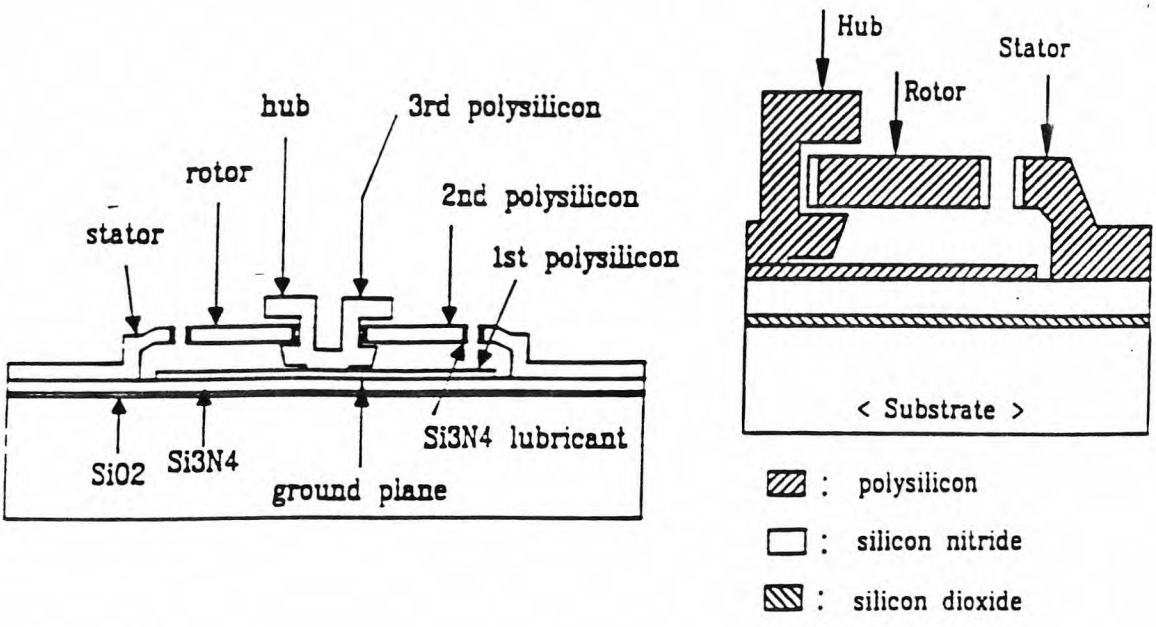


Figure 2.2 Schematic cross section of the micromotor in Figure 2.1. [1] [3]

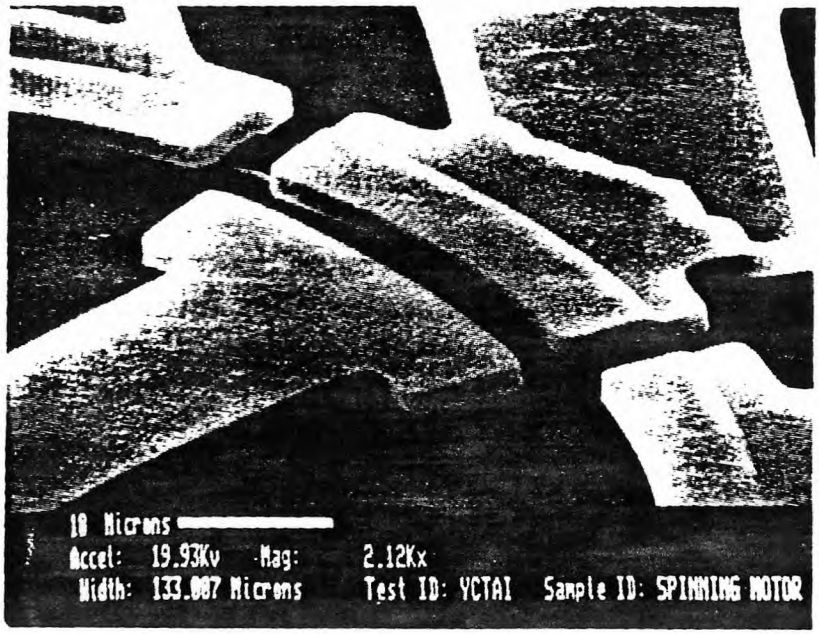


Figure 2.3 SEM close-up of the coplanar rotor-stator structure. [1]

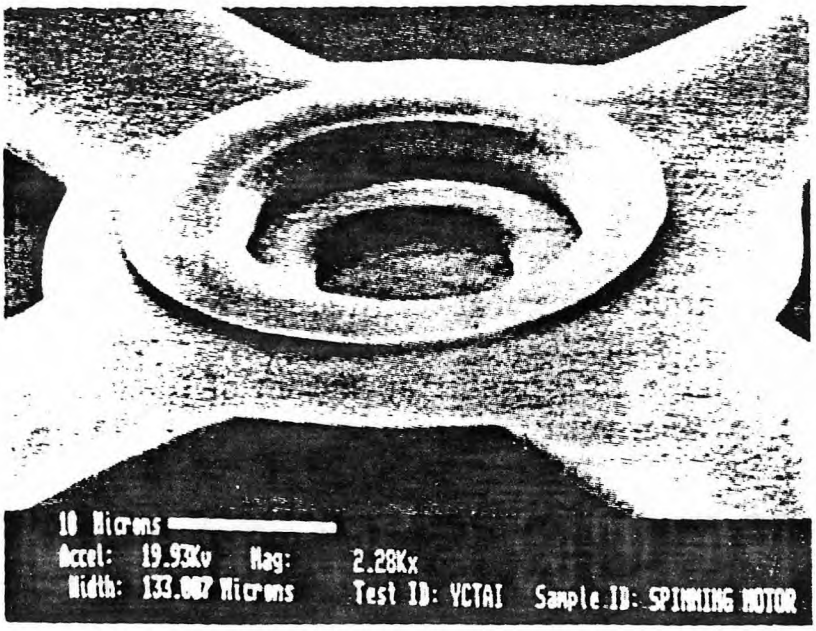


Figure 2.4 SEM close-up of the micromotor hub. [1]

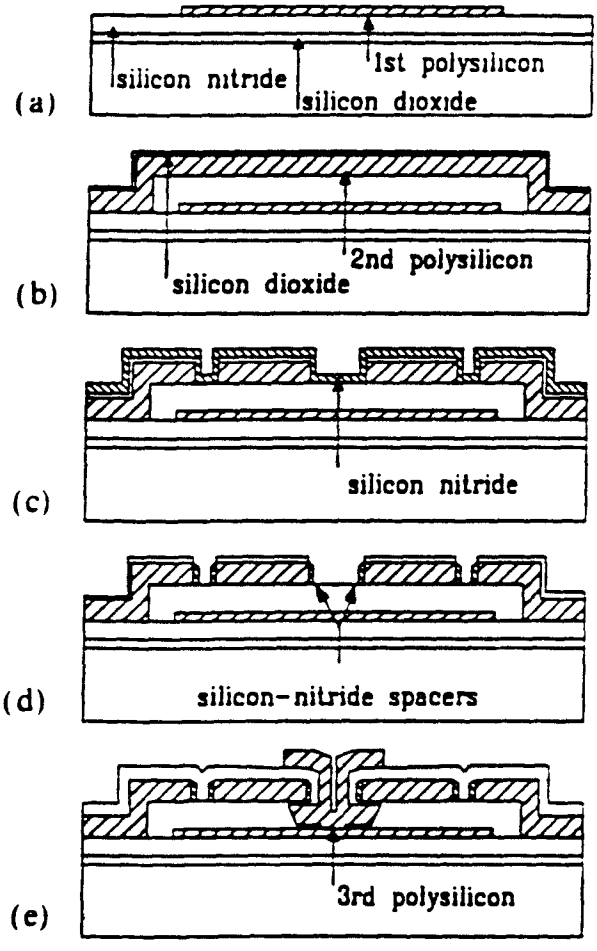


Figure 2.5 Cross-section of major fabrication steps showing construction of the hub, rotor and stator. [3]

2.2 Basic Theory of Motor Dynamics for VC Side-Drive Micromotor

Since 1989, the basic theory of micromotor dynamics has been developed successfully by scientists, mainly at UC Berkeley and MIT [1][2]][3][4], although clear insight into some tricky problems still is lacking. In this chapter, basic motor dynamics for the variable-capacitance side-drive micromotor will be presented based on the work done by those above two groups. Simulations which confirm these results have been obtained by a graduate student at NJIT, Hong Yu, in his Master thesis of 1990 [5].

The design of a rotating motor begins with an estimation of the torque exerted by the electric field. This can be expressed in terms of the derivative of the stored electrical co-energy which, for a given bias V between rotor and stator, is conveniently represented as 1/2 CV^2, where C is the capacitance across the driving electrodes. To find the rotor torque T per phase, we take the derivative of the co-energy with respect to the rotor angle θ after the method of Hamilton:

$$T(\theta) = \frac{1}{2} V^2 \frac{\partial C(\theta)}{\partial \theta} \qquad (2.01)$$

Torque values are of the order of pN-m (voltage of order 100V and typical micromotor dimensions)

A two-dimensional electrostatic numerical simulator Ansoft MAXWELL has been used to calculate the static-torque/rotor-position characteristics.[1][3] As an example, the simulation results of the torque/position characteristics associated with four equi-positioned stators energized at 200 V (with the remaining eight stators grounded) is shown in Figure 2.6. The torque on the rotor is obtained by multiplying the simulated torque density times the thickness of the rotor (therefore neglecting three dimensional effects). Figure 2.6 has a span of only 90^o because the torque/position characteristic is periodic for this four-pole rotor.

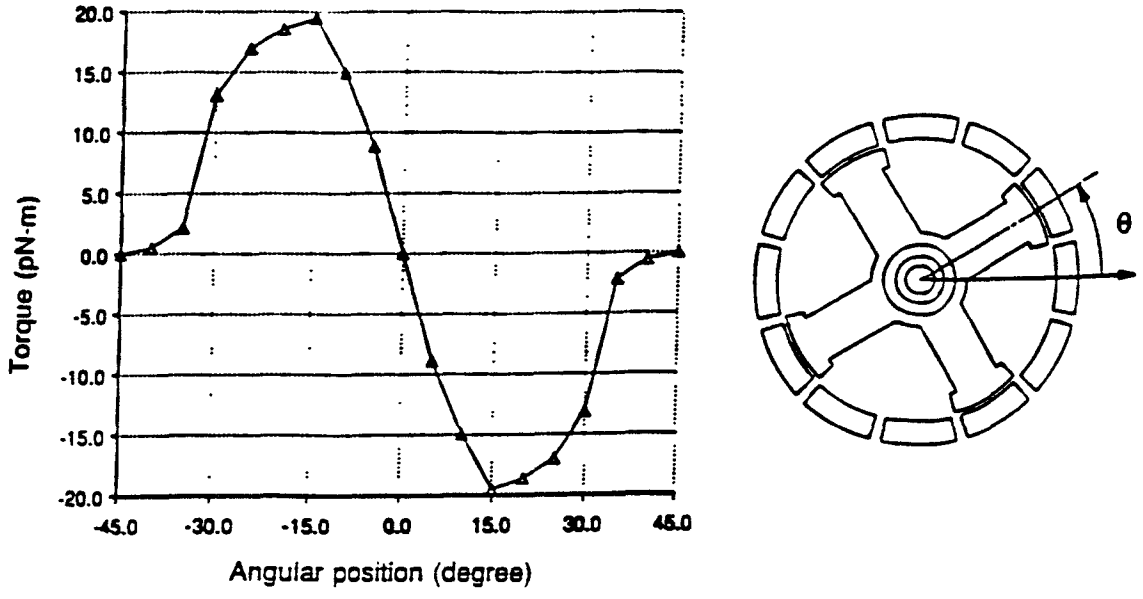


Figure 2.6 Torque/position characteristics of the micromotor as obtained from two-dimensional electrostatic simulation. [1]

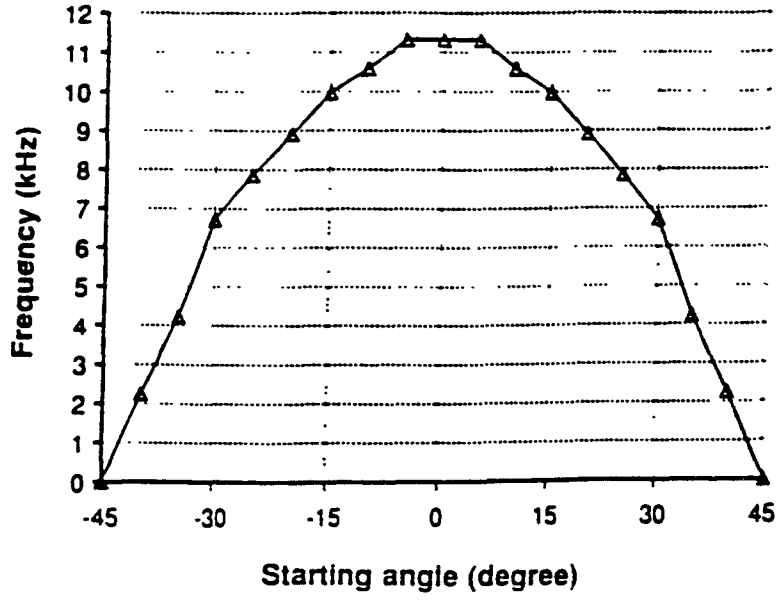


Figure 2.7 Numerical results of the oscillating frequency as a function of the starting angle. The rotor-stator bias is 200V. [3]

Assume that this micromotor operates in a stepping mode. A natural frequency, f_N, is an important parameter to characterize the motor. This frequency, which also exists for electromagnetically driven motors, arises from energy exchange between the electric field and the moving rotor. To calculate f_N, we consider rotor dynamics near an equilibrium (T=0) point assuming zero friction. The equation of motion governing the rotor is

$$I\ddot{\theta} + T(\theta) = 0 \tag{2.1}$$

where I is the rotational inertia of the rotor and $T(\theta)$ is the driving torque as a function of θ as shown in Fig. 2.6. In general, the oscillating frequency can be calculated by solving Eqn (2.1) to find

$$f_N(\theta_S) = 1/\left[4 \int_0^{\theta_S} \frac{d\theta}{\left(2I^{-1} \int_{\theta_s}^{\theta} T(\eta) d\eta \right)^{1/2}} \right] \tag{2.2}$$

where η is a dummy variable of the angular position and $T(\eta)$ is the torque in Figure 2.6. Equation (2.2) shows that the oscillating frequency is a function of the starting angle θ_S because of the shape of $T(\theta)$. The torque-angle relationship based on Equation (2.2) can only be calculated using numerical methods. The results are shown in Figures 2.6, 2.7, 2.8, where the rotational inertia for the rotor is 2.01×10^{-20} kg m^2 and the stator-rotor bias is 200V. Figure 2.7 shows that a small starting angular position has a larger natural oscillating frequency. As an example, the oscillating frequency for θ_S=30^o is 6.7 kHz and is 10 kHz for θ_S =15^o. Not only starting position but also bias voltage can change the oscillating frequency

Since the electrostatic torque acting on the rotor is proportional to the square of the voltage, the natural frequency at a different phase voltage Vp is

$$f_N(V_P) = f_{N,200}\left(\frac{V_P}{200}\right)^2 \text{ kHz} \tag{2.3}$$

where $f_{N,200}$ is the oscillating frequency (calculated in Figure 2.7) at a bias of 200 V

It is also interesting to note that when the starting angle is small and near zero, Eqn. (2.2) reduces to

$$f_N = \frac{1}{2\pi}\left(\frac{T'}{I}\right)^{1/2} \tag{2.4}$$

where $-T'$ is the slope of the T versus θ curve (Figure 6) at $\theta = 0$. Equation (4) is similar to the equation for the oscillating frequency of a spring-mass resonant system In fact, Eqn (2 4) gives the maximum oscillating frequency of the rotor

2.2.1 Maximum Rotational Speed

If we assume that the micromotor operates in a stepping mode, then the natural frequency of the motor sets an upper bound for the rate at which the rotor can respond to a switched field on the stators Here, we argue that $1/4f_N$ is the minimum time for the rotor to travel from a starting angle θ_S to $\theta = 0$ (see Figure 2.6) if the inertial angular velocity is zero as is the case for start/stop-mode stepping motors. In term of a maximum rotational speed ω_{max}, we then have

$$\omega_{max} = \frac{1}{(1/4f_N)n} \times 60 = (240 f_N / n) rpm \tag{2.5}$$

where n is the number of steps per revolution. As an example, with V_P=200 V, n=12 and θ_S=30°, f_N is 6 7 kHz and, therefore, the maximum speed of the stepping motor is predicted to be 134 krpm using Eqn. (2.5)

Experimentally, the micromotors fabricated at UC Berkeley in 1989 are found to have start/stop stepping motion when biased under open-loop control. As a result,

the argument about zero starting velocity is reasonable. However, Eqn. (2.5) only predicts an upper bound for the open-loop driving frequency. The real maximum open-loop driving frequency will be lower than predicted if the rotor velocity at each end of a step is also zero, because there is no constraint on zero-ending velocity in Eqn. (2.5). However, in order to predict the true maximum driving frequency, we must know the exact loading of the rotor.

Loading effects (other than inertial) on the rotor have so far been neglected in the analysis. These effects, principally friction, reduce the effective maximum frequency below the calculation in Eqn. (2.5) From the experiments made at UC Berkeley, friction effects completely dominate the dynamic behavior of the motor because its observed maximum rotational speed at 200 V bias is 300 rpm, far less than the 134 krpm predicted by Eqn (2 5). With friction, the equation of motion becomes

$$I\ddot{\theta} + T(\theta) + \mathrm{sgn}(\dot{\theta}) \times T_{\mathrm{fric}}(\theta) = 0 \qquad (2.6)$$

where sgn($\dot{\theta}$) is the sign function of angular velocity $\dot{\theta}$ and is +1 if $\dot{\theta}$>0 and -1 if $\dot{\theta}$ <0. $T_{\mathrm{fric}}(\theta)$ is the magnitude of the frictional torque Therefore, the damped oscillating frequency can be calculated by substituting $T(\eta)$ in Eqn. (2.2) with $T(\eta)+\mathrm{sgn}(\dot{\eta}) \times T_{\mathrm{fric}}(\eta)$. At present, insufficient information is available about friction in the motors to proceed further with this analysis.

When the friction is reduced to a low enough level, then the micromotor no longer operates in a stepping mode. Such a motor such as the design of Hong Yu [5] will have its maximum rotational speed limited only by the mechanical stability of the device.

The foregoing discussion refers to constant frequency open-loop drive of the motor, which is the mode having been used for most experiments. It is important to

know that the natural frequency limitation on the speed of the motor could be exceeded with either time-varying frequency open-loop control or closed-loop control. Time-varying frequency open-loop control requires exact knowledge of friction, which people do not have Closed-loop control. on the other hand, would require additional rotor-position sensors.

2.2.2 Forward (Synchronous) and Reverse (Asynchronous) Rotor Motion

Another surprising result from dynamic studies of the motors, in addition to the frictional effects on the motor speed discussed above, is the observation of reverse (asynchronous) as well as forward (synchronous) motion in the motors first fabricated by UC Berkeley. Specifically, people have observed that it is possible for the rotor to rotate in opposition to the rotational sense of the phasing field (reverse, or asynchronous mode). This behavior can be understood in terms of the dynamic balance between electrostatic-drive torque and that due to friction.

It is easiest to introduce this concept by considering a motor driven by only one phase of the three-phase voltage drive. The inset of Figure 2 8 shows the voltage connections for single-phase drive of the motor of Figure 1 as well as a defining condition for the initial position of the rotor (θ=30^{o}). The angle θ is measured from a rest position (T=0) The main part of Figure 2 8 (which is similar to Figure 2.6) is the corresponding normalized torque/position characteristic The straight lines indicate assumed constant frictional-torque values which oppose the applied torque T.

Consider that the horizontal stator (Figure 2.8, inset) is energized Since T exceeds the frictional value, the rotor will begin to rotate in the clockwise direction and will accelerate until it reaches angle P, at which the frictional torque equals the driving torque. As θ decreases toward zero, the rotor will decelerate because of friction. Whether the rotor passes through θ=0 depends upon specific values for frictional and driving torque as well as on the rotor inertia. If it passes θ = 0, the rotor

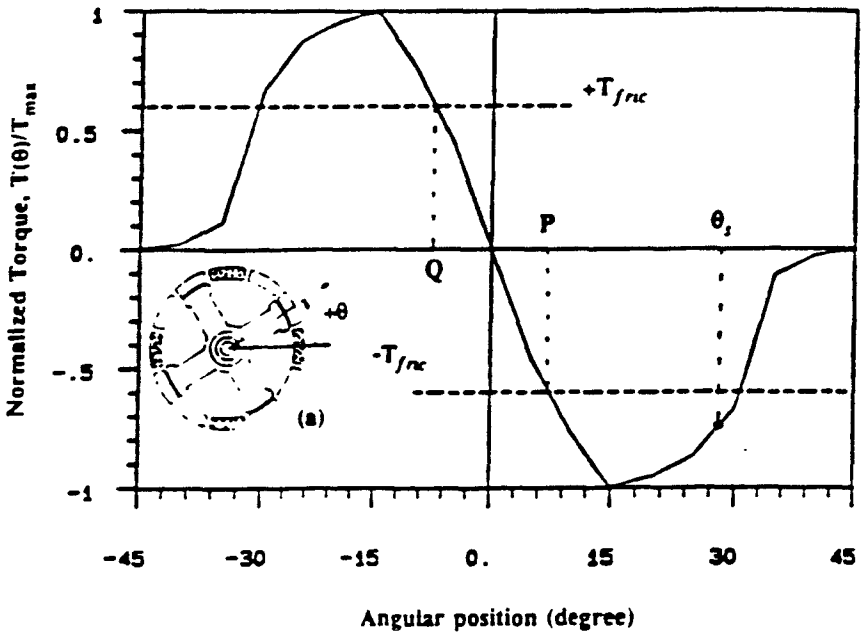


Figure 2.8 Electrical connections (inset) and single-phase torque/position characteristics of the micromotor. [3]

will continue to decelerate between θ=0 and θ=*Q*. The rotor may stop anywhere between angles *P* and *Q*, but if it can pass point *Q*, it will decelerate more strongly because the driving torque is reversed in this region. If the rotor stops between θ=*Q* and θ=-30^{o}, it will accelerate again, but this time in a counter-clockwise direction. Once again, the rotor will repeat a similar acceleration-deceleration-stop cycle, except that the direction of rotation is different. Several cycles may occur, but eventually the rotor will stop between θ=*P* and θ=*Q*.

The final resting place of the rotor after the cyclic motion discussed above (when the motor is energized by a single phase) indicates whether forward (synchronous) or reverse (asynchronous) rotation will occur in the motor when it is driven by three phases power. Forward-rotation or the anomalous reverse-rotation results primarily from the initial rotor angle with respect to the nearest stator pole.

(a) Three-phase Forward (Synchronous) Mode

Normalized three-phase torque/position characteristics of the motor are shown in Figure 2.9 for the forward mode. In Figure 2.9, the drive voltages are phased $\pm 30^{o}$ apart because the motor has twelve stator poles. The starting position is again assumed to be at $\theta=0$. In Figure 2.9, $\theta=P$ and $\theta=Q$ are the angles at which frictional and driving torque are in balance for phase A, and $\theta=R$ is one of the corresponding angles for phase B. We conclude that if a static three-phase excitation of the stator field results in a final resting position for the rotor between $\theta=P$ and $\theta=R$, or any of the corresponding $(m\pi/6)$-shifted regions (where m is an integer), the rotor will follow the stator signal synchronously.

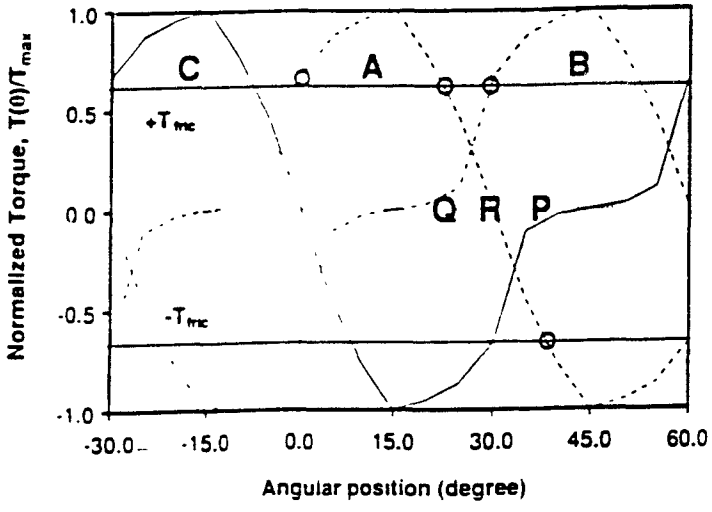


Figure 2.9 Three-phase torque/position characteristics. If the rotor rests inside $\overline{PR}$, it can rotate synchronously with the driving field. [1] [3]

The explanation is as follows. Based on the discussion for single-phase excitation above, the rotor would tend to rest inside the frictional band, either between θ=P and θ=R, or between θ=R and θ=Q. If the former (see Figure 2.9), then the rotor will rotate clockwise because of the positive, larger-than-friction, driving torque from

phase B. A similar behavior would be repeated with respect to phase C, so that the rotor would rotate synchronously with the field following phases ..ABCABC....

(b) Three-phase Reverse (Asynchronous) Mode

The motor and field rotation will be in opposite directions, however, if the rotor rest position under the conditions described in Section (a) above occurs between θ=R and θ=Q or its (mπ/6)-shifted regions as shown in Figure 2.10. The reason is as follows.

If, after phase A, the rotor rests between θ=R and θ=Q, the next phase B will not be able to rotate the rotor because inside that region (see Figure 2.10) the driving torque produced by this phase is smaller than the maximum frictional torque. However, phase C will apply a negative torque, which can overcome the friction on the rotor and make it rotate in a clockwise direction, opposite to the rotation of the stator fields For continuous motion phase C must leave the rotor at rest inside (-30°-shifted) $\overline{RQ}$. Then the next phase A will not be able to turn the rotor because of the friction. However, the following cycle of phase B will again cause counter-clockwise rotation A feature of this motion is that the rotor turns at only one-half the frequency of the driving fields because it is driven during only one half of the driving phases; for an applied signal...ABCABC..., the rotor rotates...ACBACB....

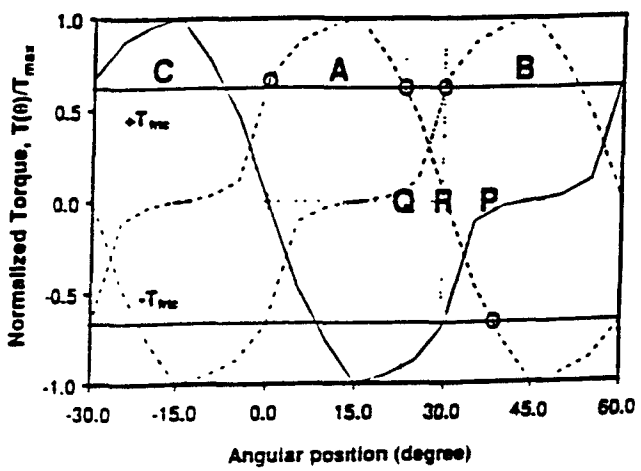


Figure 2.10 Three-phase torque/position characteristics. If the rotor rests inside $\overline{RQ}$, it rotates in the opposite direction to the driving field. [1] [3]

Experimentally, both modes have been observed. In some cases, it appears that both forward and reverse rotor motion alternate spontaneously. It is believed that this behavior can be explained by irregular friction from place to place in real motors, since friction determines the critical-angle values for the rotational variations described above.

2.3 Characteristics of Micromotors and Testing Requirements

Although the experimental data of micromotor operation based on the reports from various researchers showed a large variation, some basic characteristics of micromotors (which here is basically variable-capacitance side-drive one without air-levitation assist) can still be extracted as follows.

1. Experimental starting voltages are 60V ~ 100Volts, which are at least an order of magnitude larger than had been expected. And starting torque is around 10 pN-m
2. Maximum rotatonal speeds in the stepping mode under three-phase bias at 200V ~ 300V are varying from several hundred rpm to several thousand rpm, which are far below what should be achievable if only natural frequency were to limit the response. This is because the unexpected large friction associated with the clamping of the rotor to the electric shield beneath it.
3. Both forward (synchronous) and reverse (asynchronous) rotor motion have been observed experimentally. In some cases, it appeared that both motions alternated spontaneously because of the irregular friction from place to place in real motors or the uneven gap separations.
4. Without levitation, the micromotor has only operated for several hours due to the frictional forces associated with the clamping of the rotor to the electrical shield beneath it. This rotor clamping was attributed to electric fields between the rotor, the shield, and the bearing, due to a lack of proper electrical contact between these respective parts.

CHAPTER 3

ELECTRICAL DESIGN SPECIFICATION

3.1 Requirement for the Power Supply

The power supply specifications for electrostatic-drive micromotors are as follows:

1. A 6-phase bipolarized power supply with a rectangular pulse shape is required for this design. The term "bipolarized" refers to the balanced positive/negative voltages that are required for opposite-positioned stators. A 3-phase power supply is inadequate, because bipolarity in each phase is required to prevent, or at least reduce physical clamping of the rotor to the electric shield beneath it caused by poor electrical contact between these two structures
2. Each pair of bipolarized pulses is symmetrical with respect to the ground ("0" potential). Each pair of voltages energize stator pole pairs which are spatially symmetrical with respect to the center of motor, as shown in Figure 3.1 and 3.2.
3. The frequency and voltage are under manual control The signal output frequency range required is from 1Hz to 25KHz. For a stator · rotor = 12 : 8 motor (3 : 2 architecture), this output frequency range corresponds to a motor rotational speed range of: (1/12)x60 = 5rpm to (25K/12)x60 = 125Krpm.
4. The voltage amplitudes of all 6 phases are equal but must be varied together as a group from +20 to +200Volts and from -20 to -200Volts. The large voltage ranges are required based on previous research on micromotors, which often resulted in unexpected large starting voltage and operational voltage values.
5. Although basically power supply with non-overlapping pulses is required for the operation of normal variable-capacitance side-drive micromotor, a 6-phase power supply with variable duty-cycle (either non-overlapping or overlapping) pulses is strongely preferred for the study of micromotors operated under different duty cycle

voltage biases. The power supply is to be designed with programmable, or presettable variable duty cycle (pulse width) at a fixed frequency.

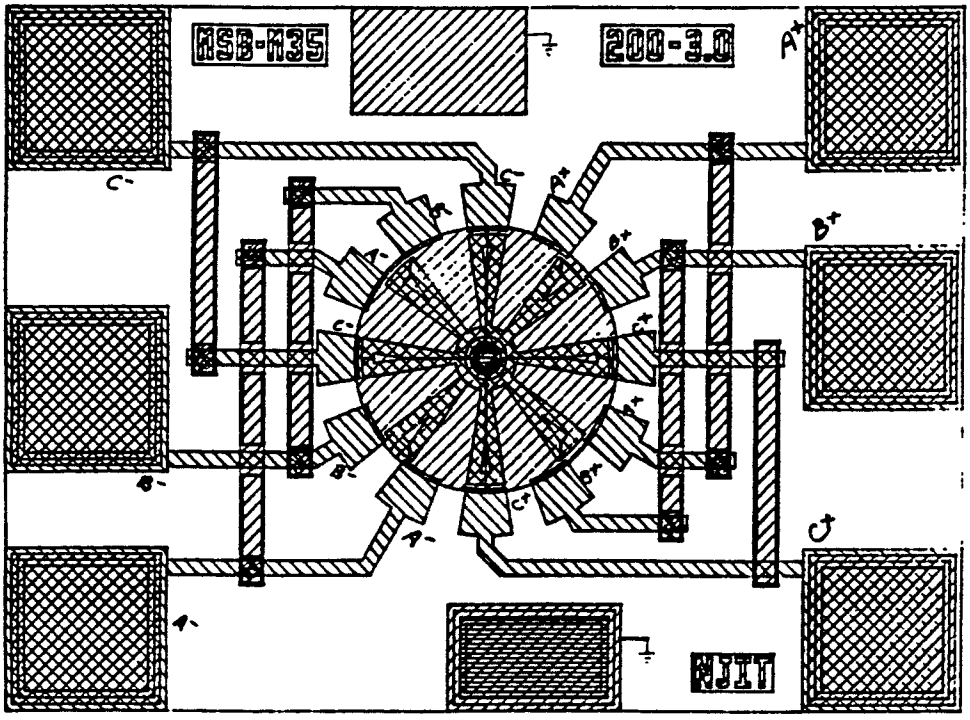


Figure 3.1 A 12:8 Micromotor with a 6-phase Bipolarized Power Supply Requirrement

The desired waveform from the power supply is shown in Figure 3.2 for a duty cycle of 100%. Note that in Figure 3 2(a) the six phases are arranged in the order of A+, B+, C+, A-, B-, C-, and in Figure 3 2(b) in symmetrical pairs, that is (A+, A-), (B+, B-), (C+, C-). Both figures show a case of exact non-overlapping pulses, 100% duty cycle (which is basically needed for normal variable-capacitance side-drive micromotor testing), while 100Volts is chosen as the magnitude of DC power source V_{dd} and $-V_{SS}$, whose polarity is opposite to each other.

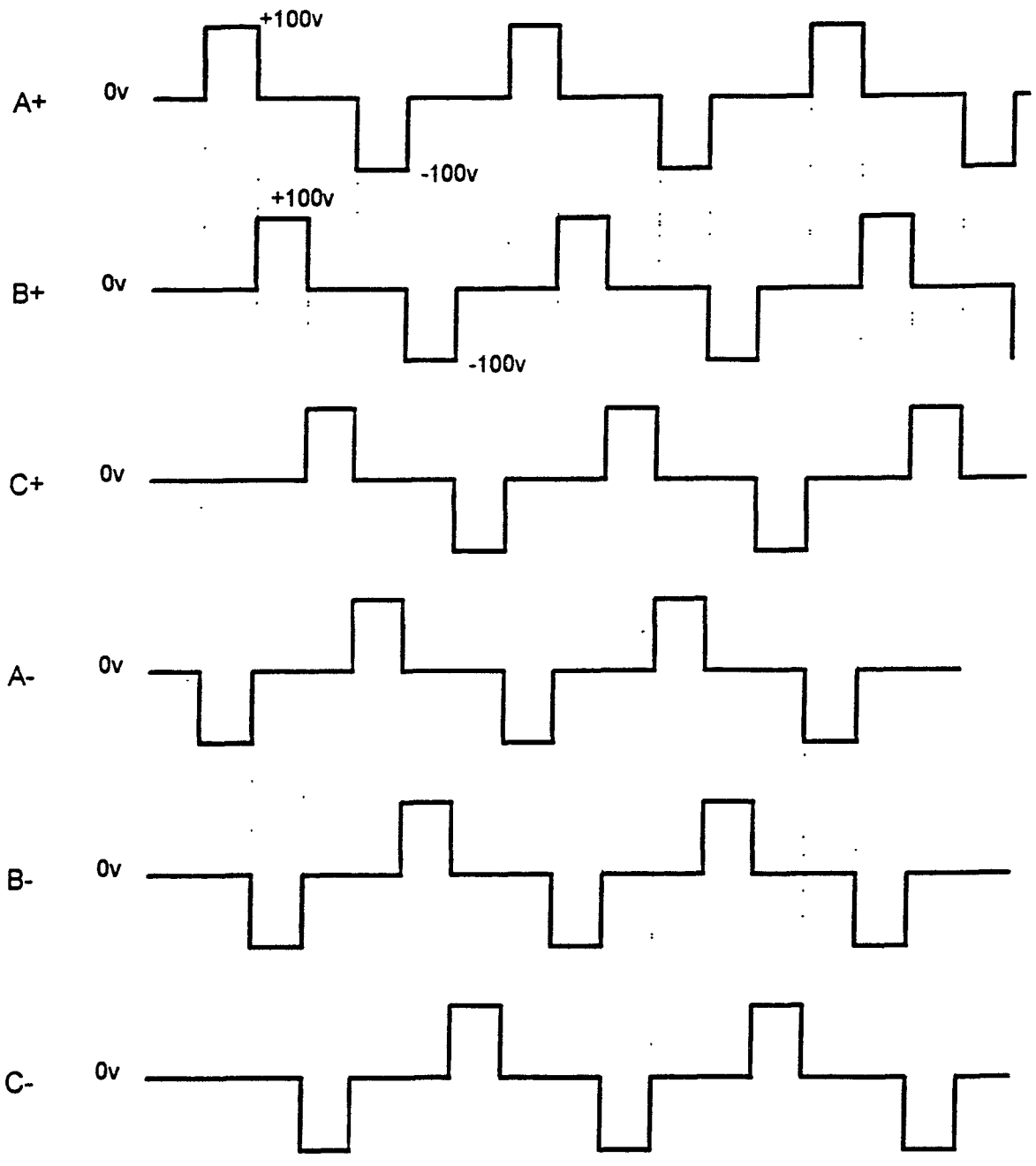


Figure 3.2(a) Six-phase bipolarized high-voltage square-wave pulses. (Non-overlapping case. 100% duty cycle).

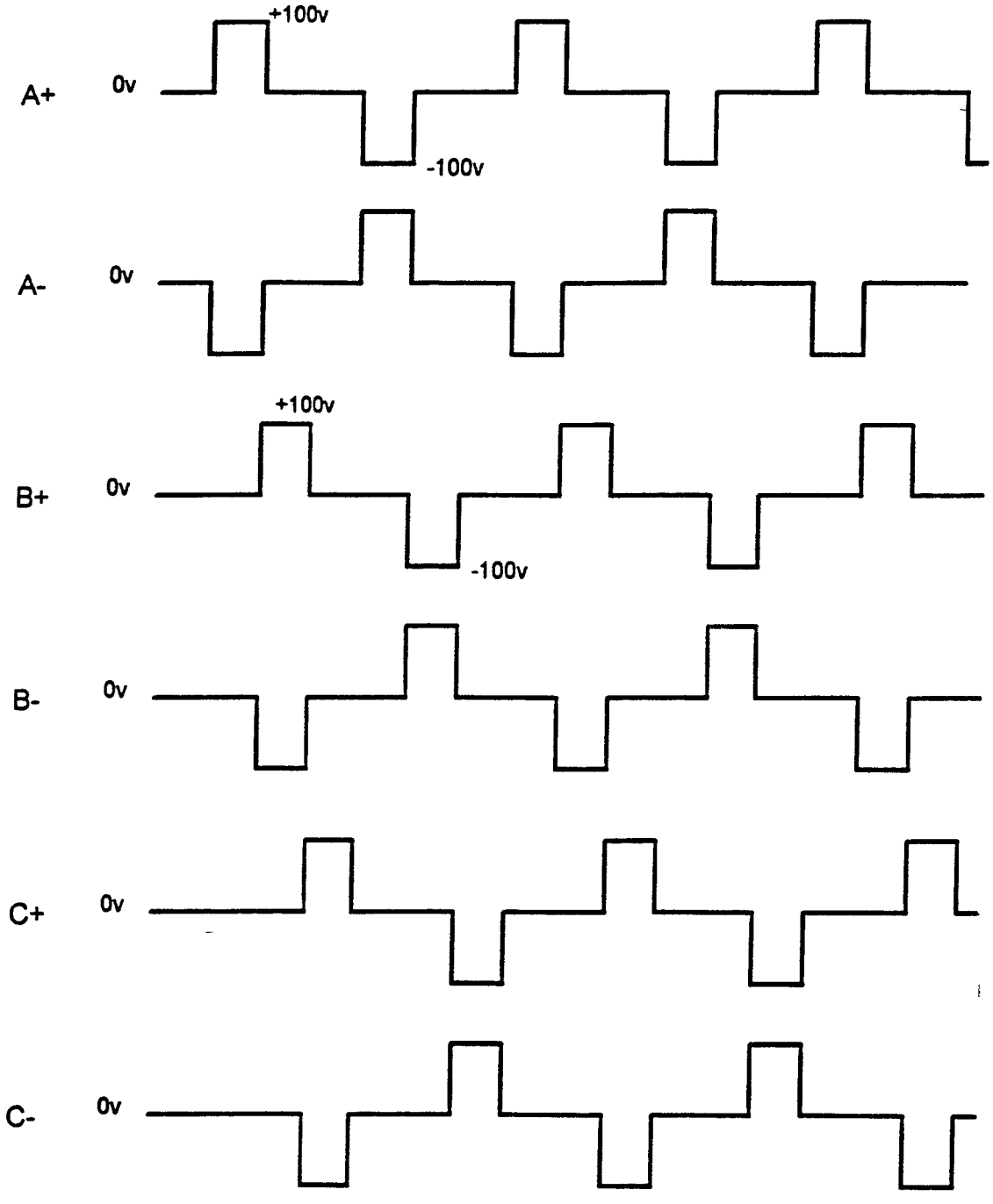


Figure 3.2(b) Six-phase bipolarized high-voltage square-wave pulses with symmetrical pairs (A+,A-), (B+,B-), (C+,C-)

3.2 Power Supply Design - Entire Circuit Structure:

The entire power supply circuit consists mainly of two portions, the digital circuit and the analog, bipolarized, high-voltage drivers circuit , as shown in Figure 3.3.

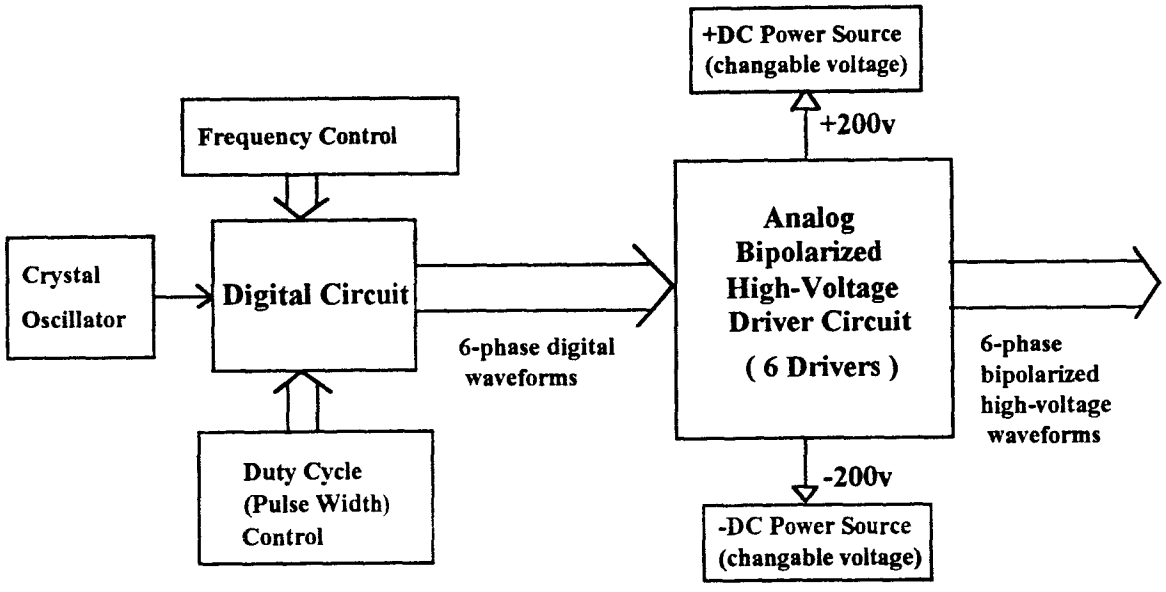


Figure 3.3 Entire Structure Diagram of Power Supply

The 6-phase digital square wave coming out from the digital circuit should have the waveform as shown in Figure 3.4 These six digital pulses feed into six analog, high-voltage drivers, as shown in Figure 3.5, to produce 6-phase bipolarized, high-voltage square-wave output in the following way: (A1, A2) → A+, (A2, A1) → A-, (B1, B2) → B+, (B2, B1) → B-, (C1, C2) → C+, (C2, C1) → C-.

It seems, from above, that only two digital inputs A1 and A2 are needed in order to generate a single bipolarized high-voltage pulse signal A+. This is true if we are not strict on the output waveform from the power supply and the operational frequency, and work with two digital inputs can be implemented by adding a proper-value resistor pulling to the ground in the driver circuit.

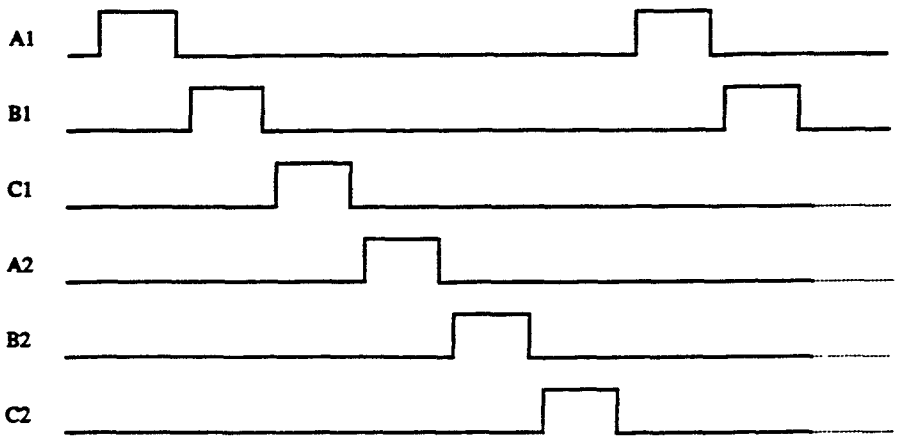


Figure 3.4 6-phase Digital Output Waveform from Digital Circuit

However, for much better waveform, two additional digital signals , named +Avin3 and +Avin4, are needed to achieve active pull-down and pull-up to the ground function. This will be understood well when we reach Chapter 5, which concerns the design of bipolarized high-voltage drivers with active pull-down and pull-up circuit. Here, we just show ideally the waveforms of +Avin3 and +Avin4 and modify the circuit structure diagram as shown in Figure 3.6. Also, we can see that -Avin3 and -Avin4 are needed together with A2 and A1 to generate A-, as shown in Figure 3.6. These additional signals can be produced from the digital circuit part of the power supply.

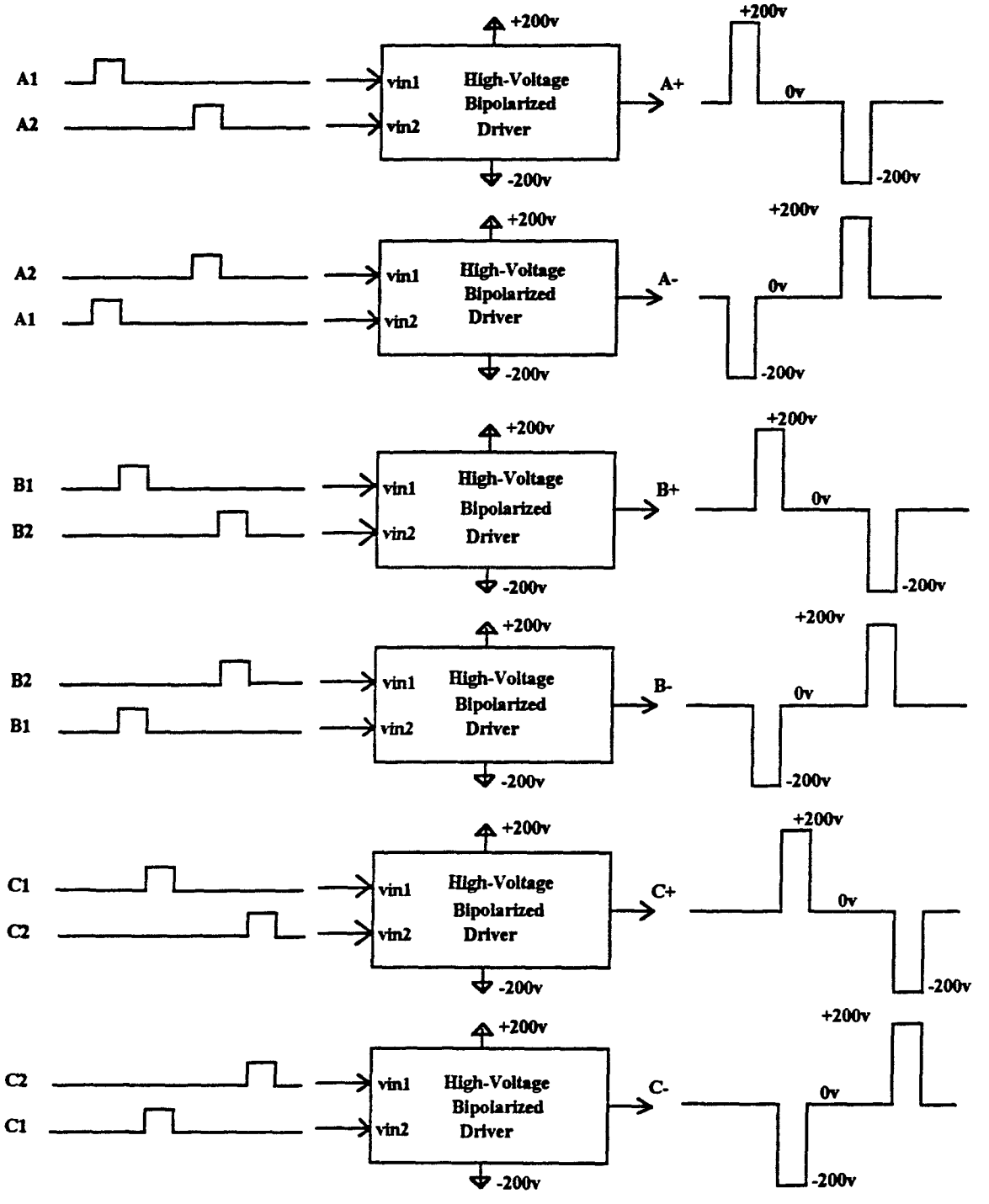


Figure 3.5 Functional diagram of 6-phase bipolarized high-voltage drivers with input and output signals.

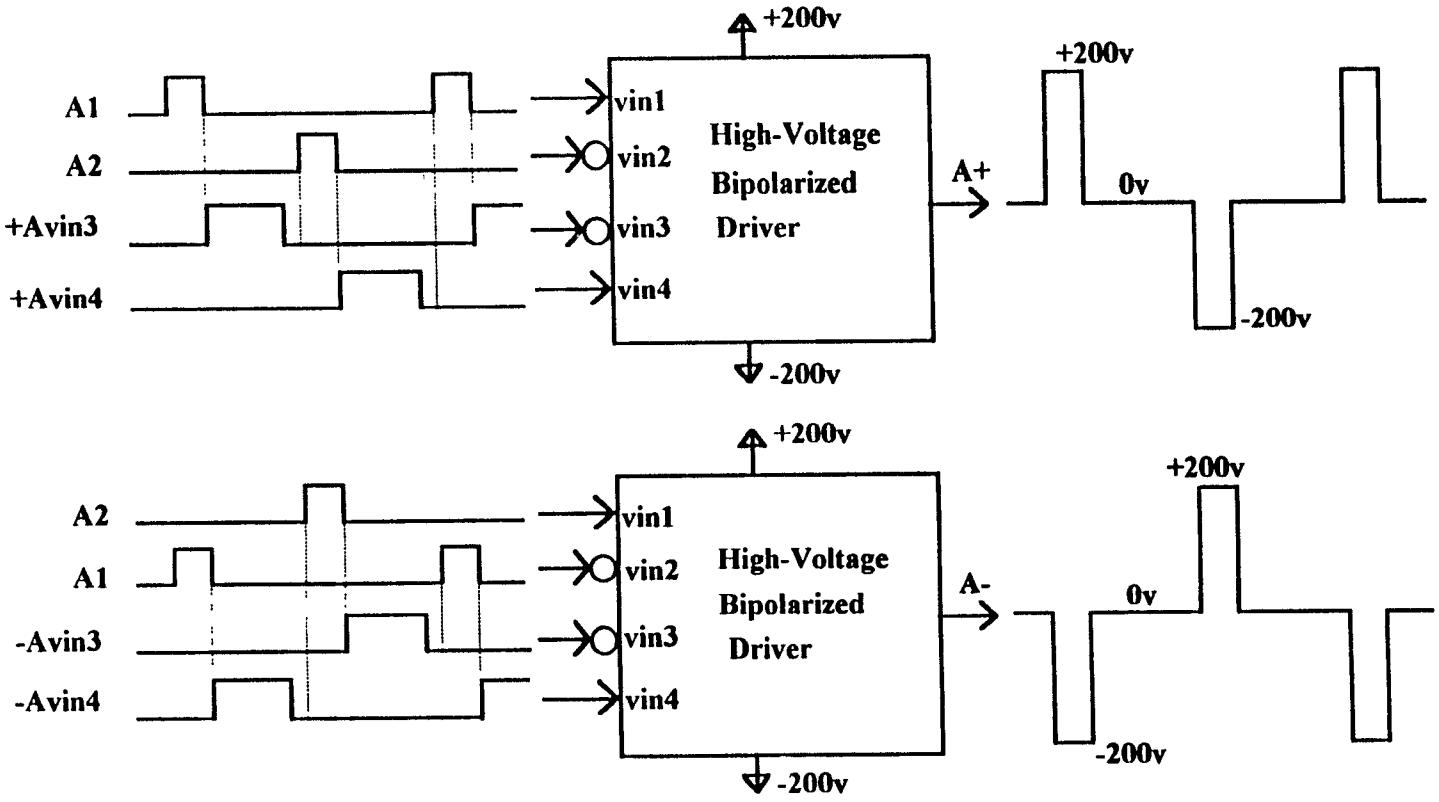


Figure 3.6 Function Diagram of Bipolarized High-voltage Drives with Additional Digital Inputs for Active Pull-down and Pull-up to Ground

CHAPTER 4
DIGITAL DESIGN

4.1 VLSI Design Methodology

The VLSI design methodology selected for this thesis requires tasks in the following sequence:

1. Chip function specification;
2. Chip architecture including circuit block diagram;
3. Detailed circuit schematic of each function block, obtained from true value table;
4. Digital simulation of the circuit of each block, and then of the entire circuit. Exercise as many states and nodes as possible. If the logic simulation shows unsatisfactory results, modify the circuit schematic design, accordingly;
5. Determine processing technology for this circuit, and then start physical layout of the circuit from its schematic design;
6. A design rule check is required. The circuit design methodology selected does not provide "correct-by-construction" synthesis. Create the MOSIS CIF-format database from the physical layout file.
7. Complete the formatting of test vectors from the functional simulation. These test vectors will be used for engineering acceptance of the IC chip.

The whole idea for the design of the digital part of the power supply comes from its specific requirements which have been stated in Chapter 2 and 3. The two major requirements of the 6-phase digital square-wave supply are that it be capable of generating variable frequency and generating variable duty cycle signals.

Figure 4.1(a) shows a function diagram of the circuit to generate a square-wave clock signal with a variable frequency control, and Figure 4.1(b) shows the generation and control of a 6-phase pulses output with variable duty cycle.

It is necessary to define duty cycle, non-overlapping, and overlapping more precisely. As illustrated in Figure 4 01, duty cycle = (t1/To)x100%. In Figure 4.01(a), percentage of non-overlapping = (t1/to)x100%; while in Figure 4 01(b), percentage of overlapping = (t2/t1)x100%. For six phases, the abutting pulse case (without time gaps) we define as (1/6)x100% duty cycle, or 100% non-overlapping. When the waveform pulses are programmable with time gaps the duty cycle is reduced to below 16 7%.

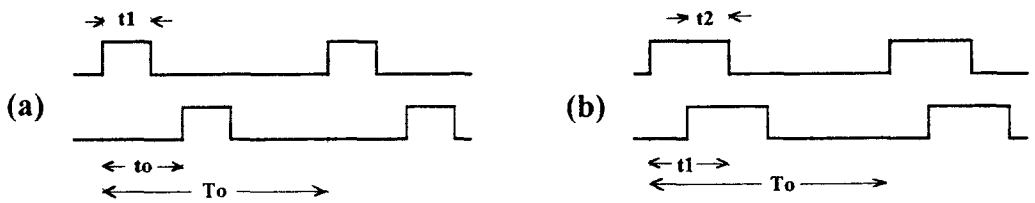


Figure 4.01 Definition of duty cycle, non-overlapping, and overlapping. (a) Non-overlapping case; (b) Overlapping case

As shown in Figure 4 2, the six-phase digital pulses with variable duty cycle and variable frequency come from the digital circuit, and will be fed into six bipolarized high-voltage drivers As mentioned in Chapter 3, for a much better waveform of a single bipolarized high-voltage square-wave signal A+, two additional signal, +Avin3 and +Avin4 are needed in addition to A1 and A2 to provide active pull-up and pull-down to ground. These four signal waveforms are shown in Figure 4.3.

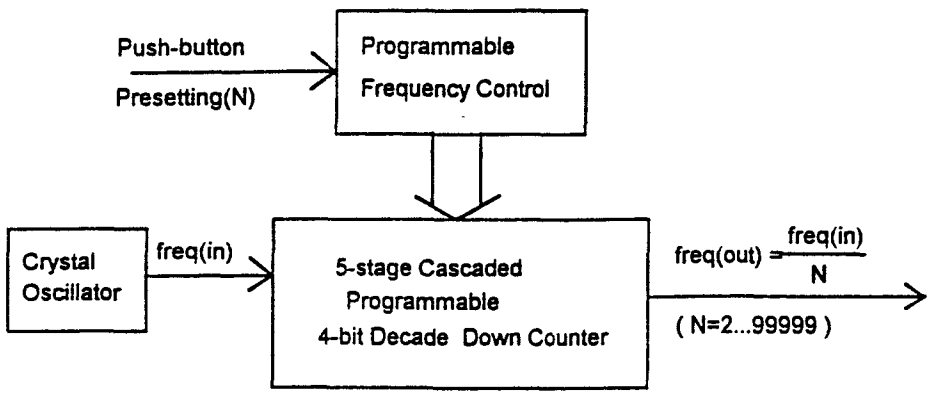


Figure 4.1(a) Generation of Square-wave Clock Signal with Variable Frequency Control.

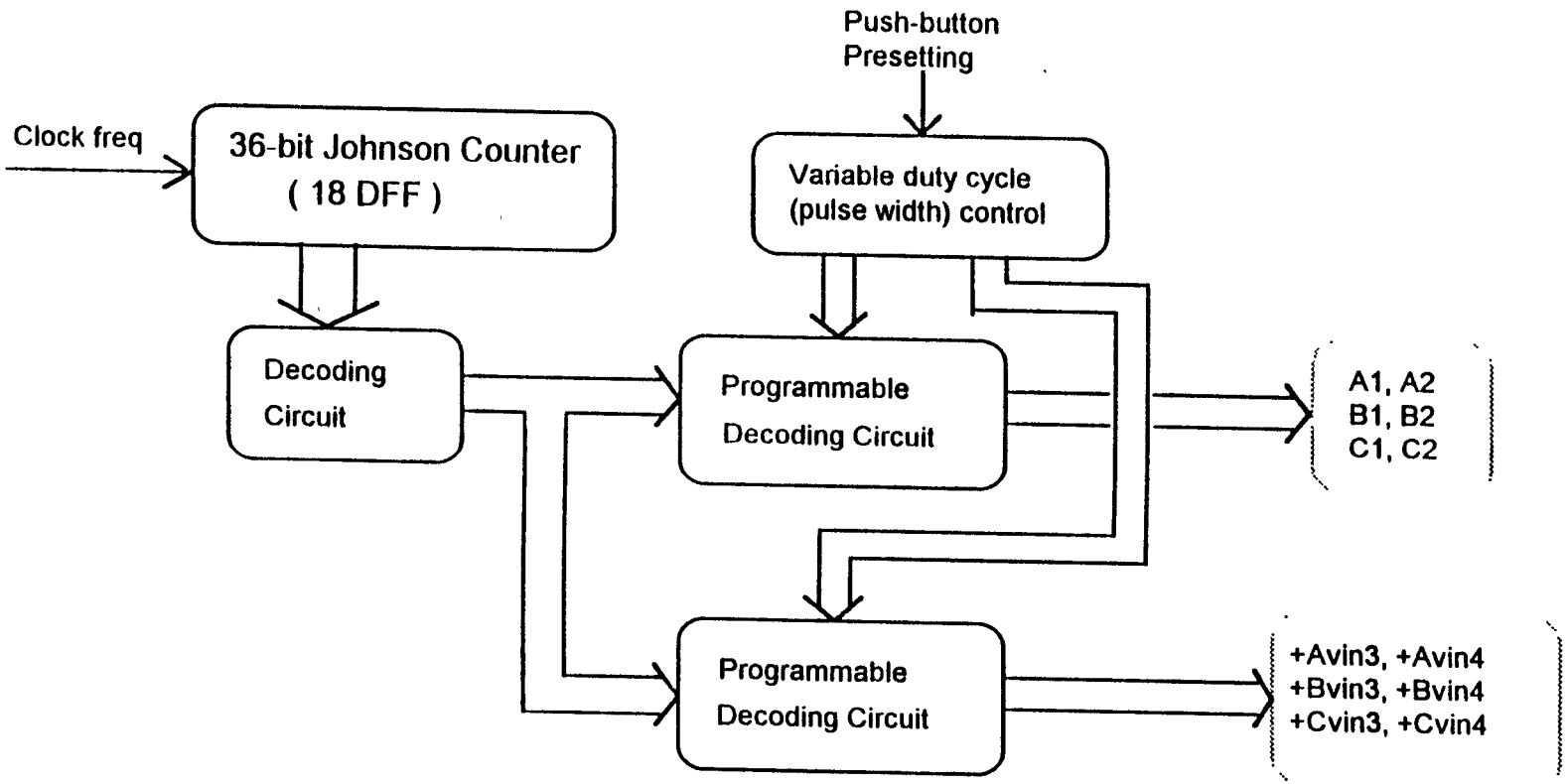


Figure 4.1(b) Generation and control of variable pulse duty cycle

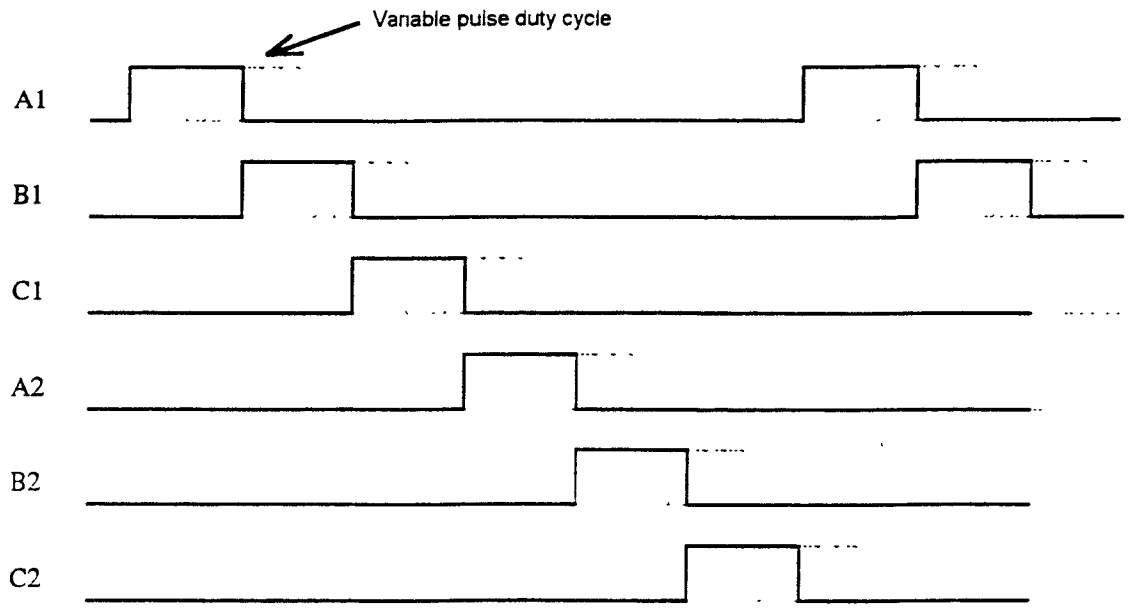


Figure 4.2 Six-phase digital pulse output from the digital circuit with variable duty cycle

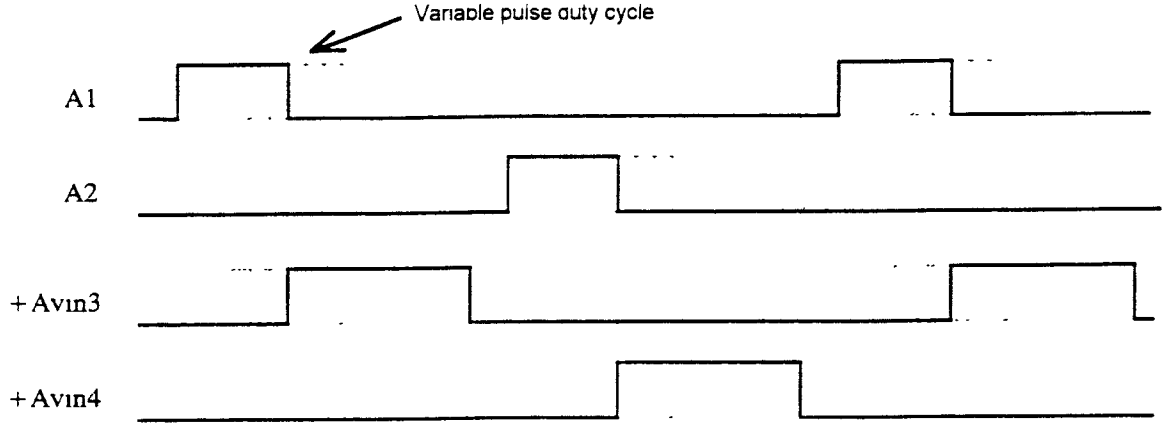


Figure 4.3 Four digital pulses to generate a single bipolarized high-voltage signal A+ with active pull-up/down to ground

4.2 Detail Circuit Schematic Design and Analysis

The entire digital circuit part of the power supply is functionally comprised of two major parts. One is a programmable frequency divider, made with cascaded 5-stage presettable 4-bit BCD down counters, dealing with adjusting the frequency used as a clock signal for the power supply. The other is a programmable variable-pulse-duty-cycle generating circuit, consisting of a 18-DFF Johnson counter with two presettable decoding circuits, dealing with changing the pulse duty cycle to produce either non-overlapping or overlapping pulses.

4.2.1 Programmable Divide-by-N Frequency Divider

As shown in Figure 4.4 , we construct the programmable frequency divider with 5 stage cascaded presettable 4-bit BCD down counters. Let us start with the design and analysis of a single presettable. cascadable 4-bit BCD down counter which is perfect for this frequency division application.

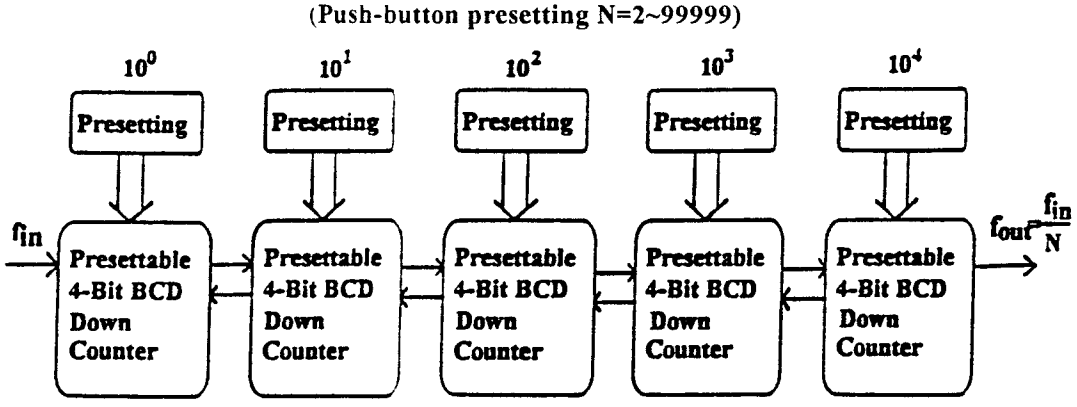


Figure 4.4 Function Diagram of Cascaded 5-stage Programmable Divide-by-N Frequency Divider. (N=2~99999 by push-button presetting.)

The synchronous down counter we have designed here consists of four "T" flip flops and a few gates, connected in an internally synchronous way for high internal and external speeds. Its logic design method is almost standard and straightforward,

except some special parts. Thus, we will give its function table in Table 4 1(a) (b) (c), and its logic diagram, as shown in Figure 4.5, and will analyze its operation in following paragraphs.

Table 4.1 (a) Function Table of the 4-bit BCD Down Counter

	Output			
Count	Q3	Q2	Q1	Q0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

Table 4.1(b) Function Table of the 4-bit BCD Down Counter

CF	Q3 - Q0	"0"
1 0	Not all 0	0 0
1 0	All 0	1 0

Table 4.1 (c) Function Table of the 4-bit BCD Down Counter

Inputs											
CLK	CT	PE	MR	P3	P2	P1	P0	Q3	Q2	Q1	Q0
x	x	x	1	x	x	x	x	0	0	0	0
x	x	1	0	P3	P2	P1	P0	P3	P2	P1	P0
↓	0	0	0	x	x	x	x	Down Counting			
↓	x	0	0	x	x	x	x	No Counting			
x	↓	0	0	x	x	x	x	No Counting			
1	↓	0	0	x	x	x	x	Down Counting			

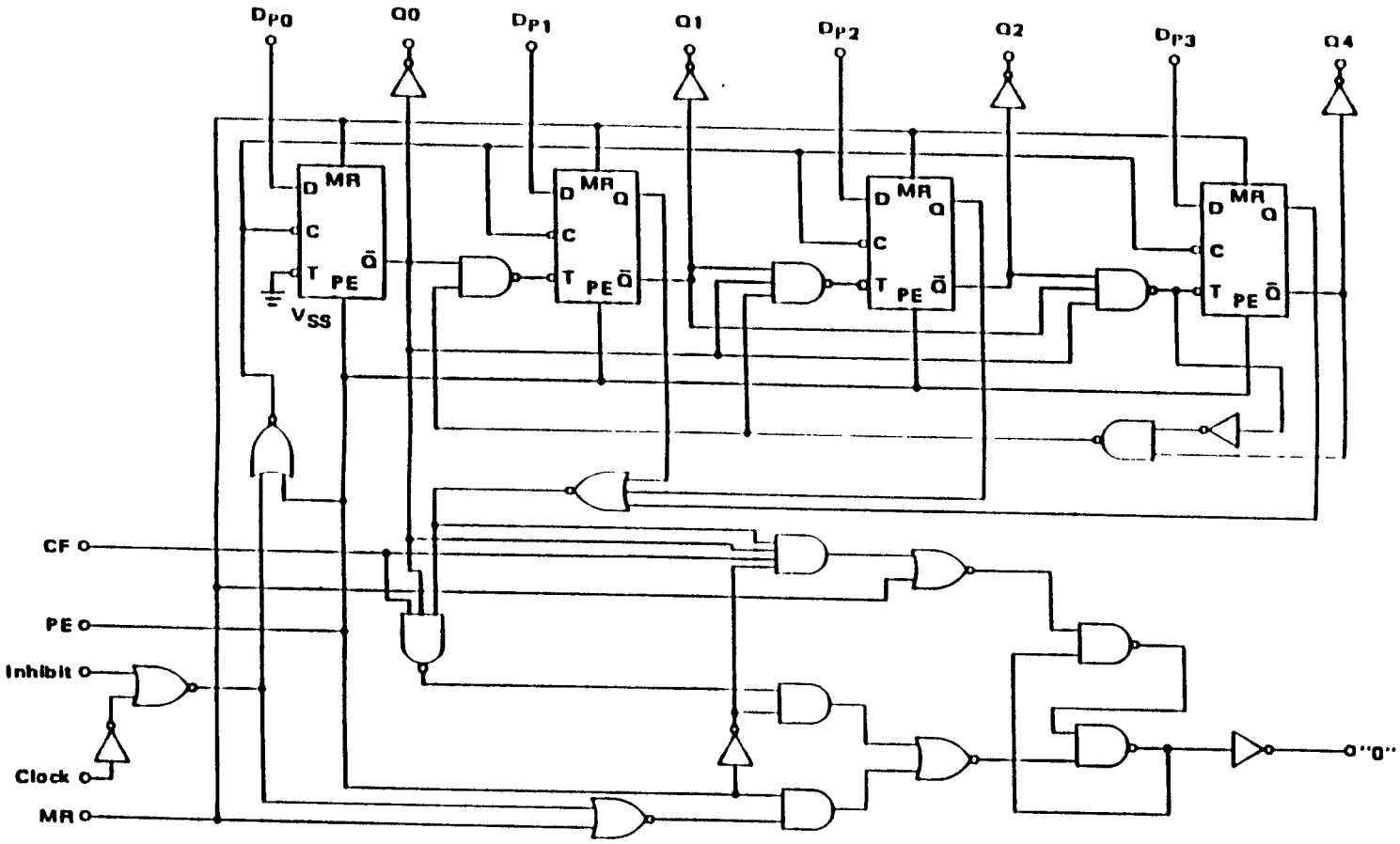


Figure 4.5 Logic Diagram of 4-bit BCD Divide-by-N Counter

Note that inside the BCD down counter, there are four special Parallel Load "T" Flip Flops which are designed exclusively for this counter They have following functions·

"D" - data in; "PE" - Preset Enable. when PE=1, Q = Data in;

"MR" - Master Reset: when MR=1, Q=0,

T=0. Q changes its previous state on every clock pulse, T=1: Q doesn't change its state

This Parallel Load "T"FF can be implemented by modifying a normal J-KFF with preset and clear, as shown in Figure 4.6.

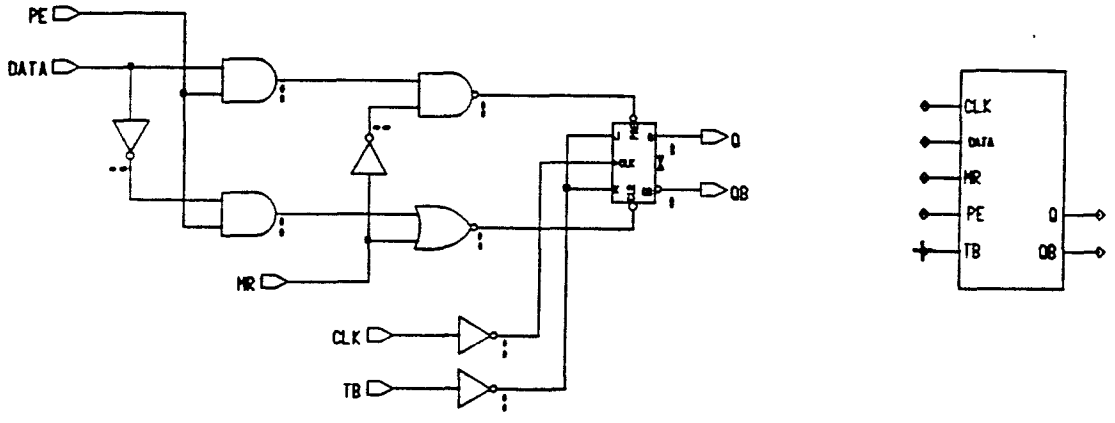


Figure 4.6 Parallel Load "T" Flip Flop implemented by a normal J-K FF

From Table 4.1(a) and Figure 4 5, we can see that the counter works as follows. For first "T"FF (Q1), T1=0 all the time, and Q1 changes its previous state on every clock pulse. Second "T"FF (Q2), T2 = 0 only when (Q1=0) AND (Q4=1 OR Q3=1 OR Q2=1 OR Q1=1). Third "T"FF (Q3), T3 = 0 only when (Q2=0) AND (Q1=0) AND (Q1 or Q2 or Q3 or Q4 = 1). Forth "T"FF (Q4), T4 =0 only when (Q3=0) AND (Q2=0) AND (Q1=0) For example, when all "0"s, Q4Q3Q2Q1="0000"; from above analysis, we know that Q1 and Q4 will change their previous states. Then the next state will be "1001".

The down counter is constructed internally with four parallel load "T" flip flops, and has four data inputs and five control inputs, CLK, CT (Inhibit), PE, MR (Reset),

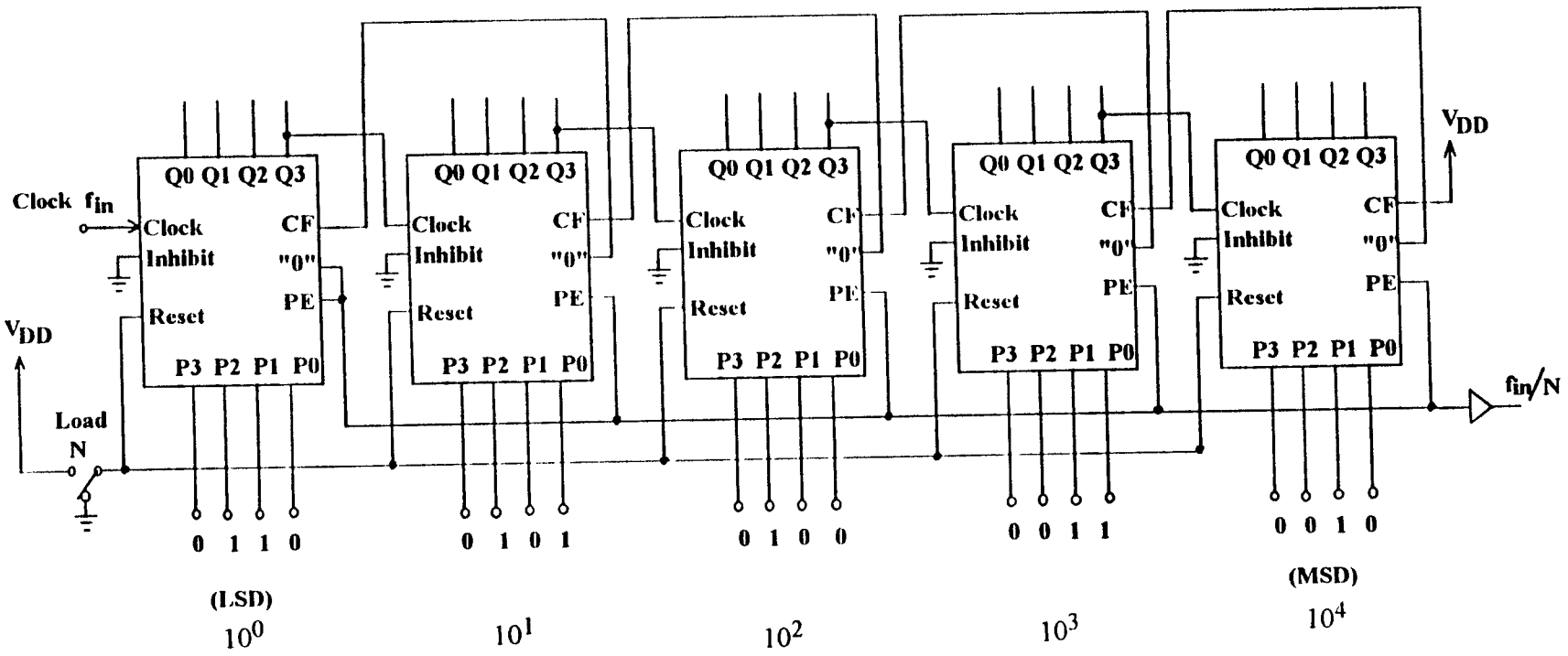


Figure 4.7 Programmable Divide-by-N Frequency Divider
Constructed by Cascaded 5 stage the Presettable 4-bit Down Counters.

CF (Cascade Feedback), and an output "0". CLK and Inhibit are rising-edge triggered and falling-edge triggered, respectively, meaning that the FF function is incremented on positive transition of Clock or negative transition of Clock Inhibit. When input clock signal comes into one of these inputs, the other acts as a control. For example, if the input clock comes into CLK, it will count down only when Inhibit =0, and will not count when Inhibit=1. PE is preset enable control; the counter can be preset when PE=1, and the clock signal is not functioning at that moment.

CF (Cascade Feedback) is the working mode control. The circuit has a logic function of a divide-by-N counter when CF=1, and only performs 2-10 down counting when CF=0 MR (Master Reset) resets all "T" flip flops to 0 when it is "1". Output "0" is an indication of an all 0 situation while the circuit is working as a 1/N counter; that means that if the circuit works as a 1/N counter, "0" outputs 1 when Q3 - Q0 all=0, indicating a loop cycle ends If CF=0, the circuit operates only as a down counter, and then "0" outputs 0 all the time

Now that we have understood how the presettable BCD down counter works, we can implement frequency-divide counting of 1~ (10^m-1) by cascading m stages of this BCD down counter. Let us take a look at a 5-stage cascaded case, as shown in Fig. 4 6, which is exactly the circuit we have designed for our power supply, and which will achieve frequency dividing of N=1~99999. Let's take an example, say, N=23456.

First of all, the value of N=23456 is preset to the data outputs of each down counter. The counter for MSD (Most Significant Digit, 10^4 digit) is preset to 2, namely P3P2P1P0=0010; and then the counter for 10^3 digit to 3, namely P3P2P1P0=0011; and the counter for 10^2 digit to 4, namely P3P2P1P0=0100; and 10^1 digit to 5, namely P3P2P1P0=0101; and the counter for LSD (Least Significant Digit, 10^0 digit) to 6, namely P3P2P1P0=0110.

At the beginning, MR is set to V_{DD} to clear all the counters to zero. At this moment, "0" output of LSD sends out a high level signal ("1") to PE (Preset Enable), to

let the data transmit to the outputs, that means that now the outputs of each stage of counters are 23456

Then, MR goes back to ground and stays there, and the counting pulse starts to be fed in. At this moment, CF of MSD is 1, performing the function of divide-by-N counting. And other digits counters are all in the state of CF=0, so they all perform normal down counting After 10 clock pulses have been input, Q3 of LSD sends out a pulse to the counter for 10^1 digit as its clock input. After 100 clock pulses have been input, Q3 of the 10^1 digit counter sends out a pulse to the 10^2 digit counter as its clock signal. .... After 10000 clock pulses have been input, Q3 of 10^3 digit counter sends out a pulse to MSD (10^4 digit) counter as its clock input

Therefore , when 20000 clock pulses have been input, MSD counter counts down to zero. And its "0" pin outputs "1", to make CF of 10^3 digit counter be "1", and to switch it to divide-by-N counting mode When 3000 more clock pulses have been input consecutively, the counter for 10^3 digit counts down to zero And its "0" pin sends out an "1", to make CF of the 10^2 digit counter be "1", and to switch it to divide-by-N counting mode . . Finally, after 6 more clock signal pulses have been consecutively input, LSD counter is also restored to 0. and its "0" pin sends out a "1" to set the PEs of all counters to be "1" Thus, once again. the presetting number 23456 is being set into each counter, and another counting loop starts. In this way, the cascaded circuit is operating as a programmable divide-by-N frequency divider.

Presetting Circuit for Programmable Frequency Divider:

To preset the programmable frequency divider, we need a simple 4-bit BCD up counter with reset as its presetting circuit for each (4 bits) of all five digits, as shown in Figure 4 8. .This presetting circuit is under manual control with push-buttom input

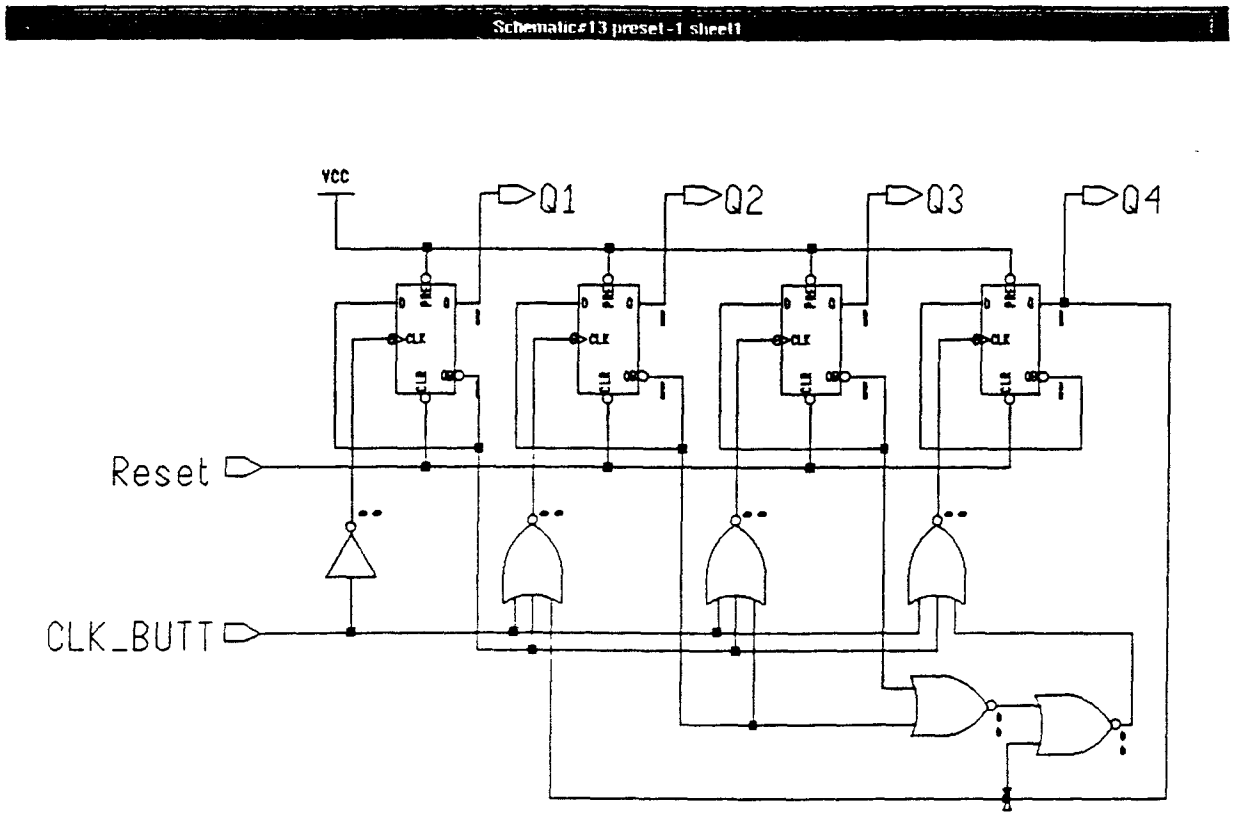


Figure 4.8 BCD up counter - Presetting circuit for the programmable frequency divider. This is only for one digit.

4.2.2 Programmable Variable-duty-cycle Generating Circuit

1. 18DFF (36-bit) Johnson Counter and its decoding circuit:

The Johnson Counter we have used in our circuit is composed of 18 DFF structured as shown in Figure 4.10, which have 18 ouputs, Q1, Q2, Q3..., Q18.

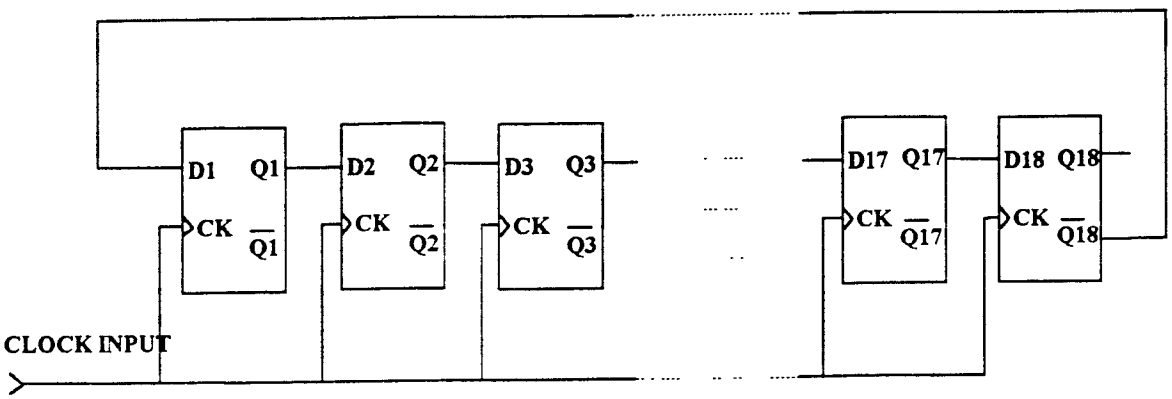


Figure 4.10 18 DFF Johnson Counter Structure

The counter can provide 36 states, which are s1, s2, . , s36, by its decoding circuit, as shown in Table 4 2 and 4 3 Obtained from observation of Table 4 2 and 4 3, this special and simple decoder consists of only NAND2 gates or NOR2 gates for generating each of all 36 states, as follows.

$$\overline{s1} = \overline{(\overline{Q18} \cdot \overline{Q1})}\,, \quad \overline{s2} = \overline{(Q1 \cdot \overline{Q2})}\,, \quad \overline{s3} = \overline{(Q2 \cdot \overline{Q3})}\,, \quad \ldots\ldots, \quad \overline{s18} = \overline{(Q17 \cdot \overline{Q18})}\,,$$

$$\overline{s19} = \overline{(Q18 \cdot Q1)}\,, \quad \overline{s20} = \overline{(\overline{Q1} \cdot Q2)}\,, \quad \overline{s21} = \overline{(\overline{Q2} \cdot Q3)}\,, \quad \ldots\ldots, \quad \overline{s36} = \overline{(\overline{Q17} \cdot Q18)}$$

This is very different from the decoder of other counters, like binary or BCD counters. Shown in Figure 4 11 is the circuit diagram of 18-DFF (36-bit) Johnson Counter with its decoder (on page 42).

Table 4.2 Function Table of a 18 DFF's Johnson Counter

Clock	Q1	Q2	Q3	.. ..	Q16	Q17	Q18
1	0	0	0	.....	0	0	0
2	1	0	0	.....	0	0	0
3	1	1	0	.. ..	0	0	0
..	...	...	..	... .	.		
...	...	...	...	.....	..	...	...
. .	..	...		....	...	.	.
19	1	1	1	....	1	1	1
20	0	1	1	.....	1	1	1
21	0	0	1	... ...	1	1	1
	..	.		.....	...		. .
. .	.	...		..... .	...	..	..
.	..	...		.....	..	.	.
35	0	0	0	. . .. . .	0	1	1
36	0	0	0	..... .	0	0	1

Table 4.3 Function Table of 36-bit output
from a 18 DFF's Johnson Counter with its decoder

Clock	s1	s2	s3	s4	. . ..	s34	s35	s36
1	1	0	0	0	. . ..	0	0	0
2	0	1	0	0	....	0	0	0
3	0	0	1	0	.....	0	0	0
4	0	0	0	1	. ... .	0	0	0
...	...	...	.	. .	.....	..	.	..
...	...	...	. .	..	.....	..	..	..
...	..	. .	.	..	..... .	.	.	. .
34	0	0	0	0	....	1	0	0
35	0	0		0	. ...	0	1	0
36	0	0		0	... .	0	0	1

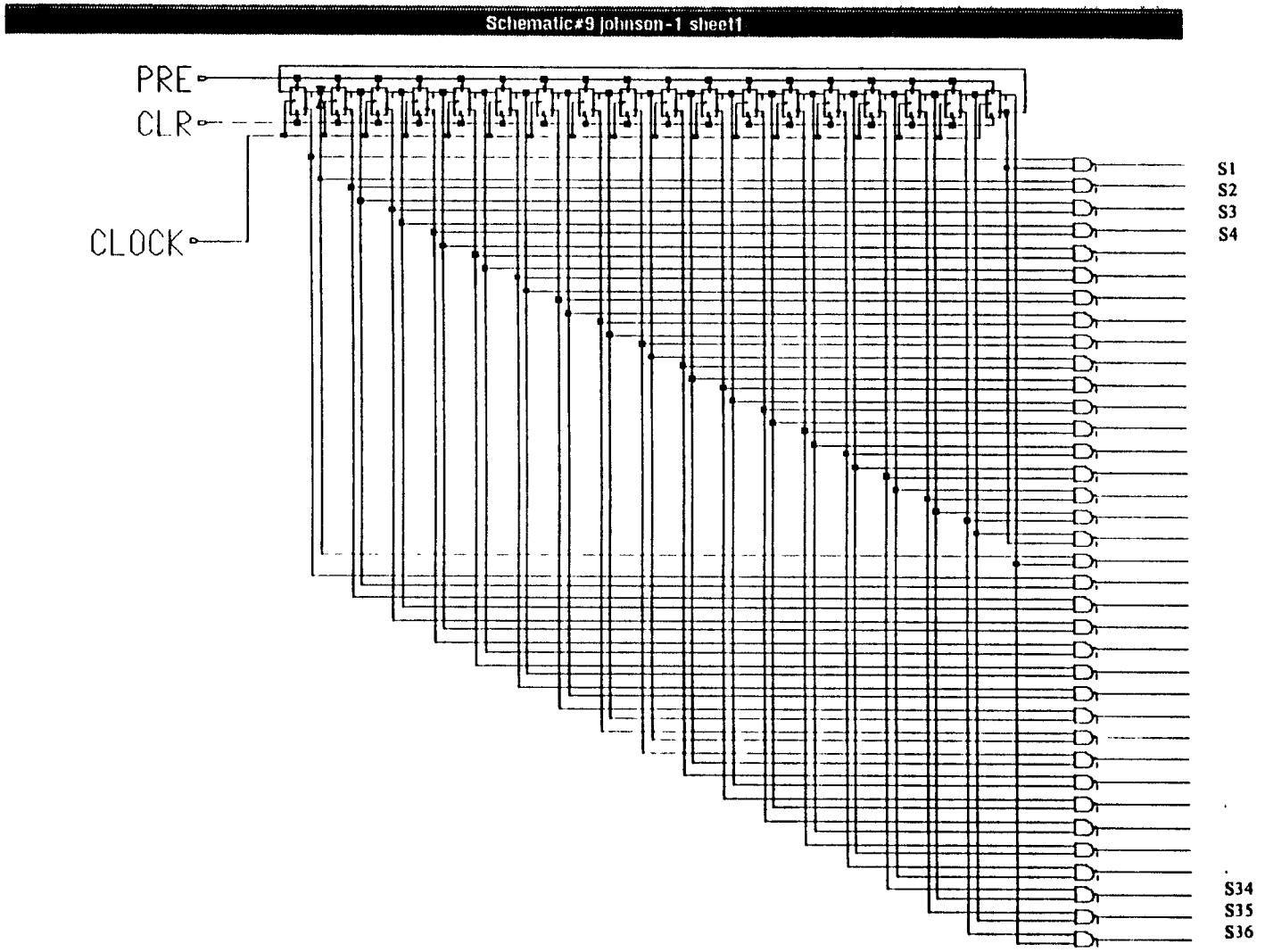


Figure 4.11 Circuit diagram of 18-DFF(36-bit) Johnson Counter with its decoder

2. *Decoding Circuit of variable-duty-cycle control:*

According to the waveforms in Figure 4 2 and 4 3, six control presetting signals, ct1, ct2, ct3, ct4, ct5, ct6, are needed to produce all the variable duty cycle pulses, providing from one-half non-overlapping to one-third overlapping. When control ="000000", it is 50% non-overlapping; when control = "100000", it is 66.7% non-overlapping; when control = "110000", it is 83.3% non-overlapping, when control = "111000", it is 100% non-overlapping; when control = "111100", it is 16.7% overlapping; when control = "111110", it is 25% overlapping; when control = "111111", it is 33.3% overlapping.

The logic expressions of all the signals under the control of six presetting inputs are as follows.

$$A1 = \overline{(s1+s2+s3)\cdot\left(\left(\overline{ct1+s4}\right)+\left(\overline{ct2+s5}\right)+\left(\overline{ct3+s6}\right)\right)\cdot\left(\left(\overline{ct4+s7}\right)+\left(\overline{ct5+s8}\right)+\left(\overline{ct6+s9}\right)\right)}$$

$$B1 = \overline{(s7+s8+s9)\cdot\left(\left(\overline{ct1+s10}\right)+\left(\overline{ct2+s11}\right)+\left(\overline{ct3+s12}\right)\right)\cdot\left(\left(\overline{ct4+s13}\right)+\left(\overline{ct5+s14}\right)+\left(\overline{ct6+s15}\right)\right)}$$

$$C1 = \overline{(s13+s14+s15)\cdot\left(\left(\overline{ct1+s16}\right)+\left(\overline{ct2+s17}\right)+\left(\overline{ct3+s18}\right)\right)\cdot\left(\left(\overline{ct4+s19}\right)+\left(\overline{ct5+s20}\right)+\left(\overline{ct6+s21}\right)\right)}$$

$$A2 = \overline{(s19+s20+s21)\cdot\left(\left(\overline{ct1+s22}\right)+\left(\overline{ct2+s23}\right)+\left(\overline{ct3+s24}\right)\right)\cdot\left(\left(\overline{ct4+s25}\right)+\left(\overline{ct5+s26}\right)+\left(\overline{ct6+s27}\right)\right)}$$

$$B2 = \overline{(s25+s26+s27)\cdot\left(\left(\overline{ct1+s28}\right)+\left(\overline{ct2+s29}\right)+\left(\overline{ct3+s30}\right)\right)\cdot\left(\left(\overline{ct4+s31}\right)+\left(\overline{ct5+s32}\right)+\left(\overline{ct6+s33}\right)\right)}$$

$$C2 = \overline{(s31+s32+s33)\cdot\left(\left(\overline{ct1+s34}\right)+\left(\overline{ct2+s35}\right)+\left(\overline{ct3+s36}\right)\right)\cdot\left(\left(\overline{ct4+s1}\right)+\left(\overline{ct5+s2}\right)+\left(\overline{ct6+s3}\right)\right)}$$

The decoding circuit diagram for these six digital signals is shown in Figure 4 12. The additional digital signal for active pull-up and pull-down to ground are also controlled, as follows, by the six presetting signals to generate proper pulse width Shown in Figure 4.13 is the circuit diagram for the above signals.

$$+Avm3 = \overline{(ct1+\overline{s4}+ct2+\overline{s5}+ct3+\overline{s6})\cdot(ct4+\overline{s7}+ct5+\overline{s8}+ct6+\overline{s9})}\ \overline{(s10+s11+s12)\cdot(s13+s14+s15)}$$

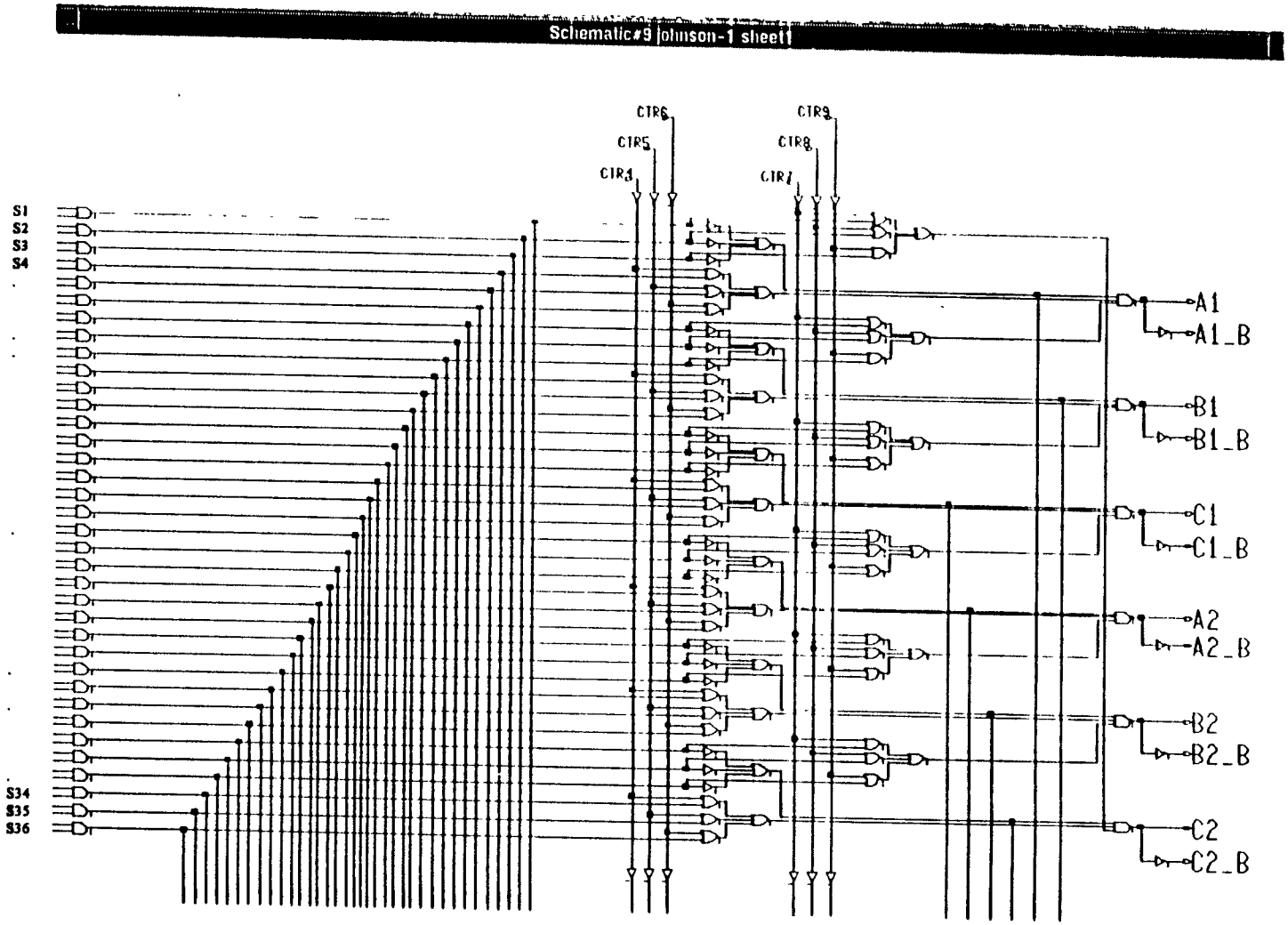


Figure 4.12 Decoding Circuit of A1, B1, C1, A2, B2, C2 with variable-duty-cycle control

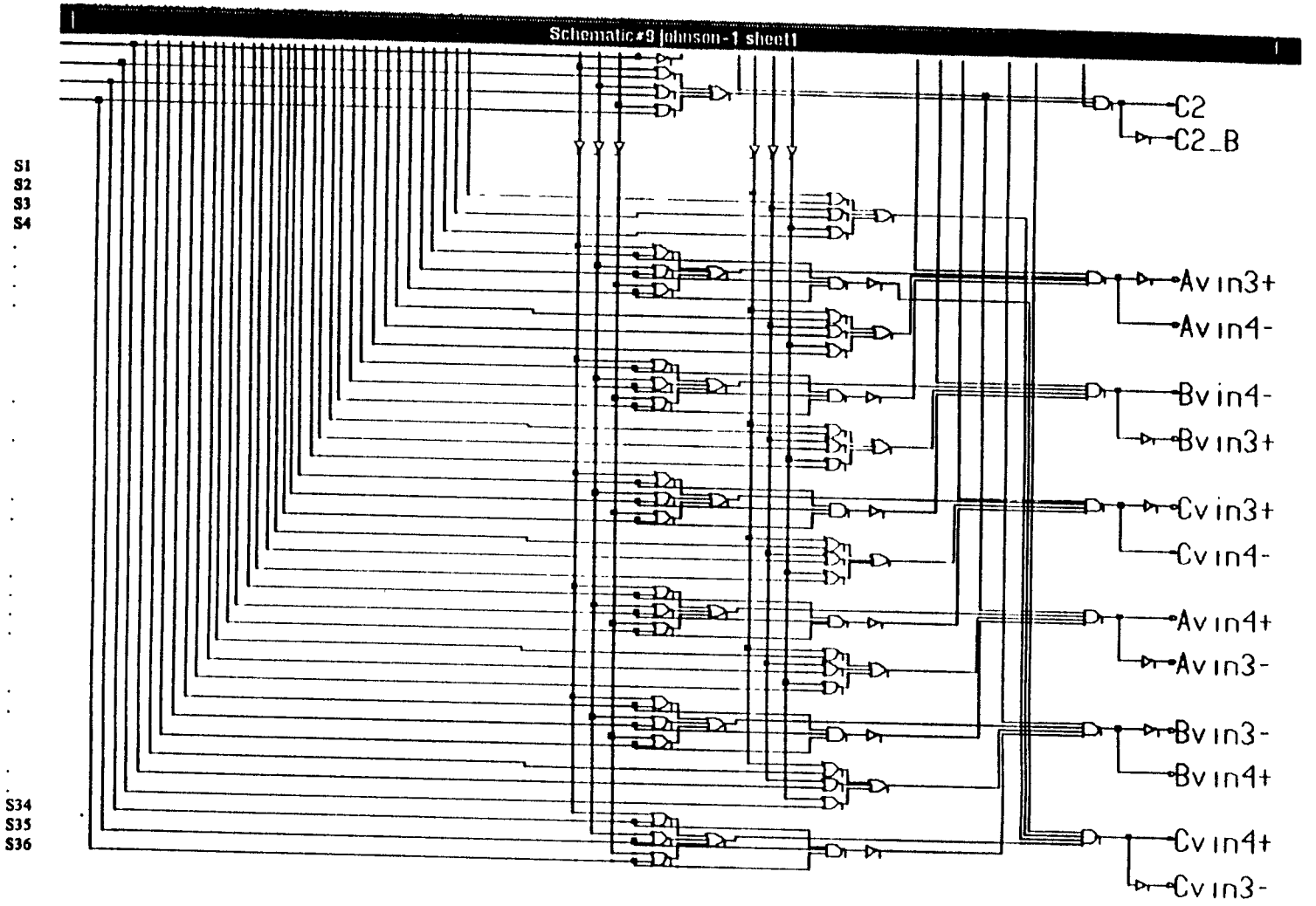


Figure 4.13 Decoding Circuit of the additional digital signals for active pull-up/down to ground

$$\overline{+Avin\,4} = \overline{(ct1 + s22 + ct2 + s23 + ct3 + s24)} \cdot \overline{(ct4 + s25 + ct5 + s26 + ct6 + s27)} \cdot \overline{(s28 + s29 + s30)} \cdot \overline{(s31 + s32 + s33)}$$

$$+Bvin\,3 = \overline{(ct1 + s10 + ct2 + s11 + ct3 + s12)}\ \overline{(ct4 + s13 + ct5 + s14 + ct6 + s15)}\ \overline{(s16 + s17 + s18)} \cdot \overline{(s19 + s20 + s21)}$$

$$\overline{+Bvin\,4} = \overline{(ct1 + s28 + ct2 + s29 + ct3 + s30)} \cdot \overline{(ct4 + s31 + ct5 + s32 + ct6 + s33)} \cdot \overline{(s34 + s35 + s36)} \cdot \overline{(s1 + s2 + s3)}$$

$$+Cvin\,3 = \overline{(ct1 + s16 + ct2 + s17 + ct3 + s18)} \cdot \overline{(ct4 + s19 + ct5 + s20 + ct6 + s21)}\ \overline{(s22 + s23 + s24)} \cdot \overline{(s25 + s26 + s27)}$$

$$\overline{+Cvin\,4} = \overline{(ct1 + s34 + ct2 + s35 + ct3 + s36)} \cdot \overline{(ct4 + s1 + ct5 + s2 + ct6 + s3)} \cdot \overline{(s4 + s5 + s6)} \cdot \overline{(s7 + s8 + s9)}$$

$$\overline{-Avin\,3} = +Avin\,4$$

$$-Avin\,4 = \overline{+Avin\,3}$$

$$\overline{-Bvin\,3} = +Bvin\,4$$

$$-Bvin\,4 = \overline{+Bvin\,3}$$

$$\overline{-Cvin\,3} = +Cvin\,4$$

$$-Cvin\,4 = \overline{+Cvin\,3}$$

Presetting Circuit for Programmable Duty-cycle Control:

This presetting circuit has 7 states, as shown in Table 4.4 It is implemented by a modified Johnson counter, as shown in Figure 4.14 , under the manual control of the push-buttom input (pulse).

Table 4.4 State table of the presetting circuit for programmable duty-cycle control

Input pulse	ct1	ct2	ct3	ct4	ct5	ct6
(All clear)	0	0	0	0	0	0
1	1	0	0	0	0	0
2	1	1	0	0	0	0
3	1	1	1	0	0	0
4	1	1	1	1	0	0
5	1	1	1	1	1	0
6	1	1	1	1	1	1

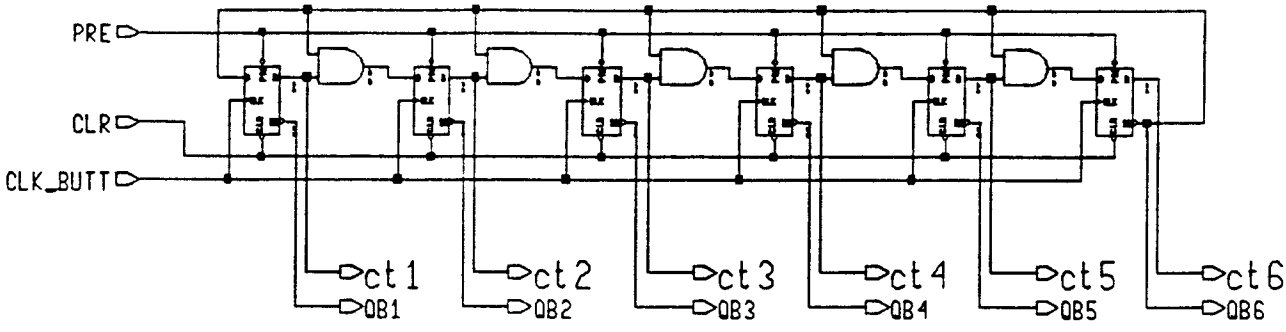


Figure 4.14 Presetting circuit for programmable duty-cycle control

4.3 Logic Simulation

The logic simulation is performed using Mentor Graphics' VLSI Design Tools. First of all, the circuit schematic is captured Design Architecture. QuickSim II is used to perform the actual simulation.

1. Simulation of the Presettable 4-bit BCD Divide-by-N Counter

Figure 4.16(a) shows the schematic capture and symbol of the special Parallel Load "T" FF made by normal JK FF. Figure 4 16(b) shows its simulation results including its input and output waveforms.

Figure 4.17 shows the schematic capture and symbol of the presettable 4-bit BCD down counter we have designed Figure 4 18 shows its logic simulation result, its input and output waveforms, from QuickSim II.

2. Simulation of Programmable Frequency Divider

The divide-by-N frequency divider is constructed by cascaded 5-stage presettable BCD down counters Its schematic capture is shown in Figure 4 19, in which the symbol of the 4-bit counter is used instead of its real circuit. Figure 4 20 shows its simulation results Because it is not practical to simulate a large value of N , we have selected several different values of N with relatively small magnitude, as shown in Figure 4 20(a) N=5, (b) N=13, (c) N=2, (d) N=44 for simulation

3. Simulation of 36-bit Johnson Counter with Decoding Circuits for Variable Duty-cycle Control

Figure 4 21 is the schematic capture of 36-bit Johnson Counter with decoding circuits for variable duty-cycle control Figure 4 22 shows simulation results for different, variable duty-cycle control. Figure 4 22(a) presents the case of "ct1ct2ct3ct4ct5ct6" = "000000" Figure 4 22(b) presents the case of "ct1ct2ct3ct4ct5ct6" = "100000". Figure 4 22(c) presents the case of "ct1ct2ct3ct4ct5ct6" = "110000" Figure 4 22(d) presents the case of "ct1ct2ct3ct4ct5ct6" = "111000" Figure 4 22(e) presents the case of "ct1ct2ct3ct4ct5ct6" = "111100" Figure 4 22(f) presents the case of "ct1ct2ct3ct4ct5ct6" = "111111"

4. Simulation of Presetting Circuits for Frequency Divider and Variable Duty-cycle Control

Figure 4 23 shows the simulation result of presetting circuit, a BCD up counter, for each digit of the programmable frequency divider. Figure 4 24 shows the simulation result of presetting circuit for variable duty-cycle control.

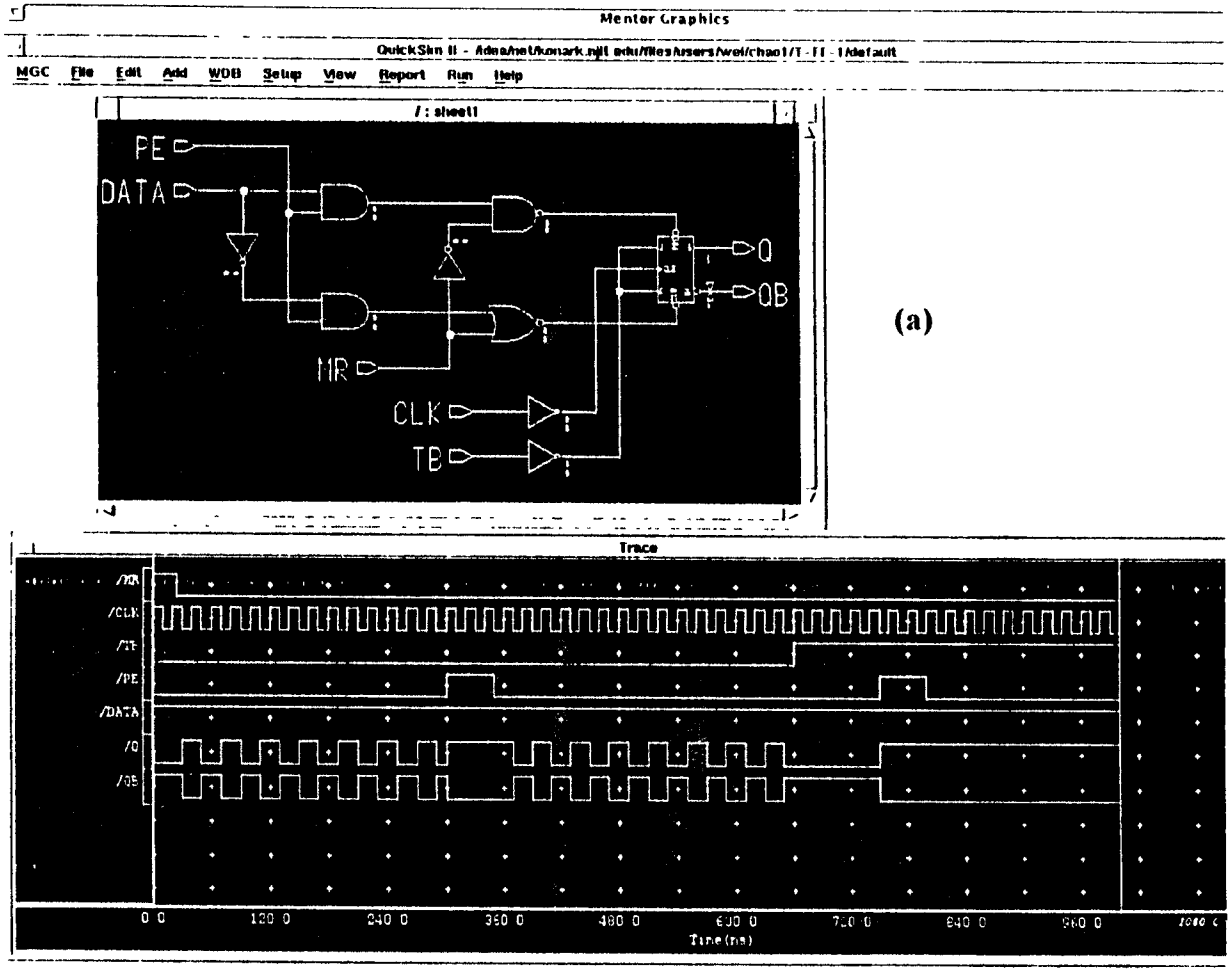
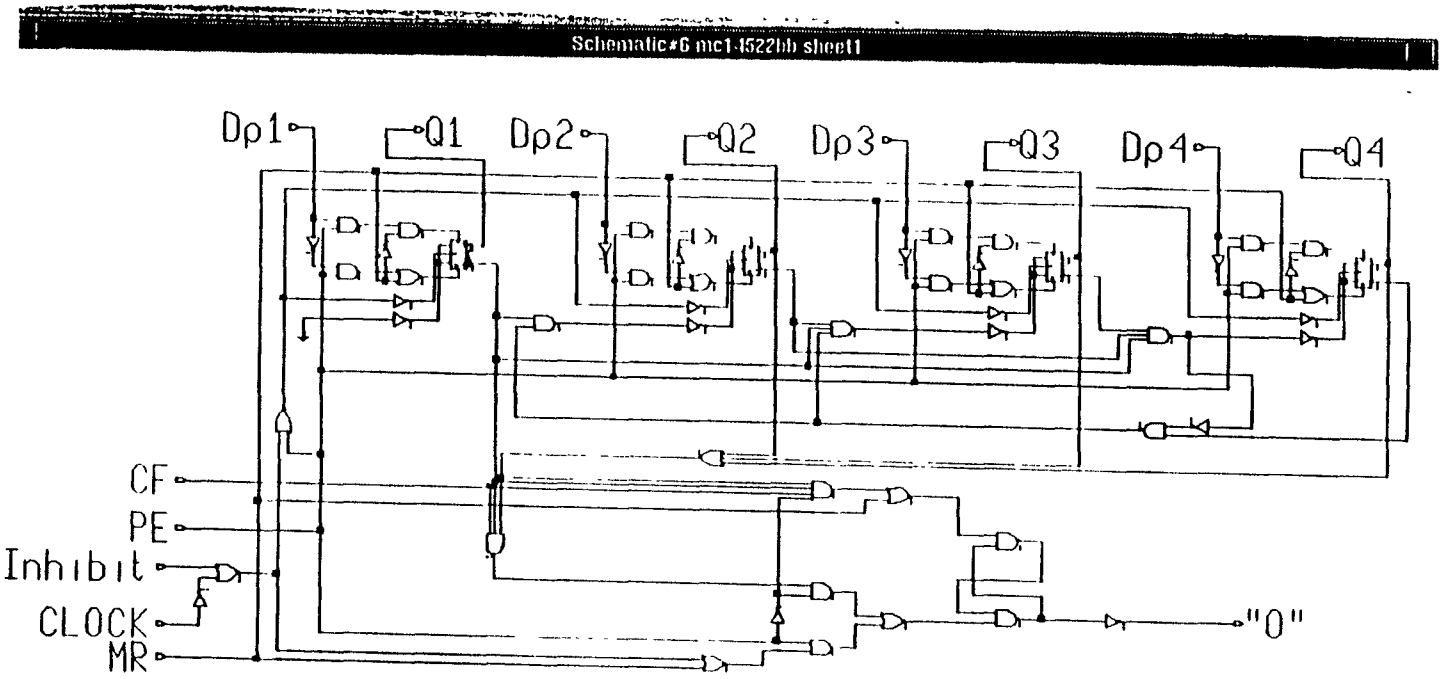


Figure 4.16 **(a)** The schematic capture of the special parallel load "T"FF
(b) Its simulation result including inputs and output waveforms



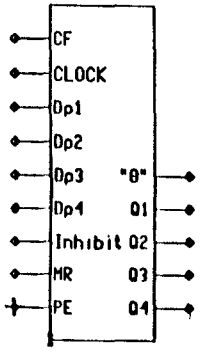


Figure 4.17 The schematic capture of the presettable 4-bit BCD down counter/frequency divider

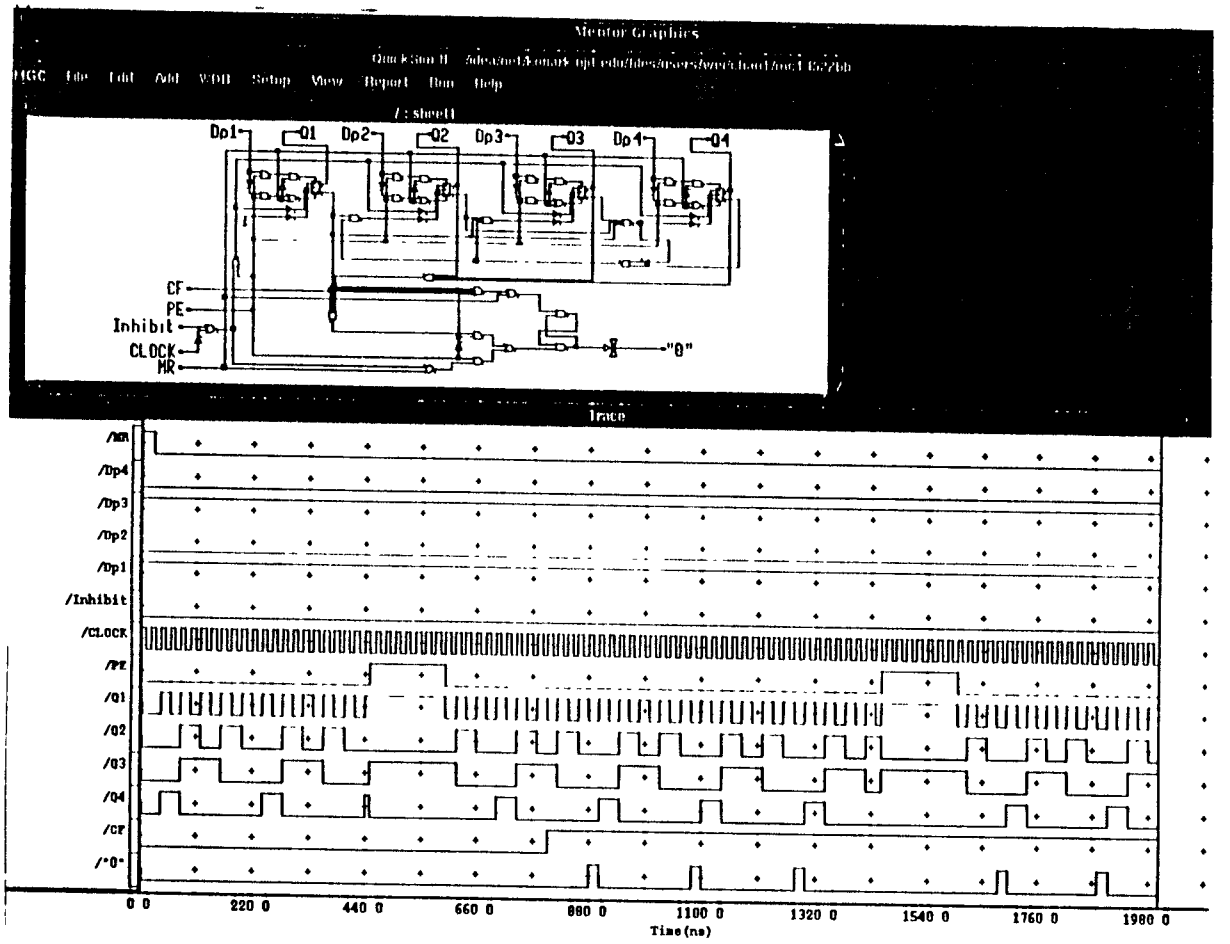
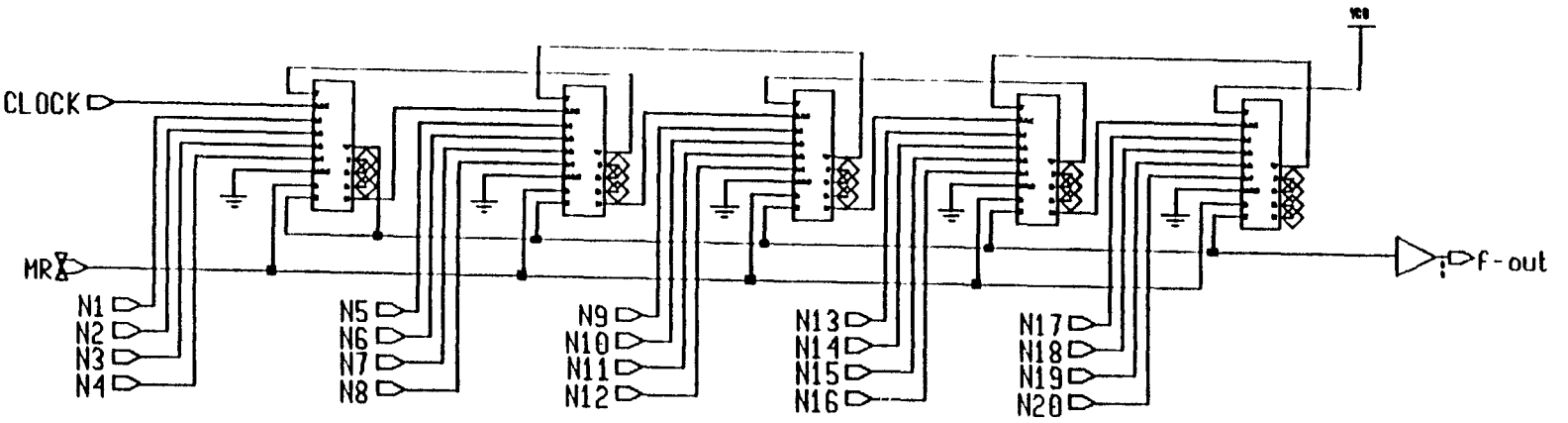


Figure 4.18 The logic simulation result of the presettable 4-bit BCD down counter/frequency divider in Figure 4 17



(a)

(b)

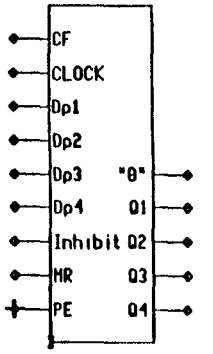


Figure 4.19 **(a)** The schematic capture of the programmable divider-by-N frequency divider and **(b)** The symbol of one-stage presettable BCD down counter.

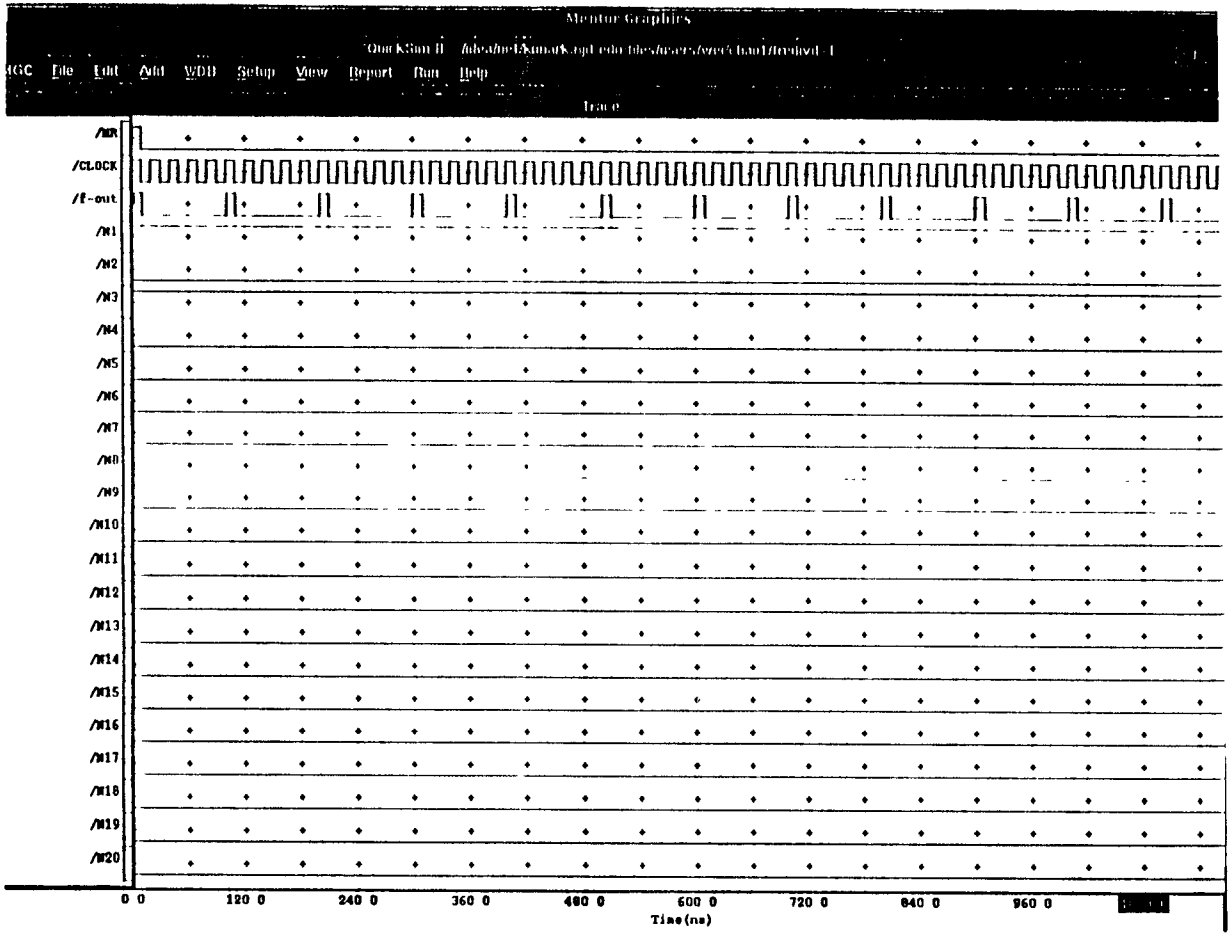


Figure 4.20 (a) The simulation result of the programmable divide-by-N frequency divider (in Figure 4.19) for presetting N=5, namely f_{out}=fin/5.

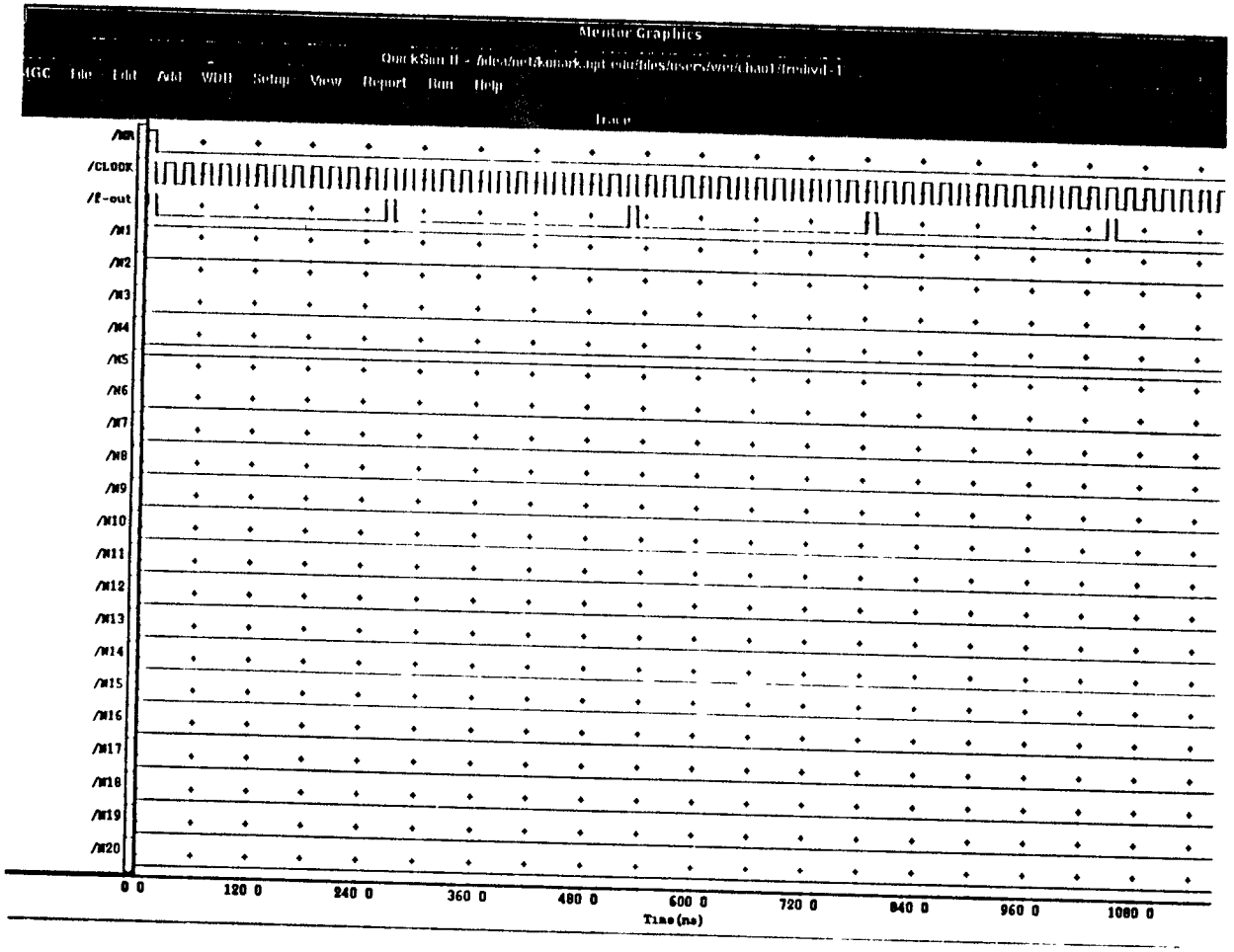


Figure 4.20 (b) The simulation result of the divide-by-N frequency divider for presetting N=13, namely f_{out}=fin/13

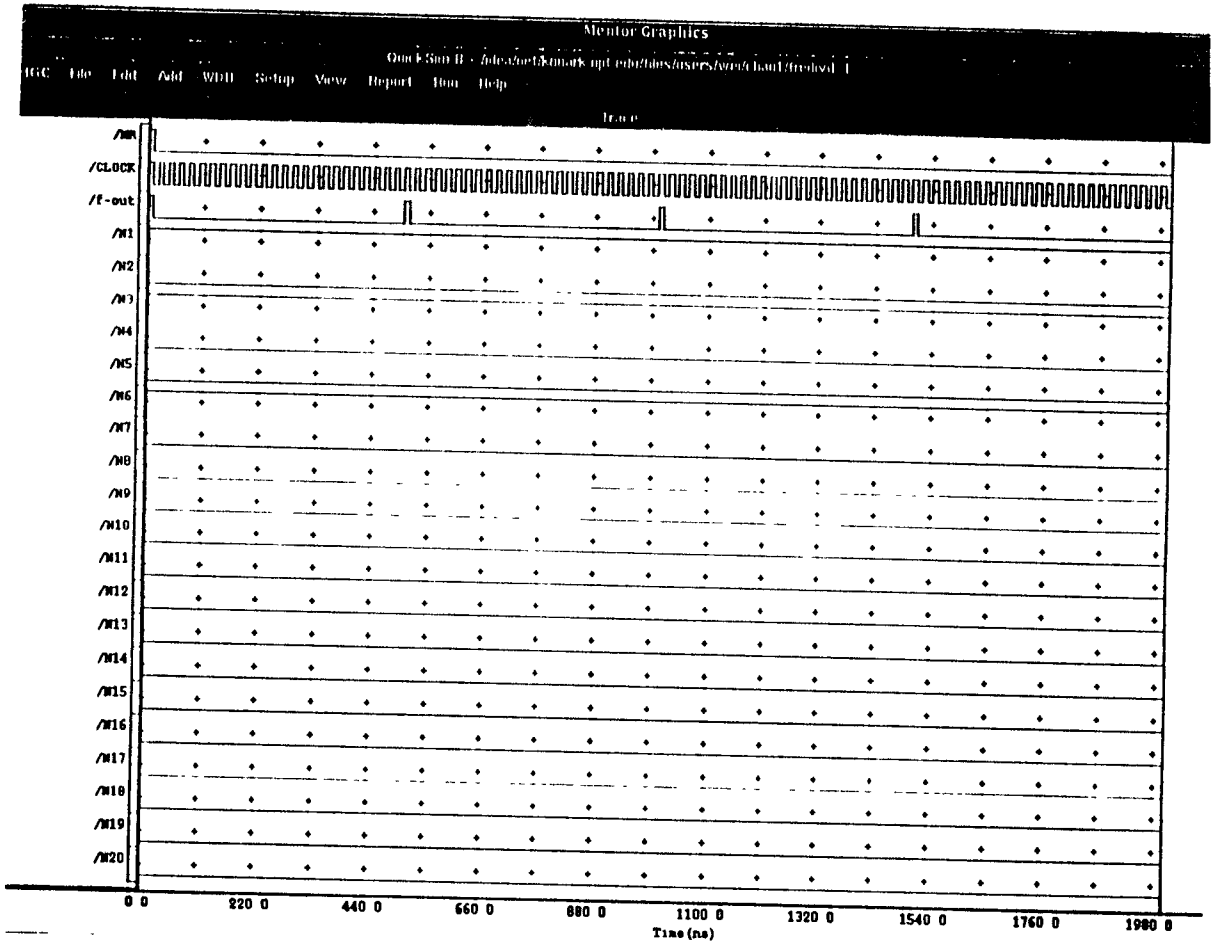


Figure 4.20 (c) The simulation result of the programmable divide-by-N frequency divider for presetting N=25, namely f_{out}=fin/25

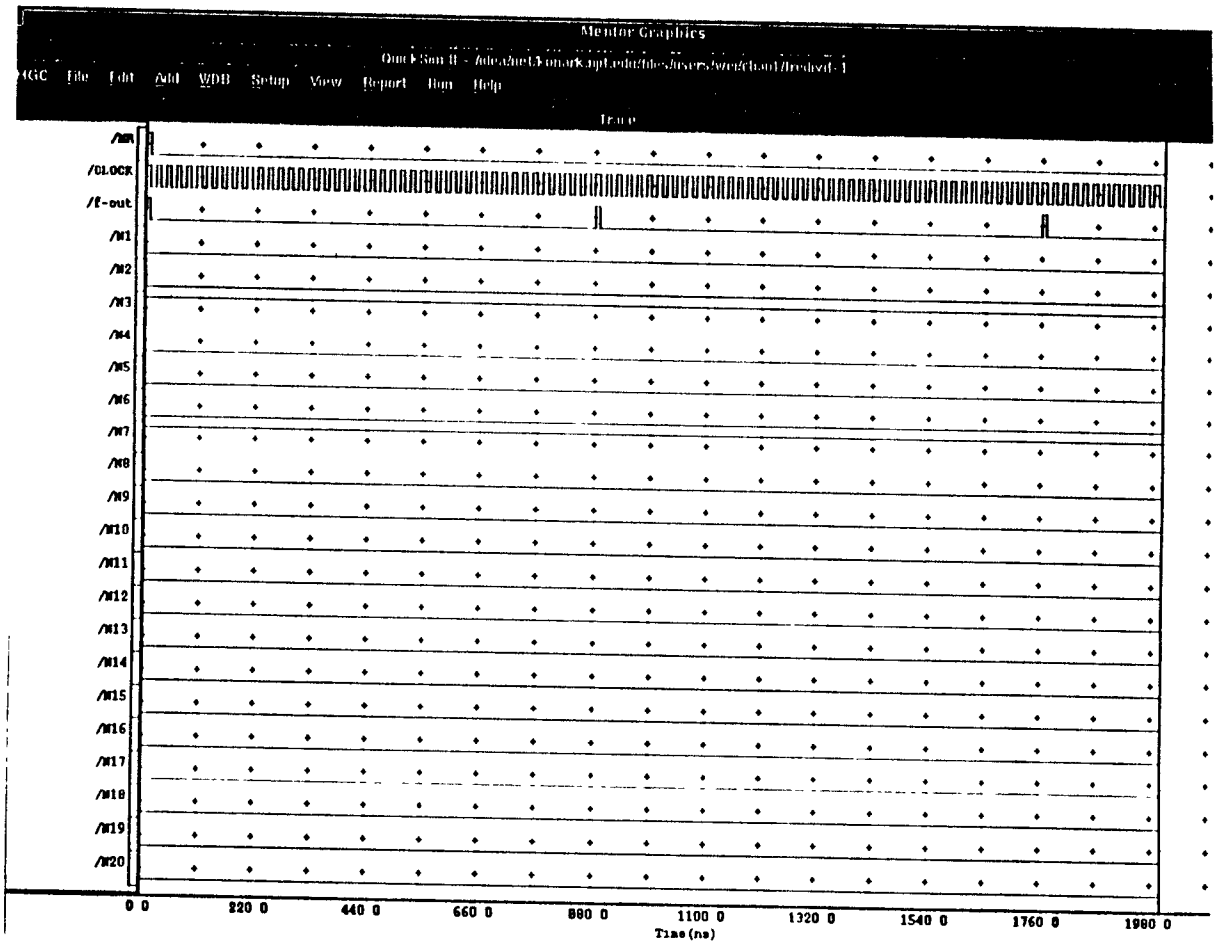


Figure 4.20 (d) The simulation result of the programmable divide-by-N frequency divider for presetting N=44, namely f_{out}=fin/44

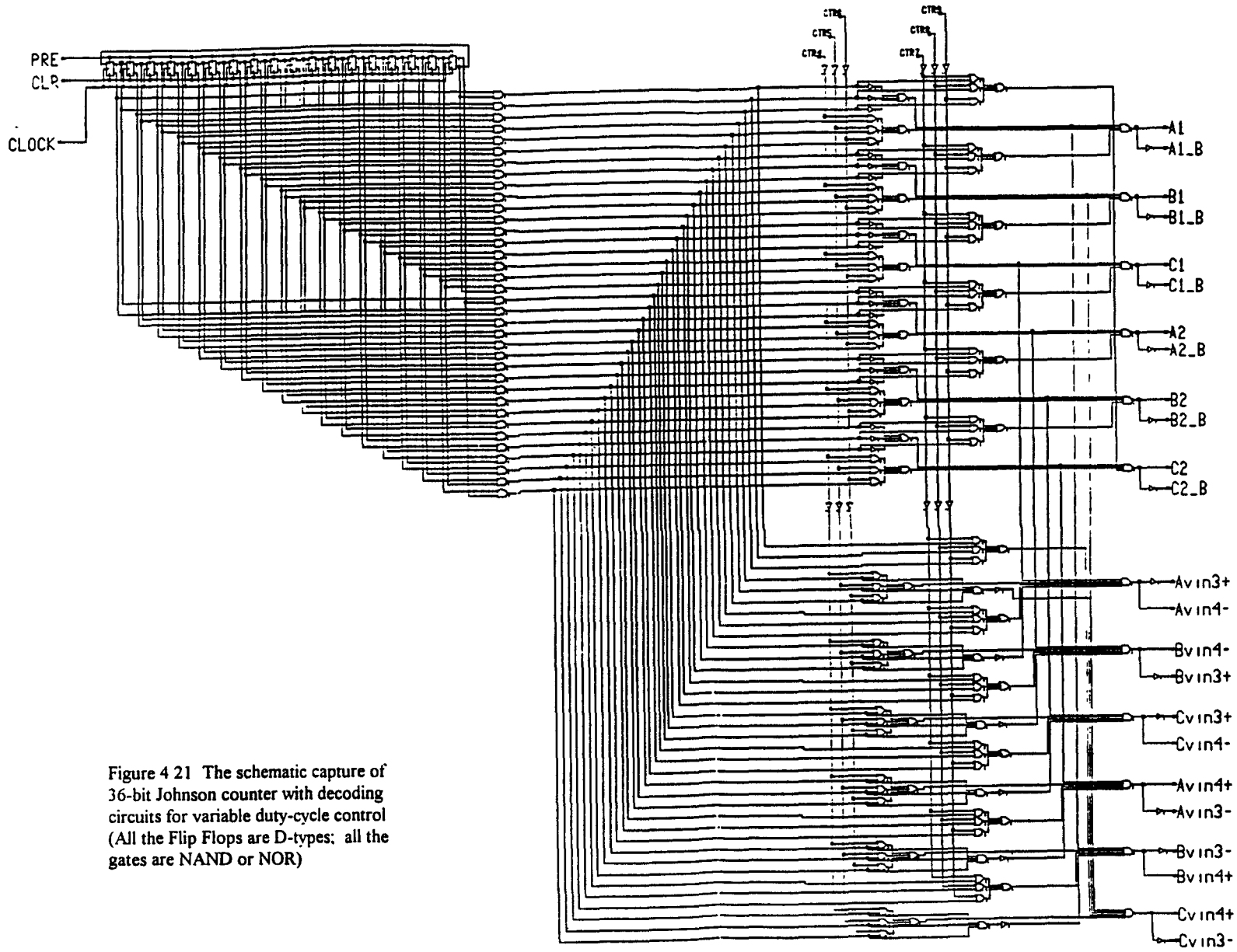


Figure 4 21 The schematic capture of 36-bit Johnson counter with decoding circuits for variable duty-cycle control (All the Flip Flops are D-types; all the gates are NAND or NOR)

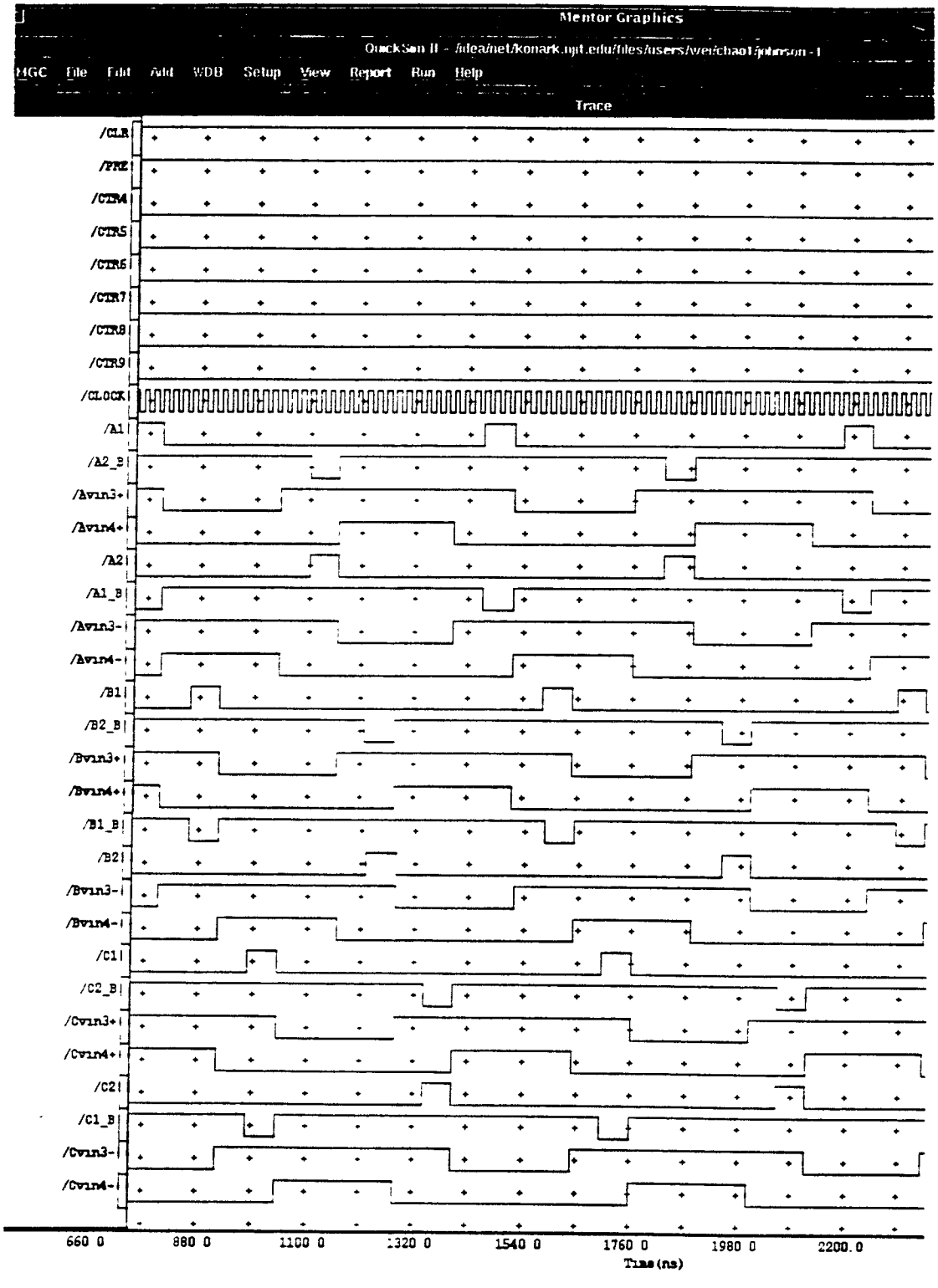


Figure 4.22 (a) The simulation result of the circuits for variable duty-c
(in Figure 4.21) in case of "ct1 ct2 ct3 ct4 ct5 ct6" = "000000"

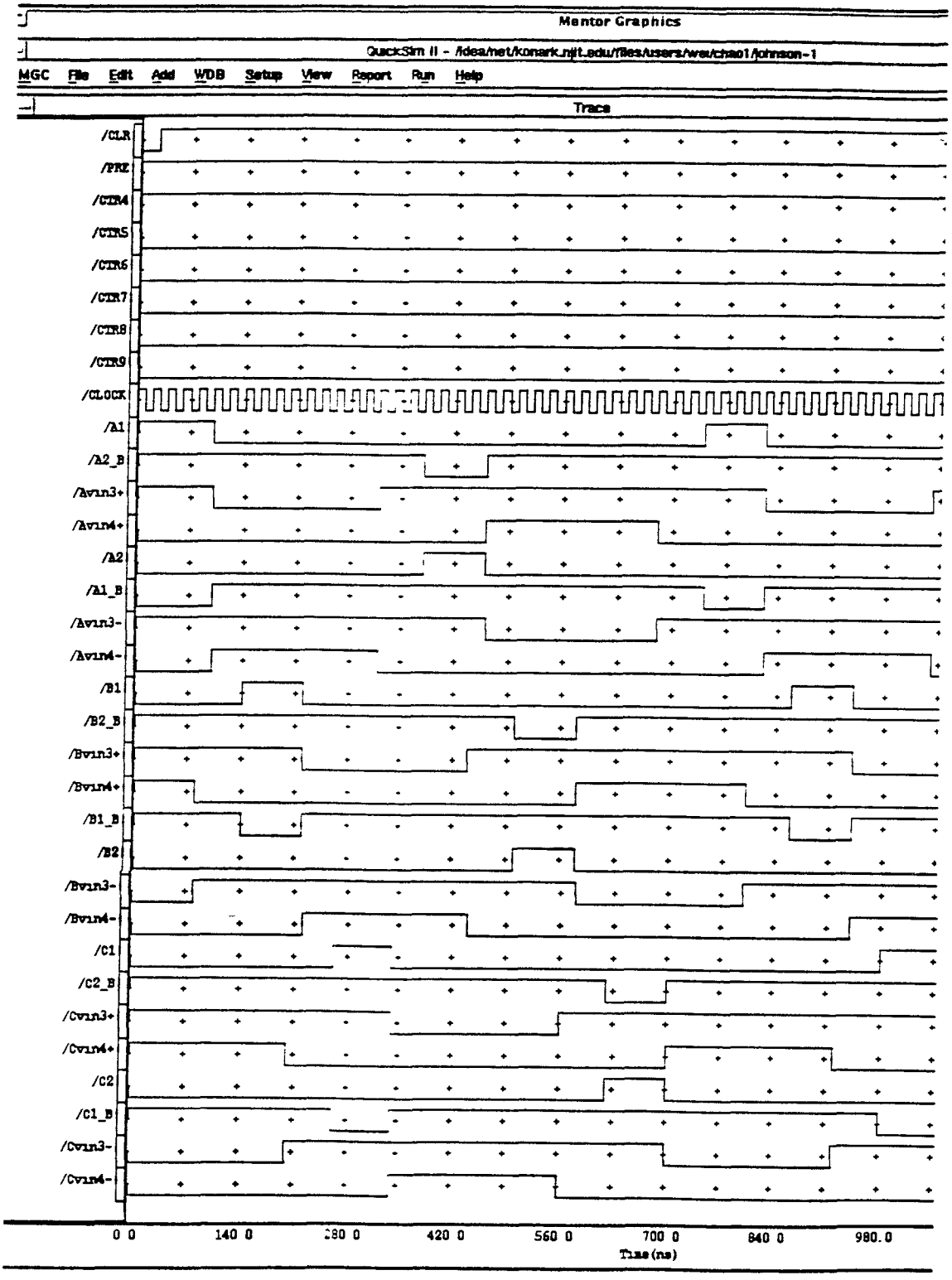


Figure 4.22 (b) The simulation result of the circuit in Figure 4.21 in case of "ct1 ct2 ct3 ct4 ct5 ct6" = "100000"

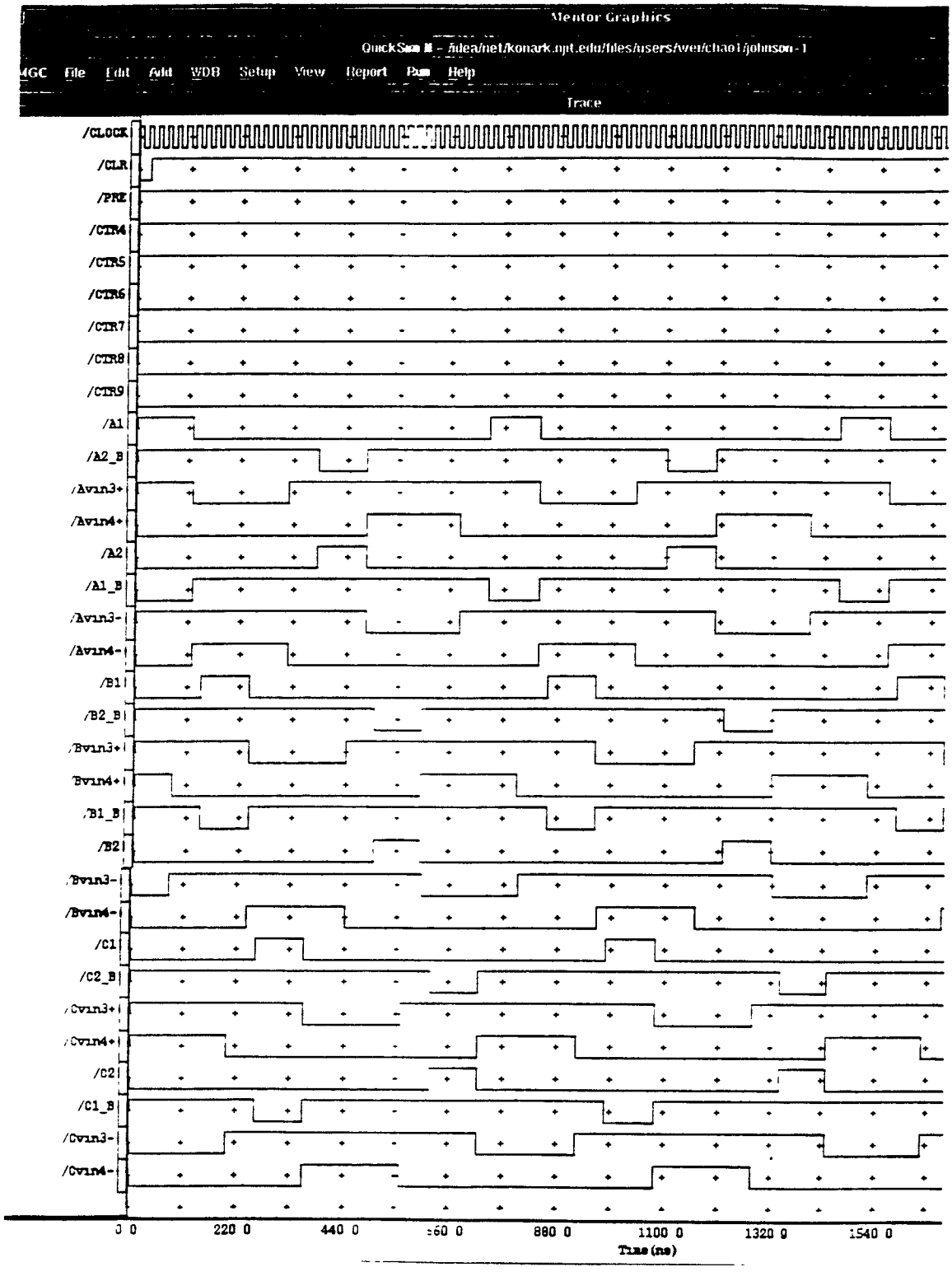


Figure 4.22 (c) The simulation result of the circuit in Figure 4.21 in case of "ct1 ct2 ct3 ct4 ct5 ct6" = "110000"

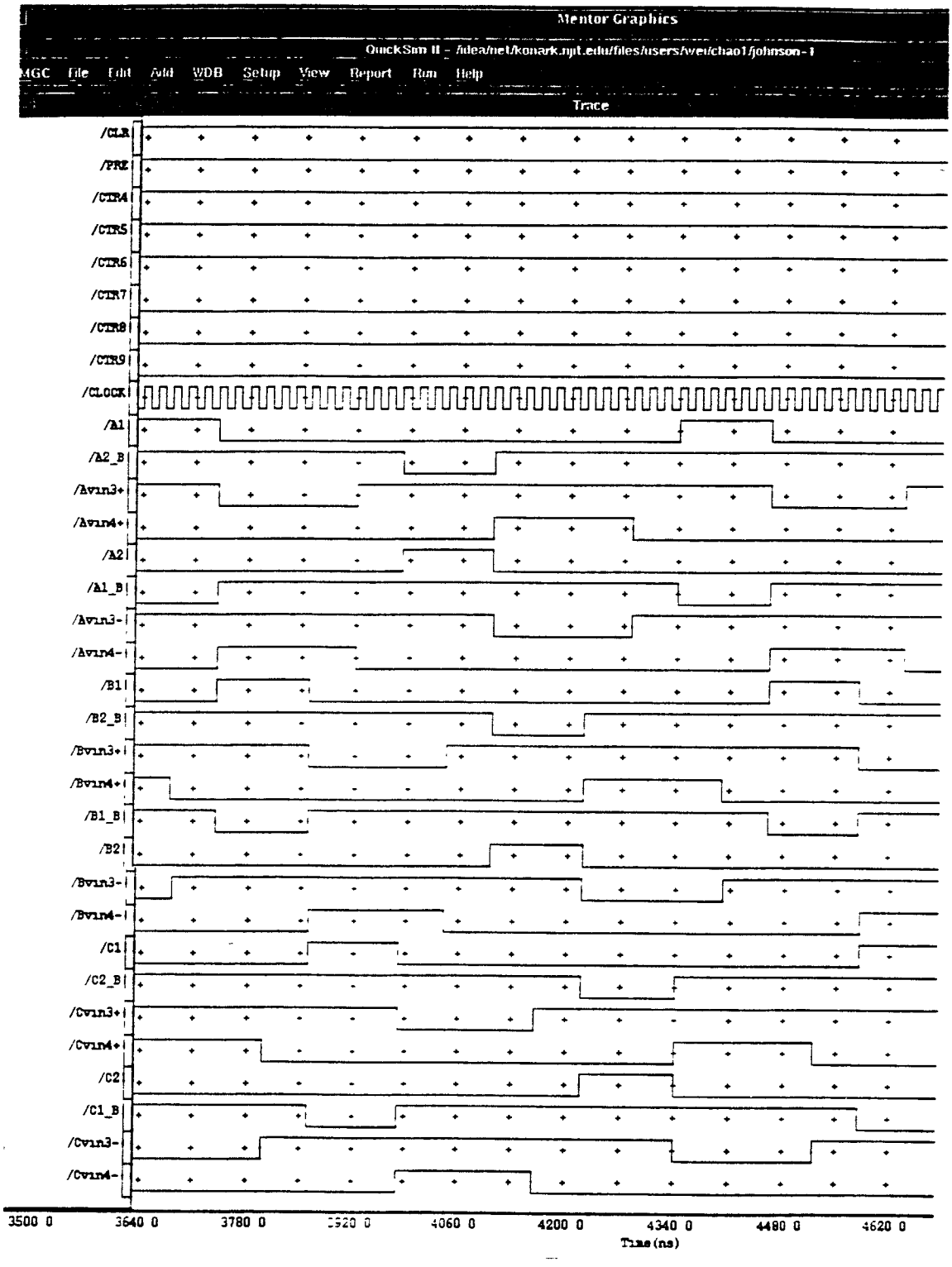


Figure 4.22 (d) The simulation result of the circuit in Figure 4.21 in case of "ct1 ct2 ct3 ct4 ct5 ct6" = "111000"

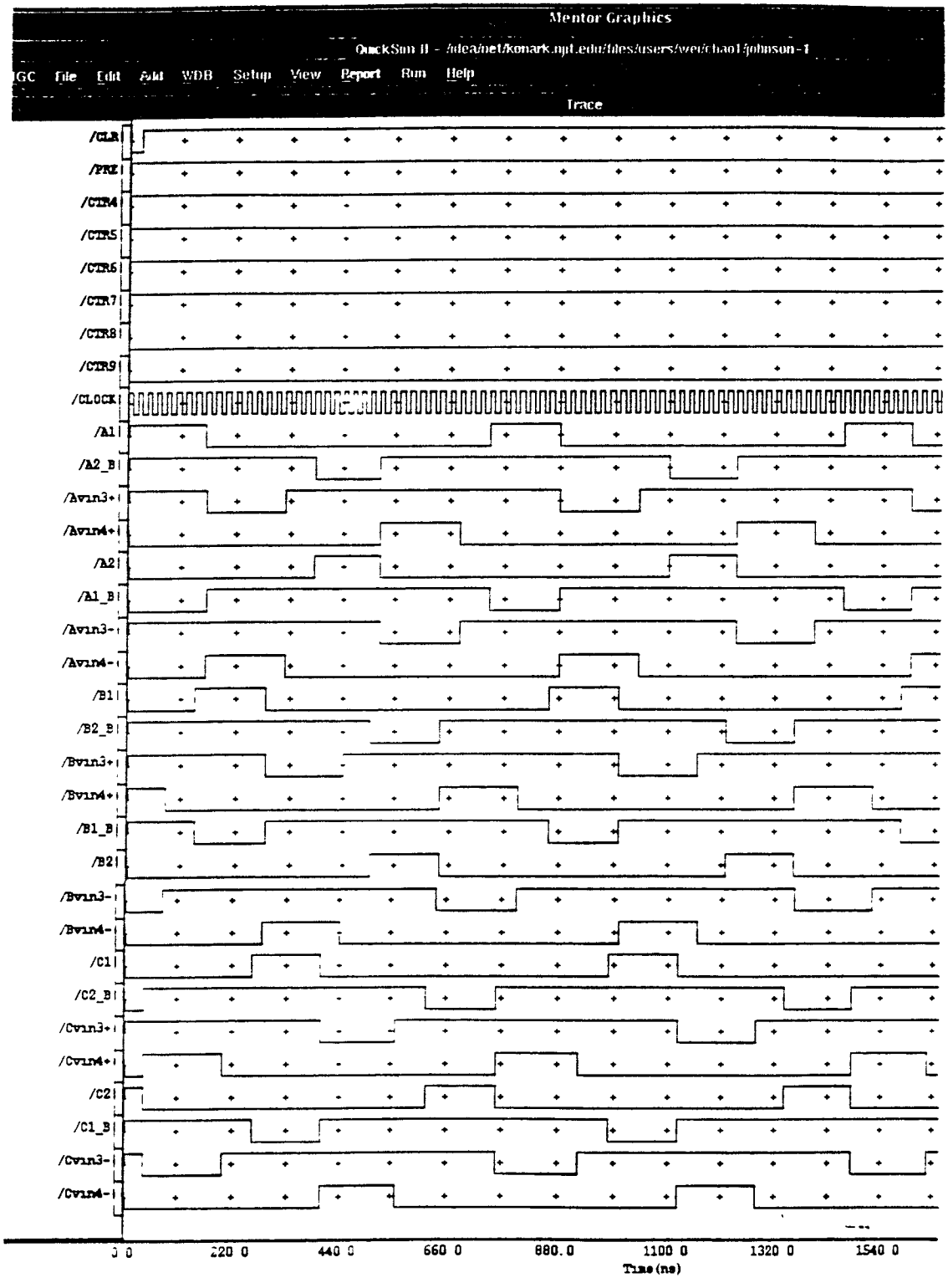


Figure 4.22 (e) The simulation result of the circuit in Figure 4.21 in case of "ct1 ct2 ct3 ct4 ct5 ct6" = "111100".

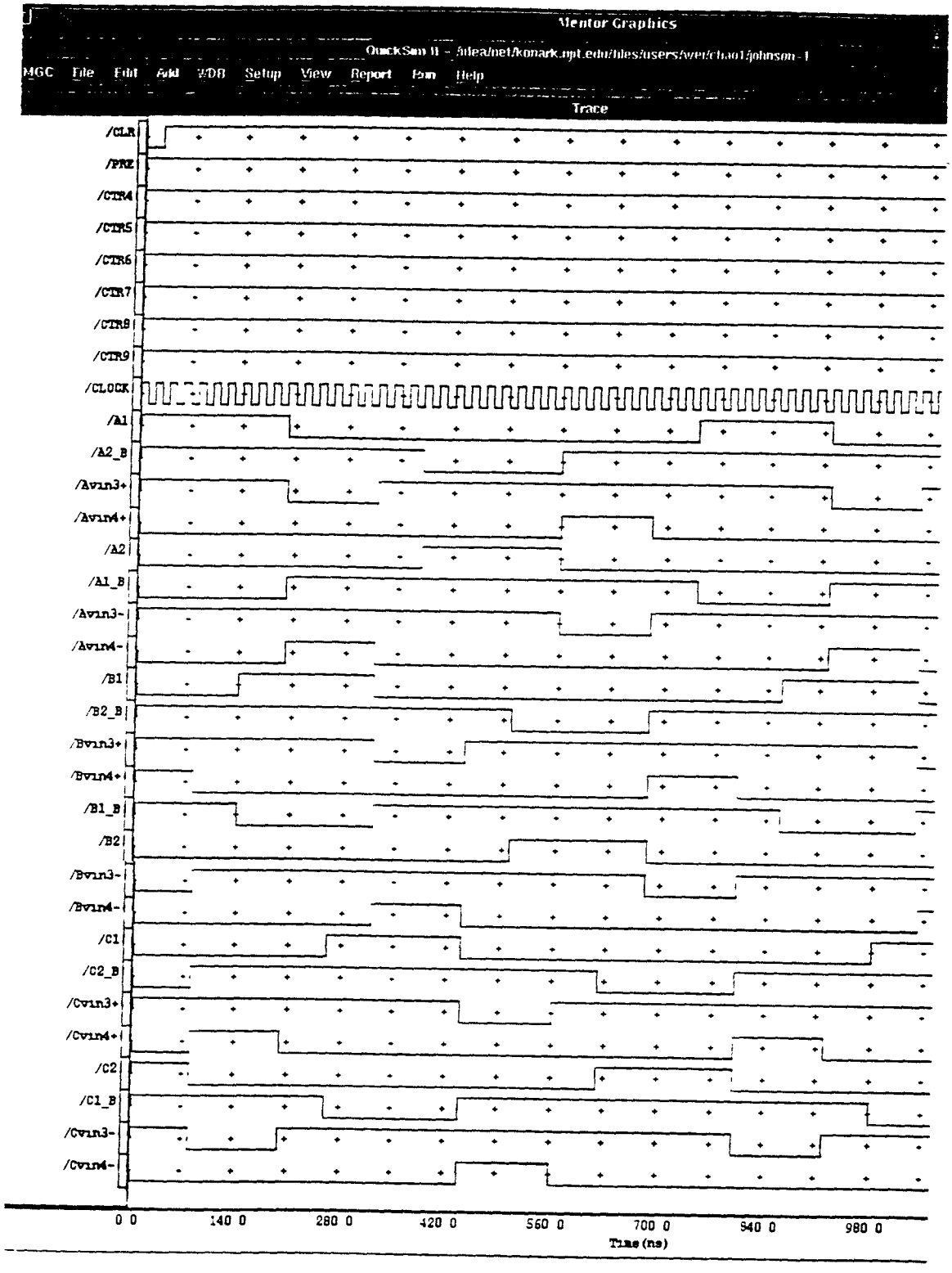


Figure 4.22 (f) The simulation result of the circuit in Figure 4.21 in case of "ct1 ct2 ct3 ct4 ct5 ct6" = "111111"

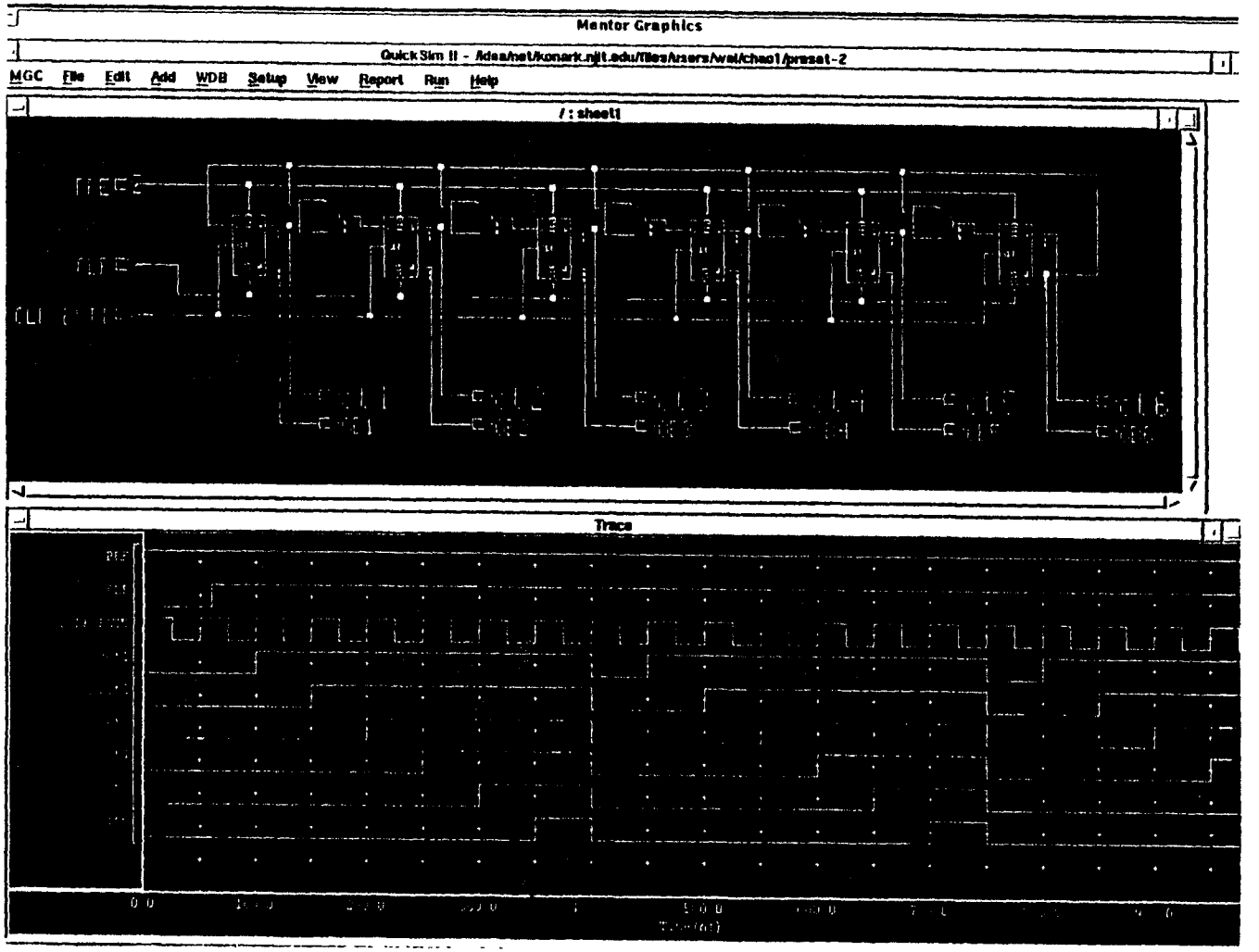


Figure 4.24 The simulation result of presetting circuit for variable duty-cycle control.

4.4 Physical Layout

Physical layout for the digital circuit of this power supply has been done using VLSI Design Tools, Mentor Graphics (V8) IC Graph. The process technology which has been selected for this IC layout is MOSIS 2μ, single poly, double metal, n-well, CMOS technology.

This IC chip has total physical size, including bonding pads, of around 2.5mmX2.5mm It has 37 pins, including VDD and VSS (GND), 11 inputs and control signals, and 24 outputs

CLKIN is high frequency clock input (which is supposed to be 80KHz) from a off-chip crystal oscillator. Reset1 is to load the presetting number N into the frequency divider. Dpb0, Dpb1, Dpb2, Dpb3 and Dpb4 are five push-button inputs for presetting N of the five digits in the frequency divider; Reset2 is clear these presetting registers. Reset3 is to reset the 36-bit Johnson counter PB6 is a push-button input for the presetting circuit of variable-duty-cycle control, Reset6 is to reset this presetting circuit

24 outputs, which are to be used by six high-voltage bipolarized drivers, are as follows:

A1, A1_B, B1, B1_B, C1, C1_B, A2, A2_B, B2, B2_B, C2, C2_B; Avin3+, Avin4+, Bvin3+, Bvin4+, Cvin3+, Cvin4+, Avin3-, Avin4-, Bvin3-, Bvin4-, Cvin3-, Cvin4-.

A photocopy of a portion of this IC layout is attatched in Appendix B.

CHAPTER 5

ANALOG DESIGN

5.1 Analog Design Methodology

To achieve the design requirements and specifications of the power supply in Chapters 2 and 3, the high-voltage circuit requires six identical analog bipolarized drivers to level-shift the required six phases for the power supply output.

The functional diagram of a single bipolarized high-voltage driver is shown in Figure 5.1. One can see from the figure that the driver consists of four parts, each with its own function.

5.2 Circuit Schematic Design of a Single High-voltage Driver

As mentioned in Chapter 3.2, one can have a simpler circuit based on a passive pulling-to-ground load resistor However, this simple circuit will not provide the desired rising and falling time required and frequency requirement of the bipolarized rectangular waveform. We prefer active pulling-up or pulling-down to ground in order to obtain much better waveform and higher frequency, as in our current design. Now let us look at the functional diagram of a high-voltage driver (Figure 5.1) and start to design and analyze circuit in detail for each of the four parts one by one.

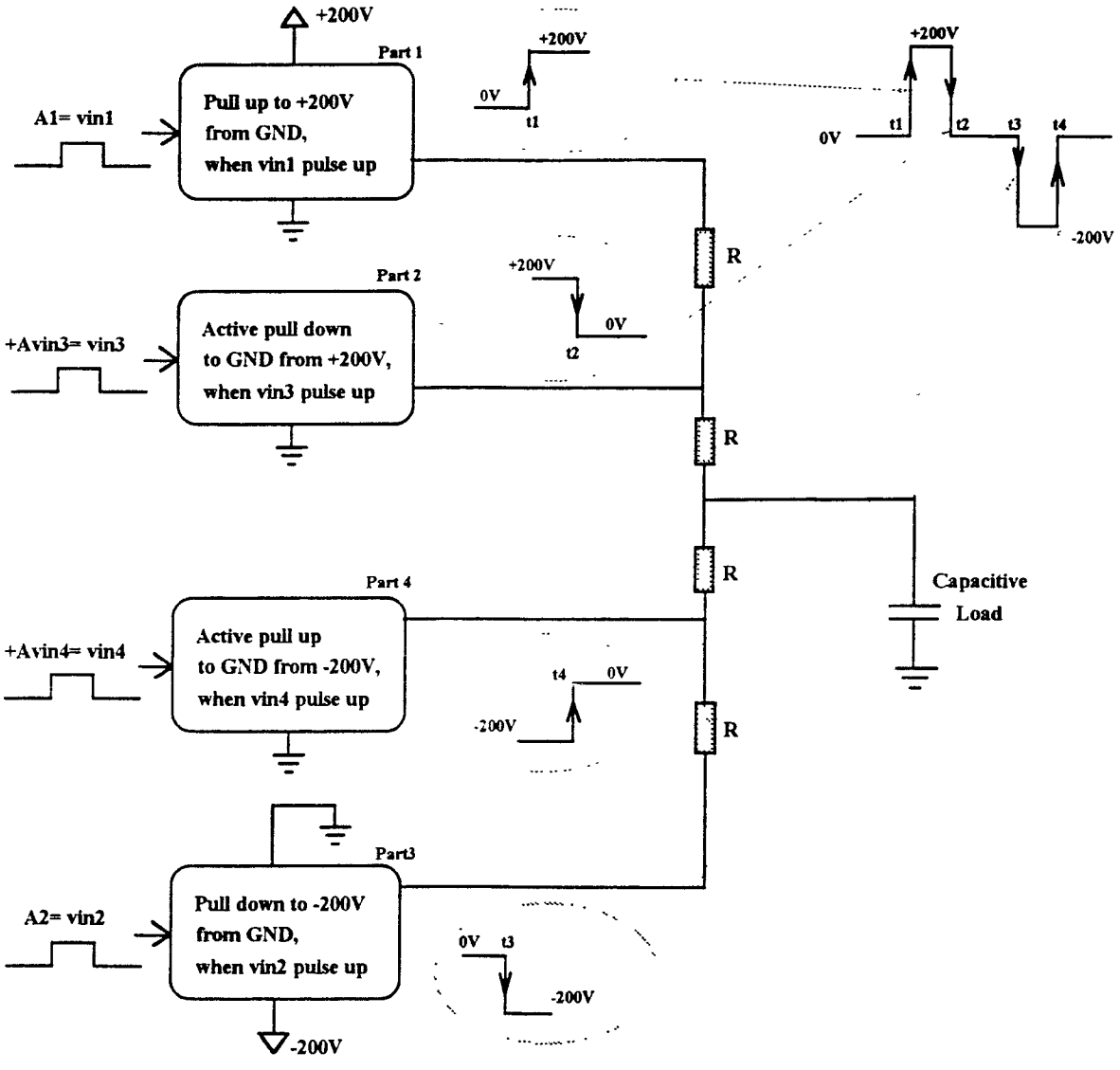


Figure 5.1 Entire Functional Diagram of a Single High-voltage Driver with Active Pull-up/down to GND

5.2.1 Design of Part 1 - Pull Up to +200V from GND When Vin1 Pulsing Up

After intuitive thinking, we have implemented Part 1 function with a circuit design shown in Fig. 5.2. Now let us analyze how it works.

When initially vin1=0V, Q1 (power NPN) is off, and voltage at nodes 5 and 105 are kept to be VDD1=+200V. Thus for M1 (power PMOS), V_{gs}=0V, and so it is off, and acting as a turned-off switch between nodes 1 and 99, the loading.

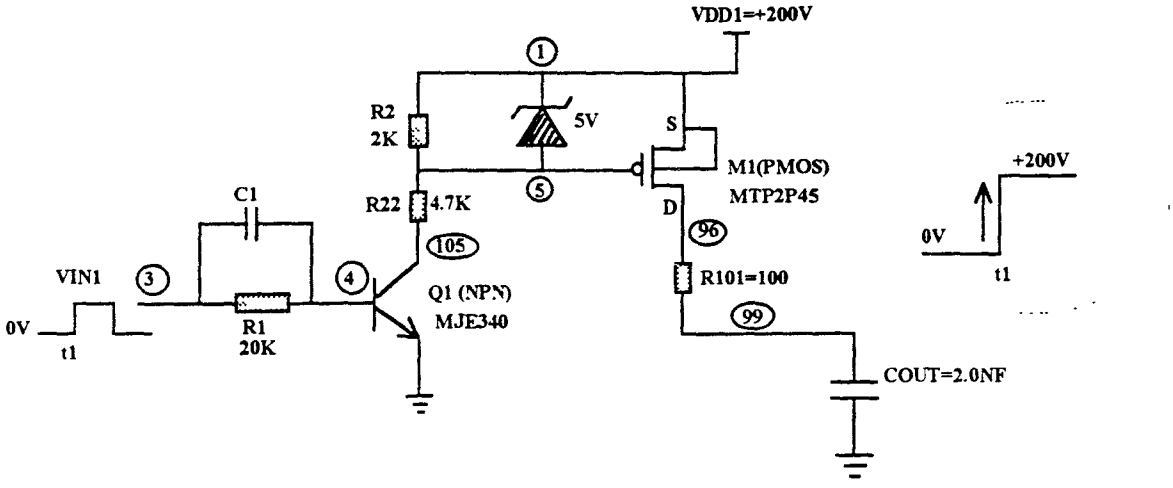


Figure 5.2 Circuit Schematic of Part 1 of a Single High-voltage Driver

Then, at a certain time t1, vin1=+5V, Q1 is turned on and driven into saturation. So a large current flows down through R2, ZD1(Zener Diode) and R22, and makes V@105 drop down to almost ground (=0.3~0 4V). Since the existence of the Zener diode (ZD1), the potential difference between nodes 1 and 5 is held to be 10V, no matter how large the voltage dropping on R22 is. Thus now for M1 (PMOS), V_{gs} = -10V, and it is turned on, acting as a turned-on switch between nodes 1 (VDD1) and 99 (output). The reason for which we choose 10V Zener diode here is that M1 is supposed to turn on at that moment, and that the power PMOS (MTP2P45) has a threshold voltage of -2~-3V, and usually has a hard-on voltage of Vgs=-10V, but not greater than 20V So, there is a current flowing from VDD1 down to the capacitive

load and charging it up to +200V, and keeping this potential until vin1 drops back to 0V again.

The resistor R22 should be a high-power-dissipation one because of the high voltage (almost 200V) dropping on it. Besides, we add a small-value current-limiting resistor R101 between nodes 1 and output 99.

5.2.2 Design of Part 2 - Active Pull Down to GND from +200V When Vin3 Pulsing Down

Function of Part 2 of a single high-voltage driver can be achieved by a circuit design shown in Fig. 5.3. Let us assume that the voltage on C_{out} is initially +200V.

When, at the beginning, vin3 is high (=+5V), Q3 (power PNP) is on and working in saturation. Voltage at node 13 keeps almost 0V (around 0.3~0.4V). Thus for M3 (power NMOS) , V_{gs} is only 0 3~0 4V, which is much lower than M3's threshold voltage, and it keeps off, acting as a turned-off switch between node 15 and 99

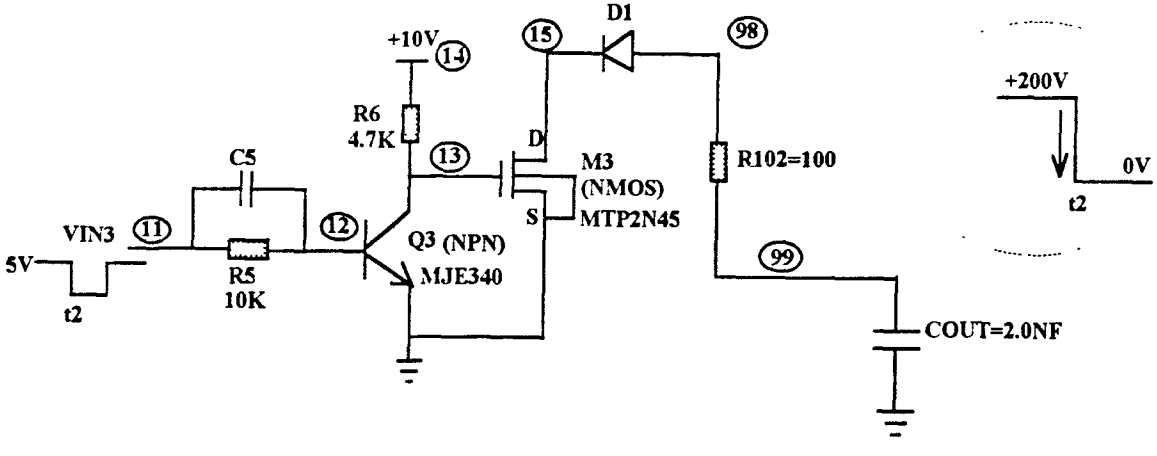


Figure 5.3 Circuit Schematic of Part 2 of a Single High-voltage Driver

When, at a certain time t2, vin3 suddenly drops down to 0V, then Q3 is turned off, and voltage at node 13 goes up immediately to VDD2=+10V The reason for which we choose 10V as source VDD2 also comes from the threshold voltage

(2.0~3.0V) and hard-on voltage (usually 10V) of M3 Thus for M3, V_{gs} becomes 10V, which makes M3 be turned on, like a switch being turned on between node 15 and 99. Therefore, C_{out} will be discharged very fast from +200V down to 0V, and be kept grounded as long as vin3 is low (=0V).

Also, a small-value resistor R102 is used to limit a might-be-high current flowing from nodes 99 to 15.

Note that there exists a high-voltage diode (D1) between nodes 98 and 15. The diode is necessary here, and its function will be understood well when we connect these four circuit parts together later in this section

5.2.3 Design of Part 3 - Pull Down to -200V from GND When Vin4 Pulsing Down

As shown in Fig. 5 4, function of Part 3 of a single high-voltage driver can be implemented with a circuit design which is very symmetrical to that of Part 1 And the detail analysis of the circuit is also symmetrical to that of Part 1.

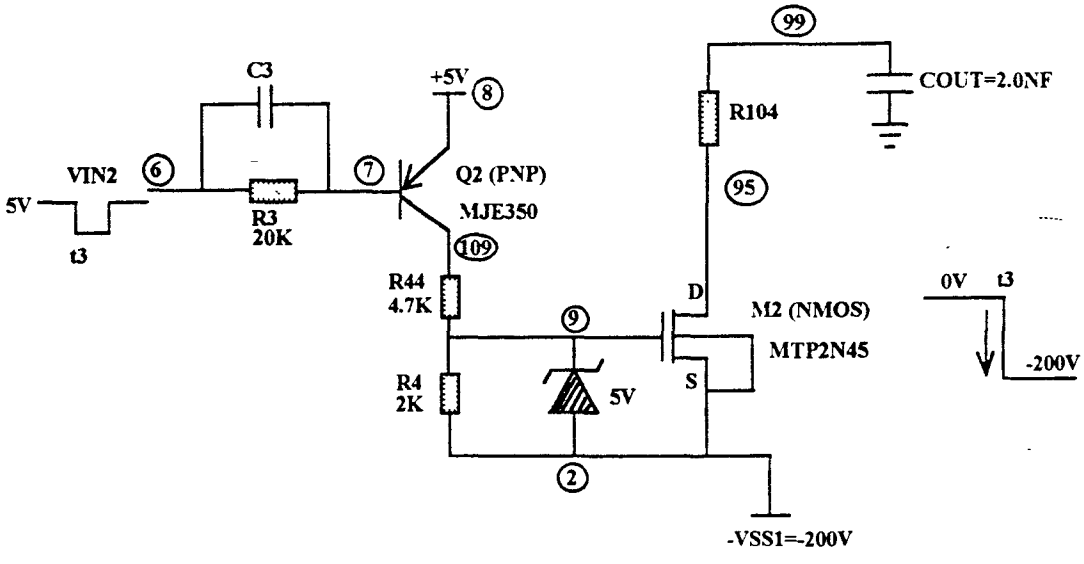


Figure 5.4 Circuit Schematic of Part 3 of a Single High-voltage Driver

Initially, when vin2 is high (=+5V), V_{eb} of Q2 (power PNP) is equal to 0V and so Q2 is off. Voltage at node 9 and 109 are held low to V_{SS}=-200V Thus for M2 (power NMOS), V_{gs}=0V, and so it keeps off, acting as a turned-off switch between node 2 and output 99.

At a certain time t3, when vin2 goes down to 0V, Q2 (PNP) is turned on and is driven into saturation. A large current flows down through R44, R4 and ZD2 (Zener Diode), and makes voltage at node 109 go up to almost +5V (=4.7~4.8V). Since the existence of the Zener diode (ZD2), the potential difference between nodes 9 and 2 is kept to be 10V, no matter how large the voltage dropping on R44 is. Thus now for M2 (NMOS), V_{gs}=10V, and so it is turned on, acting as a turned-on switch between nodes 1 (VSS1) and 99 (output) The reason for which we choose 10V Zener diode here is that the threshold voltage of the power NMOS is 2~3V, and its usual hard-on voltage is around 10V. So, there is a current flowing between VSS1 and the capacitive load, and charging it to -200V, and keeping it over there until vin2 goes up back to +5V

Also, the resistor R44 should be a high-power-dissipation one, and a small-value current-limiting resistor R101 is needed between nodes 95 and 99.

5.2.4 Design of Part 4 - Active Pull Up to GND from -200V When Vin4 Pulsing Up

The function of Part 2 of a single high-voltage driver can be achieved by a circuit design, as shown in Fig. 5.5, which is symmetrical to that of Part 2. And the circuit could be understood in a similar way as that of Part 2. Anyway, we will present the analysis here for completeness.

Let us assume that the voltage on C_{out} is initially -200V. When, at the beginning, vin4 is low (=0V), Q4 (power NPN) is keeping on since the emitter of Q4 is connected to +5V DC source The voltage at node 23 is pulled up to almost +5V

(=4.7~4.8V), because Q4 is driven into saturation. Thus for power PMOS M4, V_{gs}=4 7V > 0, and so it keeps off, and acting as a turned-off switch between node 99 and ground.

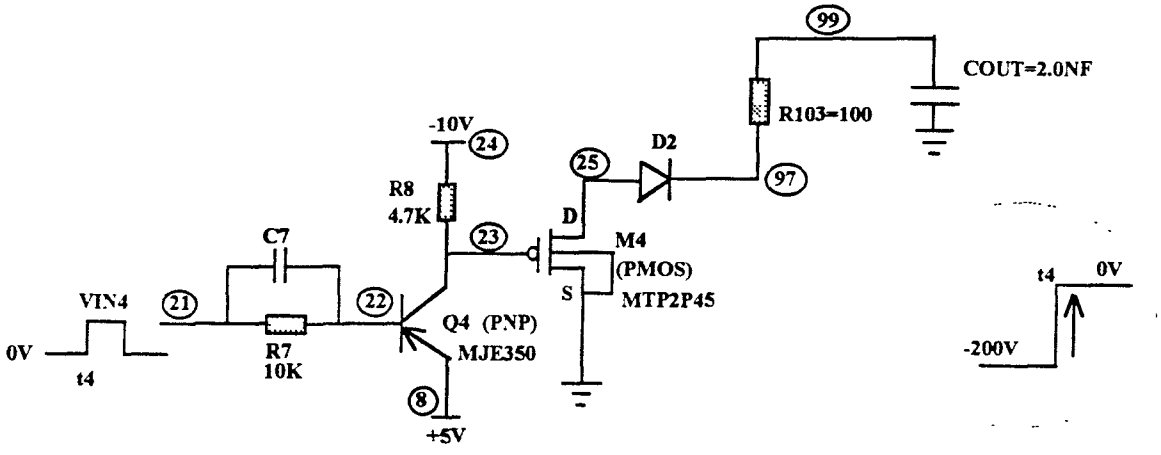


Figure 5.5 Circuit Schematic of Part 4 of a Single High-voltage Driver

Then, at a certain time t4, vin4 suddenly goes up to +5V, Q4 is turned off, and voltage at node 23 drops fast down to -10V Usually, PMOS M4 (MTP2P45) has a $V_{threshold}$ of -2.0V and an hard-on voltage of -10V Thus for M4 here, V_{gs} becomes -10V, which makes M4 be turned on, acting as a being-on switch between node 99 and ground. Therefore, C_{out} will be discharged very fast from -200V to 0V, and be held grounded as long as vin4 is high (=5V).

Also note that there exists a high-voltage diode (D2) between nodes 25 and 97, whose important function will be understood clearly when these four circuit parts is connected together later in this section. Besides, a small-value, current-limiting resistor R104 is needed between nodes 97 and 25.

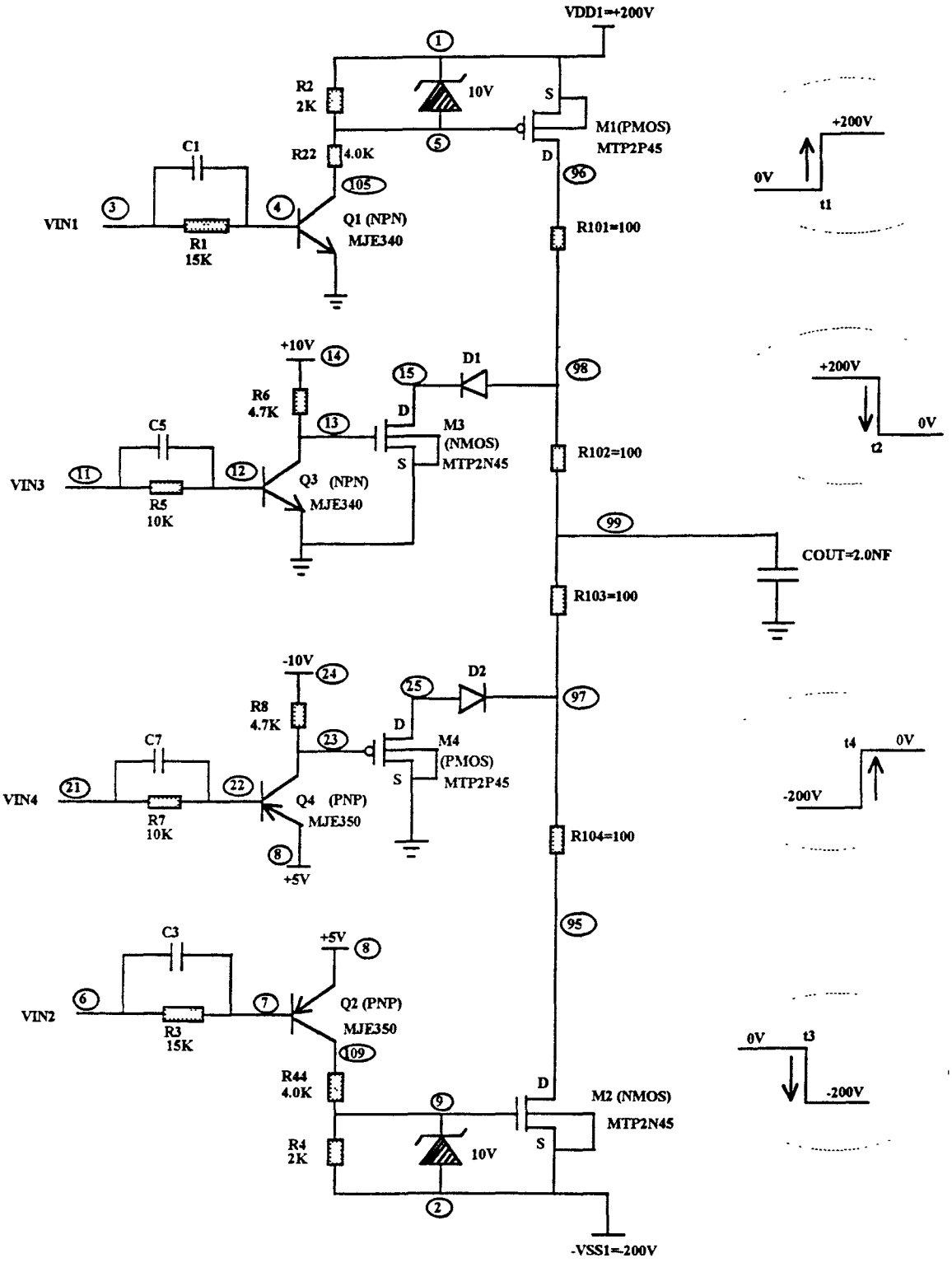


Figure 5.6 Schematic of a Single Bipolarized High-voltage Driver with Active Pulling-to-Ground

5.2.5 Entire Circuit Structure of A Single Bipolarized High-voltage Driver

Now that we have finished designing and analyzing each of the four parts of a single bipolarized high-voltage driver, let us connect them together properly to achieve the function of the driver. Shown in Figure 5 6 is the entire circuit structure of a single bipolarized high-voltage driver, for which we will do some further analysis.

Although this circuit deals with bipolarized high voltage up to more than +200V and -200V, every power transistor in the circuit is working in a switching mode. And each of the four parts of the driver is acting as a switch between +200V and output load, or between -200V and output load, or between ground and output load, being turned on or off properly in time under the control of the four input digital signals. Thus, it is not a real analog amplifying circuit, but more like a digital switching circuit dealing with high voltage. But anyway, we still name it here "Analog, bipolarized, high-voltage driver".

Note that there exist two high-voltage diodes (D1 and D2) in Part 2 and Part 4. The reason is as follows. When V@99 is pulled down to -200V, the Part 2 (mainly transistor M3) will tend to be turned on to pull V@99 up to GND which it is not expected to do. So we put a high-voltage diode D1 (in the direction as shown in Figure 5.6) between nodes 15 and 98 to keep V@15 high and keep M3 be off. In the same way, when V@99 is pulled up to +200V, the Part 3 (mainly transistor M4) will tend to be turned on to pull V@99 down to GND, which it is not expected to do. Thus a high-voltage diode D2 is also needed between nodes 25 and 97 to keep V@25 low and keep M4 be off.

Also note that there is a capacitor in each part of the circuit, C1, C3, C5, C7, respectively, which is called speed-up capacitor. Take a look at Figure 5.7(a) Ideally, with a step of voltage at the input, we would like to have a step change of collactor current. However, we notice that the change in collector current of takes time, especially for power bipolar transistor we have used. The performance of the circuit

can be improved if a capacitor C is added, bypassing the base resistor R, to speed up its turn-on and turn-off, as shown dotted in Figure 5.7(a) Their values vary with the practical parameters of each transistor. See Figure 5 7(b) and (c) for more illustrations. This use of a speed-up capa itor to improve the transient characteristics is a viable technique with discrete bipolar transistors, which are actually used in our high-voltage drivers implementation.

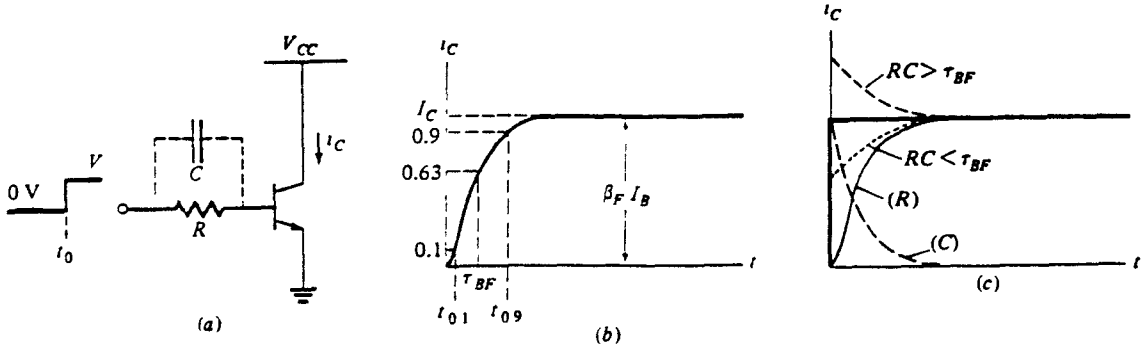


Figure 5.7 Illustration of Speed-up Capacitors.
(a) Simple common-emitter amplifier with speed-up capacitor.
(b) Colector current waveform for circuit without speed-upcapacitor
(c) Collector current waveform illustrating effect of speed-up capacitor.

5.2.6 Four Digital Input Configuration - Elimination of "Both Switch-on" Problem

Looking at Figure 5.6, entire circuit of a single high-voltage driver, note that Part 1 can be "switched on" only when Part 2 and Part 3 are under "switching-off". Part 4 will not affect Part 1 since it has a high-voltage diode D2.

Also note that, similarly, Part 2 can be "switched on" only when Part 1 and Part 3 are under "switching-off". Part 3 can be "switched on" only when Part 1 and Part 4 are under "switching-off". Part 4 can be "switched on " only when Part 1 and Part 3 are under "switching-off".

Thus, to implement driver circuit with active pull-up and pull-down to ground, we must be very careful with those four digital input pulses As shown in Figure 5 8, we have two kinds of digital signal configuration which are interesting and worth discussion.

Figure 5 8(a) is the case which most people would probably think of. Ideally and theoretically it should work very well, but practically not Consider that the power transistors which we use in the circuit have relatively large and various turn-on and turn-off time, it will possibly make both Part 1 and Part 2 of the circuit "switch on" for even a very short moment at around time = t1, or both Part 3 and Part 2 "switch on" at time = t2, or both Part 3 and Part 4 "switch on" at time = t3, or both Part 3 and Part 1 "switch on" at time = t4

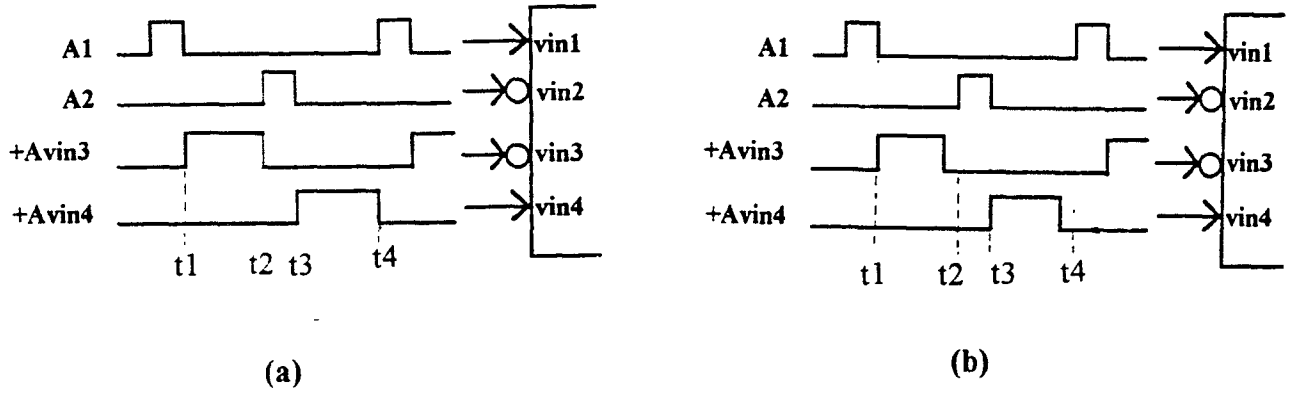


Figure 5.8 Two Different Configurations of 4 Digital Input Pulses

By adding some speed-up capacitors across the base resistors of each bipolar, e.g., C1, C3, C5 and C7 as shown in Fig. 5.6, we can adjust turn-on and turn-off time of power bipolar transistors, so that the "both switch-on" problem can be probably eliminated at time = t1 and t3. However, under a same condition of capacitor's values, it is very difficult, or almost practically impossible to eliminate this problem at

all t1, t2, t3 and t4. Any a little bit "both on" will destroy seriously the circuit performance when reaching high voltage or high frequency

On the other hand, the configuration of 4 digital inputs in Fig. 5.8(b) figures out this problem smartly. It definitely will not have any "both switch-on" problem at time = t2 and t4. By adding speed-up capacitors of proper value, as having already stated above, it is not difficult to eliminate any "both on" problems existing at time = t1 and t3. Therefore, this configuration works much better, and has been chosen in our design.

5.3 Circuit Simulation Using PSPICE

PSPICE is a very popular software package for analog simulation of, basically, small-signal circuits It can, however, also be used for power circuit simulation, just as in our case, with some modification of some parameters and choices of some options.

The important thing during this simulation is that, although PSPICE has its own large Parts Library, the four power transistors which are used in our circuit, MJE340, MJE350, MTP2N45, and MTP2P45, are not included in the PSPICE Library So I have to create my own parts models for these four, using Parts Program in PSPICE. The parameters were extracted from the data sheets of these parts.

Using circuit nodes in Figure 5.6 as reference, let's take a look at simulation results. The waveforms of four digital input signals, V@3, V@6, V@11 and V@21, are shown in Fig. 5.9. And the output waveform, V@99, is shown in Figure 5.10. Also waveforms of some interesting nodes are shown in Figure 5.11. Waveforms of these nodes under different conditions are shown in Fig. 5.12 and 5.13.

The PSPICE circuit description input file and output file are attatched in the Appendix.

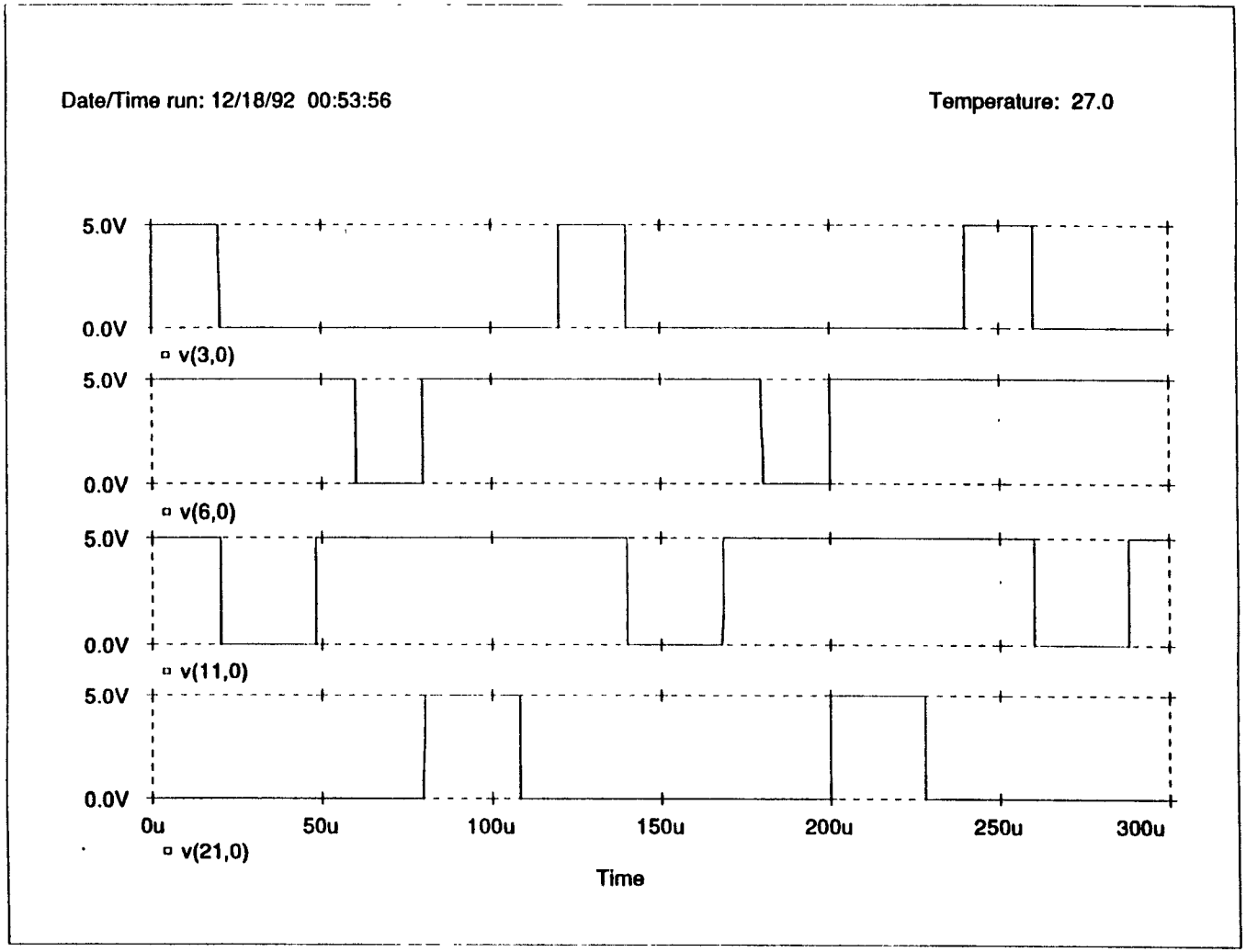


Figure 5.9 Waveforms of four digital input signals for the high-voltage driver

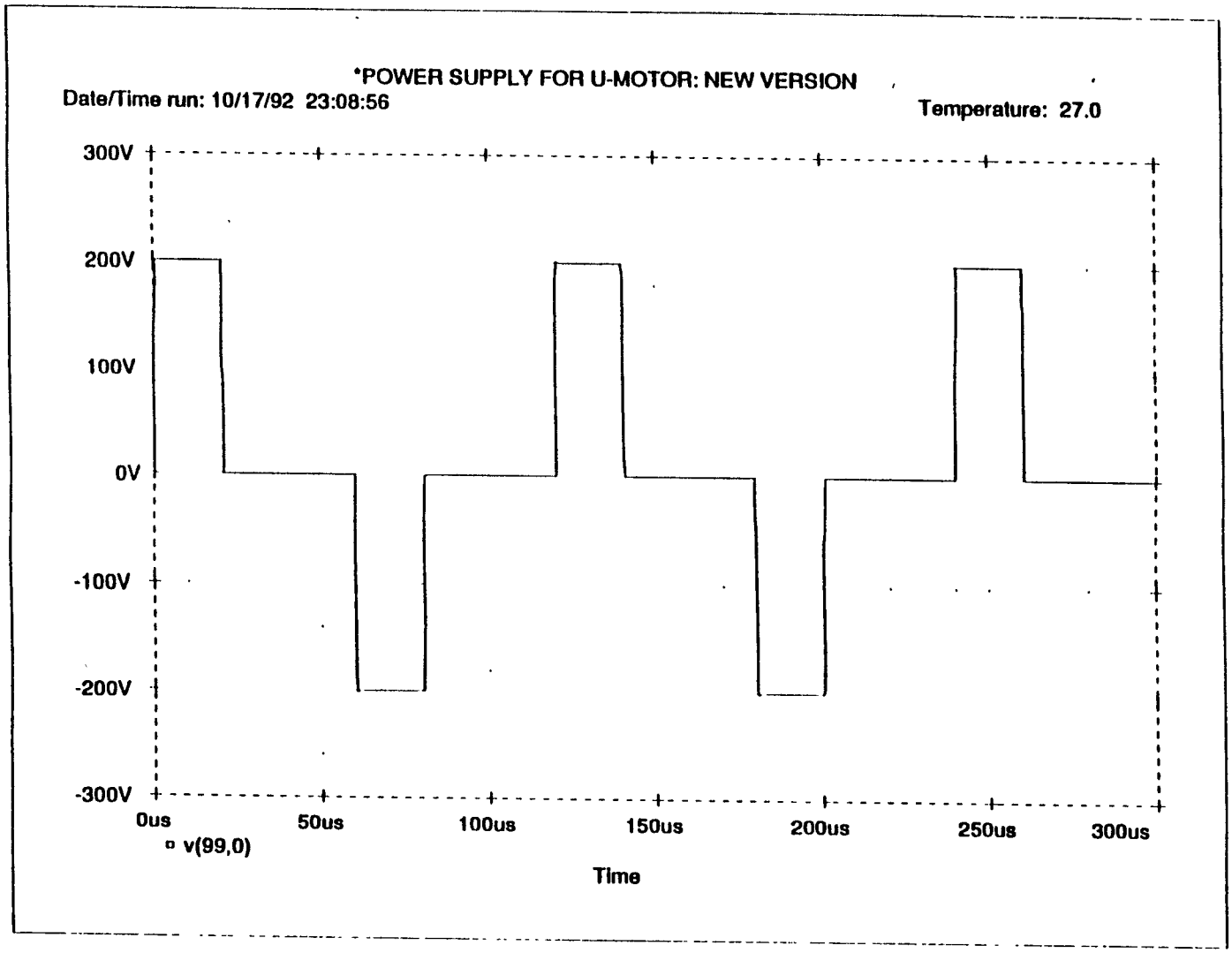


Figure 5.10 Waveform of output, V@99, of the bipolarized high-voltage driver. R101=R102=R103=R104=20Ω; Cout=50nF.

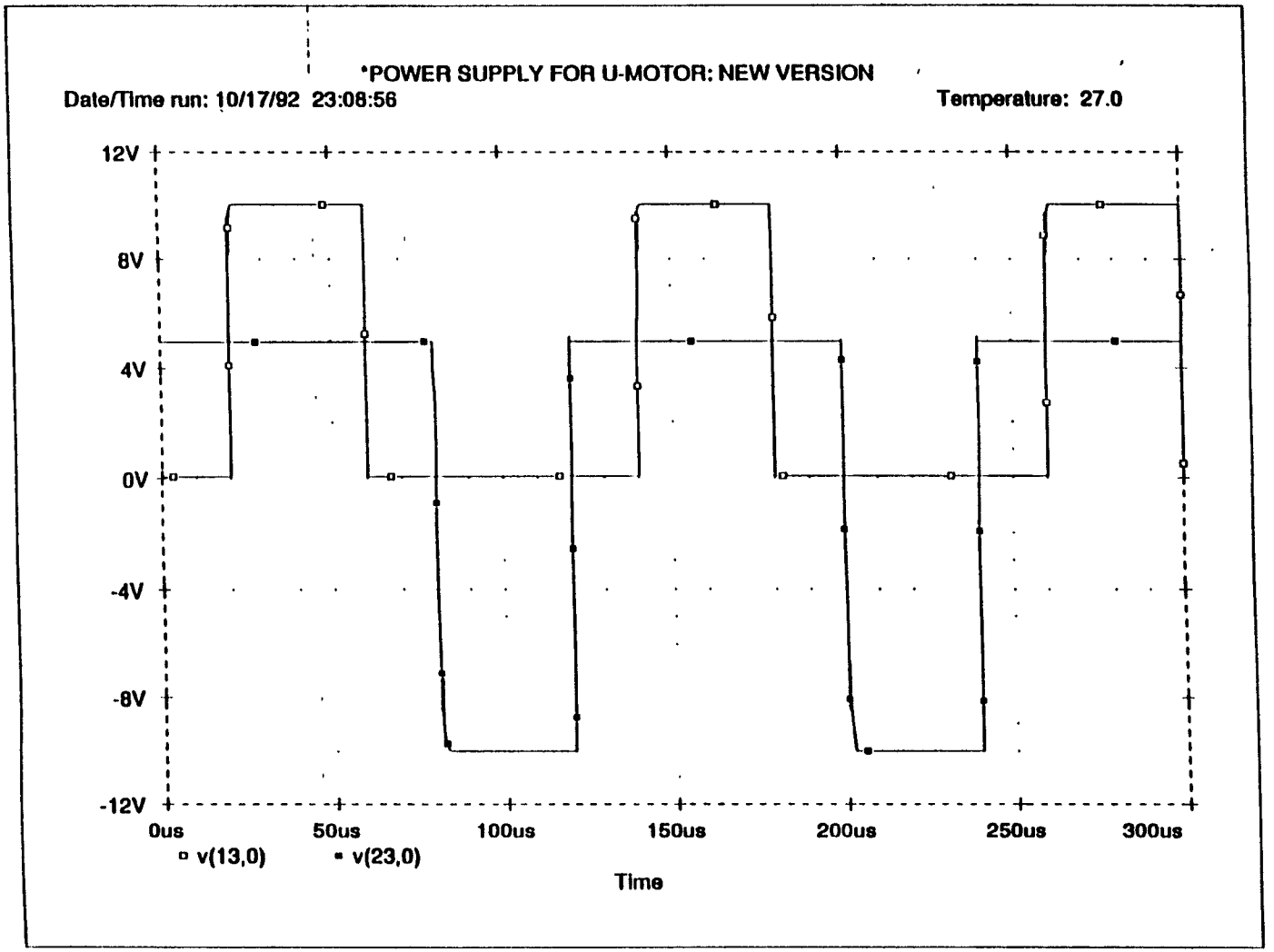


Figure 5.11 Waveforms of V@13 and V@23 of the high-voltage driver. R101=R102=R103=R104=20Ω; Cout=50nF

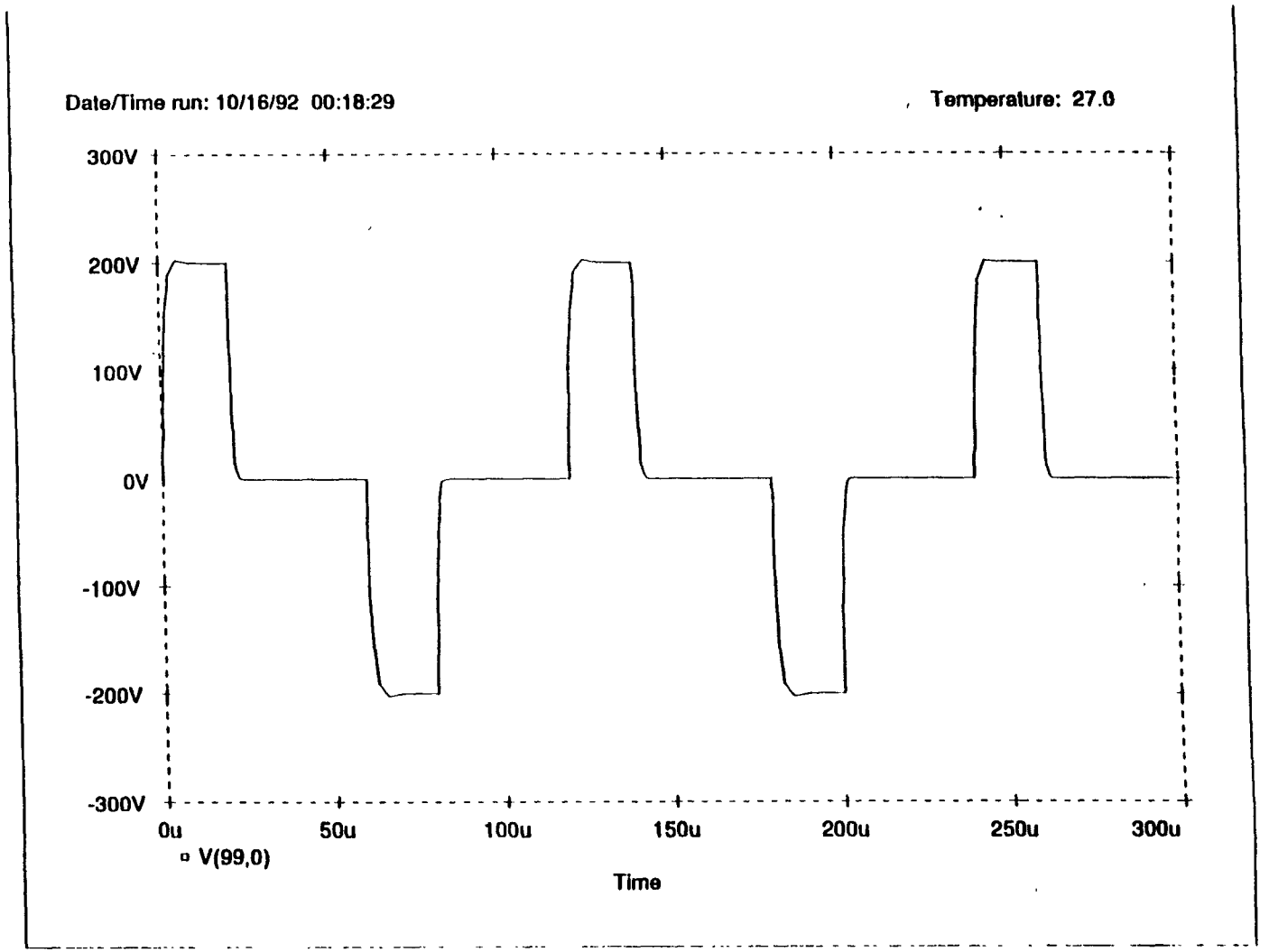


Figure 5.12(a) Output waveform of V@99 of the high-voltage driver.
R101=R102=R103=R104=200Ω; Cout=200nF

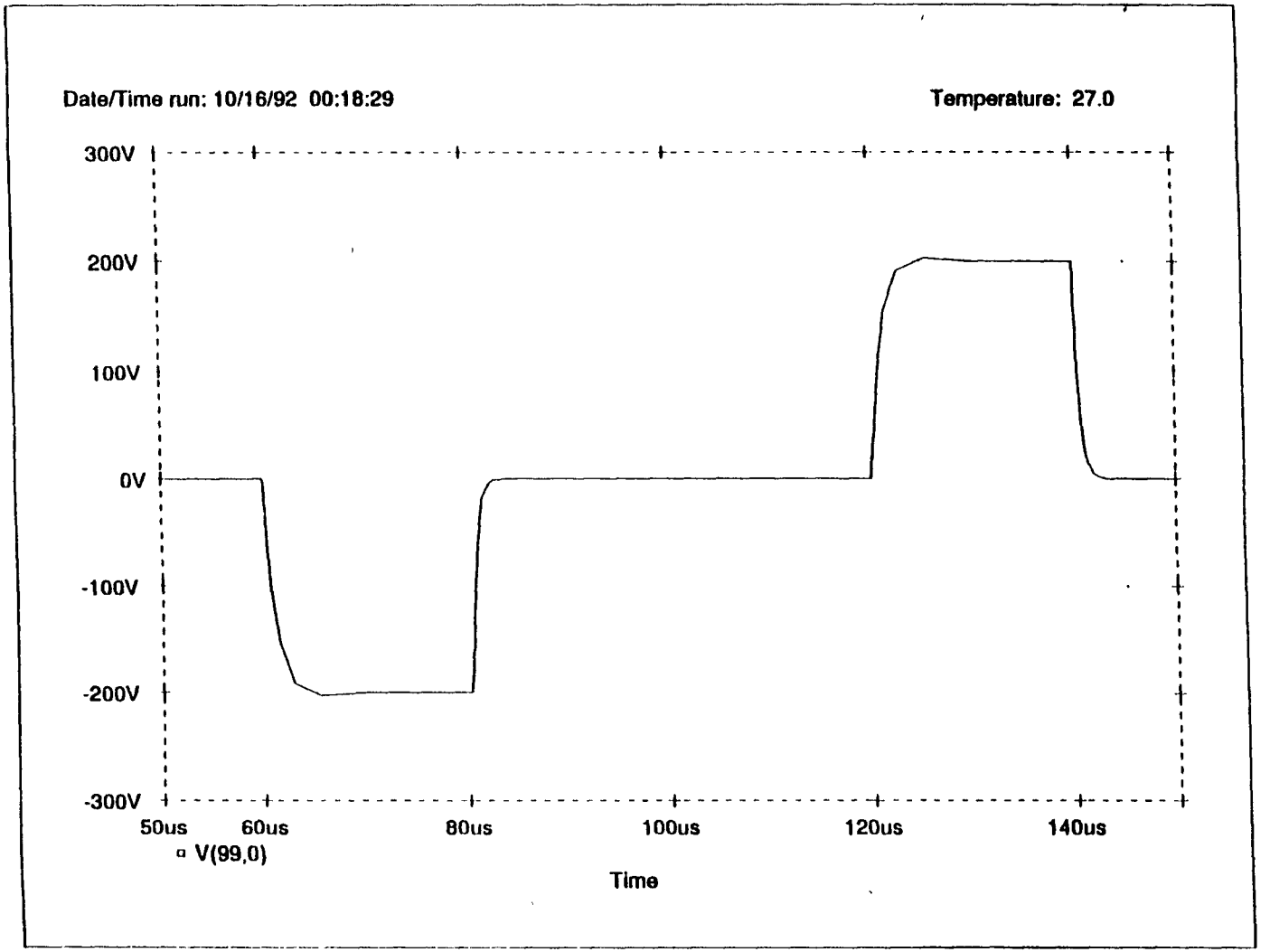


Figure 5.12(b) Close-up of the waveform in Figure 5 12(a).

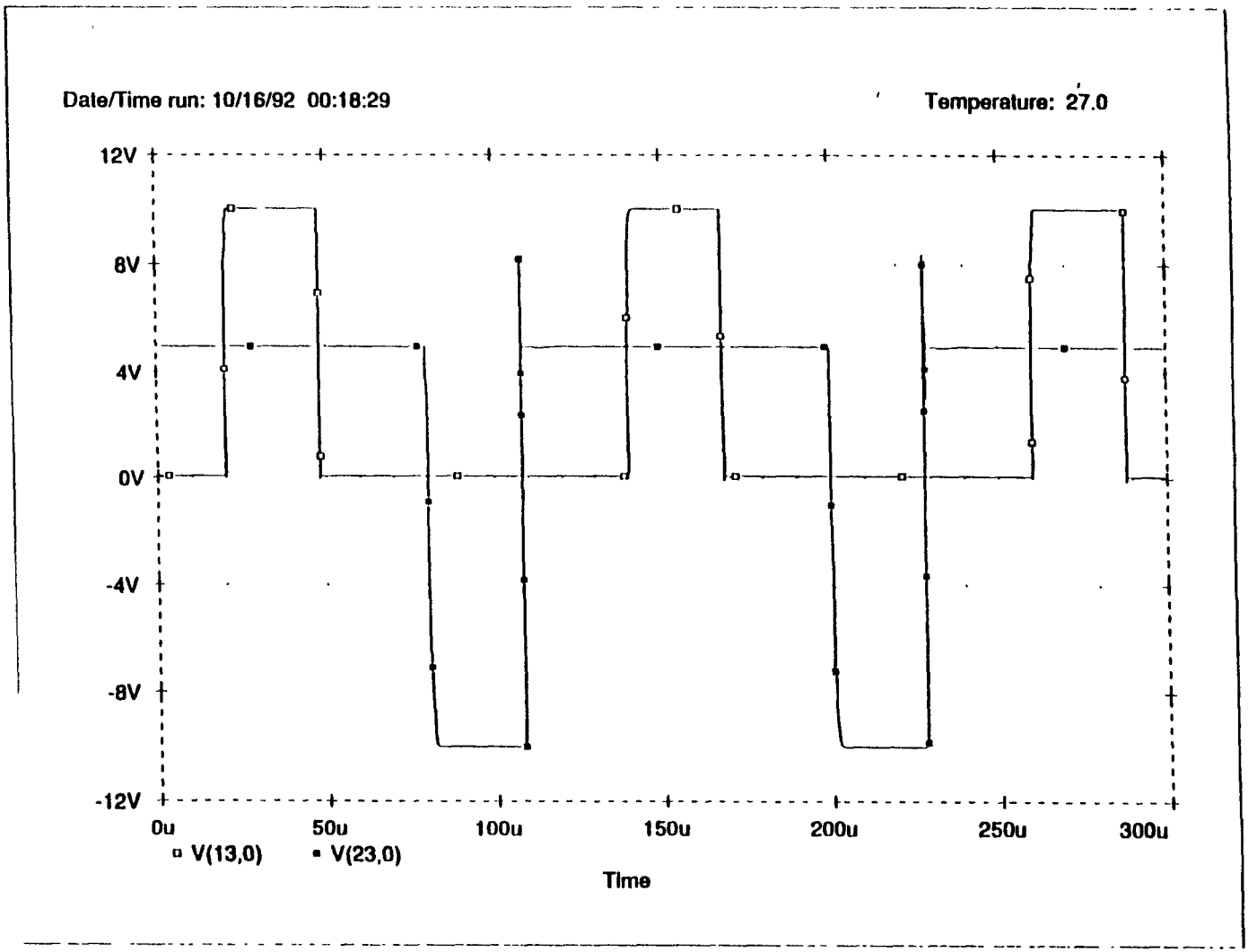


Figure 5.13 Waveforms of V@13 and V@23 of the high-voltage driver.
R101=R102=R103=R104=200Ω, Cout=200nF

CHAPTER 6

CIRCUIT IMPLEMENTATION

When we were designing this programmable integrated power supply for micromotor, we also started doing implementation of this circuit in the meantime for prelimianry testing and use, in the way of prototype construction using wire wrap technique, because the IC chip which I have designed needs to be fabricated by MOSIS and will not be obtained very soon. Both digital circuit and high-voltage drivers have been implemented on Plugbord prototyping boards.

6.1 Digital Prototype Construction

1 A sweep/function generator, BK PRECISION 3022 (0.2Hz~2MHz), has been used to provide square-wave clock pulse with manually controlled variable frequency, whose range is large enough for our requirement, 0 2Hz~30KHz.

2. A much simpler digital circuit has been used for prototype construction implementation It is actually a 12-bit Johnson counter, consisting of 6 DFFs with some decoding circuits. As shown in Figure 6 1, it provides 6 phase digital square-wave with exact non-overlapping pulses, and other additional digital pulses which are needed for active pull-up and -down to ground in the high-voltage drivers. It does not have variable duty-cycle control, anyway.

The digital circuit has been implemented on a Plugbord prototyping board using existing IC chips for all the flip flops and gates. The wire wrap technique has been used for circuit connection on back side of the board. Figure 6.2 is the photograph of the digital circuit on the Vector board.

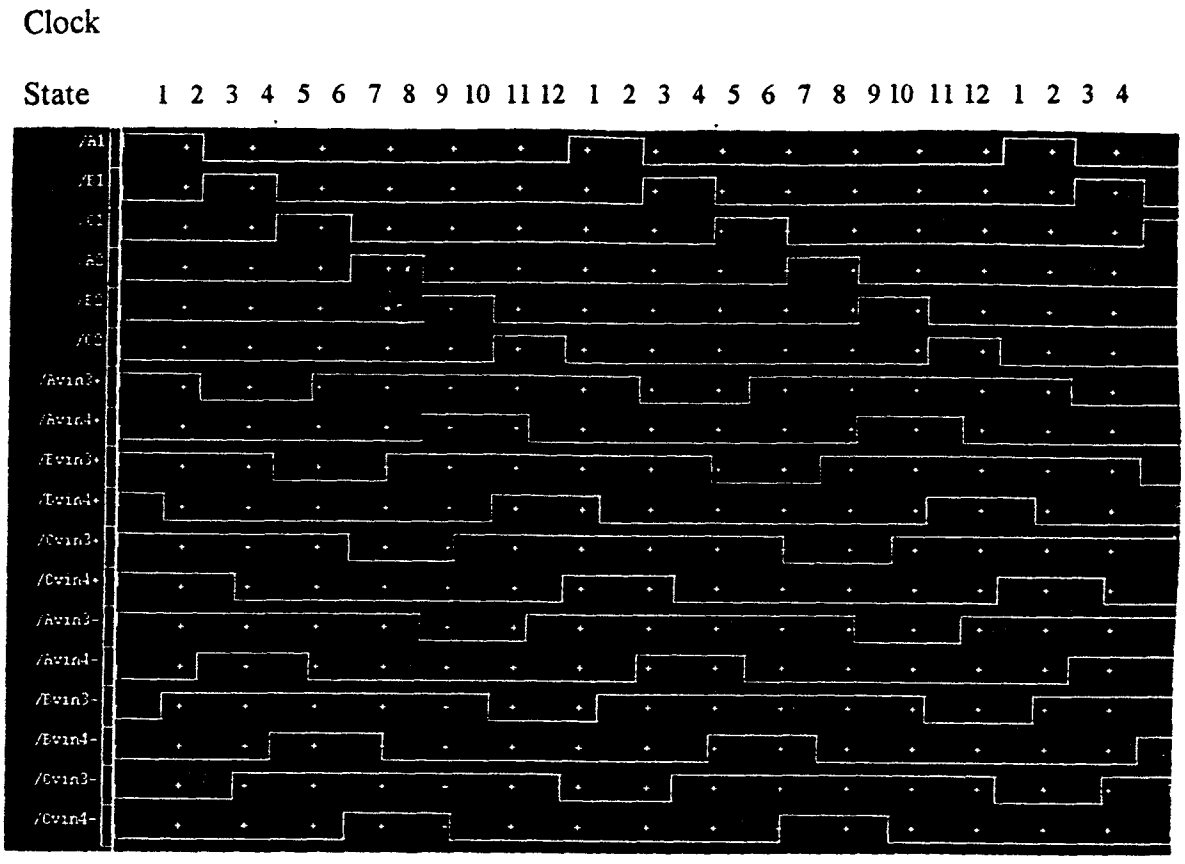


Figure 6.1 Waveform of 6-phase Digital Pulses output from the Simpler Digital Circuit

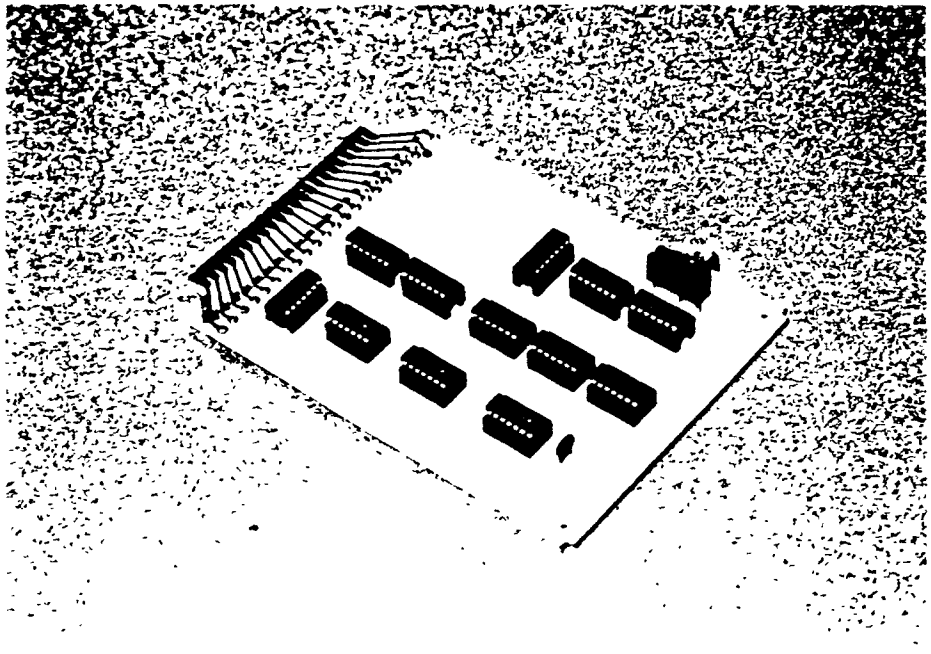


Figure 6.2 The Digital Circuit on a Vector Board

6.2 Analog Prototype Construction

1. For analog prototype construction, we use the exact same circuit structure of bipolarized high-voltage drivers as we have designed in Chapter 5, as shown in Figure 5.6 Each single driver is implemented on a Vector board, using discrete components, e.g., power Bipolars (MJE340, MJE350) and power MOSFET (MTP2N45, MTP2P45), and high-voltage diodes and power resistors, as shown in Figure 6.5. The wire-wrapping technique has also been used for circuit connection.

2. Two DC power, HP 6209B (0~320Volts, 0.1Amp), have been used, serially connected to provide "+VDD" -- "0V" -- "-VSS" construction, the "Positive--GND--Negative" voltage. VDD and VSS can be adjusted manually from 0V to higher than 200V.

3. To improve frequency response for the power transistor circuit, decoupling capacitors of 4 7μF are added both between VDD and GND, and between VSS and GND near each high-voltage input pin on each driver's board This helps a lot in this wirewrap circuit by increasing the frequency reponse by more than 80%.

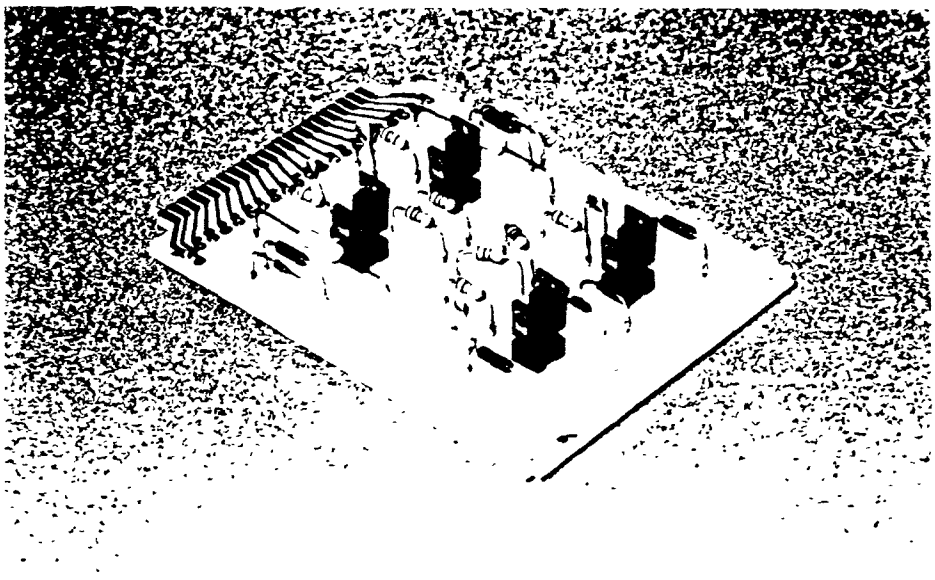


Figure 6.5 Photograph of a Single High-voltage Driver on a Vector Board

Finally, one digital circuit board and all six high-voltage drivers' boards have been assembled into a Vector card cage, with wire-wrap connection among all the boards on the backplane of contact edge connectors. Figure 6.6 shows the digital circuit board and six high-voltage drivers' boards. Figure 6.7 shows a photograph of entire power supply implemented on Vector boards in a Vector card cage.

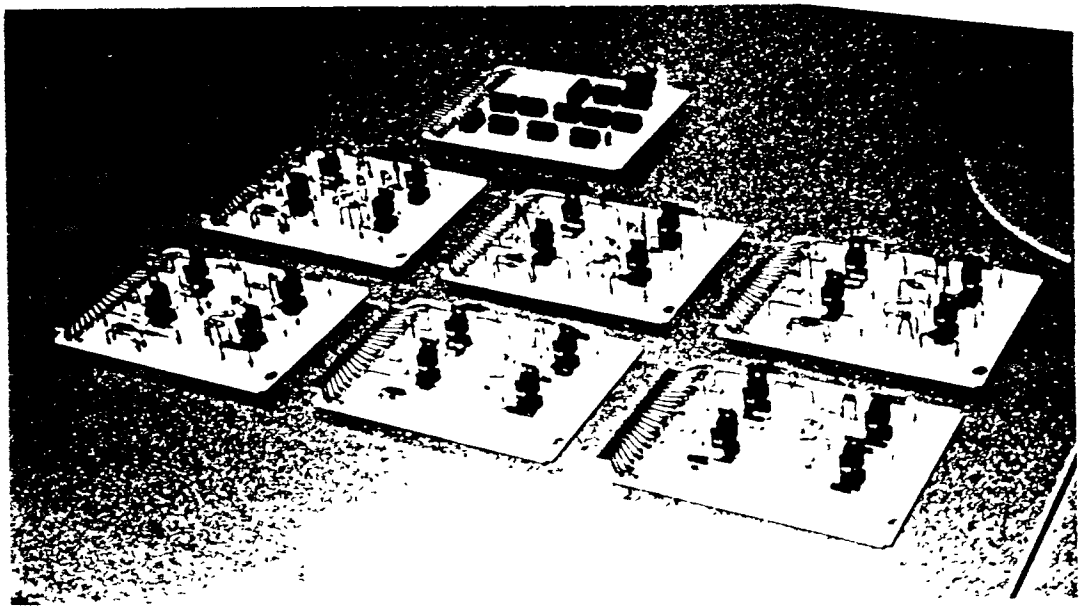


Figure 6.6 One digital board and six high-voltage driver boards

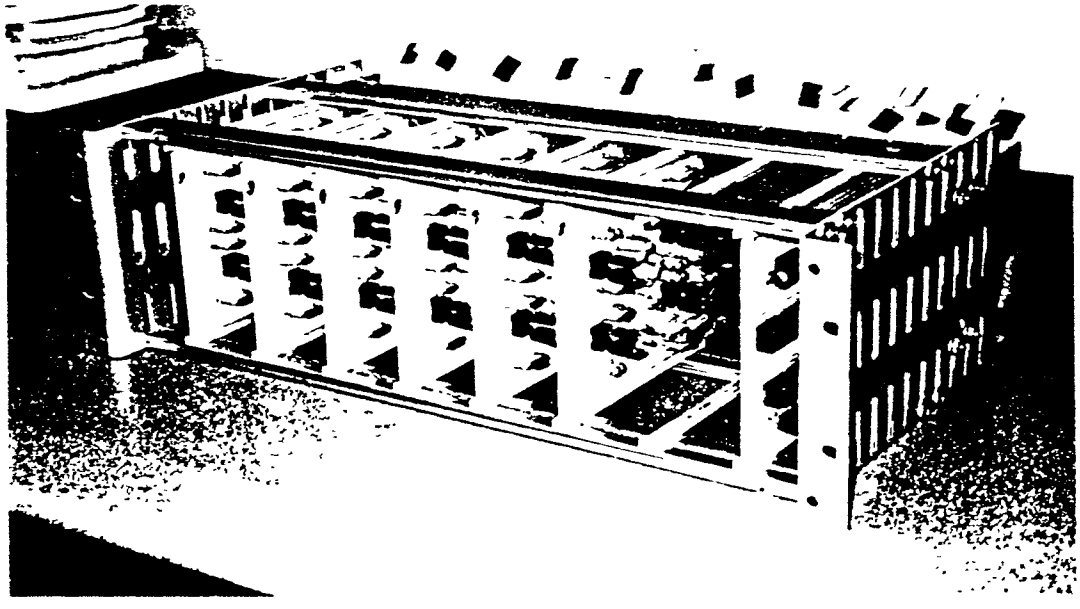


Figure 6.7 Entire Power Supply including Vector Boards and a Card Cage

6.3 Preliminary Testing of the Power Supply

A preliminary engineering acceptance testing has been done to observe the performance of the power supply we implemented. For each output phase, a capacitor load of around 10 ~ 20 NF is used, to simulate micromotor conditions. All the scope photographs have been taken using a DC source voltage of VDD=-VSS=100Volts.

1. The waveforms of bipolarized high-voltage pulses we observed from the oscilloscope have acceptable rectangular shapes, as shown in Figure 6.8 (for a single phase). With a capacitor load of around 20 NF for each output phase, the rising time of the pulse is about 1.5~2.0 μsec and falling time is about 2.0~3.0 μsec.

2. The output signal frequency can reach 40KHz and the signals are still stable, although at 40KHz the waveforms are no longer rectangular as in Figure 6 9 This maximum corresponds to a motor rotational speed of 200Krpm.

3. Illustrated in Figure 6.10, 6 11, 6 12, 6 13, are the waveforms of different output phases at various frquencies. Note that there exist a little overlapping between two adjacent phases (Figure 6 10), and a little non-matching between two opposite phases (Figure 6 11) The percentage of these overlapping or non-matching increases when the frequency is increased. When output frequency is lower than 2.5KHz, these overlapping and non-matching become around 6% ~ 8%, and will not affect the operation of micromotor very much. This is very desirable.

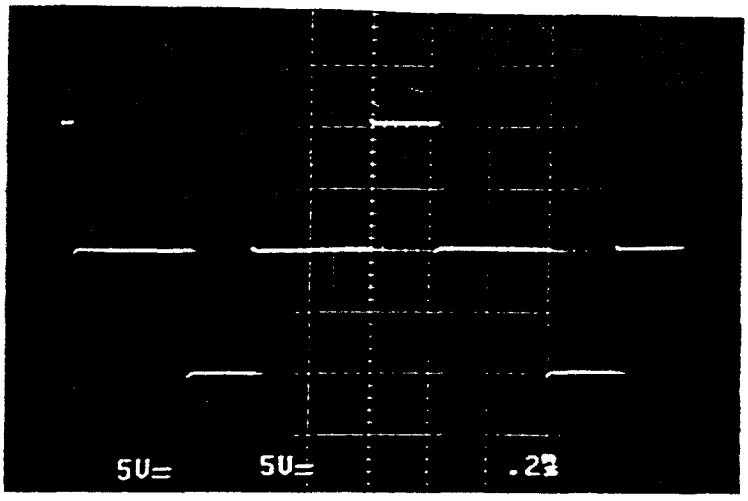
Waveform degradation at high frequency is due to the relatively large turn-off time of the power bipolar transistors in the circuit. The large turn-off time causes the relatively large delay of the pulse on its falling edge. Let's look at Figure 5.6 in Chapter 5. The rising edge from 0V to +VDD of the pulse corresponds to turn-on of Q1(NPN), and the rising edge from 0V to -VSS corresponds to turn-on of Q2(PNP). The falling edge of +200V →0V corresponds to turn-off of Q3(NPN) and Q1, and the falling edge of -200V to 0V

corresponds to turn-off of Q4(PNP) and Q2. Normally, the turn-off time is much larger than turn-on time. Therefore, the pulse width is experimentally larger

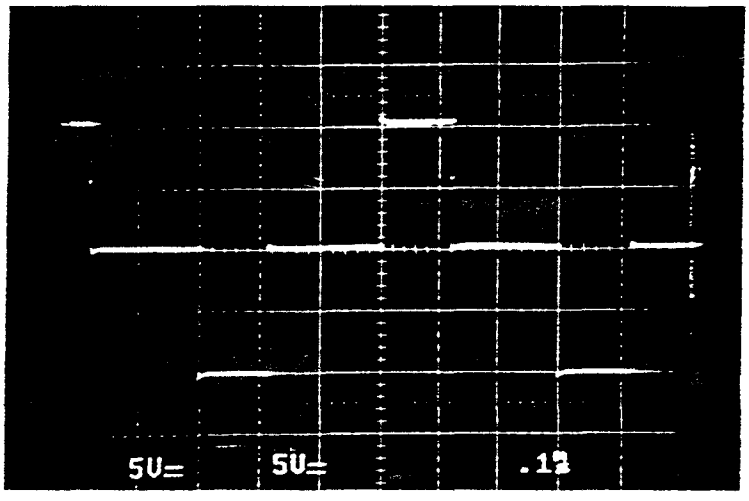
Also note that the extents of overlapping and non-matching, and actually the delays on the falling edge, vary from one phase to another (namely from one high-voltage driver to another), and from positive pulse to negative pulse of a single phase. Some drivers provide perfect output with only around 5μsec delays on the falling edge, and are very symmetrical on both positive and negative pulses, as shown in Figure 6.12. Some other drivers exhibit an output with 20~30μsec delays on the falling edges (Figure 6.8), and are unsymmetrical (Figure 6 10) This results from the internal charge stored in the base region of these transistors when they are driven into satuaration, which causes that the transient characteristics and parameters of the power transistors vary from one to another, and from NPN to PNP. By selecting transistors or designing with higher frequency transistors, the high frequency performance can be improved.

4. Power dissipation of the entire circuit can be obtained by measuring the output voltage and current of two DC power source which are being used The result is shown in Table 6.1 and 6 2. Figure 6 15 and 6 17 show the total power dissipation changing with clock frequency and DC power voltage, respectively. With different values of the load capacitor and even unloaded, almost the same result of power dissipation has been obtained, which means, the power dissipation are not on the load capacitor, but mainly on the power resistors (R22 and R44 in Figure 5.6).

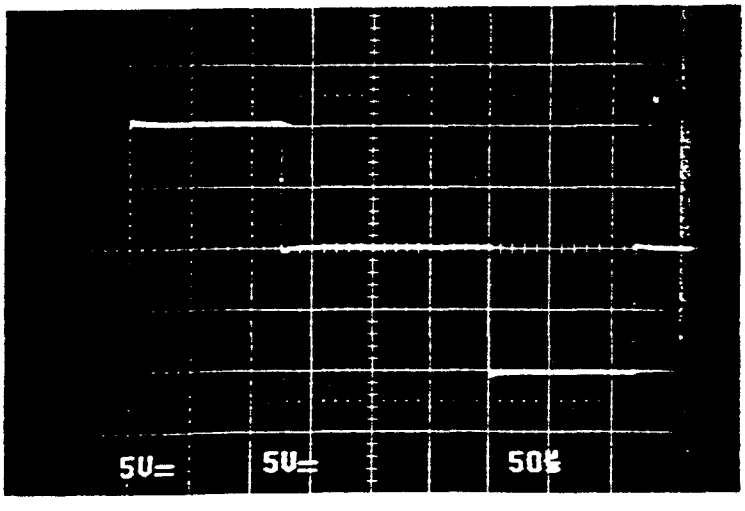
The increment of the total power dissipation with the clock frequency also reveals the overlapping existing between each two adjacent phases. The percentage of this overlapping increases when clock frequency increases.



(a) Output f=5KHz.
(50 Volts/Division
0.2 msec/Division)

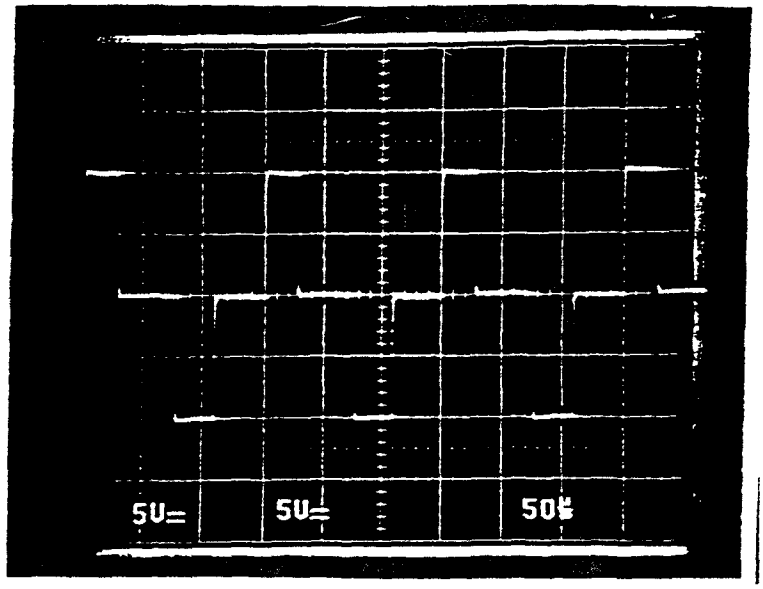


(b) Output f=10KHz.
Obvious delay
on the falling edge.
(50 Volts/Division
0.1 msec/Division)



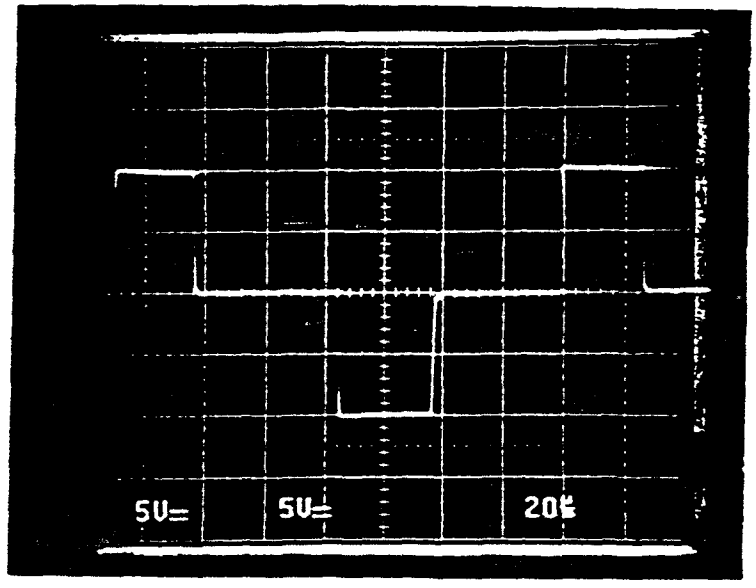
(c) Output f=10KHz.
Close-up of (b).
(50 Volts/Division
50 μsec/Division)

Figure 6.8 Single phase of a high-voltage bipolarized power supply with rectangular waveform.



(a)

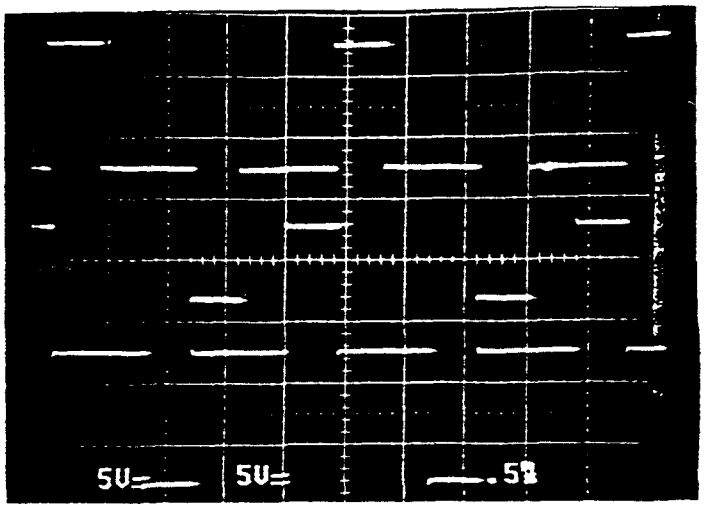
(50 Volts/Division
50 µsec/Division)



(b)

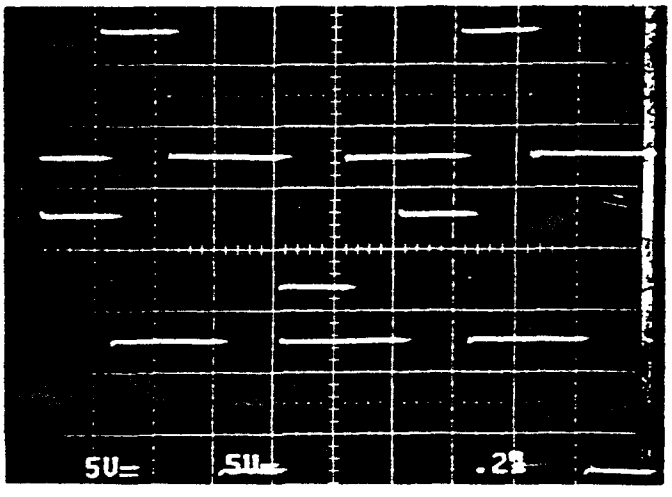
(50 Volts/Division
20 µsec/Division)

Figure 6.9 One phase waveform at output frequency=40KHz.
(b) is a close-up of (a).



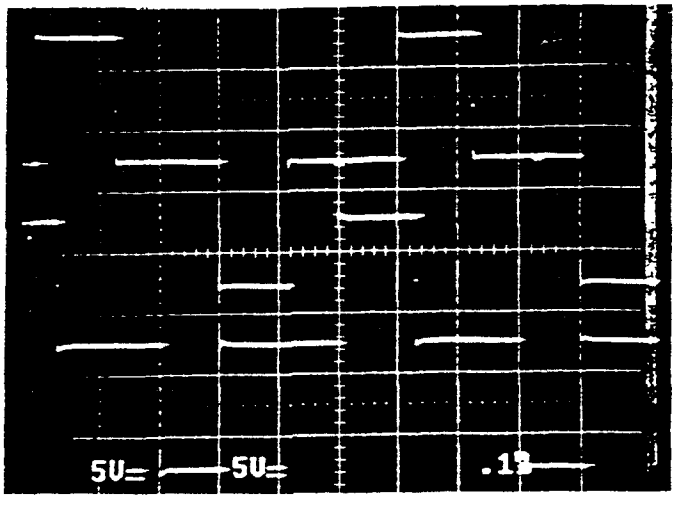
(a) Output f=2.5KHz. Overlapping due to the delay can be ignored.

(50 Volts/Division
0.5 msec/Division)



(b) Output f=5KHz. Overlapping can be observed.

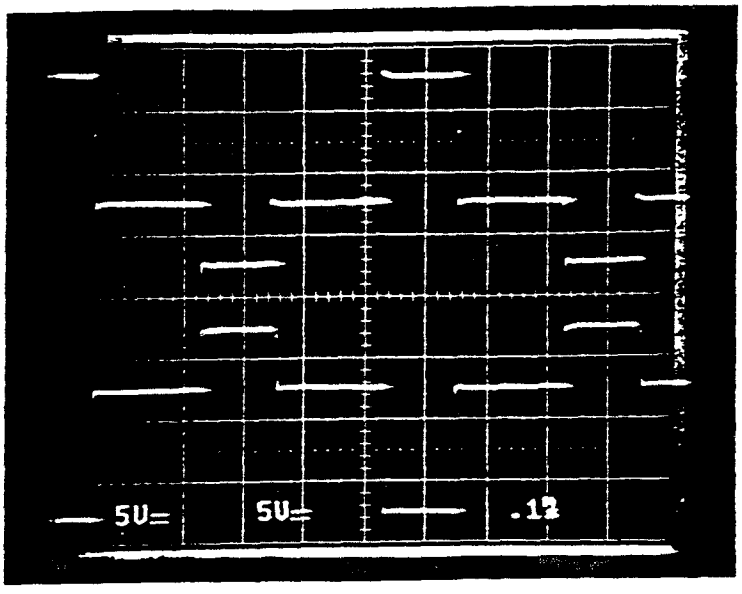
(50 Volts/Division
0.2 msec/Division)



(c) Output f=10KHz. Overlapping due to the delay is considerable.

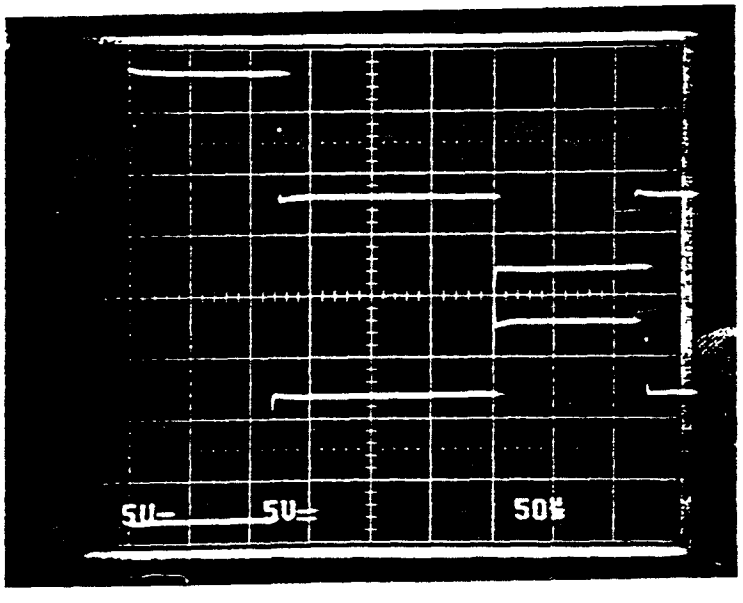
(50 Volts/Division
0.1 msec/Division)

Figure 6.10 Two adjacent phases at different frequencies, e.g. (A+, B+).



(a)

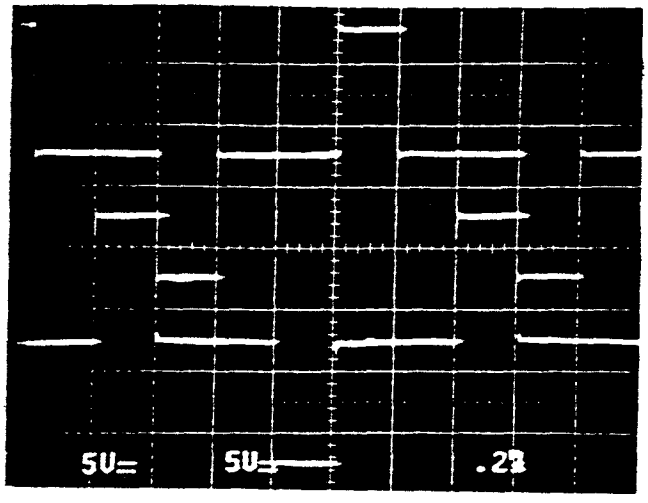
(50 Volts/Division
0.1 msec/Division)



(b)

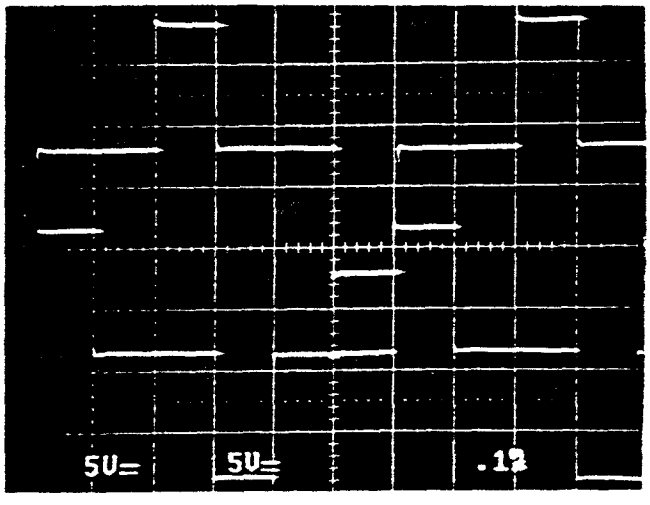
(50 Volts/Division
50 μsec/Division)

Figure 6.11 (a) Two opposite phases, e g., (A+, A-) at output f=10KHz.
(b) Close-up of (a); non-matching is observed due to different delay of each phase.



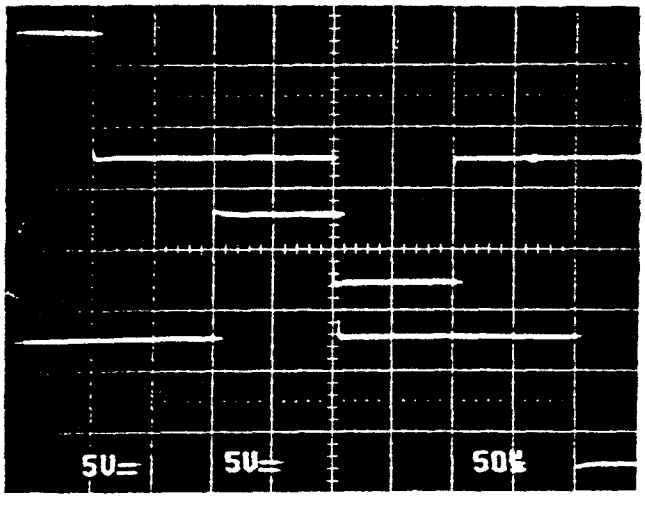
(a) Output f=5KHz: No delay or overlapping between two phases can be observed.

(50 Volts/Division
0.2 msec/Division)



(b) Output f=10KHz: Almost no delay or overlapping between two phases can be observed.

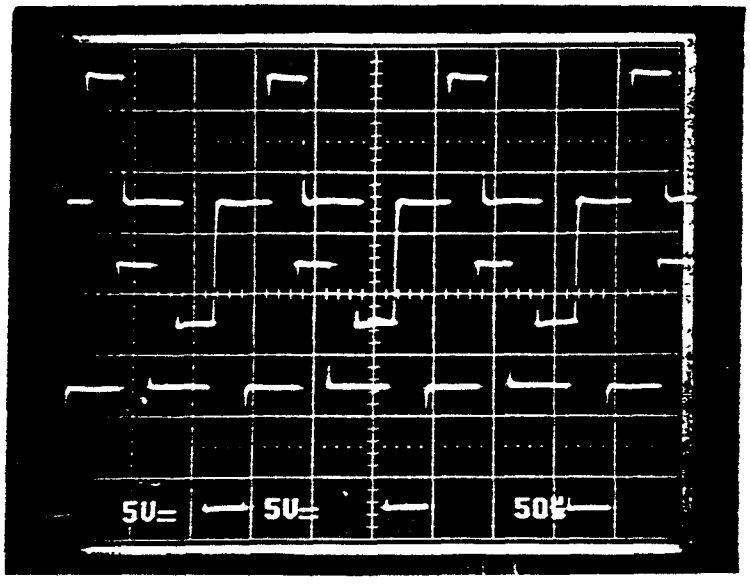
(50 Volts/Division
0.1 msec/Division)



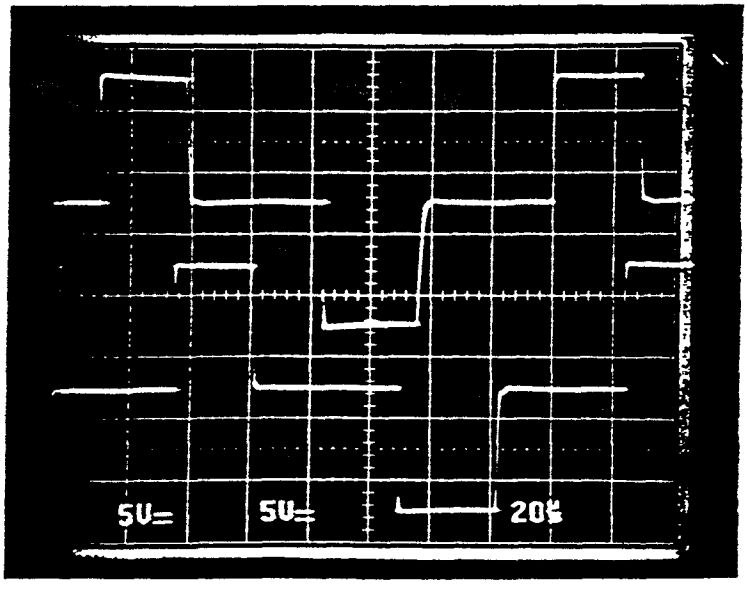
(c) Output f=10KHz: close-up of (b). Overlapping and delay can be observed, but are very little.

(50 Volts/Division
50 μsec/Division)

Figure 6.12 Two adjacent phases of selected drivers showing minimum fall-time waveforms.



(50 Volts/Division
50 µsec/Division)



(50 Volts/Division
20 µsec/Division)

Figure 6.13 Two adjacent phases (A+ and B+) at output frequency=40KHz; Overlapping and unsymmetrical phases become more apparent at high frequency.

Table 6.1 Total Power Dissipation at Different Clock Frequency

With Capacitive Load = 20 NF (All Six Phases)			
	VDD = -VSS = 120Volts		
Clock Frequency (KHz)	Current I(+) (mA)	Current I(-) (mA)	Power Dissipatrion (Watts)
20.0	32	30	7.44
15.0	31.5	30	7.38
10.0	30	29	7.08
5.0	29	28	6.84
2.0	28	28	6.72

Table 6.2 Total Power Dissipation at Different DC Power Voltage

With Capacitive Load = 20 NF (All Six Phases) Clock Frequency = 10.0 KHz			
VDD = -VSS (Volts)	Current I(+) (mA)	Currrent I(-) (mA)	Power Dissipation (Watts)
200	45	40	17.00
180	42	38	14 40
160	38	36	11.84
140	33.5	33	9.31
120	29.5	29.5	7.08
100	27	27	5.40
80	22	22	3.52
60	17.5	17.5	2.10
40	11.2	11.4	0.904
20	5.6	5 5	0.222

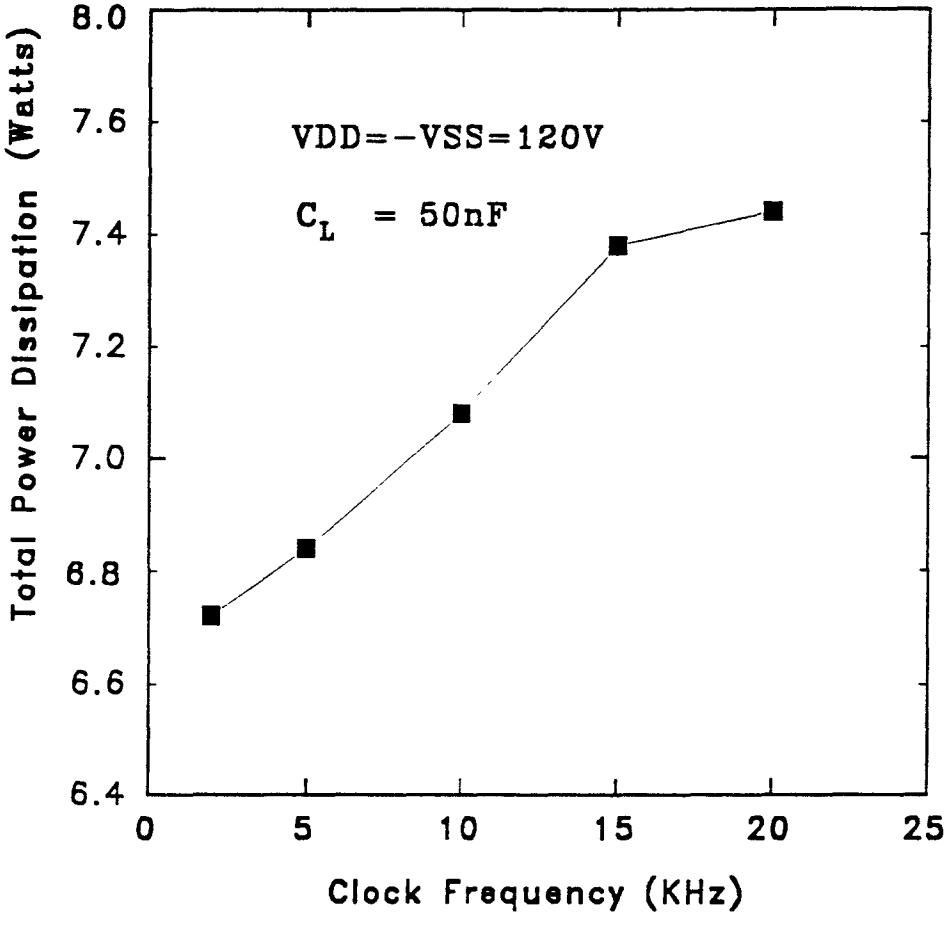


Figure 6.14 Total power dissipation vs. clock frequency

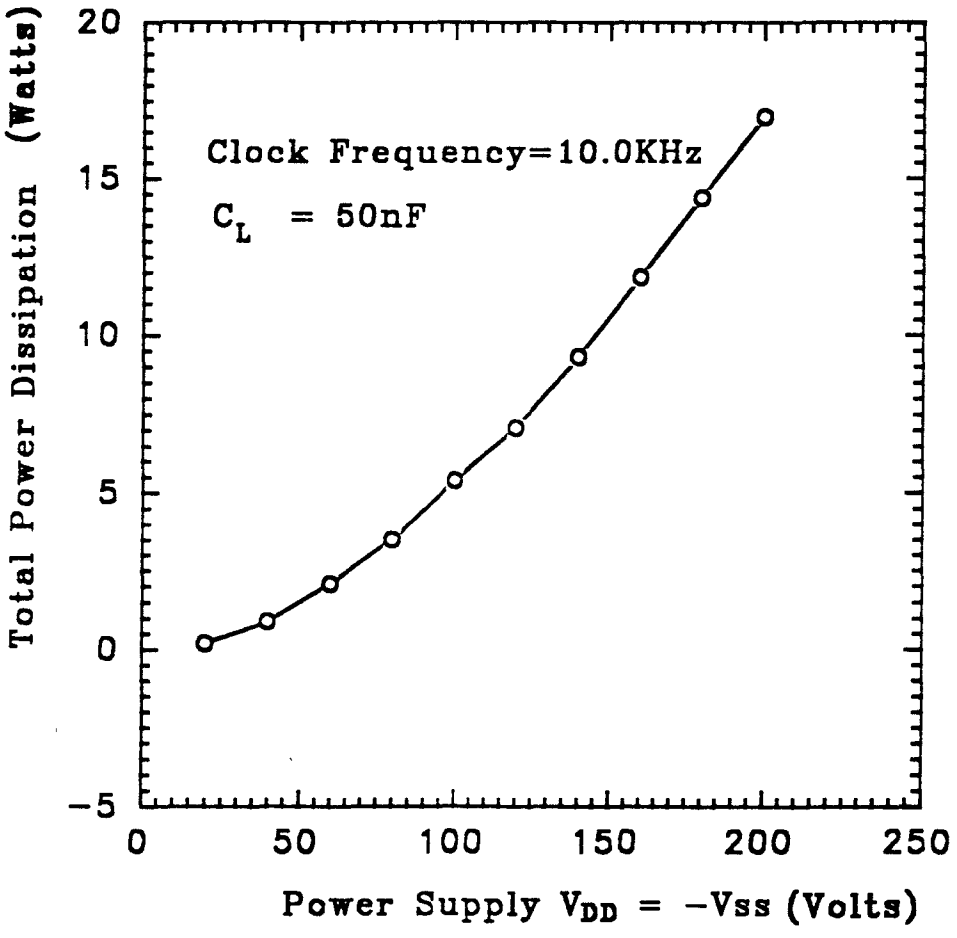


Figure 6.15 Total power dissipation vs. DC power supply voltage.

6.4 Further Discussion and Improvement

From the result of preliminary testing of the power supply, a few unsatisfactory performances have been found out in the high-voltage drivers. The following are some suggestions for improvement.

1. Test every power bipolar transistor using Curve Tracer, to find out those which have good and symmetrical transient characteristics for both NPN and PNP types, and select and use them in our circuit.

2. In the circuit of Figure 5.6, for Q3(NPN) and Q4(PNP), instead of using power transistors which are actually not necessary, use normal bipolar transitors which have much better transient characteristics.

3. In the circuit of Figure 5 6, use higher value of resitors for R22 and R44 (and also R2 and R4, correspondingly), e g., choosing R22=R44=8K (also R2=R4=4K, correspondingly), to decrease the I_{ce} current when Q1 and Q2 are turned on. And therefore to reduce the total power dissipation However, this modification should be done without affecting seriously the transient characteristics of the high-voltage driver.

CHAPTER 7

SUMMARY AND CONCLUSIONS

To study the special operational characteristics of various electrostatic-drive micromotor, basically the variable-capacitance side-drive micromotor, a 6-phase bipolarized, high-voltage power supply with rectangular pulse shape, with variable frequency and voltage, and variable duty-cycle control has been designed. Simulation has been done to prove the correctness.

The bipolarization of each pair of the phases has been designed and achieved to overcome, or reduce the serious problem of physical clamping of the rotor to the electrical shield beneath it caused by poor electrical contact between these two.

The output signal frequency range varying from 1Hz to 40KHz has been achieved. This frequency range corresponds to motor rotational speed range of 5rpm to 200Krpm, for a micromotor of stator : rotor = 12:8 (3:2 architecture). The voltage amplitudes of all six phases can be varied together as a group from +20 to +200Volt and from -20 to -200Volts.

The duty-cycle of each phase can be changed together at a fixed frequency. The output with variable duty-cycle has been obtained, changing from one-half non-overlapping to one-third overlapping.

A power supply of 6-phase bipolarized output with variable frequency and variable high voltage has been implemented on the vector prototyping boards, assembled in a vector card cage, using the wire-wrapping technique. Preliminary testing of the power supply has been performed, coming out with satisfactory output waveforms. Suggestion has been given on how to improve the high frequency characteristics of the circuit.

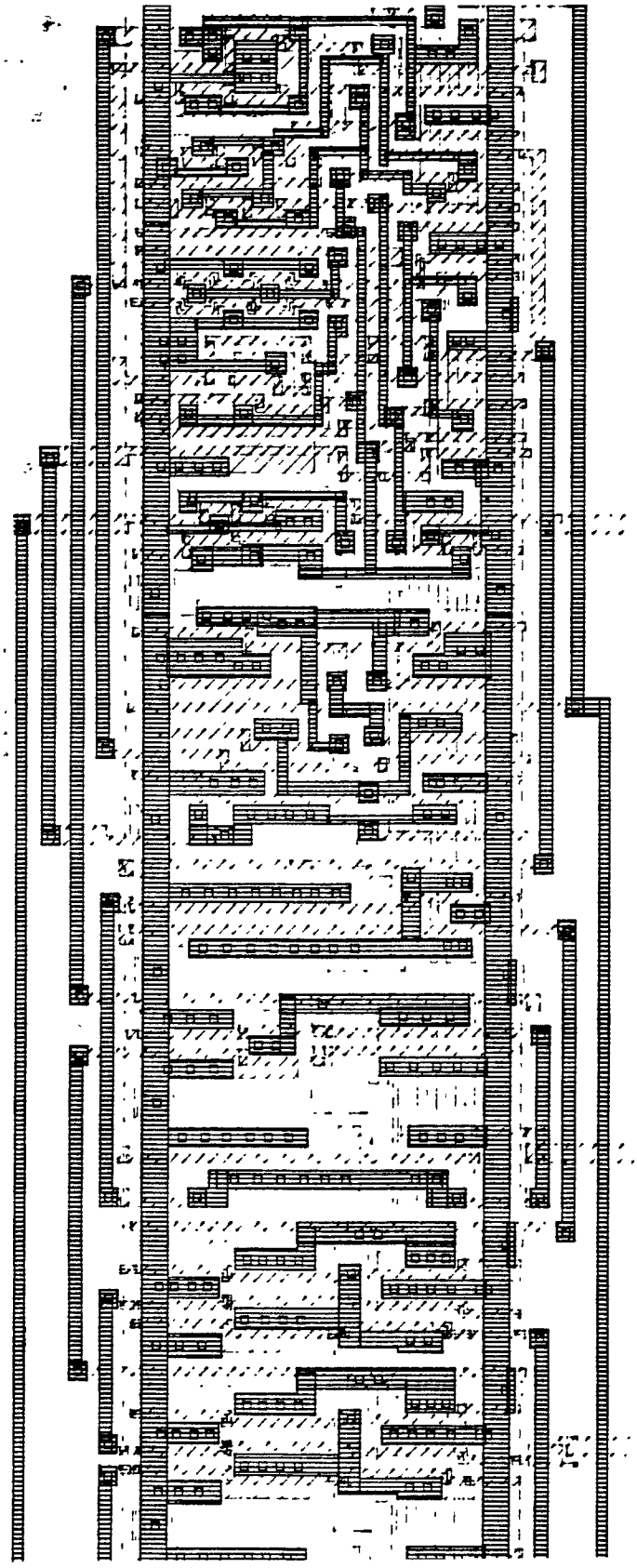
APPENDICES

A. PSPICE Input File for Simulation of a Single High-voltage Bipolarized Driver

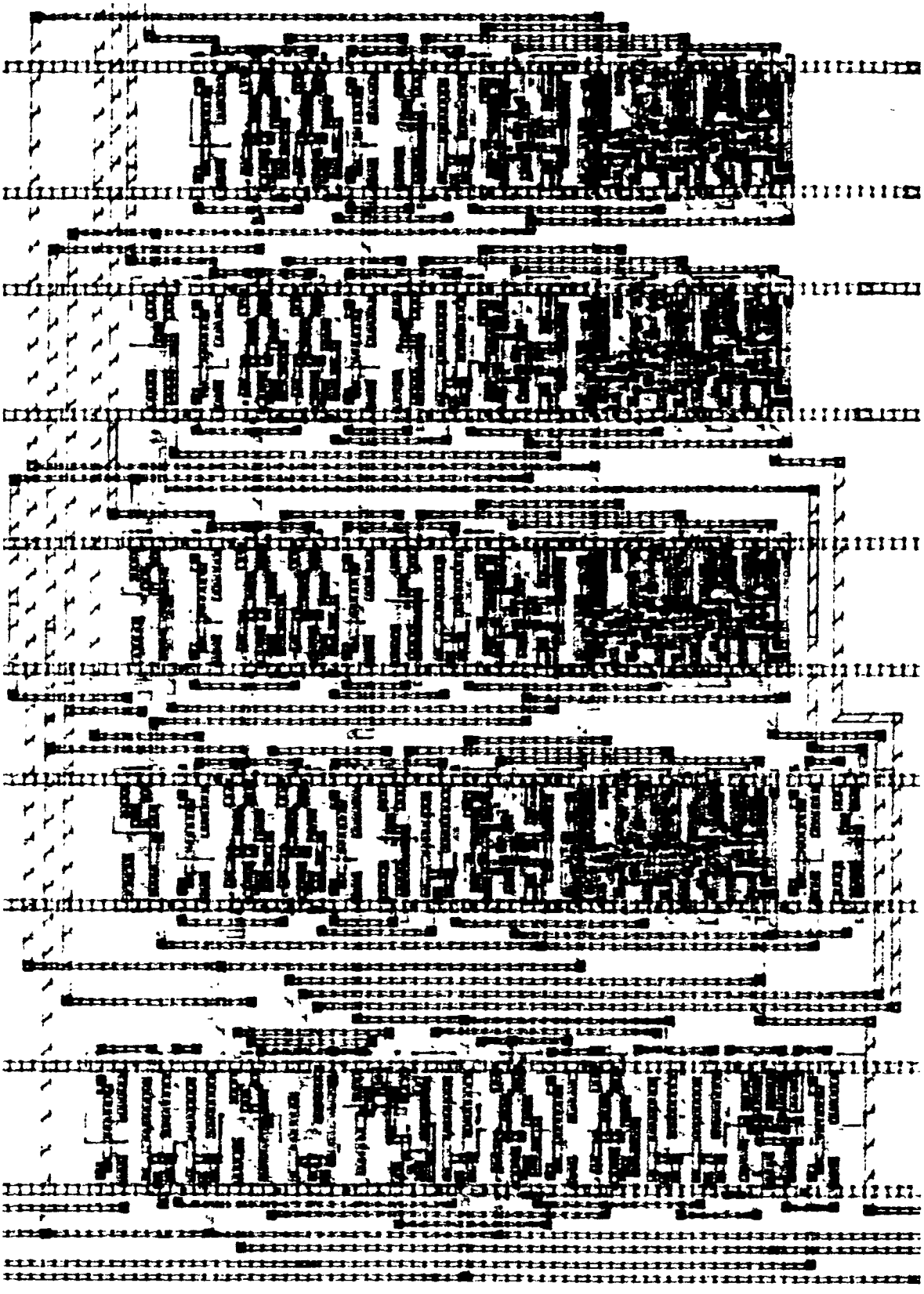
```
*POWER SUPPLY FOR U-MOTOR: NEW VERSION
VDD1  1   0   200v
VSS1  2   0   -200v
VDD2  14  0   10v
VSS2  24  0   -10v
VREF1   8  0   5v
*  VREF2   26 0   5V
Q1    105   4   0   MJE340
.LIB  MYPARTS.LIB
Q2    109   7   8   MJE350
.LIB  MYPARTS.LIB
Q3    13    12  0   MJE340
.LIB  MYPARTS.LIB
Q4    23    22  8   MJE350
.LIB  MYPARTS.LIB
M1    96  5   1  1    MTP2P45
.LIB  MYPARTS.LIB
M2    95  9   2  2    MTP2N45
.LIB  MYPARTS.LIB
M3    15  13  0  0    MTP2N45
.LIB  MYPARTS.LIB
M4    25  23  0  0    MTP2P45
.LIB  MYPARTS.LIB
D1    98  15  DIODE1
D2    25  97  DIODE1
R1    3   4   10K
C1    3   4   200PF
R2    105   5   4.7K
R22    5    1   4.7K
S1    1    5    1    5    SZENOR
R3    6   7   10K
C3    6   7   200PF
R4    9   109   4.7K
R44   2    9    4.7K
S2    9    2    9    2    SZENOR
R5    11  12   5K
C5    11  12   150PF
R6    14  13   4.7K
R7    21  22   5K
C7    21  22   150PF
R8    23  24  4.7K
R102  96  98  40
R101  98  99  40
R103  97  99  40
R104  95  97  40
COUT    99  0   50000P
**
**.MODEL NPN1 NPN  BF=120  IS=1.0E-10
**.MODEL PNP1 PNP  BF=100  IS=1.0E-10
**.MODEL NMOS1  NMOS ( VTO=2.0V  LEVEL=2  KP=20.0E-6  W=32000U L=4U )
**.MODEL PMOS1  PMOS ( VTO=-2.0V  LEVEL=2  KP=10.0E-6 W=64000U L=4U )
.MODEL DIODE1  D ( BV=500V  IS=1.0E-10  RS=0.01   CJO=5P )
.MODEL  SZENOR  VSWITCH  VON=10.1V  VOFF=9.9V  RON=0.1  ROFF=100MEG
**
VIN1   3  0  PULSE ( 0  5V  0US  0.01US 0.01US 19.98US 120US )
VIN2   6  0  PULSE ( 5V  0  60US  0.01US 0.01US 19.98US 120US )
VIN3  11  0  PULSE ( 5V   0  20US   0.01US  0.01US  39.98US  120US )
VIN4  21  0  PULSE ( 0   5V  80US   0.01US  0.01US  39.98US  120US )
**
```

```
.TRAN  2US  300US
.PLOT TRAN   V(13,0)
.PLOT TRAN   V(23,0)
.PLOT TRAN V(99,0)
.WIDTH OUT=80
.OPTION RELTOL=0.01 ITL4=40  VNTOL=1MV  ABSTOL=10NA
.OPTION  ITL5=0 LIMPTS=100000
.PROBE  V(3,0) V(6,0) V(11,0) V(21,0)
.PROBE  V(99,0)  V(13,0) V(23,0)
.END
```

B.(1) A Portion of the IC Layout - The Special "T" Flip Flop:



B.(2) A Portion of The IC Layout - The Presettable Divide-by-N Down Counter:



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