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ABSTRACT

Linear CCD Motion Detection System

by

Thekepat J. Sudesh

The mechanical response to electrical stimuli of the human membrane represents an important area of research in medicine. A linear sensing system was designed and fabricated to measure the displacements (along a specified direction) and the frequency response of a ear membrane, the Outer Hair Cell (OHC). The output of this system was a voltage proportional to the instantaneous position of the bimorph and could be displayed on an oscilloscope.

The system consisted of optics to project the image of the vibrating membrane onto a Linear CCD Camera and electronic analog and digital circuitry which produced an instantaneous voltage proportional to the position of the edge of the OHC. It was designed to observe opaque and partially transparent objects and even objects with completely transparent holes at various locations.

The system was successfully tested with a CCD clock rate of 2.5Mhz, using an opaque object at five fixed object locations. Object frequencies of 1Khz and spatial resolution of 14μm, are within the capability of the designed system. With higher speed circuitry, object movements up to 15Khz can be measured.

LINEAR CCD MOTION DETECTION SYSTEM

by
Thekepat J. Sudesh

A Thesis
Submitted to the Faculty of
New Jersey Institute of Technology
in Partial Fulfillment of the Requirements for the Degree of
Master of Science in Electrical Engineering

Department of Electrical and Computer Engineering

October 1993

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Linear CCD Motion Detection System

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This thesis is dedicated to my wife, Ajitha.

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CHAPTER 1

INTRODUCTION

1.1 Introduction

The purpose of this research was to develop a linear imaging system to measure and study the displacement of the outer hair cell (OHC) in response to electrical stimuli. The designed system had to be capable of measuring displacements along one dimension with a resolution of 20μm and with a frequency of displacement as high as 1000Hz. The CCD image sensor array can meet the 20μm resolution requirement because the distance between adjacent pixels can be of the order of 10μm. Images can be sensed at rates corresponding roughly to the clock frequency divided by the pixel elements in the array. Clock frequencies can be as high as 30Mhz. Thus array widths, for example 1024 pixels could measure displacement frequencies up to 30Khz. Therefore CCD image sensors are ideally suited for OHC displacement measurements.

The study of the mechanical response to electrical stimuli of the inner ear membrane and vice versa has become an important area of research in medicine. One such pioneer in this field is Dr. Joseph Santos - Sacchi at the laboratory of Otolaryngology, Yale School of Medicine. The imaging system developed in this thesis work was done to facilitate his research.

The object whose frequency of motion was measured using the designed imaging system was the bimorph, a cylindrically shaped artificial equivalent of the OHC which is opaque throughout except for several possible translucent regions that are between 30 and 150 microns long. It responds to electrical stimuli by contracting or expanding its shape, depending on the piezoelectric stimuli given to it. The bimorph isdesigned imaging system was the bimorph, a cylindrical shaped artificial equivalent of the OHC which is opaque throughout except for several possible translucent regions that are between 30 and 150 microns long. It responds to electrical stimuli by contracting or

expanding its shape, depending on the piezoelectric stimuli given to it. The bimorph is easier to work with than the OHC and was used in all experiments for evaluation of the performance of the developed position sensor due to economical and practical considerations. The OHC is an oblong shaped object which is translucent to a higher degree than the bimorph and is an actual biological part in the inner ear of mammals, used to couple the vibrations from the outer ear to the Auditory nerve.

The photon to current method of measuring displacements was developed by Dr. J. Santos (5). This method employed relatively large area photodiodes to measure the hair displacement. It consisted of four photodiodes positioned under the outer edge of the hair cells as shown in Fig 1.1(a). The photodiodes are electrically connected to the positive and negative terminals of an op amp. as shown in Fig 1.1(b). The voltage output of the high gain differential op amp depends on the position of the outer edge of the hair. The transfer characteristic of the system output versus cell position is shown in Fig 1.1(c). This approach had the following disadvantages:

1) The image of the OHC had to be aligned so that the top photodiodes were covered only partially by the cell as shown in Fig 1.1(a). This required a video camera to be included in the experimental setup and also required precise mechanical adjustment of the hair cell relative to the photodiodes.

2) The frequency response was limited by the low sensitivity of large capacitance photodiodes. As illustrated in Fig 1.1(c), as long as the edge of the OHC falls between the positions X_{min} and X_{max}, the op amp would have an output voltage, which would depend on the position of the edge of the OHC, as illustrated by the transfer Curve. Thus the spatial range is limited to the distance between X_{min} and X_{max}. Thus relatively large capacitances of the photodiodes are required that convert the light incident on the device to instantaneous voltage. The photodiode approach does not integrate the detected charge as does the CCD pixel system and does not have the sensitivity of the CCD image sensor with

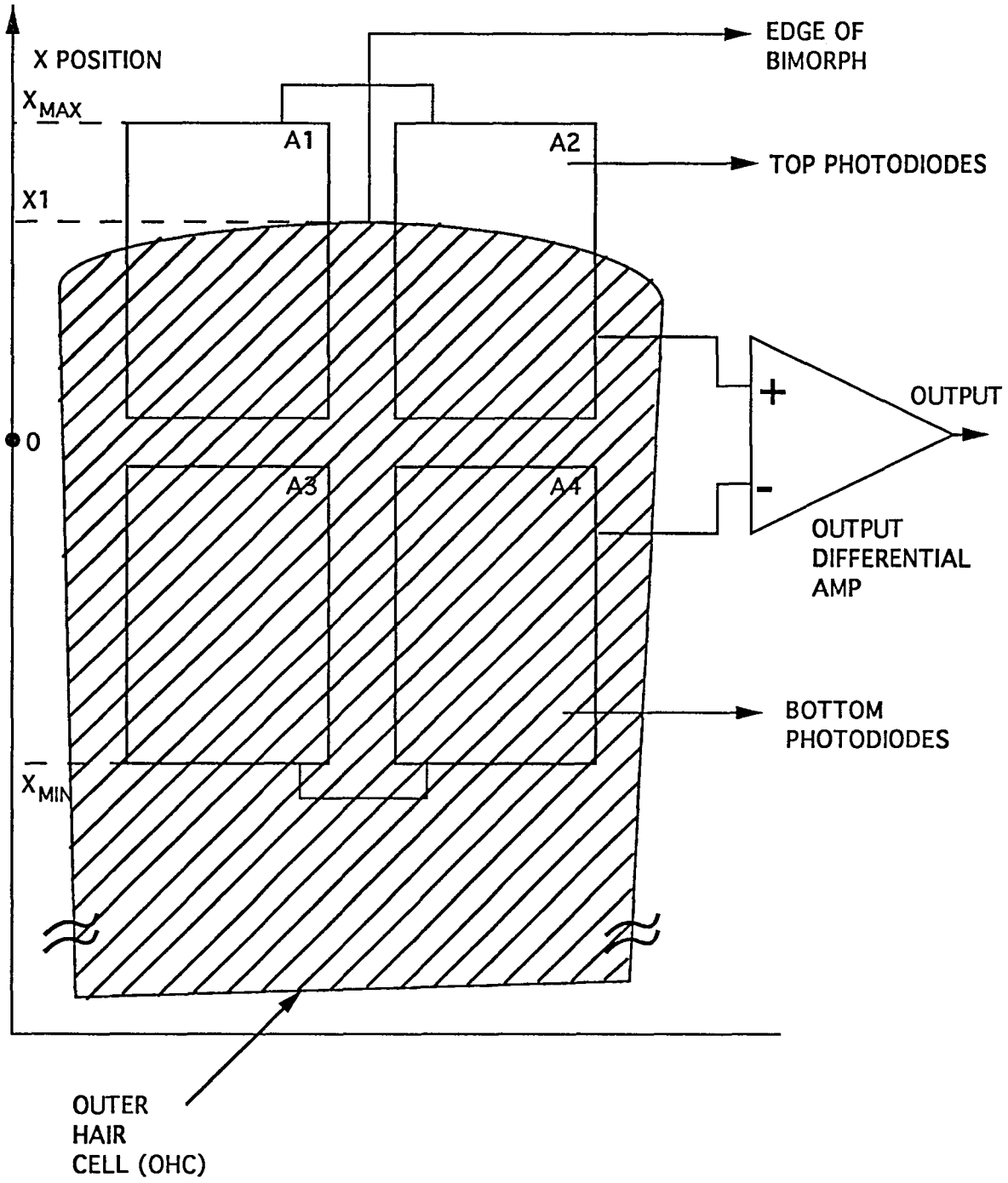


Fig 1.1(a) THE QUAD PHOTO-ELEMENT SYSTEM

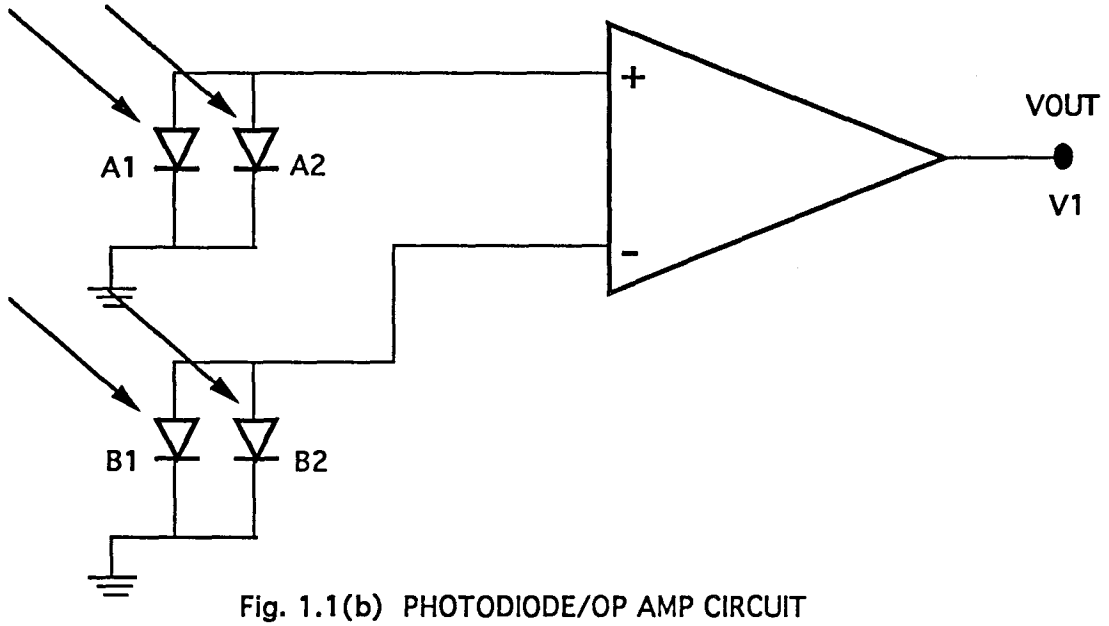


Fig. 1.1(b) PHOTODIODE/OP AMP CIRCUIT

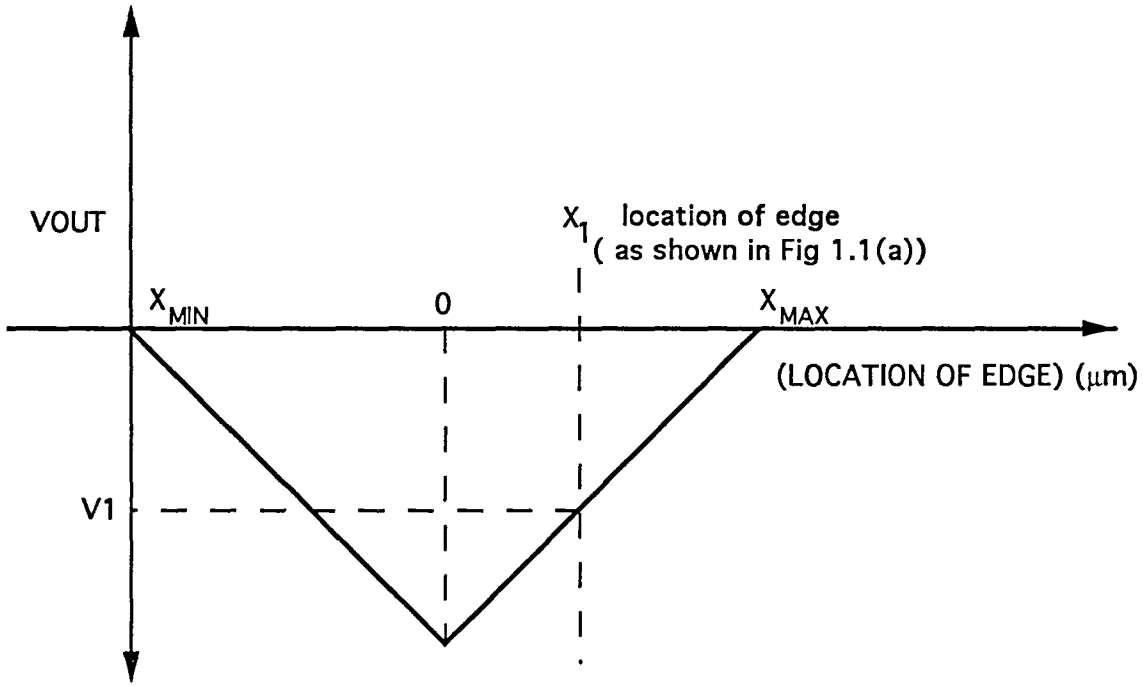


Fig 1.1(c) VOLTAGE TRANSFER CURVE

very small capacitance. An introductory discussion of CCD image sensors is given in the second chapter.

Figure 1.2 illustrates the sensing of the edge of an object by a linear CCD image sensor. The sensor output voltage is proportional to the light intensity falling on the image sensor of the camera. The opaque part of the object reduces the light intensity, while the intensity increases at the edge of the cell. At this edge the signal rises rather abruptly to V_{MAX}. The sharpness of the rise is limited by the diffraction effect only if the opaqueness of the cell is uniform throughout its length. The voltage V_{MIN} is due to any light on the sensor through the opaque part of the object. It would be zero if the cell is not partially transparent. This signal, SENSOR VIDEO OUTPUT, represents the waveform corresponding to one line scan.

The thesis has been organized as follows: Chapter 2 presents a review of CCD optical sensors. Chapter 3 gives the overview of circuit description. Chapters 4 through 10 describe the various circuits of the designed motion detector. Chapter 11 presents the experimental results. The twelfth chapter gives the discussion of the experimental results and presents conclusions.

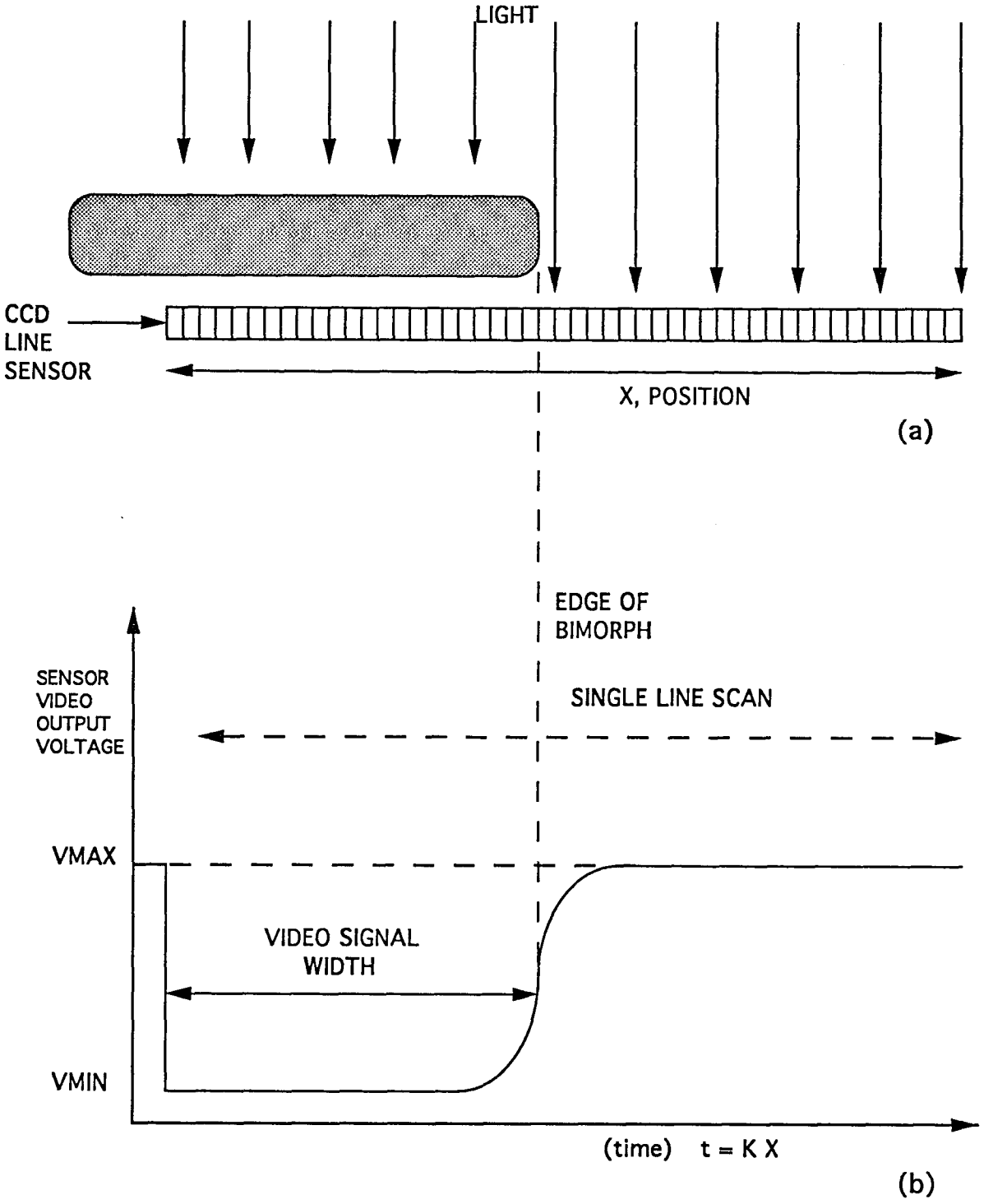


Fig 1.2 SENSING THE EDGE OF HAIR CELL BY A LINEAR CCD IMAGER
(a) SKETCH OF THE SYSTEM
(b) DEPENDENCE OF THE CCD SENSOR OUTPUT ON CELL POSITION

CHAPTER 2

REVIEW OF CCD OPTICAL SENSORS

A CCD optical sensor array can be best described as a series of parallel plate capacitors which store charge. The charge is optically generated by the absorption of photons which are converted to electron hole pairs in the same manner as for a photodiode. However a major difference is that the CCD device is operated in an integrating mode, not the conductive mode. That is, instead of reverse biasing the diode and constantly sensing the variation in current caused by photons, a CCD photoelement (PIXEL) senses the change in voltage induced by the total collection of charge during the optical integration period. The optical integration period must be shorter than a time T due to the fact that the P substrate CCD has only a temporary, negative space charge depletion layer, created by a pulse of positive bias on the gate. The space charge collapses in time T due to the thermal generation of electrons in the space charge region that are swept to the oxide/semiconductor interface. The time T is relatively long, more than 100msec. As given in equation 2.1, it depends on the minority carrier thermal generation time in the depletion layer, τ, the doping of the silicon substrate, N_A, and on the intrinsic carrier concentration, n_i (3).

$$T = 2\,\tau\,(N_A / n_i) \qquad (2.1)$$

For typical values of 10^{-6} sec, 10^{15} cm^{-3}, and 10^{10} cm^{-3} for τ, N_A and n_i respectively, T is 0.2 seconds and the integration time can be as much as 100msec.

The operation of a CCD device is best understood by the energy-band diagram, shown in Fig 2.1, which was first presented in 1975 (2). A good detailed discussion of this figure is given by Sze (3) and will not be repeated here. However, it will be pointed out that as the electron charge Q_{sig} (generated either by light or by thermal excitation)

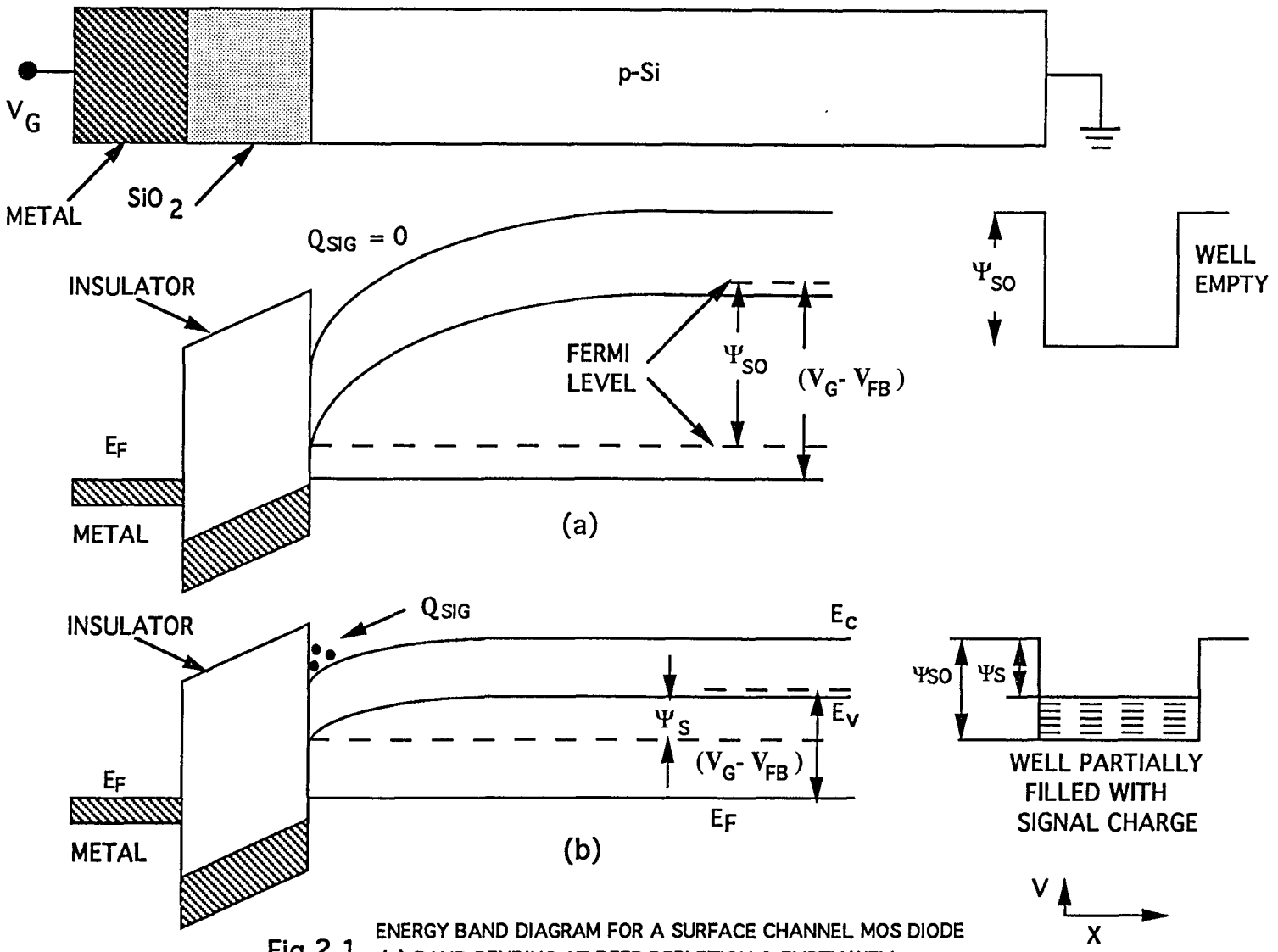


Fig 2.1 ENERGY BAND DIAGRAM FOR A SURFACE CHANNEL MOS DIODE
(a) BAND BENDING AT DEEP DEPLETION & EMPTY WELL
(b) BAND BENDING AT Si-SiO2 INTERFACE AND PARTIALLY FILLED WELL

increases, the depletion layer width W decreases and the potential well depth, surface potential ψ_S, decreases; i.e. the well or bucket is filled up by electrons. The surface potential depends on the applied gate potential minus the signal charge divided by the gate capacitance. The flat band voltage and a term dependent on the square root of the surface potential, ψ_S, also subtract from the gate voltage, as shown by equation 2.2.

$$\psi_S = V_G - Q_{sig}/C_i - V_{FB} - \sqrt{2\varepsilon_S q N_A \psi_s}/C_i \qquad (2.2)$$

Since the last term effects ψ_S by less than 10 percent, the surface potential well can be seen by equation 2.2 to be almost linearly dependent on Q_{sig} and the device can be thought to be a potential well bucket that fills up with electrons. In the case of the CCD light sensor, the charge in each well depends on the number of photons that illuminated the CCD element, i.e. pixel. These charges are allowed to accumulate during a light illumination time, the integration time. The electron packets under the well can be transferred from one gate to the next by a series of clock pulses as shown in Fig 2.2 (3). The signal transfer occurs entirely in the charge domain.

In a less technical explanation, the CCD can be described as a sensor made up of a series of buckets which store photons in the form of electrical charge as shown in Fig 2.3. Using the bucket analogy, the charge corresponds to a drop of water. The photon to electron conversion is identical to that for a photodiode sensor. The major difference is that these bucket sensors are arranged in a serial fashion which permits the charge in a PIXEL bucket to be poured into the next adjacent bucket in a serial fashion. The charge in each bucket eventually is converted to current using a readout drain diffusion well at the end of the pixel array. The array may contain up to 4096 elements because of the very low loss, less than 10^{-2} percent, associated with the charge transfer between elements.

Fig 2.4 shows the organization of a CCD optical sensor system. The pixel elements

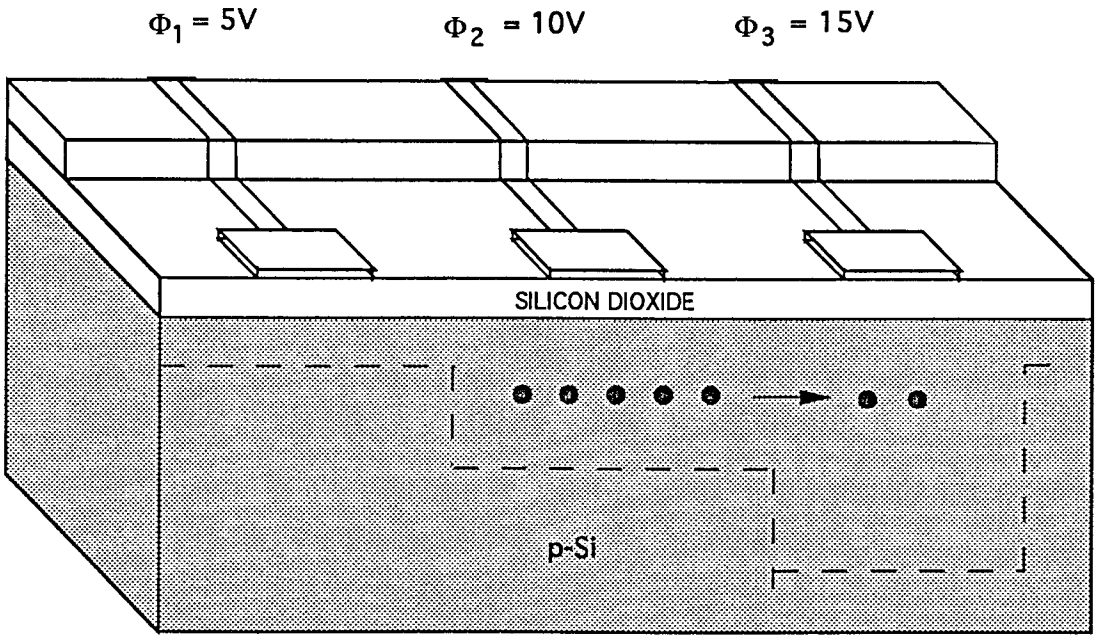


Fig 2.2 SIGNAL TRANSFER BY CCD CLOCK PULSES

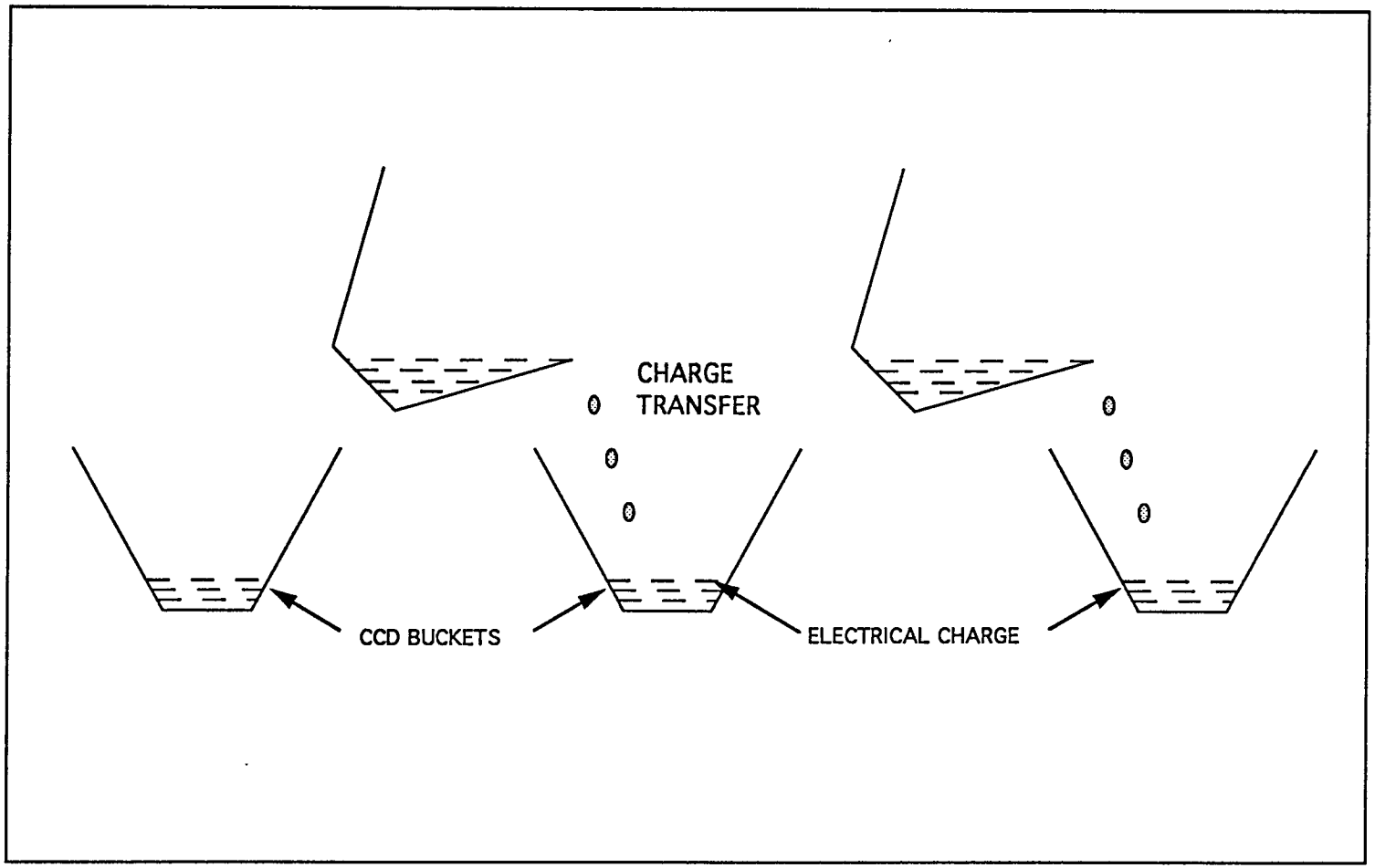


Fig 2.3 SERIAL ORIENTATION OF CCD SENSORS

have a dual side readout structure, which increases the speed at which the signal is transferred out of a pixel linear array. The transfer of the signal from the pixel elements to the corresponding CCD shift registers is carried out under the influence of a transfer gate clock which is pulsed high during the period of transfer. The white reference generator in the pixel shift registers produce a reference output voltage, which occurs once during each line scan time. The dark current collection CCD registers serve to collect the thermally generated electrons, which are then canceled with those generated in the pixel CCD shift registers by the output differential amplifiers, as shown in the figure. The outputs are read out from the CCD pixel shift register by means of a floating diffusion amplifier. The output differential amplifiers give two video signals, OS_1 and OS_2, which are the even and odd pixel video signals respectively.

The camera operates the CCD sensor by providing the necessary biasing and clocking information to run the buckets or charge storage capacitors in the correct sequence. The signal charge is converted to a voltage by the sensor. The voltage waveform is then amplified and shaped by the camera circuitry. The circuitry is on two optional boards in the camera, the MULTIPLEXER board and the SAMPLE-AND-HOLD board.

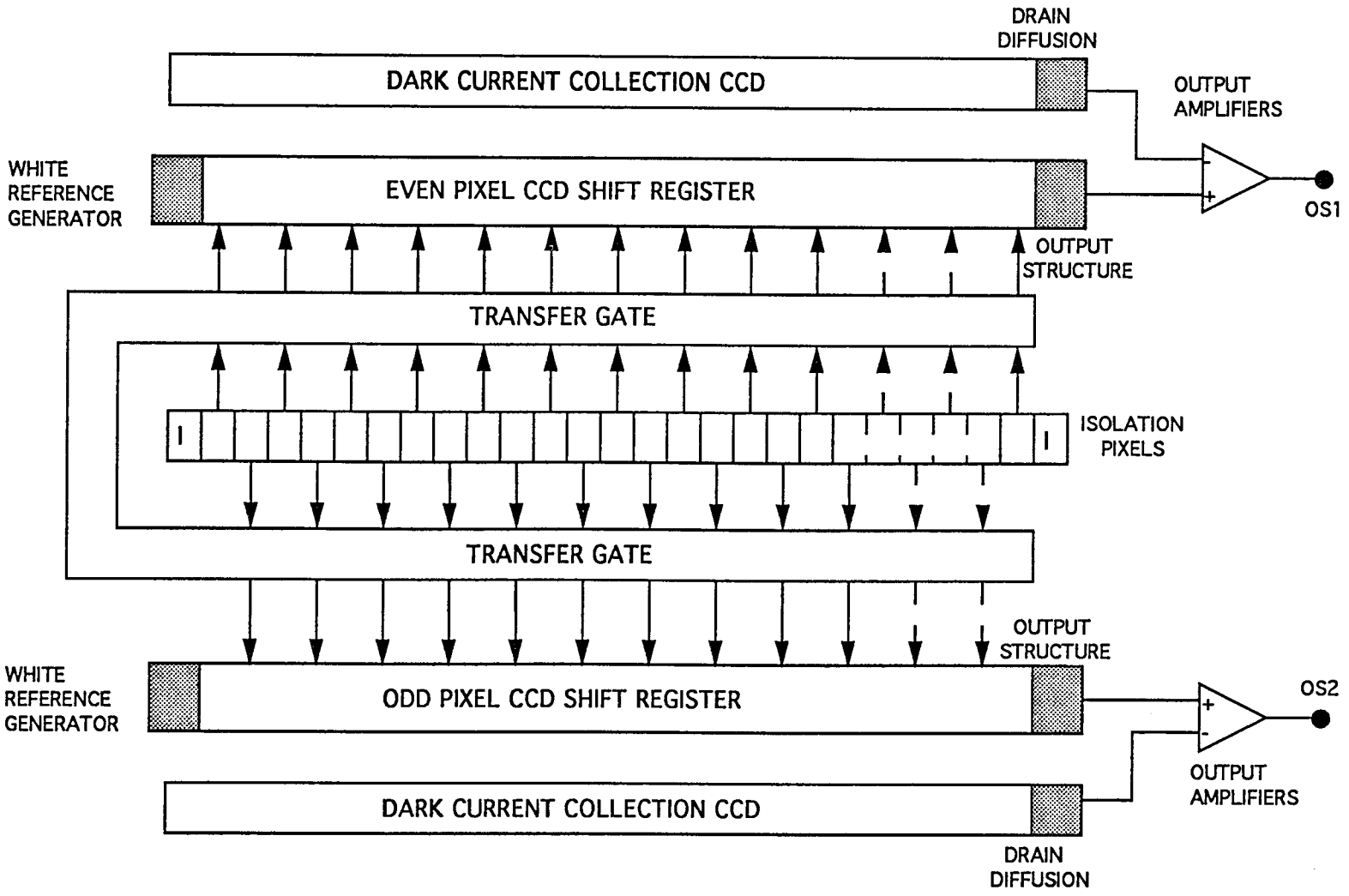


Fig 2.4 ORGANIZATION OF A TYPICAL CCD

CHAPTER 3

OVERVIEW OF CCD MOTION DETECTOR

3.1 Introduction

This chapter gives an overview of the designed motion detector system. A brief account of the operation, with reference to the chapter giving its details, has been included.

3.2 CCD motion detection system

A block diagram of the designed system is shown in Fig 3.1. As shown in the figure, the system can be divided into three subsystems:

the camera; the line controller; and the image grabber, whose circuitry was designed as the major part of this thesis work. The camera and the controller were purchased from DALSA Inc. (1).

3.2.1 Description of the camera

The CL-Cx camera manufactured by DALSA Inc. consists of an image sensing readout chip containing 1024 photo elements. Each element is 14μm X 14μm, with the center to center spacing 14μm. The camera can handle data rates up to 30Mhz with either external or internal clock synchronization. The camera has both exposure and anti-blooming controls. The CCD read-out registers connected to the pixel array are in a dual structure, on either side of the photo-elements, to double the speed of signal transfer. The operation of the camera is controlled by the line controller box, which provides the MASTER clock pulses and DC supply voltages. The camera provides a VIDEO output, which is directly connected to the image grabber subsystem through an RG-59 co-axial cable. More details on the camera are given in the Camera Manual.

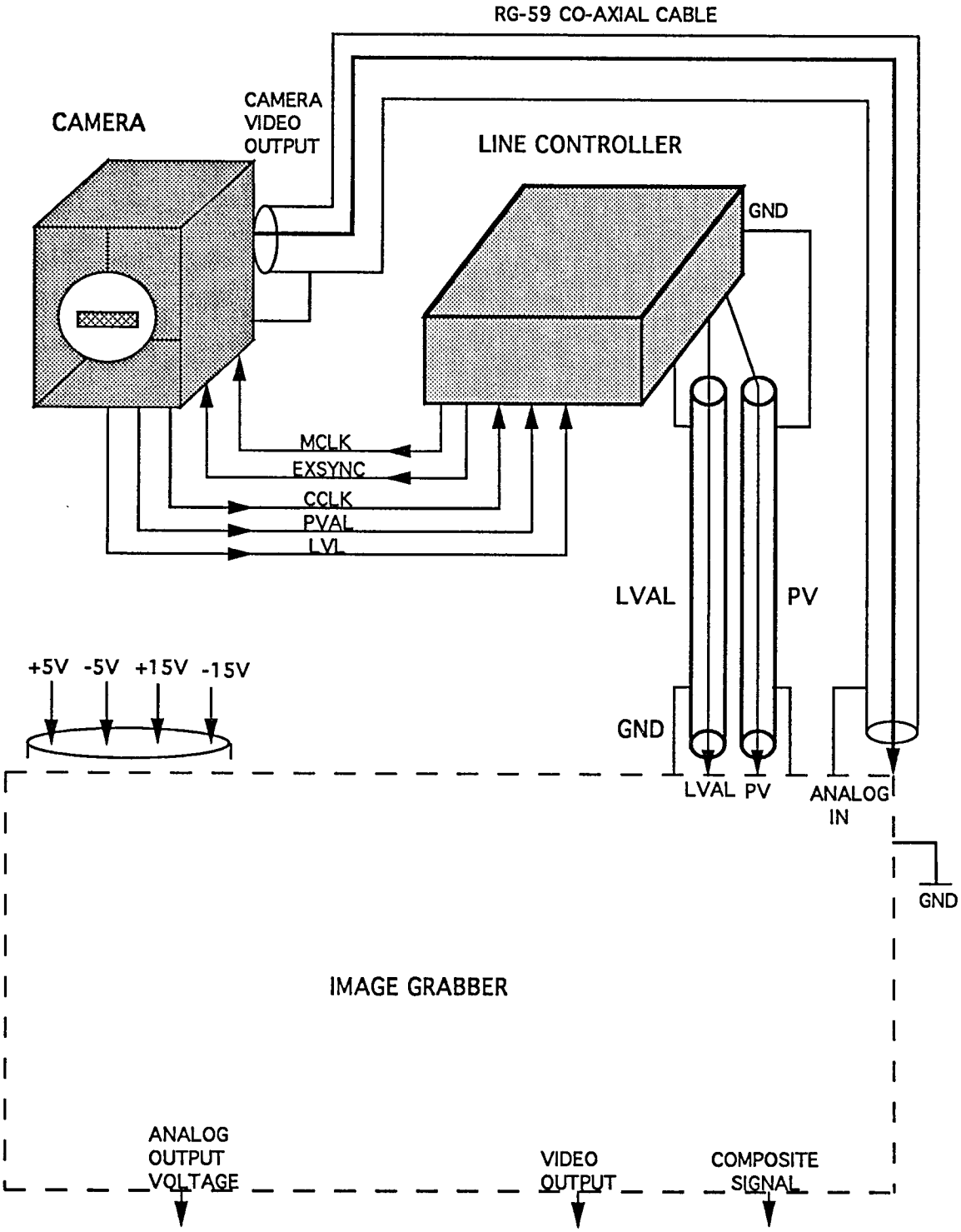


Fig 3.1 SCHEMATIC OF IMAGE SENSING SYSTEM

3.2.2 Description of the line controller

The PB-xx-L200B controller unit provides both the camera and the image grabber with control signals and power supply voltages as shown in Fig 3.1. The interface with the camera is through a multipin connector (DB-25), which couples the control signals between the two subsystems. The Master clock (MCLK) and the External Synchronization pulse (EXSYNC), are the signals sent from the controller to the camera. The Master clock is generated by a quartz crystal oscillator and the clock can be configured for five different frequencies: 2.5Mhz, 5Mhz, 10Mhz, 20Mhz and 30Mhz. Using jumper cable connections any one of the five frequencies could be selected. The Image Grabber system was designed to allow any one of the five clocks to be used. The Master clock generates all the timing signals including the EXSYNC pulse, which synchronizes the start of each readout period during which one line of data is read out of the image sensing array. The DB-25 connector also transfers the control signals from the camera to the Line Controller. These are the Output Master clock (CCLK, CCLK*), the Line Valid (LVL, LVL*) and the Pixel Valid pulse (PVAL, PVAL*). The Line Valid pulse (LVL) is high for the period of the pixel readout, i.e. the line scan time of the camera. The Pixel Valid pulse is the Master clock incorporated with delays required to compensate for the internal delays generated in the camera subsystem.

The controller can provide three signals to the Image Grabber subsystem. These are the PIXEL clock (PV), the FRAME valid pulse and the LINE VALID (LVAL), of which only the PV and LVAL pulses were used in the application, as shown in Fig 3.1. These high frequency pulses are connected to the Image Grabber through shielded cables. More details on the Line Controller are given in Manual.

3.2.3 Description of the image grabber

The function of the Image Grabber subsystem is to convert the video signal into a voltage whose amplitude is proportional to the instantaneous length of the hair cell. The inputs to

the grabber from the line controller are the synchronizing signals, the LVAL and the PV (Fig 3.1). The subsystem provides a video output (after amplification) and also a signal called COMPOSITE signal, which contains the analog video plus a pulse which indicates the point at which sampling is started, and the required analog output. It is comprised of the following circuits shown in Fig 3.2: Video Amplification; Variable trigger; Phase shift; Sampling; Intermediate; Digital; and Adding circuit. A detailed description of each of the seven circuits is contained in chapters 4 to 10.

3.2.4 Operation of the image grabber subsystem

Fig 3.3 shows the circuit waveforms associated with the conversion of the VIDEO SIGNAL into an analog voltage that depends on the number of pixels blocked from the light input by the hair cell; that is, it depends on the location of the edge of the hair cell. As shown in the figure 1.2, the width of the video signal is proportional to the number of pixel elements blocked from the light. The number of pixel cells shadowed depends on the position of the hair cell, as previously discussed in chapter 1. As the hair cell moves, e.g. in a direction to shadow more pixels, the width of the video signal in each line scan time would increase. The main function of the Image Grabber (I.G.) subsystem is to generate an analog signal whose amplitude is proportional to the width of the video signal generated in each line scan time. Fig 3.4 has been drawn for two video pulse widths, T_1 and T_2, which correspond to two instantaneous lengths of the hair cell, X_1 and X_2, where $X_1 = k\ (T_1)$ and $X_2 = k\ (T_2)$, where k is a constant. The FINAL OUTPUT VOLTAGES for the two instances, V_1 and V_2 respectively, are shown in the waveform at the bottom of fig 3.4. These values are proportional to the pulse widths of video signal, T_1 and T_2. Thus $V_1 = K * X_1$ and $V_2 = K * X_2$, where K is a constant of proportionality. Thus the output voltage is seen to be linearly proportional to the instantaneous displacements of the hair cell.

The first step in the conversion of the video signal width to a output voltage is to amplify the signal in the first stage of the I.G. subsystem, the Video Amplification Circuit,

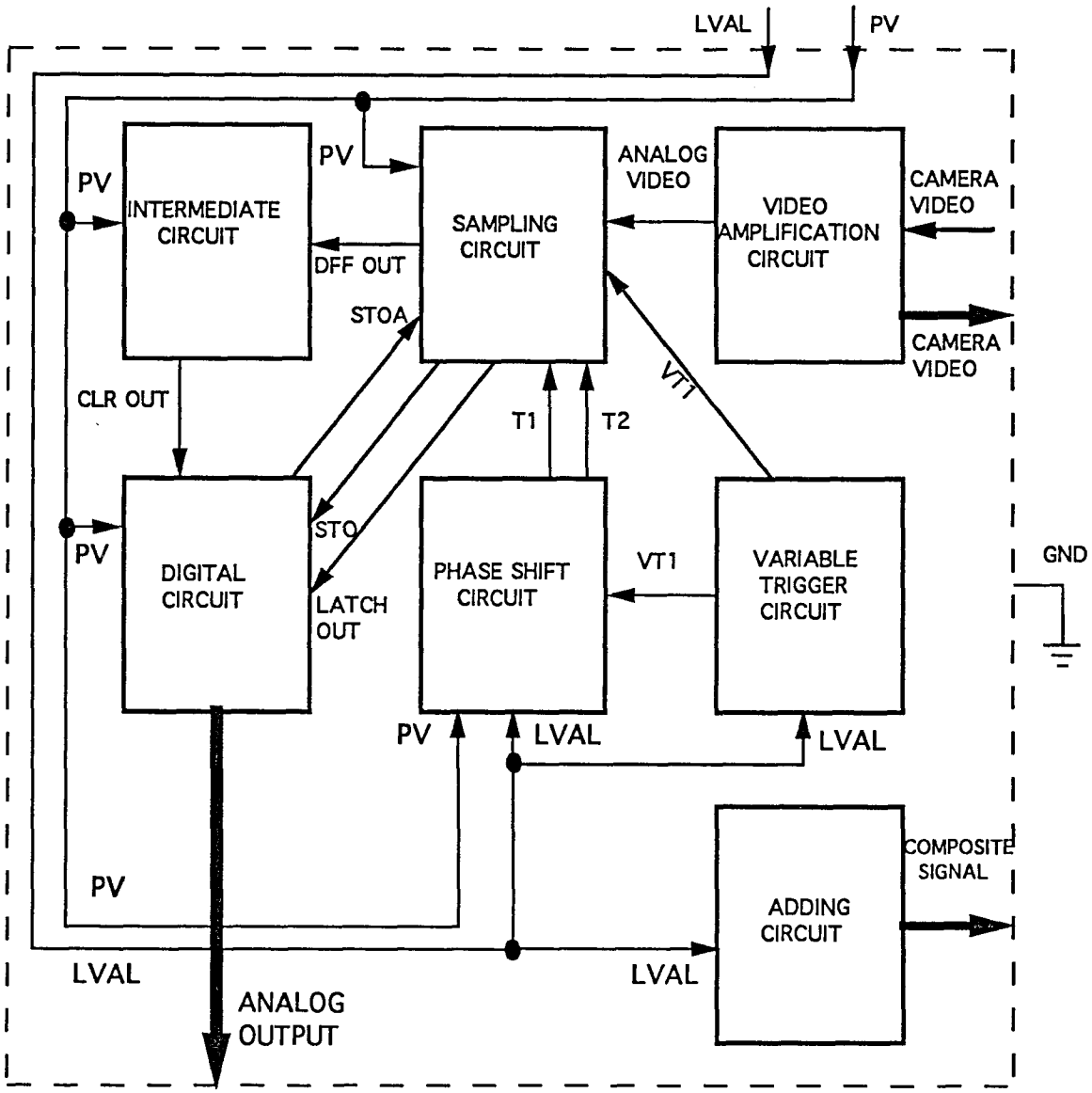


Fig 3.2 DESIGNED IMAGE GRABBER SUBSYSTEM

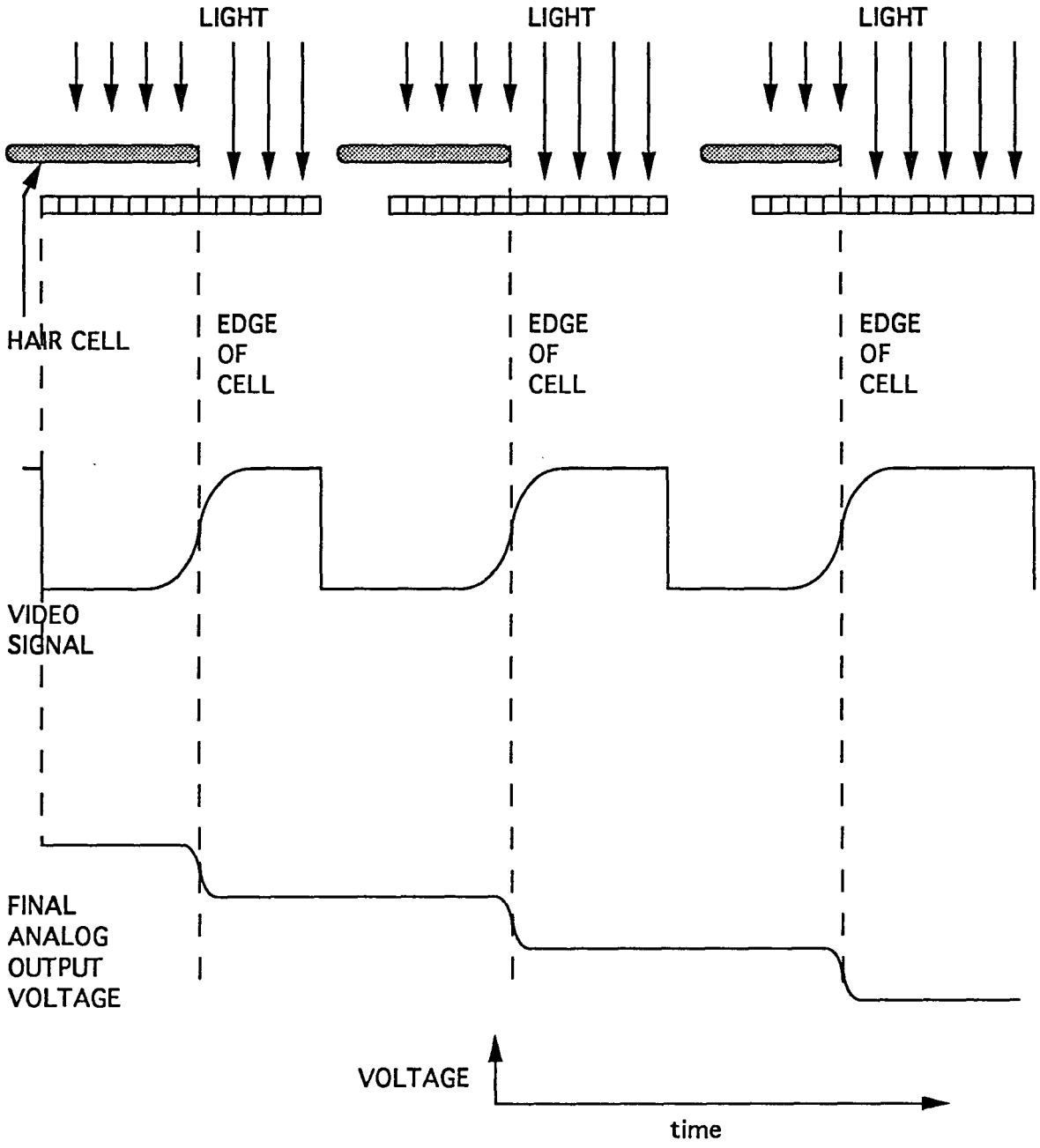


Fig 3.3 VARIATION OF SYSTEM ANALOG VOLTAGE WITH CELL POSITION

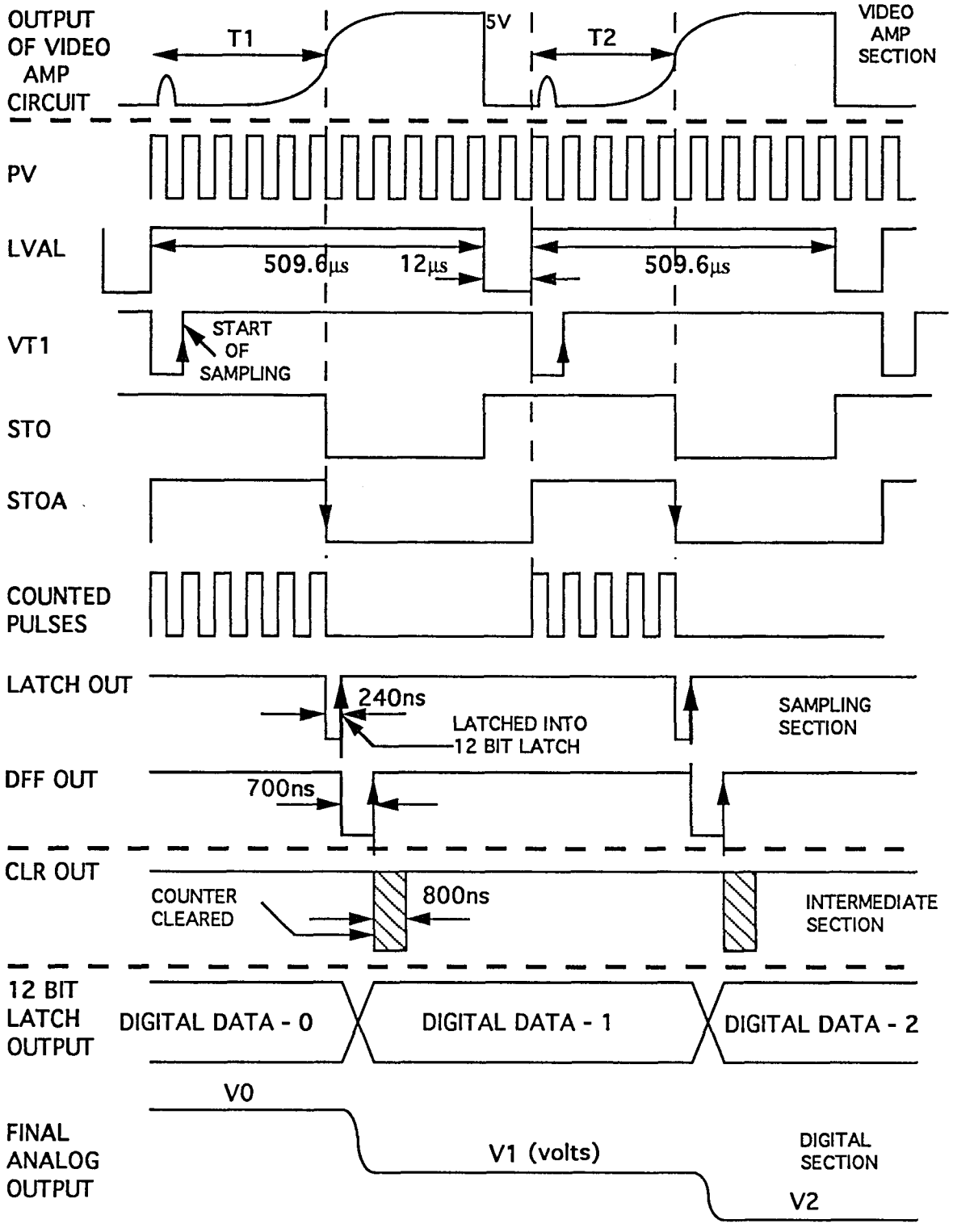


Fig 3.4 BLOCK TIMING DIAGRAM

which consists of three stages of amplification and an overall gain of about 500. The maximum output of this amplified output waveform is five volts, as shown in the first waveform in Fig 3.4. Chapter 4 describes the Video Amplification circuit in detail. The VT1 pulse, shown in the diagram, serves to delay the time at which sampling of the analog signal starts. More detailed discussion on the VT1 pulse is in the fifth chapter. The analog video signal, first waveform of Fig 3.4, is fed to a sampling circuit which uses a Schmitt Trigger to convert the video signal into a digital pulse, STO in Fig 3.4. The trigger point is kept at a constant value of 2.2V, but the offset introduced into the signal in the Video Amplification stage can be varied to trigger at different voltage levels on the waveform. Thus the Video Amplification circuit allows the triggering level to be controlled. This feature allows the user to change the light sensitivity level of the system to test samples with different transparencies. Also shown in Fig 3.4 is the Line Valid, LVAL, signal coming from the line controller, whose rising edge is used as a fixed reference time. The Pixel Valid (PV) signal, also shown, provides the clock pulses that will be converted during the STOA pulse time. The STOA pulse is generated in the Digital Circuit by an AND operation, with the LVAL and STO pulses as inputs. This can be seen by comparing the LVAL, STO, and STOA waveforms. Note that the rising edge of the trigger pulse, VT1, which begins after the rising edge of the LVAL pulse is used to gate the PV clock pulses to the sampling circuit thus preventing noise pulses, such as the dotted one shown in the T_1 time of the video signal, from discontinuing the count. Its duration can be varied from 50ns to over 500μs. The STOA pulse controls the counting of a 12 bit counter, whose clock is the PV signal; with the fall of the STOA pulse the count is frozen. The falling edge of the STOA pulse triggers a monoshot , which generates the 240ns LATCH OUT pulse. Details on the sampling circuit are included in the seventh chapter. The rising edge of LATCH OUT pulse latches the value of the PV pulses counted into a 12 bit latch. This digital output drives a D/A converter, setting its output analog level to e.g. V_1. The instant when the LATCH OUT pulse rises, the 12 bit DIGITAL DATA count shows a new value, which is

that of the counted PV pulses latched into the 12 bit latch. This operation has been described in detail in the ninth chapter. The rising edge of the LATCH OUT triggers another monoshot in the sampling circuit, generating the DFF OUT pulse which has a duration of 700ns. The rising edge of the DFF OUT triggers a monoshot in the intermediate circuit. This circuit generates the 800ns CLR OUT pulse. The CLR OUT pulse is used to clear the counters in the Digital Section, shown by shading the CLR OUT pulse. Details on the intermediate circuit are included in the eighth chapter. Note that all these operations are completed before the rising edge of the next LVAL pulse. Also note that the DFF OUT pulse, shown here as 700ns pulse, controls the time duration between LATCH OUT pulse (given to latch the 12 bit value) and the CLR OUT pulse (given to clear the 12 bit counter). It can be changed from about 50ns to about 4 or 5 μs so that on board transmission line delays can be compensated for.

CHAPTER 4

VIDEO AMPLIFICATION CIRCUIT

4.1 Introduction

The main function of the section is to amplify the video signal adequately so that it can be properly be sampled by the Sampling circuit, while isolating the input signal from the Sampling circuit.

This circuit was designed with three operational amplifiers configured in the differential mode (Fig 4.1), to reject the common mode

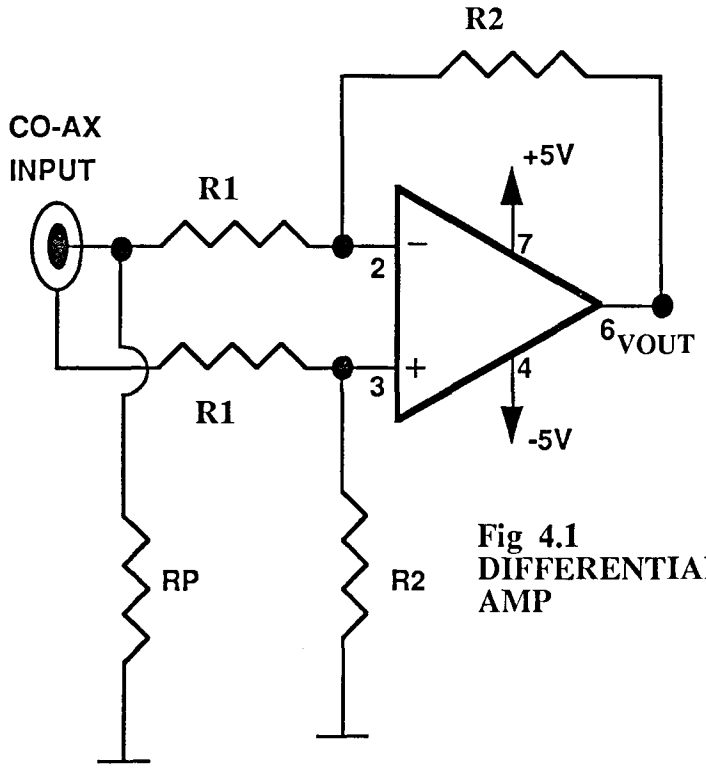


Fig 4.1
DIFFERENTIAL
AMP

signals. The first operational amplifier uses the shielded ground of the co-axial cable to feed the non-inverting input. The signal is fed into the non-inverting input to obtain the necessary inversion of the signal, since the incoming signal is a negative going video.

The input impedance was designed to match the characteristic impedance of the co-axial cable, 75Ω, and was set by the parallel combination of R1=1K and RP=100Ω which gave a value of 90Ω. Experience showed that this match was sufficient and did not load the

signal from the cable.

4.2 Criteria for choosing the opamp

In addition to high input impedance, high gain and low output impedance, an op-amp with a moderate slew rate (~1V/uS) and a gain bandwidth product was required. These performance parameters could be obtained with the LM-741A, which costs only 2 dollars. The LM-741A also had several other desirable features including:

1) Overload protection on the input and output.

2) No latch-up when the common mode signal was exceeded.

3) Freedom from oscillations when driving capacitive loads.

The LM-741A was chosen over the LM-741C, because of its largest operating range, -55 to 125°C, versus only 0 to 70°C for the LM-741C. Table 4.1 presents the typical op-amp parameter values for the LM-741A. The values of the input offset voltage and input offset current are within tolerable limits, since the input signal to the first stage is greater than 200mV. The 6MΩ input impedance is sufficiently high since the circuit input impedance of each stage is less than 2.2KΩ. The output short circuit current of 25mA is more than the largest required current, estimated by the following:

Consider the case when the first stage has saturated. The current through the second stage would be 5v divided by the resistance of the non-inverting leg (about 10K), which comes to 0.5mA. This value is far less than 25mA, the output short circuit current.

For the specification values of the common mode rejection ratio (CMRR) and the power supply rejection ratio (PSRR), 95dB and 96dB respectively, the maximum circuit input impedance levels should not exceed 50KΩ according to the manufacturer. The maximum circuit input impedance levels in the video amplification section were designed to be less than 10KΩ, which insures low noise operation.

Insight into the frequency response needed in the video amplification section can be obtained from the following discussion. The camera video signal has a line scan rate of

TABLE 4.1 TECNICAL SPECIFICATIONS OF THE LM-741A OP-AMP

SNO	PARAMETERS	CONDITIONS	TYPICAL VALUE	UNITS
1	INPUT OFFSET VOLTAGE	T_A=298K	0.8	mV
2	INPUT OFFSET CURRENT	T_A=298K	3.0	nA
3	INPUT BIAS CURRENT	T_A=298K	30	nA
4	INPUT RESISTANCE	T_A=298K VSUPPLY= ±20V	6.0	MΩ
5	OUTPUT SHORT CIRCUIT CURRENT	T_A=298K	25	mA
6	COMMON MODE REJECTION RATIO	V_{CM}= ±12V $R_S \leq$ 50KΩ	95	dB
7	POWER SUPPLY REJECTION RATIO	V_S = ±20 to ± 5V $R_S \leq$ 50KΩ	96	dB
8	RISE TIME	T_A=298K	0.25	μs
9	OVER SHOOT	UNITY GAIN CONFIGURATION	6	%
10	UNITY GAIN BANDWIDTH	T_A=298K	1.5	MHz
11	SLEW RATE	T_A=298K UNITY GAIN CONFIGURATION	0.7	V/μS
12	SUPPLY CURRENT	T_A=298K	1.7	mA
13	POWER CONSUMPTION	V_S = ±20 to ± 5V $R_S \leq$ 50KΩ	150	mW

about 2.5Khz, obtained by dividing the Master clock frequency of 2.5Mhz by the number of pixels in the linear array of the camera (i.e. 1024). This signal is conditioned by the sample-and-hold board (located within the camera) to give a continuous waveform that does not have the pixel voltage reset pulses between adjacent pixel video signals. The smallest transition time for the camera video signal occurs over a length of 2 pixels, after the last pixel has been read out i.e., in synchronism with the trailing edge of the LVAL signal. Thus the fall time would be 0.8μs, since the master clock has a frequency of 2.5Mhz. This time is greater than the op-amp specification value of 0.25μs shown in the table. However, the circuit is still able to function because only the time duration between successive pulses is critical to the measurement of object displacement.

The overshoot value of 6%, as given in the table, is not significant as the output of the amplification stage is used to trigger a circuit whose threshold for triggering is half of the peak value of the waveform. Since the waveform extends to 4.5v, this value would be fixed at about 2.2v. A 6% overshoot of 4.5v is about 270mV, which would not affect the trigger point level positioned at 2.2V. The bandwidth of the op-amp, 1.5Mhz, is equal to 0.35 divided by the risetime response of the op-amp to a step input. This value of 1.5Mhz is sufficient for clock rates of 2.5Mhz, as previously explained.

The slew rate is the only parameter which causes a limitation on the highest frequency that the circuit can be operated at. As mentioned previously the critical falltime has a value of 0.8μs, during which the waveform changes by 4 volts. This requires an op-amp having a slew rate of atleast 5V/μs. The LM-741A has a slew rate of 0.7V/μs, as shown in the table. A slew rate less than the required value causes a delay in the rise and fall of the signals. This time delay, however, does not affect the operation as only time durations are converted to voltage.

The power supply current and power consumption are reasonable values.

4.3 Description of the design

Since the required output to the sampling section had to be 4V and the input signal could be as low as 10mV, a gain for the video amplification section of at least 400 was required.

The signal from the video out of the camera was terminated at the input of the amplification section using a 75Ω Coaxial cable of the shortest length (about 1.5 meters). As shown in figure 4.2, the input is terminated using a 100Ω resistor with 1% tolerance. The parallel combination of this resistor with the input impedance of the first stage(designed to be 1KΩ), gives an effective signal impedance of 90Ω, which experimentally gave the least signal rejection. The incoming signal was given to the inverting input of the first stage to achieve the required inversion. The shielded coaxial ground was connected to the non-inverting input to feed the ground noise as the common mode signal. It should be noted that the rms value of the noise signal, V_{og}, is fed to both inputs of the differential stage. During subtraction of the signals fed to the inverting and non-inverting inputs, the ground noise is canceled as shown by equation 4.1.

$$(V_+ - V_-) = (V_{sig} + V_{og} - V_{og}) = V_{sig}. \qquad 4.1$$

The output signal V_{out} is obtained by multiplying V_{sig} by the resistive ratio of R_2 / R_1. The bandwidth of the first stage should be at least 150Khz, which would allow the op-amp to follow an input waveform with a risetime of 0.35 / 150Khz, i.e. 2.3μs. Although the minimum calculated value of the fall time is 0.8μs, the signal swing, which occurs at the edge of the object changes over a length corresponding to about 10 pixels, giving a rise time of 10 multiplied by the period of the MASTER clock i.e. 4μs. To design the differential stage with a closed loop bandwidth of atleast 150Khz, would limit the gain to 10 since the closed loop gain times the closed loop bandwidth is equal to the unity gain bandwidth product, 1.5Mhz as specified in table 4.1.

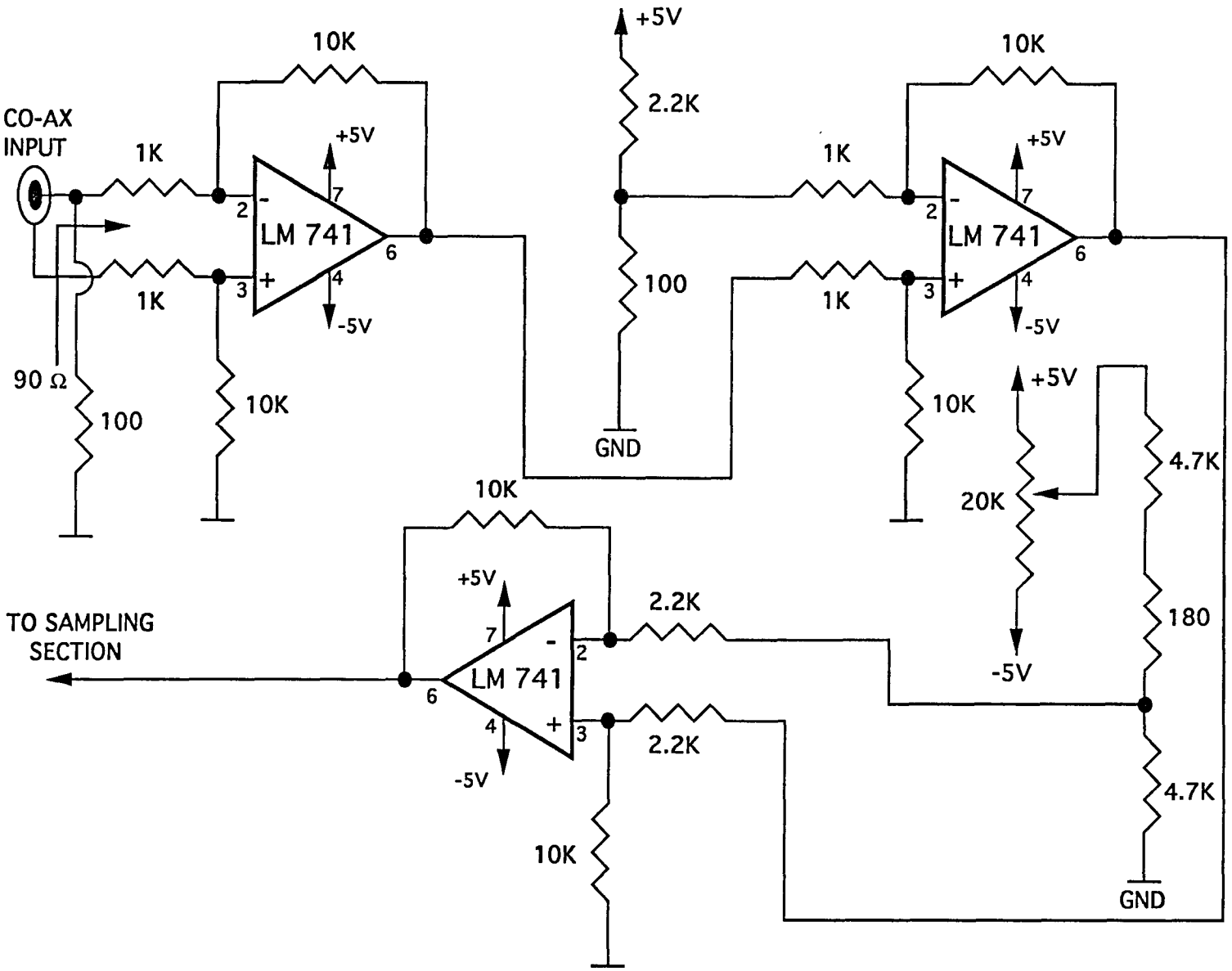


Fig. 4.2 VIDEO AMPLIFICATION CIRCUIT DIAGRAM

The second stage was configured in the non-inverting mode and was designed to provide a gain of 10, the maximum permissible gain for the required frequency response. It was experimentally found that a DC shift of about 200mV was required to bring the video signal to the zero volt reference. Thus the design included a resistor divider network which provided a voltage shift of 5V multiplied by the resistive ratio of 90Ω/2.29KΩ, i.e. 196mV. The current drawn by the network from the supply is 2.18mA.

The third stage was configured similarly to the second stage. A variable DC voltage bias shift was obtained by connecting +5 and -5v supplies to a 20 turn 20KΩ potentiometer connected to a resistive divider network as seen in figure 4.2. The attenuation ratio of the resistive network was 0.235, giving a bias shift range of +1.175V to -1.172V, fed to the inverting input. The purpose of this bias network is two fold:

1) It serves to provide a variable DC level shift, which is additional to the one of the previous stage.

2) Since the triggering level of the Schmitt trigger circuit is designed to be a constant, the DC level of the video signal must be changed to obtain an effective variable triggering level.

The gain of the third stage, 4.53, was fixed by the ratio of 10KΩ/2.2KΩ. Thus the total gain of the video amplification section was 453, adequate to provide the sampling section with a TTL compatible input of about 5V.

CHAPTER 5

VARIABLE TRIGGER CIRCUIT

5.1 Introduction

The purpose of this circuit is to compensate for the signal due to the partial transparency of sections of the bimorph or other objects, which would otherwise cause false triggering in the sampling section and stop the count as explained in chapter 3. The circuit allows the voltage level point at which sampling occurs to be varied using a simple monostable multivibrator.

Fig 5.1 illustrates the problem of false triggering due to the partial transparency of the object. The "false pulse" could cause false triggering of the trigger circuit in the sampling circuit if the amplitude of the pulse exceeds the trigger threshold (as it does in the figure). It therefore becomes necessary to begin sampling after the occurrence of such pulses. The desired point of sampling has been shown in the figure. There is a need for a circuit to vary the start of sampling depending on the location of the translucent regions of the bimorph.

5.2 Description of variable trigger section

Consider Fig 5.2. The circuit consists of a non-retriggerable monostable multivibrator(96S02). The positive edge of the LINE VALID (LVAL) signal triggers the multivibrator. Detailed information on the 96S02 is available in the National Semiconductor Data book. The pulse width (T_X) of the output pulse is controlled by the values of R and C in the figure. T_X, calculated with the formula, 1.1RC, for the pulse output, can be varied up to a maximum value of 570μs, which is greater than the LVAL active line time of 509.6μs. The value of C was selected as 0.047μf and R as 1.0KΩ in series with a variable 10KΩ, 20 turn precision potentiometer. The 1.0KΩ resister was placed within 2 mm of pin 2 to reduce the stray capacitance effects between pins 1 and 2. The potentiometer was also

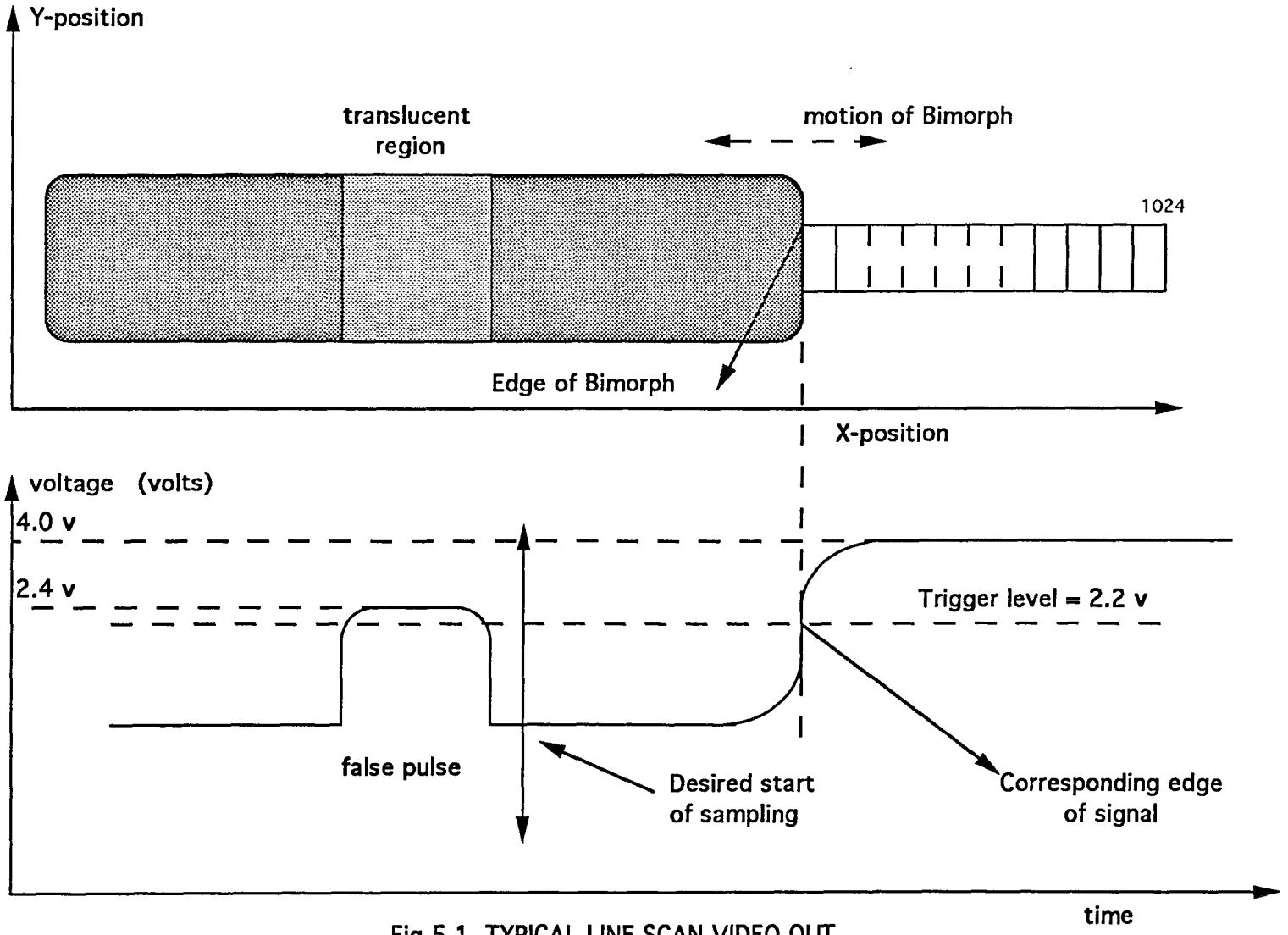


Fig 5.1 TYPICAL LINE SCAN VIDEO OUT

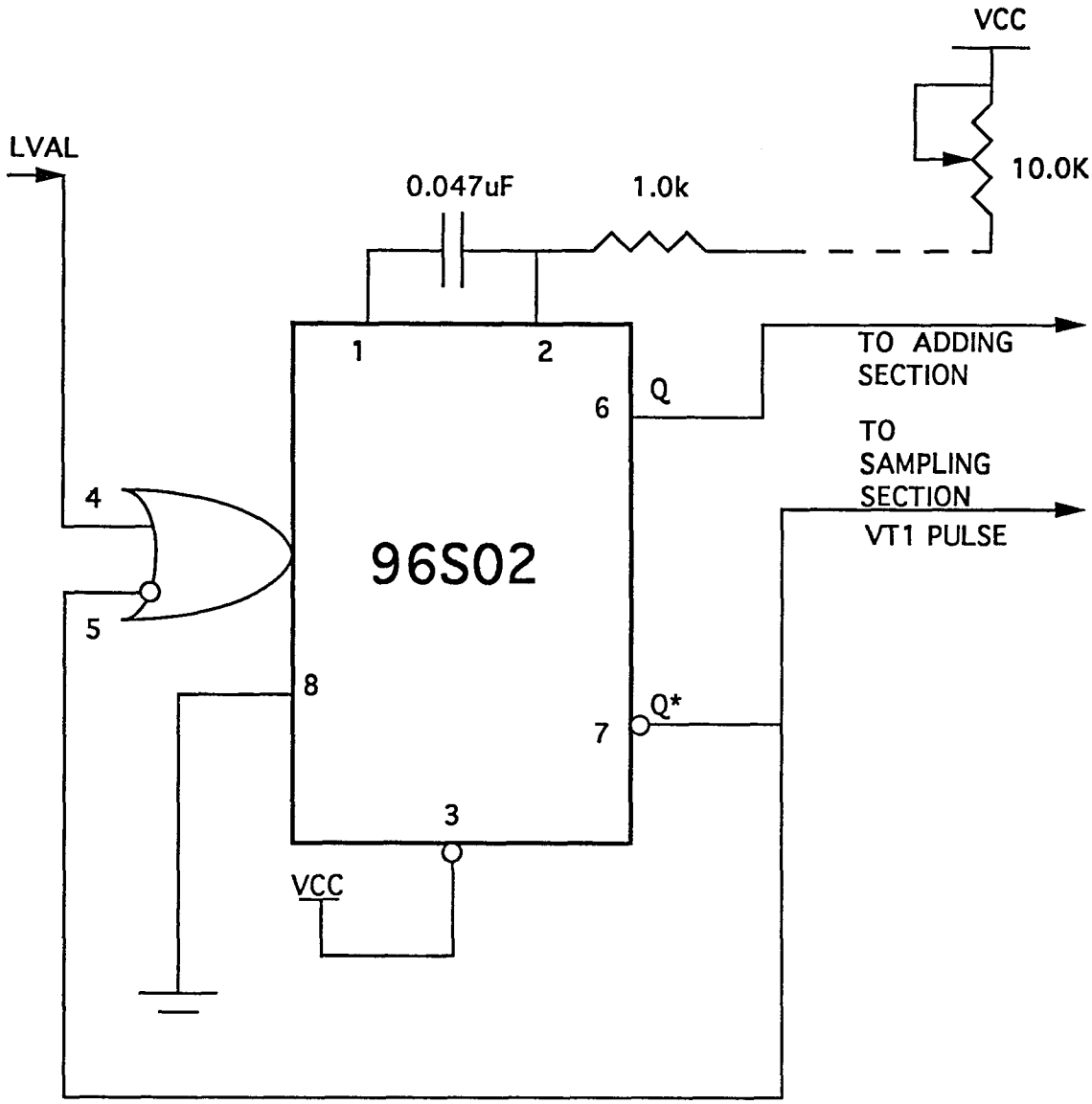


Fig 5.2 VARIABLE TRIGGER CIRCUIT

placed close to the resister at a distance of about 10 cm. The Q^* output was connected to the negative edge trigger input (pin 5) to prevent retriggering. This configuration prevents retriggering between the time the circuit gets triggered and when the output pulse returns to its stable state, here the zero volt reference.

The timing diagram shown in figure 5.3 further describes the circuit operation. The required output of this circuit is the negative VT1 pulse, which is generated from the complementary output Q^* of the 96S02. The edge marked "start of sampling" determines the point at which the sampling of the analog video signal is started. By varying the potentiometer, the leading pulse of VT1 is varied 50ns to 570µs, well beyond the active line time. The VT1 pulse is a control signal to both the sampling and the phase shift circuits. The Q output is an input to the adding section.

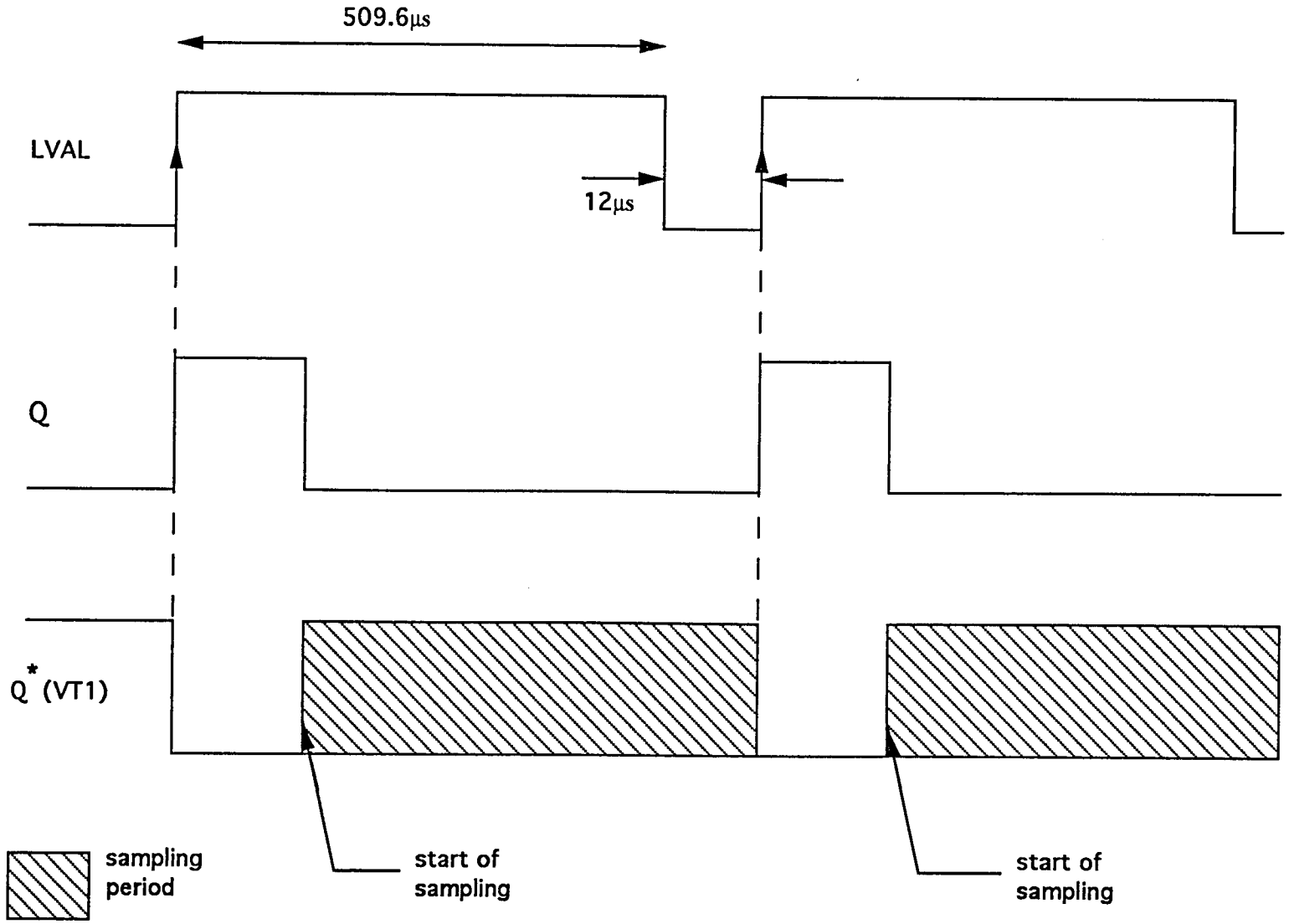


Fig 5.3 VARIABLE TRIGGER TIMING DIAGRAM

CHAPTER 6

PHASE SHIFT CIRCUIT

6.1 Introduction

This circuit shapes the control signals, T1 and T2, fed to the sampling circuit. As previously mentioned, dual sampling of the same analog video in two separate channels is done. The sampling of these channels is controlled by these two signals, which are generated and shaped in this circuit.

6.2 Description of the T1 circuit

The T1 signal is generated for the main channel, which continuously samples the video signal. The PV signal is buffered by ANDING it with a +5V DC signal as shown in Fig 6.1. This is done using an F-series TTL 74F08 AND gate, which has a delay time of 5ns. The positive edge of the gated PV signal triggers the monostable 2A, which is configured in the non-retriggerable mode. By this it is meant that the input can only trigger the monoshot once before its Q output pulse returns to its stable state. The Q output of the monoshot 2A, shown in Fig 6.1 has been designed to have a pulse width of 277ns. The pulse width is given by 1.1RC, where R is the resistance between the pin 1 and supply and C is the capacitance between the pins 1 and 2 .The negative going edge of the Q output of monoshot 2A is used to trigger monoshot 2B. The pulse width of the Q output of 2B was set at 44ns. The monoshot 2B was also configured in the non-retriggerable mode. The Q output of the monoshot 2B constitutes the T1 pulse.

6.2.1 Description of the T1 timing diagram

The LVAL signal, which indicates the pixel line readout period, has an active going period of 509.6μs and a line off period of 12μs as shown in Fig 6.2. All the timing signals are

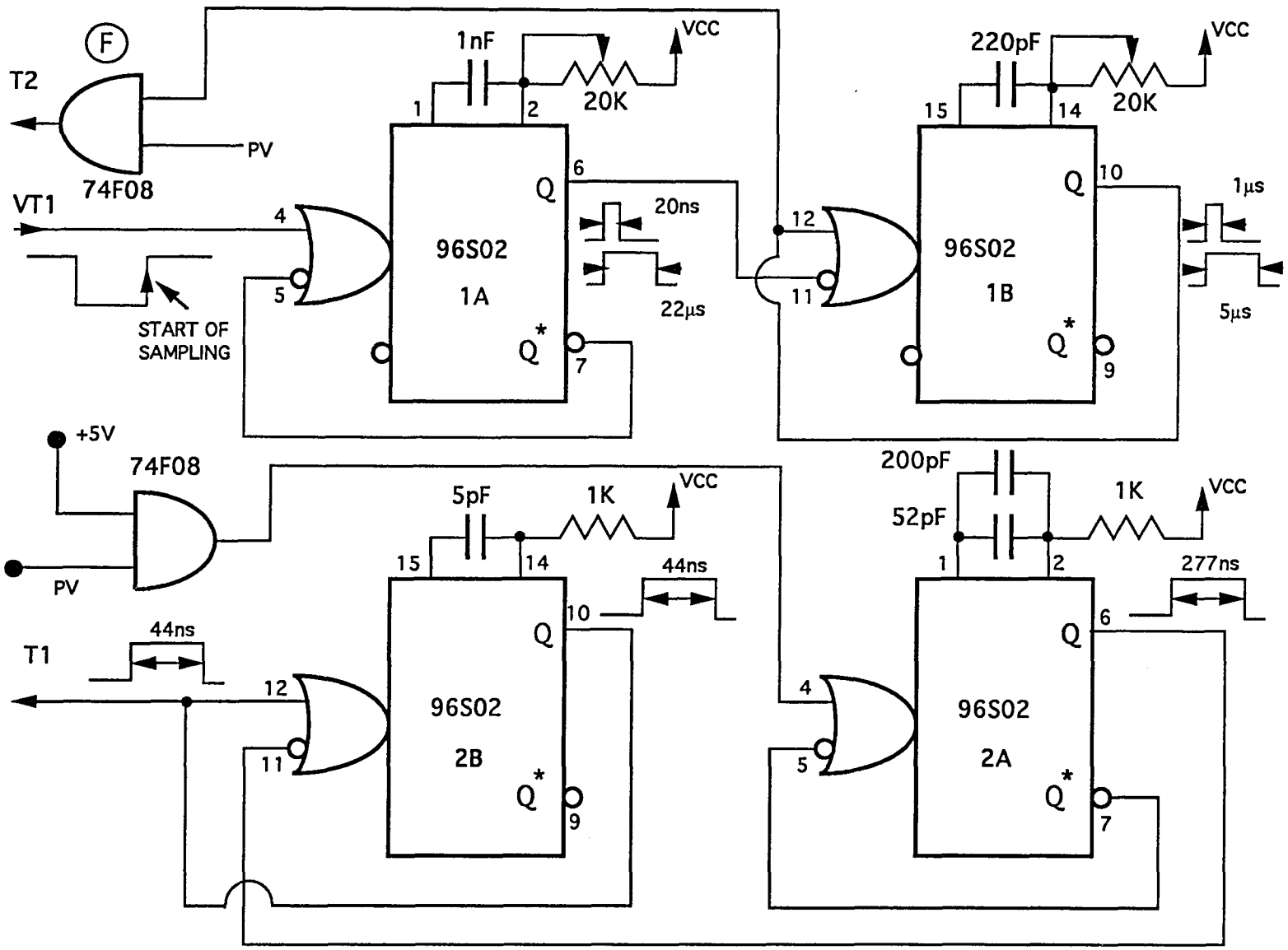


Fig 6.1 PHASE SHIFT CIRCUIT DIAGRAM

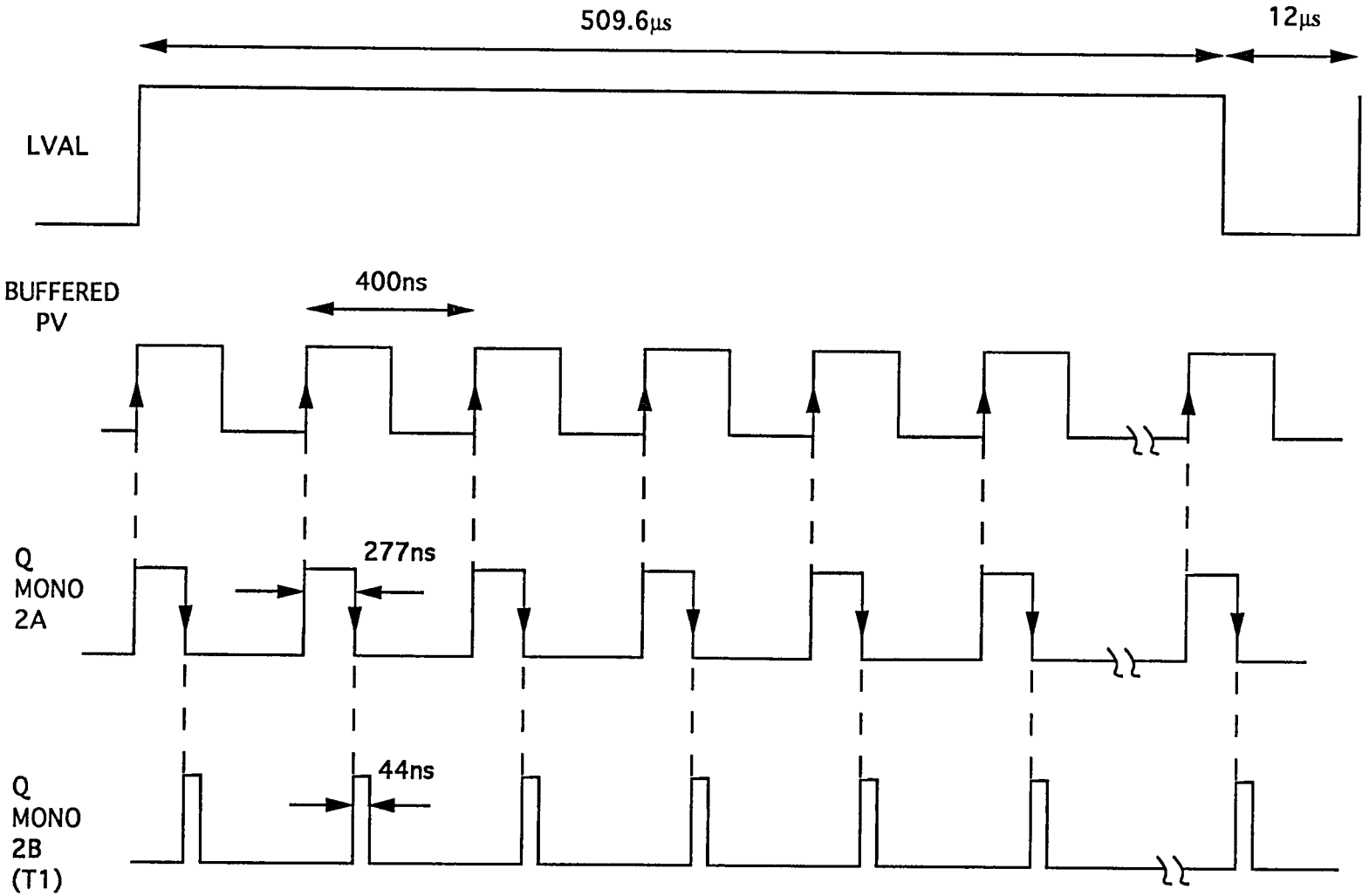


Fig 6.2 T1 TIMING DIAGRAM

synchronized with respect to the LVAL pulse. This signal and the PV signal, both generated in the Line controller box, control the clocking of the sensor pixel array. The buffered PV signal has a 50% duty cycle and a period of 400ns. As shown in the timing diagram, this signal triggers a pulse of width equal to 277ns, which comprises the output from the Q output of monoshot 2A (Fig 6.1). The trailing edge of this pulse triggers a pulse of width 44ns, which is the Q output from monoshot 2B (Fig 6.1). This output forms the T1 pulse, which is used as the sampling signal in the main channel of the sampling circuit.

6.3 Description of the T2 circuit

The T2 signal generation uses a configuration similar to the T1 signal generation, with the only difference being the pulse widths and the input signal used to trigger it. Consider Fig 6.1. The upper half of the circuit generates the T2 signal. The rising edge of the input pulse (VT1), from the variable trigger section, controls the time at which the sampling starts. This pulse triggers the monoshot 1A with its positive going edge. The monoshot output pulse duration can be varied over a wide range, i.e. from 20ns to 22μs. The pulse width is normally set at about 50ns to allow the settling down of transients associated with the rest of the circuitry. The negative edge of the Q output pulse of monoshot 1A triggers monoshot 1B, whose Q output pulse can be varied from 1μs to 5μs. Note that the width of this pulse has to be large enough to accommodate at least two PV pulse periods. The pulse width of this output is normally set to 2μs. The Q output of the monoshot 1B is ANDED with the PV signal by the AND gate marked F in the figure. The output of the AND gate is the T2 signal, which is used as the sampling signal to the auxiliary channel in the sampling section.

6.3.1 Description of the T2 timing diagram

The VT1 pulse from the variable trigger section has been shown in Fig 6.3 to be triggering a pulse that can be varied between a minimum of 20ns and a maximum of 22μs, determined

by the pulse width of the output of monoshot 1A. The negative edge of this pulse triggers monoshot 1B, whose Q output pulse has a width that can be varied from 1μs to 5μs, as shown in the Fig 6.1. The ANDED pulse of PV and the Q output of monoshot 1B is the T2 pulse.

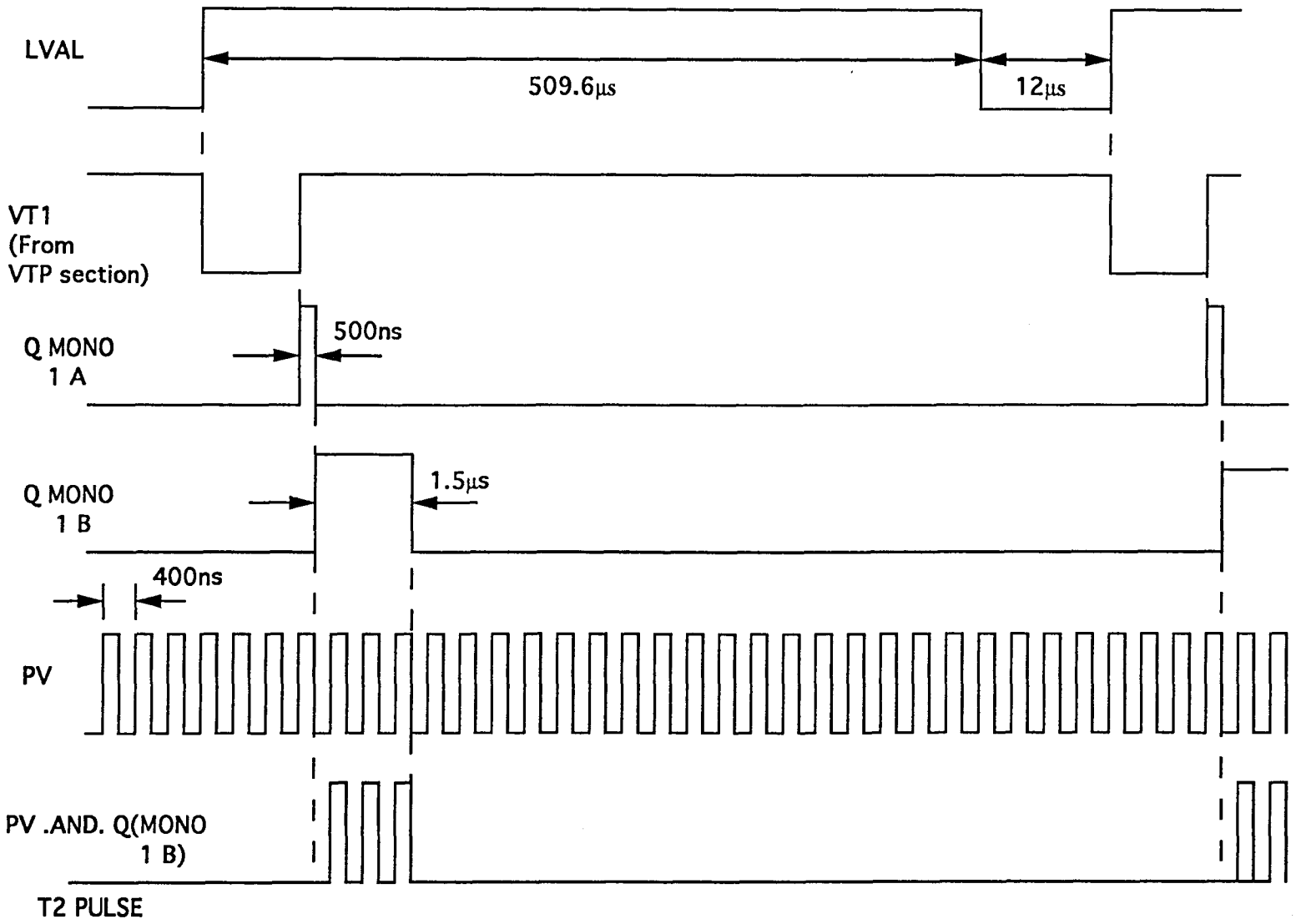


Fig 6.3 T2 TIMING DIAGRAM

CHAPTER 7

SAMPLING CIRCUIT

7.1 Introduction

The sampling circuit converts the analog video signal to a pulse width modulated signal, whose width corresponds to the length of the object. The outputs of the variable trigger circuit enable the sample-and-hold amplifiers in this circuit to sample only the required part of the video signal.

The LVAL and PV pulses control all the signals generated in this section. As previously described, the LVAL signal is high during the shift-out of the pixel video signals (509.6μs) and goes low for a period of 12μs. The PV signal has a duration of 400ns and a 50% duty cycle. The timing required for the digital section is also generated here. This circuit cancels the DC offset in the analog video signal. An optional jumper connection has been provided for measuring the edge of the bimorph from the opposite side of the reference (which is the 0^{th} pixel) i.e. from the 1024^{th} pixel.

7.2 Description of the dual sampling circuit

Consider Fig 7.1. The analog video signal from the video amplification section is fed to input pin (pin-6) of two sample-and-hold amplifiers, the CLC 940s. Thus the analog video signal is simultaneously sampled by both the MAIN channel (top CLC 940) and the AUXILIARY channel (the bottom CLC 940).

The CLC 940 is a fast sampling, wideband sample-and-hold amplifier. It has a 10ns acquisition time, a 12ns settling time, an aperture jitter of 1ps and a bandwidth of 150Mhz, which were found adequate for the application. The Comlinear Data book contains more details on the CLC 940. The sampling ON/OFF in the chip is controlled by a pair of differential inputs, namely the track (pin-2) and hold (pin-1) inputs as shown in Fig 7.2. The chip samples when the voltage on the track pin is greater than that on the hold pin.

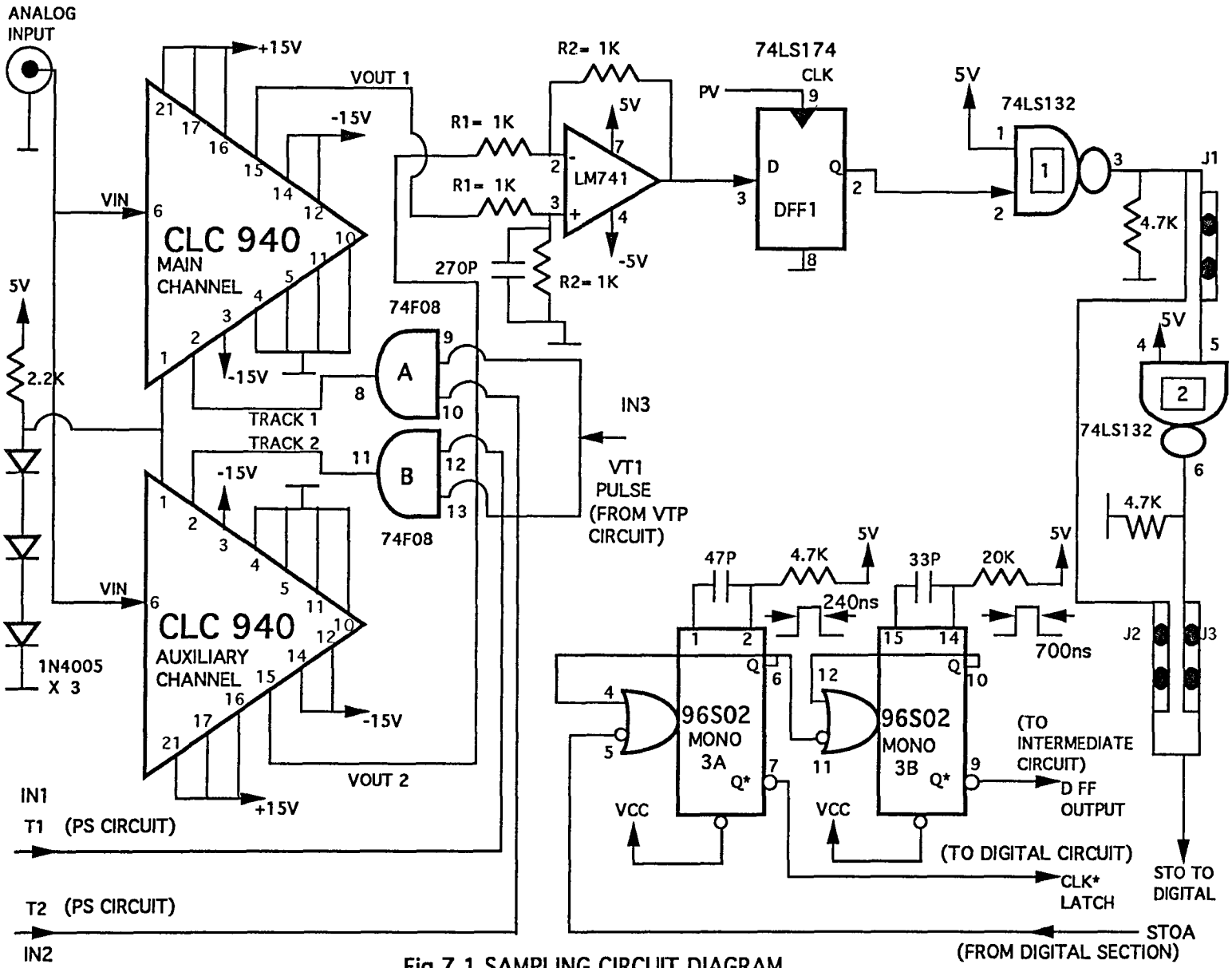


Fig 7.1 SAMPLING CIRCUIT DIAGRAM

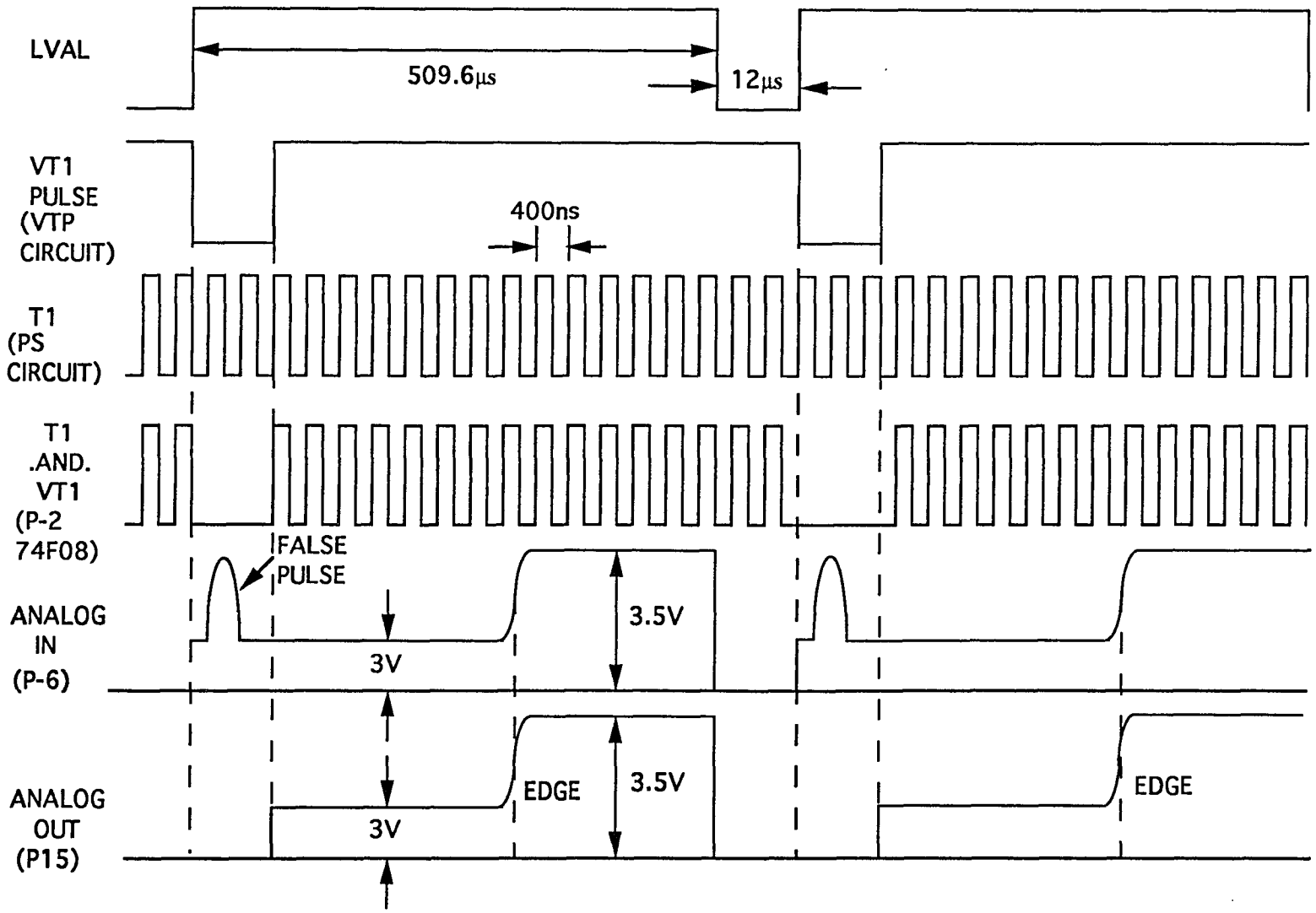


Fig 7.2 MAIN CHANNEL TIMING DIAGRAM

The chip stops sampling i.e. goes into the hold mode, when the voltage on the hold pin is greater than that of the track pin. The best switching is achieved when the slew rate of the digital pulses given to the two inputs is greater than 20V/μs with a differential signal excursion not exceeding 2.5V. To maintain a differential voltage of 2.5V between the track and hold pins, a diode network as shown in Fig 7.2 was designed to feed a voltage of 2.3V (the sum of the voltage drops across the three diodes) to the hold input (pin-1). The CLC 940s use power supplies of ±15V.

In the main channel the track pin is fed with the output (pin-8) of the AND gate (74F08) marked A in the figure, the inputs to which are the VT1 pulse (from the variable trigger circuit) fed to pin-9 and the T1 pulse (from the phase shift circuit) fed to pin-10. The output of the CLC 940, pin-15, is fed to the non-inverting input of the differential amplifier. In the auxiliary channel, the track input is fed with the output (pin-11) from the AND gate marked B, the inputs of which are the T2 signal (from the phase shift circuit), pin-12, and the VT1 pulse (from the variable trigger circuit), pin-13. The output of the S/H amplifier, pin-15, is fed to the inverting input of the differential amplifier.

7.2.1 Description of main channel timing

Consider Fig 7.2. As previously discussed, the analog signal input to the S/H amplifier can have a spurious pulse. Note that it has been assumed that the bimorph is partially transparent to light, resulting in a DC offset in the analog video waveform shown here as 3V. The VT1 pulse has been adjusted in the variable trigger section so that the rising edge of the pulse occurs after the spurious pulse in the video signal. This can be seen in the ANDED waveform (T1.AND.VT1). Note that the sampling extends into the LVAL off periods to sample the portion of the video waveform, which is low (the video is brought back to 0 volt reference during LVAL off periods). It remains low till the sampling starts. The output of the S/H amplifier is the last waveform in the figure, with the spurious pulse not influencing the sampling.

7.2.2 Description of auxiliary channel timing

Consider Fig 7.3. The analog video in this channel is sampled merely to obtain the DC offset voltage associated with the analog video. This is done by sampling the analog video during the pulse duration of T2, which is shown as a group of PV pulses in the figure. The T2 pulse is ANDED with the VT1 pulse to eliminate any spurious noise pulses outside the VT1 pulse duration. The result is a sampling pulse (fed to the track input) of the auxiliary channel. Note from the figure that sampling starts 50ns after the rising edge of the VT1 pulse and is completed in 1μs (the pulse duration of T2 burst), resulting in a DC voltage at the output of the S/H amplifier, which is the DC offset of the analog video signal. This has been shown in Fig 7.3 as the last waveform.

7.3 Description of the D/A pulse circuit

Referring to Fig 7.1, the output of the main channel S/H amplifier is fed to the non-inverting input of a differential amplifier, while the output of the auxiliary channel is fed to the inverting input. The resistive combination of R_2 and R_1 was chosen to give a unity gain to obtain a mere subtraction of the two signals. A diode is placed between the output of the differential amp and ground to prevent signals going negative, as this would upset the conversion of the analog video into the corresponding digital pulse. The output of the differential amplifier is digitally sampled and synchronized to the PV signal by feeding the output of the differential amplifier to input (pin-3) of the D flip-flop (74LS174). Note that since the transition region width for TTL logic is 0.2V, the signal is converted to a digital pulse at a threshold voltage of 2.2V (the value of INPUT HIGH in TTL logic). The output of the D flip-flop (pin-2) is given to a Schmitt trigger NAND gate numbered 1(74LS132), which does the same function as the D flip-flop, except for the synchronization. The output of the NAND gate (pin-3) constitutes the STO (Schmitt trigger pulse output), which is fed to the digital section via the jumper marked J2. An optional circuit with another 74LS132

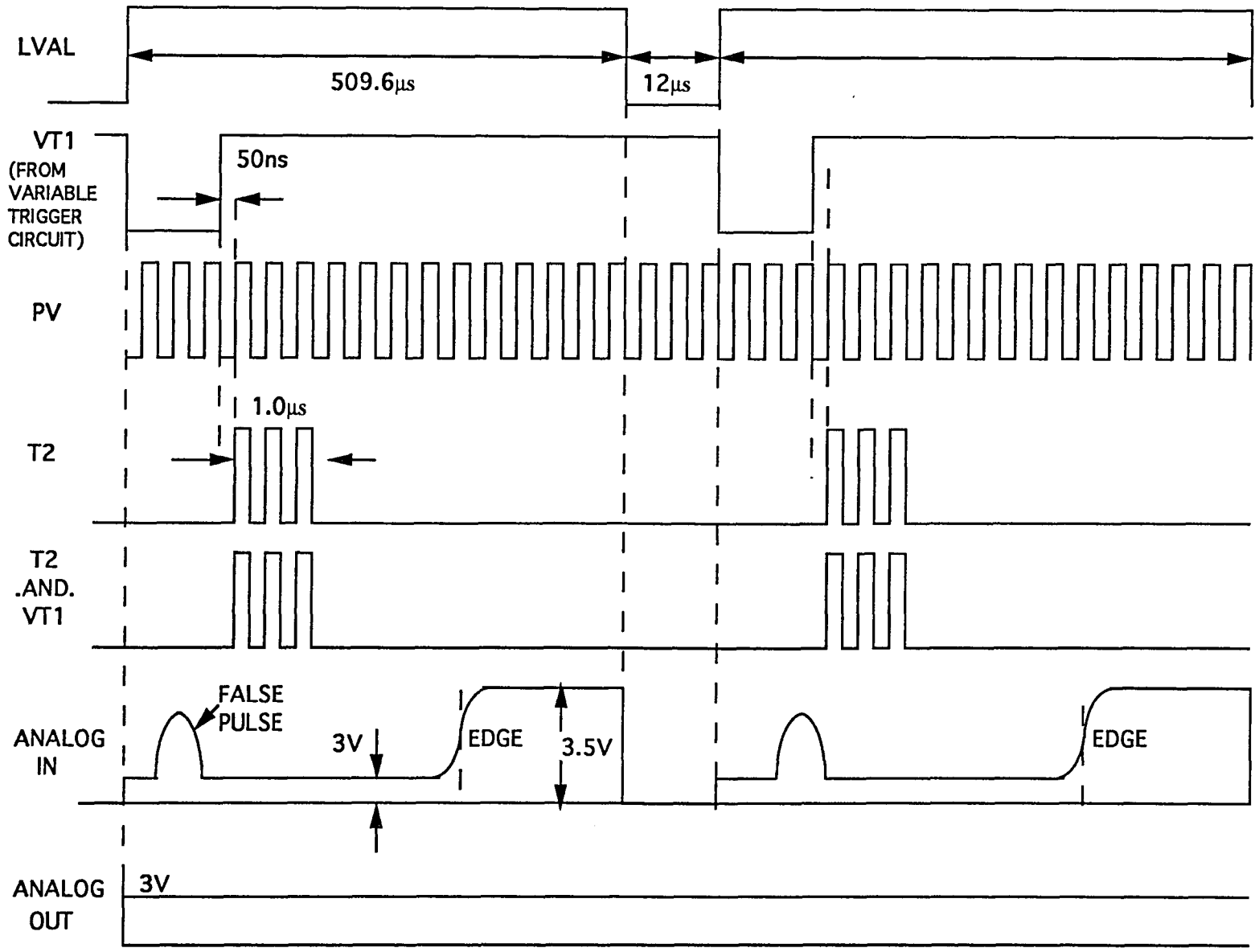


Fig 7.3 AUXILIARY CHANNEL TIMING DIAGRAM

NAND gate was provided to measure the edge of the pulse from the lighted side. This is accomplished by inverting the STO pulse. To select this option, the jumpers J1 and J3 have to be in and J2 removed. In the normal operating mode the jumper J2 is in, while J1 and J3 are out.

7.3.1 Description of the D/A pulse timing

The timing of the After Sampling circuitry is shown in Fig 7.4. The output of the differential amplifier subtracts the auxiliary channel waveform from the main channel waveform resulting in the output shown as DIFFERENTIAL OUTPUT. Note that the DC offset of the input video signal has been canceled. The DC offset has been exaggerated to 3V, with the signal rise after the edge only 0.5V. Under more probable conditions, the DC offset would be of the order of 0.5V and the signal rise of the order of 4V, which would result in the Differential amplifier having an output pulse which could be reliably converted into a digital pulse by the D flip-flop. This pulse is labeled as DFF1 OUT in the figure. The STO pulse, the inversion of the DFF1 OUT pulse, is the input to the next circuit, the digital circuit.

The timing for the optional circuitry (consisting of the additional NAND gate) is shown in Fig 7.5. The STO pulse obtained above is inverted by the additional NAND gate (numbered 2 in Fig 7.1) giving the STO^* pulse.

7.4 Description of the digital timing circuitry

The STOA pulse (ANDED STO), which was obtained from the Digital section of the sampling circuit, by ANDING the STO pulse with the LVAL pulse, generates all the timing of this circuit. Refer to Fig 7.1. The negative edge of the STOA pulse triggers the monostable 3A (pin-5), which is the monoshot 96S02 configured in the non-retriggerable mode. More details on the 96S02 are available in the National Semiconductor Data book. The Q output of mono-3A (pin-6) is connected to its positive edge triggered input (pin-4) to

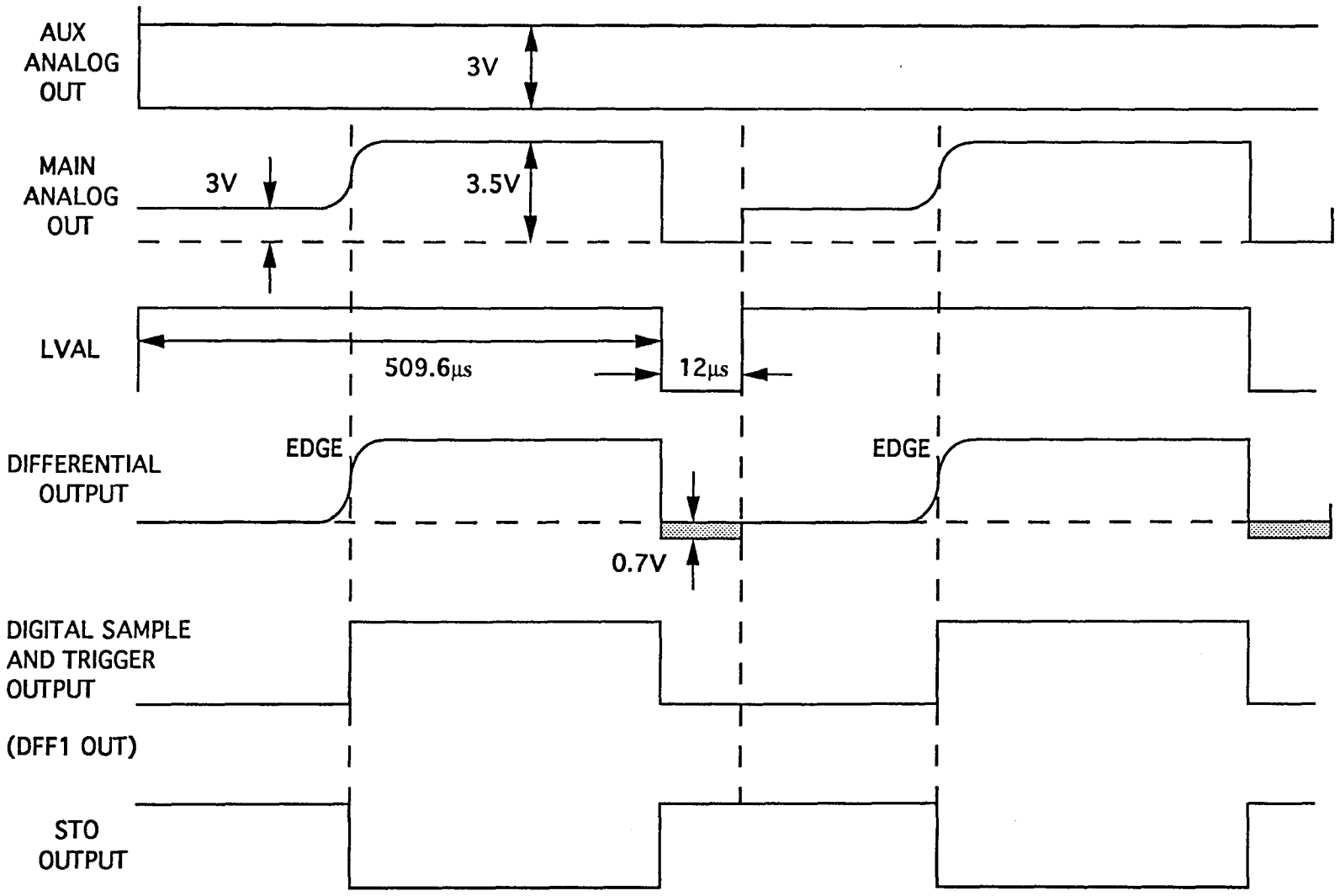
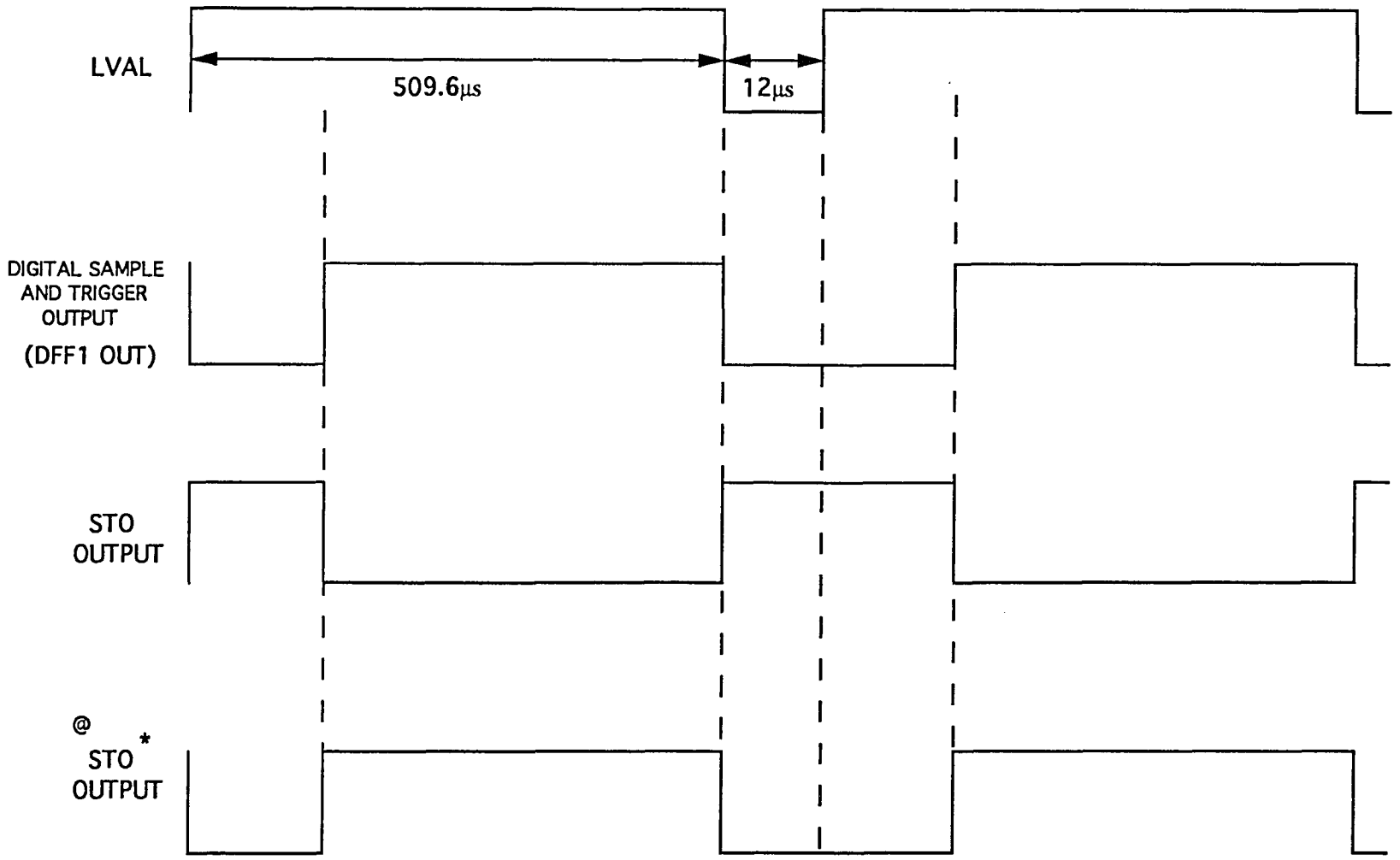


Fig 7.4 STO TIMING DIAGRAM



@ OPTIONAL (TO MEASURE REVERSE EDGE)

Fig 7.5 STO* TIMING DIAGRAM

prevent retriggering of the monoshot by a pulse occurring at the negative edge triggered input (pin-5) when its Q output is high. The negative edge of the Q output of the mono-2A triggers a monoshot 3B (pin-11) also configured in the non-retriggerable mode, which has its Q output (pin-10) connected to the positive edge triggered input (pin-12). The pulse widths of the monoshots 3A and 3B were set at 240ns and 700ns respectively by their respective resistors 4.7K(20K) and capacitors 47pf(33pf). The design equation for the pulse width, i.e. $T_X = 1.1RC$, was used.

7.4.1 Description of the digital timing diagram

As shown in Fig 7.6, the negative edge of the STOA pulse, generated in the digital circuit, triggers the mono-3A generating a pulse of 240ns. The Q^* output of the mono-3A (labeled LATCH OUTPUT) is fed to the digital circuit. The negative edge of the Q output of mono-2A triggers the mono-3B as shown by the curved arrow in the figure giving a pulse of 700ns duration. The Q^* of the mono-3B (labeled DFF OUT) is the input to the next designed circuit named the intermediate circuit.

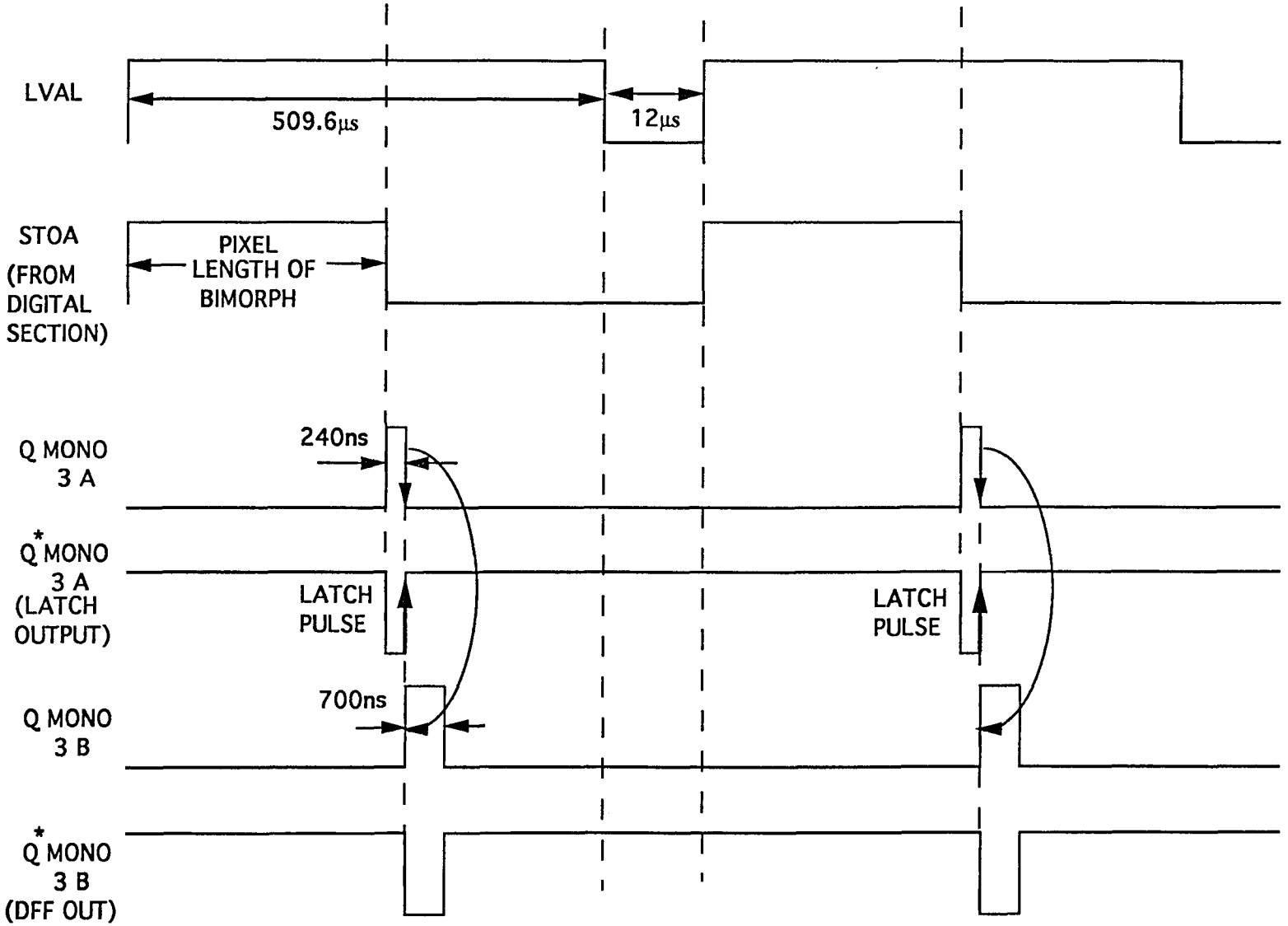


Fig 7.6 DIGITAL CIRCUIT TIMING DIAGRAM

CHAPTER 8

INTERMEDIATE CIRCUIT

8.1 Introduction

This circuit is the intermediate stage for the signals going from the sampling circuit to the digital circuit. It performs digital sampling to remove phase shift errors inherent in long distance transmission of high frequency signals. It also introduces delay in certain critical timing as discussed below.

8.2 Description of intermediate circuit

Consider figure 8.1. The output from the sampling section (the Q^* output of monoshot 3B) is fed to the D input (pin-4) of the D flip-flop DFF1 to digitally sample and synchronize the input pulse with the PV pulse, which is the clock input to the D flip-flop (pin-9). The positive edge of the output of the D flip-flop (pin-5) triggers the monoshot 4A, which is configured in the non-retriggerable mode. The Q output of the monoshot 4A was designed to be varied between 50ns and 3μs. The Q^* output of the mononshot 4A is sampled and synchronized with the PV pulse by connecting it to the input of the D flip-flop DFF2. The PV pulse is the clock input at pin-9. The output at pin-7 is given to the digital circuit.

8.2.1 Description of the intermediate timing

The timing diagram is shown in Fig 8.2. The input to this section is from pin-9 (monoshot-3B) of the sampling circuit. This pulse is synchronized with the rising edge of the PV pulse to give the pulse output of the D flip-flop DFF1. The positive edge of this pulse triggers the monostable 4A to give a Q output of 800ns. The inverse pulse (Q^*) is synchronized to the PV pulse (by the D flip-flop DFF2) and is the output of the circuit. Note that all transitions occur at the positive edge of the PV pulse as shown in the diagram by the dashed lines.

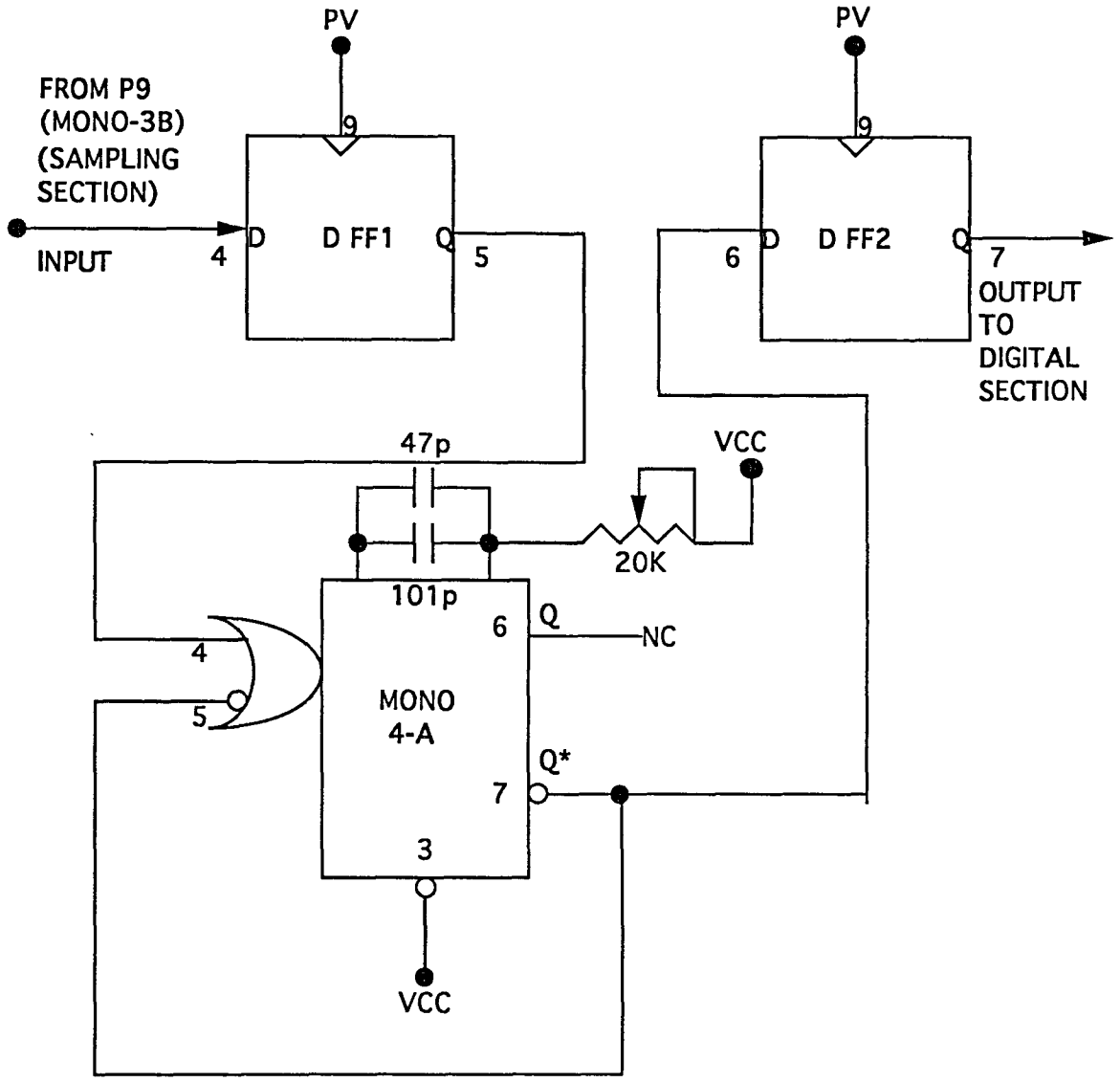


Fig 8.1 INTERMEDIATE STAGE CIRCUIT DIAGRAM

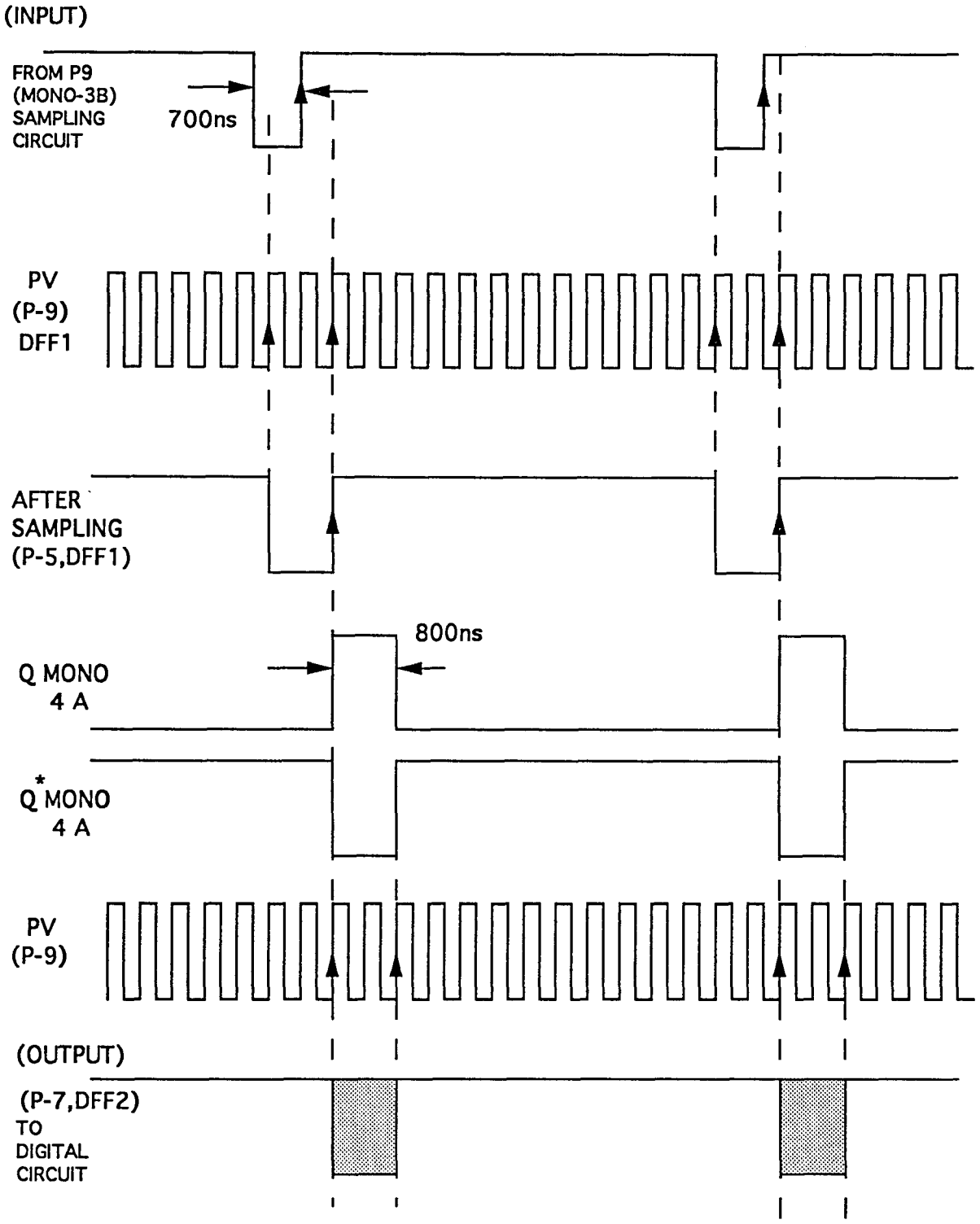


Fig 8.2 INTERMEDIATE CIRCUIT TIMING DIAGRAM

CHAPTER 9

DIGITAL CIRCUIT

9.1 Introduction

This circuit converts the pulse width modulated signal, i.e. the STOA pulse, to a voltage that is proportional to the width of the pulse. The STOA pulse width is proportional to the length of the object. The count of the PV clock during the duration of the STOA pulse gives the number of pixels blocked from the light by the bimorph, and indicates the bimorph length. The counting is done by a 12 bit counter, three 4 bit counters working in cascade, and clocked by the PV pulse. The latches used to hold the data at the end of the STOA pulse are twelve D flip-flops triggered by the LATCH OUT pulse. These latches drive a D/A converter which is used to produce an analog output, whose amplitude is proportional to the number of pulses counted during the STOA pulse width, the object length.

9.2 Description of the digital circuit

Refer to fig 9.1. The STOA pulse was generated in the digital circuit (by ANDING the STO pulse from the sampling section and the LVAL pulse by an AND gate) to shorten the signal path to the digital circuits. This gate is shown as A^* in the figure. The STOA pulse is sampled and synchronized with the PV clock by the positive edge triggered D flip-flop (74LS174) shown as DFF3 in Fig 9.1. The counting is accomplished by three 74LS161s (4 bit slices) working in cascade. These are synchronous counters with internal look-ahead carry generation. The National Semiconductor Data book has more information on them. To enable counting both the P-enable (pin-7) and the T-enable (pin-10) inputs should be in the high state. For the counter number 1, the P-enable was held at +5V (logic 1) and the T-enable was fed withthe STOA pulse coming from the output of DFF3 (pin-15), as seen in the figure. This configured the counter as the least significant bit (LSB) counter. The ripple carry output (pin-15) of the LSB counter was connected to the P-enable (pin-10) of the next

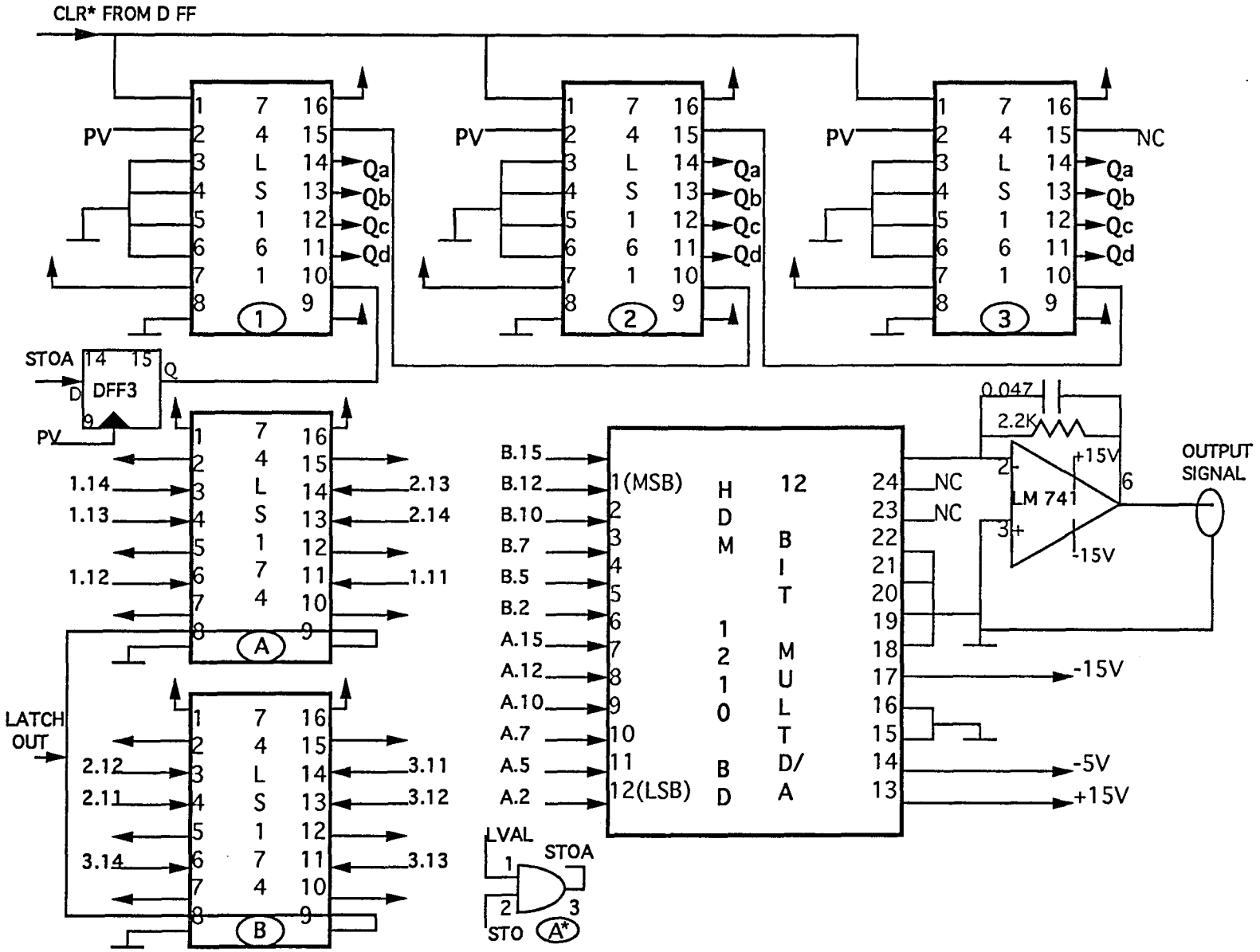


Fig 9.1 DIGITAL CIRCUIT DIAGRAM

counter, marked 2 in the figure, and so on for the last counter numbered 3. The parallel load inputs of the counters i.e. pins 3-6 were grounded as they were not used. Pin-8 was connected to the ground point and the power supply (+5V) to pin-16. The 4 bit outputs of the counters from the LSB to the MSB (most significant bit) were from pins 10-14 respectively.

The 12 bit outputs from the counters are connected to two 74LS174s (positive edge triggered D flip-flops), which serve as latches. The notation 1.14 refers to output of pin 14 of IC numbered 1, etc. The LATCH output from the sampling section is given to pin-9, the clock input of the two 74LS174s operated in parallel to simultaneously latch the 12 bits. The latch marked A carries the six LSB bits and B carries the six MSB bits. More details on 74LS174 are given in the National Semiconductor Data book. The output from the two 74LS174s are continuously fed to the digital to analog converter (DAC) 12 bit inputs.

9.2.1 Programming the HDM-1210 (DAC)

The HDM-1210 D/A converter, a high speed current output DAC, needs to be programmed with a set of input voltages to set the maximum reference current. This value would depend on the particular application. The converter has a typical settling time (settle to within 1% of final output value) and a 3dB bandwidth of 85ns and 10Mhz respectively, which is adequate for the designed motion detector. More technical specifications are in the Harris Semiconductor Data book.

Fig 9.2 shows the block diagram of the programmable part of the DAC. The value of I_{ref} is set to an optimum value. The DAC uses two analog inputs, V_{analog} (2) and V_{analog} (1), to set the reference current I_{ref} to the maximum permissible value. According to the manual for the converter this value is 1.25mA. Thus the applied voltages must not exceed certain values. A configuration using the -5V supply at V_{analog} (1) (pin-14) and 0V (ground) at V_{analog} (2) (pin-16) was used. Referring to the Fig 9.2 and applying Kirchoff's law, the maximum current value of 1.25mA is obtained with a 5V input and a

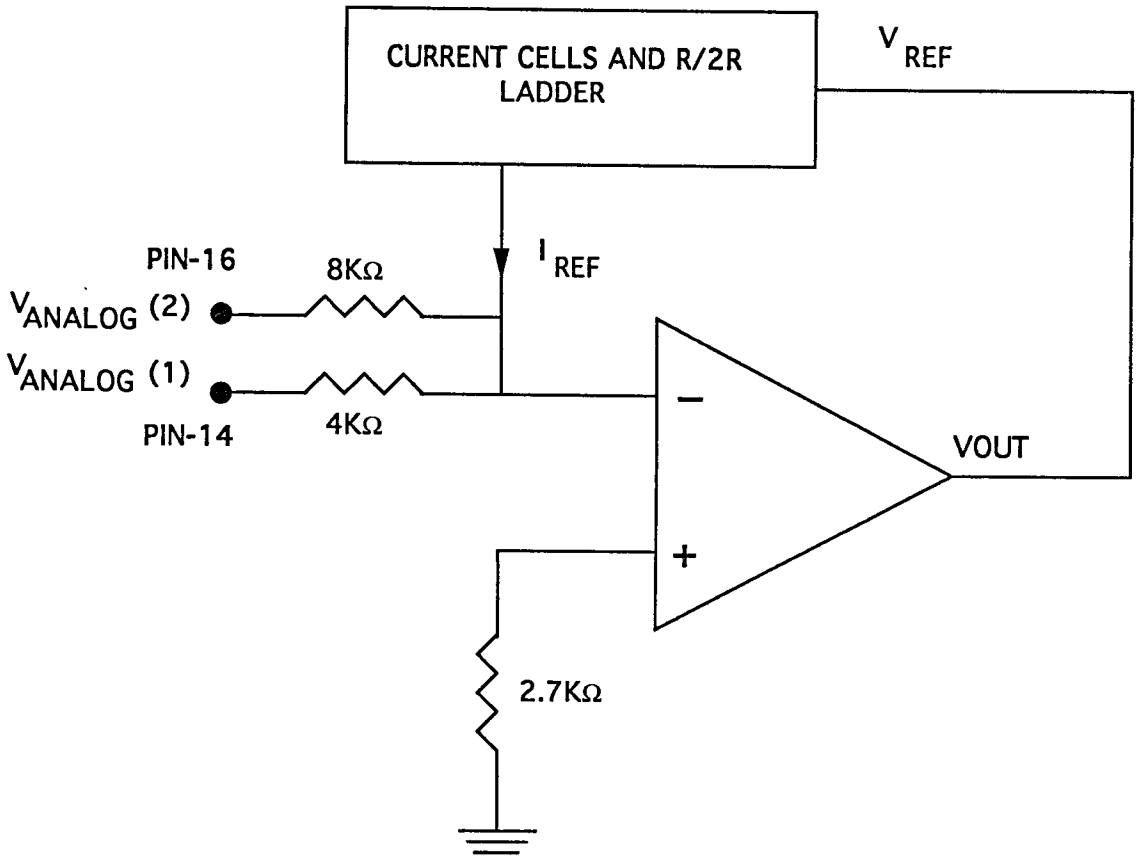


Fig 9.2 DAC PROGRAMMABLE CIRCUIT

4K resistor.

$$I_{ref} = V_{analog}(1) / 4K + V_{analog}(2) / 8K = -5 / 4K = \mathbf{-1.25mA}$$

The next part of the design was to convert the output current of the DAC into a corresponding voltage. The design incorporated an active I-to-V converter, using an LM-741A op-amp as shown in Fig 9.3. The maximum output current at the output (pin-24), 10.24mA, is obtained by multiplying the reference current, 1.25mA, by a factor of 8.192.

As may be recalled, a maximum count of 1024 occurs if the pulse width of STOA equals that of the LVAL pulse (for a 1024 pixel array). But the maximum resolution of the D/A is 12bits, corresponding to a count of 4096. Therefore the maximum output current possible is **2.56mA** (obtained by multiplying 10.24 by 1024 divided by 4096).

This maximum value of current should result in a maximum output voltage of 5V for the I-to-V converter so that it is TTL compatible.

The resistance R_{FB} of the I-to-V converter would have a value of 5V divided by 2.56mA, i.e. **2KΩ**. A value of 2.2K was selected, giving a maximum output voltage of 5.63V.

Referring to Fig 9.1, the pins (1 - 12) of the DAC are connected to the 12 bit latch (the two 74LS174s). The 0.047μf capacitor was introduced to remove the glitch noise associated with latching the 12 bits at the next line scan.

9.3 Digital timing circuit

Consider Fig 9.4. The pulse STOA generated in the digital section controls the counting operation of the three counters. As shown in the figure, the STOA pulse goes low the moment the edge of the object is detected, which freezes the 12 bit value in the three counters. The rising edge of the LATCH output (derived from the sampling section and shown as IN1) latches the 12 bit outputs of the 3 counters (74LS161s) into the 12 bit latch (two 74LS174s). The change in the DIGITAL output data is indicated in the figure by the

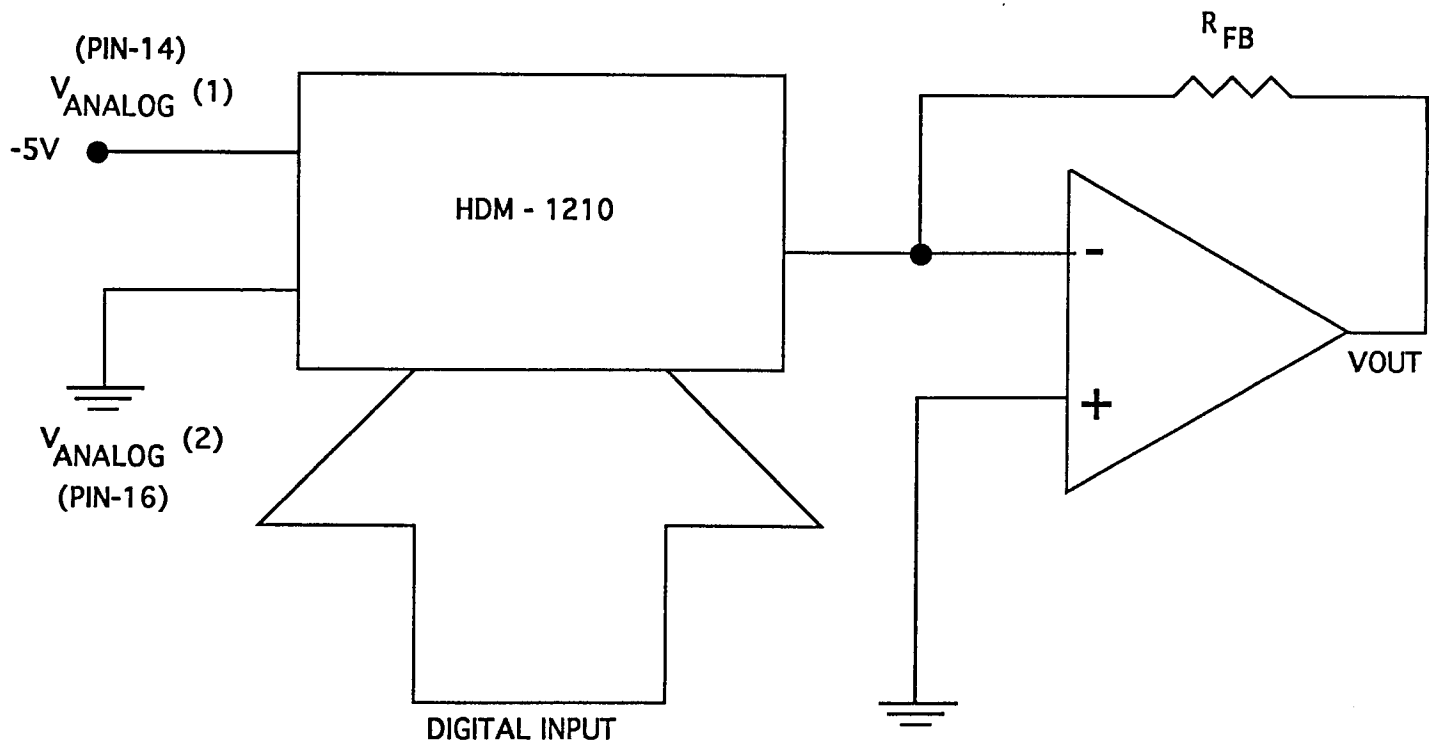


Fig 9.3 I-TO-V CONVERTOR CIRCUIT

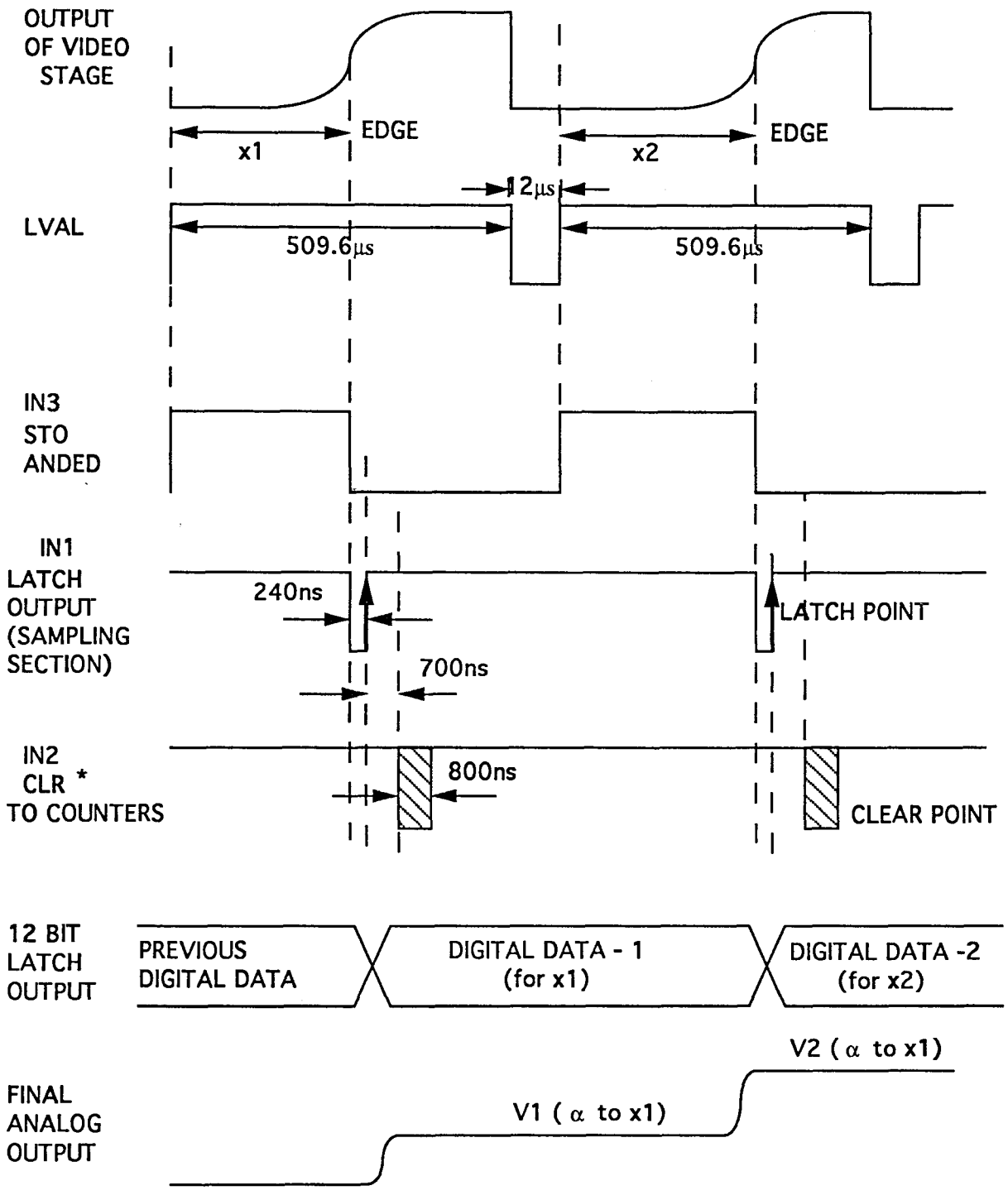


Fig 9.4 DIGITAL TIMING DIAGRAM

second last waveform. Note that the STOA pulse goes low 240ns before the latching occurs. The latching action holds the last value in the counters until they are cleared to count at the next line scan. Once latched the digital word in continuously converted into the proportional analog signal by the DAC and the I-to-V converter associated with it. The input pulse IN2, obtained from the intermediate section, clears the three counters after a period of 700ns from the time of latching. The pulse width of the IN2 is 800ns, which gives the counter adequate time to reset all the flip-flops in it so that it is ready to start afresh at the next rising edge of the LVAL pulse. This can be seen by observation of the timing diagram. Thus the output of the I-to-V converter is directly proportional to the width of the STOA pulse. Fig 9.4 illustrates this by considering two cases of STOA pulse widths, namely x_1 and x_2 where $x_2 > x_1$. The voltage output of the I-to-V converter is linearly proportional to the STOA pulse width.

The sampling frequency (F_S) of the bimorph displacement can be seen equal to the LINE SCAN RATE of the camera, which is equal to the Master clock frequency divided by the number of pixels (1024) in the image sensor, i.e.

$$F_S = 2.5\text{Mhz} / 1024 \sim= 2.5\text{Khz}$$

This limits the maximum frequency of the object displacement (F_d) that can be detected by this circuit to

$$F_d = 2.5\text{Khz} / 2 = 1.25\text{Khz}$$

using the sampling Theorem. The factor of 2 is from the Nyquist sampling criteria.

CHAPTER 10

ADDER CIRCUIT

10.1 Introduction

The purpose of this circuit is to produce a waveform indicating the point at which the sampling starts along with the analog video signal. The variable trigger circuit can then be used to adjust the point at which the sampling starts. The VT1 pulse (from the variable trigger circuit) and the analog video (from the video amplification circuit) form the inputs to this circuit.

10.2 Description of the adder circuit

Consider Fig 10.1. The circuit consists of an LM-741A opamp, configured in the differential mode. As may be recalled, the gain of such a configuration is determined by the resistive combination of R1 and R2, i.e. the output voltage V_{out} is equal to R2 multiplied by the differential voltage (V2 - V1) divided by R1. As shown in the Fig 10.2, If R1 = R2 then the above circuit functions as a subtracter giving an output voltage, V_{out} = V2 - V1. This is the principle used to superimpose the two input signals. Reconsider Fig 10.1. The signal given to the non-inverting input is the analog video derived from the video amplification circuit. The signal given to the inverting input is the inverse of the VT1 pulse, derived from the variable trigger circuit. From experience the resistors were chosen to be 10K, to reduce the loading of the outputs connected to the inverting and the non-inverting inputs of this op-amp subtractor. The output of the op-amp (pin-6) is the algebraic sum of the two input signals.

10.2.1 Description of the adder circuit timing

The purpose of the adder circuit is to generate a composite pulse which serves to

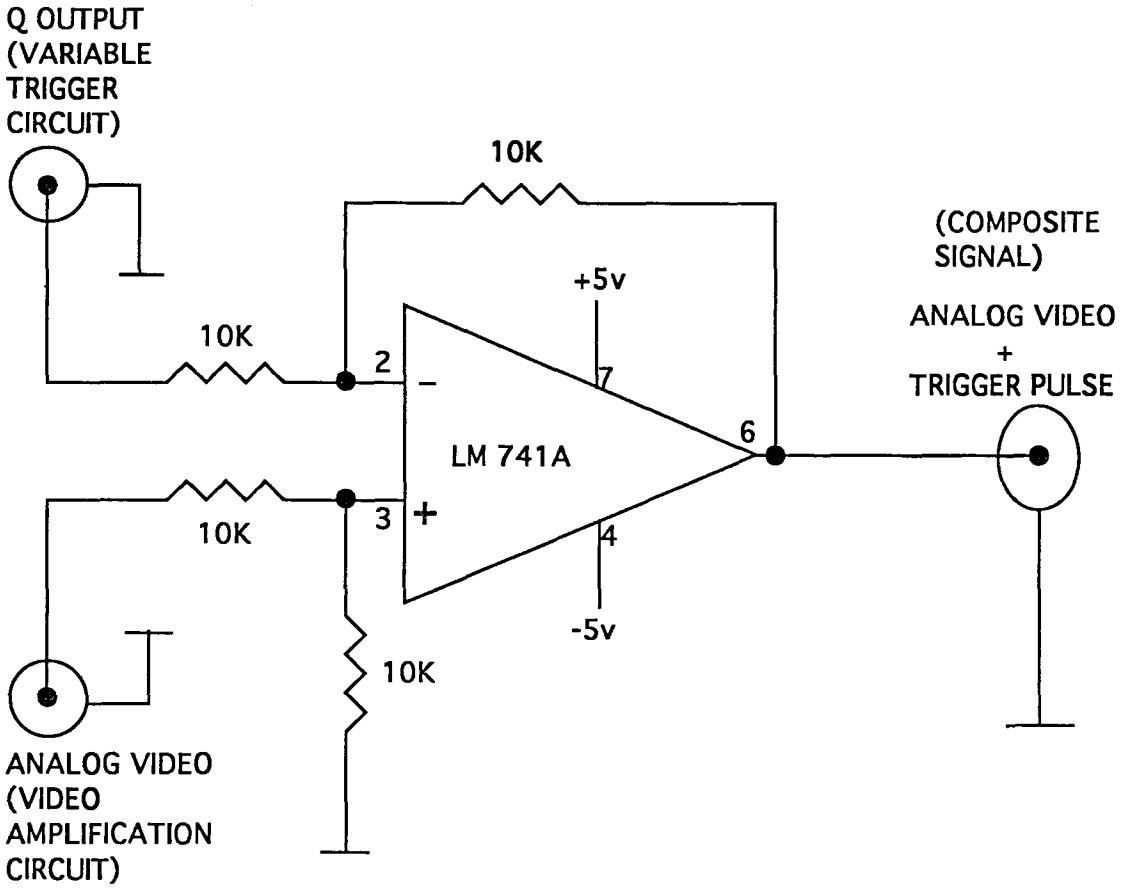


Fig 10.1 ADDER CIRCUIT DIAGRAM

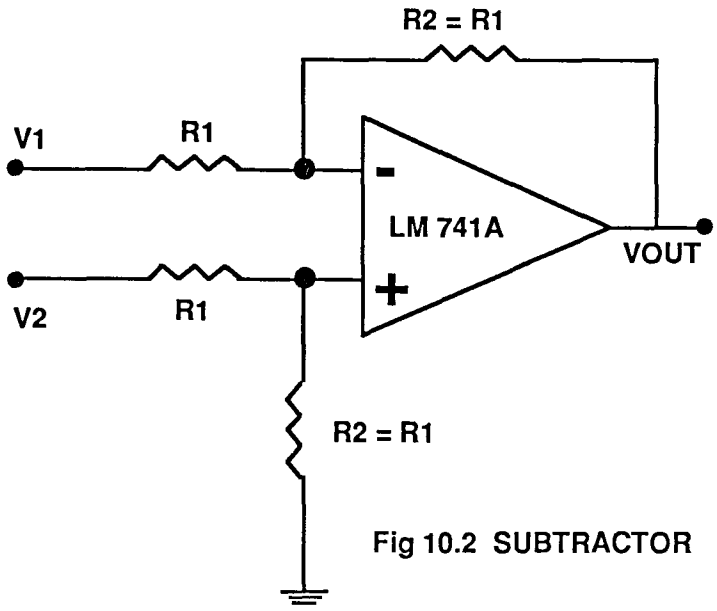


Fig 10.2 SUBTRACTOR

synchronize external devices such as a monitor, to the image grabber subsystem. Fig 10.3 shows the Timing diagram. The signal given to the non-inverting input is the analog video, labeled as IN2. The inverting input is fed with the inverse of the VT1 pulse ($VT1^*$) labeled as IN1. The LVAL pulse has also been shown.

As shown in the figure the ($VT1^*$) pulse is subtracted from the analog video. The output of the adder op-amp (pin 6 in fig 10.1) contains the subtracted signals. The leading edge, marked by the upward arrow, indicates the point at which the sampling starts. Using this composite signal, the start of sampling could be located at a point beyond the occurrence of the false pulse, as indicated in the Fig 10.3.

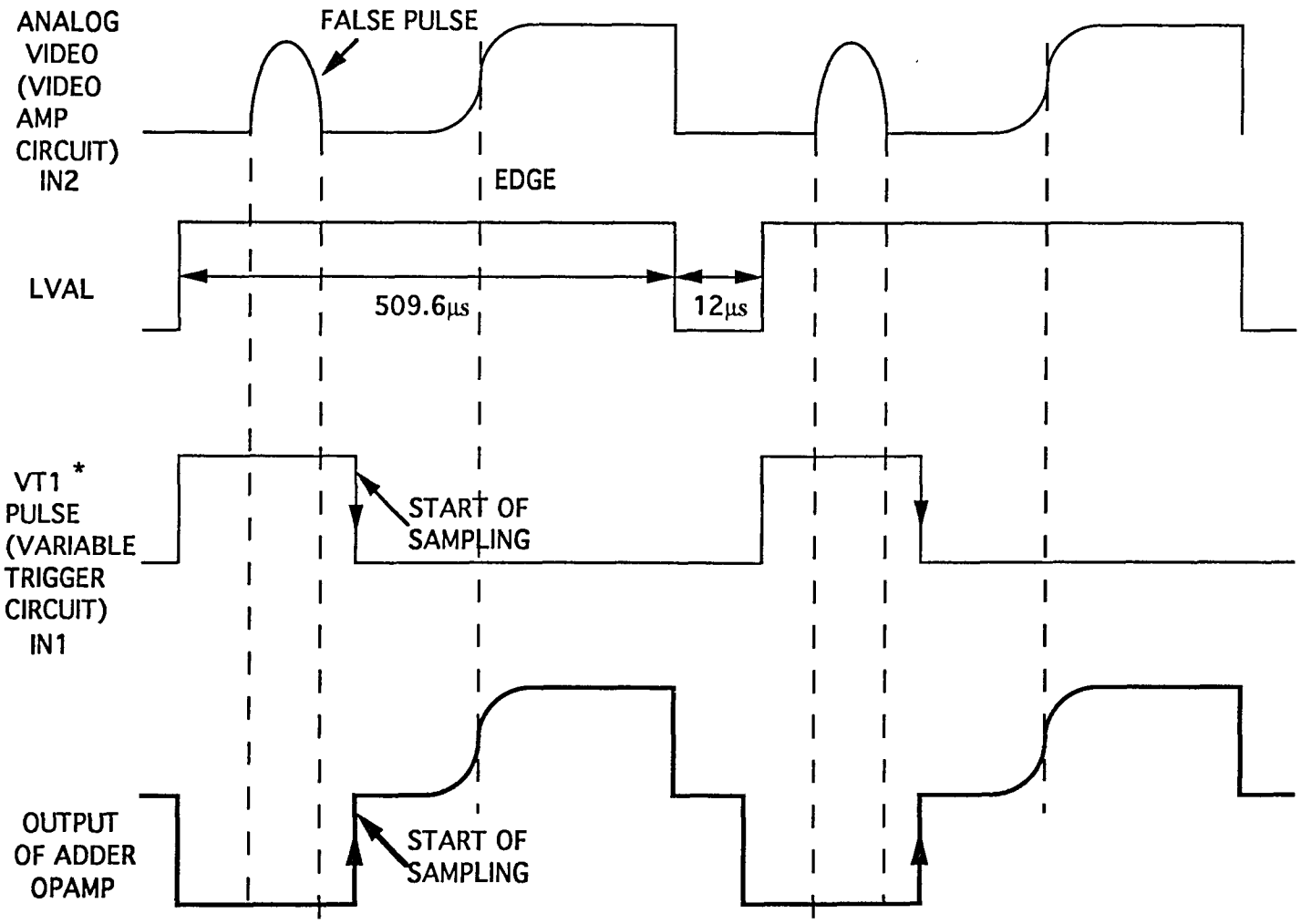


Fig 10.3 ADDER TIMING DIAGRAM

CHAPTER 11

EXPERIMENTAL PROCEDURE AND RESULTS

11.1 Experimental procedure

To test the operation of the designed system, measurements of the pulse waveforms at the critical points of the system were taken under different input conditions, i.e. with the light illuminating five different pixel segments of the linear CCD array. Fig 11.1 shows the portion of the 1024 pixel array not blocked, i.e. for one input condition. The position of the opaque object was controlled by the placement of a stand holding the object, as shown in the figure. The length of the illuminated pixels was varied by gently pushing the stand; five input conditions were randomly chosen.

The frequency response of the designed system was studied by exciting a bimorph at audio frequencies in the 0 to 20Khz range using a sweep generator. The output voltage was measured for each of the input frequencies and a FFT Transformer was used to display the spectral response on a monitor and to record this response using a digital recorder. The digital recorder was connected to the FFT Transformer.

11.2 Description of measured waveforms

Fig 11.2.1 shows the waveform at the output of the first stage in the video amplification stage. The voltage swing is of the order of 300mV and there is a DC offset of 122mV. The noise seen riding on the pulse is due to partial signal rejection at the input of the first op-amp.

The analog video signal at the output of the second stage of amplification is shown in Fig 11.2.2. The voltage swing is of the order of 2.2V. The noise is considerably reduced due to the differential mode of the op-amps. The rise time of the waveform is approximately 0.1 times the time per division i.e. 0.1 x 100μs = 10μs.

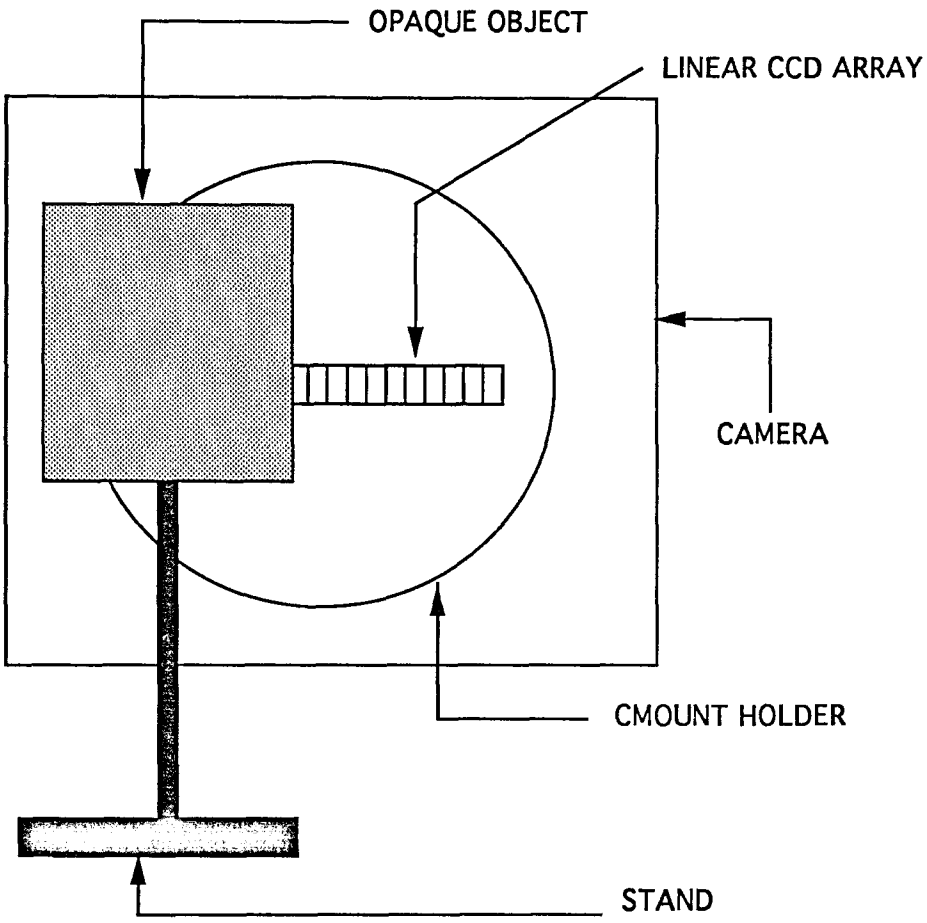


FIG 11.1 FRONT VIEW OF THE EXPERIMENTAL SET-UP

Fig 11.2.3 shows the analog video signal at the output of the third stage of amplification. The voltage swing is of the order of 4.2V. The output from the third stage is seen to be almost devoid of noise. The noise voltages seen riding on the waveforms are of the order of 20mV, which can be neglected, since the signal voltage level at this output is of the order of 4V, giving a signal-to-noise ratio of 46dB.

Figs 11.2.4 - 11.2.8 show five outputs for five input conditions, which corresponded to having five different pixel length segments illuminated with light. The period of the pulse waveforms is of the order of 320μs, which is smaller than the stipulated width of 400μs, corresponding to a Master clock frequency of 2.5Mhz. As previously pointed out the five positions were randomly chosen. It may be seen that the part of the waveforms (low voltage with only DC offset) represent the pixels covered by the opaque object. Note that there is a gradual change in the voltage from low to high at the edge of the object and it occurs over a duration of about 5μs. This transition time can be attributed to the partial transparency of the bimorph.

Fig 11.2.9 shows the LVAL and the PV signals, as inputs to the image grabber subsystem from the line controller. The period of the LVAL pulse can be seen to be of the order of 320μs, corresponding to a master clock frequency of 3.2Mhz, which exceeds the expected value of 2.5Mhz by a factor of 1.28.

Fig 11.2.10 is the same waveform as for Fig 11.2.9 except that the time scale is expanded. The waveform was recorded in the logic mode and thus does not show the rise and fall times of the PV pulse.

Fig 11.2.11 shows the PV signal. The ringing is due to small mismatches of the transmission line impedance of the co-axial cables used for transferring the signal from the line controller to the I.G. subsystem. Also the inability of the driver stage in the Line controller to drive the capacitive loads on the circuit board of the I.G. arising from the $C^{dV}/_{dt}$ effect.

Fig 11.2.12 shows the sample pulse given to the SAMPLE-AND-HOLD amplifier of the MAIN channel in the sampling section. The ringing of this pulse is seen to be reduced compared to the PV pulse due to the buffering done by the AND gate (as this waveform is the ANDED signal of the VT1 pulse and the T1 pulse) .

The sampling pulse of the above figure (channel 2) and the PV signal (channel 1) is shown in Fig 11.2.13. This figure shows the portion of the signals before the start of sampling and after the rising edge of the LVAL pulse. The sampling pulse is low since the start of sampling has not occurred.

The PV signal (channel 1) and the Sampling pulse (channel 2) applied to the MAIN channel are shown in Fig 11.2.14. Unlike fig 11.2.13 it shows the portion of the waveforms after the start of sampling. The ringing is due to the capacitive loading of the signals.

The output of the Differential Amplifier in the Sampling section (channel 2) and the analog input to the sampling section (channel 1) is shown in Fig 11.2.15. Note that the auxiliary channel (the channel sampling the DC offset) could not be implemented in the actual design. The output of the Differential amp is however referenced to ground as seen in the figure. This is accomplished by adjusting the DC offset in the Video amplification section.

Fig 11.2.16 shows the waveform in Fig 11.2.15 (channel 2) on an expanded time scale.

Fig 11.2.17 shows the output of the 74LS174 (Schmitt trigger and digital sampler) in the sampling section. As seen this waveform has a very fast rise time that could not be measured with the oscilloscope used. This is due to the digital sampling performed by the D flip-flop (74LS174) on its input waveform, the waveform in Fig 11.2.16.

Fig 11.2.18 - Fig 11.2.21 show four cases of the STOA pulse corresponding to four different pixel length segments of the linear CCD array blocked by the opaque object. Note the reversal of polarity between the STOA pulses and the waveforms in Figs 11.2.15

- 11.2.17. The noise riding on the STOA pulses has no effect on the performance as only the pulse widths are of significance and not the voltage level of the pulses, an inherent advantage of such a conversion (analog voltage signal to a pulse width modulated signal).

Fig 11.2.22 - 11.2.23 show the critical timing waveforms of the LATCH OUT, CLR OUT and the STOA pulses. Fig 11.2.23 is the expanded version of Fig 11.2.22. The first waveform labeled PWM is the STOA pulse, which triggers the LATCH ALL (LATCH OUT) pulse to load the counter value into the 12 bit latch at the rising edge of its pulse. The width of the LATCH OUT pulse is seen to be of the order of 20μs. The gap between the CLR OUT (clear pulse to the 12 bit counters) and the rising edge of the LATCH OUT signal is of the order of 44.1μs.

Fig 11.2.24 shows the LATCH OUT pulse by itself. The rise time is less than what could be measured in the oscilloscope. The voltage swing of the pulse is close to 4V.

Fig 11.2.25 shows the DFF OUT waveform, which forms the input to the intermediate circuit. The pulse width of the waveform is relatively large (20μs). However this pulse is used to trigger the monoshot in the Intermediate circuit which generates the CLR OUT pulse.

Fig 11.2.26 shows the inverse of the CLR OUT waveform (Intermediate circuit). The voltage swing is of the order of 4V, which is TTL compatible. The rise time of the waveform could not be measured in the oscilloscope used.

Fig 11.2.27 shows the output pulse of the intermediate circuit before the digital sampler (D flip-flop). Note that the pulses are of uneven magnitude. This is believed to be caused by the effect of transmission line capacitance on the pulse.

Fig 11.2.28 shows the CLR OUT pulse (the output from the Intermediate circuit), which is used to reset the 12 bit counters. The amplitudes of the consecutive pulses are the same.

Fig 11.2.29 shows the output of the adding circuit, the COMPOSITE pulse. This waveform is composed of the inverted VT1 pulse added on to the analog video signal. The

waveform distortion is due to the digital mode of the Oscilloscope and is not present in the waveform. The leading edge of the inverted VT1 pulse (negative half of the waveform) is the point at which the sampling starts.

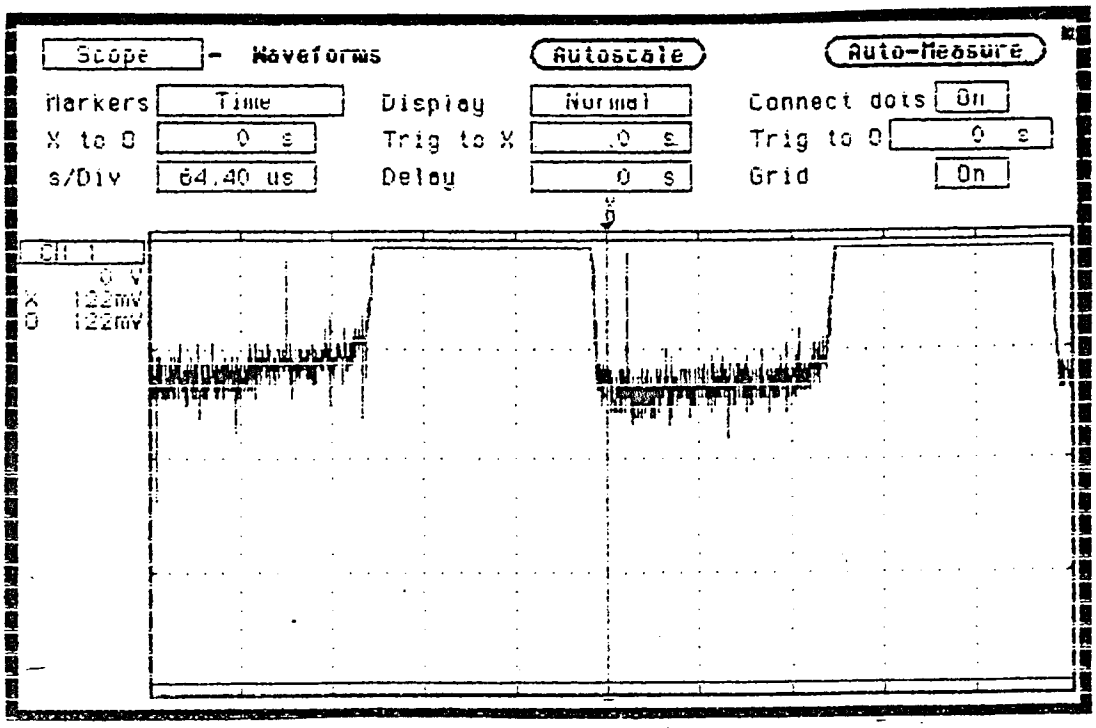


Fig 11.2.1 FIRST STAGE OUTPUT

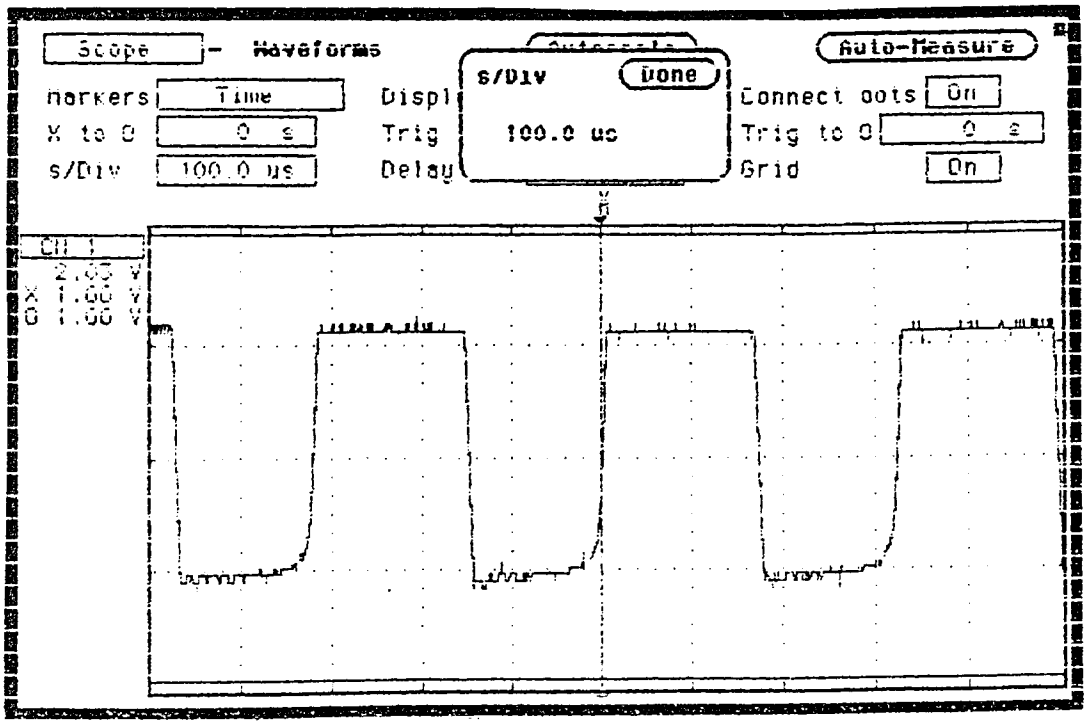


Fig 11.2.2 SECOND STAGE OUTPUT

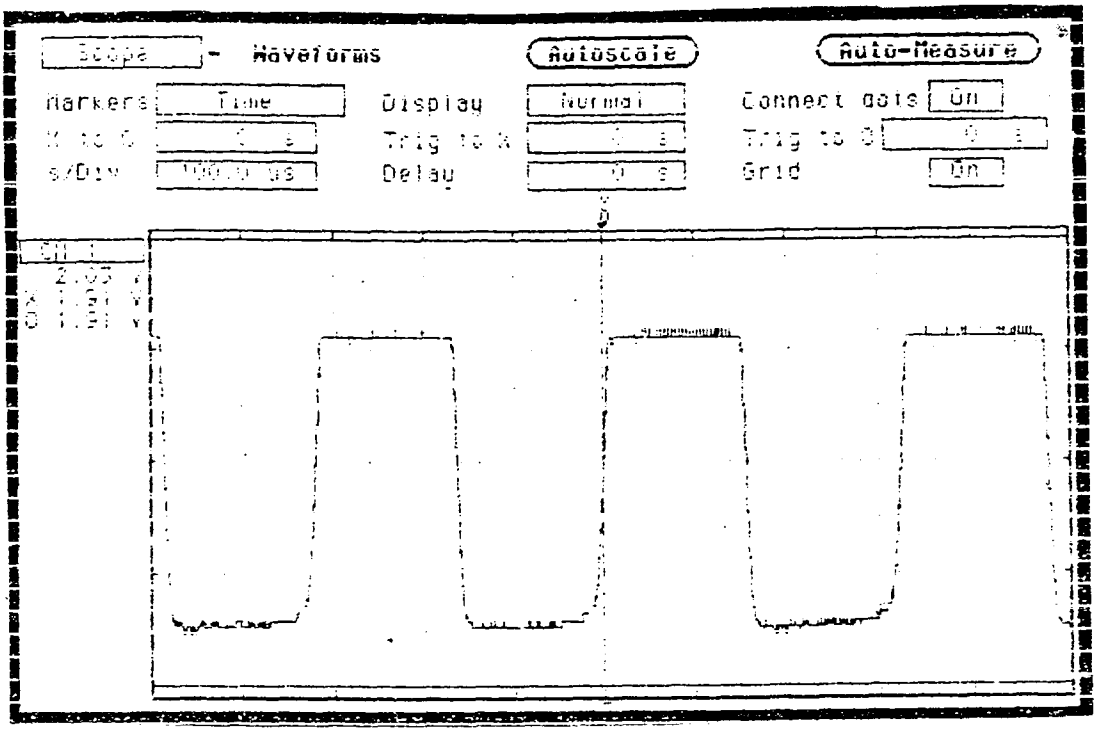


Fig 11.2.3 THIRD STAGE OUTPUT

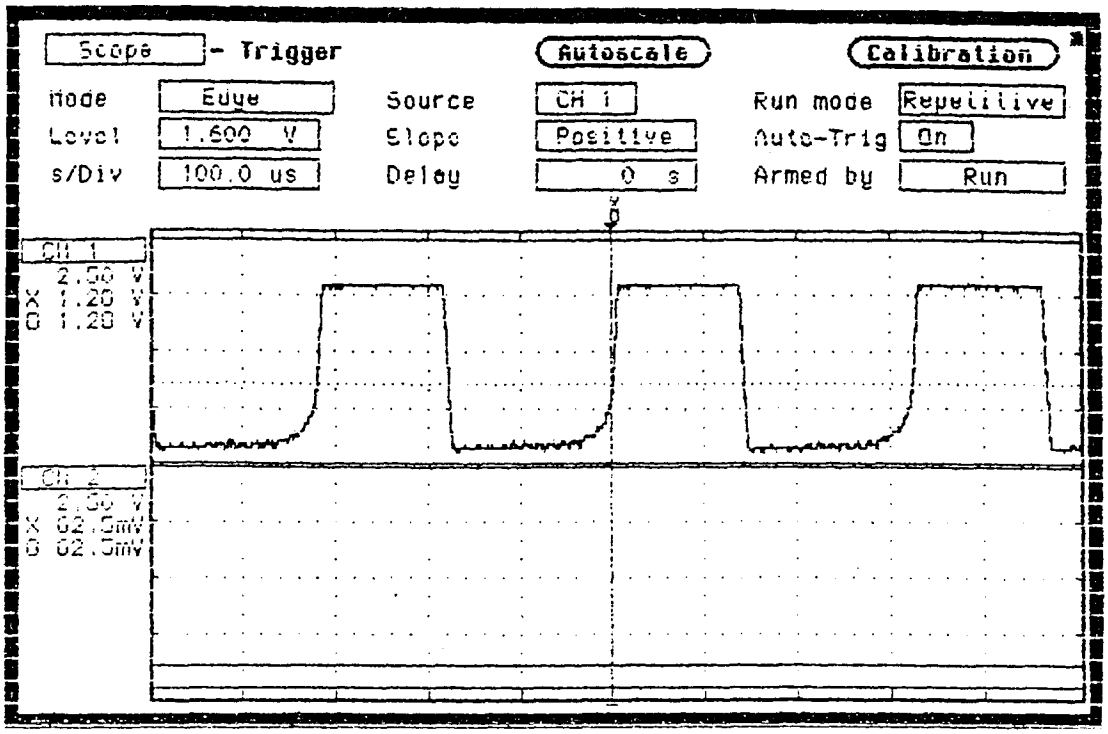


Fig 11.2.4 OUTPUT OF THIRD STAGE (CASE 1)

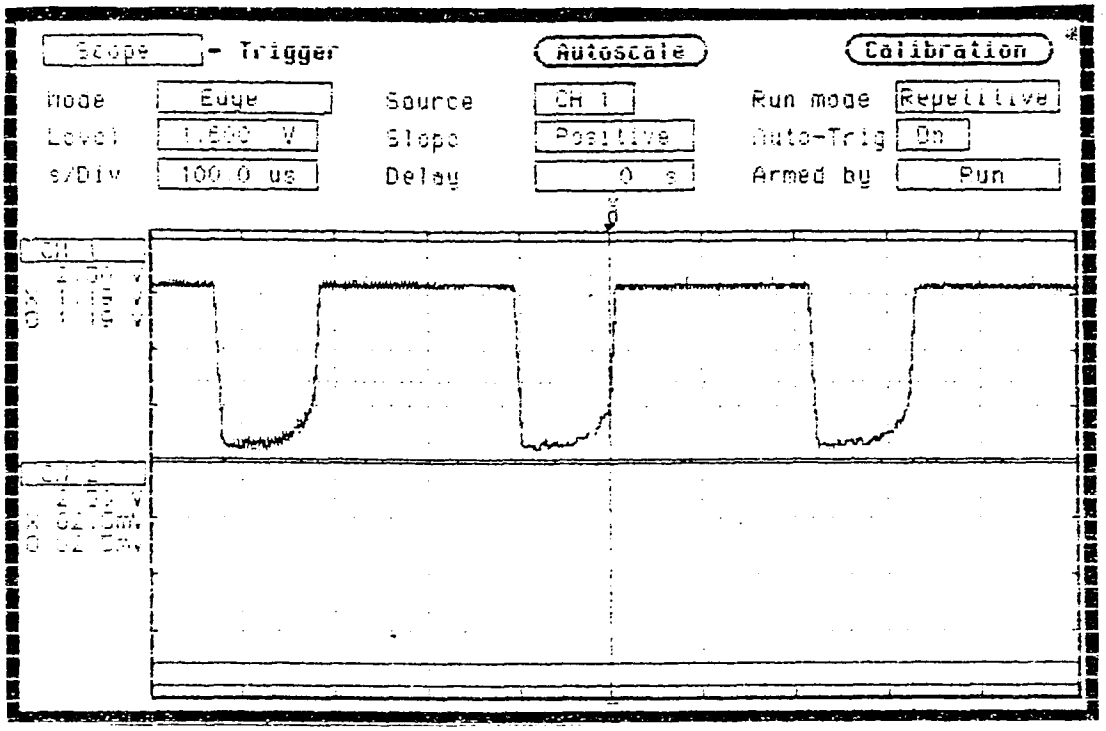


Fig 11.2.5 OUTPUT OF THIRD STAGE (CASE 2)

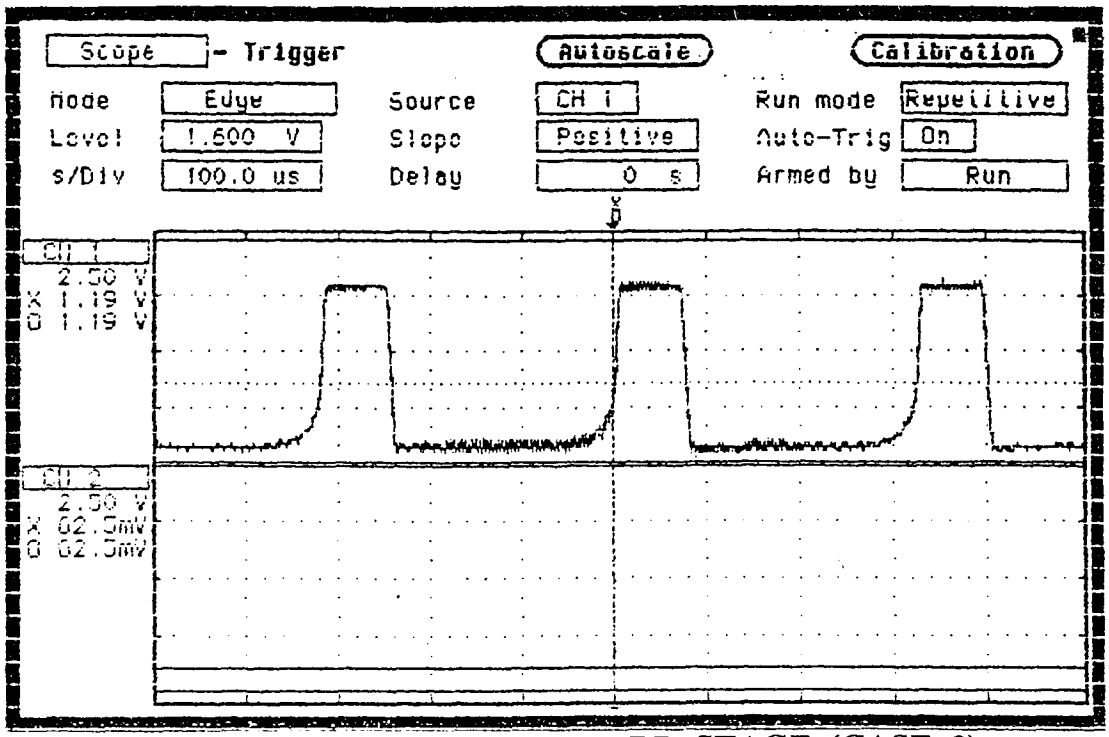


Fig 11.2.6 OUTPUT OF THIRD STAGE (CASE 3)

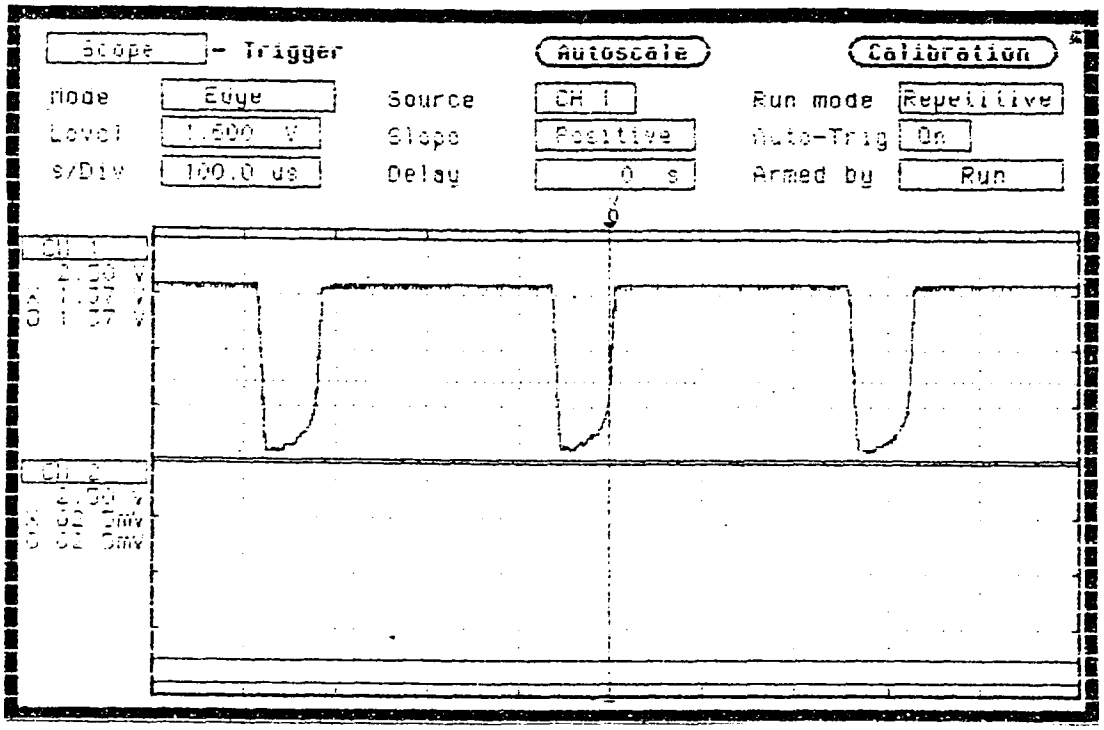


Fig 11.2.7 OUTPUT OF THIRD STAGE (CASE 4)

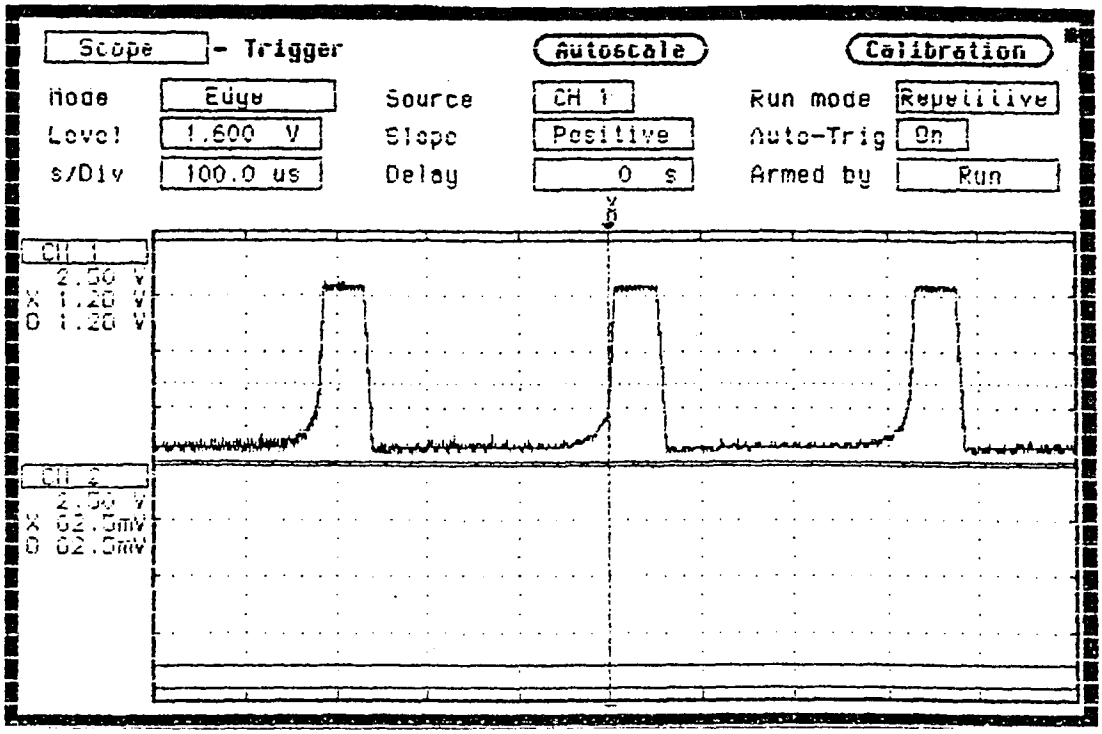


Fig 11.2.8 OUTPUT OF THIRD STAGE (CASE 5)

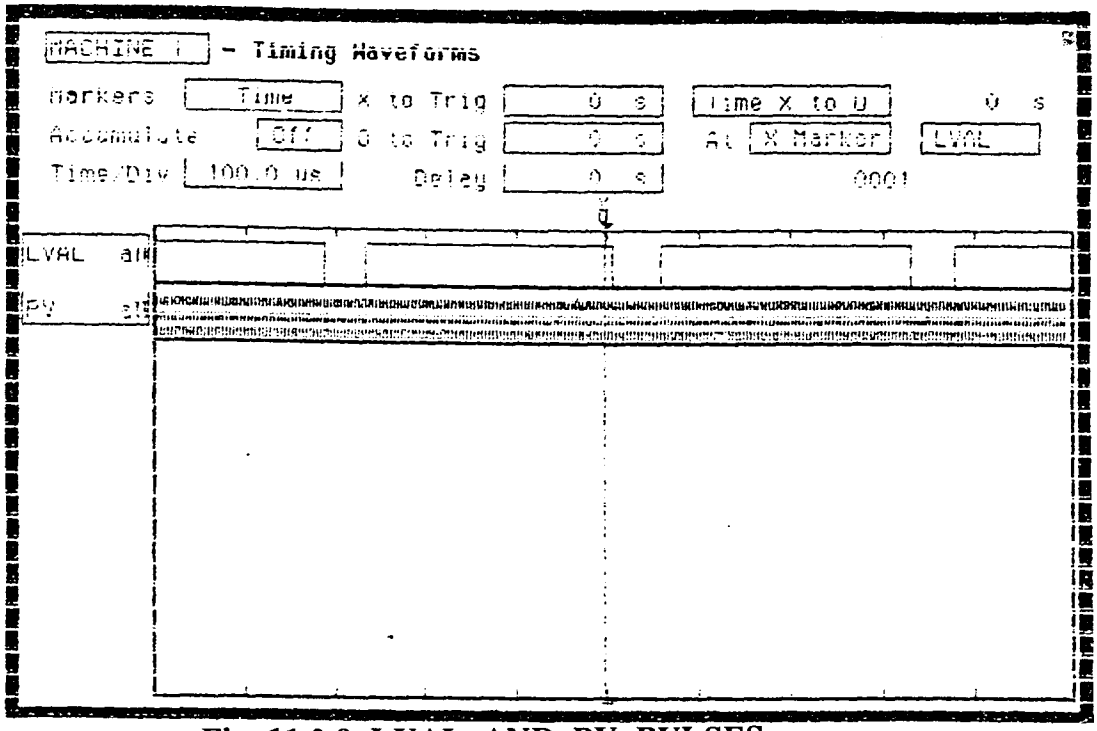


Fig 11.2.9 LVAL AND PV PULSES

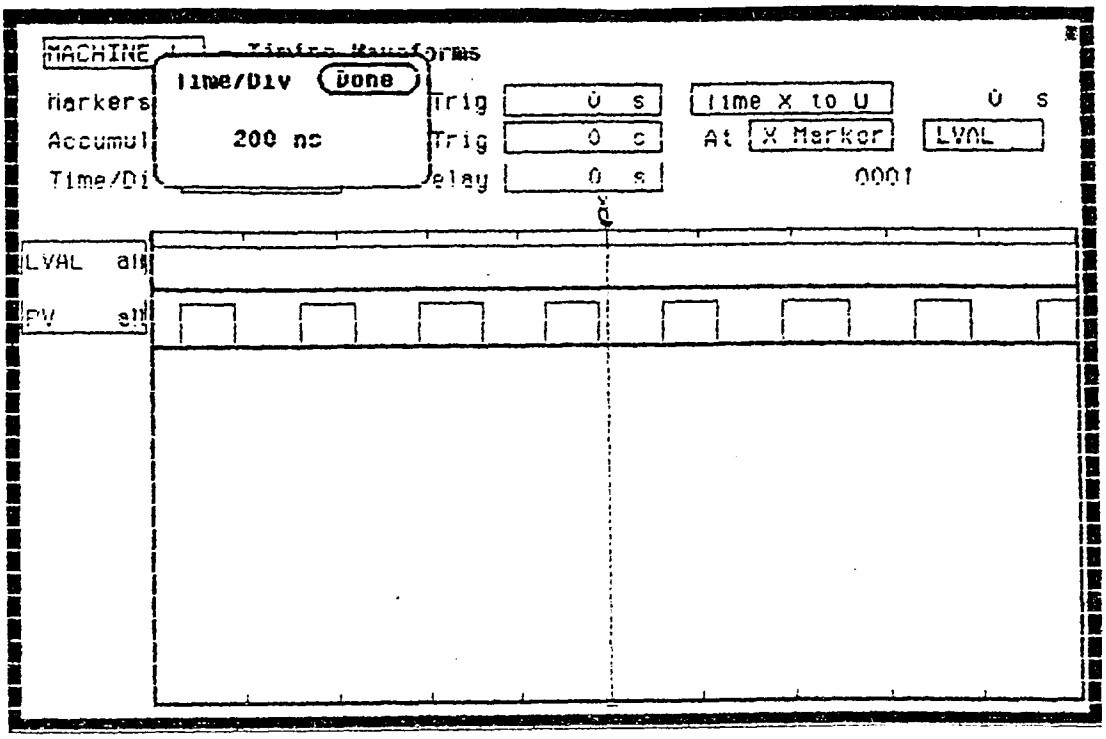


Fig 11.2.10 LVAL AND PV PULSES (EXPANDED)

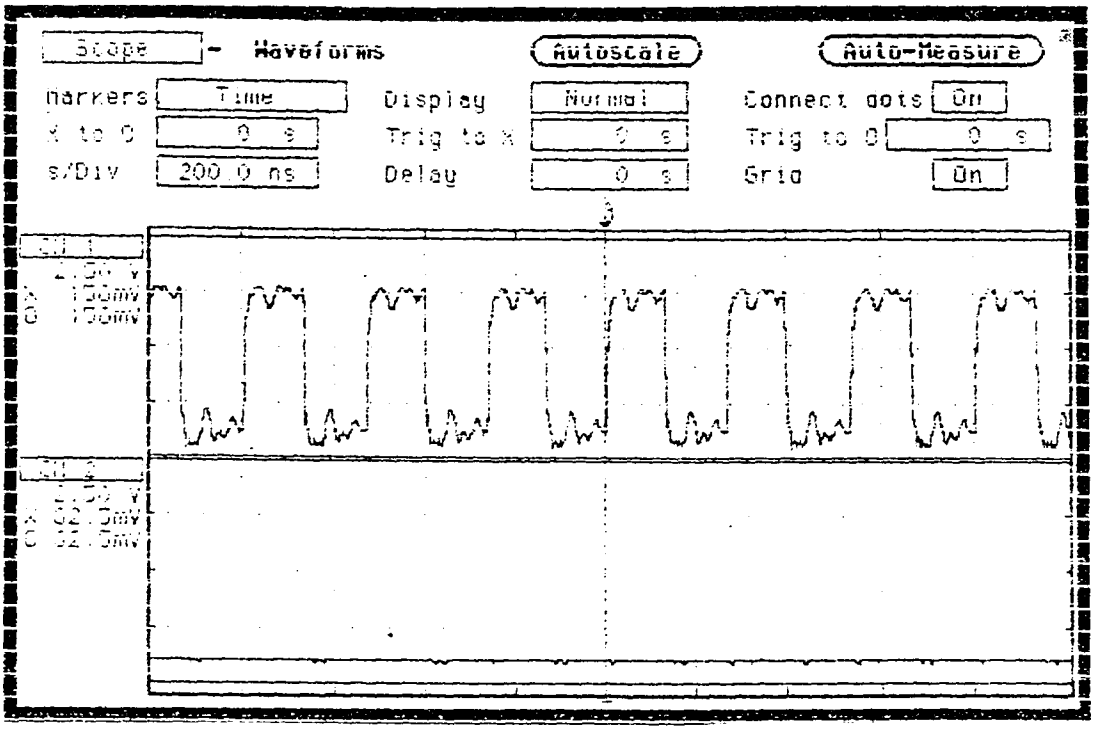


Fig 11.2.11 PV PULSE

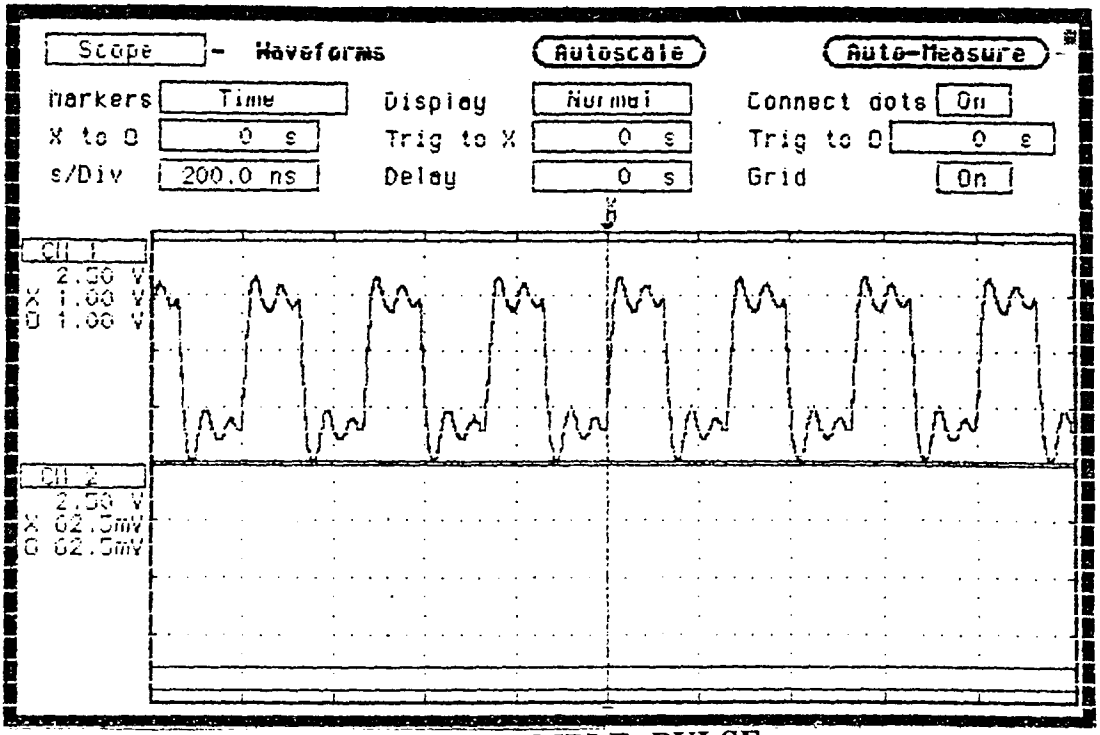


Fig 11.2.12 SAMPLE PULSE

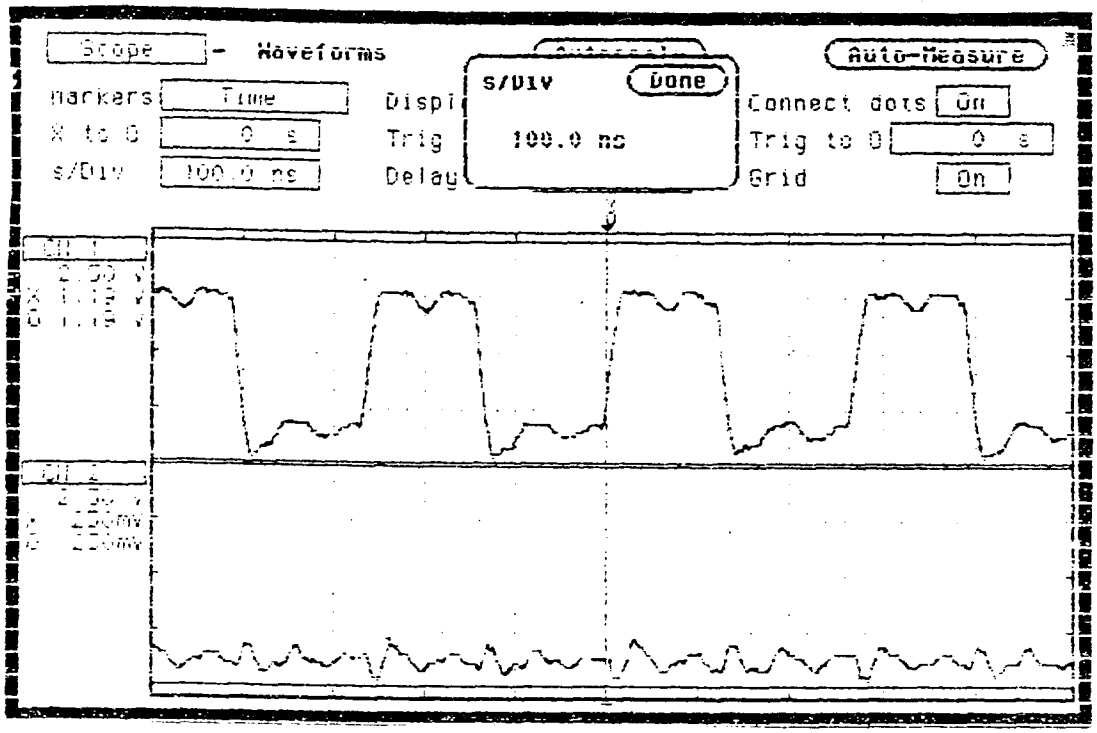


Fig 11.2.13 SAMPLE PULSE (CH-1) AND PV PULSE (CH-2)

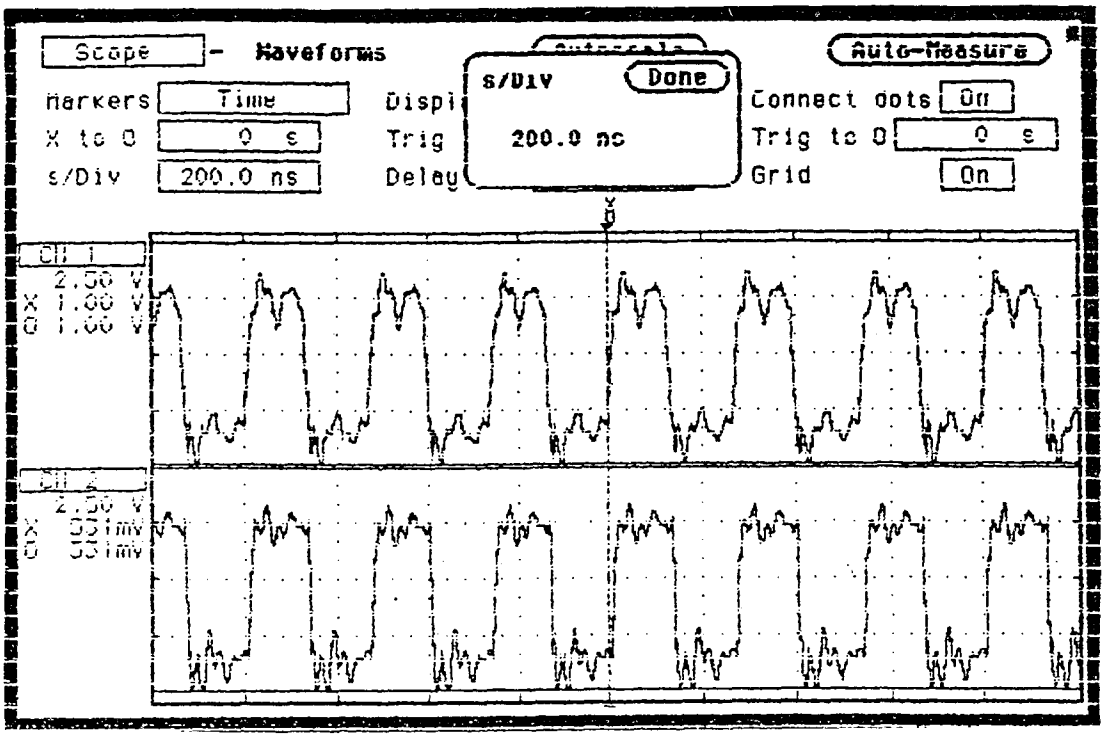


Fig 11.2.14 PV PULSE (CH-1) AND SAMPLE PULSE (CH-2)

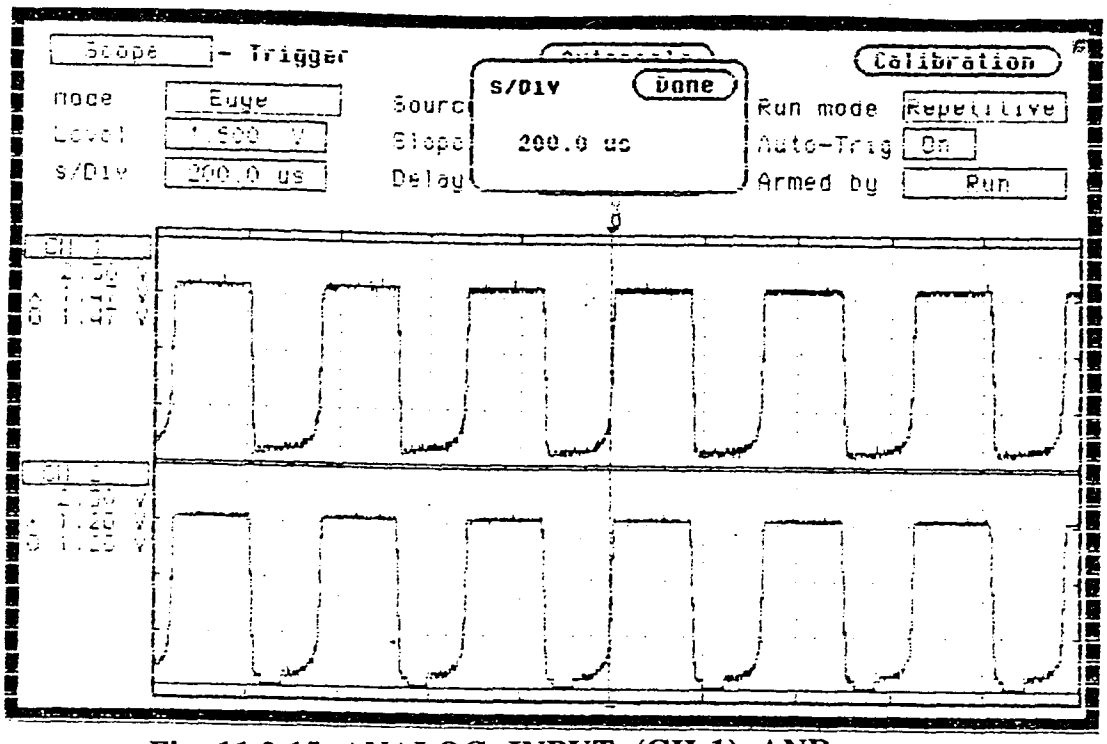


Fig 11.2.15 ANALOG INPUT (CH-1) AND DIFF AMP OUT (CH-2)

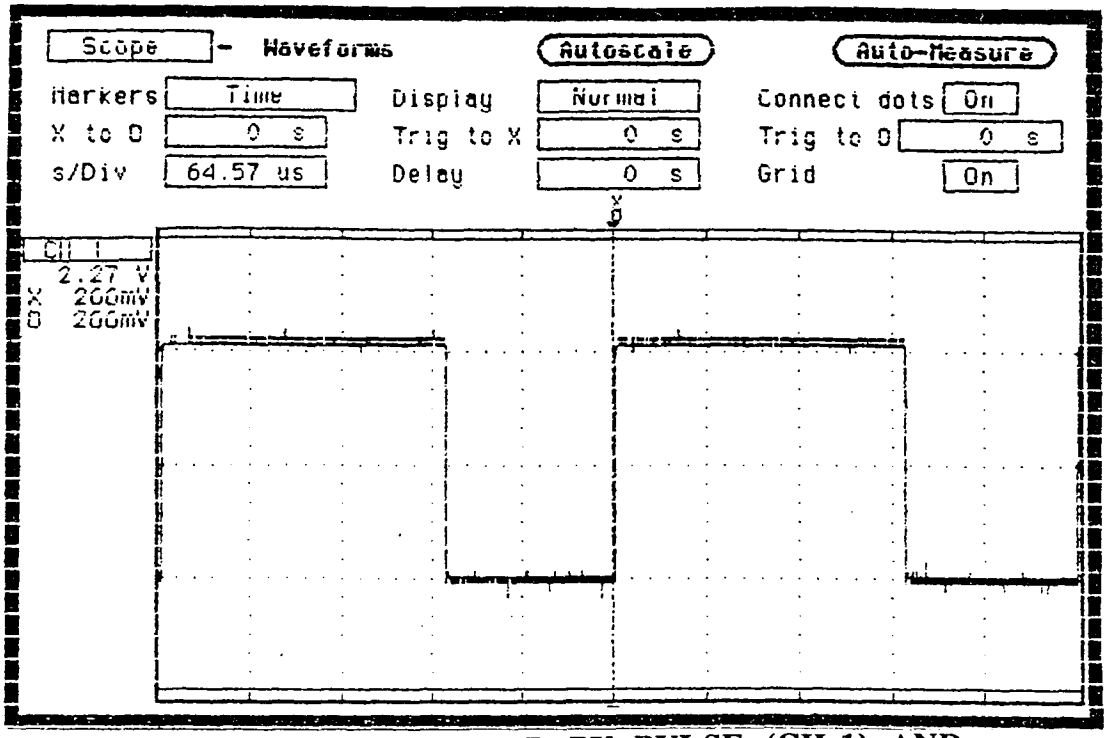


Fig 11.2.16 EXPANDED PV PULSE (CH-1) AND SAMPLE PULSE (CH-2)

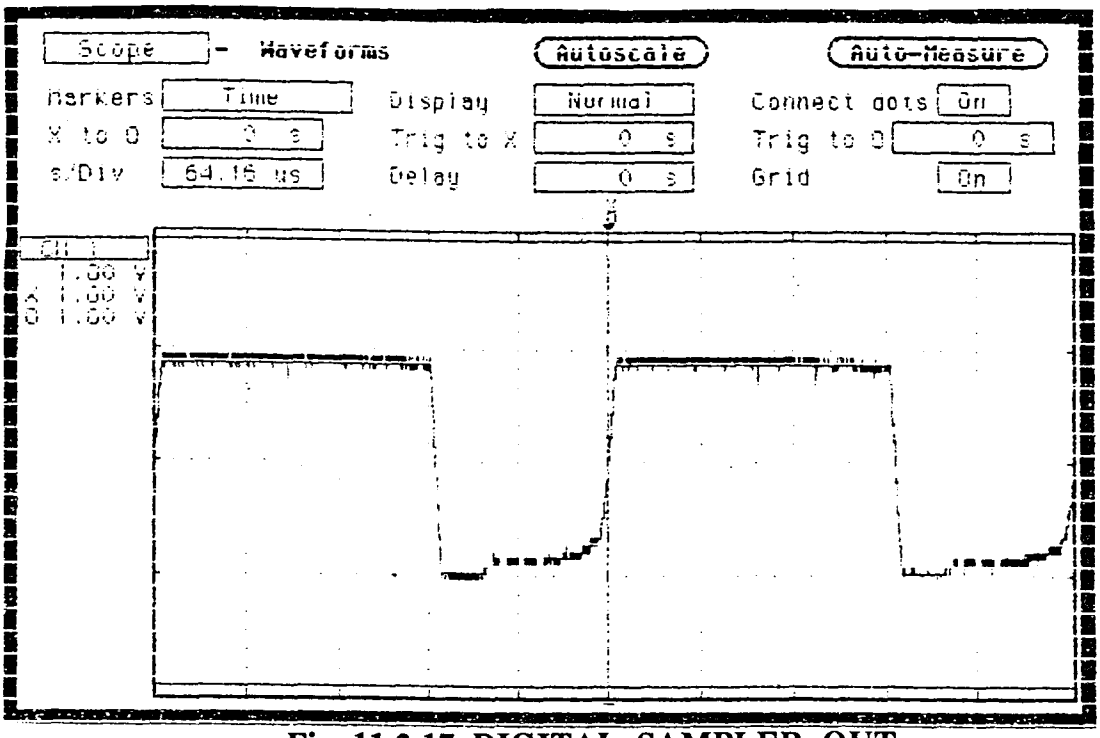


Fig 11.2.17 DIGITAL SAMPLER OUT

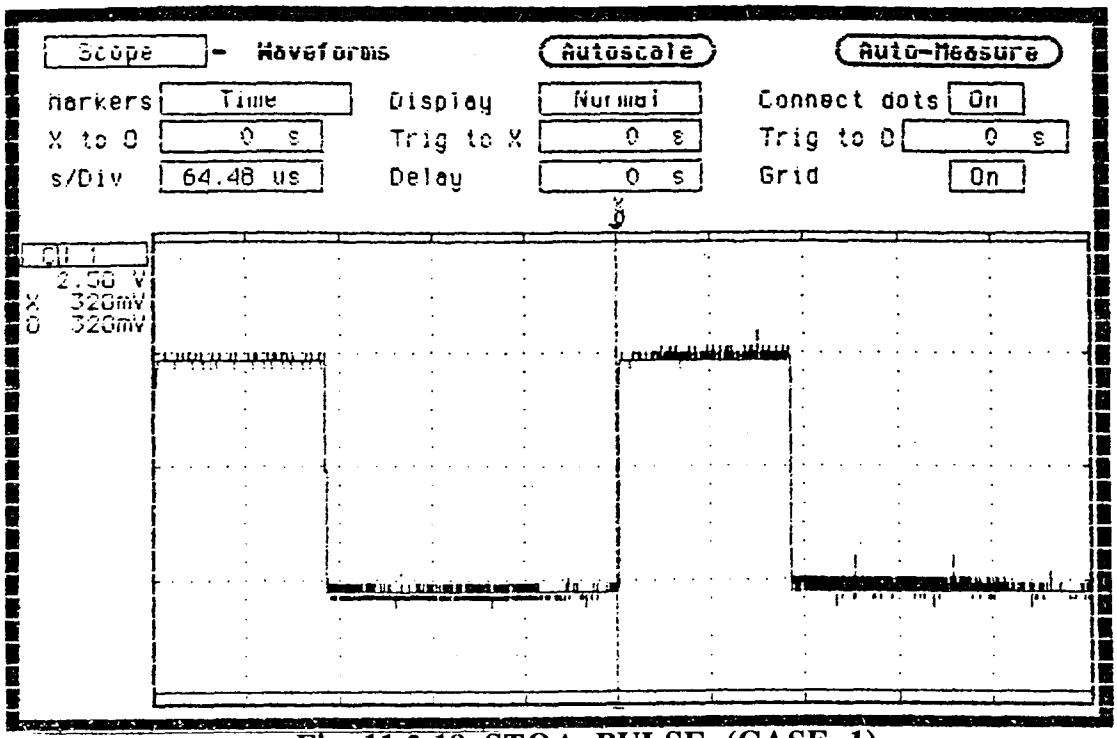


Fig 11.2.18 STOA PULSE (CASE 1)

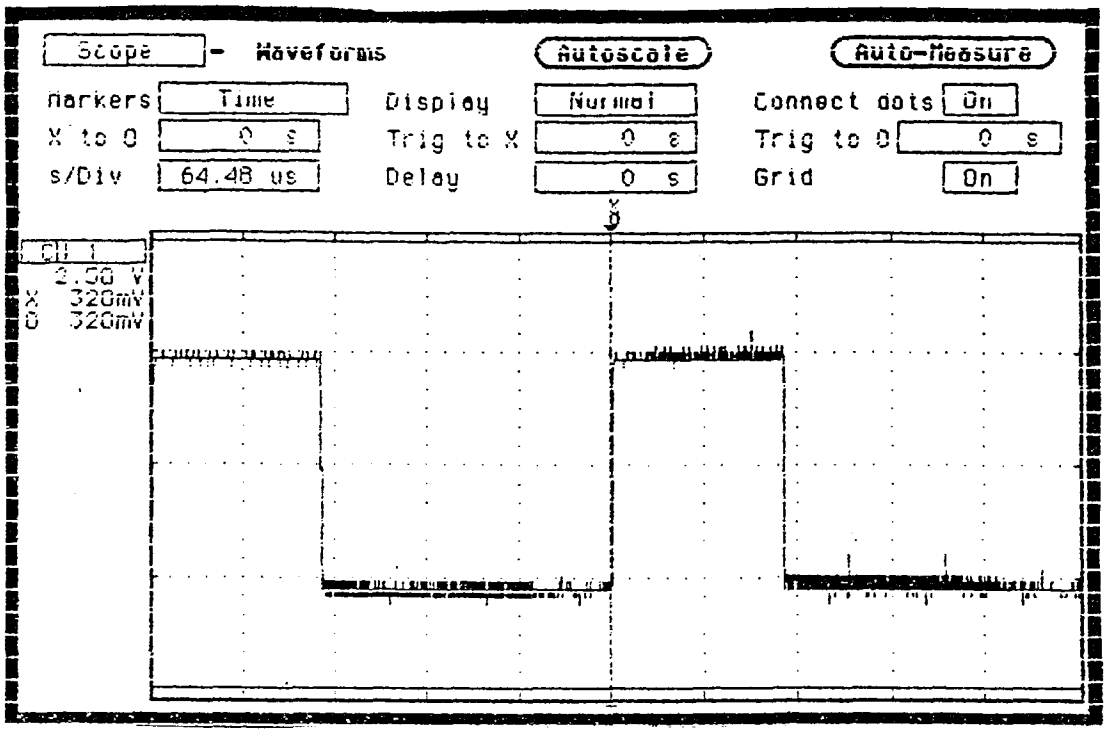


Fig 11.2.19 STOA PULSE (CASE 2)

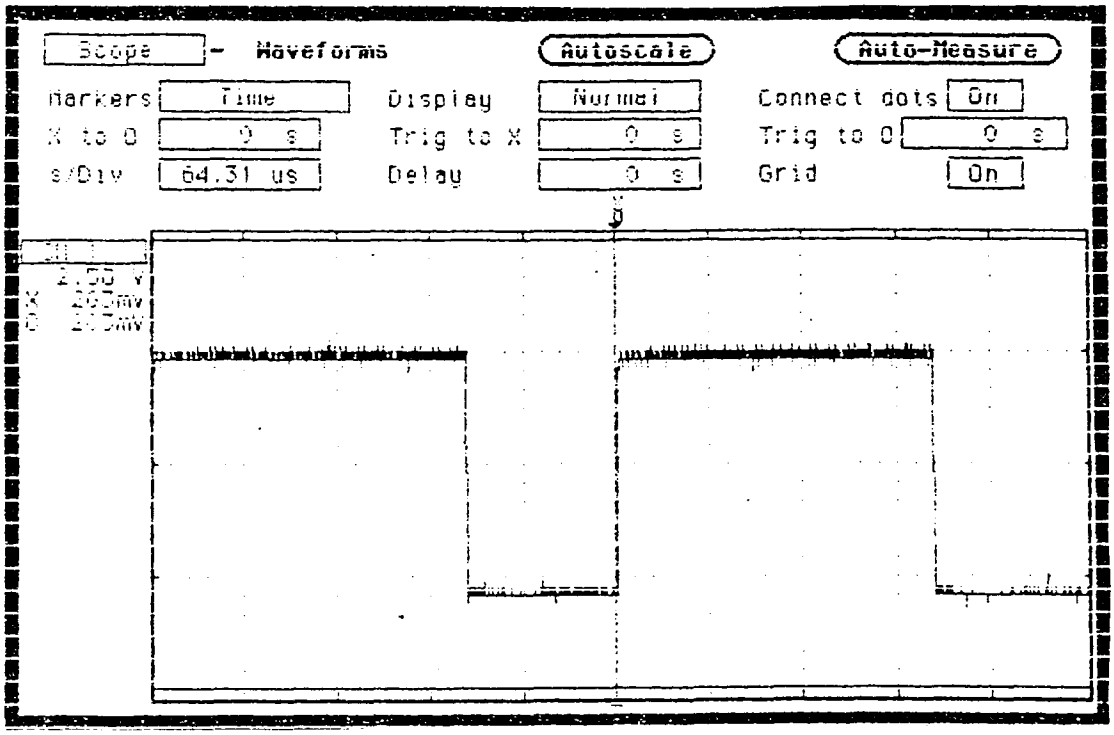


Fig 11.2.20 STOA PULSE (CASE 3)

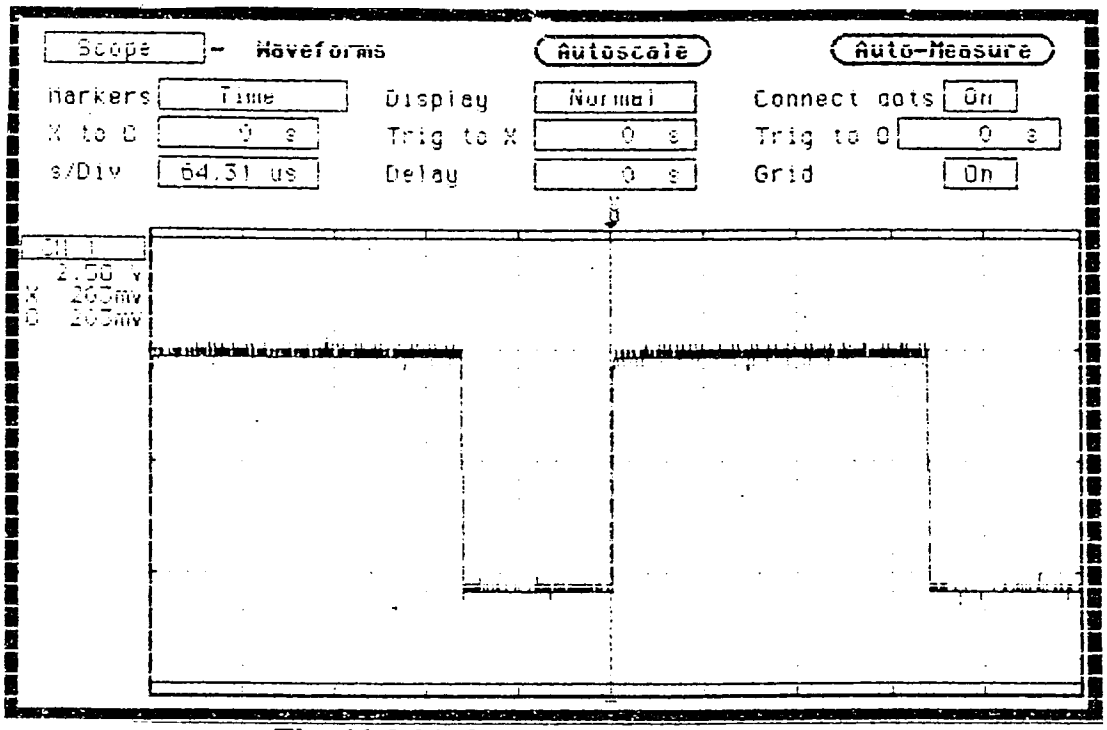


Fig 11.2.21 STOA PULSE (CASE 4)

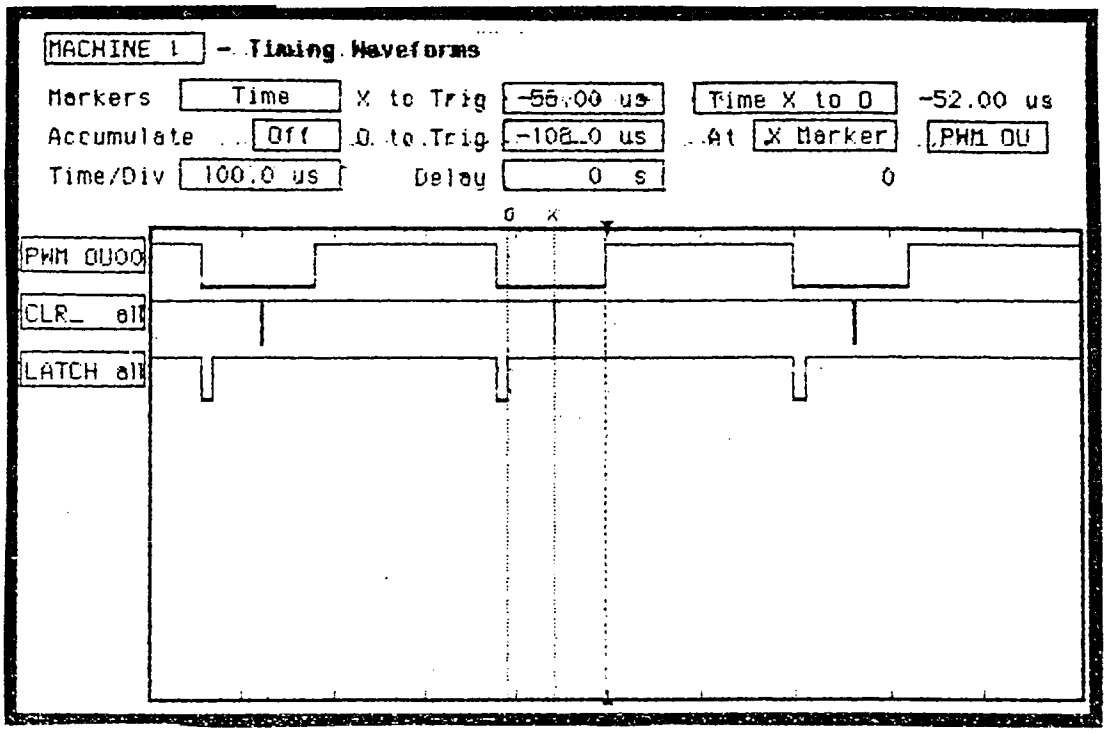


Fig 11.2.22 LATCH OUT AND CLR PULSES

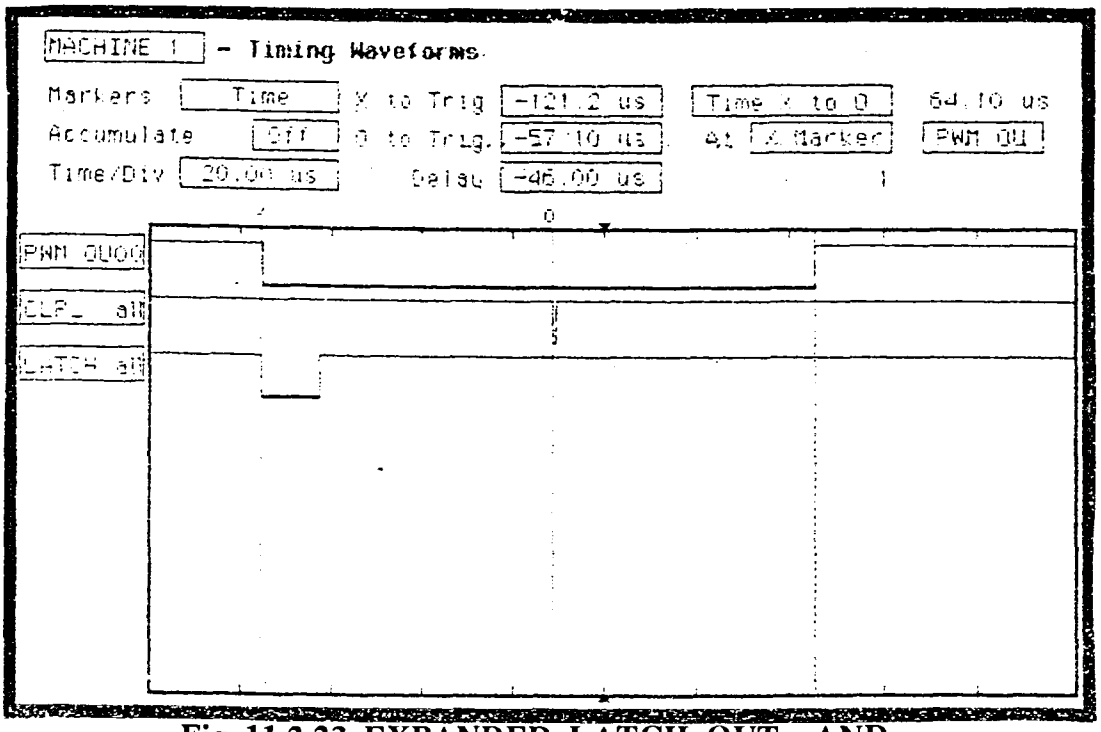


Fig 11.2.23 EXPANDED LATCH OUT AND CLR PULSES

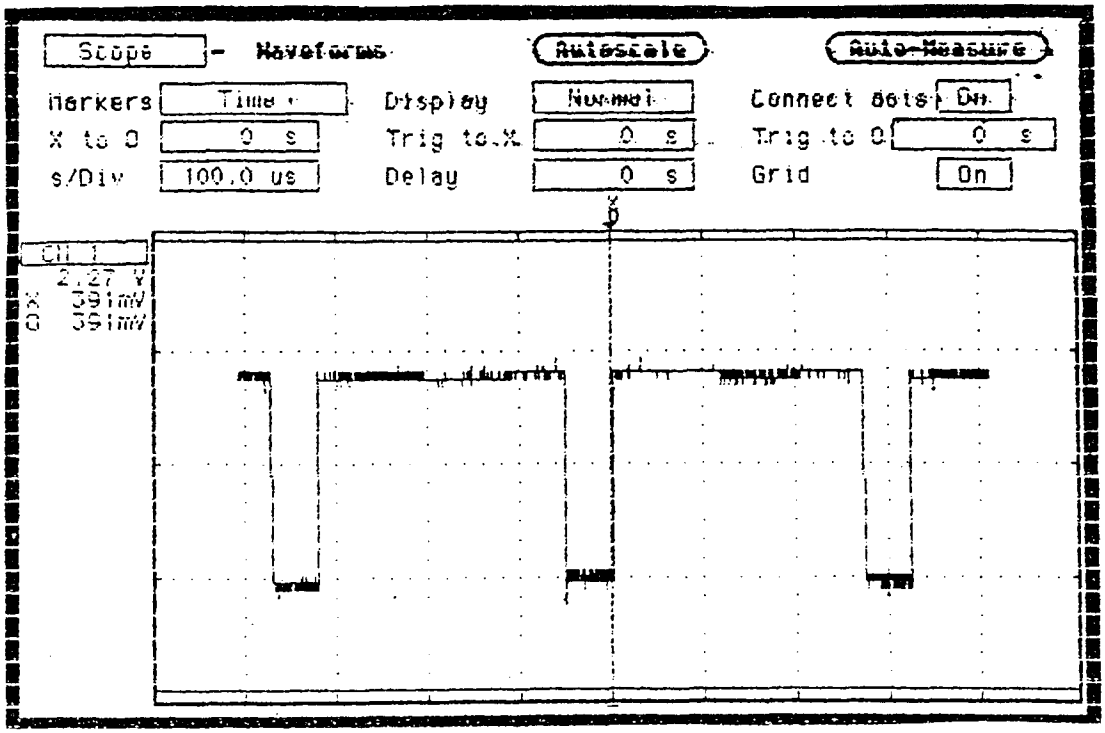


Fig 11.2.24 LATCH OUT PULSE

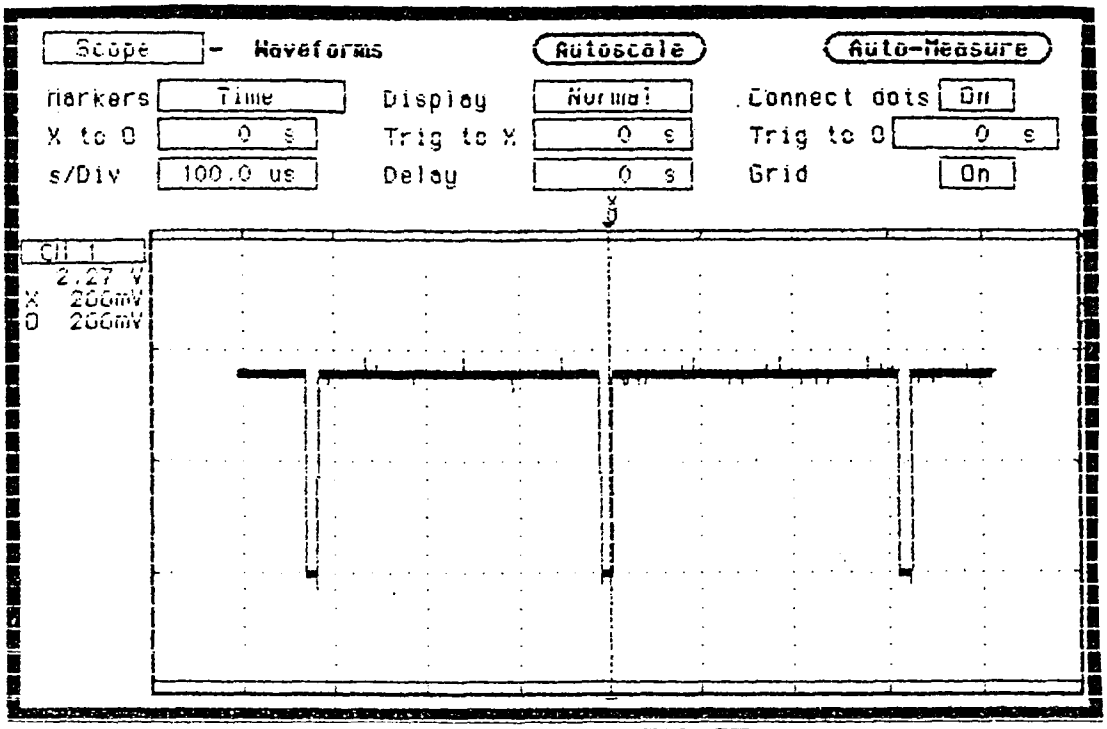


Fig 11.2.25 DFF OUT PULSE

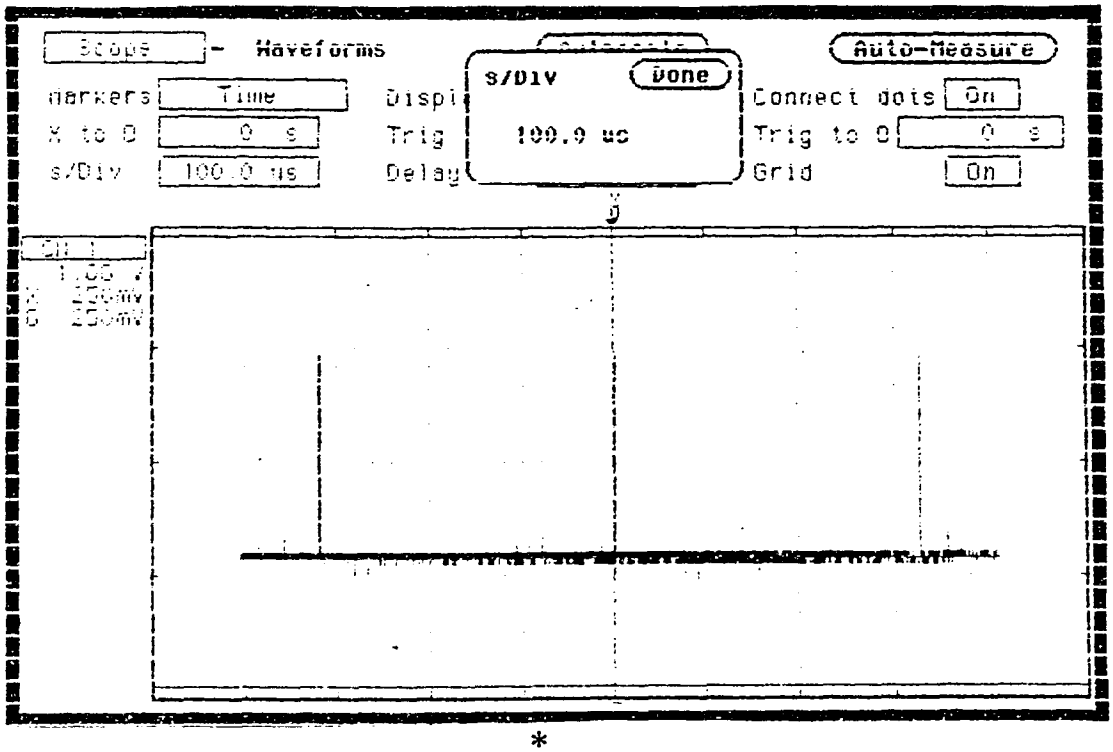


Fig 11.2.26 CLR OUT PULSE

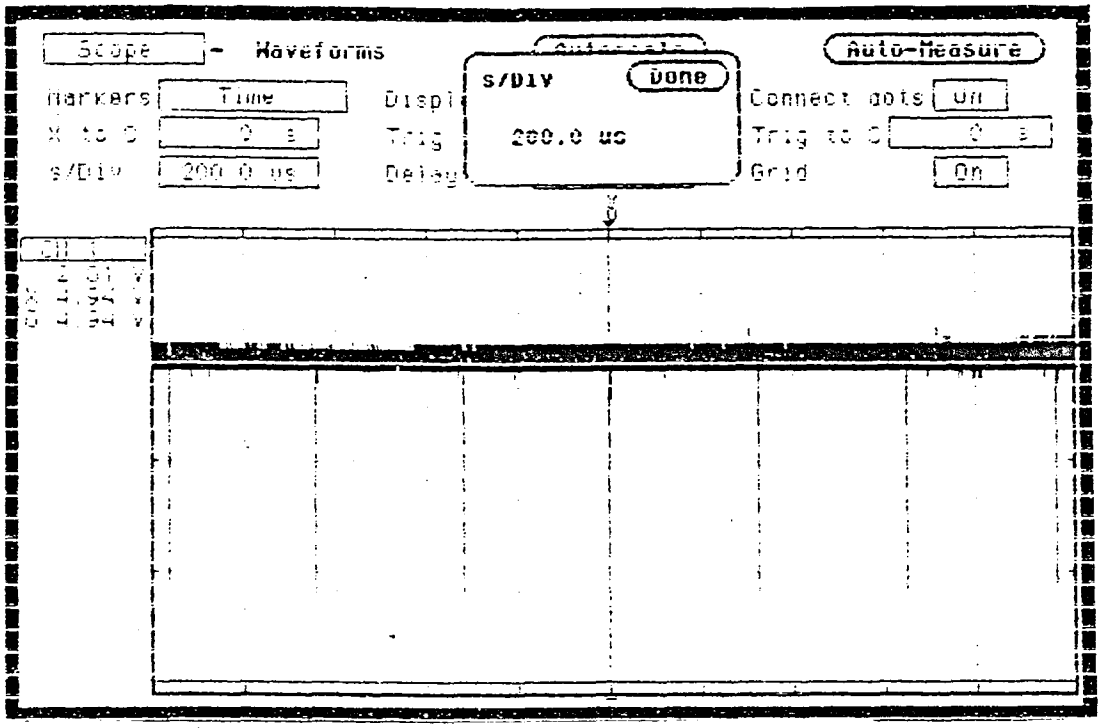


Fig 11.2.27 CLR OUT (BEFORE DIGITAL SAMPLER)

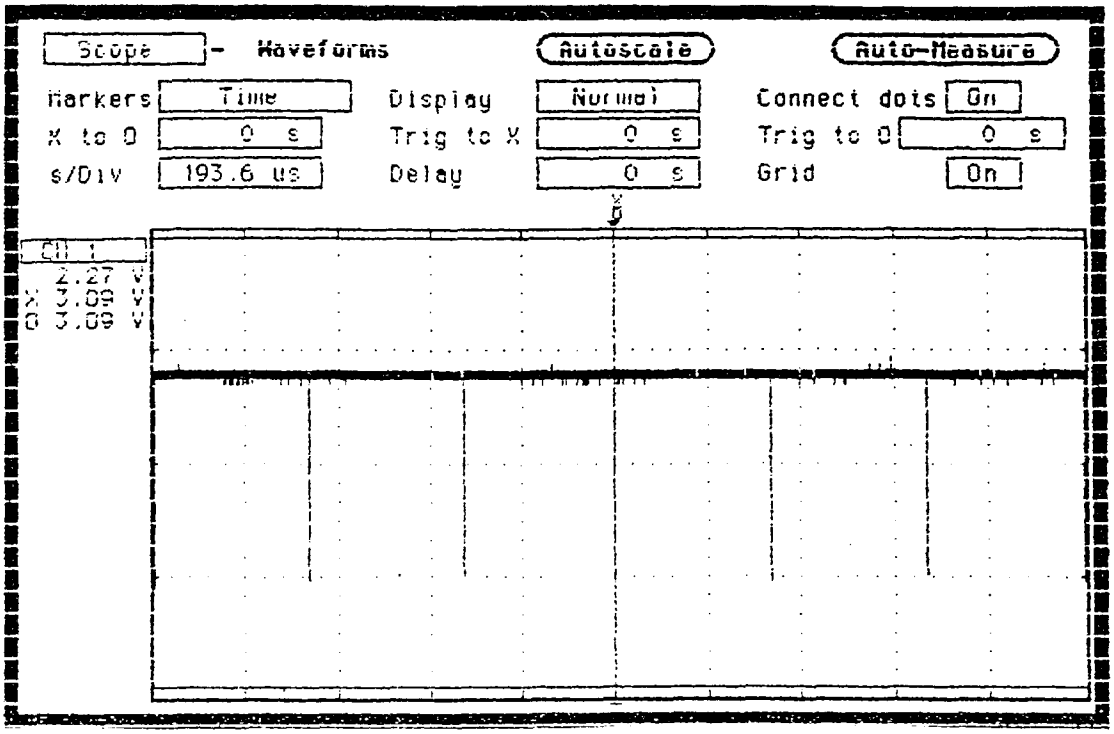


Fig 11.2.28 CLR OUT PULSE

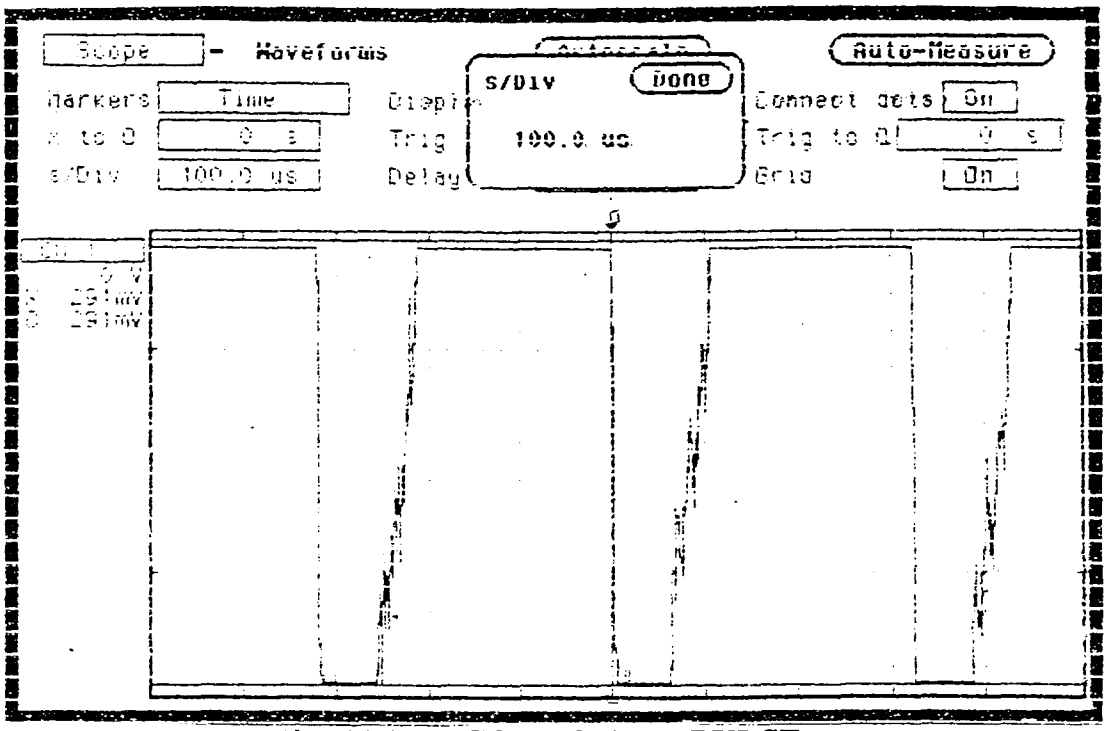


Fig 11.2.29 COMPOSITE PULSE

CHAPTER 12

DISCUSSION OF EXPERIMENTAL RESULTS

12.1 Discussion of results

The measurement of the waveforms in the Image Grabber (I.G.) subsystem under five object location test conditions showed that the I.G. Circuitry operated as designed. The PV clock pulse rate used for the measurement was 2.5Mhz. This clock rate would allow the measurement of object motion at frequencies of about 1Khz. It was expected that the designed circuitry would function at the higher clock frequencies offered by the camera subsystem (5, 10 and 30Mhz); however, when the tests were made with a clock frequency of 5Mhz, the power supply voltages decreased by more than 3 volts on the $\pm$15v and 1v on $\pm$5v, indicating that the current drawn by the circuitry exceeded the current ratings of the power supplies : 1A for the $\pm$5v supply; 700mA for the $\pm$15v supply.

Some noise was observed on the waveforms obtained using the 2.5Mhz clock; however the circuit design features, particularly the digital sampling of the sampled analog video (in the sampling circuit) and the digital sampling along with synchronization with the PV clock of the digital pulses (in the intermediate circuit) reduce the effects due to noise. This enabled the I.G. Subsystem to function without error. However, it is anticipated that if higher clock frequencies are used the cross-coupling of signals will increase during the switching time, e.g. perhaps by 4 times for 5MHz. The noise increase would probably cause the I.G. Circuitry to malfunction. The cross-coupling problem was due to the low cost standard computer add-on board which held the I.G. integrated circuitry. This board has a pin to pin spacing of only one mm. This causes the wires connecting the IC chips to be too closely spaced and resulted in cross-coupling of signals. This problem can be avoided in the future by using a customized, relatively large, printed circuit board that would have greater pin to pin spacing and IC chip separation.

Another factor that can limit the circuitry from operating at higher clock frequencies is the slew rate of the op-amp. The 741A presently used has a slew rate of 0.8V/μs versus 4V / (1 / 2.5 x 10^6) -> 10V/μs. Thus the present circuitry has a resolution of about 10 pixels obtained from the ratio of 10V/μs to ~1V/μs. To operate at clock frequencies of 5,10 and 30Mhz would require slew rates of 20V/μs, 40V/μs, and 120V/μs respectively. A rate of 60V/μs can be obtained with the LF400A.

12.2 Conclusions

The thesis work showed that it is possible to design a CCD optical sensor array that can measure frequencies up to 1KHz of object edges moving a distance less than 14336μm, obtained from the product of the number of pixels in the array and the pixel to pixel spacing. The performance of the designed system could be improved. This will require the following changes.

1) First the power supplies with current ratings of 1A and 0.7A for the 5V and 15volt supplies should be replaced with supplies having current ratings of 5 and 3A respectively.

2) The 741 op-amp with a slew rate of 0.8V/μs would have to be replaced by an op-amp such as the LF-400A, which has a slew rate of about 100V/μs.

3) Another necessary improvement is replacing the PC add-on board with a custom built printed circuit board which would increase the chip to chip spacing, reducing signal cross-coupling.

It was shown that the detectable motion frequency is the clock rate divided by the number of pixels in the array divided by the Nyquist factor of 2. Thus the above mentioned improvements would enable a motion frequency of 15Khz to be detected using a clock rate of 30Mhz and an array of 1024 pixels. Edge motion as small as the separation between pixels is detectable; thus using a 1024 array a displacement as small as of 14μm could be measured.

The system was designed to handle objects that are partially transparent and even objects with completely transparent holes at various locations. This was done by generating a variable width pulse in the variable trigger circuit. This pulse delays the start of sampling in the sampling circuit to a later time and thus would prevents spurious pulses from terminating the counting of the clock pulses. It is to be noted that the displacement of the edge of the object is equal to the sum of the displacements of the individual sections of the specimen and thus the maximum analog output changes, and more accurate object frequency measurements, are obtained by following the edge.

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