ABSTRACT

Design of a 320X122 MWIR-CCD PtSi:Si Imaging Radiometer with Automatic Optical Integration Time Control

by

Nathaniel Joseph McCaffrey

An infrared CCD camera system was designed and developed to operate a 320X244 Schottky-barrier IR-CCD Focal Plane Array (FPA) as an imaging radiometer. The goal of this research was to develop a reliable radiometer capable of resolving temperatures between 50 and 1000°C to within 1°C accuracy using non-contact spectral thermographic methods. To accomodate this wide dynamic range, the imager was operated in a non-interlaced format with variable optical integration times ranging from 120μsec to 122msec. Variable integration control was achieved by employing a "dump and read" timing procedure. To facilitate this operation, novel circuitry was developed for dynamically controlling the CCD waveforms to operate at the required integration time. Circuits were developed to embed critical information in the video signal to facilitate radiometric post-processing. An optoelectronically buffered digital interface was developed to connect the camera system to a Datacube processor. Additional circuitry enabled all frame rates to be displayed on an RS-170 monitor after processing. This system was designed to monitor the temperature of semiconductor wafers in Rapid Thermal Processing (RTP) reactors acting as the feedback control to the flash lamp heat sources.

DESIGN OF A 320X122 MWIR-CCD PtSi-Si IMAGING RADIOMETER WITH AUTOMATIC OPTICAL INTEGRATION TIME CONTROL

by

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A Thesis
Submitted to the Faculty of
New Jersey Institute of Technology
in Partial Fulfillment of the Requirements for the Degree of
Master of Science in Electrical Engineering

Department of Electrical and Computer Engineering

May 1993

APPROVAL PAGE

Design of a 320X122 MWIR-CCD PtSi-Si Imaging Radiometer with Automatic Optical Integration Time Control

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This thesis is dedicated
to Kimberly for all
the love and patience...
(and for cutting and pasting)

ACKNOWLEDGMENT

The author wishes to express his sincere gratitude to individuals who have provided technical support and have contributed to aspects of this thesis. Special thanks to my supervisor, Professor Walter F. Kosonocky for technical direction and project management throughout this project. With many friendly discussions and invaluable suggestions, I have learned a great deal from Dr. Kosonocky's years of experience. Special thanks are due to Professors Constantine Manikopoulous and Edwin Hou for serving as members of my committee and for many of their suggestions that have been incorporated into these designs.

The author is also grateful to the Optoelectronic Systems Group at the David Sarnoff Research Center for their many technical contributions. Special acknowledgment is due to Benjamin Esposito who has provided invaluable support in both the design and testing of this camera. Our discussions helped me to fully understand many of the complexities I had encountered. Dr. John Tower is also recognized for his management and guidance during this research.

The author appreciates the friendship and guidance from the members of the Electronic Imaging Center at NJIT including: Vipul Patel, Jitesh Shah, Michael Kaplinsky, and Jun Li.

The author wishes to acknowledge the financial support offered during my graduate career by the New Jersey Institute of Technology Foundation Chair for Optoelectronics and Solid State Circuits held by Professor Walter F. Kosonocky and also expresses his gratitude to Dr. Gary Hughes, Head of the Optoelectronics Systems Group at the David Sarnoff Research Center, for providing the facilities for this research.

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CHAPTER 1

INTRODUCTION

The research described in this thesis was performed at the David Sarnoff Research Center (DSRC) in Princeton, New Jersey under the direction of Dr. Walter F. Kosonocky, NJIT Foundation Chair for Optoelectronics and Solid State Circuits and supported by DARPA contract number F33615-92-C-5817 "Multi-Wavelength Imaging Pyrometry (MWIP) for Semiconductor Process Monitoring and Control". The goal of this research was to develop a reliable staring focal plane array (FPA) radiometer for non-contact spectral thermographic applications in semiconductor processing. The radiometer was required to effectively measure the temperature of a semiconductor wafer to within 1°C over the temperature range 50 to 1000°C. A 320X244 element platinum silicide (PtSi) Shottky-barrier detector FPA, developed at DSRC was chosen for this study and one-half of the vertical elements will be used in a non-interlaced format for data collection [1-2]. By employing variable integration time control ranging from 120μsec to 122ms, the effective dynamic range is improved a thousand times over the standard (single integration time) camera system.

Chapter 2 serves as an introduction to the field of infrared engineering and radiometry. Chapter 3 describes the construction and operation of the PtSi:Si imager sensors, and the dump and read procedure for sub-frame integration. Chapter 4 begins with a description of the basic camera electronics and concludes with a description of the custom timing board required for multi-integration time operation. Chapter 5 describes

the operation of the video processor and the functions of the multifunction board developed for this application. The interface between the camera and the Datacube computer was custom designed and its operation is explained in Chapter 6. Optical considerations for an application for this camera system are discussed in the Appendix.

The basic units of the Système International or SI consisting of the meter (m), kilogram (kg), and second (s) are used throughout the text with exception to the use of the micron (μm) which will be used to represent $1X10^{-6}m$.

CHAPTER 2

2 INFRARED IMAGING

2.1 The Electromagnetic Spectrum

The infrared portion of the electromagnetic spectrum spans from the millimeter wave region to the red edge of the visible spectrum. This band corresponds to wavelengths ranging from approximately 0.75 to 1000 microns. The infrared spectrum is classically divided into three regions; near infrared (NIR 0.7 to 3μm), middle infrared (MWIR 3 to 6μm), and far infrared (LWIR 6 to1000μm). The distinctions for these three bands arise when infrared radiation is transmitted through the atmosphere. Shown in Fig. 1 is the transmittance of radiation over the infrared band with references to the molecules responsible for absorption at that wavelength. Distinct windows of high transmittivity are clearly shown.

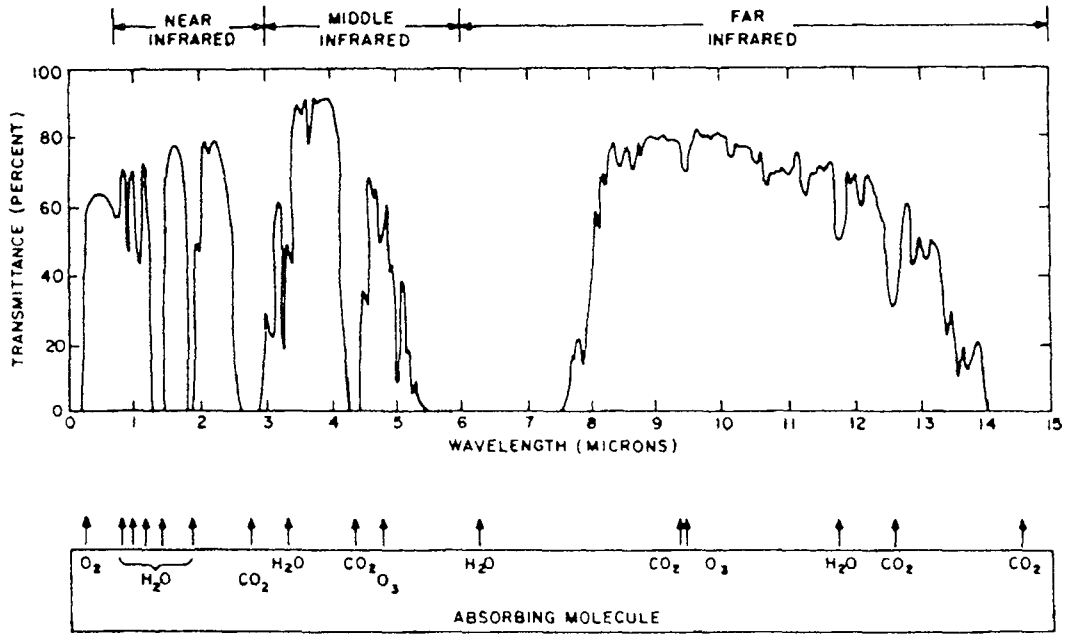


Figure 1 Transmission of the infrared spectrum through the atmosphere.

The sensors used in the radiometer design are platinum silicide Schotkky barrier detectors (SBD). These detectors are sensitive to radiation in the MWIR band.

The mechanisms for production of MWIR radiation consist entirely of molecular vibrations in solids and liquids and vibration rotation transitions in gases. In the equilibrium state, these vibrations are caused by thermal agitation and therefore, MWIR imaging measures the emission and reflection of radiation from objects with non-zero temperatures. The emitted photon with an energy of $h\nu=\Delta E_{therm}$ due to the electron-phonon interaction and subsequent electron relaxation implies that the radiant emission depends on the temperature of the object and its emissivity. For conduction and convection, the transfer of energy between two locations depends on the temperature difference to the first power. However the radiative transfer of power depends on the differences of the individual temperatures each raised to the fifth power. Imaging is then an effective measure of this radiative energy transfer and the study of radiometry concerns itself with the geometrical and spectral aspects of thermal energy transmission. This chapter will describe the basic formulae required to perform radiometric measurements. Later chapters will draw upon the formulae developed to solve problems specific to the present application.

2.2 Radiant Sources

The interaction of radiant energy with matter consists of reflection, transmission, and absorption. When radiation is incident on a homogeneous object, part of the radiation will be reflected at the surface while the rest will penetrate into the bulk of the body. If the body has high

internal absorption, the radiation will be used to increase the internal energy of the object. To be a good absorber of incident energy, the object must have a low surface reflectivity and a high internal absorption to prevent radiation from passing through the sample.

A blackbody is an object with zero surface reflection and complete internal absorption. A blackbody radiates in a continuous fashion over a broad band of frequencies. Commercial blackbody simulators approximate ideal radiators and are used as the primary calibration standard for infrared detector testing.

According to Planck's equation, blackbody radiation is characterized by a relationship between the magnitude of the emitted intensity at each wavelength versus temperature is given by

$$L(\lambda,T)=\frac{2hc^2}{\lambda^5}\frac{1}{e^{hc/\lambda kT}-1} \qquad [\mathrm{W\ m^{-3}\ sr^{-1}}] \qquad (1)$$

where h is Planck's constant, 6.6262×10^{-34} Js

λ is the wavelength in meters

c is the velocity of light, 2.997×10^{8} m/s

k is Boltzmann's constant, 1.3806×10^{-23} J/K,

T is the absolute temperature in kelvins.

A plot of this relationship is shown in Fig. 2. The spectral radiance for temperatures of 300, 500, 850, and 1000°C is shown. The units for radiance plotted in the y-axis are in $\mathrm{W \cdot cm^{-2} \cdot sr^{-1} \cdot \mu m^{-1}}$. Also plotted is the locus of the points of maximum radiation.

This relationship is known as the Wein displacement law. It shows the maximum radiation shifts toward shorter wavelengths as the temperature of the radiator is increased.

$$\lambda_m = 2898/T \qquad [\mu m] \qquad (2)$$

Fig. 2 shows that the peak radiation for temperatures ranging from 300-1000°C lie within the operating range of the PtSi detector response.

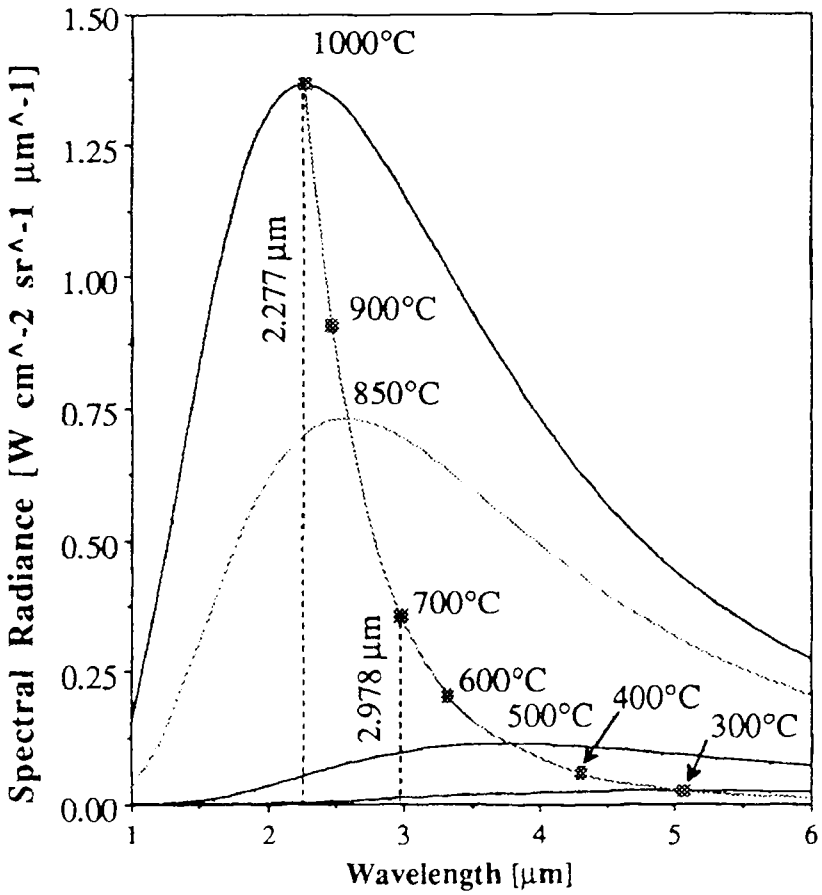


Figure 2 The Planck distribution and Wein displacement for MWIR signals for temperatures ranging from 300 to 1000°C.

The total power radiated per unit area of a blackbody is obtained by integrating Planck's radiation relation for all wavelengths at a given temperature, and the result is known as the Stefan-Boltzmann law:

$$M = \varepsilon\sigma T^4$$

where

$$\sigma = \frac{\pi^2 k_B^4}{60\hbar^3 c^2} \tag{3}$$

$$\sigma = 5.66961X10^{-8}\, W \cdot m^{-2} \cdot K^{-4}$$

In equation (3), ε is termed the total hemispherical emissivity. A perfect blackbody has an emissivity of one. A silicon wafer of six inch diameter occupies an area of:

$$A = \pi \cdot (0.0762)^2$$

$$A = 0.0182m^2$$

Table 1 lists the total power a blackbody with an area equivalent to the six inch wafer would emit for each given temperature.

Table 1 Total emitted power of a wafer sized blackbody for certain temperatures

Temperature [°C]	Total Power [W]
25 (Room Temperature)	8.137
300	111.235
500	368.420
850	1641.132
1000	2709.806

It is important to note that if the surroundings are at the same temperature, the object would absorb the same amount as it emits.

In many cases it is the temperature that must be determined given the radiance. Equation (1) can be rewritten as follows:

$$T = \frac{1.43883X10^4}{\lambda \cdot \ln\left[\left({}^{1.191066X10^4}\!/_{L(\lambda)\lambda^5}\right)+1\right]} \quad [K] \qquad (4)$$

2.3 Transfer of Radiant Flux

To correctly determine the radiometric characteristics of the camera system, a knowledge of the effective flux transferred from the source through the intervening media to the photovoltaic detector is required. Modeling the source of optical flux in terms of geometrical radiant quantities will help to predict the radiant energy transfer.

Fig. 3 shows an illustration of the differential solid angle $\Delta\omega$, and the differential projected solid angle $\Delta\Omega$. The steradian (sr) is a measure of the solid angle and is defined as the ratio of the area A on the surface of a sphere to the square of the radius. The differential solid angle is given by:

$$\Delta\omega = \frac{dA}{r^2} = \sin\theta d\theta d\phi \quad [sr] \qquad (5)$$

The projected solid angle can be visualized as the projection of the solid angle area A onto the base of the hemisphere. The solid angle ω and

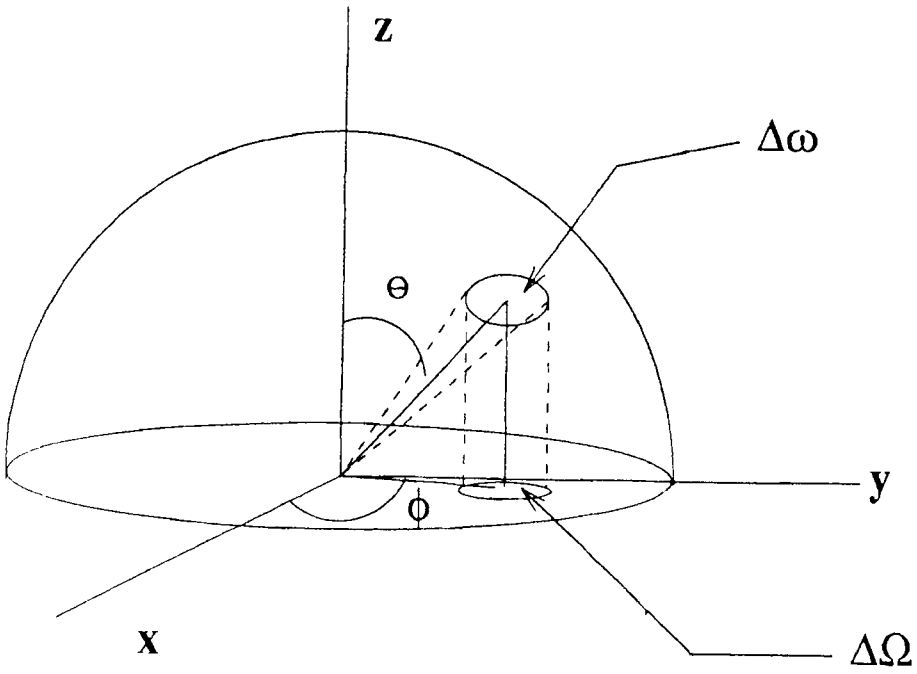


Figure 3 Illustration of the solid angle and projected solid angle.

the associated projected solid angle Ω, for a right circular cone oriented with the center on the Z-axis are given respectively by:

$$\omega = \int_0^{2\pi} d\phi = \int_0^{\Theta} \sin\theta d\theta = 2\pi(1-\cos\Theta)$$
$$\Omega = \int_0^{2\pi} d\phi = \int_0^{\Theta} \sin\theta\cos\theta d\theta = \pi\sin^2\Theta \qquad (6,7)$$

where Θ is the half angle measured from the Z-axis to the cone edge.

A beam of radiant energy is defined in terms of two areas shown in Fig. 4. The areas are separated by a distance d. All the flux in the beam flows from A_1 to A_2. The throughput is defined as

$$\gamma = n^2 A\Omega \qquad (8)$$

where n is the index of refraction for the intervening medium.

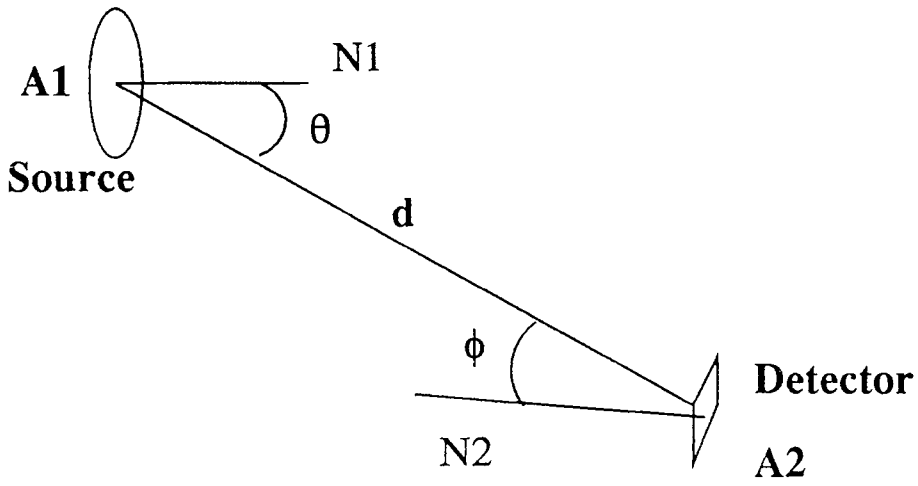


Figure 4 The geometrical illustration of beam throughput.

Following Lambert's cosine law [6], the throughput for n=1 is given generally by

$$\gamma_1 = A_1 \cos\theta\omega_1 = A_1 \cos\theta \frac{A_2 \cos\phi}{d^2} \qquad [\text{cm}^2\ \text{sr}] \qquad (9)$$

This result is valid only in the limit where d is large with respect to the largest dimension of A_1. The exact relationship is given by

$$\gamma_1 = \int_{A1\omega1} \int dA_1 \cos\theta d\omega_1 \qquad [\text{cm}^2\ \text{sr}] \qquad (10)$$

Equations (9) and (10) agree to within 1% when d is 20 times greater than the largest dimension of A_1. For distances smaller than this, the integral of equation (10) needs to be solved because ω_1 is no longer independent of A_1.

Flux (Φ) is the general term used to describe a quantity that is propagated according to geometrical laws. Radiance is the most general

way of describing flux because it characterizes the beam both in position and direction.

Radiance can best be analogized to brightness in the visual spectrum. Radiance is defined as

$$L = \frac{d^2\Phi}{\cos\theta \cdot dA \cdot d\omega} \qquad [\text{W cm}^{-2}\,\text{sr}^{-1}] \qquad (11)$$

where θ represents the angle that the right circular flux cone makes with the source normal.

Emissivity is a measure of the relative response of a radiator with respect to a blackbody. Emissivity is a function of direction, wavelength, and temperature. A greybody is defined as $\varepsilon(\lambda,T,\theta)$ = constant <1, while a colorbody is defined as $\varepsilon(\lambda,T,\theta)=f(\lambda,T,\theta)$. Emissivity can be derived from the Kirchoff relations by considering an object in an isothermal cavity. If there is a temperature difference between the object and the cavity, there will be heat transfer. If the object absorbs a portion α of the input exitance M that a blackbody would absorb, the emitted energy will equal the absorbed flux. Including all optical processes, the relationship

$$\alpha + \rho + \tau = 1 \qquad (12)$$

is an expression of the conservation of energy where ρ is the reflectivity and τ is the transmitivity of the material. For an opaque body where τ=0, it is apparent that good reflectors have low emissivities. The emissivity term is used to scale radiometric equations that use blackbody models.

Calculations of the flux transfer from an extended area source to the sensor, are based on the radiometric definitions. The solid angle is measured at the sensor aperture.

The total flux is measured by spatially integrating over the entire source area, and integrating the solid angle beam the source is radiating and also the wavelength band of the response.

$$\Phi = \tau_{path}\varepsilon(\lambda,T,\theta)L(\lambda,T)\int_{\lambda}d\lambda)\int_{\omega}\cos\theta d\omega\int_{A}dA$$

$$\Phi = \varepsilon(\lambda,\theta)L(\lambda)A\Omega\tau_{path} \qquad (13)$$

This equation is valid when the source to detector distance is 20 times greater than the length of the object, the object is isothermal, and τ_{path} represents the aggregate transmission characteristics of the path medium. These assumptions are usually valid when a single pixel in the array is defined as the sensor. The path transmission must be found experimentally or by computer model to include effects such as molecular absorption, scattering and window/lens effects. Our system can use these assumptions for the distances used to image the semiconductor wafers. The light is transmitted through several materials and these materials need to be modeled to complete the radiometric analysis. The optical system will be further discussed in the Appendix.

CHAPTER 3

3 IR Imaging Devices

3.1 Platinum Silicide Detectors

In 1973 Shepherd and Yang proposed the development of infrared detector arrays based on the internal photoemission from silicon Schottky barrier diodes [7]. PtSi sensor technology matured with focal plane arrays now containing up to $1.5X10^6$ pixel elements and noise equivalent differential temperatures (NEΔTs) below 0.1 K. Two different imagers developed at the David Sarnoff Research Center were investigated to determine the best device for the camera design.

3.1.1 Metal Semiconductor Junctions

When a metal and a semiconductor are brought into intimate contact, a separation of charges at the interface forms a high resistance region devoid of mobile carriers in the semiconductor. Figure 5 shows the energy band diagram for a metal with a work function ϕ_m and a p-type semiconductor with a work function ϕ_s before and after contact. The gradient of the Fermi level must be invariant so the bands will bend to accommodate the disparity between the affinities of the two materials. The barrier height for holes is given by

$$\phi_b = \chi_s + E_g - \phi_m$$
$$\phi_b = 4.05 + 1.16 - 5.65 = -0.44eV \qquad \text{[eV]} \qquad (16)$$

where E_g represents the band gap of the semiconductor [8]. This represents the band bending for a PtSi Schottky barrier diode. The formation of a silicide from the metal will lower this barrier height as will the effects of image charges. The barrier height is found experimentally to be in the range of 0.16-0.23 eV.

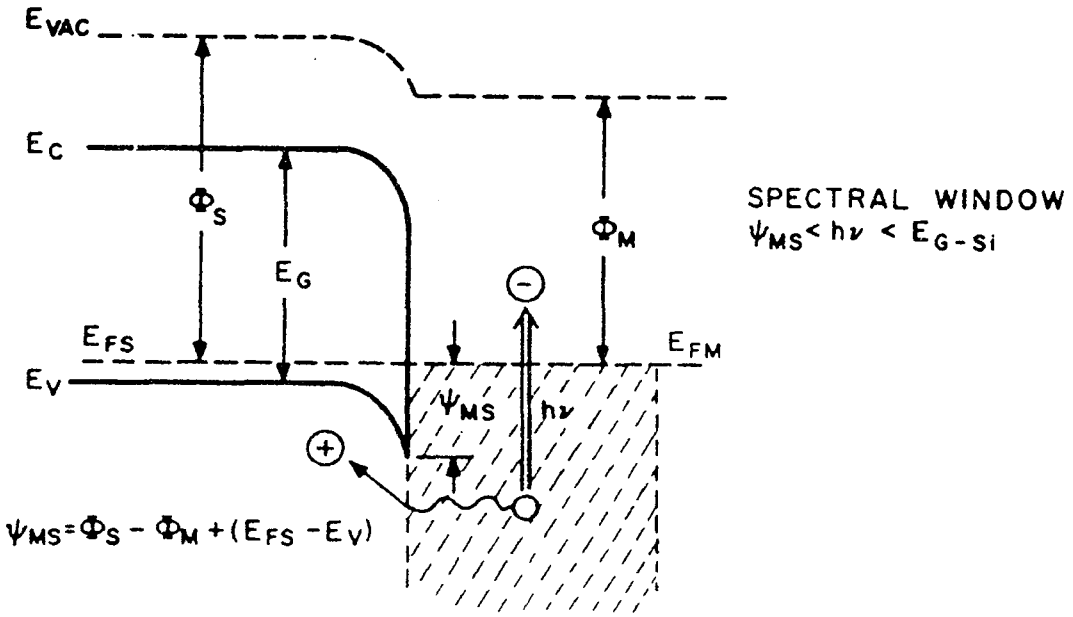


Figure 5 Energy band diagram for a PtSi Schottky Barrier Diode

The barrier height can be verified with a variety of methods. Capacitance-voltage measurements yield both the barrier height and the donor concentration as a function of distance. The photoelectric method has proven to be the most accurate way of directly measuring ϕ_b [9]. Monochromatic light in the form of filtered blackbody radiation is incident on the diode with a photon energy greater than the barrier height. The resulting photo generated current can be approximated by a Fowler equation for thermionic emission.

$$J = a \cdot (h\nu - \phi_b)^2 \tag{17}$$

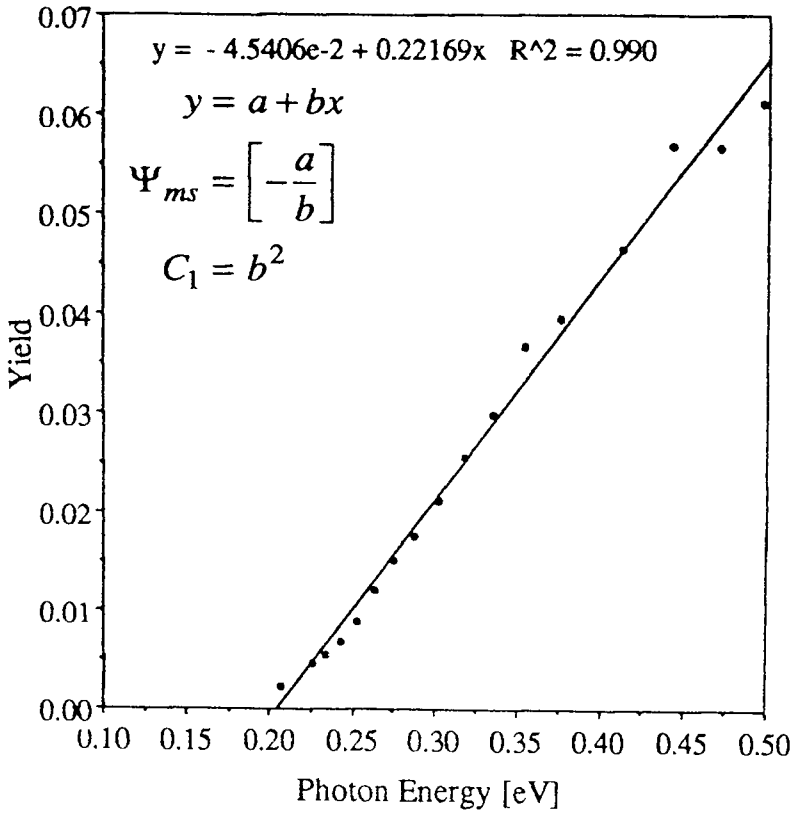


Figure 6 Photon yield vs. Energy.

Plotting the square root of the photoresponse as a function of photon energy yields a straight line that determines the barrier height. Shown in Fig. 6 is a photon yield plot from a PtSi test diode. The measured barrier height is 0.1976 eV.

Silicides are formed by depositing a layer of metal on a clean silicon surface and a subsequent thermal annealing at the junction. This causes the metal to diffuse into the silicon and react. Thermal annealing of thin platinum films on silicon leads to formation of Pt_2Si. After all the Pt is consumed, PtSi begins to form until all Pt_2Si has been converted to PtSi [10].

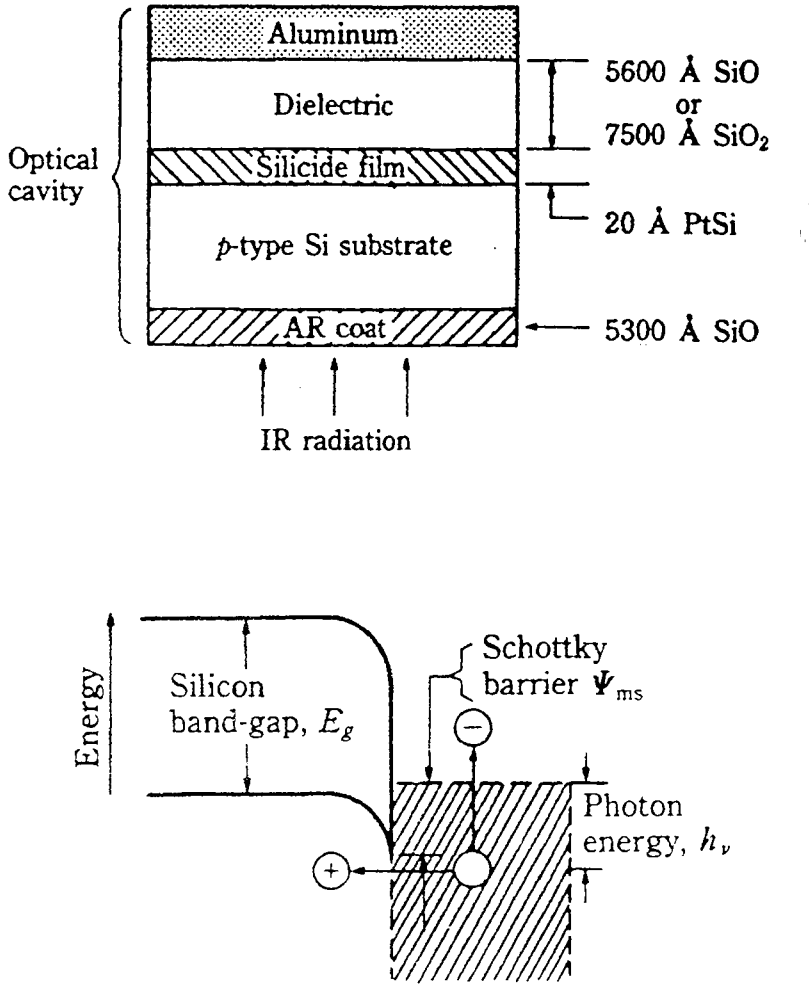


Figure 7 PtSi-Si SBD construction and operation.

The basic construction and operation of the PtSi SBD is shown in Fig. 7. The chip is illuminated from the back side and infrared radiation with photon energy less than the bandgap of silicon (1.16 eV @ 77 K) is transmitted through the silicon substrate. Thus the substrate acts as a long pass filter. Photons with energies greater than the bandgap are absorbed in

the bulk and the electrons recombine without contributing signal charge. The substrate surface is coated with an antireflection layer to increase the coupling of the IR radiation into the SBD by about 30% [3]. The photons are absorbed in the silicide layer.

Carrier momentum is conserved at the junction and carriers with sufficient kinetic energy in the normal direction to the junction can overcome the barrier potential. Holes that have surpassed the barrier ("hot" holes) are injected into the silicon substrate. The electron that is left behind contributes to a net negative charge in the silicide that is proportional to the local image irradiance. The negative charge is transferred into a CCD readout structure after a specific charge integration time as the pixel video signal. The imager responds to radiation with a spectral bandwidth of

$$\Psi_{ms} \langle h\nu \langle E_g \tag{18}$$

The layer of platinum that is deposited is around 9Å thick and this is followed by a 16-h anneal. The resulting active silicide layer has a thickness of about 20Å [1]. Absorbence is a function of thickness and in order to increase the efficiency, the imager used in this study is fabricated with an optical cavity placed on top of the thin silicide layer. This Fabry-Perot mirror is "tuned" to a wavelength of 4.1μm by separating an aluminum mirror from the silicide with a one quarter wavelength thickness layer of either SiO or SiO_2. This essentially sets up a standing wave at resonance, maximizing the optical absorbency.

Responsivity [$\Re$ A/W] is the measurement of a diode's performance to both different signal levels and different frequencies of radiation. The basic test station includes a temperature variable black body source, band

pass filters to spectrally decompose the radiation, a current meter and a computer. The responsivity data set is calculated by measuring thedetector output and dividing it by the input radiation flux at that wavelength.

$$\Re(\lambda,T,n)=\left[\in\left[\frac{I\cdot d_{s-d}{}^{2}}{A_{apt}\cdot A_{\det}\cdot\int_{0}^{\infty}L(\lambda,T)\cdot\tau_{n}(\lambda)\cdot d\lambda}\right]\right] \quad [A/W] \qquad (19)$$

where $L(\lambda,T)$ is the spectral radiance of the black body

$\tau_n(\lambda)$ is the transmission response of filter n

A_{apt} is the limiting aperture area

A_{det} is the detector area

d_{s-d} is the source to detector distance

An enhanced responsivity test station was developed to improve the results of photo yield experiments at DSRC. Improvements included the averaging of readings till a threshold statistical deviation had been reached, the measurement of background current for each bandpass filter, and improved field stops to reduce stray leakage radiation. Shown in Fig. 8 is the measured responsivity of a large area (2.5 X105 μm^2) test diode operating with a reverse bias of 4 volts. It should be noted that the test diode measured did not have a resonating optical cavity. The photoresponse of this device is lower than responses found experimentally with standard diodes.

The data set representing the responsivity readings can be approximated by a Fowler equation [3] as.

$$\Re = C_1 \cdot \left(1 - \frac{\Psi_{ms}\lambda}{hc}\right)^2 \tag{20}$$

where R is the responsivity in [A/W]

C_1 is the quantum efficiency coefficient in eV^{-1}

Ψ_{ms} is the silicide-semiconductor barrier in eV

λ is the wavelength of the radiation in μm.

The yield of the detector can also be determined from the responsivity using the equation

$$Y = \sqrt{\Re}\left(\frac{hc}{\lambda}\right) \tag{21}$$

Where the straight line obtained when Y is plotted against E_{photon} determines the barrier height.

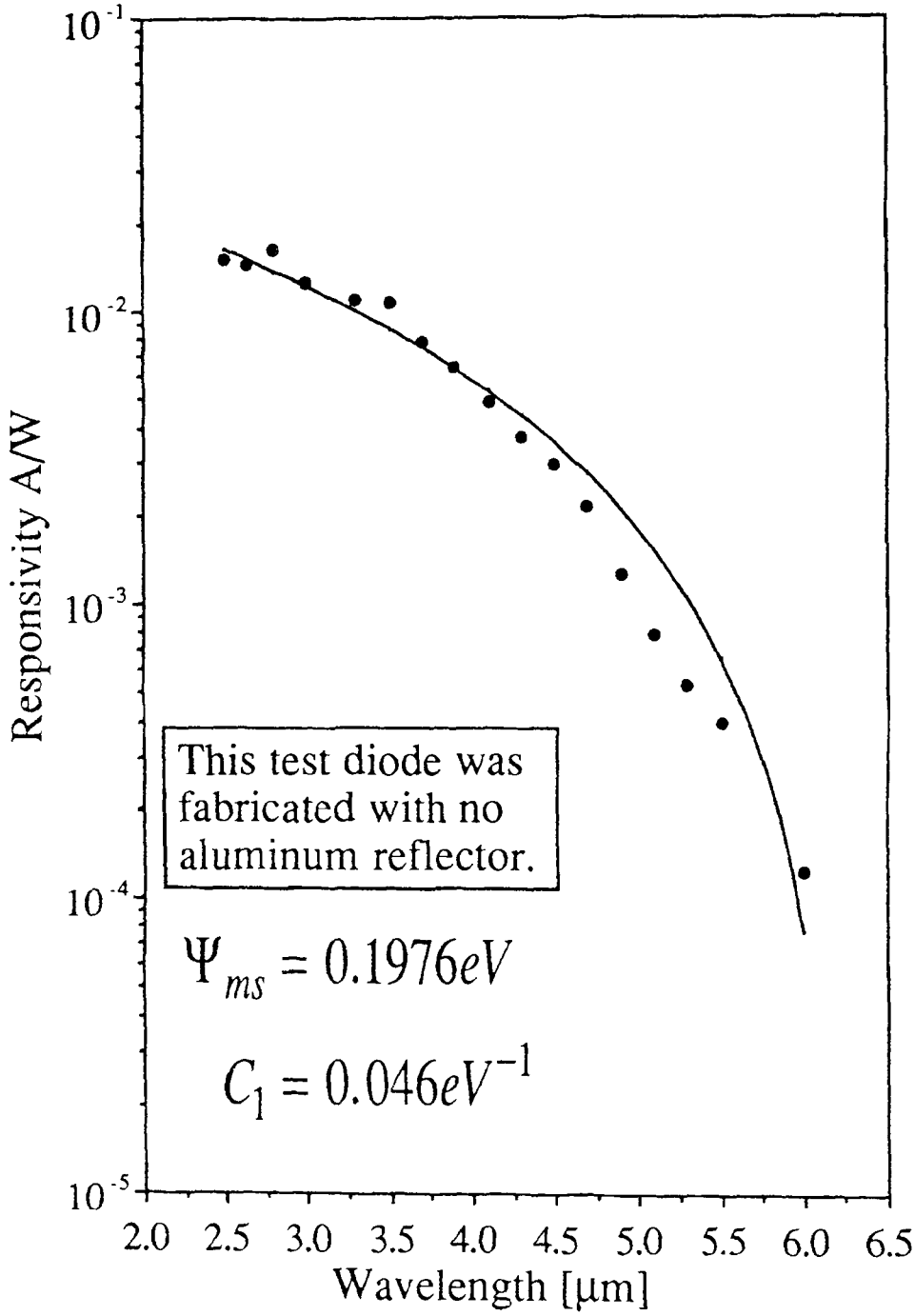


Figure 8 Responsivity plot of large area (2.5 X105 μm^2) test diode.

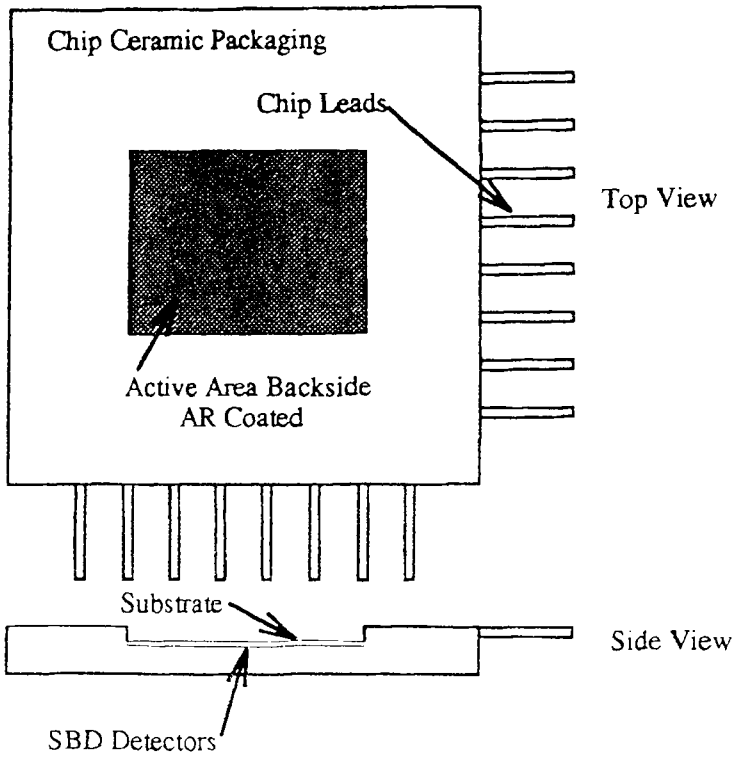
3.2 Focal Plane Array

Two imagers were analyzed to determine the best device for the camera system. The 320 X 244 IR-CCD [1-3] device can be set-up to operate in either the field or frame readout modes and utilizes charge coupled device (CCD) channels to readout charge to the output amplifier. The charge is transferred from the detectors by a universal transfer pulse. The 640 X 480 IR-MOS imager [4] was evaluated [5] to assess its usefulness in sub-frame integration. The 640 X 480 imager uses MOS transistors to readout the acquired signal from individual pixels by column and row addressing. During normal operation, the signal is read out from the detectors sequentially line by line. Therefore, the time that each line spends integrating charge is equivalent in length to every other line yet the start of integration is offset from each previous line.

The 320X244 IR-CCD array used for this thesis occupies an active area of 504 mil X 384 mil on 40 X 40 μm centers. The optically active area represents 43% of the total device area because detection occurs in SBDs and does not occur in the CCD channels. This differs from visible imagers where the entire array can be photo active. The imager is designed as an interline transfer with two vertical detectors interlaced to the same vertical CCD channel. The operation of two interlaced fields represents frame integration and is done so that the display will contain less flicker and is easier to view. Our application entails machine vision and field integration is the most efficient way of entering video data into the computer. Field integration involves operating the imager with one field (either half the pixels or combining fields together in the form of a double sized pixel) with the frame made up of that field. A schematic of

the CCD chip and the array layout is shown on Fig. 9. As stated previously, electrical signal derived from photodetection is allowed to accumulate in the PtSi detectors for a specific charge integration time. A transfer pulse activates the overlapping surface channel CCD (SCCD) by bringing one phase of the B clocks high. The CCDs in this design are fabricated for four-phase operation. This transfers charge from the detectors into the B-registers [vertical buried channel CCDs (BCCDs)].The B-registers are clocked downward at the line rate of 63.5 μs. At the same time, the horizontal C-Registers [BCCDs connected to the B-registers at the bottom of the array] are clocked at the pixel rate and read one line of 320 pixels to the on-chip output amplifier in one line time. For a full description of the design and fabrication of the imager chip and the clock signals necessary to operate the imager see Patel [11]. For an understanding into the kinetics of charge transfer in a cryogenically cooled BCCD, see Esposito [12].

The 640 X 480 IR-MOS pixel dimensions are 24X24 μm. The pixels are addressed using column and row registers. This allows for spatial sub-frame windowing at higher frame rates. This imager can be operated in the field or frame integration mode. The 640 X 480 imager can be operated in a sub-frame integration mode by clearing the detectors a certain time before interrogating them. IR-MOS imagers developed at DSRC contain an 8:1 MUX to reduce the line capacitance and the kTC noise associated with it. This also allows the resetting of video lines not addressed by the multiplexer. IR-MOS imagers can be reset by biasing the



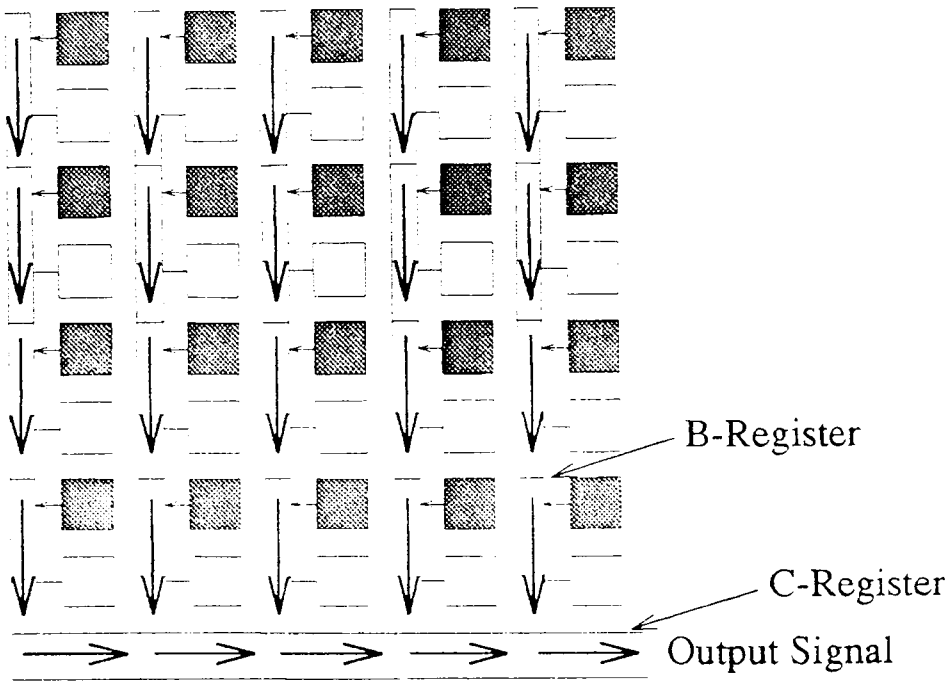


Figure 9 The 320 X 244 chip (a), and the layout of the SBD array (b)

pixel transistors on the line preceding the readout line to clear the detector. The integration time is then $T_i = n \cdot 63.55\mu s$ where n is the number of vertical clock periods between the two lines. Using this operation the integration time can be varied from 60μs to 30ms [4]. Shown in Fig. 10 is the sub-frame integration operation of an IR-MOS imager. This method however does not measure image with the identical exposure time.

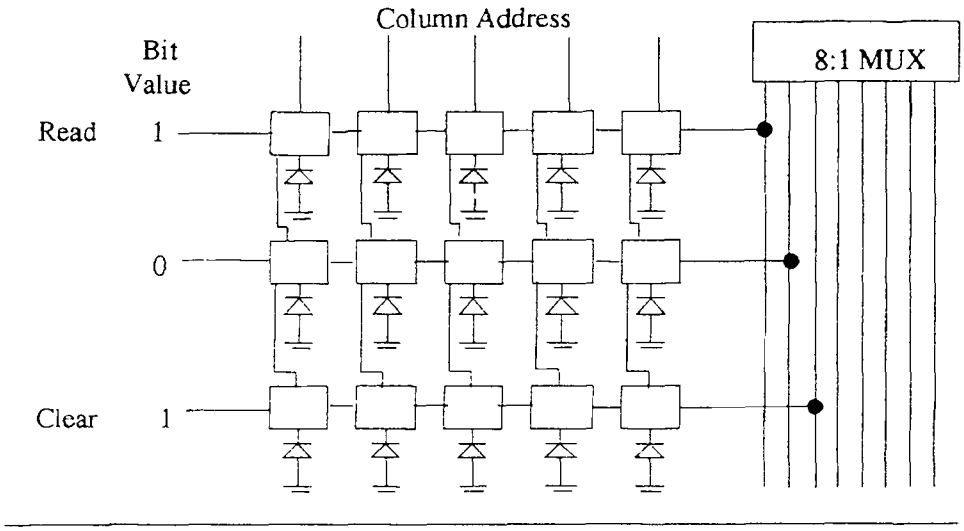


Figure 10 Sub-Frame optical interrogation with an IR-MOS imager.

3.2.1 Spectral Uniformity

When employing individual pixel elements arranged in an array to perform high spatial resolution radiometry, the uniformity in the response of the pixels is essential. Measurements were made to determine the uniformity in both spectral and spatial responses of the focal plane array

[5]. The experiments were carried out with a DSRC 640 X 480 IR-MOS imager. Figure 11 shows the test camera integrated into the primary evaluation system (additional equipment was utilized for some of the testing). The test apparatus consists of a square radiator, a filter wheel, a current picoammeter, a data acquisition unit, two video digitizers, an Apple MAC IIfx computer and *FrameGrabber* software [13]. These units are consolidated under the computer's control to work as an automated characterization system. The black body source, an Electro Optical Industries (BH2450E) large aperture radiator (with a range of 25 to 170°C), was controlled and monitored using an IEEE-488 interface. Two video digitizers were employed to convert the odd and even video fields into computer data. The test setup was controlled by a computer utilizing software developed at the David Sarnoff Research Center. *FrameGrabber* is a flexible, high speed, data acquisition software system developed specifically for the characterization of solid state imaging arrays. The video signal is captured and analyzed using a Macintosh graphical interface. *FrameGrabber* can print the captured image, generate defect lists and uniformity histograms, and calculate multiplicative correction coefficients that can be applied to any acquired frame.

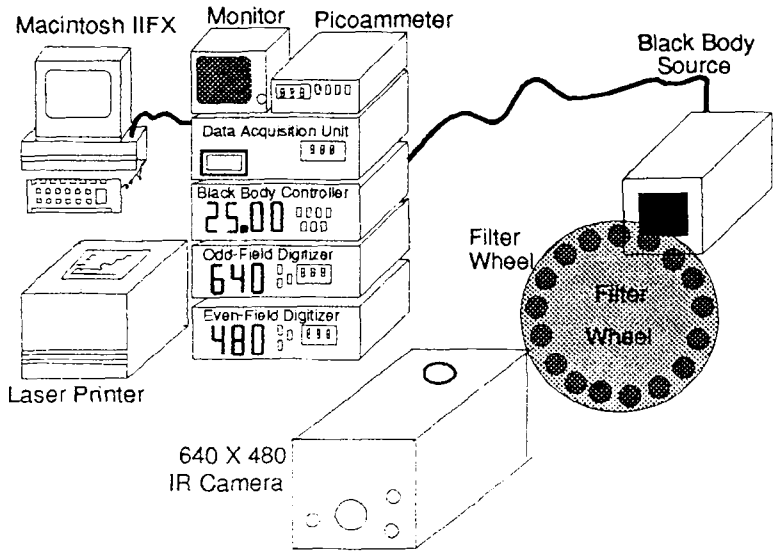


Figure 11 Uniformity test station for PtSi detector arrays.

By controlling the temperature and by placing filters between the source and detector, the responsivities of individual pixels can be found. Bandpass filters with sidebands of the order (± 0.1 μm) were placed inside the dewar and a constant temperature of 150°C was maintained. Signals were acquired with the *FrameGrabber* software and 16 frames were averaged to make a composite image with reduced temporal noise effects. This image was analyzed to yield measurements of the electrical output signal for ten representative pixels chosen to represent the entire area of the FPA. The spectral responsivity has been defined as the output diode current divided by the input optical power per unit wavelength. Shown in Fig. 11 is the spectral responsivity in A/W as a function of wavelength.

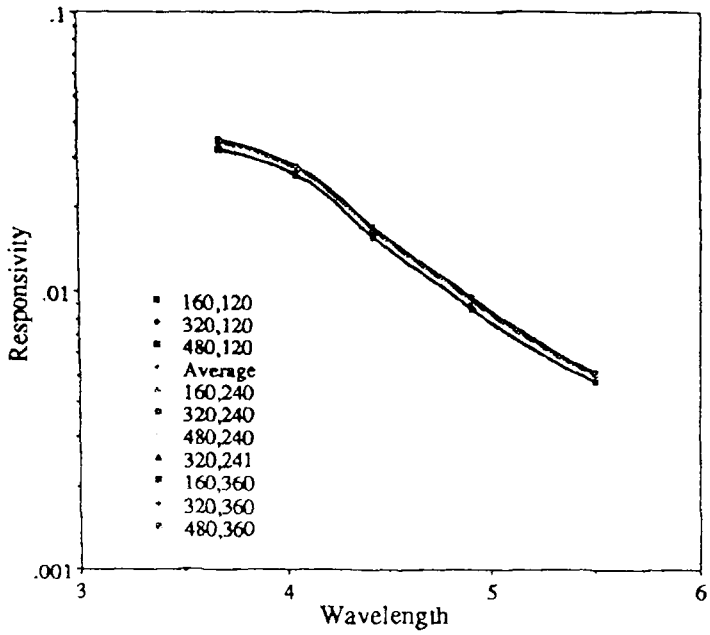


Figure 12 Spectral responsivity of the PtSi array for ten representative pixels.

Also shown is the spectral response of the average pixel. The data in Fig. 12 shows that detectors have practically identical responsivities for the wavelengths of interest (3.5 to 5.5 μm). The spectral nonuniformity is estimated to be ±1.1%. Therefore, pixel to pixel nonuniformities should not vary significantly with incident power spectral density.

3.1.2 Spatial Uniformity

Spatial nonuniformity measures the deviation in a pixel's response to that of the average array response. When the camera is uniformly illuminated, the signal from each pixel in the array should be equal. Furthermore, any change in temperature ΔT should induce equal changes in the pixel signal ΔS. Due to inherent anomalies in the process of

fabricating the imaging chip, nonuniformities in both the offset and slope of the pixel response are present. These nonuniformities need to be corrected for the chip to perform as a radiometer. Correcting for both the slope and offset of individual pixels in an array is called two point correction. Figure 13 shows graphically the procedure for obtaining two point correction*. Part 1 shows the response of any arbitrary uncorrected pixel (i) and the average response of the FPA for two reference

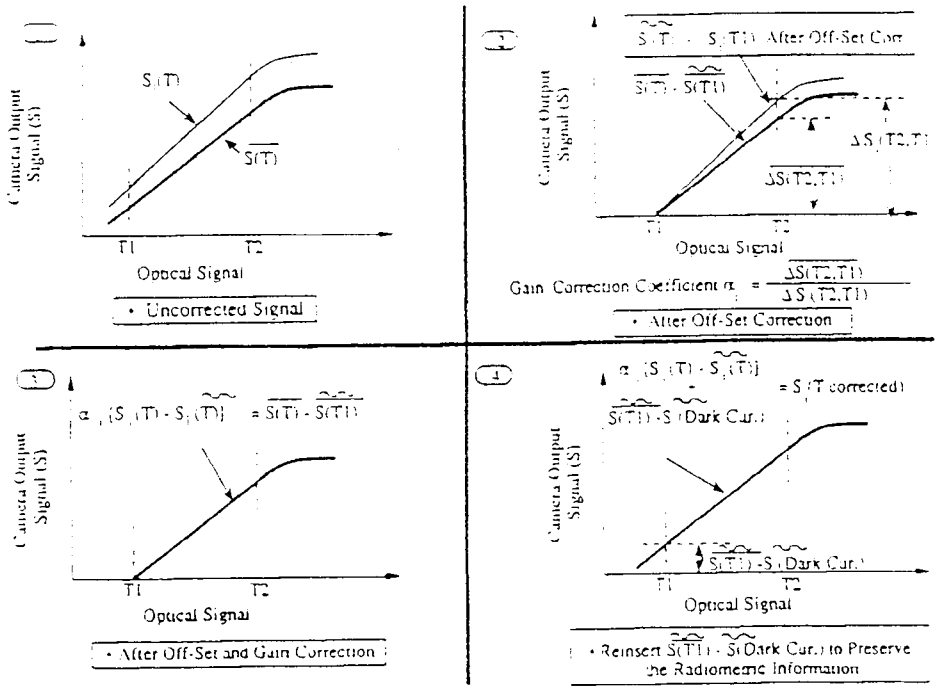


Figure 13 Procedure for obtaining two-point correction.
* The concept of one and/or two point uniformity correction preserving radiometric accuracy was proposed by W.F. Kosonocky prior to the summer of 1992.

temperatures T_1 and T_2. The offset has been subtracted in Part 2 at the temperature T_1 from all pixel responses. At this point, the only difference in pixel responses is due to their varying slopes. Gain coefficients are now

computed which are used to force the differential response of each pixel to be the same as that of the average pixel. This is shown in Part 3. Illustrated in Part 4, to preserve the radiometric information, the same signal due to T_1 minus the dark current is added to the offset and gain corrected signal of Part 3. The reinserted offset signal can be either average array signal or a local average signal near the center of the imager.

Data was acquired by the *FrameGrabber* program at two temperatures (T_1 and $T_2=T_1 + 5°C$) A 20 frame average of the blackbody radiator scene was used to calculate the uniformity of the array. The mean was calculated as the average pixel amplitude of the scene. The response is the measured change in the amplitude of the pixel at the two different temperature scenes. The mean response is the average calculated response of the array. Percent deviations were calculated and the % rms nonuniformity was calculated from these deviations. Data were taken at temperatures ranging from 25 to 65°C at full frame integration. The camera used for this experiment was a camera equipped with two point correction circuitry. The camera was offset corrected while staring at the blackbody radiator to remove irregularities in the emissivity of the square radiator if any were present. Multiplicative coefficients were generated to correct for nonuniformities encountered while staring at 25°C radiation and were stored in memory. These coefficients were applied to the signals acquired at the various temperatures of this experiment.

Figure 14 illustrates the distributions of the array uniformities for the corrected camera. The histogram plot shows the percentage of pixels along the y-axis versus the percent deviation from the mean along the x-axis. The calculated mean is placed at the center of the x-axis and the

number of pixels falling into equally sized bins around the mean are plotted in both directions away from the center. Bins to the left of the mean represent pixels whose displays are darker than average. Fig 14a shows the camera system behaving with high uniformity at the temperature where the coefficients were originally generated. This behavior is expected. As the signal level is increased in Figs. 14(b,c,&d), the detectors respond similarly and the deviation of the pixel response increases only slightly. Above 70°C however, as pixels begin to saturate, the nonuniformities increase dramatically. Also shown in Fig. 14d are two distinct peaks in the plot. This is thought to be due to the uneven responses of the two fields used in the interlaced mode. This deviation is small however.

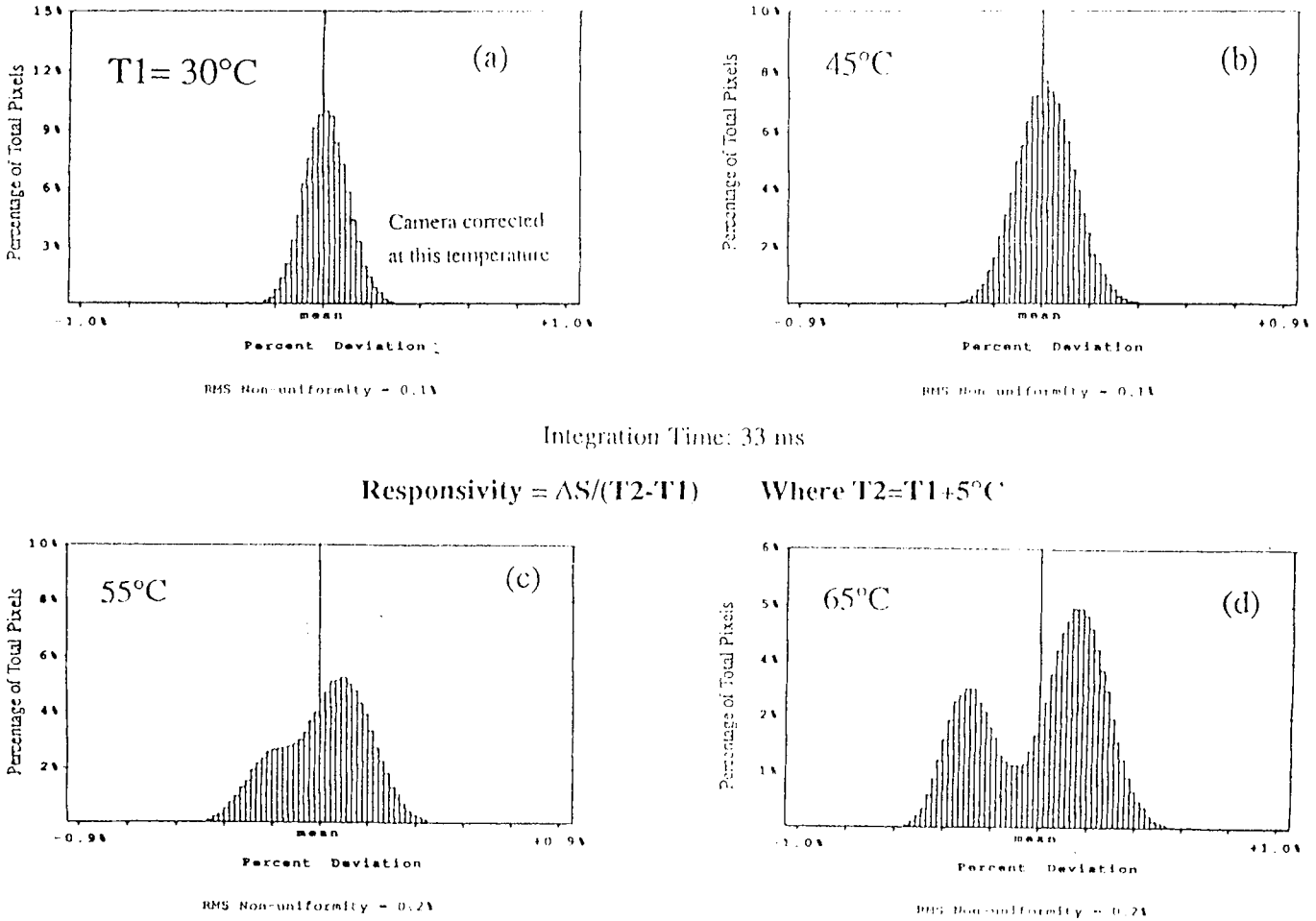


Figure 14 Uniformity of corrected 640 X 480 IR-MOS FPA with temperature.

3.3 Variable Sub-Frame Integration Time

The maximum charge storage capability of the SBD detectors is approximately one million electrons. To find the maximum flux density that will saturate the detectors at normal operation.

$$40\mu m \times 40\mu m = 1.6\times10^{-5}\, cm^2 = A_d$$
$$1\times10^6 \times 0.2 = 5\times10^6\, photons/\text{det}\cdot frame$$
$$\Phi_{ph} = 5\times10^6\, photons/\text{det}\cdot frame$$

This calculation assumes an average photo conversion quantum efficiency of 0.20.

$$E[eV] = h\nu = \frac{hc}{\lambda} = \frac{1.237}{\lambda[\mu m]}$$
$$E(4.0\mu m) = 0.3093 eV$$
$$E = 4.948\times10^{-20}\, J/photon$$
$$N = \Phi_{ph} \div A_d = 3.125\times10^{11}\, photons/frame\cdot cm^2$$
$$P = N\cdot E\cdot F_{rame}R_{ate} = 4.638\times10^{-7}\, W/cm^2$$

This shows the maximum flux (@ 4μm) that the detector can measure without saturating is approximately 0.468 μW/cm^2 · To effectively measure

radiances above this level, the absolute time that the detector "looks" at the radiation should be reduced. The detectors are continually gathering electrons so excess charge will quickly accumulate when staring at high temperature scenes. The frame readout time cannot be changed, so the

time the detectors spend gathering useful data should be a fraction of the frame time. The operation of the camera with variable integration time requires the detectors be reset at a precise time before transferring the charge to be read out.

The IR-CCD imager transfers charge from all pixels to the readout simultaneously. This means that the imager essentially takes 'snapshots' of the infrared scene. This made the camera the better choice for our camera design. However, sub-frame integration with IR-CCD imagers cannot be accomplished in the same way as IR-MOS imagers because there is no way to interrogate lines or pixels, and the primary mechanism for removing charge is through the CCD channels. In the IR-MOS, each line is read out sequentially whereas in the IR-CCD readout, the pixels are transferred simultaneously with a universal transfer pulse. To implement integration time control, the charge needs to be swept out through the CCD registers. A dump-and-read procedure was developed to facilitate this clearing of excess charge [14]. To investigate the quickest and most efficient means to clear the excess charge, clocking circuits were developed to allow different frequencies to act as the master clock. The sweep out procedure begins as charge that has accumulated in the detectors from the last transfer pulse is transferred to the B-registers through a transfer pulse. The B-registers are then clocked rapidly and charge immediately saturates the C-registers that are simultaneously clearing charge through the output amplifier. The sweep out procedure is completed as the charge is cleared from all the CCD registers.

A test camera was then retrofitted with the custom clock chip and the charge was swept from the array at different rates. At 12 MHz, the charge was shown to be cleared from the array in two line times. At high

illumination, the inefficiency present at this sweep rate becomes significant and increases the sweep time to five lines. The charge is cleared from the B-registers in two lines but three additional lines are required to clear the C-registers. The minimum optical integration time available for this camera is two line times or 127μs. To insure radiometrically correct data, the first ten lines of video should be discarded at this integration time, because they contain residue charge from the inefficient sweep procedure. It is important to note that as the charge is being swept out of the CCD channels, photo-charge is accumulating in the SBD detectors. This represents the first charge of the signal data.

The operation of variable integration timing is shown pictorially in Fig. 15. The first frame 15a begins the sequence with the detectors fully saturated. Clearly shown are the B-registers with two SBD detectors connected to each register. With the camera operation only utilizing half vertical resolution, only one pixel will be used per vertical register. This saturation charge needs to be swept out and is transferred to the B-registers in 15b. In 15c, the charge is clocked down and out at 12MHz/16 from the horizontal register. Shown in 15d, the B-registers are cleared in 127 μs. The C-register may contain some residue charge. During the sweep out, charge can be seen collecting in the SBDs. The integration time initialized when dump sequence began and charge was transferred to the B-registers. After the required optical integration time has integrated, the signal charge is transferred to the B-registers in 15f. The charge is then read out at video rate as shown in 15g and 15h. Dump charge for the next sweep out is seen to collect during readout. The variability of integration time can be controlled in increments of line times. The timing diagram of sub-frame optical integration time is shown in Fig. 16. A frame can be thought of as

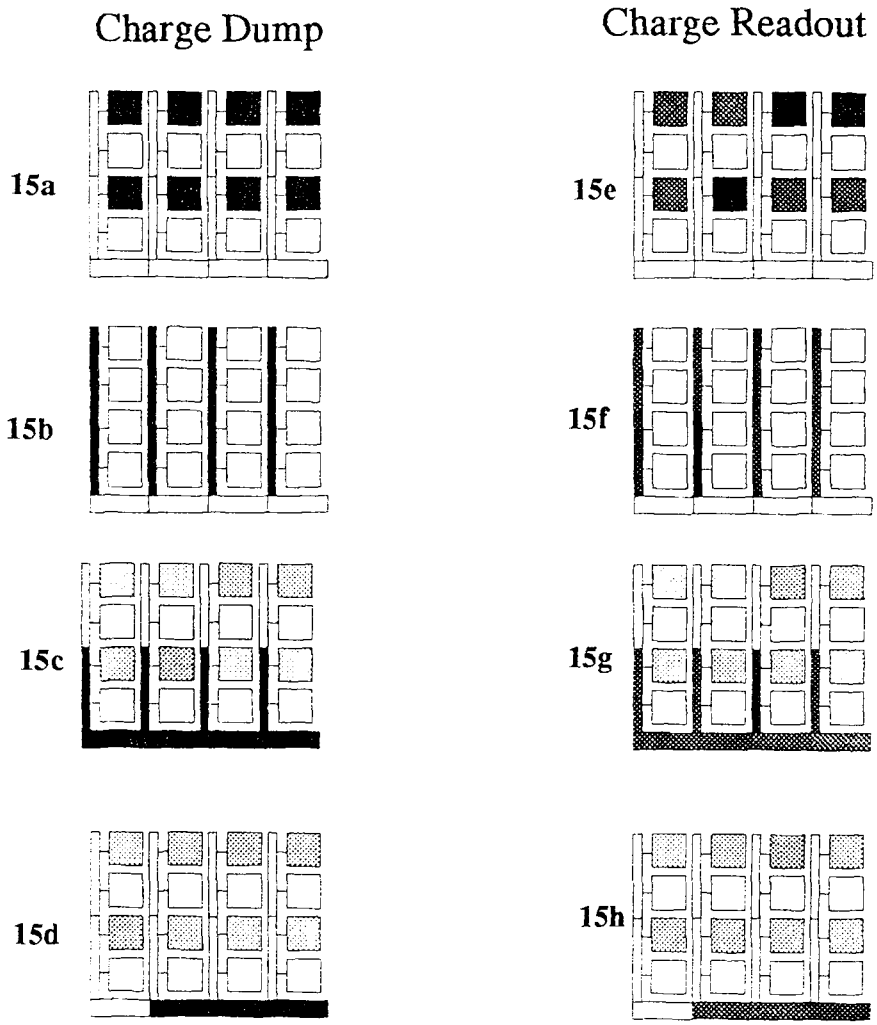


Figure 15 The operation of the 320 X 122 IR-CCD imager for sub-frame integration.

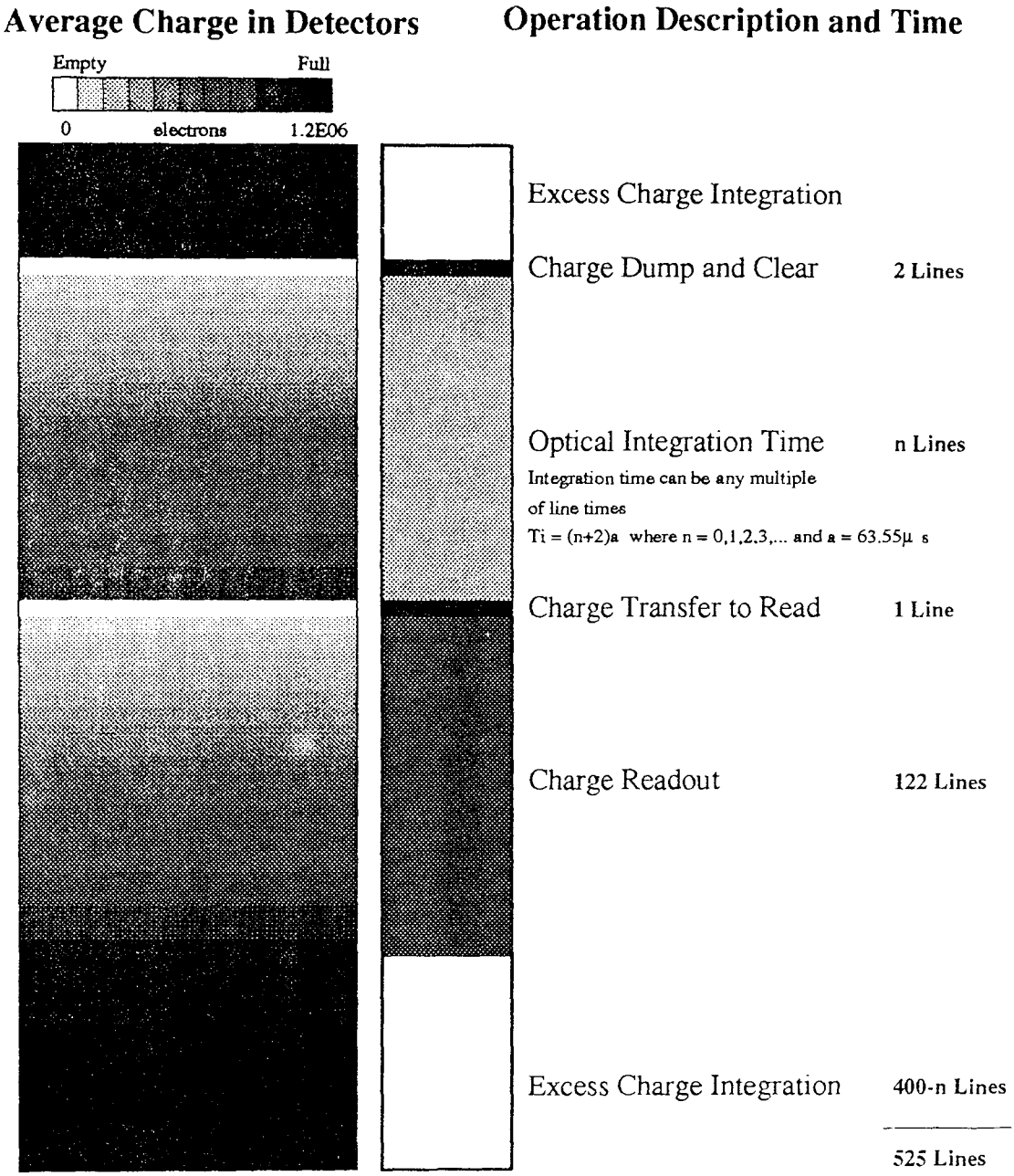


Figure 16 The timing diagram for variable optical integration time.

525 lines. Taking into account all required timings, one variable is left. The integration time can be set to any integer of line times greater than or equal to zero. The excess dump charge integration is determined from the integration time.

3.4 Variable Multi-Frame Integration Time

When imaging scenes of low temperature, the reduction in flux causes a reduction in the amount of charge signal integrated over standard 33 ms operation. This decreases the signal to noise ratio and the response of the camera deviates from linearity. To improve the radiometric performance, the optical integration time should be increased. With the understanding of sub-frame charge integration, it is easy to extend this concept to charge integration times larger than 525 lines. By suppressing the readout at the normal frame rate, the imager is allowed to integrate charge for a certain number of frames before being readout. Shown in Fig. 17 is the timing diagram for supra-frame optical integration. There is no dump procedure, only integration and readout and all charge is used in the signal. This is essential when viewing low radiance scenes. The frame rate of the camera must be decreased because the rate at which new information is generated decreases below 30 frames/s. The maximum integration time is limited by the detector shot noise as this signal is also being accumulated during integration.

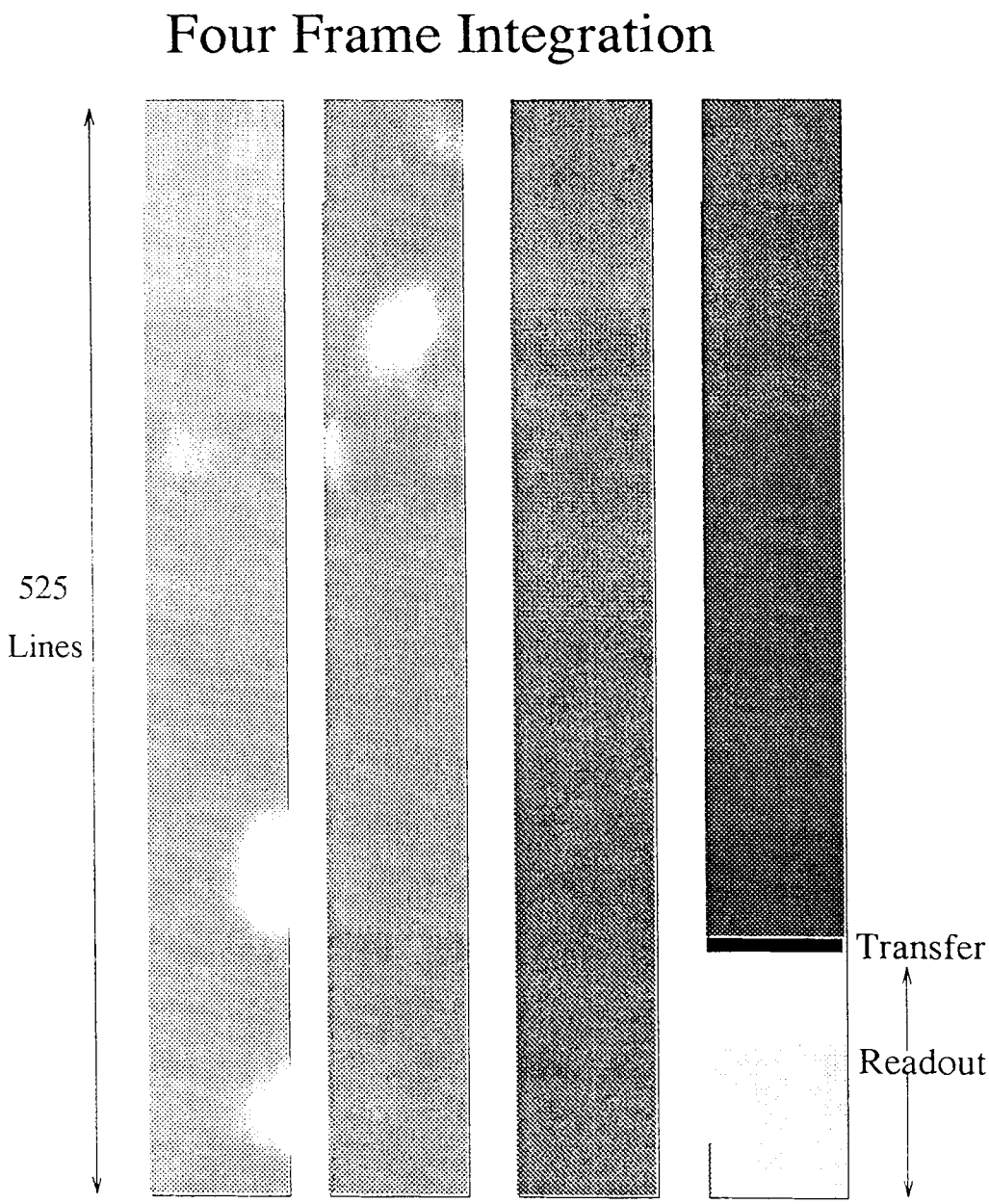


Figure 17 Multi-frame Optical Integration.

CHAPTER 4

4 CAMERA ELECTRONICS

There are two separate units that comprise the total camera system, the camera head and the video processor box. The camera head electronics (with the exception of the custom sequencer board) have been built using the designs and printed circuit boards developed at the David Sarnoff Research Center. These designs are markedly different in their layout than from previous cameras developed for NJIT and described in thesis by Patel [11] and Blume [15].

4.1 Camera Head

The camera head consists of four printed circuit boards affixed to the mini-sized liquid nitrogen dewar. Also affixed to the dewar is the imager chip. The chip is placed in a vacuum chamber with a 2" silicon window to allow incident light to be imaged. The dewar holds 0.5 liters of liquid nitrogen and it is easy to calculate the approximate heat load on the system and the approximate nitrogen replacement time using the Stefan-Boltzmann relation of equation (3). Assume the imager is staring at 1000°C radiation.

This radiation can be assumed to fill the sensor's hemispherical field of view, $\gamma = \pi \cdot A_{chip}$. Then

$$\Phi = L_{1273} \cdot \pi \cdot A_{wndw} = \sigma \cdot T^4 \cdot A_{wndw}$$
$$\Phi = 5.67X10^{-8}\left[W \cdot m^{-2} \cdot K^{-4}\right] \times 1273^4\left[K^4\right] \times$$
$$10^{-4}\left[m^2 \cdot cm^{-2}\right] \times (2 \times 2.54)^2\left[cm^2\right] \times \frac{\pi}{4} \qquad (22)$$
$$\Phi = 301.8W$$

Using the heat of vaporization for liquid nitrogen of approx. 752.5 W·liter^{-1}·h^{-1}, The sensor requires 0.4 liters of liquid nitrogen per hour to absorb the heat load in a 2 inch diameter aperture while staring at 1000°C radiation.

The four boards that make up the camera head electronics are:

- Bias Board
- Clock Generator or Variable Integration Sequencer
- Analog Board
- Pre-Process Board

Shown in Fig. 18 is a scale drawing side view of the dewar assembly with the four boards assembled. The entire camera head measures 10.4 X 5.7 X 4.8 inches. The camera head is connected to the video processor by a 34-pin connector cable.

4.1.1 Bias Board

The bias board is mounted rearmost and provides back panel access to all analog chip voltage levels set by potentiometers for calibration and adjustment. Probe pins are placed next to each of the 23 potentiometers to

allow for convenient connection to measurement equipment. The board has two connectors with connector 1 (60 pin) connected to the back-plane and connector 2 (60 pin) connected to the pre-process board.

4.1.2 Analog Board

The analog board resides in front of the bias board to the rear of the camera and provides analog signal amplification and control for transmission to the

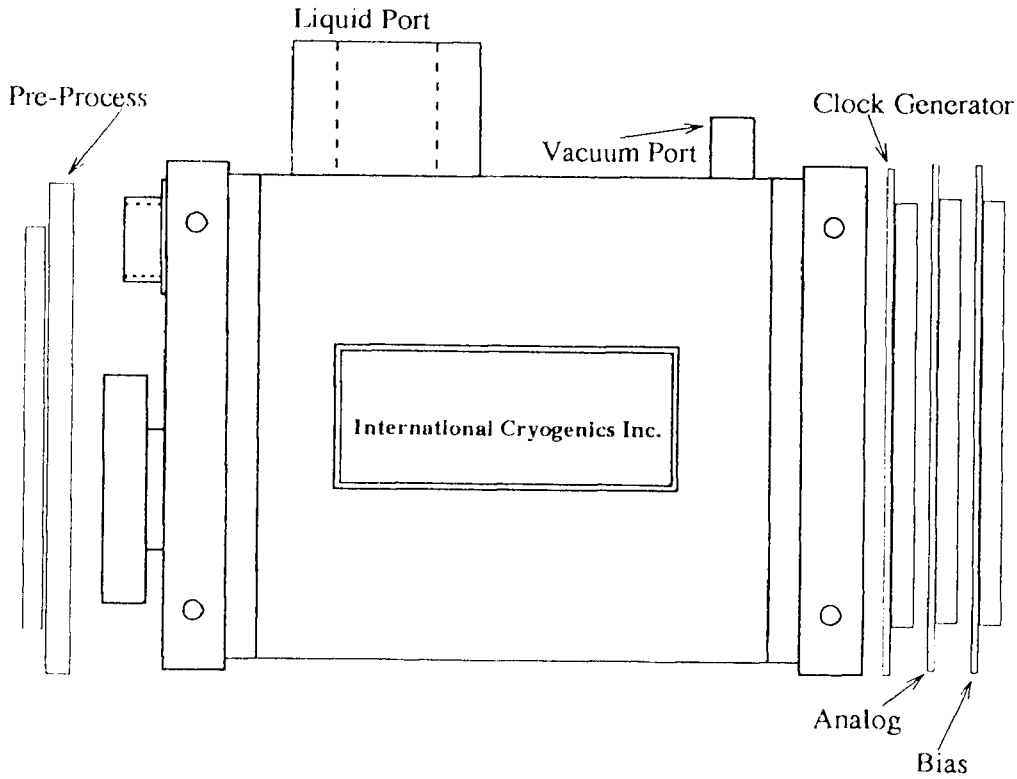


Figure 18 Dewar Assembly (side view)

video processor unit. Synchronization pulses provided by the clock board are added to the "raw" signal to provide a composite video signal. The

video signal is sent from the pre-process board and is processed by a correlated
double sampling (CDS) unit. This sampling reduces the sampling noise that occurs when more primitive sampling methods are used. For a discussion of CDS circuitry, see Romanowich [16]. Potentiometers external to the camera on its rear panel control the initial gain and offset of the camerafor RS-170 display. The analog board receives these signals and impresses gain and offset onto the sampled video. The synchronization pulses are imposed onto the video and composite video is routed to an SMA connector at the rear of the camera. This video may be used to display the image on a standard RS-170 monitor or may be sent to the video processor. Two ribbon connectors attach this board to the camera system. Connector 1 (60 pin) is connected to the back plane and Connector 2 (14 pin) is connected to the gain/offset pots.

4.1.3 Pre-Process Board

The pre-process board is located at the front of the dewar, near the imager chip. The board is shaped like a horseshoe to allow for the installation of the cold shield assembly. The board is connected to the imager chip via a 22 pin hermetically sealed gold connector. The connector provides electrical access to the vacuum chamber. All input bias and clock signals as well as output pixel data are sent via this connector. Biases sent to the pre-process board from the bias board are buffered and routed to the dewar connector. Clock biases are imposed on clock signals generated in the clock board and drive the CCD imager with clock phases timed and biased for optimal performance. The output video is buffered with a low-noise buffer amplifier and the pixel data are amplified on board before being

sent to the analog board. There are three ribbon connectors that are connected to the bias board. Connector 1 has 26 pins, Connector 2 and Connector 3 each contain 14 pins.

4.1.4 Standard Clock Generator

The standard clock generator contains a programmable gate array (PGA) that is programmed to operate the imager at 320 X 244 resolution with interlaced 30 frames/sec display. Interlaced operation is a frame integration mode [1-3] where the field rate is 60 frames/sec and alternating fields are overlapped to prevent flicker effects in the display. Flicker is a psychophysical effect and interlacing the frame accomplishes the same flicker reduction as increasing the frame rate [17]. The resulting output conforms to the RS-170 format [18], suitable for display standard NTSC compatible monitors.

The signals generated to synchronize the processor are vertical active (VA), horizontal active (HA), system clock (CLOCK), horizontal sync (HSYNC), and camera lock (LOCK). The relationship between these signals in the standard mode of operation is shown in Fig. 19. The VA pulse is active high at the start of the frame. It is followed immediately by a falling edge of HA. HA is active high for 52 μs after an 11.5 μs blanking period and the rising edge of HA signals the start of a line. CLOCK is a 12 MHz signal with 50% duty cycle. The CLOCK is used to synchronize all operations. HSYNC provides a synchronization signal to create the front and back "porches " needed to run on an NTSC system. LOCK is a negative pulse one pixel wide at a rate of 30 Hz that is pulsed immediately following the rising edge of VA if present. The measured signals are shown in Fig. 20.

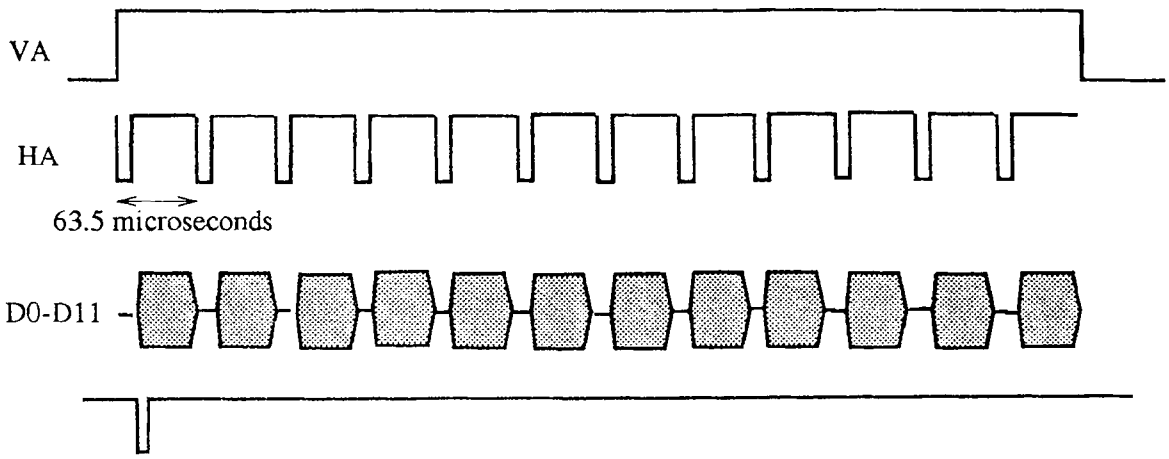


Figure 19 Timing Relationships for Normal Operation of 320 X 244 Camera.

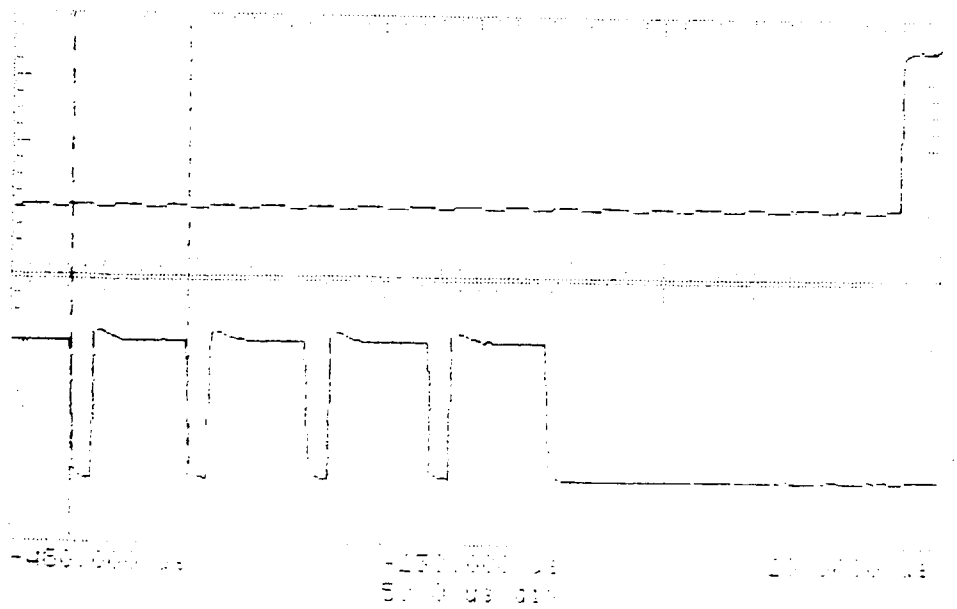


Figure 20 Measured Timing Signals in Normal Operation.

This board was constructed to allow for the standard operation of the camera with full resolution video imagery. It also facilitated the testing of the camera at an early stage, and so data comparisons between existing cameras could be done. The clock generator board sits in front of the analog board, at the rear and adjacent to the dewar. Two connectors are needed to connect this board to the system. Connector 1 (60 pins) is connected to the back plane while Connector 2 (40 pin) is connected to the 34 pin cable connecting the processor and the head. All power and non-video data communication is contained in this connection. A power harness was fabricated to allow for the testing of the camera head without the need for the processor box by mimicking Connector 2 and its power pin connections. Power supply connections (banana) are marked to allow for the autonomous operation of the camera head with suitable bench power supplies.

4.2 Variable Integration Sequencer

This board was custom designed for the specific application outlined in this thesis. This board receives a four-bit nibble representing the integration time suggested by the video processor box and automatically sequences the operations required to perform the dump and read procedure described in the previous chapter. There are four operating modes of the sequencer in any integration time: READOUT, DUMP, TRANSFER, and SWEEPOUT. The integration time is input to a differential receiver (SN75ALS193) and input to a XILINX (XC3042-PC84) field-programmable gate array (FPGA). The array provides pulses to the stand-alone microsequencer (SAM) to generate the proper transfer and CCD clock pulses to perform variable integration. The XILINX FPGA provides

pulses DUMP, SWEEP, and TRANS to the Altera (EPS448) SAM. The SAM is user configurable and is a function-specific programmable state-machine. The internal EPROM memory allow up to 448 unique states to be specified and contains an internal clock and a pipeline register for high speed output state transition operation. By impressing a "1" to any of the three inputs, the SAM switches to one of three modes.

The operation of variable integration will be explained by "walking through" a sample cycle beginning with the charge transfer and ending with a high speed sweep of dump charge.

If the TRANFER pin is at logic 1, the SAM will be placed in the TRANSFER mode. In the TRANSFER mode, the SAM is programmed to pulse the proper B-phase with a transfer pulse to clear the detectors and drive the contents into the B-register. The beginning of the line clears the register with 31 high speed B-clocks. The diode transfer pulse occurs after the phase between the C and B registers is set. The transfer pulse is approximately 10 μs. The C-register is clocked during transfer to sweep out any excess charge. Shown in Fig. 21 is the general measured relationship of the clocks during transfer.

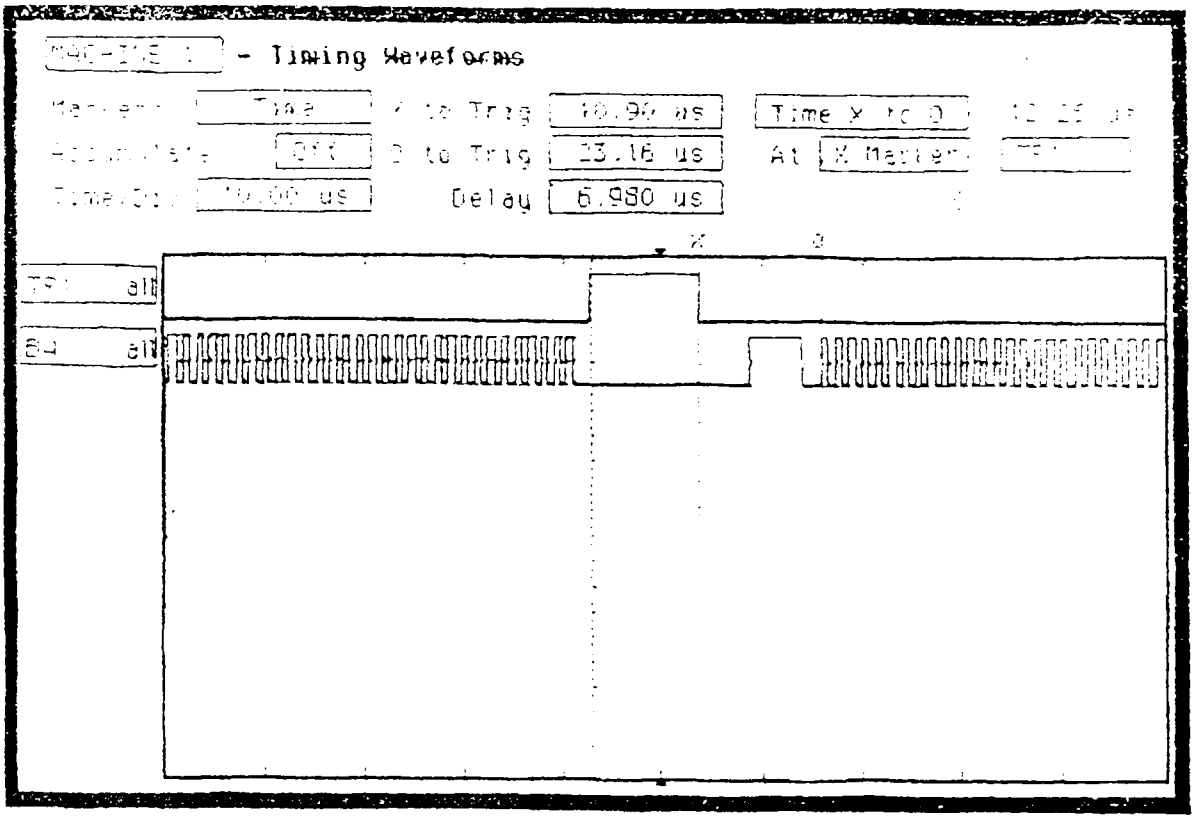


Figure 21 TRANSFER mode waveforms (measured).

If all three control pulses are at logic 0 the SAM is placed in the readout mode. In the READOUT (default) mode, the B-clocks are operated for four-phase standard operation at the line rate of 63.55 μs. The C-clocks operate in four-phase readout at the pixel rate. Several additional C-clock pulses occur after the falling edge of HSYNC to provide for overscan. Figure 22 illustrates the clock waveforms in the READOUT mode.

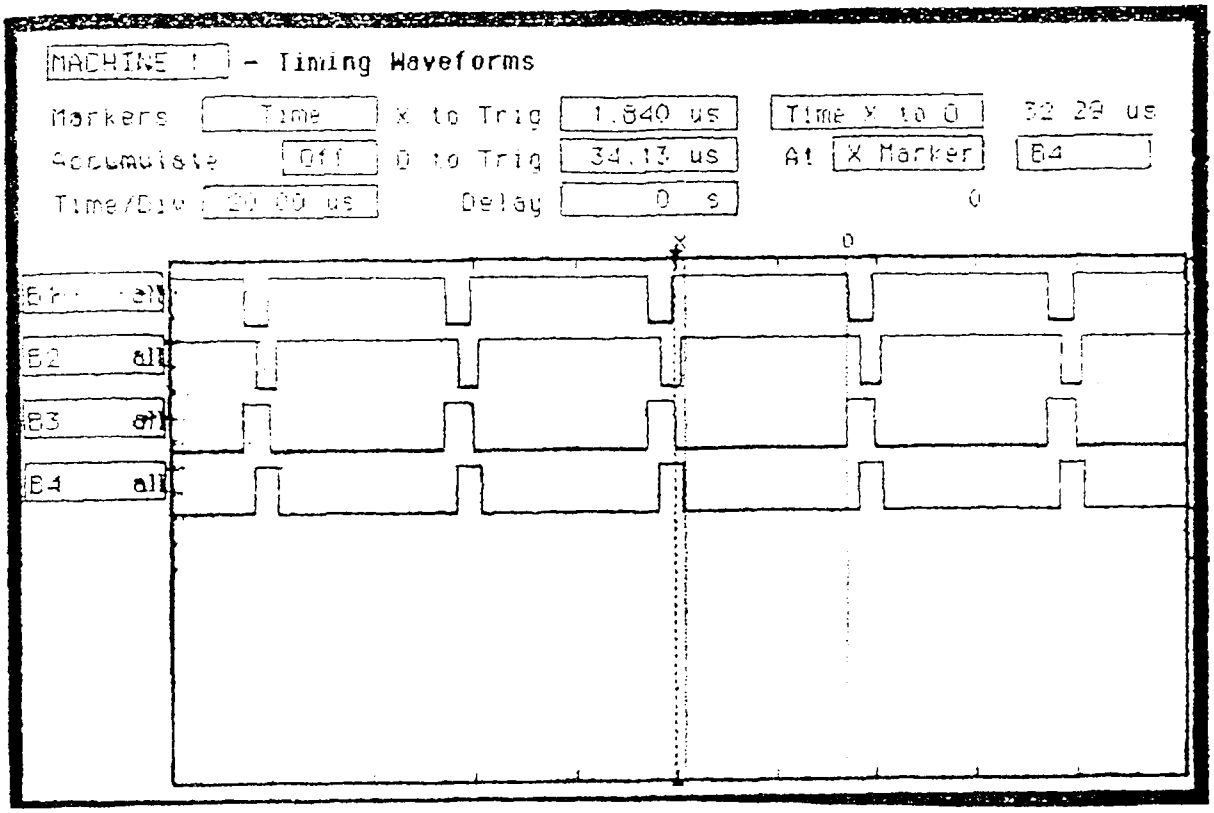


Figure 22 READOUT mode waveforms (measured).

After READOUT, the detectors have been integrating dump charge. By impressing a "1" on the DUMP pin of the SAM, the DUMP operation begins. This mode is similar to the TRANSFER mode, however, there are no clear pulses for the B-register and the beginning of the line starts with a 10ms long transfer pulse. The B-clocks are run continuously at the high rate of 750 X 10^3 transfers/s. The C-register is also being clocked continuously including overscan. At the end of the line, the timing generator internal to the SAM checks to see the next state sequence. Fig. 23 shows the waveforms associated with the DUMP mode.

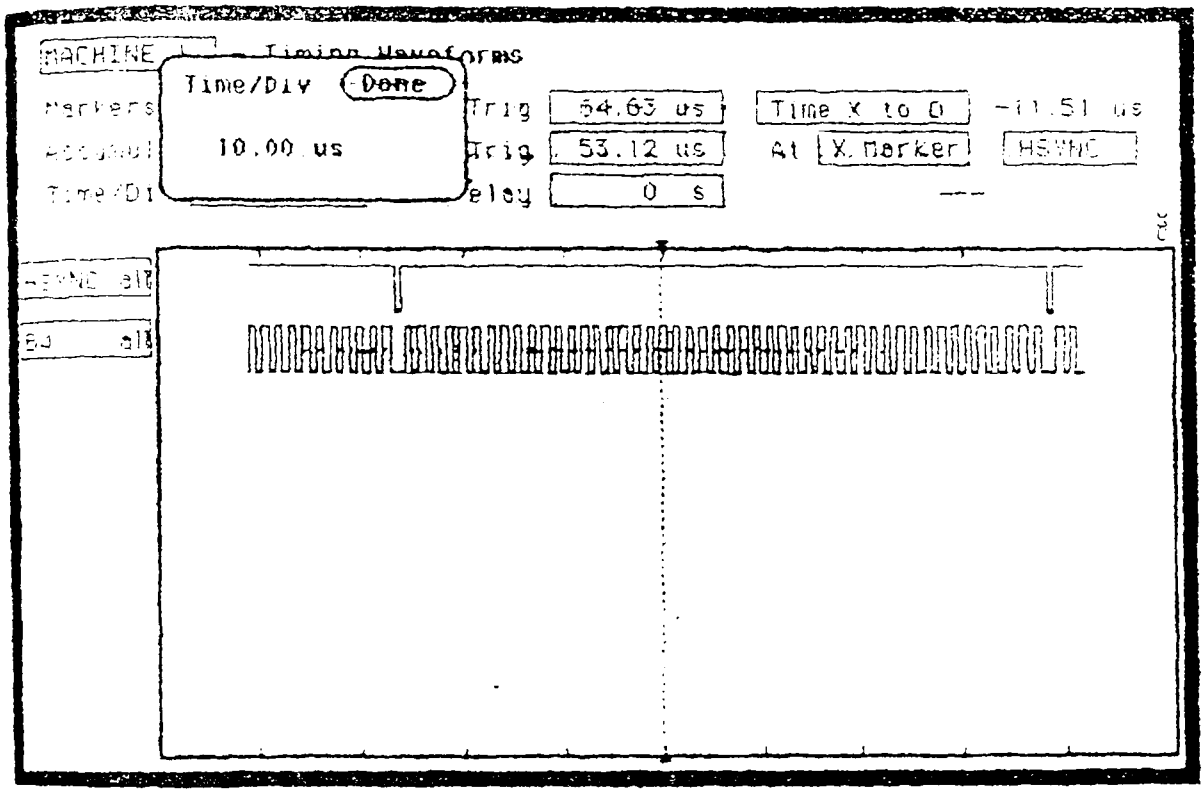


Figure 23 DUMP mode waveforms (measured).

The SWEEP mode continues the clearing of dump charge that was initiated in the DUMP operation. Both the B and C clocks are operated continuously at high speed to remove charge from the registers. Shown in Fig. 24 are the waveforms associated with the SWEEP mode of operation.

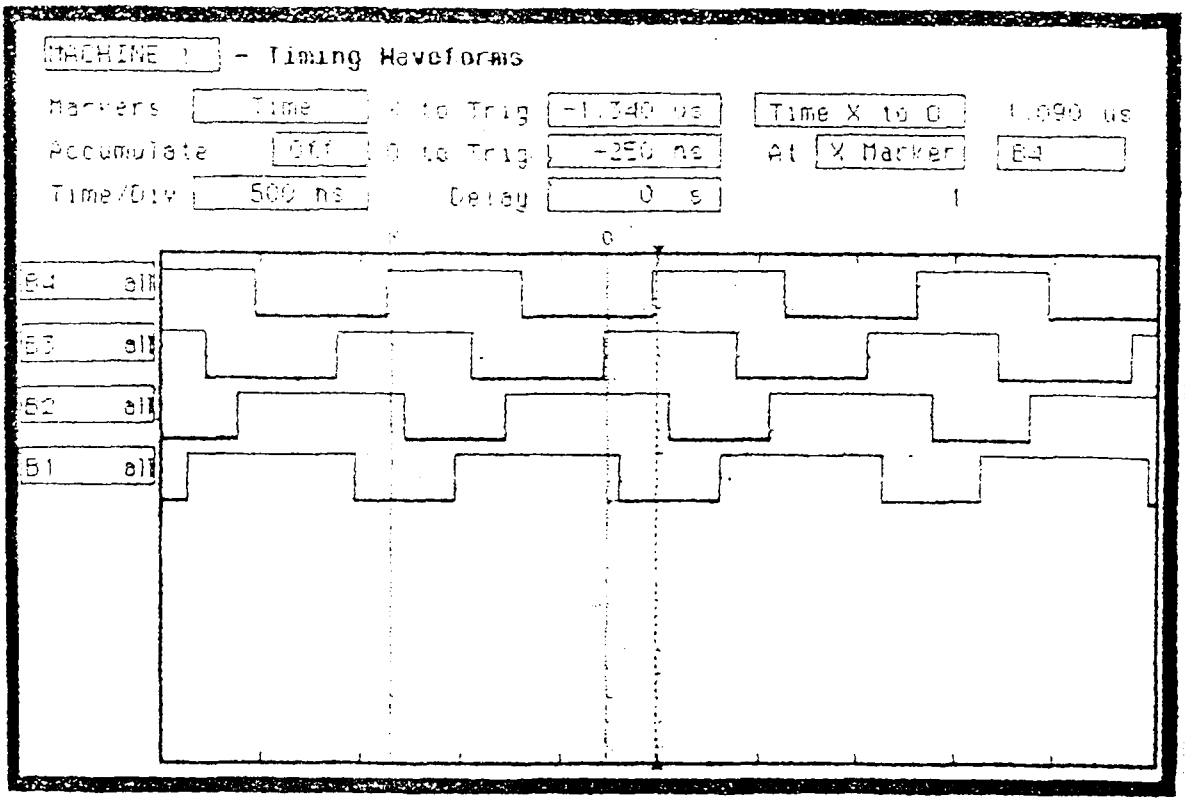


Figure 24 SWEEP mode waveforms (measured)

It should be noted that the state of the pulse applied to the SAM should be stable while HSYNC is low. The XYLINX provides the pulses in the correct sequence and at the proper time. The timing diagrams of Figs. 16 and 17 provide all the information necessary to properly time the sequence for any integration time.

CHAPTER 5

5 VIDEO PROCESSOR

The video processor provides digital conversion and manipulation for signal processing. The video processor also provides feedback (either manual or automatic) to control the optical integration time. The main user interface is through the processor and the ports which connect the camera to other computing and control equipment is through the processor. The processor box contains all the power supplies necessary to run the processor and the camera head. The box measures 17 X 18 X 5.5 inches and contains a card cage with 10 slots to provide for adaptability and easy maintenance. PC-type edge connector cards with 102-pin Euro connectors are used and the card cage back plane is set up with the data stream running from left to right when viewed from the front. This means that the order that the cards are placed in the cage is critical. Shown in Fig. 25 is a drawing of the processor box.

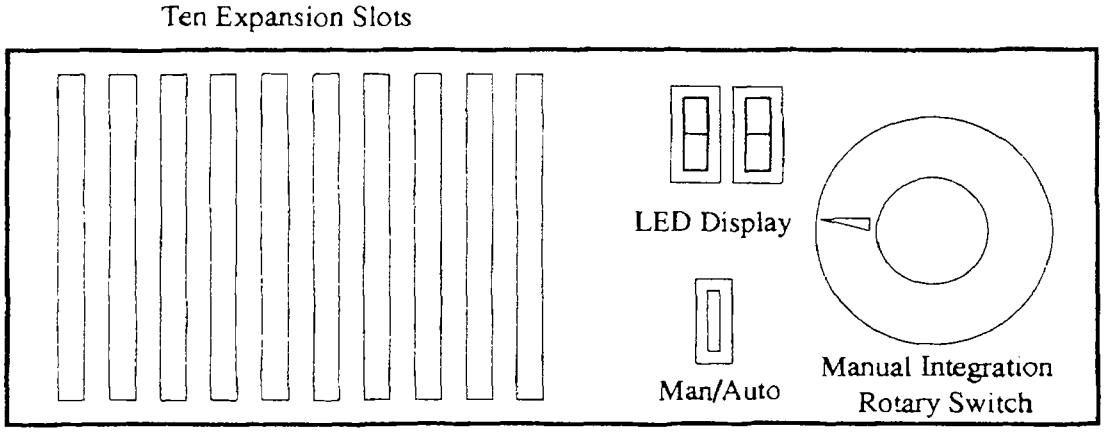


Figure 25 The video processor.

While there are no necessary boards required to operate the camera, the analog to digital (ADC) board and the output board are required to operate the camera with the Datacube. Datacube is needed to provide flexible real time digital video processing capabilities. Currently there are five boards completed for implementation in the processor.

- A/D Board
- Multifunction Board
- I/O Board
- Test Board
- Jumper Board

5.1 Analog to Digital Conversion

The video signal that arrives at the video processor port is in sampled analog form. The pixels are discrete packages of information in analog form streaming in at approximately 6 Msamples/s. The video signal is digitized with 12-bit resolution by utilizing the Burr-Brown 10MHz 12-bit A/D converter (ADC603H). The ADC converts analog signals with a full scale range of -1.25 to +1.25 volts. The conversion is enabled by the clock pulse acting as the sample. On-board digital delay circuitry insures that the clock pulse is positioned at the center of the pixel to obtain the most accurate sampling. The data is converted into inverted two's complement form. The MSB of the data is inverted to convert the word into pure binary representation. The conversion is shown graphically in Table 2.

Therefore the data can assume 4096 discrete states with each state corresponding to a voltage change of 0.61 mV. This is the resolution of the converter board. The conversion linearity error is listed as ±0.5 LSB [19].

Table 2 True binary conversion from the output of the ADC 603 chip

Analog Signal Level	Inverted 2's Complement	True Binary $\overline{MSB}$	Decimal Value
+ Full Scale	011111111111	111111111111	4096
+ 0.75 Scale	011000000000	1110000000000	3584
+ 0.50 Scale	010000000000	1100000000000	3072
+ 0.25 Scale	001000000000	1010000000000	2560
+ 1 Bit	000000000001	1000000000001	2049
Zero	000000000000	1000000000000	2048
- 1 Bit	111111111111	0111111111111	2047
- 0.25 Scale	111000000000	011000000000	1536
- 0.50 Scale	110000000000	010000000000	1024
- 0.75 Scale	101000000000	001000000000	512
- Full Scale	100000000000	000000000000	0

The digital data is then sent to the next board in the stream but is also available and ported to the rear of the processor box as uncorrected digital video. The next board in line to process video is the multifunction board. A board was developed to simulate the A/D board and it provides test patterns for evaluation of the processor box.

5.2 Simulator Board

The Simulator board resides in the same slot as the ADC board. By replacing the ADC board, the Simulator board emulates a temporally and spatially noise-free digital pixel stream. The board consists of two pattern

generators and twelve 2:1 multiplexers to choose one of the two patterns. The patterns are generated from the control signals sent from the camera head (VA, HA, and CLOCK). The patterns simulate a horizontal ramp assuming all pixel values and a set of sixteen horizontal bars of multi-line width. The board allows the evaluation of the digital noise generation in the video processor, enables the investigation of the least significant bit operation as the camera noise de-stabilizes these pixel values, and allows for accurate linearity testing of processor components and computer interfaces.

The first test pattern produces a linear ramp across each line by clocking an 8-bit counter circuit at the pixel rate and applying the count as the 8-MSBs of the digital stream. The 4-LSBs are held at logic 0. The count is cleared at the beginning of each line producing a pattern that increases in intensity to column 256 and repeats to column 320. The count is disabled during ($\overline{VA} \cup \overline{HA}$.)

The second test pattern is generated by clocking an 8-bit counter at the line rate (HA) and applying the count to the 8-MSBs of the digital video bus. The 4-LSBs are all set to logic 1. The count is cleared at the beginning of the frame and counting is disabled during ($\overline{VA}$). The pattern appears as horizontal bars increasing in intensity with each row. Shown in Fig. 26 are the actual test patterns generated by the camera and input into the Datacube system. The images were acquired and stored with a Sun computer. The images were subsequently transferred in digital format over the INTERNET computer network to another computer system and printed.

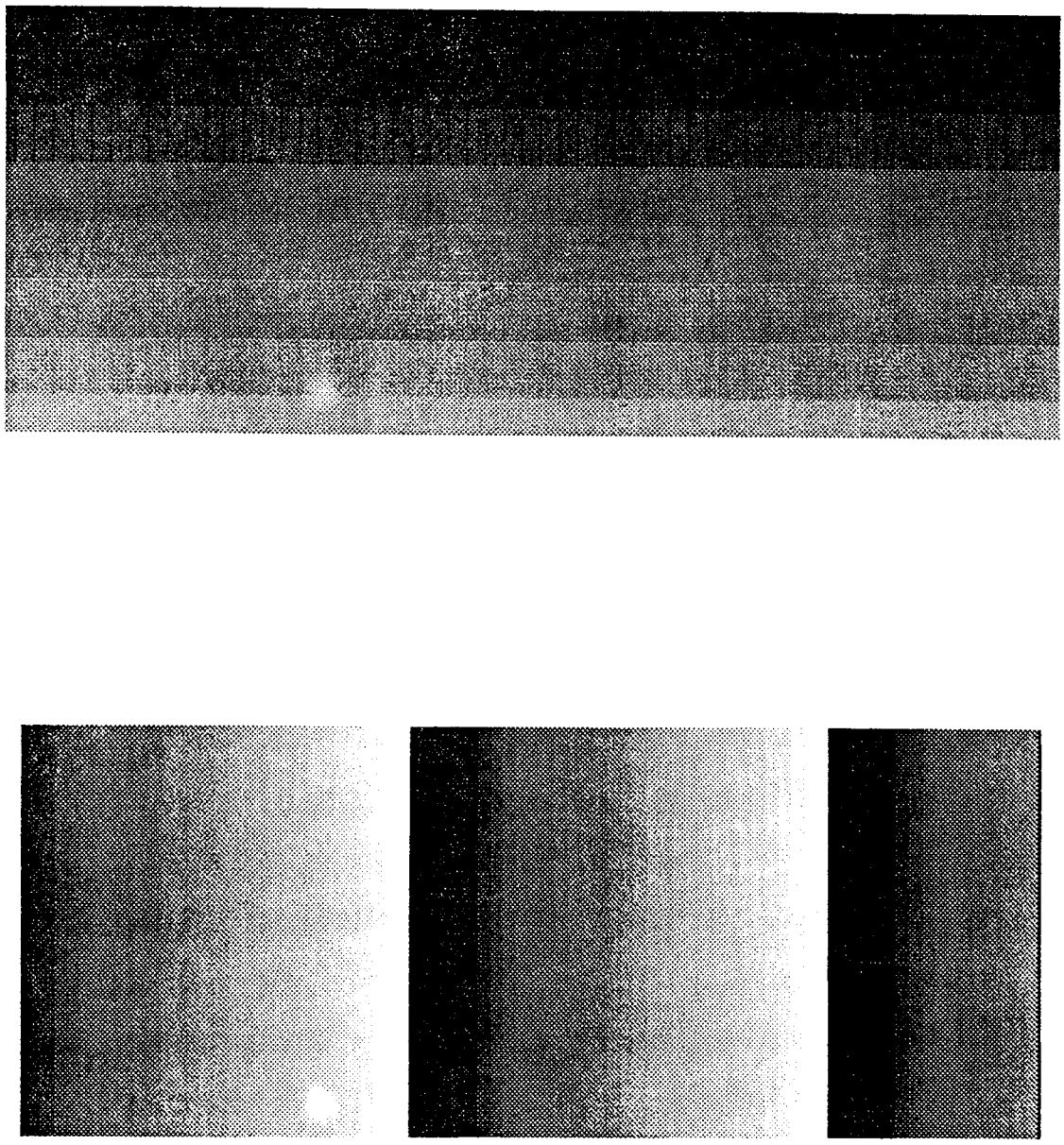


Figure 26 Test-pattern images acquired and stored by a Sun computer.

5.3 Multi-Function Board

The radiometer is designed to automatically control the exposure time and relay the exposure time to the processing computer. A time base must also be generated to coordinate the data acquired from other diagnostic equipment. These functions are performed on the multifunction board. This board resides in the video processor box directly downstream from the A/D or Simulator boards.

5.3.1 Head Receiver

This circuitry receives differential data transmitted from the camera head representing all timing signals generated there and transforms them into single ended TTL signals suitable for further processing. Two SN75ALS193 differential receivers are used to accept differential control signals from the camera head. These signals are input with the 12-bit data to a 16-bit latch constructed from 74ALS273 Octal D-Type flip flops. All signals are now latched on to the board with the came clock pulse and are lined up in time.

5.3.2 Variable Integration Time with Front Panel Display

The camera's integration time can be analogized as the exposure time in a film camera system. As the photon flux density increases, the charge saturation signal (approx.$1X10^6$ electrons) of the SBD pixels is approached. The integration time must then be reduced to provide a non saturating signal that lies in the linear response region of the camera. Equally important, if the photon flux rate decreases, the integration time must be increased to keep the signal in the linear portion of the response as well as to preserve the signal to nose ratio at a respectable level. The

frame may be considered the collection of 39040 pixels and the design of a robust control circuit for the integration time must be flexible. The control scheme compares the pixel signals individually and then decides upon action after considering the state of the entire ensemble of pixels that make up the frame.

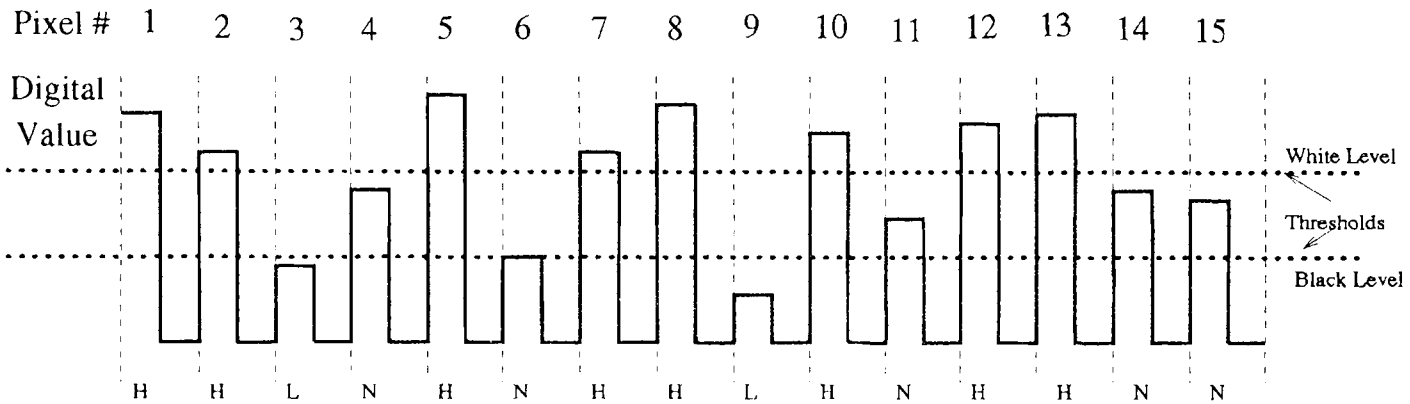
The control of the optical integration time is performed digitally for greater flexibility, lack of drift and ease in implementation. The video signal is compared against preset levels to determine the state of the pixel. This is accomplished with 74LS682 Octal Flash Comparators that output a zero whenever the P (video) inputs exceed the Q (switch) inputs. In the case of white pixels, the Q inputs are provided by an octal DIP switch wired to represent logical signals. Pixels that are out of these preset ranges are counted and compared against preset total pixel counts pre-stored on-board. The white level is set to the top eight video bits (D04 to D11), representing signals ranging from 0.36% to 99.63% of the full well signal. The Black level is set with th P inputs logically switched with an octal DIP switch to the video bit signals D03 to D10, representing signals ranging from 0.17% to 49.82% of the full well signal. The pixel counts are chosen from the top eight bits of a sixteen bit pixel counter. These thresholds are summarized in Table 3.

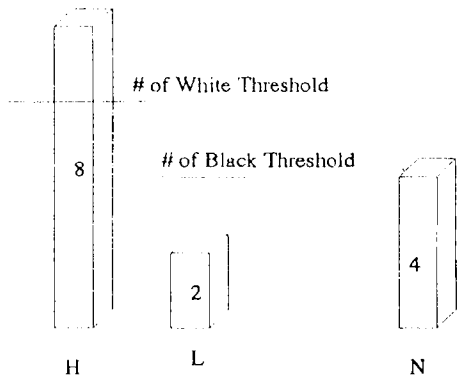
Table 3 Threshold levels as a percentage of full well signal.

Threshold Type	Lowest Count	Percent of Total	Highest Count	Percent of Total
White Pixel	000000001111 (15)	0.36% (4095)	111111110000 (4080)	99.63% (4095)
Black Pixel	000000000111 (7)	0.17% (4095)	011111111000 (2040)	49.82% (4095)
Pixel Count (B/W)	00FFH (255)	0.65% (39040*)	FF00H (65280)	100% (39040)

* This represents the pixel count for 320X122 pixels (9880H). Setting the pixel count threshold higher than 9880H will disable the automatic integration time for black and/or white pixels.

The method employed in this effort is shown symbolically in Fig. 27. The data are shown streaming from left to right with their bar heights proportional to their magnitude. Gating circuitry insures that only valid pixels are compared by enabling flash comparison only during (VA AND HA) pulses. Also shown are the black and white threshold levels which are user settable from on-board 8-pin DIP switches. Pixels that exceed the white level are tagged as high and pixels that fall below the black level are deemed low. Pixels that fall between the levels are set as neutral. These pixels are counted separately and stored in two registers (16-bit counters 74LS161). At the end of the frame, the signal $\overline{VA}$ latches these totals (74LS274) and compares the top eight bits of the counts against the pixel count thresholds for both black and white totals. The signals TOOLITE and TOODARK are used as inputs to a combinational logic circuit that performs the operation shown in the truth table at the bottom of Fig. 27.





#W	#B	INT
0	0	nothing
0	1	increase
1	0	decrease
1	1	nothing

Figu Variable Integration Calculation

This output is applied to a binary up/down counter providing a four-bit nibble representing the integration time. Decoding circuitry prevents the integration time from exceeding the operating range 0-11 (0000-1011). This circuitry is shown in Fig. 28.

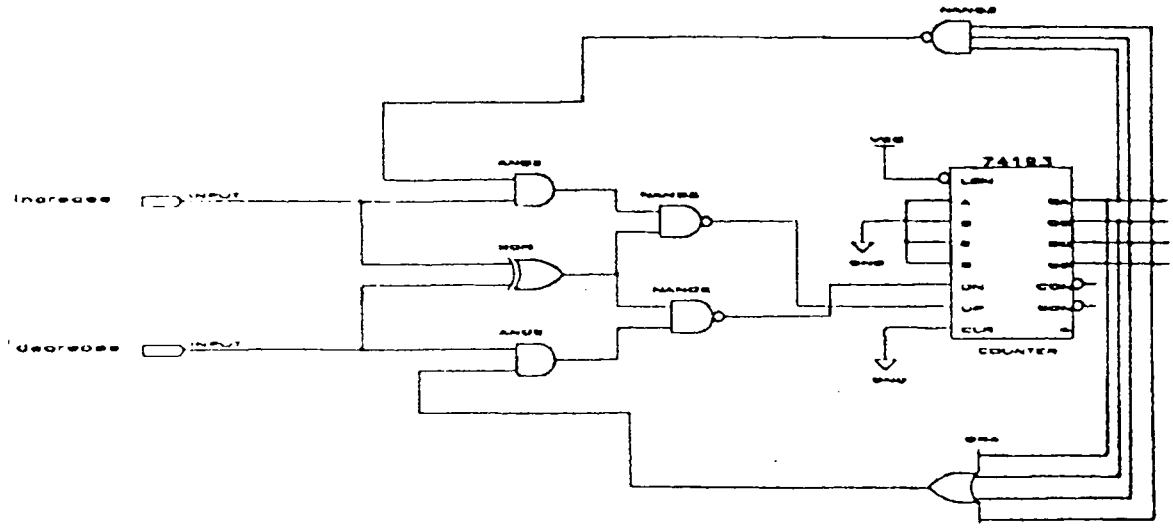


Figure 28 Integration Time Decision Circuitry.

These signals are applied to a multiplexer that selects either this or a manual integration time. The integration times represented by the four-bit nibble are shown in Table 4.

Table 4 Available integration times and their cooresponding control signals

INT03	INT02	INT01	INT00	Intgtion Time	Fr. Rate fr/sec
0	0	0	0	120μsec	60
0	0	0	1	240μsec	60
0	0	1	0	480μsec	60
0	0	1	1	960μsec	60
0	1	0	0	2msec	60
0	1	0	1	4msec	60
0	1	1	0	8msec	60
0	1	1	1	16msec	30
1	0	0	0	25msec	30
1	0	0	1	33msec	30
1	0	1	0	66msec	15
1	0	1	1	122msec	7.5
1	1	X	X	Not Used	----

The automatic exposure control may be defeated and the camera can be operated in the manual mode. Circuitry located on the front panel of the processor box contains a switch that toggles the processor between the automatic and manual modes. Also located on the front panel is an eleven position rotary switch. By rotating the switch to the required integration time position marked on the front panel, dual 8:3 binary encoders (74LS138) and a 74LS157 multiplexer circuitry convert the impressed rotary signal into a four-bit nibble representing optical integration times 0001 to 1011. The twelfth integration time is chosen when none of the eleven positions are grounded. A 12-input AND gate senses that no inputs have been impressed and decodes a 0000 integration time. Shown in Fig 29 is the circuitry for rotary encoding.

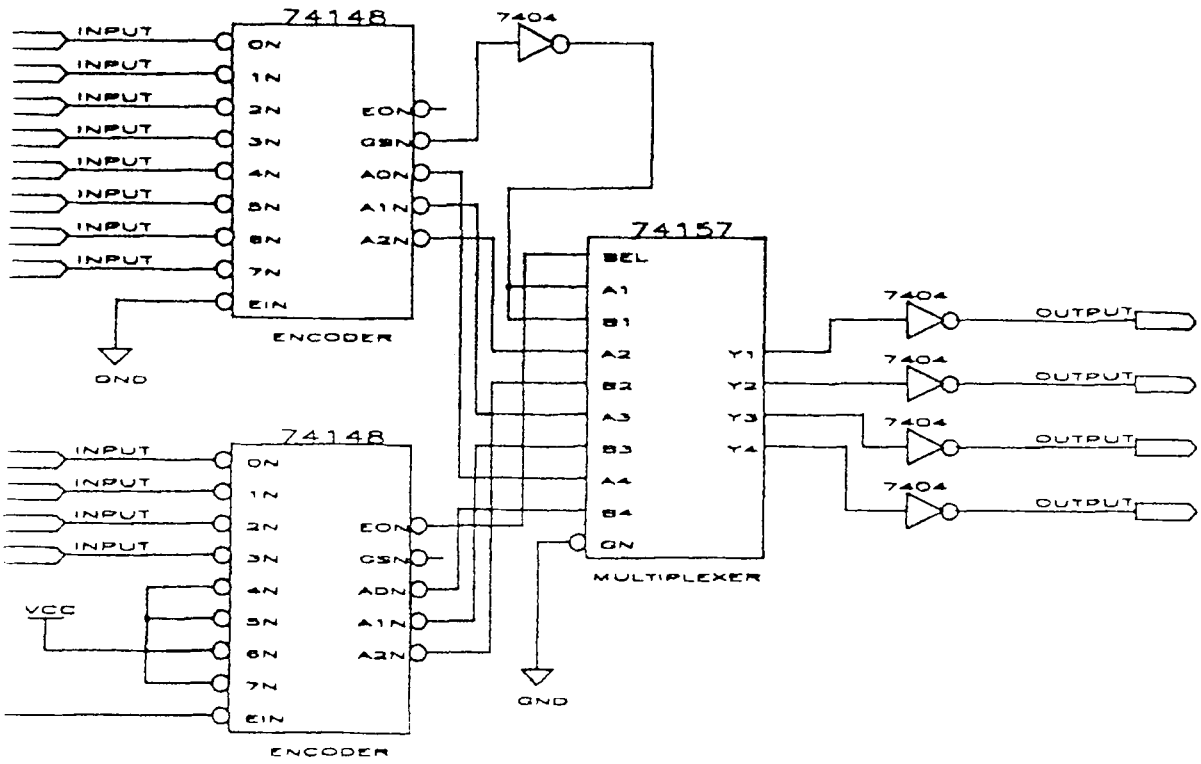


Figure 29 Rotary Encoding Circuitry.

This signal is transmitted to the multifunction board and input to a quadruple 2:1 multiplexer. This integration time is chosen upon proper setting of the Manual/Automatic integration time switch. This integration time is buffered to be sent to three locations. The information is driven differentially to the camera head and the Variable Integration Sequencer board to provide the timing signals to run the CCD chip at these custom rates. In addition, the signals are sent to the Smart Frame circuitry and the display circuitry. The display circuitry decodes the binary signal into seven-segment display signals and drives LED displays representing the integration time located on the processor front panel. The block diagram of the variable integration time is shown on Fig. 30.

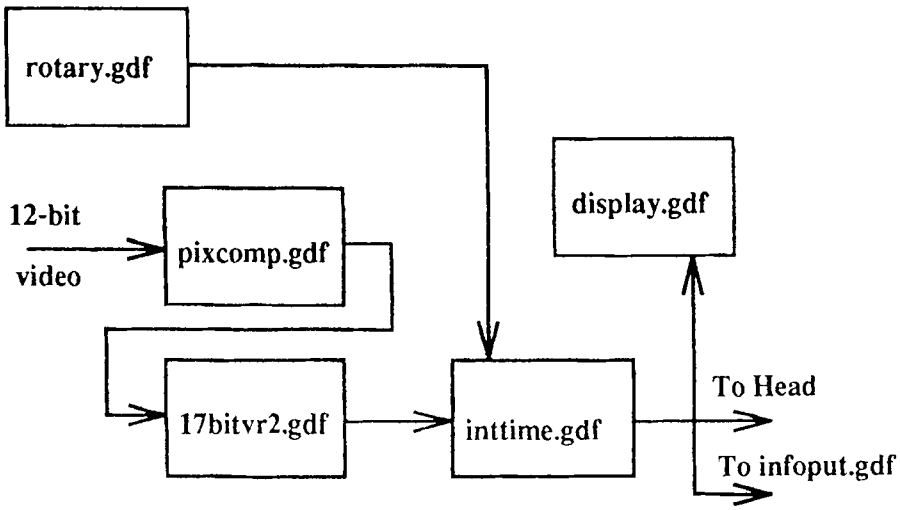


Figure 30 Block Diagram of Variable Integration Time Circuitry.

5.3.3 Frame Count Circuitry

The camera system's primary task is in the acquisition of thermal and emissivity data from semiconductor wafers in processing environments. Therefore the measurement of temperature as a function of process time is critical. The experimental system will also include silicon test wafers with thermocouple gages affixed to them to verify temperature measurements. These thermocouple readings are made by a microcomputer that is equipped with commercial software dedicated to acquiring data from Type J thermocouples. The output of the computer program is in units of absolute temperature. Since this is a dynamic system, there needs to be a common clock to these separate measurements so that the data can be compared reliably. A frame counter was designed to provide an unique address to each video frame acquired during an experiment. An electrical port at the rear of the video processor box provides the START pulse from the semiconductor processing instrument and signals to the camera that the

experiment has been initiated. This clears a sixteen bit counter (4 X 74LS161) and enables counting VA pulses. Since the frequency of VA is at the frame rate, accurate frame counting is established. Knowing the frame rate (from the integration time) for each frame, the cumulative elapsed time can be calculated. The maximum experiment time allowed with unique time stamping follows the following relationship.

Table 5 Maximum time for unique time stamping.

60 frames/sec	**0 hr. 18 min. 03 sec**
30 frames/sec.	**0 hr. 36 min. 07 sec.**
15 frames/sec.	**1 hr. 12 min. 01 sec.**
7.5 frames/sec.	**2 hr. 25 min. 00 sec.**

The output of this circuit is routed to the Smart Frame circuitry and is also ported to the front of the processor box to a DB-25 connector for interface to the IBM-PC AT for input to the thermocouple data acquisition system. Shown in Fig. 31 is the circuitry to perform frame counting.

5.3.4 Smart Frame

With the camera operating at various integration times, the data from this radiometer can only be interpreted if one knows the integration time used to image that particular scene. Circuitry was developed to impress data crucial to properly processing the video data in the video signal. The information

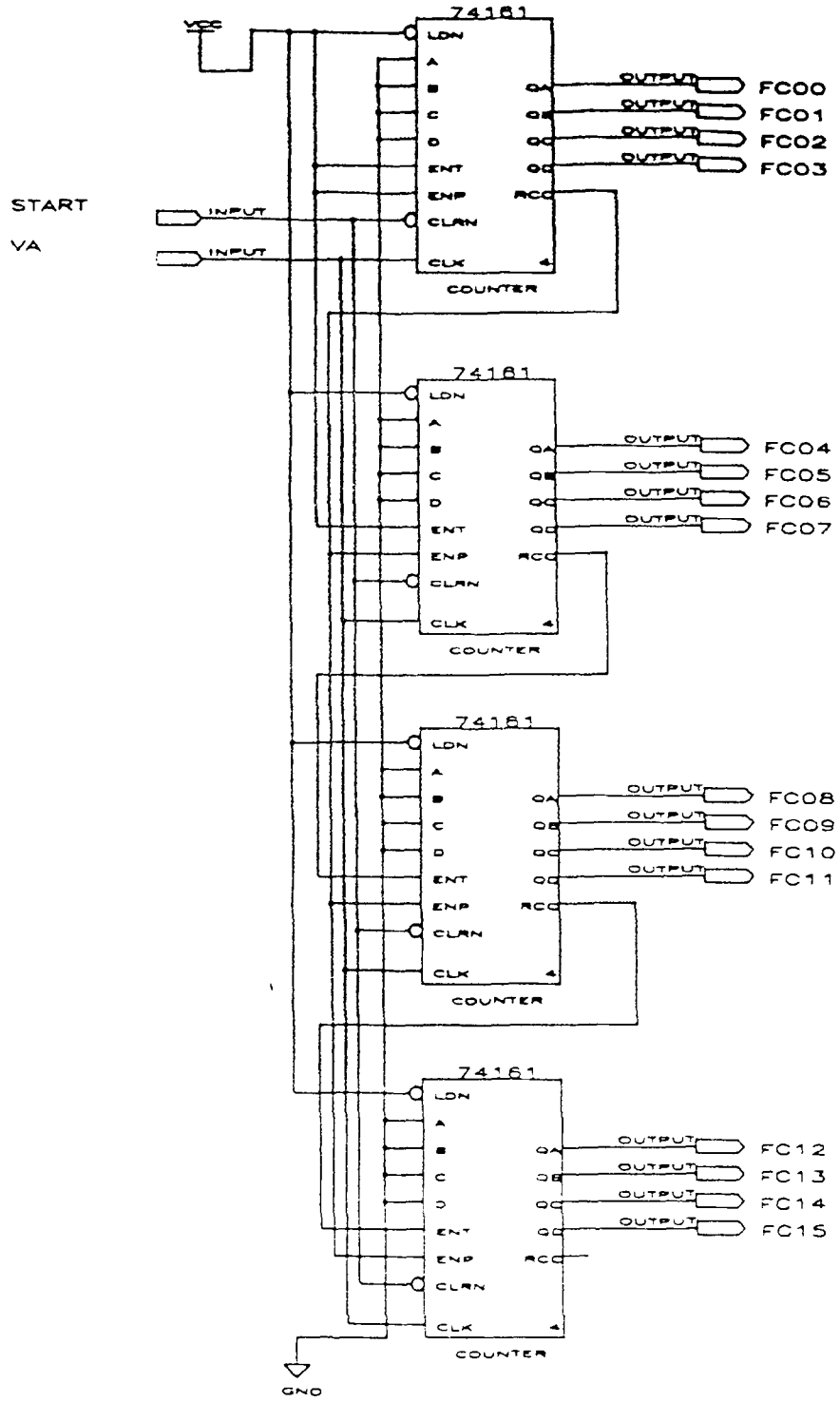


Figure 31 Frame Count Circuitry.

was embedded in one of the first lines of data to easily facilitate Datacube processing. It is easier to retrieve the information during active video than during blanking and the first 10 lines of video have been chosen to be ignored due to residue charge discussed earlier.

The information sent to the Datacube is the optical integration time and the frame count. This represents a total of 20-bits of data. The video data bus is 12-bits wide so the information was coded to fit on the data bus. The information was also repeated 80 times to insure that the radiometric information of the frame could be guaranteed in the event of corrupted pixels in the information line due to noise. This redundancy was synchronized by embedding synchronization bits between the information to facilitate detection. The format for the data is shown in Fig. 32.

The circuit consists of two 74LS161 four-bit binary counters operating in parallel. Counter 1 is clocked at the pixel rate while Counter 2 is clocked at the line rate. When a new frame begins, VA and HA are at logic 1 and this clears both counters. Counter 1 counts as a 2-bit counter and continuously outputs a binary number cycling every fifth pixel during active video. The HA clears the counter to 00 at every pixel # 1. This 2-bit number is transformed to signal lines using a 74LS139 2:4 decoder and the resulting signals represent the four states required to run the sequence of Fig. 27. The signal INT is just the combination (1+2). Counter 2 counts lines beginning from 0000 and is disabled when the count reaches 0010. This corresponds to line three of video. The counter is not enabled again till the next frame. The output of the counter is then only active high for line two of the video frame. This signal (MUXSEL) is latched

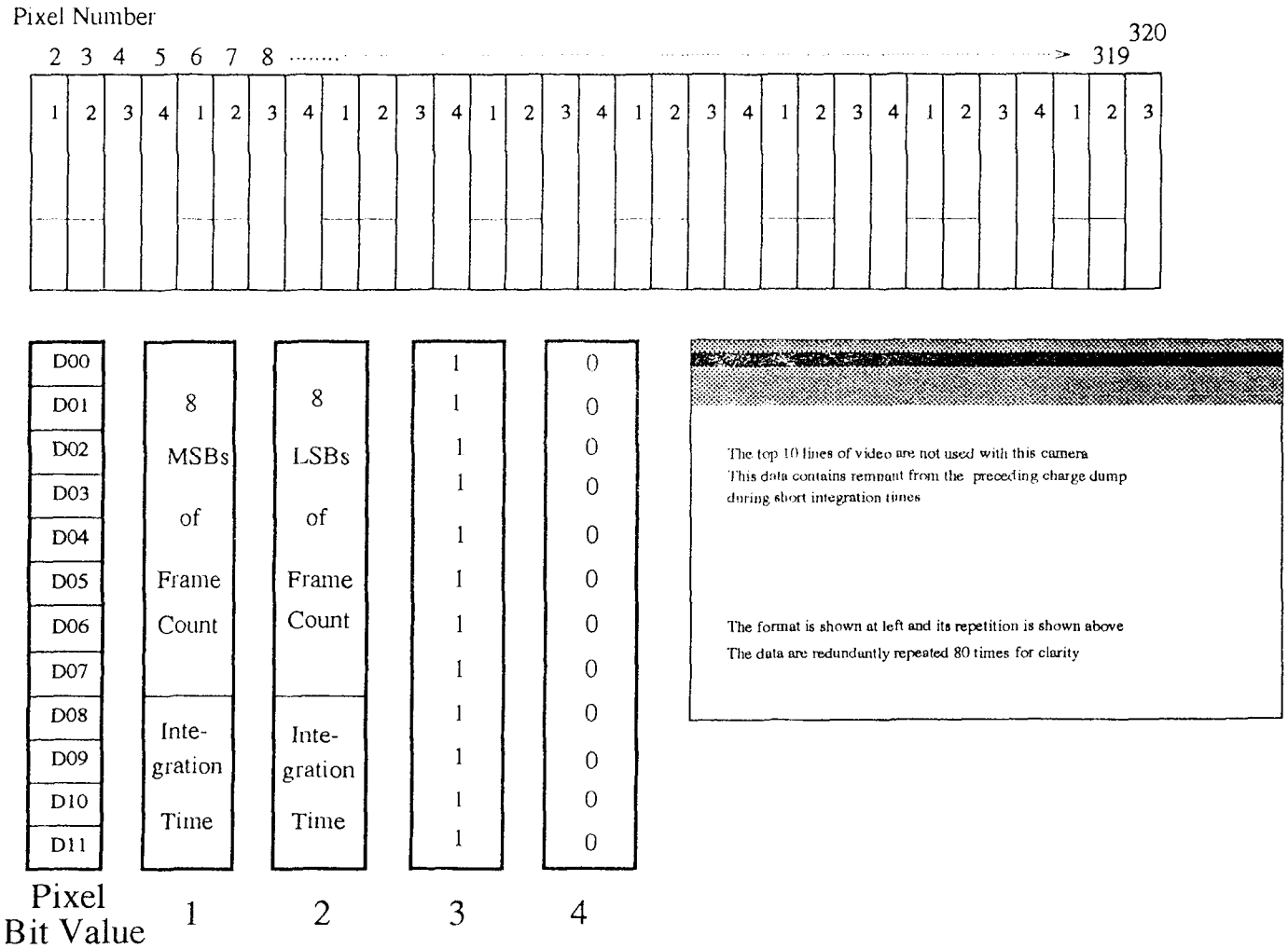


Figure 32 Smart Frame Data Encoding.

with the other control signals in a 74LS273 D-type flip flop on the clock edge. MUXSEL allows the data bus to transmit active video for all lines except line three where it interrupts the bus and inserts the contents of the seven 74LS374 TRI-STATE Octal-Edge Triggered flip flops. The contents of the flip flops are shown in Table 6.

Table 6 Smart Frame data-bus interface.

74LS374 #	Contents	Resp to Signal
1	8 MSB of FC	1
2	8 LSB of FC	2
3	11111111	3
4	00000000	4
5	Int. Time	INT
6	1111XXXX	3
7	0000XXXX	4

The 74LS374s are continually transmitting the data as the pixel counter enables them but the data are stopped by MUXSEL. MUXSEL controls three 74LS399 quad 2-input multiplexers with storage capability. The information from the '374s is put at the "A" inputs with the camera pixel data put at the "B" inputs. The camera data is transparently routed to the next board on the bus except during line three of active video. The data is blocked and the Smart Frame information replaces it. The circuitry for Smart Frame is shown in Fig. 33.

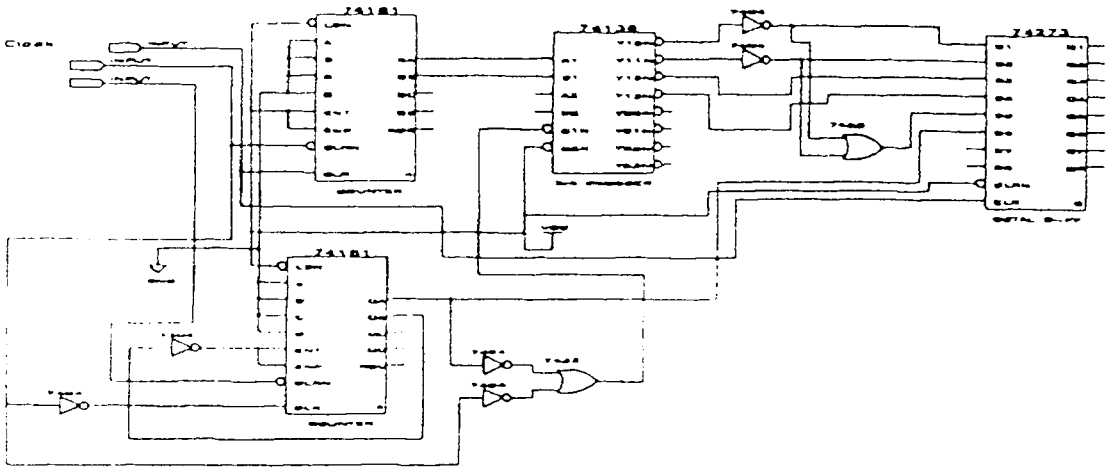


Figure 33 Smart Frame Encoding Circuitry.

5.4 Jumper Board

The back plane of the processor bus is set up as a stream. If a slot is not occupied by a board, the data cannot travel across this empty slot. A jumper board was fabricated to allow for the data to jump across unused slots to reach the output board at slot # 10. Because the board connects in front, jumper board also prevents the accidental insertion of a board into a slot where data cannot reach it.

5.5 The Input/Output Board

The connection of the processor to a Datacube system required that the digital data and sync signals be transmitted differentially for greater noise immunity. An I/O board was designed and fabricated to facilitate this objective. The signals were latched to line up the signals in time and differential drivers (SN74393) were used to transmit the paired signals off the processor bus and to a 78 pin ribbon connector at the rear of the processor. The signals were sent to the custom Datacube interface circuit designed for this application.

CHAPTER 6

6 DATACUBE INTERFACE CIRCUITRY

The design of this interface was necessary to accomplish four major tasks. The camera data needs to be input to a computer system for real-time data manipulation and storage. The data should be stored with full 12-bit resolution. Thirdly, the camera data and control signals should be electrically isolated from the Datacube bus, and finally, there needs to be a redesigned display driver for viewing the post-processed image at the standard size and frame-rate. The Datacube interface is comprised of two boards; the input board and the display board. Both are constructed with Euro-type perf boards to fit into the Datacube card cage. Whenever possible, Datacube designs were incorporated into the circuit plans to better match the signals that the host computer requires. Much of this work was done with collaboration with Dr. Edwin Hou.

6.1 Datacube Input Board

The Datacube input board performs two tasks. It optoelectronically isolates the Datacube machine and the camera system and provides a simple test pattern for Datacube testing and evaluation. Shown in Fig. 34 is the circuit layout of the Input Board. The input to the board consists of a 34-pin ribbon connector carrying the camera signals to 16 (HP2400) optoisolator chips. The optoisolator consists of a photodiode/Darlington phototransistor pair hermetically sealed in a hollow cavity 8-pin dual inline package. The inputs to the optoisolators are impedance matched to both

the bus impedance and the frequency of operation. The resulting data are single ended TTL compatible signals. These signals are latched using 74LS374 Octal D-type flip flops to line them up in time. The output enable to these latches is controlled by a two-position switch mounted on the top of the circuit board. The switch can be enabled to send the camera data to the computer or divert test pattern data which is an exact emulation of the camera signals, to the computer.

The test pattern circuit is an autonomous circuit that requires no inputs. The Datacube can then test algorithms on this test pattern without having the camera connected to the computer. An on-board crystal oscillator provides the CLOCK*2 pulses and clocks the circuit contained in the Altera (EPM5064) PGA. The PGA contains counting circuitry that emulates the camera control signals. The lengths of the active fields and blanking intervals have all been programmed to exactly replicate the camera design, operating in the non-interlaced mode with 320 X 122 pixel resolution at 30 frames/s. The PGA is optically erasable and any frame rate or scanning scheme can be easily implemented for computer simulation of performance by reprogramming the chip. The data programmed in the chip to display a test pattern is shown in Fig. 35. Fig. 35 shows the data positions and the blanking intervals. The data is shown in reverse to what would be seen on a television screen with the black pixels shown white and vice versa. The pixels are set white by bringing the 2 MSBs to logic 1 with black pixel's data bits all logic 0.

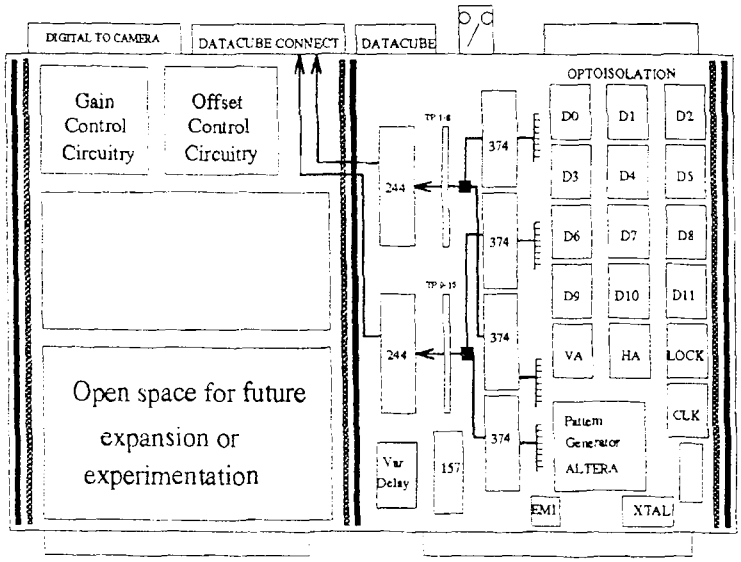


Figure 34 Datacube Input Board Component Layout.

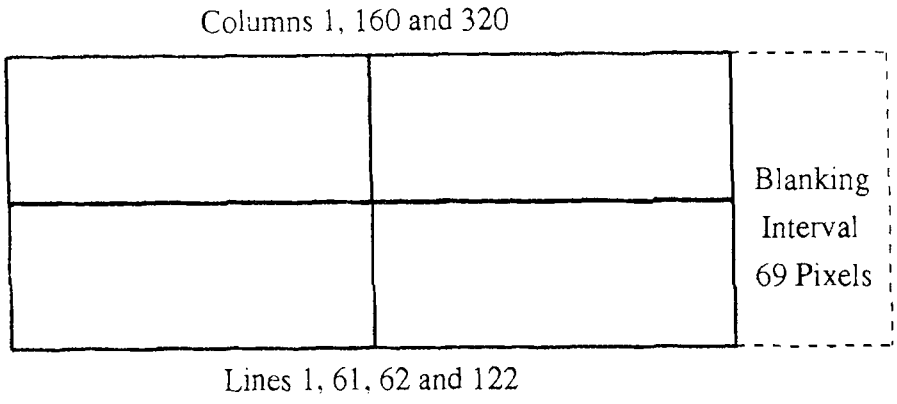


Figure 35 Test Pattern for Datacube Input Board.

The data are latched using 74LS374 flip flops and are output enabled opposite to the camera input flip flops. The outputs to all the 74LS374s are connected to (3) 74LS244 Octal Buffers/Line Drivers. These chips drive the signals to the output connector; a 34-pin connector that is connected to the MAX-SCAN board. Shown in Fig. 36 are waveforms measured from the output connector of the Input board running in the test pattern mode.

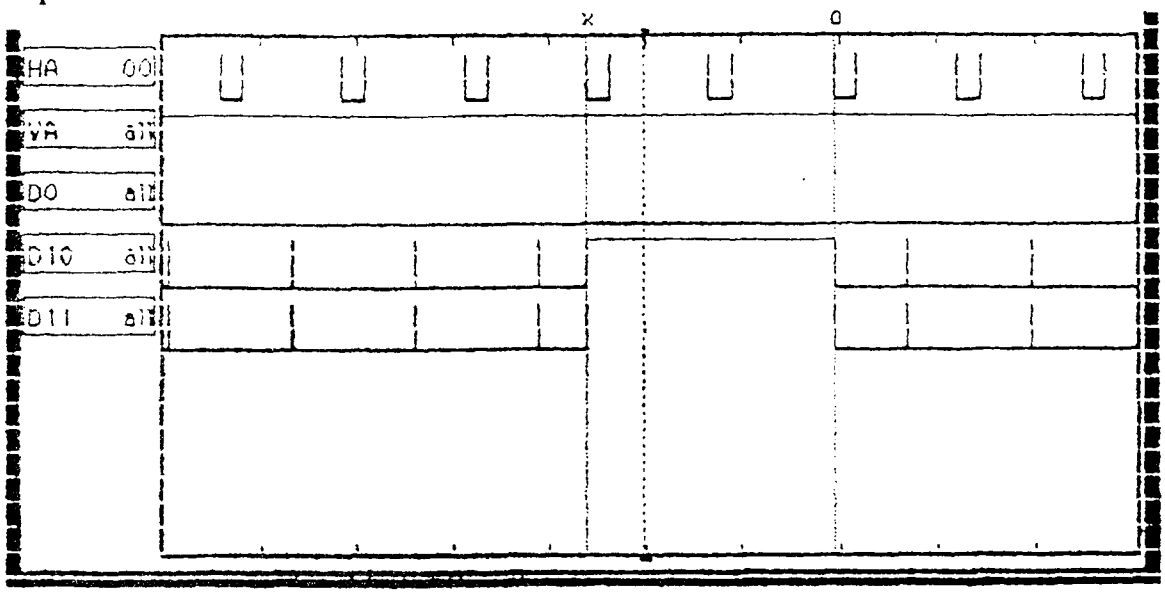


Figure 36 Test Pattern Waveforms (measured).

The MAX-SCAN board is a programmable asynchronous input module to acquire digital input data with a variety of resolutions and frame rates. MAX-SCAN creates a 10 MHz stream of scan sequential digital video data to connect to other Datacube modules. The board contains digital signal processing DSP circuitry to perform look-up table operations, two-point correction and pixel averaging functions. The output of the MAX-SCAN contains a first-in first-out (FIFO) buffer to port the data out at 10

MHZ. This is to facilitate further processing such as MAX-GRAPH functions and ROI-STORE operations. When data at this rate is displayed on a standard 6 MHz NTSC monitor, the data is compressed to the top left hand corner. To properly format this video for display, a second board was designed and fabricated.

6.2 Datacube Display Board

The display board functions as a reformatter for output display video. This video has been processed by the computer and is streaming out at 10 MHz. Furthermore, at long integration times, the frame rate drops below 30 frames/sec and if frames are not stored and re-displayed, the screen will flicker. Normal NTSC video contains 488 lines of active video. With the camera operating with 122 lines of vertical resolution, the display board must do a 4X scan conversion to fill the screen with video.

Shown on Fig. 37 is the circuit layout for the Display Board. The circuit has 4 digital input connectors (P3, P4, P5, and P6) and one analog video output. Connector P3 inputs the Datacube system clocks onto the board from the MAXbus. The pixel clock, the RS-170 horizontal sync and RS-170 vertical sync are all carried on the MAX bus P3 ECL Timing bus. These signals provide robust synchronizations for all data transfers including ROI transfers. The four clocks received are E4DC, four times the dot clock rate, E2DC, two times dot clock, horizontal reset EHR and vertical reset EVR. The timing diagram for these signals is shown in Fig. 38. The receiver circuit consists of a MC10H125 ECL to TTL translator. By clocking the TTL4DC with a delayed version of TTL2DC into a 74F109 JK flip flop, the true non delayed version of the master clock is restored. There are eight switches connected to a network

of resistors that perform transmission line termination if the display board is the last board to receive MAXbus timing signals. The output of the circuitry is a signal called DC or dot clock. This is the master clock for all Datacube operations on the board.

Connector P4 transfers synchronization signals designed to handle ROI transfers. ROIs are arbitrarily-sized rectangular areas of an image. They are sub-areas of the RS-170 image. The P4 connector is a 14-pin flat cable with 8 TTL signals. Each of the four pairs of signals are separate vertical and horizontal sync signals. Hsync is an active low signal which is active for only one pixel time. Vsync is also an active low signal which is low for between one pixel and two line times. Shown in Fig. 39 are the sync signals and their relationship to the active video data.

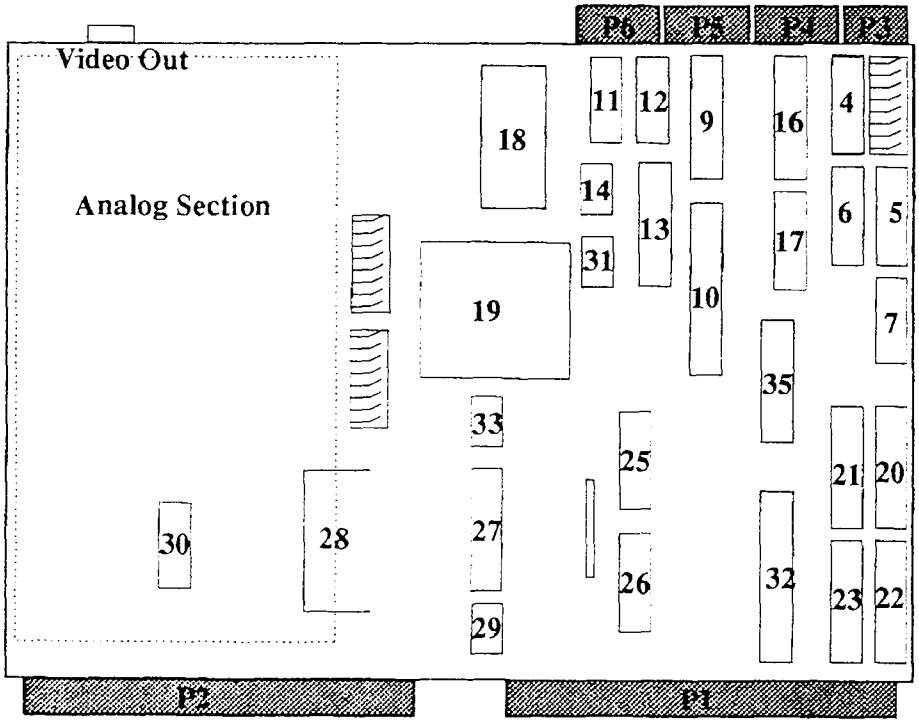


Figure 37 Datacube Display Board Circuitry.

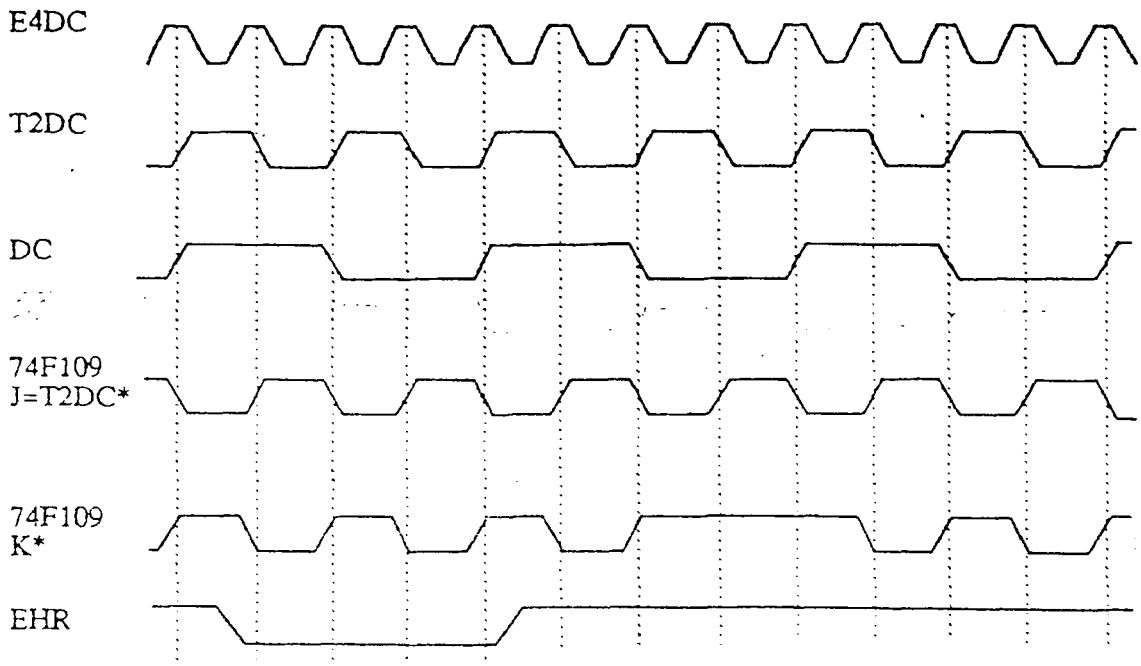


Figure 38 Datacube P3 ECL System Clock Signals.

The signals from P4 are latched onto the board and lined up with DC. A 74LS153 Dual 4:1 Multiplexer chooses one pair of sync signals from the four. Selection is made by a pair of on-board jumpers that supply a 2-bit address. The outputs from this circuitry are HSYNC and VSYNC, the board ROI sync signals.

Connector P5 supplies the Display Board with 8-bit processed data for display. The data are the top 8-bits from the 16-bit data bus. The data port is connected to the output FIFO from the MAX-SCAN board but the data has been processed through the entire Datacube system. Because

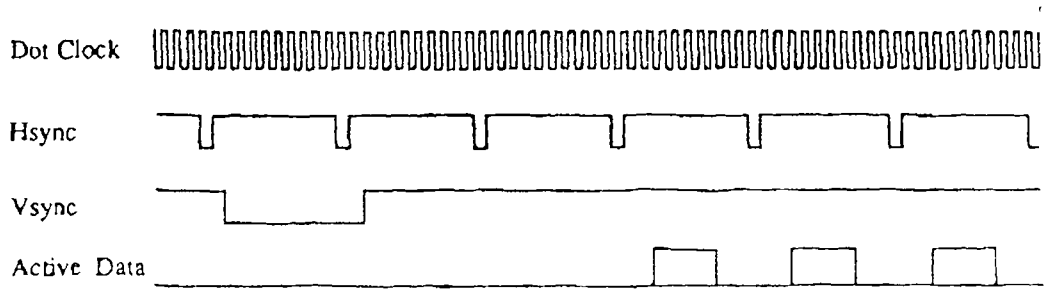


Figure 39 Datacube P4 ROI Synchronization Signals (Even Field)

the P3 and P4 connectors have been used, data input to the Display Board can be either RS-170 or ROI blocks. The data are read in at the Datacube rate of 10 MHz and latched with a 74LS374 with DC. The data are then input to a Cypress CY7C441 Clocked 512 X 9 FIFO. The transfers in and out of the FIFO are asynchronous and the FIFO is clocked out at the NTSC rate of 6 MHz which is supplied from either the camera head or the Input Board (when the test pattern is enabled). Enable pulses for both input and output are generated on-board. The NTSC data are then latched at the camera clock rate with a 74LS273.

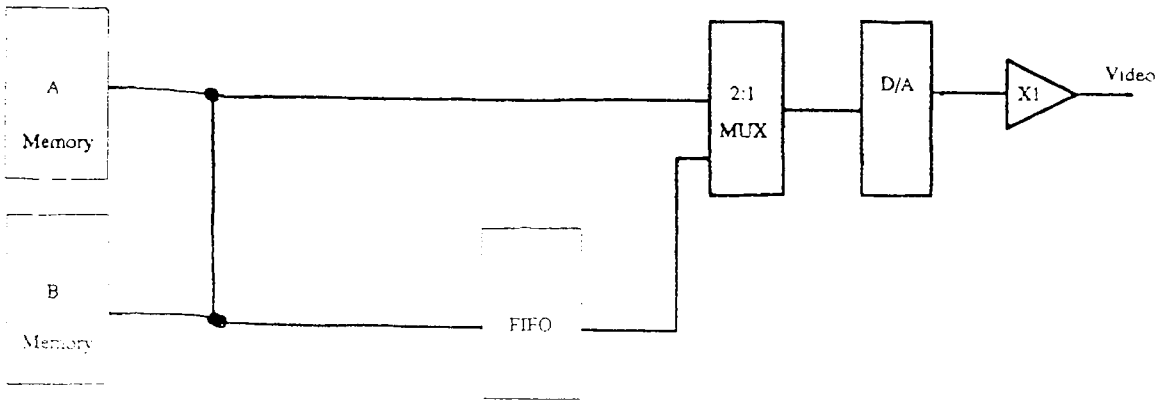


Figure 40 Ping-Pong Memory Operation.

The data are input to Hitachi HM53051P 262,144 word X 4-bit frame memory chips. These chips offer high speed cycling times of 60ns and input and output data are independently controlled and synchronized to the system clock. The data are separated into A and B "fields" to perform scan conversion. Alternate frames are toggled between separate frame memories and stored. This ping-pong operation is shown in Fig. 40. These two memories work in tandem with an output FIFO to operate a 4X scan conversion. The procedure is illustrated in Fig. 41. If no scan conversion were performed, the screen would appear as Fig 41a. By repeating each line four times interlaced between A and B frames, the screen will be filled with information and will appear brighter and clearer. This is illustrated in Fig. 41b. The signals required to perform this operation are shown in Fig. 42.

The MUXSEL signal toggles between the FIFO and the memory contents while AOEB and BOEB toggle between memory A and

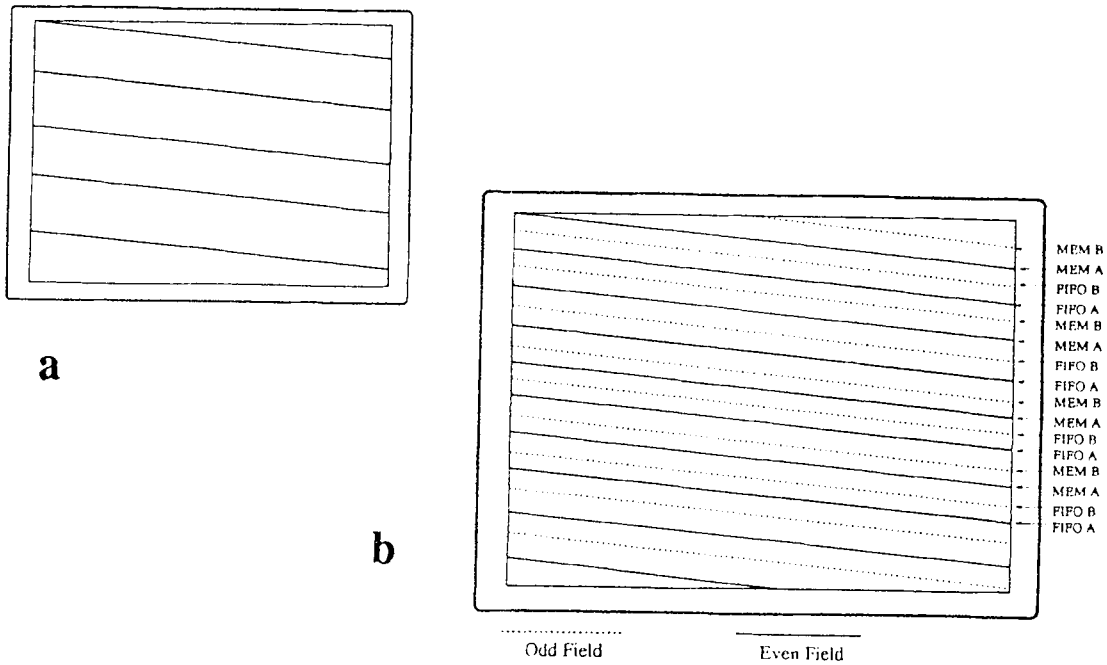


Figure 41 4X Scan Conversion

a) no conversion b) Full screen resolution

memory B. When data is read from memory A, it is written to memory B. If data are arriving at a rate slower than 30 frames/sec, the memory contents are repeated until new data appear. This eliminates any flicker.

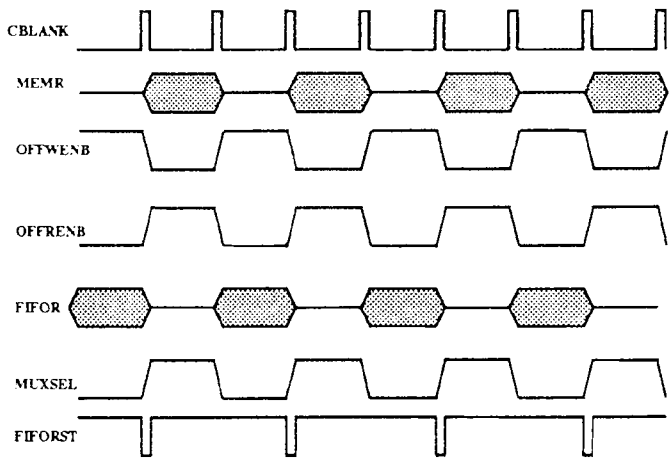


Figure 42 Waveforms to perform scan conversion.

The 8-bits of data are latched with an RS-170 generated clock before being input to the Brooktree Bt106 8-bit video digital to analog converter (DAC). This chip is specifically designed for high resolution color graphics. The input controls are sync, blank, and reference white. These signals are available from RS-170 control data. The linearity error of this device is ±1 LSB. The output analog signal is matched to a 75Ω load. The circuit requires a reference potential of 1.2 V. This is provided by an LM385 adjustable voltage reference. The chip is situated with its digital side over the digital ground plane and its analog side over the analog ground plane for noise immunity. Separate voltage regulators provide analog power and the analog section of the board is completely isolated from any digital signals. The analog signal is buffered and driven with an LH002 buffer amplifier and the signal is transmitted to the top of the board via coaxial cable to an SMA connector. This connector may directly drive the NTSC display monitor.

The camera operates with a variety of frame rates so a separate RS-170 sync generator is required on the Display Board to drive the 30 frame/sec monitor. Connector P6 is connected to the Input Board and provides timing signals from the camera or Input Board (if the test pattern is enabled). The LOCK pulse is generated at 30 frames/sec regardless of the frame rate of the camera. This signal is input with the camera's system clock to an Altera EPS464 Sync generator. The sync generator drives the output DAC and memory to output data at the standard RS-170 format. VA is input at P6 to tell the board when new information is arriving. Many of the memory and FIFO control signals are generated from a XYLINX (XC3064PC84) FPGA. This chip is

programmed at power-up by a XYLINX (XC1764) PROM. The XC3064 receives inputs from sync signals, clocks, and delays to derive the correct control pulses to drive the input and output devices.

CHAPTER 7

CONCLUSIONS

A camera system was designed and built to perform as a spectral radiometer over the 3 to 5 μm infrared band capable of imaging temperatures between 50 and 1000°C by employing variable optical integration time. A dump and read procedure for sub-frame integration was developed for this project and circuitry was developed to facilitate this procedure.

The camera was fabricated and tested. The mini dewar and the associated electronics provided infrared images to be used for radiometric measurements.

Analog to digital conversion circuitry was built and tested. Circuitry was developed to automatically select the optimal integration time based on the previous frame image. This decision circuitry was comprehensively tested. The circutry to count frames and embed the integration time and the frame count into the video signal were designed, built and tested. Output circuitry was designed to transmit the digital data to a computer and was tested.

The optoelectronically isolated interface between the camera and the Datacube processor was designed built and tested. The on-board test pattern facilitated the development of video processing software. A test pattern designed for use in the processor provided camera data to the computer which was stored and transmitted digitally to a host computer. The Datacube display board was designed built and tested and provided

for the display of nonstandard video rates without flicker and at full resolution.

The camera will continue to be tested to calibrate the unit for thermographic measurements. Linearity, spectral and spatial uniformity and temporal stability tests will be performed. Spectral bandpass filters will be placed in the dewar chamber to decompose the signal in the frequency domain to perform MWIP.

Research will be performed to examine the feasibility of using acousto-optic tunable filters (AOTFs) to perform the spectral decomposition. These filters have the advantage of providing full screen resolution at a small spectral band of radiation and then the ability of randomly selecting another bandpass for examination. The switching of frequencies can be accomplished in approximately 200 μs allowing for switching during the transfer of charge to the CCD channels. This provides for full resolution MWIP imaging without lost frames.

APPENDIX

A1 THE OPTICAL SYSTEM

The camera and the object being imaged remain mechanically stable throughout the silicon processing experiments. Therefore precise optical measurements may be taken to both facilitate radiometric calculations and maximize the imaging performance. Optical design in the planning stages of both camera development and experimental setup realize these goals.

A1.1 The Optical Setup

The optical system for imaging semiconductors in RTP environments is subject to the following requirements.

Dimensions	
Wafer Diameter:	1-6"
Imager Shortest Dimension	0.936 cm
Minimum Detector/Wafer Distance	50 cm
Minimum Criterion to Satisfy Eq. (9)	
1" Wafer	51 cm
6" Wafer	305 cm
Transmission Losses	
Reactor Window	Quartz
Exit Window	Sapphire
Mirror	Gold
Lens System	Silicon
Dewar Window	Silicon
Absorbing Molecules	CO_2, H_2O

A1.2 Simple Lens Systems

The imaging of an object onto a FPA can be accomplished using a simple convex lens. By mounting the lens into a mechanism that can vary the image to lens distance, imaging can be realized for a range of working distances and object sizes. The basic equation describing the relationship between the image and working distances and the lens focal distance is shown as

$$\frac{1}{p}+\frac{1}{q}=\frac{1}{f} \tag{23}$$

where: p is the working (object to lens) distance
q is the image (image to lens) distance
f is the focal length of the lens.

The focal length is an inflexible term derived from material and geometric variables.

$$f=\frac{R_1R_2}{(n-1)\left[(R_2-R_1)+\left(\frac{n-1}{n}\right)t\right]} \tag{24}$$

where R_1, R_2 are the radii of curvature for the aspheric surfaces
n is the refractive index of the material (n= 3.4 for Si)
t is the lens thickness.

Fig. 43 shows the relationship between image and working distance for two popular focal lengths. It shows clearly that the larger focal length requires a larger range of image distance required to focus the same working distances as the shorter focal length. It's advantage is that images

can be focused more precisely with the larger focal length, but means that your lens length must be longer.

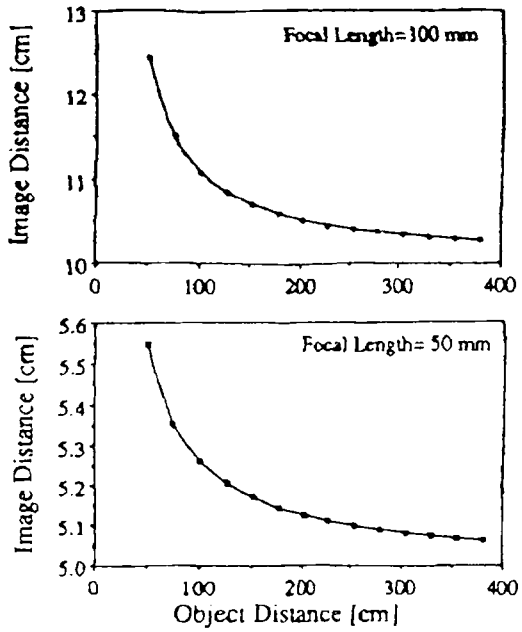


Figure 43 Relationship between image and working distances for two focal lengths.

Two dimensional ray-tracing is the easiest way to visualize the method of image formation. Ray-tracing is shown schematically in Fig. 44. Three rays map the object onto the image line. Ray 1 begins at the top of the object and proceeds straight to the center of the lens where it is deflected to pass through the optical axis at the focal length. It continues traveling straight until it encounters the image line. Ray 2 propagates from the top of the object through the optical axis at the negative focal length and to the center of the lens. The lens deflects the beam to travel straight and the ray propagates to the image line. Ray 3 (called the Chief Ray) propagates straight from the top of the object at an angle to intersect with the other two rays at the image line. The angle

which the Chief Ray makes with the optical axis is called the Field of View (FOV).

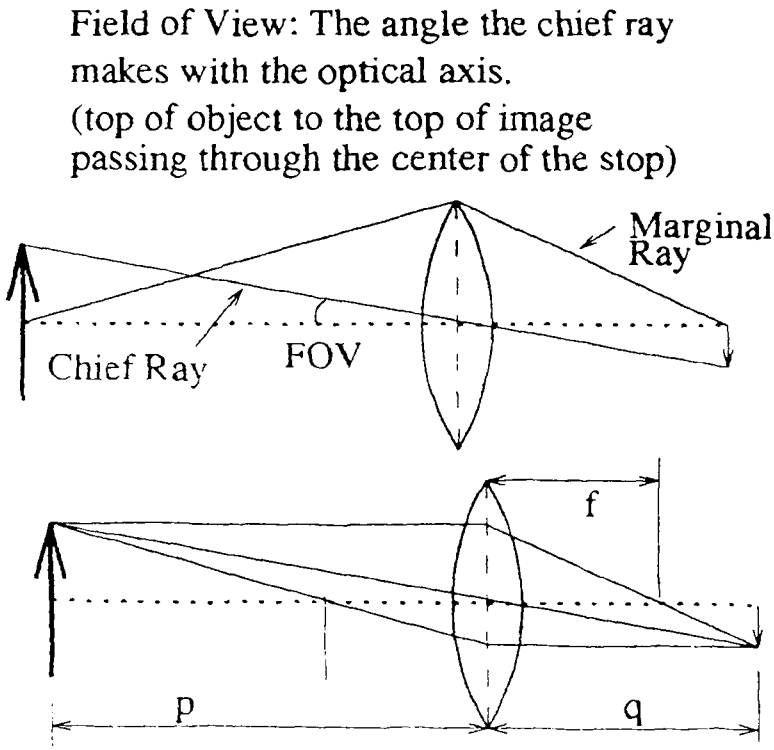


Figure 44 a) Field of View and b) Image formation by ray-tracing.

It can be seen from Fig. 44 that the image size does not have to be the same size as the object. The relationship between the two sizes is described mathematically by the magnification (M).

$$M = \frac{image\,size}{object\,size} = \frac{-q}{p} = \frac{-image\,distance}{working\,distance} \qquad (25)$$

The magnification required to image a 4-inch wafer can be shown schematically in the scale drawing of Fig. 45. The four-inch object is shown next to a representation of the largest full image of the object possible. The image occupies a length of (234 X 40 μm) to accommodate

the 10 top lines disregarded. The largest full circular image dimension that this camera can measure is then d=0.936 cm.

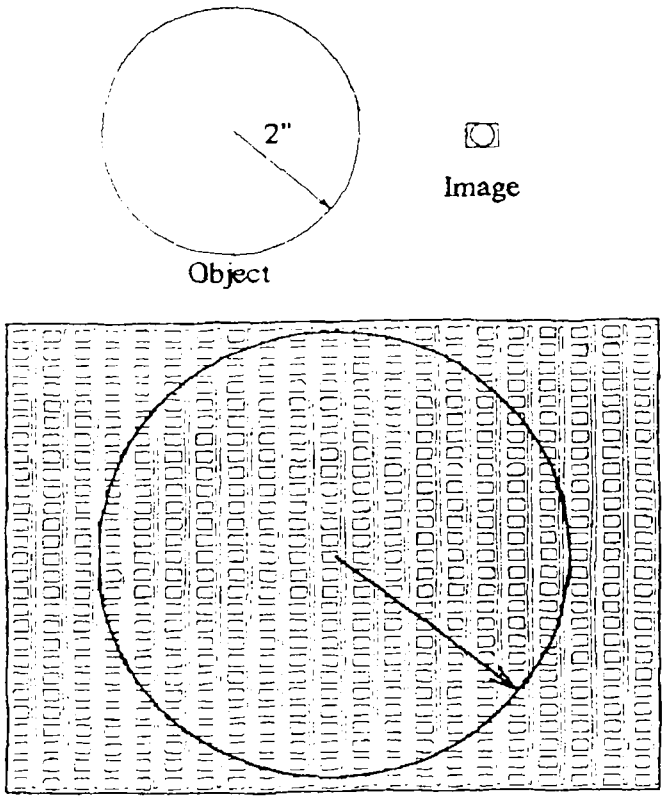


Figure 45 Scale drawing of the magnification of the wafer image.

Equations (18) and (19) can be combined to determine the image or working distance required to image at a certain magnification.

$$p = f\left(1 + \frac{1}{M}\right) \qquad (26, 27)$$
$$q = f(1 + M)$$

Knowing the maximum magnification for each size wafer, the working distance required to obtain the maximum full image size is shown in Fig. 46. The plot shows that to image one-inch wafers with a focal length of 100 mm, the working distance should be 37 cm. This requires that the lens

be placed 14 cm from the image plane. If these requirements cannot be met, a longer focal length lens is necessary.

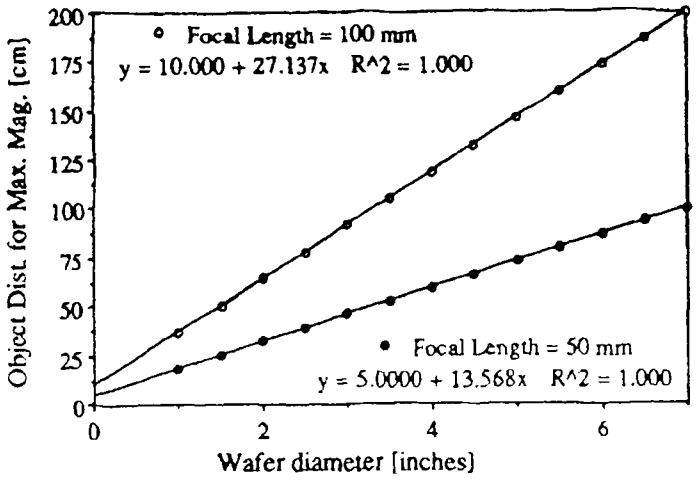


Figure 46 The Working distance required to obtain maximum full image vs. wafer size for two focal lengths.

A1.3 Optical Limitations

To determine whether a single lens element is suitable for this application, it is necessary to determine the aberrations of the lens. There are many types of aberrations and each contributes a certain blur which is superimposed onto each other. The reduction in size of the blur spot is critical to eliminate cross talk and to contain the optical energy into the smallest space.

The largest design related aberration is the spherical aberration. This is due to the deviation of the wavefront from pure spherical convergence. It arises as a result of the lens design and can never be eliminated. Reducing the aperture improves the performance. Spherical aberration follows the following relationship.

$$\beta = \frac{k}{(f/\#)^3} \tag{28}$$

where β denotes the conical angle the blur will make. Multiplying it by the image length will yield the blur spot size.

Chromatic aberration occurs due to the fact that a single material's index of refraction varies with optical wavelength. It follows that the focal length for 1 μm energy will be different from 5 μm energy. The relationship follows

$$\beta = \frac{1}{2V(f/\#)} \cdots V = \frac{n-1}{\Delta n / \Delta \lambda} \tag{29}$$

Coma is an aberration that arises due to the deviation from optical design during manufacture of the lens. Coma is a measure of the variation in the magnification with aperture. It is described by the relation

$$\beta = \frac{\pi}{16(n+2)(f/\#)^2} \tag{30}$$

Astigmatism is the variation in the focal length between the saggital and tangential optical planes. This measurement is made at best focus.

$$\beta = \frac{\pi^2}{2(f/\#)} \tag{31}$$

Defocus is the measure of the increase in the image size as the object is brought out of focus by a small amount. When imaging a three-dimensional object, the defocus is a measure of how well parts of the image above and below the focal palne are resolved. This is refered to as

the depth of field. The wafers imaged in this application can be considered flat for our optical system but the equations are given for completeness.

$$d_{defocus} = \frac{\delta}{f/\#} \tag{32}$$

where δ is the depth of field.

When imaging in the relatively long wavelengths of MWIR, diffraction effects become noticeable. Diffraction is a wave-like phenomenon that occurs when a wave encounters an obstacle who's dimension is comparable to the wavelength of the incident energy. The optical beam can be thought of as a Gaussian beam. This beam has a central maximum with concentric smaller maximum around it. It has been determined that 84% of the energy can be found in the first light spot of the beam. Diffraction follows the following relationship.

$$d_{diff} = 2.44 \cdot \lambda \cdot (f/\#) \tag{33}$$

with the dimension of d_{diff} in microns.

These effects are superimposed onto eachother and the total blur spot can be calculated for a simple lens system as a function of its optical number (f/#). Shown in Fig. 47 is the blur spot size in microns as a function of optical number. The sperical aberration is the predominat effect at low f/#s while diffraction effects dominate the blur spot at higher f/#s. The blur spot should be maintained below the pixel size of 40 μm, so the lens system should be chosen between 1.3-4.0 [f/#].

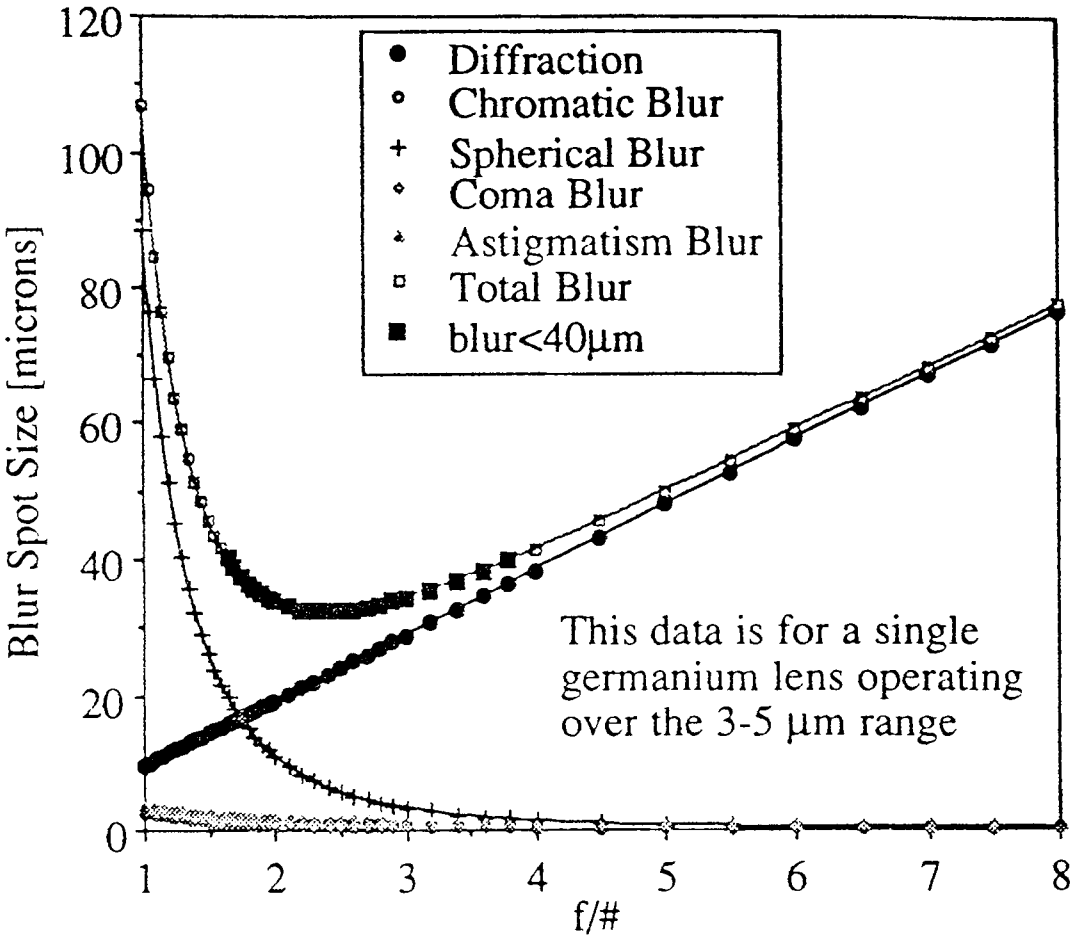


Figure 47 Optical Aberrations vs. f/#.

A1.4 Cold Shield Design

The cold shield reduces the amount of stray radiation from reaching the detector. The radiation can come from objects out of the field of view or from reflections from the side walls or even returned from the imager chip. The side walls of the dewar are in contact with the atmosphere (298 K) and would easily flood the imager with emitted photons. A baffle was designed to attach to the cold finger of the dewar to provide an out of field view of around (80 K). The geometry of the baffle was determined by a program developed at the DSRC with optical inputs provided by the user. A scale drawing of the baffle assembly with a ray tracing is shown in Fig. 48. Reflected light is trapped in the concentric compartments that surround the device.

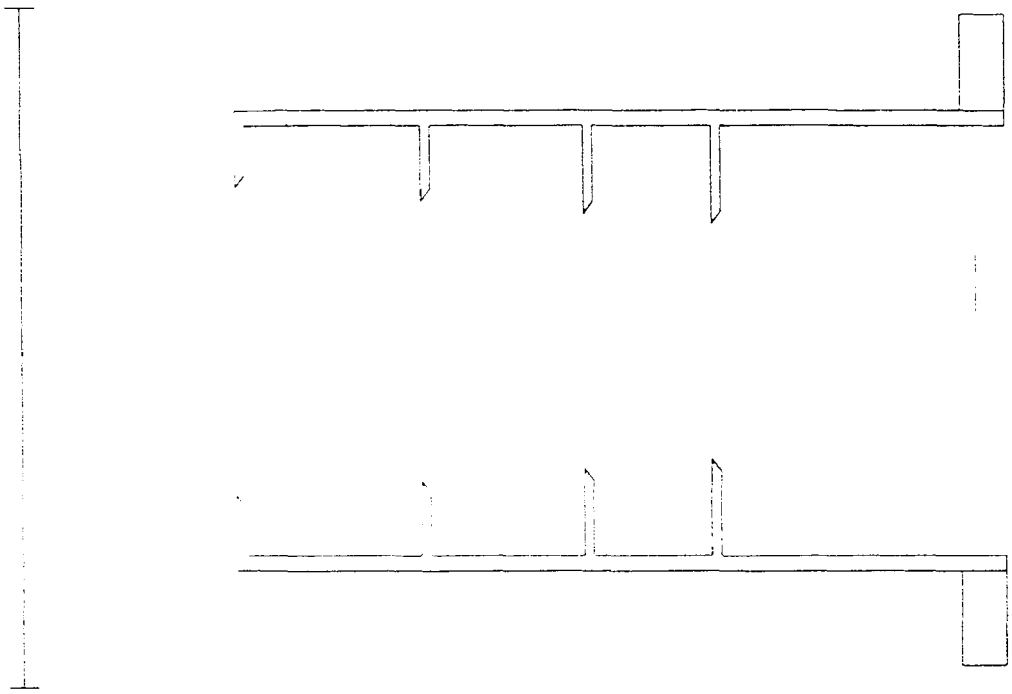


Figure 48 The baffle design with ray-tracing.

A1.5 The Experimental Setup

The geometry and dimensions for the RTP reactor application are shown in Fig. 49. There are five scattering elements, nine reflecting surfaces and three atmospheres involved in the complete optical system.

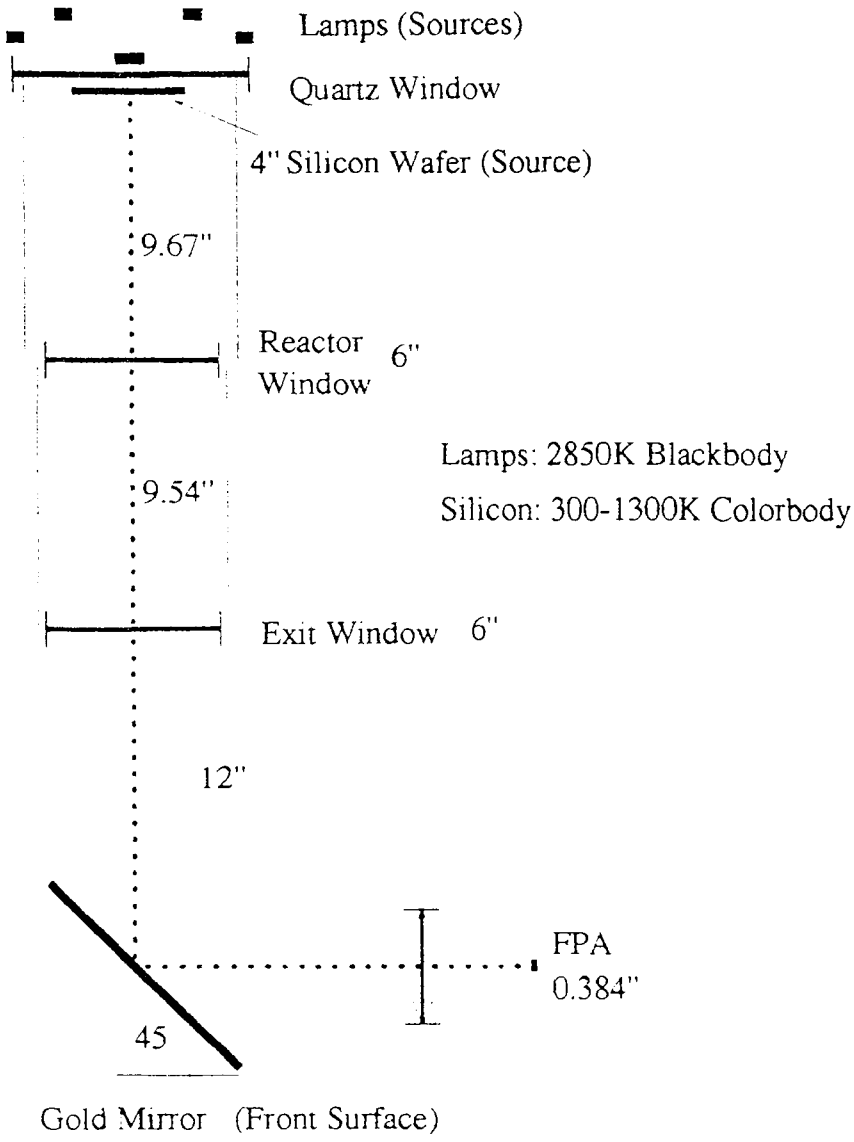


Figure 49 The RTP Optical System.

Radiometric evaluation requires that each element should be modeled and all transmission losses be accounted. In complex systems involving optics, a matrix system known as the ABCD matrix is used to facilitate complex measurements. Each element is assigned a matrix element representing its current ray position and slope and its exit ray position and slope. Space translations are also assigned a matrix. This is equivalent to electrical two-port calculations. The matrix elements can be operated on in series and a "black box" type solution can be determined for the system. The source can then be modeled and a Gaussian beam solution can be obtained. For example, a lens is represented as a matrix

$$\begin{bmatrix} y' \\ m' \end{bmatrix} = \begin{bmatrix} 1 & d \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} 1 & 0 \\ \frac{-1}{f} & 1 \end{bmatrix} \cdot \begin{bmatrix} y \\ m \end{bmatrix} \qquad (34)$$

where d is the distance traveled before reaching the lens. A light ray encountering a dielectric interface, i.e. a reactor window, would be transformed using the matrix

$$\begin{bmatrix} 1 & 0 \\ 0 & \frac{n_1}{n_2} \end{bmatrix} \qquad (35)$$

where n_2 is the index of the exiting material. To find the total effect of all optical elements, the ABCD matrix becomes,

$$\begin{bmatrix} A_T & B_T \\ C_T & D_t \end{bmatrix} = \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix} \cdot \begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix} \cdots \begin{bmatrix} A_n & B_n \\ C_n & D_n \end{bmatrix} \qquad (36)$$

The use of a plane mirror requires the introduction of a different type of matrix. The plane mirror couples the direction cosines of incoming and outgoing rays. For the gold mirror used in this application, the mirror can be more simply modeled as a thin scatterer/absorber. The model should consider the beam travelling in a straight line through the mirror. The analysis are carried out for each wavelength over the operating bandwidth.

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