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ABSTRACT

Microwave GaAs MESFET Nonlinearity and Large-Signal Modeling

by
Yan He

The nonlinearity analysis for a 0.5μm gate length microwave GaAs metal-semiconductor field-effect transistor (MESFET) by HP85150B Microwave Design System was investigated. The analysis starts with the construction of a large-signal MESFET equivalent circuit model. This model consists of bias dependent elements that were extracted by the optimization of DC and small-signal S-parameter measurement data. The details on this construction procedure are included in this work. The MESFET third-order intermodulation distortion was then simulated by HP85150B Microwave Design System. Reasonable agreement was obtained between simulation and measurement results. Microwave GaAs MESFET nonlinearity principles and large-signal modeling technique review are also presented. Finally, the basis for a physics-based large-signal analytical model is outlined to the interests of a transistor or MMIC design engineer who is concerned in the microwave performance as function of device design parameters such as gate length and channel doping.

Microwave GaAs MESFET
Nonlinearity and Large-Signal Modeling

by
Yan He

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Submitted to the Faculty of
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Chapter 1

INTRODUCTION

Linear amplification has been an important and vital aspect in various analog microwave applications. The spurious emission level should be expected to be very small for a high performance receiver/amplifier system which enables the successful processing of input signals. A microwave amplifier comprises of passive (e.g. resistors, capacitors and inductors) and active devices (e.g. diodes, transistors). The presence of active components causes the response to be nonlinear since the terminal current is a complicated function of the terminal voltage.

Microwave monolithic integrated circuit (MMIC) is one of the rapidly developing circuit technologies at microwave frequencies. The passive and active devices in MMICs are integrated on a semiconductor substrate such as GaAs wafer. Optical or electron beam lithography enables micron or submicron structures in the MMICs. The small parasitic effects due to the small volume along with the high electron mobility in GaAs material makes the GaAs MMIC very attractive for high speed and wide-band applications.

GaAs-based metal-semiconductor field-effect transistor (MESFET) is the key component in GaAs MMICs. Its cut-off frequency can be as high as 25 GHz. The GaAs MESFET linearity design is thus an important issue in the development of linear amplification MMICs. While other compensation techniques such as feedback self-adjusting, feed forward and cubic predistortion can be applied to improve the MMIC linearity, a highly linear MESFET is still essential. The MESFET linearity design involves transistor physics, intermodulation measurements and computer simulations based on a

large-signal model. Although many contributions have been made to this aspect, the importance of this subject motivates this research to establish a procedure for the MESFET nonlinearity analysis and design in a practical application environment.

HP 85150B Microwave Design System (MDS) developed by Hewlett-Packard is a powerful CAD tool suitable for linear and nonlinear circuit simulations. The basic power transfer characteristics P_o~P_i of the MESFET can be determined by this software. The important microwave nonlinear parameters such as 1-dB compression point power P_{1dB} and third-order intercept point power TOI are then obtained from this transfer characteristics.

An important aspect of GaAs MESFET nonlinearity analysis is the availability of a large-signal model. Several approaches have been applied to establish a large-signal model for a MESFET:

1. A large-signal model whose topology is the same as a small-signal one. The nonlinear behavior is represented by about four bias-dependent circuit elements. The bias-dependent functions can be obtained by curve fitting techniques as described by Willing [1] and Rauscher [2] in 1978 and 1979, respectively;

2. Curtice model [3] in which gate-source and drain-gate current sources are included. The gate capacitance C_{gs} and drain current source I_d are represented by pre-defined empirical equations. The parameters in the equations are also obtained by curve fitting techniques;

3. A physics-based large-signal model that is derived from the basic charge transport equations in the MESFET channel. No simplified assumption is made to the large-signal characteristics, and it is quite an accurate large-signal model ever since [4-7]. The basis of this model is given in Appendix.

In this work, the nonlinearity analysis and design for a 0.5μm gate length ion-implanted GaAs MESFET by HP85150B MDS was investigated. A Willing type large-signal equivalent circuit model [1] was constructed upon small-signal S-parameter measurements and DC-measurements along with the application of modified Curtice empirical equations. The intermodulation characteristics of the MESFET were obtained by HP85150B MDS. The results were compared with actual intermodulation measurements made at Anadigics Inc. The basic nonlinear principle, details on the equivalent circuit extraction procedure, nonlinearity simulation results, and future work directions on physics-based model are presented.

Chapter 2

NONLINEARITY BASIS OF A GaAs MESFET

2.1 Nonlinear Behavior of an Amplifier

As a signal (fundamental) is applied to the input of a ideally linear amplifier, the output power should have varied linearly with the input signal as long as the input signal is above the minimum detectable level (limited by the noise figure). Since the DC power supply can not be infinitely large, however, the output power tends to saturate at a certain input power level as shown in Fig.2.1(a). If nonlinear active devices are included in the amplifier, the saturation will occur at even smaller input power levels. This saturation effect results in a nonlinear behavior which leads to the creation of the high-order harmonics (or spurious emissions) as shown in Fig.2.1(b).

The linear variation region in this power transfer characteristics is referred as the dynamic range. The lower-limit of the dynamic range depends upon the amplifier's noise figure F_n. The upper-limit of the dynamic range is characterized by 1-dB compression point output power, P_{1dB}, at which the output power was compressed by 1-dB below the extrapolated linear output power curve (or the power gain dropped by 1-dB below the one in a linear region). P_{1dB} is one of the most important parameters which characterizes the microwave linear amplifying device. It represents the power capability of the linear amplifier. A larger P_{1dB} indicates a larger linear dynamic range.

The standard method to evaluate the nonlinearity is to apply two equal amplitude input signals called fundamentals (f_1 and f_2) at the input and measure the intermodulation product level at the output by a spectrum

analyzer (two-tone method) [8]. The output power spectra is shown in Fig.2.1(b), where f_1 and f_2 are the fundamentals, $2f_1$ and $2f_2$ are the second harmonics, $3f_1$ and $3f_2$ are the third harmonics, $f_1 \pm f_2$ are the second-order intermodulation products, $2f_1 \pm f_2$ and $2f_2 \pm f_1$ are the third-order intermodulation products.

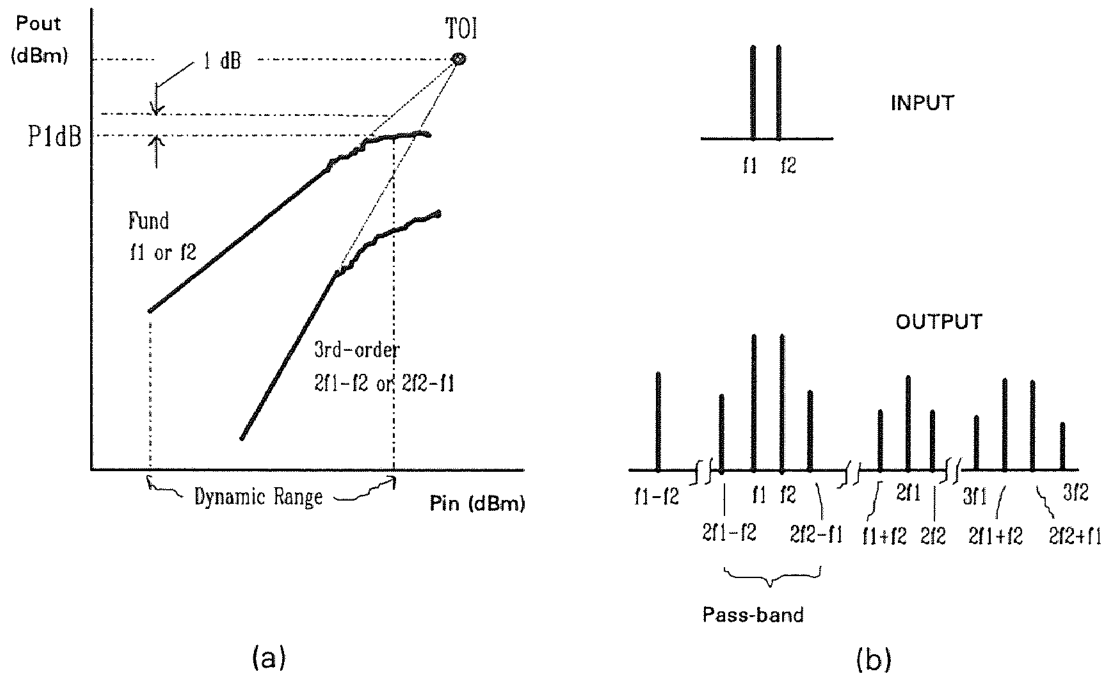


Figure 2.1 Microwave Amplifier Power Transfer Characteristics and Nonlinearity

The third-order intermodulation product $2f_1 - f_2$ or $2f_2 - f_1$ are the ones most close to the fundamental signals and fall within the amplifier pass-band, producing distortion at output. The power level of this intermodulation distortion (IMD) product is also plotted as a function of input power P_{in} in Fig.2.1(a). The linear amplifier design requires this 3rd-order IMD curve to be as below the fundamental curve as possible. This leads to another important parameter for the characterization of a linear amplifier --- third-order intercept point power (TOI) which is defined as the linear extrapolation intercept point of the fundamental power curve and 3rd-order IMD power

curve. A larger TOI indicates a lower level 3rd-order intermodulation product. By a simple geometrical calculation, the TOI is related to the output power of one of the tones P_0 and the third-order product level P_{IMD3} by

$$TOI = P_o + (P_o - P_{IMD3}) / 2 \quad (1)$$

Practically, TOI at the input terminal is also measured to characterize a linear amplifier.

2.2 Fundamental Limitation on Linearity

As described by Perlow [9], even if the amplifying device were ideally linear, gain compression (or power saturation) would still occur as long as the dc power supply remained unchanged. This is easily understood by the following energy conservation analysis:

Considering a two-port amplifier of Fig.2.2, no assumption about the linearity of the amplifier is made. The total input power to the amplifier must be equal to the total output power:

$$P_{in} + P_{dc} = P_o + P_{diss} \quad (2)$$

Power gain G_p is defined as

$$G_p = \frac{P_o}{P_{in}} \quad (3)$$

The dissipated power P_{diss} is given by

$$P_{diss} = P_{dc} - (G_p - 1) P_{in} \quad (4)$$

If the power gain G_p were to remain constant and greater than unity, then at some level of input power the dissipated power P_{diss} would become negative. This is clearly impossible and, therefore, the power gain must be compressed unless the dc power supply is infinitely large. This conclusion is independent of the amplifier nonlinearity. Practically, the dc power supply to

an amplifier can not be infinitely large. The gain compression or power saturation is thus a fact no matter how linear is the amplifier.

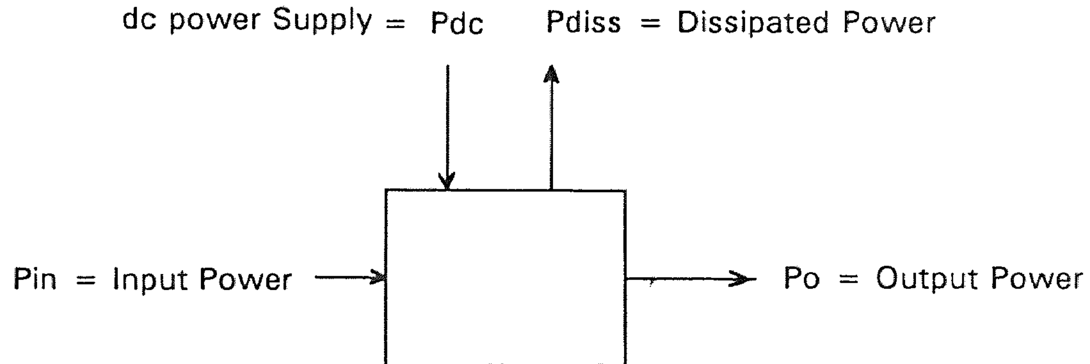


Figure 2.2 Two Port Amplifier

Because of the power saturation, as the input signal amplitude is increased, the output of the amplifier will become increasingly distorted. Then, the transfer characteristics is no longer linear. It can be represented by an infinite series

$$P_o = \sum_{n=1}^{\infty} k_n \, P_{in}^n \qquad (5)$$

where the coefficients of the transform network function k_n are generally complex quantities.

In the linear region of small input power level, only the first term of the expansion is non-zero. Then

$$P_o \approx k_1 \, P_{in} \qquad (6)$$

In slightly nonlinear region, the transfer characteristics can be represented by the first three terms

$$P_o \approx k_1 \, P_{in} + k_2 \, P_{in}^2 + k_3 \, P_{in}^3 \qquad (7)$$

This is an important approximation that will lead to the concept of the third-

order intermodulation components as mentioned in Section 2.1.

If the input to the amplifier consists of two sinusoidal type signals f_1 and f_2, the high order terms in Eq.(7) will create new frequency components.

The first order term reproduces two fundamental signals f_1 and f_2. The second order term creates output signals at the second harmonic $2f_1$ and $2f_2$ as well as f_1-f_2 and f_1+f_2. They are all located outside the amplifier pass-band.

The third order term creates output at frequencies $3f_1$, $3f_2$, $2f_1+f_2$, $2f_2+f_1$ as well as $2f_1-f_2$, $2f_2-f_1$ and exactly at fundamental input frequencies f_1 and f_2.

The components $2f_1-f_2$ and $2f_2-f_1$ are so important since they are very close to the input frequencies and usually fall within the passband of the amplifier and can not be filtered out. These components are called third-order intermodulation distortion products.

The components that are exactly at the input frequencies f_1 and f_2 will add vectorially to the output produced by the first order term. If the phase of the component created by the third order term is 180 degrees out of phase with that produced by the first order term, the output power at that frequency will be compressed. Since the output amplitude of the signal created by the third order term is a function of input signal level, this reduction in output amplitude will increases as the input signal level increases. This is known as gain compression or power saturation.

If the output component created by the third order term is not 180 degrees out of phase with the component produced by the first order term, then the output power amplitude and phase will all be functions of the input signal level. The change in output amplitude when the input level is changed is so called AM to AM conversion. The change in output phase angle when the input level is changed is known as AM to PM conversion.

The above analysis shows that the high order intermodulation distortion is the natural consequence of power saturation or gain compression.

2.3 Microwave GaAs MESFET Nonlinearity

As described above, gain compression or power saturation exists for all amplification schemes whether they are linear or nonlinear. The use of active devices will speed-up the power saturation and worsen the amplifier linearity. For a GaAs microwave amplifier, the GaAs MESFET linearity is thus so important that it is necessary to address the nonlinear sources in the MESFET.

A typical MESFET output characteristics is shown in Fig.2.3(a). Two nonlinear behaviors are observed from the figure. The first one is the transconductance nonlinearity, g_m. Note that at both low I_{ds} and high I_{ds} regions, the variation of I_{ds} with V_{gs} at a fixed drain voltage V_{ds} becomes very non-uniform. The variation of I_{ds} with V_{gs} is thus not a linear function. This is known as nonlinear gate transfer characteristics and is shown in Fig.2.3(b). Another way to describe the nonlinear gate transfer characteristics is by the use of transconductance g_m that is defined as the variation of I_{ds} with V_{gs} at a fixed drain voltage V_{ds}:

$$g_m = \left. \frac{\partial I_{ds}}{\partial V_{gs}} \right|_{V_{ds}} \tag{8}$$

The nonlinear variation of g_m with V_{gs} is shown in Fig.2.3(c).

The second nonlinear behavior is the output resistance nonlinearity, R_{ds}. It is noticed that the I_{ds} current increases rapidly with drain voltage V_{ds} at high drain voltage region since it is near the drain breakdown region. Thus, the

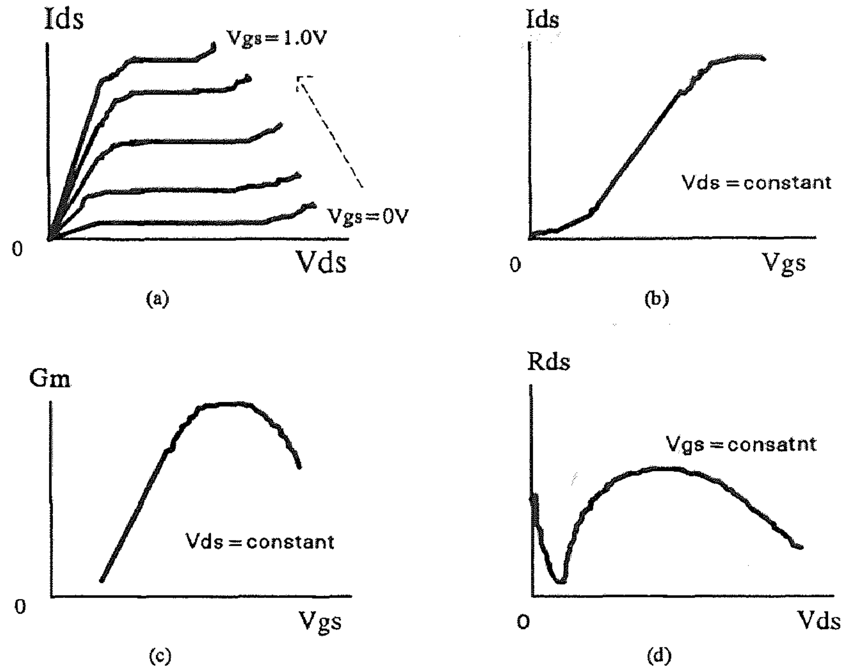


Figure 2.3 Nonlinear DC-Characteristics of a MESFET

variation of I_{ds} with V_{ds} at a fixed gate voltage results in a nonlinear behavior. The output drain-source resistance R_{ds} is defined as

$$R_{ds} = \left. \frac{\partial V_{ds}}{\partial I_{ds}} \right|_{Vgs} \qquad (9)$$

And the nonlinear variation of R_{ds} with V_{ds} at a fixed gate voltage is shown in Fig.2.3(d).

In the two nonlinear behaviors described above, the g_m nonlinearity is the most important one since it directly relates the MESFET output v_o to the input v_i variation. If the load resistance is R_L, then the MESFET output voltage is

$$v_o = v_i \, g_m \, R_L \qquad (10)$$

If the input signal v_i is the combination of two equal-amplitude tones f_1 and f_2, then the g_m nonlinear behavior can produce third-order intermodulation distortion at $2f_1$-f_2 or $2f_2$-f_1 as described in Section 2.2. By Taylor expansion

of Eq.(10), Parker [10] has shown that the third-order intercept point power TOI is given by

$$TOI = 8\, g_m^3\, R_L\, (\frac{d^2 g_m}{d\, v_i^2})^{-1} \tag{11}$$

Hence, the second derivative of transconductance g_m can be used to predict the third-order intermodulation. From Eq.(8), g_m is the derivative of drain current with respect to the gate potential. This implies that the third derivative of drain current can also be used to predict the third-order intermodulation distortion.

It becomes clear that to obtain a highly linear MESFET, a technique to maintain a constant transconductance g_m over a large gate voltage swing must be developed. It has been found that [11] the linearity of a depletion-mode MESFET can be improved substantially by heavily doping the channel near the buffer layer and lightly doping the channel near the gate surface. Since the lower electron mobility near the buffer layer that limits the channel current near pinch-off region can be compensated by providing more electrons through this grading doping technique, this approach enhances the current capability in this region and offers a nice flat transistor I_{ds}-V_{ds} output characteristics as shown in Fig.2.4(b). The transconductance g_m is seen to be a constant over the variation of V_{gs}. Obviously, large maximum drain current $(I_{ds})_{max}$ and high breakdown voltage BV_{ds} will lead to an even more linear MESFET since the AC-current and voltage can swing over a larger range without suffering distortion.

As described in reference [11], a grade doped channel can provide a highly linear MESFET with a constant transconductance g_m. This is based upon the following analysis:

Transconductance, $$g_m \equiv \frac{\partial I_{ds}}{\partial V_{gs}} \equiv \frac{\varepsilon_o \varepsilon_r \upsilon_{sat} W}{d_d(V_{gs})} \tag{12}$$

Depletion depth, $$\frac{\partial d_d(V_{gs})}{\partial V_{gs}} \equiv \frac{\varepsilon_o \varepsilon_r}{q} \frac{1}{d_d N_d(d_d)} \tag{13}$$

Gate capacitance, $$C_{gs} \equiv \varepsilon_o \varepsilon_r \frac{L_g W}{d_d(V_{gs})} \tag{14}$$

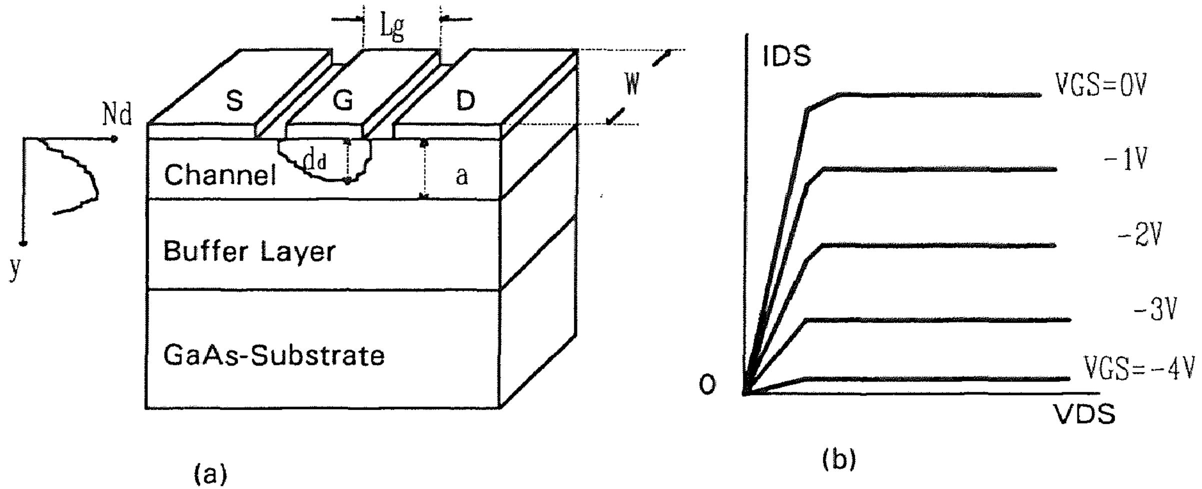


Figure 2.4 MESFET Structure and Output Characteristics

where υ_{sat} is the saturation velocity, L_g is the gate length, W is the gate width, $N_d(d_d)$ is the doping concentration in the channel, $d_d(V_{gs})$ is the depletion depth under the gate which is the function of applied gate voltage.

High linearity at DC implies a constant g_m. From Eq.(12), if $d_d(V_{gs})$ is insensitive to the gate voltage variation, constant g_m can be obtained. From Eq.(13), this can be realized by lightly doped channel near the gate (increase depletion depth d_d) and highly doped channel near the buffer layer (increase

doping concentration N_d). By adjusting the ion-implanted doping profile in the channel, this goal can be achieved.

Even though a large d_d will reduce g_m, the RF performance can still be maintained since $f_T \propto g_m / C_{gs} = \upsilon_{sat} / L_g$ is a constant.

At microwave frequencies, the linearity will be characterized by a low 3rd-order intermodulation level and the S-parameters insensitive to the bias voltages.

One of the benefits of heavily doping the channel near the buffer layer is a low noise. Since minimum noise figure is usually obtained when the FET is biased near pinch-off region and noise figure is inversely related to g_m, this doping technique can increase g_m near pinch-off and hence the noise figure is reduced.

In summary, constant g_m, S-parameters insensitive to the bias points, and lower intermodulation product level have to be satisfied to realize a highly linear field-effect transistor.

Chapter 3

LARGE-SIGNAL MODELING TECHNIQUES OF A MESFET

The goal of this thesis is to predict the nonlinear response of a MESFET by using HP85150B Microwave Design System. The information will be helpful in the design of the microwave linear GaAs MESFET. However, the success of CAD simulation relies heavily on an accurate transistor model. The nonlinear simulation requires a large-signal model. Though a small-signal model is not adequate for nonlinear characterization, it is still the basis for the construction of a large-signal model.

3.1 Small-Signal Equivalent Circuit Model

A small-signal lumped element equivalent circuit model operating at saturation region is shown in Fig.3.1(a) with the corresponding physical origin as shown in Fig.3.1(b). This model is capable of modeling the MESFET microwave performance up to 26 GHz.

In the figure, R_g, R_s, R_d, L_g, L_s, L_d are the parasitic resistances and inductances of the gate, source, and drain, respectively. C_{in} and C_{out} are the capacitances of input and output bonding pads to substrate. C_{gs}, C_{dg}, C_{ds}, R_i, R_{ds}, g_m, and τ should have been the bias dependent elements. However, they are assumed to be constants in a small-signal model since the device is operated only in a linear, flat region of the MESFET output characteristics, and the input signal swing is very small. C_{gs} is the gate barrier capacitance from gate to source. Since channel has resistance, a resistance R_i is in series with C_{gs}. C_{gs} and R_i comprise a RC circuit. Its charge and discharge will

limit the MESFET frequency performance. τ is the electron transit time under the gate which is equal to $C_{gs}R_i$. C_{dg} is the gate capacitance between drain

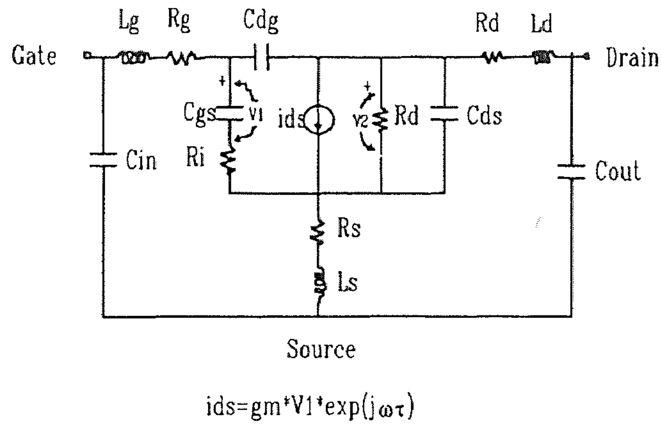


Figure3.1(a) MESFET Small-Signal Equivalent Circuit

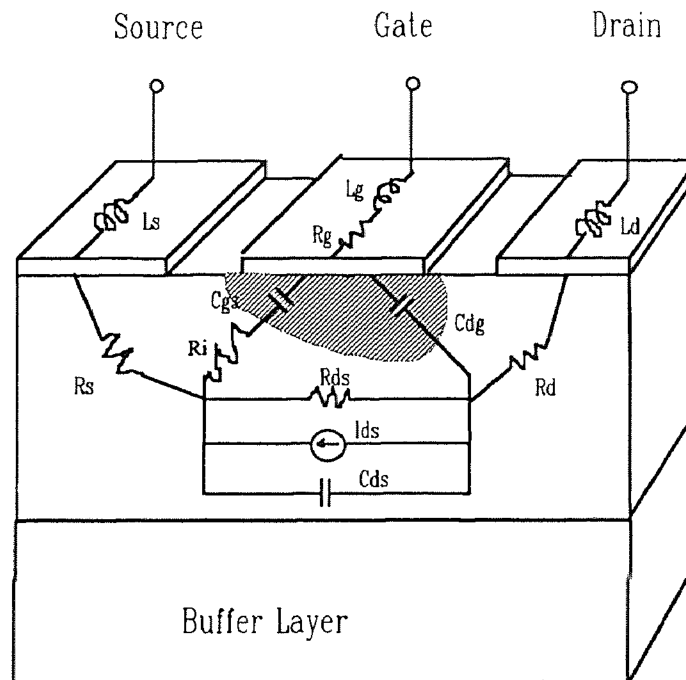


Figure 3.1(b) Physical Origin of the Circuit Elements of the MESFET

and gate which represents the feedback from drain to gate and leads to reduction of MESFET high frequency gain. C_{gs} and C_{dg} are actually two portions of the same gate barrier capacitance. R_{ds} is the intrinsic resistance between drain and source. I_{ds} is the gate voltage controlled drain current source. It is actually controlled by the voltage across C_{gs} at higher frequencies. The parasitic resistances R_g, R_s, R_d in the model are determined by Fukui dc-measurements [12], while parasitic inductances L_g, L_s, L_d are extracted by "cold-FET" (drain voltage $V_{ds} = 0$) S-parameter optimization [3]. The rest of the parameters are extracted by "hot-MESFET" (drain voltage $V_{ds} \neq 0$) S-parameter optimization [3]. The optimization matches the calculated and measured S-parameter data until the required error is met. Since the model is a small-signal one and the input signal is varied only in a very small range around the operating bias point, all the elements are supposed to be constants. Thus only one set of S-parameters at one V_{gs} and V_{ds} bias point in the linear saturation region is needed to extract the model.

3.2 Several Large-Signal Modeling Techniques

It is obvious that the assumption of constant elements in a small-signal equivalent circuit model will not be valid for the large-signal case since the large input signal will easily sweep into the nonlinear regions of the MESFET output I_{ds}-V_{ds} characteristics. Several techniques were then proposed for the construction of a large-signal equivalent circuit model.

3.2.1 Willing Type Large-Signal Model [1,2]

In 1978, Willing proposed a large-signal model [1] in which the topology is the same as that of the small-signal model described above. The only difference is that the bias dependent elements C_{gs}, C_{dg}, C_{ds}, R_i, R_{ds}, g_m, and τ

have to be incorporated into the model.

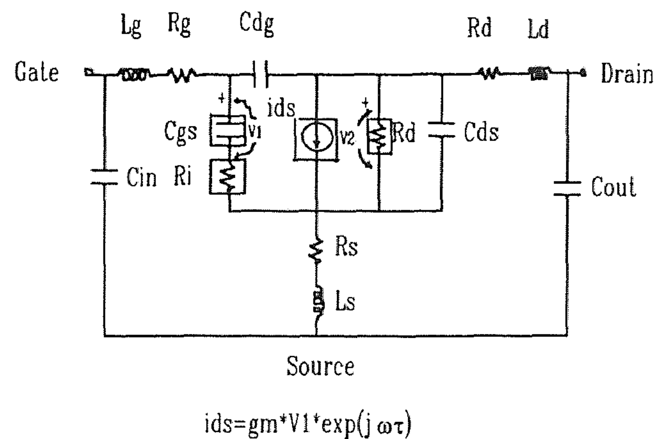


Figure 3.2 Willing Large-Signal Equivalent Circuit

The dependence of these elements on bias voltages V_{gs} and V_{ds} are obtained by measuring the MESFET S-parameters under various frequency and bias conditions and then fitting simulated S-parameters to measured S-parameters. The bias dependent functions of the elements are obtained by curve fitting technique. From his research, only four elements are found to be the most bias dependent. They are g_m (related to I_{ds}), C_{gs}, R_i, and R_{ds}. The other elements C_{dg} and C_{ds} can be assumed to be practically linear. Actually, these two capacitances are very small in values. The large-signal model is shown in Fig.3.2 where the elements in square represent the bias dependent nonlinear elements. Also, the dependence of C_{gs} and R_i on only V_{gs} is always assumed since the bias dependent results show that C_{gs} and R_i have strong dependence on V_{gs} while dependence on V_{ds} is small.

The above functions, however, are obtained under static bias conditions. Under normal high frequency operation, the MESFET is in a dynamic state. The instantaneous function expressions for the elements have to be expressed explicitly. Rauscher's research [2] provides clear

relationships between the instantaneous and the static expressions. These relationships are given as follows, where x denotes the instantaneous element expression while $\bar{x}$ denotes the static element expression:

For C_{gs}:

$$C_{gs}(V_{gs},V_{ds}) = \overline{C}_{gs}(V_{gs},V_{ds}) \tag{15}$$

For R_i:

$$R_i(V_{gs},V_{ds}) = \overline{R}_i(V_{gs},V_{ds}) \tag{16}$$

For g_m:

$$g_m(V_{gs},V_{ds}) = \frac{1}{V_{gs}} \cdot \int_0^{V_{gs}} \overline{g}_m(v,V_{ds})dv \tag{17}$$

As for R_{ds}, it is equal to $1/g_{ds}$, where g_{ds} is given by

$$g_{ds}(V_{gs},V_{ds}) = \frac{1}{V_{ds}} \cdot \int_0^{V_{ds}} \overline{g}_{ds}(V_{gs},v)dv \tag{18}$$

3.2.2 Curtice Large-Signal Model [3]

Curtice large-signal model is the one most commonly used in commercial CAD packages such as MWSPICE, HP85150B MDS, etc. The circuit topology is shown in Fig.3.3.

The feature of this model is the existence of two voltage-controlled current sources at both gate-source and gate-drain junctions. i_{gs} represents gate current that occurs when the gate-source junction is forward biased. i_{dg} represents the drain-gate avalanche current that can occur at large-signal operation. They are usually represented by a linear junction model:

$$i_{gs} = \frac{V_{gs} - V_{bi}}{R_F} \tag{19}$$

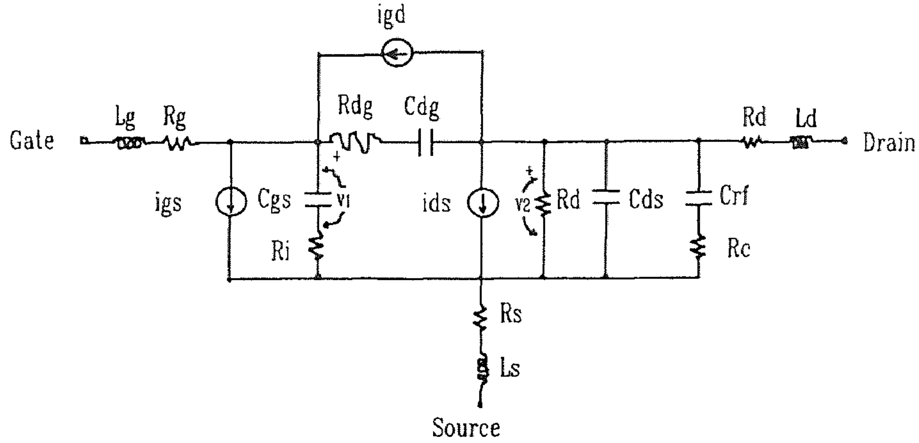


Figure 3.3 Curtice MESFET Large-Signal Equivalent Circuit Model

where V_{bi} is the built-in voltage and R_F is the junction forward resistance.

and
$$i_{dg} = \frac{-V_{dg} + V_B}{R_1} \tag{20}$$

Where $V_B = V_{BR} + R_2 \cdot I_{ds}$, V_{BR} is the junction reverse breakdown voltage, R_1 is the approximate breakdown resistance and R_2 is the resistance relating the breakdown voltage to the channel current.

C_{gs} and C_{dg} are represented by pn-junction capacitance model:

$$C_{gs} = \frac{C_{gs0}}{\sqrt{1 - \frac{V_{gs}}{V_{bi}}}} \tag{21}$$

and
$$C_{dg} = \frac{C_{dg0}}{\sqrt{1 - \frac{V_{dg}}{V_{bi}}}} \tag{22}$$

where C_{x0} denotes zero bias capacitance.

Other parameters R_i, R_{ds} and C_{ds} will be given as constants determined by small-signal S-parameter optimization.

The important nonlinear source is the voltage controlled drain current source I_{ds}. Curtice gave two empirical expressions for the drain current source.

The first one is a square-law relationship and is called Curtice quadratic model:

$$I_{ds} = \beta_1 \,(V_{gs} - V_{TO})^2 \,(1 + \lambda V_{ds}) \tanh(\alpha V_{ds}) \tag{23}$$

where V_{TO} is the threshold voltage of the MESFET. β_1, λ, and α are the fitting parameters determined by DC-measurements. The disadvantage of this model is that it can not model the I_{ds} nonlinear behavior accurately in high I_{ds} region.

The second expression for the drain current is a cubic approximation and is called Curtice cubic model:

$$I_{ds} = (A_0 + A_1 V_1 + A_2 V_1^2 + A_3 V_1^3) \tanh(\gamma V_{ds}) \tag{24}$$

where

$$V_1 = V_{gs} \,[\, 1 + \beta_2 \,(V_{ds0} - V_{ds})\,] \tag{25}$$

and V_{dso} is the drain-source voltage where parameters A_0, A_1, A_2 and A_3 are evaluated.

In a commercial CAD package, the Curtice model is usually given by a set of parameters as shown in Table 3.1. Some of these parameters can be determined from the above equations.

The difference between Curtice model and Willing model is that the Curtice model uses empirical equations to fit the model as well as the inclusion of gate-source and drain-gate current sources to represent the breakdown mechanism.

Compared with Willing model, an extra avalanche breakdown measurement must be carried out to determine the fitting parameters. Also, Curtice model reveals less physical behavior of model elements' variation with bias voltages V_{gs} and V_{ds}. If one needs to understand more about the model elements and fully explore the CAD package, Willing model is the candidate.

Table 3.1 Curtice Cubic Model Parameter Table Form in HP85150B MDS

CMP1
CurticeC

* CURTICE CUBIC MESFET MODEL *

MODEL=MESFETMODEL

IDS model	Gate model	Parasitics	Breakdown
NFET=yes	RIN=	RG=	GSFWD=
PFET=	RF=	RD=	GSREV=
IDSMOD=2	FC=	RS=	GDFWD=
BETA2=	GSCAP=	LG=	GDREV=
RDS0=	CGS=	LD=	R1=
VDS0=	GDCAP=	LS=	R2=
VDSDC=	CGD=	CDS=	VBI=
TAU=		CRF=	VBR=
A5=		RC=	VJR=
GAMMA2=			IS=
TNOM=			IR=
IDSTC=			XTI=
A0=			EG=
A1=			N=
A2=			IMAX=1
A3=			

In this work, a Willing type large-signal model is constructed upon dc and S-parameter measurements. Modified Curtice empirical equations were developed to fit the measured element values as functions of bias voltage V_{gs} and V_{ds}. This model gives a quick turn-out and reasonable accuracy. Furthermore, the construction of the model provides an opportunity for fully understanding of the HP85150B Microwave Design System.

Chapter 4

MESFET R240522 LARGE-SIGNAL MODEL CONSTRUCTION

The details on the construction of MESFET R240522 large-signal model will be discussed in this Chapter. DC and small-signal S-parameter measurement data at various bias points were first provided from measurement carried out in Anadigics Inc. The equivalent circuit topology used is the Willing type as shown in Fig.3.2 which is based upon the small-signal equivalent circuit of Fig.3.1(a). The construction is carried out in the environment of HP85150B Microwave Design System and ORIGIN curve-fitting software.

4.1 Determination of Parasitic Resistance R_s, R_d, and R_g by Fukui DC-Approach

The determination of the parasitic resistance R_s, R_d, and R_g is the first step for the construction of a large-signal model. Fukui approach [12] is a common technique for the determination of the resistance. This approach is based upon the MESFET output I_{ds}-V_{ds} characteristics. The measurement results of this characteristics for R240522 is shown in Fig.4.1.

The threshold voltage V_{TO} of the MESFET at which the drain current dropped to zero must be first available. It is determined from the gate transfer characteristics I_{ds}-V_{gs} at a fixed drain voltage V_{ds}. This V_{ds} is usually chosen in the flat region of the MESFET output I_{ds}-V_{ds} characteristics of Fig.4.1. The gate transfer characteristics I_{ds}-V_{gs} at drain voltage V_{ds}=3V is shown in Fig.4.2. By linear extrapolation of the curve in the figure, the intercept point at $I_{ds} = 0$ gives the threshold voltage as $V_{TO} = +\ 0.05$ V.

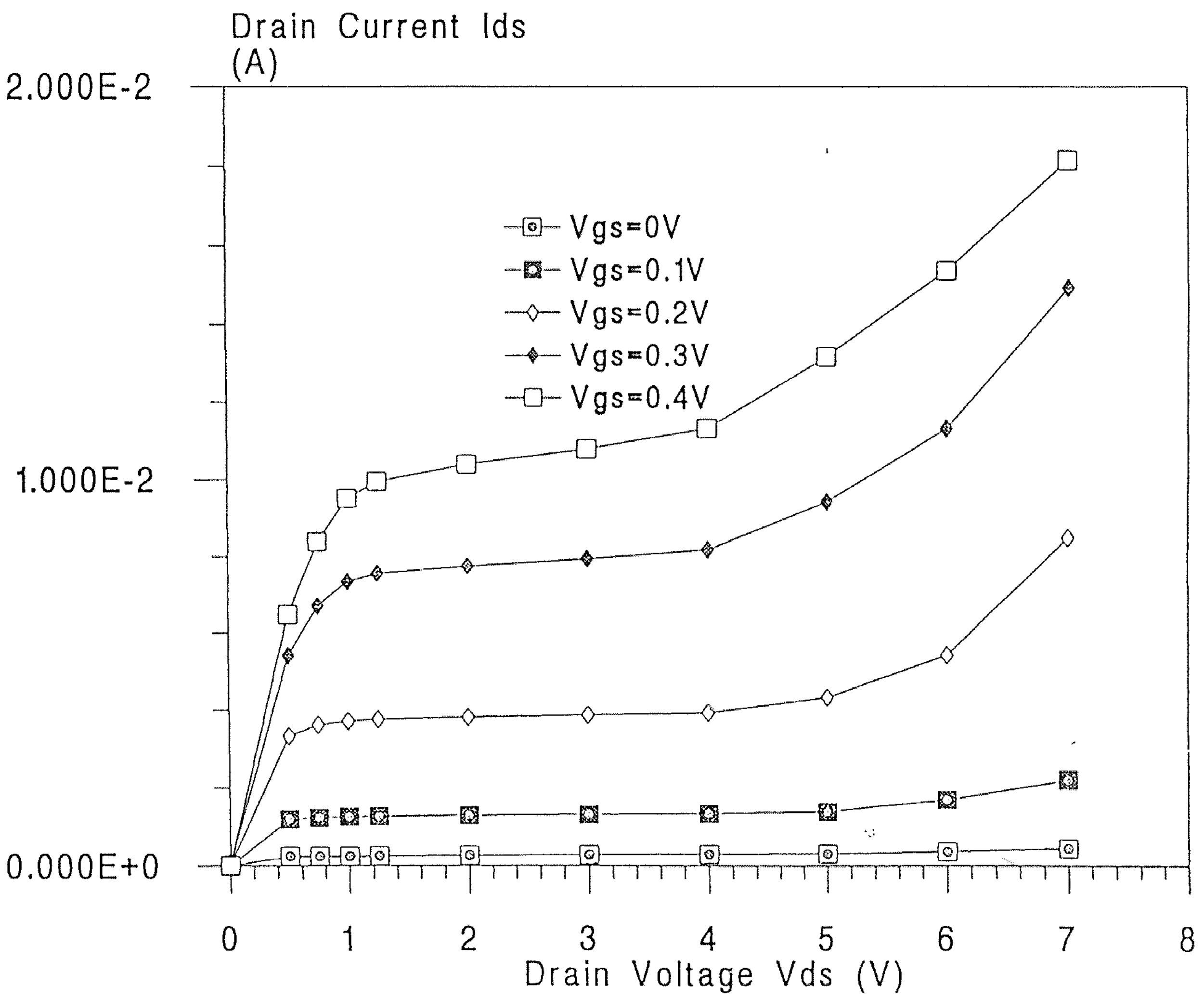


Figure 4.1 Measured MESFET R240522 output I_{ds}-V_{ds} characteristics.

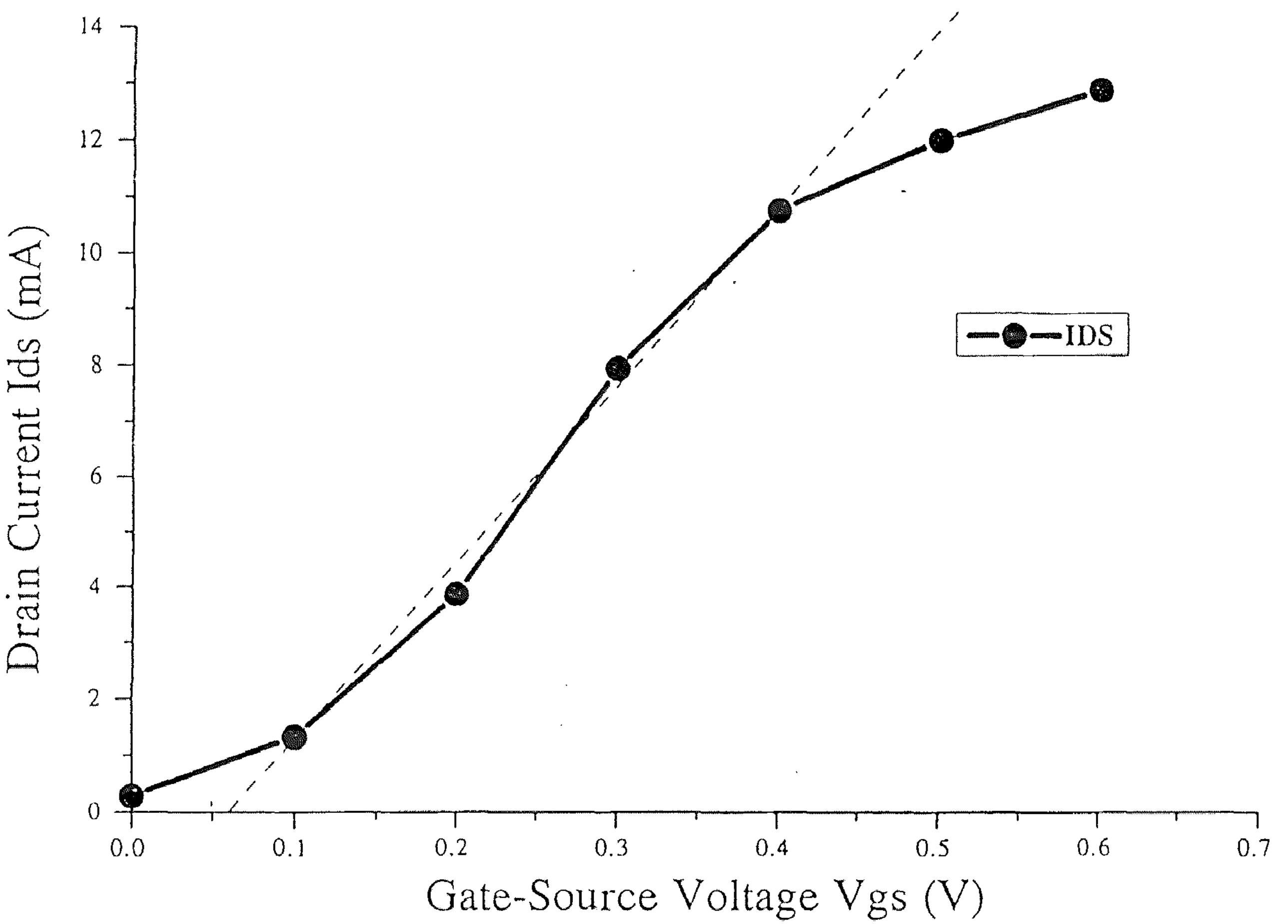


Figure 4.2 Measured MESFET R240522 gate transfer characteristics Ids-Vgs.

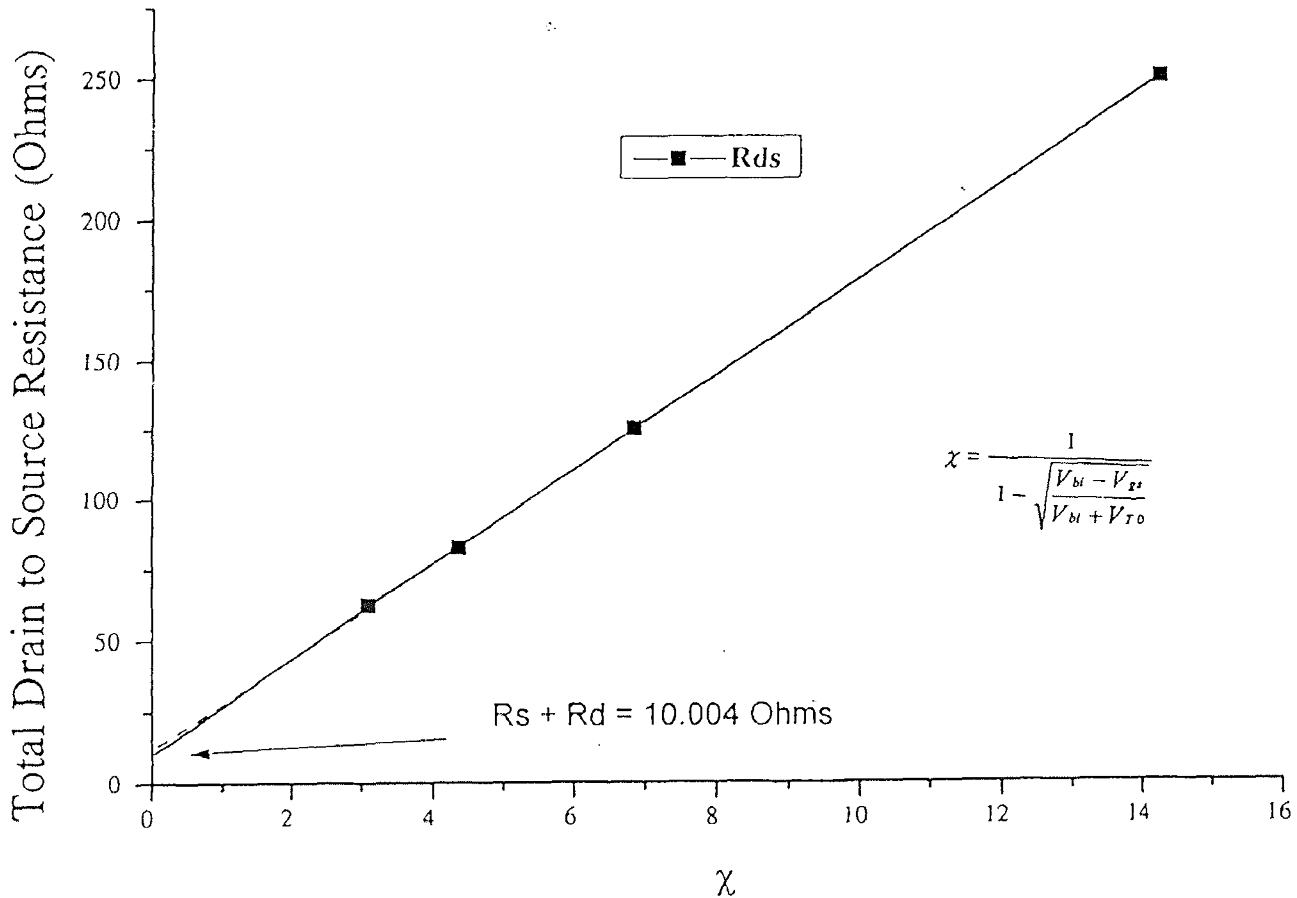


Figure 4.3 Total drain-source resistance R_{ds} as function of χ.

The total drain-source resistance R_{ds} in the linear region of Fig.4.1 is a linear function of χ:

$$R_{ds} = (R_s + R_d) + k\chi \tag{26}$$

where χ is defined as

$$x = \frac{1}{1 - \sqrt{\frac{V_{bi} - V_{gs}}{V_{bi} + V_{TO}}}} \tag{27}$$

The built-in voltage V_{bi} for Au-GaAs gate barrier is about 0.75V. The total drain-source resistance R_{ds} in the linear region of Fig.4.1 can be calculated as $R_{ds}=V_{ds}/I_{ds}$ for different gate voltages from +0.1V to +0.4V. These results are shown in Table 4.1 and plotted in Fig.4.3.

Table 4.1. Linear Region Drain-Source Resistance R_{ds} as Function of V_{gs}

Vgs (V)	0.1	0.2	0.3	0.4
χ	14.28	6.85	4.37	3.10
Rds (Ω)	250	125	83	63

By linear extrapolation of the plot of Fig 4.3 to the ordinate, the intercept with R_{ds}-axis gives combined parasitic resistance as

$$R_s + R_d = 10.004\,\Omega \tag{28}$$

In order to separate R_s and R_d and determine R_g, gate current measurement at three different grounding conditions, i.e. source grounding, drain grounding and source/drain combined grounding, must be made. These measurement results are shown graphically in Fig.4.4.

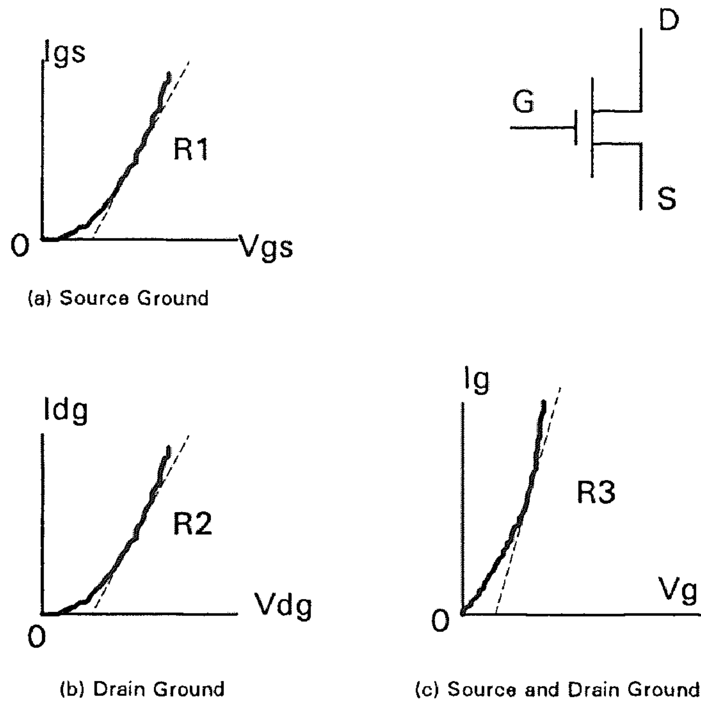


Figure 4.4 Gate Current Measurement for Rs, Rd, and Rg

From Fig.4.4(a) and Fig.4.4(b), R_s-R_d is given by

$$R_S - R_d = R_1 - R_2 \quad (\Omega) \tag{29}$$

From Fig.4.4 (a), (b) and (c), R_g is given by

$$R_g = R_3 - R_1 // R_2 \tag{30}$$

Equations (28), (29) and (30) will give the results for three parasitic resistances.

For simplicity, however, R_d and R_s are assumed to be the same since the MESFET should be symmetrical on both source and drain sides. This assumption will give R_s and R_d based on only Eq.(27) as R_s=5Ω and R_d=5Ω.

As for R_g, it is can be calculated from gate geometrical dimensions and the gate material resistivity ρ by

$$R_g \approx \frac{\rho z^2}{3 L_g h Z} \tag{31}$$

where z is the unit width of the gate metalization, Z is the total gate width, h is the metalization thickness, and L_g is the gate length. For R240522, z=100 μm, Z=200μm, h=1.5μm, and L_g=0.5μm. The gate metalization material is Au-based. By using the Au resistivity ρ = 2.44E-6 Ω-cm, the gate resistance R_g is calculated as 1.52 Ω.

In summary, Fukui approach provides the following initial values for the parasitic resistances:

$R_g \approx 1.5\ \Omega$

$R_s \approx 5.0\ \Omega$

$R_d \approx 5.0\ \Omega$

These values will be further evaluated by "cold-FET" S-parameter fitting.

4.2 Determination of Parasitic Inductance L_g, L_s, and L_d by "Cold-FET" S-parameters

In the case of zero drain bias, i.e. Cold-FET, the equivalent circuit for the MESFET is much simpler since there is no voltage dependent current source. This circuit is suitable for the determination of parasitic inductances L_g, L_s, L_d. It is also used to finalize the parasitic resistances R_s, R_d, and R_g. The cold-FET model of Curtice [3] is shown in Fig.4.5.

By calculating the S-parameters of the cold-FET model and matching with the measured S-parameters, parasitic elements L_s, L_d, L_g and R_s, R_d, R_g can be extracted. The initial values for the R_s, R_d, and R_g are from Fukui measurements as described in Section 4.1. Four sets S-parameters at bias V_{ds}=0V and V_{gs}=0, 0.1, 0.2, 0.3V are optimized to obtain more accurate

results as shown in Table 4.2. The average values in the table will be used for the construction of the large-signal model later.

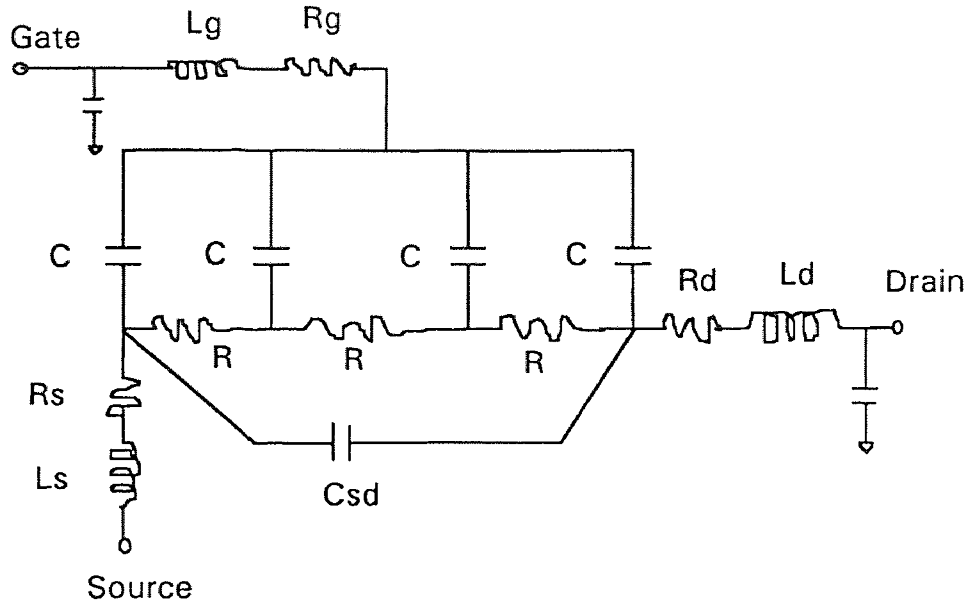


Figure 4.5 Curtice Cold-FET Equivalent Circuit Model

Table 4.2 Optimized Parasitic Element Values For R240522
(V_{ds} = 0V, S-parameters Ranged From 2.5-25 GHz)

V_{gs} (V)	R_s (Ω)	R_d (Ω)	R_g (Ω)	L_s (nH)	L_d (nH)	L_g (nH)
0.0	5.028	10.000	2.585	0.001	0.119	0.053
0.1	1.000	7.327	5.366	0.002	0.058	0.076
0.2	1.721	7.806	2.850	0.026	0.117	0.082
0.3	1.000	6.456	3.392	0.004	0.054	0.094
Average	*2.22*	*7.78*	*3.54*	*0.0082*	*0.087*	*0.0763*

4.3 Determination of Bias Dependent Elements

The S-parameter optimization at full-bias will be used for the extraction of the bias dependent elements C_{gs}, R_i, C_{dg}, C_{ds}, R_{ds}, g_m and τ. The dependence

functions will be obtained by curve fitting technique. The circuit topology is a Willing type as shown in Fig.3.2 that is based on the small-signal model of Fig.3.1(a). The small-signal S-parameters available are ranged from 2.5GHz to 25 GHz and under various bias conditions. V_{gs} bias was chosen at 0.0, +0.1, +0.2, +0.3, and +0.4V. Under each V_{gs}, the drain bias V_{ds} was chosen at 0.0, 0.5, 0.75, 1.0, 1.25, 2.0, 3.0, 4.0, 5.0, 6.0, and 7.0 V. The bias points cover all the regions across the output I_{ds}-V_{ds} characteristics of Fig.4.1. There are totally 55 sets of S-parameter used for the extraction.

A typical S-parameter optimization process on HP85150B MDS is given as follows:

The measured S-parameters were first read into the dataset in HP85150B MDS. In order to be read by HP85150B MDS, the S-parameters must be in a Touchtone format as shown in Table 4.3. They follow the order of

f mag(S11) Pha(S11) mag(S21) Pha(S21) mag(S12) Pha(S12) mag(S22) Pha(S22).

Table 4.3 Touchtone Format S-parameters

```
!  IDS= 1.3160e-003  DELI=0.0  VDS= 3.0000e+000  VGS= 1.0000e-001  VBS= 0.0
#  MHz    S    MA    R 50
 2500   0.922   -43.228   0.990  135.104   0.028   65.937   0.937   -6.701
 3000   0.894   -50.404   0.936  127.417   0.035   63.211   0.930   -7.773
 3500   0.858   -57.517   0.891  120.203   0.042   58.325   0.927   -9.178
 4000   0.829   -64.237   0.840  113.479   0.044   55.439   0.918   -9.908
 4500   0.801   -69.669   0.781  106.941   0.047   50.591   0.916  -11.000
 5000   0.769   -75.750   0.741  101.840   0.050   48.435   0.913  -11.996
 5500   0.751   -80.484   0.684   95.818   0.055   46.013   0.907  -13.185
 7000   0.696   -93.445   0.591   82.137   0.059   37.441   0.894  -15.732
 9000   0.661  -106.300   0.478   66.344   0.068   28.562   0.871  -19.774
11000   0.638  -117.371   0.409   52.770   0.072   20.011   0.816  -23.359
13000   0.610  -128.128   0.358   44.579   0.077   19.601   0.928  -22.525
15000   0.615  -136.044   0.310   30.598   0.076   10.649   0.801  -29.754
17000   0.621  -142.946   0.284   22.221   0.080    7.247   0.872  -32.195
19000   0.599  -148.540   0.269   15.539   0.088    3.168   0.851  -36.091
21000   0.608  -156.171   0.255    8.131   0.083   -2.201   0.840  -38.959
23000   0.602  -160.085   0.224    0.887   0.083  -11.279   0.861  -45.415
25000   0.621  -164.600   0.204  -10.477   0.089   -3.064   0.837  -46.888
```

A small-signal equivalent circuit topology of Fig.3.1(a) was then constructed

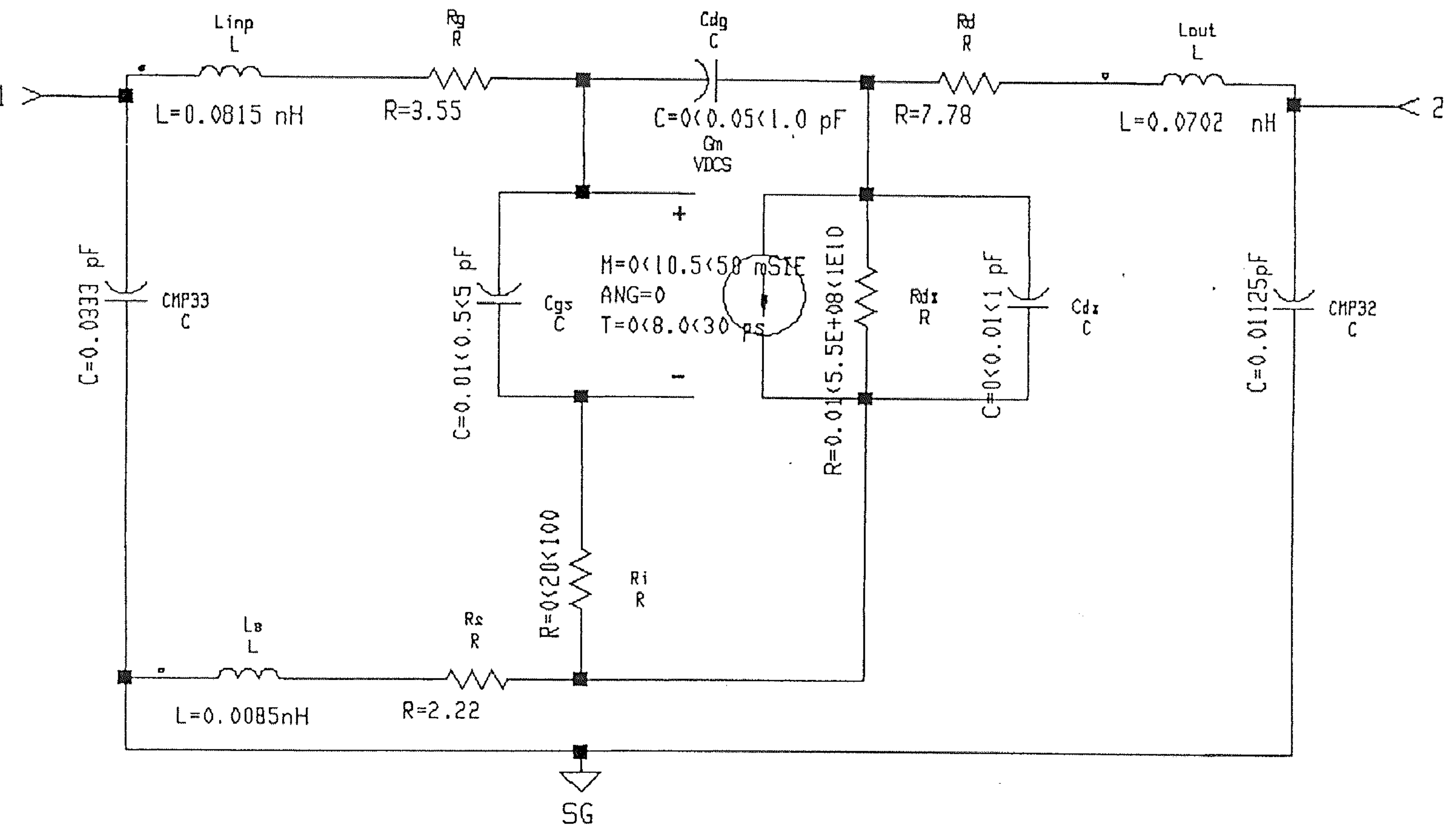


Figure 4.6 Small-signal equivalent circuit model before optimization. Element value variation ranges are specified in the circuit.

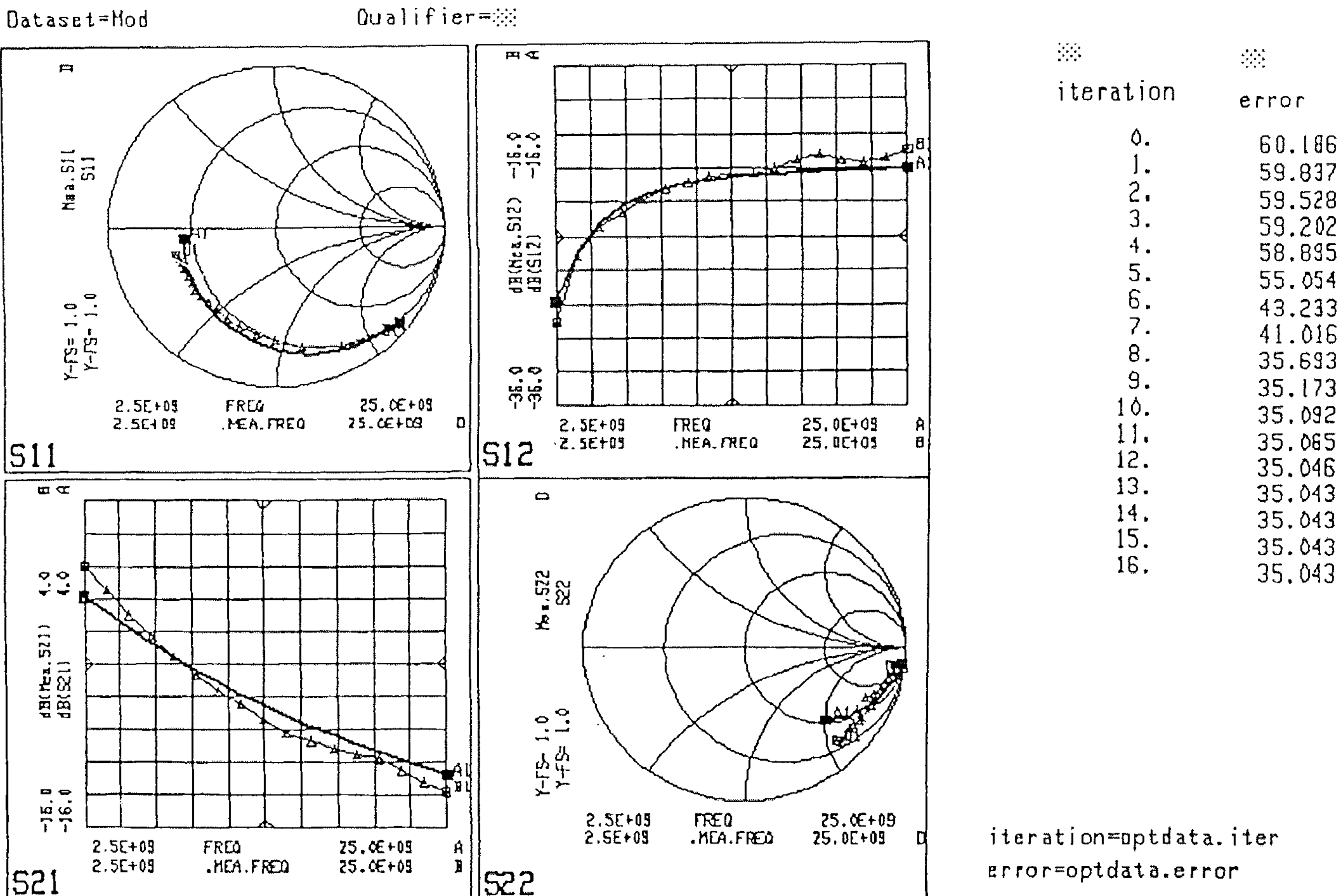
Table 4.4 Optimization goals for S-parameter optimization.

OPTIMIZATION GOALS

Item	Value
Freqs Name	Optfreq
Goal	MAG((Mod.S11-Mea.S11)/Mea.S11)
Good	0
Bad	.01
Bad	
Freqs Name	Optfreq
Goal	MAG((Mod.S12-Mea.S12)/Mea.S12)
Good	0
Bad	.01
Bad	
Freqs Name	Optfreq
Goal	MAG((Mod.S21-Mea.S21)/Mea.S21)
Good	0
Bad	.01
Bad	
Freqs Name	Optfreq
Goal	MAG((Mod.S22-Mea.S22)/Mea.S22)
Good	0
Bad	.01
Bad	

Table 4.5 Optimization method for S-parameter optimization.

OPTIMIZATION PARAMETERS Item	Value
Set-Up Information:	
Optimization Method	gradient
P Factor	4
Minimum Error	.001
Iterations	25
Iterations Per Update	5
Outputs to be Saved:	
Error vs Iteration	yes



iteration	error
0.	60.186
1.	59.837
2.	59.528
3.	59.202
4.	58.895
5.	55.054
6.	43.233
7.	41.016
8.	35.693
9.	35.173
10.	35.092
11.	35.065
12.	35.046
13.	35.043
14.	35.043
15.	35.043
16.	35.043

Figure 4.7 Modeled and measured S-parameter comparison for MESFET R240522. The bias vltages are V_{gs}=+0.1V, V_{ds}=3.0V.

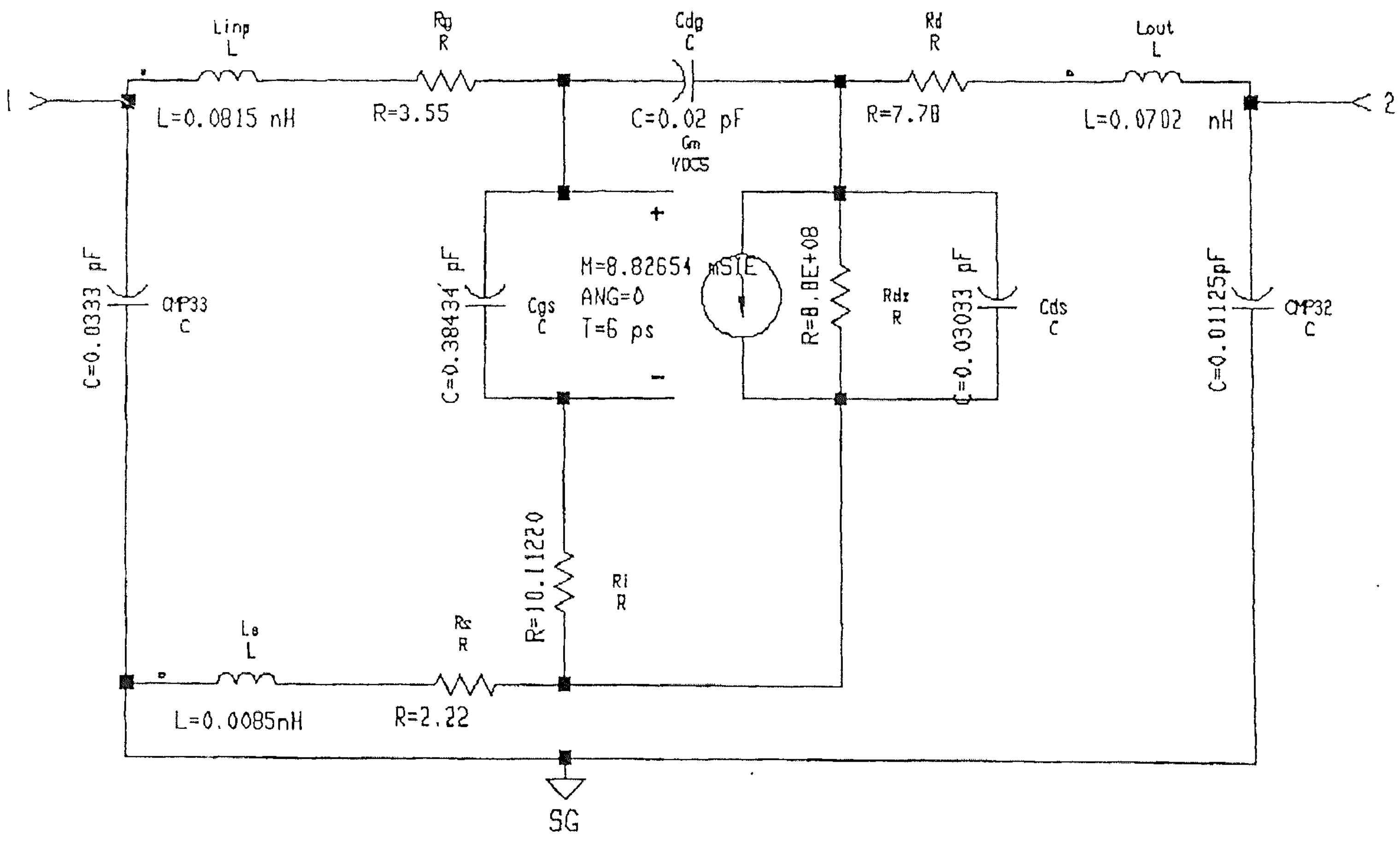


Figure 4.8 Optimized element values for the small-signal equivalent circuit. The bias voltages are V_{gs}=+0.1V and V_{ds}=3.0V.

into a design icon as shown in Fig.4.6. Note that the initial values for all the bias dependent elements with variation ranges are specified in the circuit. The optimization goals and optimization method were then setup as shown in Table 4.4 and Table 4.5. The optimization goals set up the error requirements for measured and modeled S-parameter comparison. The optimization method specifies whether gradient, random, or hybrid optimization approach is used. The optimization can then be initiated. The model-predicted S-parameters were compared with the measured data which have already been stored in the dataset. The optimization process was stopped when the error goals are met. The comparison of measured and modeled S-parameters at bias V_{gs}=+0.1V and V_{ds}=3V is given in Fig.4.7. The optimized equivalent circuit elements are finally extracted as shown in Fig.4.8.

The same procedure was followed by all other bias points. The variations of the bias dependent elements with bias voltages V_{gs}, and V_{ds} were then obtained as shown from Fig.4.9(a) to Fig.4.9(g).

Fig.4.9(a) shows that the active channel capacitance C_{gs} increases as V_{gs} increases. This is due to the decrease of the depletion depth under the gate. Also, at a fixed gate voltage V_{gs}, C_{gs} increases monotonically as V_{ds} increases. This is due to the charge accumulation effects in the channel. However, the dependence of C_{gs} on V_{gs} is much stronger than that on V_{ds}. It is thus always assumed that C_{gs} is the function of V_{gs} only. A general empirical equation describing C_{gs} as function of V_{gs} is given by

$$C_{gs} = \frac{C_{gs0}}{(1 - \frac{V_{gs}}{V_{TO}})^m} \tag{32}$$

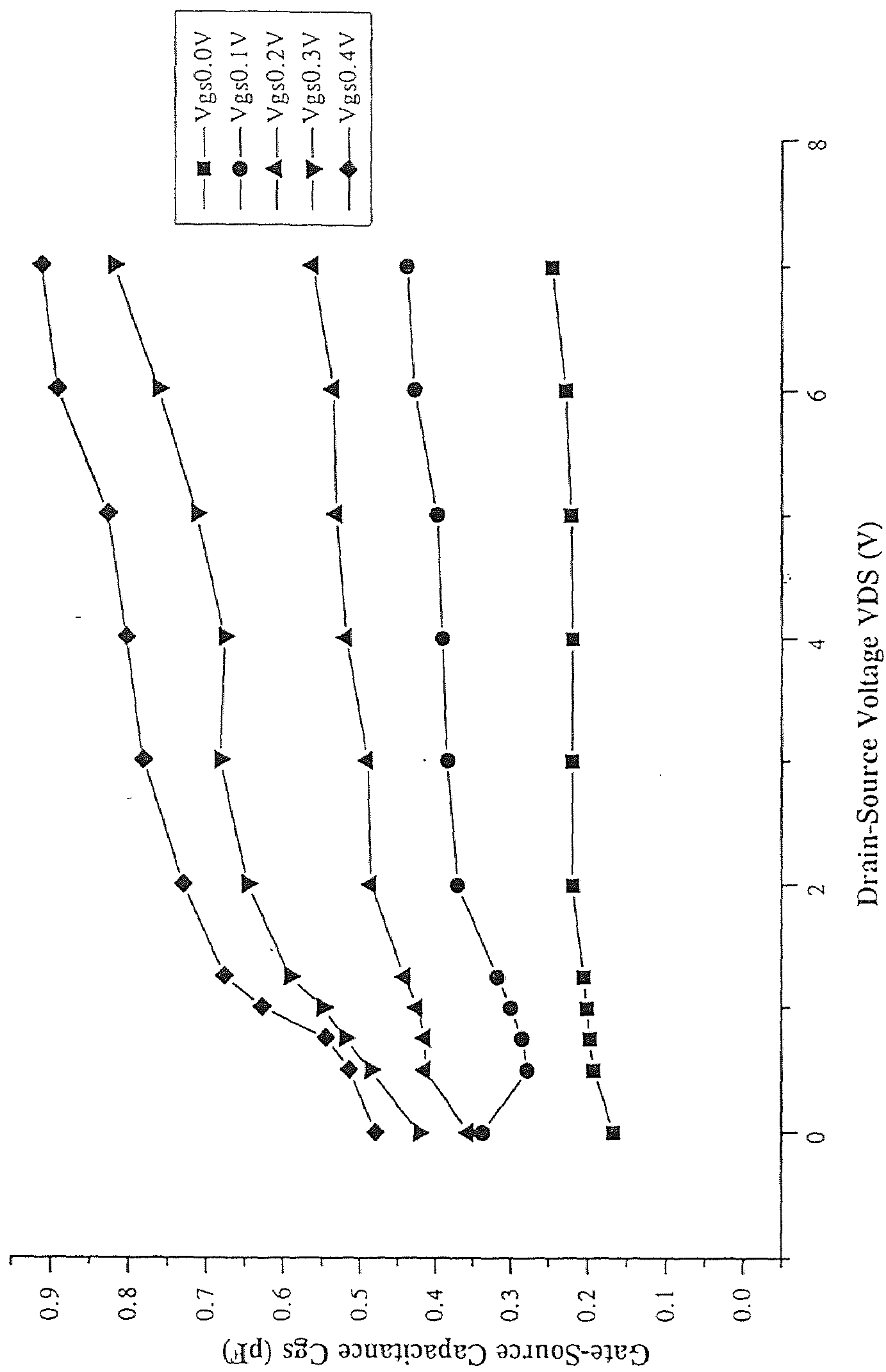


Figure 4.9(a) Gate-source capacitance C_{gs} bias dependent characteristics.

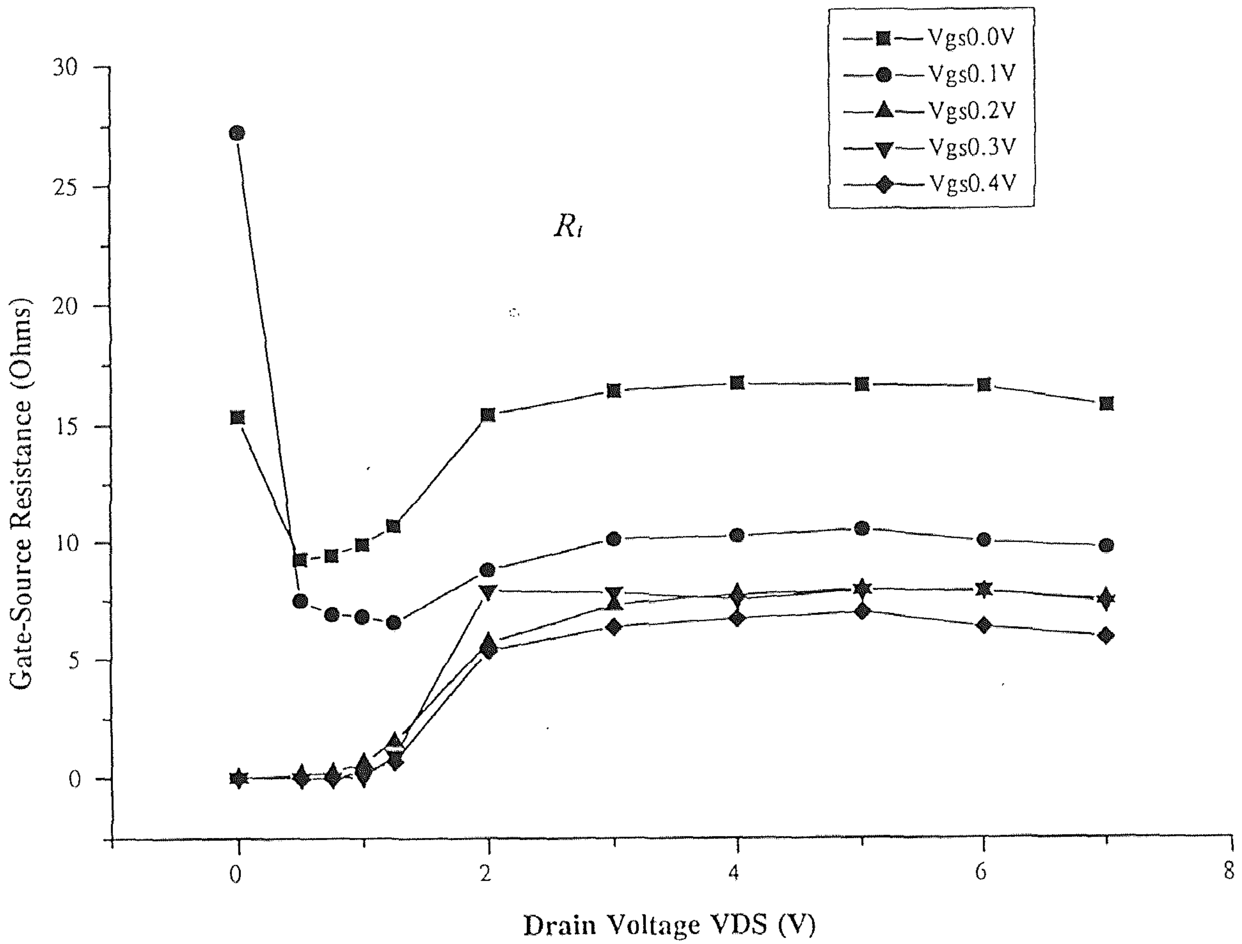


Figure 4.9(b) Gate-source resistance R_i bias dependent characteristics.

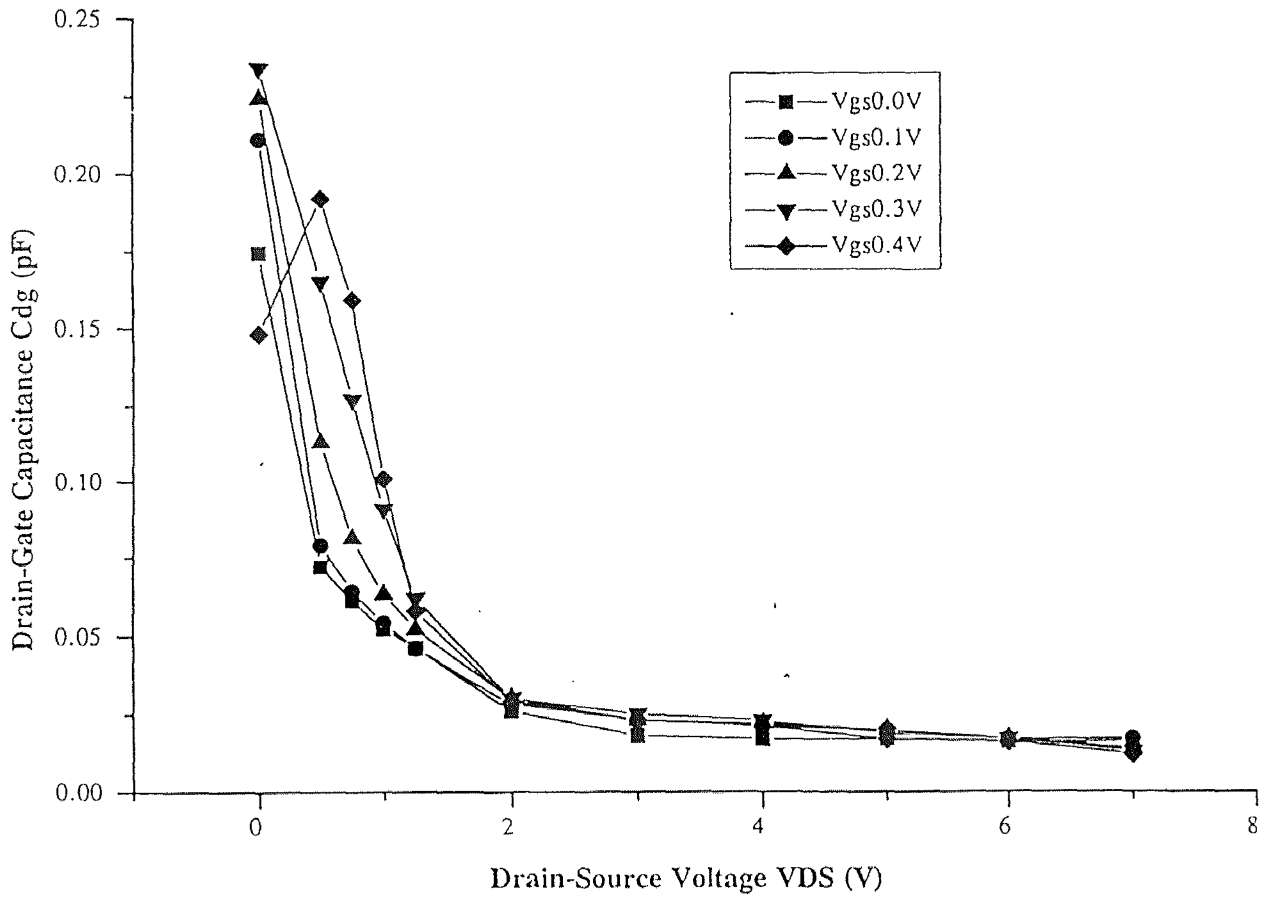


Figure 4.9(c) Drain-gate capacitance C_{dg} bias dependent characteristics.

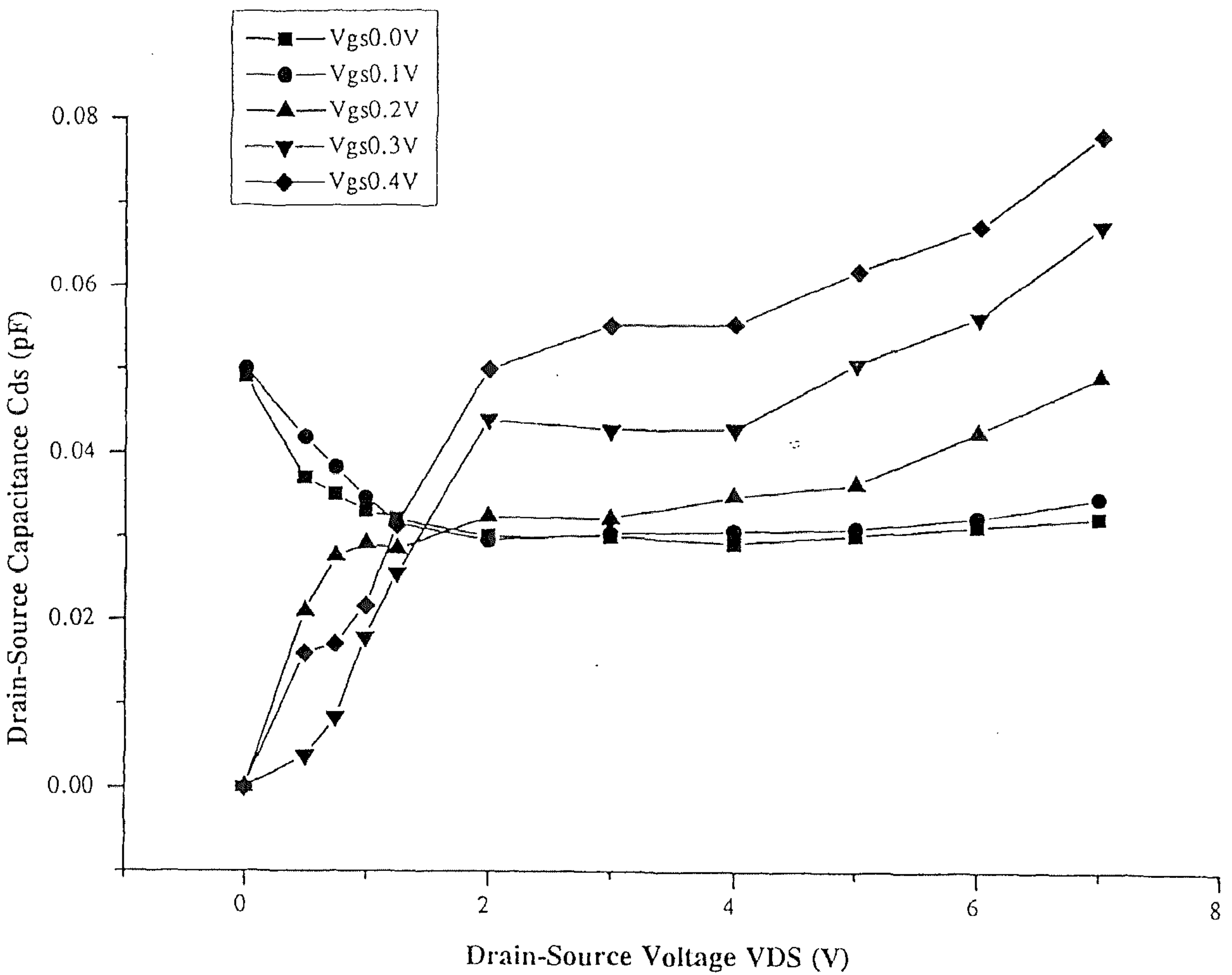


Figure 4.9(d) Drain-source capacitance C_{ds} bias dependent characteristics.

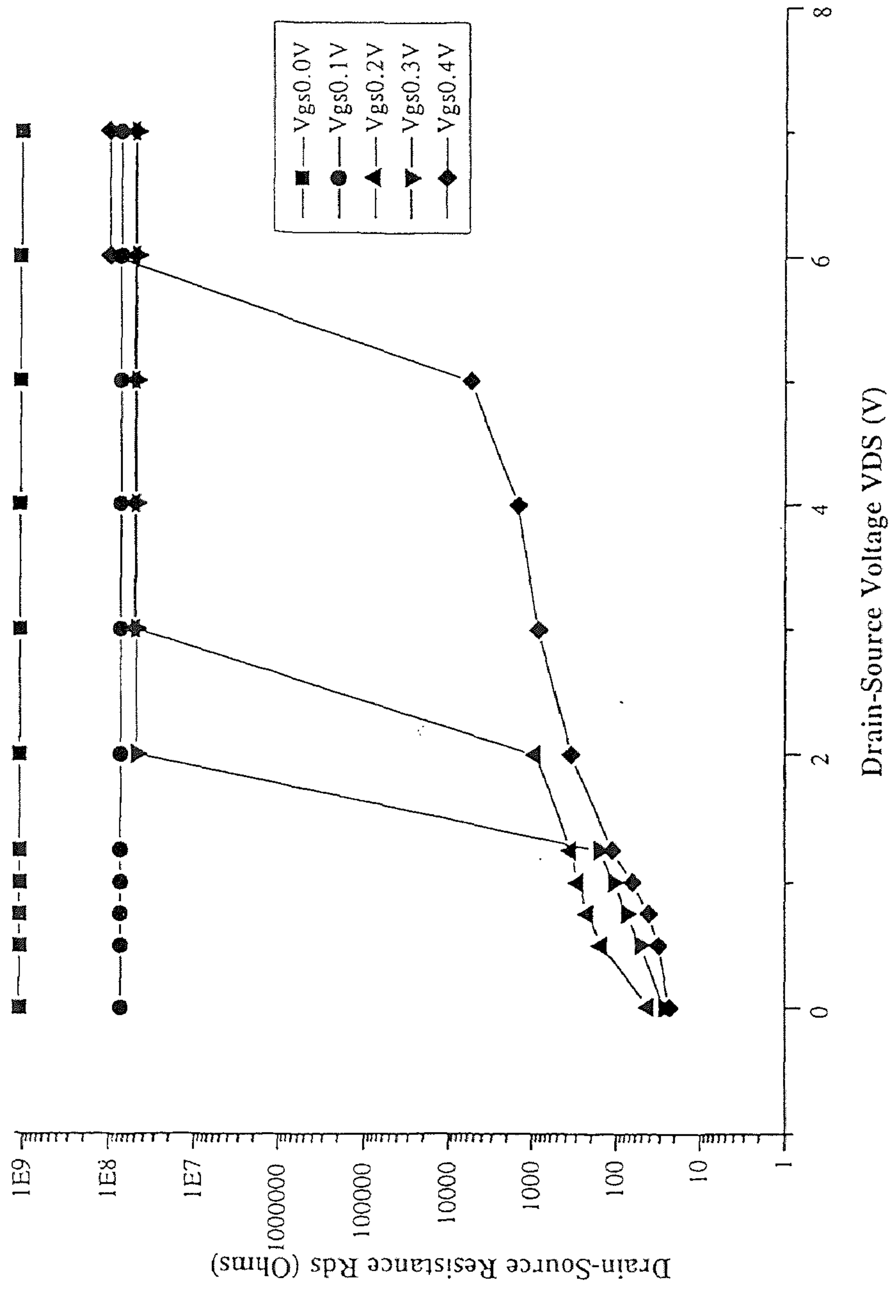


Figure 4.9(e) Drain-source resistance R_{ds} bias dependent characteristics.

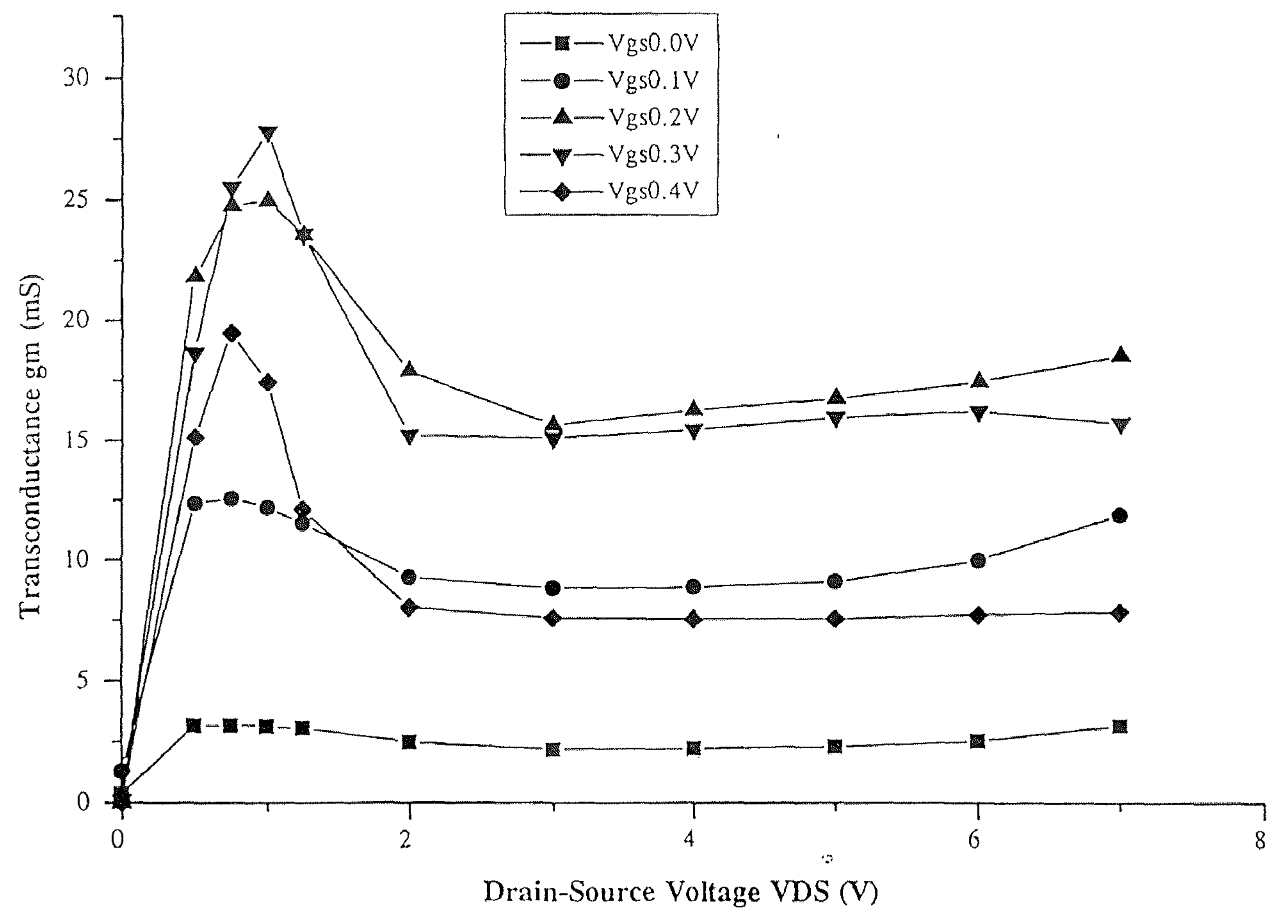


Figure 4.9(f) Transconductance g_m bias dependent characteristics.

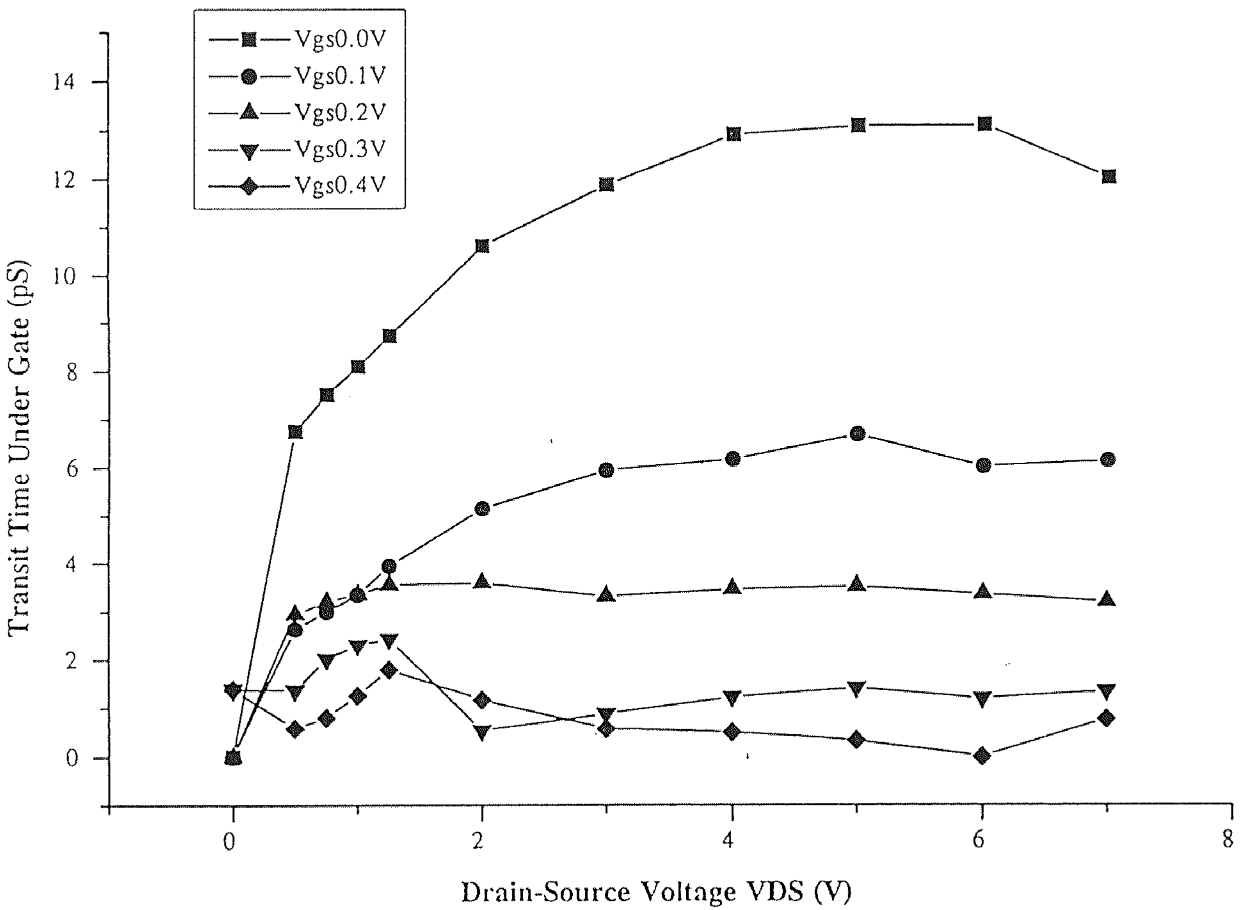


Figure 4.9(g) Delay time τ bias dependent characteristics.

Fig.4.9(c) shows that the feedback capacitance C_{dg} decreases sharply as V_{ds} approaches saturation voltage $V_{DS,SAT}$. This reduction is the evidence of charge accumulation at channel edge of the gate. C_{dg} in the saturation region is almost independent of V_{gs}. Also, it is very small in value. A constant C_{dg} is thus assumed in a MESFET large-signal model. Capacitance C_{ds} in Fig.4.9(d) is less dependent on V_{ds}. It is also very small in value. The dependence on V_{gs} can be neglected. C_{ds} is thus treated as a constant in a large-signal model.

Fig.4.9(b) shows that R_i is a strong function of V_{gs} in saturation region . It decreases as V_{gs} increases, and is less dependent on V_{ds}. An empirical equation described R_i as function of V_{gs} is given by

$$R_i = \frac{R_{i0}}{1 + \frac{V_{gs}}{B}} \tag{33}$$

R_{ds} in Fig.4.9(e) is seen to be the function of both V_{gs} and V_{ds}. It decreases as V_{gs} increases, and increases as V_{ds} increases.

g_m in Fig.4.9(f) is a strong function of V_{gs} but is less dependent on V_{ds}. τ in Fig.4.9(g) decreases as V_{gs} increases since the MESFET is kept turned-on. Also it is less dependent on V_{ds}.

4.4 Element Bias-Dependent Functions

The small-signal S-parameter optimization in Section 4.3 provides the results of circuit elements as functions of bias voltages V_{gs} and V_{ds}. It is also shows that the most bias dependent elements are C_{gs}, R_i, R_{ds}, g_m and τ (related to Ids current source). The mathematical dependence functions for the elements must be available for the construction of a Willing type large-signal model. These functions can be obtained by curve fitting technique.

The method used here was slightly different from traditional Willing curve fitting technique. Instead of purely relying on polynomial curve fitting, empirical equations for the elements were used. ORIGIN curve-fitting software was applied as the fitting tool. The empirical equations were fed into the software, and the fitting parameters could be found.

It has been shown in Section 4.3 that C_{gs} and R_i are the functions of V_{gs} only. The empirical equations for these two parameters are repeated here

$$C_{gs} = \frac{C_{gs0}}{(1 - \frac{V_{gs}}{V_{TO}})^m} \tag{34}$$

$$R_i = \frac{R_{i0}}{1 + \frac{V_{gs}}{B}} \tag{35}$$

As for the drain current source I_{ds}, a modified Curtice equation was developed for the curve fitting.

The Curtice quadratic model equation is given as

$$I_{ds} = \beta_1 (V_{gs} - V_{TO})^2 (1 + \lambda V_{ds}) \tanh(\alpha V_{ds}) \tag{36}$$

where V_{TO} is the threshold voltage of the MESFET. β_1, λ, and α are the fitting parameters determined by DC-measurement.

The Curtice cubic model equation is given as:

$$I_{ds} = (A_0 + A_1 V_1 + A_2 V_1^2 + A_3 V_1^3) \tanh(\gamma V_{ds}) \tag{37}$$

where

$$V_1 = V_{gs} [1 + \beta_2 (V_{ds0} - V_{ds})] \tag{38}$$

and V_{dso} is the drain-source voltage where parameters A_0, A_1, A_2 and A_3 are evaluated.

Eq.(36) can not describe I_{ds} behavior in high I_{ds} region accurately, while Eq.(37) can not describe I_{ds} behavior accurately in high V_{ds} region. A modified Curtice empirical equation that combines Eq.(36) and Eq.(37) was found to be quite accurate:

$$I_{ds} = \beta_1 (A_0 + A_1 V_{gs} + A_2 V_{gs}^2 + A_3 V_{gs}^3) (1 + \lambda V_{ds}) \tanh(\alpha V_{ds}) \quad (39)$$

As for R_{ds}, it is equal to $1/g_{ds}$, where g_{ds} is given by

$$g_{ds} = \left. \frac{\partial I_{ds}}{\partial V_{ds}} \right|_{V_{gs}} \quad (40)$$

which is equal to

$$g_{ds} = \beta_1 (A_0 + A_1 V_{gs} + A_2 V_{gs}^2 + A_3 V_{gs}^3) (\lambda \tanh(\alpha V_{ds}) + \alpha(1 + \lambda V_{ds}) / \cosh(\alpha V_{ds})) \quad (41)$$

Eq.(34), (35), (39) and (41) are the bias dependent functions which will be used for curve fitting to construct a large-signal model.

By using ORIGIN curve-fitting software and fitting Eq.(34) and Eq.(35) to the data obtained from Fig.4.9(a) and Fig.4.9(b) at V_{ds}=3.0V, the bias-dependent functions of C_{gs} and R_i for R240522 can be found as

$$C_{gs} = \frac{0.309}{(1 - \frac{V_{gs}}{0.75})^{1.294}} \quad (42)$$

$$R_i = \frac{16.02}{1 + \frac{V_{gs}}{0.215}} \quad (43)$$

As for I_{ds}, the experimental data is the one shown in Fig.4.1. HP85150B MDS was used to accomplish the fitting. A "curve-tracer" as shown in

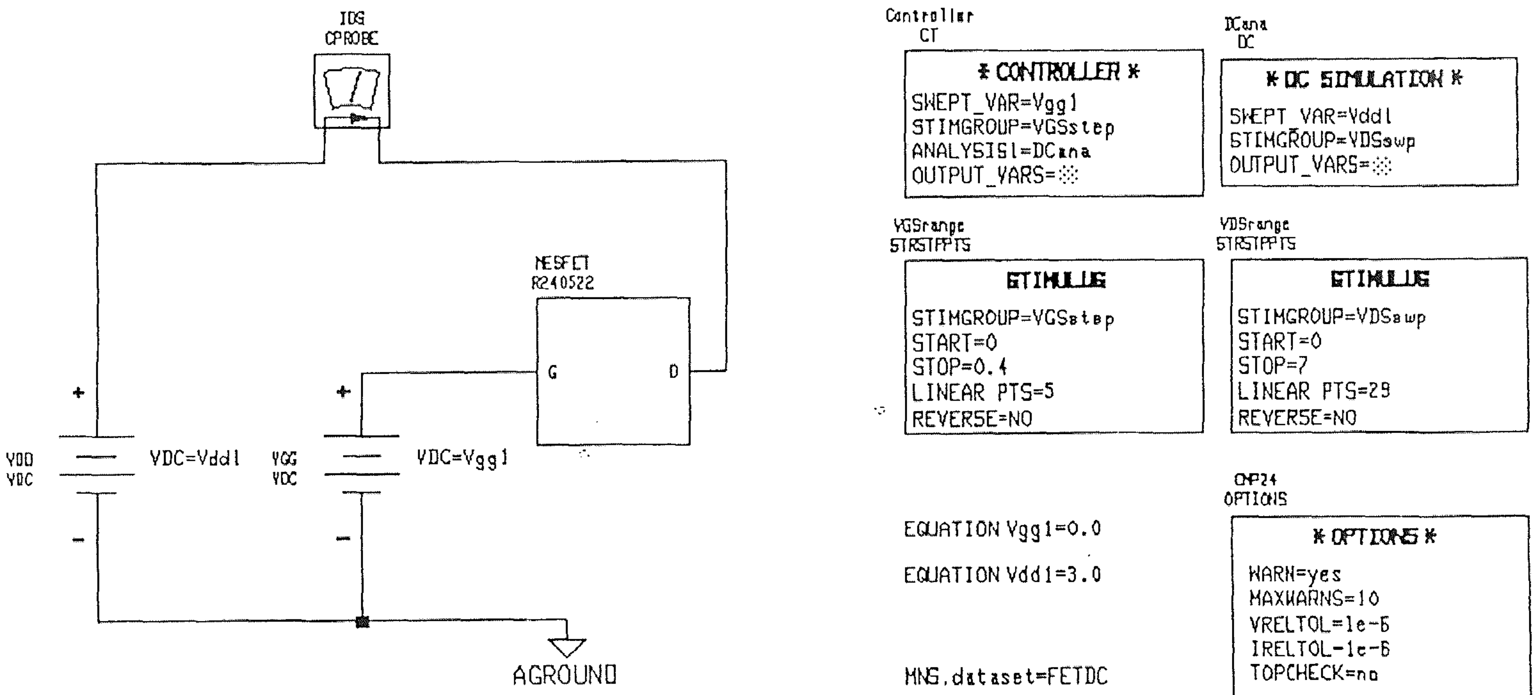


Figure 4.10 MESFET "curve-tracer" setup in HP85150B MDS. The MESFET output characteristics can be "measured" by this setup.

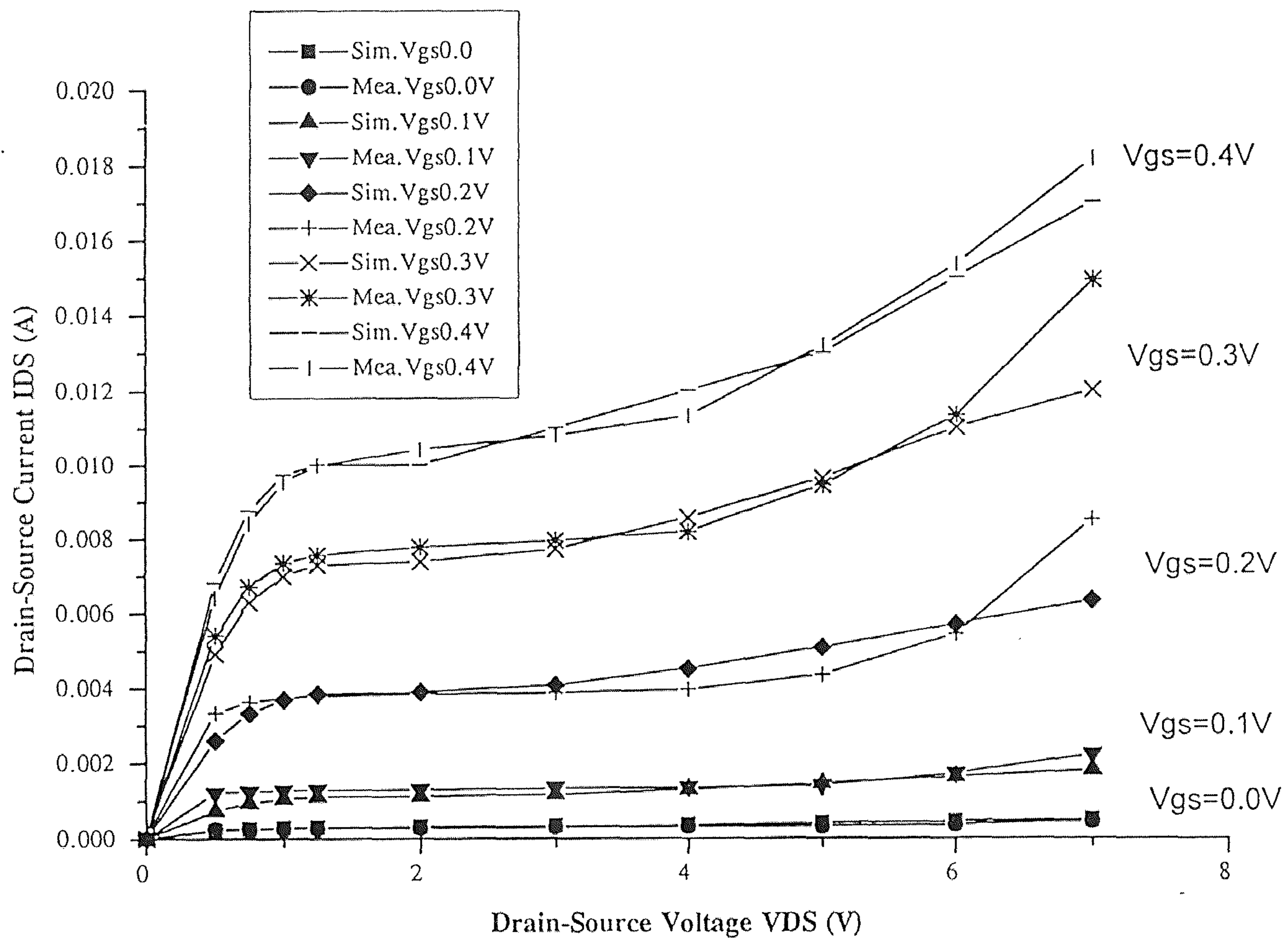


Figure 4.11 Simulated and measured MESFET R240522 output characteristics comparison. Good match is obtained.

Fig.4.10 was first built into a design icon. The constructed MESFET large-signal model was then "measured" by this "curve-tracer". By slightly adjusting the fitting parameters in Eq.(39), the simulated output I_{ds}-V_{ds} characteristics was matched reasonably well with Fig.4.1. The result is shown in Fig.4.11. The bias dependent function of I_{ds} for R240522 is then given by

$$I_{ds} = 0.46(\, 0.0003218 - 0.00675\, V_{gs} + 0.17427\, V_{gs}^{2} - 0.22933 V_{gs}^{3}\,)\,(\, 1 + 0.1676\, V_{ds}\,) \tanh(\, 1.50\, V_{ds}\,) \tag{44}$$

where A_0, A_1, A_2, A_3 are determined from curve fitting of the I_{ds}-V_{gs} data in Fig.4.1 at V_{ds}=3.0V. The parameters to be adjusted in the "curve-tracer" are β_1 , λ , and α.

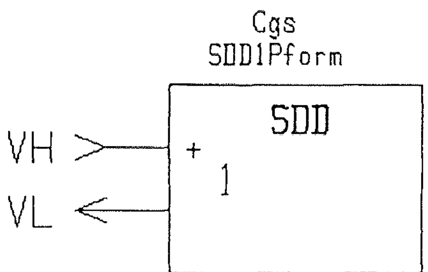
4.5 Large-Signal Model For MESFET R240522

A Willing type large-signal model of MESFET R240522 can finally be built based upon all the constant element values have been determined, as well as Eq.(42), (43), (44) and (41) for the bias dependent elements C_{gs}, R_i, I_{ds}, and R_{ds}. In order to have the bias dependent elements included in the model, a symbolically-defined device (SDD) in HP85150B MDS was used.

SDD is such a device by which the user can use an equation to specify the terminal current and voltage relationship of the device. This is just suitable for the construction of the bias dependent elements of a Willing large-signal model. Especially, the following formula are needed for a voltage-dependence capacitor:

since
$$I(t) = \frac{\partial Q}{\partial t} = (\frac{\partial C}{\partial V}\frac{\partial V}{\partial t})\, V(t) + C(V)\,(\frac{\partial V}{\partial t}) \tag{45}$$

so
$$I(t) = \frac{\partial V}{\partial t}(V\frac{\partial C}{\partial V} + C\,) \tag{46}$$



PORT CURRENTS

PORT	WT.FCN.	EXPRESSION = I
1	1	(_V1)*(0.309pF)*(1-_V1/0.75)^(-1.294)*(1+_V1*1.294/(0.75*(1-_V1/0.75)))
1		

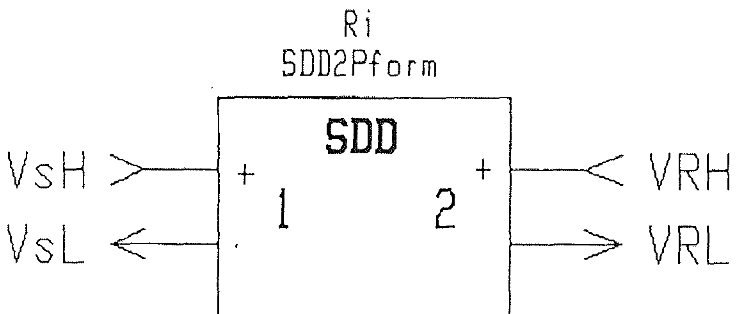
PORT I and V

PORT	WT.FCN.	EXPRESSION = 0
1		
1		
1		

WEIGHTING FUNCTIONS:

WT.FCN.	EXPRESSION

Figure 4.12 Symbolically-defined device (SDD) for C_{gs}. The bias dependent function is based on Eq.(42).



PORT CURRENTS

PORT	WT.FCN.	EXPRESSION = I
1	0	0.0
2	0	(_V2)/(16.02/(1+_V1/0.215))

PORT I and V

PORT	WT.FCN.	EXPRESSION = 0

WEIGHTING FUNCTIONS:

WT.FCN.	EXPRESSION

Figure 4.13 Symbolically-defined device (SDD) for R_i. The bias dependent function is based on Eq.(43).

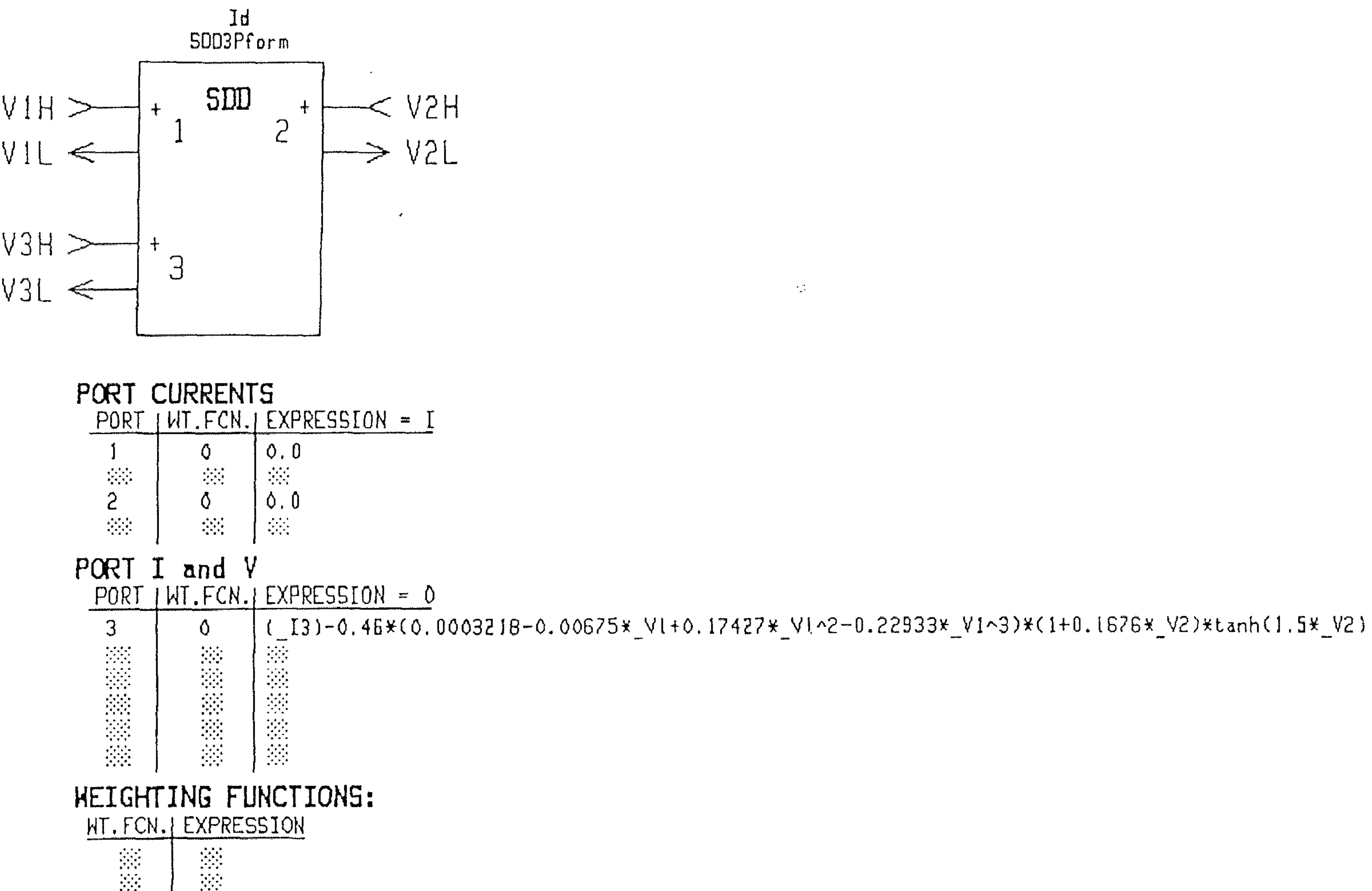
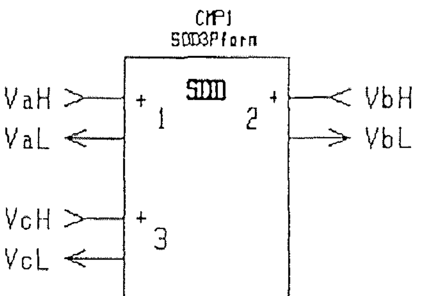


Figure 4.14 Symbolically-defined device (SDD) for I_{ds}. The bias dependent function is based on Eq.(44).



PORT CURRENTS

PORT	WT.FCN.	EXPRESSION - I
1	0	0.0
2	0	0.0
3	0	(_V2)*0.46*(0.000318-0.00675*_V1+0.17427*_V1^2-0.22933*_V1^3)*((0.1676)*tanh(1.5*_V2)+1.5*(1+0.1676*_V2)/cosh(1.5*_V2))

PORT I and V

PORT	WT.FCN.	EXPRESSION - 0

WEIGHTING FUNCTIONS:

WT.FCN.	EXPRESSION

Figure 4.15 Symbolically-defined device (SDD) for R_{ds}. The bias dependent function is based on Eq.(41).

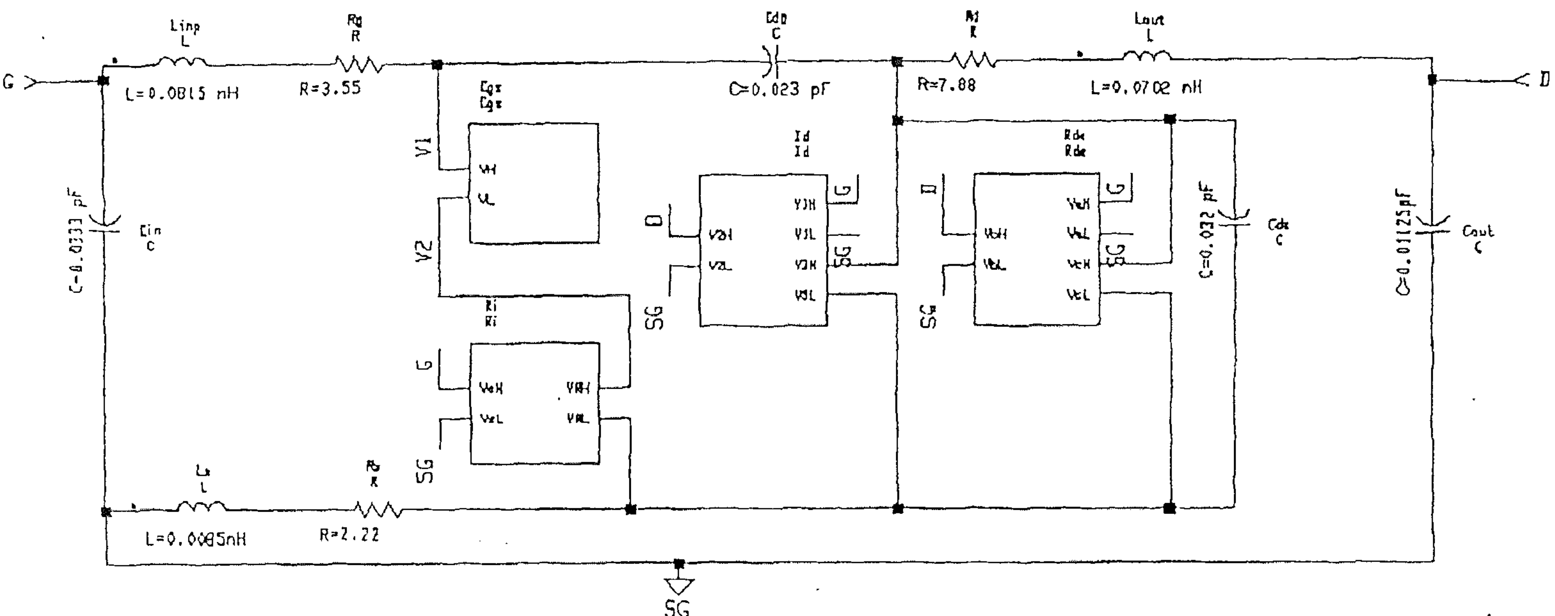


Figure 4.16 MESFET R240522 large-signal equivalent circuit model. The four bias dependent elements are represented by the SDDs.

In frequency domain, $\partial/\partial t$ can be replaced by $j\omega$. The terminal current for C_{gs} of Eq.(34) is then given by

$$I_{cgs} = \frac{j\,\omega V_{gs}\,C_{gs0}}{(1-\frac{V_{gs}}{V_{TO}})^{m}}\,(1+\frac{m\,V_{gs}}{V_{TO}\,(1-\frac{V_{gs}}{V_{TO}})}) \qquad (47)$$

The symbolically-defined device (SDD) for C_{gs}, R_i, I_{ds}, and R_{ds} is shown in Fig.4.12, Fig.4.13, Fig.4.14, and Fig.4.15, respectively. The final large-signal model for R240522 is shown in Fig.4.16. The four SDDs have been incorporated into the model.

Chapter 5

MICROWAVE GaAs MESFET NONLINEARITY SIMULATION AND MEASUREMENT

The construction of a MESFET R240522 large-signal model has been completed. The nonlinearity of the MESFET can now be simulated by HP85150B Microwave Design System. The simulation results will be compared with practical intermodulation measurements. The model accuracy will then be verified.

5.1 Intermodulation Measurement Setup in HP 85150B MDS

Fig.5.1 is the MESFET intermodulation measurement setup in HP85150B Microwave Design System where no external matching circuits are included. The MESFET is connected directly to 50Ω line. This allows the output information directly related to the MESFET rather than the matching circuits. Two equal amplitude fundamental input signals f_1=0.83GHz and f_2=0.84GHz are combined to the input. The bias point is V_{gs}=+0.2V and V_{ds}=3.0V. Total power dissipated is 12.22 mW. The input power level is specified to vary continuously.

Instead of measuring the power directly, the node voltages V_{out} and V_{in} on output and input terminals are measured. This is accomplished by placing a voltage probe at the node of interest. In HP85150B MDS, this probation is simply realized by putting a wire label at the corresponding position.

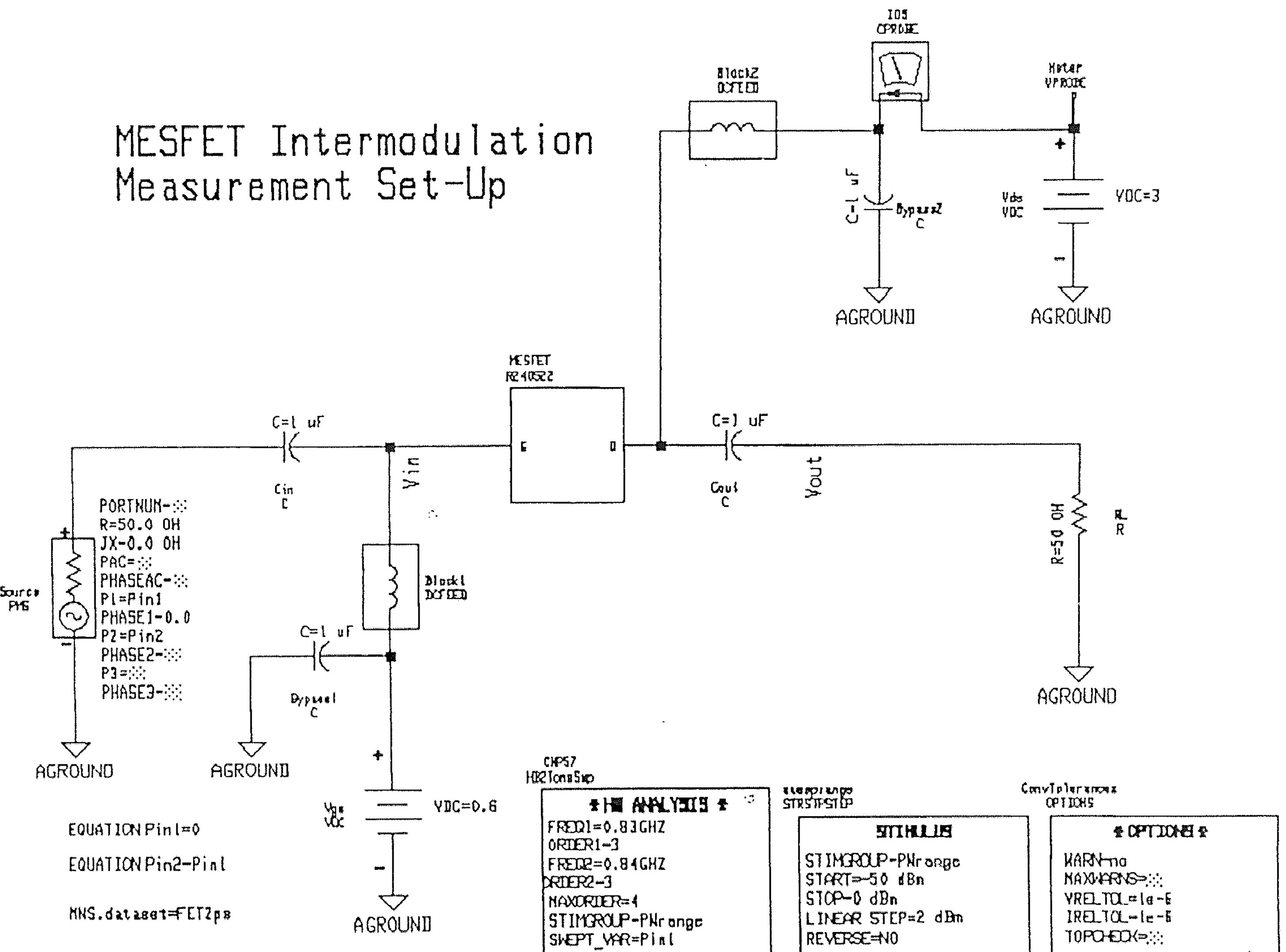


Figure 5.1 MESFET intermodulation measurement setup in HP85150B Microwave Design System. The frequencies of the two fundamentals are f_1=0.83 GHz and f_2=0.84GHz. The input power P_i is swept continuously.

The voltage probed is a peak voltage. The related average power is given by

$$P_{out} = \frac{V_{out}^{2}}{2\,R_{out}} \tag{48}$$

If the unit of the power is in dBm, it will relate to the voltage by

$$P_{out}\,(dBm) = 10\,Log\,(\,1000 \times \frac{V_{out}^{2}}{2\,R_{L}}\,) \tag{49}$$

For a load impedance of 50Ω

$$P_{out}\,(dBm) = 10 + dB(\,V_{out}\,) \tag{50}$$

Power gain is defined as

$$G_{p}\,(dB) = P_{o}\,(dBm) - P_{i}\,(dBm) \tag{51}$$

Gain compression is defined as

$$Compression\,(dB) = G_{p}\,(at\ lower\ power\,) - G_{p}\,(\,at\ higher\ power\,) \tag{52}$$

Third-order intercept point power TOI is given by Eq.(1) and is rewritten here

$$TOI\ (dBm) = P_{o} + (\,P_{o} - P_{IMD3}\,)\,/\,2 \tag{53}$$

The power added efficiency is defined as

$$PAE\ (\%) = \frac{P_{o}\,(mW) - P_{i}\,(mW)}{P_{dc}\,(mW)} \tag{54}$$

It is clear that as long as voltage V_{out} is probed, all the parameters related to the nonlinearity of a MESFET can be displayed by the software.

5.2 Simulation and Measurement Results

Fig.5.2 is a demonstration of the output power spectra. Many IMD products are observed in the figure. The two input signals f_1 and f_2 were chosen at 700MHz and 800MHz rather at 0.83 GHz and 0.84 GHz to separate the intermodulation products from the fundamental signals even further.

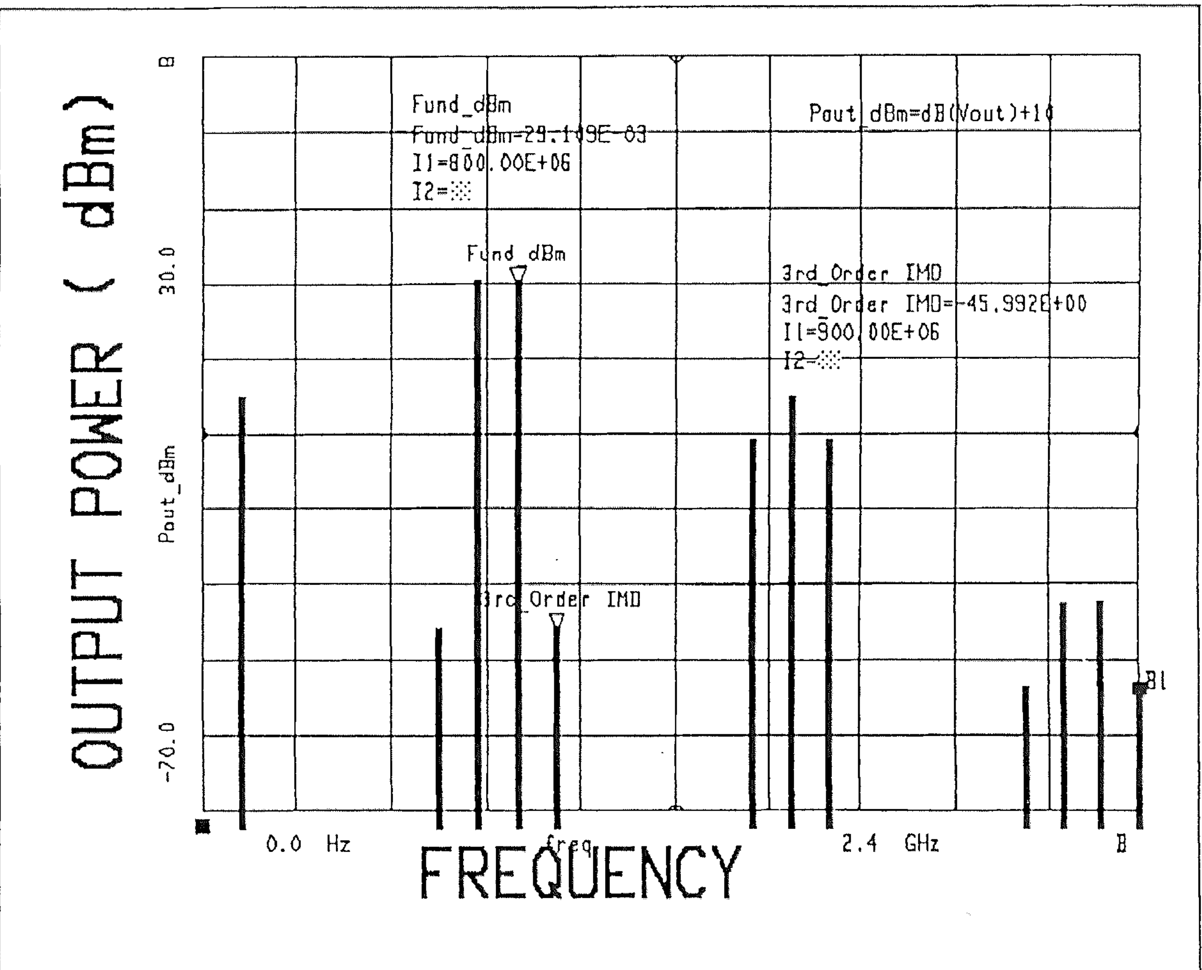


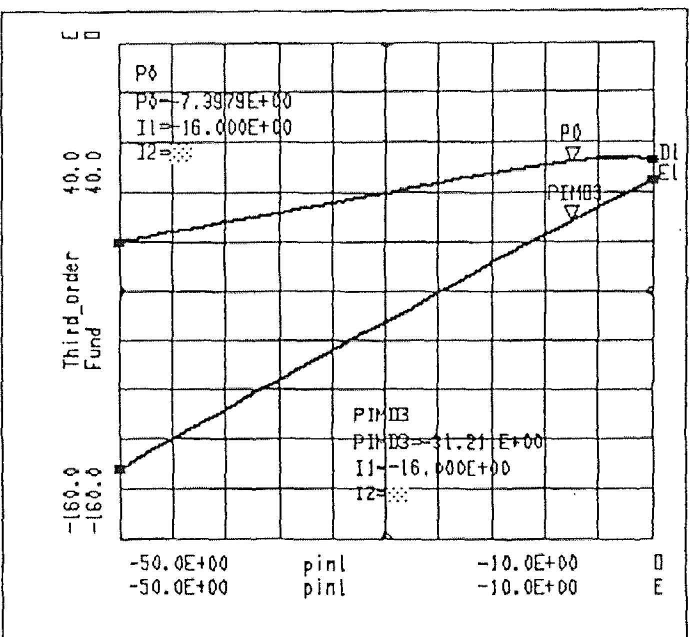
Figure 5.2 Simulated MESFET R240522 output power spectra. f_1=0.70GHz and f_2=0.80GHz are chosen in this figure. The intermodulation products can be observed more clearly.

Dataset-FET2ps Qualifier-░

Pout_dBn=dB(Vout)+10
Fund=dB(Vout[x,5])+10
Third_order=dB(Vout[*,4])+10

Gain=Fund-Pin1
Compression=Gain[1]-Gain[*]
TOI=Fund+(Fund-Third_order)/2
Pdc=1000*(VDS[5,1])*(IDS.i[5,1])

Po=EXP(LN10*(Fund/10))
Ps=EXP(LN10*(Pinl/10))
PAE=100*(Po-Ps)/MAG(Pdc)



TOI	Pin1	KEY1[x,5]
6.421	-50.000	1.000
6.421	-48.000	2.000
6.420	-46.000	3.000
6.419	-44.000	4.000
6.417	-42.000	5.000
6.415	-40.000	6.000
6.411	-38.000	7.000
6.404	-36.000	8.000
6.393	-34.000	9.000
6.376	-32.000	10.000
6.349	-30.000	11.000
6.307	-28.000	12.000
6.239	-26.000	13.000
6.131	-24.000	14.000
5.959	-22.000	15.000
5.683	-20.000	16.000
5.237	-18.000	17.000
4.509	-16.000	18.000
3.293	-14.000	19.000
1.190	-12.000	20.000
-2.701	-10.000	21.000

freq	Key2[5,x]
0.000	1.000
10000000.	2.000
20000000.	3.000
820.0E+06	4.000
830.0E+06	5.000
840.0E+06	6.000
850.0E+06	7.000
1.650E+09	8.000
1.660E+09	9.000
1.670E+09	10.000
1.680E+09	11.000
1.690E+09	12.000
2.490E+09	13.000
2.500E+09	14.000
2.510E+09	15.000
2.520E+09	16.000
3.330E+09	17.000
3.340E+09	18.000
3.350E+09	19.000

Pdc	IDS.i[5,1]	VDS[5,1]
12.221+j0.000	4.07E-03+j0.000	3.000+j0.000

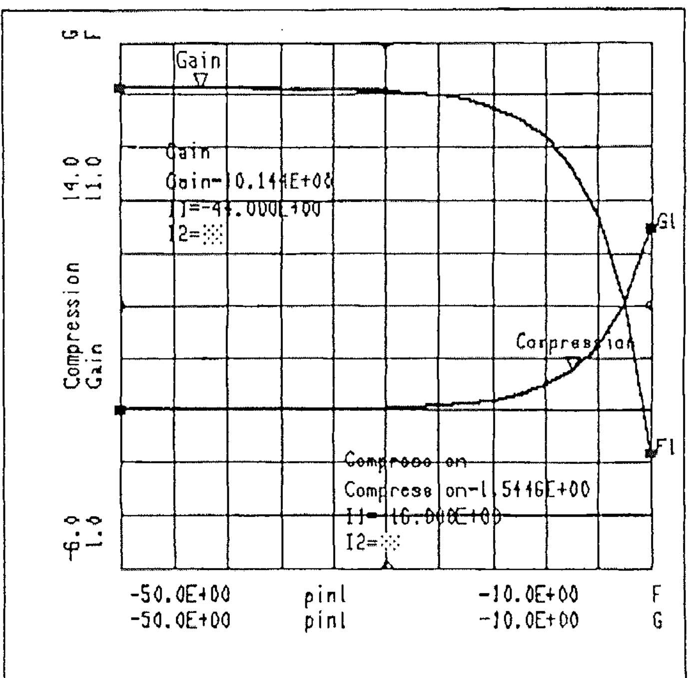
Figure 5.3 Simulated MESFET R240522 power transfer characteristics. The 3rd-order IMD power is also shown. P1dB is about -7.4 dBm. The bias voltages are V_{gs}=+0.2V and V_{ds}=3.0V.

Dataset-FET2ps Qualifier-░

Pout_dBm=dB(Vout)+10
Fund=dB(Vout[x,5])+10
Third_order=dB(Vout[*,4])+10

Gain-Fund-Pin1
Compression=Gain[1]-Gain[*]
TOI-Fund+(Fund-Third_order)/2
Pdc=1000*(VDS[5,1])*(IDS.i[5,1])

Pa=EXP(LN10*(Fund/10))
Ps=EXP(LN10*(Pin1/10))
PAE-100*(Po-Ps)/MAG(Pdc)



TOI	Pin1	KEY1[x,5]	freq	Key2[5,x]
6.421	-50.000	1.000	0.000	1.000
6.421	-48.000	2.000	10000000.	2.000
6.420	-46.000	3.000	20000000.	3.000
6.419	-44.000	4.000	820.0E+06	4.000
6.417	-42.000	5.000	830.0E+06	5.000
6.415	-40.000	6.000	840.0E+06	6.000
6.411	-38.000	7.000	850.0E+06	7.000
6.404	-36.000	8.000	1.650E+09	8.000
6.393	-34.000	9.000	1.660E+09	9.000
6.376	-32.000	10.000	1.670E+09	10.000
6.349	-30.000	11.000	1.680E+09	11.000
6.307	-28.000	12.000	1.690E+09	12.000
6.239	-26.000	13.000	2.490E+09	13.000
6.131	-24.000	14.000	2.500E+09	14.000
5.959	-22.000	15.000	2.510E+09	15.000
5.683	-20.000	16.000	2.520E+09	16.000
5.237	-18.000	17.000	3.330E+09	17.000
4.509	-16.000	18.000	3.340E+09	18.000
3.293	-14.000	19.000	3.350E+09	19.000
1.190	-12.000	20.000		
-2.701	-10.000	21.000		

Pdc	IDS.i[5,1]	VDS[5,1]
12.221+j0.000	4.07E-03+j0.000	3.000+j0.000

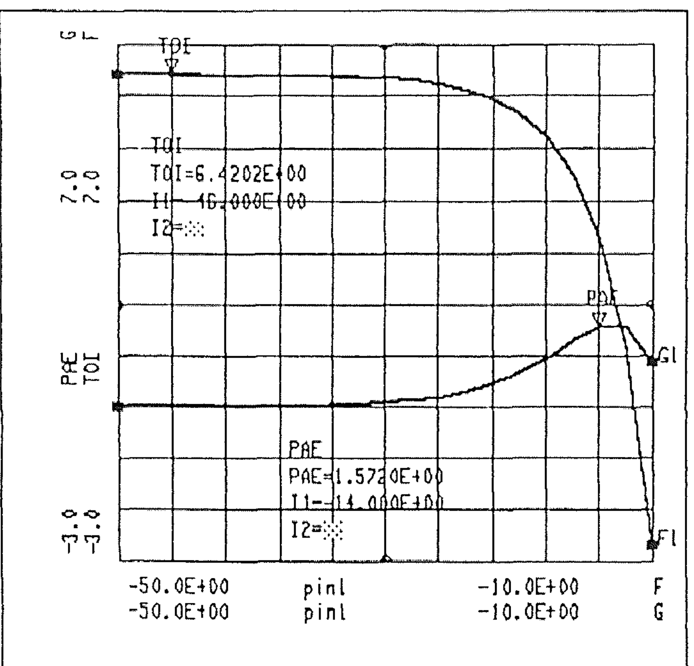
Figure 5.4 Power gain and gain compression simulation results. The power gain is equal to 10.14 dB. The bias voltages are V_{gs}=+0.2V and V_{ds}=3.0V.

Dataset-FET2ps Qualifier-

Pout_dBm=dB(Vout)+10
Fund=dB(Vout[*,5])+10
Third_order=dB(Vout[*,4])+10

Gain-Fund-Pin1
Compression=Gain[1]-Gain[*]
TOI-Fund+(Fund-Third_order)/2
Pdc=1000*(VDS[5,1])*(IDS.i[5,1])

Pa=EXP(LN10*(Fund/10))
Ps=EXP(LN10x(Pinl/10))
PAE-100*(Po-Ps)/MAG(Pdc)



TOI	Pinl	KEY1[*,5]
6.421	-50.000	1.000
6.421	-48.000	2.000
6.420	-46.000	3.000
6.419	-44.000	4.000
6.417	-42.000	5.000
6.415	-40.000	6.000
6.411	-38.000	7.000
6.404	-36.000	8.000
6.393	-34.000	9.000
6.376	-32.000	10.000
6.349	-30.000	11.000
6.307	-28.000	12.000
6.239	-26.000	13.000
6.131	-24.000	14.000
5.959	-22.000	15.000
5.683	-20.000	16.000
5.237	-18.000	17.000
4.509	-16.000	18.000
3.293	-14.000	19.000
1.190	-12.000	20.000
-2.701	-10.000	21.000

freq	Key2[5,*]
0.000	1.000
10000000.	2.000
20000000.	3.000
820.0E+06	4.000
830.0E+06	5.000
840.0E+06	6.000
850.0E+06	7.000
1.650E+09	8.000
1.660E+09	9.000
1.670E+09	10.000
1.680E+09	11.000
1.690E+09	12.000
2.490E+09	13.000
2.500E+09	14.000
2.510E+09	15.000
2.520E+09	16.000
3.330E+09	17.000
3.340E+09	18.000
3.350E+09	19.000

Pdc	IDS.i[5,1]	VDS[5,1]
12.221+j0.000	4.07E-03+j0.000	3.000+j0.000

Figure 5.5 Third-order intercept point power TOI and power added efficiency PAE simulation results. TOI=6.421 dBm. The highest PAE is equal to 1.6%. The bias voltages are V_{gs}=+0.2V and V_{ds}=3.0V. P_{dc}=12.22mW.

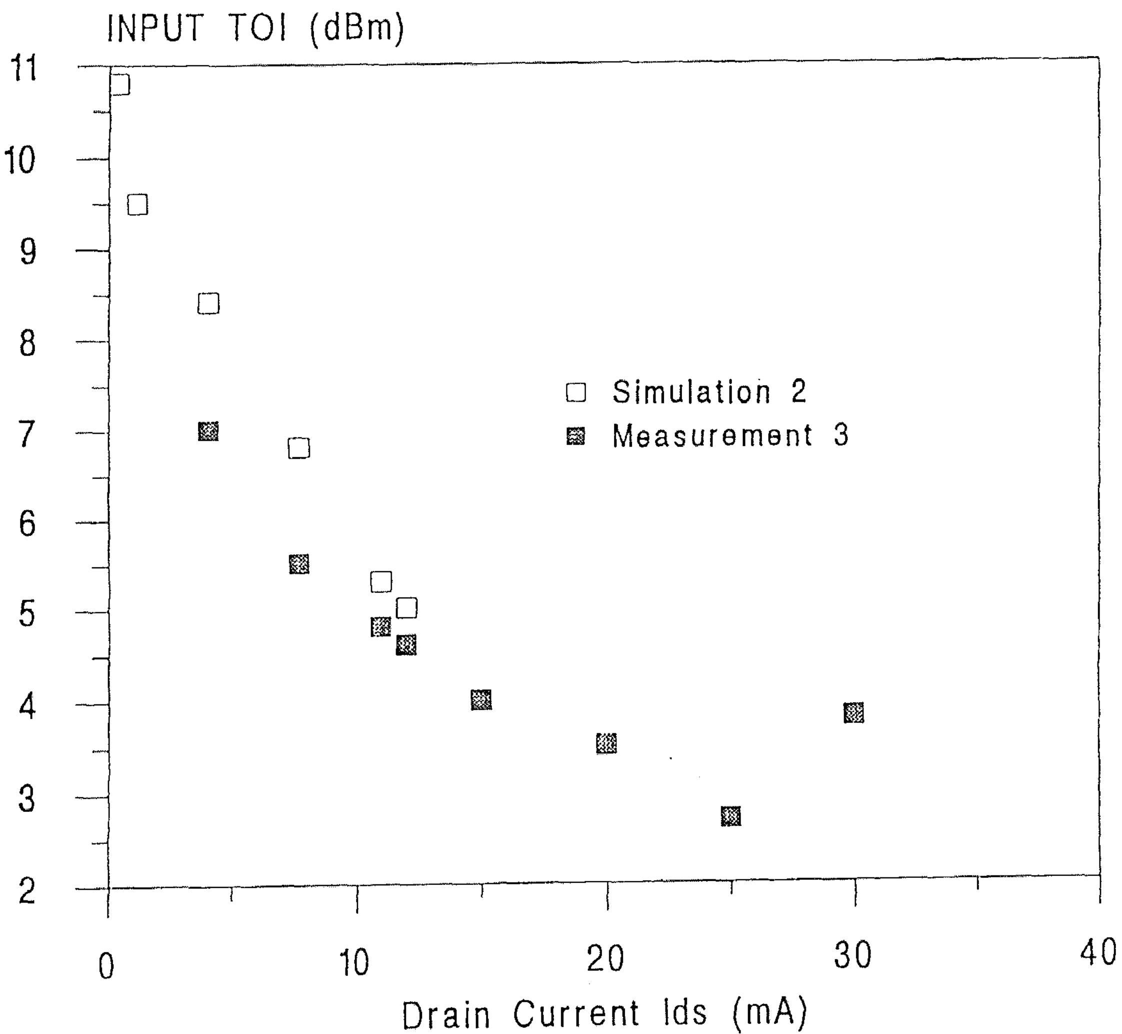


Figure 5.6 Simulated and measured result comparison for input TOI as function of I_{ds}. The results show that the linearity of the MESFET becomes worse at higher I_{ds}. The drain voltage was set to V_{ds}=3.0V.

Fig.5.3 shows the simulated power transfer characteristics for the fundamental signal and third-order intermodulation signal. The 1dB compression point is about -7.4 dBm at bias point of V_{gs}=+0.2V and V_{ds}=3.0V. This MESFET is thus a small power device.

Fig.5.4 shows the simulated power gain and gain compression at the same bias voltages. The power gain at lower input power level is 10.14dB. It drops as input power level increases since the output power is compressed at higher input power level.

Fig.5.5 shows the third-order intercept point power TOI and power added efficiency PAE as functions of input power level. The TOI at low power level (flat region) should be taken as the correct TOI since it is in linear region and the linear extrapolation of the fundamental and third-order IMD curves at this region will give a more reliable value of TOI. The power added efficiency PAE is quite small. The peak value is only at about 1.6%. The small PAE indicates that the device is operated in a class-A state.

Practically, the input TOI is also measured to characterize a MESFET since it is more easily measured practically. As mentioned before, the g_m nonlinearity or I_{ds} nonlinearity is the most important nonlinear source in a MESFET. Therefore, TOI as function of I_{ds} is usually measured to demonstrate the MESFET nonlinearity. Fig.5.6 shows the simulation result for input TOI as function of I_{ds}. The linearity is better at lower I_{ds} while it is worse at higher I_{ds}. This is partially due to the input impedance matching. MESFET is a high input impedance device. It matches well when the device is turned-on more. And the nonlinear components will transfer to the source resistance more easily. As a comparison, the actual input TOI measurement result for a device on the same wafer is also shown in the figure. Reasonable match is obtained. The measured device is a 800μm gate width device and

has higher current capability, while the gate width of the simulated device is only 200μm, it can not operated into higher I_{ds} region. However, the same variation trend is obtained and the match is reasonable well. This proves the success of the large-signal MESFET model construction.

Chapter 6

CONCLUSIONS

In summary, the construction of a 0.5μm gate length ion-implanted microwave GaAs MESFET large-signal equivalent circuit model by HP85150B Microwave design System has been investigated. The large-signal model is based upon the optimization of small-signal S-parameter measurement and DC measurement. The nonlinear behavior of the MESFET is represented by four bias-dependent elements in the model. The symbolically-defined-device (SDD) allows the inclusion of such bias dependent elements in the model equivalent circuit. The simulation of the MESFET intermodulation characteristics by HP85150B Microwave Design System has been successful. The third-order intermodulation intercept simulation results match reasonably well with the measurement data. The probing of the terminal voltages V_{in} and V_{out} provides the necessary information about all the possible spurious emission products at input and output of the MESFET. The power transfer characteristic provides key parameters for the characterization of a linear MESFET. These parameters are 1-dB compression point output power P_{1dB} and third-order intercept point power TOI. The power gain G_p, power added efficiency (PAE), and power compression can all be determined from the transfer characteristics.

This thesis research was based upon the basic understanding of the nonlinear theory, MESFET modeling techniques, and a powerful CAD tool. A large amount of work has been spent on the construction of a large-signal model since the bias dependent functions must be obtained by the optimization of large sets of small-signal S-parameters under various bias

conditions and frequency ranges. Finally, the basis for a MESFET physics-based analytical large-signal model was provided in Appendix . This model is highly desirable by a transistor design engineer. To foresee the microwave performance as function of design geometrical and material parameters of a MESFET is the future goal for a transistor or MMIC designer in the foundry.

Appendix

GaAs MESFET Physics-Based Large-Signal Model

As a microwave transistor or MMIC design engineer, it is highly desirable to predict the microwave performance at design stage. The model employed for the nonlinearity analysis above, however, was obtained from measurement of S-parameters and DC-characteristics, and it has little to do with the device geometrical and material parameters. The designer will be very uncertain about the outcome of the design parameters chosen. Physics-based large-signal GaAs MESFET analytical model provides an opportunity.

The two-dimensional GaAs MESFET physics-based model [4-7] is based upon the following charge transport equation in the channel:

Poisson's equation $$\nabla^2 \psi \equiv -\frac{q}{\varepsilon_o \varepsilon_r}\left[N_d(y) - n(x,y)\right] \qquad (A.1)$$

Conduction Current $$\vec{J} \equiv -q\,n\,\vec{v} + q\,D\,\nabla n \qquad (A.2)$$

Current continuity equation $$\nabla \cdot \vec{J} \equiv q\,\frac{\partial n}{\partial t} \qquad (A.3)$$

Total current $$\vec{J}t \equiv \vec{J} + \varepsilon_o\,\varepsilon_r\,\frac{\partial \vec{E}}{\partial t} \qquad (A.4)$$

and $$\vec{E} \equiv -\nabla\,\psi \qquad (A.5)$$

$$\vec{v} \equiv -\mu(E)\,\vec{E} \qquad (A.6)$$

where $\vec{E} \equiv -\nabla\,\psi$ is the electrical field, ψ the electrical potential, q the electron charge, $\varepsilon_o\,\varepsilon_r$ the permitivity of the GaAs channel material, N_d the

donor concentration in the channel, n the free electron density, $\vec{J}$ the conduction current density (drift + diffusion), $\vec{J}_t$ the total current density (conduction + displacement current), and $\mu(E)$ the electron mobility which is dependent on the electrical field in the channel.

The above equations should have been solved for ψ and $\vec{J}$ by numerical techniques. But the numerical solution approach is very time consuming and not suitable for the circuit simulation application. An analytical solution was then developed which speeds up the simulation substantially.

To solve the equations above analytically, the device dimensions and doping profile should be given. The gate and drain bias voltages will be given as boundary conditions. The velocity-electric field relation $\vec{v} \equiv -\mu(E)\vec{E}$ should be also given. If potential ψ is solved, current $\vec{J}$ will be also known.

In order to solve for ψ, $N_d(y)$ and $n(x,y)$ in Eq.(A.1) should be first determined. The $N_d(y)$ is determined from ion-implantation doping profile which can be arbitrary. This profile could be found by C-V measurement. By least-square fit to this measurement data, an analytical function for $N_d(y)$ is found.

To derive an analytical expression for $n(x,y)$, it should be first noticed that the MESFET active region under the gate is subdivided into three parts as shown in Fig.A.1: a depletion region right under the Schottky barrier gate where n=0; a conducting channel region near the buffer layer where $n = N_d$; and a transition region in which $n(x,y)$ varies smoothly from 0 to N_d along the y-direction.

Since the numerical solutions to Eq.(A.1)-Eq.(A.6) can give a free electron density distribution $n(x,y)$, an analytical expression for $n(x,y)$ in

the transition region can be found by curve fitting these numerical solution results as given by Khatibzadeh et al [6] :

$$n(x,y) = N(y)\left[1+\gamma(x-L_1)\right]T(d(x),y) \tag{A.7}$$

where L_1 denotes the separation point between the linear and saturation region. The γ and L_1 can be determined from the boundary and bias conditions. And $T(d(x),y)$ is a transition function which is given by

$$T(d(x),y) = 1 - \frac{1}{1+\exp(\frac{y-d(x)}{\lambda})} \tag{A.8}$$

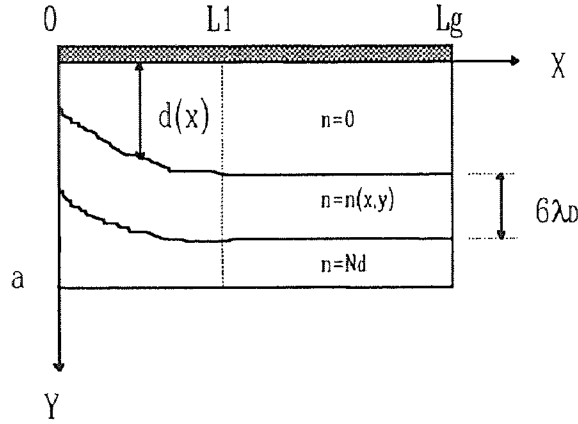


Figure A.1 The Three Parts in a MESFET Active Channel Region

With given $N_d(y)$ and $n(x,y)$, potential ψ can now be solved. Following Yamaguchi et al [4], the solution to Eq.(A.1) can be represented by a linear superposition of two components, i.e. $\psi = \psi_0 + \psi_1$, where ψ_0 is due to the impressed voltages on the electrodes, and ψ_1 is due to the space charge in the channel.

ψ_0 satisfies Laplace's equation with the following boundary conditions:

$$\nabla^2 \psi_0 = 0 \tag{A.9}$$

$$\psi_0(0,a)=0 \tag{A.10 a}$$

$$\psi_0(L,a)=V_0 \tag{A.10 b}$$

$$\frac{\partial \psi_0}{\partial y}(x,a)=0 \tag{A.10 c}$$

$$\psi_0(x,0)=0 \tag{A.10 d}$$

ψ_1 satisfies Poisson's equation with the following boundary conditions:

$$\nabla^2 \psi_1=-\frac{q}{\varepsilon_o\,\varepsilon_d}(N_d-n) \tag{A.11}$$

$$\psi_1(0,a)=0 \tag{A.12 a}$$

$$\psi_1(L,a)=V_1 \tag{A.12 b}$$

$$\frac{\partial \psi_1}{\partial y}(x,a)=0 \tag{A.12 c}$$

$$\psi_1(x,0)=V_{gs}-V_{bi} \tag{A.12 d}$$

where V_{bi} is the built-in voltage of the gate Schottky contact, V_{gs} is the applied gate-source voltage, and $V_{ds} = V_1 + V_0$ is the applied drain-source voltage.

Khatibzadeh shows that [6] the solution to Eq.(A.9) is given by

$$\psi_0(x,y)=\frac{V_0}{\sinh\left(\frac{\pi L_g}{2a}\right)}\sinh\left(\frac{\pi x}{2a}\right)\sin\left(\frac{\pi y}{2a}\right) \tag{A.13}$$

While the solution to Eq.(A.11) is dependent on the carrier concentration n:

$$\psi_1(x,y) = -\frac{q}{\varepsilon_o\,\varepsilon_r} F_1(d(x),y) + \frac{V_1}{L_g}x\ , \qquad 0 \le x \le L_1 \tag{A.14}$$

$$\psi_1(x,y) = -\frac{q}{\varepsilon_o\,\varepsilon_r} F_1(d_1,y) + \frac{V_1}{L_g}x + \frac{q}{\varepsilon_o\,\varepsilon_r}\gamma(x-L_1)\,F_2(d_1,x)\ , \qquad L_1 \le x \le L_g \tag{A.15}$$

where,
$$F_1(d(x),y) = \int_y^a \int_t^a [1 - T(d(x),\tau]\,N_d(\tau)\,d\tau\,dt \tag{A.16}$$

$$F_2(d_1,y) = \int_y^a \int_t^a T(d_1,\tau)\,N_d(\tau)\,d\tau\,dt \tag{A.17}$$

If d(x) and γ are known, F_1 and F_2 will also be known, and ψ_1 can be determined. Unfortunately, for the arbitrary doping profile in the channel, there is no analytical expression for d(x) available.

To solve d(x), apply Eq.(A.12 d) to Eq.(A.14), then

$$-\frac{q}{\varepsilon_o\,\varepsilon_r} F_1(d(x)) + \frac{V_1}{L_g}x = V_{gs} - V_{bi} \tag{A.18}$$

For any given x and V_{gs}, $F_1(d(x))$ can be tabulated numerically. And cubic spline interpolation can be used on the tabulated number to get d(x).

To determine γ, applying Eq.(A.12 d) to Eq.(A.15) yields

$$-\frac{q}{\varepsilon_o\,\varepsilon_r} F_1(d_1) + \frac{V_1}{L_g}x + \frac{q}{\varepsilon_o\,\varepsilon_r}\gamma(x-L_1)F_2(d_1) = V_{gs} - V_{bi} \tag{A.19}$$

Define a pinch-off voltage V_{po} at which the channel is completely pinch-off at the source side (x=0). If $V_{gs} = V_{po}$, $d(0) \rightarrow \propto$, and $n(0,y) \rightarrow 0$. From Eq.(A.14),

$$V_{p0} = V_{bi} - \frac{q}{\varepsilon_o\,\varepsilon_r}\int_0^a \int_t^a T(d_1,\tau)\,N_d(\tau)\,d\tau\,dt \tag{A.20}$$

From the definition of V_{p0} and $F_1(d)$, it follows that

$$F_2(d) = -\frac{\varepsilon_o\,\varepsilon_r}{q}(V_{p0} - V_{bi}) - F_1(d) \tag{A.21}$$

So if F_1 and V_{po} are known, F_2 will also be known. This leads to the determination of γ :

$$\gamma = -\frac{\varepsilon_o\,\varepsilon_r\,V_1}{q\,L_g\,F_2(d_1)} \tag{A.22}$$

$$(\gamma = 0, \text{ if } L_1 < x < L_g)$$

If $V_1 > 0$, and $\gamma < 0$, charge depletion in the channel occurs. If $V_1 < 0$, and $\gamma > 0$, charge accumulation in the channel occurs. V_1 can be determined from the channel continuity equation $I_d = I_s$ by iteration approach.

The input data for solving the above equations are the MESFET geometrical and material design parameters as well as bias voltages. The solutions will be in the form of instantaneous terminal (gate, source, and drain) current and voltage relations. Small-signal S-parameters or Y-parameters of the MESFET can be determined from these solutions. A commercially available physics-based MESFET simulator--FETPro by GaAsCode Ltd. has been released [13]. This simulator can provide MESFET S-parameter data and a bias dependent small-signal equivalent circuit model. The inputs to the simulator are the MESFET structural parameters and bias voltages.

In order to use this physics-based model effectively for a nonlinear circuit analysis, the technique of interacting this model with a simulator must be developed. There are three possible approaches available:

The first approach is to interact this physics-based analytical model with an analysis program directly by harmonic balance technique as

described by Khatibzadeh et al [6]. However, this needs special skill of writing the whole CAD program, and it is usually not an easy task.

The second approach is the construction of a large-signal equivalent circuit model as described in this work. An automatic large-signal model extraction program can also be used if it is available [14]. Since the physics-based model can provide S-parameters, the same measurement-oriented extraction procedures can be adopted to extract a large-signal equivalent circuit model for the MESFET. The model is then embedded into the external circuit, and the MESFET or the whole MMIC can be analyzed. This device/circuit linking technique offers the advantage of fully utilizing the powerful CAD tools existing such as HP85150B Microwave Design System.

The third approach is by using Root model [15]. This is a data-base model in which there are no pre-defined empirical or physical equations to represent the model currents and charges as functions of terminal voltages. It uses S-parameter data stored in a tabular form and interpolates them to arrive at model port relations or equivalent circuit element constitutive relations. The model generation is thus fast and very accurate. The S-parameters can be obtained from practical measurements or from physics-based device simulations. The Root model has been incorporated in HP85150B MDS revision B.04. The combination of FETPro and HP85150B MDS revision B.04 would be a better choice for the physics-based simulation by a designer in the foundry.

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