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A HIGH-TEMPERATURE PRESSURE SENSOR UTILIZING LINEAR VOLTAGE DIFFERENTIAL TRANSFORMER (LVDT) AND SILICON WAFER-TO-WAFER FUSION BONDING TECHNOLOGIES

by
Robert Sylvester Okojie

A Thesis
Submitted to the Faculty of
New Jersey Institute of Technology
in Partial Fulfillment of the Requirements for the Degree of
Master of Science in Electrical Engineering

Department of Electrical and Computer Engineering

October 1993

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APPROVAL PAGE

A HIGH-TEMPERATURE PRESSURE SENSOR UTILIZING LINEAR VOLTAGE DIFFERENTIAL TRANSFORMER (LVDT) AND SILICON WAFER-TO-WAFER FUSION BONDING TECHNOLOGIES.

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ABSTRACT

A High-Temperature Pressure Sensor Design Utilizing Linear Voltage Differential Transformer (LVDT) and Silicon Wafer-to-Wafer Fusion Bonding Technologies

by
Robert Sylvester Okojie

A novel high-temperature pressure sensor was designed based on the principle of magnetic induction. The device is meant to correct the problems inherent in conventional Solid-State pressure transducers such as piezoresistive and capacitive at temperatures above 300°C. Prominent among these problems are increased leakage current, reduced absolute sensitivity, redistributed impurity concentration profile, and thermal mismatch.

This thesis combined the Biot Savart magnetostatic principle and the theory of deflecting clamped circular plates to obtain the microelectromechanical relationship. The problem of thermal mismatch was resolved by the symmetrical layering of a $Si_3N_4/TaSi_2/Si_3N_4$ sandwich, thereby controlling runaway thermal expansion of $TaSi_2$. Single-wafer and Wafer-to-Wafer fusion bonding fabrication processes are proposed for making the device.

The device operating temperature range is extended above that obtainable with piezoresistive silicon to 650°C, based on theoretical and simulation results. The full-scale Temperature Coefficient of Offset (TCO) of 771ppm/°C, and pressure sensitivities of 0.4mV/kPa and 0.54mV/kPa at 25°C and 650°C, respectively, were achieved. The output voltage Temperature Coefficient of Sensitivity (TCS) for temperatures over the range of -50 to 650°C is 800ppm/°C. The large output voltage dynamic range of over 100mV competes well with conventional sensors. The increased pressure sensitivity at high temperatures is an added advantage.

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I thank Michael J. Grieco and Michael S. Berry for helping me throughout my assignment in the device fabrication lab (Cleanroom) of the Microelectronics Research Center at NJIT.

My thanks also go to Yang Guang for keeping the computer terminals 'alive' throughout this period, and to Prasad Nevrekar for material support.

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CHAPTER 1
INTRODUCTION

1.1 Overview

The oldest pressure sensors are of course those of living fauna. The human ear is an example. The first pressure sensor built by man is the Torricelli manometer, with the mercury column, from which the unit "**mmHg**" originated. The Torricelli manometer has continued in use to this day.

There are now many types of pressure sensing devices of which the manometer is an example. Some of these devices are invented and developed to operate in a specific environment. Among the well-known pressure measuring devices today are the piezoresistive, capacitive, and deflecting beam sensors. A typical piezoresistive pressure sensor (35) is shown in fig. 1-1 The piezoresistive sensor is sensitive changes in strain induced by applied pressure on the diaphragm. These devices use an optimal crystallographic orientation of resistors in silicon. The resistance changes in response to the change in strain. The change in output voltage as a result of resistance change corresponds to the applied pressure. A capacitive pressure sensor (24) is shown in fig. 1-2. In this sensor, two oppositely charged plates are brought in close proximity to each other. As pressure is applied on one plate, the plate gap changes, thereby changing the capacitance. The resonant beam pressure sensor (36), shown in fig. 1-3 uses the natural resonance of a beam tethered on one end. When pressure is applied, the resonant frequency changes. All these and other pressure sensors have their advantages and disadvantages. However, one problem that is common is that of reliability at high temperatures.

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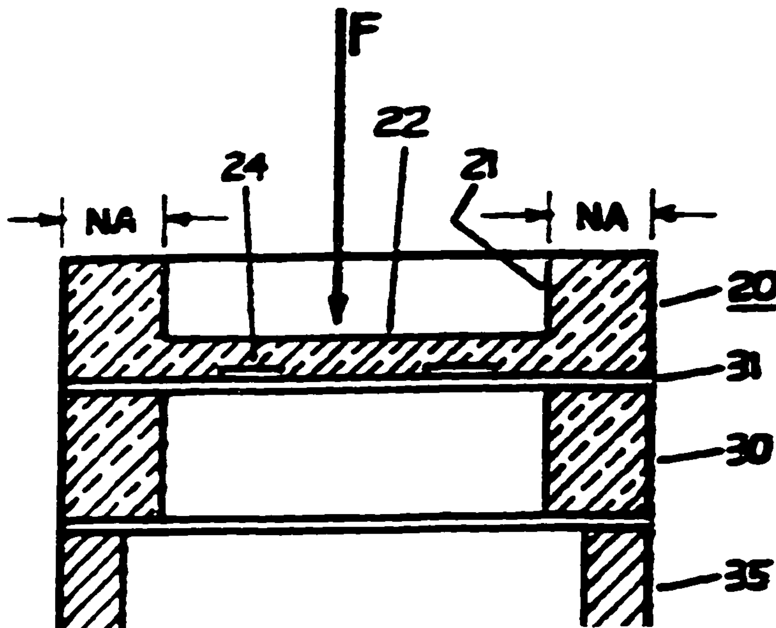

Fig. 1-1 A piezoresistive pressure sensor. [35]

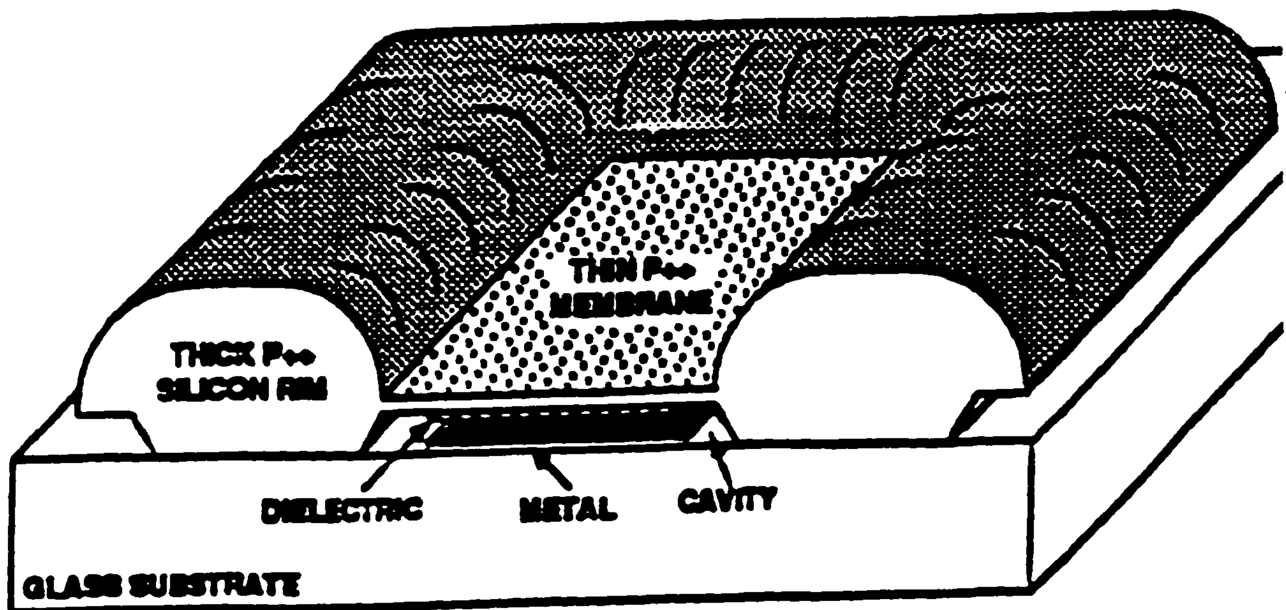

Fig. 1-2 A capacitive pressure sensor. [24]

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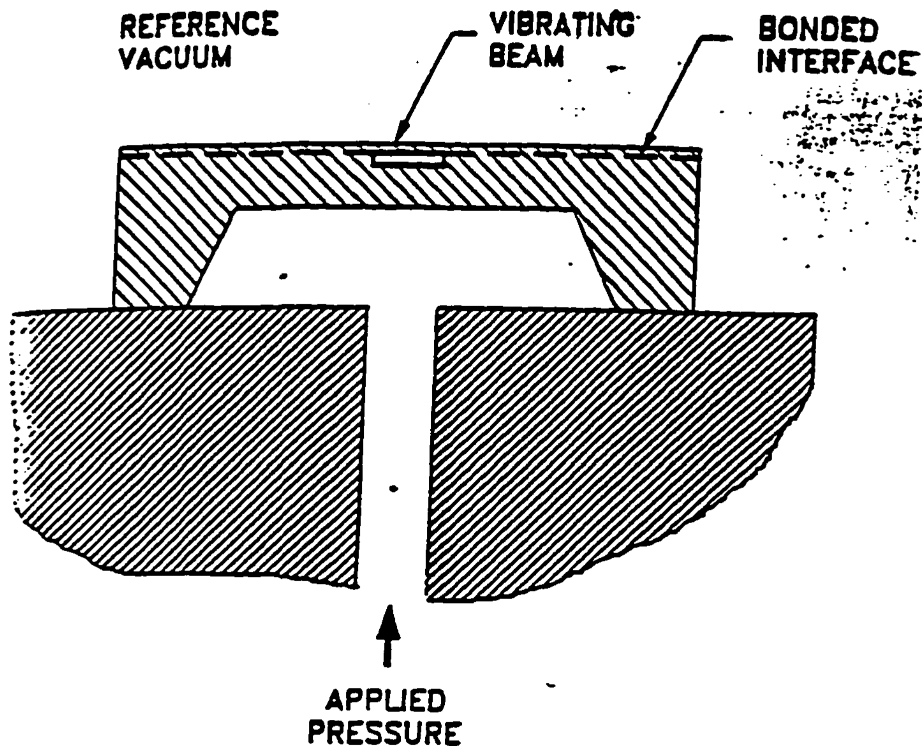

Fig. 1-3 A resonant beam pressure sensor.[36]

The quest for energy conservation, waste management, and process optimization, has created a growing need for more accurate and precise measurement of energy consumption rates inside combustion chambers and reactors. To achieve these goals, it is imperative for sensing devices to interact directly with the sensed environment. Secondly, data obtained should be transmitted with minimum distortion through the interface circuitry. The major difficulty encountered in attempting to make these sensors interact directly is the fact that typical temperature of the chamber is usually above 125°C. Beyond this

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temperature, device reliability and survivability becomes questionable for most conventional pressure sensors due to the strong dependence of their parameters on temperature. As a result, related industry has intensified its research into resolving these problems.

This thesis is proposing a new generation of device that could survive temperature environments as high as 700°C. Several papers (17, 25, 37) have recently reported pressure sensors suitable for temperatures of around 350°C. Because most of these reported devices still retain the high temperature sensitive parameters, they are essentially an upgrade of existing devices such as piezoresistive and capacitive pressure sensors. In these devices, the problems of redistributed impurity concentration profile, leakage current, and strain-inducing TCE mismatch have at best been reduced but not eliminated.

This thesis attempts to solve these problems by applying different technology that does not use diffused resistors or capacitors. Sensitivities due to TCE mismatch is reduced by **symmetrical layering**. Two designs using single-wafer process and silicon wafer-to-wafer bonding has been proposed. The active element is Tantalum Silicide ($TaSi_2$) inductors.

1.2 Chapter Synopsis

There are twelve chapters in this thesis. The chapters are divided into four sections. In chapters two and three the goal of the thesis and the definition of the device are respectively discussed. The second segment contains chapters four, five, six, seven, and eight. Chapter four establish the fundamentals of Biot Savart principle (2) as it supports the device electrical concept. This is followed by large and small membrane stress and deflection analysis based on the equations of Timoshenko *et al* (9, 10) in chapter five. Chapter six meshes the theories of the

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two previous chapters to develop the microelectromechanical relationships and first order sensitivities. In chapter seven, other secondary sensitivities of great importance are discussed. The third section contains chapter eight, nine, and ten. In chapter eight, the optimization of the device is discussed, in which issues such as power budget, tradeoffs and others are investigated. Chapter nine discusses the mask design for single-wafer and wafer-to-wafer bonding processes. In chapter ten, the proposed fabrication process is presented. The final section is chapter eleven, the conclusion, in which the optimized device is compared with some devices currently in the market and also reported in several papers.

1.3 Thesis Goal

The original goal of this thesis are three-fold. The first involves the conceptual development of the high-temperature pressure sensor in terms of the electromechanical parameters. The second is to establish a relationship between these electromechanical parameters to operate as a high-temperature pressure sensor. The third is the physical realization of the device by utilizing the fabrication facilities in the Cleanroom of the Microelectronics Research Center (MRC) at NJIT. In this thesis, the first two of the three goals are achieved and reported. The stage to begin the physical realization of the device has been set. Unfortunately, however, time does not permit this to happen for now.

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CHAPTER 2

BRIEF HISTORY OF PRESSURE SENSORS

2.1 From Torricelli to LVDT

As previously stated, the first known industrial pressure sensor is the **Torricelli manometer**. The is named after Evangelista Torricelli (1608-1647), an Italian scientist. It is important to note that at the same period in history, Blaise Pascal (1623-1662), a French

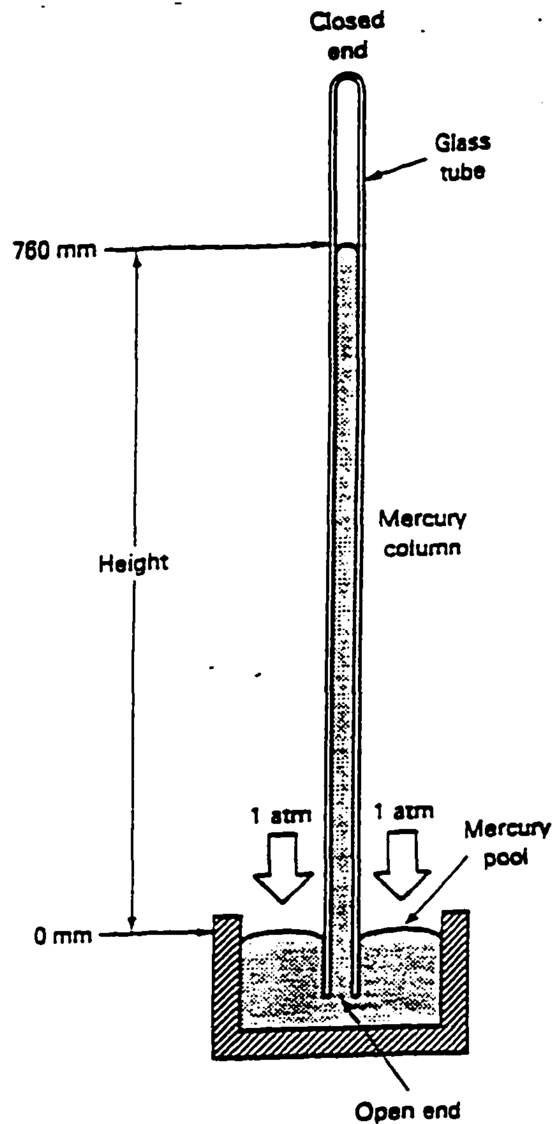

Fig 2-1 The Torricelli manometer [38]

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scientist, is propounding the principle that states:

> Pressure applied to an enclosed fluid is transmitted undiminished to every portion of the fluid and walls of the containing vessel

The pressure units of **"Torr"** and **"Pascal"** are evidently named after both men. They remain part of the pressure measuring units today and is recommended by the United States National Institute of Standards and Technology (NIST). To convert "Pascal" to "Torr", multiply "Pascal" by 7.5×10^{-3}. Figure 2-1 shows the Torricelli manometer (38). A vacuum is initially created within the tube. The tube is then inverted into a pool of mercury. A column of mercury would rise up the tube and stop at a height. This weight of mercury within this height is at equilibrium with the external pressure. Usually at sea level, this height of mercury is 760mm, explaining why 760mmHg became the standard for measuring pressure. Therefore, **1atm=760mmHg**.

Although the Torricelli manometer has remained in use to this day, pressure sensing has undergone dramatic and radical evolutionary changes within the past three hundred years. This change is fueled by the industrial revolution, in which demand for specialized pressure sensors escalated. It becomes impracticable for the Torricelli manometer to measure pressure in some conditions due to size, position, stability, temperature, and other limitations.

In 1905, Nicholas Korotkoff pioneered the pressure measuring method called **sphygmanometry**. In this method, which is still in wide use, a hollow flexible band is wound around the arm. Air is blown in causing it to tighten round the patient's arm. As the air is let out, the reading on the mercury-filled glass tubing is observed. At a certain point when the patient's pressure is equal to the tube pressure, there is a resonance. This causes the mercury to "leap" in response to the pressure amplification, called systolic. From this process, the patient's systolic and diastolic pressures are measured. One disadvantage of this method is the fact that pressure sensing is indirect, leaving room for inaccuracies.

Several improvements have been made to make it possible to measure pressure

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directly. This is brought about by the advent of semiconductor technology. It is now possible to fabricate a pressure sensor small enough to be implanted into the blood stream and without any external wiring connected. Such pressure sensor called **Remotely Interrogated Passive Pressure Sensor (RIPPS)**. It is made by fabricating a variable resonance circuit on a silicon diaphragm. The vacuum cavity makes it possible to measure absolute pressure. The resonance circuit changes with the cranial pressure. It could be implanted through the skull to measure cranial pressure. Pressure is measured by sending bursts of harmless electromagnetic waves while varying the frequency. At the resonance frequency, the device transmits the response. This response depends on the change in resonance circuit due to change in absolute pressure.

Industrial pressure sensors have also undergone changes since Torricelli. At the turn of the century, pressure measurement methods are mainly fluid and spring-based. In

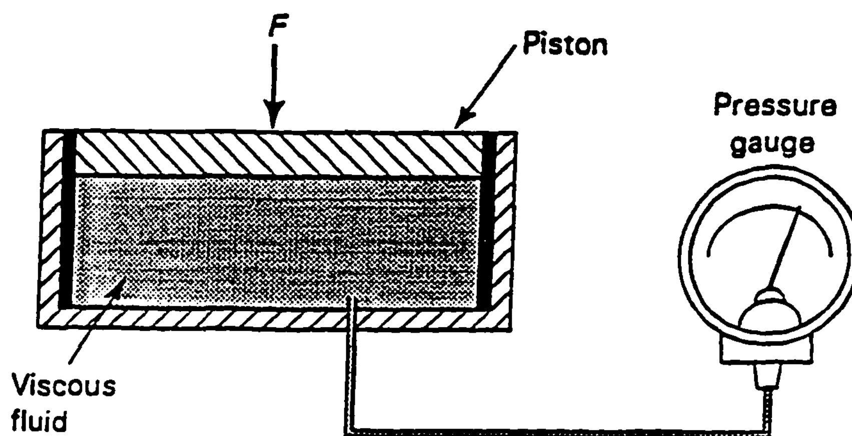

Fig. 2-2 A fluid-filled pressure sensor [38].

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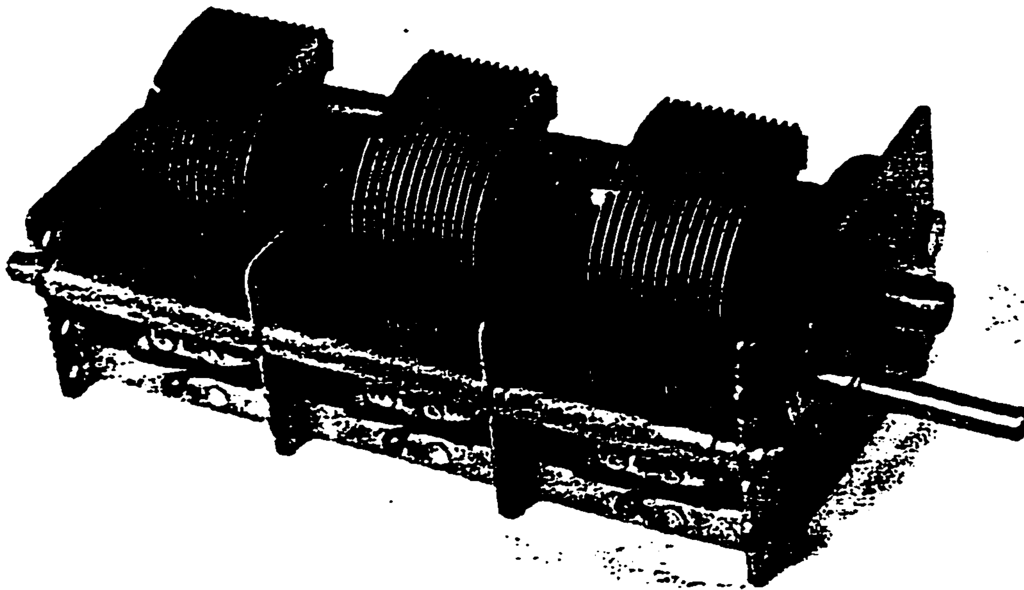

Fig. 2-3 A variable air-capacitor pressure sensor [38].

this method, a pressure gauge connected to fluid-filled piping shown in fig. 2-2 measures the force due to an applied pressure on the platform at the other end of the pipe. Another type of industrial pressure sensor is the **variable air capacitor pressure sensor.** shown in fig. 2-3. The hollow protrusion is connected to fluid-filled pipe that is sealed with the platform (not shown). Inside the capacitor assembly is a shaft that is driven by gears. When pressure is applied on the platform, it is transmitted through the pipe to the diaphragm connected to the gears. The gears drive the shaft that rotates the plates. At full scale pressure, therefore, the plates are well into each other, giving largest capacitance.

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CHAPTER 3
THE LINEAR VOLTAGE DIFFERENTIAL TRANSFORMER

3.1 Definition

The Linear Voltage Differential Transformer (LVDT) is a pressure sensor that utilizes the principle of inductive coupling as link between electrical and mechanical actions. It takes advantage of transformer action in the transfer of energy from one conductor to another. The term 'Linear' means that the two conductors are moving in only one direction, either toward or away from each other. So the movement is 'linear'. As they move away or come toward each other, the current-carrying conductor induces a voltage on the passive conductor. Hence the term 'voltage'. Since the magnetic field linking the passive conductor changes with the gap between the two conductors, the induced voltage would also change. Therefore at any change in gap, there is a difference in voltage. Hence the term 'Differential'. The last term 'Transformer' makes it self evident that the phenomena is basically a transformer action.

The acronym LVDT, it is only recently learnt, has been used to describe some actions that is similar to the above description (34). In fact, it turns out that the device is a pressure sensor that utilizes LVDT action! Figure 3-1a shows the innards of an OMEGA LVDT pressure sensor. The electrical schematic is shown in fig. 3-1b. The core is made of a high permeability constant alloy of nickel-iron, thereby enhancing high flux density to link the secondary wiring. The limitations of this device becomes apparent. Generally, ferromagnetic materials are unstable at high temperatures. The typical operating range of the Omega device is 80°C and a compensated range of 150°C. Another limitation is size. It has a typical core mass range of between 0.2oz and 1.0oz and a radial core clearance of 0.06in. It would be impossible to implement as and on-chip integrated smart sensor. However, it is an LVDT!

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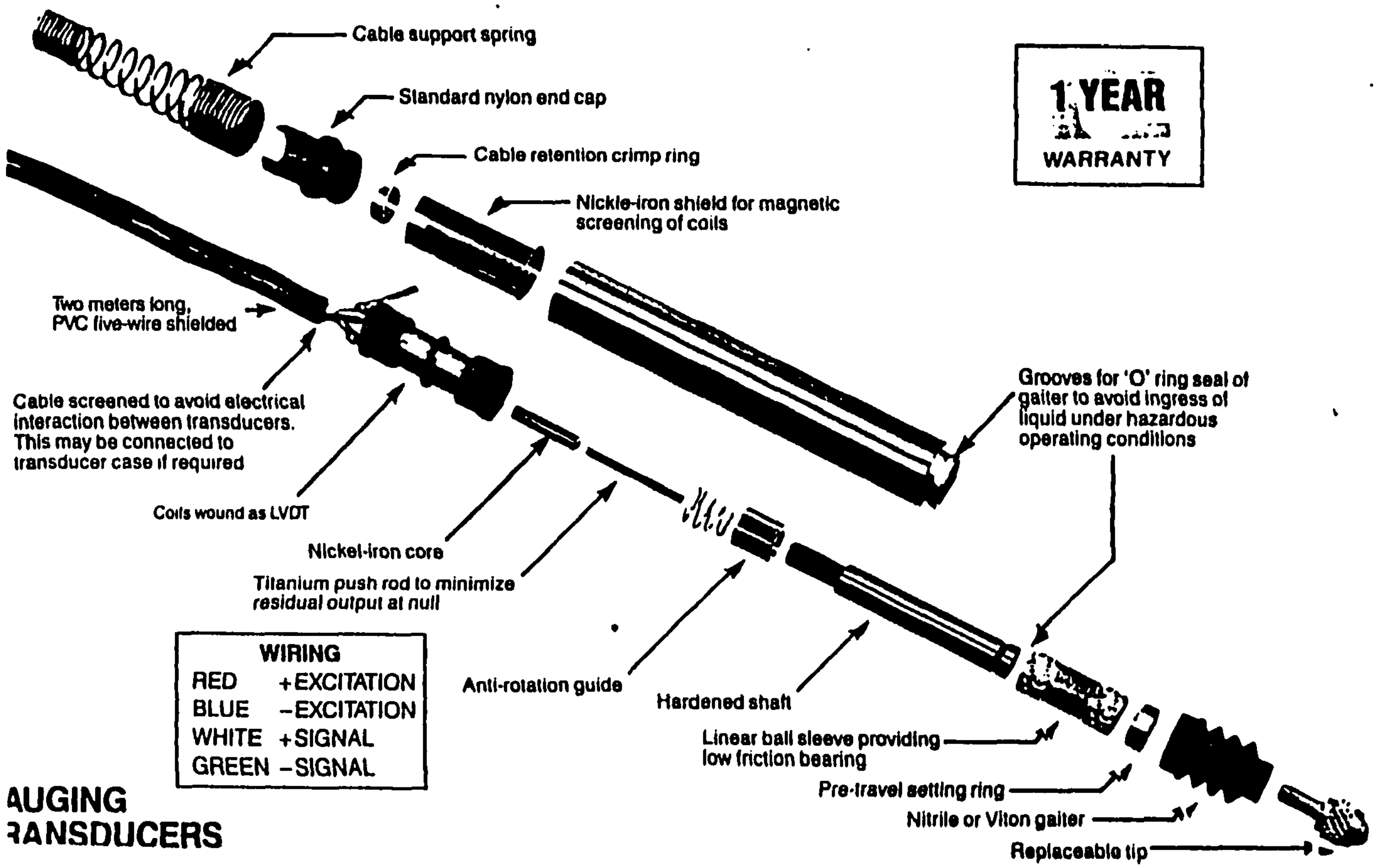

Fig 3-1a A typical OMEGA LVDT showing disassembled pieces [34]

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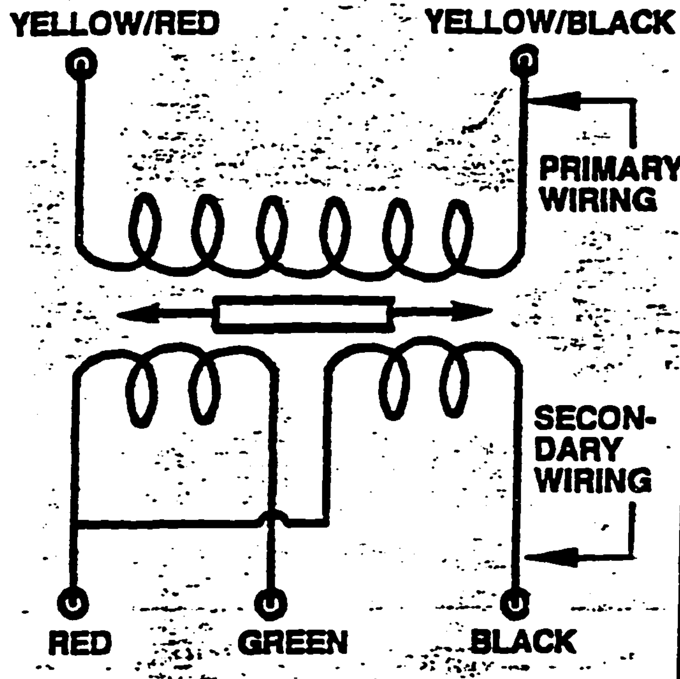

Fig 3-1b The OMEGA LVDT schematic [34].

In this thesis, the proposed LVDT has the capability to operate at temperature range of 650°C without compromising reliability and measurement accuracy. All materials used have melting points above 1000°C. Unlike the OMEGA-LVDT with the NiFe core, this device uses an air core. It can be fabricated on-chip as part of an integrated smart sensor chip. The die size of the proposed device is $560 \times 500 um^2$, creating a potential for high yield and throughput. Response time is not evaluated in this thesis, but is believed to be in the order of $10^8 ms^{-1}$.

3.2 Microembodiment

The proposed high_temperature pressure sensor is made primarily of two square-shaped Tantalum Silicide ($TaSi_2$) conductors sputtered and patterned into coils. One conductor is

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the primary coil and the other the secondary of M and N turns, respectively. Figure 3-2a to d shows the top , crossectional, and three dimensional view, respectively, of the device. The top coil is the primary coil and the bottom is the secondary. The later lies on the bed of a cavity etched in a high resistivity n-type wafer. The secondary coil link to output voltage 1 (V_{out} 1) terminal is first sputtered and patterned on oxide layer. The next layer is Silicon Nitride (Si_3N_4) that provides dielectric isolation between coil and link. This nitride layer also forms part of the symmetrical layer arrangement that would control runaway Silicide thermal expansion. This layer is followed by the Silicide conductor coil with link extending to output voltage (V_{out} 2) terminal. Another nitride layer covers the Silicide. The Silicide is thus effectively encapsulated in nitride.

The cavity is at the pressure of the fluidic via sealing process level, which is essentially about 10^{-3} Torr. On the cavity is the primary coil, again encased in nitride. A layer of Low Temperature Oxide (LTO) is deposited on the nitride to mechanically passivate the top polysilicon layer. The effective thickness of the membrane is the combination of the nitride, oxide, and polysilicon. The bonding pads are the standard 100x100 um^2.

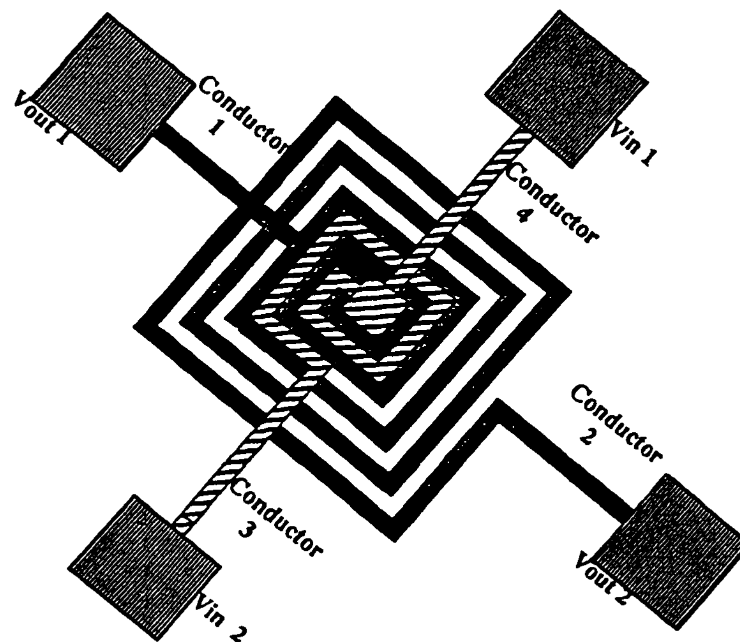

Fig. 3-2a Top view of proposed LVDT high-temperature pressure sensor

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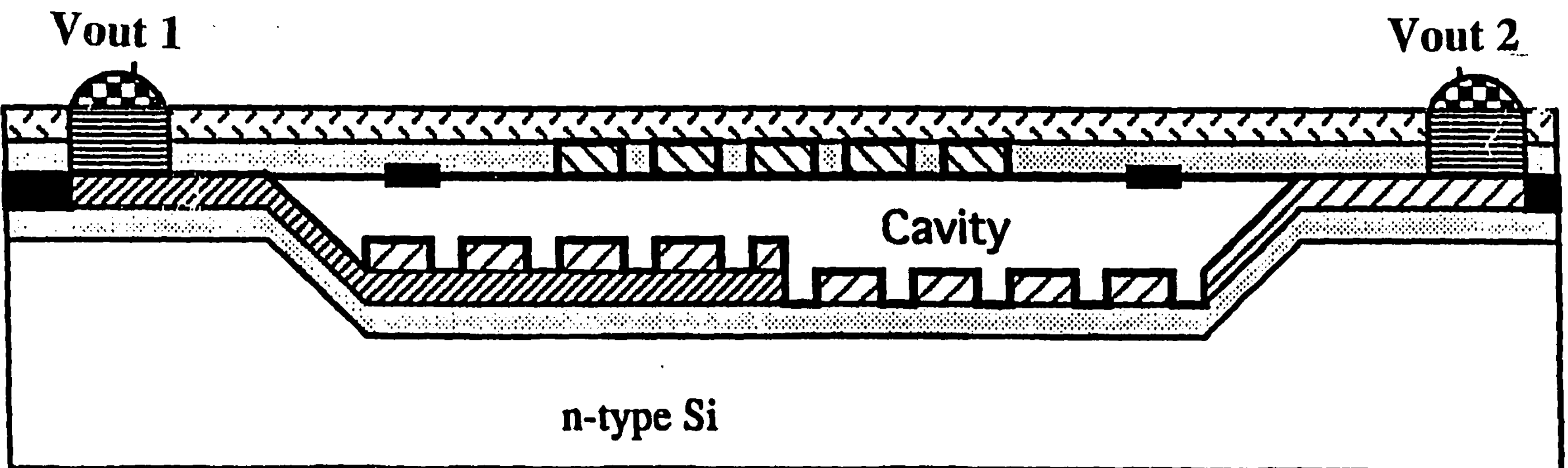

Fig. 3-2b Cross-sectional view of HT-LVDT pressure sensor. (Single wafer process)

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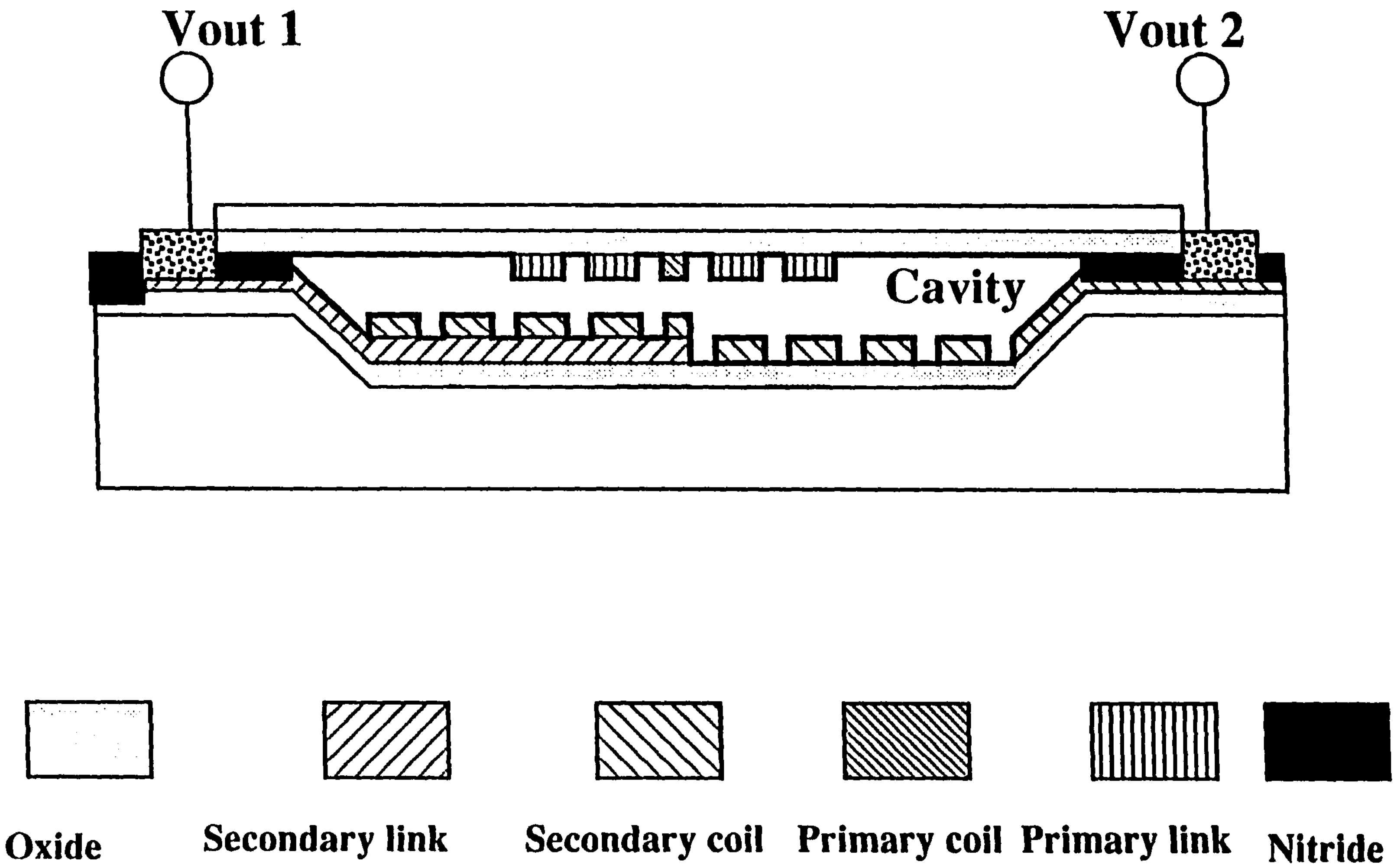

Fig. 3-2c Crossectional view of HT-LVDT pressure sensor. (Wafer-to-Wafer fusion bonding process)

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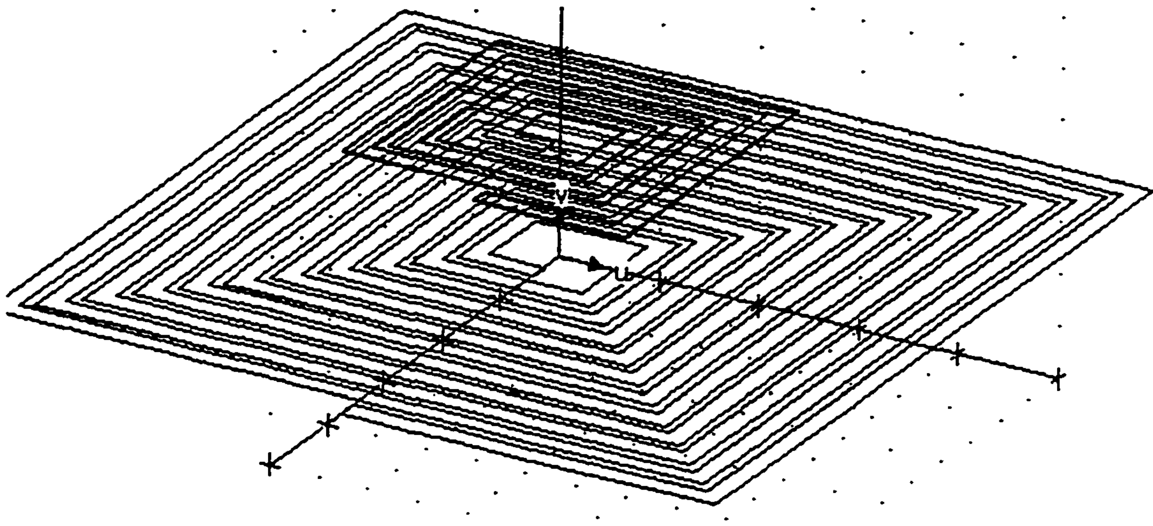

Fig. 3-2d A 3-D perspective of proposed high-temperature pressure sensor.

3.3 Device Operation

The microsensor described in this paper operates by the principle of magnetic induction. An alternating current passes through the primary coil, generating a magnetic field that creates a flux in the secondary coil. Upon application of pressure on the diaphragm, the gap between the two coils would change, thereby changing the induced voltage on the secondary coil.

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CHAPTER 4
MICROMAGNETIC DESIGN PRINCIPLES

4.1 Generalization of Biot-Savart law in Magnetostatics.

The principle that drives the proposed pressure sensor is based on the general fundamentals of Biot-Savart Law. It essentially offers a theoretical analysis of the magnetic flux density B at an observation point. This law is defined in terms of the magnetic flux density observed at a position P' that is contributed by a current-carrying element located at a point P shown in Fig 4-1. The general mathematical expression of this law can be written as follows (2):-

$$d\mathbf{B}(\mathbf{r}) = \frac{\left[\mu \mathbf{J}(\mathbf{r}) dV \times \hat{\mathbf{r}}_{PP'}\right]}{4\pi\left|\mathbf{r}-\mathbf{r}'\right|^2}, \tag{4.1-1}$$

where

μ=Permeability (H/m) of air

$d\mathbf{B}(\mathbf{r})$= Differential magnetic flux density (Wb/m^2),

$\mathbf{J}(\mathbf{r})$= Current density (A/m^2),

dV= Differential volume of the current-carrying element (m3),

$\hat{\mathbf{r}}_{PP'}$= Unit vector of distance between P and P'(m).

The symbol '$\times$' represents the cross-product unless otherwise stated.

4.1.1 Coils Description

The objective of this segment of the thesis is to directly apply this law to the case of two square planar coils, each of N-turns and M-turns, aligned in vertical orientation with one another as shown in fig. 4-1. The primary coil side length is denoted b_i, with 'i' symbolizing 'ith' turn. The primary coil lies on the x-y plane.The origin,'O', is placed at the center of the primary coil, dividing the plane into equal quadrangles. The secondary coil

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lies on the x'-y' plane, with the origin at P'. Like the primary coil, the origin is placed at the center of the secondary coil. Its side length is denoted as b_j.

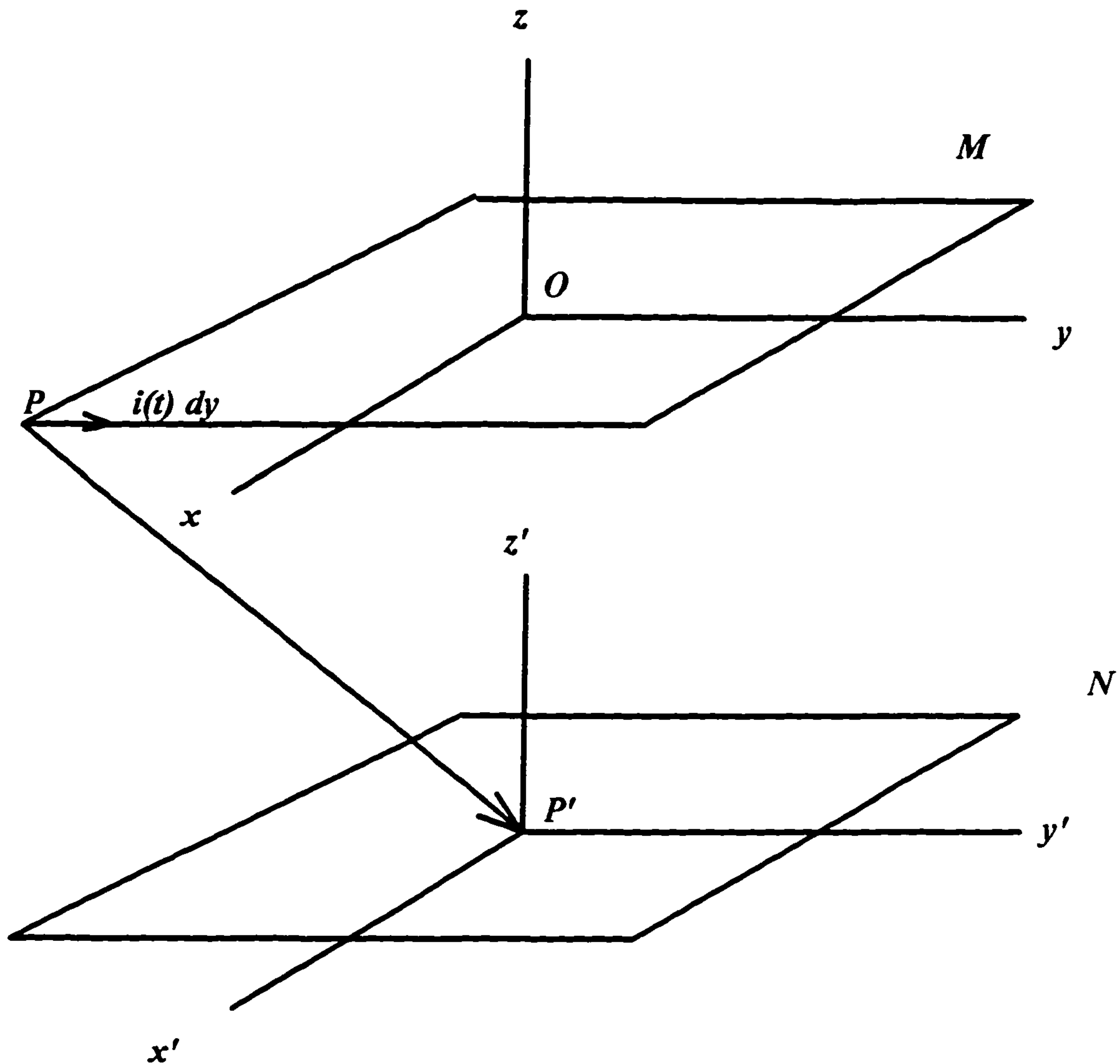

Fig. 4-1 Two square planar coils of one turn each

The arrangement of the two coils is such that the primary coil is placed directly above the secondary coil. The objective of the setup described above is to evaluate the following for the secondary coil N:

a. Distributed magnetic flux density in the secondary coil

b. The equivalent magnitude of the magnetic flux(flux yield) obtained

c. The resultant voltage V_S generated as a function of primary

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current I_p flowing in the primary coil M.

4.1.2 Magnetic Flux Density Calculation

We wish to determine the magnetic flux density **B** that exists in the secondary coil contributed by the current, $i(t)$, flowing in the primary coil. Let g represent the distance between the two planar coils. To evaluate the magnetic flux density, we consider the total contribution by each turn of the primary coil. Therefore, for an M-turn coil, the total flux density contribution would be the summation of the contribution by each turn. Using figure 4-1, we see that there are four sides on each primary turn contributing equally to the flux density inside the secondary coil N. The assertion that each side of turn is the same length might seem erroneous at first glance. However, an in-built Dimensional Correction Factor (DCF) (30) shown in fig. 4-2.

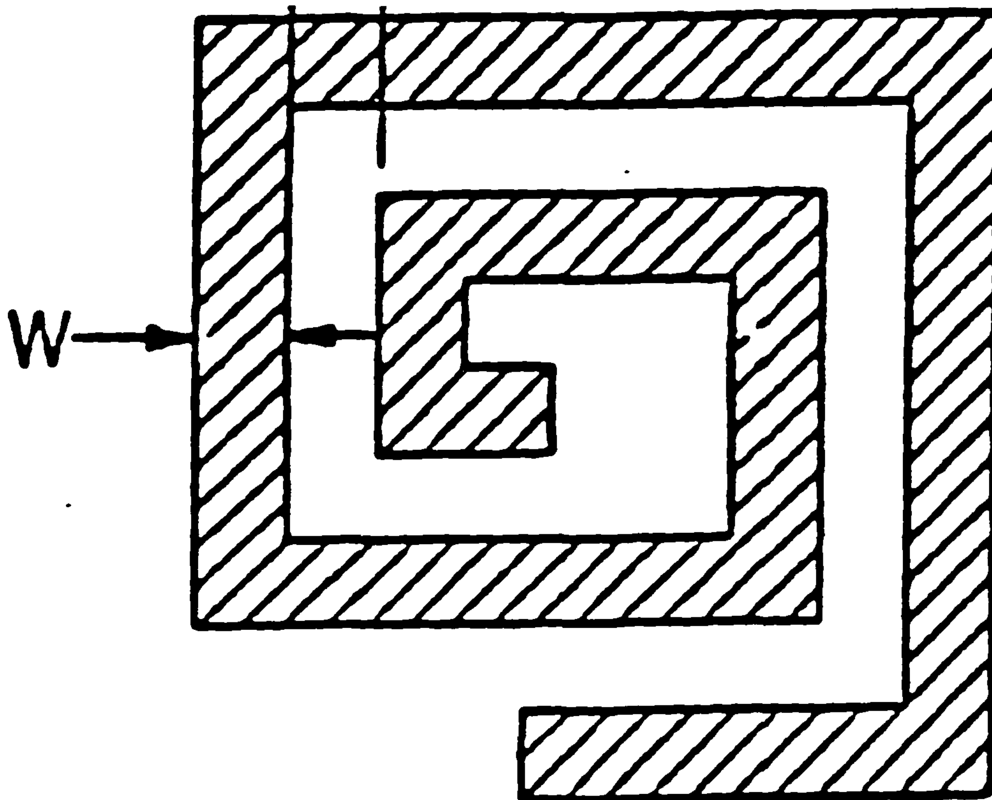

Fig. 4-2 Center-fed rectangular spiral dimensions

The symmetry in each turn makes it possible to evaluate only one side-length and

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then multiplying the result by four. Each side ideally contributes equal amount of flux. Starting with a primary coil turn measuring b_i, on edge, consider the current, $i(t)$, flowing through a differential length d_y in the positive y-direction. At point P' on the secondary coil plane, the magnetic flux density contributed by the current in this differential length of primary current-carrying element, $y' i(t) d_y$ is

$$dB(r) = \frac{\left[y' \mu i(t) d_y \times \bar{r}_{PP'} \right]}{4 \pi r^2} \qquad (4.1.2\text{-}1)$$

The differential magnetic flux dB(r) can be expressed as a function of y and g in the following derivation:

From fig. 4-1, the distance r between P and P' is evaluated vectorally as:

$$\bar{r} = \hat{a}_x (x' - x) + \hat{a}_y (y' - y) + \hat{a}_z g \qquad (4.1.2\text{-}2)$$

Evaluating its magnitude,

$$|\bar{r}| = \sqrt{(x' - x)^2 + (y' - y)^2 + g^2} \qquad (4.1.2\text{-}3)$$

The unit vector is determined as

$$\hat{r} = \frac{\bar{r}}{|\bar{r}|} = \frac{\hat{a}_x (x' - x) + \hat{a}_y (y' - y) + \hat{a}_z g}{\sqrt{(x' - x)^2 + (y' - y)^2 + g^2}} \qquad (4.1.2\text{-}4)$$

From the above analysis, equation 4.1.2-1 becomes

$$dB'(\bar{r}) = \frac{\hat{a}_y \mu I_0 d_y X \left[\hat{a}_x (x' - x) + \hat{a}_y (y' - y) + \hat{a}_z g \right]}{4 \pi \left[(x' - x)^2 + (y' - y)^2 + g^2 \right]^{3/2}} \qquad (4.1.2\text{-}5)$$

From figure 4-1, we see that point P' is at zero. From the set up, we also see that plane of the primary and secondary coils are divided into four equal segments. From the point of evaluation, the terms (x'-x) and (y'-y) are equal ($-b_i/2$) and y, respectively because x'=y'=0.

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Resolving the vectors by taking the cross-products, the differential magnetic flux density becomes

$$dB_i'_{(+y)} = \frac{\mu I_o \left[\hat{a}_z \frac{b_i}{2} + \hat{a}_x g\right] dy}{4\pi \left[\left(\frac{b_i}{2}\right)^2 + y^2 + g^2\right]^{3/2}} \quad (4.1.2\text{-}6)$$

The magnetic flux density at point P' contributed by the current in the side-length coil element is therefore

$$B_i'_{(+y)} = \frac{\mu I_o \left[\hat{a}_z \frac{b_i}{2} + \hat{a}_x g\right]}{4\pi} \int_0^{\frac{b_i}{2}} \frac{dy}{\left[\left(\frac{b_i}{2}\right)^2 + y^2 + g^2\right]^{3/2}} \quad (4.1.2\text{-}7)$$

$$B_i'_{(+y)} = \frac{\mu I_o \left[\hat{a}_z \frac{b_i}{2} + \hat{a}_x g\right]}{4\pi} \left. \frac{y}{\left[\left(\frac{b_i}{2}\right)^2 + g^2\right]\left[y^2 + \left(\frac{b_i}{2}\right)^2 + g^2\right]^{1/2}} \right|_0^{\frac{b_i}{2}} \quad (4.1.2\text{-}8)$$

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$$B_i'_{(+y)} = \frac{\mu I_o\left[\hat{a}_z\frac{b_i}{2}+\hat{a}_x g\right]}{4\pi\left[\frac{b_i^2}{4}+g^2\right]}\left[\frac{\frac{b_i}{2}}{\left[2\frac{b_i^2}{4}+g^2\right]^{\frac{1}{2}}}\right] \quad (4.1.2\text{-}9)$$

By virtue of symmetry of each coil turn, we are now capable of evaluating the flux density contribution of each side length by simply multiplying 4.1.2-9 by eight: Below summarizes the result of such evaluation:

$$B_i' = -\hat{a}_z 8\frac{\mu I_o b_i^2}{16\pi\left[\frac{b_i^2}{4}+g^2\right]}\frac{1}{\left[\frac{b_i^2}{2}+g^2\right]^{\frac{1}{2}}} \quad (4.1.2\text{-}10)$$

As we know, the above result represents the contribution of all the segments at a particular point P'. The total flux density over the entire secondary coil plane can be determined by modifying 4.1.2-10. So that for a non trivial solution, the total magnetic flux density on ith secondary coil plane is expressed as

$$B' = -\hat{a}_z 8\frac{\mu I_o b_i^2}{16\pi\left[\frac{b_i^2}{4}+g^2\right]}\frac{1}{\left[\left(x'-\frac{b_i}{2}\right)^2+g^2\right]^{\frac{1}{2}}} \quad (4.1.2\text{-}11)$$

A plot of the magnetic flux density on the plane of the secondary coil for various coil gaps is shown in fig. 4-3.

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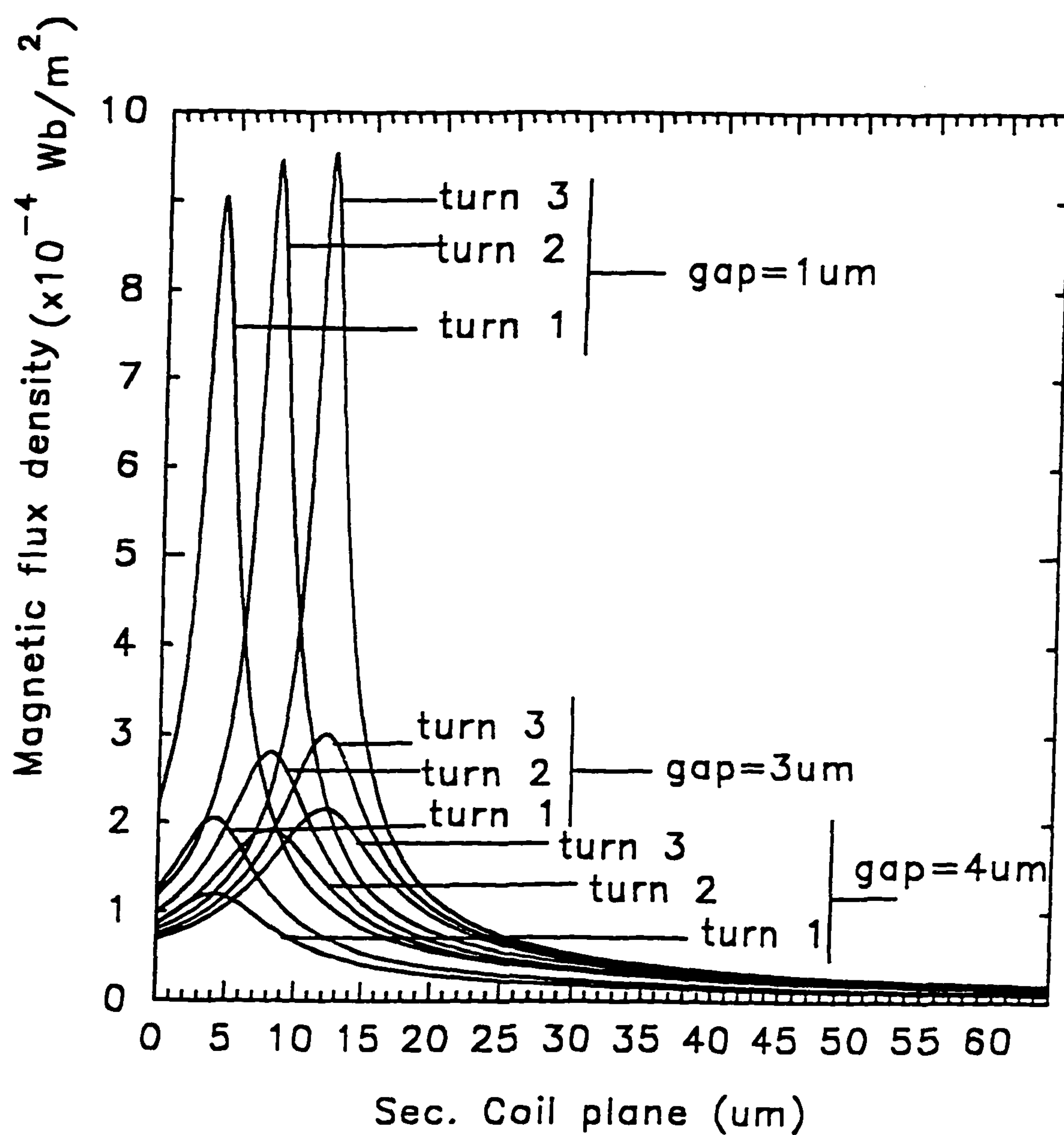

Fig. 4-3 Magnetic flux density on the plane of the secondary coil for various coil gaps

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4.1.3 Flux Calculation

The flux is obtained from the above result by taking the surface integral of the area enclosed by each turn of the secondary coil. In the case of a conventional transformer, this integration is carried out over one surface area and then multiplied by the number of secondary turns. In the proposed configuration, however, since each turn has different surface area it encloses, N number of integrations would have to be done and then summed up. The total flux yield on the secondary coil turns is expressed as

$$\phi = -2\frac{\mu I_0 b_i^2}{\pi}\frac{1}{\frac{b_i^2}{4}+g^2}\int_0^{\frac{b_j}{2}}\int_0^{\frac{b_j}{2}}\frac{dx'dy'}{\left[\left(x'-\frac{b_i}{2}\right)^2+g^2\right]^{1/2}} \qquad (4.1.3\text{-}1)$$

where, again we have taken advantage of symmetry to consider only one quadrangle and multiplying by four. Integrating the above equation as it is would be cumbersome. By changing the x' variable we can easily evaluate the flux yield.

Let

$$\left(x'-\frac{b_i}{2}\right)^2 = v^2 \qquad (4.1.3\text{-}2)$$

So that

$$x'-\frac{b_i}{2} = v \qquad (4.1.3\text{-}3)$$

Solving for x' in terms of v, we get

$$x' = \frac{b_i}{2} + v \qquad (4.1.3\text{-}4)$$

Differentiating x' with respect to v, we get

$$dx' = dv \qquad (4.1.3\text{-}4)$$

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Given the above algebraic manipulations, equation 4.4-1 now becomes

$$\phi = -2\frac{\mu I_o b_i^2}{\pi}\frac{1}{\frac{b_i^2}{4}+g^2}\int_{\frac{b_i}{2}}^{\frac{b_j-b_i}{2}}\int_0^{\frac{b_j}{2}}\frac{dv\,dy'}{\left[v^2+g^2\right]^{1/2}} \qquad (4.1.3\text{-}5)$$

Integrating, we have the flux to be

$$\phi = -\frac{\mu I_o b_i^2}{\pi}\frac{b_j}{\frac{b_i^2}{4}+g^2}\ln\left[\frac{\frac{b_j-b_i}{2}+\sqrt{\left(\frac{b_j-b_i}{2}\right)^2+g^2}}{-\frac{b_i}{2}+\sqrt{\frac{b_i^2}{4}+g^2}}\right] \qquad (4.1.3\text{-}6)$$

Since the flux linking each turn changes with time, the total flux yield is expressed as

$$\phi(t) = -\frac{\mu I(t) b_i^2}{\pi}\frac{b_j}{\frac{b_i^2}{4}+g^2}\ln\left[\frac{\frac{b_j-b_i}{2}+\sqrt{\left(\frac{b_j-b_i}{2}\right)^2+g^2}}{-\frac{b_i}{2}+\sqrt{\frac{b_i^2}{4}+g^2}}\right]$$

(4.1.3-7)

A summation of the flux contribution by each primary coil turn is therefore expressed as

$$\phi_{ij}(t) = -\frac{\mu I(t)}{\pi}\sum_{i=1}^{M}\sum_{j=1}^{N} Q_{ij} \qquad (4.1.3\text{-}8)$$

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$$\text{where } Q_{ij} = \frac{b_i^2 b_j}{\frac{b_i^2}{4} + g^2} \ln \left[\frac{\frac{b_j - b_i}{2} + \sqrt{\left(\frac{b_j - b_i}{2}\right)^2 + g^2}}{\frac{b_i}{2} + \sqrt{\frac{b_i^2}{4} + g^2}} \right]$$

4.1.4 Output Voltage V_S Calculation

The evaluation of the output voltage is obtained by numerically evaluating the analytical solutions above. This is expressed as

$$V_S = -\frac{d}{dt} \phi_N(t) \qquad (4.1.4\text{-}1)$$

$$= \frac{d}{dt} \frac{\mu I \sin(\omega t)}{\pi} \sum_{i=1}^{M} \sum_{j=1}^{N} Q_{ij} \qquad (4.1.4\text{-}2)$$

$$= \frac{\omega \mu I \cos(\omega t)}{\pi} \sum_{i=1}^{M} \sum_{j}^{N} Q_{ij} \qquad (4.1.4\text{-}3)$$

Equation 4.1.4-3 expresses the output voltage as function of coil geometry. The equation represents a model that assumes a finite length of wire. We find that assuming an infinite length model will lead to a trivial solution.

4.1.5 Relationship Between Linear Voltage Transformer Action and Biot-Savart Principles

Equation 4.1.4-3 is the key design equation needed for calculating the output voltage V_S for specific microsensor geometries. Important parameters that strongly affect the output voltage in the secondary coil. are included within equation (4.1.4-3). A detail numerical calculation using 4.1.4-3 is paramount for the following reasons:-

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- determination of the best operating distance between the two coils,
- determination of most reasonable operating frequency,
- determination of best operating linear region
- analysis of properties of the materials to be used

The effect of frequency f, coil turns M, N, dimensions b_i, b_j and coil gap g will now be evaluated for specific geometries. The following constants are selected for the analysis based on system-level considerations:-

Primary coil current I_p =10mA

Frequency f = 2MHz

Relative Permeabilty=1

4.2 Effects of Number of Turns M, N and Coil Gap g Between Coils on Output Voltage V_s

We proceed to analyze the voltage output response to changing coil gap g, while varying the number of primary turns M. The effect of number of primary and secondary coil turns is evaluated with a conductor Pitch of 8um. This dimension is compatible with the design rule of NJIT Microelectronics Research Center where the device would be fabricated using 4um conductor widths. Figure 4-4, shows the output voltage response for different primary coil turns with gap g for various secondary coil turns (pitch = 8um). The maximum number of secondary coil turns is eight because the walls of the silicon cavity is a little less than 200um in diameter. Therefore, the maximum sidelength of 128um creates a diagonal of 182um. The number of primary turns is set at three. This number is chosen arbitrarily. Also, given that the diaphragm deflects more at the center, fewer turns would be loaded at the center to achieve appreciable deflection with the diaphragm. From fig. 4-4 we see that higher V_S of 200mV is obtained with a secondary-primary turns ratio M/N of 8/3.

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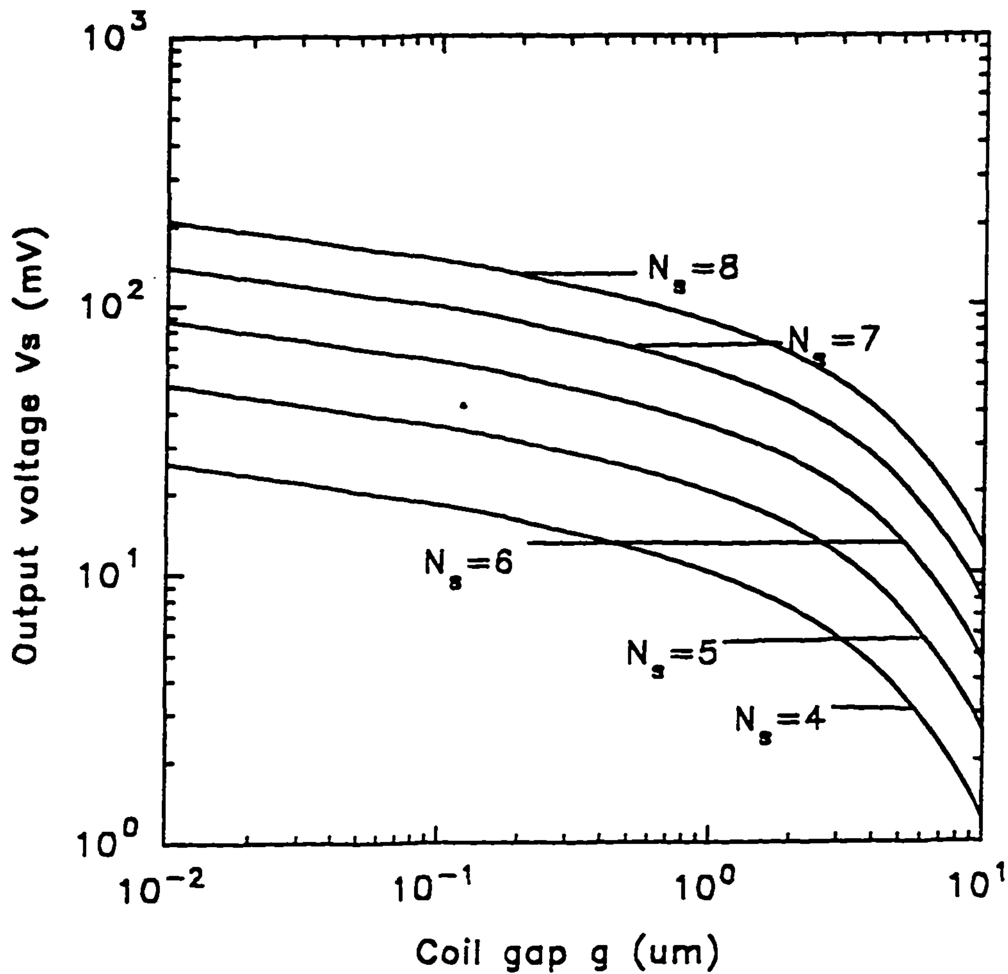

Fig. 4-4 Output voltage Vs as function of coil gap for various secondary coil turns.

We observe that as g increases, the output voltage initially drops slowly then rapidly. This plot is similar to that of Wagner *et al* (5) in which a magnet is used in place of current-carrying primary coil as a source of magnetic field. It is of interest to note that the output voltage V_S is proportional to g^{-2}. It is also interesting to note that when g approaches zero, the output voltage Vs approaches a quantity equal to a factor of the primary voltage. A close-up assessment of the coil gap is made by reducing the gap to 5um. This is shown in fig. 4-5.

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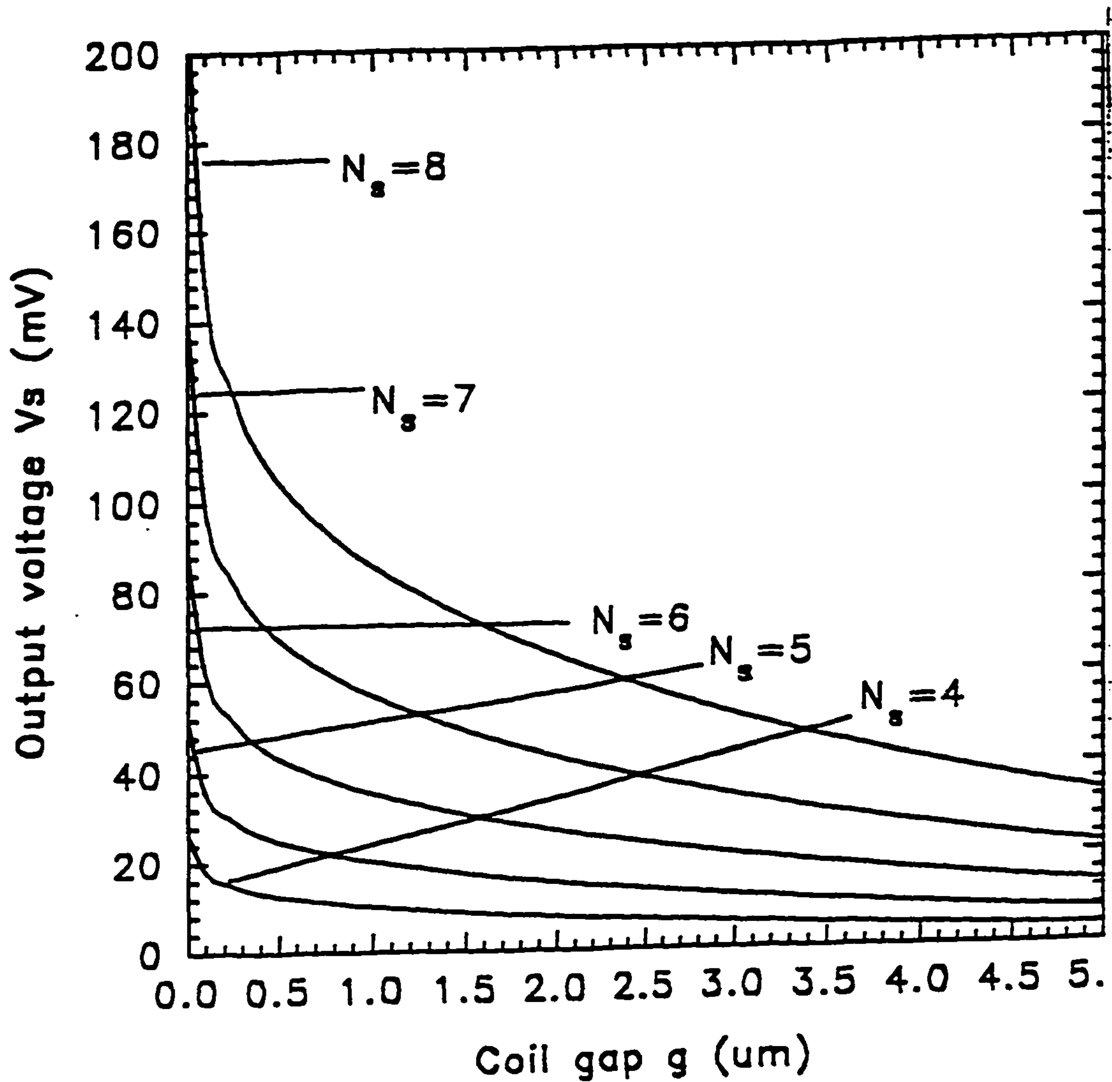

Fig. 4-5 Voltage output versus coil gap for various secondary coil turns (coil gap range of 0-5 um) due to input current I_p

Figure 4-5 also indicates the apparent non-linear response of the output voltage V_S. The critical range of distance between the two coils where the device is proposed to operate is

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within one to eight microns. A considerable degree of linearity in output voltage response is clearly evident as the two coils approach each other within 5um as shown in fig 4-5.

To determine how much window of linearity we have, the output voltage gradient with respect to coil gap g is evaluated. We are also interested in knowing the sensitivity of the output voltage to changing coil gap g. The derivative of the output voltage V_S with respect coil gap g is expressed as

$$\frac{d}{dg}V_S = \frac{d}{dg}\frac{\omega\mu I\cos(\omega t)}{\pi}\sum_{ij}^{M}\sum_{j}^{N} Q_{ij} \tag{4.2-1}$$

$$= \frac{\omega\mu I\cos(\omega t)}{\pi}\sum_{ij}^{M}\sum_{j}^{N} U_{ij} \tag{4.2-2}$$

where U_{ij} is expressed as

$$g\frac{b_i^2 b_j}{\frac{b_i^2}{4}+g^2}\left\{\frac{2}{\frac{b_i^2}{4}+g^2}\ln\left[\frac{-\frac{b_i}{2}+\sqrt{\frac{b_i^2}{4}+g^2}}{\frac{b_j-b_i}{2}+\sqrt{\frac{(b_j-b_i)^2}{4}+g^2}}\right]+\frac{\sqrt{\frac{b_i^2}{4}+g^2}-\sqrt{\frac{(b_j-b_i)^2}{4}+g^2}}{\sqrt{\frac{b_i^2}{4}+g^2}+\sqrt{\frac{(b_j-b_i)^2}{4}+g^2}}\right\}$$

Assuming the last term to be negligible, the output voltage gradient now becomes

$$\frac{d}{dg}V_s = \frac{\omega\mu I\cos(\omega t)}{\pi}\sum_{ij}^{M}\sum_{j}^{N}\frac{2gb_i^2 b_j}{\left[\frac{b_i^2}{4}+g^2\right]^2}\ln\left[\frac{-\frac{b_i}{2}+\sqrt{\frac{b_i^2}{4}+g^2}}{\frac{b_j-b_i}{2}+\sqrt{\frac{(b_j-b_i)^2}{4}+g^2}}\right] \tag{4.2-3}$$

Figure 4-6 shows the gradient of the output voltage response with respect to

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distance between the two coils. We note that the point of maximum output voltage sensitivity of 4.3kV/m is obtained at coil gap of around 3um. This confirms that the proposed device has the potential of being a highly sensitive pressure sensor, especially at low pressures.

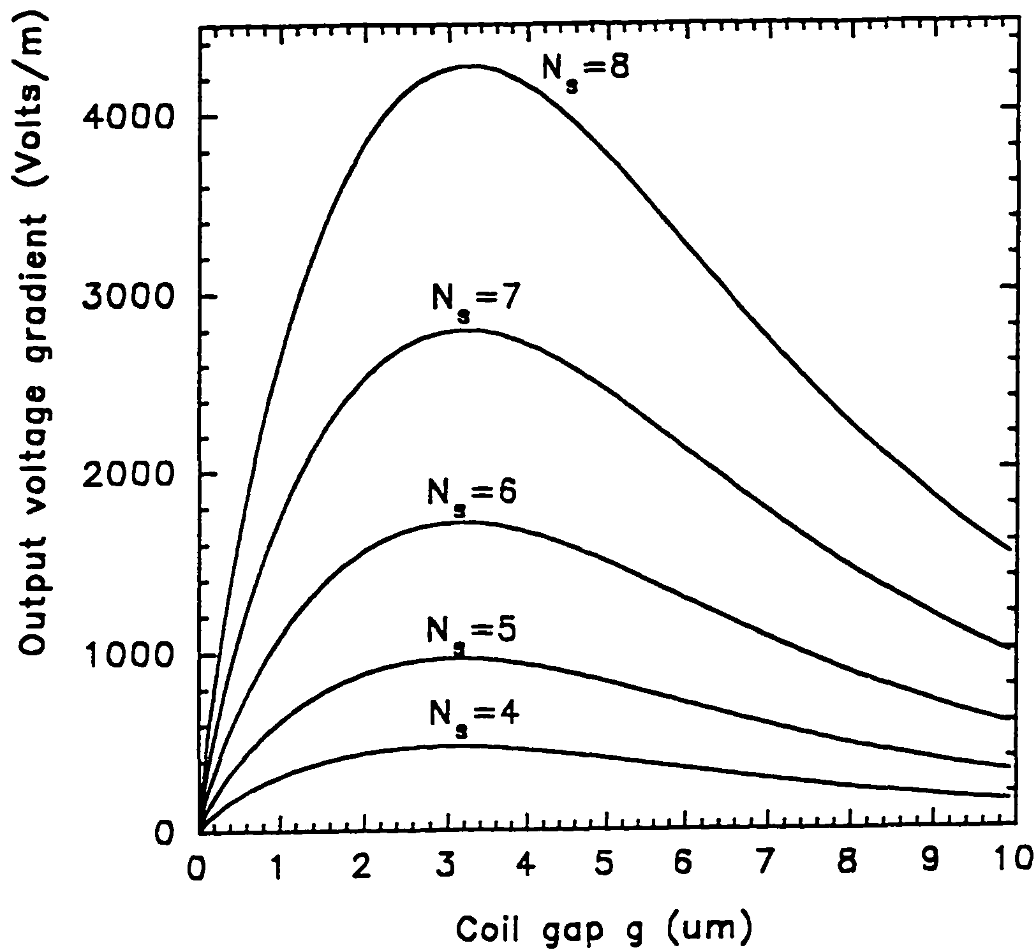

Fig. 4-6 Output voltage gradient with respect to coil gap.

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CHAPTER 5
MICROMECHANICAL DESIGN PRINCIPLES

5.1 Overview

Generally, the design of devices that sense physical phenomena and electrical readouts call for the interpolation of two or more kinds of mathematical relationships. In the design of the proposed high temperature pressure sensor, the equations that explain the physical phenomena, (i.e. pressure and diaphragm deflection) are interpolated with equation of the output voltage. The equations of deflecting diaphragms are in two categories. One supports maximum diaphragm deflections less than its thickness while the other supports diaphragms with maximum deflections larger than its thickness. One fundamental reason for having separate expressions has to do with the problem of linearity in membrane deflection. It was found that there was need to restrict the maximum deflection to less than the membrane thickness for applications of short range pressure measurement in order to preserve a reasonable degree of linearity of diaphragm deflection in response to applied pressure. For wide band pressure measurements, however, the deflection of the diaphragm in response to applied pressure is no longer linear. A correction to the small deflection is therefore made to describe it. Design considerations is therefore based on both small and large deflections in order to broaden the range of application. For the proposed high-temperature pressure sensor, the reliability of the device is strongly dependent on membrane integrity.

For the device to be used continuously over a long period of time, the membrane

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must be capable of responding to applied pressure with precision and with little hysterisis. To achieve this, it means the membrane must retain its elastic property after applied maximum pressure differential. To that effect, there is need to choose materials with an appreciable linear region on the stress-strain curve shown in fig. 5-1. In this figure, for the diaphragm to retain its elastic integrity, the stress induced by pressure must not exceed point A (yield point).

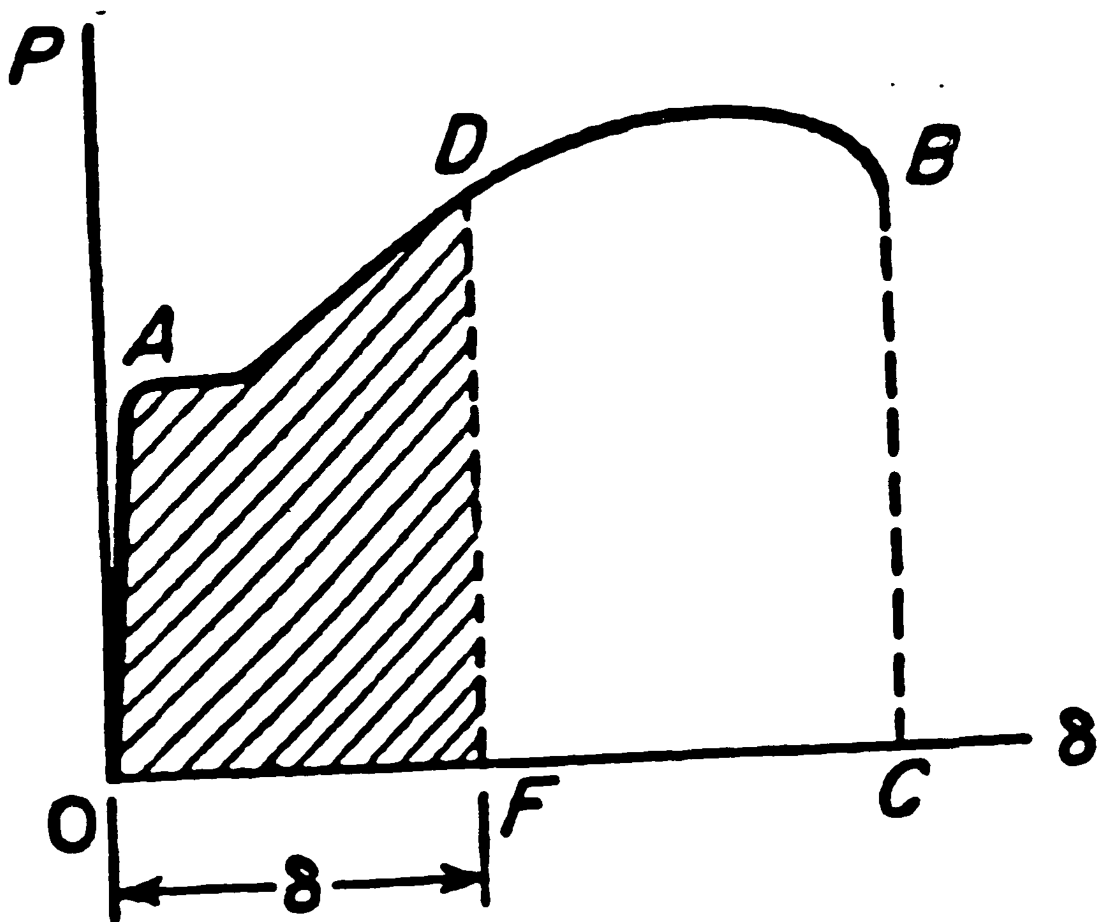

Fig. 5-1 Typical stress-strain curve

In essence, the operating point should swing between O and A. If the stress

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reaches point D (elastic limit), there is very strong likelihood the diaphragm would lose a huge chunk of its elasticity and become permanently deformed. The specification of this device demands a maximum of 2% of strain. The Young's modulus of the materials should be reasonably high. Care must also be taken not to choose materials with too sharp slopes. This might lead to high rigidity and hence cracking. In this design, polysilicon (Young's modulus = 190GPa) and silicon nitride (Si_3N_4) (Young's modulus=380GPa) (31) are selected for various reasons that would be enumerated from time to time. The membrane is composed of an upper polysilicon layer of 1μm, a low temperature (LTO) deposited SiO_2 that is 20nm thick, followed by sequential layers of Si_3N_4 with combined thickness of 0.3um. Although Si_3N_4 has a high Young's modulus, it has the tendency to crack as its thickness increases during deposition due to internal stress. Advantage is taken of its high Young's modulus and rigidity but thickness is kept low. Therefore, the polysilicon is used to increase the membrane thickness. Another advantage of Si_3N_4 that is utilized is its hardiness (3486kg/mm^2) and low Temperature Coefficient of Expansion (TCE = 0.8ppm/^{o}C). These properties are utilized to contain the thermal expansion of the tantalum Silicide ($TaSi_2$) (TCE = 8ppm/^{o}C) conductors that are encapsulated within nitride layers. This aspect would be discussed extensively in chapter seven.

5.2 Deflection and Stress Analysis of Thin Circular Diaphragm

The goal of this section is to establish the relationship between the equation of symmetrical bending of clamped circular plates with the output voltage equation. Large deflection of circular plates is governed by the equation below (10),

$$w = 0.662a\left(\sqrt[3]{\frac{Pa}{Eh}}\right) \qquad (5.2\text{-}1)$$

where

w=deflection of membrane (μm)

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a=radius of membrane (μm)

P=applied pressure (Pascal)

E=Young's modulus (Pascal),

h=membrane thickness (μm)

The Young's modulus E is mathematically expressed as E = $\dfrac{Stress}{Strain} = \dfrac{Stress}{(L_f - L_o)/L_o}$, where L_f and L_o are the final and initial length of the material, respectively.

It is necessary to analyze the stress profile that is characteristically inherent in large deflections. It is found that the membrane center and edge exhibit higher stress than any section. It turns out that the section between the center and the edge exhibit well distributed stress contour as has been confirmed in some Finite Element Analysis (FEA) (32). In large deflection analysis, the stress at the center and edge of the membrane is expressed respectively as:-

$$(\sigma_r)_{r=0} = 0.432\left(\sqrt[3]{\frac{EP^2a^2}{h^2}}\right) \tag{5.2-2}$$

and

$$(\sigma_r)_{r=a} = 0.328\left(\sqrt[3]{\frac{EP^2a^2}{h^2}}\right) \tag{5.2-3}$$

We wish to evaluate the membrane deflection as it relates directly with applied pressure. from this analysis, it would become possible to determine what safe range of pressure the device can sustain without deforming. A stress analysis will then be conducted to determine the percent strain. The deflection of the membrane due to applied pressure is shown in fig. 5-2. We see that for a 450kPa maximum pressure differential, there is a 3μm membrane deflection. For this deflection the center and edge stress induced by the pressure is evaluated using equations 5.2-2 and 5.2-3, respectively. This is shown in

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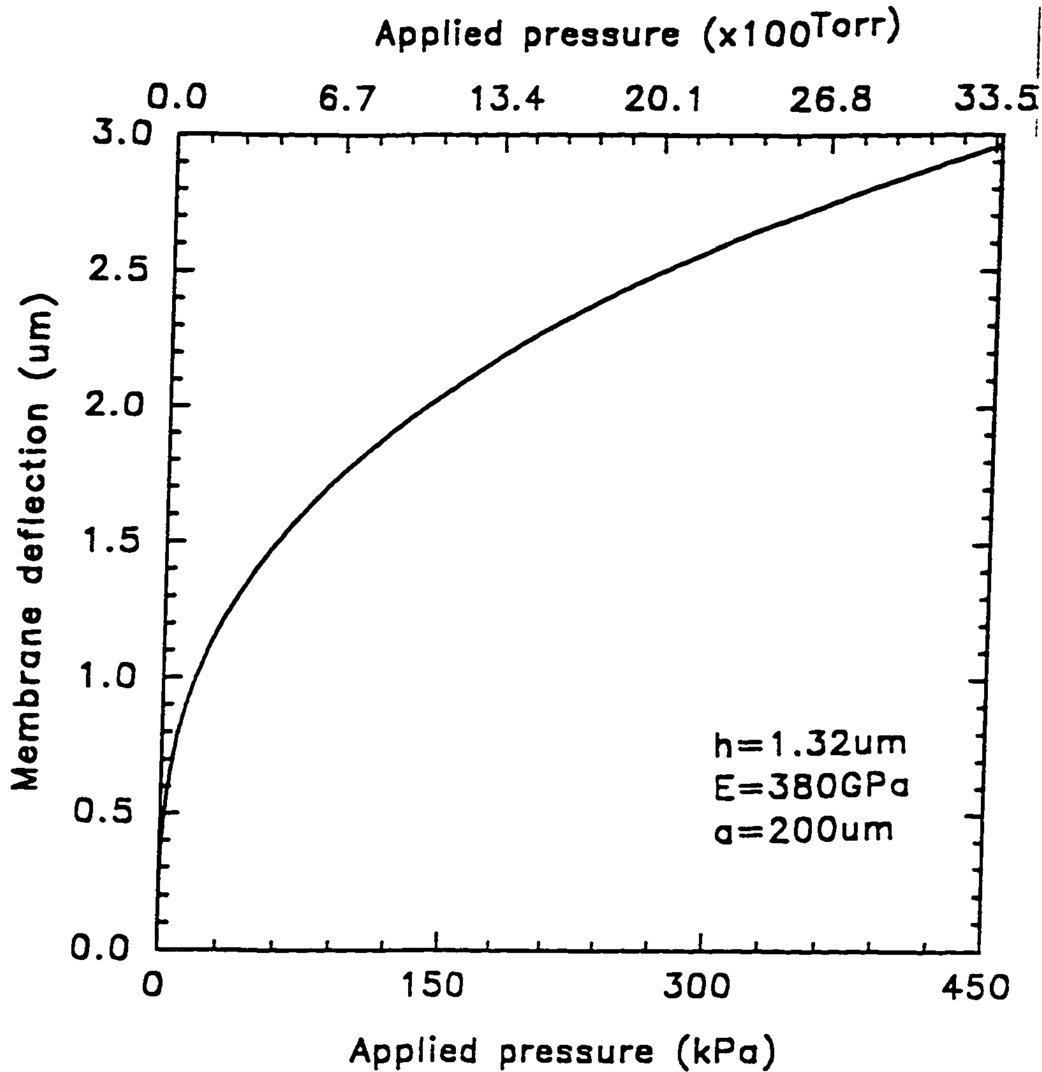

Fig. 5-2 Membrane center deflection versus applied pressure (Large deflection)

fig. 5-3. The maximum center stress is 320MPa for a maximum pressure differential of 450kPa while the edge stress is about 250MPa. To calculate the strain, the respective stress is divided by the nitride Young's modulus. For center stress the strain is

$$\frac{320 \times 10^{6}\ \text{Pa}}{380 \times 10^{9}\ \text{Pa}} \times 100 = 0.084\%$$

and for the edge strain is

$$\frac{250 \times 10^{6}\ \text{Pa}}{380 \times 10^{9}\ \text{Pa}} \times 100 = 0.067\%$$

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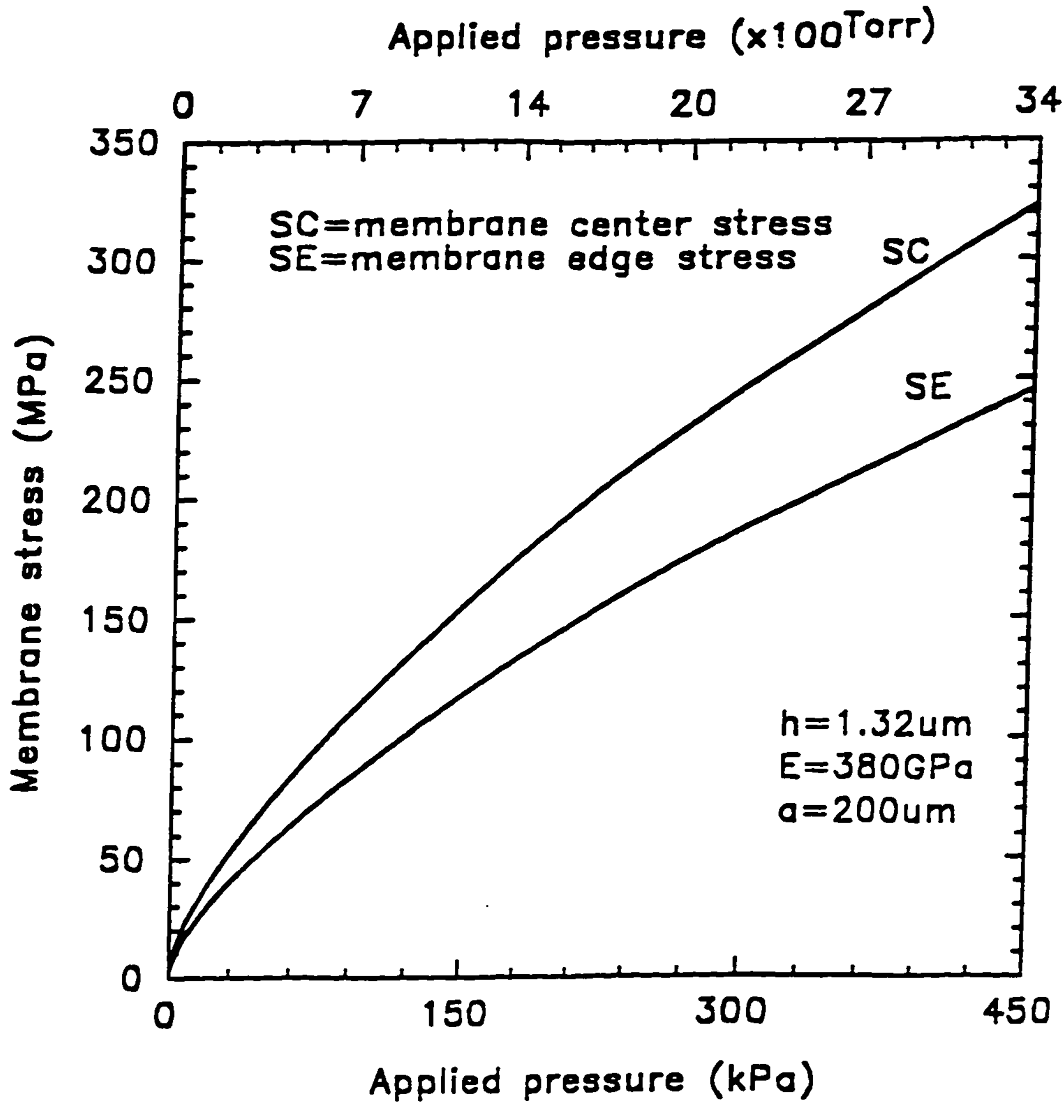

Fig. 5-3 Membrane center and edge stress versus applied pressure (Large deflection)

From the above evaluations, it has been determined that the $3\mu m$ deflection due to 450kPa maximum pressure differential causes a center and edge strain of less than 2%, the specification ceiling.

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When the maximum deflection of a clamped circular plate is less than its thickness, the equation that describes it is expressed as (10)

$$w = 0.89 \frac{Pa^4}{64D} \quad (5.2\text{-}4)$$

where

D = fluxural rigidity of the membrane material and expressed as:-

$$D = \frac{Eh^3}{12\left(1 - \upsilon^2\right)} \quad (5.2\text{-}5)$$

where

ν = Poisson constant

The total stress on the membrane associated with such small deflection is expressed as:-

$$\left(\sigma_r\right)_{max} = \frac{3}{4} \frac{Pa^2}{h^2} \quad (5.2\text{-}6)$$

The choice of large or small deflection equation, as stated before, is basically dictated by device application. A deflection and stress analysis is also conducted on small deflections. Figure 5-4 shows the deflection of the membrane in response to applied pressure. It is interesting to note the linear response of the deflection to applied pressure as evidently predicted from equation 5.2-5. For a membrane deflection of 1.3μm, the maximum applied pressure differential is 75kPa. The stress response of the membrane is determined using equation 5.2-6 and plotted in fig. 5-5. The maximum stress at maximum differential pressure of 75kPa is found to be 315MPa. The corresponding strain is calculated to be 0.083%.

From the above analysis, the necessary precautionary measures against mechanical failure of the membrane has been established. These equations of membrane deflections form the foundation of the electromechanical relationship, and would be substituted, where need be, in the output voltage equation.

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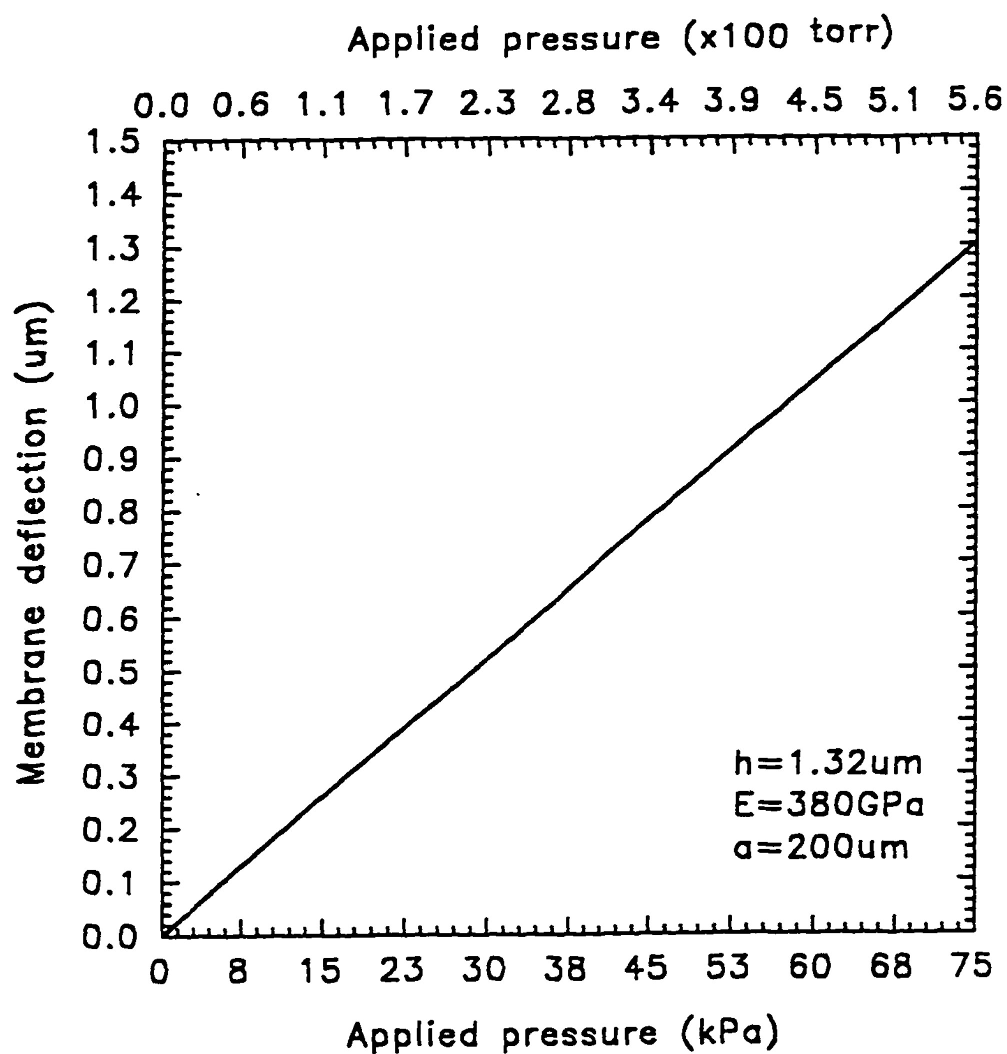

Fig. 5-4 Membrane deflection versus applied pressure (Small deflection)

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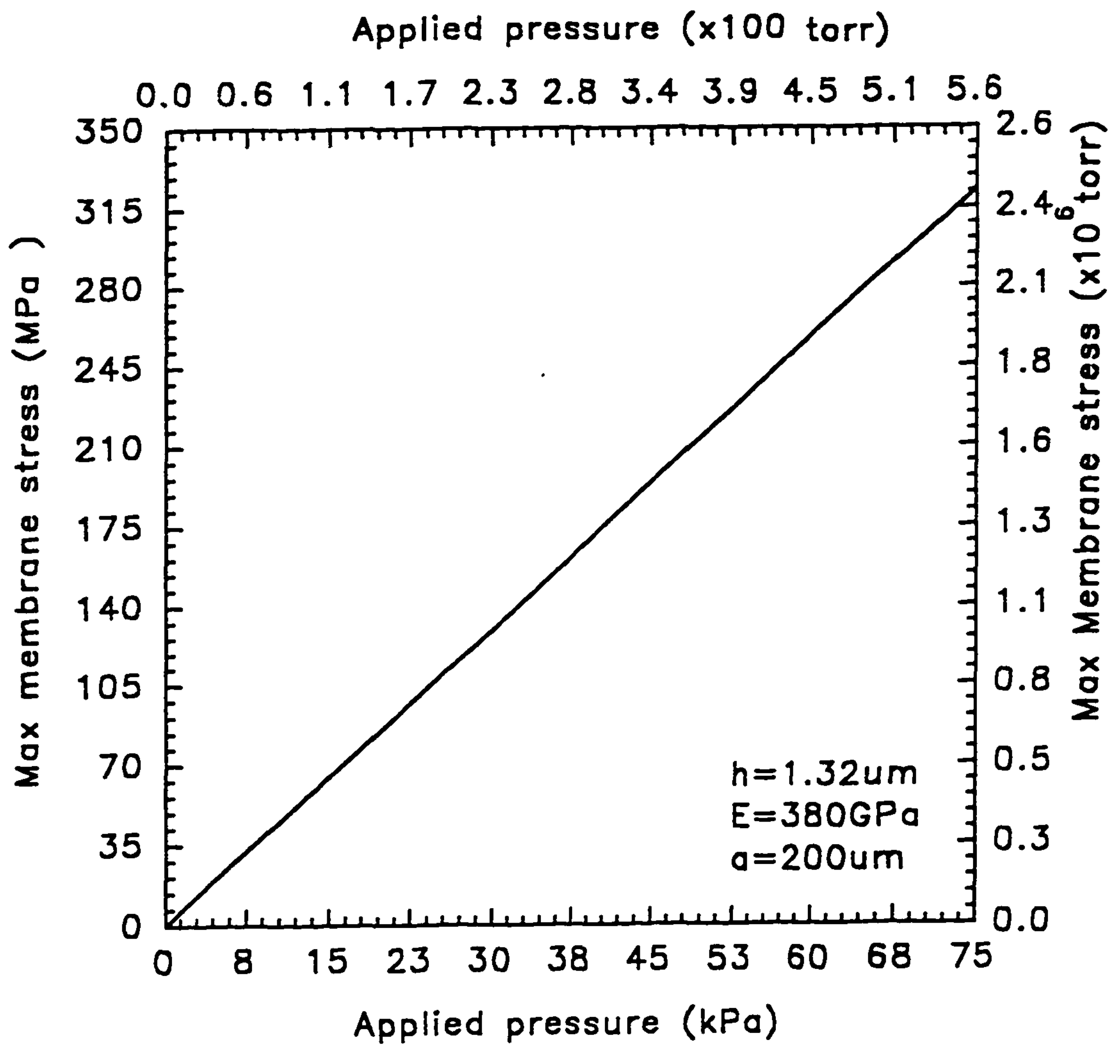

Fig. 5-5 Maximum membrane stress versus applied pressure (Small deflection)

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CHAPTER 6
DEVICE DESIGN

6.1 LVDT Device Design

In chapter four, the mathematical derivation of the output voltage based on the proposed coil geometry is established. Chapter five essentially presents the functional equations as they relate to physical deflection of diaphragms and associated stress. This chapter combines the established equations of the two proceeding chapters to produce the basis for the design of the device. As a result, it becomes possible to resolve attendant issues that are paramount in sensor designs. This chapter, therefore, discusses the following issues for small and large deflections:-

- Transfer function calculation relating coil gap and output voltage
- Output voltage sensitivity to applied pressure
- Output voltage linearity of response and associated percentage errors from the ideal situation.

6.1.1 Transfer Function Calculation

The transfer function calculations for small and large diaphragm deflections are presented. It essentially evaluates the induced voltage V_S in the secondary coil by current flowing through the primary coil while pressure is uniformly applied on the membrane. In this regard, the deflection equations 5.2-1 and 5.2-4 for large and small deflections, respectively, are algebraically related to coil gap g. We recall in chapter four that the output voltage V_S is proportional to the inverse of the square of the gap between the two coils. Generally, the algebraic relations between g and membrane deflection is expressed

as, $g = g_O - w$ (6.1.1-1)

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where g_o is the initial coil gap (um) and w the membrane deflection (um). We see from this equation that when w is equal to go, g becomes zero. This means a case when the membrane has deflected to its limit, to the point of 'touching' the secondary coil. The challenge is to model the device such the coil gap and membrane deflection are inter-related.

We now proceed to evaluate the output voltage as function of membrane deflection due to applied uniform pressure. For sake of convenience, the output voltage equation 4.1.4-3 is reintroduced below:-

$$V_S = \frac{\omega \mu I \cos(\omega t)}{\pi} \sum_{ij}^{M} \sum_{j}^{N} Q_{ij} \qquad (6.1.1\text{-}2)$$

where

$$Q_{ij} = \frac{b_i^2 b_j}{\frac{b_i^2}{4} + g^2} \ln \left[\frac{\frac{b_j - b_i}{2} + \sqrt{\left(\frac{b_j - b_i}{2}\right)^2 + g^2}}{-\frac{b_i}{2} + \sqrt{\frac{b_i^2}{4} + g^2}} \right] \qquad (6.1.1\text{-}3)$$

With respect to large deflections, coil gap g, in 6.1.1-1 is expressed as:-

$$\begin{aligned} g &= g_o - w \\ &= g_o - 0.662a \left[\sqrt[3]{\frac{qa}{Eh}} \right] \end{aligned} \qquad (6.1.1\text{-}4)$$

Substituting 6.1.1-4 for g in 6.1.1-3, the output voltage V_S as it relates to membrane deflection yields:-

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$$V_S = \frac{\omega \mu I \cos(\omega t)}{\pi} \sum_{ij}^{M} \sum_{j}^{N} Q_{ij} \qquad (6.1.1\text{-}4a)$$

where Q_{ij} now becomes a function of membrane deflection, expressed as

$$\frac{b_i^2 b_j}{\frac{b_i^2}{4} + \left(g_o - 0.662a\left(\sqrt[3]{\frac{Pa}{Eh}}\right)\right)^2} \ln\left[\frac{\frac{b_j - b_i}{2} + \sqrt{\left(\frac{b_j - b_i}{2}\right)^2 + \left(g_o - 0.662a\left(\sqrt[3]{\frac{Pa}{Eh}}\right)\right)^2}}{-\frac{b_i}{2} + \sqrt{\frac{b_i^2}{4} + \left(g_o - 0.662a\left(\sqrt[3]{\frac{Pa}{Eh}}\right)\right)^2}}\right]$$

(6.1.1-4b)

From this equation, it is possible to evaluate the voltage response to applied pressure. Let us choose g_o to be 3μm, where g_o is the maximum distance between the two coils. We recollect in chapter four that the near linearity range is between zero and ten microns. This distance essentially represents the limit after which output voltage becomes seriously nonlinear and drops off sharply. The objective is to remain as close as possible to the area where output voltage is above noise level.

We wish to determine the response of the output voltage to changes in applied pressure. The radius, *a*, thickness, *h*, and Young's modulus, *E*, of the membrane is fixed. We begin with a membrane radius and effective thickness of 100μm and 1.32μm, respectively, and Young's modulus of 380GPa. Based on the turns ratio analysis of chapter four the secondary and primary coil turns ratio is set at 8:3. Given the above parameters, the output voltage response as function of applied pressure for large

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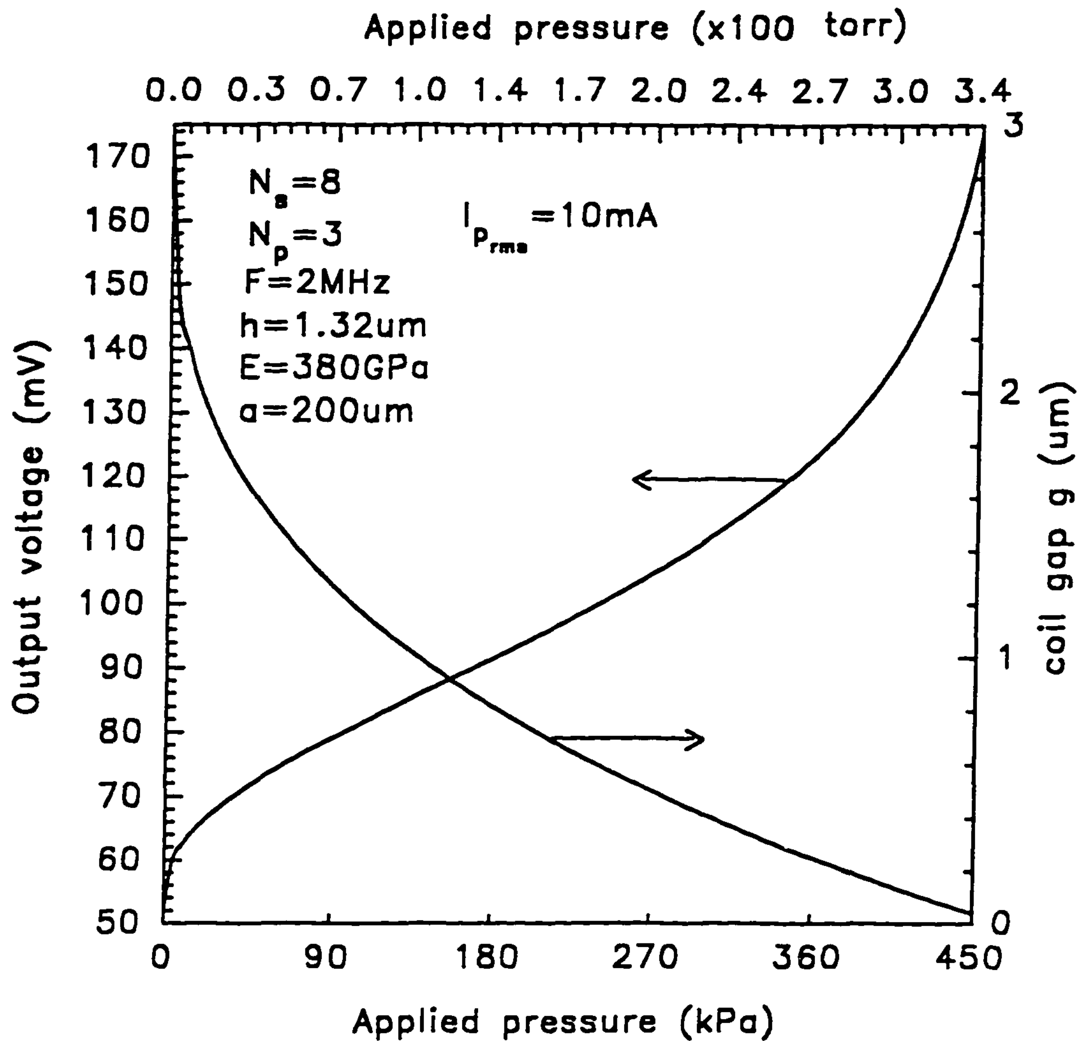

Fig. 6-1 Output voltage versus applied pressure (Large deflection)

deflections is evaluated and shown in fig. 6-1. The maximum output voltage for 2MHz input primary current of 10mA (rms) is seen to be 175mV, at maximum pressure differential of 450kPa (34×10^2Torr) for a membrane deflection of about 3μm. The offset output voltage at zero pressure is 50mV. This gives a dynamic range (span) of 125mV. A plot of the coil gap change is also shown on the plot. This gives us an appreciation of how the coil gap and output voltage are related. For dynamic range of 125mV, the coil gap decreases from 3μm to 0.2μm, translating into a membrane deflection of 3μm. This is in

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agreement with the membrane deflection at 450kPa pressure differential evaluated and plotted in fig. 5-1. The dependence of the output voltage on frequency is apparent. This frequency dependency of the output voltage will be discussed in subsequent chapters.

Small deflection analysis is also conducted. In this case the equation for small membrane deflection replaces *w* in equation. 6.1.1-4 and expressed as

$$g = g_o - w = g_o - 0.89\frac{Pa^4}{64D} \qquad (6.1.1\text{-}5)$$

Substituting for g in equation 6.1.1-3, the output voltage as function of applied pressure is expressed as

$$V_S = 4\frac{\omega\mu I\cos(\omega t)}{\pi}\sum_{ij}^{M}\sum_{j}^{N} Q_{ij} \qquad (6.1.1\text{-}6)$$

where Q_{ij} now becomes a function of small membrane deflection, expressed as

$$\frac{b_i^2 b_j}{\frac{b_i^2}{4} + \left(g_o - 0.89\frac{Pa^4}{64D}\right)^2}\ln\left[\frac{\frac{b_j - b_i}{2} + \sqrt{\left(\frac{b_j - b_i}{2}\right)^2 + \left(g_o - 0.89\frac{Pa^4}{64D}\right)^2}}{-\frac{b_i}{2} + \sqrt{\frac{b_i^2}{4} + \left(g_o - 0.89\frac{Pa^4}{64D}\right)^2}}\right]$$

(6.1.1-7)

The output voltage response Vs to applied pressure in this case is plotted and shown in fig. 6-2. We observe the linearity of the response to applied pressure, a sharp contrast from that of large deflections. However, the maximum output voltage is 130mV for a

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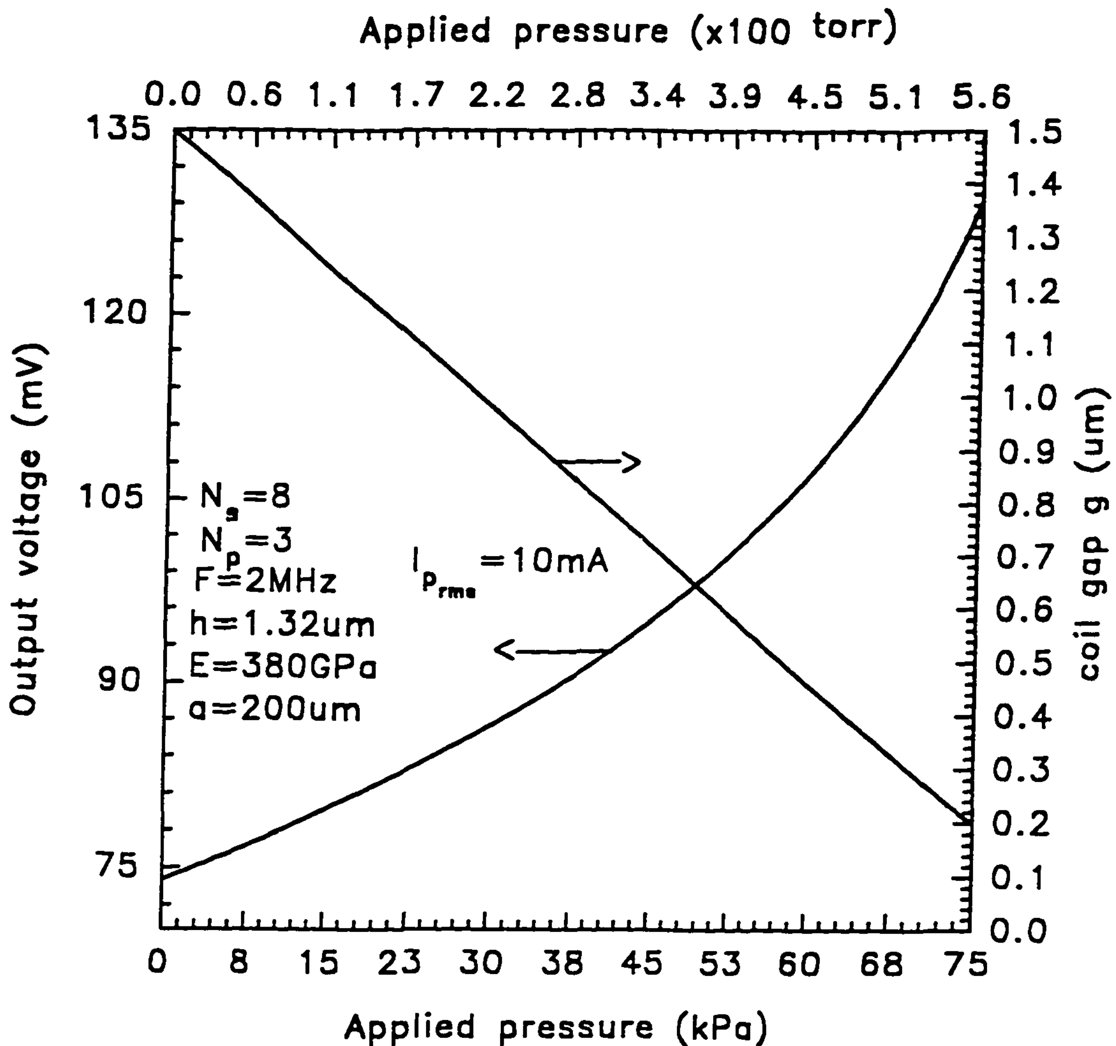

Fig. 6-2 Output voltage versus applied pressure(Small deflection)

maximum differential pressure of 75kPa. For an offset voltage of 75mV at 1.5μm initial coil gap, the dynamic range is 55mV, at a membrane deflection of 1.3μm.

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6.1.2 Linearity of Response

The linearity of the output voltage of any device is of utmost importance. The degree of linearity determines the accuracy of the device. In addition, it determines to what degree a correction circuitry would have to be added. This translates into cost and space management. The goal therefore is to ensure that the device output is as close to first order response as possible. Usually, this true output of the device is compared with a Best Fit Straight Line (BFSL). The amount of deviation of the output voltage from this ideal line is defined as the linearity error. In applying this principle for large membrane analysis of the output voltage, the true output is compared with the ideal curve. We observe from fig.6-3 the evident non linearity of the output voltage response to applied pressure. This

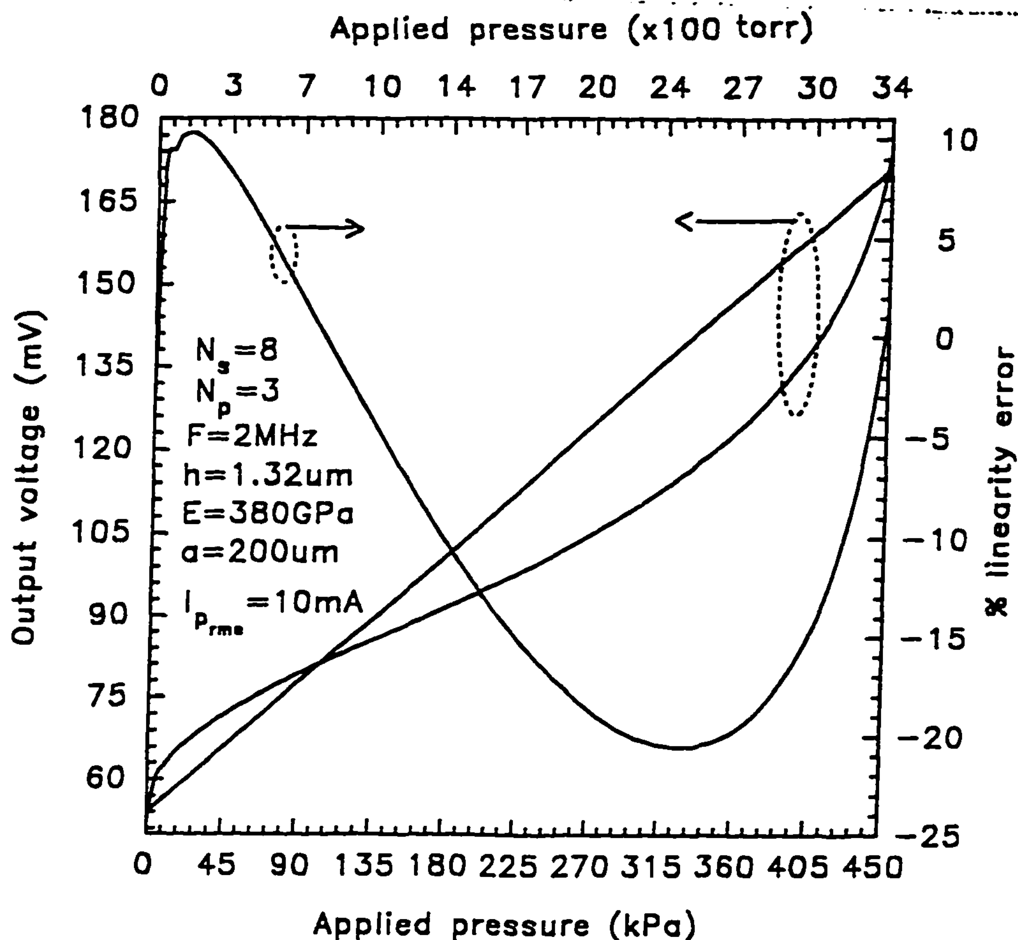

Fig. 6-3 Percent deviation from linearity versus applied pressure (Large deflection)

We see that the full scale linearity error is about 1.5%.

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In the low pressure regime, using small deflection analytical approach, the linearity

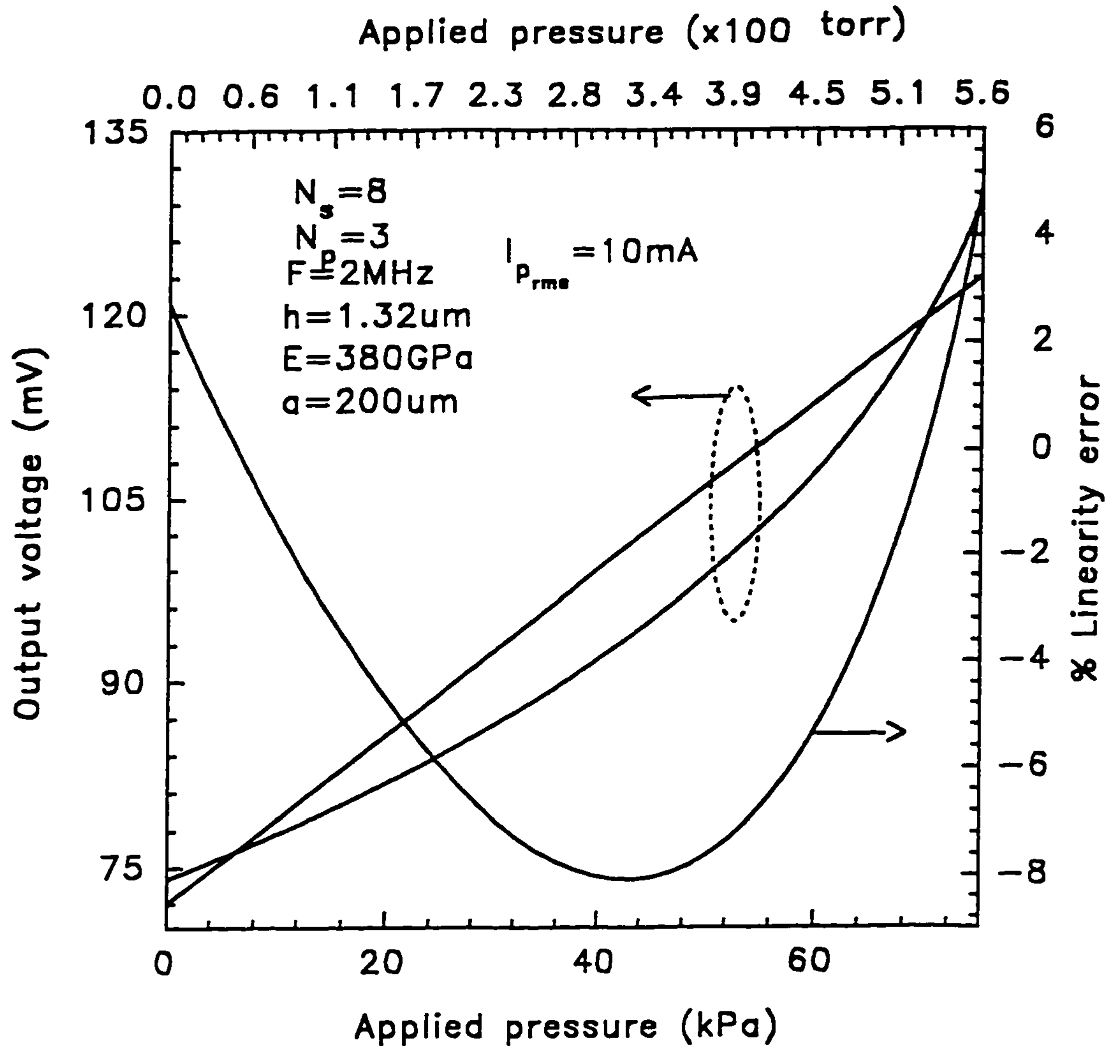

Fig. 6-4 Percent deviation from linearity versus applied pressure (Small deflection)

condition is predicted by equation 6.1.1-4. It is seen that the response is inversely proportional to applied pressure. The percent linearity error is evaluated and plotted in fig. 6-4. Error is determined using the same procedure as done with large membrane deflection. The result of the evaluation is shown in fig. 6-4. We note the apparent shift in linearity response of the output voltage when plotted against the ideal curve. From this

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comparison it is possible to deduce the percent linearity error which is shown in the figure. We observe that the maximum percent linearity error is about 8% at close to midscale. The linearity error percent at full scale is 5%.

6.1.3 Output Voltage Sensitivity to Pressure

It is important to analyze the sensitivity of the output voltage to applied pressure. By taking the derivative of the output voltage with respect to applied pressure, the output voltage sensitivity can be evaluated. We realize, however, that there is a direct relationship between coil gap and pressure expressed as $g = g_O - w$. If we take the derivative of coil gap with respect to pressure, for large membrane analysis, we get

$$dg = -0.22a^2 \frac{1}{Eh}\left(\frac{Pa}{Eh}\right)^{\frac{-2}{3}} dP \qquad (6.1.3\text{-}1)$$

From equation 4.2-1 and 2,

$$\frac{d}{dg}V_S = \frac{d}{dg}\frac{\omega\mu I\cos(\omega t)}{\pi}\sum_{ij}^{M}\sum_{j}^{N} Q_{ij} \qquad (6.1.3\text{-}2)$$

$$= \frac{\omega\mu I\cos(\omega t)}{\pi}\sum_{ij}^{M}\sum_{j}^{N} U_{ij} \qquad (6.1.3\text{-}3)$$

where U_{ij} is

$$\frac{2gb_i^{\,2}b_j}{\left[\frac{b_i^{\,2}}{4}+g^2\right]^2}\ln\left[\frac{-\frac{b_i}{2}+\sqrt{\frac{b_i^{\,2}}{4}+g^2}}{\frac{b_j-b_i}{2}+\sqrt{\frac{(b_j-b_i)^2}{4}+g^2}}\right] \qquad (6.1.3\text{-}4)$$

by substituting for dg, with equation 6.1.3-1, we get

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$$\frac{d}{dg}V_S = \frac{\mathrm{d}}{-0.22a^2 \frac{1}{Eh}\left(\frac{Pa}{Eh}\right)^{\frac{-2}{3}} dP} V_S = \frac{\omega\mu I\cos(\omega t)}{\pi} \sum_{ij}^{M} \sum_{j}^{N} \mathrm{U}_{ij} \qquad (6.1.3\text{-}5)$$

Therefore,

$$\frac{d}{dP}V_S = -0.22a^2 \frac{1}{Eh}\left(\frac{Pa}{Eh}\right)^{\frac{-2}{3}} \frac{\omega\mu I\cos(\omega t)}{\pi} \sum_{ij}^{M} \sum_{j}^{N} U_{ij} \qquad (6.1.3\text{-}6)$$

where g in Uij is now is expressed in terms of P.

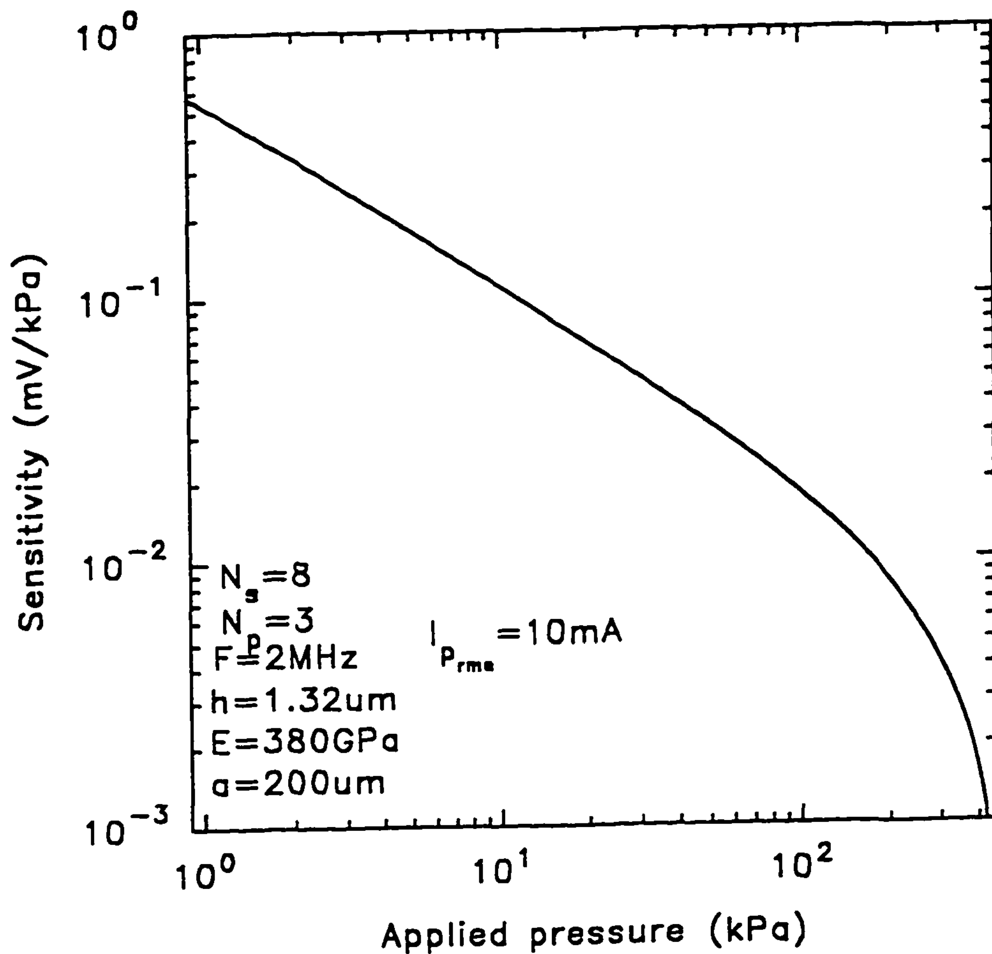

Fig. 6-5 Output voltage sensitivity versus applied pressure. (Large deflection)

We now have the Output voltage sensitivity to applied pressure for large

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membrane deflections. A plot of the Output voltage sensitivity to applied pressure for large deflection analysis is shown in fig. 6-5. This plot raises a lot of interesting issues. First, we notice that the output voltage sensitivity to applied pressure has a linear negative slope on the log scale, decreasing from a high sensitivity of 0.6mV/kPa at low pressure to .001mV/kPa at high pressure. Secondly, the high sensitivity at low pressures indicates that the device has potential for special applications in sub atmospheres. Another point raised by this plot is that to increase the sensitivity, the initial coil gap should be greater than 3um that has been used.

Small deflection analysis of the output voltage sensitivity to applied pressure is carried out by repeating similar procedure as is done in large deflection analysis. This time, however, the small membrane deflection equation of 6.1.1-5 is applied. By taking the derivative of g with respect to pressure, we get

$$dg = -0.89\frac{a^4}{64D}dP \tag{6.1.3-7}$$

By substituting for dg in 4.2-1, 2a, and 2b we determine the output voltage sensitivity to applied pressure for small deflections expressed as

$$\frac{d}{dP}V_S = -0.89\frac{a^4}{64D}\frac{\omega\mu I\cos(\omega t)}{\pi}\sum_{ij}^{M}\sum_{j}^{N}U_{ij} \tag{6.1.3-8}$$

where g in Uij has been replaced by 6.1.1-5. The sensitivity to pressure is plotted and shown in fig. 6-6. We notice the that the sensitivity is 0.062mV/kPa at full scale pressure differential. The change in sensitivity from zero to maximum pressure is small. This tells us that at low pressure regime and using the low deflection analysis, output voltage sensitivity to applied pressure is near constant. It generally confirms the fair linear response of the device at low pressure regime.

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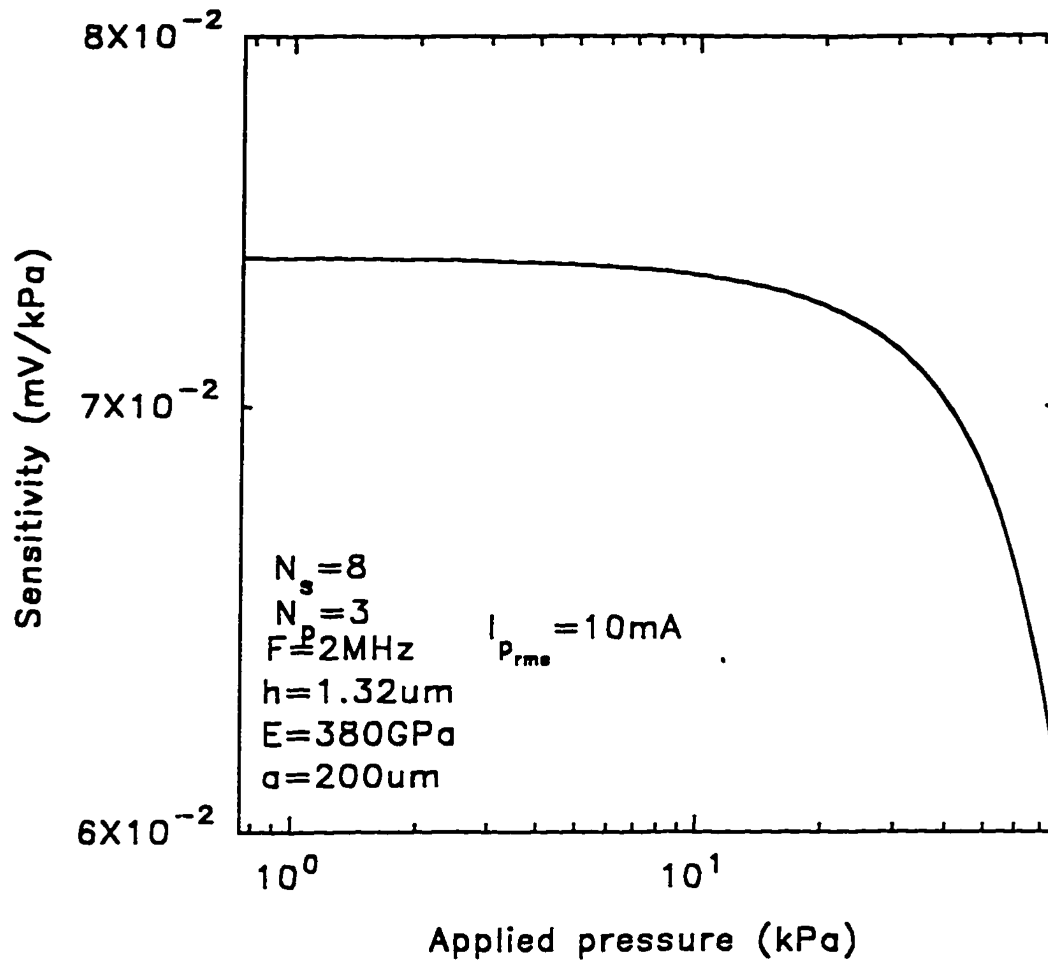

Fig. 6-6 Output voltage sensitivity versus applied pressure. (Small deflection)

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CHAPTER 7
IMPORTANT SECONDARY SENSITIVITIES

7.1 Effects of Temperature

The effects of temperature on device performance can be viewed from many perspectives. The main interest here is to investigate the areas where temperature effects are considered critical to device performance, reliability, and survivability. The main issues of discussion in this chapter is that of thermal stress, its effect on device performance, and also temperature effects on output voltage. From these effects, it would be possible to evaluate important device specifications and then determine if it offers any advantage at elevated temperatures. There are two kinds of stress: compressive and tensile. Figure 7-1a (33) shows a case of tensile stress in which the film on substrate tends to expand thereby forming a concave shape. Compressive stress is defined as when a film tends to bend such as to constrict its size, thereby forming a convex shape. Compressively stressed films on substrate is shown in fig 7-1b.

These stresses play very dominant roles in device performance and survivability at high temperatures. Most existing pressures sensors in one way or another suffer from thermal stress. At high temperatures, thermal mismatch between layers and other components become more pronounced due to differences in Thermal Coefficients of Expansion (TCE). The usual consequence is device short life span and subsequent failure. Thermal effects also create the redistribution of doped impurity concentrations profiles of piezoresistive, and capacitive pressure sensors and causes increased leakage currents. Pressure sensors using the piezoresistive properties of crystals also suffer considerably at high temperatures due to the thermal effect on the piezoresistive coefficient. Up to some point on the

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temperature scale, external circuitry and microprocessors are always needed to compensate for deviating

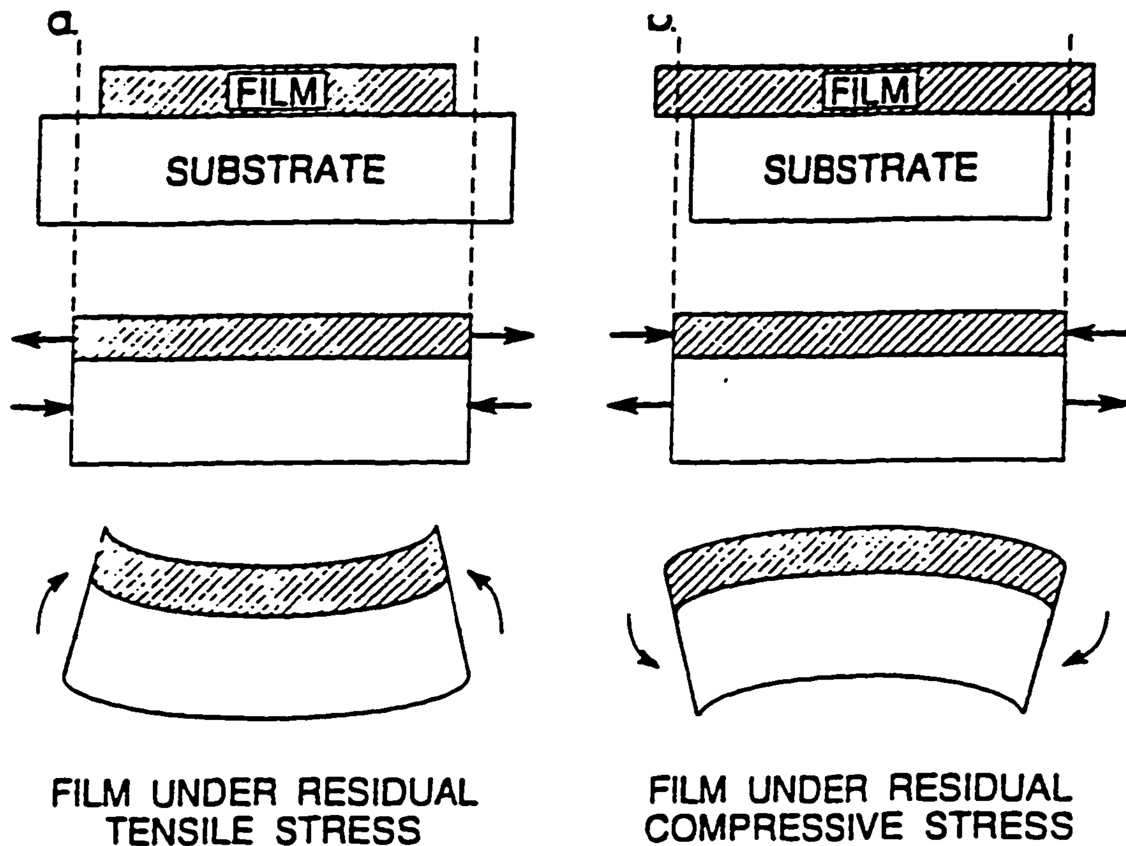

Fig. 7-1 (a), Example of residual stress of film on substrate. Film tends to form a concave bow. (b), Example of compressive stress of film on substrate. Film tends to form a convex bow (33).

output signals caused by thermal effects. Figure 7-2a is a typical example of the effect of temperature on the Motorola MPX100 piezoresistive pressure sensor. We notice the massive shift in output voltage of about 20mV at maximum pressure differential at 125°C. To control such runaway voltage output, common solution is to add temperature compensating external circuitry as shown in fig. 7-2b.

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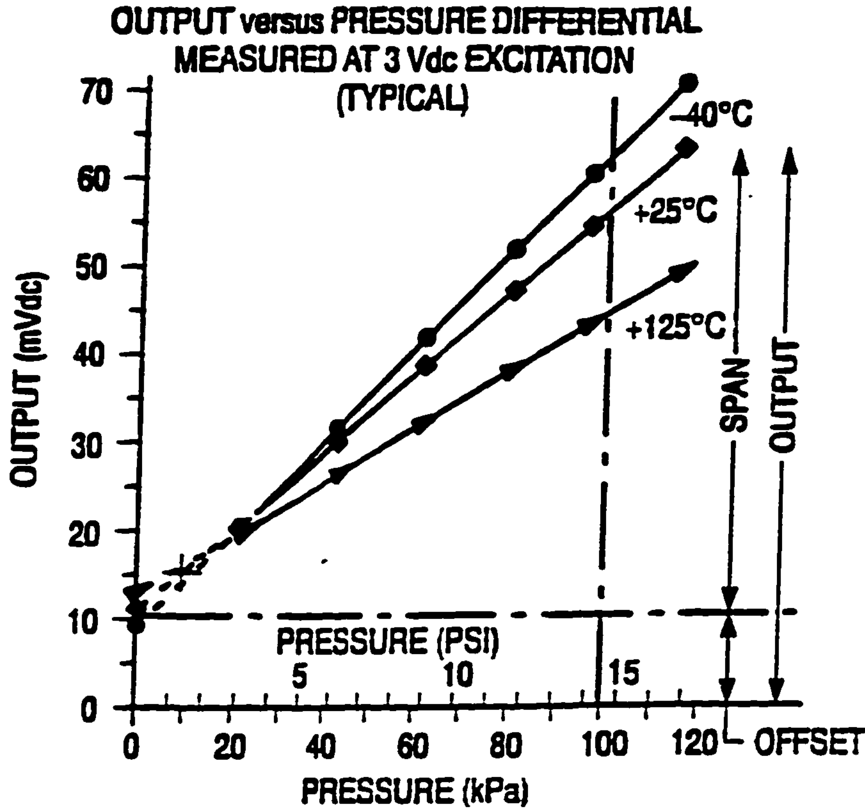

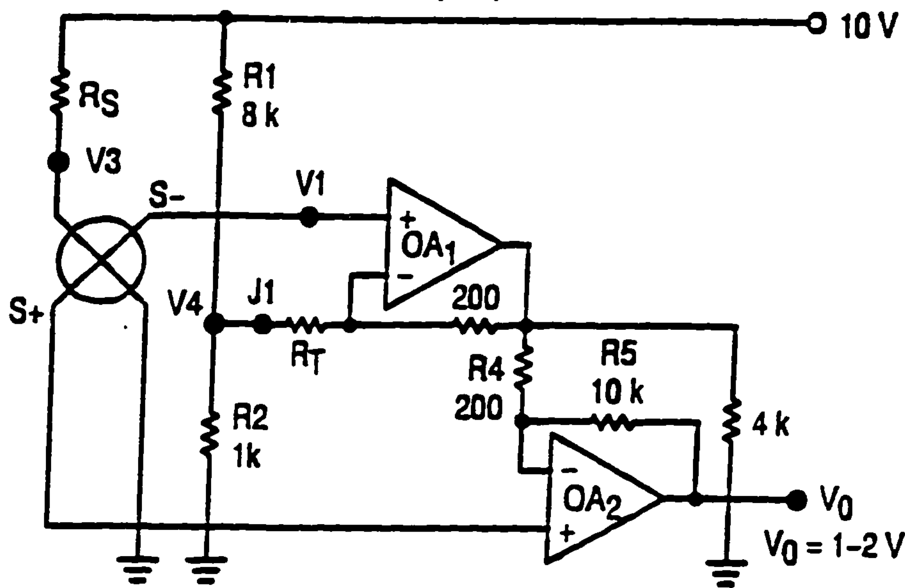

Fig. 7-2 (a) Graphical representation of temperature effect on voltage output on a Motorola MPX100 piezoresistive pressure sensor. (b), Temperature effect compensation circuit.[40]

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However, at very high temperatures of above 400°C, device reliability becomes questionable and such conditioning would require more expensive circuitry. The challenge therefore is to develop new generation of devices with outputs that are less sensitive to temperature changes, operate at higher temperatures, and would require minimum external compensation.

7.1.1 Temperature Effect on Stress

In this thesis, due consideration is taken for the choice of materials to be used for the device fabrication. The unique properties of tantalum Silicide ($TaSi_2$) and silicon nitride (Si_3N_4) are exploited in the development of the device. Table 7-1 shows a comparison of properties of important Silicides used in semiconductor technology (7). $TaSi_2$ has a high melting point of 2200°C (7). That makes it stable at 650°C. The low resistivity (50$\mu\Omega$-cm) (8) makes it viable as interconnect for low power dissipation devices. Cognizance is taken of its high Temperature Coefficient of Expansion (8ppm/°C). The properties of Si_3N_4 is taken advantage of in many ways. The method of **symmetrical layering** is used to counter the high TCE of $TaSi_2$. In this approach, $TaSi_2$ coils are completely sandwiched by layers of nitride. The nitride has a low TCE (0.8ppm/°C) and experimental results (28) show that it has excellent stability at high temperatures. Also its Young's modulus of about 380GPa and hardiness makes it a very strong material to withstand high pressures. In essence, this thesis combines these qualities in the development of the high temperature pressure sensor.

We wish to analyze the interface stress between $TaSi_2$ and Si_3N_4 because it forms the critical foundation upon which the proposed device lies. We wish to investigate the effect of temperature on the conductor. We realize from chapter four that the dimension of the conductor affects the output voltage. We therefore

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Silicide (Co-Sputtered)	Resistivity (μΩ-cm)	Thermal Expansion Coefficient (ppm/°C)
$TiSi_2$	25	12.5
$ZrSi_2$ (Metal on Poly)	35-40	8.3
$HfSi_2$	60-70	
VSi_2 (Metal on Poly)	50-55	11.2, 14.65
$NbSi_2$ (Metal on Poly)	50	8.4, 11.7
$TaSi_2$	50-55	8.8, 10.7
$MoSi_2$	100	8.25
WSi_2	70	6.25, 7.90
$CoSi_2$	25	10.14
$NiSi_2$	50-60	12.06
Pd_2Si (Metal on Poly)	30-35	
PtSi	28-35	

Table 7-1 Comparison of some properties of Silicides

need to know what extent the conducting element deviates from its normal (room temperature) dimension. From such investigation, it would become possible to extract the Temperature Coefficient of Offset (TCO) of the device- a figure that determines how much deviation from nominal value the device suffers due to

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changing temperature. Naturally, the wish is for very low TCO. The Output voltage sensitivity to temperature will also be investigated to determine how responsive the device is to temperature. Again, the goal is for very low Temperature Coefficient of Sensitivity. (TCS). Film stress due to temperature is usually evaluated as (33)

$$\sigma = E\ \alpha\left(T_f - T_i\right) \qquad (7.1.1\text{-}1)$$

Where σ, E, α, T_i, and T_f represents thermal stress (Pa), Young's modulus of film (Pa), film Temperature Coefficient of Expansion (TCE), initial temperature (^{O}C) and final temperature (^{O}C), respectively. Given the condition

$$\frac{h_s E_s}{(1-\upsilon_s)} \Big/ \frac{h_f E_f}{(1-\upsilon_f)} \qquad (7.1.1\text{-}2)$$

where h_S, E_S, v_S, h_f, E_f, and v_f represents substrate thickness, Young's modulus, poisson ratio, film thickness (μm,, Young's modulus, poisson ratio, respectively, thermal stress between film and substrate is evaluated as

$$\sigma_f(\mathrm{T}) = \frac{(\alpha_s - \alpha_f)\ \Delta\ T\ E_f}{(1-\upsilon_f)} \qquad (7.1.1\text{-}3)$$

The design decision takes into consideration problems of high temperature operation. Typical of such problems are degradation of piezoresistors at elevated temperatures and also TCE mismatch. The starting material is a <100> silicon wafer (n-type). A 0.1um SiO_2 is grown on the wafer. This is followed by 0.25um $TaSi_2$ over the oxide. The next is 0.1um thick LPCVD Si_3N_4 followed by another 0.25um $TaSi_2$ layer. The thicknesses of Si_3N_4 and $TaSi_2$ are the same. The SiO_2 is 0.02um thick. The polysilicon membrane thickness is 1μm. We are interested in two sections of the layers: The SiO_2/Si_3N_4 interface and the $Si_3N_4/TaSi_2$ interfaces. We are interested in the former because the thermal mismatch

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determines the effective diameter of the membrane. The $Si_3N_4/TaSi_2$ interfaces are of great importance because it determines if symmetrical layering method is effective to contain the Silicide expansion. A successful containment of the expansion forms the basis for the claim that the device has potential for high temperature applications.

Membrane stress is evaluated by determining the effect of temperature on it. The thermal stress exhibited by the membrane at 650°C is assumed to be negligible for the reason that the polysilicon membrane is originally deposited at process temperature higher than that. Secondly, it so happens that the underlying SiO_2 and Si_3N_4 have lower TCEs (0.55ppm/°C for oxide) than silicon (TCE=2.33ppm/°C). Hence, at high temperatures the thermal mismatch force between the oxide and nitride is evaluated as (33)

$$F_f = \frac{w(\alpha_s - \alpha_f)\Delta T}{\left[(1-\upsilon_f) / h_f E_f \right] + \left[(1-\upsilon_f) / h_s E_s \right]} \qquad (7.1.1\text{-}4)$$

where w represents the film width (diameter). In the worse case scenario therefore, given a poisson ratio of 0.7, with the E of polysilicon as 190GPa, thickness of 1um, E of SiO_2.as 73GPa and thickness of 0.02um, the thermal mismatch force between polysilicon and oxide is in microNewtons. Extensive studies also indicate the stability of the Si/SiO_2 interface. It is found that developed thermal mismatch force due to stress build-up is minimal. At cool down regime, the membrane is essentially under slight tension. At elevated temperatures, however, the membrane becomes relaxed, with little or no effect on device performance. Similar calculatuion is done on the Si_3N_4/SiO_2 and the thermal mismatch force is also found to be negligible. Based on the above analysis, the large deflecting membrane

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center stress is evaluated at various temperatures with applied pressure using equations 5.2-2 and 5.2-6, taking into account the temperature element:

$$\left[\sigma_r(T)\right]_{r=0} = 0.432\ \sqrt[3]{\frac{E(T)P^2 a(T)^2}{h(T)^2}} \qquad (7.1.1\text{-}5)$$

for large deflection analysis and

$$\left(\sigma_r(T)\right)_{max} = \frac{3}{4}\frac{P\ a(T)^2}{h(T)^2} \qquad (7.1.1\text{-}6)$$

for small deflection analysis. Generally, the following parameters are expressed as functions of temperature:

$E(T)$=-80x10^{6}T+382x10^9 [Pa]

$a(T)$=100x10^{-6}(1+(0.8-0.55)10^{-6}(T-25)) [um], and

$h(T)$=1.32x10^{-6} [um], assuming no significant change in thickness.

It is necessary to note that the effective membrane thickness is 1.32um. Also, the nitride TCE and Young's modulus is used for this analysis as previously done in other chapters. The reason being that the underlying nitride with higher Young's modulus would be the dominant material. Figure 7-3 shows the large deflection analysis of the membrane center stress with applied uniform pressure at a temperature range of -50°C to 650°C. We note the stress variations at different temperatures.

There is a high stress build up at lower temperatures while low stress is noticeable at higher temperatures. Maximum stress of 330MPa (2.475Mtorr) is evident at the maximum pressure differential of 450kPa, at -50°C. This is translated as 0.17% and 0.09% strain on the polysilicon membrane and underlying nitride, respectively. At elevated temperature of 650°C, the membrane stress is reduced to 315MPa, resulting in lesser strain on nitride. As stated in previous

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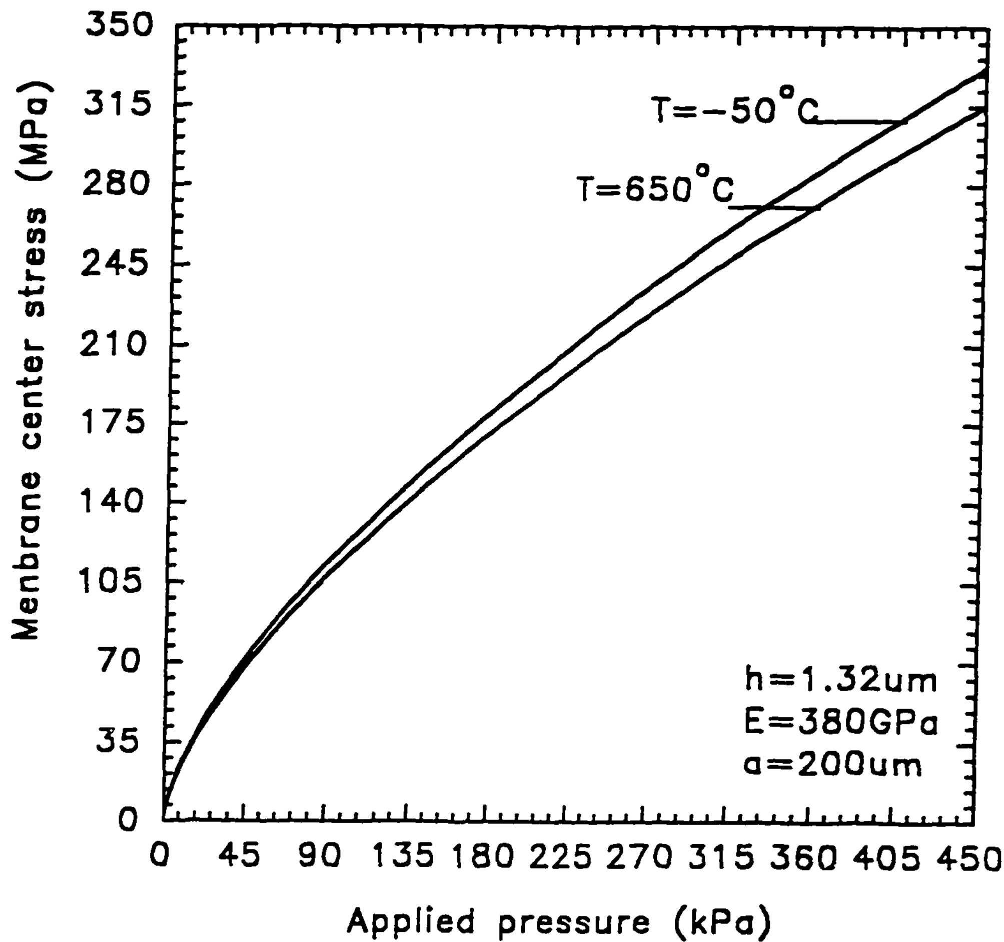

Fig. 7-3 Membrane center stress versus applied pressure at temperature range of -50°C to 650°C (Large deflection)

chapter, the proposed strain safety threshold for this device must not exceed 2% on the linear region of the stress-strain curve in order to maintain membrane elasticity and integrity. In the case of small deflection stress analysis, fig. 7-4 shows that temperature effects on membrane stress is not as pronounced as in the case of large deflection analysis. This plot is compared with that of 5.2-2 at room temperature and it could be seen that there is no variation in stress at different

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temperatures. It can be deduced from this analysis that at low pressure differential regime, membrane stress is predominantly due to the applied pressure.

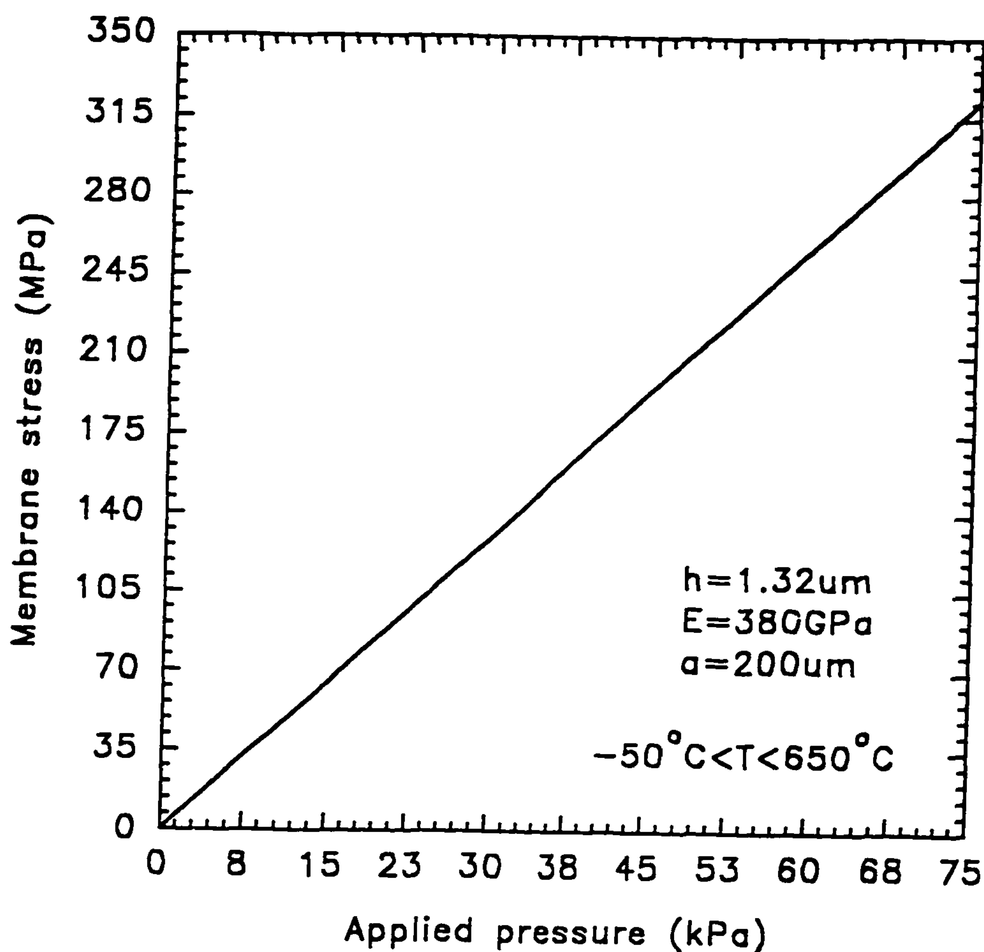

Fig. 7-4 Membrane center stress versus applied pressure at temperature range of -50°C to 650°C (Small deflection)

Critical to device performance is the thermal stability of the $Si_3N_4/TaSi_2/Si_3N_4$ interfaces at elevated temperatures. The $TaSi_2$ is the spiraling strip of conductor that is sandwiched between two Si_3N_4 layers. This coil is

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effectively encapsulated by the two nitride layers. The dimension of the coil is 4um wide, 0.25um thick and 90um long to the 100um x100um bonding pad. Figure 7-5 shows the crossection view of the $TaSi_2$ conductor encapsulated by nitride layers. At elevated temperatures, the $TaSi_2$ (TCE=9ppm/^oC) would tend to expand against two nitride (TCE=0.8ppm/^oC) surfaces. If it indeed expands, the effect would be

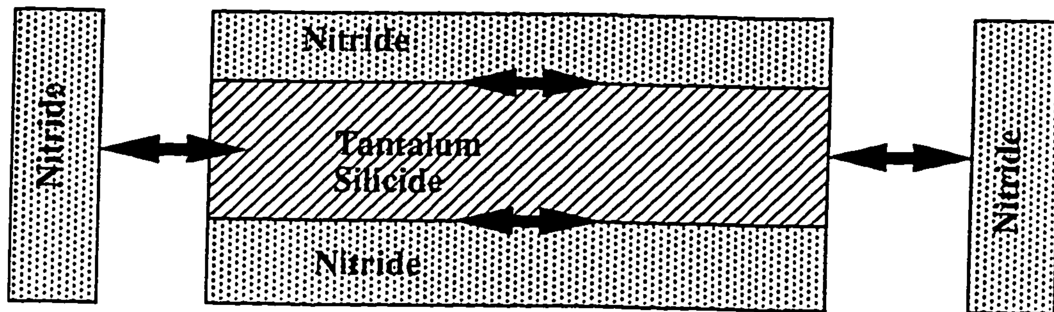

Fig. 7-5 Thermal mismatch force between encapsulated $TaSi_2$ and Si_3N_4 at elevated temperatures.

to change the coil dimension., resulting in deviation of output voltage readout. The objective is to contain such expansion. By the **symmetrical layering** of $TaSi_2$

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between two nitride, it is anticipated that the developed tensile/compressive stress would be absorbed by the nitride layers and distributed evenly. To support this idea, the thermal mismatch force between nitride and $TaSi_2$ at 650°C is evaluated using equation 7.1.1-4. The thermal mismatch force is found to be a couple of microNewtons. Therefore, it is strongly believed that **symmetrical layering** has effectively contained any expansion of $TaSi_2$ at 650°C. Extensive stress related experiments with $TaSi_2$ (3, 4, 7) conclude that indeed at higher temperatures, $TaSi_2$ stress reduces greatly. Generally, stress in $TaSi_2$ is attributed to the high temperature sintering process to the effect that at cool down regime, the film is in tensile stress and tends to peel away from the substrate. This situation is not anticipated in this device because application is for high temperature environment where the $TaSi_2$ conductor is relaxed and also that any developed stress would be transferred to the nitride layers.

7.1.2 Effect of Temperature on Membrane

Based on the stress analysis stated above, it is possible to evaluated the effect of temperature on the membrane. We realize the differences in the TCEs of the layers. We also realize the dominating effect of the nitride under layers in terms of its hardiness, low TCE, and high Young's modulus. Temperature effect on membrane would be mainly to either expand (high temperature) or constrict it (low temperature). This would result in changing the deflection characteristics of the membrane, consequently resulting in output voltage error. The fundamental objective is to ensure minimum deflection due to change in temperature. How much deviation from room temperature membrane deflection has is evaluated with equations 5.2-1 and 5.2-4 for large and small deflections, respectively as

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$$w = 0.662a\sqrt[3]{\frac{Pa(T)}{E(T)h(T)}} \quad (7.1.2\text{-}1)$$

$$w = 0.89\frac{P\,a(T)^4}{64E(T)h(T)^3}12(1-\upsilon^2) \quad (7.1.2\text{-}2)$$

These equations are used to plot the membrane deflections to applied pressure for various temperatures. The plot of membrane deflection versus applied pressure is shown in fig. 7-6 for large membrane deflection analysis.

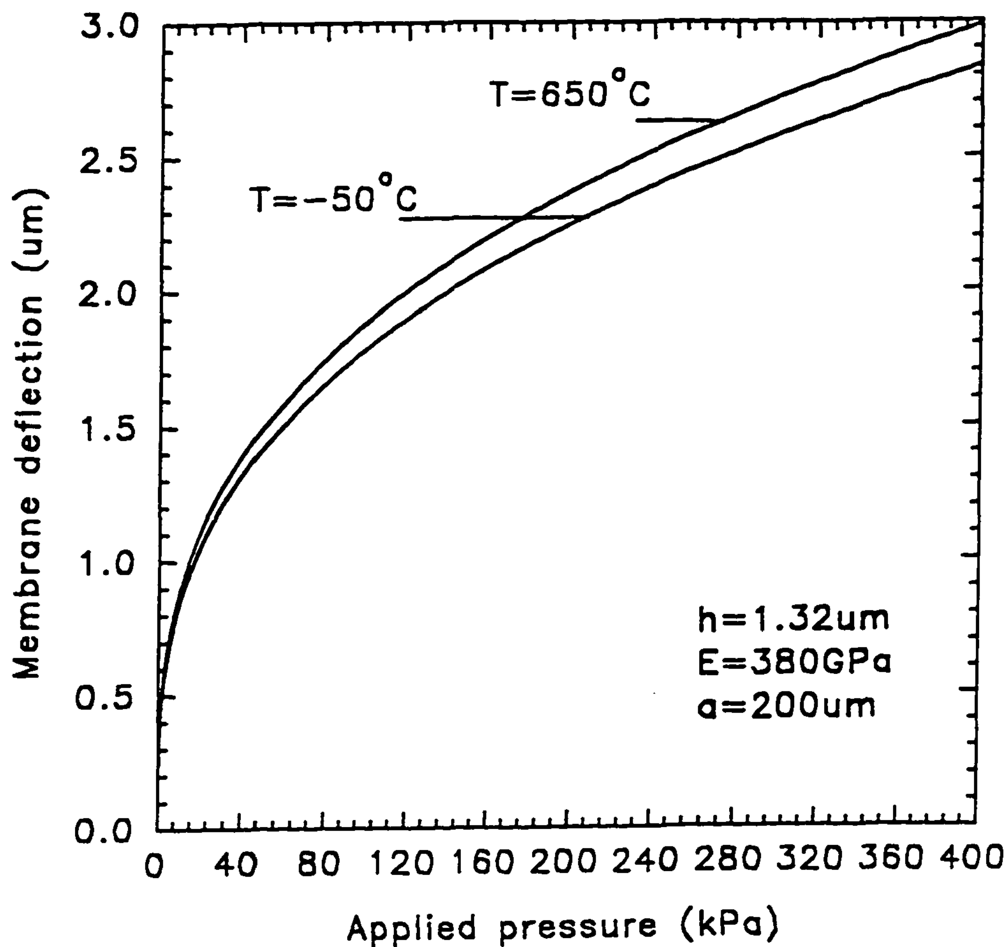

Fig. 7-6 Membrane center deflection versus applied pressure for temperature range of -50°C to 650°C (Large deflection)

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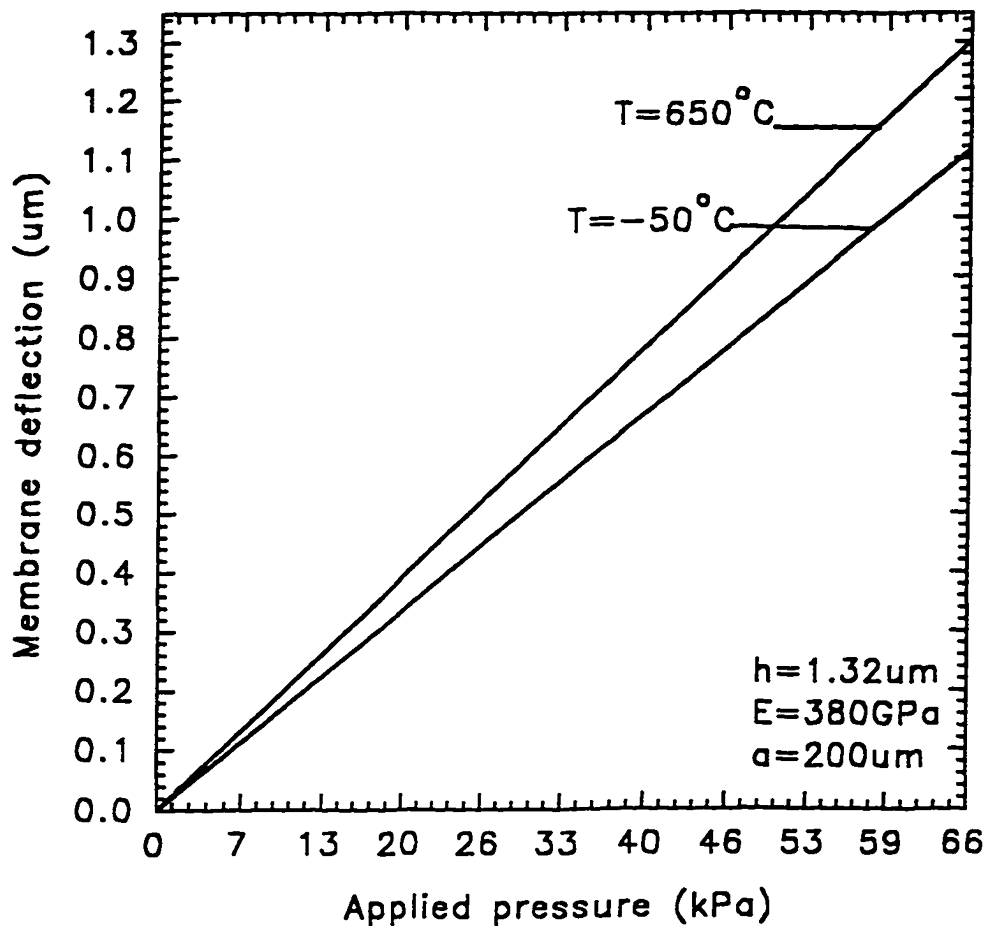

Fig. 7-7 Membrane center deflection versus applied pressure for temperature range of -50°C to 650°C (Small deflection)

The effect of temperature is very noticeable. We see that at maximum pressure differential the deflection of the center membrane at 650°C is about 3um. This is .3um more than room temperature deflection. Two things are of interest at this deflection: The membrane center does not touch the cavity bottom and also the

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maximum strain is well below the 2% threshold. Even at touch down, when the membrane center touches the cavity base, the strain would remain below the specification threshold. In essence, the device is immune against rupture due to over pressure.

In the case membrane deflection for small deflection analysis shown in fig. 7-7, the maximum membrane deflection at maximum pressure differential is observed at 650°C to be 1.3um at 66kPa pressure differential. This deflection is about .3um above room temperature deflection at that pressure. However, stress analysis at this deflection shows that the induced strain does not exceed the specified 2% level. At below room temperature, deflections in both cases, the maximum membrane deflection is noticeable.

7.1.3 Temperature Effects on Output Voltage, Sensitivity, Temperature Coefficient of Offset (TCO), and Temperature Coefficient of Sensitivity (TCS)

The stress and deflection analysis conducted earlier basically set the stage for the evaluation of the effects of temperature on the output voltage. The output voltage is a function of membrane deflection. This part of the analysis makes it possible to determine the Temperature Coefficient of Offset (TCO) of the voltage, Temperature Coefficient of Sensitivity (TCS), Temperature Coefficient of Span (TCP), and the output voltage sensitivity to temperature. These figures form the basis of quantifying degree of device performance. The output voltage Vs as function of pressure at different temperatures is evaluated using the equation 4.1.4-3, reproduced below

$$V_S = \frac{\omega\mu I\cos(\omega t)}{\pi}\sum_{ij}^{M}\sum_{j}^{N} Q_{ij} \qquad (7.1.3\text{-}1)$$

where

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$$Q_{ij} = \frac{b_i^2 b_j}{\frac{b_i^2}{4} + g^2} \ln \left[\frac{\frac{b_j - b_i}{2} + \sqrt{\left(\frac{b_j - b_i}{2}\right)^2 + g^2}}{-\frac{b_i}{2} + \sqrt{\frac{b_i^2}{4} + g^2}} \right]$$

Applying this for large membrane deflection analysis, the first step is to express the membrane deflection as function of temperature. This is expressed as

$$w = 0.662a \sqrt[3]{\frac{Pa(T)}{E(T)h(T)}} \qquad (7.1.3\text{-}2)$$

The relationship between coil gap and temperature is expressed as

$$g = go - 0.66a \sqrt[3]{\frac{Pa(T)}{E(T)h(T)}} \qquad (7.1.3\text{-}3)$$

By substituting 7.1.3-3 for g in 7.1.3-1 we get

$$V_s(T) = \frac{\omega\mu I\cos(\omega t)}{\pi} \sum_{ij}^{M} \sum_{j}^{N} Q_{ij} \qquad (7.1.3\text{-}4)$$

where the g variable in Qij is now a function of temperature.

With this equation, the effect of temperature on output voltage can now be calculated. In applying this equation, consideration is given to the range of temperature. Although the proposed device is meant for use in high temperature environment, it is equally efficient at low temperatures. In this regard, temperature analysis is carried out in the range of -50°C to 650°C. The output voltage response to applied pressure for different temperatures for large deflection analysis is plotted and shown in fig. 7-8. We notice the evident effect of temperature on

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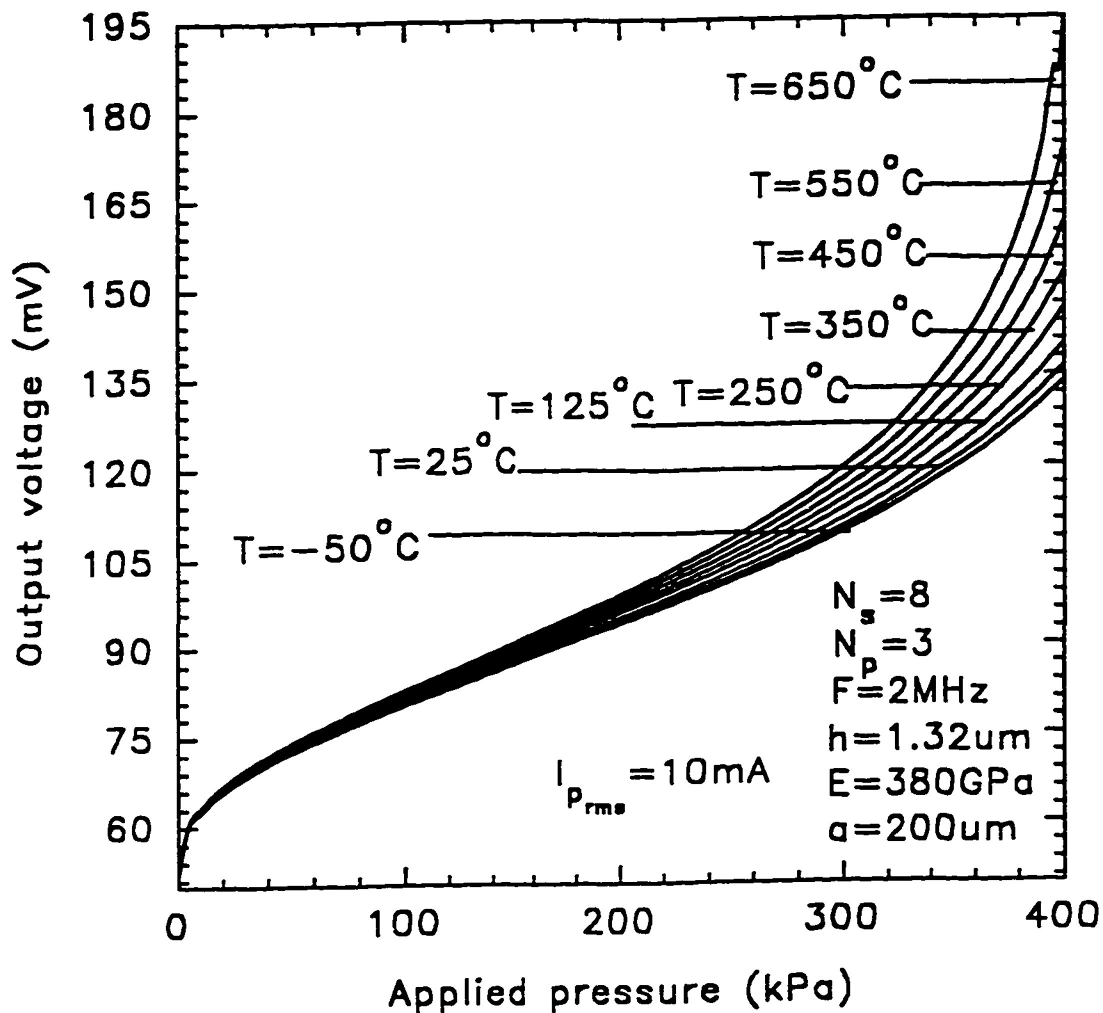

Fig. 7-8 Output voltage versus applied pressure at various temperatures (Large deflection)

the output voltage. This is due to the combination of the thermal expansion of the membrane and controlled expansion of the Silicide conductor. At 650°C, we see that the full scale output voltage has increased from 135mV at 25°C at to 195mV, at differential pressure of 400kPa. At -50°C, the output voltage is slightly less than

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135mV. This represents a change of 60mV from room temperature signal condition. It is now possible to determine the Temperature Coefficient of Offset at both zero and maximum pressure differential of the device. Generally, Temperature Coefficient of Offset is expressed as (24)

$$TCO = \frac{1}{V_o}\frac{V_f - V_o}{T_f - T_o}, \qquad (7.1.3\text{-}5)$$

where V_o,=Initial Output voltage; V_f=final output voltage; T_o=Initial temperature; T_f=final temperature. In this analysis, the initial values are those obtained at room conditions. The calculation of the maximum pressure TCO at 650°C is shown below

$$TCO|_{P=400kPa} = \frac{1}{135}\frac{195-135}{650-25} = 711 ppm/^oC$$

The output voltage Vs as function of pressure at different temperatures using small deflection analysis is also evaluated equation 4.1.4-3. The first step is to express the membrane deflection as function of temperature such that

$$w = 0.89\frac{P\,a(T)^4}{64E(T)h(T)^3}12(1-\upsilon^2) \qquad (7.1.3\text{-}6)$$

The relationship between coil gap and temperature is expressed as

$$g = go - 0.89\frac{P\,a(T)^4}{64E(T)h(T)^3}12(1-\upsilon^2) \qquad (7.1.3\text{-}7)$$

By substituting 7.1.3-7 for g in 7.1.3-1 we get

$$V_s(T) = \frac{\omega\mu I\cos(\omega t)}{\pi}\sum_{ij}^{M}\sum_{j}^{N}Q_{ij} \qquad (7.1.3\text{-}8)$$

where Qij now contains the expressions for coil gap as function of temperature. The output voltage response to applied pressure for different temperatures for

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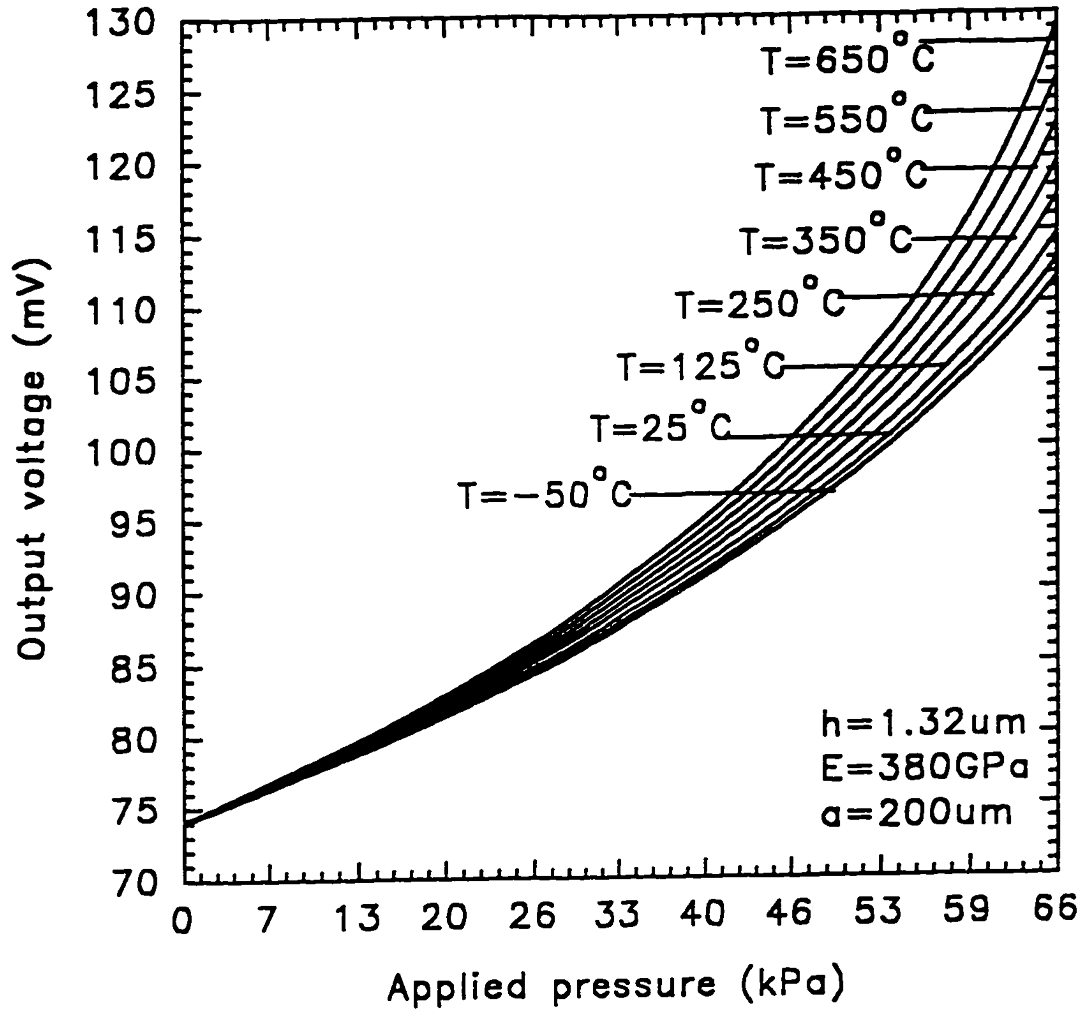

Fig. 7-9 Output voltage versus applied pressure at various temperatures (Small deflection)

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small deflection analysis is plotted and shown in fig. 7-9. We notice the evident difference in the effect of temperature on the output voltage compared to large deflections. At 650°C, we see that the full scale output voltage has increased from 113mV at 25°C to 129mV, representing a change of 16mV. At -50°C, the output voltage is 112mV for full scale pressure differential. This represents a change of 1mV from room temperature signal condition. The calculation of the maximum pressure TCO at 650°C is shown below

$$TCO|_{P=66kPa} = \frac{1}{113}\frac{129-113}{650-25} = 226\, ppm/^{o}C$$

The room temperature sensitivity of the device has been evaluated in chapter six. This part evaluates the sensitivity of the output voltage due to temperature changes. There is need to determine how the device sensitivity deviates from that at room temperature. We recollect that in chapter six, the sensitivity is obtained by taking the derivative of the output voltage with respect to applied pressure. The same procedure is repeated here, but at different temperatures. The effect of temperature on the output voltage sensitivity is shown in fig 7-10 for the temperature extreme of -50°C and 650°C. Here again we see how temperature affects the device sensitivity to applied pressure. The sensitivity to pressure between the two extreme temperatures is nearly equal. While the sensitivity is observed not to change much at increased temperatures, the gradient remains constant. This very much unlike conventional pressure sensors that experience degradation of sensitivity with increase temperature.

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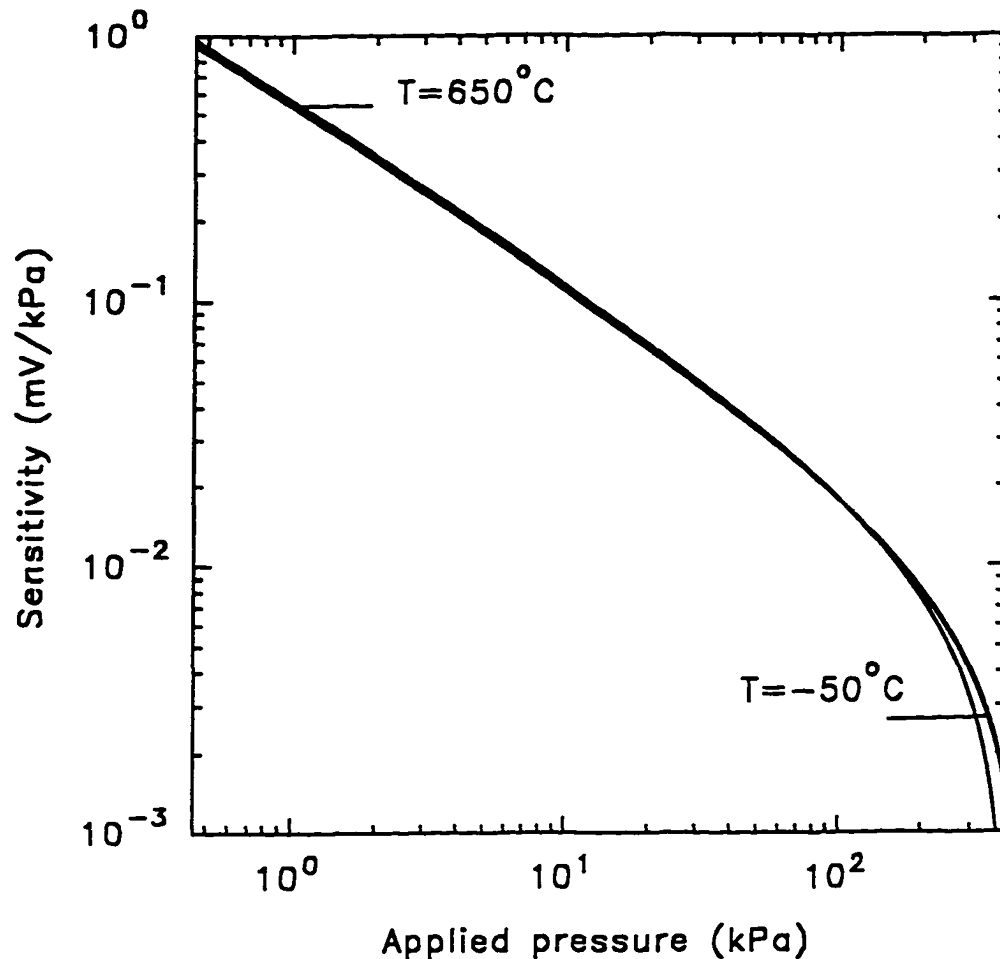

Fig. 7-10 Effect of temperature on output voltage sensitivity (Large deflection)

With this, we are able to determine how the sensitivity changes with temperature by calculating the Temperature Coefficient of Sensitivity (TCS) generally expressed as

$$TCS = \frac{1}{S_o}\frac{S_f - S_o}{T_f - T_o} \qquad (7.1.3\text{-}9)$$

From data obtained, full scale pressure TCS for 650°C is calculated

$$TCS|_{P=450kPa} = \frac{1}{0.001}\frac{0.0015 - 0.001}{650 - 25} = 0.8x10^{-3} /^o C$$

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The same analysis is done for small membrane deflections. The procedures are essentially the same, but as we shall see, the results are different due the

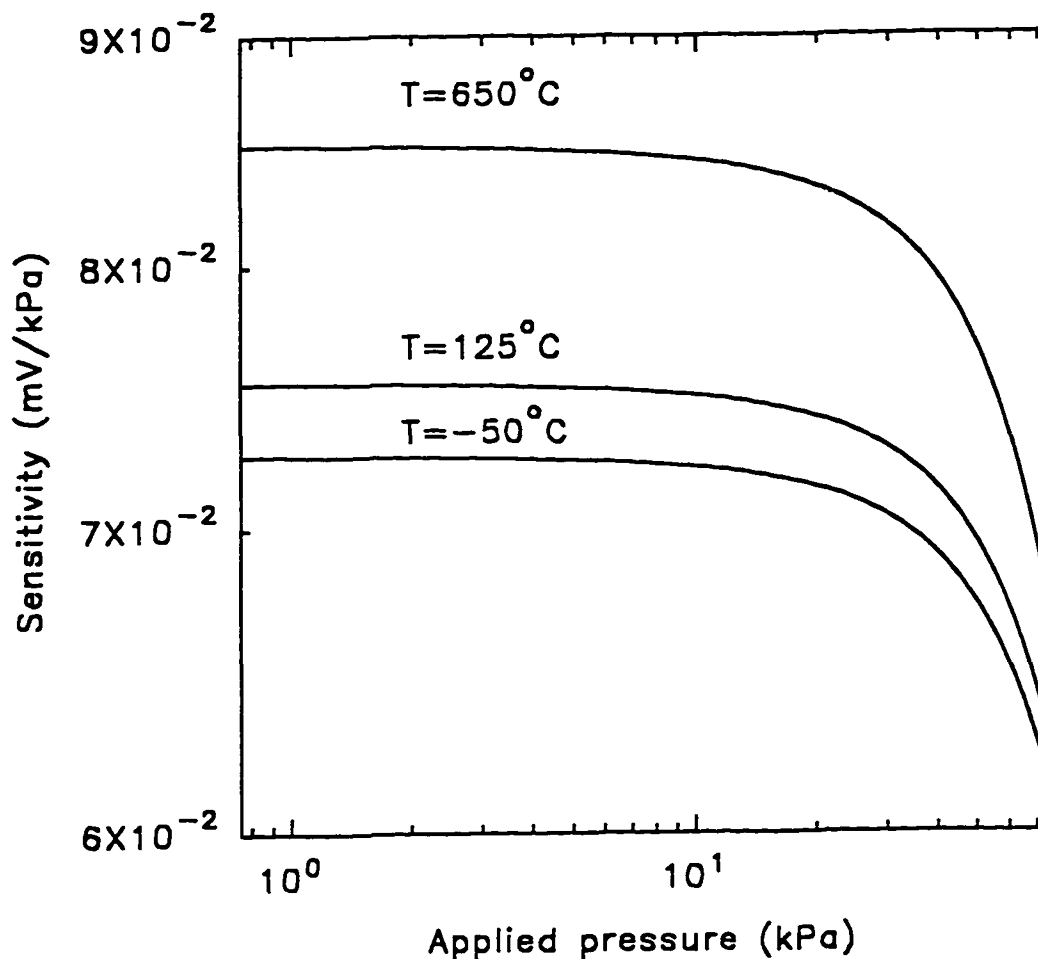

Fig. 7-11 Effect of temperature on output voltage sensitivity (Small deflection) conditions imposed. The effect of temperature on the output voltage sensitivity is shown in fig 7-11 for the temperature extremes under investigation. Here again we see how temperature affects the device sensitivity to applied pressure. The full

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scale sensitivity is obtained to be 0.068mV/kPa at 650°C at all pressures. The TCS at 650°C is calculated as

$$TCS = \frac{1}{0.061}\frac{0.068-0.061}{650-25} = 0.18x10^{-3} /^{o} C$$

7.2 Effects of Membrane Thickness

Membrane thickness is an important element in pressure sensing devices for various reasons. High among these are the effects on output voltage and sensitivity. There is need to identify what thickness limit is acceptable for a particular specification. Mechanical considerations demand that we know the developed stress due to increased thickness. As is well known, film thickness processing is limited by internal stress. Adding to this stress is that due to applied pressure. The specification of this device calls for a maximum membrane strain of not more than 2%. We recollect that the maximum strain for a membrane thickness of 1.32um has been determined to be less than 1%. Membrane thickness effect on deflection, stress, and output voltage is

7.2.1 Effect of Membrane Thickness on Stress and Output Voltage.

We first consider the effect of membrane thickness on stress using large deflection analysis. We have used equation 5.2-2 and 3 to evaluate the developed center and edge stresses, respectively, on the membrane due to applied pressure. This evaluation is done with a membrane thickness of 1.32um. Here, various thickness would be used and the developed stress and strain evaluated. By using 5.2-2 and 3, the stress and resultant strain relationship for various membrane thickness is evaluated. This is graphically shown in fig. 7-12 for large deflection analysis. We take note of the stress reduction as thickness increases. For a thickness of 2um, the

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center stress on the membrane is at full scale pressure is 250MPa, down from 315MPa at 1.32um thickness.

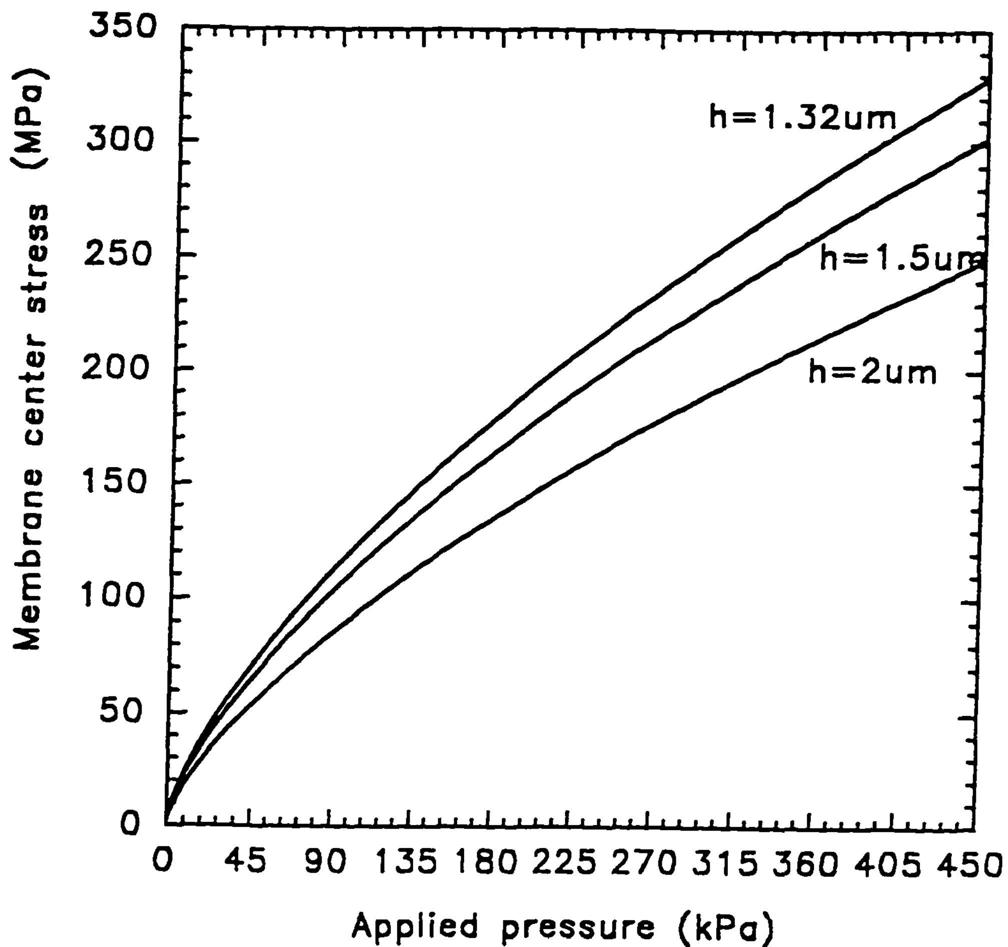

Fig. 7-12 Membrane center stress versus pressure for various membrane thicknesses. (Large deflection)

For the case of small deflections, shown in fig. 7-13, membrane stress changed from 320MPa at thickness of 1.32um to 140MPa at thickness of 2um.

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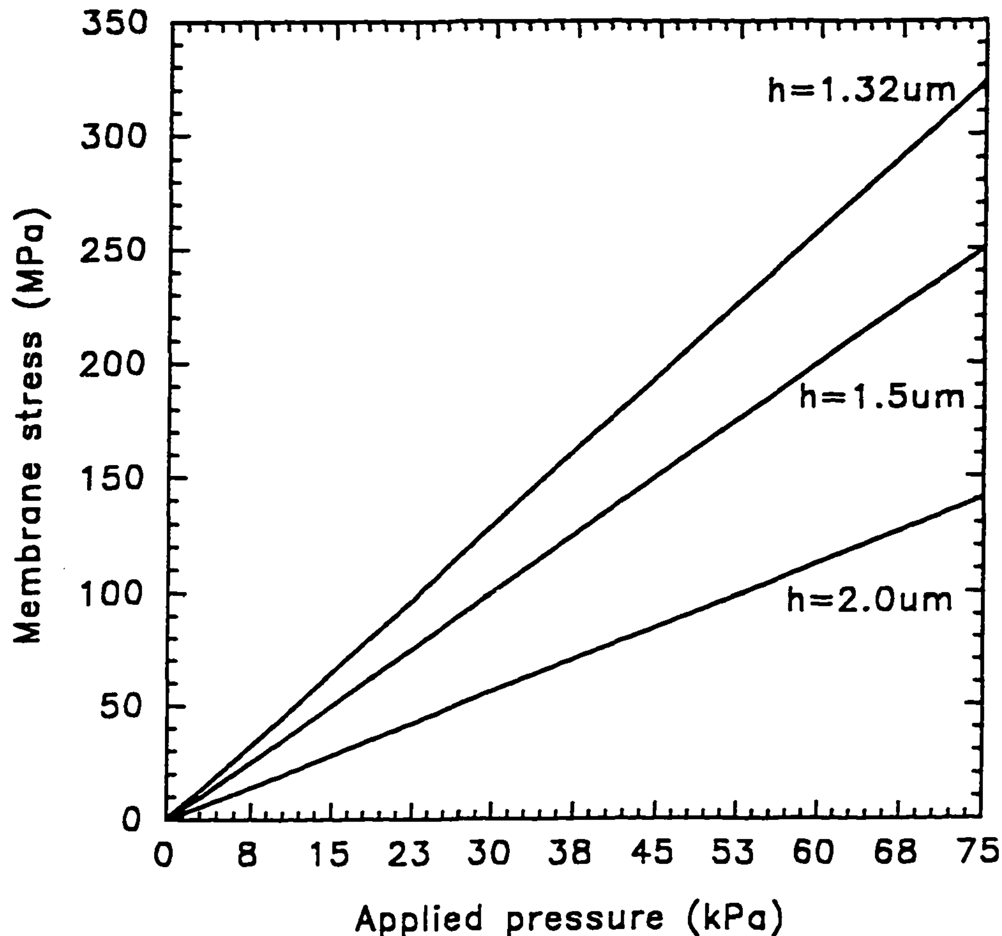

Fig. 7-13 Membrane center stress versus pressure for various membrane thicknesses. (Small deflection)

The next pertinent question is what effect does changing the membrane thickness has on the output voltage of the device. The is answered by varying the membrane thickness using the voltage equations 6.1.4b and 6.1.7 for large and small deflection analysis, respectively. A plot of the output voltage response to applied pressure for large deflection analysis is shown in fig. 7-14. We see the big reduction of the full scale output voltage of 175mV at 1.32um to 110mV at 2um thickness. Small membrane deflection does not fair any better. Shown in fig. 7-15 is the output voltage response to pressure for various membrane thickness.

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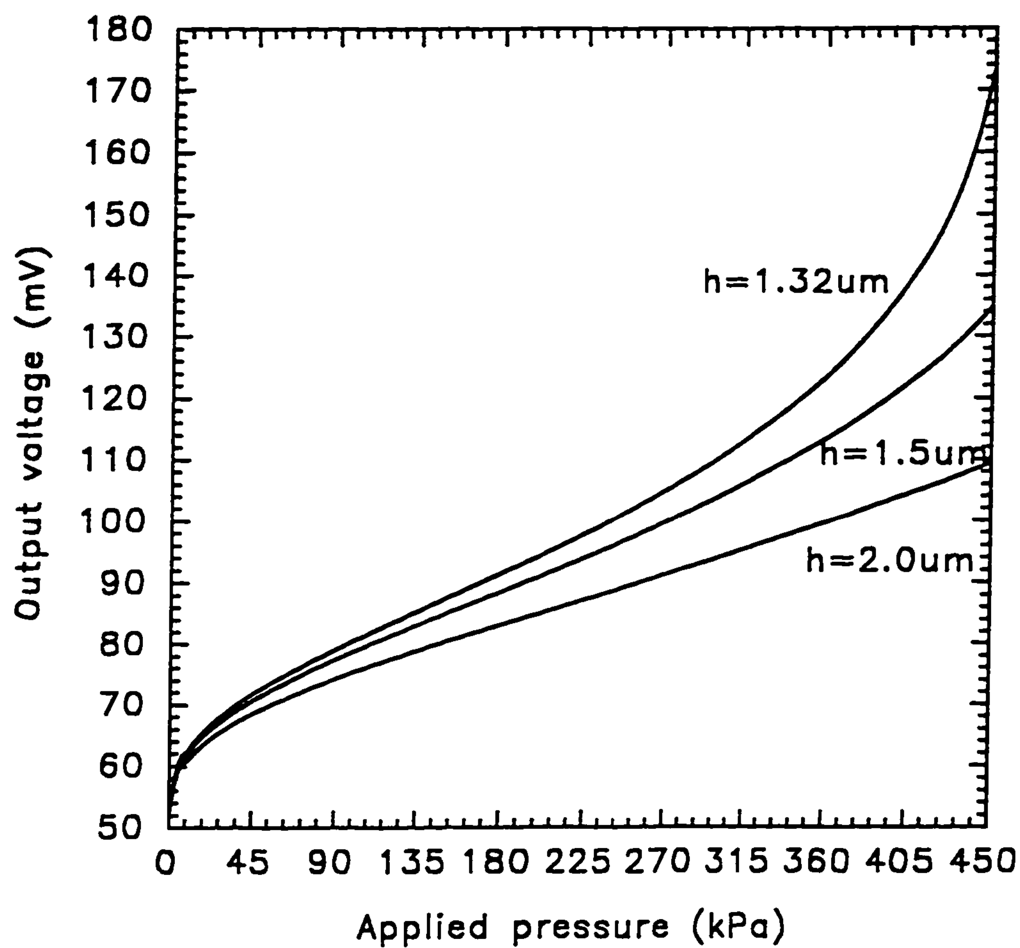

Fig. 7-14 Output voltage versus pressure for various membrane thicknesses. (Large deflection)

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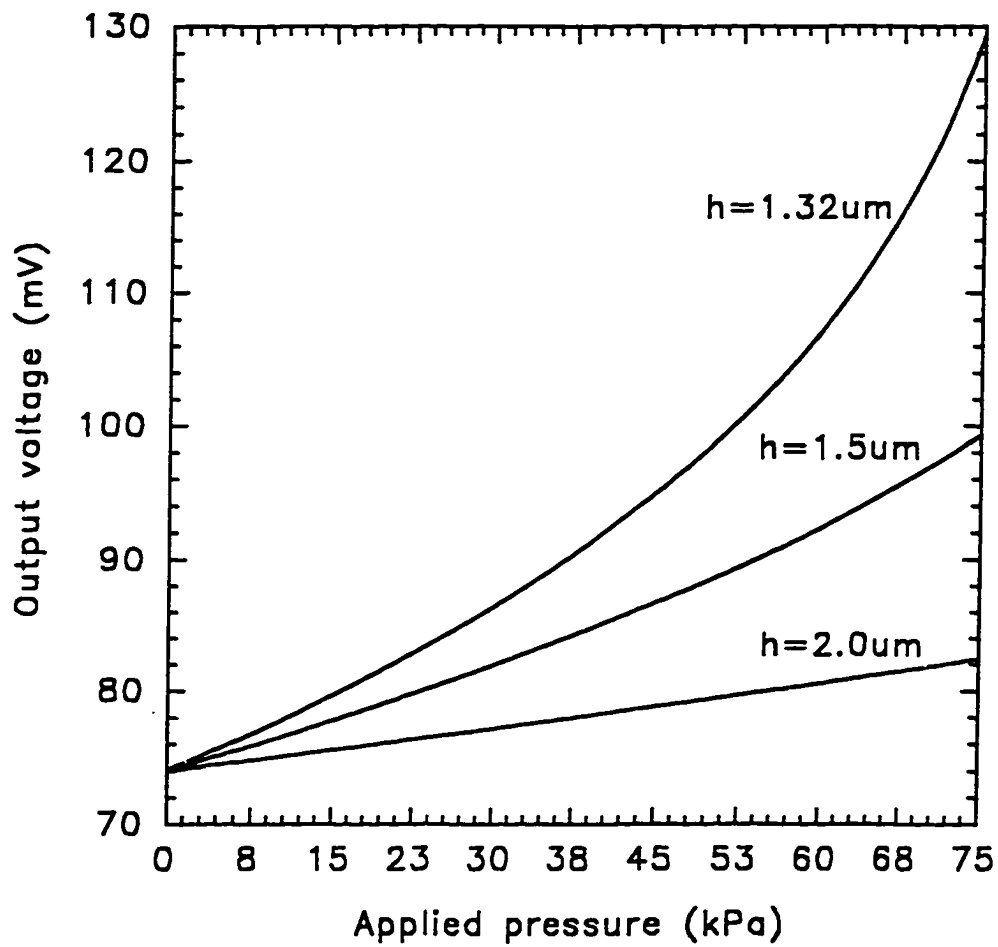

Fig. 7-15 Output voltage versus pressure for various membrane thicknesses. (Small deflection)

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7.2 2 Effect of Membrane Thickness on Sensitivity

Sensitivity analysis is conducted for different membrane thickness in order to determine voltage behavior. There is no dramatic shift from the initial thickness as depicted in fig. 7-16 and 17, for large and small deflections, respectively. However, appreciable degradation in sensitivity is evident for small deflections.

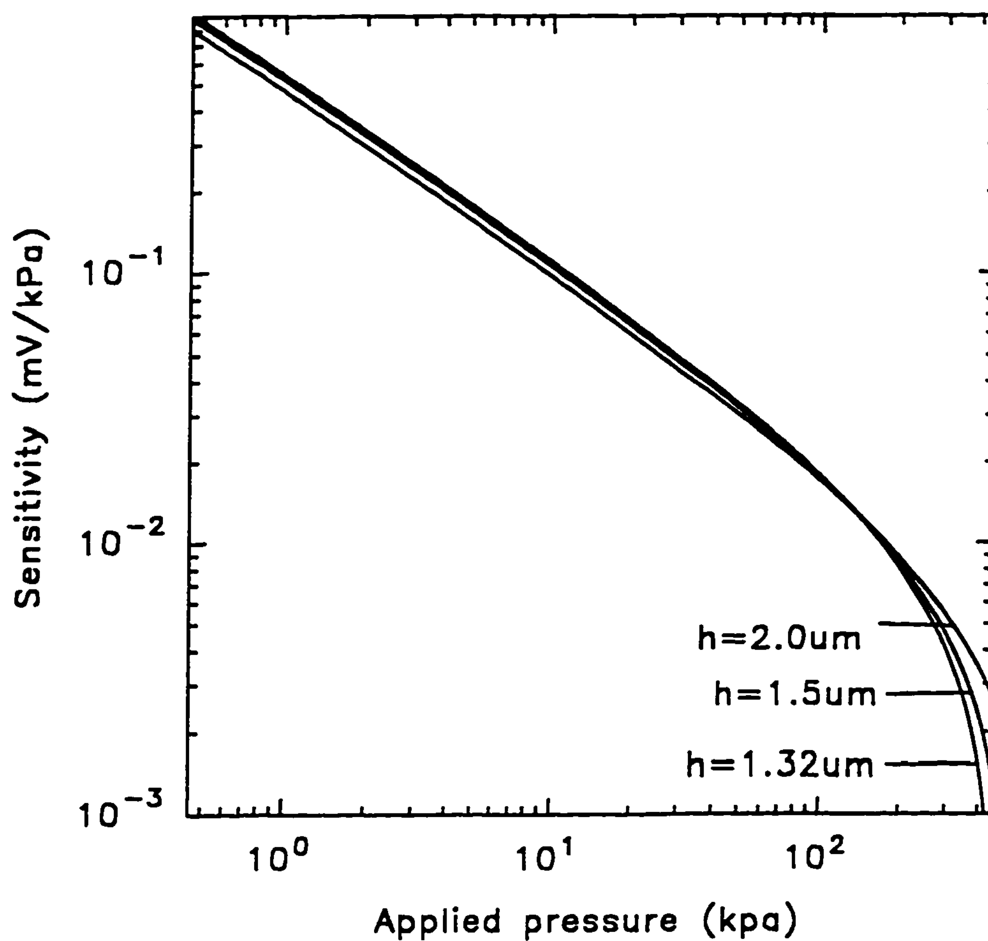

Fig. 7-16 Output voltage sensitivity versus pressure for various membrane thicknesses. (Large deflections)

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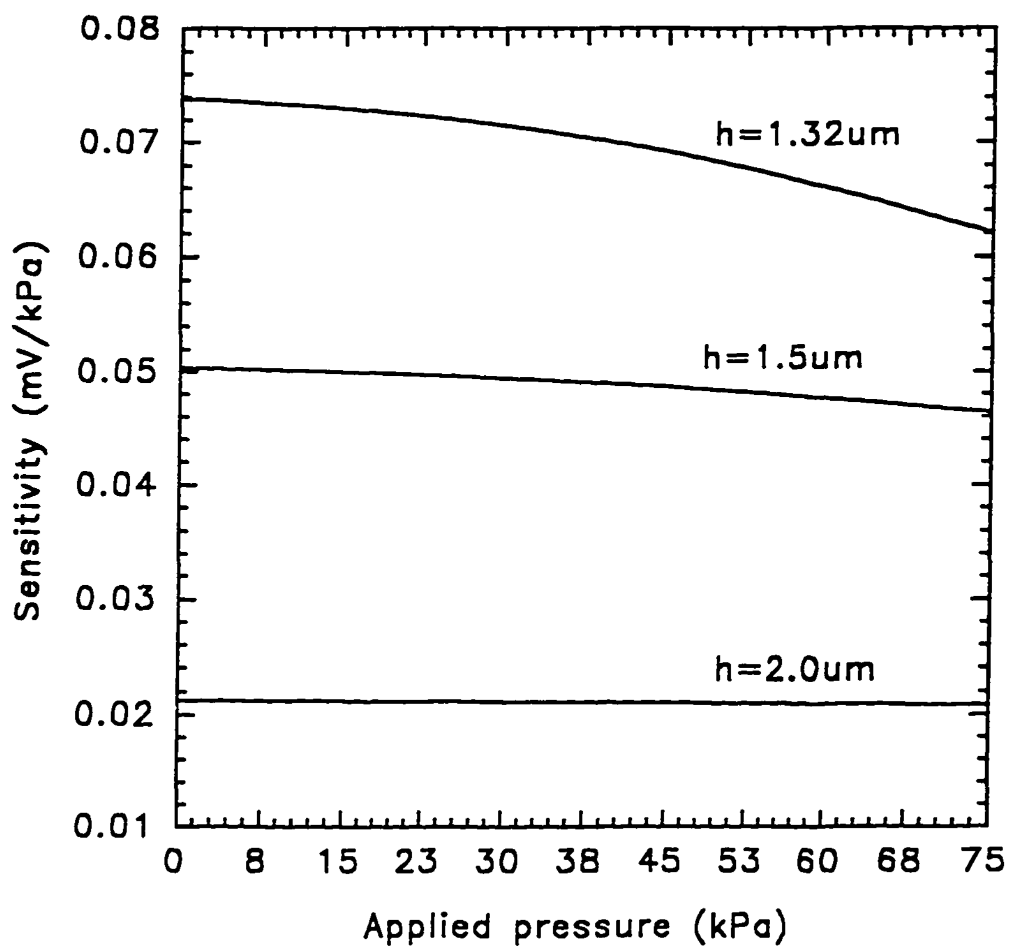

Fig. 7-17 Output voltage sensitivity versus pressure for various membrane thicknesses. (Small deflections)

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CHAPTER 8
OPTIMUM MICROELECTROMECHANICAL DESIGN

8.1 Winding Separation

This chapter deals with the optimization of the design based on established analysis. We wish to explore the effect of winding separation has on the output voltage. This is followed by a frequency analysis and its effect on the output voltage. The critical parameter considered here is the pitch of both the primary and secondary coils. The pitch of the secondary coils are fixed while varying that of the primary coil. The pitch used previously is 8um. By varying the primary coil pitch, we are able to understand the effect on the output voltage. The pitches selected are 6um, 10um, 12um, and 16um. Figure 8-1 shows the output voltage as function of these primary coil pitches. We see that for a pitch of 6um for the primary coil and 8um for the secondary coil, the zero pressure output voltage has dropped from 50mV to about 25mV. Interestingly, the full scale output voltage is very close to a 75mV, same as with previous analysis. This translates to a broadening of the dynamic range of the device to 150mV, compared to a primary coil pitch of 8um with a dynamic range of 125mV. The reason for this phenomena can be better explained by a computer simulation (30) of the magnetic field linking the secondary coil that is generated by current flowing in the primary coil. Figure 8.1-2a and b show the magnetic field distribution for a primary coil pitch of 8um and 6um, respectively. We notice that the field is denser within the secondary coil for the 6um pitch case (a), linking more turns than that of the 8um pitch case (b). We observe a higher loss of magnetic field for the latter case. Having determined the advantage of compacting the primary coils, we now consider the case of compacting the secondary coils. By reducing the secondary coil pitch to 6um, we can actually place eleven coil turns in the cavity.

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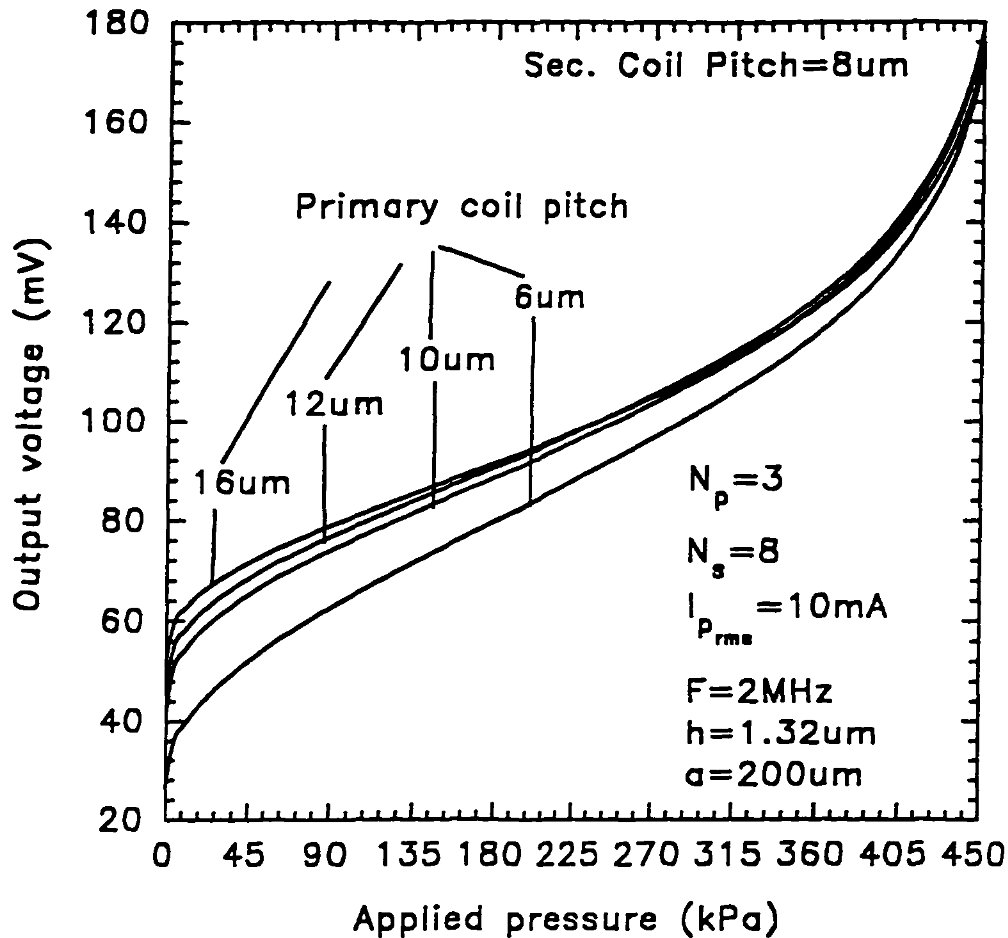

Fig. 8-1 Output voltage versus pressure for various primary coil pitches [Large deflection]

In fig. 8-2a and b, notice that the full scale output voltage for the 6um secondary/primary coil pitch is 280mV for large deflections and 200mV for small deflections. One big advantage of having a lower pitch is that the dynamic range of the output voltage is greatly enhanced, resulting in a span of 250mV and 120mV for large and small deflections, respectively. To achieve this, however, the process design rule for fabrication must have a critical dimension of 2um. It becomes important to evaluate the sensitivity of the device for a 6um primary/secondary coil pitch

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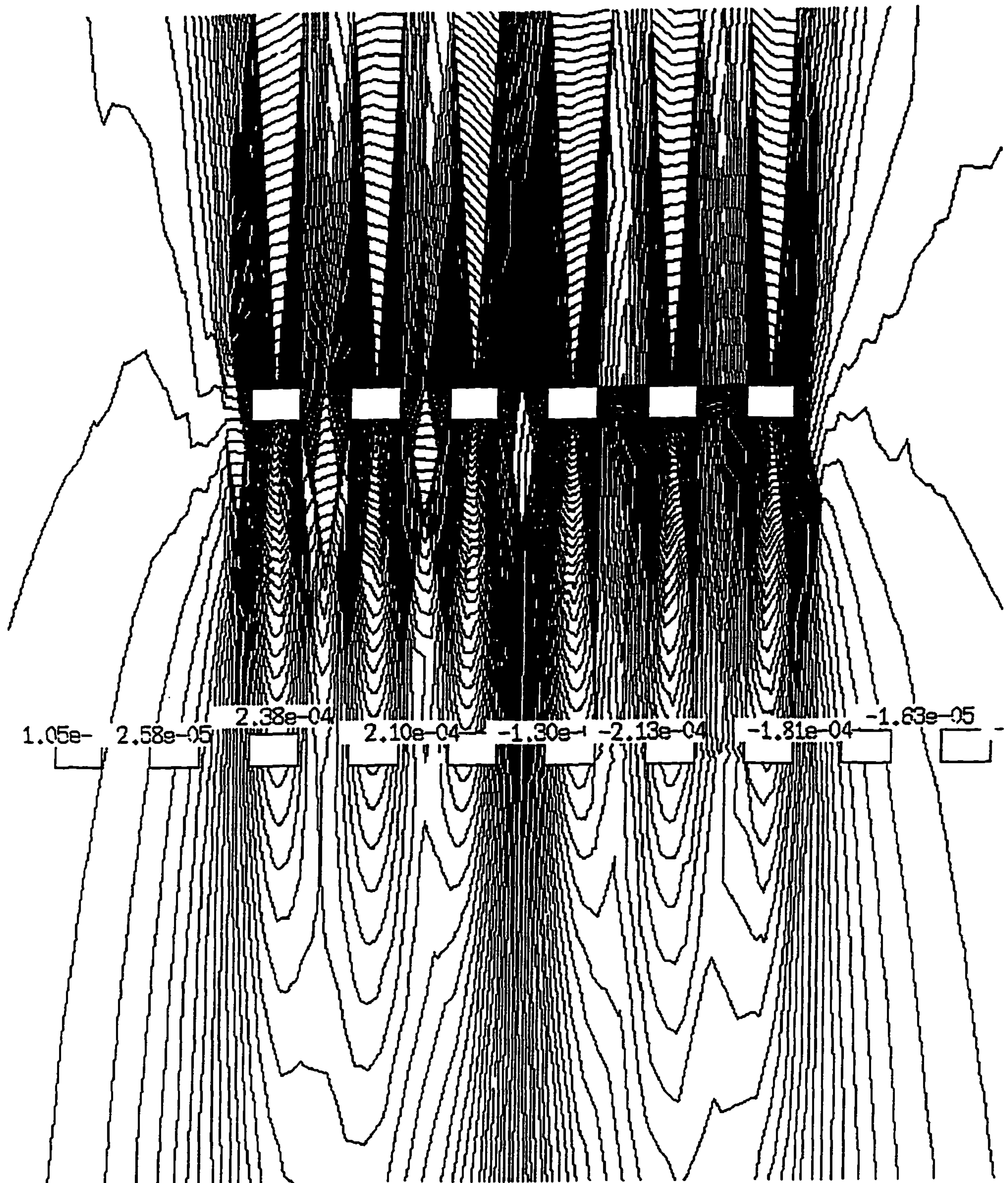

Fig. 8-2a Magnetic field profile on the crossection of device for 8μm primary coil pitch. Coil gap = 3μm.

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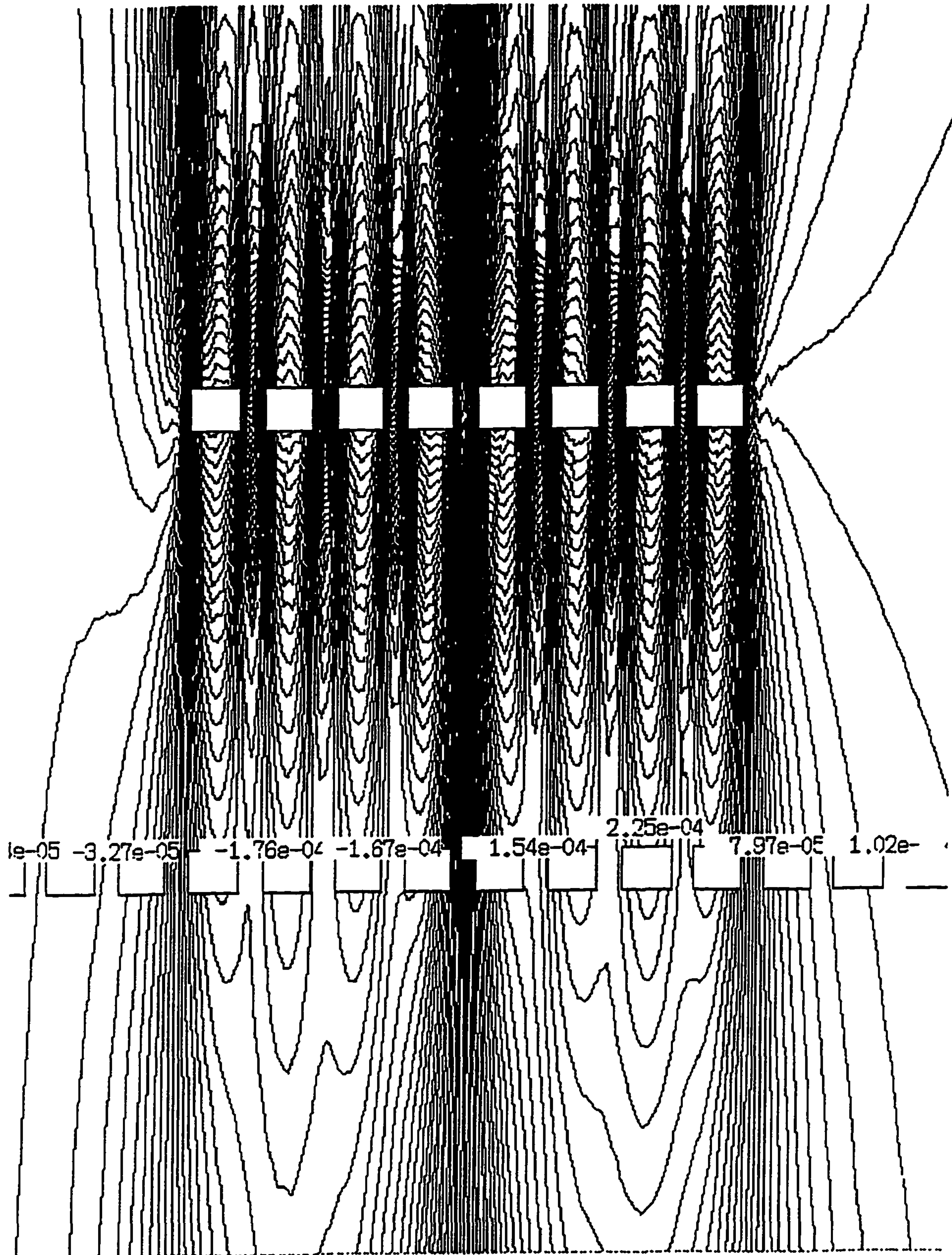

Fig. 8-2b Magnetic field profile on the crossection of device for 6um primary coil pitch. Coil gap = 3μm.

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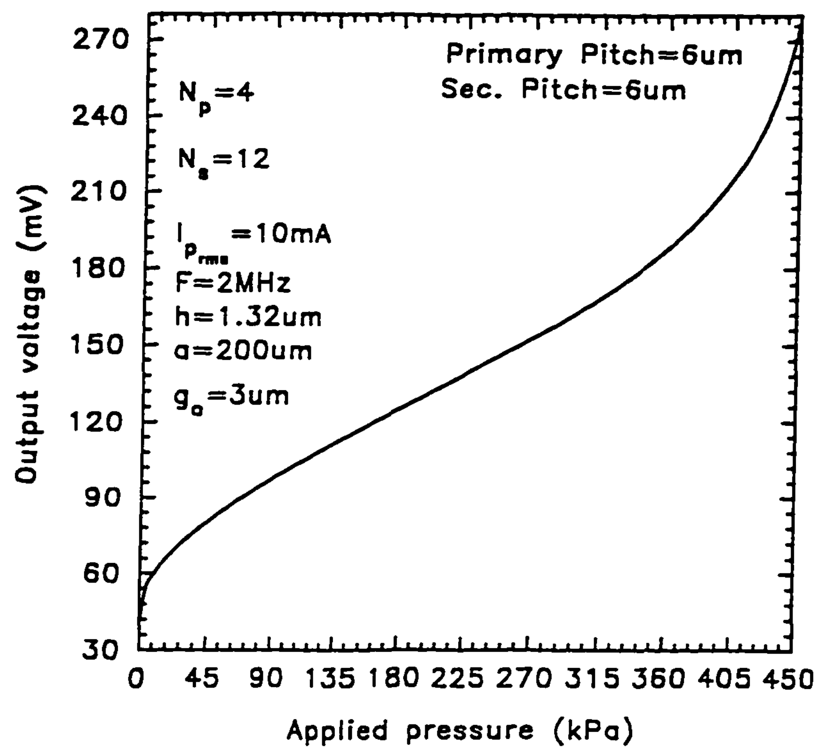

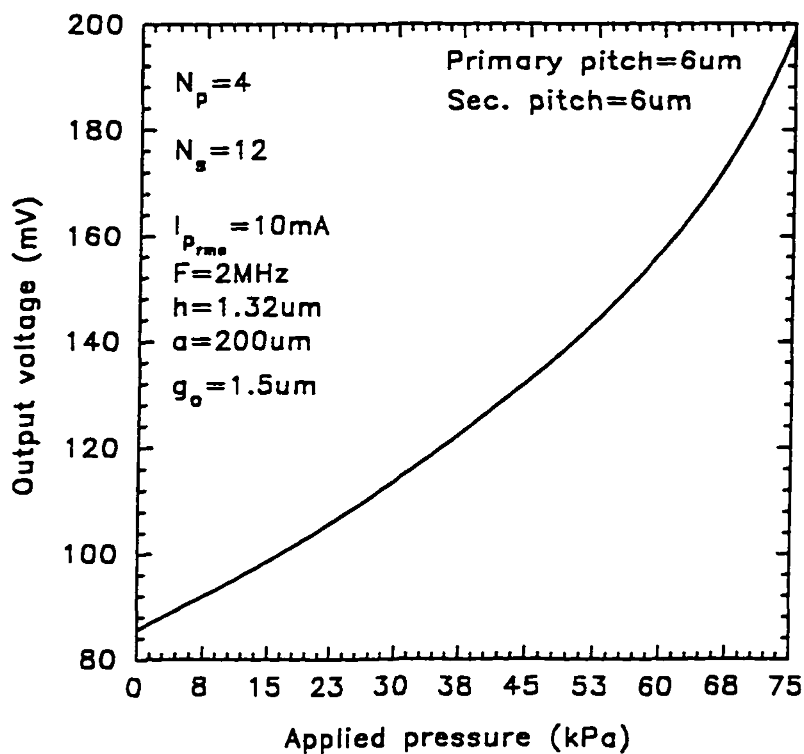

Fig. 8-3. (a) Output voltage versus pressure for large deflections. (b) Output voltage versus pressure for small deflections. (Primary/Secondary coil pitch = 6μm)

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8.2 Power Budget

Power dissipation in devices is crucial. High dissipation reduces the life time of conductors and other active elements. Generally, the calculation of power dissipation is expressed as

$$I^2R \text{ [Watts]}$$

where I is the current and R is the resistance. We therefore need to know the effective resistance of both the primary and secondary coils. For a Tantalum Silicide conductor, the resistivity is given to be $50\mu\Omega$-cm. The equation for resistance in terms of resistivity is

$$R = \rho\frac{l}{A}[\Omega]$$

where l is the length of the conductor (um), A is the crossection area (um^2), and ρ is the resistivity (Ω-cm). The dimension of conductors used has width of 4um and thickness of .25um. Therefore, for an 8um primary/secondary coil pitch, the primary coil has a total length of 534um. The input power dissipated is calculated as

$$P_{in} = (0.01\text{A})^2 \times 50 \times 10^{-8}\,\Omega\text{m}\frac{534 \times 10^{-6}\,\text{m}}{.25 \times 4 \times 10^{-12}\,\text{m}^2} = 26.7\text{mW}$$

$$P_{out_{max}} = \frac{\left(175 \times 10^{-3}\,\text{V}\right)^2}{\left[50 \times 10^{-8}\,\Omega\text{m}\frac{2404 \times 10^{-6}\,\text{m}}{.25 \times 4 \times 10^{-12}\,\text{m}^2}\right]} = 25.4\,\mu\,\text{Watts},$$

for large deflection and In the case of 6um pitch primary/secondary coils, the input power dissipation is

$$P_{in} = (0.01\text{A})^2 \times 50 \times 10^{-8}\,\Omega\text{m}\frac{598 \times 10^{-6}\,\text{m}}{.25 \times 4 \times 10^{-12}\,\text{m}^2} = 29.9\text{mWatts}$$

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$$\text{and } P_{out_{max}} = \frac{\left(350 \times 10^{-3}\,\text{V}\right)^2}{50 \times 10^{-8}\,\Omega\text{m}\,\dfrac{3.18 \times 10^{-3}\,\text{m}}{.25 \times 4 \times 10^{-12}\,\text{m}^2}} = 77\,\mu\,\text{Watts},$$

for large deflections.

The disadvantage of more compact turns is that more power is dissipated. The tradeoff in power for output voltage span is determined by the power specification.

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CHAPTER 9
PHYSICAL SENSOR DESIGN

The design of the high-temperature pressure sensor takes into consideration two different process technologies. One is the single-wafer process in which only one wafer is used. The other is the wafer-to-wafer bonding process in which two wafers are utilized. The rationale for adopting two processes is to explore the unique advantages each posses. The mask designs for both processes are done with **MENTOR GRAPHICS version** 7 Chipgragh layout simulator (39). Final version of the designs are then converted into **GDSII** stream format and transmitted to the photo mask maker.

9.1 Mask Designs For Single-Wafer Fabrication

The first level mask is the cavity rim mask shown in fig. 9-1a. The diameter is 200μm. On this level, an alignment mark is made in order to align the next mask level to the previous. The base diameter of the cavity is a few microns less than the rim diameter because the anisotropic etching of a <100> orientation creates an incline that makes a 54.7^{o} angle with the rim plane. Therefore, for a 200μm rim diameter, the effective base diameter will be 197μm.

The next mask level is secondary coil link to output voltage 1 (V_{out} 1) shown in fig. 9-1b. The total strip length is 100μm to the bonding pad contact. The bonding pad contact is 100x100μm^2. We see the alignment mark (hatch cross) made to align with the earlier cavity mask. The other mark is created to align with the next level mask. Figure 9-1c shows the contact hole mask. This is a dark field mask meant to expose the photoresist only at the shaded areas. That then makes it possible to etch through the 4x4μm^2 contact hole at the center to expose the a portion of the secondary coil link. The large square shade is made to expose the contact pad of the secondary coil link into which

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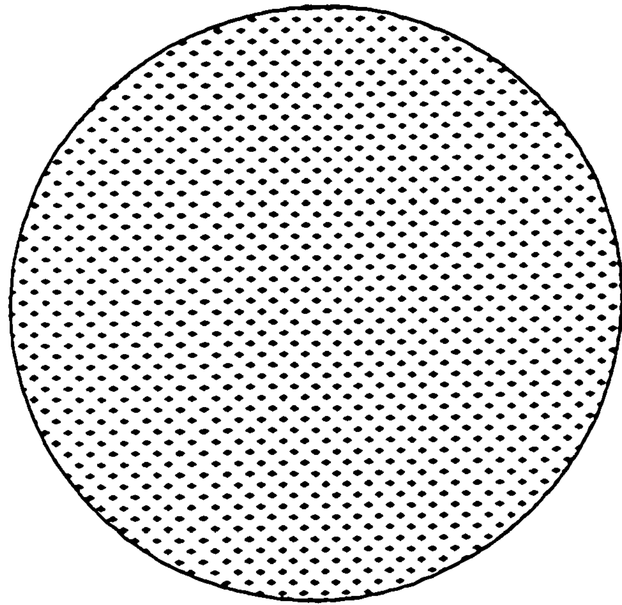

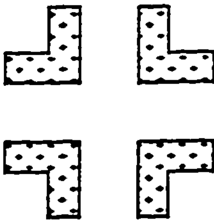

Fig. 9-1a Mask 1. cavity rim mask. Single-wafer process

Silicide would be sputtered. The bottom alignment mark is used to align with the previous layer while the top mark aligns the next level to the bottom level. Mask four, fig. 9-1d, is used to pattern the secondary coil and second output terminal (V_{out} 2). Again we see the sequence of alignment marks. The mark on the left aligns with the bottom while that on the right aligns with the next level. On the right is a square shade. The patterned square

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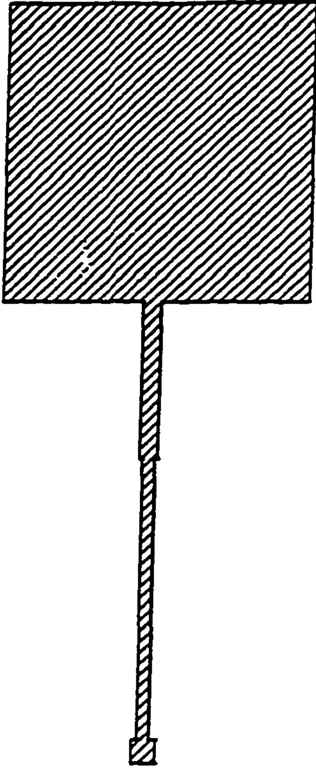

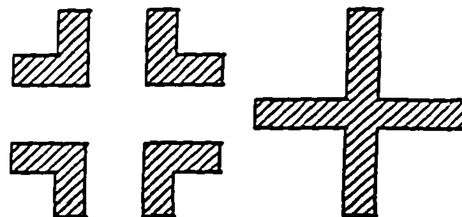

Fig. 9-1b Mask 2. Secondary coil link to $V_{out}1$ terminal mask. Single-wafer process would form a contact with the bottom secondary coil link in order to "raise" its foundation to the same planar level as the other output terminal. In fig. 9-1e, we see mask five to be

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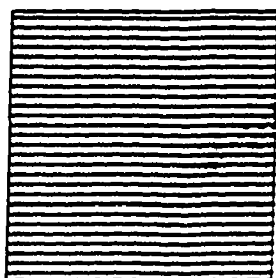

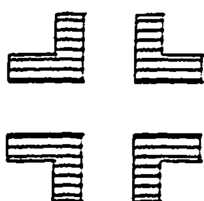

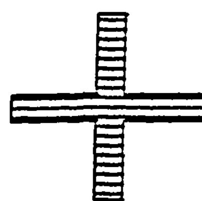

Fig. 9-1c Mask 3. Contact hole to connect secondary coil link to secondary coil to create a loop. Single-wafer process.

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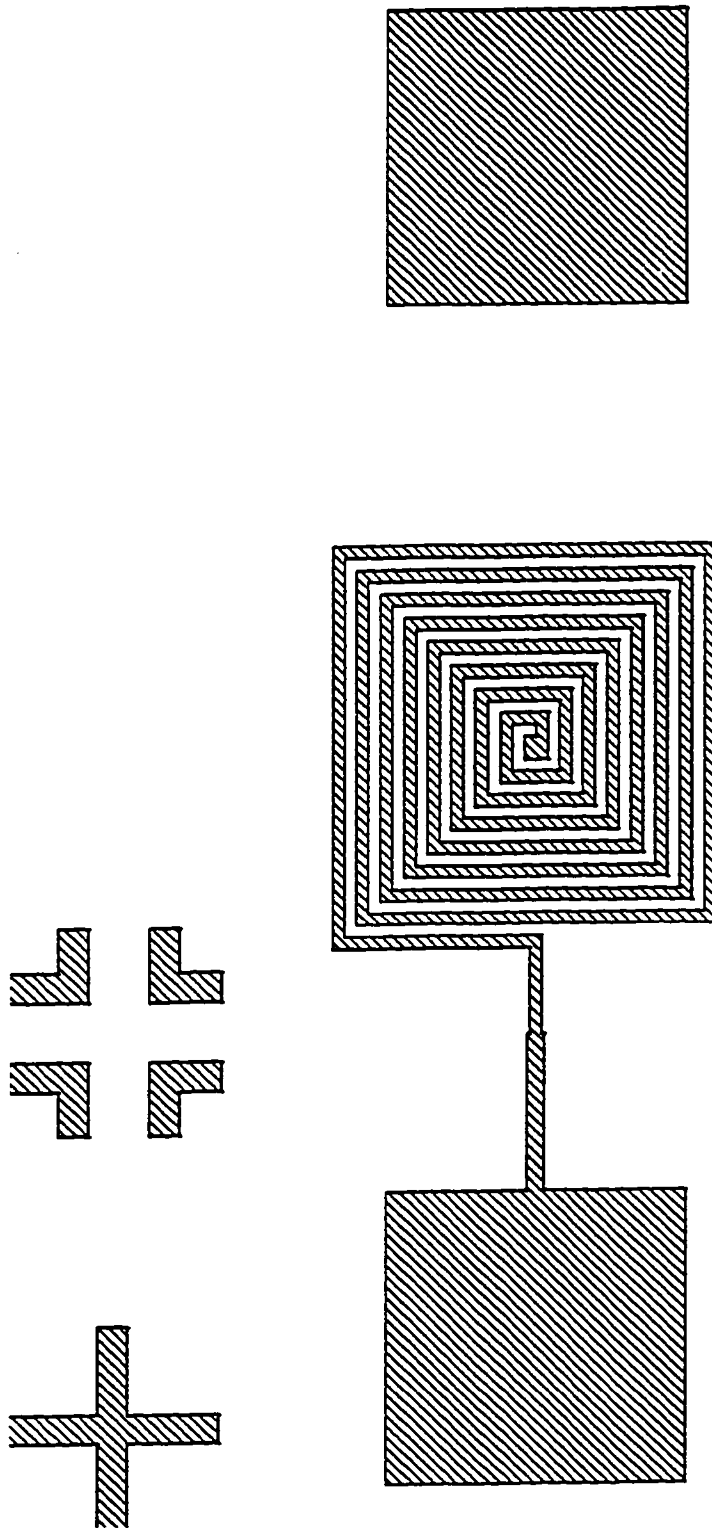

Fig. 9-1d Mask 4. Secondary coil and V_{out} 2 terminal mask Single-wafer process.

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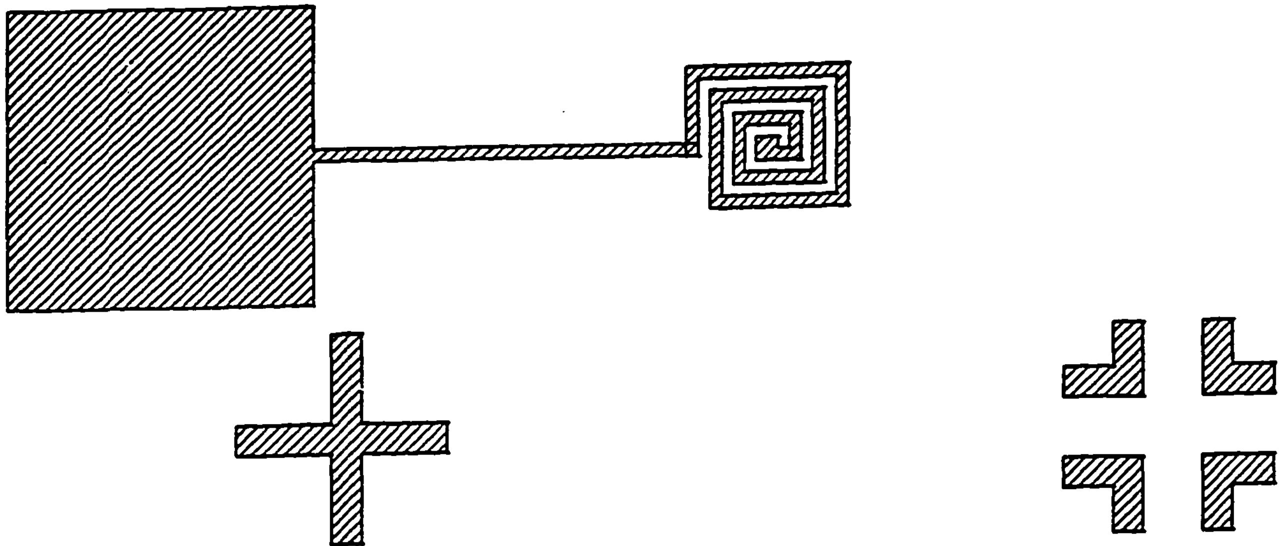

Fig. 9-1e Mask 5.Primary coil and Input terminal 1 (V_{in} 1) mask. Single-wafer process

used for patterning the primary coil and associated alignment marks. The input terminal (V_{in} 1) is set at 90° with the output terminals. The next mask level is mask six shown in fig. 9-1f. This is a dark field mask that will be used to create the fluidic via and edge. The fluidic via are intended for opening the cavity that is hitherto covered with nitride. This mask level is the most critical of all the steps. As has been discussed, two nitride layers sandwich the primary coil. This mask is aligned so that the shortest distance between the fluidic via and a conductor is not less than $10\mu m$. It is envisaged that by the

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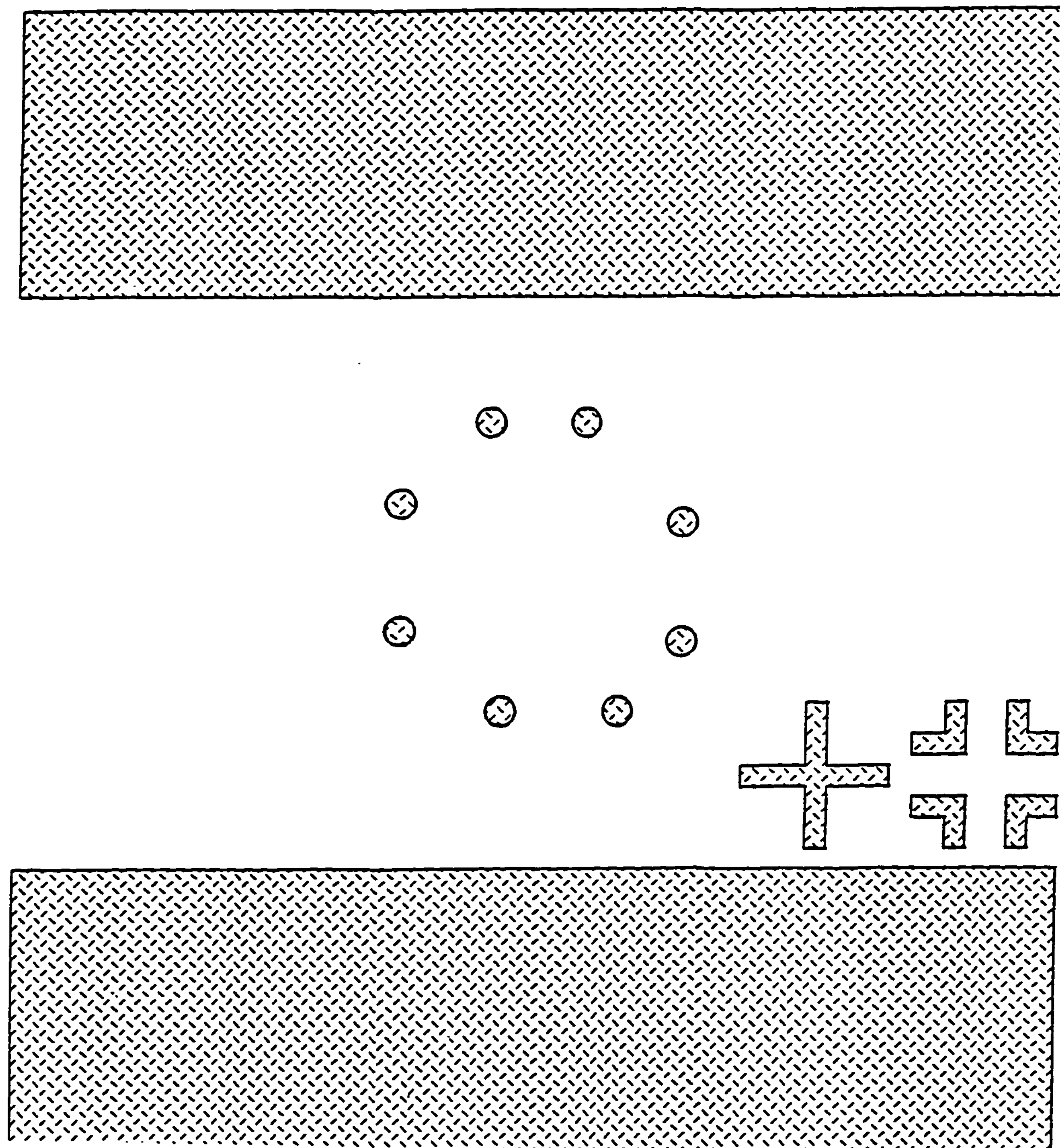

Fig. 9-1f. Mask 6. Fluidic via and edge mask. Single-wafer process

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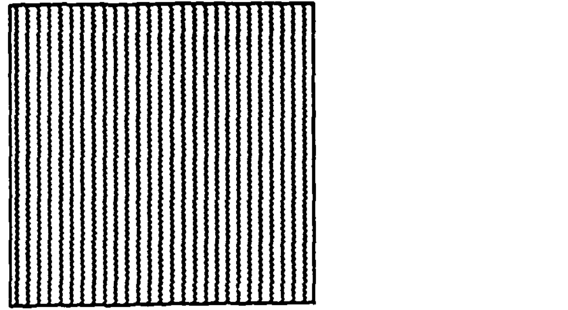

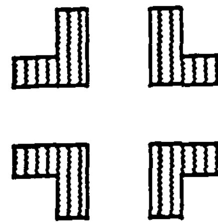

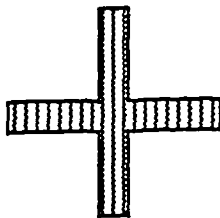

Fig. 9-1g Mask 7. Contact hole to connect primary coil and primary coil link to form a loop.

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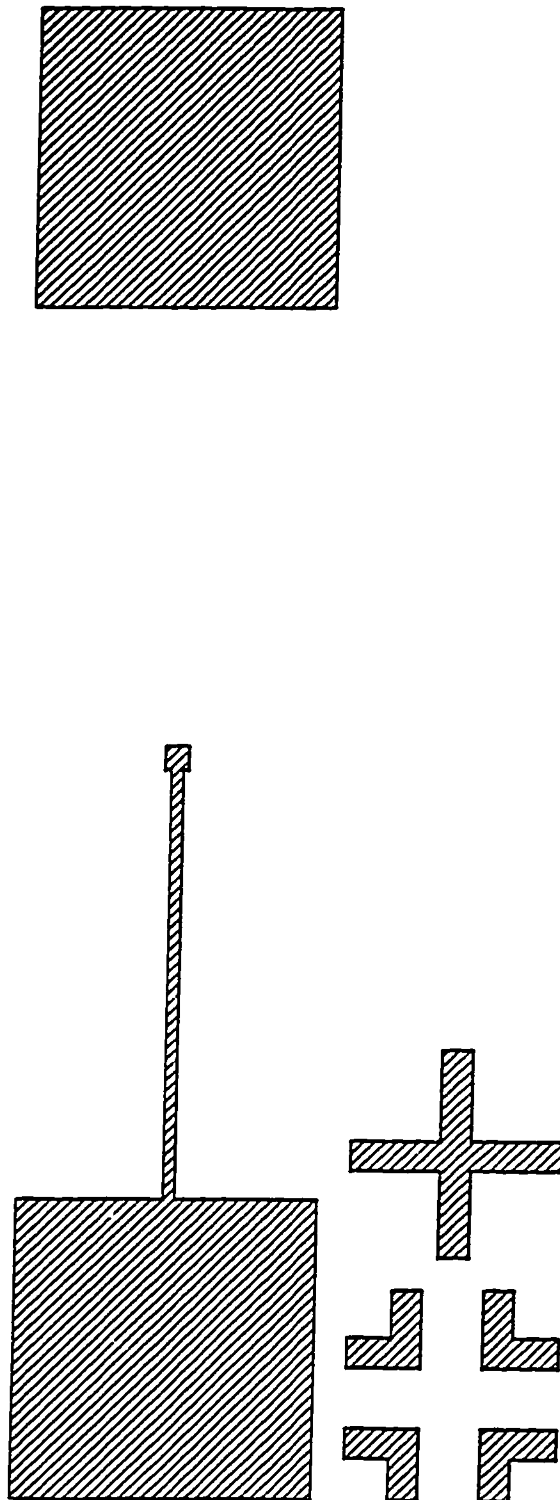

Fig. 9-1h. Mask 8. Primary coil link and $V_{in}2$ mask. Single-wafer process.

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time the Spin-On-Glass (SOG) inside the cavity is sacrificed, the Buffered Oxide Etch (BOE), being a slow nitride etchant will not expose and attack the conductor. The edge

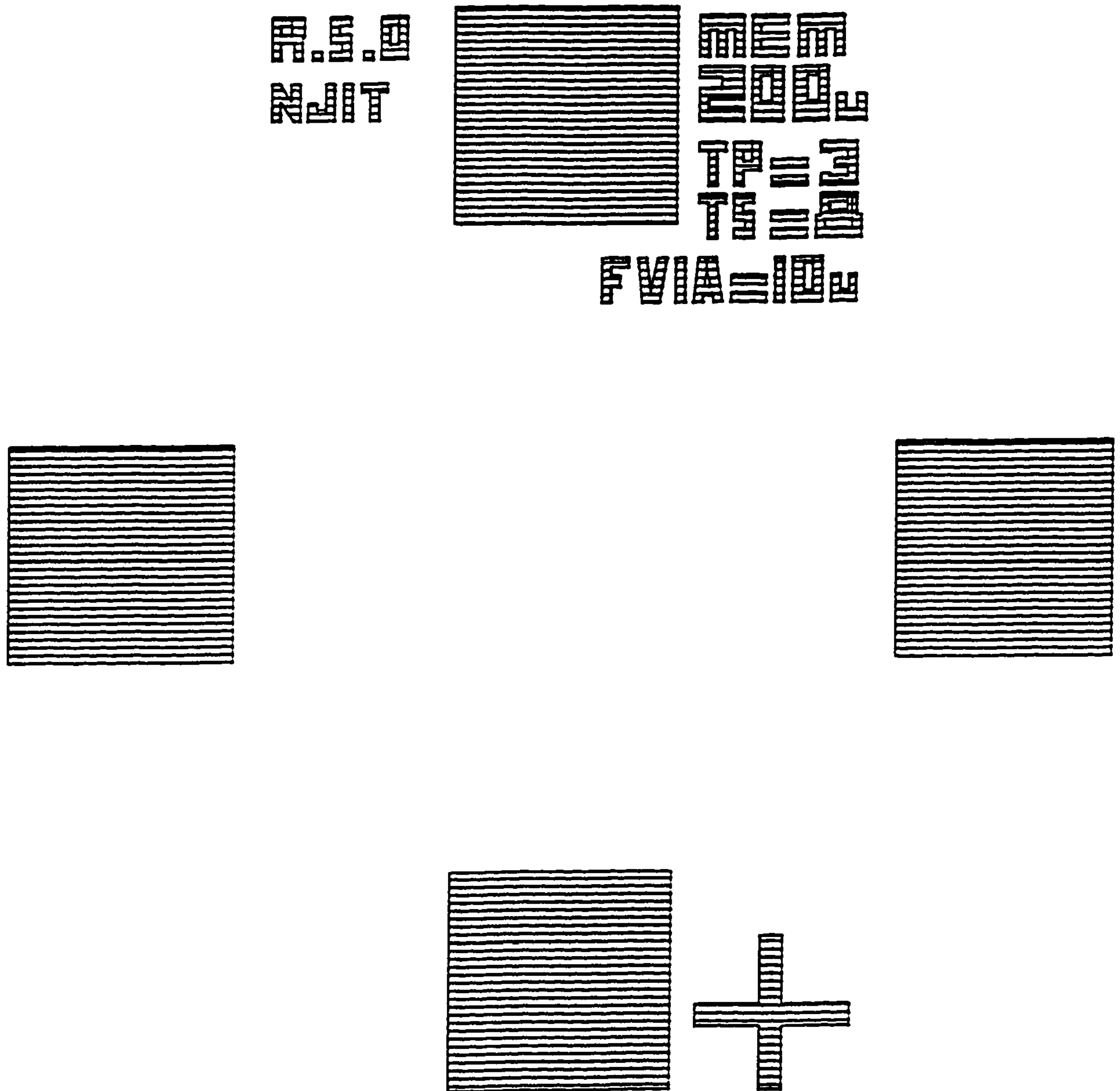

Fig. 9-1i Mask 9. Pad contacts. Single-wafer process.

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etch are the two vertical shaded bars. It allows a vertical etching of the nitride layers down to the cavity rim. This process makes it possible to eventually etch the four bonding contacts at the same time, thereby saving one mask level and process step. Mask seven is shown in fig. 9-1g. This mask level is a dark field. It is used to open the contact hole to expose a $4x4\mu m^2$ pattern of the primary coil for the purpose of creating a current loop with the next metal level eight shown in fig. 9-1h. Finally, fig. 9-1i is mask nine, the dark field mask that opens the four terminals for wire bonding. A complete set of the above masks are shown in fig. 9-2 to indicate how all the alignment marks are positioned with respect to each other.

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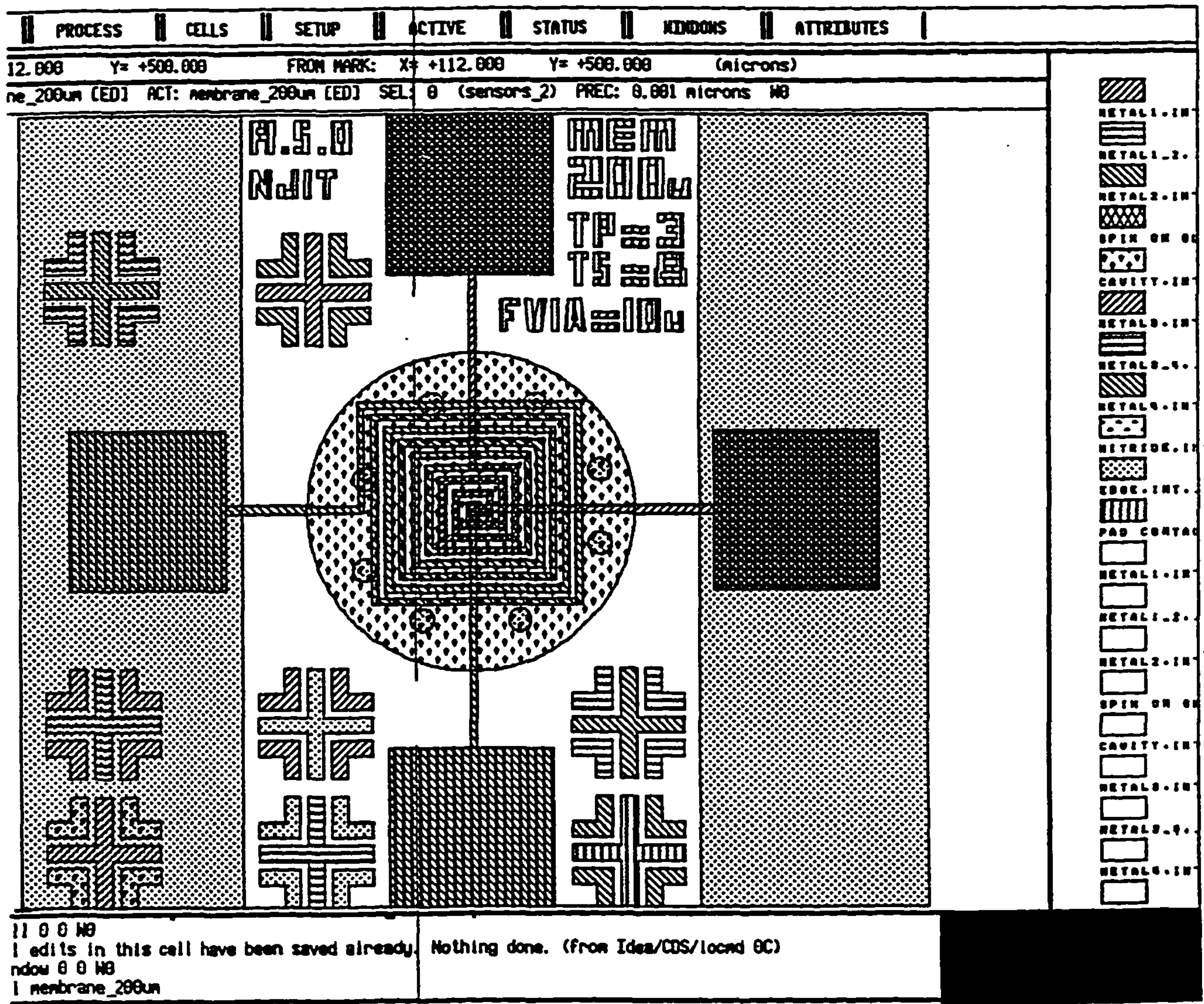

Fig. 9-2 Mask levels 1-9 for Single-wafer process

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9.2 Mask Design For Wafer-to-Wafer Bonding Process

For the wafer bonding process, mask levels one to four is the same as in single wafer process. These masks represent the set that is used on the bottom wafer for both processes. With wafer bonding, the second set contains five masks for processing the top wafer. The first mask of set two is the primary coil link to input terminal 2 (V_{in} 2) shown in fig. 9-3a. This is followed by set two mask 2 shown in figure 9-3b. This mask opens

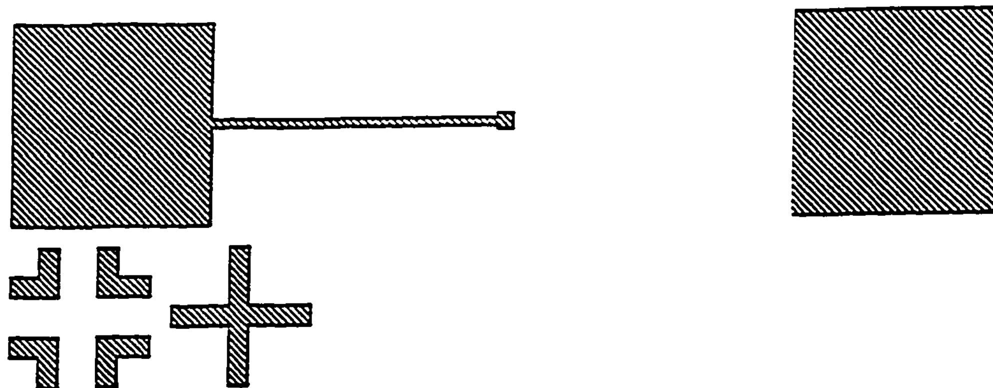

Fig. 9-3a Mask 1 of set 2. Primary coil link to primary coil. Wafer bonding process.

the contact hole to expose the primary coil link to terminal 2. It also opens a pad contact hole for the next process level, which is sputtering of Silicide. Mask three of set two patterns the deposited conductor to form the primary coil and the second input terminal (V_{in} 1) shown in fig. 9-3c. After this second wafer is bonded to the bottom one and lapped to desired thickness, mask four of set two, fig. 9-3d, is used to pattern the edge for the eventual vertical etch to the plane of the cavity rim. This is a dark field mask and has no fluidic via as in single wafer process because in the wafer bonding process, no holes

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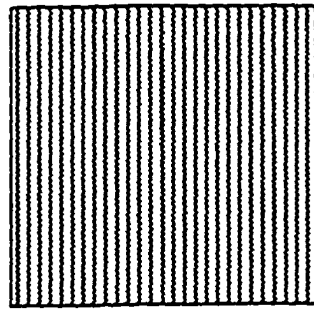

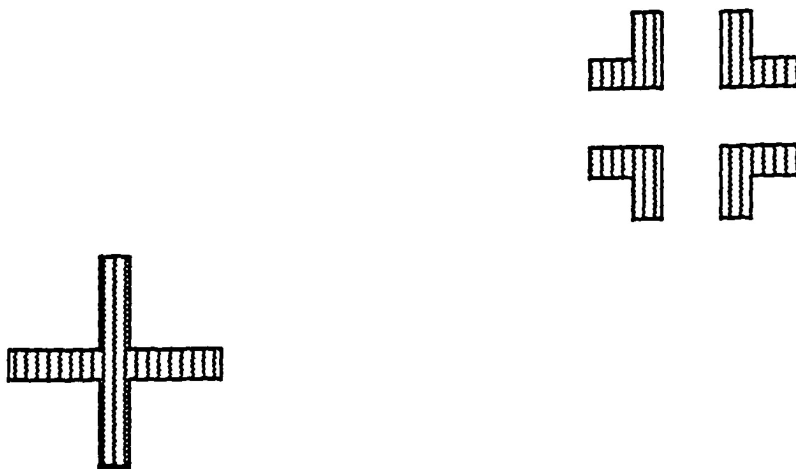

Fig. 9-3b Mask 2, set 2. Contact via to connect primary coil to link.

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are needed to open up the cavity. The membrane, once created through lapping of the top wafer, is untouched. Finally, mask five of set two is used to pattern the bonding pad contacts. This is shown in fig. 9-3e.

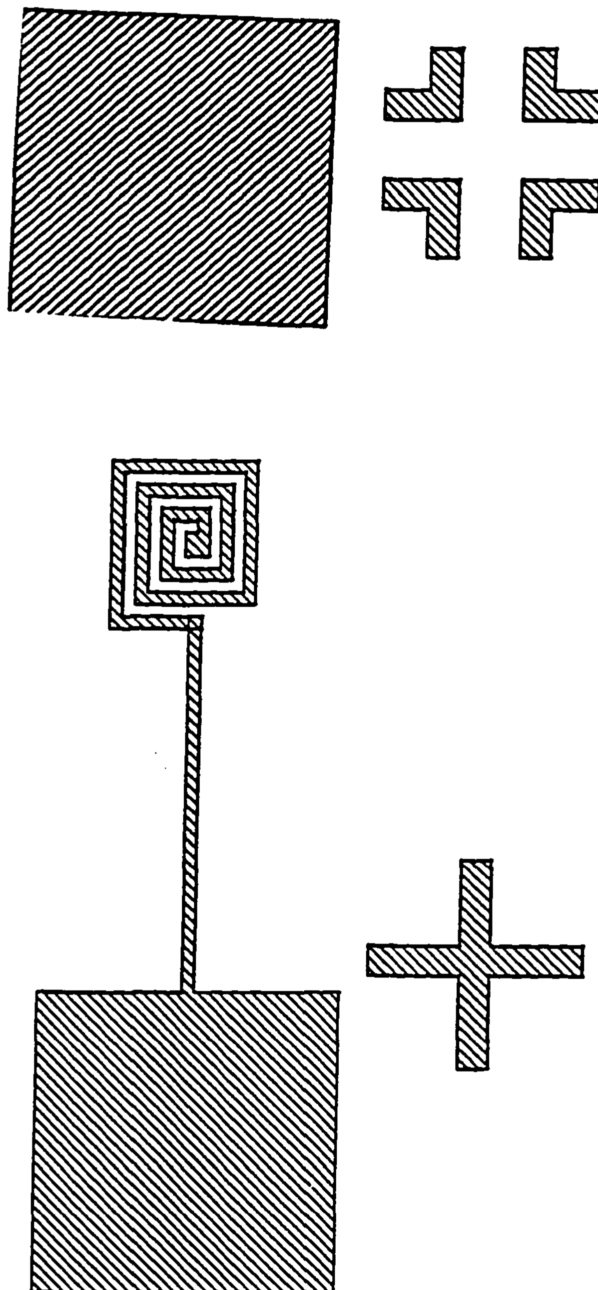

Fig. 9-3c Mask 3, set 2. Primary coil and input terminal 2 mask.

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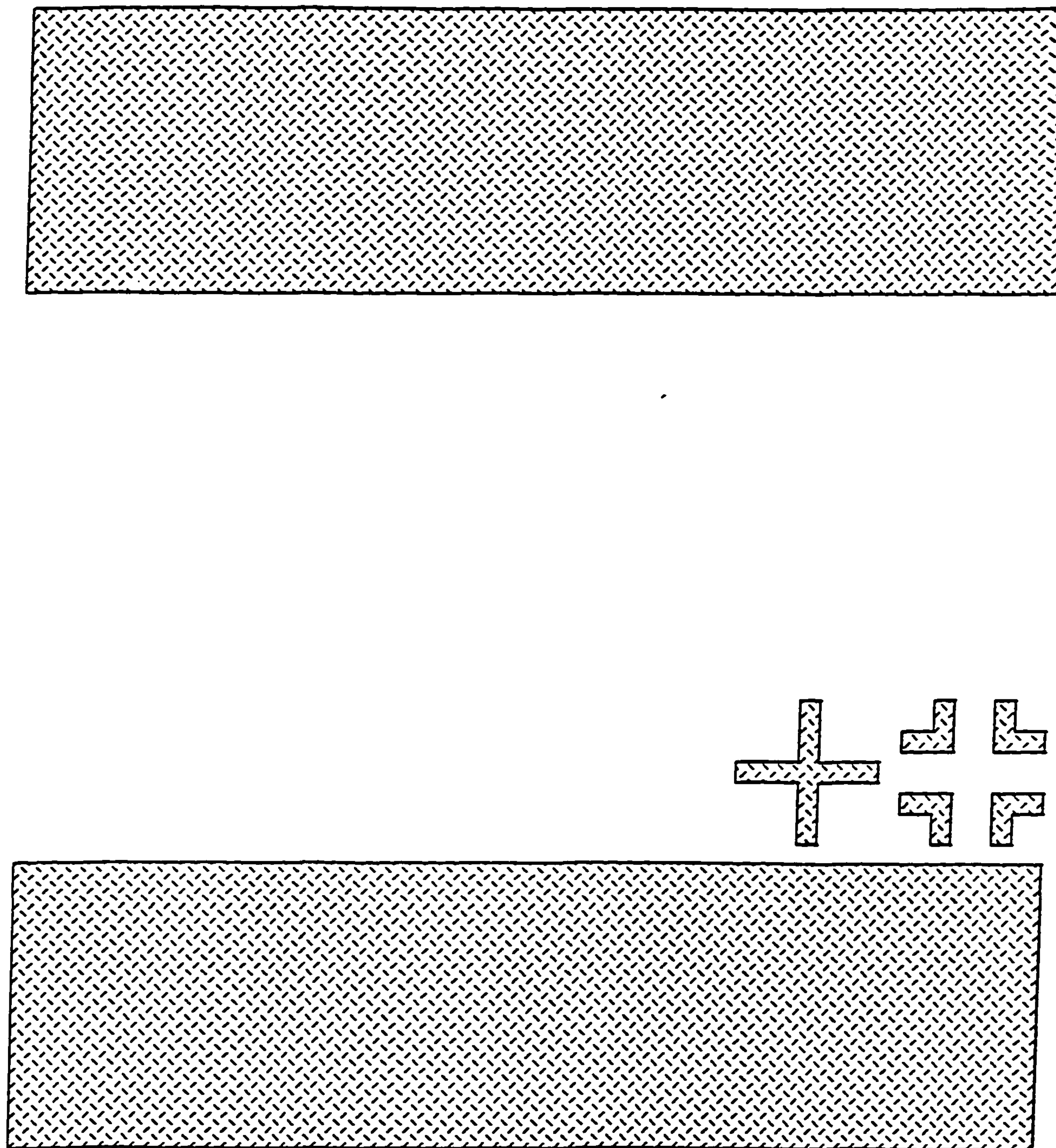

Fig. 9-3d Mask 4 set 2. Edge mask. Wafer-to-Wafer bonding.

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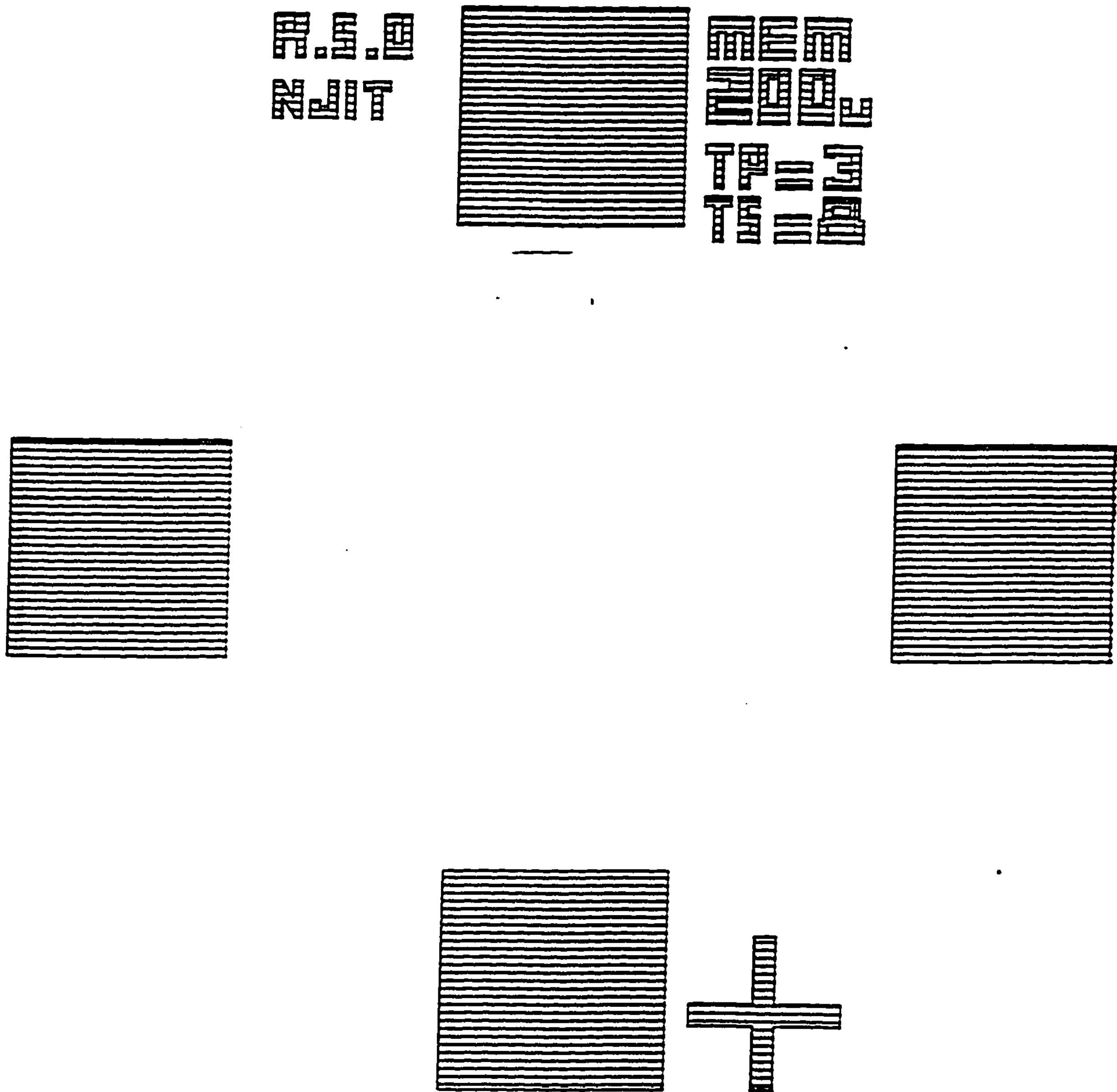

Fig. 9-3e Contact pad mask. Wafer-to-Wafer bonding.

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CHAPTER 10
FABRICATION PROCESS

The design of the high temperature pressure sensor follows the design rule of the Microelectronics Research Center of the New Jersey Institute of Technology where the device would be fabricated. The design decision takes into consideration problems of high temperature operation. Typical of such problems are degradation of the performance of piezoresistors at elevated temperatures and also TCE mismatch. To resolve the problems, the device uses Tantalum Silicide ($TaSi_2$) as a coil conductor for its excellent properties. It has a high melting point that makes it stable to 650°C. The low resistivity (50$\mu\Omega$-cm) makes it viable for low power dissipation devices. This thesis presents two fabrication processes. One is the single wafer process and the other is the wafer-to-wafer fusion bonding process. Evidently, by using double wafers in the bonding process, the cost advantage seem to go to single wafer process. It is important to consider all the advantages each technology has over the other before determining which process is appropriate to use.

10.1 Single-Wafer Fabrication

Single-Wafer fabrication process flow is shown graphically in fig. 10-1a-i. The starting material is a <100> silicon wafer (n-type) polished on one side.

Step 1:

Wafer preclean for 10minutes in 10:1 H_2SO_4:H_2O_2 at 110°C.

Rinse and spin-dried for 5 minutes.

Furnace pre-clean follows. Dip in 100:1 H_2O:HF for one minute.

Rinsed in DI water and spin-dry.

Apply photoresist.

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Mask 1 defines the cavity rim diameter.

Expose photoresist to define cavity diameter. Develop photoresist.

Etch in 95°C KOH for five minutes to create an 3 μm deep cavity, fig. 10-1a.

Strip photoresist with J100. Rinse in Trichloroehtylene (TCE) and in DI water, and spin-dry.

Grow oxide, (fig. 10-1b) in steam at 950°C for 50 minutes to yield 1000 Å thick oxide. Main oxygen flow rate is 7.5 L/min and oxygen through bubbler is 0.53 L/min.

Sputter 2500 Å Tantalum Silicide ($TaSi_2$).

Anneal at 900°C in Argon ambient for 30minutes.

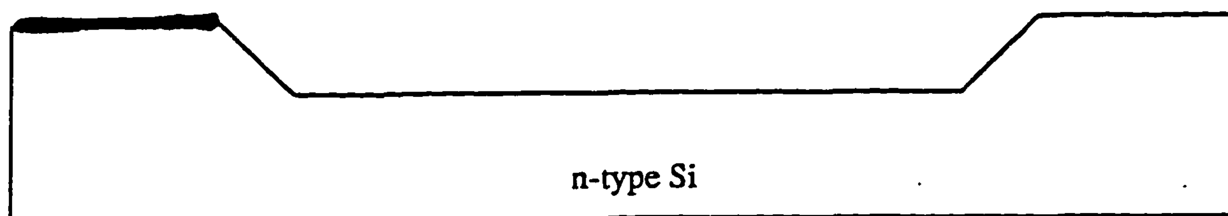

Fig. 10-1a Etched cavity in n-type silicon wafer.

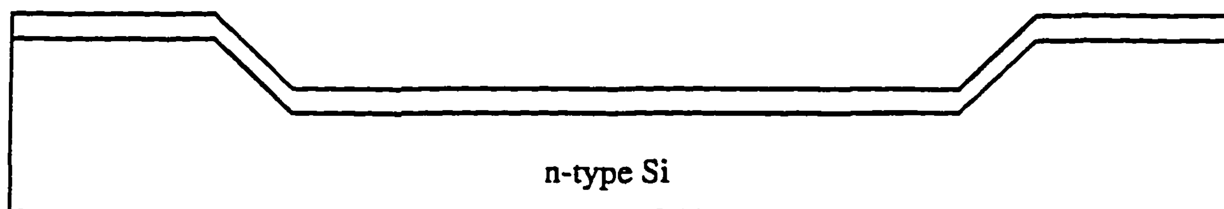

Fig. 10-1b Steam-grown 1000 Å oxide.

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Step 2: Fig. 10.1-1c

Apply photoresist on blanket Silicide.

Mask 2 defines secondary coil link and output voltage terminal 1.

Expose photoresist and develop.

Etch Silicide in 10:1 BHF for 8 minutes (etch rate 300Å/min) to pattern secondary coil link and Vout 1 terminal.

LPCVD 1000Å Si_3N_4.

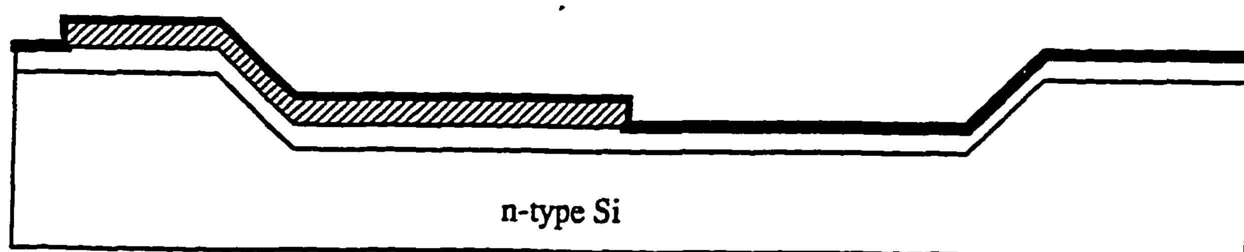

Fig. 10-1c Deposition of first level conductor and first layer nitride

Step 3:

Apply photoresist.

Mask 3 defines central via and V_{out} 1 terminal thickness enhancement.

Expose resist. Develop.

Plasma-etch nitride in 70%CF_4/30%O_2 for 5minutes to open central via and V_{out} 1 terminal thickness enhancement.

Sputter 2500Å Tantalum Silicide ($TaSi_2$).

Anneal at 900°C in Argon ambient for 30minutes.

Step 4: Fig. 10-1d

Apply photoresist on blanket Silicide.

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Mask 4 defines secondary coil, output voltage terminal 2, and Vout 1.

Expose photoresist and develop.

Etch Silicide in 10:1 BHF for 8 minutes to pattern secondary coil, output voltage terminal 2, and "raises" Vout 1 terminal to V_{out} 2 terminal plane.

LPCVD 1000Å Si_3N_4 to complete encapsulation of secondary coil.

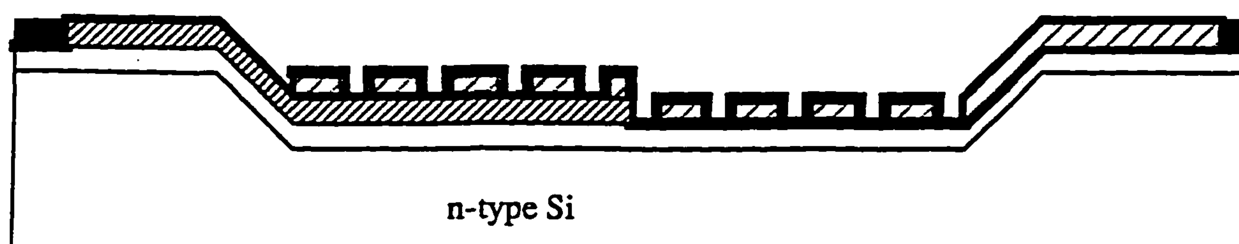

Fig. 10-1d $TaSi_2$ sandwiched between two nitride layers-Symmetrical Layering.

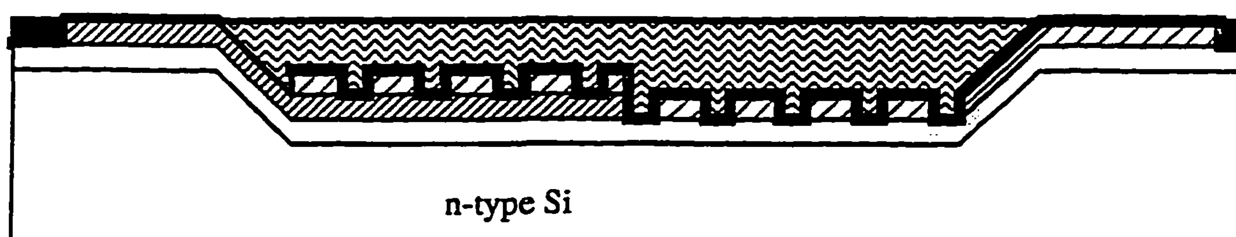

Fig. 10-1e Spin-On-Glass (SOG) in cavity and planarized at the rim.

Spin-On-Glass to cover cavity, fig. 10.1-1e

Apply photoresist.

Apply negative of cavity mask to define cavity rim edge.

Expose and develop.

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Etch SOG 100:1 H_2O:HF for 10seconds to planarize cavity rim.

LPCVD 1000Å Si_3N_4.

Sputter 2500Å Tantalum Silicide ($TaSi_2$).

Anneal at 900°C in Argon ambient for 30minutes.

Step 5: Fig 10.1-1f

Apply photoresist on blanket Silicide.

Mask 5 defines primary coil and input voltage terminal 1 (V_{in} 1).

Expose photoresist and develop.

Etch Silicide 10:1 BHF for 8 minutes to pattern primary coil V_{in} 1 terminal.

LPCVD 1000Å Si_3N_4 to complete the encapsulation of primary coil.

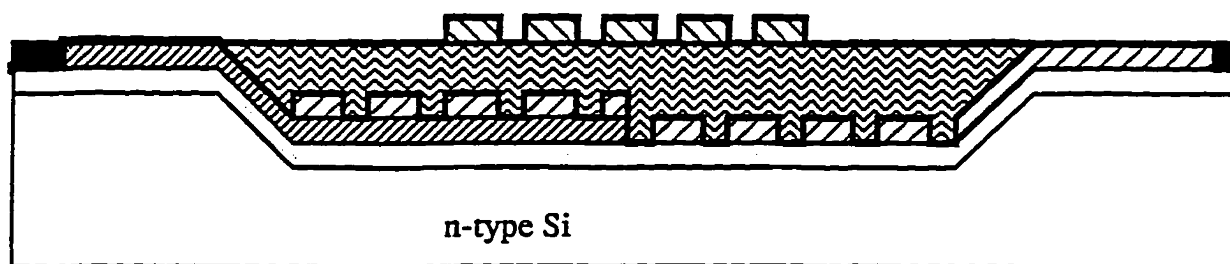

Fig. 10-1f The encapsulation of primary coil in nitride.

Step 6: Fig. 10-1g

Apply photoresist

Mask 6 defines fluidic via and edge.

Plasma-etch nitride in 70%CF_4/30%O_2 for 10minutes to open holes into Spin-On-Glass.

Etch sacrificial SOG in cavity with 49%HF

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LPCVD 1000Å Si_3N_4 to seal fluidic via-fig. 10-1h.

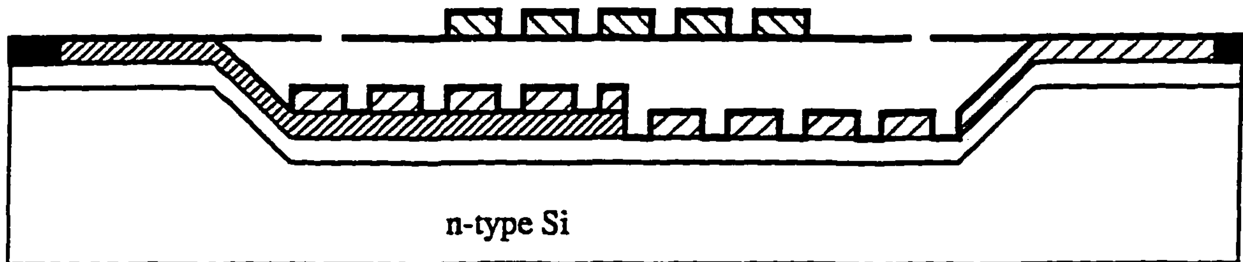

Fig. 10-1g Opening of the fluidic via by plasma etching to expose sacrificial SOG

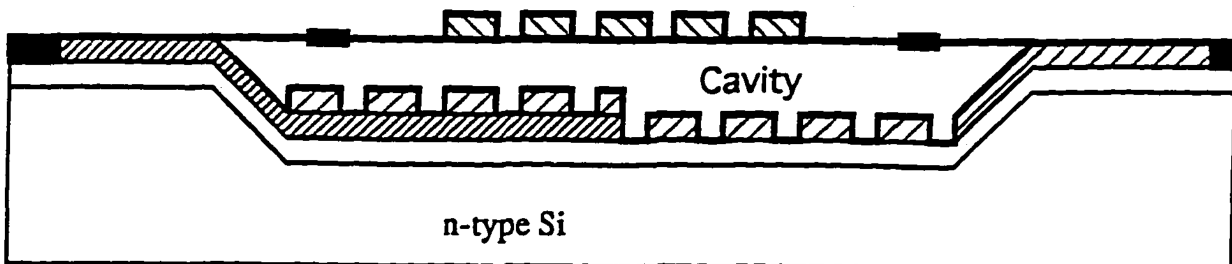

Fig. 10-1h Sealing of fluidic via to create near-vacuum cavity.

Step 7:

Apply photoresist.

Mask 7 defines central via and V_{in} 1 terminal height enhancement.

Expose resist. Develop.

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Plasma-etch nitride in 70%CF_4/30%O_2 for 5minutes to open central via and V_{in} 1 terminal height enhancement.

Sputter 2500Å Tantalum Silicide ($TaSi_2$).

Anneal at 900°C in Argon ambient for 30minutes.

Step 8:

Apply photoresist on blanket Silicide.

Mask 8 defines primary coil link and input voltage terminal 2 (V_{in} 2).

Expose photoresist and develop.

Etch Silicide 10:1 BHF for 8 minutes to pattern primary coil link and V_{in} 2 terminal.

CVD 200Å by Low Temperature Oxidation (LTO)

LPCVD 1um Polysilicon.

Step 9: Fig. 10-1i

Apply photoresist.

Mask 9 defines pad contact holes.

Expose and develop resist.

Etch polysilicon with 1%HF in HNO_3

Etch Oxide in Buffered Oxide Etch (BOE) to open input contact pads.

Selectively etch nitride in hot H_3PO_4 to open output contact pads.

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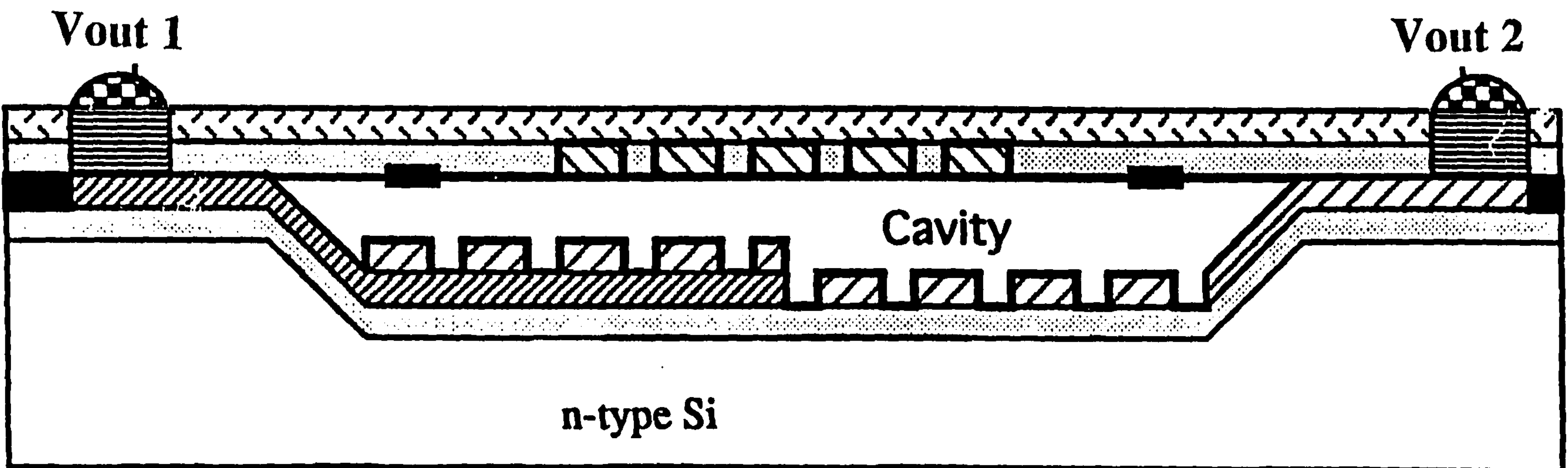

Fig.10-1i Crossection of high-temperature pressure sensor using single-wafer process.

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10.2 Wafer-to-Wafer Bonding Fabrication Process

Wafer One

Repeat steps one to four is the same as in the single wafer process.

Wafer Two

Step 1: Fig. 10-2a

LPCVD 1000Å Si_3N_4

Sputter 2500Å Tantalum Silicide ($TaSi_2$).

Anneal at 900°C in Argon ambient for 30minutes.

Apply photoresist on blanket Silicide.

Mask 1 of wafer 2 defines primary coil link, input voltage terminal 2 (V_{in} 2), and V_{in} 1 height enhancement.

Expose photoresist and develop.

Etch Silicide 10:1 BHF for 8 minutes to pattern primary coil V_{in} 2 terminal and V_{in} 1 height enhancement.

LPCVD 1000Å Si_3N_4

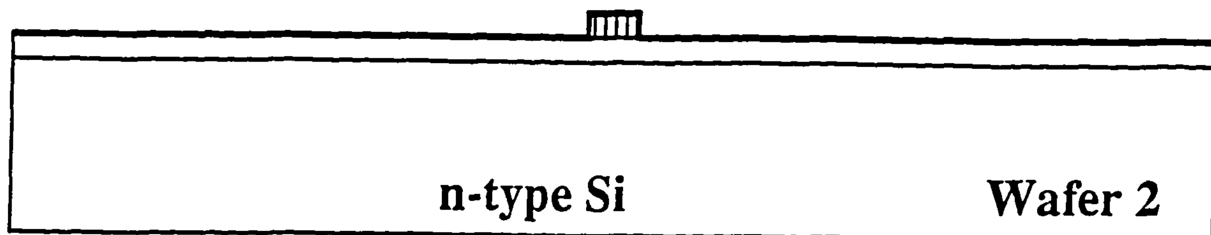

Fig. 10-2a Crossection view of primary coil link on wafer 2

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Step 2:

Apply photoresist

Mask 2 of wafer 2 defines the contact hole to connect link with coil.

Plasma-etch nitride in $70\% CF_4/30\% O_2$ for 5 minutes to open via.

Sputter 2500Å Tantalum Silicide ($TaSi_2$).

Anneal at 900^oC in Argon ambient for 30minutes.

Step 3: Fig. 10-2b

Apply photoresist on blanket Silicide.

Mask 3 of wafer 2 defines the primary coil

Expose resist and develop.

Etch Silicide 10:1 BHF for 8 minutes to pattern primary coil and V_{in} 1 terminal.

LPCVD 1000Å Si_3N_4.

CVD 200Å oxide by Low Temperature Oxidation (LTO)

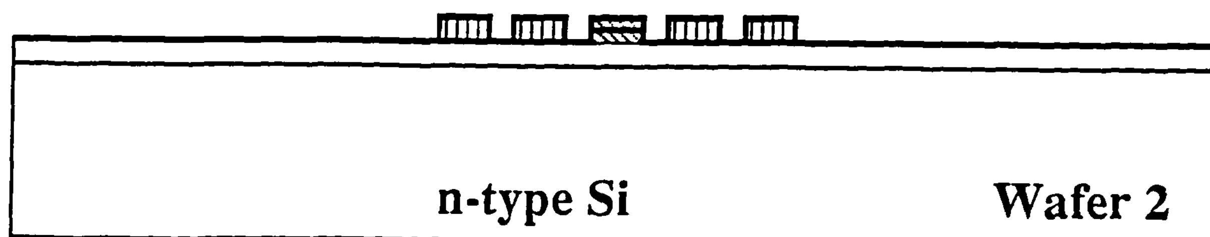

Fig. 10-2b Encapsulation of primary coil in nitride

Step 4: Fig. 10-2c

Spin SOG on wafer 2

Flip wafer 2, align and bond to wafer 1

Bake in nitrogen ambient at 1100^oC to bond.(40)

Etch back wafer 2 to 1um thickness. (36)

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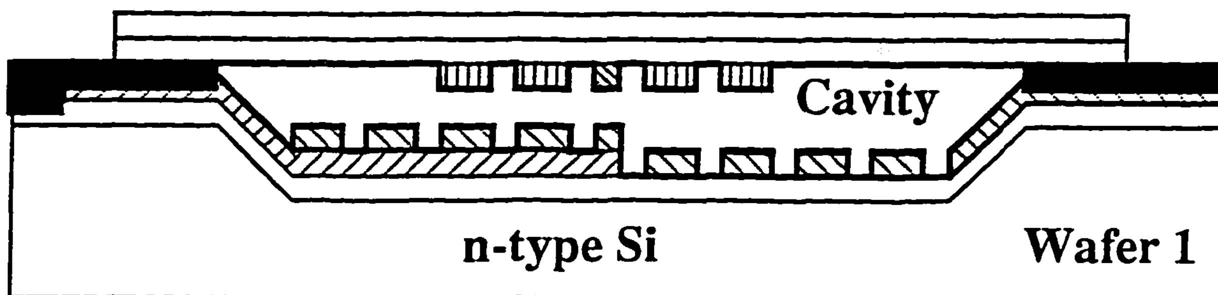

Fig. 10-2c Wafer 2 bonded to wafer 1 and wafer 2 is etched back to 1 μm thickness

Step 5: Fig. 10-2d

Apply photoresist on wafer 2.

Mask 4 defines the edge

Expose and develop resist

Etch Silicon in 3:5:3 $HF:HNO_3:CH_3COOH$ to nitride.

Selectively etch nitride in hot H_3PO_4 to oxide.

Selectively etch oxide to nitride.

Apply photoresist.

Mask 5 defines the contact pads.

Expose resist and develop.

Selectively etch Silicon in 3:5:3 $HF:HNO_3:CH_3COOH$ to nitride.

Selectively etch nitride in hot H_3PO_4 to open contact pads.

Wire bond pads.

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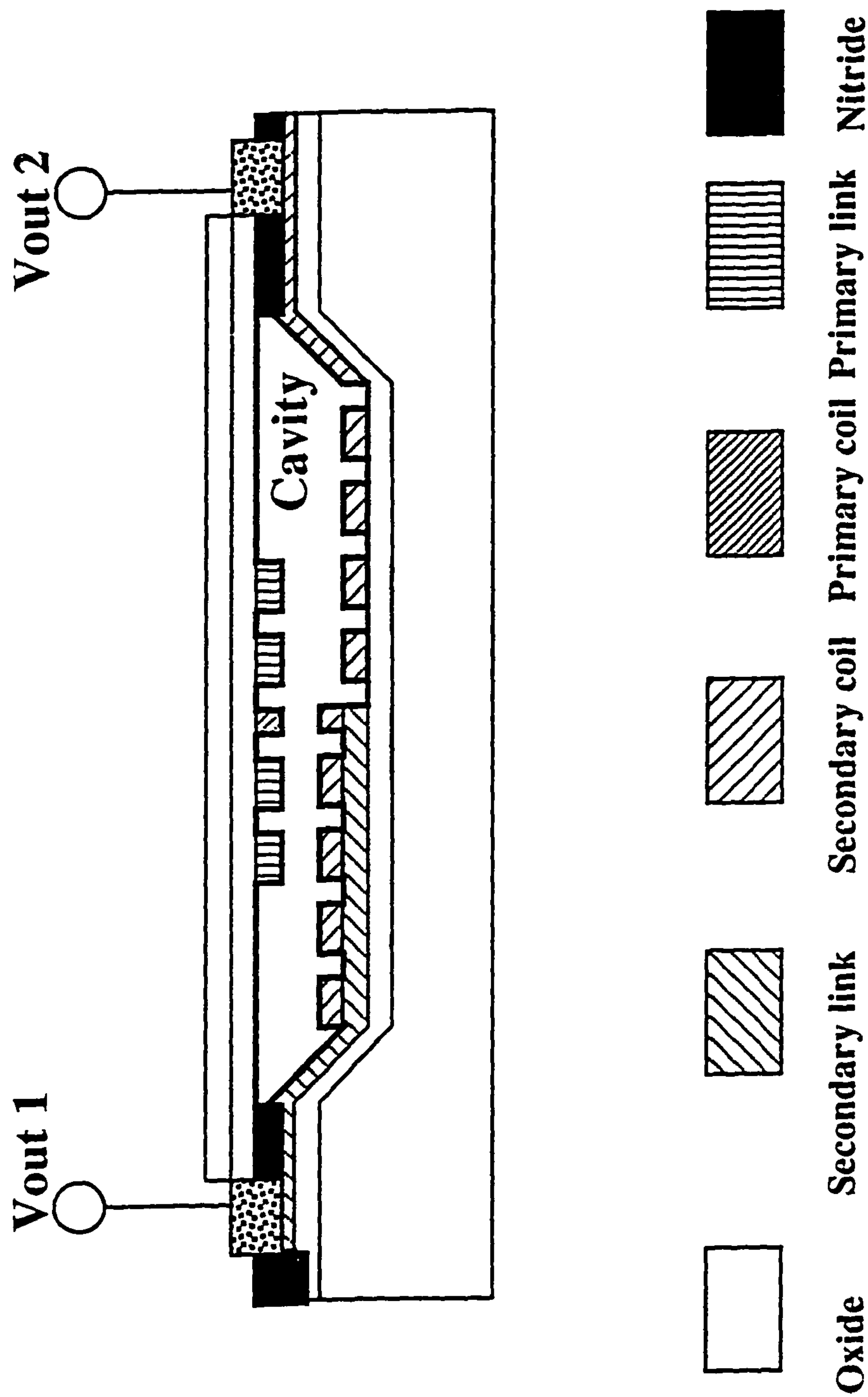

Fig. 10-2d Crossection of the pressure sensor device

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CHAPTER 11
CONCLUSION

This thesis has presented a detailed electrical and process design for a high-temperature silicon pressure sensor by combining the principle of inductive coupling and the theory of deflection of clamped circular plates. The fabrication process flow is also presented based on single-wafer and wafer-wafer fusion bonding technologies. The capability of the pressure sensor to survive environments of temperatures up to $650^{o}C$ has also been presented in detail. The non utilization of temperature-dependent parameters of piezoresistive or capacitive pressure sensors resolves the problems of high leakage current and thermal mismatch. The moderate sensitivity obtained is due to the fact that the evaluation is based on second or higher order equations. This confirms that higher sensitivity is expected from first order analysis. The large output voltage span of over 100mV is an indication of its viability for digitization. The miniature size of the device and the fact that it could be mass produced on wafer opens the possibility for potential large scale commercial exploitation.

In table 11-1, summary of the results of the optimized high temperature pressure sensor is presented and compared it with some temperature-compensated pressure sensors in the market. The sensitivities used are extracted from first order graphical interpretations of the optimized device discussed in chapter eight. A comparison of the voltage transfer function obtained from theoretical, computer and upscale model experimental setup is shown in table 11-2 for a coil gap of 3um and different coil pitches. We see that the results are closely matched.

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11.1 Future Work

The physical realization of this device would help in comparing detailed experimental results with the established analytical evaluation of this thesis. The result would then form the basis for improvement, optimization, and other applications other than high temperature pressure sensors such as an LVDT accelerometer shown in fig. 11-1.

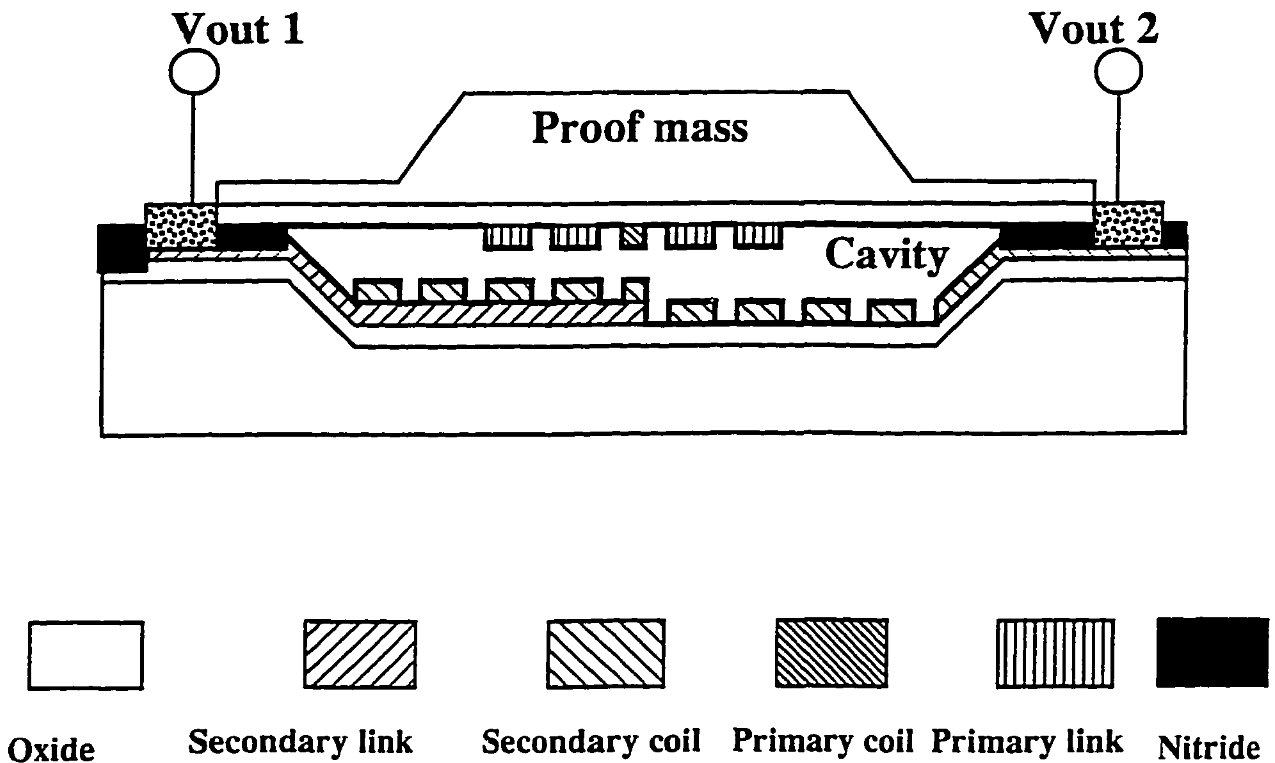

Fig. 11-1 Crossection of proposed LVDT accelerometer

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Characteristics	HT-LVDT Pressure Sensor.	Motorola MPX2700 Series	SenSym LX0XXXG Series
Supply voltage (V)	2	16	16
Temperature Compensation Range (°C)	350-700	-40-125	-40-125
Pressure Range (kPa/Psi)	450/67.5	700/105	±1psig
Pressure Sensitivity (mV/Pa)	0.4	0.057	4.155
Temperature Coefficient of Offset (ppm/°C)	711	1% Full Scale Span offset (0-85°C)	1.5% Full Scale Span Offset (0-50°C)
Voltage Offset (mV)	30	1	2
Output Voltage Span (mV)	240	41.5	30.5
Full Scale Linearity (%)	1.5	0.5	1.5

Table 11-1 Performance comparison of proposed high-temperature pressure sensor with Motorola's and Sensym devices

Ns/Np	Pitch (um)	Analytical model (Volts/Amp)	Numerical calculation - MAXWELL 2-D (Volts/Amp)	Experimental data-upscaled size (Volts/Amp)
8/3	8	5.4	5.8	6
11/4	6	3.5	4	-

Table 11.2 Comparison of voltage transfer function for a 3um coil gap.

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