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# ABSTRACT

## Three Dimensional Magnetic Field Sensors and Array in BiCMOS Technology

by
Bingda Wang

This thesis presents new designs of three dimensional magnetic field sensors in BiCMOS technology. The detailed design of the merged structure device by common diffusion and the high gain transduction circuit are presented. The merged structure has the advantage of less area, less external contacts and less parasitic capacitance. Cross-sensitivity is also eliminated by employing the merged structure. Three active on-chip loads are introduced to improve the sensitivity. The SPICE simulation results show that when a relative change in current $\Delta I/I$ is 0.001, about $13.6mV$and $8.5mV$ can be detected at the output in X(or Y) and Z directions, respectively. The experimental results from a standard (non-merged) BiCMOS magnetic sensor is presented. The 3-D sensor element has been integrated with the signal processing circuits to build a monolithic $8 \times 8$ sensor array. The detailed SPICE simulation results on the critical path shows the array can be operated with elimination of column-to-column offset voltages under a maximum scanning clock speed of about 0.5MHz. The array structure can find application in precise manufacturing as a position sensor .

# THREE DIMENSIONAL MAGNETIC FIELD SENSORS AND ARRAY IN BICMOS TECHNOLOGY

by
Bingda Wang

A Thesis
Submitted to the Faculty of
New Jersey Institute of Technology
in Partial Fulfillment of the Requirements for the Degree of
Master of Science

Department of Electrical and Computer Engineering

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This thesis is dedicated to
My Parents

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And finally, the author wishes to avail himself of this opportunity to extend his heartfelt thanks to his parents, whose profound concern and great encouragement have always been a major inspiration to the author.

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# CHAPTER 1
# INTRODUCTION

Silicon has already revolutionized the way we think about electronics and is now in the process of altering conventional perceptions on sensors and transducers. This holds in particular in the case of magnetic field sensors.

Integrated silicon magnetic field sensors can now be manufactured using standard integrated circuit (IC) processing technologies without invoking additional processing steps such as 'micromachining' or film deposition as in the case of most mechanical or chemical sensors. Integrated sensors are being increasingly developed for a variety of the magnetic field sensitive element together with amplifiers and signal processing circuitry on the same semiconductor chip.

A magnetic field sensors (MFS) is an input transducer that is capable of converting the magnetic field H into a useful electronic signal. A magnetic field sensor is also needed whenever a nonmagnetic signal is detected by means of an intermediary conversion into **H** ('tandem' transduction), e.g., the detection of a current through its magnetic field or the mechanical displacement of a magnet. Thus we can distinguish two main groups of magnetic field sensor applications.

In direct application case, the magnetic field sensor is part of a magneto-meter. Here are some examples:

* Earth magnetic field measurements
* Reading of magnetic tapes and disks
* Recognition of magnetic ink patterns of banknotes and credit cards
* Control of magnetic apparatus

With respect to high-density magnetic recording, some of the recently

devised integrated silicon magnetic field sensors are now able to compete with traditional NiFe thin-film magneto-resistor devices.

In indirect Applications case, the magnetic field is used as an intermediary carriers for detection nonmagnetic signals. Examples are as follow:

* Contactless switching

* Linear and angular displacement detection

* Potential-free current detection

* Integrated wattmeters

Practical applications require the detection of magnetic fields in the range of micro and millitesla. It can be achieved by the integrated semiconductor sensors. Among the above application, each comes with its specific sensor requirements such as the required sensitivity, field resolution and sensor geometry, etc.

Integrated magnetic field sensors have recently employed various device configurations as a means of detecting the presence of a magnetic field vector. These include vertical magnetotransistors[1],[2] (Figure 1.2), lateral magnetotransistors[3-6], Hall devices[7-9], SD-MAGFETs[10],[11] (Figure 1.1) and Suppressed Side Injection Magnetotransistor[12 ](Figure 1.3).

Each type has both advantages and disadvantages in one way or another. In general, high absolute sensitivities can be obtained with SD MAGFET when devices operating in the saturation region and drains are connected with high load resistance. In this case, the useful signal is the differential voltage between the two drains. However, SD MAGFETs are one-dimensional magnetic field sensors since they are only sensitive to the magnetic field perpendicular to the chip surface.

For the detection of magnetic fields in nanotesla range, Dual-Collector

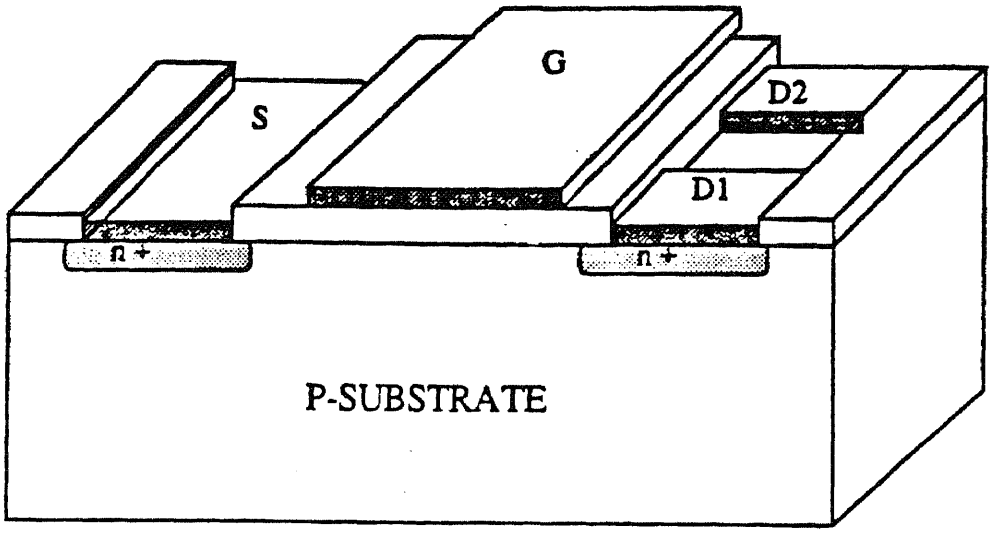



**Figure 1.1** Split-Drain MAGFET

Magnetotransistor with large current gain is desirable. The newly reported Suppressed Sidewall Injection Magnetotransistor displays a range of sensitivities from 0.5/T to 30/T. This sensitivity exceeds by an order of magnitude or more, than the previously reported values for comparable magnetotransistors It can be fabricated by standard CMOS technology. However, from previous report, this kind of magnetic field sensor is still not able to simulatanenously measure more than two components of the magnetic-flus-density vector B.

There are potential applications of three-dimensional magnetic field sensor as in most of the real case the magnetic field is not simply one-dimension. Here are some examples of possible 3-D magnetic filed sensor applications :

* Full magnetic vector measurements on magnetic materials and apparatus

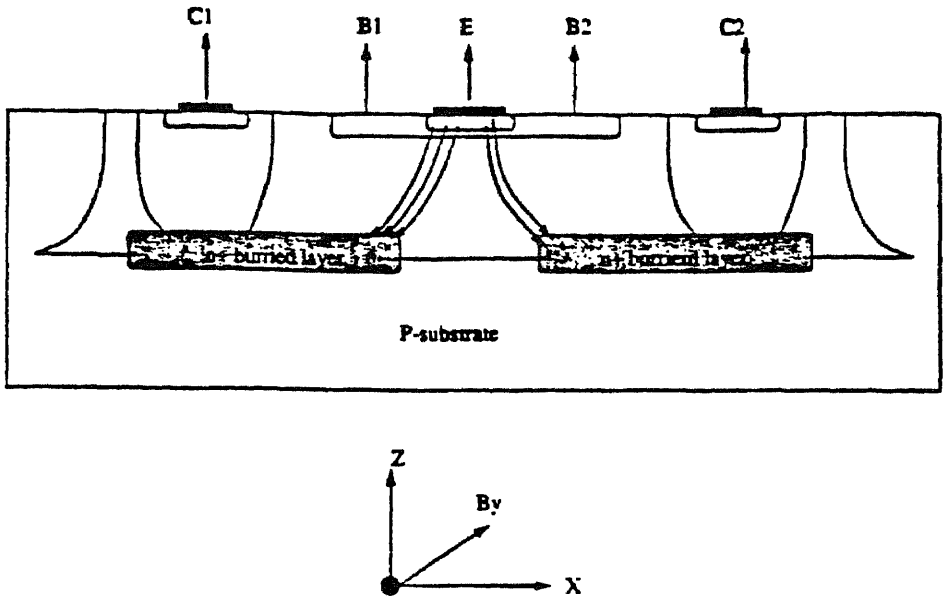



**Figure 1.2** Cross section of a vertical magnetotransistor

* Earth magnetic field measurements for navigational or geological purposes

* Proximity switches

* Contactless angular position encoders

Efforts are being made in developing the multi-dimensional magnetic field sensors which enable the detection of the three components of the magnetic field simultaneously. The first fully integrable 3-D magnetic field sensor was proposed by [13] in 1986, which was fabricated in standard bipolar technology. It combines an in-plane 2-D sensor with a lateral magnetotransistor. The device cannot eliminate the cross-sensitivity between x and z, or y and z direction because of the presence of the vertical component in the lateral magnetotransistor[14]. A 3-D vertical Hall magnetic field sensor has been reported recently[9]. The cross-sensitivity between x and z directions disappears, but the cross-sensitivity between x and y directions remains. In our previous work, a 3-D magnetic field sensor fabricated in standard CMOS

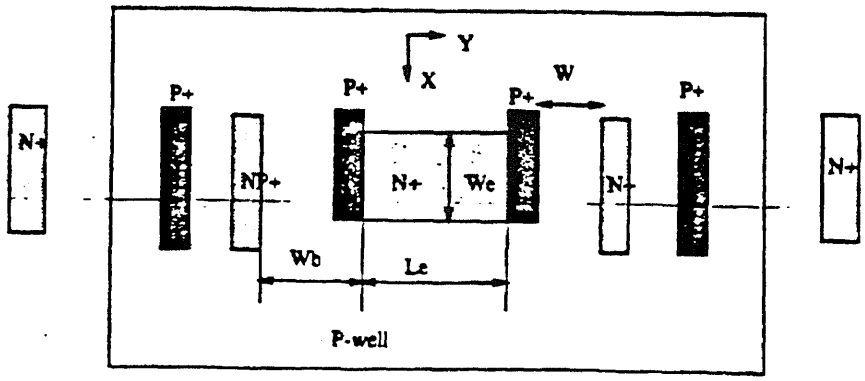



**Figure 1.3** Top view of a suppressed sidewall injection magnetotransistor

technology has been developed[15]. Although the sensitivity of z direction has been improved by the control of the base surface potential through the biasing of the gate terminal, the cross-sensitivity could not be eliminated completely. In designing a 3-D magnetic sensor, the basic approach is to combine different devices in different orientations on the same chip in a single technology[9],[13]-[16]. However, the 3-D integrable sensors are facing the challenge of implementing the compact sensing structures for all three components of magnetic field on a single plane with relatively lower or no cross-sensitivities.

In this thesis, a three dimensional magnetic field sensor is proposed, using the Stanford merged BiCMOS technology. The design of this BiCMOS 3-D sensor discussed in this work has the following advantages compared to previously reported 3-D magnetic field sensors[9],[13]-[16].

(1). By using the triple diffusion BiCMOS process, the sensor with the four collector vertical npn transistors together with split drain PMOS, as a

single device, is able to eliminate completely the cross-sensitivities which were inherent to the previously reported three dimensional magnetic field sensors in either CMOS or bipolar technology.

(2). The designed BiCMOS sensor can operate in the voltage scale from 0-5V with satisfactory output voltage swings. The device is compatible to the post processing circuits in the BiCMOS technology and can be connected directly without additional voltage transfer. For example, the sensor element can be easily integrated with the signal processing circuitry acting as "smart sensor" in a robotic arm for position detection in a magnetic environment.

(3). In this design, a merged structure from Stanford BiCMOS process is used to reduce the chip area . The advantage of area and number of contacts will become more obvious when the sensing part is used as a building block of a large sensor processing system[17].

Although much effort has been expended in the development of sensors, proportionally less effort has been directed to make integrated arrays of sensors, especially in the multi-dimensional high frequency sensing systems. In this thesis, a development of a 3-D magnetic field sensor array is also presented. The above mentioned 3-D merged BiCMOS magnetic field sensor is used as an individual cell in the processing array system. Such an array has many applications, for example, it can act as the compliant tactile sensor to measure the deformation of a membrane to which small magnetic dipoles are attached[3]. In many cases, the multi-dimensional high frequency response sensing systems can meet the requirements of mapping a quickly varying field. This kind of 3-D magnetic field sensor system can be used in precise manufacturing as a position sensor in a robotic arm in a magnetic source environment which requires that the sensor system not only be capable of detecting absolute positions but also detecting very rapid position changes.

Another useful application is the high frequency contactless switching. We often need a tactile sensor which can sample a quickly changing magnetic field. Of course the sensor array can be also used in the general application like determining the fringing fields in an electric motor.

In the following chapters, details about device working principles, design considerations, device and circuit simulations and some test results are presented.

Chapter 2 gives a review of integrated semiconductor magnetic field sensors, describing the physical mechanism basic to the action of the electrons and the main principles about sensitivity, resolution, and technology in typical magnetic field sensors.

Chapter 3 describes the novel 3-D magnetic field sensor designed in Stanford BiCMOS technology with and without the merged structure. The sensors is designed together with output processing circuitry. Design consideration, layouts, PISCES and SPICE simulation and test results are presented.

Chapter 4 gives the design of the 3-D magnetic field array system. The principle of the processing system and optimization through simulation are presented.

Finally the summary and conclusion are provided in chapter 5.

All the computer simulation input data and device layouts for fabrication are presented in Appendix.

# CHAPTER 2

# PRINCEPLES AND OF INTEGRATED MAGNETIC FIELD SENSORS AND REVIEW OF PREVIOUS WORK

## 2.1 Galvanomagnetic Effects in Semiconductors

Most MFSs exploit the Lorentz force $\vec{F} = q\vec{V} \times \vec{B}$ on electrons in a metal, a semiconductor, or an insulator in one way or another, where $q$ denotes the electron charge, $\vec{V}$ the electron velocity, and $\vec{B}$ the magnetic induction. A simple example is shown in Figure 2.1.

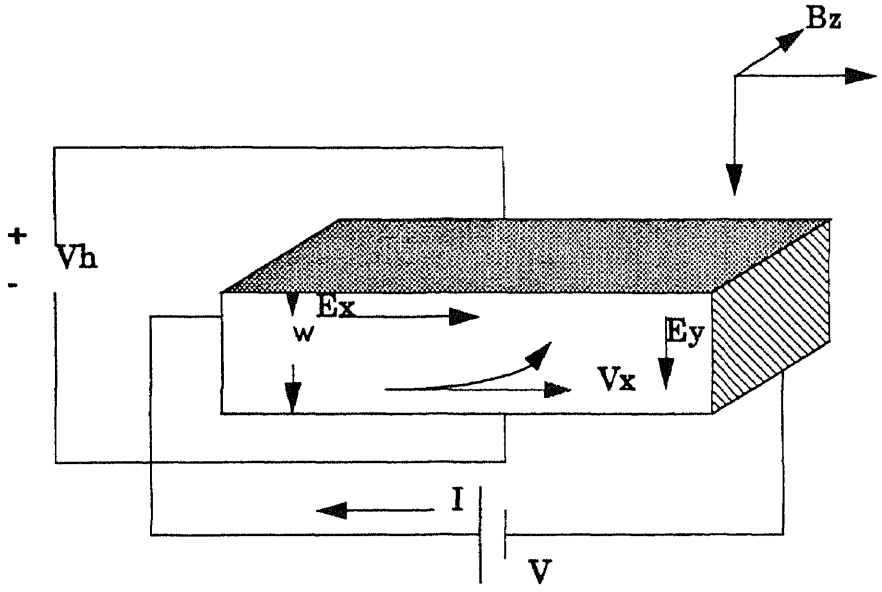



**Figure 2.1** Example of Hall effect

As mentioned in Chapter 1, semiconductor MFSs exploit the galvanomagnetic effects such as Hall voltage, carrier deflection, magnetoresistance and magnetoconcentration, which are due to the action of the Lorentz force on the charge carriers (electrons and holes). In n-type semiconductor material, for instance, the magnitude of the sensor effect is controlled by the product of the electron mobility and the magnetic induction.

Hence high electron mobility is crucial for achieving high sensitivity. Thus n-type material is superior to p-type material because of mobility.

The action of the Lorentz force manifests itself in the carrier-transport equations. We assume isotropic n-type material with zero temperature gradient. Let us denote the electron current density for $\vec{B} = 0$ by $\vec{J}_{n(0)}$ The diffusion approximation of the Boltzman transport equation leads to

$$\vec{J}_n = \sigma_n \vec{E} + (qD_n \vec{\nabla} n) \tag{2.2}$$

where $\sigma_n = q\mu n$ denotes the electronic conductivity for $\vec{B} = 0$, $\vec{E}$ the electrical field, $D_n = \mu\kappa(T/q)$ the electron diffusion constant, n the electron density, and $\mu$the electron drift mobility. In (2.1) the term $\sigma_n \vec{E}$ describes the drift current and $qD_n \vec{\nabla} n$ the diffusion current. For nonzero magnetic induction $\vec{B}$, the electron current density $\vec{J}_n(B)$ obeys the equation

$$\vec{J}_n(\vec{B}) = \vec{J}(0) - \mu_n^* (\bar{J}(\vec{B}))$$

Where $\mu_n^*$ is the Hall mobility for electrons. Equation (2.2) can be solved with respect to $\bar{J}(\vec{B})$ viz.

$$\bar{J}(\vec{B}) = [\vec{J}_n(0) + \mu_n^* \vec{B} \times (\vec{B} \bullet \vec{J}(0)\vec{B})] \left[1 + (\mu_n^* \vec{B})^2\right]^{-1} \tag{2.3}$$

This equation comprises the isothermal galvanomagnetic effects for electrons. It accounts for the direct effects of temperature on carrier concentration, diffusion, and mobility, but does not include thermomagnetic or thermoelectric effects. An analogous equation holds for the hole current density. In general, the electron and hole current equations have to be solved together with the pertinent continuity equations for electrons and holes as well as Poisson's equation.In specific configurations characterized by the device geometry, doping, and boundary and operation conditions, the one or

the other galvanomagnetic effect may prevail.

Equation (2.3) induces the action of the Lorentz force on both carrier drift (terms containing $\vec{E}$) and diffusion (terms containing $\vec{\nabla} n$). Diffusion is important in the case of magnetoconcentration or space-charge effects occurring, e.g., in magnetodiodes (injection of both electrons and holes). If carrier concentration gradients can be neglected, as,e.g.,in n-type slabs with ohmic contacts,(2.3) becomes

$$\vec{J}_n(\vec{B}) = \sigma_{nB}[\vec{E} + \mu_n^*(\vec{B} \times (\vec{B} \bullet \vec{E})\vec{B})] \tag{2.4}$$

where $\sigma_{nB} = \sigma_n\left[1 + (\mu_n^* \vec{B})^2\right]^{-1}$. If $\vec{B}$ is parallel to $\vec{E}$, $\vec{B} \times \vec{E} = 0$ leads to $\vec{J}_n(\vec{B}) = \sigma_{nB}\vec{E} = \vec{J}_n(0)$: this means that no longitudinal galvanomagnetic field effect is observed in isotropic semiconductors. For $\vec{B}$ normal to $\vec{E}$, $\vec{B} \bullet \vec{E} = 0$, we obtain

$$\vec{J}_n(\vec{B}) = \sigma_{nB}[\vec{E} + \mu_n^* \vec{B} \times \vec{E}] \tag{2.5}$$

This equation describes the transverse galvanomagnetic effects in the case of negligible diffusion. In terms of $\vec{B} = (0, 0, B)$, $\vec{E} = (E_x, E_y, 0)$ and $\vec{J}_n(\vec{B}) = (J_{nx}, J_{ny}, 0)$, (2.5) becomes

$$J_{nx} = \sigma_{nB}(E_x - \mu_n^* B E_y) \;\&\; J_{ny} = \sigma_{nB}(E_y + \mu_n^* B E_x) \tag{2.6}$$

Two limiting cases are usually distinguished:

1) Hall field:

It is assumed that the current density has only an x-component, i.e., $J_{ny} = 0$. This can be achieved approximately in a long, thin rod sample geometry with current electrodes at the small faces. Then the Hall field

$$E_y = -\mu_n^* B E_x = R_H J_{nx} B \tag{2.7}$$

Where

$$R_H = -\mu_n^*/\sigma_n = -\gamma_n/(qn) \tag{2.8}$$

denotes the Hall coefficient. this results in a rotation of the equipotential lines by the Hall angle $\theta_H$ with

$$\tan\theta_H = E_y/E_x = -\mu_n^* B = \sigma_n R_H B \tag{2.9}$$

For a long Hall plate of thickness t carrying a current I, the Hall field produces the Hall voltage $V_H = R_H/t$. The corresponding Hall sensor has the sensitivity $V_H/(IB) = R_H/t = \gamma_n/(qnt)$. Thus high sensitivity requires small carrier concentration n. This explains why semiconductors are more useful here than metals.

2) Carrier deflection:

Now zero Hall field, $E_y = 0$, is assumed. This condition can be realized approximately by a short sample of wide cross section with current electrodes at the large faces. The carrier deflection resulting is given by the ratio

$$-J_{ny}/J_{nx} = \mu_n^* B = \tan\theta_H \tag{2.10}$$

## 2.2 Design Consideration

Although different applications of magnetic field sensor has different considerations which may emphasize one or two requirements, there are some general design criteria which should be take into account when designing a magnetic field sensor.

First of all, we must consider the availability of technology. Such as standard Bipolar, NMOS, CMOS, and BiCMOS technology. Second, we need to think over total manufacturing cost, which should be as low as possible. Then the environment to which sensor is exposed should also be taken into consideration. This includes temperature, humidity and chemical stress,

mechanical stress, vibrations, etc. These conditions will influence the sensor performance.

As to the properties of magnetic field sensor, we should consider the following aspects:

* Sensor geometry (H parallel or perpendicular to chip surface)
* Sensitivity (absolute sensitivity and relative sensitivity)
* Magnetic field resolution signal to noise ratio)
* Spatial resolution (device geometry size)
* Linearity (response to magnetic field)
* Time resolution (frequency response)
* Offset, temperature dependance of offset
* Power consumption
* Stability, reliability, lifetime

## 2.3 Split-Drain MAGFET

Split-Drain MAGFET is a MOSFET with two or three adjacent drain regions which share the drain current. A magnetic field perpendicular to the chip surface can cause defection of the current lines in the channel region. By operating the MOSFET in the 'pinch-off' mode ($V_{DS} > V_{GS} - V_T$) the output impedance is made very high, so that large output voltage swings may be obtained. Beyond the 'pinchoff region', the depletion layers formed between drains and channel would prevent voltage changes on the drains from affecting the channel voltages. Since the MOS transistor works as current source, the output impedance would therefore be high and so the device would be capable of producing high output voltages under suitable load conditions. Moreover, this bias condition also ensure that the lateral parasitic npn bipolar

formed by two split drains and substrate operates in the cut-off mode [10].

The first magnetic-field sensitive MOS device was the MOS element proposed by Gallagher and Corak [25]. About $10^3 V/(AT)$ sensitivity can be achieved in this way. The split-drain MOS transistor configuration as proposed by Fry and Hoey [25] shows a much higher sensitivity, viz. about $10^4 V/(AT)$, provided load resistors well within magaohm range are applied. The structure of a split-drain MAGFET is shown in Figure 1.1. The separation of the two drains are determined by the minimum spacing of technology. Each drain is L-shaped to provide more drain area, which helps to shape the surface potential for better collection of deflected electrons. The width at the middle of the channel is taken as the minimum width of the device. The length is taken to be the minimum distance covered by the carriers in traveling from the source to the drain [10].

## 2.4 Dual-Collector Magnetotransistor

Dual-collector Magnetotransistor is a bipolar transistor whose design and operating conditions are optimized with respect to magnetic field sensitivity of the collector current $I_c$. Because of the geometrical symmetry, the two collector current should be equal without magnetic field. However, when we apply magnetic field in a particular direction, the current flow will deflect and cause more current in one collector and less current in the other. The first magnetotransistor was proposed by Hudson [6] in 1968. The relative sensitivity was about $0.05T^{-1}$. This is the vertical two-collector bipolar transistor, where the magnetic field causes an imbalance in the two collector currents. A lateral magnetotransistor was first described by Davies and Wells [7]. This device was essentially a merged combination of planar Hall plate and

a lateral two-collector transistor. The relative sensitivity was about $0.5T^{-1}$. A vertical magnetotransistor and a lateral magnetotransistor are shown in Figure 2.2 and Figure 2.3.respectively

The sensitivity of a vertical 1-D magnetotransistor can be calculated from Figure 2.4. The path of the total collector current $I_c$ is shifted over a distance $\Delta y$ under the influence of the lateral magnetic field $B_x$. the shift $\Delta y$ depend on the Hall angle $\theta_H$

$$\tan\theta_H = \mu_H B_x \tag{2.11}$$

Hall mobility of the material $\mu_H$, and the distance L' over which the

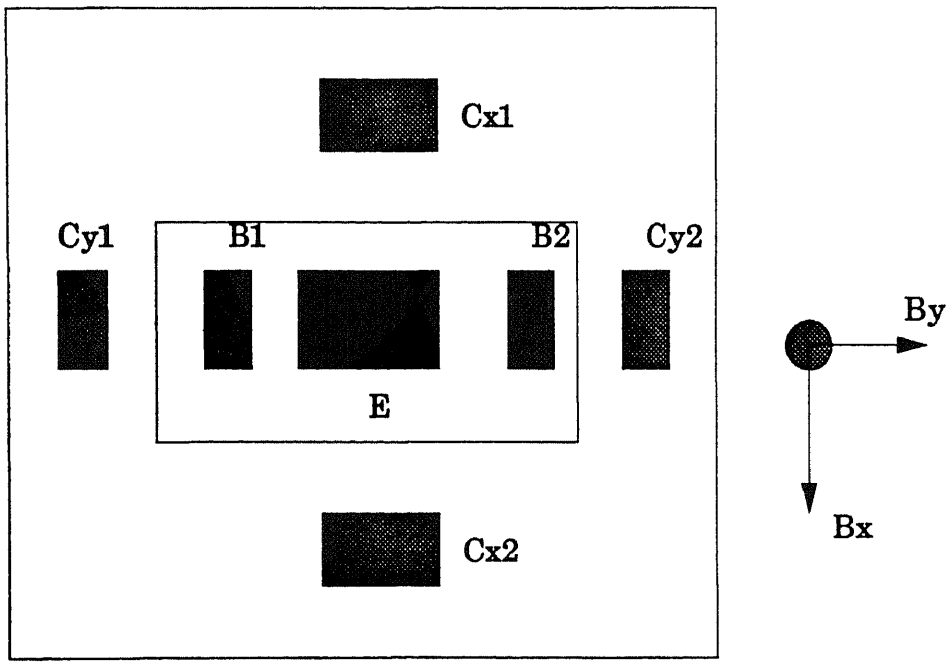



**Figure 2.2** Top view of a vertical magnetotrasistor

deflection takes place. L' is smaller than the thickness of the epitaxial layer because of the presence of the buried layers, emitter and base diffusions, depletion layers, and current spreading. The shift $\Delta y$ becomes

$$\Delta y = L' \tan\theta_H \tag{2.12}$$

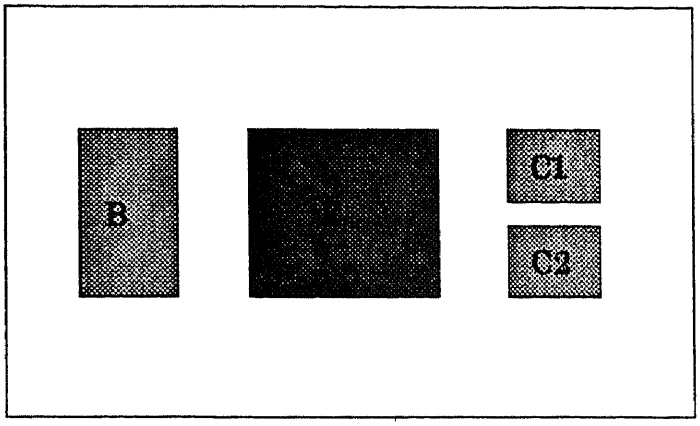



**Figure 2.3** Top view of a lateral magnetotrasistor

$$\Delta y = L'\mu_H B_x \tag{2.13}$$

We assume that current to the left of the central line between the buried layers is collected be collector $C_x$, while the current to the right is collected by collector $C'_x$. Because of the shift, currents $I_x$ in collector$C_x$ and $I'_x$in the collector $C'_x$are unequal.

$$I_x = (\frac{1}{2} + \frac{\Delta y}{W_e}) I_c \tag{2.14}$$

$$I'_x = (\frac{1}{2} - \frac{\Delta y}{W_e}) I_c \tag{2.15}$$

$W_e$ is the emitter width. The output signal $\Delta I_x = I_x - I'_x$, which is the current difference between the two collectors, becomes

$$\Delta I_x = 2I_c (\frac{\Delta y}{W_e}) \tag{2.16}$$

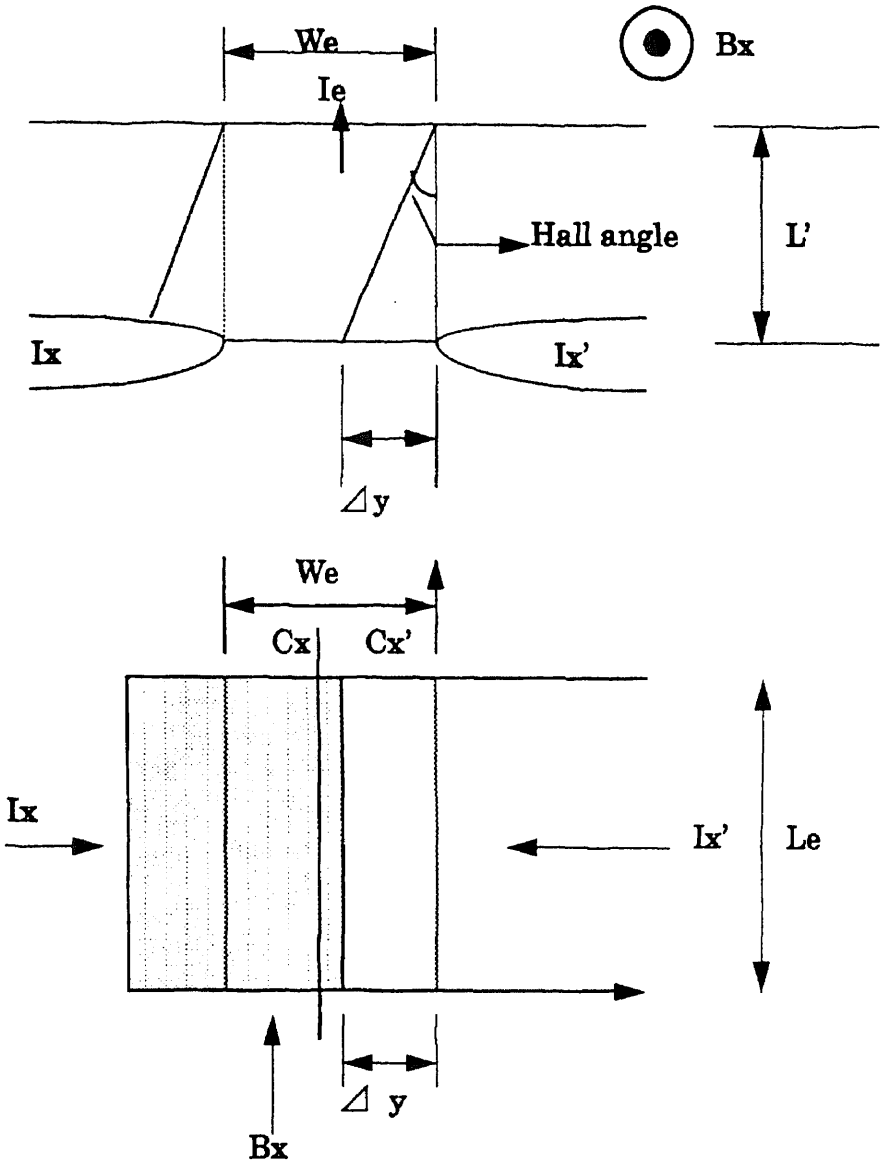



**Figure 2.4** One-dimensional sensor-Magnetic-flux density Bx cause a shift in the collector profile

With (2.13) the output signal can be written as

$$\Delta I_x = 2I_c \mu_H B_x \left(\frac{L'}{W_e}\right) \tag{2.17}$$

In the case of a 2-D in-plan sensor Figure 2.4, the sensitivity can be

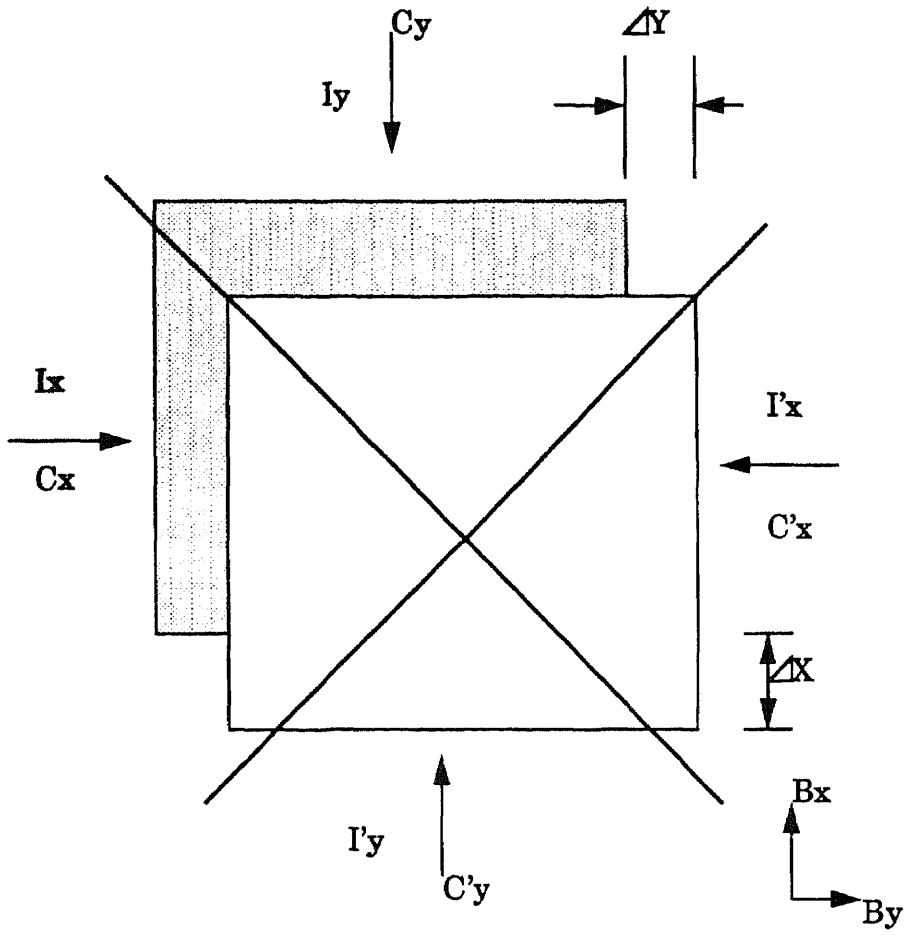



**Figure 2.5** Current shift in a 2-D sensor. Bx and By will shift the injected current profile respectively

calculated similarly. From Figure 2.5 we can see that the in-plane field components $B_x$ and $B_y$ cause a shift in the current by $\Delta y$ and $\Delta x$

$$I_x = I_c\left(\frac{1}{4} + \frac{\Delta y}{W_e} - \frac{\Delta x \Delta y}{W_e^2} + \frac{\Delta y^2}{2W_e^2} - \frac{\Delta x^2}{2W_e^2}\right) \tag{2.18}$$

$$I'_x = I_c\left(\frac{1}{4} + (-\frac{\Delta y}{W_e}) + \frac{\Delta x \Delta y}{W_e^2} + \frac{\Delta y^2}{2W_e^2} - \frac{\Delta x^2}{2W_e^2}\right) \tag{2.19}$$

The output signal $\Delta I_x = I_x - I'_x$ of the x channel is

$$\Delta I_x = 2I_c\left( (\frac{L'}{W_e})\,\mu_H B_x - \left(\frac{L'\mu_H}{W_e}\right)^2 B_x B_y \right) \tag{2.20}$$

Currents $I_y$ and $I'_y$ in the channel can be calculated in a similar manner, and the output signal $\Delta I_y$ of the y-collector pair is

$$\Delta I_y = I_c\left(\frac{2L'\mu_H B_y}{W_e} - \left(\frac{L'\mu_H B_y}{W_e}\right)^2 - \left(\frac{L'\mu_H B_x}{W_e}\right)^2\right) \tag{2.21}$$

The output signals of the 2-D sensor can be writer for $|B_y| \geq |B_x|$ as

$$\Delta I_x = 2I_c\left(\frac{L'\mu_H B_x}{W_e}\right)\left(1 - \frac{L'\mu_H |B_y|}{W_e}\right) \tag{2.22a}$$

$$\Delta I_y = 2I_c\left(\frac{L'\mu_H B_y}{W_e}\right)\left(1 - \left(\frac{L'\mu_H B_x^2}{2W_e|B_y|}\right) - \left(\frac{L'\mu_H B_x^2}{2W_e|B_y|}\right)\right) \tag{2.22b}$$

The difference in the form of these equations is caused by the square shape of the current profile. We can see from (13) that both output signals are nonlinear and that they are also dependent on both in-plane field components. In the case of the device used in the experiments with $W_e = 20\mu m$, $\mu_H = 0.114\,(m^2/Vs)$, and L' smaller than $8\mu m$, for magnetic-flux-density values lower than 1T, the contribution of the second-order terms is a factor of 20 lower compared to the first-order terms. Under the above conditions (2.24) can be reduced to

$$\Delta I_x = 2I_c\left(\frac{L'\mu_H B_x}{W_e}\right) \tag{2.23a}$$

$$\Delta I_y = 2I_c\left(L'\mu_H \frac{B_y}{W_e}\right) \tag{2.23b}$$

## 2.5 3-D MT Based on Bipolar Technology

### 2.5.1 Device Structure and Operation

We have discussed 1-D and 2-D magnetic field sensors in the previous sections. As in most of the real case, we need to measure the 3-D magnetic field. This can be performed by successively changing the orientation of the one-dimensional sensor and measuring the field component. A simultaneous measurement of all three field components can be achieved by attaching three 1-D sensors to the orthogonal faces of a cube. The spatial resolution of a measurement would not be satisfactory in this case it highly divergent fields were to be measured, nor is the sensor integrable.

A recent report [26] shows that a 3-D magnetic sensor has been designed and fabricated by standard Bipolar technology. As the current flow in a 2-D in-plane magnetotransistor is not completely vertical; there are also significant lateral components of the total current in the n epitaxial collector region. Just as in the case of lateral magnetotransistors, the lateral component of the total collector current can be deflected by $B_z$, and this can be used in sensing the last field component. Figure 2.6 shows the structure of the 3-D magnetotransistor.

### 2.5.2 Sensitivity of the 3-D Magnetotransistor

In general, the output signal of the sensor can be written as

$$\begin{bmatrix} \Delta I_x \\ \Delta I_y \\ \Delta I_z \end{bmatrix} = S \begin{bmatrix} B_x \\ B_y \\ B_z \end{bmatrix} \tag{2.24}$$

Where $\Delta I_i$ (i=x,y or z) is the collector-current difference of the

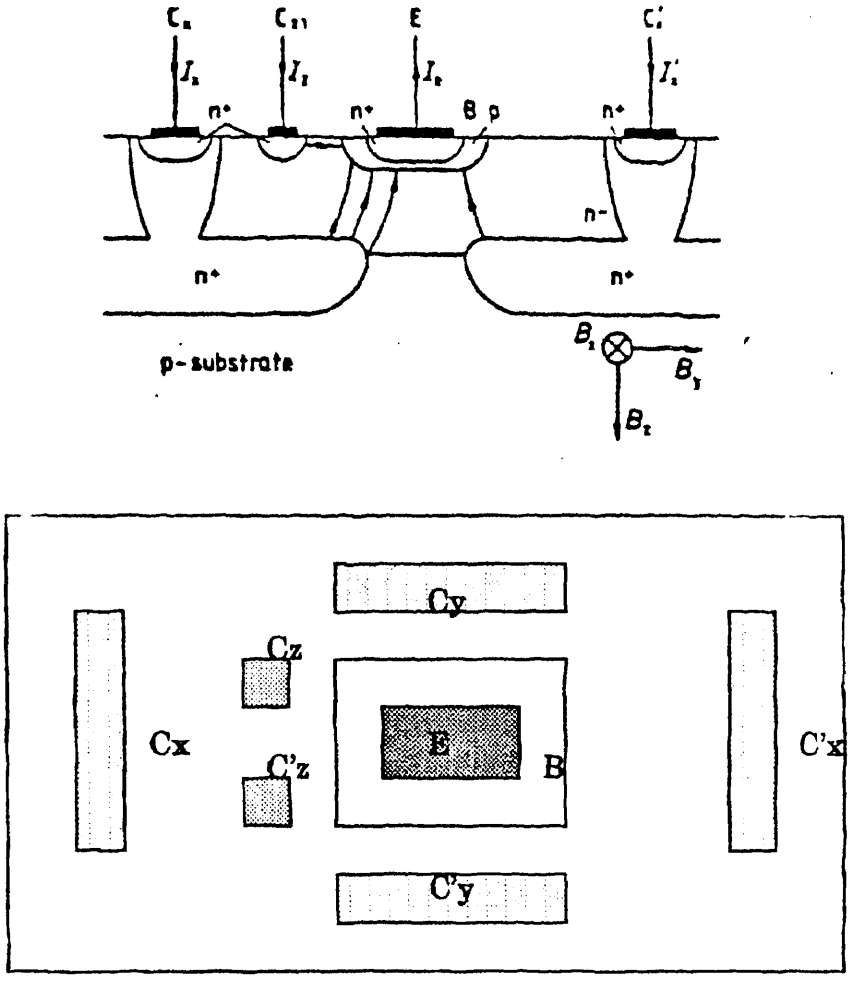



**Figure 2.6** By merging a 2-D in-plane sensor with a 1-D lateral device, a sensor is obtained that is sensitive to all three components of the magnetic field vector

associated channel. S is a $3 \times 3$ sensitivity matrix, which is not necessarily a diagonal matrix because the output signal $\Delta I_i$ of the channel i will not only depend on the field component$B_i$, but also on the other two components. The sensitivity matrix of the structure shown in Figure 2.6 with one z-collector pair is

$$S = \begin{bmatrix} S_{xx} & 0 & 0 \\ 0 & S_{yy} & 0 \\ 0 & S_{xy} & S_{zz} \end{bmatrix} \tag{2.25}$$

The measurements are presented in Figure 2.7

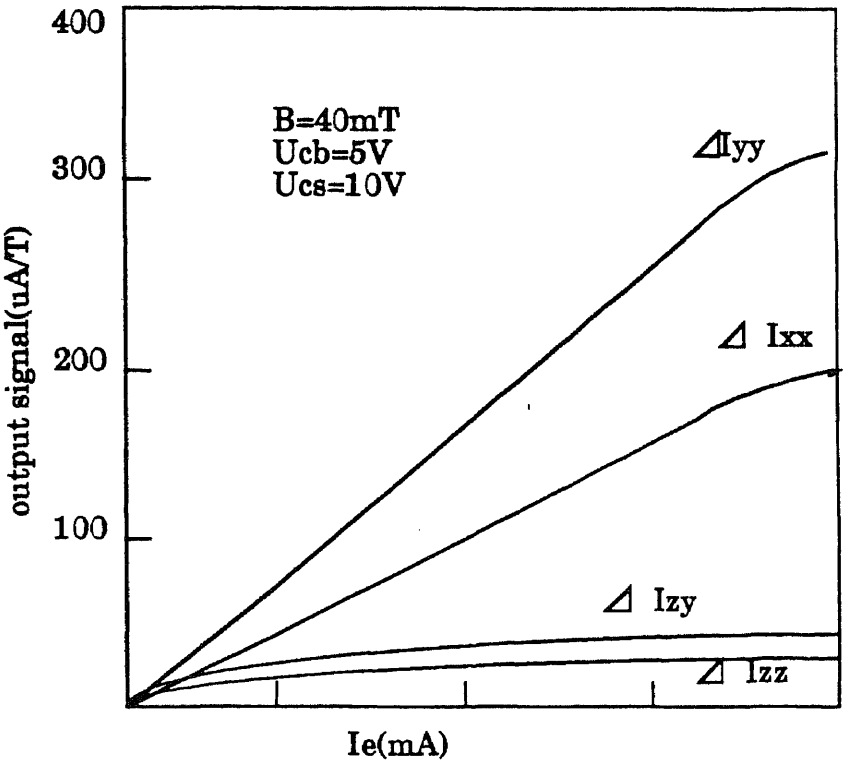



**Figure 2.7** The response of different sensor channels to a magnetic filed as a function of the emitter current.

## 2.6 3-D Magnetotransistor in CMOS Technology

The realization of a 3-D Magnetotransistor in CMOS technology has been accomplished by Ms. Zhang in our Sensor Lab. The device was fabricated in standard 2um CMOS technology. The operation description and test results are given below.

### 2.6.1 Device Structure and Operation

Use of bipolar devices that are reliable with existing CMOS technologies is inexpensive and has wider applications. One possibility is the vertical transistor where the substrate is used as the collector and a separate well as the base. A lateral bipolar transistor can also be formed in the base region. In

this section, we first describe the device structure and then analyses its operation.

The structure of the new 3-D magnetic field sensor is shown in Figure 2.8. It is basically similar to the conventional 3-D magnetotransistor which has been discussed in last section. The device is situated in a p-well, serving

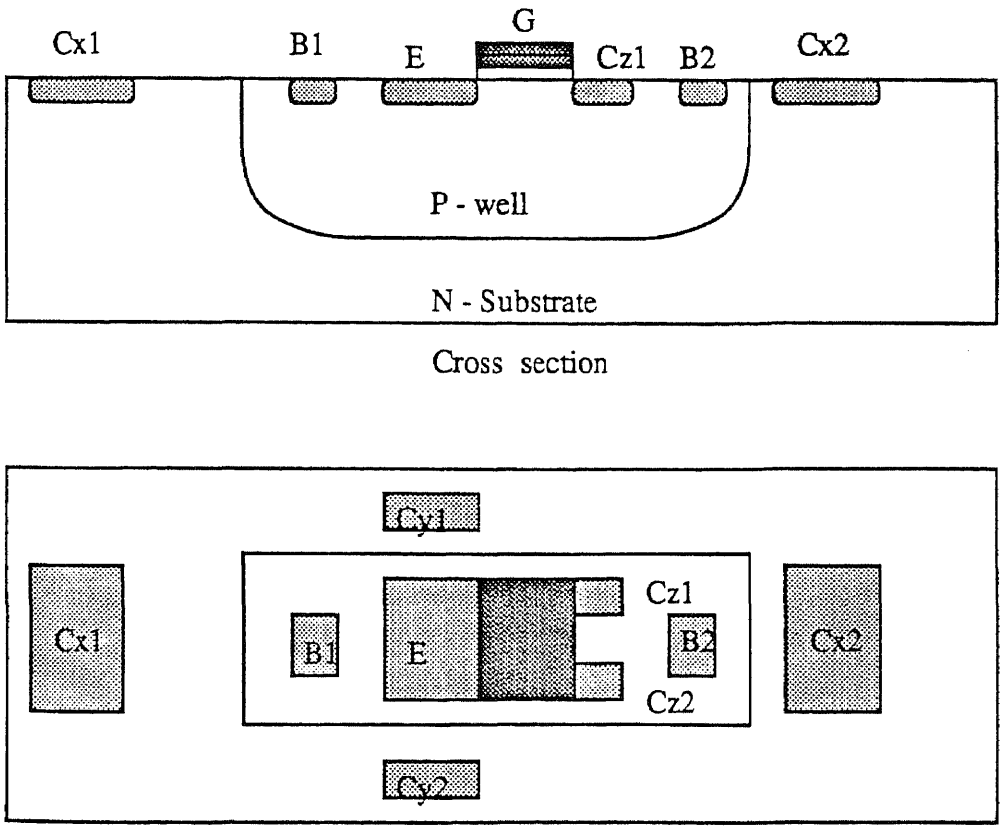



**Figure 2.8** Device structure of 3-D magnetotransistor in CMOS technology

as the base region of the transistor. The substrate serves as collector for the two vertical npn transistors and another lateral bipolar transistor with two-

collector pair is formed within the base region. The two vertical magnetotransistor are sensitive to the 2 in-plane magnetic field and the lateral magnetotransistor can measure the magnetic field perpendicular to the chip surface.

However, there are two changes in this new device compared with traditional magnetotransistor. First, two base contacts, $B_1$ and $B_2$ are used. This allows the application distribution of collector current. For example, if the device is ideally in geometrical symmetry, each collector current should be equal to corresponding collector pair. However, because the fabrication process may cause asymmetry in device structure which will cause current imbalance even without magnetic field. By applying two slight different voltages to$B_1$ and $B_2$, the imbalance can be dispelled. From Figure 2.8, it is evidenced that additional Z-collector pair partakes of the X- collector current. Adjusting the two base voltages will provide a reasonable distribution of those collector currents.

Second, the device is also similar to a MOS transistor as the base region is covered by the thin oxide and polysilicon gate layers. This was done for two reasons. First, it makes the device fully compatible with a standard CMOS process, so that the emitter and collector can be fabricated as the source and drain of the NMOS transistor, respectively. Second, the gate makes it possible to control the base surface potential. This feature is important for both sensitivity and noise performance of the device. For example, when a magnetic field perpendicularly to the device plane is applied, the electron flux lines are deflected toward the device surface. The two lateral collector currents will be reduced a little because of the recombination at the silicon-oxide interface. The MOS structure on top of the base region serves to reduce this recombination. Application of a negative voltage to the gate repels the

minority carriers away from interface. As recently demonstrated by Vittoz [6].

To consider the operation, let us assume that the device is biased adequately for the forward active operation, that is the emitter-base junction is forward biased, both collector-base junctions are reverse-biased. Electrons are injected into the base region laterally and vertically and are collected by corresponding collectors.If we apply a magnetic field $\vec{B}_x$or $\vec{B}_y$, it will cause a change in the two vertical collector pairs due to the deflection of the electron paths. When the field is directed perpendicular to the Figure plane, the Lorentz force on charge carriers will cause an imbalance of collector current in the Z-collector pair.

In the long base region device, because p-well with depth about $5\mu m$ is used as base region, we must consider the Lorentz force on minority carriers (electrons) as well as that on majority carriers. It is known that the Hall field generated by deflected electrons in silicon is in an opposite direction of the Hall field generated by holes. Therefore, the majority carriers (holes) cancel the Hall field that the minority carrier (electrons) flow would produce, in the same way as they cancel any other space-charge effect. Thus sensitivity can be increased by using minority-carrier deflection in the long-base region. The deflection efficiency is not linked to the device geometry, biasing condition is more related with the device sensitivity. Evidently, this kind of 3-D magnetic field sensor has better performance than those 3-D magnetotransistors discussed previously.

# CHAPTER 3

# THREE DIMENSIONS MAGNETIC FIELD SENSOR BASED ON BICMOS TECHNOLOGY

In this chapter, different 3-D MFSs are designed in Stanford BiCMOS technology. The 3-D sensor using merged structure with voltage output circuits is discussed. The device simulations for both non-merged MFS and merged MFS are presented. The SPICE simulation and the test results are also given.

## 3.1 Introduction of BiCMOS Technology

### 3.1.1 BiCMOS Technology

In recent years there has been strong interests in BiCMOS. In the past, however, the cost of more complex process, has restricted such technologies to rather specialized applications. In modern technologies both bipolar and CMOS have shown very similar complexity. By using BiCMOS technology, we can exploit the performance advantages of bipolar and CMOS and at the same time use the higher yield capability of MOS.

Table 1 lists some important properties of bipolar and CMOS transistors in circuits

From table 1 it can be deduced that generally for devices bipolar is in an advantageous position for analog applications because of the better gain and low wideband noise. CMOS obviously is more attractive for digital control and data processing functions because of its low quiescent power, good speed and generally good packing density. The mixture of bipolar and MOS offers unique advantages, however, in both the analog and the digital fields. It features for instance, high-impedance zero dc gate current, high gain

**Table 1** Comparison of Bipolar and CMOS

| strengths of Bipolar and CMOS | |
|---|---|
| Bipolar | CMOS |
| Large transconductance | high impedance |
| exponential characteristics | near quaqratic |
| low voltage offset | zero DC dissipation |
| low supply voltage | low narrow band noise |
| low 1/f noise | high slew rate |
| fast | no second breakdown |
| low logic swing | self isolating |
| good capacitor drive capability | no avalanche breakdown reductionCom- |
| no hot electron limit | parision of Bipolar and CMOS |

operational opamps, switch capacitor filters and gyrators. Futhermore, precision pairs in mixed AD and DA systems in the field of analog applications are possible. In digital applications mixed sense-amplifiers and buffers can significantly increase the capability of CMOS with regards to speed and compactness.

In the context of electronic advantages it should be noted that some problems can also occur. Because bipolar transistors can inject into the substrate one has to take measures to prevent latch-up. Futhermore CMOS logic generates considerable transient noise which must be prevented from entering into an adjacent sensitive analog part. Both problems can effectively suppressed by proper measure.

### 3.1.2 Overview of the Stanford BiCMOS Process

Stanford BiCMOS process is using a $2\mu m$ technology. A number of key features include:

* A single level of polysilicon is used for emitter contacts, base contacts, collector contacts, n- and p-channel gates, and n- and p-channel source/drain contact regions. This allows us to produce high performance polysilicon emitter bipolar transistors coupled with dense, low capacitance contacts to all regions.

* N+ doped poly is used for emitter contacts, collector contacts, n-channel source/drain contacts, and n-channel gates.

* P+ doped poly is used for base contacts, p-channel source/drain contacts, and p-channel gate regions. In particular, this avoids problems associated with buried channel p-channel devices which are frequently encountered when n+ polysilicon is used as the gate material for p-channel devices.

* selective tungsten is used as a strapping layer on top of all polysilicon regions in order to provide a low sheet resistance ( $R < 2\,(\Omega/\,(square))$ ) local interconnect layer and to short out any possible n+/p+ diodes occurring in the polysilicon layer.

* Local oxidation is used to pattern most of the polysilicon regions. In particular, this results in an exceedingly planar surface after all polysilicon processing. This, in turn, greatly eases the task of adding two levels of metallization to this structure. Furthermore, the local oxidation of poly enables us to produce overlapping contact holes (i.e., non-dog-bond poly) between first metal and underlying polysilicon structures further increasing the packing density of this technology.

Figure 3.1 shows a completed cross-section of the vertical NPN

transistor and the NMOS transistor that result from the Stanford BiCMOS process.

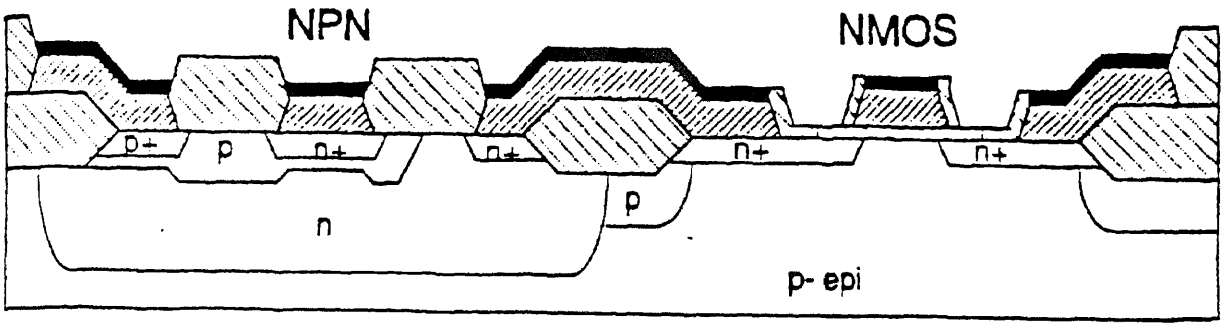



**Figure 3.1** Cross-section of the NPN transistor and the NMOS transistor

**Mask Level of Stanford BiCMOS Process**

Starting material is p-type <100> boron dopped wafer with 100mm in diameter. It is a $2\mu m$ process.

Mask 1 : n-well mask

Mask 2 : collector mask

Mask 3 : active mask

Mask 4 : n-channel field implant mask

Mask 5 : p-channel threshold adjust implant mask

Mask 6 : n-channel threshold adjust implant mask

Mask 7 : active base implant mask

Mask 8 : buried contact mask

Mask 9 : poly oxidation mask

Mask 10: poly etch mask

Mask 11: N+ implant mask

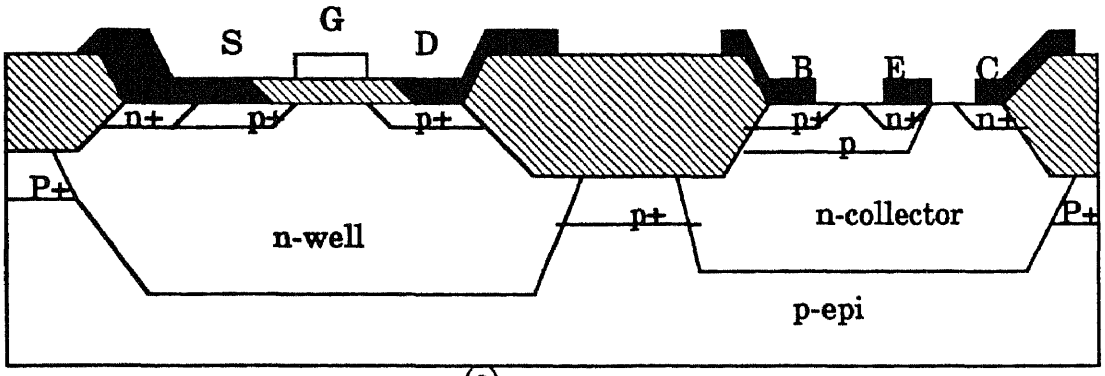
Mask 12: P+ implant mask

Mask 13: polysilicon resistor mask

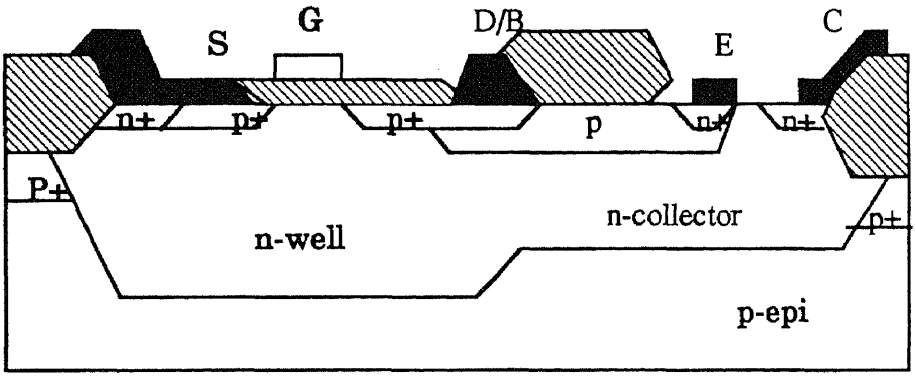
Mask 14: metallization mask, etc.

### 3.1.3 Merged Structure in BiCMOS Technology

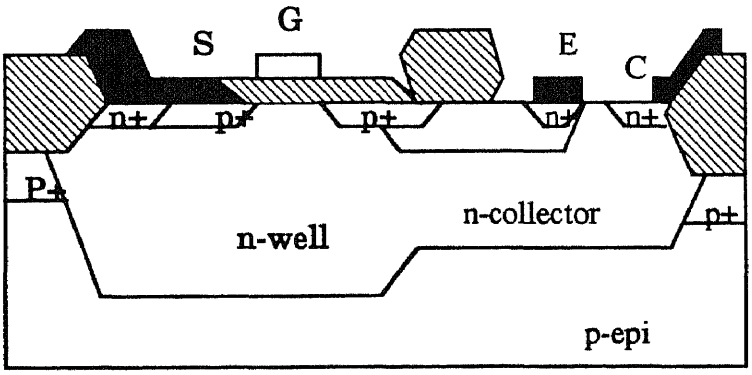
Key device and circuit parameters that require optimization in any application are device density, speed, reliability, and functionality at scaled supply voltages. The merged structure in BiCMOS process focuses on the issue of device density. In standard BiCMOS technology, the PMOS-NPN combination is built as shown in Figure 3.2. The PMOS FET and NPN transistor are built as seprate devices and the drain and base nodes are connected externally with a polysilicon or metal wire. In the merged structure, the external connection is removed and the devices are connected by merging the p-type base and drain in a common diffusion. Two types of merged structures have been built as shown in Figure 3.2. In the first (Figure 3.2b), the devices have been merged, but the contact to the base/drain region is preserved. This contact is often needed in circuit applications. The most compact merged structure is shown in the Figure 3.2c. In this case, there is no contact to the base/drain region. Gate to emitter spacing is determined by process design rules and the space required to isolate n+ and p+ diffusions. It has been demonstrated that the merged structure occupies 35% less area than the equivalent non-merged representations. In Stanford merged BiCMOS process, the layout constrains has been developed to allow latch-free design.




(a)




(b)




(c)

**Figure 3.2** Cross-sections of the various PMOS-NPN configurations

## 3.2 3-D Magnetic Field Sensor in Non-merged Stanford BiCMOS Technology

The 3-D MFS combines magnetotransistor together with MAGFET on a single chip. This combination has great advantages for improving the sensitivity of 3-D magnetic field sensor. The design can eliminate cross-sensitivities completely by using a MAGFET to measure a magnetic field perpendicular to the chip surface instead of the lateral magnetotransistor. The test results of a designed device is presented.

### 3.2.1 Device Structure and Simulation Results

Figure 3.3 shows the top view of the BiCMOS magnetic field sensor. Two dual-collector NPN transistors are used to measure the 2 in-plane magnetic field and one NMOS MAGFET can be sensitive to the third direction. The operation of each kind of sensor is similar to what we have discussed in chapter 2 relevantly.

### 3.2.2 Layout Design and Experimental Results

Mask design of this 3-D magnetic field sensor has been done by MAGIC version 6.3 using Stanford $2\mu m$ n-well BiCMOS technology file. Figure 3.4 shows the final layout.

The device has been fabricated in Stanford BiCMOS process by the Integrated Circuits Lab of Stanford University. The Gummel Plots is shown in Figure 3.5. Figure 3.6 shows the measured current changes in the three terminals of the BiCMOS sensor as a function of the applied magnetic field up to 1000 Gauss. The sensor response is basically linear for the range of the field used in this experiment. Because the operating current for the magnetotransistor is greater than that of the MAGFET, we use the relative

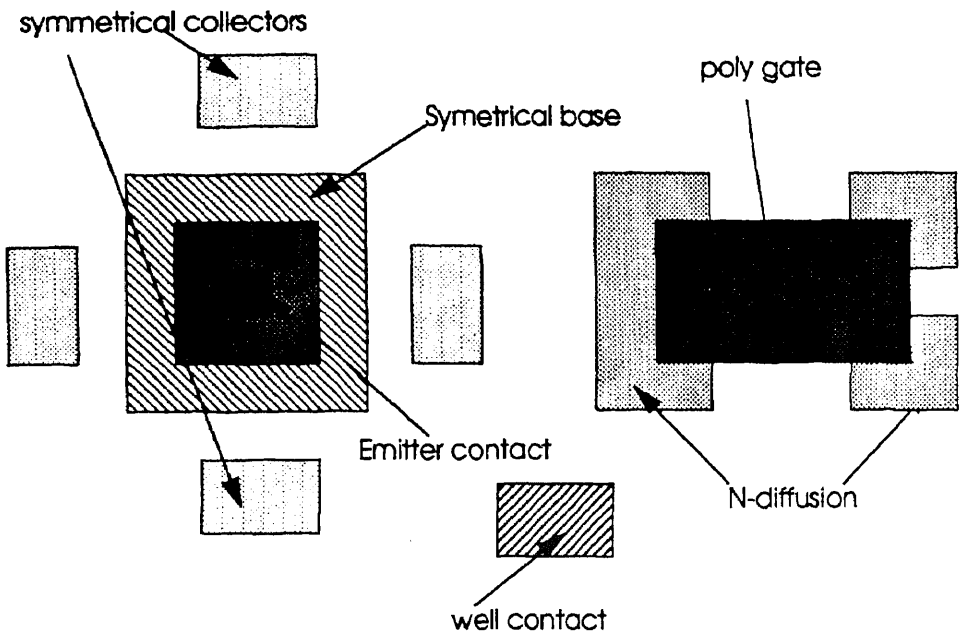



**Figure 3.3** Top View of Non-merged BiCMOS 3-D MFS

sensitivities, calculated from $S_{ri} = -\left(\frac{\partial I_i}{\partial B_i}\right)/I_i$[22] with $I_i$ indicating the bias current for the different direction($i = X, Y, Z$), to evaluate sensitivities of the device in three dimensions. Results show the relative sensitivity in X and Y direction are identified and of $7.3 \times 10^{-7}/G$ whereas in Z direction it is $2.8 \times 10^{-6}/G$.Figure 3.7 shows the photomicrography of the tested chip.

No cross-sensitivity between any two different directions has been found. This is because the n-MOS device and npn transistor are completely isolated in the substrate by p+ isolation between the n-channel MOS device and npn bipolar transistor [20] which was instrumental in eliminating the cross-sensitivity. The disadvantage of this design is that the sensor is not a compact structure. The 3-D sensor with merged structure which is more compact is discussed in the following section.

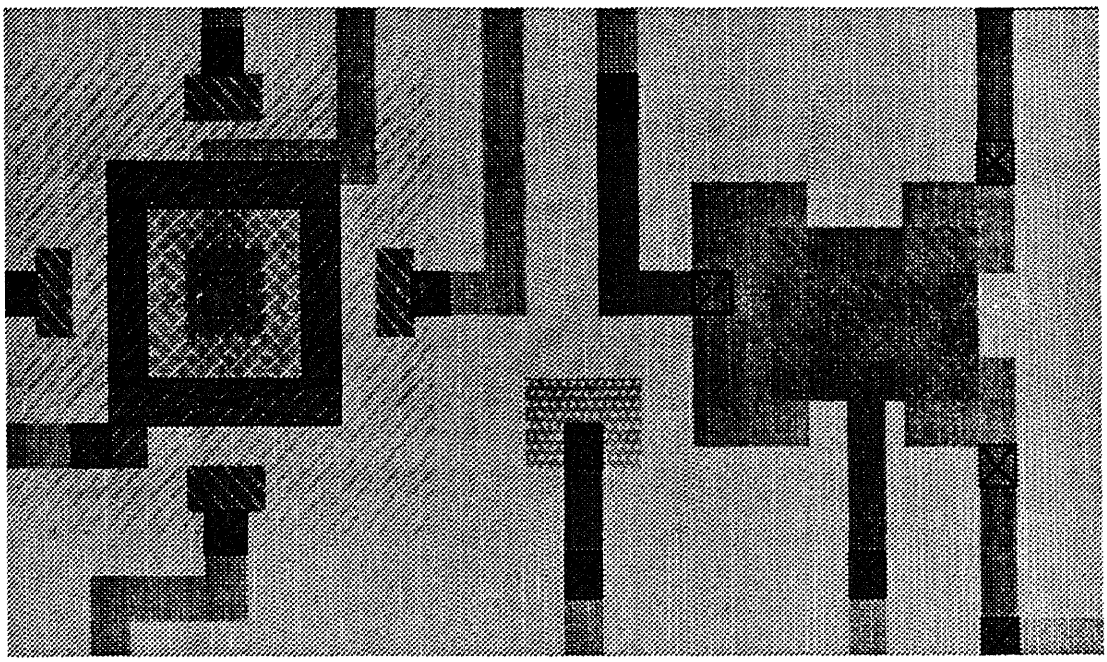


**Figure 3.4** Magic layout of 3-D Non-merged BiCMOS MFS

### 3.3 3-D Magnetic Field Sensor in Merged BiCMOS Technology

In this section, a design of a 3-D magnetic field sensor with merged structure in BiCMOS technology is given. The detailed design of the merged structure by common diffusion as well as the high gain transduction circuit are presented. The merged structure has the advantage of less area, less external contacts and less parasitic capacitance. The area of the sensing part with the merged structure is estimated to be $25\mu m \times 48\mu m$. The SPICE simulation results show that when a relative change in current $\Delta I/I$ is 0.001, about $13.6mV$ and $8.5mV$ can be detected at the output in X(or Y) and Z directions, respectively. The cross-sensitivity is eliminated. The designed BiCMOS sensor can operate in the voltage scale from 0-5V with satisfactory output voltage swings. That makes the device compatible to the post signal processing circuits and can be

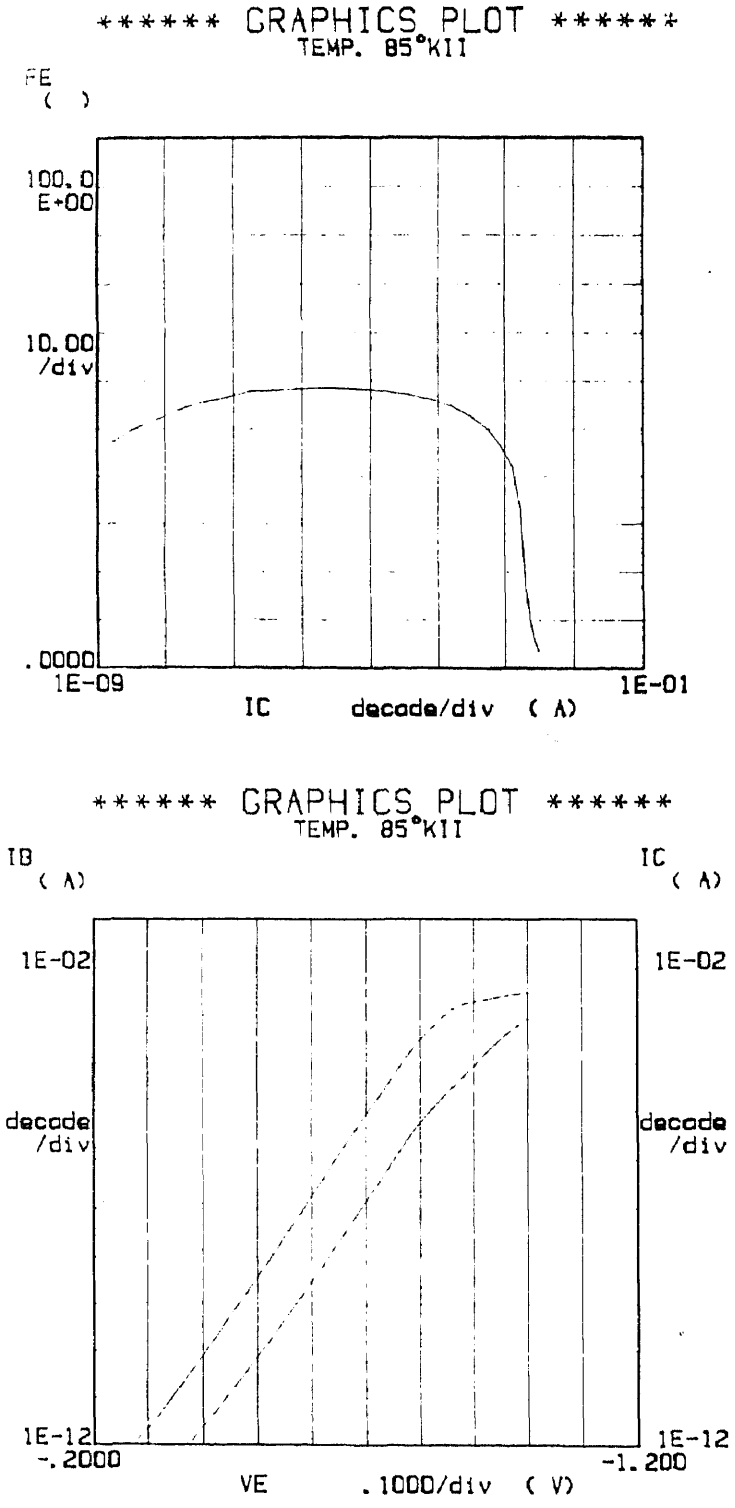



**Figure 3.5** Gummel plot of the four collector NPN in 3-D MFS

connected directly without additional voltage transfer. For example, the sensor element can be easily integrated with the signal processing circuitry acting as

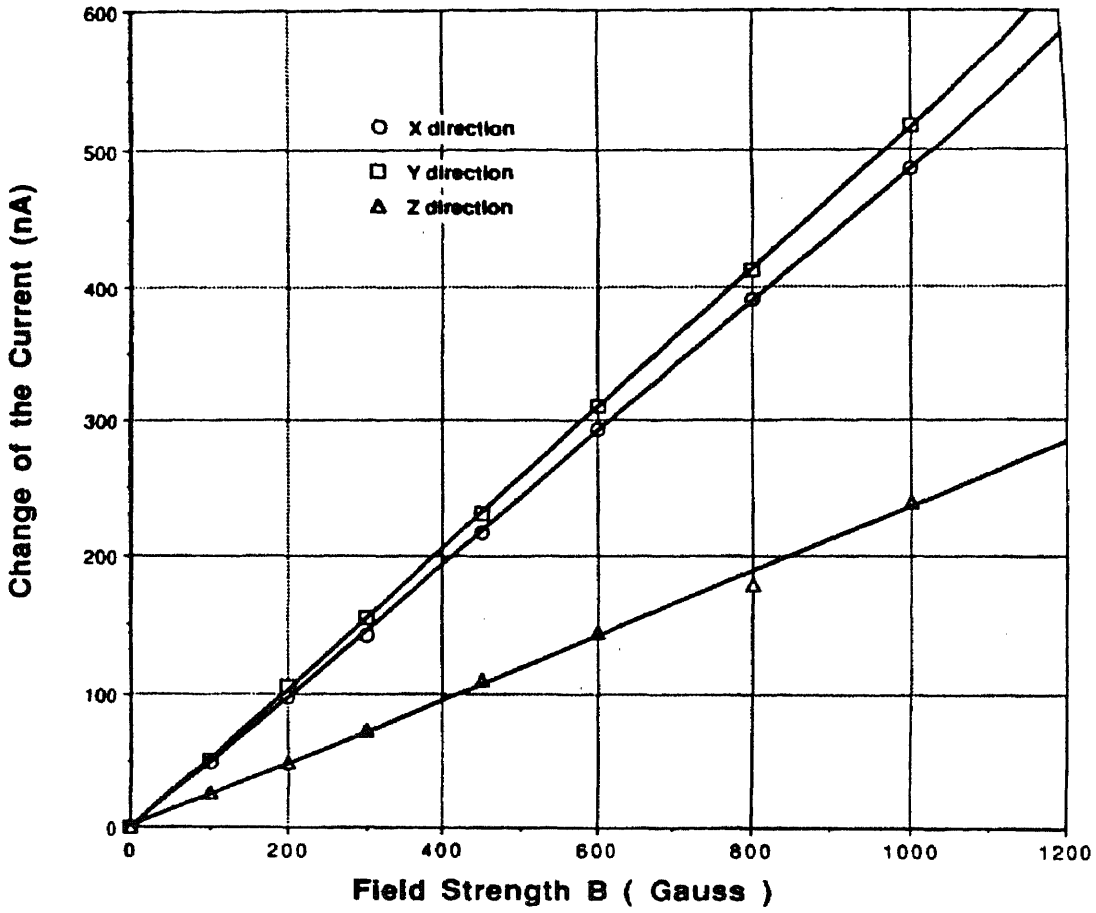



**Figure 3.6** Test results of sensitivities of 3-D MFS in BiCMOS process

"smart sensors". The designed sensor has been used as an individual cell of a large sensor processing system( in chapter 4)

### 3.3.1 Device Structure and Operation

The Stanford $2\mu m$ BiCMOS technology has the advantage of implementing high gain polyemitter bipolar transistors. The npn-PMOS merged structure[18]-[21] has been developed and used successfully in digital BiCMOS circuits. According to the design rules of the process, in an non-merged structure, the base diffusion of npn and the source of PMOS cannot be

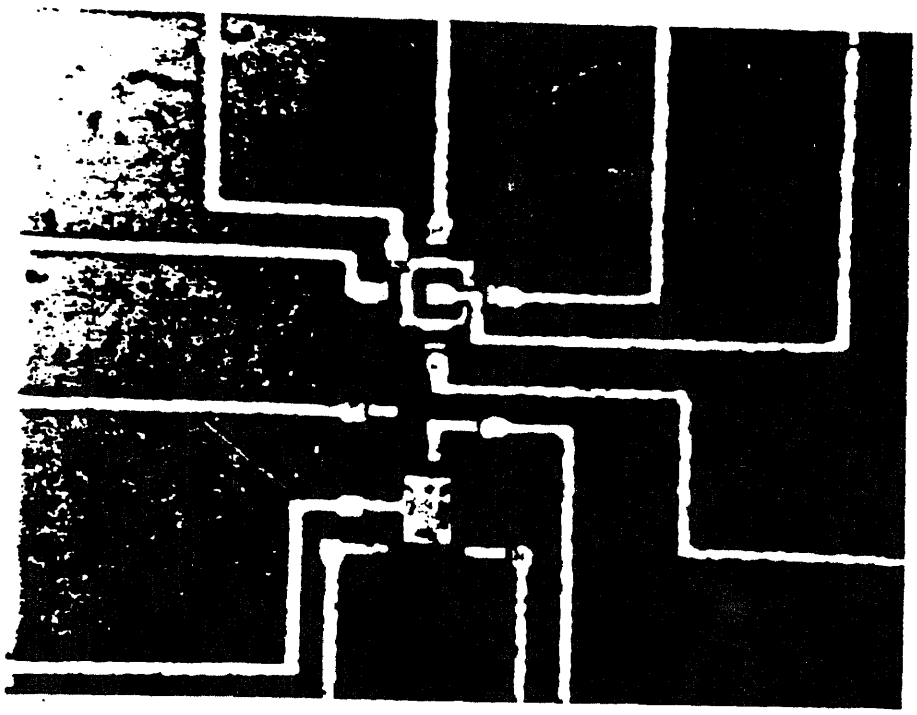


**Figure 3.7** Photomicrography of the BiCMOS 3-D magnetic field sensor in non-merged BiCMOS technology

fabricated too closely to each other because the p-diffusion must be at least 5 micron from the edge of the n-well and the n-collector also needs to be at least 4 micron away from the n-well. In the merged structure, however, the p-base of a vertical npn bipolar transistor is merged with the p-diffusion of the PMOS transistor[20],[21], which has the advantage of a more compact device design. Not only there is an area advantage, but also the external contacts between npn and PMOS by polysilicon and metal has been removed to reduce the parasitic capacitances and resistances. A compact structure is extremely important for the design of a 3-D magnetic sensor to avoid any undesired

spatial resolution due to the magnetic field gradient. It is therefore necessary to have a uniform field through out the device area.

To achieve uniform sensitivity, proper bias conditions are necessary to keep the npn transistor operating in its linear region and the PMOS transistor in its saturation region. The collector should always be kept at higher potential than that of the source of PMOS because the collector diffusion of npn transistor is in contact with the substrate (n-well) of the PMOS.

The basic three dimensional BiCMOS magnetic field sensor based on the Stanford merged process is shown in Figure 3.8. The base of the vertical npn transistor is merged with the source of the PMOS through a common p+ diffusion. The four collector contacts $C_{x1}$, $C_{x2}$, $C_{y1}$, and $C_{y2}$ are placed symmetrically with respect to the central emitter. The base contact(p+ diffusion) is also placed symmetrically and merged with the source of the split-drain PMOS. The collector diffusion is connected with the n-well.
The device cross-section through A-A' and B-B' are shown in Figure 3.8(b) and Figure 3.8(c) respectively. The voltage bias of each electrode ensures the operation of the PMOS device in its saturation region and npn transistor in its active region. As we know, when the PMOS is operating in its saturation region, the carrier flow from source to drain is mainly taking place in the inversion layer along the $SiO_2 - Si$ interface under the gate, as shown in Figure 3.8(b). This lateral flow is responsible for the z component of the magnetic field. When the magnetic field in z direction is absent, i.e. $B_z$, the currents flowing through both the drains of PMOS are equal (geometrical symmetry), i.e. $I_{D1} = I_{D2} = I_D/2$, where $I_D$ is the bias current, $I_{D1}$ and $I_{D2}$ are the currents flowing in drain1 and drain2 respectively. However, when there is an non-zero magnetic field, $B_z$, the carriers flowing in the transistor

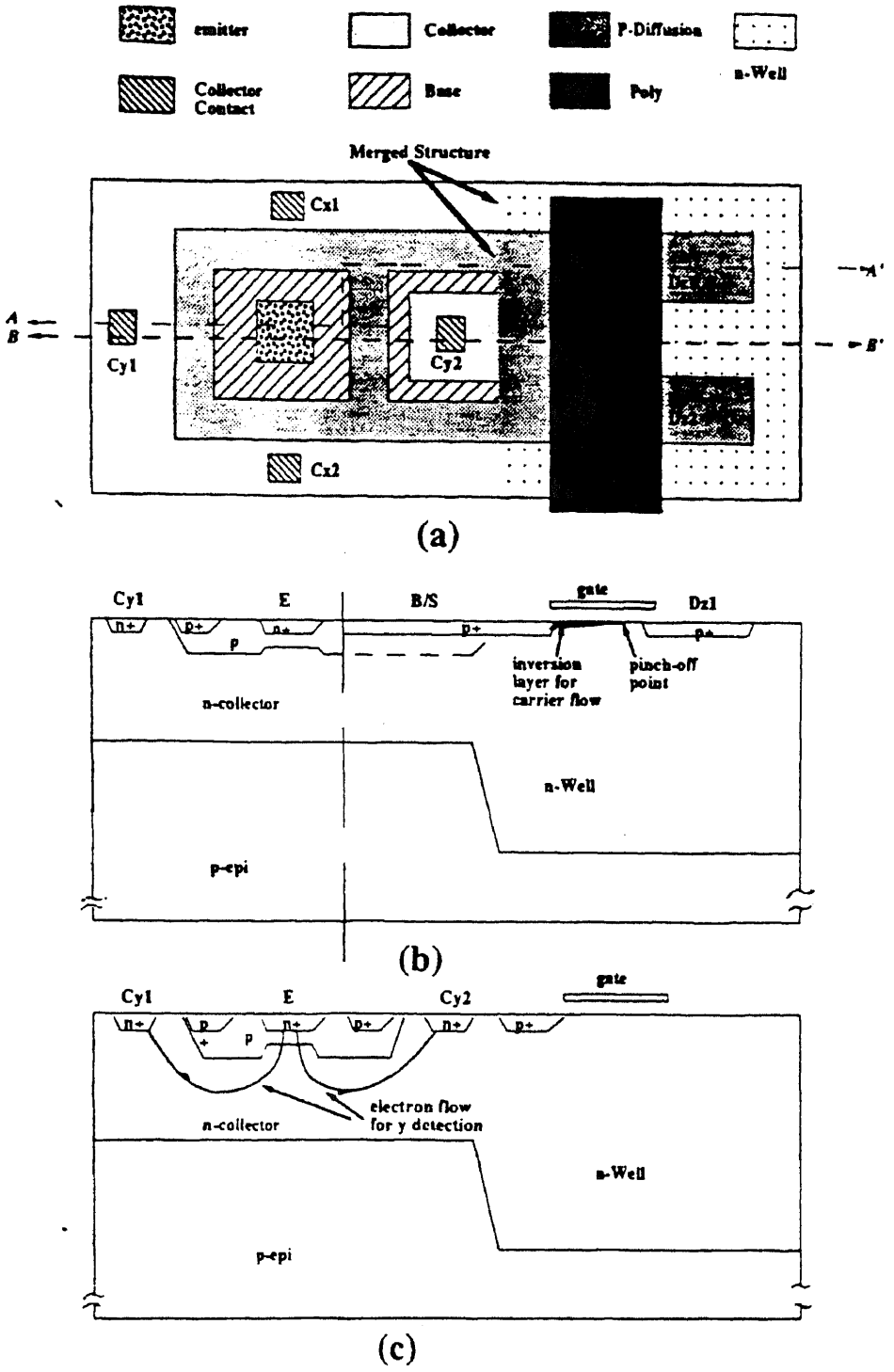



**Figure 3.8** The BICMOS merged device structure of the 3-D magnetic field sensor. (a)The top view of the device showing the symmetrical structure: the four collector contacts and the two split drains; (b)the cross-section of the device along the A-A' axis showing the merged base and the source through common p+ diffusion and connection of n-collector with n-well; (c)the cross-section of the device along B-B' axis showing the vertical component of the carrier flow, used to sense By.

are deflected, due to the Lorentz force, which is a vector product of the current and the magnetic field vector. This results in an imbalance in the current flowing through the two drains of the MAGFET. They are in the form of $I_{D1} = I_D/2 + \Delta I_{ZZ}$ and $I_{D2} = I_D/2 - \Delta I_{ZZ}$, where $\Delta I_{ZZ}$ is the current splitting as a function of $B_Z$. The total drain current$I_{D1} + I_{D2} = I_D$ remains constant.

The y component of the magnetic field is responsible for the deflection of the vertical component of the collector current in the y direction (causing a collector current difference $\Delta I_{YY}$ between the collector $C_{y1}$ and $C_{y2}$, as shown in the Figure 3.8(c). Similarly the x component of the field is responsible for the deflection of the collector current in the x direction( $\Delta I_{XX} = I_{Cx1} - I_{Cx2}$). The change of the currents due to the field is [14] $\Delta I_i = 2I_{Ci}L'B_i\mu_H/W_e$ where, $W_e$ is emitter width; and $L'$ is mean length of the vertical collector current path.

### 3.3.2 Sensitivity analysis

In the device structure, since the n-collector, formed by the triple-diffusion process, is in-contact with the n-well of the PMOS(Figure 3.8(b) and Figure 3.8(c)), the cross-sensitivity could be analyzed in the following details. The lateral current in the PMOS device does not have any vertical component, therefore the response of the device to the z component of the magnetic field will be free from the cross-sensitivities from the y or x component of the field. The voltage at the $C_{y2}$will be modified when the y component of the field is present. The voltage modification at $C_{y2}$ will modify the substrate voltage of the PMOS device thereby modifying the threshold voltage. Any modification of the threshold voltage will modify the device current $I_D$. Even if the value of the lateral current $I_D$ is slightly changed because of the change of the substrate

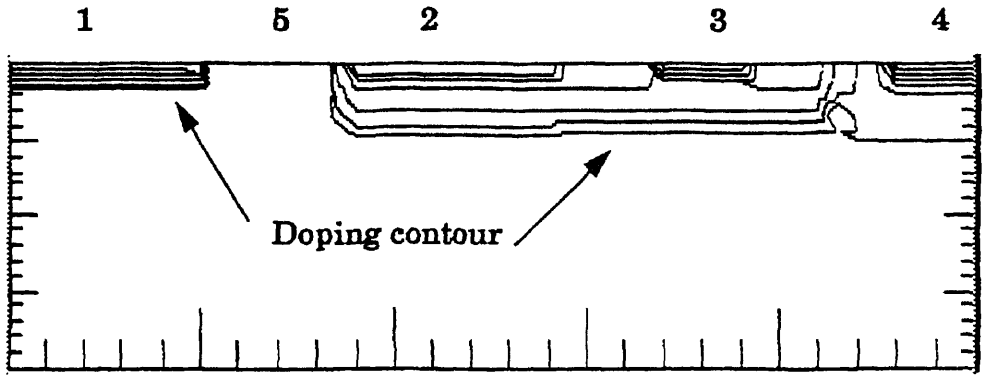



**Figure 3.9** PiscesII simulation structure. Number 1 through 5 presents the position of drain, source(merged with base), emitter, collector and gate.

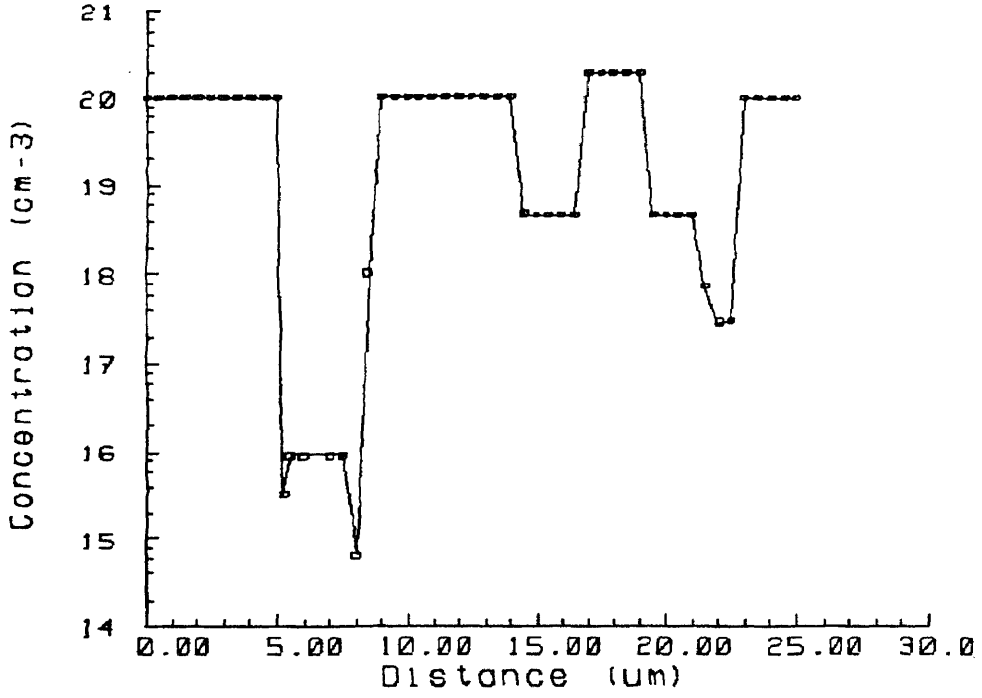



**Figure 3.10** Lateral doping profile through Y direction

voltage during the presence of $B_y$, the changes in $I_{D1}$ and $I_{D2}$ occur by the same amount, since the device is strictly in geometric symmetry along B-B' axis. The difference of the current between two split drains will be unchanged.

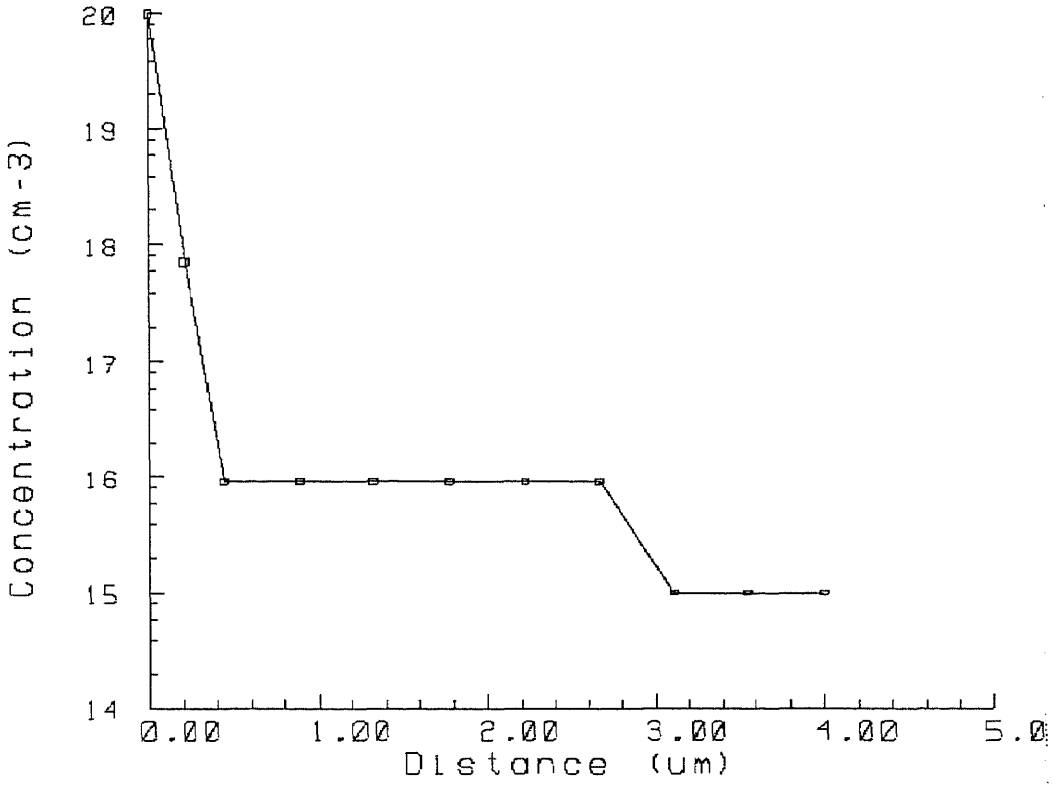



**Figure 3.11** Vertical doping profile through drain of MAGFET

The other possibility of current sharing between $C_{y2}$ and the MOS inversion layer during the presence of $B_y$ (when $C_{y2}$ receiving more current) can be ruled out because of the presence of the reverse biased p+ – n junction.

### 3.3.3 PISCES simulation

The two dimensional device simulation tool PISCES-IIB[23] has been used for the device optimization. Different sizes and distributions of the base contact

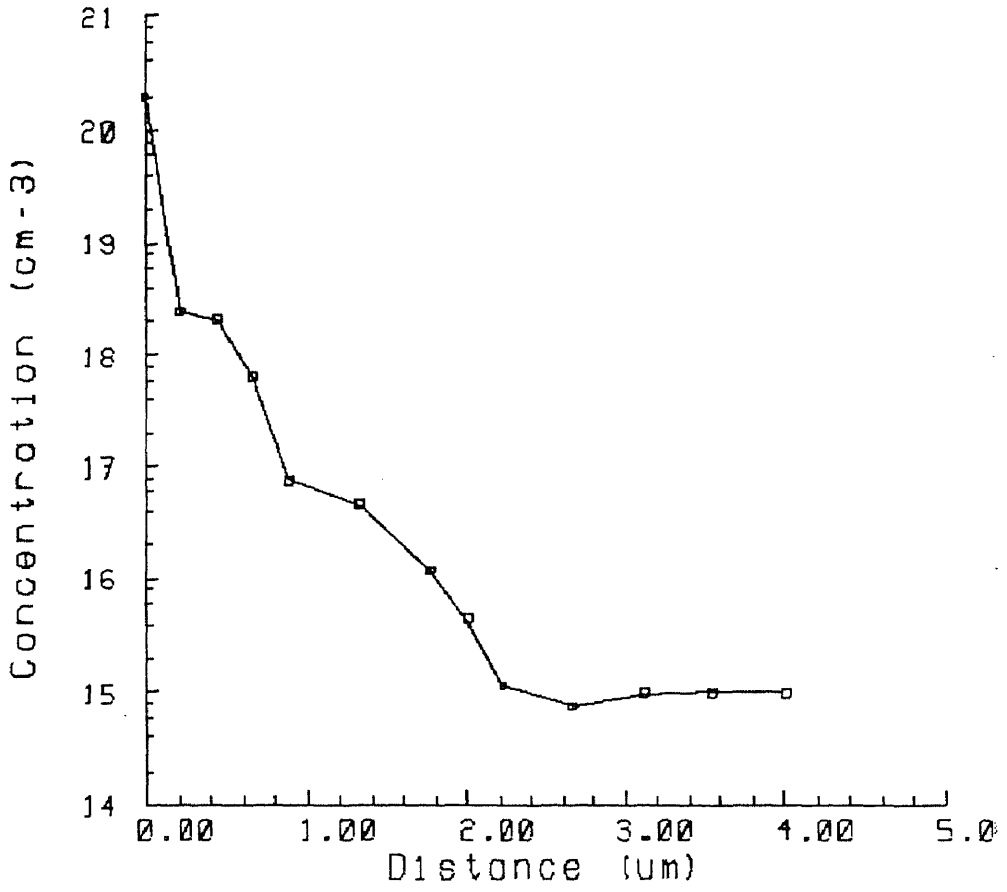



**Figure 3.12** Vertical doping profile through the emitter

and emitter were designed to get an optimized geometry for improved electrical characteristics and high current gain. The process parameters such as doping concentration, gate oxide thickness, etc. determine the device response to an applied magnetic field. A fully simulated example is shown in the following Figures. Figure 3.9 shows the simulation structure for the merged 3-D MFS. Figure3.10 to Figure 3.13 show the doping profiles through different cross-sections. I-V characteristics are shown in Figure 3.14 to Figure 3.16.

### 3.3.4 Circuit Implementation

From the above description of the device, a proper circuit has to be designed to ensure that the device operates in an optimized state and to amplify the signals so that high sensitivities can be obtained. Figure 3.17 shows the complete circuit diagram of the 3-D magnetic field sensor. In the Figure, the transistor M1 is a split-drain PMOS whose gate is connected to Vss to ensure its operation

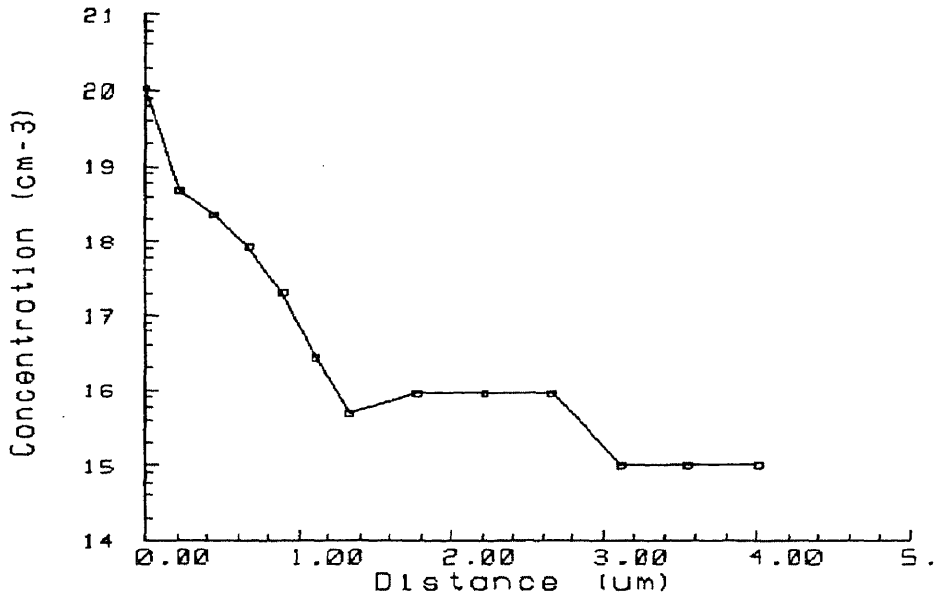



**Figure 3.13** Vertical doping profile through the merged structure

in saturation region. This transistor is sensitive to the vertical (Z direction) magnetic field. Q2 is the vertical npn bipolar transistor with two pairs of symmetric collectors, two of them detecting the magnetic field in X direction and the other two in Y direction. Q1 and Q3 act as current sources which can provide constant currents when the biases are adjusted to keep the transistors operating in their deep active regions. Transistors M2-M3, M4-M5 and M6-M7 form the three current mirrors which act as active loads, to three different

directions, for higher impedance thus improves the absolute sensitivities of the

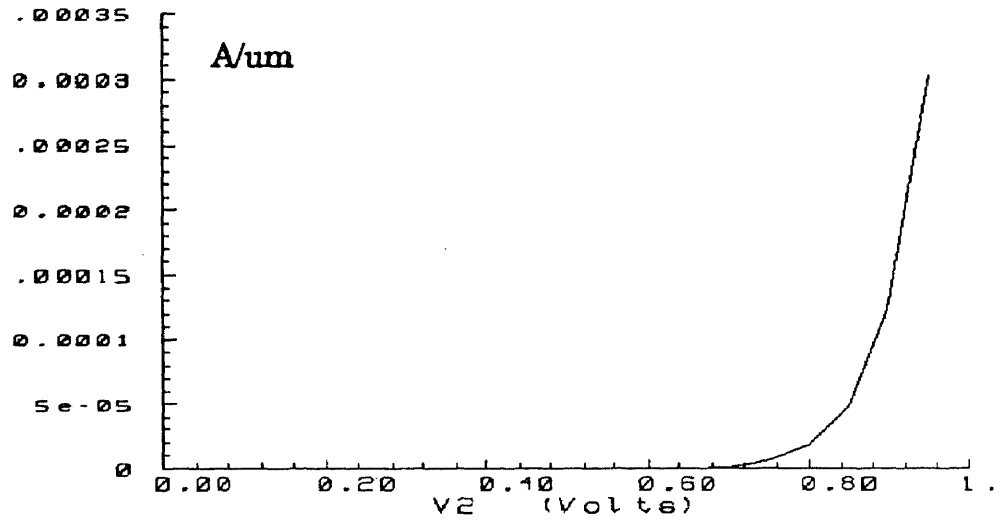



**Figure 3.14** Base current vs. base voltage for magnetotransistor

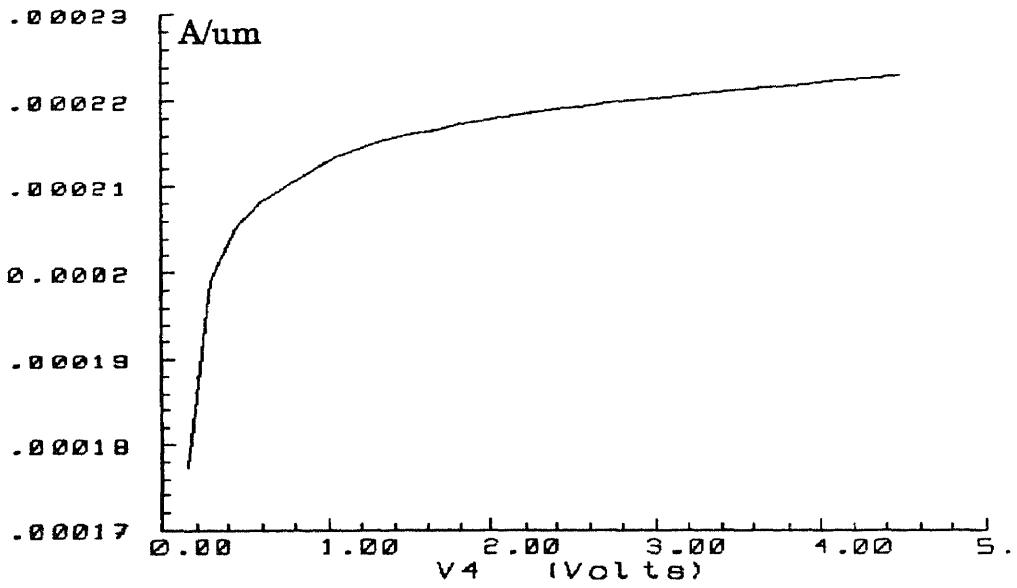



**Figure 3.15** Collector current vs. voltage of magnetotransistor

sensor. $V_x$, $V_y$, $V_z$ indicate the outputs in three dimensions.

In the circuit design, the inherent advantages of the BiCMOS

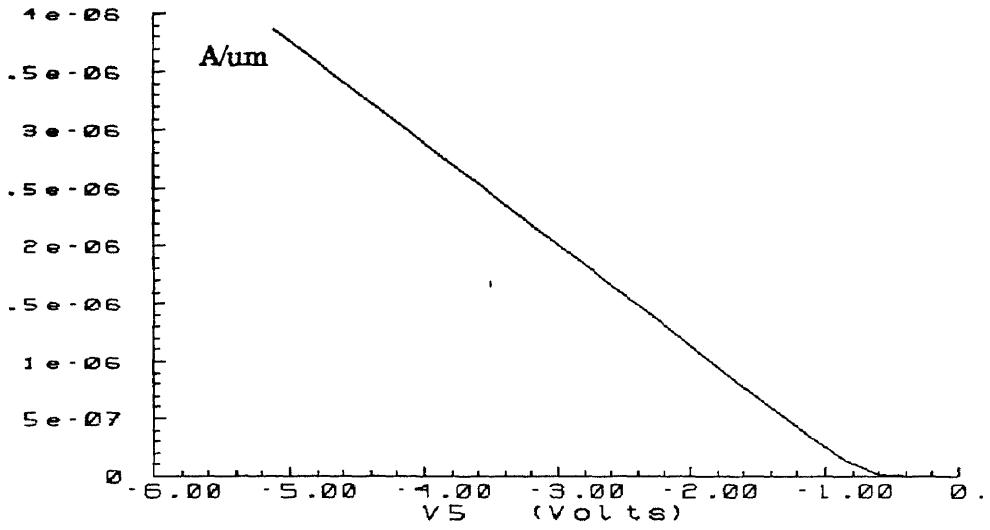



**Figure 3.16** Threshold voltage for the MAGFET

technology have been exploited. Since higher current density can be more easily achieved from bipolar transistors, two npn transistors (Q1 and Q3) are used as the current source in order to keep the sensing transistor M1 and Q2 operating in their deep saturation and active regions respectively. Meanwhile the MOSFETs are used to build three pairs of current-mirrors so that a good output voltage swing and less off-set voltage can be obtained due to the high resistive property of the MOSFET. The detailed optimization simulation of the whole 3-D Magnetic field sensor is given in the following section.

### 3.3.5 Layout

The layout has been implemented with the MAGIC V6 by using the Stanford 2 $\mu m$ BiCMOS technology file(Figure 3.18). The gate length of M1 is $4\mu m$, and

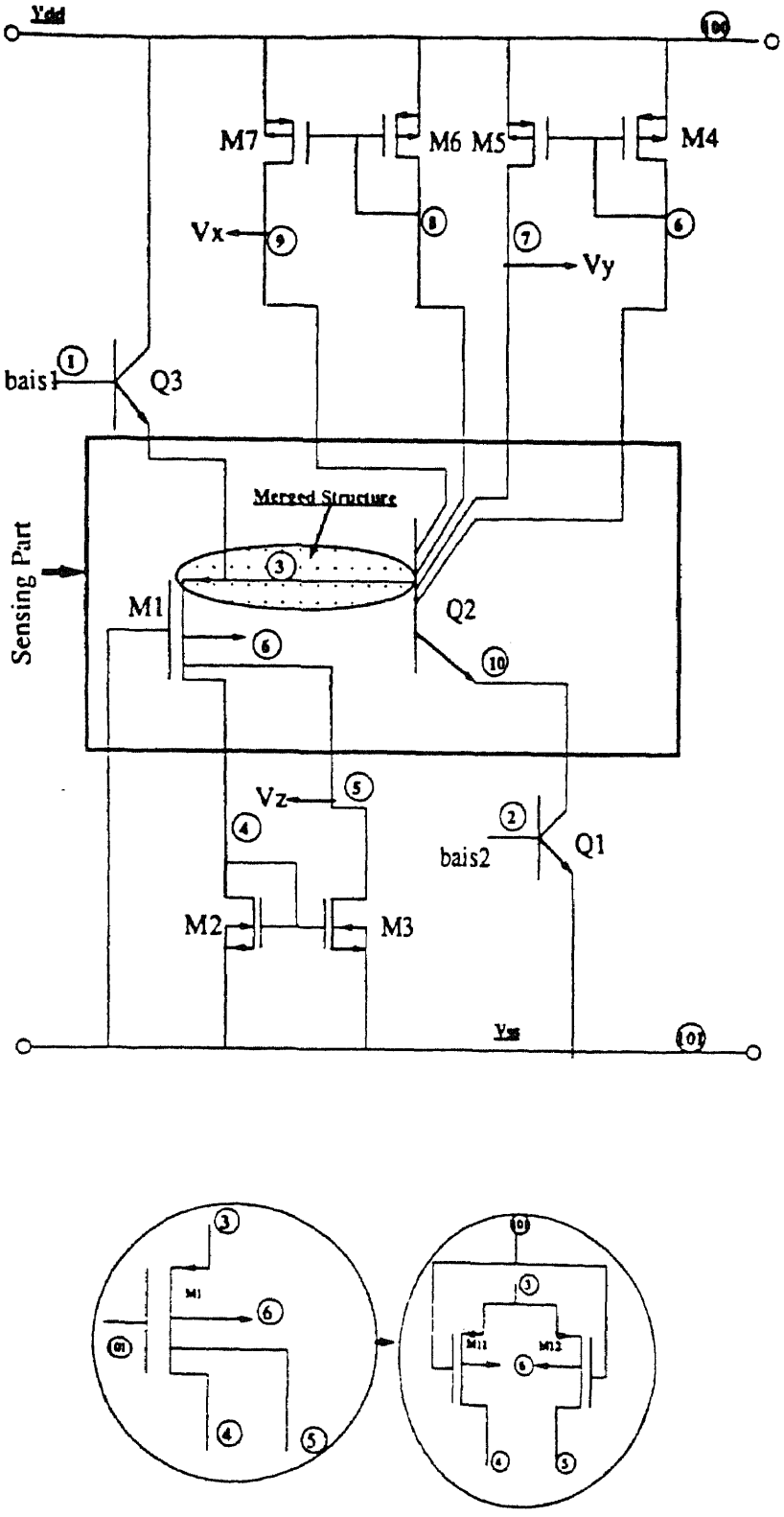



**Figure 3.17** The circuit diagram of 3-D magnetic field sensor in merged BiCMOS technology. The transistors and the nodes are labeled for SPICE simulation. M12 and M11 are the equivalent transistors to the split-drain MAGFET in the simulatio Vx,Vy and Vz are the outputs.

the width is 12 $\mu m$ with the two symmetric drains whose areas are both 16 $\mu m^2$. The base of Q2 is a $12\mu m \times 12\mu m$ square surrounded by four collector contacts symmetrically. The active area of Q2 is selected as $4\mu m \times 4\mu m$. Both the active areas of Q1 and Q3 are $2\mu m \times 2\mu m$. The aspect ratio of the rest of the transistors, from M3 to M8, is unity so that the total chip area can become as small as possible. The area of the sensing part is $48\mu m \times 25\mu m$ in the merged structure compared to $58\mu m \times 30\mu m$ in the non-merged structure (Figure 3.4).

### 3.3.6 SPICE Simulation

The designed circuit has been simulated with the SPICE2.G circuit simulation package.We have assumed a linear device response to incorporate the effect of magnetic field for simulation purposes. The effect of the magnetic field manifests itself in the current density distribution in the base-collector region in a bipolar transistor[24] and in the pinch-off region of a split-drain MOSFET. The magnetic field modulation of the emitter injection is assumed negligible and carrier deflection was considered to be the dominant mechanism for the linear magnetic response. Possible nonlinearities in response, due to magnetoconcentration effect[24] is neglected in our SPICE simulation.

The objective of the simulations are:

(1)To determine the DC operating conditions with suitable bias voltages when Vdd=5V,Vss=0V;

(2)to determine the gains with the active load circuits.

(3)to determined the frequency response of the designed 3-D magnetic filed sensor.

The circuit description used for SPICE simulation was directly extracted from the device layout to include all the parasitic capacitance in the

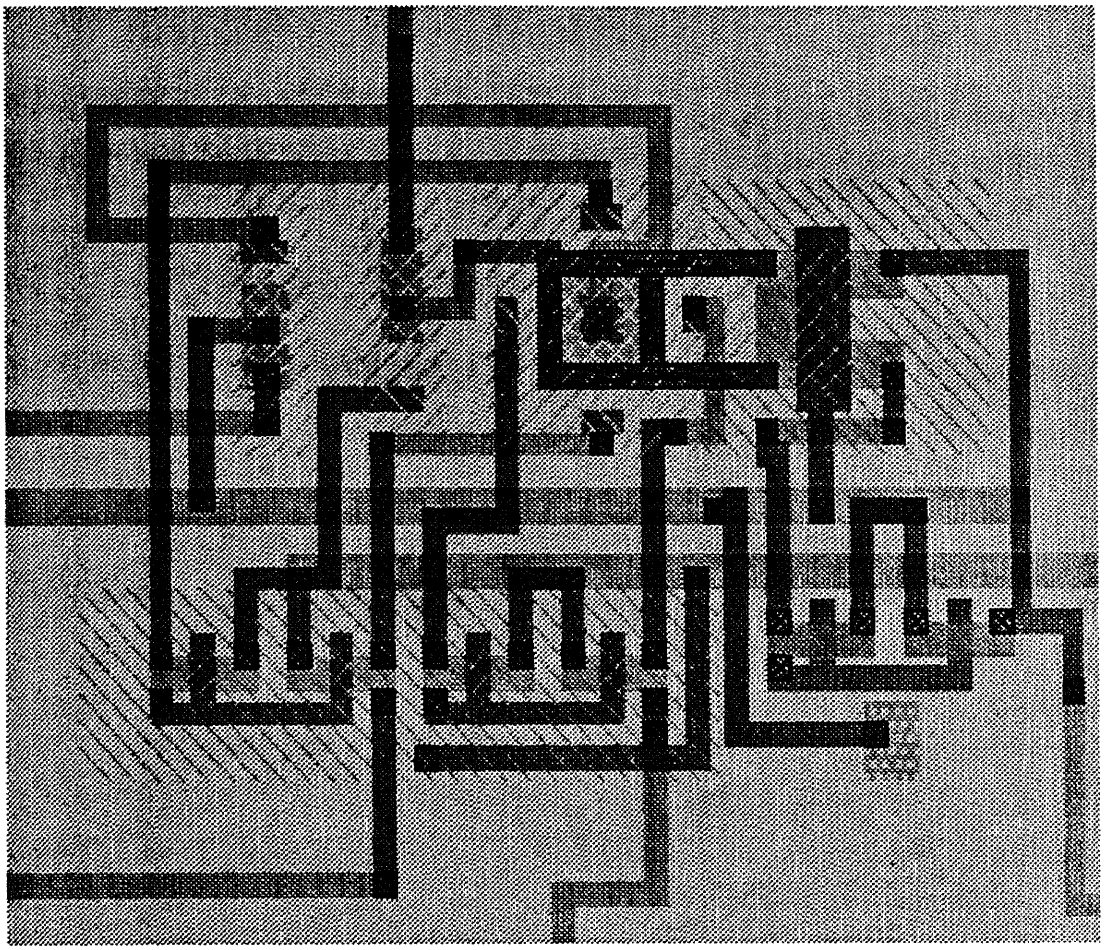


**Figure 3.18** Magic layout of the 3-D magnetic Field sensor with voltage output circuit in merged BiCMOS technology

design. The simulation also uses the most updated Stanford BiCMOS parameter models. The labeled nodes for simulation and the equivalent circuits for the split-drain PMOS and four-collector npn transistor are shown in Figure 3.17.

### 1) Bias Voltages Simulation

The bias conditions were chosen to ensure that all MOSFETs are operating in saturation and all bipolar transistors operating in the forward active regions.

Meanwhile the bias conditions are also optimized to ensure the three outputs have their possibly maximum voltage swing. The detailed simulation results are shown in the following tables. Here the gate of the MAGFET is connected to 0V, node 4 and bias2 respectively. At each case, both bias conditions bias1 and bias2 are set at different values during simulation. The detailed simulation results are listed in following tables respectively. The node voltages are listed for analysis of the DC operation states of every transistors. Obviously, V(4)=V(5), V(6)=V(7)=V(8)=V(9) when no magnetic field appears. So, in the following tables, only V(3), V(4), V(6) and V(10) are listed when different bias conditions are applied.

**Table 2** Voltage Distribution with the Gate of the MAGFET(M1) Connected to Node 4

| | Bias voltage(v) | | Node voltage(v) | | | |
|---|---|---|---|---|---|---|
| | Bias1 | Bias2 | V(3) | V(4) | V(6) | V(10) |
| case 1 | 3.7500 | 0.7800 | 2.9811 | 1.0208 | 3.5043 | 2.2793 |
| case 2 | 4.0000 | 0.8000 | 3.2189 | 1.1309 | 3.3866 | 2.4994 |
| case 3 | 4.4000 | 0.7800 | 3.6068 | 1.2678 | 3.4879 | 2.9027 |

**Table 3** voltage distribution with gate of MAGFET (M1) connected to node 101

| | Bias voltage(v) | | Node voltage(v) | | | |
|---|---|---|---|---|---|---|
| | Bias1 | Bias2 | V(3) | V(4) | V(6) | V(10) |
| case 1 | 3.2300 | 0.7800 | 2.4447 | 1.2073 | 3.5187 | 1.7450 |
| case 2 | 4.0000 | 0.8000 | 3.1821 | 1.6042 | 3.2202 | 2.4627 |
| case 3 | 4.4000 | 0.8000 | 3.4718 | 1.7394 | 3.2102 | 2.7512 |

From table 2, in case2, we can see the V(6) is very near V(3), so the Q2

is hardly working in its active region; when we increase the bias1 more, as in case 3, the Q2 is totally cut off. In case 1, we can see, Q2 is working in its active region, and M1 is also working in its saturation region, as we desire, because the voltage drop between drain and source of M1 is greater than 0.8v, which is the threshold voltage value of this PMOS transistor. The other node voltages also show that all the load MOS transistors are working in their saturation region. Meanwhile Q3 and Q1 are both working in their active region which are expected to provide constant currents to M1 and Q2 for detecting of magnetic field vector.

**Table 4** Voltage Distribution with the Gate of MAGFET Connected to Bias2

| | Bias Voltage(v) | | Node Voltage(v) | | | |
|---|---|---|---|---|---|---|
| | Bias1 | Bias2 | V(3) | V(4) | V(6) | V(10) |
| case 1 | 3.5000 | 0.7200 | 2.7360 | 1.6473 | 3.8997 | 2.0734 |
| case 2 | 4.0000 | 0.7500 | 3.4956 | 1.4204 | 3.9622 | 2.8395 |
| case 3 | 4.5000 | 0.7800 | 3.6852 | 1.5464 | 3.4859 | 2.9807 |

Now let us take a look of the output voltage swings. Under all the transistors work in their required region, from Figure 3.17, we can see the Z direction output voltage can swing from 0.8v to 2.18v(which is calculated from V(3)-Vth), so the swing value is about 2.18-0.8=1.38v. As to the x and y direction, the lowest voltage permitted at node 6 or 7 is 2.2793+1.0000 = 3.2793v (which ensure Q2 still in its required region), so the voltage swing can be 5-0.8-3.2798=0.9202v.

The same analysis can be applied on the table 3 and table 4. For table 3, the circuit configuration set the gate of MAGFET M1 to 0v. That makes the M1 working in more saturation region compared to table 2 case. In table 3,

case 2 and case 3 are no good because at these bias conditions, Q2 is nearly not working in the required region. In case 1, the voltage swing in Z direction is 2.4047-0.8-0.8=0.8047v, and the voltage swing in X and Y directions should be 5-2.7450-0.8=1.455v.

In table 4, as calculated, the gate of M1 is connected to bias2, whose voltage is between V(4) and V(101). From the obtained data, we can see, all three bias condition can make the circuit working in required situation. Of course, the bias conditions in case 1 provides best results. At this time, the voltage swing in Z direction is 1.1360v, and the voltage swings in X and Y direction cab be 1.1263v. So the voltage swing in X, Y and Z direction have closer value than in case of table 2 and table 3.

**2) Sensitivity gain simulation**

Because the SPICE can not simulate the magnetic field parameter directly, in our simulation, a very slight difference between the aspect ratios(W/L) of M12 and M11 in the SPICE input card is made. As the effect of magnetic field is represented by current density distribution[24], it can be taken into account qualitatively through an artificial current asymmetry. The quantitative representation was selected through the experimental results of the device as discussed in previous section. A small change of current $\Delta I$ between two drains was introduced, i.e.: $I_{D1} = I + \Delta I, I_{D2} = I - \Delta I$, which is analogous to the situation caused by the applied magnetic field. A similar procedure has been applied to Q2 by making a very small change of the active areas. The relative sensitivities of X, Y, Z directions are proportional to the relative changes of current, $\Delta I/I$, and thereby proportional to $\Delta V/V$. The response of the sensor to the magnetic field vector is, therefore represented through the gain of the circuit, as shown in the Figure 3.19. When a relative change in current $\Delta I/I$

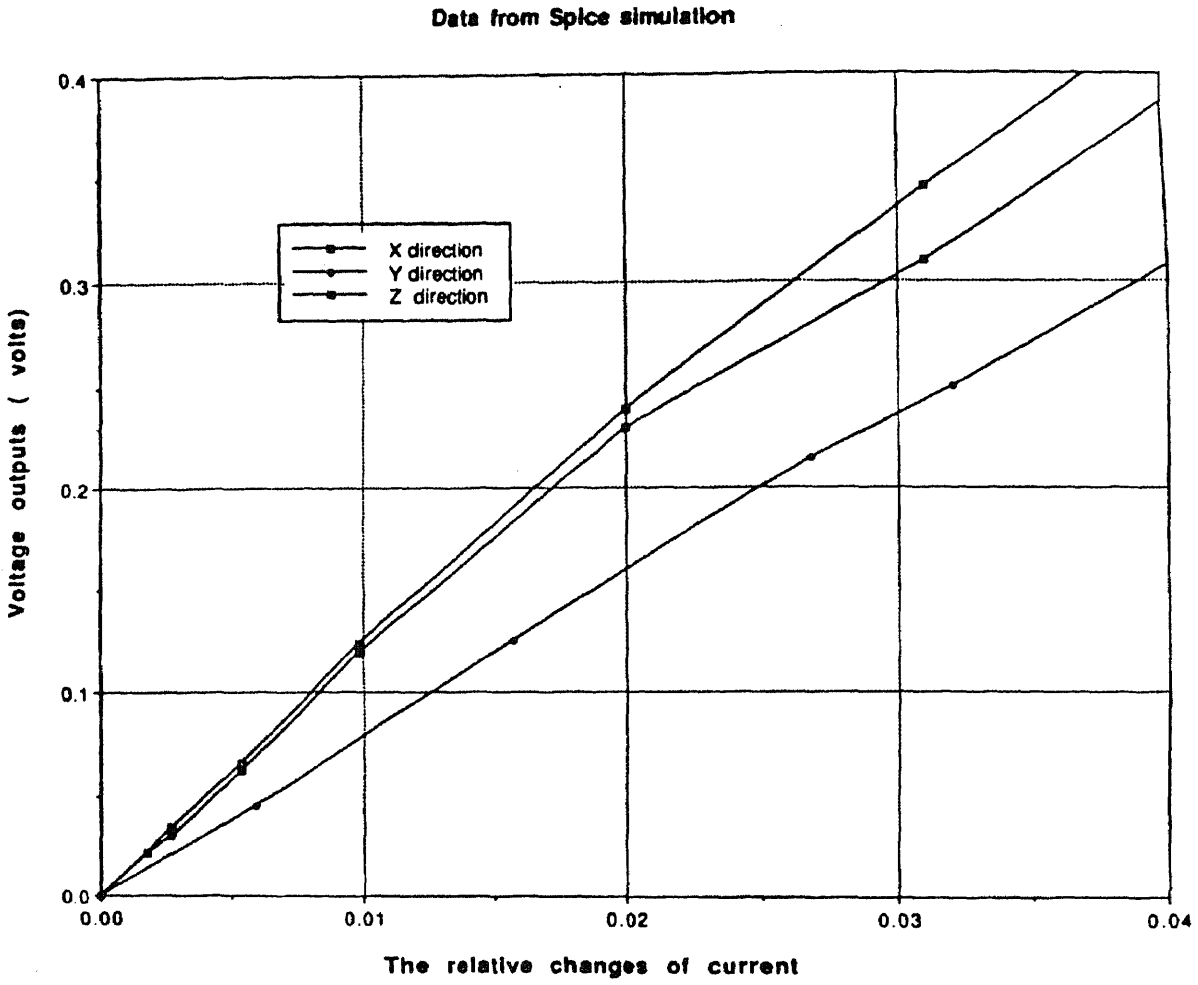



**Figure 3.19** SPICE simulation results showing the possible current splitting in the 3-D merged BiCMOS sensor circuit.

is 0.001, about 13.6mv and 8.5mv can be detected at the output in X(or Y) and Z directions respectively. The non-linearity in Figure 3.19 is due to the modifications of the dc operating bias conditions of the corresponding nodes where the MOS and bipolar transistors are driven into the linear and saturation region respectively.

### 3) Frequency Response Simulation

To verify the ability of the circuit to sense a time varying magnetic field, the frequency response has been estimated. All the capacitances simulated, are directly included from the circuit layout. The result is shown in Figure 3.20

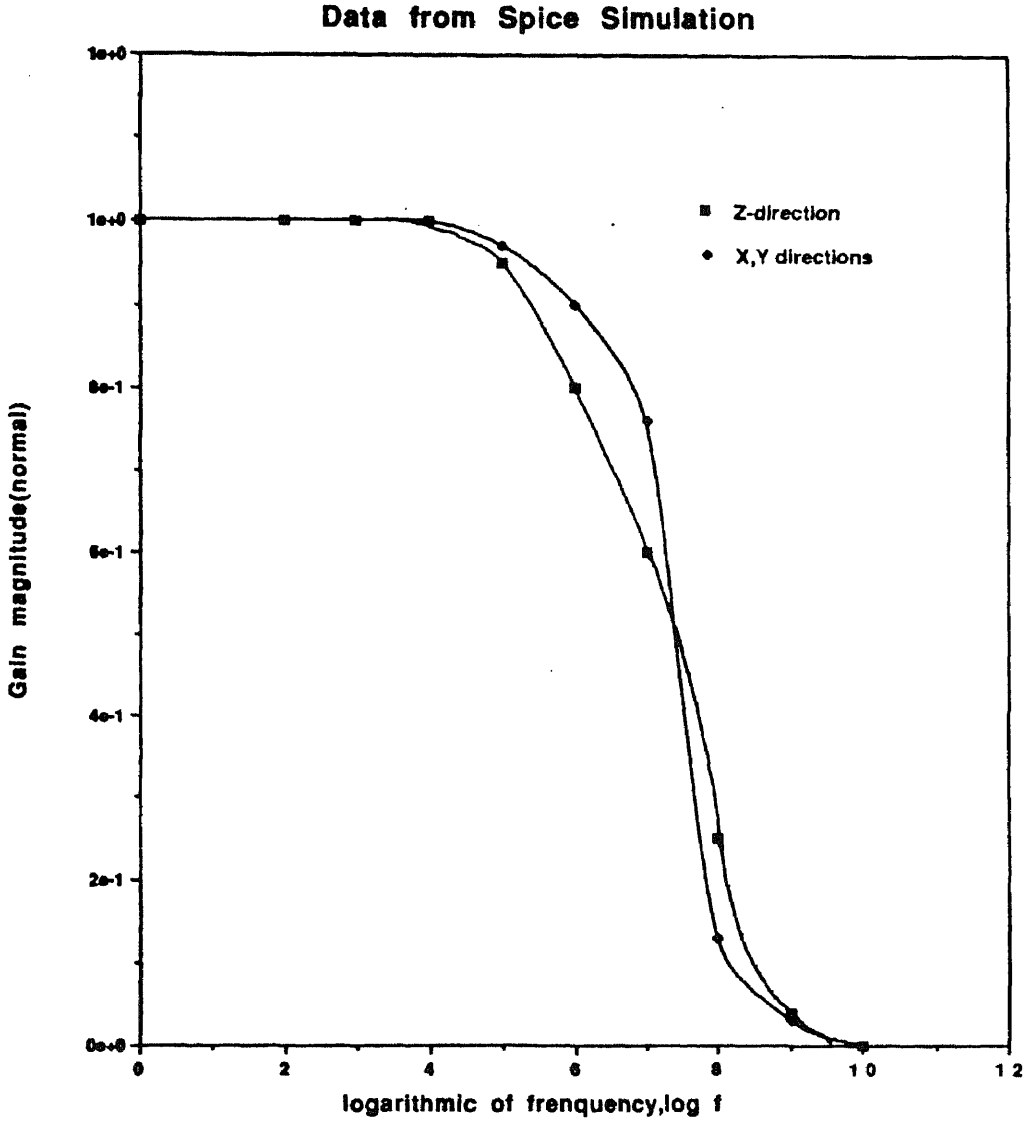



**Figure 3.20** Frequency response of the 3-D merged magnetic field sensors circuit

# CHAPTER 4

# 3-D MAGNETIC FIELD SENSOR ARRAY AND ITS APPLICATION

As mentioned in chapter 1, the integration of sensor technology and information processing circuitry is a goal which has great importance in implementation of computer vision system as well as robotic tactile sensing system. This chapter describes the development of a high resolution integrated magnetic field sensor array, where the 3-D merged BiCMOS magnetic field sensor, which has been discussed in last chapter, is used as an individual cell( build block). System architecture and circuit configuration are presented. Two applications of the designed array are described.

## 4.1 System Operation

The system architecture is shown in Figure 4.1. It is basically composed the main cell array, one row selection, three column selections ( for three dimensions respectively), active loads and input/output buffers. One column selection circuit is used all three directions x, y and z, because the sensing signals from three dimensions are expected to output simultaneously. The current mirror(CM) is used as the active load, and the 3-D merged BiCMOS magnetic field sensor described in last chapter is used as the cell(MC) in the array( Figure 3.17).

The cell array is scanned in a raster scan fashion. Two slightly different scanning methods are proposed in Figure 4.2 and Figure 4.3, respectively. because the scanning structure are strictly symmetrical in x, y and z direction( Figure 4.2 and Figure 4.3), only one direction in each Figure is

drawn for explanation of the scanning methods.

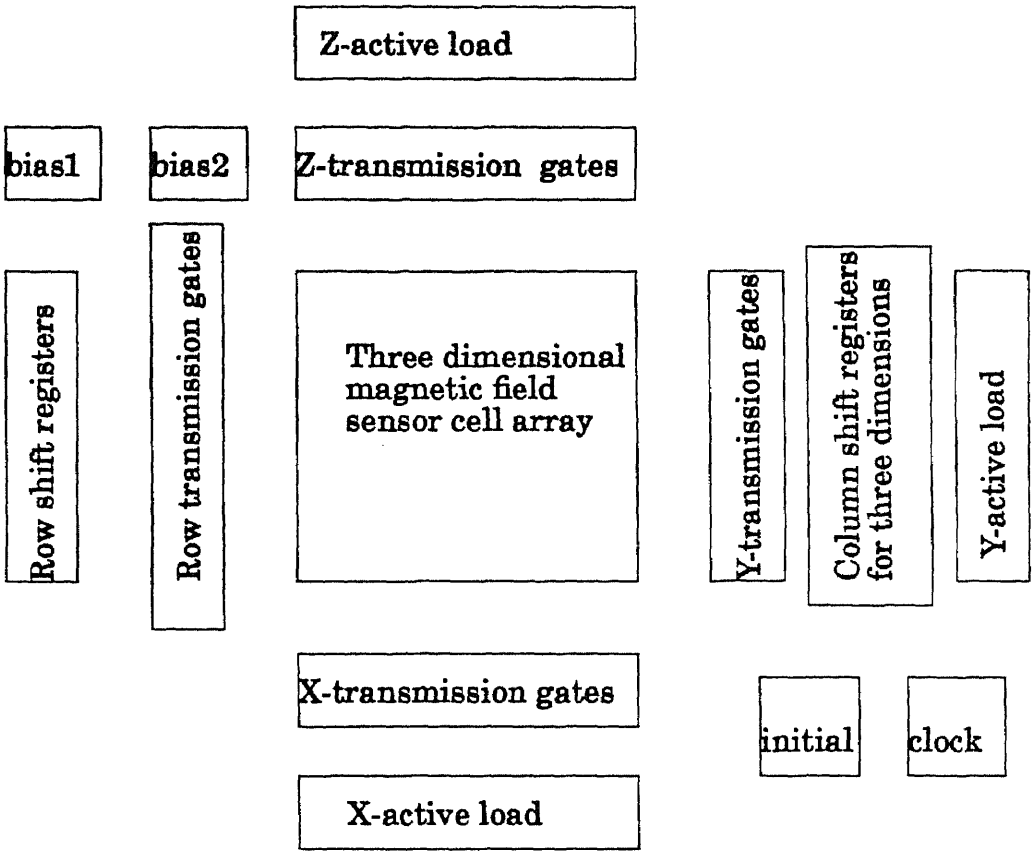



**Figure 4.1** System structure

In both Figures, shift registers along the left-hand side of the circuit shift a single "turn-on" bit, which allows current to flow through all the sensor cells in a single row. The current (actually there are three currents for x, y and z directions respectively, here we can select any one of them for illustration, like Z direction) through a cell is controlled by a switchable current source as shown in Figure 4.4. When the row select buffer is turned on, the bias voltages $V_{Bias1}$ and $V_{Bias2}$ are applied to the bases of Q3 and Q1( refer to the cell circuit in Figure 3.17). When the row select buffer is turned off, Vss is

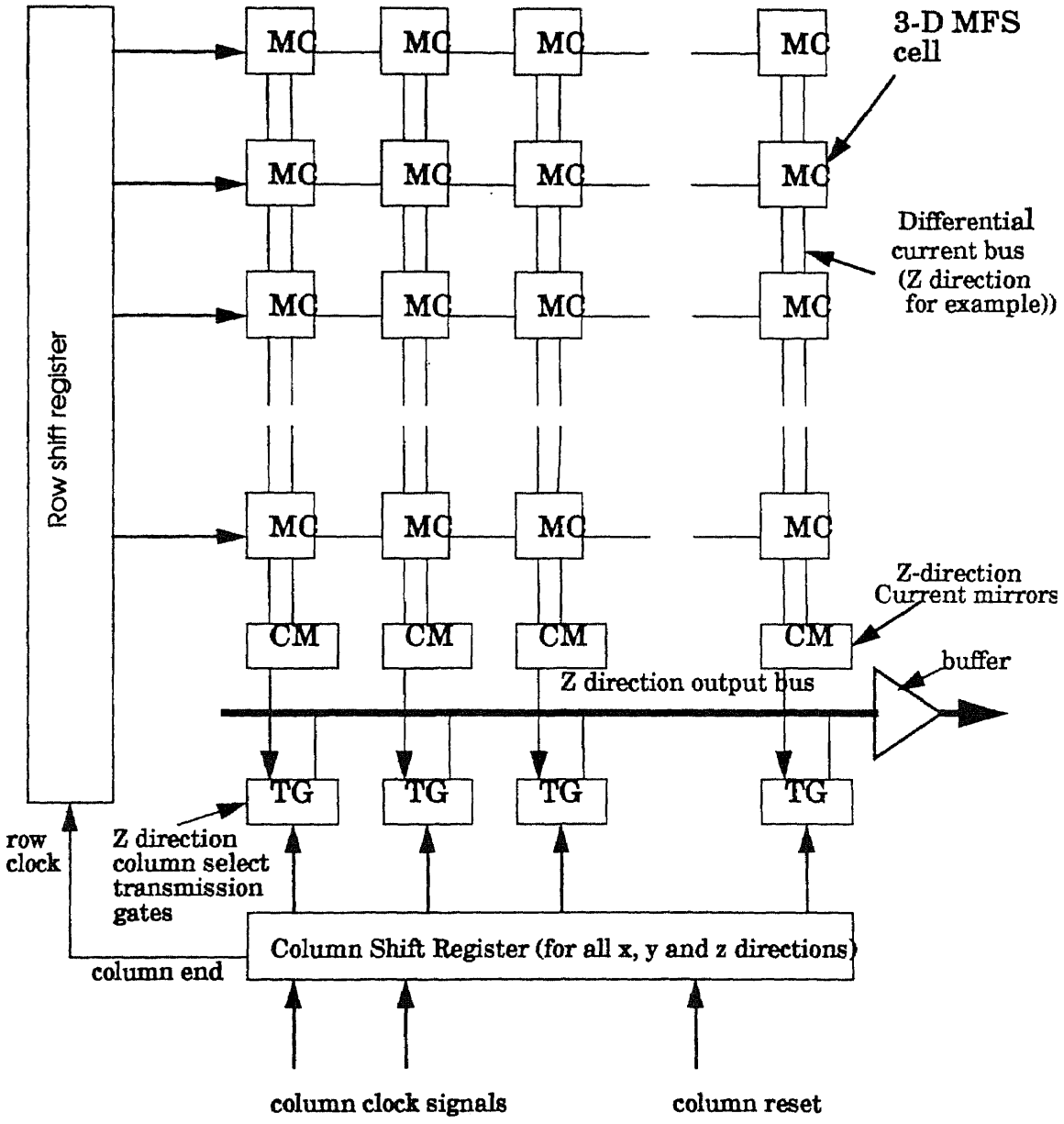



**Figure 4.2** The scanning circuitry A:.Each column has current mirror (note: For a clear view, only Z direction current buses are drawn in the Figure, the X and Y direction are similar, they both have other two sets transmission gates and current mirrors, but share the same column shift registers as Z direction's)

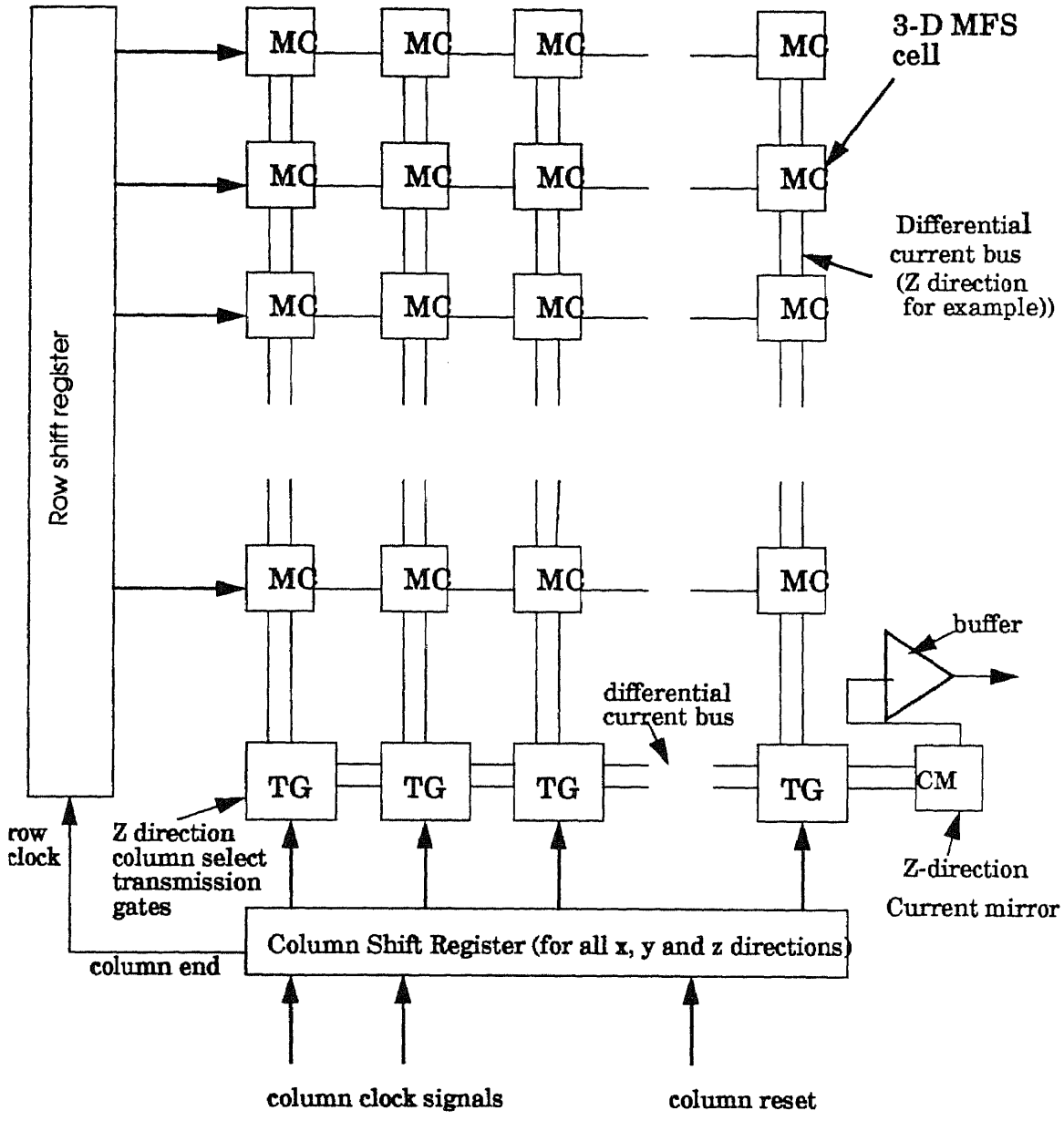



**Figure 4.3** The scanning circuitry B:.One current mirror common to all columns (note: For a clear view, only Z direction current buses are drawn in the Figure, the X and Y direction are similar, they both have other two sets transmission gates and current mirrors, but share the same column shift registers as Z direction's)

applied to the bases of Q1 and Q3, cutting off the flowing current through the 3-D sensor cells in that row.

As the scan proceeds, successive rows are turned on. Only one row at a time is on. Shift registers along the bottom shift a single "column-select" bit, which selects the output of one column at a time. In Figure 4.2, all devices in a given column share a single current mirror transistance amplifier located at the bottom of the column( in x, y directions, the current mirrors are put in the top side and right side respectively, which are not shown in the Figure)Since only one row is on at a time, these current mirrors have current flowing through them from one cell only. The row shift register is shifted only when a

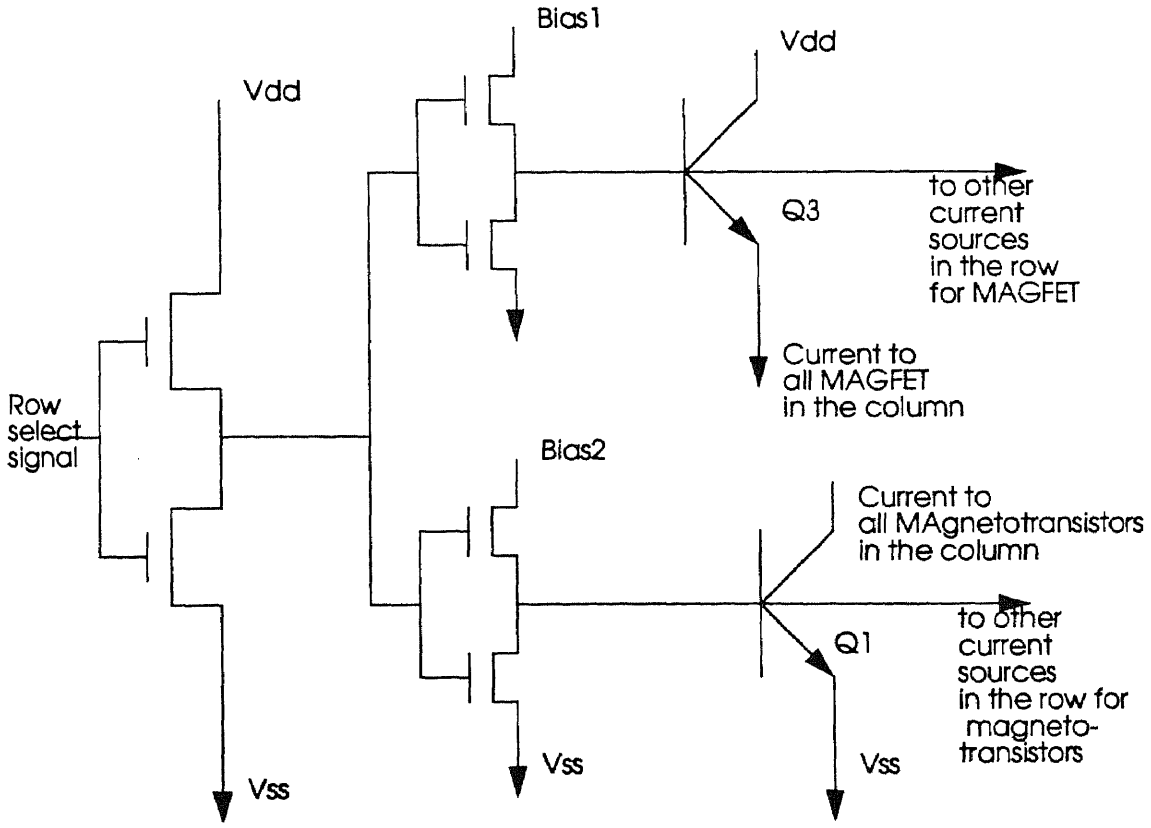



**Figure 4.4** The switchable current source supplying the 3-D MFS

complete column scan has been finished. The column shift register is shifted by an external clock signal. The outputs (x, y and z) of the selected cell current

is amplified and buffered before it is sent to an analog output pad. The shift registers are initialized by a reset pulse.

In Figure 4.3, there is only one current mirror amplifier for entire array in each direction( the Z direction is shown in the Figure). The current differential buses for each column are multiplexed onto a common differential current bus by transmission gates controlled by the column select signals. The common bus is terminated by the current mirror/transistance amplifier, which converts the current differential to a voltage. This voltage is then buffered and amplified before it is sent to the Z- output pad. The same situations to X and Y directions.

There is both an advantage and a disadvantage in performing the array scanning in this manner(Figure 4.3). The advantage is that one does not have to worry about the column-to-column offset voltages induced by slight difference in the current mirrors at the bottom of each column in the scanning method shown in Figure 4.2.In Figure 4.3, each column in each direction shares the same current mirror. Thus the method of Figure 4.3 results in lower relative offset voltages between sensors.

The disadvantage of the scanning method shown in Figure 4.3 is that it is slow. The reason this method results in a slow pixel clock rate can be understood with the aid of Figure 4.3. Consider the case of column $i$ and row $j$ being selected. In this case the $i$th differential current bus is at a voltage determined by the current mirror and sensor $ij$, for example, in Z direction, the typical voltage value is around 1 to 2 volts ( the detailed analysis has been discussed in section 3.3.6 in last chapter, and some values are listed in table3, table4 and table 5). All of the other differential current buses are charged to around 5v, since they are not pulled low by the current mirror, but are being charged through the MAGFETs in row $i$. The differential current buses have

the relatively large capacitance which must be discharged from 5v to around 1.5v when one clock from one column to the next. The discharge path is through the column-select transmission gate and the current mirror. The conductance of the current mirror is limited by biasing considerations( typically one wants to keep the current mirror transistors in saturation for linear sensitivity requirement, which has been detailed in section 3.3.6 in last chapter), and the size of the transmission gate is limited by the layout constraints. The capacitance of the differential current buses is set by the size of the chip (since they travel almost the entire length of the chip) and by the minimum allowable width of the metallization or polysilicon layer. The detailed circuit simulation will be presented in the next section of this chapter. From previous description, the scanning period T is decided by the total delay time $\tau$ of the complete array system, which could be express as,

$$T_{min} = \tau = \Sigma\tau_{sr} + \Sigma\tau_{tg} + \Sigma\tau_{bus} + \Sigma\tau_{cell} \qquad (4.1)$$

where,

$\tau_{sr}$: delay time of each shift register;

$\tau_{tg}$: delay time of each transmissions gate;

$\tau_{bus}$: bus delay time;

$\tau_{cell}$: cell delay time.

of course, the larger the array is, the larger period T should be due to the increasing of dimension number n and longer bus lines.

## 4.2 Circuit Implementation

A monolithic 3-D magnetic field sensor array is designed in Stanford $2\mu m$ BiCMOS technology. The array uses the scanning method shown in Figure 4.3. The merged structure is used in both cell and processing circuits.

### 4.2.1 3-D Merged BiCMOS Magnetic Field Sensor Cell

The 3-D magnetic field sensor,which has been described in section 3.3 of last chapter, is used as individual cell to build up the array. The merged structure

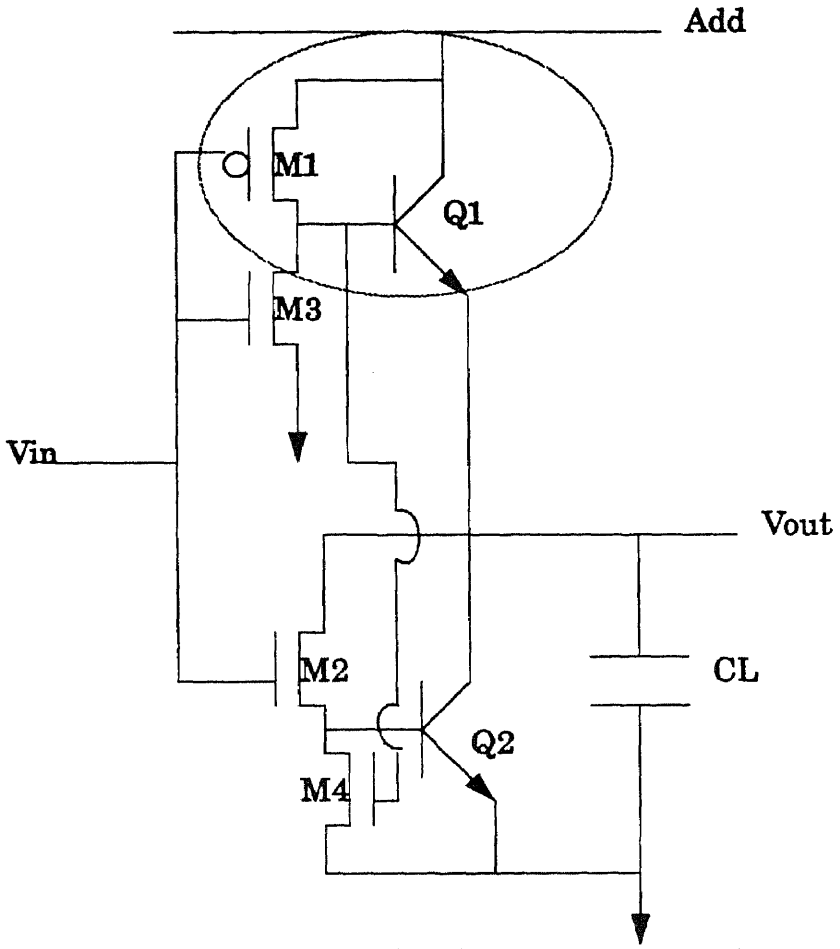



**Figure 4.5** The BiCMOS inverter with merged structure

has the advantage of less area, less external contacts and less parasitic capacitance. In Figure 3.17, the part inside the dash lines is the building block for the sensor array.

### 4.2.2 Complementary Merged BiCMOS Gate

The complementary merged structure is used in basic gate to build up the

whole scanning circuit, including the shift registers. It obtains bipolar drive capability with densities comparable to CMOS, and with much higher drive per

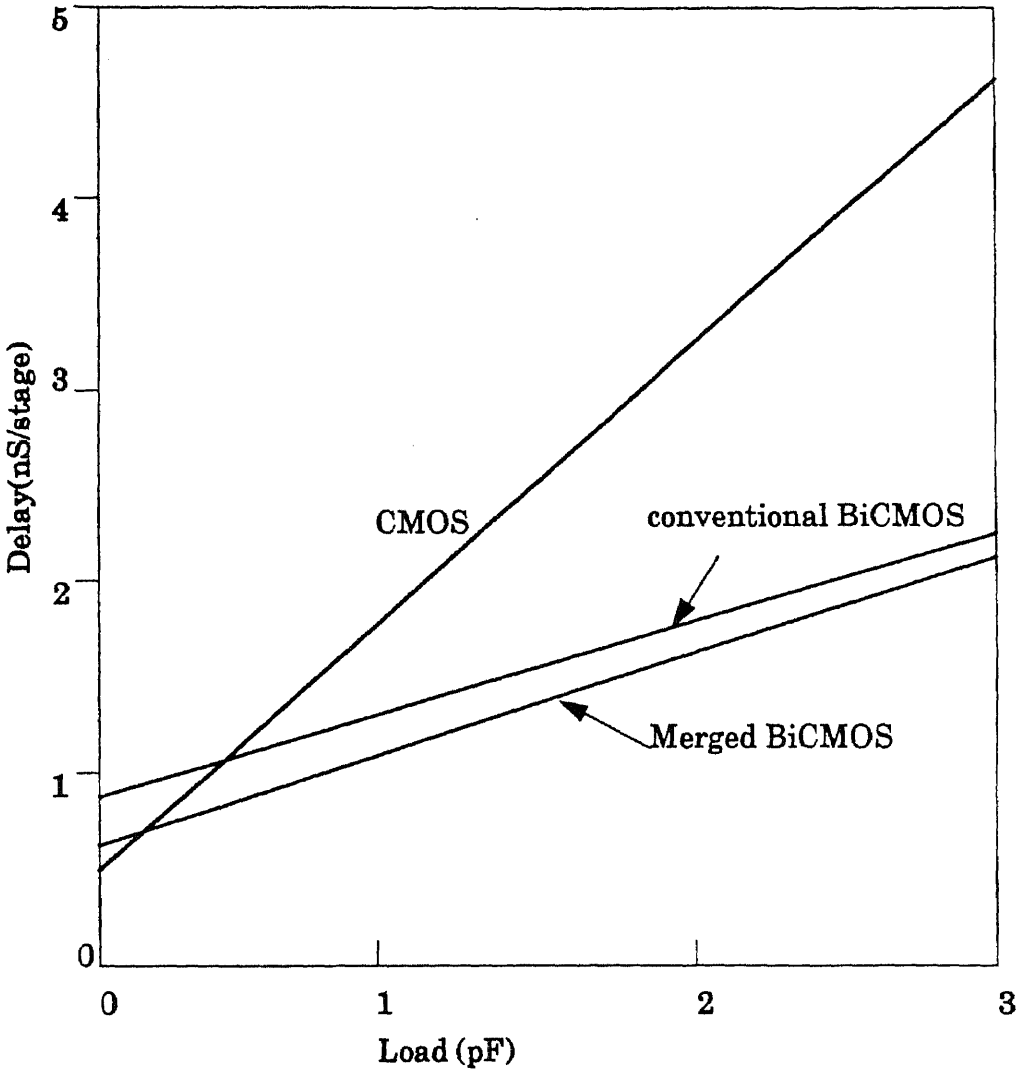



**Figure 4.6** Measured delay comparison[25]

unit area than either CMOS or standard, non-merged BiCMOS. Figure 4.5 shows the invert circuit. Circuit operation is as follows:

1) INPUT LOW: M1 is ON and supplies base current to turn Q1 ON. M2 and Q2 are OFF. output is HIGH;

2) INPUT HIGH: M2 is ON and supplies base current to turn Q2 ON. M3 is ON, pulling charge out of the base of Q1. M1 and Q1 are OFF. Output is LOW;

3) Transistor M1 and M2 supply base current to turn on Q1 and Q2;

4) Transistors M3 and M4 are not necessary for circuit operation. They are present to increase switching speed by pulling charge out of the bases of Q1 and Q2, respectively.

The merged structure schematics is inside the dash circle in Figure 4.5. The cross-section configuration of the merged structure which has already been shown in Figure 3.8(c), which is the most compact merged structure. The measured delay vs. load capacitance for CMOS, BiCMOS and merged BiCMOS gates are compared in Figure 4.6. In the Figure, the delay of the merged BiCMOS gate is slightly smaller than the non-merged one. This can be explained by the lower internal capacitance associated with the smaller structure. This difference in internal capacitance is insignificant if the measured load capacitance has much large values. Figure 4.7 compares simulated values of delay versus supply voltage for CMOS, BiCMOS and complementary merged BiCMOS gates in Stanford process with 0.5pF loads.

### 4.2.3 Dynamic Shift Register

The shift register used in the scanning system is the simple dynamic shift register , which use the merged BiCMOS inverters and transmission gates. The schematics is shown in Figure 4.8. The merged inverters (Figure 4.5) are connected by the transmission gates clocked with a 2-phase non-overlapping clock. Charge stored on the gates of the driver transistors hold the inverter output stage between the clock periods.

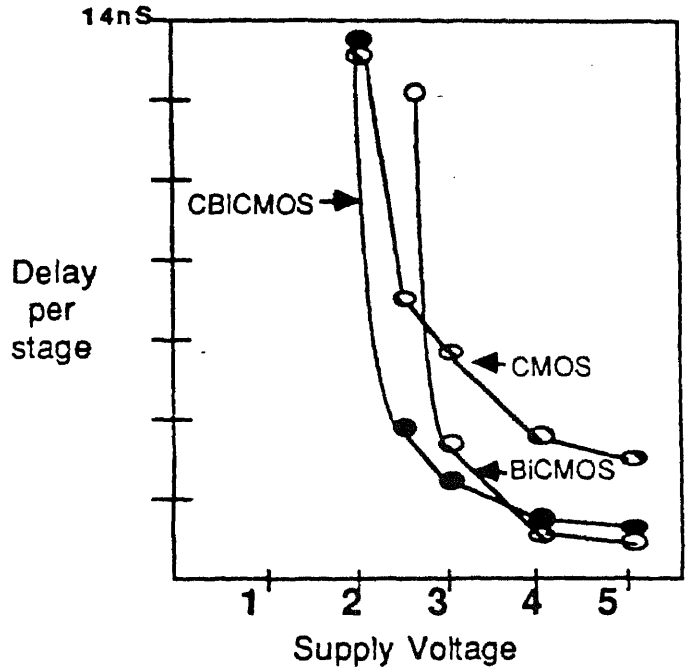



**Figure 4.7** Simulated delay comparison[25]

## 4.3 Layout

The layout of the $8 \times 8$ array has been carried out with MAGIC version6 by using Stanford $2\mu m$ BiCMOS technic file. The area of the array including the scanning circuits is about $1.2mm \times 1.3mm$, the total chip area including all pads is around $1.8mm \times 1.9mm$. A picture of the layout is shown in Figure 4.9.

## 4.4 SPICE Simulation

The SPICE simulations is used to analysis the system delay time, estimating the maximum clock rate. Most element of the system have been simulated. Details of simulation of the shift register built in merged BiCMOS technology

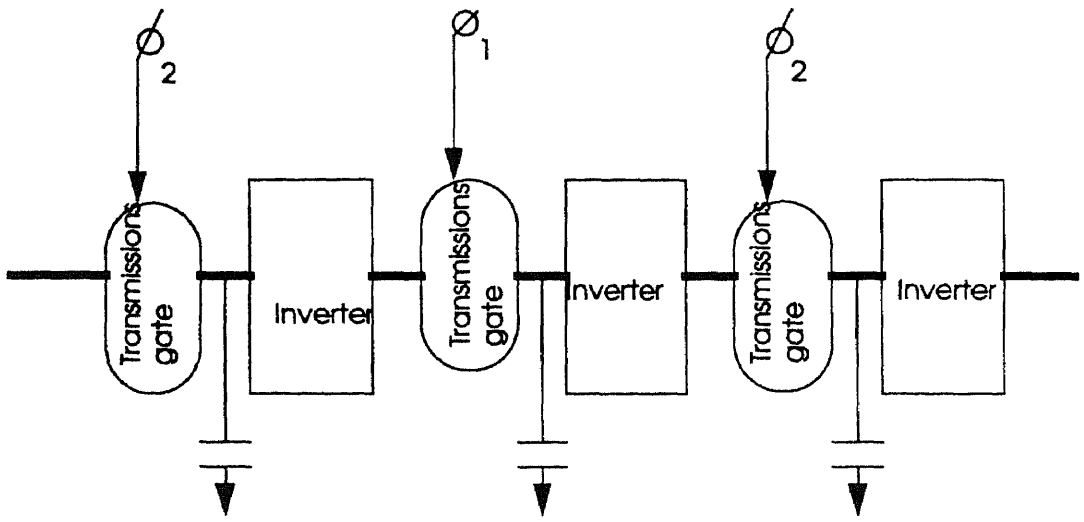



**Figure 4.8** Simple dynamic shift register

and critical path of the delay time of the whole system are described below. All the parasitic capacitors in our simulations are directly extracted from the layouts. The entire extracted files and SPICE input files are listed in the appendix.

### 4.4.1 Simulation of Shift Register

The single gate (inverter) in merged BiCMOS technology is first evaluated. The normal CMOS gate is also simulated for comparison. Both of them are shown in Figure 4.10. From this Figure, we can easily find that when both of these two gates are input with the same frequency pulse (T=10ns), the outputs signal clearly shows that the merged BiCMOS gate (Figure 4.5) can work in higher frquency.In the other words, the BiCMOS gate has much less delay than the CMOS one. This simulation result fits the measurement result very well (Figure 4.6). Note that the voltage difference between the input and output of merged BiCMOS gate( $V_{HI} - V_{HO}$) is due to the voltage drop of the base

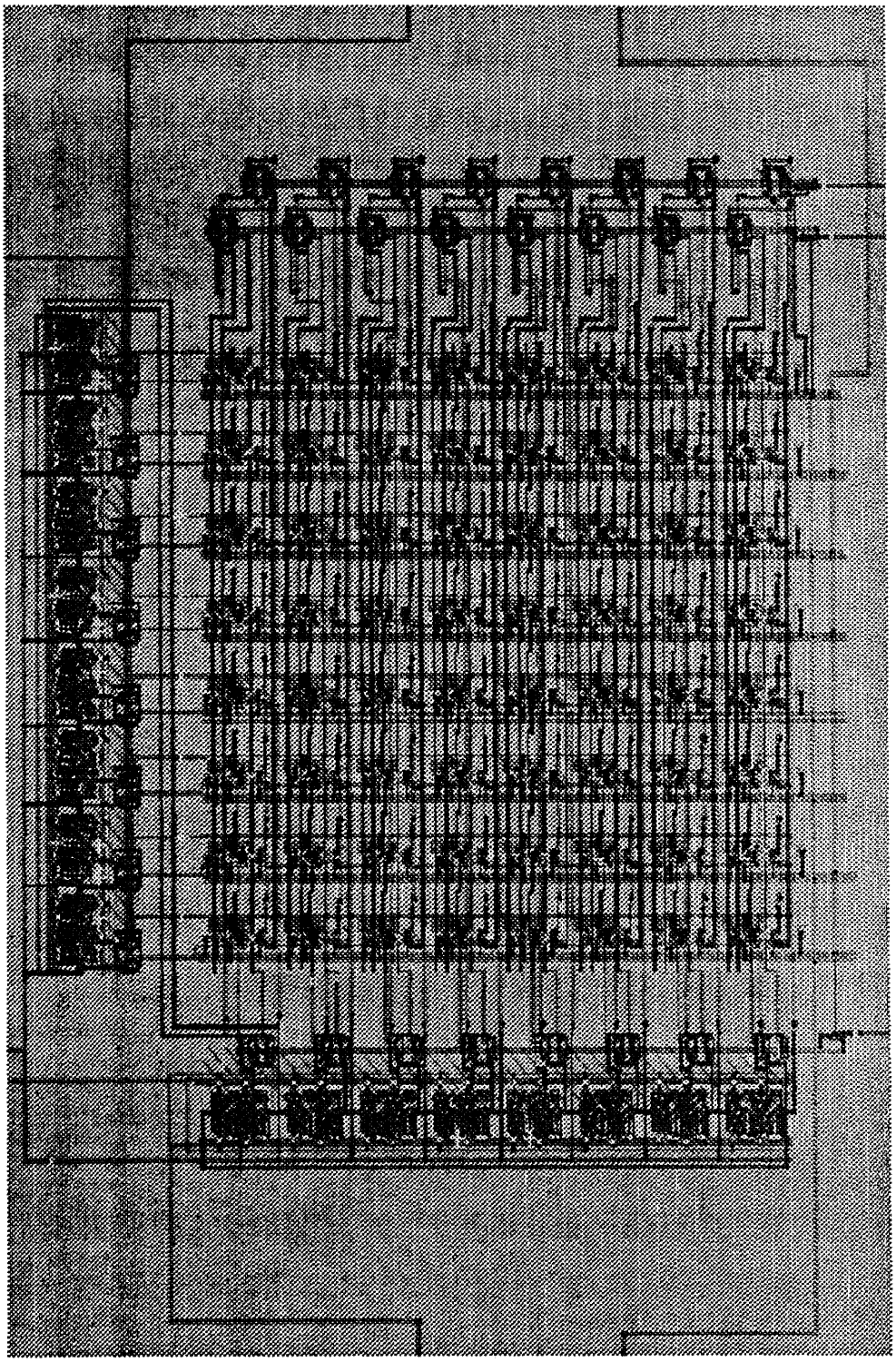
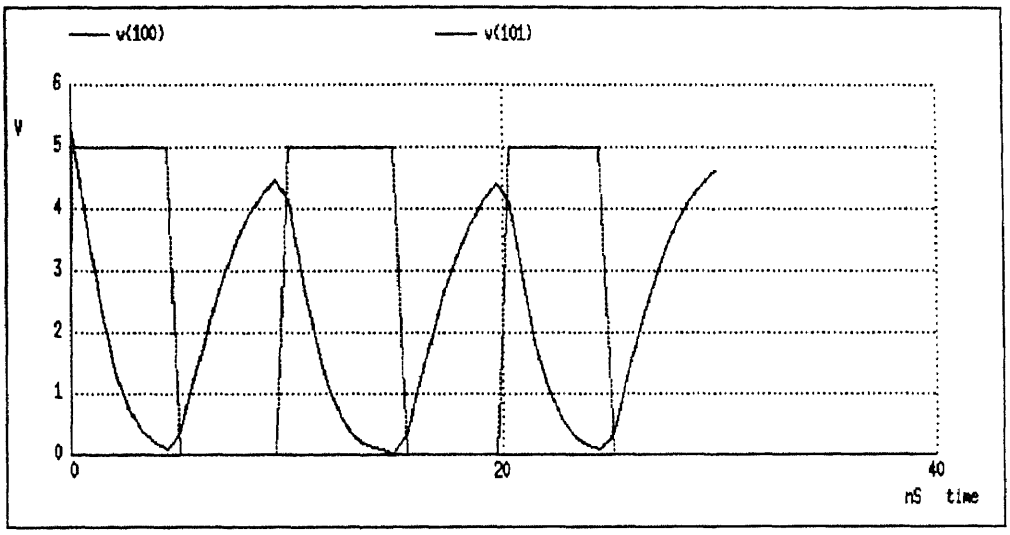
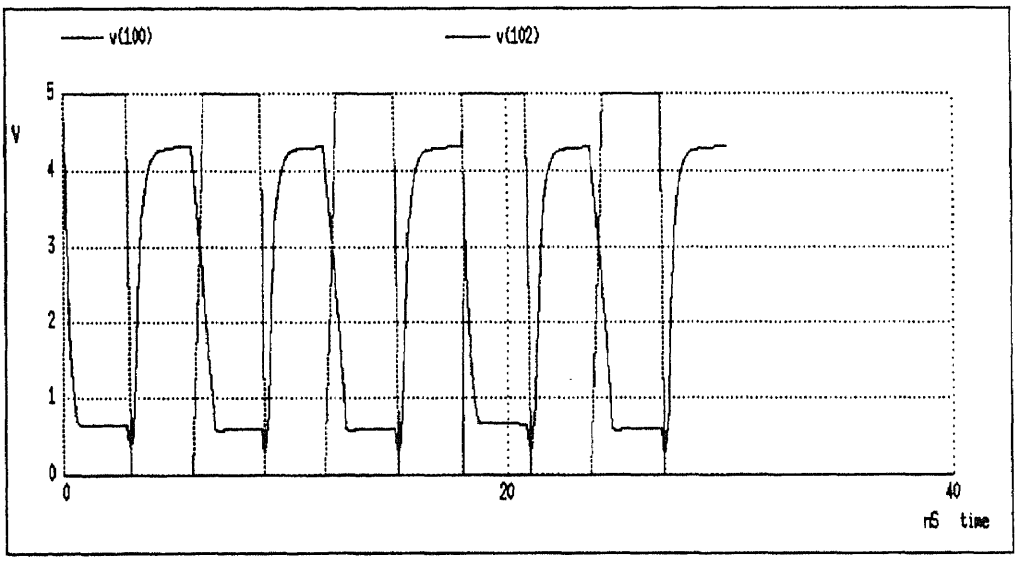


**Figure 4.9** The layout of the 8 x 8 sensor array




(a) CMOS gate: V(100) is input and V(101) is output




(b)BiCMOS gate: V(100) is input and V(102) is output

**Figure 4.10** The simulation comparison of CMOS and merged BiCMOS gates The BiCMOS gate can work under higher frequency with better output voltage waveshape

emitter junction of the bipolar transistor in the gate.

The dynamic shift register is composed of the merged BiCMOS gate and transmission gate. The simulation nodes are labeled in the shift register layout Figure

The SPICE simulation of the merged BiCMOS shift register is shown in

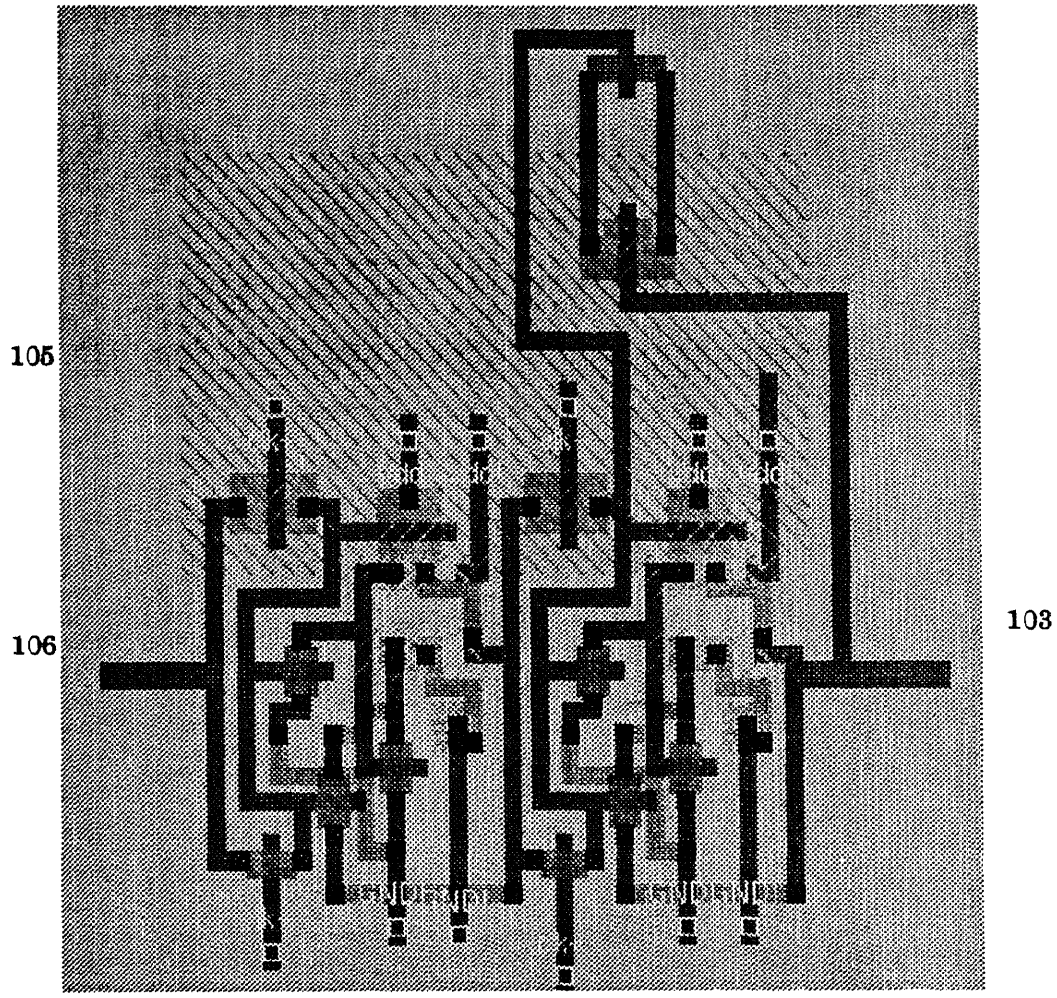



**Figure 4.11** the MAGIC layout of the merged BiCMOS shift register with nodes labeled for spice simulation. Node 106 is the input, node 105 and 110 are the clock signals, node 108 is the mid-stage voltage and node 103 is the output voltage.

Figure 4.10. From the Figure,we can see the output signal V(103) is one clock period delay to the input signal V(106), and the shift register can work properly under this clock frequency (T=6ns). The shift register array constitutes the row select and the column select circuits. We have also simulated the shift registers in chain. A two shift register chain is shown in Figure 4.11.

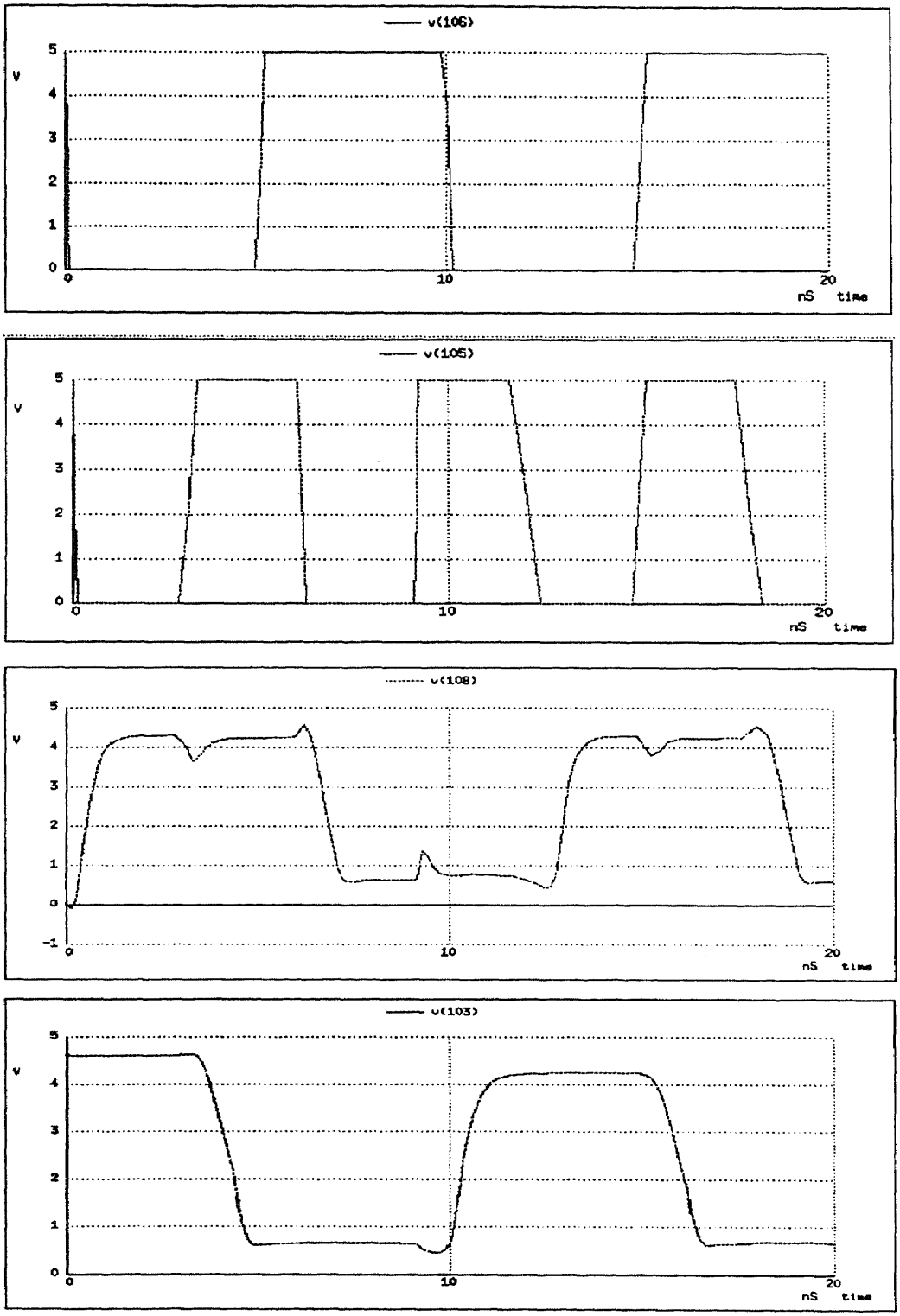



**Figure 4.12** SPICE simulation results for merged BiCMOS shift register shown in Figure 4.9.

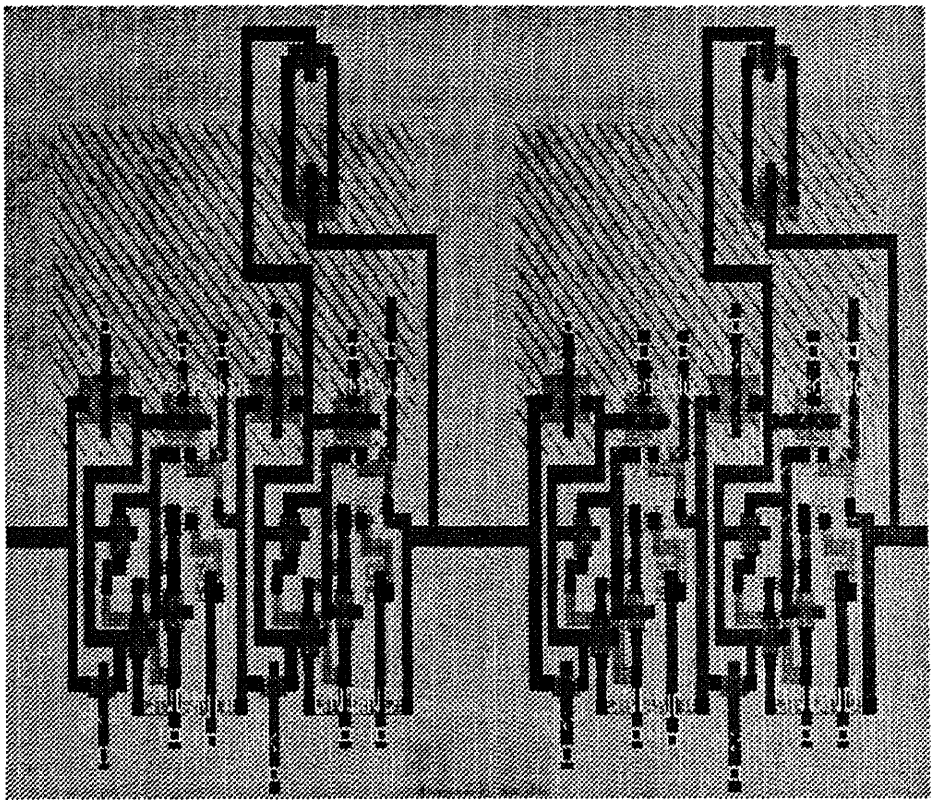



**Figure 4.13** Two shift registers in chain. Node 106 is the input, node 103 is the out put from first stage and input of second stage; Node 116 is the output of the second stage.

The SPICE simulation results is also shown in Figure 4.14.

At last, we make 8-stage ring counter as a row or column select circuit by employing the simulated merged BiCMOS shift registers. The complete input data files including the extracted file from MAGIC and adjusted simulation signals are listed in the appendix.

### 4.4.2 Simulation of the 3-D MFS Cell

The details about the simulation of the three dimension merged BiCMOS magnetic field sensor cell has already been done in section 3.4 of last chapter.

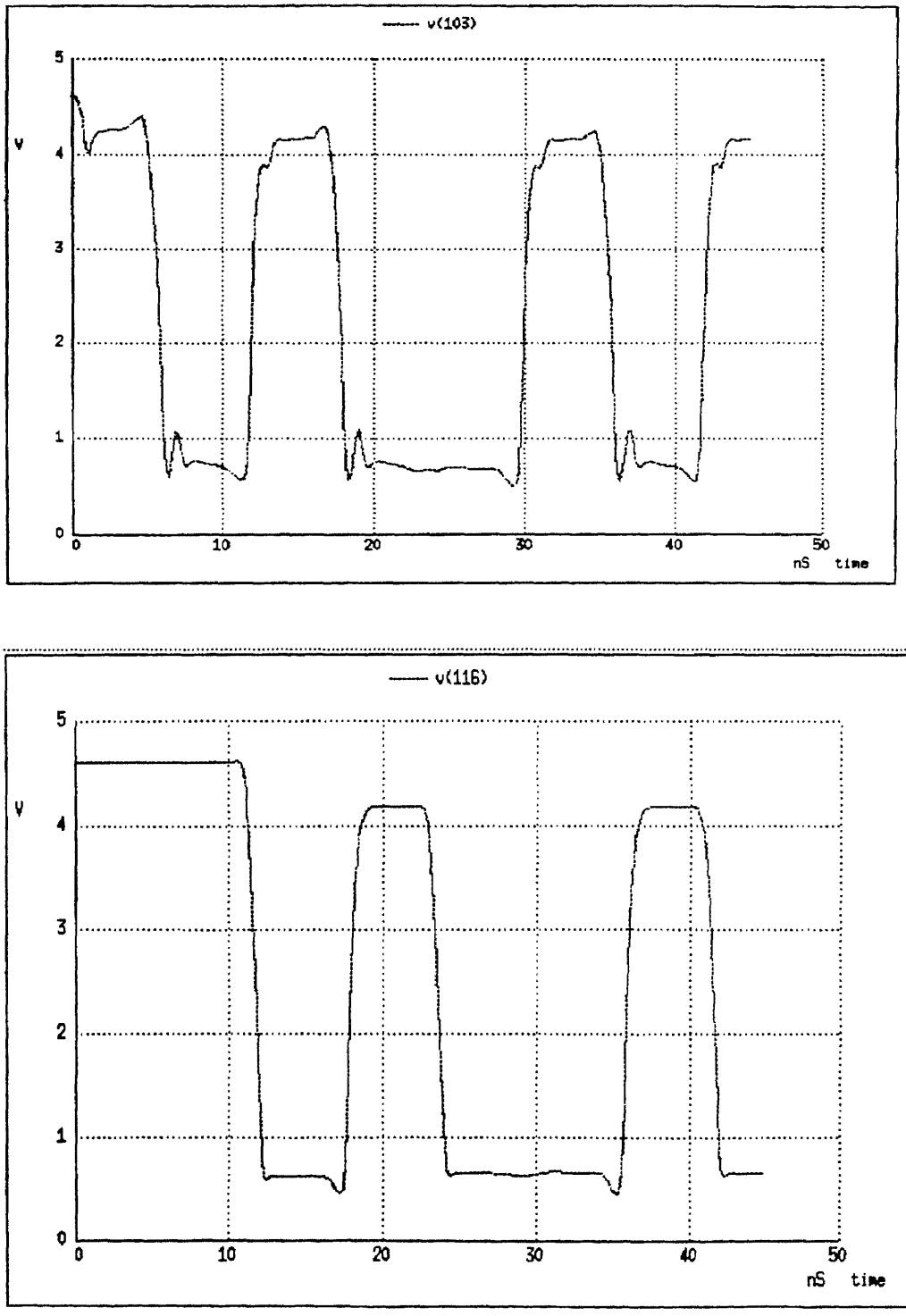



**Figure 4.14** Simulation result of Figure 4.13.

The simulation results together with the shifts register simulation results are used to analyze the whole system operation of the sensor array.

### 4.4.3 Simulation of the System Delay

The system operation has been detailed in the previous section. As we know, the system working frequency depends on the system delay time, which is expressed in equation (4.1). Not all the items in the equation (4.1) have the same importance in deciding the clock frequency. In the $8 \times 8$ sensor array, the scanning configuration of Figure 4.3 is used. From previous analysis in section 4.1, we have known that the bus delay is relatively bigger than others. So SPICE simulation is applied at the critical path of the bus delay. In fact, from the layout extract file ( please see the appendix on extract file of whole array system), we can notice that the parasitic capacitance of the buses are much larger than others, since the bus lines( metal or poly) are almost through out the entire chip.So from equation (4.1), we can see that the pixel clock rate is basically dependent on the critical path delay.

Now let us have a look on the delay times of the buses at different directions (X, Y and Z directions). From the extracted file, we find the bus capacitances of the three directions are identical in magnitude. That is because in chip layout, the buses in three directions are designed symmetrically. With the analysis in section 4.1, we know that the bus delay is dependent on the voltage change when one clock from one column to the next, and the parasitic capacitance of the column buses. Now the bus capacitances for X, Y and Z directions are almost same, so the critical delay is decided by the one of the directions which has the larger voltage shift.

From the SPICE simulation of the 3-D magnetic field sensor cell (section 3.3.6), we know that in Z direction, if the cell is selected, i.e. when the

transmissions gates in Z direction is on, the out put $V_Z$ is around 1.6473v (please refer to table 5 in last chapter); and when the cell is unselected, the voltage will be pulled up to V(3)=2.7v because no current is flowing through the MAGFET and no voltage drop between the source and drain of device (Figure 3.18 and Figure 4.4), so the voltage shifting is around 2.7-1.6=1.1v. Now consider the X and Y direction, when the cell is selected, the working voltage of output (connected to the buses) is 3.8997v, and when it's unselected, it drops to 2.7v. That means the voltage shifting between selected and unselected is 3.9 -2.7=1.2v, which is a little larger than that of Z direction.

From previous calculation, we can say the critical path is the delay in the X (or Y) direction.Our SPICE simulation is applied at this critical path of the array system. The circuit for simulation of X direction bus delay is shown in Figure 4.15.In this Figure, the capacitances of the buses in X direction Cbus1 and Cbus2 which is directly extracted from the whole array layout is included with the X outputs nodes. As easily referred with Figure 3.18, all the transistors and nodes are labeled with the same names as in Figure 3.18.The select transmission gates are also put in serie with the current mirrors. Nodes are labeled for simulation. Node 201 and node 200 are the clock signal.

The SPICE simulation results is shown in Figure 4.16. From the Figure, the rising edge of the output V(6) or V(7) is about $0.525\mu S$, and the falling edge is around $1.350\mu S$. The reason about why the rising delay is different as falling delay can be explained as below.

When the transmission gates are turned off from on, the voltage of the emitter of the magnetotransistor is pulled up ( Figure 4.16 V(10)). This results the magnetotransistor at a less active region as compared to when the cell is selected. So the dynamic resistor of the magnetotransistor comes up. Hence the RC discharging time constant becomes larger when the output voltage

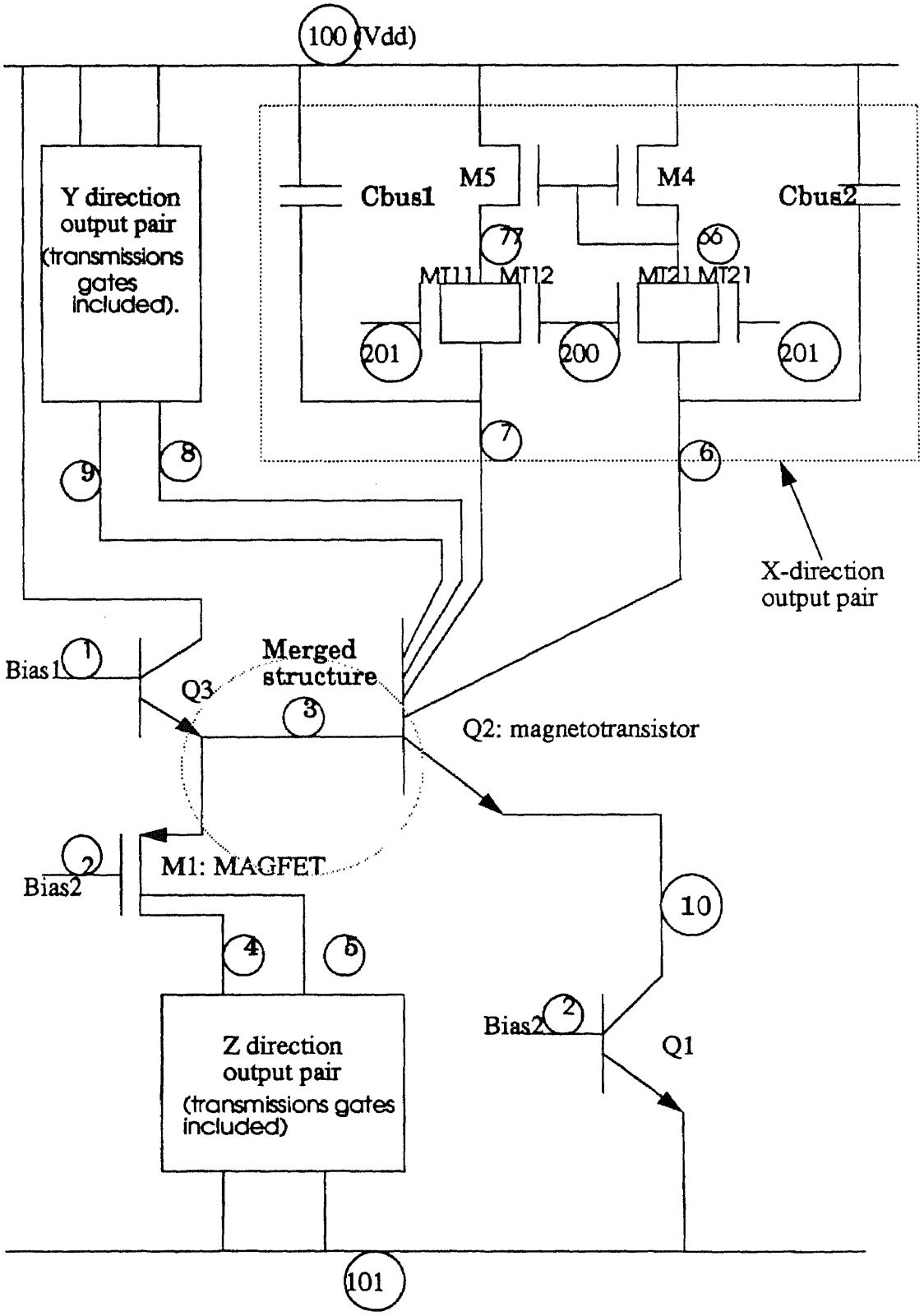



**Figure 4.15** Bus lines delay simulation circuitry

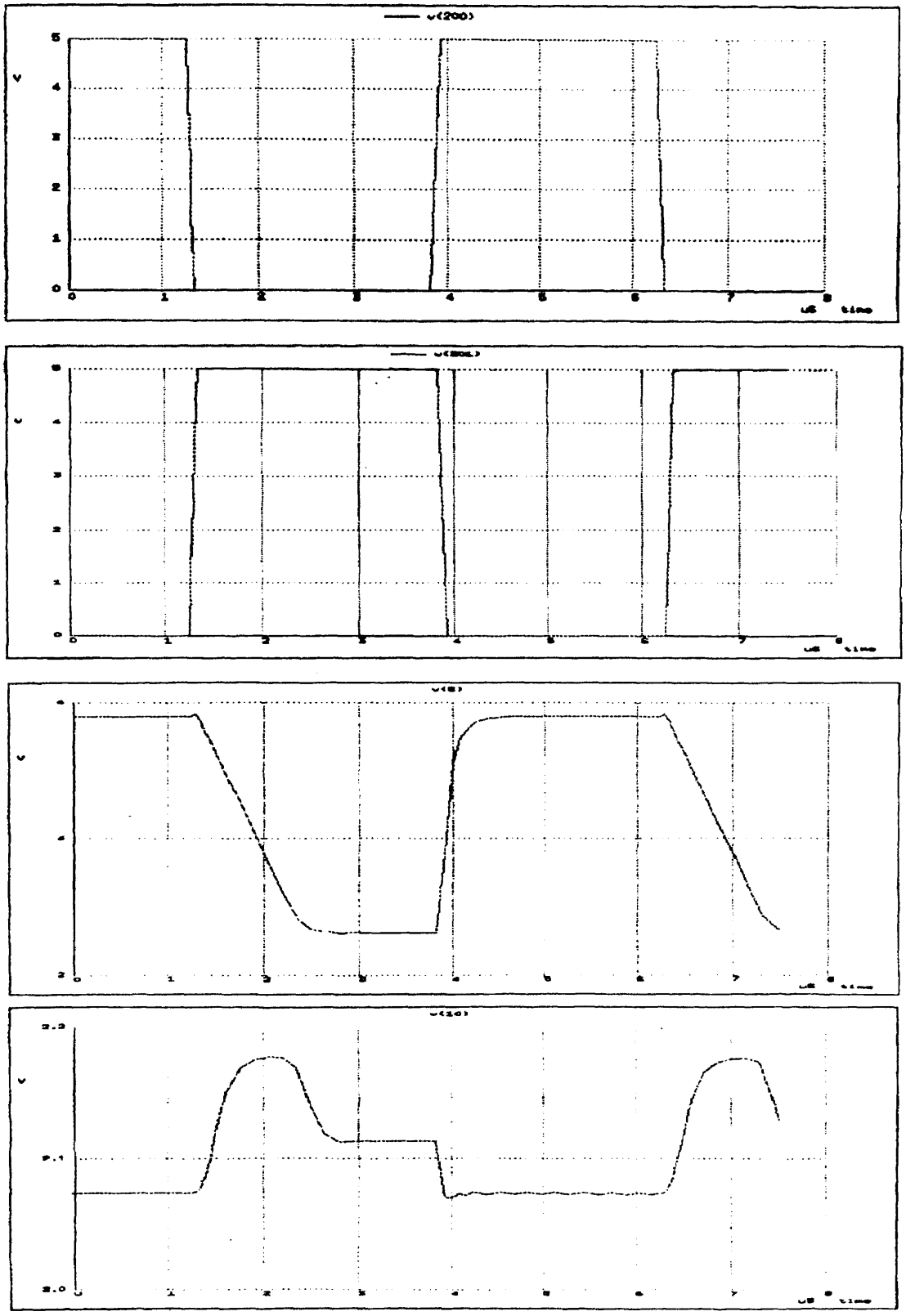


**Figure 4.16** The simulation results of system bus line s delay.

V(6) is discharged through Q2 and Q1.

When the transmissions gates are turned on from off. Both transistor Q2 and Q1 are in their deep saturation regions, in which they have very low dynamic resistance. Hence the output voltage can be charging up much quicker. As shown in Figure 4.16.

From the Figure, we can see the column selecting period is about $5\mu S$. The possible smallest working period is estimated from the falling and rising delays, which is: $T_{min} > 0.525 + 1.350 = 1.875\mu S$ Compared to equation (4.1), the other delay time items are omitted, since they are much smaller than the bus delay, as we have analysis detail in previous descriptions. In fact, from our previous simulation to the shift register(Figure 4.10) and 3-D magnetic field sensor cell (Figure 3.20), both of their delay time are in the range from $1 - 5nS$, which can be ignored while added up to the buses delay.

## 4.5 Application Examples

### 4.5.1 Example One: Position Sensing of A Robotic Arm

The first example of the designed 3-D merged BiCMOS magnetic field sensor array is using it as a position sensor in a robotic arm for precise manufacturing in a magnetic source environment which requires that the sensor system not only be capable of detecting absolute positions but also detecting very rapid position change, as usually called velocity. A schematics of the sensing system is shown in Figure 4.17.

The 3-D sensor array is fixed in the robotic arm for testing the strength of the magnetic field in three dimensions in a magnetic source environment. Since the strength of the field $\vec{B}$ is not same in the space, we can give a field distribution which is known to us, for example, $B(x, y, z)$. Then by the

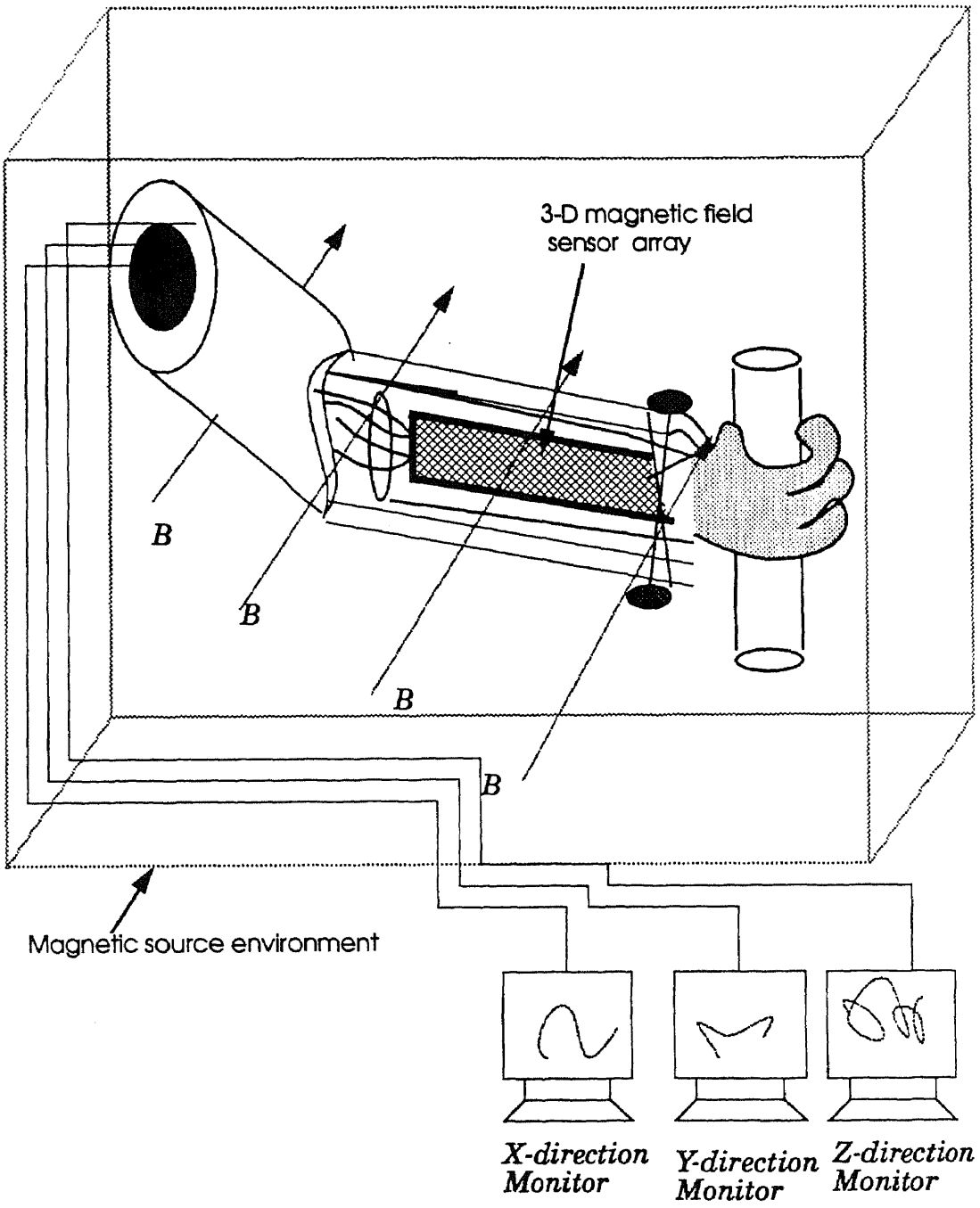



**Figure 4.17** Robotic Position Sensing System

detecting of the $\vec{B}$ in X, Y, and Z direction when the robotic arm is at a specific position, we can get the specific position of the arm. This sensing system can also easily give out the position change (velocity) of the moving robotic arm. Following is an example of testing the position change.

To simplify the situation, let us consider one dimension. The other dimensions is working in the same way. The sensing system weighting function is generally,

$$V(x, y, z) = f(B(x, y, z)) \tag{4.2}$$

Where, $f(B) = B - B_{thr}$ when $B \geq B_{thr}$; and $B = 0$ when $B < B_{thr}$. The $B_{thr}$ is the threshold value.

From our specific sensing system, assuming: 1) $B_{thr} = 0$; 2) the sensing weighting function is linear; and 3) The system has no cross-sensitivity, that is

$$V(x) = K_x B x \tag{4.3a}$$

$$V(y) = K_y B_y \tag{4.3b}$$

$$V(z) = K_z B_z \tag{4.3c}$$

Then Assuming a simple magnetic field distribution in the environment, for example an one dimension linear function, that is,

$$B(x, y, z) = B(x) = kx \tag{4.4a}$$

$$B(y) = B(z) = 0 \tag{4.4b}$$

From equation (4.4a) and (4.3a), we can have

$$V(x) = K_x k x = K x \tag{4.5}$$

We also assume the robot is moving only in X direction with a uniform velocity $v$ from a start point assumed $x_0 = 0$. At this time, we set the sensing array is scanned at a certain rate, for example, in 1 second, the whole sensor array is scanned 5 times(in practical, the scanning frequency could be much higher, up to the result which we have got from last section). Then the

waveshape appearing on the X-monitor should be as shown in Figure 4.18(c). One can know the velocity of the robotic arm's moving from the waveshape in the tracing monitor.

From monitor, one can reads out the voltages corresponding to the top value of any triangle and the 5th successive value, as labeled V1 and V2. so the voltage difference is got from $\Delta V = V1 - V2$. From equation (4.5), we have

$$\Delta V = V1 - V2 = Kx_1 - Kx_2 = K(x_1 - x_2) = K\Delta x \tag{4.6}$$

but as we know,

$$\Delta x = v\Delta \tag{4.7}$$

So we can get the average velocity between x1 to x2 is

$$v(average) = \frac{\Delta x}{\Delta t} = \frac{\Delta V}{K\Delta t} \tag{4.8}$$

Now let us see a general case: the robotic arm is moving at a radome velocity, that means the velocity at every time or position is different. At this time, we can apply a high frequency scanning signal to the sensor array. So in the monitor, we can see much more triangles between 1 second(Note, these triangle is not exactly same shape because the velocity is varying). When we apply more and more high frequency, every time interval $\Delta t$ is cut shorter and shorter. Now if we are asked to find the velocity at a specific time $t$, we just pick up two top values of the two points which is located near time $t$ (for example distance $0.5\Delta t$ for each) in the monitor, and read out the voltage values $V(t+0.5\Delta t)$ and $V(t-0.5\Delta t)$ for both point. As the time interval is cut small enough, i.e. if we use high enough scanning clock, we have

$$v(t) = \frac{\partial x}{\partial t} \cong \frac{\Delta x}{\Delta t} = \frac{\Delta V}{K\Delta t} = \frac{V(t+0.5\Delta t) - V(t-0.5\Delta t)}{K((t+0.5\Delta t) - (t-0.5\Delta t))} \tag{4.9}$$

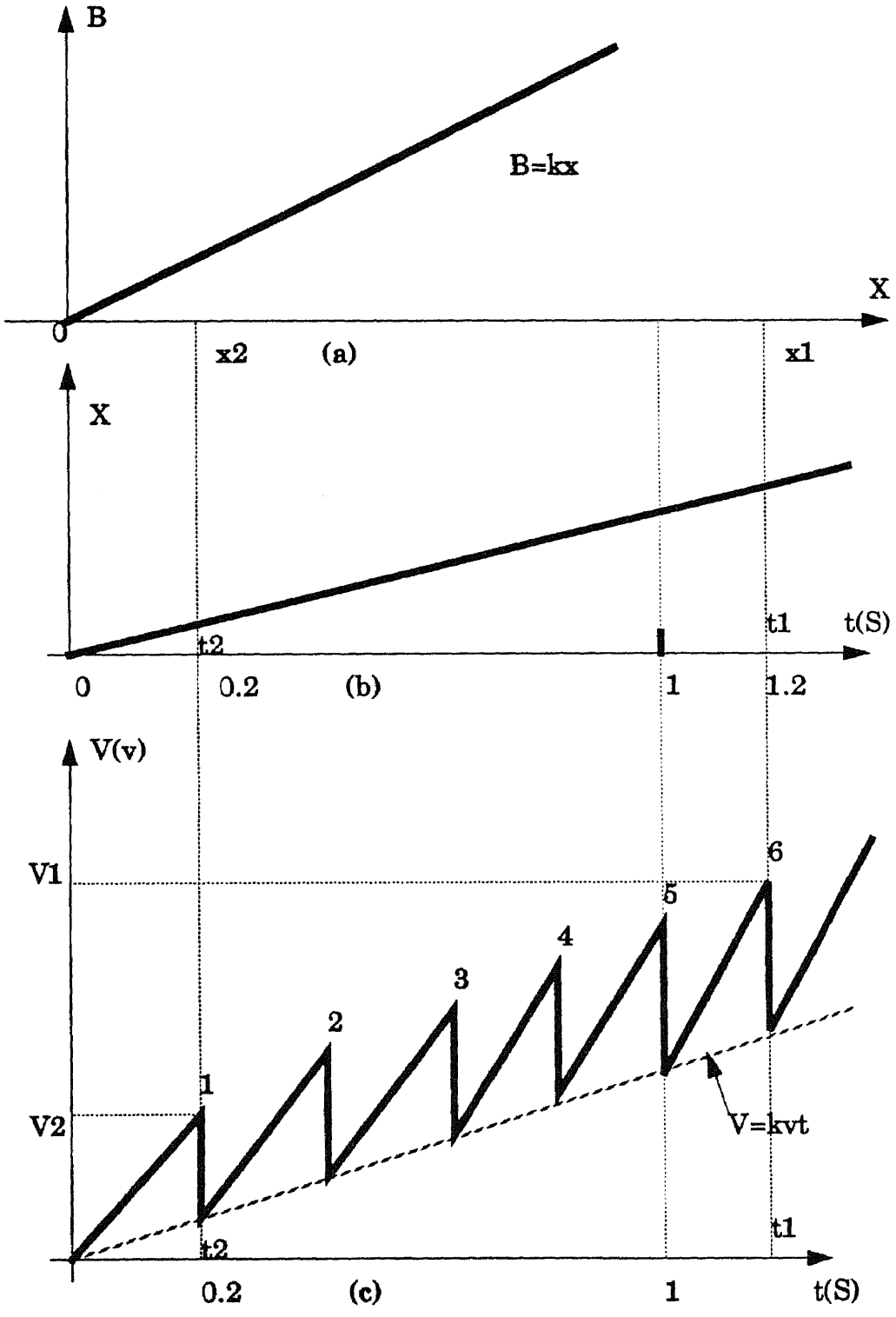



**Figure 4.18** Position change detecting, assuming the sensor array is scanned 5 time a second.

All the items in the right of (4.9) can be read out from the monitor. So we can easily know the real time velocity of any position when the robotic arm is moving in the magnetic field environment.

### 4.5.2 Example Two: Detecting Fringing Magnetic Field

Assuming magnetic field with $B\ (x, y, z, t) = B\sin wt$. This is the most simple and most useful case. From above equation, we know the fringing field is not a space function, but a Sin function of time. The Figure 4.19 shows how to use the sensor array to detect the field.

Set the scanning period $T = \frac{2\pi}{\omega}$, then from Figure 4.19,

$$X = vT = \frac{2\pi v}{\omega} \tag{4.10}$$

but we have assumed that the sensing weighting function is (4.3a), so

$$V = kB\ (t) = kB\sin\omega t = kB\sin\frac{2\pi t}{T} \tag{4.11}$$

In equation(4.11), T is the scanning period, and V is the readout voltage value from sensor array. So the value of B can be obtained.

If the fringing field is at frequency higher, we can have the following equation in general.

$$V = kB\sin\frac{2n\pi t}{T} \tag{4.12}$$

In general, if the B(x,y,z,t) is not a Sin function, we can use the Fourier function to expand it in the sum of a Sin function series. Then we can apply equation (4.12) to calculate out the $V = Bf(\frac{1}{T})$.

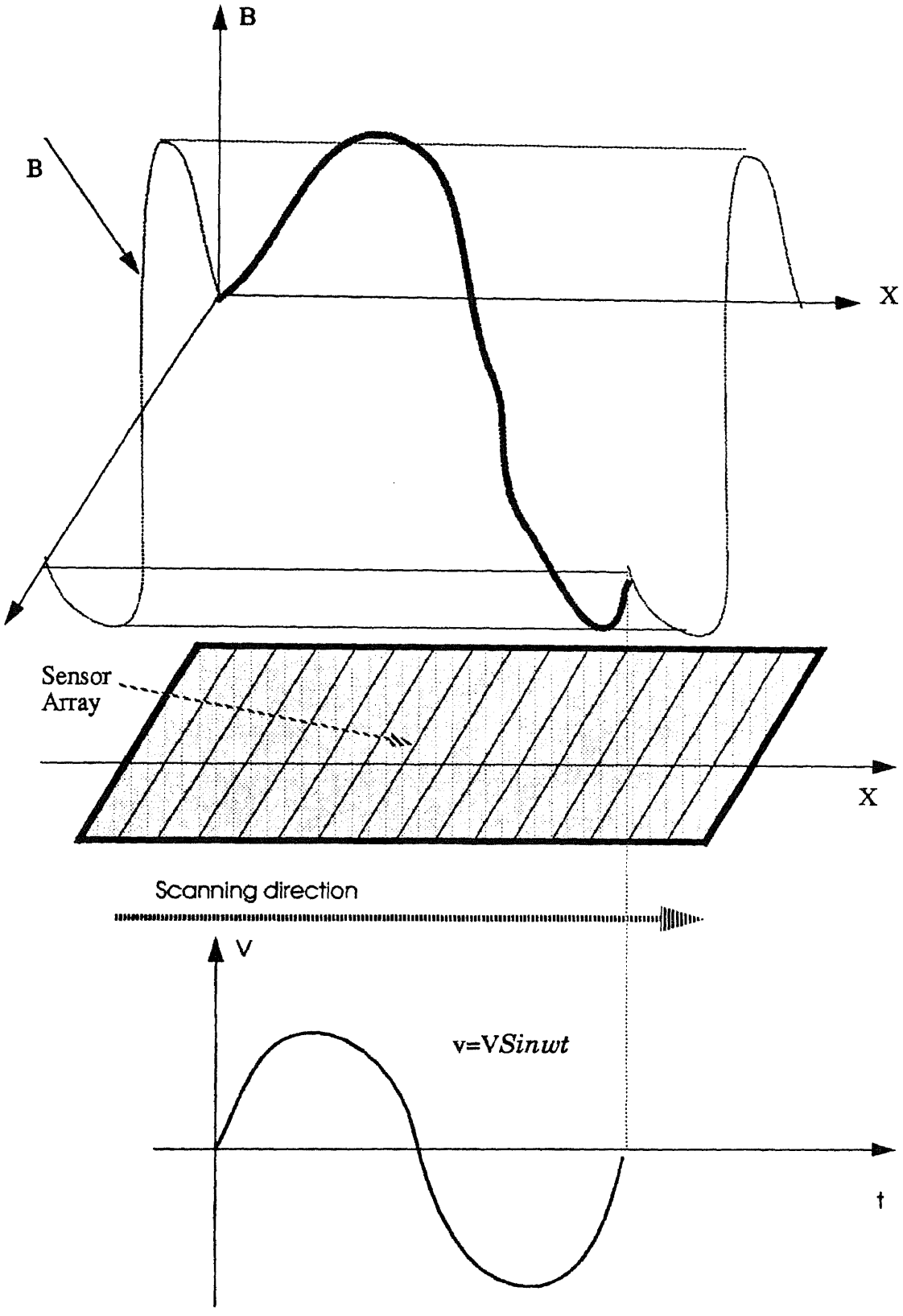



**Figure 4.19** Sensing array mapping fringing field

# CHAPTER 5
# SUMMARY AND CONCLUSION

A merged BiCMOS 3-D magnetic filed sensor has been designed. The detailed design of the merged structure by common diffusion as well as the high gain transduction circuit has been presented. The experiment results showing the sensitivity of a 3-D magnetic field sensor fabricated in Stanford BiCMOS technology has also been obtained. A new merged structure for magnetic sensor has the advantages of less area, less external contacts and less parasitic capacitance. This device can also eliminate a cross-sensitivity for different directions of the magnetic field. Device simulation package PISCESII has been used for device optimization. Appropriate bias conditions for operating the magnetic field sensor have been determined by SPICE simulation.

The sensitivity gain and frequency response have also been simulated. The simulation results show that when a relative change in current $\Delta I/I$ is 0.001, about $13.6mV$ and $8.5mV$ can be detected at the outputs in X(or Y) and Z directions, respectively. The working frequency can reach up to 1MHz.

A design has been made for a monolithic 8 by 8 array of the merged BiCMOS 3-D magnetic sensor cells. The array is scanned in a raster fashion by allowing current to flow through all elements in a given row, while all the other rows are turned off. Two scanning method has been developed. All the circuit of the array system are using BiCMOS technology. The detailed SPICE simulations has been applied on the main elements of the system and the critical paths. The maximum scanning clock speed is about 0.5MHz.

Two typical applications of the designed 3-D array have also been presented in the thesis. One is using the array as a position sensor for a

robotic arm in a magnetic source environment which requires to detect not only the absolute position but also very rapid position changes in three dimensions. The other is using the sensor array for mapping a fringing magnetic field.

The temperature dependence of the device has not been discussed and needs to be researched in the future work.

# APPENDIX

## A. PISCESII-B Input Files

### A.1 Non-merged 3-D MFS

```
*****************Simulation Structure Generation**************
title     DC npn with P-strip
options   tek
mesh      re  nx=39 ny=10 outf=npn.mesh0
x.m       n=1 l=0  r=1
x.m       n=39  l=39  r=1
y.m       n=1 l=0  r=1
y.m       n=10  l=10  r=1.0
region    num=1   ix.l=1 ix.h=39 iy.l=1 iy.h=10 silicon
elec      num=1  ix.l=2  ix.h=4  iy.l=1  iy.h=1
elec      num=2  ix.l=36  ix.h=38  iy.l=1  iy.h=1
elec      num=3  ix.l=10  ix.h=12  iy.l=1  iy.h=1
elec      num=4  ix.l=28 ix.h=30  iy.l=1  iy.h=1
elec      num=5  ix.l=19 ix.h=21 iy.l=1  iy.h=1
dop       unif   region=1 p.type conc=1e15 outf=d.0
dop       unif   region=1 n.type conc=1e17 y.top=0 y.bot=3
dop       gauss  conc=5e19   p.type
+         x.left=6  x.right=32 char=0.32
dop       gauss  conc=2e20    n.type
+         x.left=17 x.right=21 char=0.2
dop       gauss  conc=1e20   n.type
+         x.left=0 x.right=4 char=0.2
dop       gauss  conc=1e20   n.type
+         x.left=34.2 x.right=38 char=0.2
regrid    doping  log abs  step=1   smooth.k=1
+         outf=d.1  dopf=d.0
regrid    doping  log  abs ratio=3.6  smooth.k=1
+         outf=d.2  dopf=d.0
plot.2d   bound  no.top no.fill  pause
contour   doping  abs log min=17 max=21 del=0.5 pause
plot.1d  log abs dop x.start=0  x.end=38
+         y.start=0.0  y.end=0.0  points pause
plot.1d  log abs dop x.start=27  x.end=27
+         y.start=0  y.end=10  points pause
plot.1d  log abs dop x.start=35  x.end=35
+         y.start=0  y.end=10  points pause
plot.2d   bound grid  no.top no.fill pause
contour   doping  abs log  min=17  max=21
+          del=0.5  pause
options   plotdev=lw
plot.1d  log abs dop x.start=0  x.end=38
+         y.start=0.1  y.end=0.1  points outf=lw/n.dopla
plot.1d  log abs dop x.start=27  x.end=27
+         y.start=0  y.end=10  points outf=lw/n.dopvl
```

```
plot.1d  log abs dop x.start=35  x.end=35
+         y.start=0  y.end=10  points outf=lw/n.dopv2
end


*****************Ib-Vbe performence*****************************
title sensor-1D
mesh     inf=d.2
symb     gummel  carriers=2
method   iccg damped
mater    num=1
models   conmob temp=300 fldmob print
solve    init outf=n.iv0
symb     newton  carriers=2
method   autonr
log      outf=ivbe
solve    vstep=0.1 nstep=10 elect=34 outf=vbea
end


******************Ic-Vce  Performence************************
title sensor-1D
mesh     inf=d.2
symb     gummel  carriers=2
method   iccg damped
mater    num=1
models   conmob temp=300 fldmob print
load     inf=n.iv0
symb     newton  carriers=2
method   autonr
$solve    v3=1.11
load     inf=vbej
log      outf=niv2
solve    vstep=0.15 nstep=16 elect=12 outf=vcea
end
```

## A.2 3-D Merged BiCMOS sensor

```
***********Simulation  Structure generation***************
title      bicmos MFS
options     term=save
mesh        rect nx=26 ny=12 outf=bip.mesh0
x.m         n=1 l=0 r=1
x.m         n=26 l=25 r=1
y.m         n=1 l=-0.06 r=1
y.m         n=3 l=0 r=1
y.m         n=12 l=4 r=1
region      num=1 ix.l=1 ix.h=26 iy.l=1 iy.h=3 oxide
region      num=2 ix.l=1 ix.h=26 iy.l=3 iy.h=12 silicon

Comment     D=1 S=2 E=3 C=4 G=5
```

```
elec       num=1 ix.l=3 ix.h=4 iy.l=3 iy.h=3
elec       num=2 ix.l=10 ix.h=12 iy.l=3 iy.h=3
elec       num=3 ix.l=18 ix.h=19 iy.l=3 iy.h=3
elec       num=4 ix.l=24 ix.h=25 iy.l=3 iy.h=3
elec       num=5 ix.l=5 ix.h=9 iy.l=1 iy.h=1
dop        unif region=2 p.type conc=1e15 outf=d.0
dop        unif region=2 n.type conc=1e16 x.right=15 y.top=0 y.bot=3
dop        gauss conc=3e17 n.type char=1.0 x.left=15  y.top=0
dop        gauss conc=5e18 p.type char=0.5 x.left=9 x.right=21
dop        gauss conc=1e20 p.type char=0.1 x.right=5 y.top=0
dop        gauss conc=1e20 p.type char=0.1 x.left=9 x.right=14 y.top=0
dop        gauss conc=2e20 n.type char=0.1 x.left=17 x.right=19 y.top=0
dop        gauss conc=1e20 n.type char=0.1 x.left=23 x.right=25 y.top=0
regrid     doping log abs step=1 smooth.k=1 outf=d.1 dopf=d.0
regrid     doping log abs ratio=3.6 smooth.k=1 outf=d.2 dopf=d.0
$ Zero carrier poisson
$mater   num=2 g.surf=0.75
$models  conmob temp=300 fldmob
$symb    carriers=0
$solve init outf=zero_soln

$ plot.2d    bound no.top no.fill pause
$ contour    doping abs log min=17 max=21 del=0.5 pause
$  plot.1d    log abs dop x.start=0 x.end=26 y.start=0 y.end=0 points
pause
$ plot.1d    log abs dop x.start=2 x.end=2 y.start=0 y.end=8 points pause
$ plot.1d    log abs dop x.start=18 x.end=18 y.start=0 y.end=8 points
pause
 plot.1d    log abs dop x.start=11 x.end=11 y.start=0 y.end=8 points
pause
$ plot.2d    bound no.top no.fill pause
$ contour    doping abs log min=17.1 max=21 del=0.5 pause
$options    plotdev=psraw
$plot.1d    log abs dop x.start=0 x.end=26 y.start=0 y.end=0 points
$ plot.2d    bound  no.top no.fill
$ contour    doping abs log min=17.1 max=21 del=0.5
$plot.1d     log abs dop x.start=24 x.end=24 y.start=0 y.end=8 points
pause
end

***************Ib-Vbe Performence for NPN******
itle NPN
options term=save
mesh    inf=d.2
symb    gummel  carriers=2
method  iccg damped
mater   num=2 g.surf=0.75
models  conmob temp=300 fldmob print
solve   init outf=bimos.iv0
symb    newton  carriers=2
method  autonr
log     outf=ivbe
$solve   v3=0 outfile=bimos.iv1
$solve    v4=2.5 outfile=bimos.iv1
```

```
$solve    v1=5 outfile=bimos.iv2
$solve     v5=5 outfile=bimos.iv3
$solve    v4=0 outfile=bimos.iv1
solve   vstep=0.05 nstep=19 elect=2 outf=vbea
plot.1d  x.axis=v2 y.axis=i2

end

****************Ic-Vce Performence for NPN******************
options term=save
mesh    inf=d.2
symb    gummel  carriers=2
method  iccg damped
mater   num=1
models  conmob temp=300 fldmob print
load    inf=bimos.iv0
symb    newton  carriers=2
method  itlimit=60 autonr
$solve   v3=1.11
load    inf=vbes
log     outf=niv2
solve   vstep=0.15 nstep=30 elect=4 outf=vceja
$load    inf=vbei
$solve   vstep=0.1 nstep=25 elect=4 outf=vceia
plot.1d x.axis=v4 y.axis=i4
end

*****************PMOS gate characteristics***************
option term=save
mesh inf=d.2
symb gummel carriers=1 holes
method iccg damped
mater num=2 g.surf=0.75
contac num=5 p.poly
models conmob temp=300 fldmob print
solve init outfile=mos.iv0
$solve v2=5 outfile=mos.iv1
symb newton carriers=1 holes
method autonr
log outfile=ivgs
$solve v2=5 outfile=mos.iv1
solve v2=0 outfile=mos.iv1
solve v1=-0.2 outfile=mos.iv2
solve v5=-0.1 vstep=-0.25 nstep=20 electrode=5 outfile=vigsa
plot.1d x.axis=v5 y.axis=i2


end
*****************MOS Drain Chracteristics************************


title MOS
option term=save
```

```
mesh inf=d.2
symb gummel carriers=1 holes
method iccg damped
mater num=2 g.surf=0.75
contac num=1 p.poly
models conmob temp=300 fldmob print
load infile=mos.iv0
symb newton carriers=1 holes
method autonr
log outfile=ivdg
$solve v1=4.5 outfile=mos.iv1
$solve v2=5 outfile=mos.iv1
solve v1=-0.2 vstep=-0.2 nstep=15 electrode=1 outfile=vidga
plot.1d x.axis=v1 y.axis=i1

end
```

# B. SPICE Input Files

```
************Gate of MAGFET connected to Node 4**************
BICMOS MFS

Q3 100 1 3 NB4X2 AREA=0.5
M11 4 4 3 6 PM L=5U W=6U AD=20P AS=24P PD=18U PS=20U
M12 5 4 3 6 PM L=5U W=6U AD=20P AS=24P PD=18U PS=20P
M2 4  4 101 101  NM L=2U W=3U AD=14P AS=14P PD=15U PS=15U
M3 5  4 101 101 NM L=2U W=3U AD=14P AS=14P PD=15U PS=15U

Q1 10 2 101 NB4X2 AREA=0.5
Q21 6 3 10 NB4X2 AREA=2
Q22 7 3 10 NB4X2 AREA=2
Q23 8 3 10 NB4X2 AREA=2
Q24 9 3 10 NB4X2 AREA=2
M4 6 6 100 100 PM L=2U W=3U AD=14P AS=14P PD=15U PS=15U
M5 7 6 100 100 PM L=2U W=3U AD=14P AS=14P PD=15U PS=15U
M6 8 8 100 100 PM L=2U W=3U AD=14P AS=14P PD=15U PS=15U
M7 9 8 100 100 PM L=2U W=3U AD=14P AS=14P PD=15U PS=15U

VSS 101 0 0
VDD 100 0 5
VBIAS1 1 0 3.75
VBIAS2 2 0 0.78


C1 1 101 280F
C2 2 101 290F
C3 3 101  115F
C4 4 101 32F
C5 5 101 32F
C6 6 101 15F
C7 7 101 15F
C8 8 101 15F
C9 9 101 15F
C10 10 101 21F

*MODEL LIST
.MODEL NM NMOS
+ LEVEL = 2.000       VTO   = 0.5813      GAMMA = 0.4634
+ PHI   = 0.6000      TOX   = 2.5000E-08  NSUB  = 9.7303E+14
+ NFS   = 6.8755E+11  TPG   = 1.000       XJ    = 1.000E-06
+ LD    = 1.4366E-07  UO    = 477.0       UCRIT = 3.3885E+05
+ UEXP  = 0.2219      VMAX  = 6.7140E+04  NEFF  = 50.00
+ DELTA = 4.011
+ CJ    = 1.224E-4    CJSW  = 3.8024E-10  PB    = 0.5665
+ MJ    = 0.3956      MJSW  = 0.2631      FC = 0.5
+ CGDO  = 4.07E-10    CGSO  = 4.07E-10

.MODEL PM PMOS
+ LEVEL = 2.000       VTO   = -0.7407     GAMMA = 0.4583
+ PHI   = 0.6977      TOX   = 2.5000E-08  NSUB  = 5.3138E+14
```

```
+ NFS    = 4.2439E+11  XJ    = 4.3014E-08  LD    = 1.3396E-07
+ UO     = 1.687E+02   UCRIT = 2.8594E+05  UEXP  = 0.2601
+ VMAX   = 6.3062E+04  NEFF  = 8.494E+01   DELTA = 1.571
+ CJ     = 2.7077E-04  CJSW  = 3.1782E-10  PB    = 0.7329
+ MJ     = 0.4714      MJSW  = 0.3143      CGDO  = 4.55E-10
+ CGSO   =4.55E-10

.MODEL NB4X2 NPN ( IS=18.9E-18     BF=109.7     NF=1          VAF=27.84
+                  IKF=10.84M      ISE=22.5F    NE=1.739      BR=785.1M
+                  NR=1.136        VAR=1.381    IKR=67.76U    ISC=4.4E-18
+                  NC=1.033        RB=951
+                  RE=19           RC=860       EG=1.11
+                  XTI=3           VJE=1        MJE=0.5
+                  VJC=0.82        MJC=0.36     VJS=0.62      MJS=0.46
+                  CJE=30.8F       CJC=34.2F    CJS=16.1F    )


.MODEL PB4X2 PNP ( IS=18.9E-18     BF=109.7     NF=1          VAF=27.84
+                  IKF=10.84M      ISE=22.5F    NE=1.739      BR=785.1M
+                  NR=1.136        VAR=1.381    IKR=67.76U    ISC=4.4E-18
+                  NC=1.033        RB=951
+                  RE=19           RC=860       EG=1.11
+                  XTI=3           VJE=1        MJE=0.5
+                  VJC=0.82        MJC=0.36     VJS=0.62      MJS=0.46
+                  CJE=30.8F       CJC=34.2F    CJS=16.1F


.WIDTH OUT=80
*.PRINT V(1) v(2) V(3) V(4) V(5) V(6) V(6) V(7) V(8) V(9)
.OP
.END


 *****************Gate of MAGFET connected to Ground*********
BICMOS MFS

Q3 100 1 3 NB4X2 AREA=0.5
M11 1014 3 6 PM L=5U W=6U AD=20P AS=24P PD=18U PS=20U
M12 5 101  3 6 PM L=5U W=6U AD=20P AS=24P PD=18U PS=20P
M2 4  4 101 101  NM L=2U W=3U AD=14P AS=14P PD=15U PS=15U
M3 5  4 101 101 NM L=2U W=3U AD=14P AS=14P PD=15U PS=15U

Q1 10 2 101 NB4X2 AREA=0.5
Q21 6 3 10 NB4X2 AREA=2
Q22 7 3 10 NB4X2 AREA=2
Q23 8 3 10 NB4X2 AREA=2
Q24 9 3 10 NB4X2 AREA=2
M4 6 6 100 100 PM L=2U W=3U AD=14P AS=14P PD=15U PS=15U
M5 7 6 100 100 PM L=2U W=3U AD=14P AS=14P PD=15U PS=15U
M6 8 8 100 100 PM L=2U W=3U AD=14P AS=14P PD=15U PS=15U
M7 9 8 100 100 PM L=2U W=3U AD=14P AS=14P PD=15U PS=15U

VSS 101 0 0
VDD 100 0 5
```

```
VBIAS1 1 0 3.75
VBIAS2 2 0 0.78


C1 1 101 280F
C2 2 101 290F
C3 3 101  115F
C4 4 101 32F
C5 5 101 32F
C6 6 101 15F
C7 7 101 15F
C8 8 101 15F
C9 9 101 15F
C10 10 101 21F

*MODEL LIST
.MODEL NM NMOS
+ LEVEL = 2.000        VTO   = 0.5813      GAMMA = 0.4634
+ PHI   = 0.6000       TOX   = 2.5000E-08  NSUB  = 9.7303E+14
+ NFS   = 6.8755E+11   TPG   = 1.000       XJ    = 1.000E-06
+ LD    = 1.4366E-07   UO    = 477.0       UCRIT = 3.3885E+05
+ UEXP  = 0.2219       VMAX  = 6.7140E+04  NEFF  = 50.00
+ DELTA = 4.011
+ CJ    = 1.224E-4     CJSW  = 3.8024E-10  PB    = 0.5665
+ MJ    = 0.3956       MJSW  = 0.2631      FC = 0.5
+ CGDO  = 4.07E-10     CGSO  = 4.07E-10

.MODEL PM PMOS
+ LEVEL = 2.000        VTO   = -0.7407     GAMMA = 0.4583
+ PHI   = 0.6977       TOX   = 2.5000E-08  NSUB  = 5.3138E+14
+ NFS   = 4.2439E+11   XJ    = 4.3014E-08  LD    = 1.3396E-07
+ UO    = 1.687E+02    UCRIT = 2.8594E+05  UEXP  = 0.2601
+ VMAX  = 6.3062E+04   NEFF  = 8.494E+01   DELTA = 1.571
+ CJ    = 2.7077E-04   CJSW  = 3.1782E-10  PB    = 0.7329
+ MJ    = 0.4714       MJSW  = 0.3143      CGDO  = 4.55E-10
+ CGSO  =4.55E-10

.MODEL NB4X2 NPN ( IS=18.9E-18     BF=109.7     NF=1          VAF=27.84
+                  IKF=10.84M      ISE=22.5F    NE=1.739      BR=785.1M
+                  NR=1.136        VAR=1.381    IKR=67.76U    ISC=4.4E-18
+                  NC=1.033        RB=951
+                  RE=19           RC=860       EG=1.11
+                  XTI=3           VJE=1        MJE=0.5
+                  VJC=0.82        MJC=0.36     VJS=0.62      MJS=0.46
+                  CJE=30.8F       CJC=34.2F    CJS=16.1F    )


.MODEL PB4X2 PNP ( IS=18.9E-18     BF=109.7     NF=1          VAF=27.84
+                  IKF=10.84M      ISE=22.5F    NE=1.739      BR=785.1M
+                  NR=1.136        VAR=1.381    IKR=67.76U    ISC=4.4E-18
+                  NC=1.033        RB=951
+                  RE=19           RC=860       EG=1.11
+                  XTI=3           VJE=1        MJE=0.5
+                  VJC=0.82        MJC=0.36     VJS=0.62      MJS=0.46
```

```
+                CJE=30.8F       CJC=34.2F    CJS=16.1F


.WIDTH OUT=80
*.PRINT V(1) v(2) V(3) V(4) V(5) V(6) V(6) V(7) V(8) V(9)
.OP
.END


*****************gate of MAGFET connected to Bias2***********
BICMOS MFS

Q3 100 1 3 NB4X2 AREA=0.5
M11 4 2 3 6 PM L=5U W=6U AD=20P AS=24P PD=18U PS=20U
M12 5 2 3 6 PM L=5U W=6U AD=20P AS=24P PD=18U PS=20P
M2 4  4 101 101  NM L=2U W=3U AD=14P AS=14P PD=15U PS=15U
M2 5  4 101 101 NM L=2U W=3U AD=14P AS=14P PD=15U PS=15U

Q1 10 2 101 NB4X2 AREA=0.5
Q21 6 3 10 NB4X2 AREA=2
Q22 7 3 10 NB4X2 AREA=2
Q23 8 3 10 NB4X2 AREA=2
Q24 9 3 10 NB4X2 AREA=2
M4 6 6 100 100 PM L=2U W=3U AD=14P AS=14P PD=15U PS=15U
M5 7 6 100 100 PM L=2U W=3U AD=14P AS=14P PD=15U PS=15U
M6 8 8 100 100 PM L=2U W=3U AD=14P AS=14P PD=15U PS=15U
M7 9 8 100 100 PM L=2U W=3U AD=14P AS=14P PD=15U PS=15U

VSS 101 0 0
VDD 100 0 5
VBIAS1 1 0 3.75
VBIAS2 2 0 0.78


C1 1 101 280F
C2 2 101 290F
C3 3 101  115F
C4 4 101 32F
C5 5 101 32F
C6 6 101 15F
C7 7 101 15F
C8 8 101 15F
C9 9 101 15F
C10 10 101 21F

*MODEL LIST
.MODEL NM NMOS
+ LEVEL = 2.000        VTO   = 0.5813       GAMMA = 0.4634
+ PHI   = 0.6000       TOX   = 2.5000E-08   NSUB  = 9.7303E+14
+ NFS   = 6.8755E+11   TPG   = 1.000        XJ    = 1.000E-06
+ LD    = 1.4366E-07   UO    = 477.0        UCRIT = 3.3885E+05
+ UEXP  = 0.2219       VMAX  = 6.7140E+04   NEFF  = 50.00
+ DELTA = 4.011
```

```
+ CJ    = 1.224E-4    CJSW  = 3.8024E-10  PB    = 0.5665
+ MJ    = 0.3956      MJSW  = 0.2631      FC = 0.5
+ CGDO  = 4.07E-10    CGSO  = 4.07E-10

.MODEL PM PMOS
+ LEVEL = 2.000       VTO   = -0.7407     GAMMA = 0.4583
+ PHI   = 0.6977      TOX   = 2.5000E-08  NSUB  = 5.3138E+14
+ NFS   = 4.2439E+11  XJ    = 4.3014E-08  LD    = 1.3396E-07
+ UO    = 1.687E+02   UCRIT = 2.8594E+05  UEXP  = 0.2601
+ VMAX  = 6.3062E+04  NEFF  = 8.494E+01   DELTA = 1.571
+ CJ    = 2.7077E-04  CJSW  = 3.1782E-10  PB    = 0.7329
+ MJ    = 0.4714      MJSW  = 0.3143      CGDO  = 4.55E-10
+ CGSO  =4.55E-10

.MODEL NB4X2 NPN ( IS=18.9E-18     BF=109.7     NF=1          VAF=27.84
+                  IKF=10.84M      ISE=22.5F    NE=1.739      BR=785.1M
+                  NR=1.136        VAR=1.381    IKR=67.76U    ISC=4.4E-18
+                  NC=1.033        RB=951
+                  RE=19           RC=860       EG=1.11
+                  XTI=3           VJE=1        MJE=0.5
+                  VJC=0.82        MJC=0.36     VJS=0.62      MJS=0.46
+                  CJE=30.8F       CJC=34.2F    CJS=16.1F    )


.MODEL PB4X2 PNP ( IS=18.9E-18     BF=109.7     NF=1          VAF=27.84
+                  IKF=10.84M      ISE=22.5F    NE=1.739      BR=785.1M
+                  NR=1.136        VAR=1.381    IKR=67.76U    ISC=4.4E-18
+                  NC=1.033        RB=951
+                  RE=19           RC=860       EG=1.11
+                  XTI=3           VJE=1        MJE=0.5
+                  VJC=0.82        MJC=0.36     VJS=0.62      MJS=0.46
+                  CJE=30.8F       CJC=34.2F    CJS=16.1F


.WIDTH OUT=80
*.PRINT V(1) v(2) V(3) V(4) V(5) V(6) V(6) V(7) V(8) V(9)
.OP
.END


**************Gain Simulation of the cell************************
BICMOS MFS

Q3 100 1 3 NB4X2 AREA=0.5
M11 4 101 3 6 PM L=5U W=6.001U AD=20P AS=24P PD=18U PS=20U
M12 5 101 3 6 PM L=5U W=5.999U AD=20P AS=24P PD=18U PS=20P
M2 4 4 101 101  NM L=2U W=3U AD=14P AS=14P PD=15U PS=15U
M3 5 4 101 101 NM L=2U W=3U AD=14P AS=14P PD=15U PS=15U

Q1 10 2 101 NB4X2 AREA=0.5
Q21 6 3 10 NB4X2 AREA=2
Q22 7 3 10 NB4X2 AREA=2
Q23 8 3 10 NB4X2 AREA=2
Q24 9 3 10 NB4X2 AREA=2
```

```
M4 6 6 100 100 PM L=2U W=3U AD=14P AS=14P PD=15U PS=15U
M5 7 6 100 100 PM L=2U W=3U AD=14P AS=14P PD=15U PS=15U
M6 8 8 100 100 PM L=2U W=3U AD=14P AS=14P PD=15U PS=15U
M7 9 8 100 100 PM L=2U W=3U AD=14P AS=14P PD=15U PS=15U

VSS 101 0 0
VDD 100 0 5
VBIAS1 1 0 3.23
VBIAS2 2 0 0.78

C1 1 101 280F
C2 2 101 290F
C3 3 101  115F
C4 4 101 32F
C5 5 101 32F
C6 6 101 15F
C7 7 101 15F
C8 8 101 15F
C9 9 101 15F
C10 10 101 21F



*MODEL LIST
.MODEL NM NMOS
+ LEVEL = 2.000        VTO   = 0.5813      GAMMA = 0.4634
+ PHI   = 0.6000       TOX   = 2.5000E-08  NSUB  = 9.7303E+14
+ NFS   = 6.8755E+11   TPG   = 1.000       XJ    = 1.000E-06
+ LD    = 1.4366E-07   UO    = 477.0       UCRIT = 3.3885E+05
+ UEXP  = 0.2219       VMAX  = 6.7140E+04  NEFF  = 50.00
+ DELTA = 4.011
+ CJ    = 1.224E-4     CJSW  = 3.8024E-10  PB    = 0.5665
+ MJ    = 0.3956       MJSW  = 0.2631      FC = 0.5
+ CGDO  = 4.07E-10     CGSO  = 4.07E-10

.MODEL PM PMOS
+ LEVEL = 2.000        VTO   = -0.7407     GAMMA = 0.4583
+ PHI   = 0.6977       TOX   = 2.5000E-08  NSUB  = 5.3138E+14
+ NFS   = 4.2439E+11   XJ    = 4.3014E-08  LD    = 1.3396E-07
+ UO    = 1.687E+02    UCRIT = 2.8594E+05  UEXP  = 0.2601
+ VMAX  = 6.3062E+04   NEFF  = 8.494E+01   DELTA = 1.571
+ CJ    = 2.7077E-04   CJSW  = 3.1782E-10  PB    = 0.7329
+ MJ    = 0.4714       MJSW  = 0.3143      CGDO  = 4.55E-10
+ CGSO  =4.55E-10

.MODEL NB4X2 NPN ( IS=18.9E-18     BF=109.7     NF=1          VAF=27.84
+                  IKF=10.84M      ISE=22.5F    NE=1.739      BR=785.1M
+                  NR=1.136        VAR=1.381    IKR=67.76U    ISC=4.4E-18
+                  NC=1.033        RB=951
+                  RE=19           RC=860       EG=1.11
+                  XTI=3           VJE=1        MJE=0.5
+                  VJC=0.82        MJC=0.36     VJS=0.62      MJS=0.46
```

```
+                  CJE=30.8F       CJC=34.2F     CJS=16.1F    )


.MODEL PB4X2 PNP ( IS=18.9E-18     BF=109.7      NF=1          VAF=27.84
+                  IKF=10.84M      ISE=22.5F     NE=1.739      BR=785.1M
+                  NR=1.136        VAR=1.381     IKR=67.76U    ISC=4.4E-18
+                  NC=1.033        RB=951
+                  RE=19           RC=860        EG=1.11
+                  XTI=3           VJE=1         MJE=0.5
+                  VJC=0.82        MJC=0.36      VJS=0.62      MJS=0.46
+                  CJE=30.8F       CJC=34.2F     CJS=16.1F


.WIDTH OUT=80
*.PRINT V(1) v(2) V(3) V(4) V(5) V(6) V(6) V(7) V(8) V(9)
.OP
.END



******************Frequency Response of the cell**************
BICMOS MFS

Q3 100 1 3 NB4X2 AREA=0.5
M11 4 101 3 6 PM L=5U W=6U AD=20P AS=24P PD=18U PS=20U
M12 5 11 3 6 PM L=5U W=6U AD=20P AS=24P PD=18U PS=20P
M2 44 44 101 101  NM L=2U W=3U AD=14P AS=14P PD=15U PS=15U
M3 55 44 101 101 NM L=2U W=3U AD=14P AS=14P PD=15U PS=15U

Q1 10 2 101 NB4X2 AREA=0.5
Q21 6 3 10 NB4X2 AREA=2
Q22 7 3 10 NB4X2 AREA=2
Q23 8 3 10 NB4X2 AREA=2
Q24 9 3 10 NB4X2 AREA=2
M4 6 6 100 100 PM L=2U W=3U AD=14P AS=14P PD=15U PS=15U
M5 7 6 100 100 PM L=2U W=3U AD=14P AS=14P PD=15U PS=15U
M6 8 8 100 100 PM L=2U W=3U AD=14P AS=14P PD=15U PS=15U
M7 9 8 100 100 PM L=2U W=3U AD=14P AS=14P PD=15U PS=15U

VSS 101 0 0
VDD 100 0 5
VBIAS1 1 0 3.23
VBIAS2 2 0 0.78
V55 55 5 0
V44 4 44 0

VIN 11 101 SIN(0 0.1 10K)

C1 1 101 280F
C2 2 101 290F
C3 3 101  115F
C4 4 101 32F
```

```
C5 5 101 32F
C6 6 101 15F
C7 7 101 15F
C8 8 101 15F
C9 9 101 15F
C10 10 101 21F



*MODEL LIST
.MODEL NM NMOS
+ LEVEL = 2.000        VTO   = 0.5813      GAMMA = 0.4634
+ PHI   = 0.6000       TOX   = 2.5000E-08  NSUB  = 9.7303E+14
+ NFS   = 6.8755E+11   TPG   = 1.000       XJ    = 1.000E-06
+ LD    = 1.4366E-07   UO    = 477.0       UCRIT = 3.3885E+05
+ UEXP  = 0.2219       VMAX  = 6.7140E+04  NEFF  = 50.00
+ DELTA = 4.011
+ CJ    = 1.224E-4     CJSW  = 3.8024E-10  PB    = 0.5665
+ MJ    = 0.3956       MJSW  = 0.2631      FC = 0.5
+ CGDO  = 4.07E-10     CGSO  = 4.07E-10

.MODEL PM PMOS
+ LEVEL = 2.000        VTO   = -0.7407     GAMMA = 0.4583
+ PHI   = 0.6977       TOX   = 2.5000E-08  NSUB  = 5.3138E+14
+ NFS   = 4.2439E+11   XJ    = 4.3014E-08  LD    = 1.3396E-07
+ UO    = 1.687E+02    UCRIT = 2.8594E+05  UEXP  = 0.2601
+ VMAX  = 6.3062E+04   NEFF  = 8.494E+01   DELTA = 1.571
+ CJ    = 2.7077E-04   CJSW  = 3.1782E-10  PB    = 0.7329
+ MJ    = 0.4714       MJSW  = 0.3143      CGDO  = 4.55E-10
+ CGSO  =4.55E-10

.MODEL NB4X2 NPN ( IS=18.9E-18     BF=109.7     NF=1          VAF=27.84
+                  IKF=10.84M      ISE=22.5F    NE=1.739      BR=785.1M
+                  NR=1.136        VAR=1.381    IKR=67.76U    ISC=4.4E-18
+                  NC=1.033        RB=951
+                  RE=19           RC=860       EG=1.11
+                  XTI=3           VJE=1        MJE=0.5
+                  VJC=0.82        MJC=0.36     VJS=0.62      MJS=0.46
+                  CJE=30.8F       CJC=34.2F    CJS=16.1F    )


.MODEL PB4X2 PNP ( IS=18.9E-18     BF=109.7     NF=1          VAF=27.84
+                  IKF=10.84M      ISE=22.5F    NE=1.739      BR=785.1M
+                  NR=1.136        VAR=1.381    IKR=67.76U    ISC=4.4E-18
+                  NC=1.033        RB=951
+                  RE=19           RC=860       EG=1.11
+                  XTI=3           VJE=1        MJE=0.5
+                  VJC=0.82        MJC=0.36     VJS=0.62      MJS=0.46
+                  CJE=30.8F       CJC=34.2F    CJS=16.1F
```

```
.PLOT AC V(5)
.TRAN 10US 200US
.PLOT AC V(5)
.WIDTH OUT=80
.PRINT V(1) v(2) V(3) V(4) V(5) V(6) V(6) V(7) V(8) V(9)
.OP
.END


**********Merged BiCMOS Shift Register **********
*spice simulation of the merged BiCMOS shift register
*model LIST
.model NFET NMOS
+ LEVEL = 2.000        VTO   = 0.5813      GAMMA = 0.4634
+ PHI   = 0.6000       TOX   = 2.5000E-08  NSUB  = 9.7303E+14
+ NFS   = 6.8755E+11   TPG   = 1.000       XJ    = 1.000E-06
+ LD    = 1.4366E-07   UO    = 477.0       UCRIT = 3.3885E+05
+ UEXP  = 0.2219       VMAX  = 6.7140E+04  NEFF  = 50.00
+ DELTA = 4.011
+ CJ    = 1.224E-4     CJSW  = 3.8024E-10  PB    = 0.5665
+ MJ    = 0.3956       MJSW  = 0.2631      FC = 0.5
+ CGDO  = 4.07E-10     CGSO  = 4.07E-10

.model PFET PMOS
+ LEVEL = 2.000        VTO   = -0.7407     GAMMA = 0.4583
+ PHI   = 0.6977       TOX   = 2.5000E-08  NSUB  = 5.3138E+14
+ NFS   = 4.2439E+11   XJ    = 4.3014E-08  LD    = 1.3396E-07
+ UO    = 1.687E+02    UCRIT = 2.8594E+05  UEXP  = 0.2601
+ VMAX  = 6.3062E+04   NEFF  = 8.494E+01   DELTA = 1.571
+ CJ    = 2.7077E-04   CJSW  = 3.1782E-10  PB    = 0.7329
+ MJ    = 0.4714       MJSW  = 0.3143      CGDO  = 4.55E-10
+ CGSO  =4.55E-10

.model BNPN NPN ( IS=18.9E-18     BF=109.7     NF=1          VAF=27.84
+                 IKF=10.84M      ISE=22.5F    NE=1.739      BR=785.1M
+                 NR=1.136        VAR=1.381    IKR=67.76U    ISC=4.4E-18
+                 NC=1.033        RB=951
+                 RE=19           RC=860       EG=1.11
+                 XTI=3           VJE=1        MJE=0.5
+                 VJC=0.82        MJC=0.36     VJS=0.62      MJS=0.46
+                 CJE=30.8F       CJC=34.2F    CJS=16.1F    )


** SPICE file created for circuit sr2-cell
** Technology: bicmos-su
**

** NODE: 0 = GND
** NODE: 1 = Vdd
** NODE: 2 = Error
M0 100 101 102 0 nfet L=2.0U W=3.0U
M1 100 103 102 1 pfet L=2.0U W=7.0U
M2 104 105 106 1 pfet L=2.0U W=7.0U
```

```
M3 1 104 107 1 pfet L=2.0U W=8.0U
Q4 1 107 108 bnpn AREA=0.5
M5 107 104 0 0 nfet L=2.0U W=4.0U
Q6  108 109 0 bnpn AREA=0.5
M7 101 110 108 1 pfet L=2.0U W=7.0U
M8 1 101 111 1 pfet L=2.0U W=8.0U
M9 109 107 0 0 nfet L=2.0U W=4.0U
M10 109 104 108 0 nfet L=2.0U W=4.0U
M11 104 110 106 0 nfet L=2.0U W=3.0U
Q12  1 111 103 bnpn AREA=0.5
M13 111 101 0 0 nfet L=2.0U W=4.0U
Q14 103 112 0 bnpn AREA=0.5
M15 112 111 0 0 nfet L=2.0U W=4.0U
M16 112 101 103 0 nfet L=2.0U W=4.0U
M17 101 105 108 0 nfet L=2.0U W=3.0U
C0 103 112 12F
C1 108 109 12F
C2 1 111 13F
C3 107 1 13F
** NODE: 105 = clk+
** NODE: 0 = GND!
C4 112 0 19F
** NODE: 112 = 8_206_208#
** NODE: 110 = clk-
C5 111 0 23F
** NODE: 111 = 8_198_240#
C6 1 0 264F
** NODE: 1 = Vdd!
C7 109 0 19F
** NODE: 109 = 8_130_208#
C8 107 0 23F
** NODE: 107 = 8_122_240#
C9 104 0 39F
** NODE: 104 = 8_110_204#
C10 106 0 37F
** NODE: 106 = 8_74_234#
C11 100 0 27F
** NODE: 100 = 8_214_334#
C12 102 0 27F
** NODE: 102 = 8_200_334#
C13 101 0 63F
** NODE: 101 = 8_182_316#
C14 103 0 59F
** NODE: 103 = 7_216_236#
C15 108 0 57F
** NODE: 108 = 7_140_236#


Vdd 1 0 5
Vin 106 0  pulse(5 0 0ns 0ns 0ns 5ns 10ns)
Vclk 105 0 pulse(5 0 0ns 0ns 0ns 3ns 6ns)
Vclk- 110 0 pulse(0 5 0ns 0ns 0ns 3ns 6ns)
.tran 0.1ns 20ns
.end
```

```
***************Shift registers in chains*************************
***spice simulation of the two stage shift register chain
*model LIST
.model NFET NMOS
+ LEVEL = 2.000       VTO   = 0.5813      GAMMA = 0.4634
+ PHI   = 0.6000      TOX   = 2.5000E-08  NSUB  = 9.7303E+14
+ NFS   = 6.8755E+11  TPG   = 1.000       XJ    = 1.000E-06
+ LD    = 1.4366E-07  UO    = 477.0       UCRIT = 3.3885E+05
+ UEXP  = 0.2219      VMAX  = 6.7140E+04  NEFF  = 50.00
+ DELTA = 4.011
+ CJ    = 1.224E-4    CJSW  = 3.8024E-10  PB    = 0.5665
+ MJ    = 0.3956      MJSW  = 0.2631      FC = 0.5
+ CGDO  = 4.07E-10    CGSO  = 4.07E-10

.model PFET PMOS
+ LEVEL = 2.000       VTO   = -0.7407     GAMMA = 0.4583
+ PHI   = 0.6977      TOX   = 2.5000E-08  NSUB  = 5.3138E+14
+ NFS   = 4.2439E+11  XJ    = 4.3014E-08  LD    = 1.3396E-07
+ UO    = 1.687E+02   UCRIT = 2.8594E+05  UEXP  = 0.2601
+ VMAX  = 6.3062E+04  NEFF  = 8.494E+01   DELTA = 1.571
+ CJ    = 2.7077E-04  CJSW  = 3.1782E-10  PB    = 0.7329
+ MJ    = 0.4714      MJSW  = 0.3143      CGDO  = 4.55E-10
+ CGSO  =4.55E-10

.model BNPN NPN ( IS=18.9E-18     BF=109.7     NF=1         VAF=27.84
+                 IKF=10.84M      ISE=22.5F    NE=1.739     BR=785.1M
+                 NR=1.136        VAR=1.381    IKR=67.76U   ISC=4.4E-18
+                 NC=1.033        RB=951
+                 RE=19           RC=860       EG=1.11
+                 XTI=3           VJE=1        MJE=0.5
+                 VJC=0.82        MJC=0.36     VJS=0.62     MJS=0.46
+                 CJE=30.8F       CJC=34.2F    CJS=16.1F    )



** SPICE file created for circuit sr2-2cell
** Technology: bicmos-su
**

** NODE: 0 = GND
** NODE: 1 = Vdd
** NODE: 2 = Error
M0 100 101 102 0 nfet L=2.0U W=3.0U
M1 100 103 102 1 pfet L=2.0U W=7.0U
M2 104 105 106 1 pfet L=2.0U W=7.0U
M3 1 104 107 1 pfet L=2.0U W=8.0U
Q4 1 107 108 bnpn AREA=0.5
M5 107 104 0 0 nfet L=2.0U W=4.0U
Q6 108 109 0 bnpn AREA=0.5
M7 101 110 108 1 pfet L=2.0U W=7.0U
M8 1 101 111 1 pfet L=2.0U W=8.0U
```

```
M9 109 107 0 0 nfet L=2.0U W=4.0U
M10 109 104 108 0 nfet L=2.0U W=4.0U
M11 104 110 106 0 nfet L=2.0U W=3.0U
Q12 1 111 103 bnpn AREA=0.5
M13 111 101 0 0 nfet L=2.0U W=4.0U
Q14 103 112 0 bnpn AREA=0.5
M15 113 114 115 0 nfet L=2.0U W=3.0U
M16 113 116 115 1 pfet L=2.0U W=7.0U
M17 117 105 103 1 pfet L=2.0U W=7.0U
M18 1 117 118 1 pfet L=2.0U W=8.0U
M19 112 111 0 0 nfet L=2.0U W=4.0U
M20 112 101 103 0 nfet L=2.0U W=4.0U
M21 101 105 108 0 nfet L=2.0U W=3.0U
Q22 1 118 119 bnpn AREA=0.5
M23 118 117 0 0 nfet L=2.0U W=4.0U
Q24 119 120 0 bnpn AREA=0.5
M25 114 110 119 1 pfet L=2.0U W=7.0U
M26 1 114 121 1 pfet L=2.0U W=8.0U
M27 120 118 0 0 nfet L=2.0U W=4.0U
M28 120 117 119 0 nfet L=2.0U W=4.0U
M29 117 110 103 0 nfet L=2.0U W=3.0U
Q30 1 121 116 bnpn AREA=0.5
M31 121 114 0 0 nfet L=2.0U W=4.0U
Q32 116 122 0 bnpn AREA=0.5
M33 122 121 0 0 nfet L=2.0U W=4.0U
M34 122 114 116 0 nfet L=2.0U W=4.0U
M35 114 105 119 0 nfet L=2.0U W=3.0U
C0 1 111 13F
C1 1 118 13F
C2 121 1 13F
C3 107 1 13F
C4 103 112 12F
C5 108 109 12F
C6 116 122 12F
C7 119 120 12F
C8 105 0 16F
** NODE: 105 = clk+
** NODE: 0 = GND!
C9 122 0 19F
** NODE: 122 = 8_414_208#
C10 110 0 16F
** NODE: 110 = clk-
C11 121 0 23F
** NODE: 121 = 8_406_240#
C12 1 0 528F
** NODE: 1 = Vdd!
C13 120 0 19F
** NODE: 120 = 8_338_208#
C14 118 0 23F
** NODE: 118 = 8_330_240#
C15 117 0 39F
** NODE: 117 = 8_318_204#
C16 113 0 27F
** NODE: 113 = 8_422_334#
```

```
C17 115 0 27F
** NODE: 115 = 8_408_334#
C18 112 0 19F
** NODE: 112 = 8_206_208#
C19 111 0 23F
** NODE: 111 = 8_198_240#
C20 109 0 19F
** NODE: 109 = 8_130_208#
C21 107 0 23F
** NODE: 107 = 8_122_240#
C22 104 0 39F
** NODE: 104 = 8_110_204#
C23 106 0 37F
** NODE: 106 = 8_74_234#
C24 100 0 27F
** NODE: 100 = 8_214_334#
C25 102 0 27F
** NODE: 102 = 8_200_334#
C26 114 0 63F
** NODE: 114 = 8_390_316#
C27 101 0 63F
** NODE: 101 = 8_182_316#
C28 116 0 59F
** NODE: 116 = 7_424_236#
C29 119 0 57F
** NODE: 119 = 7_348_236#
C30 103 0 94F
** NODE: 103 = 7_216_236#
C31 108 0 57F
** NODE: 108 = 7_140_236#


Vdd 1 0 5
Vin 106 0  pulse(5 0 0ns 0ns 0ns 5ns 10ns)
Vclk 105 0 pulse(5 0 0ns 0ns 0ns 3ns 6ns)
Vclk- 110 0 pulse(0 5 0ns 0ns 0ns 3ns 6ns)
.tran 1ns 45ns
.end



***********Simulation of BUS lines*****************************

*The following are the main sensoring transistors for 3_d magnetic
fields:

M11 4 2 3 6 PM L=5U W=6U AD=20P AS=24P PD=18U PS=20U
M12 5 2 3 6 PM L=5U W=6U AD=20P AS=24P PD=18U PS=20P

Q1 10 2 101 NB4X2 AREA=0.5
Q21 6 3 10 NB4X2 AREA=2
Q22 7 3 10 NB4X2 AREA=2
Q3 100 1 3 NB4X2 AREA=0.5
```

```
*The following are the three pairs of the active load transistors

M2 44 44 101 101 NM L=2U W=3U AD=14P AS=14P PD=15U PS=15U
M3 55 44 101 101 NM L=2U W=3U AD=14P AS=14P PD=15U PS=15U
M4 66 66 100 100 PM L=2U W=3U AD=14P AS=14P PD=15U PS=15U
M5 77 66 100 100 PM L=2U W=3U AD=14P AS=14P PD=15U PS=15U

*The following are the transmissionsgates pairs
MT1N 66 200 6 101 NM L=2U W=3U
MT2N 77 200 7 101 NM L=2U W=3U
MT1P 6 201 66 100 PM L=2U W=7U
MT2P 7 201 77 100 PM L=2U W=7U

MT3N 5 200 55 101 NM L=2U W=3U
MT4N 44 200 44 101 NM L=2U W=3U
MT3P 55 201 5 100 PM L=2U W=7U
MT4P 44 201 4 100 PM L=2U W=7U


* The following are the bias condition adjusted for DC simulation
VSS 101 0 0
VDD 100 0 5
VBIAS1 1 0 3.5
VBIAS2 2 0 0.72


*The following capacitance are the cap. extracted from magic layout
*of the array structure: the Bus CAp. for the columns.

Cbus5 5 101 1740F
Cbus4 4 101 1750F
Cbus6 6 100 1800F
Cbus7 7 100 1900F




*MODEL LIST
.MODEL NM NMOS
+ LEVEL = 2.000        VTO   = 0.5813      GAMMA = 0.4634
+ PHI   = 0.6000       TOX   = 2.5000E-08  NSUB  = 9.7303E+14
+ NFS   = 6.8755E+11   TPG   = 1.000       XJ    = 1.000E-06
+ LD    = 1.4366E-07   UO    = 477.0       UCRIT = 3.3885E+05
+ UEXP  = 0.2219       VMAX  = 6.7140E+04  NEFF  = 50.00
+ DELTA = 4.011
+ CJ    = 1.224E-4     CJSW  = 3.8024E-10  PB    = 0.5665
+ MJ    = 0.3956       MJSW  = 0.2631      FC = 0.5
+ CGDO  = 4.07E-10     CGSO  = 4.07E-10

.MODEL PM PMOS
+ LEVEL = 2.000        VTO   = -0.7407     GAMMA = 0.4583
+ PHI   = 0.6977       TOX   = 2.5000E-08  NSUB  = 5.3138E+14
```

```
+ NFS    = 4.2439E+11  XJ    = 4.3014E-08  LD    = 1.3396E-07
+ UO     = 1.687E+02   UCRIT = 2.8594E+05  UEXP  = 0.2601
+ VMAX   = 6.3062E+04  NEFF  = 8.494E+01   DELTA = 1.571
+ CJ     = 2.7077E-04  CJSW  = 3.1782E-10  PB    = 0.7329
+ MJ     = 0.4714      MJSW  = 0.3143      CGDO  = 4.55E-10
+ CGSO   =4.55E-10

.MODEL NB4X2 NPN ( IS=18.9E-18     BF=109.7     NF=1          VAF=27.84
+                  IKF=10.84M      ISE=22.5F    NE=1.739      BR=785.1M
+                  NR=1.136        VAR=1.381    IKR=67.76U    ISC=4.4E-18
+                  NC=1.033        RB=951
+                  RE=19           RC=860       EG=1.11
+                  XTI=3           VJE=1        MJE=0.5
+                  VJC=0.82        MJC=0.36     VJS=0.62      MJS=0.46
+                  CJE=30.8F       CJC=34.2F    CJS=16.1F    )


.MODEL PB4X2 PNP ( IS=18.9E-18     BF=109.7     NF=1          VAF=27.84
+                  IKF=10.84M      ISE=22.5F    NE=1.739      BR=785.1M
+                  NR=1.136        VAR=1.381    IKR=67.76U    ISC=4.4E-18
+                  NC=1.033        RB=951
+                  RE=19           RC=860       EG=1.11
+                  XTI=3           VJE=1        MJE=0.5
+                  VJC=0.82        MJC=0.36     VJS=0.62      MJS=0.46
+                  CJE=30.8F       CJC=34.2F    CJS=16.1F



*the following are the switching signals for the transmissions gate

V+ 200 101 PULSE(5 0 1250NS 0 0 2500NS 5000NS)
V- 201 101 PULSE(0 5 1250NS 0 0 2500NS 5000NS)




.TRAN 75NS 7500NS
*.WIDTH OUT=80
*.PLOT TRAN V(200)
*.PLOT TRAN V(201)
*.PLOT TRAN V(4)
*.PLOT TRAN V(44)
*.PLOT TRAN V(6)
*.PLOT TRAN V(66)
*.PLOT TRAN V(10)
*.PRINT TRAN V(4)  V(44)
*.PRINT TRAN V(6) V(77)


.END
```

# C. Extract Files from MAGIC layouts

```
********************8 x 8 Array in merged BiCMOS********************
** SPICE file created for circuit tatol
** Technology: bicmos-su
**

** NODE: 0 = GND
** NODE: 1 = Vdd
** NODE: 2 = Error
M0 100 101 102 103 pfet L=2.0U W=7.0U
M1 100 104 102 0 nfet L=2.0U W=3.0U
M2 105 101 106 103 pfet L=2.0U W=7.0U
M3 107 101 102 108 pfet L=2.0U W=7.0U
M4 105 104 106 0 nfet L=2.0U W=3.0U
M5 107 109 102 0 nfet L=2.0U W=3.0U
M6 110 101 106 108 pfet L=2.0U W=7.0U
M7 111 101 102 112 pfet L=2.0U W=7.0U
M8 110 109 106 0 nfet L=2.0U W=3.0U
M9 111 113 102 0 nfet L=2.0U W=3.0U
M10 114 101 106 112 pfet L=2.0U W=7.0U
M11 115 101 102 116 pfet L=2.0U W=7.0U
M12 114 113 106 0 nfet L=2.0U W=3.0U
M13 115 117 102 0 nfet L=2.0U W=3.0U
M14 118 101 106 116 pfet L=2.0U W=7.0U
M15 119 101 102 120 pfet L=2.0U W=7.0U
M16 118 117 106 0 nfet L=2.0U W=3.0U
M17 119 121 102 0 nfet L=2.0U W=3.0U
M18 122 101 106 120 pfet L=2.0U W=7.0U
M19 123 101 102 124 pfet L=2.0U W=7.0U
M20 122 121 106 0 nfet L=2.0U W=3.0U
M21 123 125 102 0 nfet L=2.0U W=3.0U
M22 126 101 106 124 pfet L=2.0U W=7.0U
M23 127 101 102 128 pfet L=2.0U W=7.0U
M24 126 125 106 0 nfet L=2.0U W=3.0U
M25 127 129 102 0 nfet L=2.0U W=3.0U
M26 130 101 106 128 pfet L=2.0U W=7.0U
M27 131 101 102 132 pfet L=2.0U W=7.0U
M28 130 129 106 0 nfet L=2.0U W=3.0U
M29 131 133 102 0 nfet L=2.0U W=3.0U
M30 134 101 106 132 pfet L=2.0U W=7.0U
M31 0 102 102 0 nfet L=2.0U W=3.0U
M32 106 102 0 0 nfet L=2.0U W=3.0U
M33 134 133 106 0 nfet L=2.0U W=3.0U
M34 135 101 136 137 pfet L=2.0U W=7.0U
M35 135 104 136 0 nfet L=2.0U W=3.0U
M36 135 101 138 137 pfet L=2.0U W=7.0U
M37 135 104 138 0 nfet L=2.0U W=3.0U
M38 139 101 140 0 nfet L=2.0U W=3.0U
M39 141 140 0 0 nfet L=2.0U W=4.0U
M40 142 140 101 0 nfet L=2.0U W=4.0U
M41 139 104 140 1 pfet L=2.0U W=7.0U
M42 142 141 0 0 nfet L=2.0U W=4.0U
```

```
M43 142 0 142 101 bnpn L=1.0U W=8.0U
M44 141 101 141 1 bnpn L=1.0U W=8.0U
M45 1 140 141 1 pfet L=2.0U W=8.0U
M46 101 104 143 0 nfet L=2.0U W=3.0U
M47 144 143 0 0 nfet L=2.0U W=4.0U
M48 145 143 101 0 nfet L=2.0U W=4.0U
M49 101 101 143 1 pfet L=2.0U W=7.0U
M50 145 144 0 0 nfet L=2.0U W=4.0U
M51 145 0 145 101 bnpn L=1.0U W=8.0U
M52 146 101 147 1 pfet L=2.0U W=7.0U
M53 146 143 147 0 nfet L=2.0U W=3.0U
M54 144 101 144 1 bnpn L=1.0U W=8.0U
M55 1 143 144 1 pfet L=2.0U W=8.0U
M56 148 101 149 1 pfet L=2.0U W=7.0U
M57 148 143 149 0 nfet L=2.0U W=3.0U
M58 101 101 150 0 nfet L=2.0U W=3.0U
M59 151 150 0 0 nfet L=2.0U W=4.0U
M60 152 150 153 0 nfet L=2.0U W=4.0U
M61 101 104 150 1 pfet L=2.0U W=7.0U
M62 152 151 0 0 nfet L=2.0U W=4.0U
M63 152 0 152 153 bnpn L=1.0U W=8.0U
M64 151 153 151 1 bnpn L=1.0U W=8.0U
M65 1 150 151 1 pfet L=2.0U W=8.0U
M66 153 104 154 0 nfet L=2.0U W=3.0U
M67 155 154 0 0 nfet L=2.0U W=4.0U
M68 156 154 101 0 nfet L=2.0U W=4.0U
M69 153 101 154 1 pfet L=2.0U W=7.0U
M70 156 155 0 0 nfet L=2.0U W=4.0U
M71 156 0 156 101 bnpn L=1.0U W=8.0U
M72 146 101 147 1 pfet L=2.0U W=7.0U
M73 146 154 147 0 nfet L=2.0U W=3.0U
M74 155 101 155 1 bnpn L=1.0U W=8.0U
M75 1 154 155 1 pfet L=2.0U W=8.0U
M76 157 101 149 1 pfet L=2.0U W=7.0U
M77 157 154 149 0 nfet L=2.0U W=3.0U
M78 101 101 158 0 nfet L=2.0U W=3.0U
M79 159 158 0 0 nfet L=2.0U W=4.0U
M80 160 158 161 0 nfet L=2.0U W=4.0U
M81 101 104 158 1 pfet L=2.0U W=7.0U
M82 160 159 0 0 nfet L=2.0U W=4.0U
M83 160 0 160 161 bnpn L=1.0U W=8.0U
M84 159 161 159 1 bnpn L=1.0U W=8.0U
M85 1 158 159 1 pfet L=2.0U W=8.0U
M86 161 104 162 0 nfet L=2.0U W=3.0U
M87 163 162 0 0 nfet L=2.0U W=4.0U
M88 164 162 101 0 nfet L=2.0U W=4.0U
M89 161 101 162 1 pfet L=2.0U W=7.0U
M90 164 163 0 0 nfet L=2.0U W=4.0U
M91 164 0 164 101 bnpn L=1.0U W=8.0U
M92 146 101 147 1 pfet L=2.0U W=7.0U
M93 146 162 147 0 nfet L=2.0U W=3.0U
M94 163 101 163 1 bnpn L=1.0U W=8.0U
M95 1 162 163 1 pfet L=2.0U W=8.0U
M96 165 101 149 1 pfet L=2.0U W=7.0U
```

```
M97 165 162 149 0 nfet L=2.0U W=3.0U
M98 101 101 166 0 nfet L=2.0U W=3.0U
M99 167 166 0 0 nfet L=2.0U W=4.0U
M100 168 166 169 0 nfet L=2.0U W=4.0U
M101 101 104 166 1 pfet L=2.0U W=7.0U
M102 168 167 0 0 nfet L=2.0U W=4.0U
M103 168 0 168 169 bnpn L=1.0U W=8.0U
M104 167 169 167 1 bnpn L=1.0U W=8.0U
M105 1 166 167 1 pfet L=2.0U W=8.0U
M106 169 104 170 0 nfet L=2.0U W=3.0U
M107 171 170 0 0 nfet L=2.0U W=4.0U
M108 172 170 101 0 nfet L=2.0U W=4.0U
M109 169 101 170 1 pfet L=2.0U W=7.0U
M110 172 171 0 0 nfet L=2.0U W=4.0U
M111 172 0 172 101 bnpn L=1.0U W=8.0U
M112 146 101 147 1 pfet L=2.0U W=7.0U
M113 146 170 147 0 nfet L=2.0U W=3.0U
M114 171 101 171 1 bnpn L=1.0U W=8.0U
M115 1 170 171 1 pfet L=2.0U W=8.0U
M116 173 101 149 1 pfet L=2.0U W=7.0U
M117 173 170 149 0 nfet L=2.0U W=3.0U
M118 101 101 174 0 nfet L=2.0U W=3.0U
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M477 347 292 343 292 bnpn L=2.0U W=2.0U
M478 126 0 347 292 pfet L=9.0U W=8.0U
M479 146 348 146 208 bnpn L=1.0U W=8.0U
M480 173 0 173 349 bnpn L=1.0U W=8.0U
M481 350 292 348 292 bnpn L=2.0U W=2.0U
M482 348 346 348 292 bnpn L=2.0U W=10.0U
M483 350 292 348 292 bnpn L=2.0U W=2.0U
M484 126 0 350 292 pfet L=9.0U W=8.0U
M485 146 351 146 208 bnpn L=1.0U W=8.0U
M486 181 0 181 352 bnpn L=1.0U W=8.0U
M487 353 292 351 292 bnpn L=2.0U W=2.0U
M488 351 349 351 292 bnpn L=2.0U W=10.0U
M489 353 292 351 292 bnpn L=2.0U W=2.0U
M490 126 0 353 292 pfet L=9.0U W=8.0U
M491 146 354 146 208 bnpn L=1.0U W=8.0U
M492 189 0 189 355 bnpn L=1.0U W=8.0U
M493 356 292 354 292 bnpn L=2.0U W=2.0U
M494 354 352 354 292 bnpn L=2.0U W=10.0U
M495 356 292 354 292 bnpn L=2.0U W=2.0U
M496 126 0 356 292 pfet L=9.0U W=8.0U
M497 146 357 146 208 bnpn L=1.0U W=8.0U
M498 197 0 197 358 bnpn L=1.0U W=8.0U
M499 359 292 357 292 bnpn L=2.0U W=2.0U
M500 357 355 357 292 bnpn L=2.0U W=10.0U
M501 359 292 357 292 bnpn L=2.0U W=2.0U
M502 126 0 359 292 pfet L=9.0U W=8.0U
M503 146 360 146 208 bnpn L=1.0U W=8.0U
M504 205 0 205 361 bnpn L=1.0U W=8.0U
M505 362 292 360 292 bnpn L=2.0U W=2.0U
M506 360 358 360 292 bnpn L=2.0U W=10.0U
M507 362 292 360 292 bnpn L=2.0U W=2.0U
M508 126 0 362 292 pfet L=9.0U W=8.0U
M509 146 363 146 208 bnpn L=1.0U W=8.0U
M510 364 292 363 292 bnpn L=2.0U W=2.0U
M511 363 361 363 292 bnpn L=2.0U W=10.0U
M512 364 292 363 292 bnpn L=2.0U W=2.0U
M513 126 0 364 292 pfet L=9.0U W=8.0U
M514 148 0 148 365 bnpn L=1.0U W=8.0U
M515 146 366 146 208 bnpn L=1.0U W=8.0U
M516 157 0 157 367 bnpn L=1.0U W=8.0U
M517 368 318 366 318 bnpn L=2.0U W=2.0U
M518 366 365 366 318 bnpn L=2.0U W=10.0U
M519 368 318 366 318 bnpn L=2.0U W=2.0U
M520 130 0 368 318 pfet L=9.0U W=8.0U
M521 146 369 146 208 bnpn L=1.0U W=8.0U
M522 165 0 165 370 bnpn L=1.0U W=8.0U
M523 371 318 369 318 bnpn L=2.0U W=2.0U
M524 369 367 369 318 bnpn L=2.0U W=10.0U
M525 371 318 369 318 bnpn L=2.0U W=2.0U
M526 130 0 371 318 pfet L=9.0U W=8.0U
M527 146 372 146 208 bnpn L=1.0U W=8.0U
M528 173 0 173 373 bnpn L=1.0U W=8.0U
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M530 372 370 372 318 bnpn L=2.0U W=10.0U
M531 374 318 372 318 bnpn L=2.0U W=2.0U
M532 130 0 374 318 pfet L=9.0U W=8.0U
M533 146 375 146 208 bnpn L=1.0U W=8.0U
M534 181 0 181 376 bnpn L=1.0U W=8.0U
M535 377 318 375 318 bnpn L=2.0U W=2.0U
M536 375 373 375 318 bnpn L=2.0U W=10.0U
M537 377 318 375 318 bnpn L=2.0U W=2.0U
M538 130 0 377 318 pfet L=9.0U W=8.0U
M539 146 378 146 208 bnpn L=1.0U W=8.0U
M540 189 0 189 379 bnpn L=1.0U W=8.0U
M541 380 318 378 318 bnpn L=2.0U W=2.0U
M542 378 376 378 318 bnpn L=2.0U W=10.0U
M543 380 318 378 318 bnpn L=2.0U W=2.0U
M544 130 0 380 318 pfet L=9.0U W=8.0U
M545 146 381 146 208 bnpn L=1.0U W=8.0U
M546 197 0 197 382 bnpn L=1.0U W=8.0U
M547 383 318 381 318 bnpn L=2.0U W=2.0U
M548 381 379 381 318 bnpn L=2.0U W=10.0U
M549 383 318 381 318 bnpn L=2.0U W=2.0U
M550 130 0 383 318 pfet L=9.0U W=8.0U
M551 146 384 146 208 bnpn L=1.0U W=8.0U
M552 205 0 205 385 bnpn L=1.0U W=8.0U
M553 386 318 384 318 bnpn L=2.0U W=2.0U
M554 384 382 384 318 bnpn L=2.0U W=10.0U
M555 386 318 384 318 bnpn L=2.0U W=2.0U
M556 130 0 386 318 pfet L=9.0U W=8.0U
M557 146 387 146 208 bnpn L=1.0U W=8.0U
M558 388 318 387 318 bnpn L=2.0U W=2.0U
M559 387 385 387 318 bnpn L=2.0U W=10.0U
M560 388 318 387 318 bnpn L=2.0U W=2.0U
M561 130 0 388 318 pfet L=9.0U W=8.0U
M562 148 0 148 389 bnpn L=1.0U W=8.0U
M563 146 390 146 208 bnpn L=1.0U W=8.0U
M564 157 0 157 391 bnpn L=1.0U W=8.0U
M565 392 344 390 344 bnpn L=2.0U W=2.0U
M566 390 389 390 344 bnpn L=2.0U W=10.0U
M567 392 344 390 344 bnpn L=2.0U W=2.0U
M568 134 0 392 344 pfet L=9.0U W=8.0U
M569 146 393 146 208 bnpn L=1.0U W=8.0U
M570 208 136 136 394 pfet L=2.0U W=3.0U
M571 138 136 208 394 pfet L=2.0U W=3.0U
M572 165 0 165 395 bnpn L=1.0U W=8.0U
M573 396 344 393 344 bnpn L=2.0U W=2.0U
M574 393 391 393 344 bnpn L=2.0U W=10.0U
M575 396 344 393 344 bnpn L=2.0U W=2.0U
M576 134 0 396 344 pfet L=9.0U W=8.0U
M577 146 397 146 208 bnpn L=1.0U W=8.0U
M578 173 0 173 398 bnpn L=1.0U W=8.0U
M579 399 344 397 344 bnpn L=2.0U W=2.0U
M580 397 395 397 344 bnpn L=2.0U W=10.0U
M581 399 344 397 344 bnpn L=2.0U W=2.0U
M582 134 0 399 344 pfet L=9.0U W=8.0U
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M583 146 400 146 208 bnpn L=1.0U W=8.0U
M584 181 0 181 401 bnpn L=1.0U W=8.0U
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M586 400 398 400 344 bnpn L=2.0U W=10.0U
M587 402 344 400 344 bnpn L=2.0U W=2.0U
M588 134 0 402 344 pfet L=9.0U W=8.0U
M589 146 403 146 208 bnpn L=1.0U W=8.0U
M590 189 0 189 404 bnpn L=1.0U W=8.0U
M591 405 344 403 344 bnpn L=2.0U W=2.0U
M592 403 401 403 344 bnpn L=2.0U W=10.0U
M593 405 344 403 344 bnpn L=2.0U W=2.0U
M594 134 0 405 344 pfet L=9.0U W=8.0U
M595 146 406 146 208 bnpn L=1.0U W=8.0U
M596 197 0 197 407 bnpn L=1.0U W=8.0U
M597 408 344 406 344 bnpn L=2.0U W=2.0U
M598 406 404 406 344 bnpn L=2.0U W=10.0U
M599 408 344 406 344 bnpn L=2.0U W=2.0U
M600 134 0 408 344 pfet L=9.0U W=8.0U
M601 146 409 146 208 bnpn L=1.0U W=8.0U
M602 205 0 205 410 bnpn L=1.0U W=8.0U
M603 411 344 409 344 bnpn L=2.0U W=2.0U
M604 409 407 409 344 bnpn L=2.0U W=10.0U
M605 411 344 409 344 bnpn L=2.0U W=2.0U
M606 134 0 411 344 pfet L=9.0U W=8.0U
M607 146 412 146 208 bnpn L=1.0U W=8.0U
M608 413 344 412 344 bnpn L=2.0U W=2.0U
M609 412 410 412 344 bnpn L=2.0U W=10.0U
M610 413 344 412 344 bnpn L=2.0U W=2.0U
M611 134 0 413 344 pfet L=9.0U W=8.0U
M612 414 104 135 0 nfet L=2.0U W=3.0U
M613 414 101 135 1 pfet L=2.0U W=7.0U
M614 415 104 135 0 nfet L=2.0U W=3.0U
M615 415 101 135 1 pfet L=2.0U W=7.0U
M616 416 104 101 1 pfet L=2.0U W=7.0U
M617 1 416 417 1 pfet L=2.0U W=8.0U
M618 417 101 417 1 bnpn L=1.0U W=8.0U
M619 417 416 0 0 nfet L=2.0U W=4.0U
M620 418 0 418 101 bnpn L=1.0U W=8.0U
M621 104 101 101 1 pfet L=2.0U W=7.0U
M622 1 104 419 1 pfet L=2.0U W=8.0U
M623 418 417 0 0 nfet L=2.0U W=4.0U
M624 418 416 101 0 nfet L=2.0U W=4.0U
M625 416 101 101 0 nfet L=2.0U W=3.0U
M626 419 101 419 1 bnpn L=1.0U W=8.0U
M627 419 104 0 0 nfet L=2.0U W=4.0U
M628 420 0 420 101 bnpn L=1.0U W=8.0U
M629 414 109 212 0 nfet L=2.0U W=3.0U
M630 414 101 212 1 pfet L=2.0U W=7.0U
M631 415 109 212 0 nfet L=2.0U W=3.0U
M632 415 101 212 1 pfet L=2.0U W=7.0U
M633 421 104 101 1 pfet L=2.0U W=7.0U
M634 1 421 422 1 pfet L=2.0U W=8.0U
M635 420 419 0 0 nfet L=2.0U W=4.0U
M636 420 104 101 0 nfet L=2.0U W=4.0U
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M637 104 104 101 0 nfet L=2.0U W=3.0U
M638 422 423 422 1 bnpn L=1.0U W=8.0U
M639 422 421 0 0 nfet L=2.0U W=4.0U
M640 424 0 424 423 bnpn L=1.0U W=8.0U
M641 109 101 423 1 pfet L=2.0U W=7.0U
M642 1 109 425 1 pfet L=2.0U W=8.0U
M643 424 422 0 0 nfet L=2.0U W=4.0U
M644 424 421 423 0 nfet L=2.0U W=4.0U
M645 421 101 101 0 nfet L=2.0U W=3.0U
M646 425 101 425 1 bnpn L=1.0U W=8.0U
M647 425 109 0 0 nfet L=2.0U W=4.0U
M648 426 0 426 101 bnpn L=1.0U W=8.0U
M649 414 113 238 0 nfet L=2.0U W=3.0U
M650 414 101 238 1 pfet L=2.0U W=7.0U
M651 415 113 238 0 nfet L=2.0U W=3.0U
M652 415 101 238 1 pfet L=2.0U W=7.0U
M653 427 104 101 1 pfet L=2.0U W=7.0U
M654 1 427 428 1 pfet L=2.0U W=8.0U
M655 426 425 0 0 nfet L=2.0U W=4.0U
M656 426 109 101 0 nfet L=2.0U W=4.0U
M657 109 104 423 0 nfet L=2.0U W=3.0U
M658 428 429 428 1 bnpn L=1.0U W=8.0U
M659 428 427 0 0 nfet L=2.0U W=4.0U
M660 430 0 430 429 bnpn L=1.0U W=8.0U
M661 113 101 429 1 pfet L=2.0U W=7.0U
M662 1 113 431 1 pfet L=2.0U W=8.0U
M663 430 428 0 0 nfet L=2.0U W=4.0U
M664 430 427 429 0 nfet L=2.0U W=4.0U
M665 427 101 101 0 nfet L=2.0U W=3.0U
M666 431 101 431 1 bnpn L=1.0U W=8.0U
M667 431 113 0 0 nfet L=2.0U W=4.0U
M668 432 0 432 101 bnpn L=1.0U W=8.0U
M669 414 117 264 0 nfet L=2.0U W=3.0U
M670 414 101 264 1 pfet L=2.0U W=7.0U
M671 415 117 264 0 nfet L=2.0U W=3.0U
M672 415 101 264 1 pfet L=2.0U W=7.0U
M673 433 104 101 1 pfet L=2.0U W=7.0U
M674 1 433 434 1 pfet L=2.0U W=8.0U
M675 432 431 0 0 nfet L=2.0U W=4.0U
M676 432 113 101 0 nfet L=2.0U W=4.0U
M677 113 104 429 0 nfet L=2.0U W=3.0U
M678 434 435 434 1 bnpn L=1.0U W=8.0U
M679 434 433 0 0 nfet L=2.0U W=4.0U
M680 436 0 436 435 bnpn L=1.0U W=8.0U
M681 117 101 435 1 pfet L=2.0U W=7.0U
M682 1 117 437 1 pfet L=2.0U W=8.0U
M683 436 434 0 0 nfet L=2.0U W=4.0U
M684 436 433 435 0 nfet L=2.0U W=4.0U
M685 433 101 101 0 nfet L=2.0U W=3.0U
M686 437 101 437 1 bnpn L=1.0U W=8.0U
M687 437 117 0 0 nfet L=2.0U W=4.0U
M688 438 0 438 101 bnpn L=1.0U W=8.0U
M689 414 121 266 0 nfet L=2.0U W=3.0U
M690 414 101 266 1 pfet L=2.0U W=7.0U
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M691 415 121 266 0 nfet L=2.0U W=3.0U
M692 415 101 266 1 pfet L=2.0U W=7.0U
M693 439 104 101 1 pfet L=2.0U W=7.0U
M694 1 439 440 1 pfet L=2.0U W=8.0U
M695 438 437 0 0 nfet L=2.0U W=4.0U
M696 438 117 101 0 nfet L=2.0U W=4.0U
M697 117 104 435 0 nfet L=2.0U W=3.0U
M698 440 441 440 1 bnpn L=1.0U W=8.0U
M699 440 439 0 0 nfet L=2.0U W=4.0U
M700 442 0 442 441 bnpn L=1.0U W=8.0U
M701 121 101 441 1 pfet L=2.0U W=7.0U
M702 1 121 443 1 pfet L=2.0U W=8.0U
M703 442 440 0 0 nfet L=2.0U W=4.0U
M704 442 439 441 0 nfet L=2.0U W=4.0U
M705 439 101 101 0 nfet L=2.0U W=3.0U
M706 443 101 443 1 bnpn L=1.0U W=8.0U
M707 443 121 0 0 nfet L=2.0U W=4.0U
M708 444 0 444 101 bnpn L=1.0U W=8.0U
M709 414 125 292 0 nfet L=2.0U W=3.0U
M710 414 101 292 1 pfet L=2.0U W=7.0U
M711 415 125 292 0 nfet L=2.0U W=3.0U
M712 415 101 292 1 pfet L=2.0U W=7.0U
M713 445 104 101 1 pfet L=2.0U W=7.0U
M714 1 445 446 1 pfet L=2.0U W=8.0U
M715 444 443 0 0 nfet L=2.0U W=4.0U
M716 444 121 101 0 nfet L=2.0U W=4.0U
M717 121 104 441 0 nfet L=2.0U W=3.0U
M718 446 447 446 1 bnpn L=1.0U W=8.0U
M719 446 445 0 0 nfet L=2.0U W=4.0U
M720 448 0 448 447 bnpn L=1.0U W=8.0U
M721 125 101 447 1 pfet L=2.0U W=7.0U
M722 1 125 449 1 pfet L=2.0U W=8.0U
M723 448 446 0 0 nfet L=2.0U W=4.0U
M724 448 445 447 0 nfet L=2.0U W=4.0U
M725 445 101 101 0 nfet L=2.0U W=3.0U
M726 449 101 449 1 bnpn L=1.0U W=8.0U
M727 449 125 0 0 nfet L=2.0U W=4.0U
M728 450 0 450 101 bnpn L=1.0U W=8.0U
M729 414 129 318 0 nfet L=2.0U W=3.0U
M730 414 101 318 1 pfet L=2.0U W=7.0U
M731 415 129 318 0 nfet L=2.0U W=3.0U
M732 415 101 318 1 pfet L=2.0U W=7.0U
M733 451 104 101 1 pfet L=2.0U W=7.0U
M734 1 451 452 1 pfet L=2.0U W=8.0U
M735 450 449 0 0 nfet L=2.0U W=4.0U
M736 450 125 101 0 nfet L=2.0U W=4.0U
M737 125 104 447 0 nfet L=2.0U W=3.0U
M738 452 453 452 1 bnpn L=1.0U W=8.0U
M739 452 451 0 0 nfet L=2.0U W=4.0U
M740 454 0 454 453 bnpn L=1.0U W=8.0U
M741 129 101 453 1 pfet L=2.0U W=7.0U
M742 1 129 455 1 pfet L=2.0U W=8.0U
M743 454 452 0 0 nfet L=2.0U W=4.0U
M744 454 451 453 0 nfet L=2.0U W=4.0U
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M745 451 101 101 0 nfet L=2.0U W=3.0U
M746 455 101 455 1 bnpn L=1.0U W=8.0U
M747 455 129 0 0 nfet L=2.0U W=4.0U
M748 456 0 456 101 bnpn L=1.0U W=8.0U
M749 414 133 344 0 nfet L=2.0U W=3.0U
M750 414 101 344 1 pfet L=2.0U W=7.0U
M751 415 133 344 0 nfet L=2.0U W=3.0U
M752 415 101 344 1 pfet L=2.0U W=7.0U
M753 457 104 101 1 pfet L=2.0U W=7.0U
M754 1 457 458 1 pfet L=2.0U W=8.0U
M755 456 455 0 0 nfet L=2.0U W=4.0U
M756 456 129 101 0 nfet L=2.0U W=4.0U
M757 129 104 453 0 nfet L=2.0U W=3.0U
M758 458 459 458 1 bnpn L=1.0U W=8.0U
M759 458 457 0 0 nfet L=2.0U W=4.0U
M760 460 0 460 459 bnpn L=1.0U W=8.0U
M761 133 101 459 1 pfet L=2.0U W=7.0U
M762 1 133 461 1 pfet L=2.0U W=8.0U
M763 460 458 0 0 nfet L=2.0U W=4.0U
M764 460 457 459 0 nfet L=2.0U W=4.0U
M765 457 101 101 0 nfet L=2.0U W=3.0U
M766 461 101 461 1 bnpn L=1.0U W=8.0U
M767 461 133 0 0 nfet L=2.0U W=4.0U
M768 462 0 462 101 bnpn L=1.0U W=8.0U
M769 208 415 415 463 pfet L=2.0U W=3.0U
M770 414 415 208 463 pfet L=2.0U W=3.0U
M771 462 461 0 0 nfet L=2.0U W=4.0U
M772 462 133 101 0 nfet L=2.0U W=4.0U
M773 133 104 459 0 nfet L=2.0U W=3.0U
C0 101 444 12F
C1 462 0 19F
** NODE: 462 = 8_11502_7833#
C2 461 0 23F
** NODE: 461 = 8_11494_7801#
C3 460 0 19F
** NODE: 460 = 8_11426_7833#
C4 458 0 23F
** NODE: 458 = 8_11418_7801#
C5 457 0 39F
** NODE: 457 = 8_11406_7837#
C6 456 0 19F
** NODE: 456 = 8_11296_7833#
C7 455 0 23F
** NODE: 455 = 8_11288_7801#
C8 454 0 19F
** NODE: 454 = 8_11220_7833#
C9 452 0 23F
** NODE: 452 = 8_11212_7801#
C10 451 0 39F
** NODE: 451 = 8_11200_7837#
C11 450 0 19F
** NODE: 450 = 8_11090_7833#
C12 449 0 23F
** NODE: 449 = 8_11082_7801#
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C13 448 0 19F
** NODE: 448 = 8_11014_7833#
C14 446 0 23F
** NODE: 446 = 8_11006_7801#
C15 445 0 39F
** NODE: 445 = 8_10994_7837#
C16 444 0 19F
** NODE: 444 = 8_10884_7833#
C17 443 0 23F
** NODE: 443 = 8_10876_7801#
C18 442 0 19F
** NODE: 442 = 8_10808_7833#
C19 440 0 23F
** NODE: 440 = 8_10800_7801#
C20 439 0 39F
** NODE: 439 = 8_10788_7837#
C21 438 0 19F
** NODE: 438 = 8_10678_7833#
C22 437 0 23F
** NODE: 437 = 8_10670_7801#
C23 436 0 19F
** NODE: 436 = 8_10602_7833#
C24 434 0 23F
** NODE: 434 = 8_10594_7801#
C25 433 0 39F
** NODE: 433 = 8_10582_7837#
C26 432 0 19F
** NODE: 432 = 8_10472_7833#
C27 431 0 23F
** NODE: 431 = 8_10464_7801#
C28 430 0 19F
** NODE: 430 = 8_10396_7833#
C29 428 0 23F
** NODE: 428 = 8_10388_7801#
C30 427 0 39F
** NODE: 427 = 8_10376_7837#
C31 426 0 19F
** NODE: 426 = 8_10266_7833#
C32 425 0 23F
** NODE: 425 = 8_10258_7801#
C33 424 0 19F
** NODE: 424 = 8_10190_7833#
C34 422 0 23F
** NODE: 422 = 8_10182_7801#
C35 421 0 39F
** NODE: 421 = 8_10170_7837#
C36 420 0 19F
** NODE: 420 = 8_10060_7833#
C37 419 0 23F
** NODE: 419 = 8_10052_7801#
C38 418 0 19F
** NODE: 418 = 8_9984_7833#
** NODE: 0 = GND!
C39 417 0 23F
```

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** NODE: 417 = 8_9976_7801#
C40 416 0 39F
** NODE: 416 = 8_9964_7837#
C41 104 0 1315F
** NODE: 104 = clk+
C42 415 0 303F
** NODE: 415 = 8_10118_7691#
C43 414 0 629F
** NODE: 414 = OUT_Y
C44 413 0 19F
** NODE: 413 = 8_11508_7423#
** NODE: 412 = 8_11448_7411#
C45 411 0 19F
** NODE: 411 = 8_11508_7241#
** NODE: 409 = 8_11448_7229#
C46 408 0 19F
** NODE: 408 = 8_11508_7059#
** NODE: 406 = 8_11448_7047#
C47 405 0 19F
** NODE: 405 = 8_11508_6877#
** NODE: 403 = 8_11448_6865#
C48 402 0 19F
** NODE: 402 = 8_11508_6695#
** NODE: 400 = 8_11448_6683#
C49 399 0 19F
** NODE: 399 = 8_11508_6513#
** NODE: 397 = 8_11448_6501#
C50 396 0 19F
** NODE: 396 = 8_11508_6331#
** NODE: 393 = 8_11448_6319#
C51 392 0 19F
** NODE: 392 = 8_11508_6149#
** NODE: 390 = 8_11448_6137#
C52 388 0 19F
** NODE: 388 = 8_11302_7423#
** NODE: 387 = 8_11242_7411#
C53 386 0 19F
** NODE: 386 = 8_11302_7241#
** NODE: 384 = 8_11242_7229#
C54 383 0 19F
** NODE: 383 = 8_11302_7059#
** NODE: 381 = 8_11242_7047#
C55 380 0 19F
** NODE: 380 = 8_11302_6877#
** NODE: 378 = 8_11242_6865#
C56 377 0 19F
** NODE: 377 = 8_11302_6695#
** NODE: 375 = 8_11242_6683#
C57 374 0 19F
** NODE: 374 = 8_11302_6513#
** NODE: 372 = 8_11242_6501#
C58 371 0 19F
** NODE: 371 = 8_11302_6331#
** NODE: 369 = 8_11242_6319#
```

```
C59 368 0 19F
** NODE: 368 = 8_11302_6149#
** NODE: 366 = 8_11242_6137#
C60 364 0 19F
** NODE: 364 = 8_11096_7423#
** NODE: 363 = 8_11036_7411#
C61 362 0 19F
** NODE: 362 = 8_11096_7241#
** NODE: 360 = 8_11036_7229#
C62 359 0 19F
** NODE: 359 = 8_11096_7059#
** NODE: 357 = 8_11036_7047#
C63 356 0 19F
** NODE: 356 = 8_11096_6877#
** NODE: 354 = 8_11036_6865#
C64 353 0 19F
** NODE: 353 = 8_11096_6695#
** NODE: 351 = 8_11036_6683#
C65 350 0 19F
** NODE: 350 = 8_11096_6513#
** NODE: 348 = 8_11036_6501#
C66 347 0 19F
** NODE: 347 = 8_11096_6331#
** NODE: 343 = 8_11036_6319#
C67 342 0 19F
** NODE: 342 = 8_11096_6149#
** NODE: 340 = 8_11036_6137#
C68 338 0 19F
** NODE: 338 = 8_10890_7423#
** NODE: 337 = 8_10830_7411#
C69 336 0 19F
** NODE: 336 = 8_10890_7241#
C70 464 0 16F
** NODE: 464 = 8_10918_7225#
** NODE: 334 = 8_10830_7229#
C71 333 0 19F
** NODE: 333 = 8_10890_7059#
** NODE: 331 = 8_10830_7047#
C72 330 0 19F
** NODE: 330 = 8_10890_6877#
** NODE: 328 = 8_10830_6865#
C73 327 0 19F
** NODE: 327 = 8_10890_6695#
** NODE: 325 = 8_10830_6683#
C74 324 0 19F
** NODE: 324 = 8_10890_6513#
** NODE: 322 = 8_10830_6501#
C75 321 0 19F
** NODE: 321 = 8_10890_6331#
** NODE: 317 = 8_10830_6319#
C76 316 0 19F
** NODE: 316 = 8_10890_6149#
** NODE: 314 = 8_10830_6137#
C77 312 0 19F
```

```
** NODE: 312 = 8_10684_7423#
** NODE: 311 = 8_10624_7411#
C78 310 0 19F
** NODE: 310 = 8_10684_7241#
** NODE: 308 = 8_10624_7229#
C79 307 0 19F
** NODE: 307 = 8_10684_7059#
** NODE: 305 = 8_10624_7047#
C80 304 0 19F
** NODE: 304 = 8_10684_6877#
** NODE: 302 = 8_10624_6865#
C81 301 0 19F
** NODE: 301 = 8_10684_6695#
** NODE: 299 = 8_10624_6683#
C82 298 0 19F
** NODE: 298 = 8_10684_6513#
** NODE: 296 = 8_10624_6501#
C83 295 0 19F
** NODE: 295 = 8_10684_6331#
** NODE: 291 = 8_10624_6319#
C84 290 0 19F
** NODE: 290 = 8_10684_6149#
** NODE: 288 = 8_10624_6137#
C85 286 0 19F
** NODE: 286 = 8_10478_7423#
** NODE: 285 = 8_10418_7411#
C86 284 0 19F
** NODE: 284 = 8_10478_7241#
** NODE: 282 = 8_10418_7229#
C87 281 0 19F
** NODE: 281 = 8_10478_7059#
** NODE: 279 = 8_10418_7047#
C88 278 0 19F
** NODE: 278 = 8_10478_6877#
** NODE: 276 = 8_10418_6865#
C89 275 0 19F
** NODE: 275 = 8_10478_6695#
** NODE: 273 = 8_10418_6683#
C90 272 0 19F
** NODE: 272 = 8_10478_6513#
** NODE: 270 = 8_10418_6501#
C91 269 0 19F
** NODE: 269 = 8_10478_6331#
** NODE: 263 = 8_10418_6319#
C92 262 0 19F
** NODE: 262 = 8_10478_6149#
** NODE: 260 = 8_10418_6137#
C93 258 0 19F
** NODE: 258 = 8_10272_7423#
** NODE: 257 = 8_10212_7411#
C94 256 0 19F
** NODE: 256 = 8_10272_7241#
** NODE: 254 = 8_10212_7229#
C95 253 0 19F
```

```
** NODE: 253 = 8_10272_7059#
** NODE: 251 = 8_10212_7047#
C96 250 0 19F
** NODE: 250 = 8_10272_6877#
** NODE: 248 = 8_10212_6865#
C97 247 0 19F
** NODE: 247 = 8_10272_6695#
** NODE: 245 = 8_10212_6683#
C98 244 0 19F
** NODE: 244 = 8_10272_6513#
** NODE: 242 = 8_10212_6501#
C99 241 0 19F
** NODE: 241 = 8_10272_6331#
** NODE: 237 = 8_10212_6319#
C100 236 0 19F
** NODE: 236 = 8_10272_6149#
** NODE: 234 = 8_10212_6137#
C101 232 0 19F
** NODE: 232 = 8_10066_7423#
** NODE: 231 = 8_10006_7411#
C102 230 0 19F
** NODE: 230 = 8_10066_7241#
** NODE: 228 = 8_10006_7229#
C103 227 0 19F
** NODE: 227 = 8_10066_7059#
** NODE: 225 = 8_10006_7047#
C104 224 0 19F
** NODE: 224 = 8_10066_6877#
** NODE: 222 = 8_10006_6865#
C105 221 0 19F
** NODE: 221 = 8_10066_6695#
** NODE: 219 = 8_10006_6683#
C106 218 0 19F
** NODE: 218 = 8_10066_6513#
** NODE: 216 = 8_10006_6501#
C107 215 0 19F
** NODE: 215 = 8_10066_6331#
** NODE: 211 = 8_10006_6319#
C108 210 0 19F
** NODE: 210 = 8_10066_6149#
** NODE: 207 = 8_10006_6137#
C109 205 0 121F
** NODE: 205 = 8_9698_7473#
C110 146 0 1162F
** NODE: 146 = bias1
C111 204 0 19F
** NODE: 204 = 8_9556_7427#
C112 203 0 23F
** NODE: 203 = 8_9560_7447#
C113 202 0 73F
** NODE: 202 = 8_9536_7413#
C114 200 0 19F
** NODE: 200 = 8_9556_7351#
C115 199 0 23F
```

```
** NODE: 199 = 8_9560_7371#
C116 198 0 39F
** NODE: 198 = 8_9536_7337#
C117 197 0 121F
** NODE: 197 = 8_9698_7287#
C118 196 0 19F
** NODE: 196 = 8_9556_7241#
C119 195 0 23F
** NODE: 195 = 8_9560_7261#
C120 194 0 73F
** NODE: 194 = 8_9536_7227#
C121 192 0 19F
** NODE: 192 = 8_9556_7165#
C122 191 0 23F
** NODE: 191 = 8_9560_7185#
C123 190 0 39F
** NODE: 190 = 8_9536_7151#
C124 189 0 120F
** NODE: 189 = 8_9698_7101#
C125 188 0 19F
** NODE: 188 = 8_9556_7055#
C126 187 0 23F
** NODE: 187 = 8_9560_7075#
C127 186 0 73F
** NODE: 186 = 8_9536_7041#
C128 184 0 19F
** NODE: 184 = 8_9556_6979#
C129 183 0 23F
** NODE: 183 = 8_9560_6999#
C130 182 0 39F
** NODE: 182 = 8_9536_6965#
C131 181 0 120F
** NODE: 181 = 8_9698_6915#
C132 180 0 19F
** NODE: 180 = 8_9556_6869#
C133 179 0 23F
** NODE: 179 = 8_9560_6889#
C134 178 0 73F
** NODE: 178 = 8_9536_6855#
C135 176 0 19F
** NODE: 176 = 8_9556_6793#
C136 175 0 23F
** NODE: 175 = 8_9560_6813#
C137 174 0 39F
** NODE: 174 = 8_9536_6779#
C138 173 0 120F
** NODE: 173 = 8_9698_6729#
C139 172 0 19F
** NODE: 172 = 8_9556_6683#
C140 171 0 23F
** NODE: 171 = 8_9560_6703#
C141 170 0 73F
** NODE: 170 = 8_9536_6669#
C142 168 0 19F
```

```
** NODE: 168 = 8_9556_6607#
C143 167 0 23F
** NODE: 167 = 8_9560_6627#
C144 166 0 39F
** NODE: 166 = 8_9536_6593#
C145 165 0 120F
** NODE: 165 = 8_9698_6543#
C146 164 0 19F
** NODE: 164 = 8_9556_6497#
C147 163 0 23F
** NODE: 163 = 8_9560_6517#
C148 162 0 73F
** NODE: 162 = 8_9536_6483#
C149 160 0 19F
** NODE: 160 = 8_9556_6421#
C150 159 0 23F
** NODE: 159 = 8_9560_6441#
C151 158 0 39F
** NODE: 158 = 8_9536_6407#
C152 157 0 120F
** NODE: 157 = 8_9698_6357#
C153 156 0 19F
** NODE: 156 = 8_9556_6311#
C154 155 0 23F
** NODE: 155 = 8_9560_6331#
C155 154 0 73F
** NODE: 154 = 8_9536_6297#
C156 152 0 19F
** NODE: 152 = 8_9556_6235#
C157 151 0 23F
** NODE: 151 = 8_9560_6255#
C158 150 0 39F
** NODE: 150 = 8_9536_6221#
C159 149 0 651F
** NODE: 149 = BIAS2
C160 148 0 120F
** NODE: 148 = 8_9698_6171#
C161 147 0 637F
** NODE: 147 = BIAS!
C162 145 0 19F
** NODE: 145 = 8_9556_6125#
C163 144 0 23F
** NODE: 144 = 8_9560_6145#
C164 143 0 73F
** NODE: 143 = 8_9536_6111#
C165 142 0 19F
** NODE: 142 = 8_9556_6049#
C166 141 0 23F
** NODE: 141 = 8_9560_6069#
C167 140 0 39F
** NODE: 140 = 8_9536_6035#
C168 139 0 64F
** NODE: 139 = 8_9462_6009#
C169 138 0 675F
```

```
** NODE: 138 = OUT_X
C170 136 0 303F
** NODE: 136 = 8_9960_5833#
C171 134 0 373F
** NODE: 134 = 8_11536_7423#
C172 133 0 196F
** NODE: 133 = 8_11422_5843#
C173 131 0 231F
** NODE: 131 = 8_11524_5729#
C174 130 0 373F
** NODE: 130 = 8_11330_7423#
C175 129 0 200F
** NODE: 129 = 8_11216_5843#
C176 127 0 231F
** NODE: 127 = 8_11318_5729#
C177 126 0 373F
** NODE: 126 = 8_11124_7423#
C178 125 0 197F
** NODE: 125 = 8_11010_5843#
C179 123 0 230F
** NODE: 123 = 8_11112_5729#
C180 122 0 373F
** NODE: 122 = 8_10918_7423#
C181 121 0 197F
** NODE: 121 = 8_10804_5843#
C182 119 0 214F
** NODE: 119 = 8_10906_5729#
C183 118 0 372F
** NODE: 118 = 8_10712_7423#
C184 117 0 194F
** NODE: 117 = 8_10592_5843#
C185 115 0 230F
** NODE: 115 = 8_10694_5729#
C186 114 0 371F
** NODE: 114 = 8_10506_7423#
C187 113 0 192F
** NODE: 113 = 8_10382_5843#
C188 111 0 231F
** NODE: 111 = 8_10484_5729#
C189 110 0 371F
** NODE: 110 = 8_10300_7423#
C190 109 0 190F
** NODE: 109 = 8_10176_5843#
C191 107 0 231F
** NODE: 107 = 8_10278_5729#
C192 105 0 371F
** NODE: 105 = 8_10094_7423#
C193 106 0 647F
** NODE: 106 = OUT_Z
C194 100 0 230F
** NODE: 100 = 8_10072_5729#
C195 102 0 301F
** NODE: 102 = 8_10058_5725#
C196 459 0 57F
```

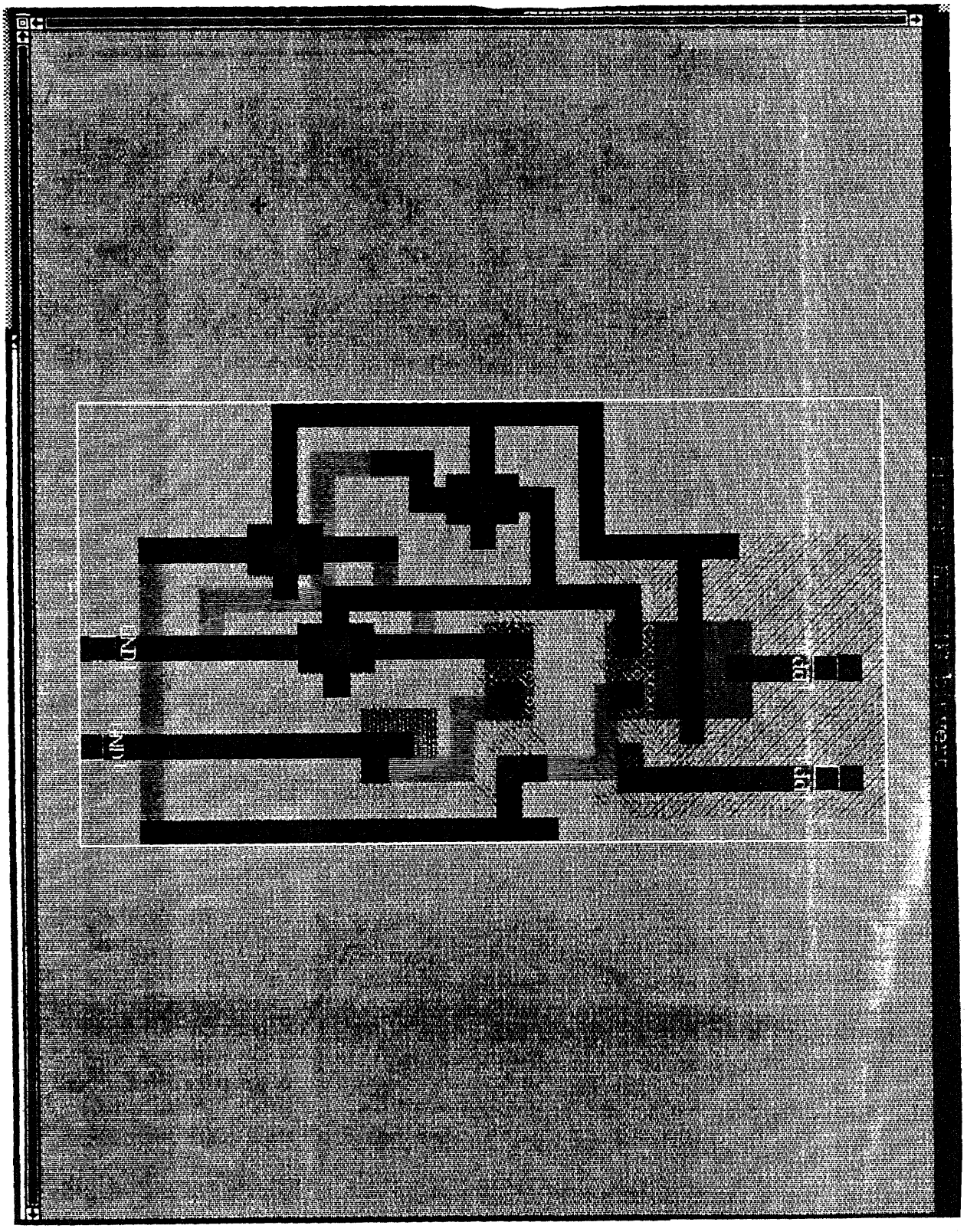
```
** NODE: 459 = 7_11436_7805#
C197 453 0 57F
** NODE: 453 = 7_11230_7805#
C198 447 0 57F
** NODE: 447 = 7_11024_7805#
C199 441 0 57F
** NODE: 441 = 7_10818_7805#
C200 435 0 57F
** NODE: 435 = 7_10612_7805#
C201 429 0 57F
** NODE: 429 = 7_10406_7805#
C202 423 0 57F
** NODE: 423 = 7_10200_7805#
C203 1 0 5708F
** NODE: 1 = Vdd!
C204 463 0 31F
** NODE: 463 = 7_11664_7651#
C205 410 0 26F
** NODE: 410 = 7_11418_7435#
C206 385 0 26F
** NODE: 385 = 7_11212_7435#
C207 361 0 26F
** NODE: 361 = 7_11006_7435#
C208 335 0 26F
** NODE: 335 = 7_10800_7435#
C209 309 0 26F
** NODE: 309 = 7_10594_7435#
C210 283 0 26F
** NODE: 283 = 7_10388_7435#
C211 255 0 26F
** NODE: 255 = 7_10182_7435#
C212 229 0 26F
** NODE: 229 = 7_9976_7435#
C213 201 0 57F
** NODE: 201 = 7_9584_7389#
C214 407 0 26F
** NODE: 407 = 7_11418_7253#
C215 382 0 26F
** NODE: 382 = 7_11212_7253#
C216 358 0 26F
** NODE: 358 = 7_11006_7253#
C217 332 0 26F
** NODE: 332 = 7_10800_7253#
C218 306 0 26F
** NODE: 306 = 7_10594_7253#
C219 280 0 26F
** NODE: 280 = 7_10388_7253#
C220 252 0 26F
** NODE: 252 = 7_10182_7253#
C221 226 0 26F
** NODE: 226 = 7_9976_7253#
C222 193 0 57F
** NODE: 193 = 7_9584_7203#
C223 404 0 26F
```

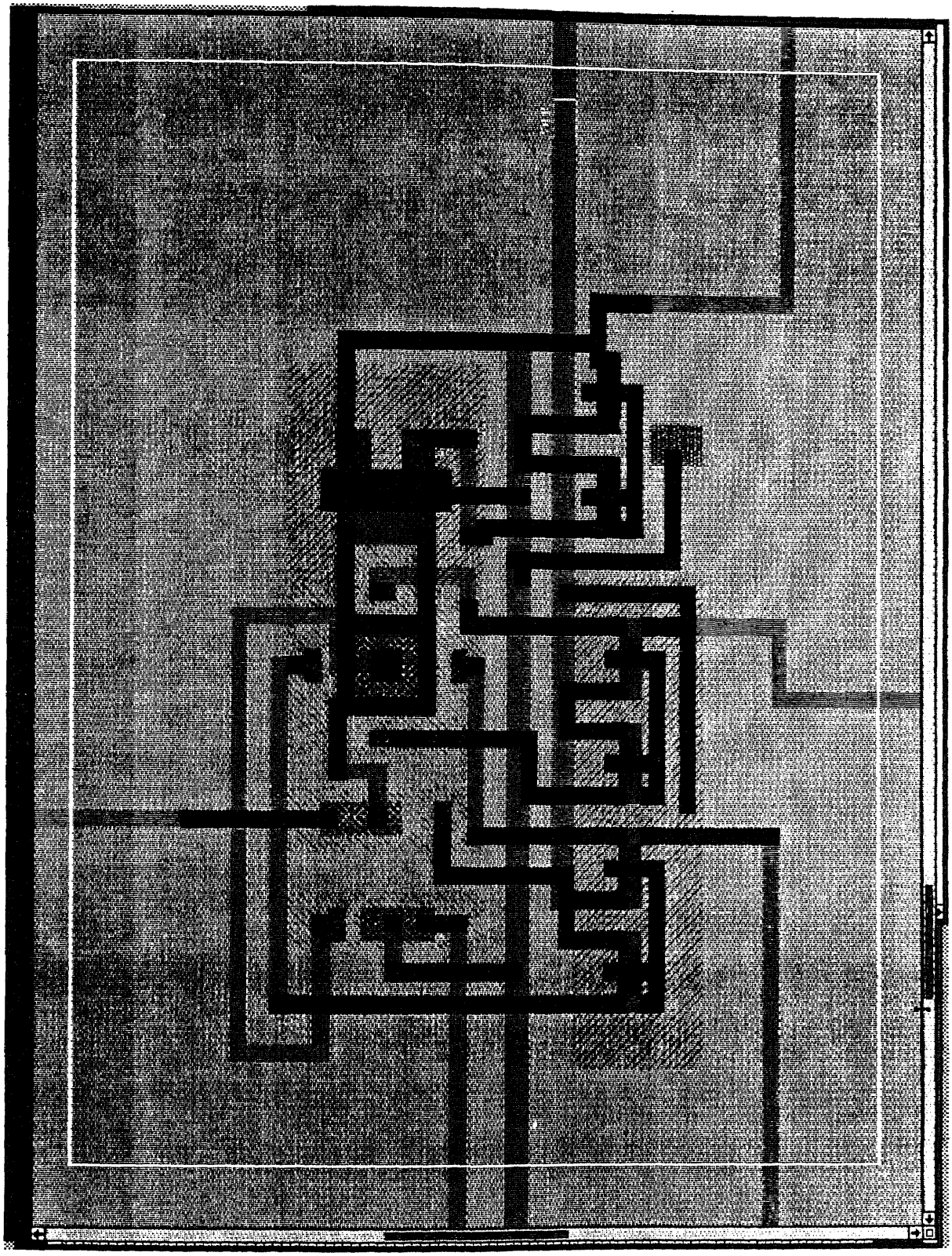
```
** NODE: 404 = 7_11418_7071#
C224 379 0 26F
** NODE: 379 = 7_11212_7071#
C225 355 0 26F
** NODE: 355 = 7_11006_7071#
C226 329 0 26F
** NODE: 329 = 7_10800_7071#
C227 303 0 26F
** NODE: 303 = 7_10594_7071#
C228 277 0 26F
** NODE: 277 = 7_10388_7071#
C229 249 0 26F
** NODE: 249 = 7_10182_7071#
C230 223 0 26F
** NODE: 223 = 7_9976_7071#
C231 185 0 57F
** NODE: 185 = 7_9584_7017#
C232 401 0 26F
** NODE: 401 = 7_11418_6889#
C233 376 0 26F
** NODE: 376 = 7_11212_6889#
C234 352 0 26F
** NODE: 352 = 7_11006_6889#
C235 326 0 26F
** NODE: 326 = 7_10800_6889#
C236 300 0 26F
** NODE: 300 = 7_10594_6889#
C237 274 0 26F
** NODE: 274 = 7_10388_6889#
C238 246 0 26F
** NODE: 246 = 7_10182_6889#
C239 220 0 26F
** NODE: 220 = 7_9976_6889#
C240 177 0 57F
** NODE: 177 = 7_9584_6831#
C241 398 0 26F
** NODE: 398 = 7_11418_6707#
C242 373 0 26F
** NODE: 373 = 7_11212_6707#
C243 349 0 26F
** NODE: 349 = 7_11006_6707#
C244 323 0 26F
** NODE: 323 = 7_10800_6707#
C245 297 0 26F
** NODE: 297 = 7_10594_6707#
C246 271 0 26F
** NODE: 271 = 7_10388_6707#
C247 243 0 26F
** NODE: 243 = 7_10182_6707#
C248 217 0 26F
** NODE: 217 = 7_9976_6707#
C249 169 0 57F
** NODE: 169 = 7_9584_6645#
C250 395 0 26F
```

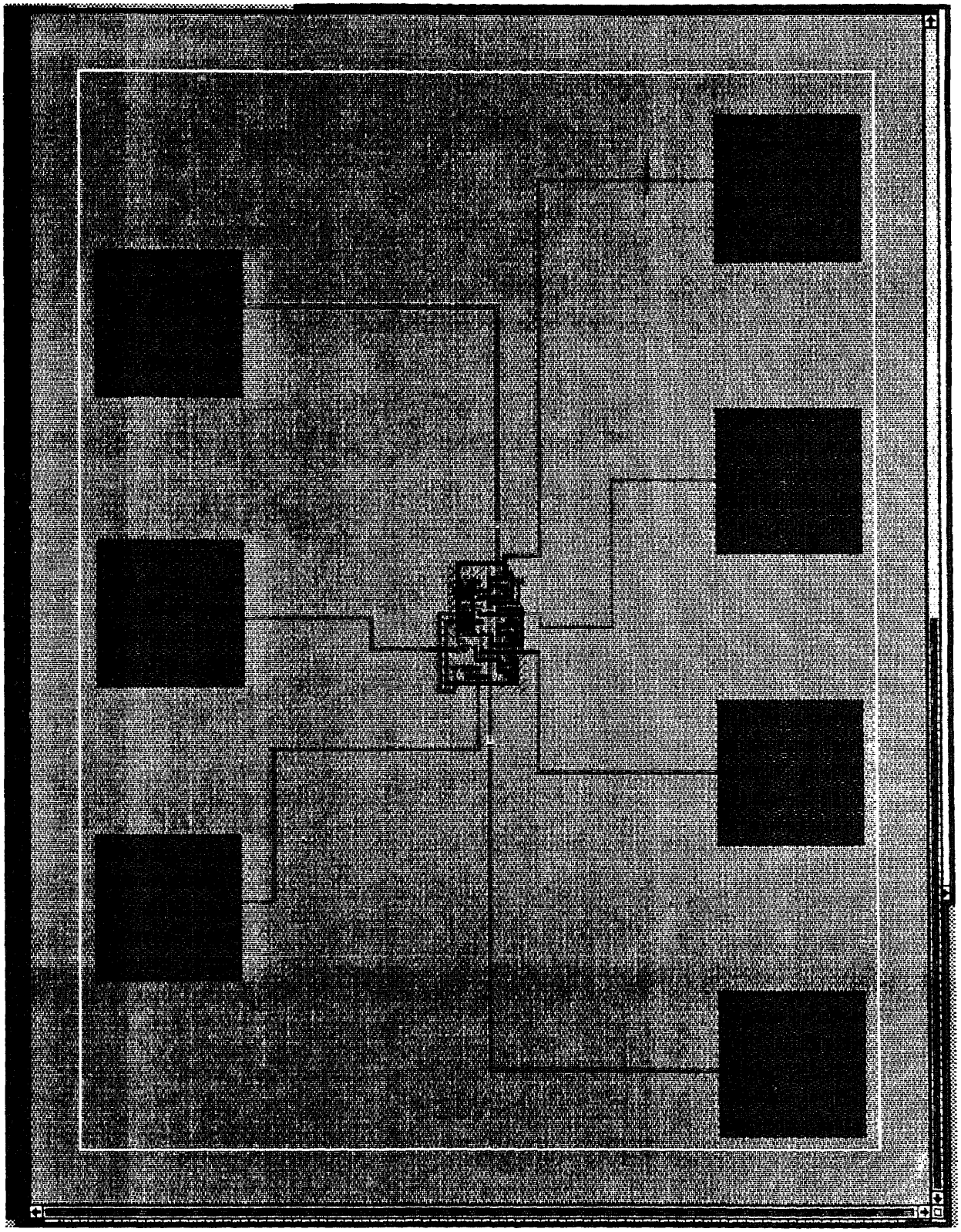
```
** NODE: 395 = 7_11418_6525#
C251 370 0 26F
** NODE: 370 = 7_11212_6525#
C252 346 0 26F
** NODE: 346 = 7_11006_6525#
C253 320 0 26F
** NODE: 320 = 7_10800_6525#
C254 294 0 26F
** NODE: 294 = 7_10594_6525#
C255 268 0 26F
** NODE: 268 = 7_10388_6525#
C256 240 0 26F
** NODE: 240 = 7_10182_6525#
C257 214 0 26F
** NODE: 214 = 7_9976_6525#
C258 161 0 57F
** NODE: 161 = 7_9584_6459#
C259 391 0 26F
** NODE: 391 = 7_11418_6343#
C260 367 0 26F
** NODE: 367 = 7_11212_6343#
C261 341 0 26F
** NODE: 341 = 7_11006_6343#
C262 315 0 26F
** NODE: 315 = 7_10800_6343#
C263 289 0 26F
** NODE: 289 = 7_10594_6343#
C264 261 0 26F
** NODE: 261 = 7_10388_6343#
C265 235 0 26F
** NODE: 235 = 7_10182_6343#
C266 209 0 26F
** NODE: 209 = 7_9976_6343#
C267 153 0 57F
** NODE: 153 = 7_9584_6273#
C268 344 0 1741F
** NODE: 344 = 7_11466_7435#
C269 389 0 26F
** NODE: 389 = 7_11418_6161#
C270 318 0 1740F
** NODE: 318 = 7_11260_7435#
C271 365 0 26F
** NODE: 365 = 7_11212_6161#
C272 292 0 1741F
** NODE: 292 = 7_11054_7435#
C273 339 0 26F
** NODE: 339 = 7_11006_6161#
C274 266 0 1741F
** NODE: 266 = 7_10848_7435#
C275 313 0 26F
** NODE: 313 = 7_10800_6161#
```

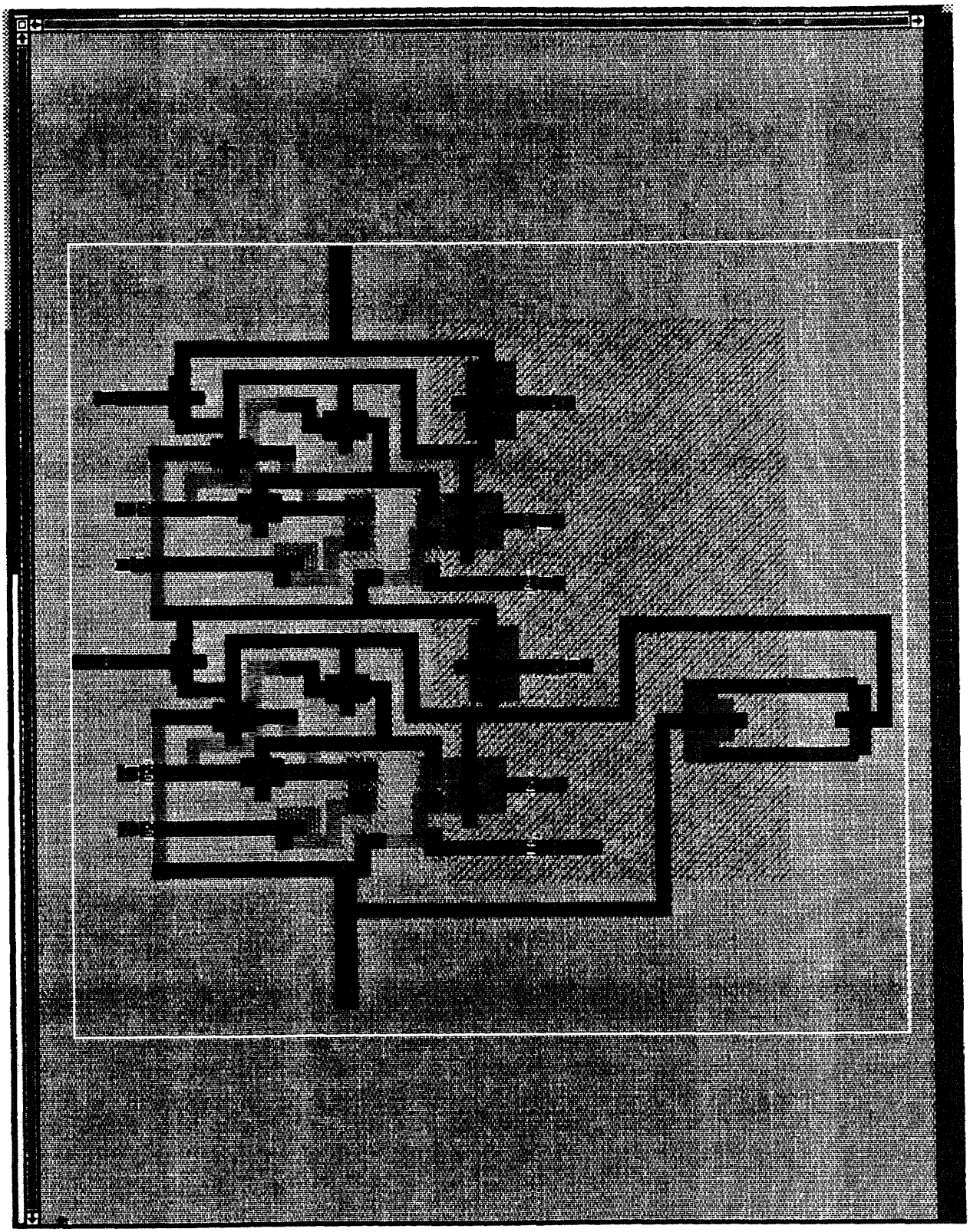
```
C276 264 0 1740F
** NODE: 264 = 7_10642_7435#
C277 287 0 26F
** NODE: 287 = 7_10594_6161#
C278 238 0 1738F
** NODE: 238 = 7_10436_7435#
C279 259 0 26F
** NODE: 259 = 7_10388_6161#
C280 212 0 1732F
** NODE: 212 = 7_10230_7435#
C281 233 0 26F
** NODE: 233 = 7_10182_6161#
C282 135 0 1735F
** NODE: 135 = Cbus2
C283 208 0 2897F
** NODE: 208 = Vdd
C284 206 0 26F
** NODE: 206 = 7_9976_6161#
C285 101 0 4960F
** NODE: 101 = init
C286 394 0 31F
** NODE: 394 = 7_11612_5841#
C287 345 0 54F
** NODE: 345 = 7_11402_5811#
C288 319 0 54F
** NODE: 319 = 7_11196_5811#
C289 293 0 54F
** NODE: 293 = 7_10990_5811#
C290 267 0 54F
** NODE: 267 = 7_10784_5811#
C291 265 0 54F
** NODE: 265 = 7_10572_5811#
C292 239 0 54F
** NODE: 239 = 7_10362_5811#
C293 213 0 54F
** NODE: 213 = 7_10156_5811#
C294 137 0 54F
** NODE: 137 = 7_9950_5811#
C295 132 0 54F
** NODE: 132 = 7_11500_5703#
C296 128 0 54F
** NODE: 128 = 7_11294_5703#
C297 124 0 54F
** NODE: 124 = 7_11088_5703#
C298 120 0 54F
** NODE: 120 = 7_10882_5703#
C299 116 0 54F
** NODE: 116 = 7_10670_5703#
C300 112 0 54F
** NODE: 112 = 7_10460_5703#
C301 108 0 54F
** NODE: 108 = 7_10254_5703#
C302 103 0 54F
** NODE: 103 = 7_10048_5703#
```

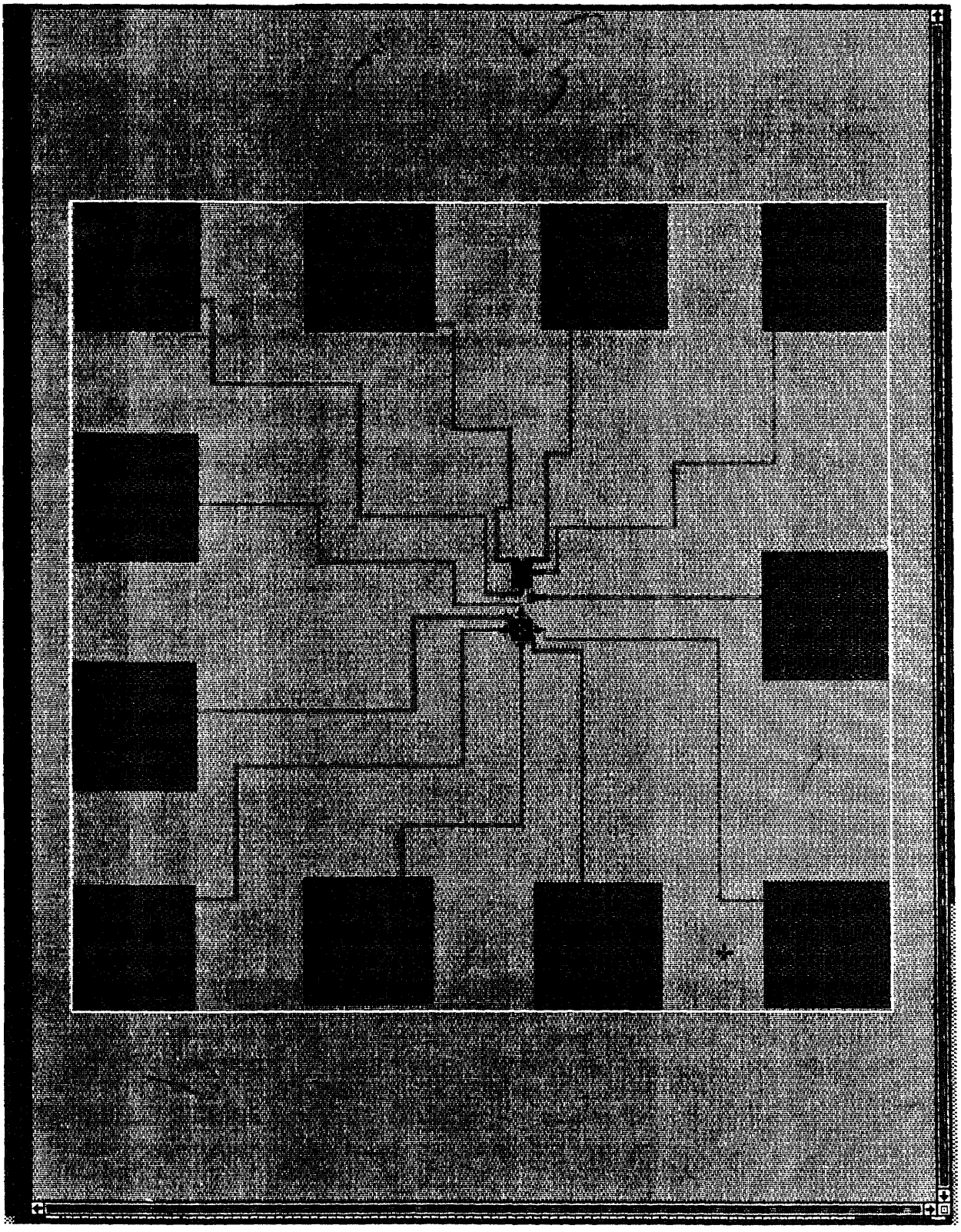
# D. Layouts

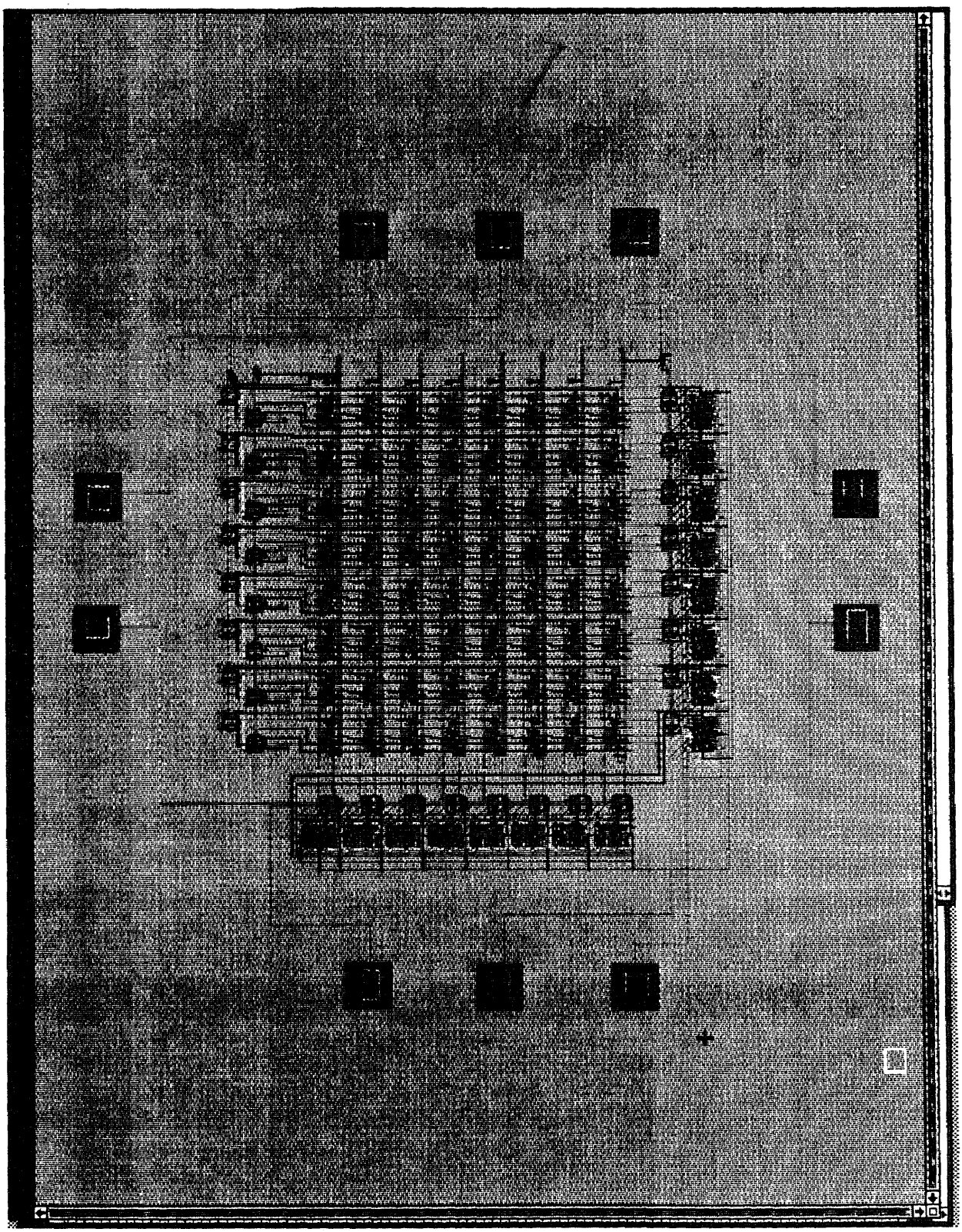


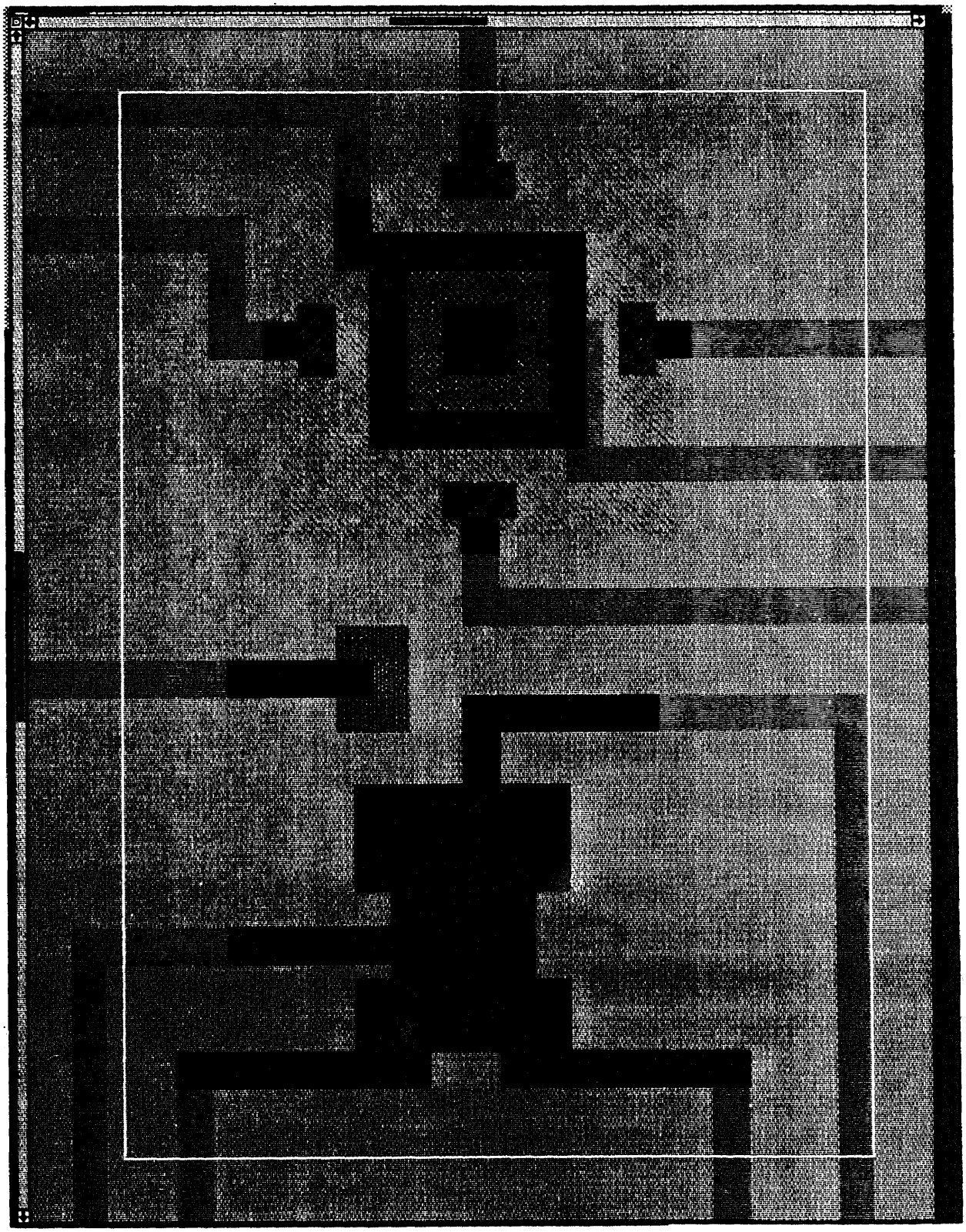












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