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Fabrication and characterization of gated silicon field emission micro triodes

Liu, Nanchou, Ph.D.

New Jersey Institute of Technology, 1992

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FABRICATION AND CHARACTERIZATION OF GATED SILICON FIELD EMISSION MICRO TRIODES

By

Nanchou Liu

A Dissertation

Submitted to the Faculty of

New Jersey Institute of Technology

in Partial Fulfillment of the Requirements for the Degree of

Doctor of Philosophy

Department of Electrical and Computer Engineering

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APPROVAL PAGE

Fabrication and Characterization

of Gated Silicon Field Emission Micro Triodes

by

Nanchou Liu

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ABSTRACT

Fabrication and Characterization

of

Gated Silicon Field Emission Micro Triodes

by

Nanchou Liu

This dissertation describes the fabrication technology and characterization of a gated silicon field emission micro triode that is a novel electron tunneling device for generating electron emission into a vacuum. Conic (point) and wedge field emitter structures with nm-scale radii were fabricated in silicon and GaAs by etching, MOCVD and dry oxidation. A new self-aligned process was developed for fabrication of vertical field emission triodes. This process allows control of gate opening to less than 0.5 μm diameter without the need of electron-beam writing. It also provides a planar gate electrode and a thick dielectric layer for reduction of the gate-cathode capacitance. Gated silicon field emission triodes, with silicon resistivity of 0.005 - 0.02 Ω-cm were studied. Gate and collector currents were measured in a vacuum of 2×10^{-8} torr, and current-voltage (I vs. V), current-time (I vs. t), Fowler-Nordheim (I/V^2 vs. $1/V$), and triode characteristics were determined. The data showed that the electron emission followed Fowler-Nordheim behavior. Single emitters had turn-on gate to cathode voltages (V) above 25 volts (typically 50 - 90 volts) and reproducible emission currents were measured in the range 5 pA - 1 μA. Emitting areas of 1.0×10^{-16} - 1.5×10^{-11} cm^2 and field conversion factors α/r (where electric field = $V\ \alpha/r$) of 3×10^5 - 8×10^5 cm^{-1} were calculated. Temporal fluctuations in emission current of 10%, 16%, and 40% were found for emission currents of 0.35 nA, 50 nA, and 0.5 μA,

respectively. The triode characteristics showed an Ig/Ic ratio of 0.25% and higher. Transconductances were found to be 3 $x10^{-8}$ mhos/tip.

Leakage characteristics of various dielectric materials used in the new self-aligned process (thermal oxide, CVD oxide, polyimide and spin-on-glass) were measured and evaluated. Electrostatic discharge and other device failure mechanisms have been observed and explained.

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This dissertation is dedicated to
my wife Yuh-Huey
and
my Parents

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CHAPTER 1
INTRODUCTION

This dissertation investigates the development and characterization of gated field emission micro triodes for vacuum microelectronic devices. The experimental work reported in this paper was done under the direction of Dr. R.B. Marcus at Navesink Engineering and Research Center of Bellcore, Red Bank, NJ.

Field emission vacuum microelectronics devices are novel electron tunneling devices for generating electron emission into a vacuum. These devices are attractive since they have higher cutoff frequency, less temperature sensitivity and better radiation hardness than solid state microelectronics devices [1]. Furthermore, field emission vacuum microelectronics devices offer a new approach to flat panel displays [2] and also to many devices using an electron source such as the scanning electron microscope, and the scanning tunneling microscope [3]. Field emission from a micro emitter has been intensively studied since the first international vacuum microelectronic symposium in Williamsburg, VA in 1988.

It is important that field emitters are sharp since the electric field scales with sharpness and electron emission is strongly dependent on the electric field [4]. Sharp emitters also make it possible for electron emission devices to operate at low voltage. The emitter damage by ion bombardment (the ions are generated by collisions with residual gas) can be reduced at low operating voltage due to kinetic energy reduction, and therefore the emitter lifetime can be extended. To reduce ionized collisions, the distance from cathode to anode

must be less than the electron mean free path (λ_C). The electron mean free path λ_C is given by

$$\lambda_C = \frac{T}{273\, pP_C(V)}\ cm$$

where P_C (V) is the average number of collisions an electron of velocity υ makes in traveling 1 cm in a gas at a pressure of 1 torr at 0° C, V is the applied potential to produce electron velocity υ, T is the absolute temperature in Kelvin, and p is the pressure in torr [4]. Since the value of P_C (V) is typically about 70, p must be < 314 torr if T is 300 °K and d = 50 μm. However, the device life can be increased in a better vacuum since ion bombardment is further reduced.

In addition to a sharp emitter, an optimum field emission device requires other features: (1) for emitters of the same radius, emission increases with smaller half angle [5]; (2) a low work function emitter helps to enhance electron emission [6]; (3) a high melting point emitter helps to withstand high temperature caused by resistive heating [7]; (4) a small gate opening for a gated emitter structure helps to increase the electric field [8]; (5) the dielectric film applied between electrodes should have high dielectric strength and the film should be thick in order to maintain the necessary operating voltage without breakdown or significant leakage; (6) a planar gate electrode helps to reduce capacitance between gate and cathode; (7) a tall emitter helps to enhance electron emission [5].

Chapter 2 describes basic features and general concepts of field emission. Various existing approaches by other researchers to fabricate gated field emitters are also discussed. These approaches are self-aligned processes, which

align the gate opening to the emitter without using lithography. Chapter 3 deals with the fabrication of micro field emitters. Various approaches to form micro field emitters developed in this research are discussed and compared including the approach using oxidation sharpening, which generates emitters with radii < 10 Å. The effect of oxygen plasma on silicon tips also will be discussed. Chapter 4 extends the fabrication of micro field emitters in Chapter 3 to gated field emitter fabrication. A new self-aligned processing approach was developed in this research which forms (1) a gate opening less than 0.5 μm diameter without electron beam writing assistance, (2) a planar gate electrode, and (3) a thick dielectric layer for capacitance reduction. Special problems associated with the electron bombardment on the surface of material during the SEM (scanning electron microscope) examination also will be discussed. Chapter 5 investigates the characterization of the behavior of the gated field emission triodes fabricated in this research. Gate and collector currents were measured and I vs. V, I vs. t, Fowler-Nordheim (I/V^2 vs. $1/V$), and triode characteristics are determined. Chapter 6 gives the conclusions of this research. The Appendix describes the detailed processing parameters used in this research.

CHAPTER 2
FIELD EMISSION: BACKGROUND

This chapter describes some basic principles of field emission. Special attention is given to the role of emitter material, emitter geometry, and triode electrode geometry on field emission. Comparisons with existing devices such as thermionic emission devices and solid state microelectronic devices are also made and discussed.

2.1 History of Field Emission

The first field emission of electrons from sharp points was observed by Wood [9] in 1897. However, field emission was never well understood until Fowler and Nordheim applied quantum tunneling to explain and model this effect in 1928 [6]. In 1953, Dyke and Dolan reported the effect of morphology on emission and suggested that a vacuum arc was initiated by field emission [7] [10]. In 1961, Shoulders proposed the first vacuum microelectronic devices [11].

Nevertheless, the high packing density of micron-size emitters (6.4×10^5 tips/cm^2) was not available until Spindt used solid state process technology for fabrication in 1968 to make tips of 500 Å radius [12] and later in 1976 [13]. This device was fabricated with a defined gate electrode on a silicon substrate followed by a molybdenum evaporation to form a sharp emitter. The emitter was self-aligned to the gate with the gate opening about 1 μm in diameter. The emitter radius was 500 Å. The major features demonstrated were: (1) a packing density of emitters of 6.4×10^5 tips/cm^2; (2) sharp emitters with radius about 500 Å; (3) maximum currents in the range 50-150 μA/tip with applied voltage in the range of 100-300 volts when operated at pressure of 10^{-9}

torr; (4) more than 7000 hrs. operating lifetime. These experiments by Spindt inspired other researchers to further investigate field emission devices. About ten years later, the first international conference of vacuum microelectronics was held in Williamsburg, VA in 1988, which made a new landmark in vacuum microelectronics. Since then, field emission vacuum microelectronics has been intensively studied and rapidly developed.

2.2 Theory of Field Emission

Electron emission from a solid surface into a vacuum may be generated by several different ways such as thermionic emission (the electrons are thermally excited over the potential energy barrier), photoemission (the electrons are excited over the potential energy barrier by the incoming photons) and field emission [14-15]. In field emission, the electrons tunnel through the surface potential energy barrier, which has been thinned by the influence of a strong electric field. The surface potential energy E for a typical value of Fermi level E_F and work function ø is illustrated in Fig. 2.2.1 [16] where Z is the distance from metal surface, Z_c is the distance from the metal surface at which the surface barrier is zero, and Z_m is the distance from the metal surface at which the surface barrier is maximum.

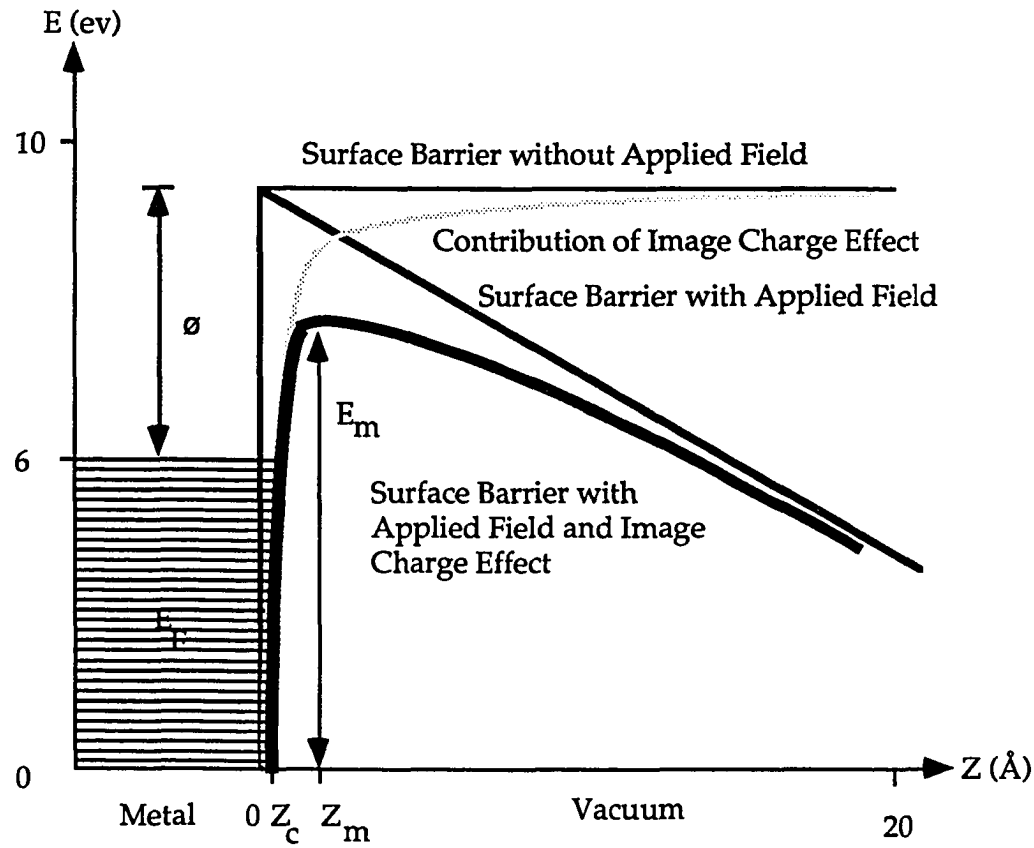


Fig. 2.2.1 The surface potential energy diagram for electrons at a metal surface in the presence of a strong electric field (bold solid line). This shaped potential energy is the results of the image potential energy (light line) and the strong electric field (solid line).

Since the image force F_i is $F_i = -e^2/4\pi\varepsilon 4Z^2$ (the image potential energy E_i is $E_i = -e^2/4\pi\varepsilon 4Z$) where ε is the permitivity in vacuum, the surface potential energy E(Z) in ev seen by an electron on the vacuum side of the metal-vacuum interface is asymptotically given by

$$E(z) \approx E_F + \text{ø} - \frac{e^2}{4\pi\varepsilon 4z} \qquad (2.2.1)$$

where E_F and ø are in ev. Eq. 2.2.1 is valid for Z > 3Å (i.e. Z_c = 3 Å). When an electric field F is applied to the surface, the surface potential energy seen by an electron changes into

$$E(z) \approx E_F + ø - \frac{e^2}{4\pi\varepsilon 4z} - eFz \qquad \text{for } Z > Z_c \qquad (2.2.2)$$

$$E(z) = 0 \qquad \text{for } Z < Z_c \qquad (2.2.3)$$

Therefore, the maximum surface barrier Em can be found

$$Em = E_F + ø - \sqrt{\frac{e^3F}{4\pi\varepsilon}} \text{ or} \qquad (2.2.4)$$

$$= E_F + ø - 3.79 \times 10^{-5}\sqrt{F} \text{ ev}$$

for F in v/m. The maximum surface barrier appears at Z_m where

$$Z_m = \sqrt{\frac{e}{4\pi\varepsilon 4F}} \text{ or} \qquad (2.2.5)$$

$$= \frac{1.9 \times 10^{-5}}{\sqrt{F}} \text{ m}$$

There are several equations describing field emission. One equation which derived by Fowler and Nordheim in 1928 [6] does not consider the barrier lowering by the image effect [17-18]. This form of the "Fowler-Nordheim" equation is given by

$$J(F) = 6.2 \times 10^{-6} \frac{\sqrt{E_F}}{(\phi + E_F)\sqrt{\phi}} F^2 e^{-6.8 \times 10^7 \phi^{3/2}/F} \qquad (2.2.6)$$

where current density J is in A/cm^2, electrical field F is in v/cm, Fermi level E_F and work function ø is in ev. Another equation is derived with consideration of the barrier lowering by the image effect [13] [19]. This modified Fowler-Nordheim equation is often used in the form

$$J(F) = \frac{1.54 \times 10^{-6}}{\phi\, t^2(y)} F^2 e^{-6.83 \times 10^7 \phi^{3/2} v(y)/F} \qquad (2.2.7)$$

where emission current density J is in A/cm^2, electric field F is in v/cm, work function ø is in ev, the Schottky lowering of the work function barrier $y = 3.79 \times 10^{-4} \sqrt{F}/\phi$. The functions v(y) and t(y) have been computed and shown in Fig. 2.2.2 [20]. The approximation 1.1 for $t^2(y)$ and $0.95 - y^2$ for v(y) can be applied in Eq. 2.2.7. It is clear from Eq. 2.2.6 (or 2.2.7) that the electric field dominants the current density. In other words, a strong electric field is a must in order to have high current density. It should be noted that a smaller r of an emitter not only means higher emission current density J but also indicates a smaller emitting area A. If the tip is too sharp, the emission current I may be decreased because of the smaller product of J and A. A simulation shows the maximum emission current is at r = 10 Å based on an extraction voltage of 30 volts, an extraction distance of 1 μm and a work function of 4.01 ev [21].

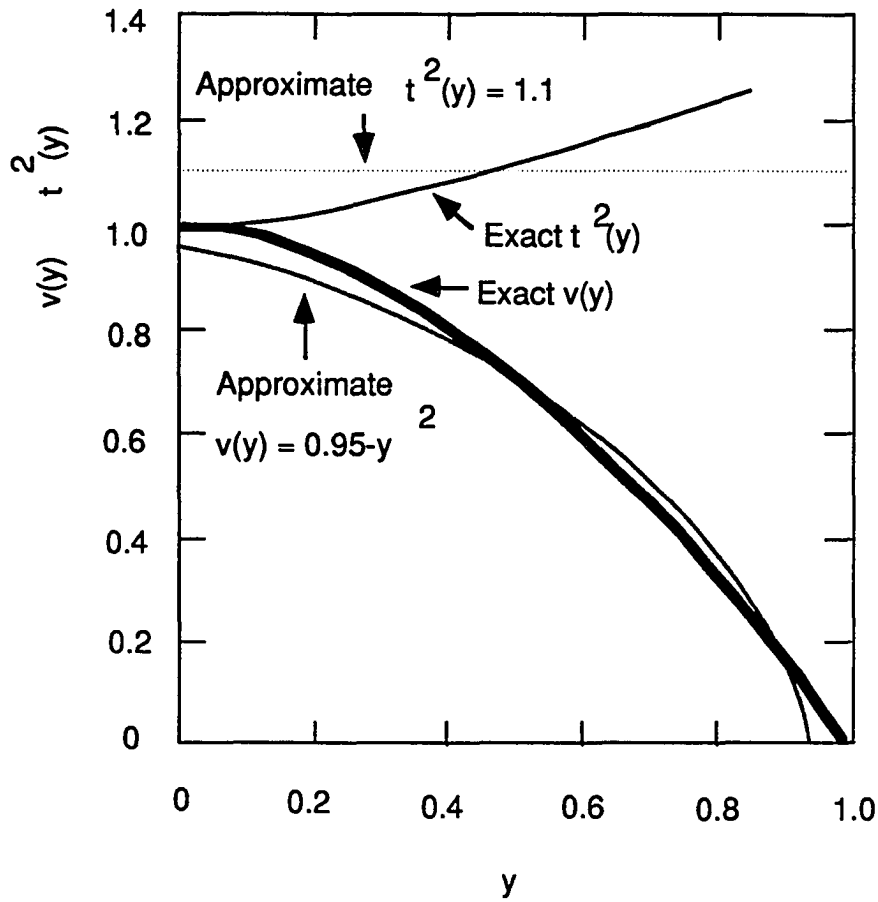


Fig. 2.2.2 Comparison of approximate forms with exact solutions for the Fowler- Nordheim field emission function v(y) and t^2 (y)

It also should be noted that the thermionic emission contribution to the emission current density becomes important when the temperature rises. In thermionic emission the metal is heated so that the electrons can be excited over the potential energy barrier. The equation of thermionic emission is given by

$$J(T) = 120\, T^2\, e^{-\frac{\phi}{kT}} \qquad (2.2.8)$$

where the emission density J is in A/cm^2 , absolute temperature T is in °K, work function ø is in ev and Boltzmann constant k is 8.625×10^{-5} ev/ °K [14]. For thermionic emission, temperature dominants the current density whereas electric field dominants the current density for a field emission. Fig. 2.2.3 shows the thermionic current emission and field emission regions for a range of temperature and applied field for a 4.5 ev work function emitter [16] [22]. This indicates that at sufficiently high field, the major emission is from field emission. But at sufficiently high temperature and low field, the major emission is from thermionic emission.

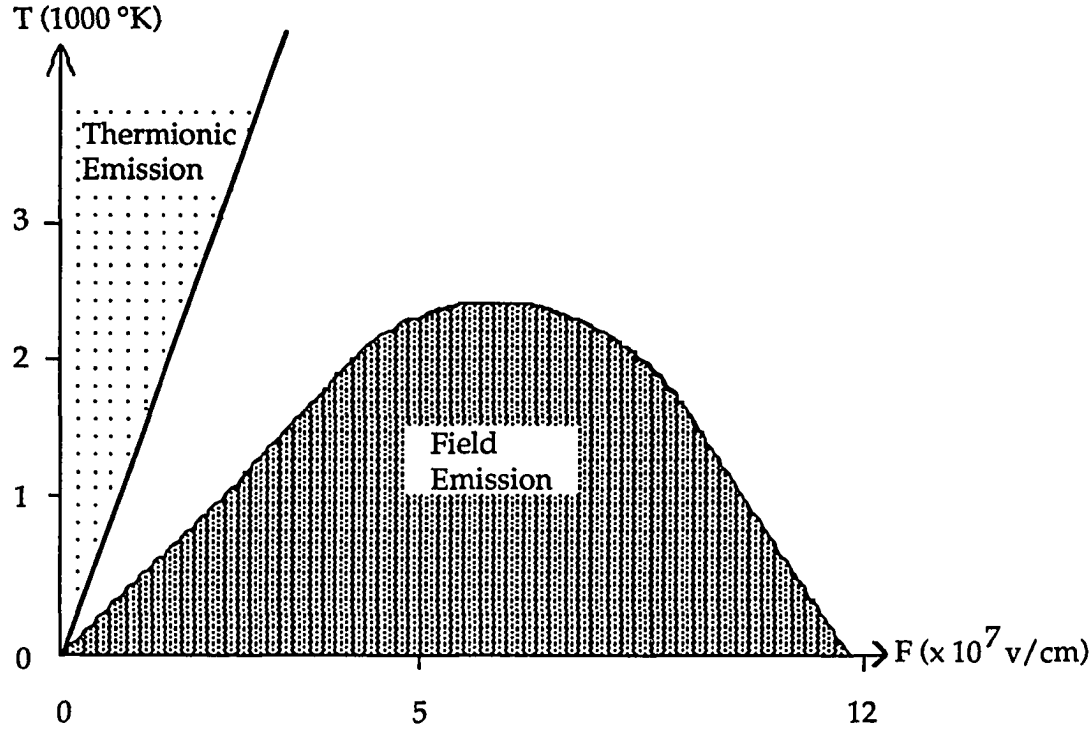


Fig. 2.2.3 Thermionic emission and field emission regions of temperature and applied field for a 4.5 ev work function emitter.

2.3 Field Emitter Materials

Many materials including semiconductors can be used as field emitters [23]. Ideally, the field emitter should be a material of high melting point to withstand more current, low work function to have more emission, and low vapor pressure to maintain necessary vacuum in a sealed device [24]. An emitter also should be sharp in order to have sufficient electric field for electron emission at a low voltage without causing dielectric breakdown. The

common emitters such as Si [25-30] , W [31-32], Mo [13] [33-34], LaB_6 [35-36], and Ta [37-38] used in field emission devices are listed in Table 2.3.1 along with some of their properties.

Table 2.3.1 The most common emitters used in field emission devices.

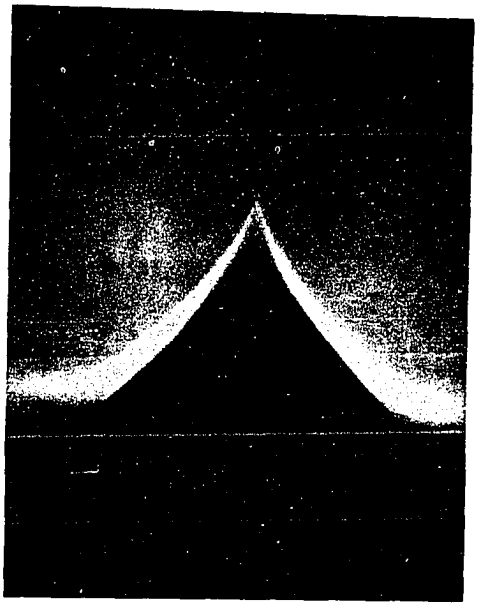
	Si	W	Mo	LaB_6	Ta
Melting Point (°C)	1410	3410	2617	> 1500	2996
Work Function (ev)	4.50	4.50	4.50	2.66	4.25
Vapor Pressure (torr)	10^{-6} at 1200°C	10^{-11} at 1800°C	$7x10^{-7}$ at 1800°C	–	$5x10^{-10}$ at 1800°C
Reported Emitter Radius (Å)	< 10 [30]	< 200 [31]	400 [34]	Not Available	< 200 [37]

Among these emitters tungsten has the highest melting point and the lowest vapor pressure, and silicon has the lowest reported emitter radius. Since

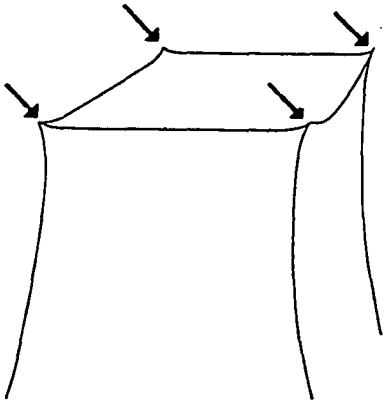
silicon can use standard semiconductor fabrication technologies to form sharp tips, it has been studied and used broadly as a field emitter in spite of its relatively low melting point and high vapor pressure compared to other materials such as W, Mo, and Ta.

2.4 Field Emitter Geometries

Field emitter structures can be in the shape of a cone, a wedge or a cylinder. The emitting region is a tip for conic type emitter, and an edge for the other structures. In order to increase the current density, each structure can have multiple emitters. Figs. 2.4.1.(a), (b), and (c) show the conic type [39], wedge type [40] and circular type [41] field emitters (arrows), respectively.

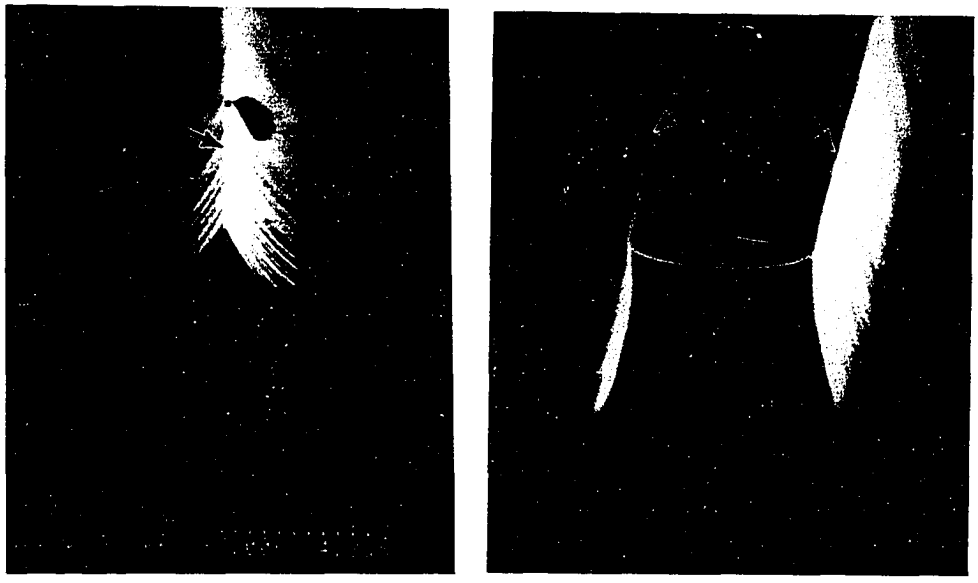


(Single Tip Emitter)



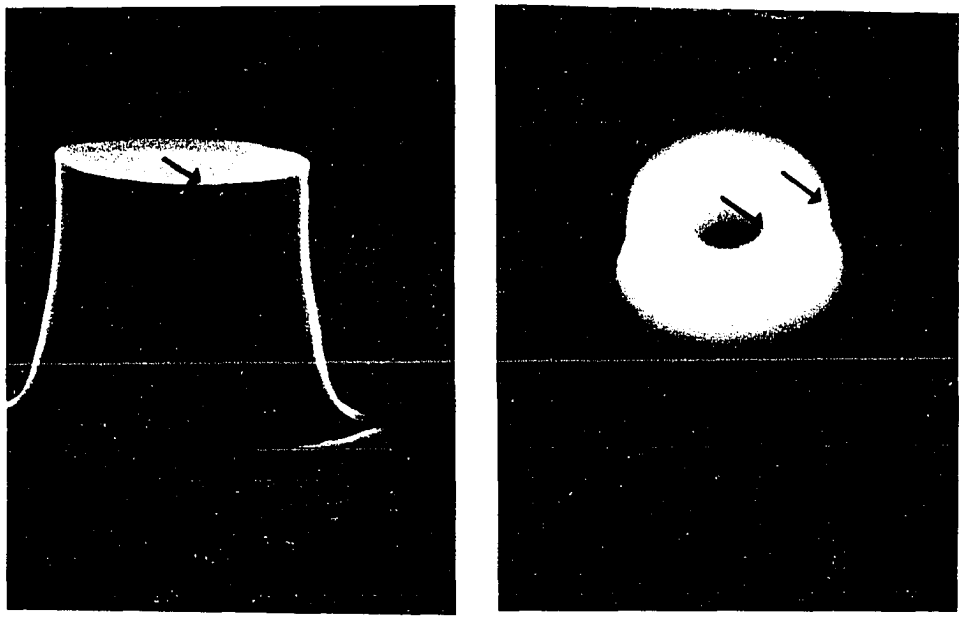
(Four Tip Emitters)

Figs. 2.4.1.(a) The conic type field emitters (arrows).



(Single Wedge Emitter) (Dual Wedges Emitters)

Figs. 2.4.1.(b) The wedge type field emitters (arrows).



(Single Circle Emitter) (Dual Circles Emitters)

Figs. 2.4.1.(c) The circular type field emitters (arrows).

2.5 Gated Field Emission Triode Geometries

Gated field emission triodes are formed by the addition of a third electrode (gate) between the collector and the emitter. The gate is usually much closer to the emitter than to the collector in order to control (or modulate) the electron emission which is from the emitter. The collector current depends on the voltage between the gate and the emitter Vge (which extracts the emission current from the emitter) and the voltage between the collector and the gate Vcg (which determines the distribution magnitude of emission current to the collector and to the gate). Fig. 2.5.1 shows a typical gated conic type field emission triode where r is emitter radius, θ is emitter half angle ,which is measured a distance r from the top of the emitter, d is diameter of the gate opening, h is the emitter height, δ is the tip elevation above the top edge of the gate, Scg is the space between the collector and the gate, Vge is the voltage between the gate and the emitter, and Vcg is the voltage between the collector and the gate. It should be noted that the electric field F is $F = f(r, \theta, d, h, \delta, Vge)$ and emission current density J is $J = f(F)$.

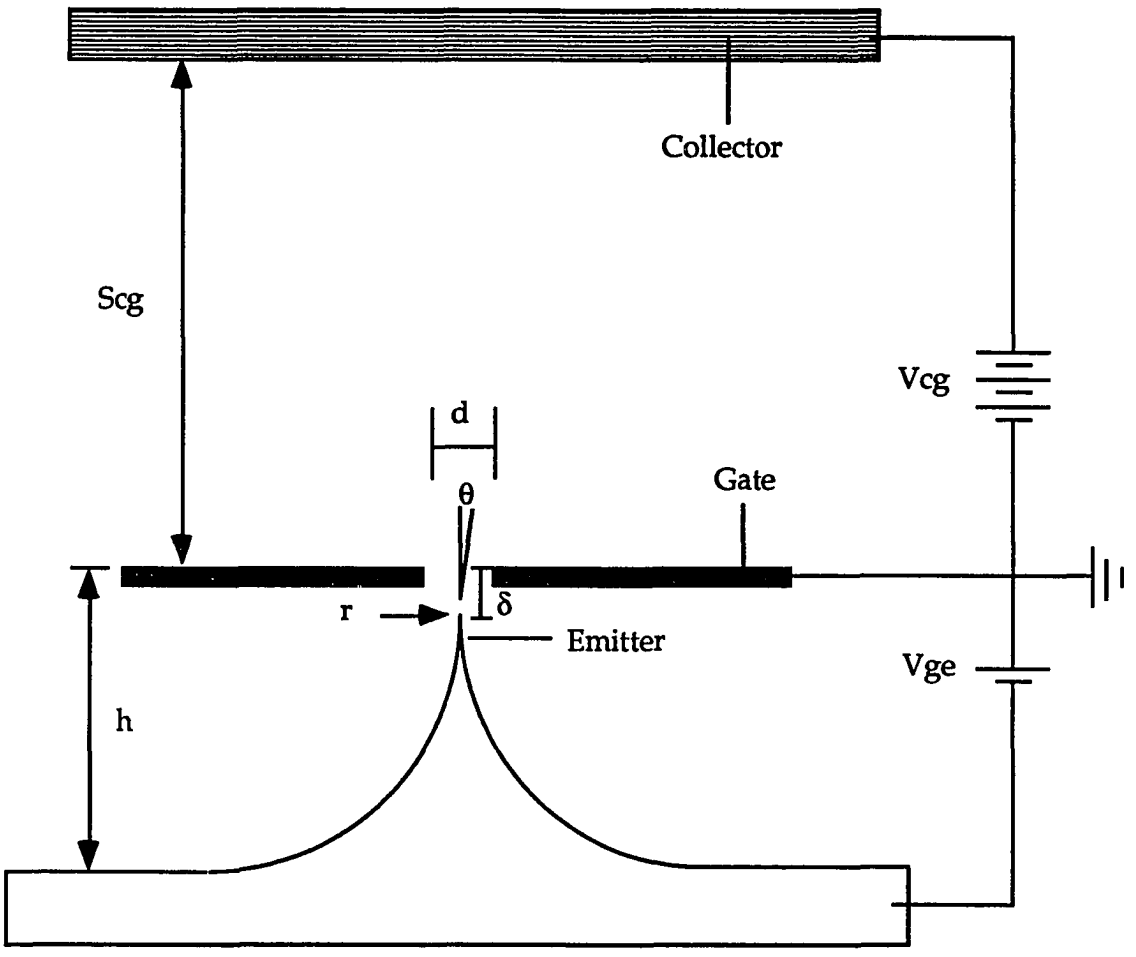
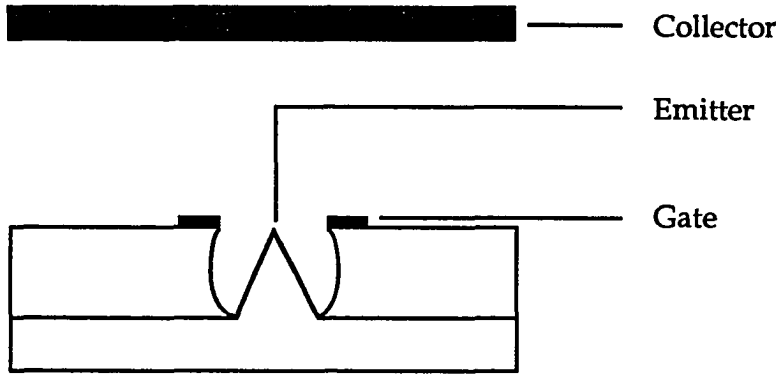


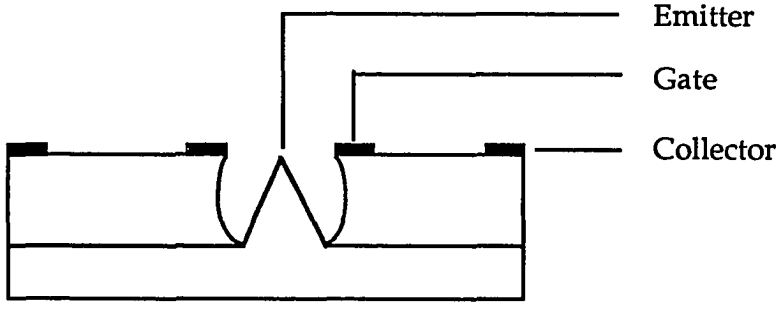
Fig. 2.5.1. A typical gated conic type field emission triode.

However, the collector, the gate and the emitter electrodes can be arranged in various configurations as shown in Fig. 2.5.2. The collector of the vertical triode is placed above the gate . The collector of the lateral and lateral edge-film triodes are placed on the same elevation level of the gate. The lateral edge-film triode is characterized by using the edge of a thin film as a linear emitter [30-31] [42-44]. Since the emitted electron must fly over the gate to reach the anode for lateral triodes or lateral edge-film triodes devices, the gate

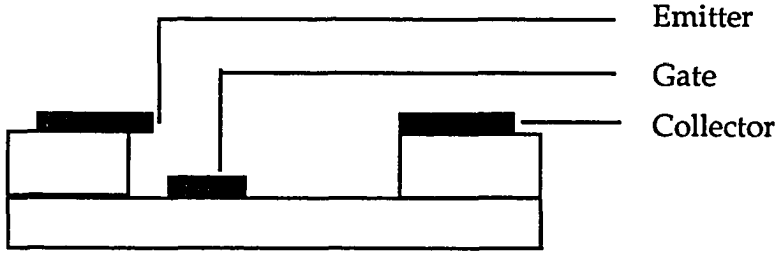
will receive more current than will the gate of vertical triodes for modest collector voltages. Modeling experiments show that the vertical triode collects more current than the collector of the lateral triode (or lateral edge-film triode) for the same operating conditions and the vertical triode has a higher transconductance and cut off frequency [45].



(I) Vertical Triode



(II) Lateral Triode



(III) Lateral Edge-Film Triode

Fig. 2.5.2 Typical triode configurations.

2.6 Fabrication Approaches for Gated Field Emitters

Many approaches has been developed to fabricate gated field emitters by other researchers. In this section three existing approaches will be discussed. These fabrication approaches are all self-aligned processes, which align either the emitter to the gate opening (Spindt approach) or align the gate opening to the emitter (shadow mask evaporation approach and resist etch back approach) without using lithography.

2.6.1 Spindt Approach

This approach fabricates the gate electrode followed by forming a sharp emitter by evaporation. The major fabrication steps are shown in Fig. 2.6.1.1 [12-13] and are described as follows:

(a) Define a gate opening.

1. Oxidize silicon wafer to have the desired thickness of silicon oxide.
2. Evaporate gate metal.
3. Spin resist on the gate metal.
4. Make a resist pattern in a desired configuration and transfer pattern to gate metal. The pattern typically is a disc.

(b) Define a silicon oxide opening.

1. Remove resist.
2. Etch silicon dioxide down to silicon base by hydrofluoric acid (HF) and form a silicon dioxide opening.

(c) Form lift-off layer.

1. Mount the sample to a substrate in an evaporation system and rotate the substrate about an axis perpendicular to its surface.
2. Evaporate aluminum (or alumina) at 15° angle to the surface of sample. The alumina layer serves as a layer for subsequent lift-off.

(d) Evaporate molybdenum at 90° angle to the surface of sample until the opening is closed. During the evaporation the size of the opening continues to decrease (because of condensation of molybdenum on its periphery) and a cone grows inside the cavity. Eventually, a sharp conic emitter is formed and self-aligned to the gate when the opening is completely closed.

(e) Dissolve aluminum (or alumina) layer and lift off molybdenum layer on the top of alumina layer. A self-aligned gated emitter therefore is formed.

This approach was the first successful method for fabricating gated field emitters. This type of emitter was first fabricated by Spindt [13] and it is known as the Spindt type emitter. There are two minor disadvantages to this approach: (1) Electron beam writing is required in order to form the gate electrode with a very small gate opening; (2) The emitter height is decided by the gate opening, and it is difficult to have a tall emitter with a small gate opening.

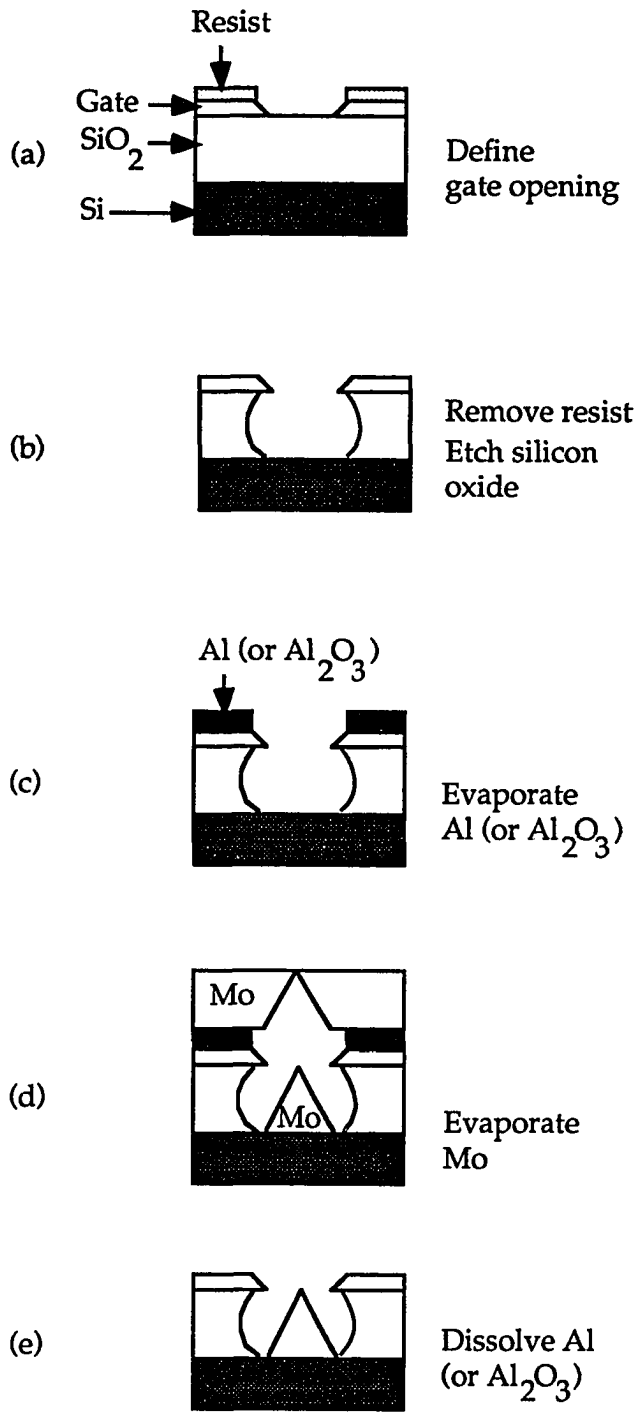


Fig. 2.6.1.1 The major fabrication steps of the Spindt approach [12-13].

2.6.2 Shadow Mask Evaporation Approach

This approach uses the initial mask used during tip formation to also serve as a shadow mask during deposition of dielectric and gate films. The major fabrication steps are shown in Fig. 2.6.2.1 [27][29] and are described as follows:

(a) Define a silicon dioxide pattern.

1. Oxidize silicon wafer to have the desired thickness of silicon dioxide.
2. Spin resist on the sample.
3. Make a resist pattern in a desired configuration and transfer pattern to silicon oxide. The pattern typically is a disc.
4. Remove the resist.

(b) Etch silicon by either dry etching or wet etching until the silicon beneath the silicon oxide mask is thin enough (usually is less than 2000 Å) but with the silicon oxide mask still in place.

(c) Oxidize silicon. The new thermal oxide then becomes continuous with the oxide mask.

(d) Deposit silicon oxide and gate metal. The oxide and gate metal are self-aligned to the silicon oxide mask during the deposition.

(e) Dissolve silicon oxide by buffered hydrofluoride (BHF) solution. A self-aligned gated emitter is formed.

There are three minor disadvantages with this approach: (1) The emitter height and gate opening are controlled by the same mask and therefore it is not easy to have a tall emitter with small gate opening. (2) Electron beam

writing is required for small gate opening. (3) This process does not permit the use of metal tips or metal coated silicon tips.

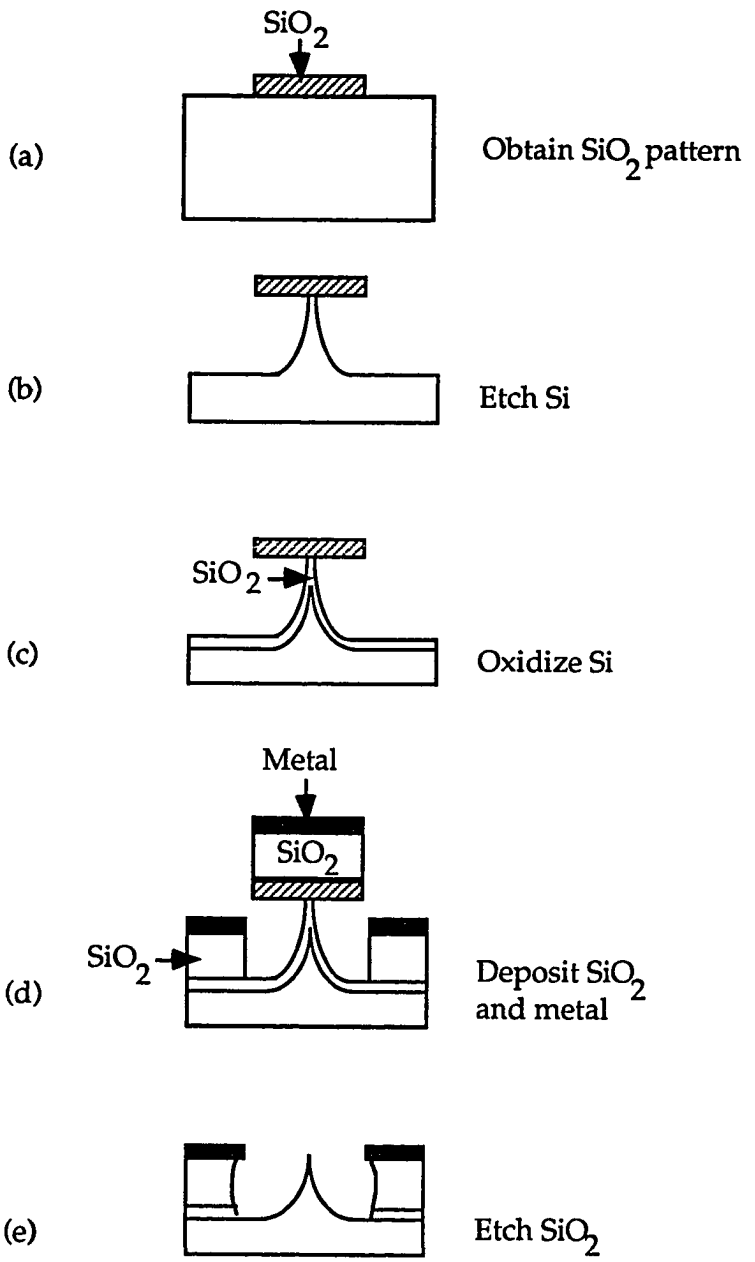


Fig. 2.6.2.1 The major fabrication steps of shadow mask evaporating approach [27][29].

2.6.3 Resist Etch Back Approach

This approach uses a sacrificial resist for etch back followed by formation of a gate opening. The major fabrication steps are shown in Fig. 2.6.3.1 [46-47] and are described as follows:

(a) Start with a metal-silicon oxide-polysilicon emitter structure. This may be obtained by the following "molding/casting" process:

1. Etch a <100> silicon substrate through a square silicon nitride mask by potassium hydroxide (KOH) until a pyramidal cavity is formed. The width of the opening determines the depth of this self-limiting anisotropic etching.

2. Oxidize silicon to have a pinhole free oxide etch barrier.

3. Deposit ("cast") polysilicon to the silicon "mold" with a thickness of several hundred microns.

4. Selectively etch silicon over the silicon oxide to remove the " mold" leaving the polysilicon substrate and a polysilicon emitter is formed.

5. Deposit chemical vapor deposition (CVD) silicon oxide and gate metal.

(b) Spin resist on the top of gate metal to planarize the surface.

(c) Etch back resist until the desired elevation level is reached. The etching back exposes the gate metal over the emitter only.

(d) Form the gate.

1. Etch out the exposed metal, followed by etching out the metal-uncovered silicon oxide.

2. Remove resist, leaving a self-aligned gated field emitter.

One disadvantage with this approach is that the leakage current from gate to emitter can be serious and the capacitance can be high when a small gate opening is required, since a small gate opening requires a thin dielectric layer.

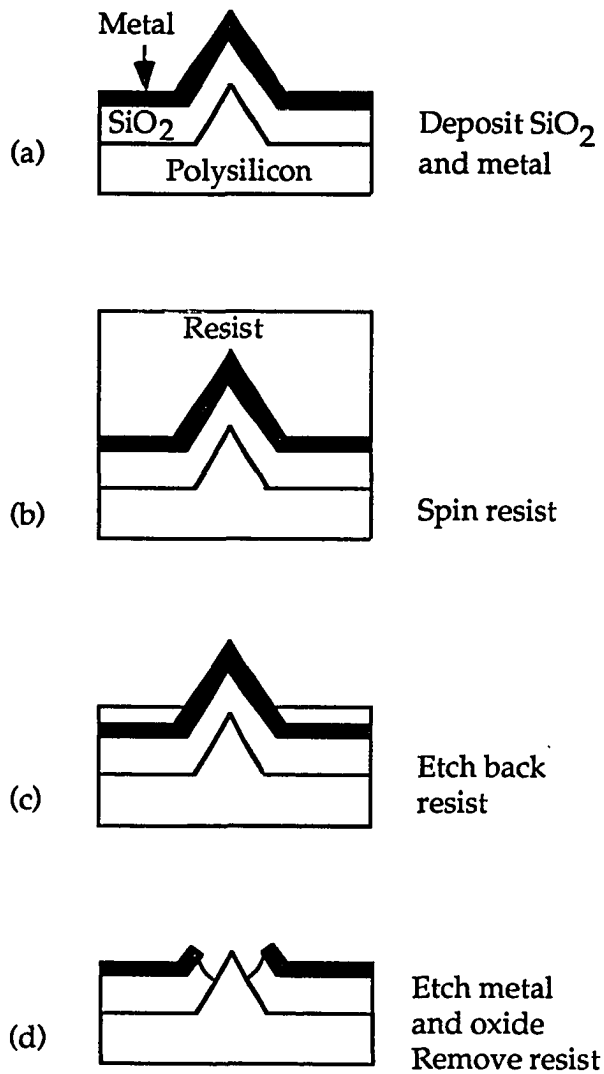


Fig. 2.6.3.1 The major fabrication steps in resist etch back approach [47][64].

2.7 Comparison of Field Emission Vacuum Microelectronics Technology with Other Technologies

Compared with thermionic devices (where electron emission is caused by thermal excitation), field emission vacuum microelectronics devices (FEVMD) have four major advantages as follows:

(1) The efficiency of thermionic emission is low and therefore thermionic devices consume more power.

(2) In thermionic devices, preheat time is needed in order to have a hot cathode and generate emission, and this can be a disvantage in some applications.

(3) FEVMD permit higher integration (higher packing density) than thermionic devices since more heat dissipation occurs with thermionic devices and a larger surface and volume per device must be provided in order to maintain a reasonable operating temperature.

(4) Since the emitters of thermionic devices are operated at high temperature (typically above 1500°C), less thermal degradation is expected from the emitters of FEVMD which operate at room temperature.

Compared with solid state microelectronics devices (SSMD), FEVMD have three major advantages as follows:

(1) Since electrons are emitted in vacuum with ballistic velocity, FEVMD have the potential to operate at higher speed (theoretically to 3×10^{10} cm/sec. and practically to 6-9 $\times 10^{8}$ cm/sec.) [48] compared with the limiting saturation

velocity of electrons in SSMD (most semiconductor velocities are limited to values less than 5×10^7 cm/sec.) [49].

(2) FEVMD have relatively wider operating temperature range than SSMD devices, which are limited to temperature where the intrinsic carrier concentration is less than the doping level (typically 200°C in silicon).

(3) Since radiation can result in SSMD electron-hole pair generation and trapping and affect the resistivity of substrate current paths, can produce lattice displacement, and can cause voltage breakdown and affect other features of device performance [50-53], SSMD are not suitable for use in a hostile radiation environment. FEVMD are expected to be less sensitive to radiation.

However, the FEVMD have two drawbacks as follows:

(1) The emitters are vulnerable during the fabrication processing. Many processes often used in the typical semiconductor fabrication process such as blowing nitrogen to speed-up drying, or using oxygen plasma for descumming, will easily destroy the emitter.

(2) The emission is sensitive to the surface condition of the emitter. A clean emitter surface is generally required to have reliable field emission.

CHAPTER 3
FABRICATION OF MICRO FIELD EMITTERS

Sharp field emitters are needed in order to permit electron emission at moderate voltage. Sharp field emitters can be produced in many ways such as anisotropic etching of silicon in KOH (potassium hydroxide) solution [44] [46] [54-55]; isotropic etching of silicon in HNO_3 (nitric acid) : CH_3COOH (acetic acid) : HF (hydrofluoric acid) solution [56]; RIE (reactive ion etching) [57]; ion milling [58]; evaporation [13]; MOCVD (metal organic chemical vapor deposition) [59]; oxidation and some of the above in combination [37][39-40][57].

However, oxidation is the only way reported that is able to generate atomically sharp silicon field emitters. During oxidation, the preliminary structure is sharpened due to the slower rate of surface reaction at the tip than at the sidewall [60]. The faster surface reaction rate at the sidewall results in more silicon being consumed than at the tip and consequently the emitter is sharpened [60]. In this chapter various approaches developed in this research for forming micro field emitter are described and compared. At the end of this chapter the effect of oxygen plasma on silicon is discussed.

3.1 Silicon Tip Formation: RIE, Wet Etching Followed by Oxidation

The method we have developed to fabricate atomically sharp silicon field emitters consists of two stages. In the first fabrication stage, C_2F_6 (hexafluoroethane) RIE is used to define the silicon oxide pattern; the silicon is etched to give a straight wall structure; finally the silicon is isotropically etched in 95ml HNO_3 : 3ml CH_3COOH : 2ml HF (the NAH solution) in order to obtain a preliminary structures [30][39][56]. In the second stage, the

preliminary structures are sharpened at the top by a dry oxidation technique which is known to sharpen convex structures [30][39][61]. The major fabrication steps are described in Figs. 3.1.1 and 3.1.2; the photographs shown in Figs. 3.1.2 were taken by the scanning electron microscope at 20 kv with a Hitachi S-800.

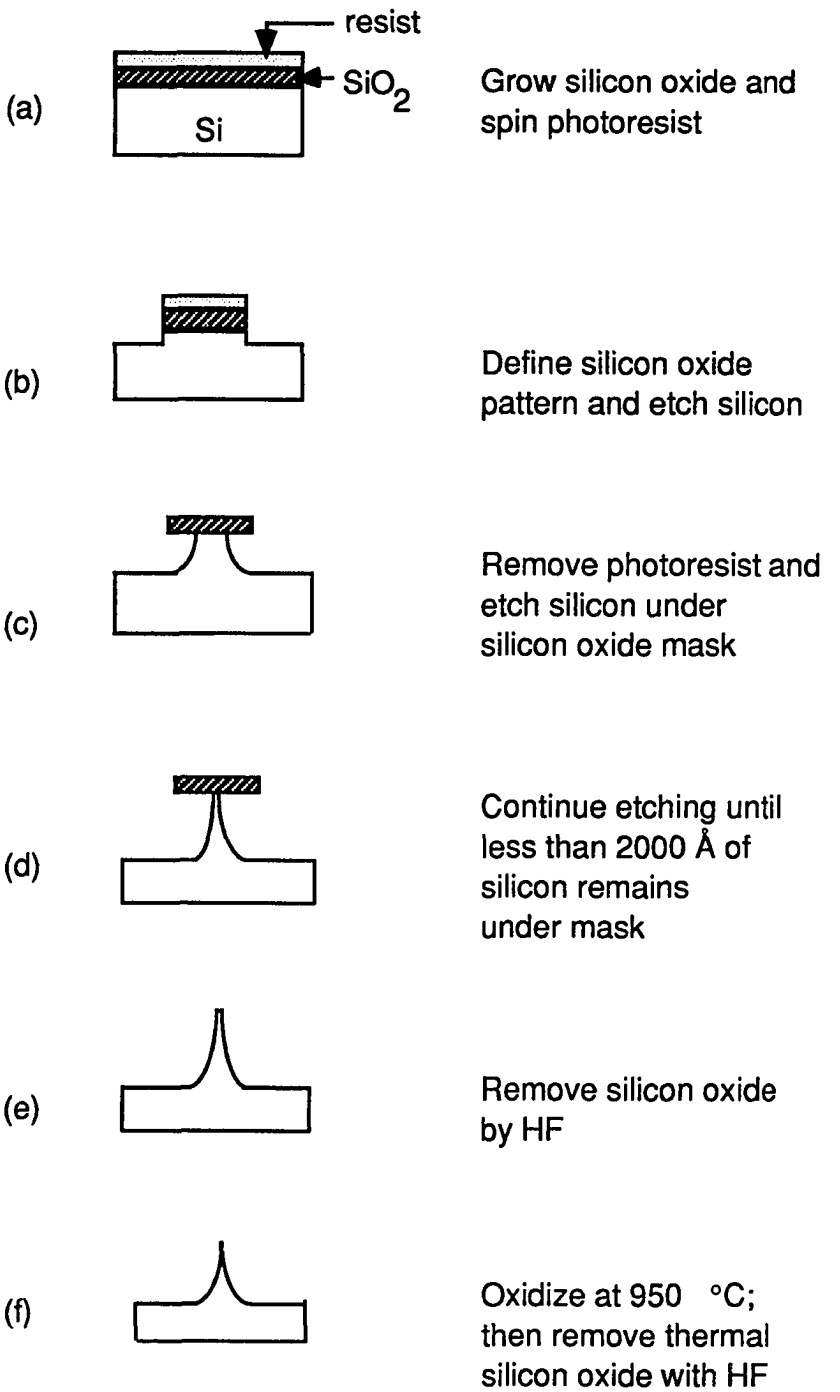


Fig. 3.1.1 The major steps to fabricate atomically sharp silicon field emitters.

(a) Oxidize a silicon sample at 1050°C for 2 hrs. in oxygen to grow a 1500 Å thermal oxide; follow this step by spinning photoresist on the surface.

(b) Define silicon oxide pattern.

1. Use lithography to transfer a pattern into resist. The pattern typically consists of 2-4 μm diameter discs.

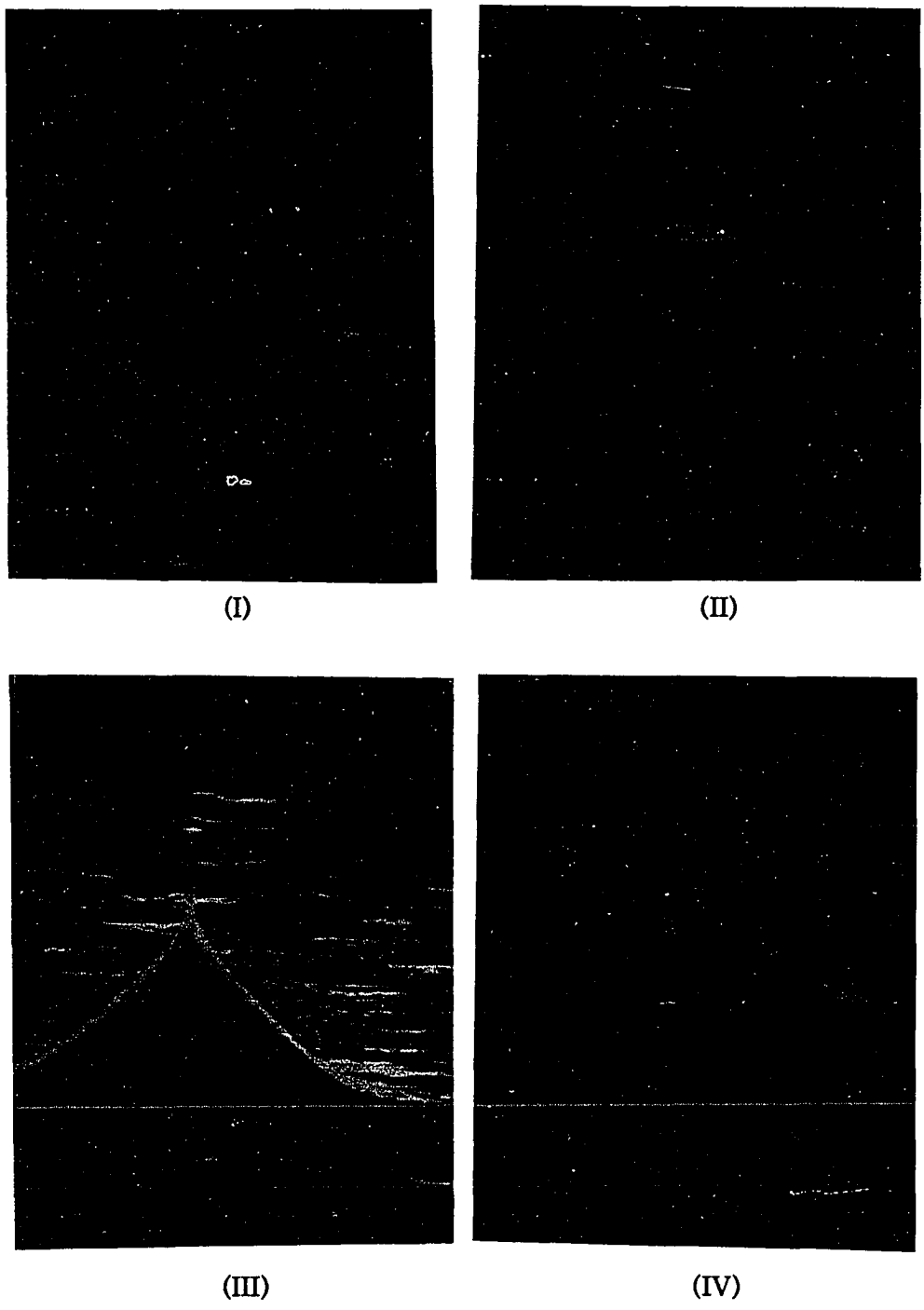
2. Transfer photoresist pattern to silicon oxide and etch silicon by RIE, followed by resist removal. The etching is performed by C_2F_6 gas using a 30 sccm (standard cm^3/min.) flow rate, 300 mtorr gas pressure, and at 100 W of RF power. The etching rate ratio for silicon : silicon oxide : photoresist (AZ 5214E) is 1: 2: 2 and the silicon etch rate is 160 Å/min.

(c) Remove the photoresist and etch the silicon under a silicon oxide mask in the NAH solution. It should be noted that during the etching the etching rate of silicon increases as the diameter of the silicon disc decreases.

(d) Continue etching until the diameter of the silicon disc which supports the silicon oxide mask is decreased to around 1000 - 2000 Å. Typical etch time for a 2 μm mask is 3 min..

(e) Remove the silicon oxide mask by HF.

(f) Oxidize at 950°C and then remove silicon oxide with HF. This step may be repeated a few times to obtain an atomically sharp emitter. The oxidation period typically was 5.5 hrs. each time. Each time after oxidation the oxide is removed by HF. Final oxide stripping is done in HF which is used not only to remove the oxide but to passivate the silicon tips against further oxidation [62].



(I) (II)

(III) (IV)

Figs. 3.1.2 (I), (II), (III), and (IV) SEM photographs corresponding to Figs. 3.1.1 (b), (c), (e), and (f), respectively.

Reactive ion etching with C_2F_6 for 35 min. was used to transfer the photoresist (AZ 5214E) pattern to silicon oxide, and 5000 Å silicon was etched to give the structure shown in Fig 3.1.2.(I). This etched silicon wall is used to obtain a tip more needlelike during the latter oxidation. Silicon was etched by the NAH solution for 2 min 15 sec. to give the structure shown in Fig. 3.1.2.(II). The width of the silicon supporting the mask is around 8500 Å. Fig. 3.1.2.(III) shows the structure after an accumulated etching time of 3 min. 30 sec. and after the silicon oxide mask removal. Fig. 3.1.2.(IV) shows the sharpen emitter with around 1 μm height after 5.5 hrs. of oxidation in oxygen at 950°C followed by silicon oxide removal. The emitter height is approximately 1/2 of the diameter of the oxide mask feature. The emitter with a relative long stalk as shown in the Fig. 3.1.2.(IV) is typical for this fabrication approach.

Transmission electron microscope (TEM) specimens were prepared from the sharp silicon emitters. The specimens did not need further thinning since the tips of the emitters were already electron transparent. A sample was mounted on its side on a 3 mm diameter molybdenum ring using silver paste for ease of removal, and the ring mounted in the TEM with the emitter axes perpendicular to the electron beam. The sharpened emitters were studied at 400 Kv with a JEOL 400 FM [39] and a typical TEM image is shown in Fig. 3.1.3.

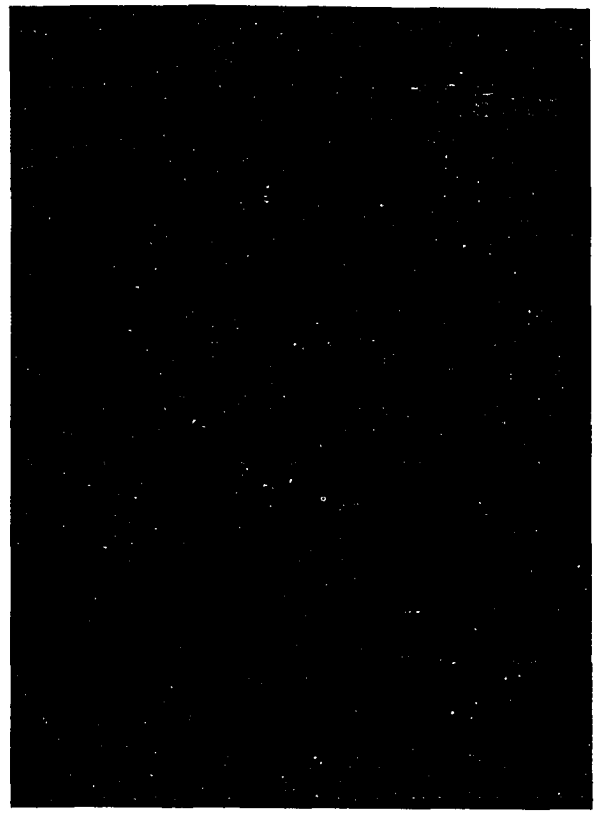


Fig. 3.1.3 High magnification TEM image of sharp emitter after removal of the thermal oxide.

The lattice image were obtained by aligning the electron beam along a silicon <110> direction. Since the space d between the {111} planes given by $d=\frac{A_O}{\sqrt{3}}$, where Ao is the lattice constant of silicon, the silicon {111} planes with a spacing 3.13 Å can be observed in the micrograph. The emitter radius was found to be less than 10 Å. The fringe contrast disappears when the tip diameter is less than 10 Å because there are too few atoms left to scatter the incident electron beam. The amorphorus image outside of the lattice image,

which has around 20 Å thickness can be a native oxide or polymerized hydrocarbon grown inside the TEM during electron beam bombardment.

Oxidation sharpening is based on an experimental study which found a 30% decrease in oxide thickness at silicon step edges following wet oxidation at 900° - 1050°C [61]. Modeling studies showed this effect to be due to an increase in the activation barrier to interfacial reaction caused by the stress build-up at these regions [60].

The classical model of planar oxidation of silicon [63] consists of two regimes. In the first regime the rate limiting step during oxidation is the interfacial reaction of an oxygen-containing species with the silicon surface and the reaction is linear. Beyond a critical oxide thickness (which depends on pressure and temperature), the rate limiting step becomes the diffusion of oxygen across the already grown oxide, and the reaction follows a parabolic rate law.

For a planar silicon surface these two mechanisms are quite sufficient to predict the oxide thickness, but at silicon wedges and other regions of high curvature, the stress built-up results in a suppression of interfacial reaction, and hence the oxidation rate slows down in the linear regime. The stress is largely a result of specific volume difference of silicon oxide with respect to the silicon which can not be relieved at temperatures less than 1050°C due to the high viscosity of the oxide which is appreciable below this temperature. For oxidation temperatures greater than 1050°C, the viscosity of the oxide is sufficiently low that the oxide can flow, relieving stress built-up. For this oxidation sharpening experiment, we used a temperature of 950°C.

To study the effect of differences in the preliminary structure morphology on the final configuration, various preliminary structures were prepared and followed by SEM during oxidation sharpening. The four preliminary structures were obtained by steps (a), (b) and (c) followed by continuous etching for 10, 20, 30 and 40 sec. (samples 48-9, 48-10, 48-11 ,and 48-12, respectively).

The results of the oxidation treatments of these different silicon preliminary structures are shown in Table 3.1.1 where r is the tip radius, and θ is the tip half angle (θ is measured at a distance r from the top of the tip). All four experimental samples were given three successive oxidations. Each oxidation was performed in dry oxygen for 5.5 hrs. at a temperature of 950°C. The radius and half angle are measured after the oxide is stripped off.

Table 3.1.1 The tip radii r and half angles θ for experimental samples.

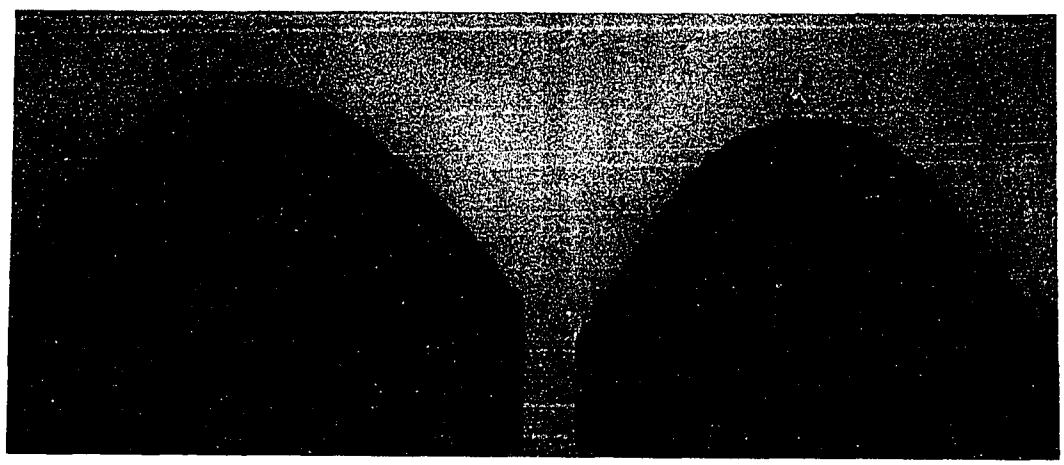
Samples	Preliminary Structure (Before Oxidation)		After First Oxidation		After Second Oxidation		After Third Oxidation	
	r (Å)	θ (°)	r (Å)	θ (°)	r (Å)	θ (°)	r (Å)	θ (°)
48-9	750	45	650	35	125	28	<50	23
48-10	1000	45	500	40	350	35	<50	25
48-11	2000	40	1750	30	600	25	<50	11
48-12	4000	36	2250	35	*		**	

* Becomes concave; circular sharp edge begins to form (see arrow).

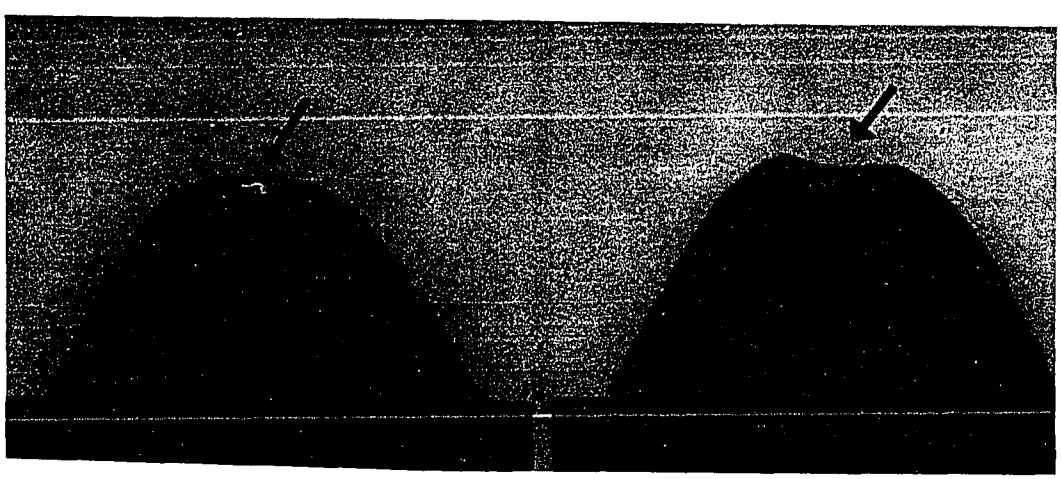
** More concave features occurs (see arrow).

It should be noted that the oxide was stripped off before the next oxidation. Table 3.1.1 shows that in general the radius and half angle became smaller as

oxidation treatments continue. However, not all preliminary structures become a single tips after oxidation treatments; sample 48-12 begins to form a circular sharp edge after two oxidation treatments. The SEM photographs of sample 48-12 in Figs. 3.1.4 shows the silicon morphology after each oxidation followed by oxide removal.



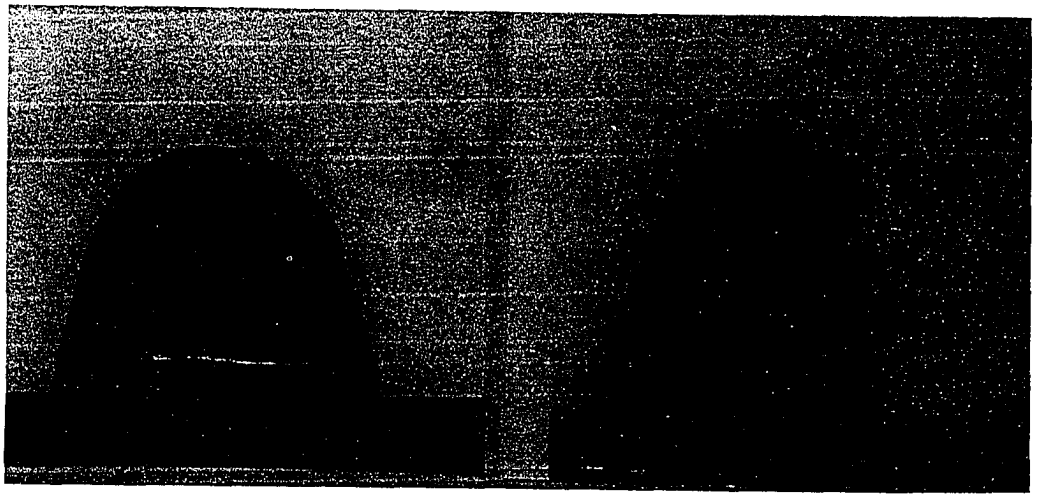
(I) (II)



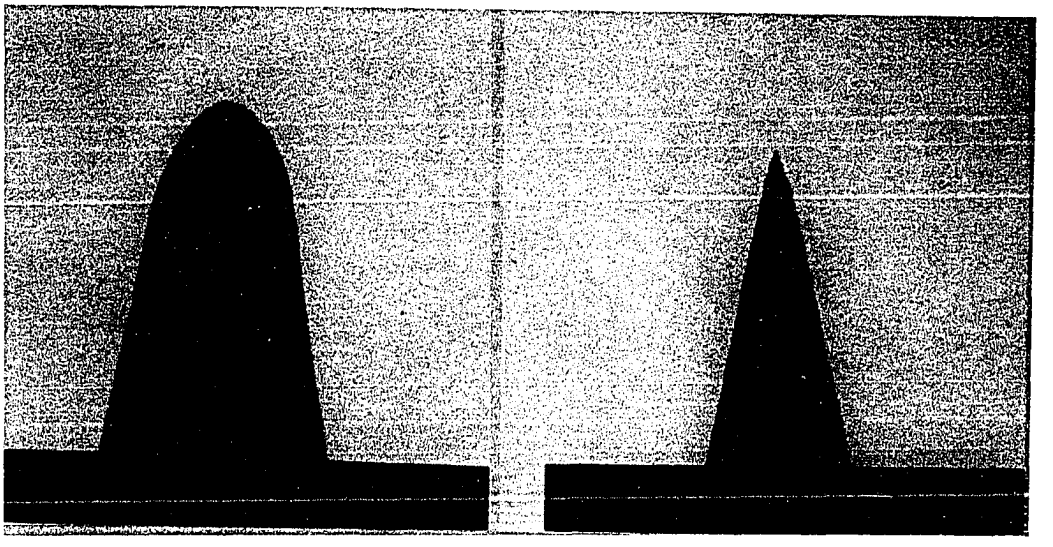
(III) (IV)

Figs. 3.1.4. The emitter morphology of sample 48-12 shown in (I) is before oxidation. Figs. (II), (III), and (IV) show the sample is after one, two, and three 5.5 hrs. oxidations followed by oxide removal, respectively. The beginning of a circular sharp edge can be seen in Fig. 3.1.4.(IV).

For most samples with $r < 2000$ Å and $\theta < 45°$, the preliminary structures are converted by oxidations to single sharp tips. Figs. 3.1.5 shows the silicon morphology of sample 48-11 after each oxidation followed by oxide removal. SEM studies show that tip radii are typically < 50 Å, and TEM studies show the radii are < 10 Å (see Fig. 3.1.3).



(I) (II)



(III) (IV)

Figs. 3.1.5.(I), (II), (III), and (IV) The emitter morphology of sample 48-11 shown in (I) before oxidation. Shown in (II), (III), and (IV) are after one, two, and three 5.5 hrs. oxidations followed by oxide removal, respectively.

These are typical results for morphology changes during the oxidation treatments described above. Further oxidation of the tip results in no change in the tip sharpness once atomic sharpness is achieved.

It is concluded that when $r < 2000$ Å and $\theta < 45°$, the preliminary structure can be a single sharp tip after oxidation. However, If the preliminary structure has $r > 4000$ Å, the preliminary structure will become concave and a circular sharp edge begins to form after oxidation.

3.2 Silicon Wedge Formation: RIE Followed by Oxidation

The fabrication of atomically sharp silicon wedges was demonstrated in this research using an approach based on RIE and dry oxidation [40]. The major fabrication steps to form silicon wedges for these studies are shown in Fig. 3.2.1. and are described as follows:

(a) Use an n^+-type (100) silicon sample and oxidize it in steam (water) at 1050°C for 1 hrs. to grow a 5000 Å thermal silicon oxide; spin photoresist on the surface.

(b) Define silicon dioxide pattern.

1. Photolithography. Rectangular patterns were used with a width of 2 μm and various lengths of 50 μm and 290 μm.

2. Transfer photoresist pattern to silicon oxide by BHF (buffered hydrofluoric acid).

(c) The silicon under the silicon oxide mask is etched down by RIE to form rectangular silicon bars. The etching is performed by a CF_3Br

(bromotrifluoromethane) gas with 15 sccm flow rate and 300 mtorr at an RF power of 100 W. The etching rate ratio for silicon : silicon oxide : photoresist (AZ 5214E) is 4 : 1 : 1 and the etching rate for silicon is 800 Å/min. [64]. The CF_3Br RIE used in this approach has higher silicon etching selectivity than the C_2F_6 RIE (see section 3.1). This higher silicon etching selectivity gives taller silicon structures which are better for field emission [5].

(d) Remove photoresist. Remove silicon oxide by HF. Figs. 3.2.2.(a) and (b) show an illustration and SEM photograph of part of a silicon bar, respectively.

(e) Oxidize in oxygen at 950°C; then use HF to remove silicon oxide. Sharp wedges are obtained.

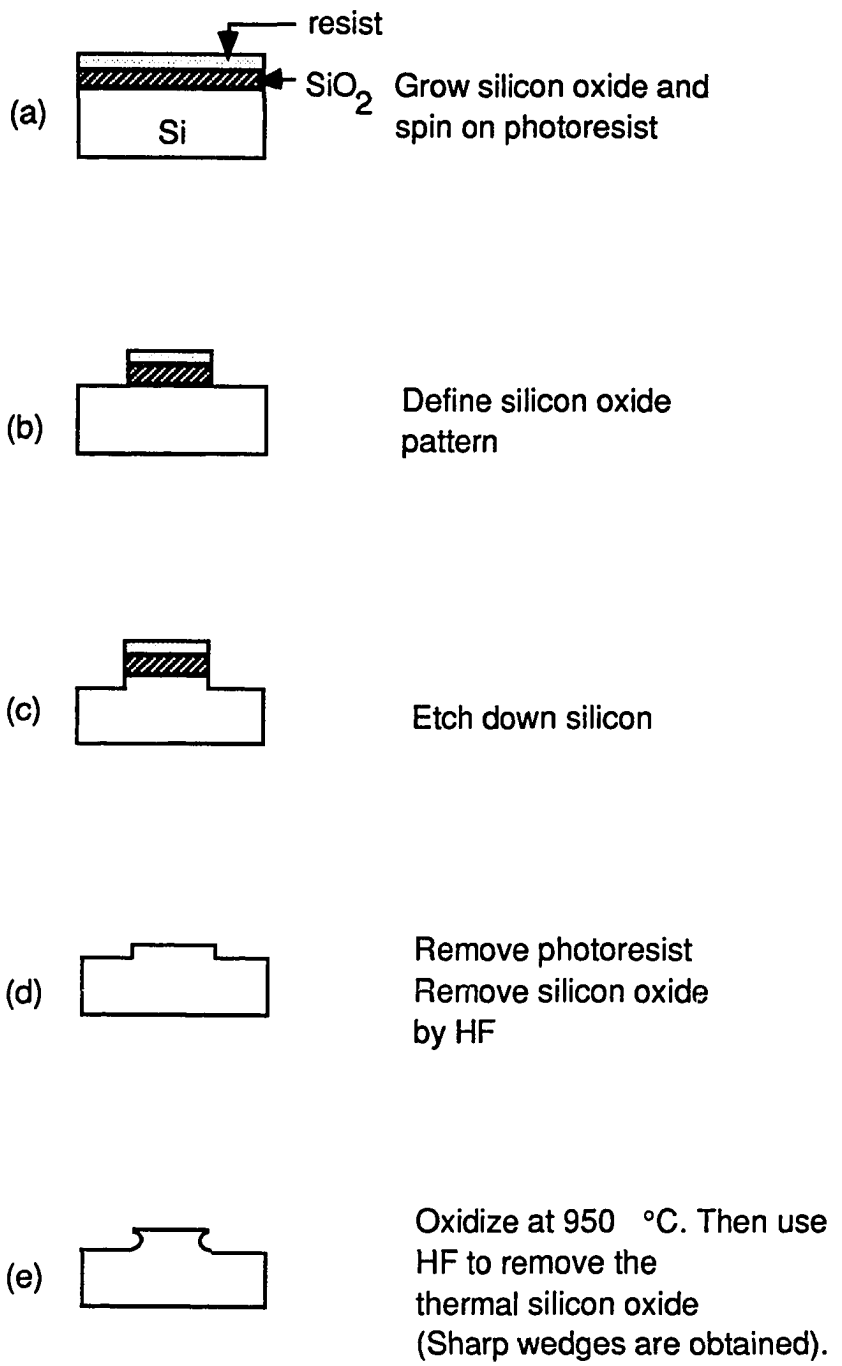


Fig. 3.2.1 The major steps to fabricate atomically sharp silicon wedge.

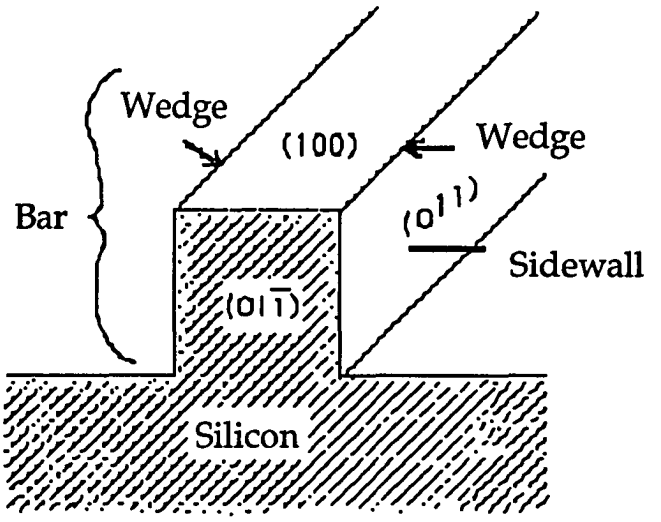


Fig. 3.2.2.(a) Illustration of part of a silicon bar used for these experiments. The wedges (arrows) are to be sharpened by oxidation treatment.

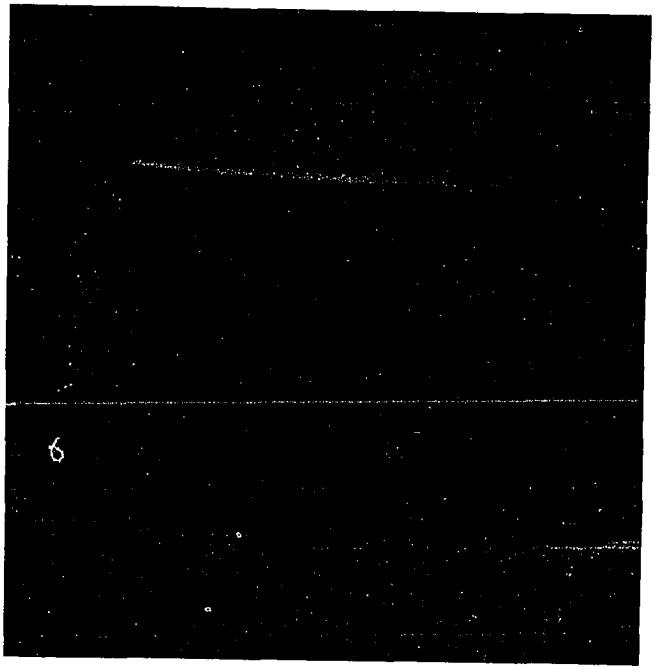


Fig. 3.2.2.(b) SEM photograph of part of a silicon bar.

The effect of oxidation on the morphology at the wedge was studied at low magnification by SEM and at high resolution by TEM. For TEM study, thin cross-section samples were made by standard techniques [65]. Wedge morphology was characterized by wedge radius and half angle. Comparisons of wedge radii and half angles after oxidation treatments in oxygen are listed in Table 3.2.1 where T is the oxidation temperature, t is the oxidation time, and d_{oxide} is the nominal thickness of silicon oxide grown on a planar silicon surface..

Table 3.2.1 Wedge radii and half angles for experimental samples.

Sample	T (°C)	t (hr.)	d_{oxide} (nm)	Wedge Radius (nm)	Wedge half angle (°)
1[a]	——	——	——	50.0	45
2	980	10.0	200	4.0	40
3	950	2.5	60	5.0	50
4	950	11.0	200	5.0	55
5[b]	950	2.5	60	1.0	30

a. Sample 1 received only RIE without oxidation.

b. Sample 5 received two oxidations and each oxidation was at 950° C for 2.5 hrs..; after the first oxidation the oxide was removed by HF and the second oxidation was performed.

Before oxidation (after RIE), the wedge radii and wedge half angles were observed to be approximately 50 nm and 45°, respectively (sample 1). The round silicon corner produced by RIE is probably due to the very thin taper of the oxide mask at the edge, and the loss of oxide protection during RIE. Nevertheless, the radii of the wedge-shaped samples after oxidation became much smaller as shown in Figs. 3.2.3 and 3.2.4. It is concluded that wedges with 1 nm radii can be made by oxidation(s) at 950°C.

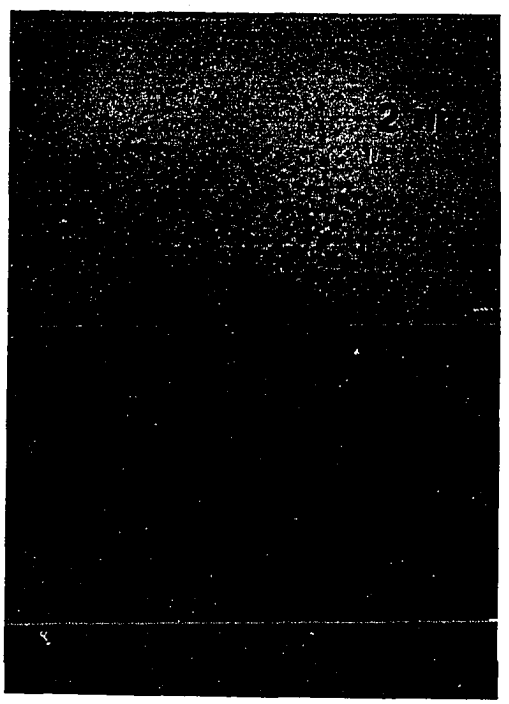


Fig. 3.2.3 High magnification TEM micrograph of a cross section of a wedge after 950°C, 2.5 hrs. oxidation (sample 3). The wedge radius and half angles are 5.0 nm and 50°, respectively.

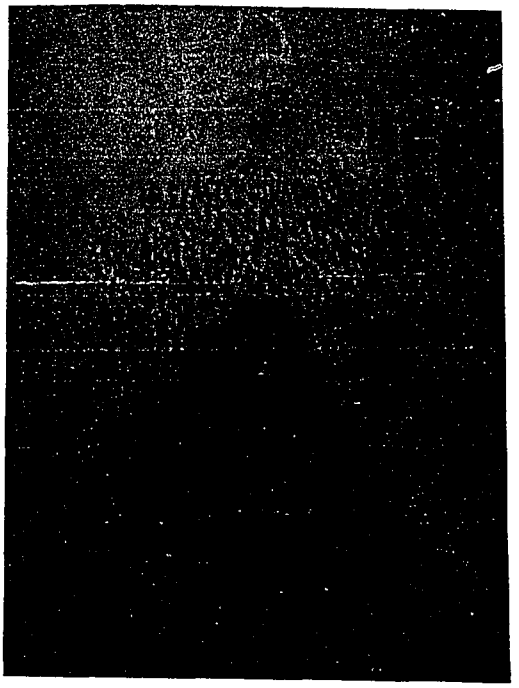


Fig. 3.2.4 High magnification TEM micrograph of a cross section of a wedge after repeated oxidation at 950°C (sample 5). The wedge radius and half angles are 1.0 nm and 30°, respectively.

3.3 GaAs Wedge Formation: RIE Followed by MOCVD

We have described an oxidation method to sharpen the silicon tips and wedges. However, GaAs also has potential to be used as a field emitter. Sharp GaAs wedges can be formed by MOCVD on n^+-type (100) GaAs samples. The major fabrication steps are best described with the aid of Fig. 3.3.1.

(a) Spin photoresist on surface.

(b) Photolithography. The pattern typically is a rectangular bar 2 μm x 50 μm with the long sides aligning along the <011> or <011> direction on (100) oriented GaAs substrate [59].

(c) GaAs, selectively protected by photoresist, is etched by RIE to form a rectangular GaAs bar, as shown in Fig.3.3.1. The etching is done with BCl_3 (borontrichloride)/argon mixtures with 90% argon and 15 mtorr pressure at 50 watt power (300 V). The etching ratio for GaAs to photoresist is 9 to 1 and the etching rate for GaAs is 280 Å/min. [66].

(d) Remove photoresist.

(e) Grow MOCVD GaAs on GaAs substrate until the GaAs wedge is formed. The MOCVD growth of GaAs is performed by TMG (trimethylgallium) and arsine at 650°C and at atmosphere pressure. The growth rate is 1300 Å/min [59].

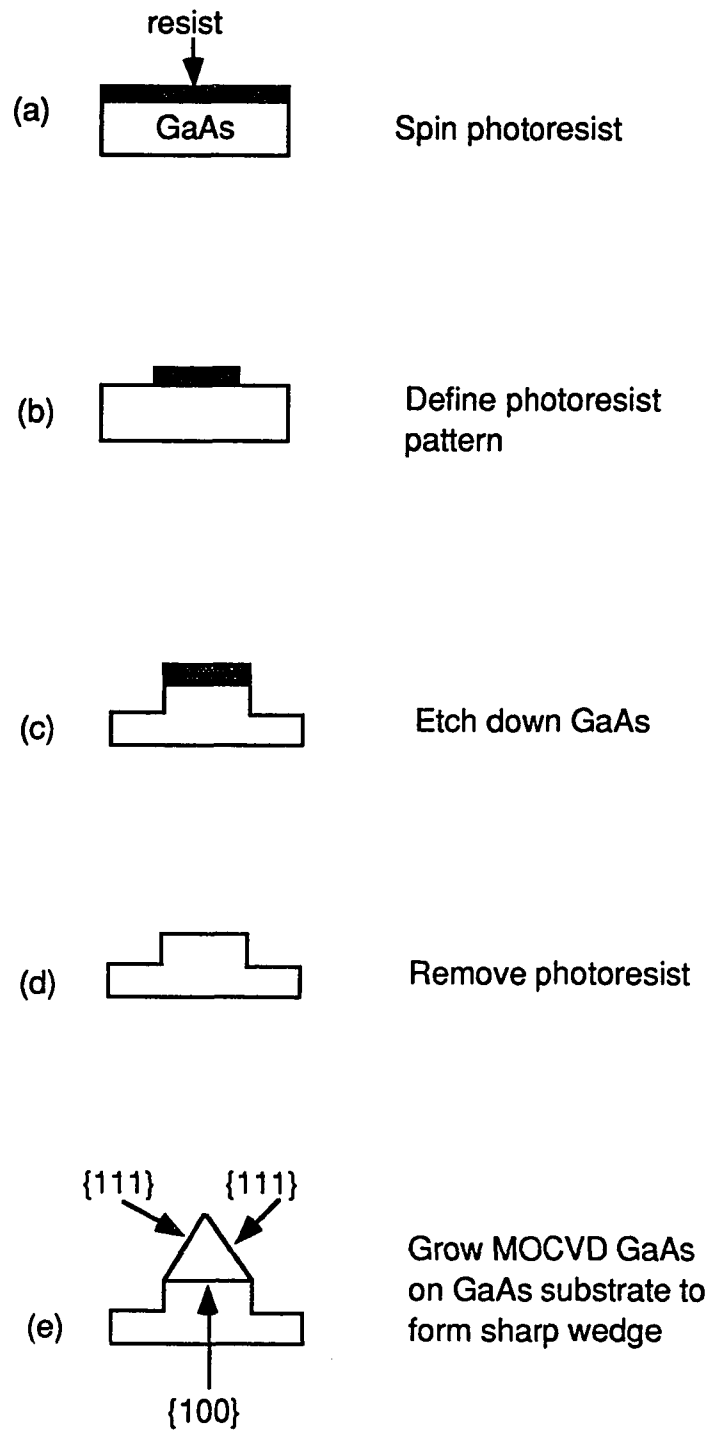


Fig. 3.3.1 The major fabrication steps of MOCVD approach.

Fig. 3.3.2 shows a low magnification SEM photograph of GaAs wedges after MOCVD GaAs growth. The wedge half angle is determined by the crystallography of the intersection of {111} planes and is 35.5°. No growth is observed on the {111} planes. It is seen as well that the growth on the edge stops once the two {111} planes meet and a sharp wedge is formed.

Fig. 3.3.2 A low magnification SEM photograph of GaAs wedges after MOCVD growth on GaAs rectangular bars.

Fig. 3.3.3 Shows a high magnification SEM photograph of a typical GaAs wedge. The radius of the wedge is approximate 400 Å. Since the surface of crystal growth is diffusion-enhanced when a growth surface, (100) plane, is adjacent to a non-growth surface, (111) plane, [67] the wedge radius could be made smaller if the diffusion-enhancement could be reduced. A lower MOCVD operating temperature which reduces the effect of diffusion-enhancement could be a method for getting a smaller radius.

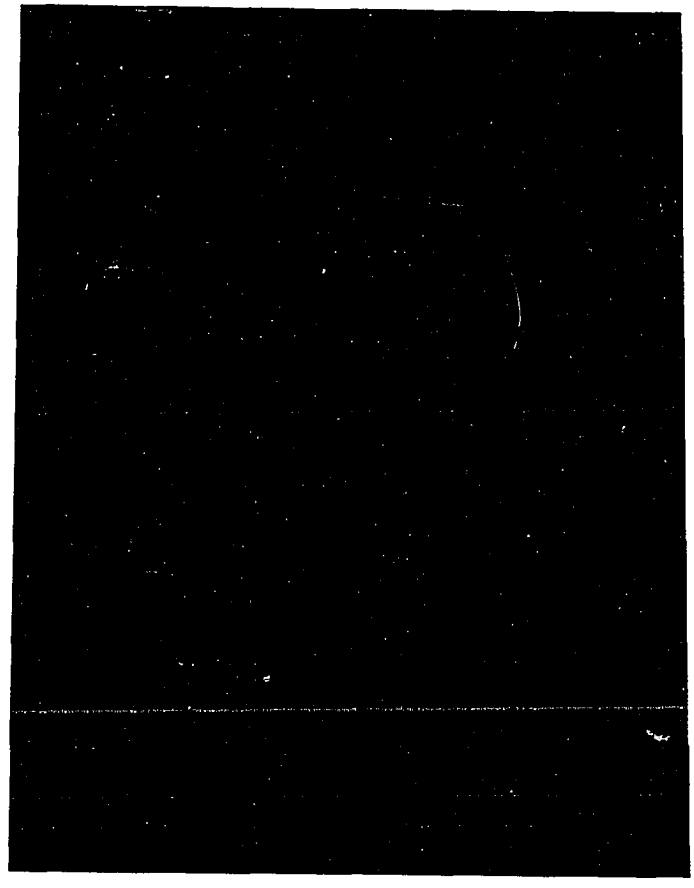
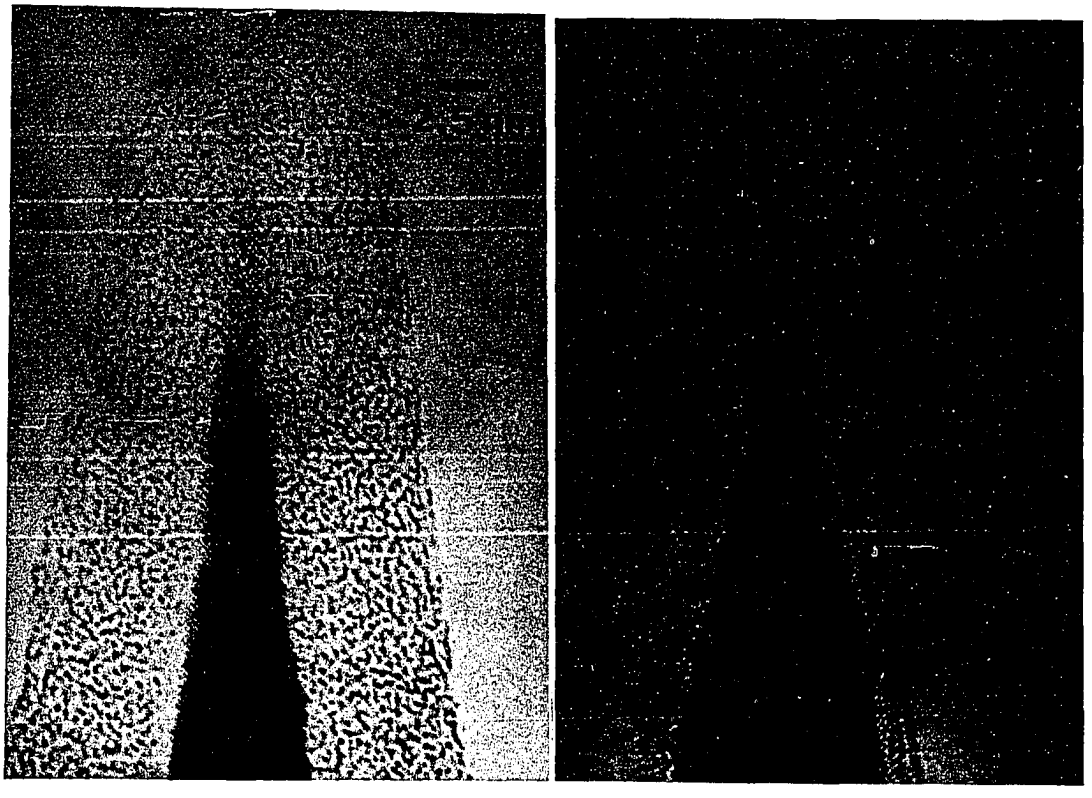


Fig. 3.3.3 A high magnification SEM photograph of GaAs wedge after MOCVD GaAs growth on a rectangular GaAs bar.

3.4 Effect of Oxygen Plasma on Silicon Tips

Oxygen plasma is a helpful aid in cleaning device surfaces. However, the effect of oxygen plasma cleaning on a silicon tip was not known. A silicon tip was treated with oxygen plasma at 50 watts of power for 5 min., and the results are shown in Figs. 3.4.1.



(a) (b)

Figs. 3.4.1.(a) and (b) A high resolution TEM micrograph of silicon tip before and after oxygen plasma, respectively.

It is concluded that oxygen plasma cleaning, which is often used in semiconductor processing to descum the surface, can attack the silicon tip.

CHAPTER 4
FABRICATION OF GATED MICRO FIELD EMITTERS

As we described in section 2.5, gated field emitters are needed in order to control (or modulate) the electron emission. This chapter will describe a new self-aligned process, discuss some properties of dielectric films and describe the fabrication of gated micro field emission devices. Special problems associated with electron bombardment of the device material during the SEM examination also will be discussed.

4.1 A New Self-Aligned Process

A new self-aligned processing approach was developed in this research. This process starts from field emitters, which can be Si or GaAs (as described in chapter 3) or metal or metal coated tips, and ends up with gated field emitters. Two different dielectric films (dielectric I and dielectric II) are used in this process to control the gate opening (by dielectric I) and planarize the surface (by dielectric II), respectively; this is followed by gate metal deposition, removal of the metal from the emitters by etching back or by anodic etching. The major steps, as shown in Fig. 4.1.1, are as follows [68]:

(a) Obtain an emitter which either is Si, GaAs, metal or metal coated tip, etc.. The Si conic tip and GaAs wedge tip can be acquired as described in chapter 3. The metal coated tip can be formed by evaporating metal on a tip.

(b) Form the first dielectric layer (dielectric I) which will control the gate opening. The diameter of gate opening is determined by the thickness of the dielectric on the sidewalls.

(c) Spin on the second dielectric layer (dielectric II), which planarizes the device surface.

(d) Etch back dielectric II to a desired level which exposes dielectric I as required. The dielectric II surface provide a planar substrate for the gate.

(e) Etch back dielectric I to form the gate opening and moreover to undercut the dielectric II layer, which enable the dielectric II to perform as a shadow mask for the following gate metal deposition. At this step dielectric II serves as an etching mask for dielectric I.

(f) Directionally deposit the gate metal with a desirable thickness. The thickness deposited at this step and the extent of etching performed in step (d) determine the elevation of the tip above the gate. The dielectric II layer is used as a shadow mask during the gate metal deposition.

(g) Remove the gate metal from the tip. There are two methods to remove the gate metal from the tip. (1) Anodic etching: A non-polar solution of tetrabutylammonium bromide (TBAB) in a acetonitrile is used as the electrolyte. This etching does not damage the emitter. Alternatively anodic etching can be done in 10% HCl (hydrochloride) solution. (2) Etch back: Since the gate metal is thinner at the tip region than on the gate area because of the slope of the tip side wall, controlled etching can be used to removed the gate metal from the tip while keeping gate metal on the gate area.

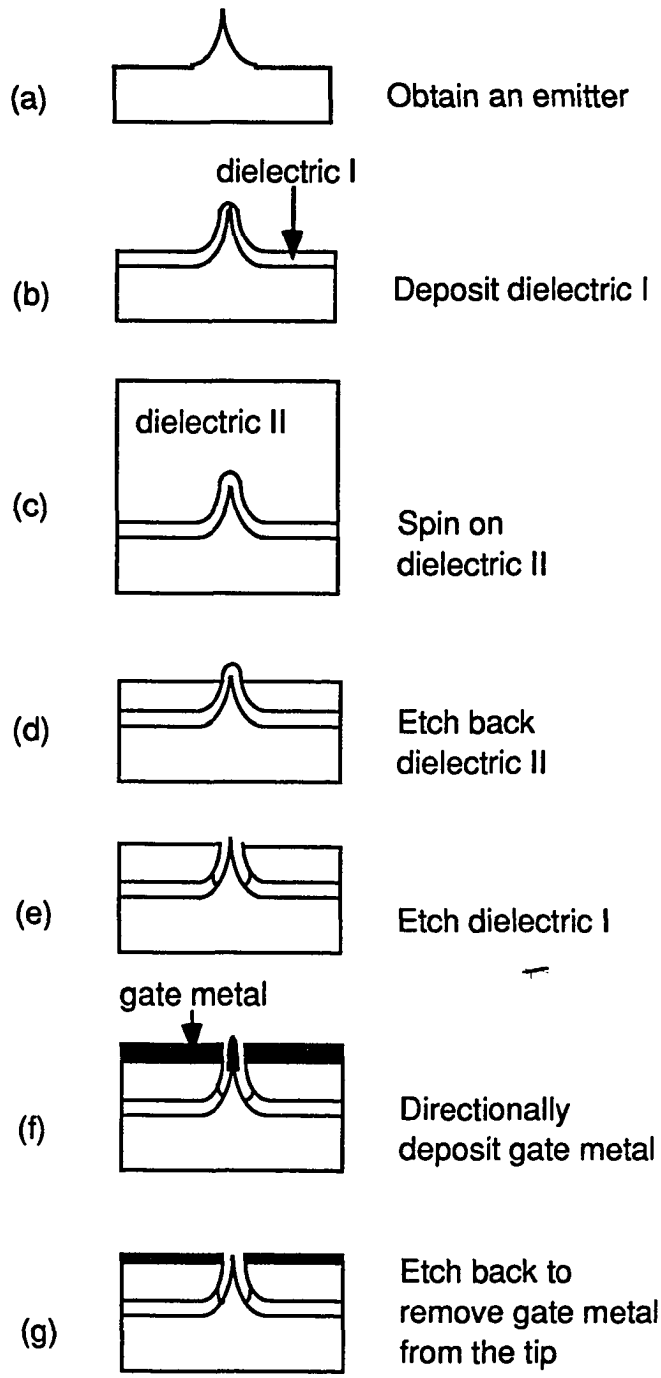


Fig. 4.1.1 The major fabrication steps of this new self-aligned process.

Using these procedures, we have obtained self aligned gated field emitters with the diameter of the gate opening equal to $2\ t + u_{si} - 2\kappa$, where t is the thickness of dielectric I at the sidewall of emitter, u_{si} is the diameter of the silicon cone at that height, and κ is the thickness of the gate metal at the edge of dielectric II.

This process using typical semiconductor processing technologies provides five main advantages over other methods for forming the gate electrode: (a) the gate is planar; this helps to reduce capacitance between the gate and the emitter. (b) The gate opening can be made with a diameter below 0.5 μm without electron beam writing assistance; a small gate opening helps to increase electron emission. (c) A thick dielectric can be used between gate and cathode simultaneously with a small gate opening; this helps to maintain the necessary operating voltage and also to reduce capacitance between the gate and the emitter. (d) Si, GaAs, metal or metal coated tips, etc. can be used in this process; and (e) the gate opening is self-aligned to the tips; this puts the tip in the center of the gate opening to the tip without lithography.

4.2 Dielectric Films Considerations

In the processing steps discussed in section 4.1, two dielectrics (dielectric I and II) are needed. In principle, there are four requirements for these dielectrics: (1) ability to form a stable coating of less than a few microns thickness; (2) ease in deposition; (3) compatibility with the rest of the process steps; (4) high dielectric strength. However, the high dielectric strength is particularly important in order to maintain the necessary applied voltage between the gate and the emitter with low leakage current and low capacitance. The dielectric leakage current must be small compared with the expected value for

the operating (collector) current (for a field-emission display application, the operating current is less than 0.1 μA/tip [69]).

Two dielectric films have been evaluated for dielectric I. (1) CVD silicon oxide; (2) Thermal silicon oxide. Thermal silicon oxide grown in oxygen at 950°C is part of the procedure for forming atomically sharp tips. For dielectric II, two dielectric films also have been evaluated: (1) Spin on glass (S.O.G.) : S.O.G. is made from a ladder siloxane made by Owens-Illinois (resin GR 650) [70]; (2) polyimide: The polyimide used in these experiment is made by National Starch and Chemical Corporation (Thermid 6800-92) [71].

Properties of these materials were explored in order to determine their suitability for the process steps outlined in Fig. 4.1.1. The CVD silicon oxide is grown by silane, nitrous oxide and argon at 300°C, and thermal silicon oxide was grown by oxidation in oxygen at 950°C. The S.O.G. was spun on for 30 sec. at 4k (4 thousand) rpm (rotation per minute), and cured for 30 min. at 130°C; the polyimide was spun on for 30 sec. at 4k rpm, and was first cured at 230°C for 30 min. followed by final cure at 400°C for 30 min.. The temperature for the final polyimide cure was gradually increased at the rate of 2°C/min. from R.T. to 400°C.

Leakage currents were measured at 140 V between gate electrodes (area= 3.12 $x10^5$ μm^2 per electrode) and the silicon substrate (gate positive) and results are shown in Figs. 4.2.1.(a) and (b). Fig. 4.2.1.(a) shows the leakage current densities of polyimide and S.O.G.; and Fig. 4.2.1.(b) shows the leakage current densities of thermal silicon oxide, and CVD silicon oxide. The leakage current of S.O.G is about two orders of magnitude less than that of polyimide at 100 volts applied voltage and at a dielectric thickness of

14000 Å. For the 8000 Å films, the leakage current of the polyimide significantly increases at voltages above 10 volts whereas the S.O.G. is much more resistive. Those results show that the S.O.G. film has lower leakage current than does the polyimide. Fig. 4.2.1.(b) shows that the thin thermal silicon oxides (1800 Å and 3600 Å films) have less leakage current than does the thicker (4300 Å) CVD silicon oxide film. This indicates that the thermal silicon oxide has a lower leakage current than does the CVD silicon oxide as expected [72].

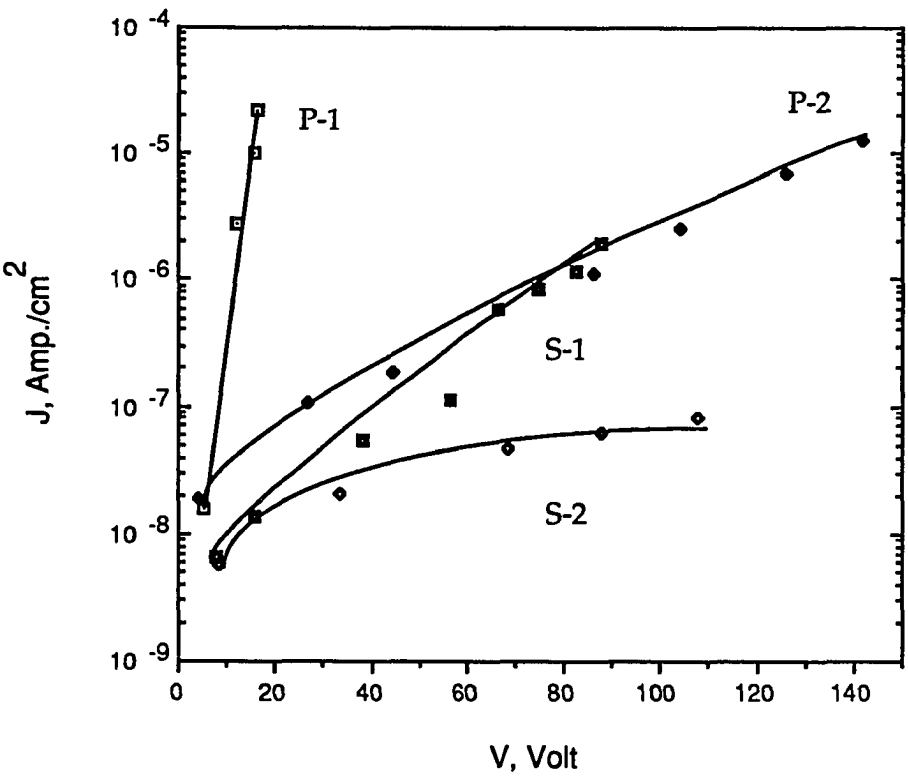


Fig. 4.2.1.(a) The leakage current densities plots of polyimide with thickness 8000 Å (P-1) and 14000Å (P-2), S.O.G. with thickness 8000 Å (S-1) and 14000 Å (S-2).

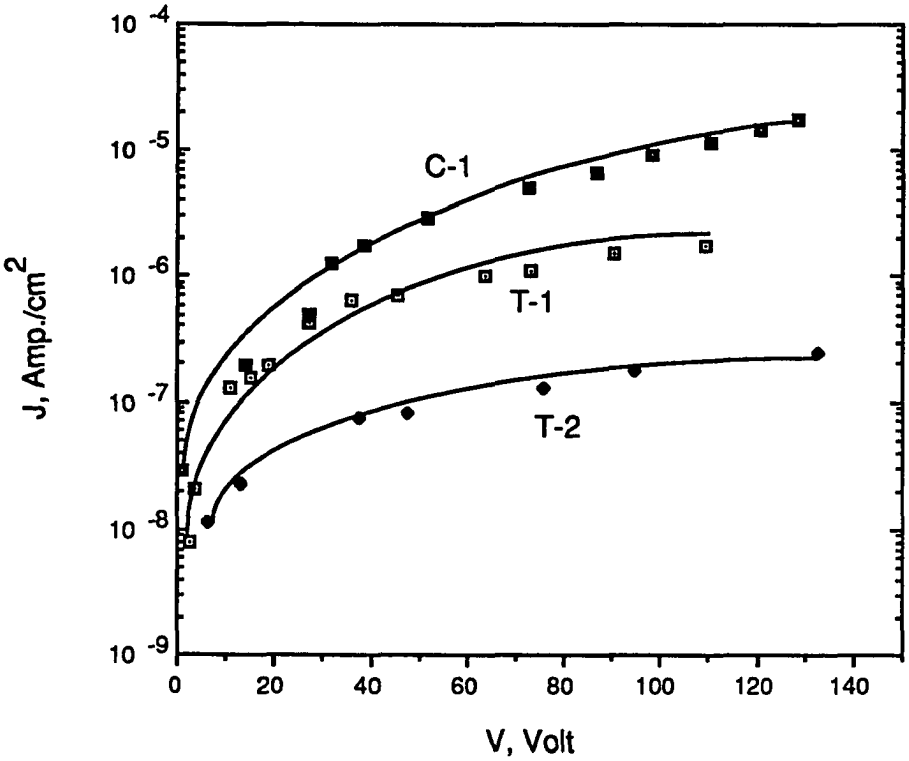


Fig. 4.2.1.(b) The leakage current densities plots of thermal silicon oxide with thickness 1800 Å (T-1) and 3600 Å (T-2), and CVD silicon oxide with 4300 Å (C-1).

4.3 Fabrication of Gated Micro Field Emitters

Based on the results in section 4.2, the CVD silicon oxide and S.O.G. are suitable to be used as dielectrics I and II in this fabrication approach. SEM photographs of the major steps are shown in Figs. 4.3.1, and the processing conditions and parameters are given as follows (the generic processing steps were shown in Fig. 4.1.1.) :

Step (a): Form an emitter using the processing step (a) shown in Fig. 4.1.1.

Step (b): CVD silicon oxide is used as the dielectric which control the gate opening. The CVD silicon oxide is grown by silane, nitrous oxide and argon at 300°C.

Step (c): the S.O.G. is deposited, followed by a cure at 130°C for 30 min..
Note: When polyimide is used, the polyimide is cured at 230°C for 120 min..

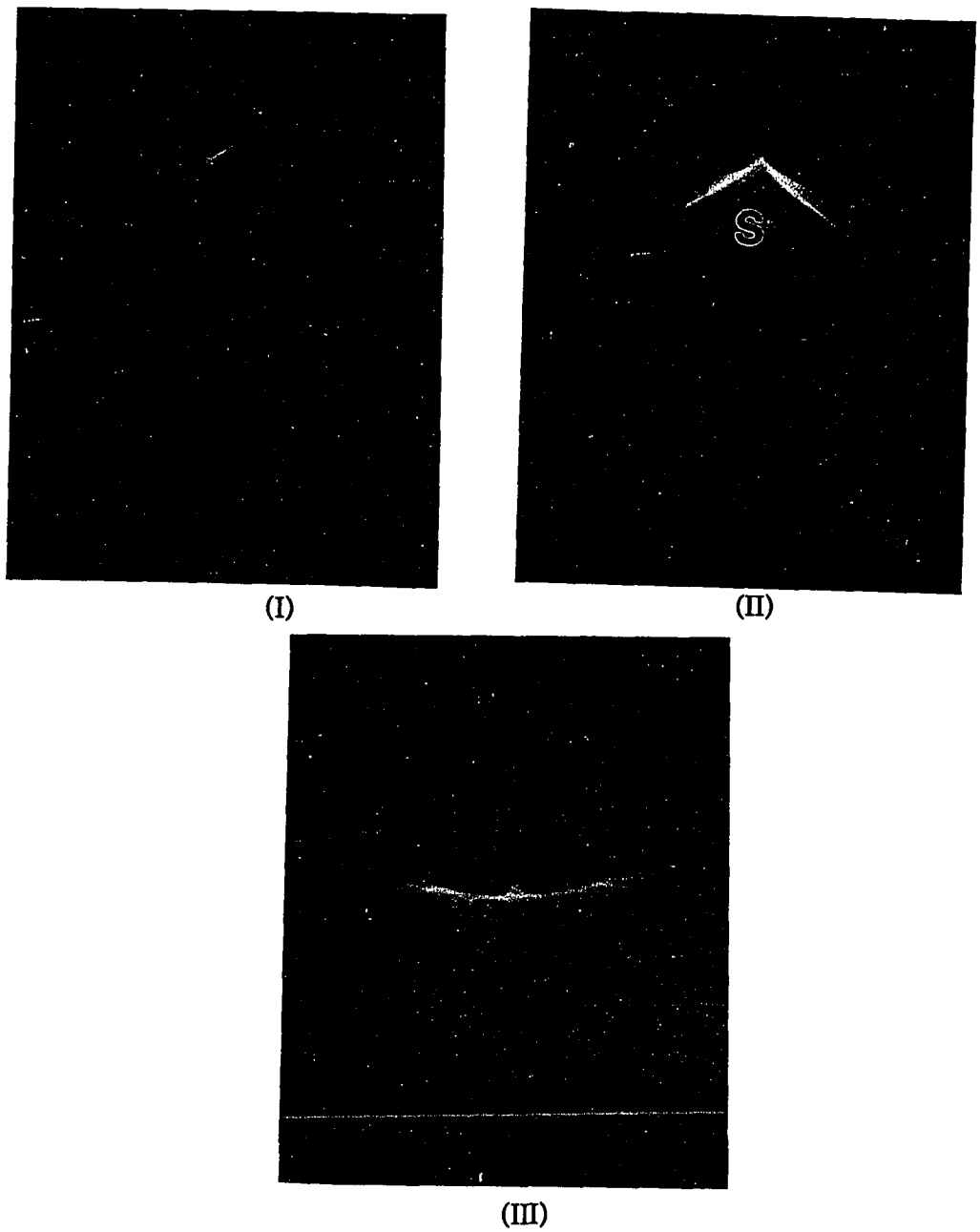
Step (d): the S.O.G. is etched back by C_2F_6 reactive ion etching with a flow rate of 5 sccm at 30 mtorr pressure and 100 W power. The etch ratio of S.O.G. to CVD silicon oxide is 2.2 to 1.0 and the S.O.G. etch rate is 650 Å/min..
Note: If polyimide is selected in step (c), it can be etched back by a barrel oxygen plasma with an etch rate 50 Å/min.. followed by a 30 min. cure at 400°C. The temperature should gradually increase at a rate 2°C/min. from room temperature to 400°C. This cure is important to prevent the polyimide film from cracking when acetone is applied to the post-oxygen-plasma etched polyimide film.

Step (e): the CVD silicon oxide is etched in BHF at an etch rate of 1000 Å/min..

Step (f): 2000 Å aluminum has been directionally deposited on the sample.

Step (g): Two methods as described in section 4.1 are used for different samples: (1) Anodic etch: This is performed with a EG & G model 179 digital coulometer set at a current source 0.2 mA. One min. is sufficient to remove aluminum from the tip; emitter sample 33-7-7 in chapter 5 was made using this method. (2) Etch back: The etchant for the gate metal Al is 3 ml D.I. (deionized water) : 12 ml CH_3COOH : 3 ml HNO_3 : 12 ml H_3PO_4 (phosphoric acid). The samples were deposited with 2000 Å aluminum. After controlled

etching at R.T. for 3.5 min. to remove the metal from the tip, around 1000 Å aluminum remained on the gate area; emitter samples 41-2-2 and 42-1-5 in chapter 5 were made using this etch back method.



Figs. 4.3.1. (I), (II), and (III) SEM photographs corresponding to Figs. 4.1.1 (b), (e), and (g), respectively; the etch back method was used to make the device shown in figure (III).

The self aligned gated field emitter shown in Fig. 4.3.1.(IV) was made with a 1 μm high Si emitter, 1000 Å Al as gate metal, 4500 Å CVD silicon oxide, 4500 Å S.O.G. as dielectric II and a 0.7 μm diameter gate opening. The tip is 1000 Å above the bottom edge of the gate film.

4.4 Special Problem: Electron Bombardment

SEM is an indispensable tool to investigate the morphology of the field emitter or gated field emitter. However, damage occurs when an electron beam hits the surface of material. The major damage occuring during study is:

(1) Contamination: Contamination occurs on the surface region being studied. The contamination resulting from SEM study of an emitter region in an array is shown in Fig. 4.4.1 (see abdc square).

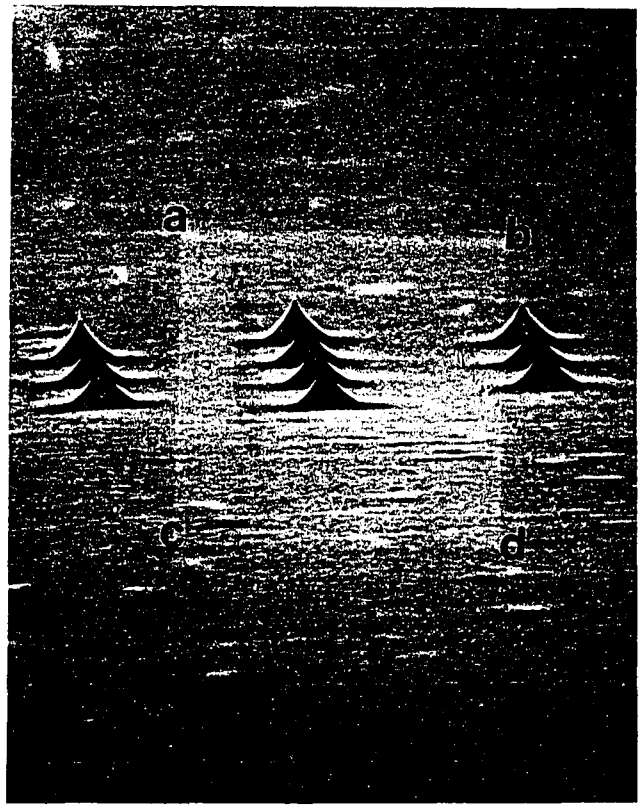


Fig. 4.4.1 Contamination (see abdc square) caused by previous higher-magnification SEM examination of emitters region. The light square area shows the contamination.

The contamination is a polymerized hydrocarbon which is grown during an incident beam bombardment. It will change the emitter work function and therefore affect the emission characteristics. The light block appearing in the picture shows the contaminated area after examined under SEM at 20 kv. A 950°C dry oxidation was used to clean up the contamination. Note that an

oxygen plasma is not a good method for removing this contamination since it will change the tip shape (see section 3.4).

(2) S.O.G. Film shrinkage: A S.O.G. film used in the new self-aligned process as dielectric II and spun on the device followed by 130°C bake for 40 min., was etched back by C_2F_6 RIE. A SEM examination resulted in the shrinkage of the S.O.G. film as shown in Fig. 4.4.2 where the hikj path is the shrinkage region. Since the S.O.G. film becomes denser at a higher temperature [70], high energy electron beam bombardment of a S.O.G. film surface, resulting in high local temperature may be responsible for this damage. Curing S.O.G. at higher temperature might avoid this SEM effect.

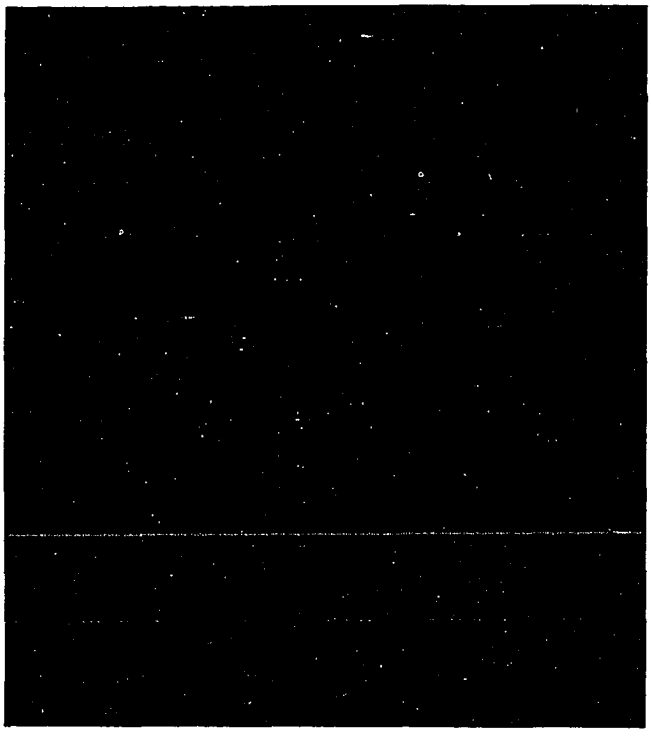


Fig. 4.4.2 A S.O.G. film shrinkage (see hikj path) caused by previous higher-magnification SEM examination.

CHAPTER 5
CHARACTERIZATION OF GATED SILICON FIELD EMISSION MICRO TRIODES

This chapter describes the measurement circuit and the test environment used to characterize the gated silicon field emission micro triodes. It also presents the measured triode characteristics. Error bars are calculated for most of the data points given in section 5.5; these error bars are determined by current fluctuations described in section 5.4.

5.1 Characterization Set-up

This section discusses the experimental procedure for characterizing the triodes. Section 5.1.1 describes the final test configuration for the gated silicon field emitter triode. Sections 5.1.2 and 5.1.3 describe the test circuit and test environment, respectively.

5.1.1 Final Device Structure

The gated silicon field emitters described in chapter 4 and used to make the final device structures are shown in Fig. 5.1.1.1.

Fig. 5.1.1.1 The gated silicon field emitters for the final device structure set-up.

Between the four crosses are eight gated field emitters devices. The ones with the larger circular area control emission from 10 emitters at each gate, while the smaller devices control emission from a single emitter. The gate opening is located in the circular area of the gate pattern and the emitter is at the center of the gate opening. These gate electrodes are extended to bonding pads which are not shown in this figure but which are shown in Fig. 5.1.1.3.

A cross-section of the final test structure including the collector electrodes is shown in Fig. 5.1.1.2 where δ is the tip elevation above the top edge of the gate.

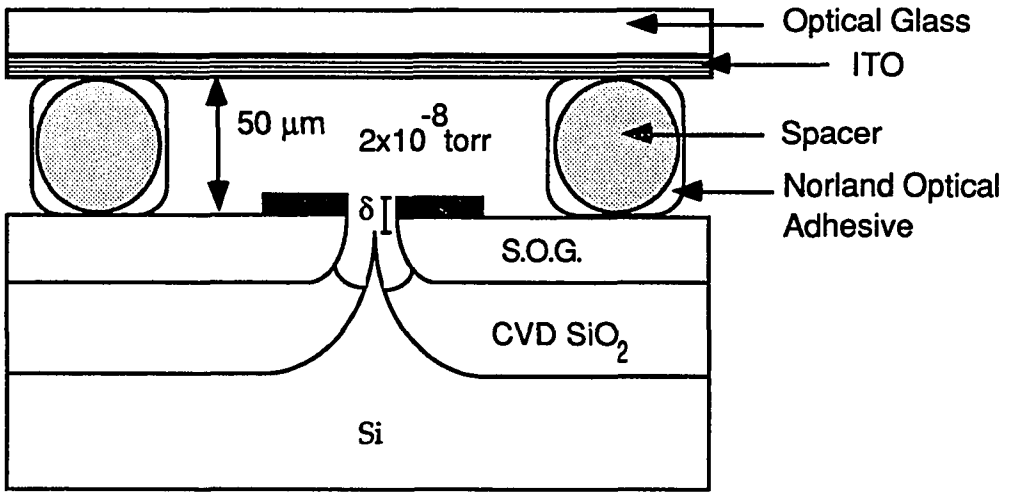


Fig. 5.1.1.2 A cross-section of the final test structure.

The collector electrode is an optical glass plate coated with ITO (indium tin oxide). The gated field emitter triode is made by placing the ITO glass on spacers on the surface of the sample containing the gated field emitters. The spacers consist of 50 μm diameter glass cylinders (obtained from EM Industries Inc.). The spacers are mixed with Norland optical adhesive 61, cured under a UV lamp for 1 hr., and placed in 4 small corners of the device, away from the gate electrodes (approximately in the four corners shown in Fig. 5.1.1.1).

This device then is placed onto a glass slide (which has 8 individual gold runners) with silver paste (obtained from SPI Inc.) and electrically connected using wire ultrasonically bonded to the bonding pads connected to the gold runners of the glass slide that connect with the gated silicon field emitters. The gold wires are bonded by a Westbond ultrasonic wire bonder; the wire bonding to four bonding pads is shown in Fig. 5.1.1.3.

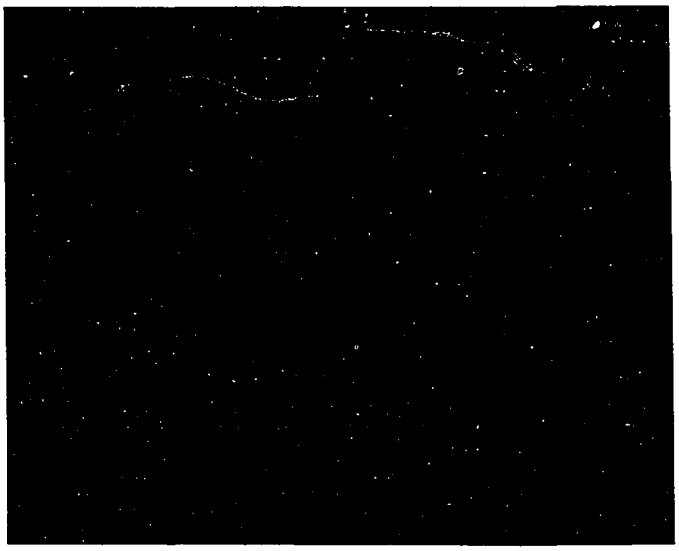


Fig. 5.1.1.3 The results of wire bonding on the bonding pads.

5.1.2 Test circuit

The test circuit for measuring the triode characteristics is shown in Fig. 5.1.2.1. Two battery power supplies (V1 and V2) were used to supply stable voltage sources for the emitter and the collector. The collector current Ic and the gate current Ig were measured by a Keithley 602 solid-state electrometer and 410 micro-microammeter, respectively. Simpson 464-4 digital multimeters measured the voltages of the supply voltage sources V_1 and V_2. A strip chart recorder was recorded the collector current as a function of time.

The resistor Rg was using as a current limiter for the gate path to protect the device from current bursts. It should be noted that the current limiting in the collector path was observed by setting the Keithley 602 at the normal position mode. The measurements were done in a vacuum 2×10^{-8} torr, at room temperature. Prior to measurements, the triodes were baked in the vacuum at

90° C for 12 hrs.. It should be noted that all the gated field emitters used for emission measurements were fabricated by the process described in Chapter 4.

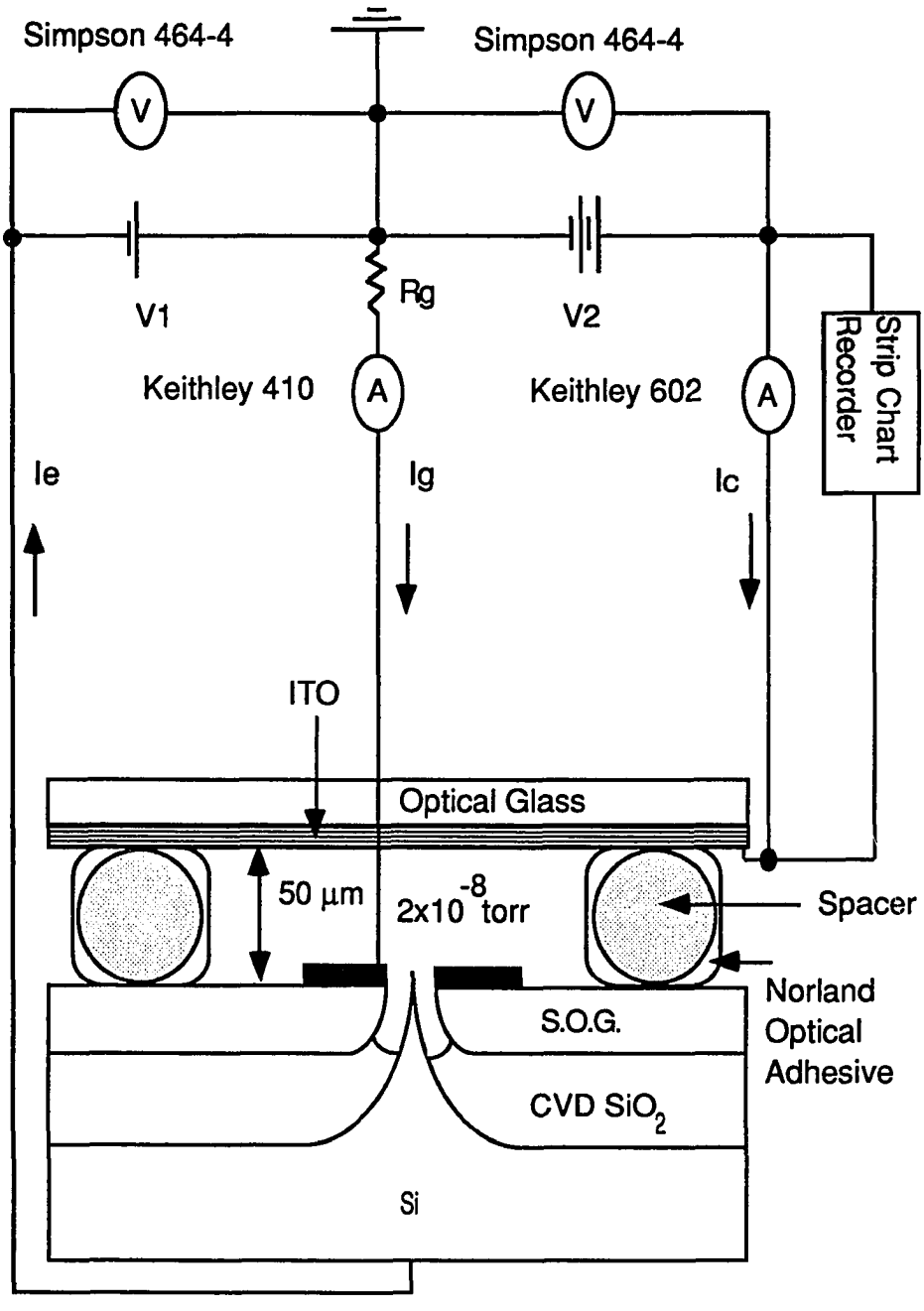


Fig. 5.1.2.1 The test circuit for the gated silicon field emitter triodes.

5.1.3 Test Environment

Since field emission devices require a vacuum, a high vacuum system was used; the schematic is shown in Fig. 5.1.3.1.

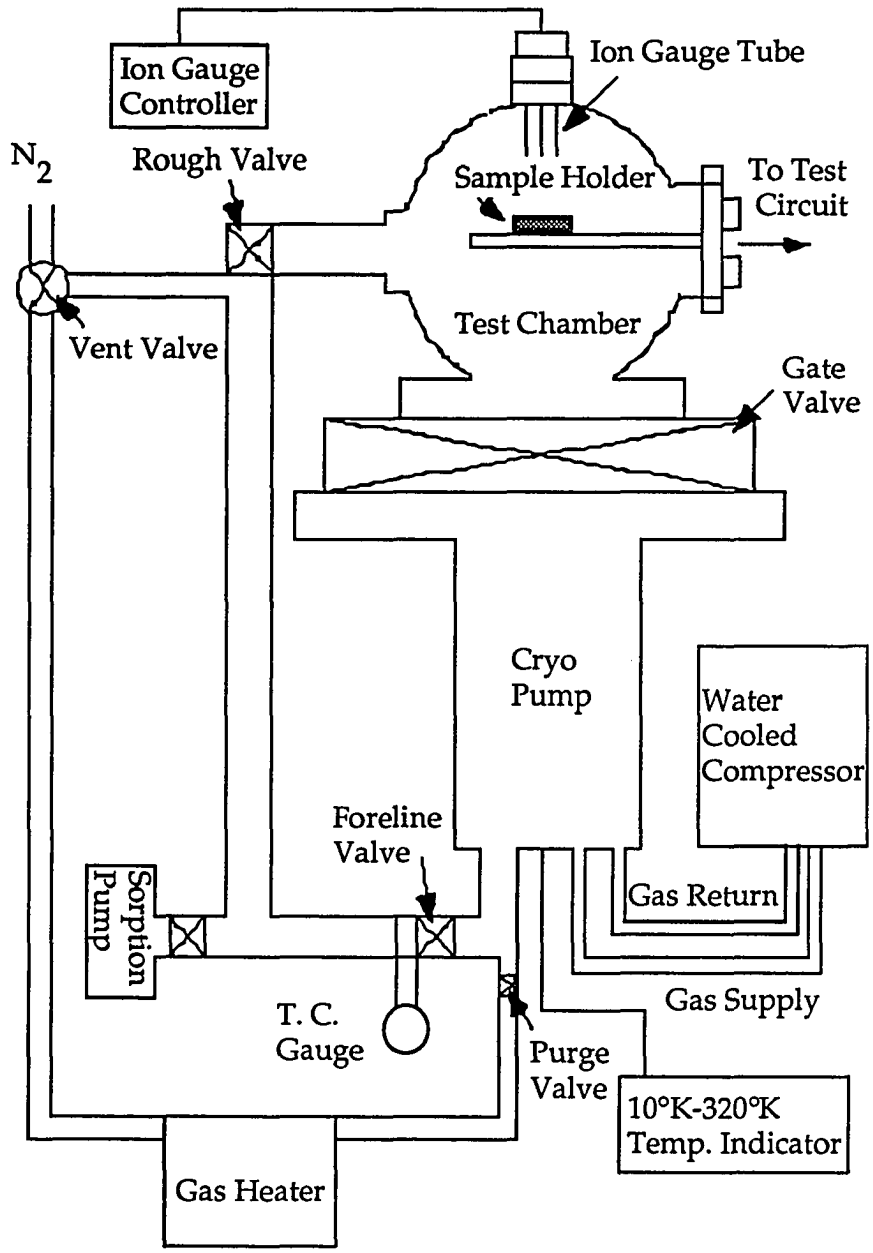


Fig. 5.1.3.1 Schematic diagram of the vacuum system used for testing field emission devices.

This vacuum system incorporates a CTI Cryo-torr 10 as the main pump, two sorption pumps for vacuum roughing, vacuum gauge systems and a temperature indicator (10°K to 300°K temperature range) for the cryo pump. The system provides vacuum of a vacuum of 2×10^{-8} torr. The pump is equipped with a water cooled compressor. The vacuum measuring apparatus includes a high vacuum indicator (ion gauge) and a low vacuum indicator (thermocouple gauge). A gas heater was used to assist the vacuum pump regeneration.

5.2 The Test Samples

A number of samples have been tested and measured in this research on field emission. The results for three typical field emission samples (33-7-7, 41-2-2, and 42-1-5) with different configurations and fabrication conditions, as summarized in Table 5.2.1, are reported. All devices tested were single-emitter conical tip devices where the emitters were silicon with the resistivity 0.005 - 0.02 Ω-cm. The radii shown in the Table 5.2.1 were measured from the SEM photographs. The tip elevation, δ, is defined as the distance from the emitter to the top edge of the gate. These different configuration devices have different emission behavior and I vs. V characteristics, as will be discussed in later sections.

Table 5.2.1 The configurations and fabrication conditions of three typical field emission samples

Sample	33-7-7	42-1-5	41-2-2
S.O.G. Baked Condition	130 °C 30 min.	130 °C 30 min.	130 °C 30 min. Followed by 380 °C 30 min.
Gate Metal Removal	Anodic Etching	Etch Back	Etch Back
Tip Radius r (Å)	< 100 *	< 100 *	< 100 *
Gate Metal Thickness (μm)	0.18 - 0.22	0.09 - 0.11	0.09 - 0.11
Gate Opening in Diameter (μm)	1.0 - 1.2	1.0 - 1.2	1.0 - 1.2
Tip Elevation δ (μm)	-0.15 - -0.14	0.04 - 0.07	0.17 - 0.23

* Probably atomically sharp, though not confirmed by TEM study.

5.3 Fowler-Nordheim Characterization

One of the characteristics of field emission is Fowler-Nordheim (F-N) behavior, in which a plot of $\log I/V^2$ vs. $1/V$ is a straight line for the narrow region of a typical field emission experiment ($3\ v/cm < F < 5\ v/cm$).

5.3.1 Derivation of the Formulas for Emitting Area and Field Adjustment Factor

In order to analyze the F-N plot, it is desirable to derive the formulas for emitting area and field adjustment factor α; α is defined as $F=V\alpha/r$ where F is the electric field, V is the applied gate to emitter voltage, and r is the emitter radius. The derivation starts from the Fowler-Nordheim equation [13] (see section 2.2).

$$J = \frac{AF^2}{\phi t1.1}\, e^{-B(0.95-y^2)\frac{\phi^{3/2}}{F}} \qquad (5.3.1.1)$$

where field emission current density J is in A/cm^2, electric field at the tip surface F is in v/cm, emitter work function ϕ is in electron volt (ev), $A=1.54\times10^{-6}$, $B=6.83\times10^{7}$, and $y=3.79\times10^{-4}\, F^{1/2}/\phi$ (y is the Schottky lowering of the work-function barrier). We may let $J = I/\beta r^2$ and use $F = V\alpha/r$ where βr^2 is the emitting area , α/r is the field conversion factor and I is the field emission current. Thus Eq. (5.3.1.2) becomes

$$I/(\beta r^2) = \frac{AV^2\alpha^2}{1.1\, \phi r^2}\, e^{-\frac{0.95Br\,\phi^{3/2}}{V\alpha}}\, e^{-\frac{1.436\times10^{-7}\,B}{\phi 1/2}} \qquad (5.3.1.2)$$

The factor βr^2 can be obtained by rearranging Eq. (5.3.1.2).

$$\beta r^2 = \frac{I}{V^2} \frac{1.1\,\phi r^2}{1.54 \times 10^{-6} \alpha^2} e^{\frac{6.49 \times 10^7 r\,\phi^{3/2}}{V\alpha}} e^{\frac{-9.81}{\phi^{1/2}}} \qquad (5.3.1.3)$$

Eq. (5.3.1.3) can also be written as:

$$\log \frac{I}{V^2} = -5.85 + \log \frac{\alpha^2 \beta}{\phi} + \frac{4.26}{\phi^{1/2}} - 2.819 \times 10^7\, \phi^{3/2} \frac{r}{V\alpha} \qquad (5.3.1.4)$$

The slope S of the $\log \frac{I}{V^2}$ vs. $\frac{1}{V}$ plot is derived as follows:

$$S = \frac{d(\log \frac{I}{V^2})}{d(\frac{I}{V})} = \frac{-2.819 \times 10^7\, r\, \phi^{3/2}}{\alpha} \qquad (5.3.1.5)$$

Thus the field conversion factor α can be obtained from the slope of the F-N plot since r and ϕ are known or assumed:

$$\alpha = \frac{-2.819 \times 10^7 r\, \phi^{3/2}}{S} \qquad (5.3.1.6)$$

Thus βr^2 and α can be calculated from Eq. (5.3.1.3) and (5.3.1.6), respectively. For an emitter with constant ϕ, r and α, the slope will be constant during the change of voltage.

5.3.2 Fowler-Nordheim Behavior

A number of single silicon emitter samples have been tested and measured for field emission. Typically when emission is first observed, it is very unstable and the average emission current keeps increasing gradually as shown in Fig. 5.3.2.1. This phenomenon is possibly caused by the emitter surface being cleaned by the emission [29]. The emission becomes relatively constant and stable after a few tens of minutes.

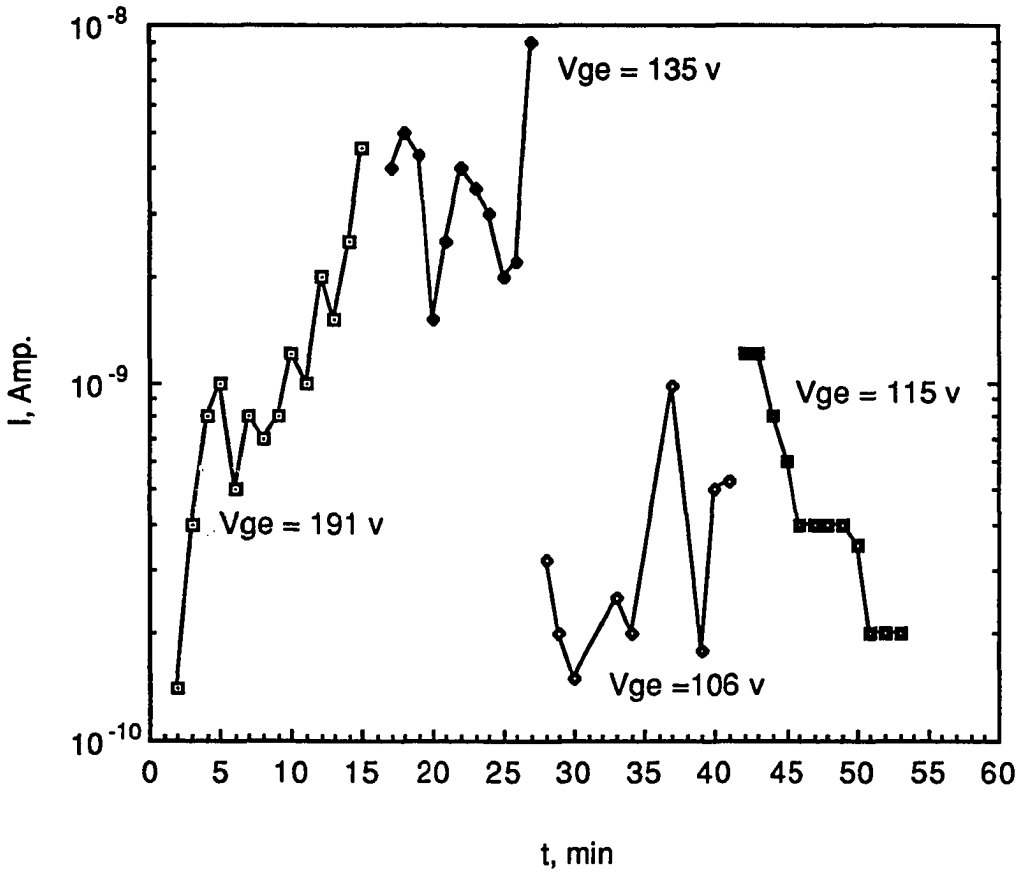


Fig. 5.3.2.1 The characteristics of initial emission of sample 42-1-5.

The emission data reported here were collected after the current was constant for constant applied voltage. The emission data followed the F-N equation. Single silicon emitters had turn-on voltages above 25 v and typically 50-90 v. Emission currents have been measured in the range 5 pA- 1 μA. for single emitter. Fig. 5.3.2.2 shows the emission data of samples 33-7-7, 41-2-2 and 42-1-5 and compares these results with other research results [13] [29] [44] [73].

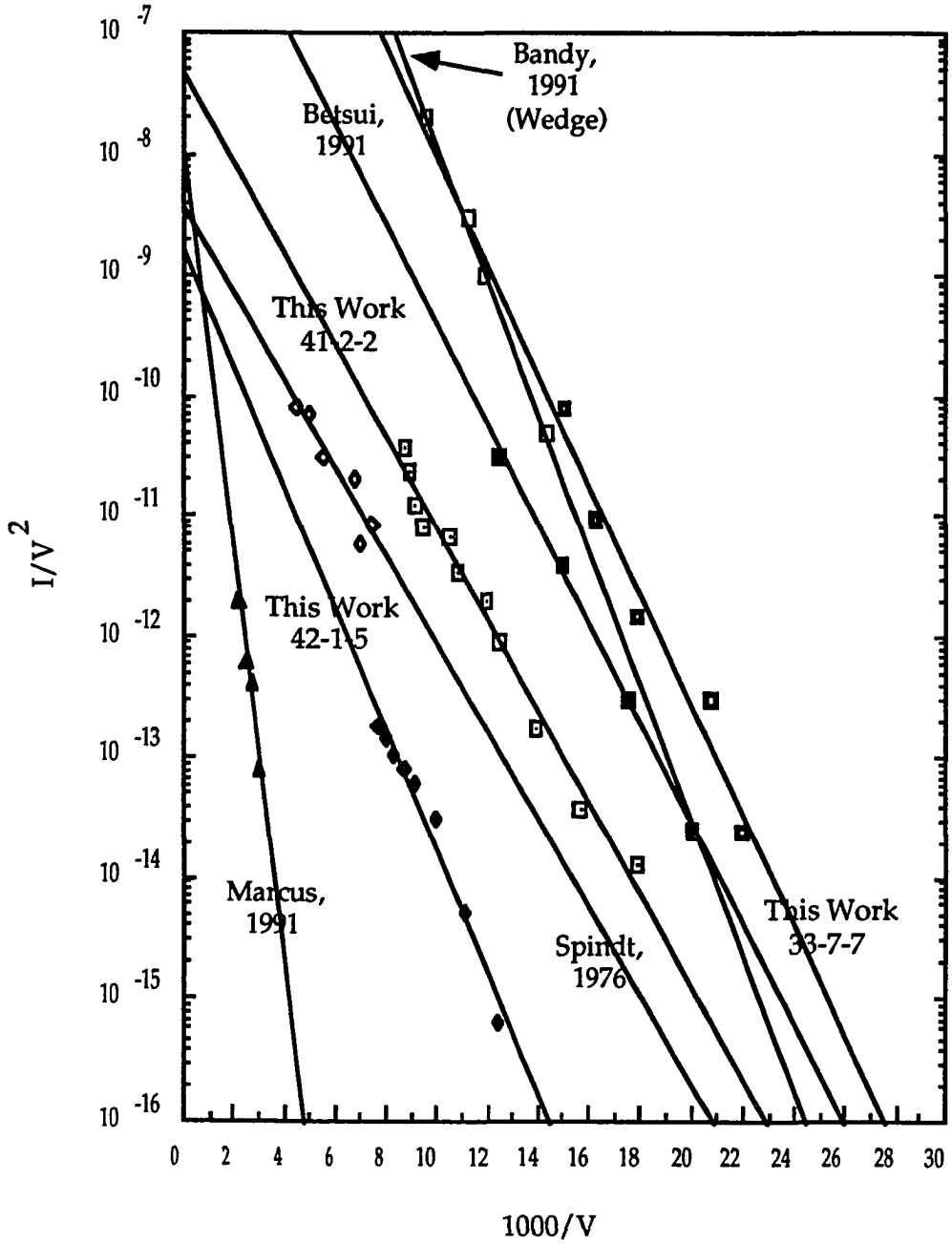


Fig. 5.3.2.2 A comparison of emission data in this research with other researches.

It should be noted that the Bandy experiment was for single edge film emitters and the other researchers used conic tip emitters. Spindt and Bandy used single metal emitters and the others used single silicon emitters. The three curves of samples 33-7-7, 41-2-2, and 42-1-5 shown in Fig. 5.3.2.2 are typical of the emission data we obtained and are similar to other researcher's curves. However, the emission data have different slopes for reasons that are not clear. It is known that the slope is a function of the field conversion factor and emitter work function. The emission current ranges shown in the curves are 40 pA - 0.4 μA, 5 pA - 0.5 μA, and 5 pA - 3 nA for samples 33-7-7. 41-2-2, and 42-1-5, respectively. The applied voltages necessary for initiation of emission currents are 45 v, 56 v, and 80 v, respectively. An SEM photograph, after being tested and having current up to 5 nA is shown in Fig. 5.3.2.3. The device configurations and fabrication conditions for these samples were described in section 5.2.

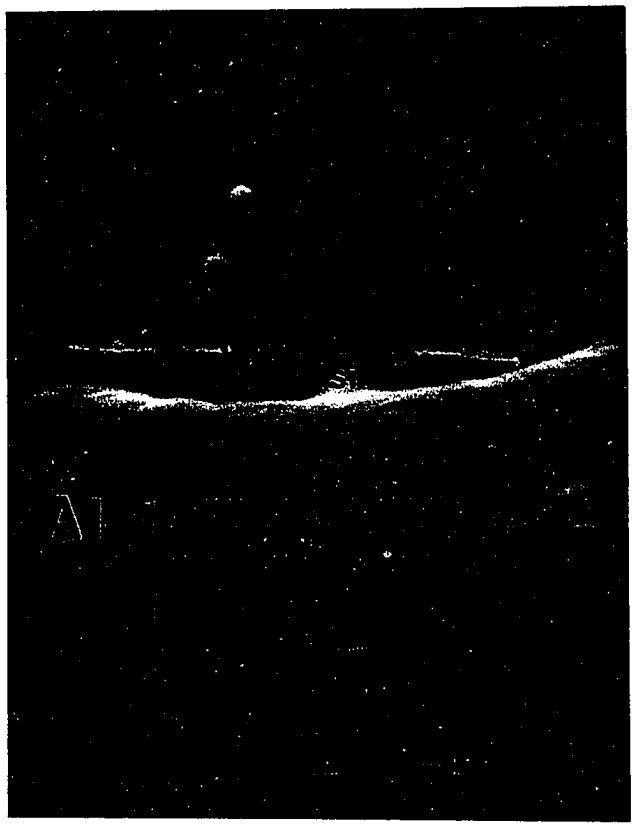


Fig. 5.3.2.3 A SEM photograph of the emitter of 42-1-5 after the emission measurement.

It should be noted that the top area of the emitter appears semitransparent since the area is very thin and therefore the electron beam transmits through it. The emitter radius is certainly less than 100 Å, which is as sharp as virgin emitters observed by SEM.

In order to analyze the emission data, Eq. (5.3.1.3) and (5.3.1.6) were used to calculate the emitting area and the field adjustment factor. Table 5.3.2.1 show the field adjustment factor and the emitting area for the same three devices shown in Fig. 5.3.2.2.

Table 5.3.2.1 Derived values of field adjustment factor α and emitting area βr^2 of samples 33-7-7, 41-1-5, and 42-2-2; $\phi = 5$ and 3 ev; r= 10^{-7} and 10^{-6} cm.

Sample	r (cm)	ø (ev)	α	βr^2 ($\times 10^{-14}$ cm)
33-7-7	10^{-7}	5	0.07	1515.00
		3	0.03	1198.00
	10^{-6}	5	0.70	1515.00
		3	0.30	1198.00
41-2-2	10^{-7}	5	0.08	0.47
		3	0.04	0.42
	10^{-6}	5	0.80	0.47
		3	0.40	0.42
42-1-5	10^{-7}	5	0.06	0.02
		3	0.03	0.01
	10^{-6}	5	0.60	0.02
		3	0.30	0.01

The calculations are based on two reasonable assumptions for r, 10^{-7} and 10^{-6} cm, and ø, 5 and 3 ev. With regard to the calculations of table 5.3.2.1 four points need to be made clear: (1) Since the emitter radius is less than 100 Å from the SEM photograph and is less than 10 Å from the TEM photograph on the typical emitters, it is reasonable to assume r as equal to either 10^{-7} or 10^{-6} cm for the calculations; (2) Since ø is not known for the measured emitters, reasonable values of 3 and 5 ev have been assumed; (3) The value of the field adjustment factor α increases as r or ø increases; (4) The derived values of the emitting area are the same for different assumed radii and change only slightly with ø.

Our results for α (or α/r) and βr^2 can be compared with other values for these parameters obtained in other field emission studies. The results of this comparison are given in Table 5.3.2.2.

Table 5.3.2.2 A comparison of field conversion factor α/r and emitting area βr^2 with other researches.

Researcher	α/r (cm^{-1})	βr^2 (cm^2)	Reference
Spindt,1976	$1.25x10^{5}$	$1.3x10^{-15}$	[13]
Harvey, 1991	$1.1x10^{5}$	$4x10^{-14}$	[74]
Busta, 1991	$6.22x10^{5}$	$5x10^{-15}$	[75]
Marcus, 1991	$0.7\text{-}1.5x10^{5}$	$6x10^{-14}$	[73]
This Work 33-7-7	$3\text{-}7^{*}x10^{5}$	$1.2\text{-}1.5^{*}x10^{-11}$	–
This Work 41-2-2	$4\text{-}8^{*}x10^{5}$	$4.2\text{-}4.7^{*}x10^{-15}$	–
This Work 42-1-5	$3\text{-}6^{*}x10^{5}$	$1\text{-}2^{*}x10^{-16}$	–

* Corresponding to ø ranging from 3.0 to 5.0 ev.

The comparison shows that the field conversion factors and most of the emitting areas are similar except for the larger area of sample 33-7-7. This is possibly due to the fact that the emitter in this sample is a relative long stalk that projects beyond the top of the emitter (see chapter 3). The significantly larger emitting area for this sample could be due to the emission area not being restricted to the top of the emitter where the top area of tip $2\pi r^2=6.28x10^{-14}$ cm^2, but to the surface of the small conical region at the top of the emitter. Since the emitting surface of a cone equals

$$\pi R\sqrt{R^2+h^2} - \pi R^2$$

where h is the cone height, R is the cone base diameter and the tip is approximated by a right cone with half angle of 10°, then an emission area of 10^{-11} cm^2 suggests that the emission region is the top 500 Å of the tip.

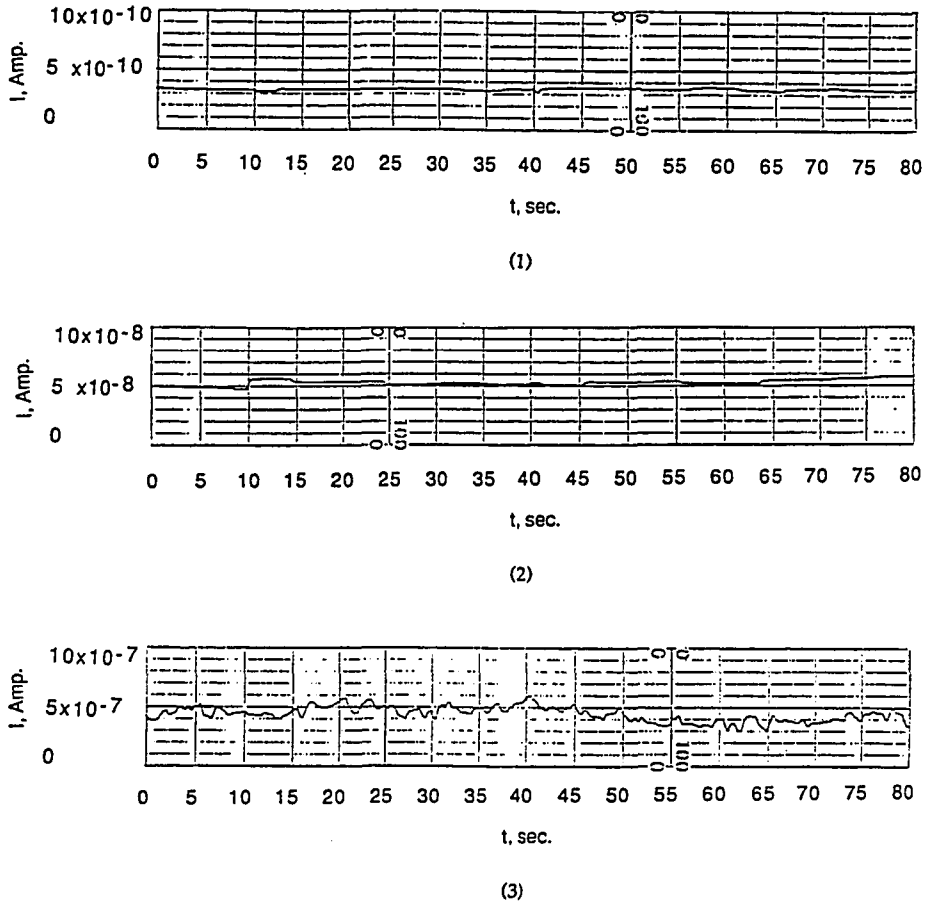
The smaller emitting areas obtained in other two samples (41-2-2 and 42-1-5) correspond to only a few atomic sites at the each emitter contributing to the emission. This result suggests that emission occurs at the atomically sharp tip region only [13].

The field conversion factors obtained from these experiments are similar to results of other research studies. This is probably due to the similar device geometry.

5.4 I vs. Time Characterization

Temporal fluctuations have been observed in emission current measurements since Spindt's observations on molybdenum around two

decades ago [13]. Fluctuations of field emission current from single silicon gated emitters were measured after the emission becomes relatively calm and stable. Figs. 5.4.1.(1), (2), and (3) show the short term fluctuation at various emission current levels for sample 41-2-2.



Figs. 5.4.1.(1), (2), and (3) The short term fluctuation of various emission current levels from single silicon gated field emitter of sample 41-2-2.

The fluctuation data of Fig. 5.4.1.(3) were obtained after the emission current reached about 0.5 μA and stabilized for a few tens of minutes. Then V was reduced to lower the emission current to around 50 nA at which values the data of Fig. 5.4.1.(2) were acquired. Finally, the emission current was reduced to 0.35 nA by further reducing the applied voltage and the data for Fig. 5.4.1.(1) were obtained. The fluctuation rates are 10%, 16% and 40% for Figs. 5.4.1.(1), (2) and (3), respectively. Similar behavior is observed for sample 42-1-5 with a 29% fluctuation rate at around 1.4 nA emission current. The higher fluctuation rate for higher emission current is not well known. However, the current fluctuation can be reduced significantly by using a field emitter array and obtaining an average current from the array [29].

5.5 I vs. V Characterization

In order to understand more about the emission, the gate current Ig and the collector current Ic were measured. Fig. 5.5.1 shows the collector current behavior as a function of both Vge and Vcg for device 42-1-5 where Vge is the voltage between the gate and the emitter, and Vcg is the voltage between the collector and the gate. The error bars are based on the temporal current fluctuations described in Fig. 5.4.1.

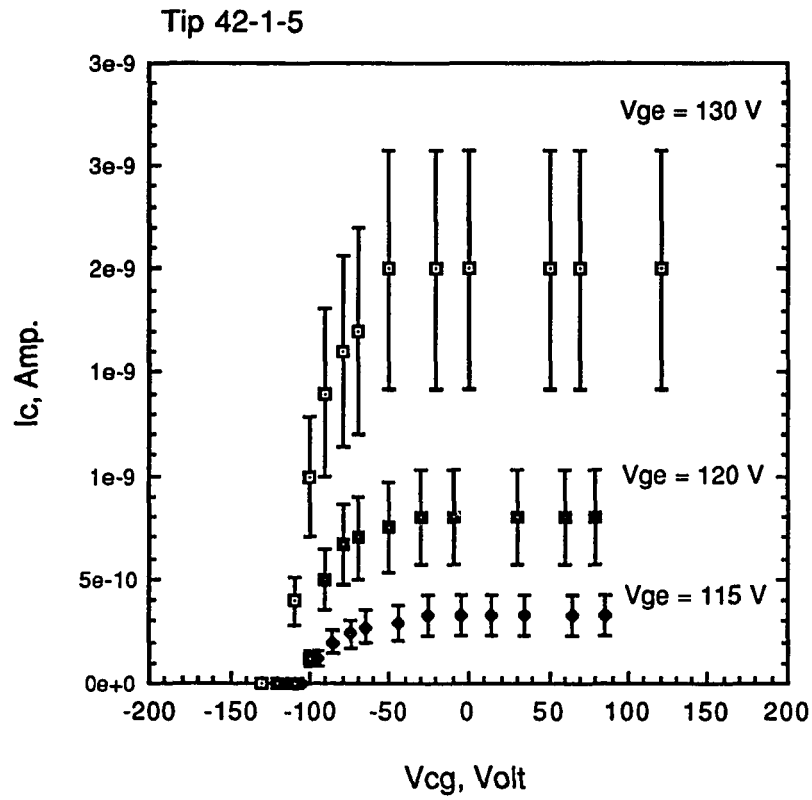


Fig. 5.5.1 The triode behavior of sample 42-1-5.

The collector begins to collect the emission current when Vcg is -100 v. The collector current increases as Vcg increases; this is the region in which the current is limited by the space charge. The collector current becomes saturated when Vcg increases to around - 50 v. In the saturation region the collector current is limited by the emission current and does not change as Vcg increases unless Vge increases.

It is interesting to set Vcg at extreme values to observe the relation of Ic and Ig. For Vcg = -200 v most of the emission current goes to the gate while the collector collects very little current (almost zero) as shown as Figs. 5.5.2. The

collector current shown in this figure is leakage current and this current does not increase as Vge increases.

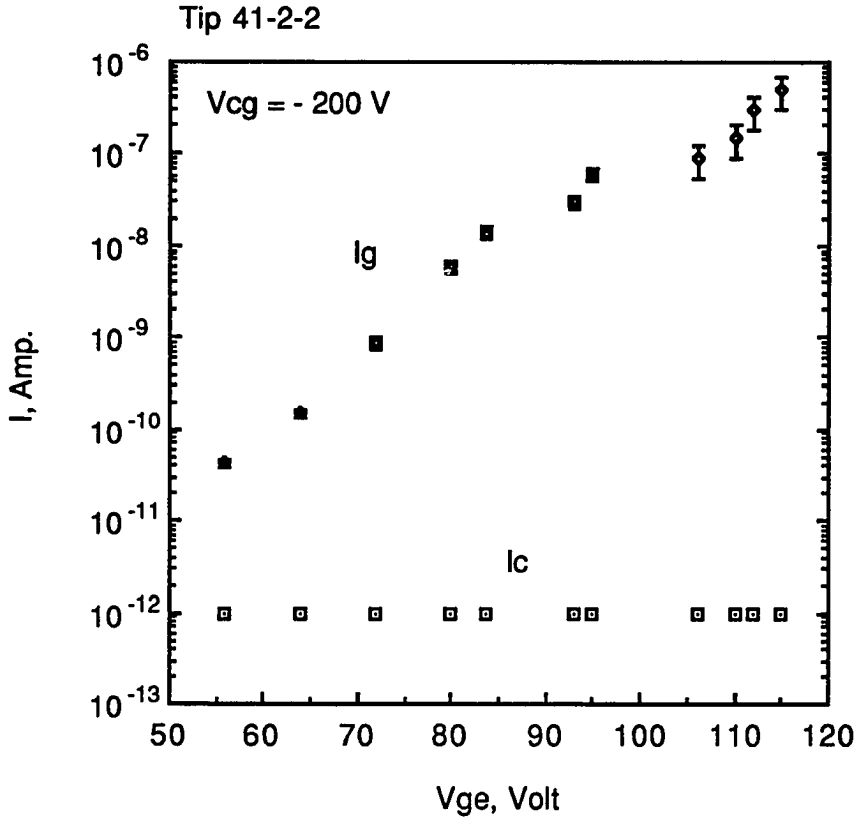


Fig. 5.5.2 The gate and the collector currents as a function of Vge for sample 41-2-2.

If Vcg is set at 200 V, a major part of the emission current goes to the collector and only a minor part to the gate. Figs. 5.5.3.(a), and (b) show the collector current Ic and the gate current Ig as a function of Vge for devices 41-2-2, and 42-1-5, respectively.

The transconductance gm, which is defined by $gm=\partial Ic/\partial Vge$ is $3x10^{-8}$ mhos for device 41-2-2 at Ic = 0.35 μA and Vge =120 v and is $5x10^{-10}$ mhos for device

42-1-5 at Ic = 5 nA and Vge = 130 v. These values can be increased (1) by increasing the Vge or (2) by using a field emitter array.

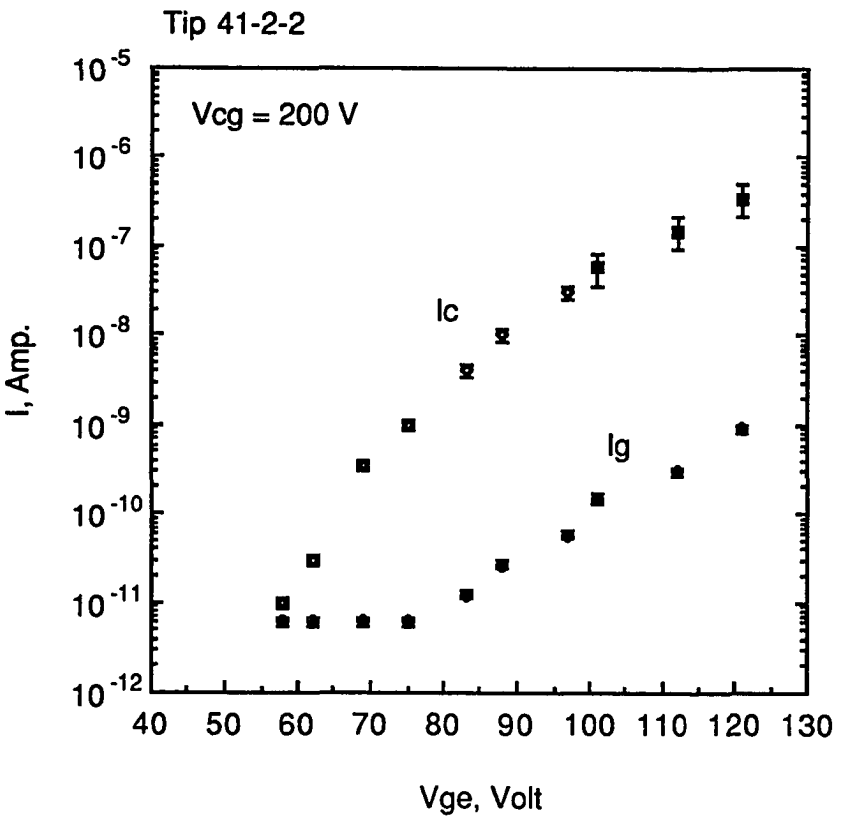


Fig. 5.5.3.(a) The collector and the gate currents as a function of Vge for sample 41-2-2.

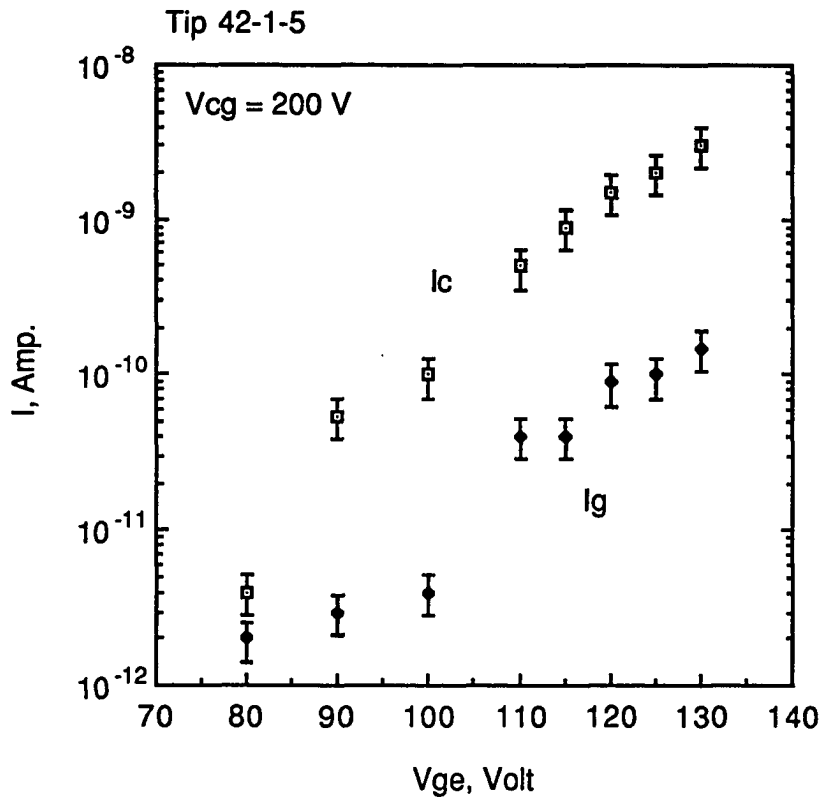


Fig. 5.5.3.(b) The collector current as a function of Vge for sample 42-1-5.

In Figs. 5.5.3.(a) and (b), the gate current is smaller than the collector current and both gate and collector currents increase as Vge increases. This triode behavior has been observed elsewhere with a Ig/Ic ratio range from 0.1% to 30% [27] [29] [47] [77-78]. The large variation of the Ig/Ic ratio is possibly due to variations in test device geometry. From the Figs. 5.5.3, the typical Ig/Ic ratios are 0.25% for device 41-2-2 and 5% for device 42-1-5. The low Ig/Ic ratio for

the former device can be explained by the fact that the emitter in device 41-2-2 protrudes more (higher δ) than in device 42-1-1.

5.6 Device Failure and Electrostatic Discharge (ESD)

(1) Device Failure:

The phenomenon of a vacuum arc completely destroying the emitters during emission measurement is generally accepted as the cause of device failure [79-81], where the vacuum arc is initiated by the high emission current density [76]. The device failure has been observed in this research as well as by other researchers [13] [27] [81].

Fig. 5.6.1 shows the various degrees of damage to the gated field emitter structures. Outgasing from the material of the device is one possible cause of the vacuum arc. Extra baking at higher temperature (380°C for 30 min.) at the final fabrication stage help to reduce outgassing was used on the device and fewer devices failed was observed. It is possibly that reduced device failure was a result of reduced outgassing. It should be noted that the damages, which occur even the applied gate to emitter voltage is less than 150 volts. The occurings do not trigger or chain trigger on neighboring gated field emitters.

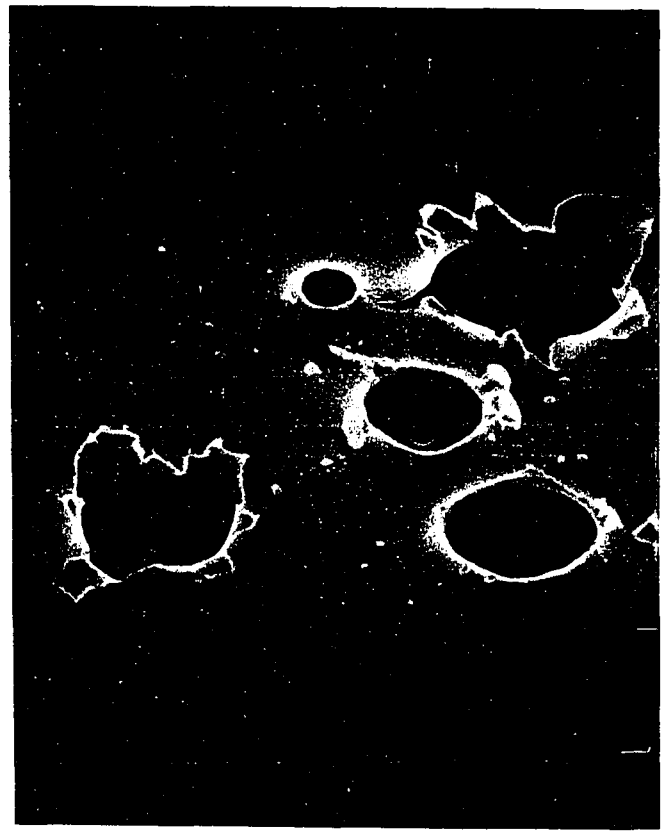


Fig. 5.6.1 Various degrees of device damage.

(2) ESD (electrostatic discharge):

Electrostatic discharge which destroys gated field emitters and produces a structure essentially the same as that shown in Fig. 5.6.1 has been observed. An electrostatic charge may accumulate on the field emission device during fabrication or while handling, as in the case of other semiconductor devices. Since the field emission device uses a sharp emitter and a narrow space separating the emitter and the gate , an accumulated electrostatic charge on the gate or on the emitter can be discharged to the other easily. In order to

avoid the ESD, there are two possible major approaches: (1) build in a protection circuit which must be able to sink a ESD to the device; (2) use extra precautions such as conducting gloves or handling tools.

CHAPTER 6
SUMMARY OF RESULTS

This experimental work has been concentrated on the fabrication of silicon conic tips, and wedges and GaAs wedges, and the characterization of gated silicon micro field emitter triodes. The main result of this dissertation are as follows:

(1) Silicon conic and wedge tips with nm-scale radii have been fabricated by etching and dry oxidation. Techniques were developed for making optimum shapes, and optimum oxidation treatments were determined.

(2) GaAs wedges with radius 400 Å or less also have been fabricated. These wedges have potential use as field emitters.

(3) A new self-aligned process has been developed to make a gated field emitter. This process provides advantages such as a self-aligned gate opening to less than 0.5 μm diameter, a planar gate electrode, and a thick dielectric layer for capacitance reduction.

(4) The effect of oxygen plasma on silicon tips and a problem of electron bombardment on the surface of the dielectric material has been revealed and discussed.

(5) Various materials such as thermal silicon oxide, CVD silicon oxide, S.O.G. and polyimide used for dielectric films have been evaluated and used for device fabrication.

(6) The emission of single gated silicon field emitters has been observed and shown to obey Fowler-Nordheim behavior. The single emitters have turn-

on voltage above 25 and typically 50-90 V, and reproducible emission currents have been measured in the range 5 pA-1μA. Emitting areas of 1×10^{-16} - 1.5×10^{-11} cm^2 and field conversion factors 3×10^5 - 8×10^5 cm^{-1} have been calculated from the emission data, and comparison were made with other research results.

(7) The gradually increasing emission current at the early stage of emission has been observed and self-cleaning is a likely cause of this phenomenon. Emission becomes relatively calm and stable after a few minutes emission.

(8) The temporal fluctuation of emission current have been measured after the emission has been stabilized. Fluctuation rates of 10%, 16% and 40% were found for emission current around 0.35 nA, 50 nA and 0.5 μA, respectively.

(9) I vs. V characteristics were investigated. The field emission triodes show an I vs. V curve similar to that of solid state triodes. One triode with a low Ig/Ic ratio of 0.25% is probably due to a high protrusion of the emitter above the gate.

(10) The device failure of the gated field emitter has been observed, and material outgassing is likely responsible. ESD which also destroys the emitter also has been experienced occuring during device handling.

APPENDIX A
SILICON FIELD EMISSION MICRO EMITTERS PROCESSING PARAMETERS

The following steps are ordered in numbers for the processing.

(1) Use a n^+ ($N_D = 10^{18}$ cm^{-3}) (100) silicon wafer.

(2) Dry oxidation to form 1500 Å silicon oxide.
Gas: oxygen
Gas: Flow Rate: 150 sccm
Reaction Chamber Pressure: 1 atm
Substrate Temp.: 1050°C
Oxidation Time: 2 hrs.

(3) Spin on resist.
Resist: AZ 5214E
Spin Rate: 4K rpm
Spin Time: 30 sec.

(4) Softbake 30 min. at 90°C oven.

(5) U.V. Exposure for 5.5 sec. followed by 1 min. at 125°C hot plate, then flood U.V. exposure for 9 sec..
Exposure Energy: 15.0 W/cm^2

(6) Develop in a solution of one part AZ developer and one part D.I. for 45 sec..

(7) Hardbake 30 min. at 130°C.
Note: Steps (3) - (7) are typical lithography technique.

(8) RIE.
Reactive Gas: C_2F_6
Gas Flow Rate: 5 sccm

Chamber Pressure: 30 mtorr
RF Power: 100 W
Etching Rate: 300 Å/min for resist; 300 Å/min. for silicon dioxide; 300Å/min. for silicon.

(9) Apply acetone, methanol to wash out resist.

(10) Use oxygen plasma to clean resist residue.
Reactive Gas: 100 % oxygen
Chamber Pressure: 280 mtorr
Power: 50 W
Etching Time: 5 min.

(11) The NAH etching.
Etchant Composition: 95ml CH_3COOH; 3mlHNO_3; 2ml HF
Etching Temp. : R.T.
Etching Time: 3 min. for 2 μm disc mask

(12) Use HF to remove silicon dioxide.

(13) Oxidation on Sample.
Gas: oxygen
Oxidation Temp.: 950°C
Oxidation Time: 5.5 hrs.
Note: The step (13) may repeat to obtain desired sharpness.

(14) Use HF to remove silicon oxide

APPENDIX B
GATED SILICON FIELD EMISSION MICRO EMITTERS PROCESSING PARAMETERS

The following processes have been used in this research for a gated field emitter. Some of them are industry standards, some are prepared to serve this research only.

(1) Deposit 4500 Å plasma CVD silicon oxide.
Gases: silane; nitrious gas; argon
Gas Flow Rate: 160 sccm/silane; 90 sccm/nitrious oxide; 680 sccm/argon
Chamber Pressure: 200 mtorr
Substrate Temp.: 300°C
RF Power: 30 W
Deposition Tme: 75 min.

(2) Check the thickness by Rudoph Research/AutoEL ellipsometer.

(3) Spin S.O.G. on sample with spin rate 4 K rpm and spin time 30 Sec..

(4) Hardbake 40 min. at 130°C.

(5) Check S.O.G. thickness by Nanometrics 210 film thickness system.

(6) Electron beam evaporate Ti/Au (200/2000 Å) on backside of sample.
Evaporation Rate: 5 Å/sec. for Ti, 10 Å/sec. for Au.

(7) RIE S.O.G..
Reactive Gas: C_2F_6
Gas Flow Rate: 5 sccm
Chamber Pressure: 30 mtorr
RF Power: 100 W
Etching Rate: 650 Å/min. for S.O.G.; 300 Å/min. for silicon dioxide.

(8) BHF (BOE 6:1) 1.5 min..

(9) Electron beam evaporation Al (2000 Å)
Evaporation Rate: 5 Å/sec.

(10) Repeat steps (3) - (7).

(11) Al etch to obtain gate runner pattern.
Etchant Composition: 3ml D.I.; 12 ml CH_3COOH; 3ml HNO_3: 12ml H_3PO_4
Etching Temp.: R.T.
Etching Time: 5 min.

(12) Use acetone, methanol to wash out resist.

(13) Al etch to remove Al from the emitter.
Etchant Composition: 3ml D.I.; 12 ml CH_3COOH; 3ml HNO_3: 12ml H_3PO_4
Etching Temp.: R.T.
Etching Time: 3.5 min.

APPENDIX C
GATED SILICON FIELD EMISSION MICRO TRIODES PROCESSING PARAMETERS

(1) Use steps (3) - (7) of Appendix A.

(2) Electron beam evaporate Ti/Au (200/2000 Å) on the sample.
Evaporation Rate: 5 Å/sec. for Ti, 10 Å/sec. for Au

(3) Lift-off by immersing in acetone solution.

(4) Package ITO plate to sample with a mixture of 50μm glass spacers and Roland Adhesive 61 followed by U.V. cured 1 hr..

(5) Place device on Au patterned glass slide with silver paste.
Note: The Au pattern glass is prepared by the following steps:
(a) Use step (2) of this Appendix
(b) Use Steps (3) -(7) of Appendix A
(c) Ion Mill: Ion mill power density: 0.25 W/cm
(d) Use step (10) of Appendix A
(e) Use acetone, methanol to wash out Resist.

(6) Connect the gate pads of the sample to Au pads of glass slide by wire bonding.
Wire Type: Au
Bonding Type: ultrasonic

(7) Put Device into Vacuum Pump with Device Holder Followed by Baking 24 hrs. at 90°C.
Vacuum Performance: 2×10^{-8} torr

APPENDIX D
TEM SAMPLE PREPARATION STEPS FOR SILICON WEDGE

1. Coat CVD silicon oxide 8000 Å on the sample.

2. Make a sandwich (sample is packaged in the middle part) and put on a stand.

3. Grind gradually and slowly until observe the wedge.

4. Polish with syton.

5. Flip sample and grind it until 100 μm thickness Left.

6. Dimple sample.

(a) Polish with 2-4 μm diamond paste until 35 μm thickness left.

(b) Polish with 0.3 μm aluminum oxide paste for 15 -20 min.

(c) Polish with syton for 10 -20 min.

(d) Place Mo ring on sample by epoxy + hardener followed by cure 2 hrs. at R.T..

(e) Remove sample with ring from stand by dipping in TCE (Trichloro ethane).

7. Ion mill sample.

Ion Miller:

Vacuum: $5x10^{-6}$ torr

Gas: Ar

Beam Angle: 20°

Gun Current: 0.5 mA

Mill Rate: 5 μm/hr at 4 kv

(a) Place sample with ring onto ion mill specimen holder.

(b) Ion mill until a small hole is formed nearly a wedge (usually takes 8 hrs. to generate a small hole).

(8) Sample is ready for TEM examination.

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