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Process technology and characterization for field emission devices

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Process Technology and Characterization for Field Emission Devices

by

Jong Min Kim

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ABSTRACT

Title of Thesis: Process Technology and Characterization for Field Emission Devices

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Thesis directed by: DR. WILLIAM N. CARR

Vacuum microelectronics is a new research field which applies semiconductor process technology to the fabrication of micron-dimensioned electron devices. Vacuum microelectronics is made possible by advances in microstructures and nanofabrication technology. Vacuum microelectronic devices are further characterized by a wide operating temperature range, nuclear radiation immunity, higher emission current density potential, and lower power consumption than that of thermionic emitters. The low mass of the electron provides a higher carrier mobility than GaAs or any solid state device. These features offer the potentials for wide variety of applications.

In this dissertation, electron field emission structures applicable to a variety of vacuum microelectronic devices have been fabricated and characterized. The cathodes are micromachined of N-type silicon and tungsten using a combination of ultraviolet liftoff lithography and reactive ion etching. A minor emphasis has been placed on micromachining surface-grooved structures for applications that include both vacuum microelectronics and optical microsystems. Optimized processing,

device modeling, and physical/electrical characterization are key elements in the research described.

The control of sidewall angle, cavity depth, and apex radius for ridge structures in silicon has been a major focus of this thesis. Reactive ion etching techniques have been studied for sidewall angles up to 45^0 and ridge apex radii of approximately 40nm.

A fluorine-based chemistry (CF_4/O_2) with oblique angles (tilted wafers) for the incident beam electric field and overetching is used in separate experiments. The use of deep UV-hardened photoresist and image- reversal aluminum liftoff for reactive ion etching masking are compared. Aluminum as a shadow mask for reactive ion etching micromachining has the advantage of lower etch/sputtering rates and higher temperature tolerance compared to photoresist in the CF_4/O_2 system. Typical etch conditions used were CF_4/O_2 flow rates of 20/2 sccm, pressure 10 to 40 mTorr, and etch duration 30 min. This thesis is one of the first detailed studies of reactive ion etching comparing tilted and untilted wafer substrates.

A new process technology for vacuum microelectronic diodes is shown, and device design with a knife-edge cathode and a lateral electron trajectory is implemented as a characterization tool. The cathode structure for these devices consists of a titanium:tungsten /tungsten film sandwich overlaying an aluminum adhesion and sacrificial film. The aluminum film is partially sacrificed to achieve the necessary sharp edge of tungsten metal surface for field emission. The tung-

sten and titanium metals are deposited by dc magnetron sputtering followed by liftoff lithography and thermal annealing. Selected devices with a cathode to anode spacing of 0.8 μm are electrically characterized in 2 to 5 $\times 10^{-9}$ Torr vacuum. A maximum static current of 26 μA current is obtained. The I-V characteristics of lateral trajectory devices with a knife-edge cathode are compared with Fowler Nordheim theory. Good agreement occurs if the cathode apex radius is approximately 10nm. Based on a Fowler Nordheim model the effective fraction γ of the knife-edge emitting electrons is in the range 3 to 80%.

This research includes the first experimental verification of the effect of deflection electrodes to confine the electron beam. Characterization and modeling comparisons for vacuum microelectronic devices with a knife-edge cathode and lateral electron trajectory are described for the first time.

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I also thank the co-advisor Dr. Robert J. Zeto, Branch Chief at U.S. Army ET & DL, Fort Monmouth, N.J. for every bit of excellent comments and helps. I also thank Dr. Kenneth Sohn for unconditional helps to my study for 7 years, and thank Dr. D. Misra and Dr. Sosnowski for the nice advises.

Thanks to Dr. Robert Marcus, I achieved my RIE etching career and applied that technology to vacuum microelectronics. His pioneering work on vacuum microelectronics cheered me up greatly.

I would also like to express my appreciation to my colleques, R. Piekarz, J. Conrad, C. Mulford, W. Windsor, L. Poli, C. Kondek, J. Perna, A. Ballekdjian, B. Widuta, E. Zakar and Dr. Daeshik Woo at U.S. Army, ET & DL, Fortmonmouth, N.J. who gave me their assistance in many ways.

I feel particularly grateful to my brother Jongoon Kim, sister-in-law Bobae Lee, my lovely nephew and niece, Ian and Elin in U.S. who helped and loved me greatly.

I really want devote this thesis to my late brother-in law Joosuk Do died at the age of 38 years.

Many thanks go to my mother, brothers and sisters in Korea.

VITA

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Contents

List of Figures

List of Tables

Chapter 1

Introduction

Vacuum microelectronics is a new field made possible by advances in microstructures and nanofabrication technology. Vacuum microelectronic devices are further characterized by a wide operating temperature range, nuclear radiation immunity, higher emission current density potential, and lower power consumption than of the thermionic emitters. The low mass of the electron provides a higher carrier mobility than GaAs or any solid state device. These features offer the potential for wide variety of applications.

In Chapter 2, the recent trends of applications are described and concepts of device physics and integration are discussed. In Chapter 3, fundamentals of RIE are presented. Chapter 4 describes the applications of silicon micromachining to the formation of vacuum microelectronics. Detailed qualitative and quantitative descriptions are given for different mask layers.

Chapters 5 and 6 describe the new processing technology for the fabrication of unique field emission tips for lateral electron trajectories. Chapter 5 gives an analysis and new technology for the recessed diode with cusp cathode and two deflecting control grids. Chapter 6 describes processing and characterization of the tungsten knife-edge emitter. Chapter 7 presents the summary and conclusions of this research together with a table of published field emission tip results.

Chapter 2

Theoretical review and applications

2.1 Theory of electron emission

Field emission is dependent upon the shape and work function of emitting material or vacuum environments which affects the work function.

Work function for field emission is modeled by (1) a close packed surface, and by (2) a loosely packed surface [Ref.2-1]. If the extrinsic species are adsorbed into the surface, the work function may increase or decrease by the amount of $\Delta\phi = 2\pi P_i N_s \theta$ where P_i, θ, N_s are the dipole moment, the fraction of filled surface sites and the number of ad-sites, respectively.

For a strong electrical field, the field emission barrier may be sufficiently reduced in width so that the excited electrons can tunnel out into the vacuum. The surface potential barrier profile from Gomer and Modinos [Ref.2-1, 2-2] is shown in Fig.2.1 for a metal surface.

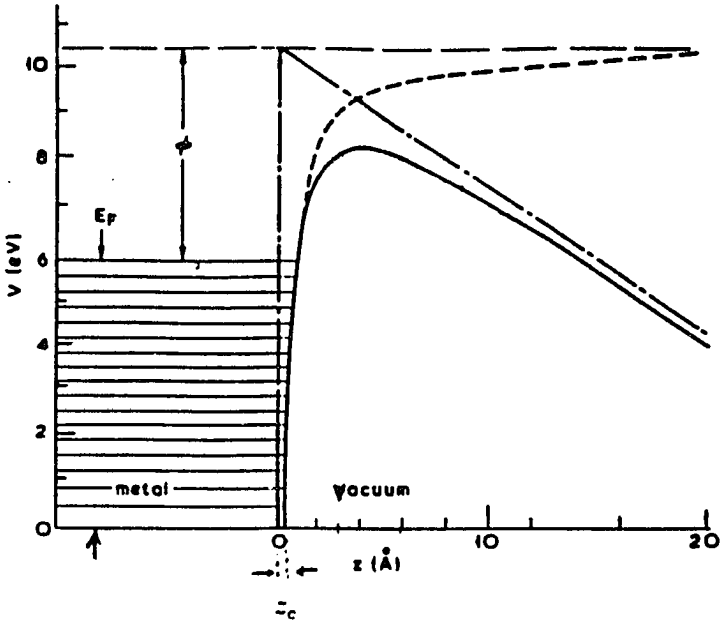


Figure.2.1. The surface potential barrier seen by an electron in a field emission experiment(solid line). The contribution of the image potential and of the applied field (F= 0.3V/Å) are shown by the broken and the broken-solid line, respectively [Ref.2-2]

A infinitely-deep metal surface from $-\infty$ to 0 in z axis is assumed in Fig.2.1. An electron situated at a distance z from a plane surface of perfect conductor is affected by the image force. Therefore, the potential energy of electrons on the vacuum side of the metal -vacuum interface, is given by

$$V(z) = E_F + \phi - \frac{e^2}{4z} \tag{2.1}$$

where E_F is Fermi level and ϕ is work function (see Fig.2.1) and is valid for $z \geq 3\mathring{A}$. The units of $V(z)$, E_F and ϕ are eV.

For $z \leq 3\mathring{A}$, the detailed shape of the potential barrier also depends on the metal surface [Ref.2-2]. When the external electrical field F is applied, the electron potential energy is given by

$$V(z) = E_F + \phi - \frac{e^2}{4z} - eFz, \quad (z \geq z_c)$$

$$V(z) = 0, \quad (z \leq z_c) \tag{2.2}$$

where z_c is determined by $V(z_c) = 0$.

The transmission coefficient and reflection coefficient for electron emission are obtained by WKB method from the Schrödinger equation with the variations of above mentioned potential energy [Ref.2-3]. A general emission current density equation which is known as the **Fowler -Nordheim equation** derived using the WKB approximation [Ref.2-4] is at low temperature,

$$J(F) = A'F^2 \exp(-B'\phi^{3/2}/F) \tag{2.3}$$

where,

$A' \equiv e^3/[16\pi^2\hbar\phi t^2[\frac{(e^3F)^{1/2}}{\phi}]]$

$B' \equiv (4/3e)(2m/\hbar)^{1/2}v[\frac{(e^3F)^{1/2}}{\phi}]$

$t(y) \equiv v(y) - \frac{2}{3}y\frac{dv}{dy}$, where v and y are numerically defined from the derivations [Ref.2-4]. This Eq(2.3) is the most important equation in field emission theory that is describing the relationships between current emission and work function.

2.2 Quantitative analysis of emission mechanism

From the field emission current given by Eq.(2.3), $\ln(J/F^2)$ versus 1/F may be plotted. The plot has straight line whose slope is given by

$$S_{FN} = \frac{d\ln(J/F^2)}{d(1/F)} \equiv -0.683s(\frac{3.79\sqrt{F}}{\phi})\phi^{3/2} \tag{2.4}$$

where $0.3V/\mathring{A} \leq F \leq 0.5V/\mathring{A}$ and $s(y) = v(y) - y/2\frac{dv}{dy}$.

While in principle work function could be determined from a measurement of slope, the surface potential barrier due to the image force and local effect such as adsorption prohibits the absolute value of work function from being determined[Ref.2-2].

The emission current with image force is at least 10 times lower than that without image force. [Ref.2-5]. The slope of the related FN plot with image force

included is changed by less than 5 % from the slope of the FN plot without the image force.

The potential barrier is lowered by the external electrical field. The work function is partly determined by lattice structure, temperature and adsorption of other species. Chemisorbed atoms form a strong electrostatic bond and dipole layer at the surface. Electropositive atoms like thorium and barium are adsorbed as positive ions and make it easier for electrons to tunnel out into the vacuum, by lowering the work function. Electronegative atoms like oxygen and fluorine make it difficult for an electron to escape by increasing the work function.

2.3 Field emission from semiconductors

Processing steps may leave an adsorbed layer on the semiconductor surface. The adsorption layer, like ionic bonding on a semiconductor surface, forms surface states with a sharply defined electron dipole layer. This is analogous to the work function increment resulting from adsorption on a metal surface. If there is no surface charge, the penetration of the applied field increases and work function is reduced. If the electronegative surface charge is high enough, charge is densified and field penetration is difficult increasing the work function.

The effective work function ϕ for electron emission into a vacuum results from the sum of several potential barriers existing at the surface.

$$\phi = \phi_i + E_g \pm \phi_F + \phi_s \tag{2.5}$$

where ϕ_i, E_g, ϕ_F and ϕ_s are the intrinsic work function, the energy band gap, the energy barrier variations due to Fermi energy level penetration, the energy barrier variations due to doping density. For a lightly doped N-type semiconductor without surface states, the effective work function is $\phi = \phi_i$ corresponding to a near-intrinsic, low field condition. For a lightly doped P-type semiconductor the

work function increases by the amount of the energy band gap to $\phi = \phi_i + E_g$. For a heavily doped P-type semiconductor, the work function increases further by the amount of Fermi energy penetration ϕ_F into the valence band to $\phi = \phi_i + E_g + \phi_F$. For heavily doped N-type is decreased by the amount of Fermi energy level penetration ϕ_F into the conduction band to $\phi = \phi_i - \phi_F$. When the semiconductor bulk doping is small, the electric field penetrates into the semiconductor and the surface space charge layer widens. Thus the work function component ϕ_s is increased further. For instance, in a heavily doped N-type semiconductor $\phi = \phi_i - \phi_F + \phi_s$ where ϕ_s is the additional energy barrier due to N-type doping density N_D where a narrow surface charge layer forms. From Poisson's equation, the additional energy barrier due to the electric field penetration into the semiconductor is

$$\phi_s = \frac{2\pi N_D e l^2}{K} \tag{2.6}$$

where N_D, e, l, and K are the donor doping density, the charge of electron, the thickness of the surface state, and the dielectric constant, respectively.

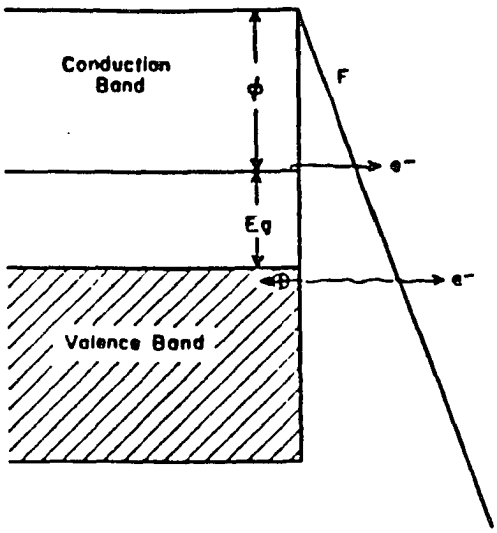
The effect of additional surface positive charge (for example, thorium and cesium) is to reduce the thickness of the surface space charge barrier and thus lower the work function for N-type material. Similarly, the effect of electronegative surface charge (for example, fluorine or oxygen) is to increase the width l of the surface space charge region and thus increase the work function component ϕ_s.

For the emission from the conduction band from the Fowler Nordheim theory, the current density is given by

$$J = \frac{2neKT}{(\pi m \phi)^{1/2}} \exp(-6.8 \times 10^7 \phi^{3/2}/F) \tag{2.7}$$

where n, e, K, T, m, and F are the number of electrons per cm^3 in the conduction band, the charge of electron, the dielectric constant, the temperature of field emitter, the mass of electron, and the surface electric field, respectively [Fig.2.2].

(a)



(b)

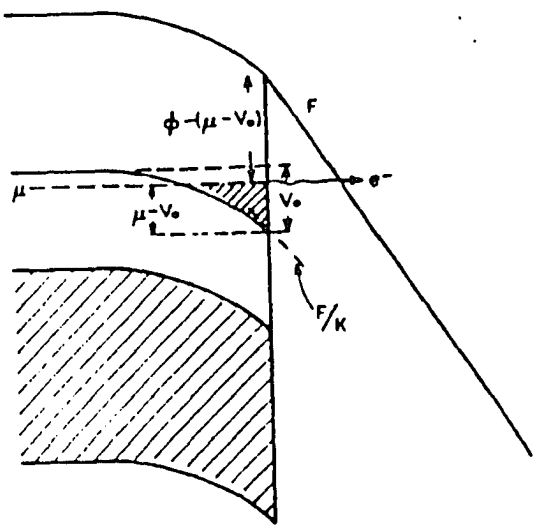


Figure2.2. (a) Diagram illustrating field emission from a semiconductor; Emission from the valence band results in creation of positive hole there. (b) Field emission from semiconductor with field penetration: μ=Fermi level, ϕ=ionization energy, V_0=lowering of the conduction band at the surface due to field penetration, $\phi - (\mu - V_0)$=effective work function, F=applied field, F/K=field in semiconductor at surface. [Ref.2-1].

When the field penetration without surface state effects is assumed [Fig.2.2.b], the emission current density is obtained by multiplying J in Eq.(2.5) with $e^{-V_0/kT}$, since the energy lowering V_0 of the conduction band at the surface due to field penetration is induced.

The total emission current density for semiconductor can include components of electron emission from energy levels in both the conduction and valence bands. For instance, a P-type semiconductor emitter operating at a high temperature can have appreciable electron population in the conduction band and thus a strong J_c component:

$$J_c = e\int_0^{\infty} j_c(\epsilon_s)d\epsilon_s$$

$$J_v = e\int_{-\infty}^{-E_g} j_v(\epsilon_s)d\epsilon_s$$

where ϵ_s, e, and E_g are the energy distribution, the magnitude of electronic charge, and the energy gap between conduction band and valence band, respectively. The parameters in the j_c, j_v, are total energy distributions of the electron from the conduction band, and the valence band, respectively [Ref.2-6]. The integration limit (0 in the above eq's) reference potential is at the bottom the conduction band.

A similar analysis applies to the case of metallic emitters. For the case of metallic emitters of course the only valid case refers to extremely heavily doped N-type bulk material without any energy band gap. For the case of metals, the effective work function for tunneling electrons simplifies to $\phi = \phi_i + \phi_s$ consistent with the above discussion. In the case of both semiconductors and metals, the presence of significant surface charge species Q_s can very significantly raise or lower the overall work function by affecting ϕ_s.

The previous discussion of the effect of surface charge Q_s has been simplified. A more precise discussion follows.

2.4 Field emission through dielectric layer

There are two types of adsorption which form surface dielectric layers; physical adsorption and chemical adsorption. Physical adsorption has Van Der Waals force coupling, and chemical adsorption has tight bonding for one or more atomic layers. Chemical adsorption is generally a type of covalent bonding instead of ionic bonding. Typically, the maximum thickness of an adsorbed layer film on semiconductor and metal is 20-30 Å. Tunneling through an adsorbed dielectric layer is affected in that (1) the field within dielectric shell (reduced by 1/K where K is the dielectric constant), (2) the image potential is reduced by 1/K, (3) the potential energy of electrons in the dielectric layer is reduced by an average polarization energy, (4) each inert gas atom such as Ar, Kr, and Xe is electropositive and represents a short range but deep attractive potential for electrons. Factors 1) and 2) contribute to an increase, while 3) and 4) contribute to a decrease of effective work function, respectively.

The potential energy of an electron in an electron emission on the vacuum side of adsorbate covered surface is given by

$$V(z) = E_F + \phi_{ad} - (\frac{eF}{K})l - eFz - \frac{(K-1)e^2}{(K+1)4z} - \frac{2e^2}{(1+K)4(z+l)} \tag{2.8}$$

where E_F, ϕ_{ad}, F, and l are Fermi level, work function of the adsorbed layer, external applied field, and thickness of dielectric layer, respectively [Ref.2-6]. Equation (2.8) is for $z \geq z_c$ as in Fig.2.1 with the adsorbed layer. Eq.(2.2) also represent the potential energy of electron for $z \geq z_c$ as in Fig.2.1 with the clean surface. The effects of a surface oxide to increase the work function were shown recently by Yang et al [Ref.2-7].

An additional case, for the tunneling through oxide, including MIM (metal-insulator-metal), MOMOM(metal-oxide-metal-oxide-metal) and MOMVM(metal-

oxide-metal-vacuum-metal) surface film has been reported by Ref.2-8.

When the metallic adsorbate on tungsten is considered, the work function is normally reduced, except for Au on tungsten where the work function increases [Ref.2-9]. This depends on the properties of metal/material at the metal/vacuum interface. However, the nature of these phenomena is not clearly understood [Ref.2-9].

2.5 Design of a field emitter

Dyke et al [Ref.2-10] reported the relationships between the emission current density and the electric field for a diode (emitter and anode). This reference expresses the electric potential at a tip:

$$V = [\frac{V}{R^n}][r^n - r_0^{2n+1} r^{-n-1}] P_n(cos\theta) \tag{2.9}$$

in spherical coordinates -r and θ, and where R, V, r_0, $P_n(cos\theta)$ and θ are the emitter-to-anode distance, applied potential, radius of emitter sphere, Legendre polynomials and cathode sidewall angle with respect to the vertical axis for vertical type cathode, respectively.

A typical field at the tip is $10^7 \leq F \leq 10^8$ V/cm. As θ increases, the electric field rapidly decreases and the emission current also decreases. McCord et al [Ref.2-11] used the spherical model in the method of images to get an improved calculation for STM applications. His results show field distributions similar to those obtained by Dyke [Ref.2-10]. To achieve the maximum emission current, the tip radius should be as small as possible. The sharpest tip with an atomic range radius has been reported by Marcus et al [Ref.2-12].

Factors limiting the maximum current density of a field emitter array (FEA) for a various tips was described by Utsumi [Ref.2-13]. One fundamental limit for current density in an FEA is thermal instability due to Joule (I^2R

loss) heating by electrical current flow in a nano scale emitter. The field emission current is approximated by $I = Jr_0^2$ where J and r_0 are the field emission current density at the emitter and the emitter radius, respectively [Ref.2-13]. If I is too high, Joule heating effect becomes serious and the emitter tip may be metallurgically damaged. Utsumi [Ref.2-13] calculated the maximum emission current density before melting to be $J_{max} = 10^6 \frac{\sqrt{2T_M \sigma K}}{h} A/cm^2$, where σ,K, T_M, h are electrical conductivity$(\Omega\text{cm})^{-1}$, thermal conductivity, melting point(^0C) and emitter height (cm) from the substrate, respectively, simply assuming a simple cone shape emitter pedestal.

2.6 Factors governing field emitter operation

Electrical breakdown strength, the tip thermal stresses, and the maintenance of a clean emission surface are factors limiting maximum emitter current over a period of time. For this purpose, an ultra high vacuum (UHV) system is required. However, the operation of these devices in vacuum at pressures as high as 10^{-3} Torr atmosphere has been demonstrated. [Ref.2-14,15].

2.7 Modeling factors for the device integration

Spindt et al [Ref.2-16,17] have reported simple design models for devices with a vertical (normal to substrate) electron trajectory. Referring to their data, the distance between grid and emitter, and the height of the tip must be considered. For a wider gap between anode and cathode, a higher voltage bias is required. Reduced anode-cathode separation d in Fig.2.3 reduces the bias voltage needed. At a larger bias voltages the device dielectric layer can be broken down electrically. In order to avoid these problems, the careful design techniques are required. With small bias voltage, the smaller emitter radii (r_0 in Fig.2.3) and the higher tips (h in

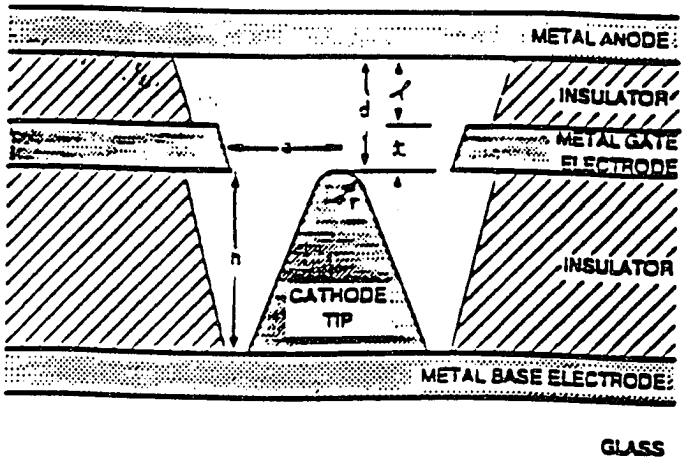


Figure 2.3: Field emission vertical microtriode model [Ref.2-14]

Fig.2.3) are preferred. From Brodie [Ref.2-14], $d = 0.5\mu$m, $h = 1.5\mu$m, $V_a = 20V$, $V_g = 10V$ are feasible for the field emission without electrical breakdown where V_a and V_g are anode and gate bias, respectively from Fig.2.3.

Orvis et al[Ref.2-18] has also presented the design rules for vertical devices. According to Orvis et al, for P -type material, the electrical field will create a depletion region on the silicon tip that will significantly reduce the field enhancement and the field emission rate. Heavily doped N-type (more than 10^{17} atom/cm^{-3}) is a superior material. It does not form a depletion layer and works like a metal surface. The electric field effect at the grid is important, since the emission from the electron extraction (positive bias) electrode may occur. This secondary emission effect represents undesirable leakage current from the extraction electrode to the anode in 3-element devices.

Electron trajectories and design descriptions have been published for a

lateral device modeled by Carr et al [Ref.2-19] with a SIMION*.

* Simulation program from the Idaho National Engineering Center

Chapter 3

Fundamentals of RIE

3.1 The concepts of RIE system

A reactive ion etching system is shown in Fig 3.1(a) with voltage potential distributions between the anode and the cathode in Fig.3.1(b). Fig.3.1(a) shows the block diagram of typical reactive ion etcher. This system has an asymmetrical electrode structure. Between electrode and plasma, a Crooke's dark space is formed[Ref.3-1]. This dark space is also called the sheath area. A detailed description and analysis of the dark space is given by Brown [Ref.3-2].

Positive ions are created and accelerated primarily in the dark space. The potential difference across the dark area is an important parameter for the ion etching and is given by

$$V_p - V_{fi} = \frac{kT_e}{2e} ln \frac{M_i T_i}{M_e T_e} \tag{3.1}$$

where V_p, M_e, M_i, V_{fi}, T_e, and T_i are plasma potential, mass of electron and ion, substrate potential and temperature of electrons and ions respectively [Ref.3-3].

Since the plasma has a very low electric field, the space within the plasma is essentially equipotential at V_p. If an isolated substrate is inserted into the plasma, the substrate takes on a "floating potential" V_{fi}. The plasma potential V_p is always greater than the floating potential V_{fi}. This potential $V_p - V_{fi}$ drives ions up against the substrate and enhances ion etching process.

Fig.3.1.b shows the potential distributions with V_a and V_c which are the anode and the cathode potentials, respectively. The substrate is mounted on the cathode with V_c. The potential difference between the cathode and plasma plays a major role of the acceleration of the ions and the electrons in the system.

In order to provide maximum rf power delivery in the system, the capacitance for impedance matching should be adjusted in Fig.3.1.[Ref.3-4].

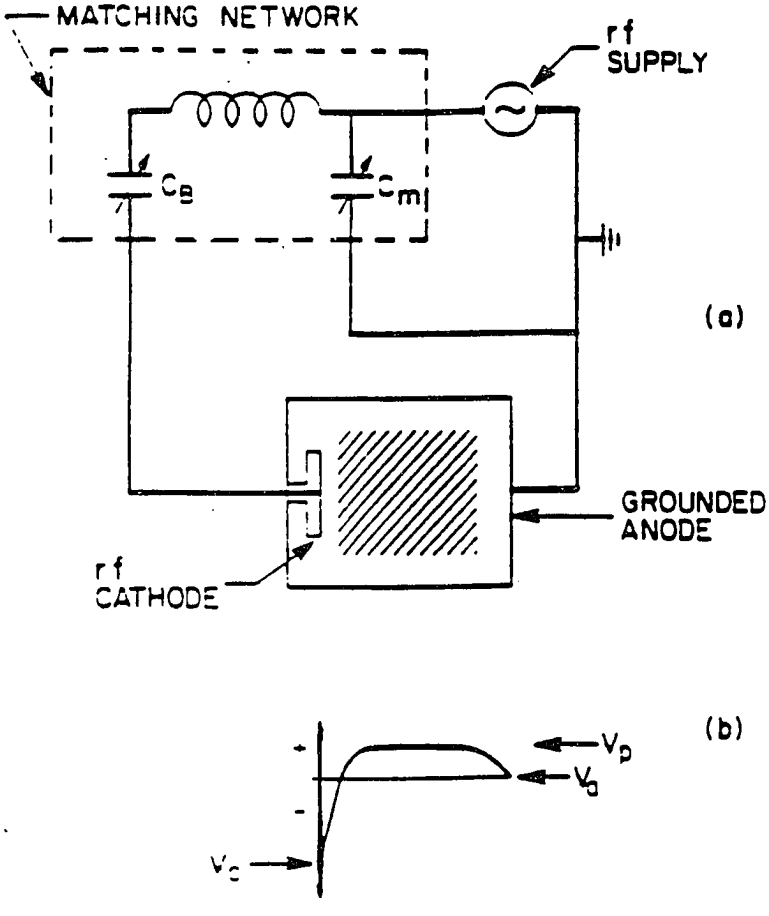


Figure 3.1: Schematic representation of (a) reactive ion etching system and (b) plasma potential distribution between anode and cathode

3.2 Etch variables

There are several variables of RIE that strongly affect the etching process. Control variables are as follows: the residence time of the etchant gases, the conductance of the pumping system, chamber operating pressure, rf power of the RIE, rf frequency of the RIE, electrode spacing, and area of electrodes.

As each substrate etches through different etching mechanisms, flow rate for different etchant gases must be carefully selected for different substrates. The following detail analysis refers to Chapman and Vossen et al [Ref.3-5,6].

3.3 Selection of etchant gases and etching mechanism

The precise mixtures for etchant gases should be decided empirically. Generally, Al and III-V compound semiconductors are etched with chlorine-based etchants, while dielectrics and silicon /silicides are etched with fluorine-based gases. Refractory metals including W and Mo are also generally etched with fluorine-based gases as the sublimation temperature of the W and Mo with fluorine gases is lower than that with the chlorine-based gases.

For silicon etching, oxygen gas is typically mixed with CF_4, because oxygen increases the etch rate and prohibits polymer formation during etching. The maximum etch rate of silicon is obtained when the flow ratio of O_2/CF_4 is 0.15-0.20 [Ref.3-7,8].

The etching mechanism for the silicon with these gases (CF_4 with O_2) is given as follows: when CF_4^0 is bombarded with electrons, major ion species for etching such as CF_3^+ are generated. This CF_3^+ sputters the silicon surface and breaks the Si-Si bonds. This results in the highly reactive radicals such as CF_3^0 or F^0 reacting with the dangling Si surface bonds, and forming the volatiles such

as SiF_4 which can be exhausted. The role of the oxygen molecule in this step is that it removes carbon atom by forming CO_2 gas, and increases net atomic F^0 concentration. The increased F^0 radical induces the high etch rate by forming SiF_4. If the O_2 concentration is too high, the Si etch rate decreases because oxygen reacts with F^0 and reduces the amount of the F^0 radical. If the O_2 concentration are too low, the polymer layer can be easily formed [Ref.3-9].

To control the etching of SiO_2, H_2 gases are normally mixed with CF_4. Since H_2 removes F^0 radical, the density of C^0 radical increases. The C^0 radical reacts with the oxide to form volatile CO_2. At high H concentration, the ratio of F/C decreases and $(CF_2)_n$ polymer is formed. It is caused by the association of fluorocarbon radicals on the surface at high pressure [Ref.3-9].This polymer passivates Si surface and hinders it from being etched.

In either silicon or silicon dioxide, the addition of Ar gas to fluorine gas increases enormously the etch rate because Ar^+ ions sputter the surface with a higher yield compared with other positive ions [Ref.3-10]. Detailed thermodynamic mechanisms and surface reaction chemistry are explained in Ref.3-10.

In order to predict the etch rate of any specific reactive ion etching process, three mechanisms must be considered: (1) sputter etch, (2) chemical etch and (3) ion assisted chemical etch. The etch rate of silicon by these three mechanisms can be calculated as follows:[Ref.3-11]

1) Sputter etch rate is given by (unit; Å/min):

$$ER_p = \frac{\Gamma_{ion} Y_p}{N} \tag{3.2}$$

where Γ_{ion} ,Y_p, and N are the ion flux, the sputter yield of ions at ion energy under investigation and the atomic density of the substrate, respectively;

2) Chemical etch rate(does not require an initial sputtering):

$$ER_c = \frac{\Gamma_n Y_n}{N} \tag{3.3}$$

where Γ_n ,and Y_n are the radical flux and the reaction probability of radicals with substrate, respectively;

3) Ion assisted chemical etch rate (requires an initial sputtering):

$$ER_i = \frac{n\Gamma_{ion} Y_n}{N} \tag{3.4}$$

for $\Gamma_{ion} n \leq \Gamma_n$, and

$$ER_i = \frac{\Gamma_n Y_n}{N} \tag{3.5}$$

for $\Gamma_{ion} n \geq \Gamma_n$,

where n and Y_n are the number of adsorbed radicals activated by incident ion and the chemical sputter yield of the ion at ion energy, respectively. The detail chemistry of etch process (3) is a combination of (1) and (2).

Chapter 4

RIE techniques for silicon sidewall angle control in microengineering

This chapter describes RIE techniques with silicon substrates for initial processing of semiconductor field emitter array cathodes for vacuum microelectronics. A secondary focus is process research for optical reflecting gratings for opto- and micromechanical devices. These applications each require control of the sidewall angle and apex radius. In this chapter, we describe micromachining control of trenches with remainder sidewall angles varying from 15 to 60^0 and resulting apex ridge radii of as small as 40nm. A fluorine-based chemistry (CF_4/O_2) with oblique angles for the incident beam (tilted substrates) and overetching is used. The use of both deep UV-hardened photoresist and aluminum as RIE shadowmasks is compared. Unannealed aluminum as a shadowmask for RIE micromachining has the advantage of lower etch/sputtering rates and higher process temperature tolerance compared to photoresist in the CF_4/O_2 RIE system. Etch environments in the pressure range 30 to 80 mTorr with CF_4/O_2 flow rates of 20/2 sccm, rf power 100 to 200 watts, and etch duration 30 min. are described. Both tilted and untilted substrates mountings were studied. Under these conditions, the surface erosion is primarily a combination of ion milling and chemical etch mech-

anisms. Both P-type and N-type substrates of 100nm diameter wafers were used. Relatively sharp single- and double-ridged silicon structures were obtained using the photoresist shadowmask on untilted substrates. The photoresist shadowmask provides an advantage over Al only for the sidewall orientation $\theta_t = 20^0$ where we were able to specify a condition for obtaining a smooth optically reflective surface. The more vertical sidewall angles obtainable with the unannealed Al shadowmask should permit fabrication of field emitter cone or ridge cathodes on pedestals with higher height-to-width ratios. A field cathode pedestal with a more vertical sidewall results in a higher electric field at the electron emission tip or ridge.

4.1 Overview

The results described in this chapter are applicable to the initial processing of semiconductor cathodes for vacuum microelectronics devices[Ref.4-1,2,3] and to the controlling the blaze angle for optical diffraction gratings[Ref.4-4,5]. Each of these applications require control of the sidewall angle θ_s in Fig.4.1. Similar structures also have application for some trench capacitors and several specialized microelectromechanical devices. RIE as a tool for microengineering has been used for shaping sidewalls for laser mirror facets[Ref.4-6] and for SAW (surface acoustic wave) devices[Ref.4-7,8]. Related RIE studies describe sidewall control in trench structures including electrical device isolation and capacitors[Ref.4-9,10,11,12]. The effects of RIE processing on surface topography with both experimental results and modeling data have been reported for several VLSI circuit fabrications [Ref.4-13,14,15,16,17,18].

Previous work with RIE systems has established that the wafer tilt angle θ_t in Fig.4.1 and etch environment greatly affects the resulting sidewall angle θ_s. In

this chapter, we compare the use of photoresist versus aluminum as a shadowmask in the RIE etching process for controlling the sidewall angle and apex sharpness. Generally, the maximum etching anisotropy is obtained at maximum beam energy and lowest pressure under conditions generally described as ion beam milling. Ion beam milling becomes significant at pressure levels of less than 10 mTorr and totally dominates the etching process at pressure levels of 0.1 mTorr and less. The striations and general roughness of the ion beam milled surface , however, are unacceptable for our applications.

At pressures higher than 10 mTorr, the density of neutral chemical etchants becomes significant and a smoother, more isotropically etched surface results. We have etched at higher pressures ranging from 30 to 80 mTorr in order to obtain a more desirable surface smoothness and also to increase the etch rate. In this chapter, the ridged structures created by etching with both resist and metallic in situ shadowmasks for tilted substrates are compared with results for conventional etching of untilted wafers. The primary objective for this work is to develop and further understand the RIE process which permits control of the sidewall angle and the sidewall smoothness in the situations selected.

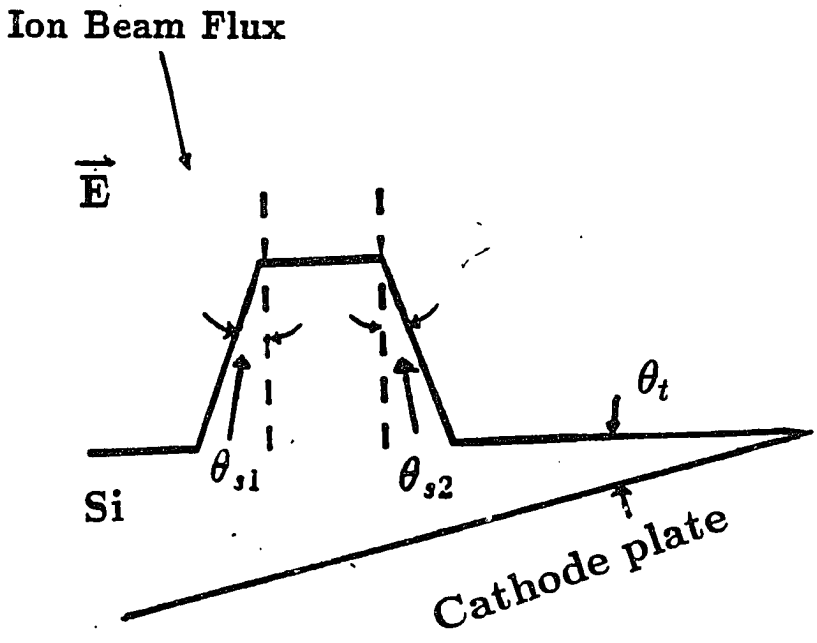


Figure.4.1. Definition of sidewall angle θ_s and wafer tilt angle θ_t

4.2 Experimental Procedures

Etching is done with an MRC RIE-51 system using CF_4, O_2, and Ar sources. The chamber base pressure was $2x10^{-5}$ Torr. The controlled operating pressures were in the 30 to 80 mTorr range during CF_4/O_2 flow. The 13.56 MHz power source of 100 to 250 watts provided 500 to 800 volt rf peak-to-peak voltage levels across the plasma diode. The reactor anode-cathode separation was 6 cm. Untilted wafers ($\theta_t = 0^0$) are positioned flat against the cathode. Stainless steel wedges were used to tilt the wafer on the cathode for the etching at angles of θ_t= 20 and 45^0. Wafers of [111] orientation, 100 mm diameter, heavily doped with arsenic or boron of less than 0.003 Ωcm resistivity were used. The wafers were patterned with four shadow films: (a) deep UV-hardened positive AZ1518 photoresist, (b) same resist not deep UV-hardened, (c) annealed Al, and (d) non-annealed Al. Processes (a) and (d) were found to be superior for our applications. Wafers were patterned using 1.23μm linewidth and 4.0μm pitch photomask which results in positive and negative final shadow "top hat" images for positive photoresist and Al, respectively. For the photoresist processes (a)and (b), a 1.8 μm thick resist was applied at 5000 rpm(40 sec.), preceded by HMDS (Hexamethyldisilazane: 10% in Xylene) spincoating at 6000 rpm (30 sec). The UV lithography exposure was preceded by a soft bake at 110^0C(1 min). The exposed wafer was developed with Shipley MIF312 (50% H_2O) followed by a hard bake at 125^0C (1 min). A final deep UV (flood exposure) hardening was accomplished while ramping the temperature from 125 to 180 ^{0}C (6 min).

The above mentioned processes (c) and (d) use an Al liftoff image-reversal technique for RIE-shadowing. An underlying 1.4 μm film of AZ 5214E resist was hardbaked at 125^0C for 1 min. and UV floodexposed at 365 nm wavelength. Following development in MIF 312 (50%H_2O), a 0.22μm e-beam deposition of Al

was made. The AZ 5214E sacrificial layer under the Al is next lifted off with an acetone rinse and ultrasonic agitation. The Al shadowmask now serves as an in situ "top hat" shadowmask for RIE micromachining. In our F-based RIE process an etch rate selectivity of 18X was observed for Si substrate versus the unannealed Al shadowmask. For comparison the Al film was annealed at 350^0C (30 min). The Al is etched with CF_4/O_2 (20/2 sccm) at 30 mTorr using a 200 watt power level. Following RIE the remaining Al was removed by $H_2SO_4 : H_2O_2$ (1:1) solution.

4.3 Results and discussion

4.3.1 Overetching with photoresist mask at $\theta_t = 0^0$

Figure 4.2(a) is the SEM cross section view of a structure obtained by two-step RIE etching with a deep UV-hardened AZ 1518 mask on untilted wafers. RIE in this experiment continues even after the photoresist was completely etched away. This is referred to as "heavy overetching" in this experiment. This figure shows symmetrical sidewalls for a wafer oriented for normal incidence (tilt angle θ_t= 0). A two-step etching sequence was used at a 100 watt power level. The first step at 80 mTorr(CF_4= 10 sccm) for 15 min. creates a ridge structure with rounded sidewalls. During the second step, pressure was reduced to 40 mTorr (CF_4/O_2= 30/7 sccm) for 15 min. and sharp sidewalls are created. The first step creates a smooth surface topography. The second step creates a more abrupt sidewall although the sidewall striations increase. The process etch profile for an untilted wafer etched with for different periods of time is shown in Fig.4.2(b). The "top hat" photoresist has been exposed to more incident photon energy near the sidewalls during the lithography process. This result of photo-diffraction in turn causes the photoresist to be more retardant to RIE etching near the sidewall

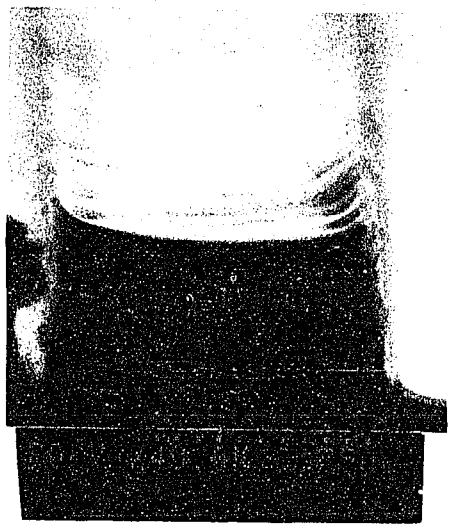
also.

In Fig.4.3(a) and (b), a single-step process is used to define ridge structures with N-type and P-type wafers, respectively. A sharp edge at the apex of the ridge is more readily obtained with the N-type substrate in Fig.4.3(a) compared with the P-type case of Fig.4.3(b). The debris on the left and right sidewall in Fig.4.3(a) is photoresist polymer. Flow rates of CF_4/O_2=20 / 2sccm at 30 mTorr for 30 minutes were used for N- and P-type substrates using power levels of 200 and 150 watt, respectively. The resulting apex radii of 40nm for the N-type and 300nm for the P-type material are estimated from SEM cross sections as in Fig.4.3(a) and Fig.4.3(b), respectively. N-type material provides the lower work function for field emission cathodes and is usually preferred for vacuum microelectronics.

The ridge structures of Fig.4.3 using a single-step process described above can be oxidized to fabricate Marcus-type field emission cathodes for devices with vertical electron trajectories[Ref4-19,20,21]. The double-ridge structure of Fig. 4.2 obtained with the two-step process may prove useful for obtaining cathode tips oriented at an oblique angle more useful for field emission devices with a lateral electron trajectory[Ref.4-22].

For the optical grating application, the P-type substrate resulted in a more planar sidewall (desirable) compared with the N-type starting material. The one-step process of Fig.4.3 is used for the optical structure.

(a)



Etch Time = 30 min

(b)

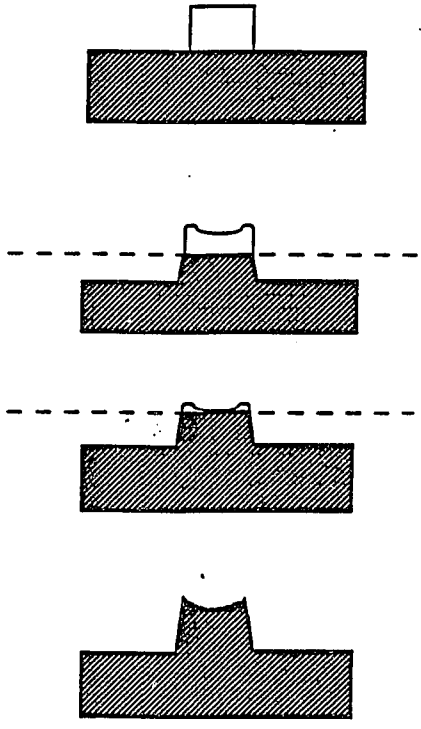
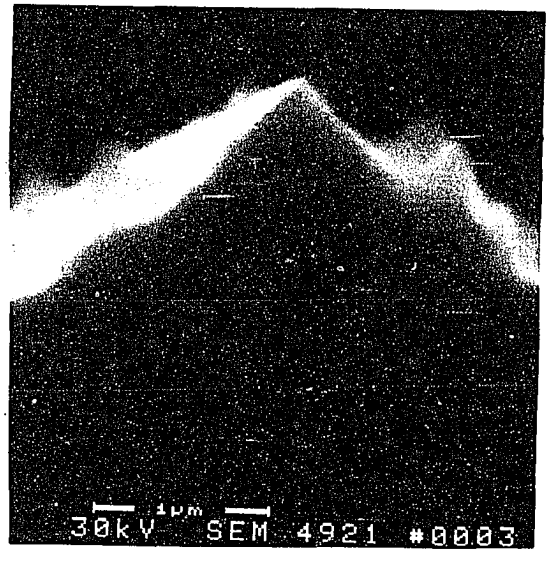


Figure.4.2. SEM micrograph of ridge cross-section with resist mask and normal incidence $\theta = 0^0$.
(a) N-type [111] with photoresist mask under CF_4/O_2=20sccm/2sccm at 30 mTorr, 200 watts with aceton cleaning. (b) P-type [111] under the same etching condition except 150 watts and Piranah cleaning.

(a)



(b)

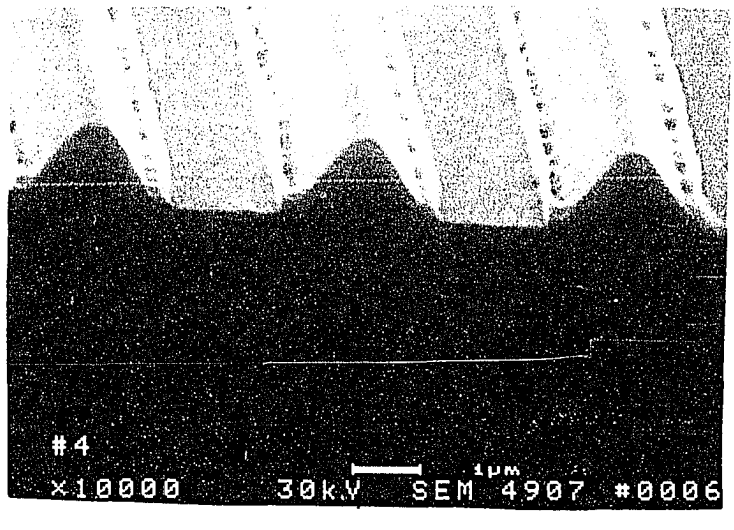


Figure.4.3. SEM micrograph of ridge cross section with resist mask and normal incidence $\theta = 0^0$.
(a) N-type [111] with photoresist mask under CF_4/O_2=20sccm/2sccm at 30 mTorr, 200 watts with aceton cleaning. (b) P-type [111] under the same etching condition except 150 watts and Piranah cleaning.

4.3.2 Wafer inclination with photoresist mask

A series of experiments with heavily doped N-type substrates were performed using deep UV-hardened photoresist as the only mask for defining trench structures. The sidewall angles θ_{s1} and θ_{s2} defined in Fig.4.1 are controlled by tilting the silicon wafer with respect to the plane of the cathode. Fig.4.4 shows a wafer tilted at an angle θ_t during the etch process with positions #1 through #5 defined along a diameter. The tilted wafer exhibits an increasing dark space thickness along the wafer diameter from position #1 to #5. The kinetic energy for ions colliding with the wafer surface increases from position #1 to position #5. The milling rate due to the ion also generally increases from position #1 to position #5 for tilted wafers corresponding to the increased energy of the incident ions as will be detailed in next section. The less dominant but important etching mechanism is that of the chemical reaction at the silicon surface. The chemical etch rate due to unmasked free radical generally decreases from position #1 to #5.

For untilted wafers $\theta_t = 0^0$ the dark space thickness is a uniform 1.5 cm. For a tilt angle $\theta_t = 20^0$ illustrated in Fig.4.4(b), the dark space thickness ranges from 1.5 cm at the cathode surface (position #5) to 0.5 cm at the wafer position near the anode edge (position #1). The dark space always forms on the wafer surface adjacent to the plasma glow.

Figure 4.5 shows three SEM cross section photo views and the corresponding drawn cross sections to show the photoresist shadowmask. The Fig.4.5 SEM views at position #1, #3, and #5 are all obtained with the wafer tilted $\theta_t = 20^0$ and with 30 min. of etching. Figures 4.5 (a), (b), and (c) show cross sections at position #1, #3, and #5, respectively. In Figure 4.5, the drawn cross sections each include an insert view of the photoresist shadowmask at $t = 0$ and $t =$ 5 minutes. At the start of etch t=0, the photoresist shadowmask is rectangular

in cross section as shown. Following a 5 minute etch the photoresist has eroded substantially as shown. The etching of the photoresist continues until it is entirely removed within approximate 15 minutes.

The sidewall angles θ_{s1} and θ_{s2} defined in Fig.4.1 vary with position along the diameter of the tilted wafer as shown in Fig. 4.5. The dominant surface removal mechanisms that can affect the sidewall formation are (1) ion milling due to physical ion bombardment, and (2) formation of volatile silicon compounds by neutral species. Also surface topography can be affected by buildup occurring when the volatile silicon compounds are redeposited on an adjacent sidewall by a local reactive redeposition. In addition, components of the photoresist "top hat" can be sputtered onto a sidewall and thus reduce the etch rate on the sidewall.

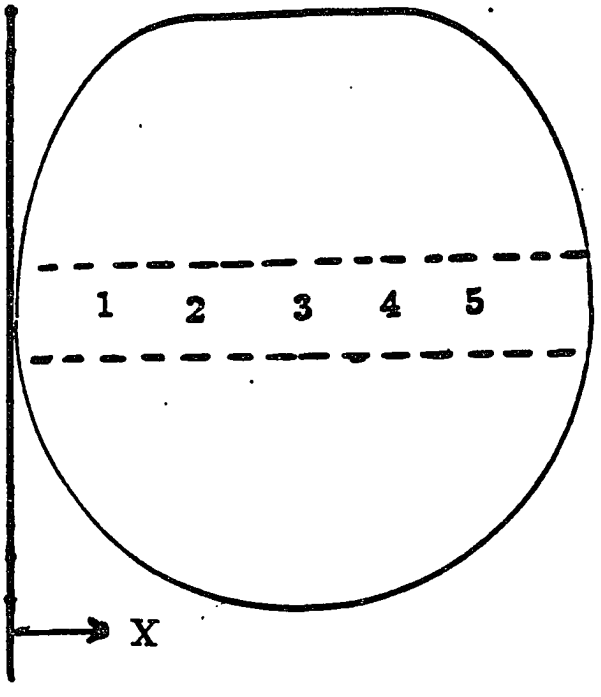
In Fig.4.5(a), the sidewalls are asymmetrical indicating an isotropic etching process at location #1. At this position the dark space has minimal thickness and the ions impinge upon the wafer surface with lower kinetic energy. The silicon surface here is closer to the plasma and should contain a higher density of free (un-ionized) radicals which are known to etch isotropically. In this case sidewalls of approximately 40^0 and 15^0 are observed for θ_{s1} and θ_{s2}, respectively.

In Fig.4.5(c) the maximum asymmetry is observed at location #5. The shadowed surface shows the striations characteristic of kinetic impacts from the incident ion stream. The maximum sidewall angle $\theta_{s2} = 60^0$ is observed for this case. The smooth surface of sidewall θ_{s1} is not characteristic of ion milling although a strong ion beam flux exists at location #5. The clean θ_{s1} surface in Fig.4.5(a) shows no evidence of sputtered photoresist debris. We believe the most likely mechanism accounting for the θ_{s1} surface smoothness is reactive redeposition excited by the ion beam. The sidewall topography shown in Fig.4.5(b) is intermediate between the (a) and (c) cases and thus is a mix of these same pro-

cesses. This technique provides the optical gratings with the desirable sidewall at position #1 and #5. There is a yield problem in that the most desirable sidewalls do not occur at all wafer positions #1-5.

Fig.4.6 summarizes the sidewall angle observations obtained from a series of SEM photos including those of Fig.4.5. A photoresist "top hat" or shadowmask is used in Fig.4.6 with a 30 min. etch and an N-type substrate tilted $\theta_t = 20^0$. This plot clearly indicates the complex nature of the erosion mechanisms as the sidewall angles θ_s vary across the wafer diameter. The sidewall angle $\theta_{s2} = 60^0$ obtained at location #5 is primarily due to the ion milling. If the shadowmask would remain intact and the etch time extended, we expect that θ_{s2} at location #5 will eventually equal to 20^0 in alignment with the incident ion beam. At location #1, the smooth sidewall $\theta_{s2} = 15^0$ observed is dominated by a chemical etching assisted by the directional ion beam. The fact that sidewall θ_{s1} is an almost constant 40^0 across the wafer diameter from location #1 to #5 is only fortuitus considering the complex interplay of surface erosion mechanisms. At other tilt angles $\theta_t = 20^0$ we do not expect the sidewall θ_{s1} to remain constant across the diameter.

(a)



(b)

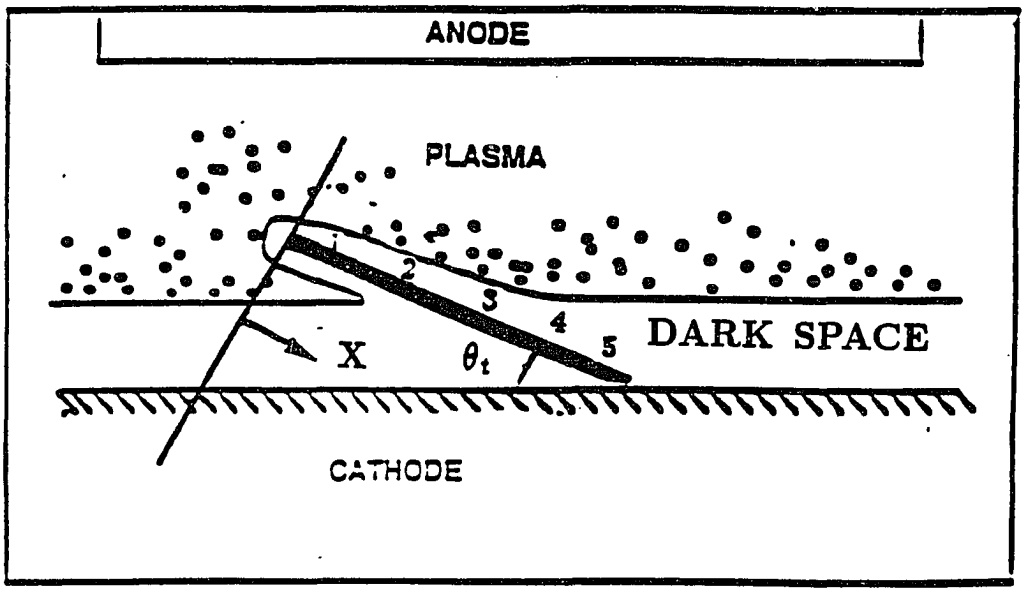


Figure 4.4: Reference notations defined (a) Reference locations defined on the wafer (b) Cross section of tilted wafer in chamber

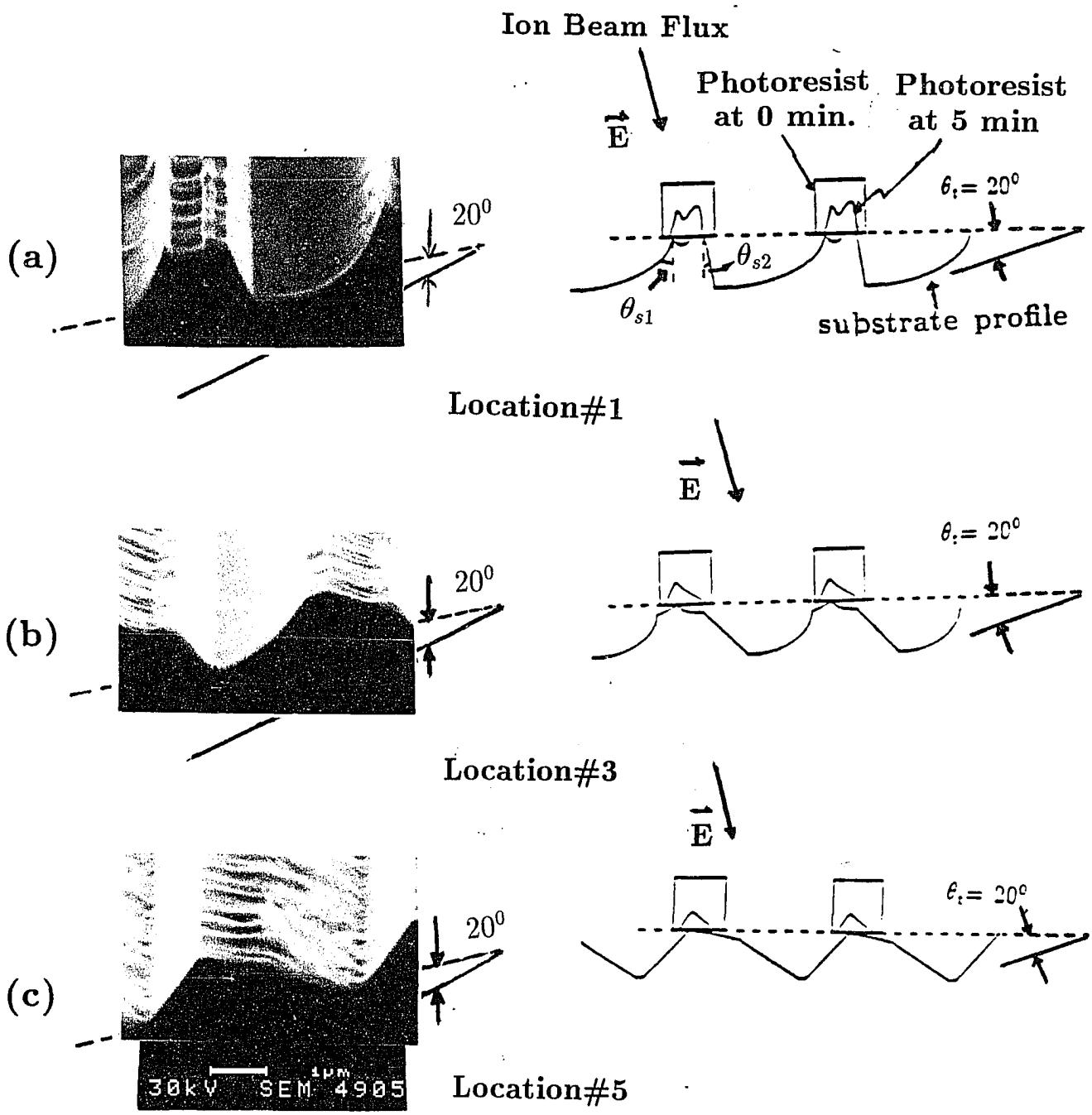
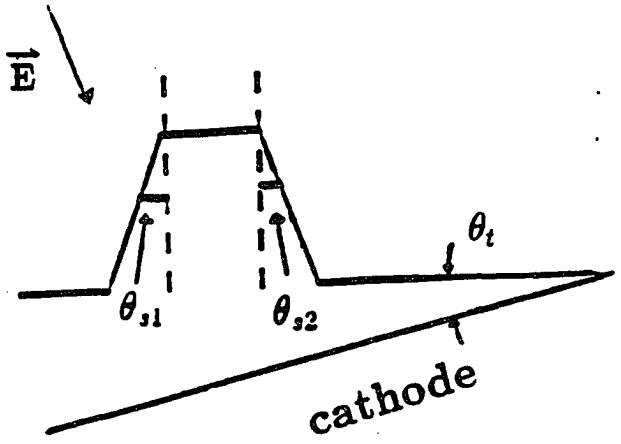


Figure.4.5 SEM micrograph (left) and corresponding cartoon view (right) showing side-wall profiles obtained with an N-type substrate using a photoresist mask θ_t=20°, CF_4/O_2=20 sccm/2 sccm, 30 mTorr, 200 watt for 30 min . (a) etch location #1. (b) etch location #3 (c) etch location #5

(a)



(b)

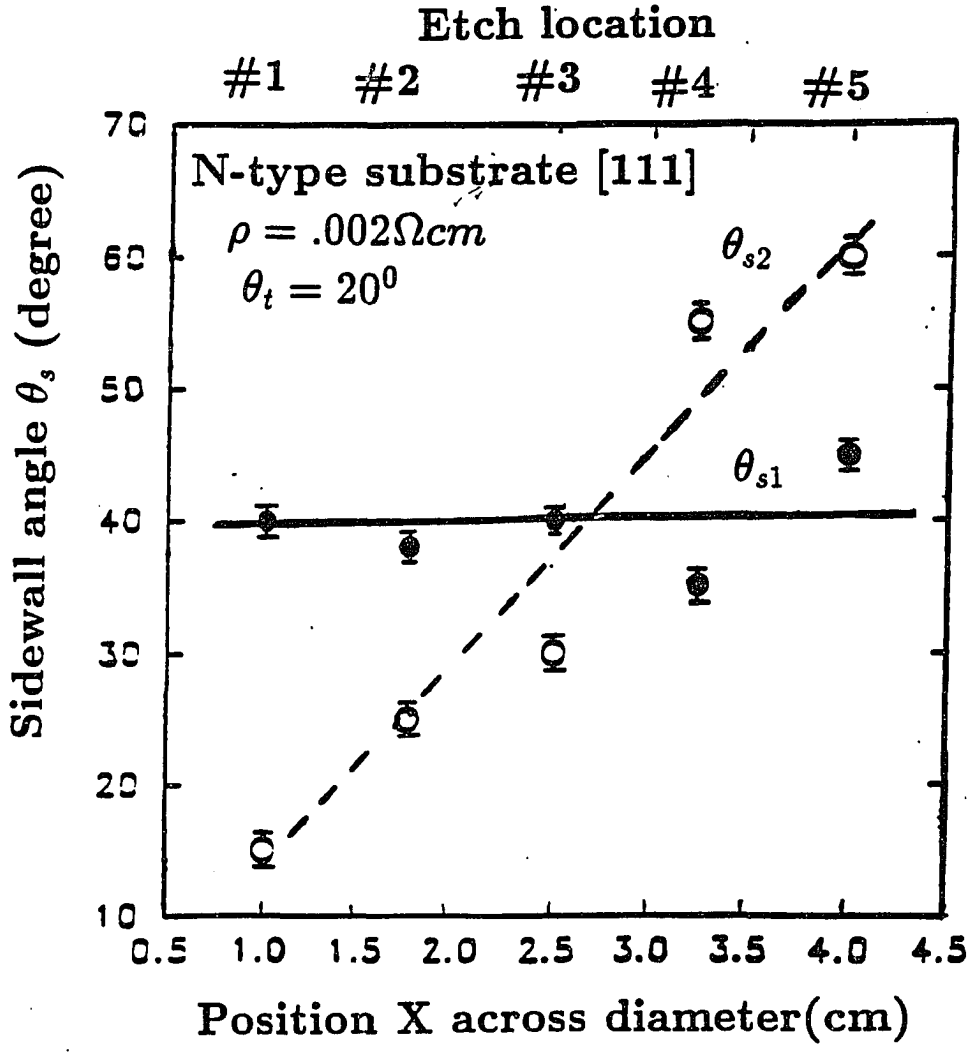


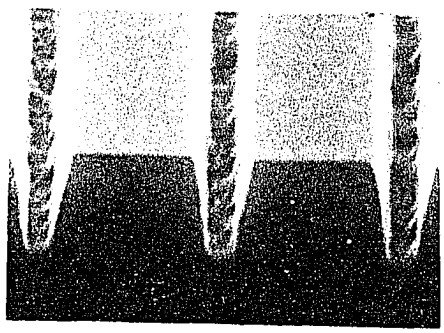
Figure 4.6: Sidewall angle definition θ_s as a function of etch location # with resist mask (a) notation defined, (b) cross section drawing. Data is fitted to a linear best fit.

4.3.3 Sidewall angle results with Al liftoff mask

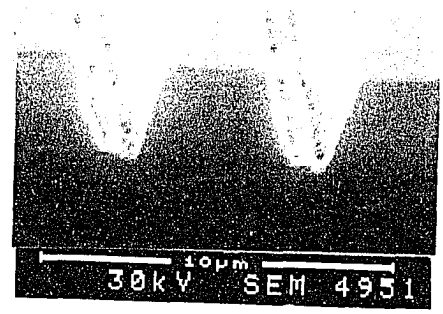
Unannealed aluminium etches a factor of 30x more slowly in the CF_4/O_2 system compared with photoresist. We have taken advantage of this differential in defining an Al liftoff process for creating deep trench structures on Si substrates. The RIE etch rate for Al with a CF_4/O_2 flow of 20/2 sccm and a 200 watt rf power level is 50Å/min ($\theta_t = 0^0$). This compares with an etch rate of 880Å/min for Si under the same conditions. The annealed Al mask withstands the RIE flux for 30 minutes, compared to 15 min for the photoresist and thus permits deeper substrate trenching compared with the previous case for the photoresist shadowmask.

A series of SEM views obtained using an Al "top hat" shadowmask are shown in Fig.4.7. These SEM cross section views are obtained at location #3. All trenches in Fig.4.7 are approximately 3.3 μm in depth. The mask used for the Al process is the reverse of that used for the previously described process in Fig.4.2,4.3, and 4.5. The Al shadowmask is defined using the mentioned liftoff lithography process. The sampled figures are obtained from the middle of the wafer at location #3.

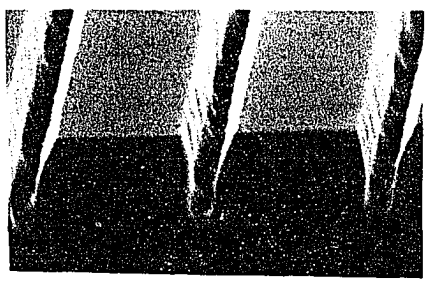
Figure 4.7(a) and (b) compare the trenching structure at $\theta_t = 0^0$ for unannealed and annealed Al shadowmasks, respectively. The aspect ratios, sidewall angles and trench depths were uniform over the entire wafer for this $\theta_t = 0^0$ case. While the annealed Al of Fig.4.7(a) survived the 30 min etch, the annealed Al mask was etched away at the periphery prior to the end of etch in (b). The increased size of Al grains which results from the thermal treatment accounts for the faster etch rate observed in the annealed Al film. The edge loss of the faster-etching annealed Al film during RIE resulted in the creation of the wider trench of Fig.4.7(b) compared to (a).



(a)



(b)



(c)

(d)

(e)

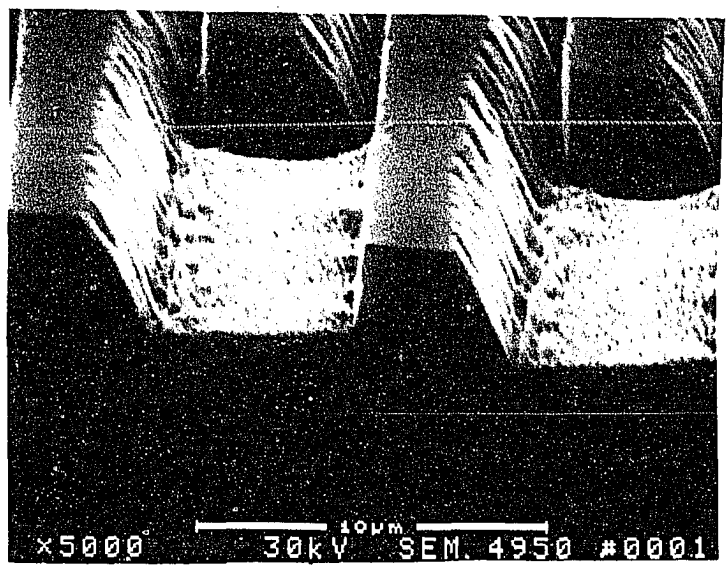


Figure.4.7 SEM photo micrographs of ridge formation with Al shadowmask on N-type substrate - CF_4/O_2= 20sccm/2sccm, 200 watt,30 mTorr for 30 minutes. (a) unannealed mask at $\theta_t = 0^0$, (b) annealed mask at $\theta_t = 0^0$, (c) unannealed mask at $\theta_t = 20^0$, (d) annealed mask at $\theta_t = 20^0$ and (e) unannealed mask at $\theta_t = 45^0$. All views are at wafer location #3

The sidewall cross section with the wafer inclined with a tilt angle $\theta_t = 20^0$ is shown in Fig.4.7(c) and (d), without and with annealing, respectively. For the $\theta_t = 0$ case, the annealed Al etch rate is faster compared to $\theta_t = 20^0$. The residue of annealed Al on the silicon surface in the case of Fig.4.7(d) compared to 4.7(b) is a consequence of the slower etch rate in (d). In Fig.4.7(e) with $\theta_t = 45^0$ at location #3, the texture of the θ_{s2} sidewall surface indicates that ion milling is dominating the erosion process and indicates a relatively small isotropic chemical etch component. In (e) the Al mask at the edge totally etched away and the the trench is widened considerably.

Chapman[Ref.4-23] reports that the etch rate increases approximately linearly as a function of the tilt angle θ_t for ion sputtering (milling), over the range $0 \leq \theta_t \leq 45^0$ at pressure levels of less than 1 mTorr. Our results cannot be compared directly since we have a much higher chamber pressure and use chemical reaction by free radicals with ion milling simultaneously. Our sidewall in Fig.4.7 shows only a partial striated surface characteristic of ion milling.

The sidewall angles θ_{s1} and θ_{s2} are plotted in Fig.4.8 as a function of the wafer tilt angle θ_t using the Al unannealed shadowmask. The sidewall angles θ_{s1} and θ_{s2} are approximately 12^0 for tilt angle of $\theta_t = 0^0$ and again cross at approximately $\theta_t = 28^0$ for the RIE parameters used. The sidewall angle θ_{s1} is maximum at an intermediate value as seen in Fig.4.8. The sidewall angle θ_{s2} is seen to increase constantly in Fig.4.8 with the tilt angle θ_t, where ion milling effects are especially important. In Fig.4.8, the sidewalls at $\theta_t = 0^0$ are of course symmetrical. As the substrate is tilted and etched at $\theta_t = 20^0$, one observes that sidewall θ_{s2} steadily increases with the tilt angle as expected with a strong ion milling anisotropy component. A very different etch mechanism is operative in Fig.4.8 on θ_{s1}. The vertical sidewall angle $\theta_{s1} = 0^0$ at $\theta_t = 45^0$ is quite smooth

and results from a combination of both erosion and deposition mechanisms.

These complex erosion effects are the result of more than the two fundamental mechanisms operating independently: (1) milling by primary ions and (2) chemical etching by neutrals. The additional mechanisms to be considered are (3) formation of C-F polymer on the sidewalls[Ref.4-24,25], (4) sputtering of Si from one surface downstream to either θ_{s1} or θ_{s2} sidewalls, (5) downstream sputtering of atomic layers of the Al shadowmask onto an adjacent sidewall θ_{s1}, and (6) secondary ions reflected from one sidewall resulting in milling of an adjacent sidewall. Among these six(6) mechanisms, only the etching by neutrals (2) is isotropic. Each of the other mechanisms is anisotropic contributing sidewall striations and strong variations of sidewall θ_s with substrate tilt θ_t. Here both primary and secondary ion milling by reflected CF_3^+ ions in addition to smooth etching by fluoride neutrals may be dominant. We do not understand the detail etch/deposition mechanisms operative for $\theta_t \geq 15^0$ on sidewall θ_{s1}.

The etch rate for the P-type wafers is reduced compared to the N-type case primarily due to the difference in Coulombic forces between the reactant F (chemisorbed singly-ionized negative charge state) and the dopant impurities. The F^- ion at the surface is attracted into the positively charged donor bonds of N-type silicon and thus the etch reaction rate is enhanced. Similarly, the F^- ion at the surface is repulsed from the negatively charged acceptors in P-type silicon and the etch reaction rate is reduced[Ref.4-26].

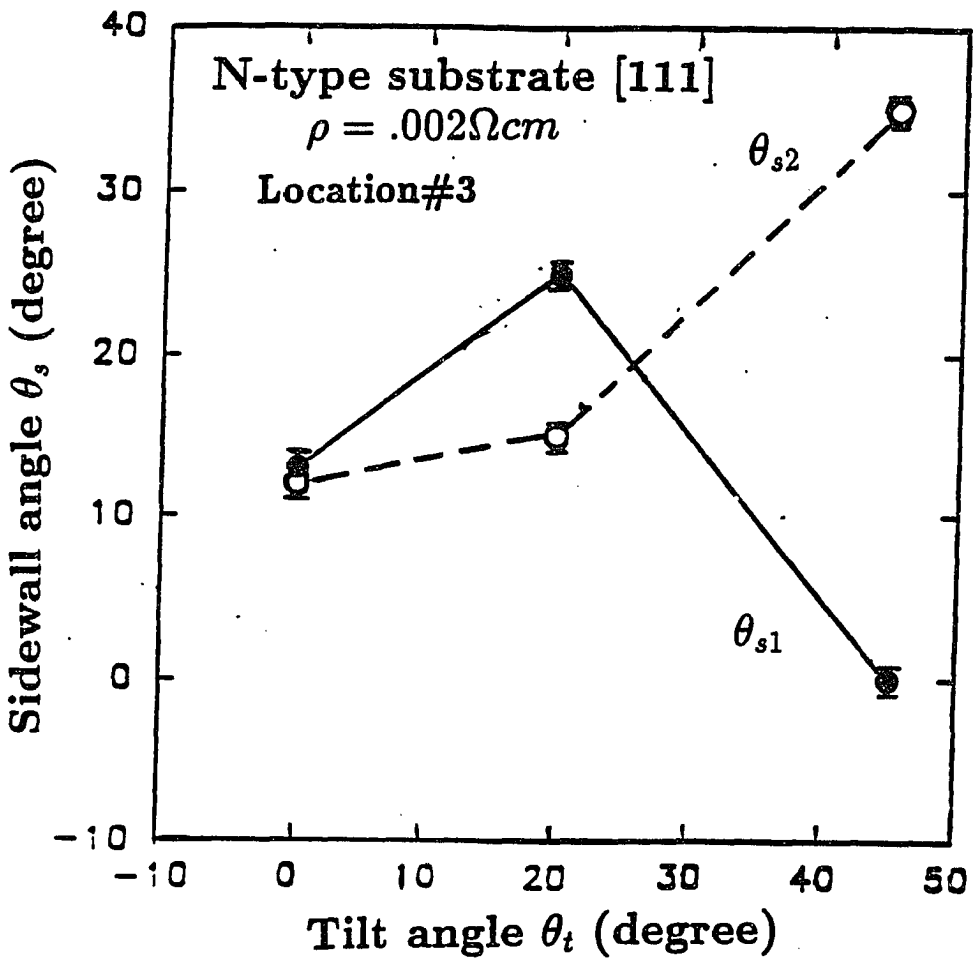


Figure.4.8 Sidewall angles θ_{s1} and θ_{s2} at location #3 for a N-type substrate as a function of tilt angle θ_t- N-type substrate (Data obtained from average of 3 sampled values from 3 wafers).

4.3.4 Trench etch rates with Al liftoff mask

The etch rates plotted in Fig.4.9 are obtained from the Alphastep-200 surface profilometer for SEM photos of trenches on wafers with the Al shadowmask. The untilted $\theta_t = 0^0$ wafer is etched at 1180 $\mathring{A}$/min with our process. Thus , the 30 min etch results in trenches of depth 3.5μ depth for the case $\theta_t = 0^0$ using the Alphastep-200 surface profilometer. In Fig.4.9, the dominance of the faster etch rate of the neutral radicals is seen at location #1. As the observed etch site moves away from location#1 the effect of ion sputtering increases and the erosion rate decreases at location #3. However, as one moves from the location#3 to location#5 in Fig.4.9 the complexity of the process is further indicated when the etch rate is seen to increase somewhat. Additional etch rate data which includes that of Fig.4.9 is shown in Fig. 4.10. The etch rate tilt angle dependency at location #1 in Fig.4.10 shows highly nonlinear characteristics. Additional studies will be required to understand this observation at location #1 in which etching is dominated by neutral species. The etch rate at location #3 and #5 is seen to be more constant with substrate tilt θ_t compared with that of location #1.

The observed dependencies cannot be fully explained as being entirely indicates due to the (1) physical erosion of the surface by the primary ion beam and (2) chemical etching by neutral radicals alone as independently acting mechanisms. The basic ion sputtering of the sidewalls is an electrodynamic process that can be described with a ballistic model [Ref.4-27]. The basic chemical etching with neutral fluoride radicals should proceed approximately independently of the ion sputtering process. However, both primary processes are clearly supplemented by the four secondary processes mentioned probably the buildup of monolayer polymers and redeposition of the substrate material on the sidewalls.

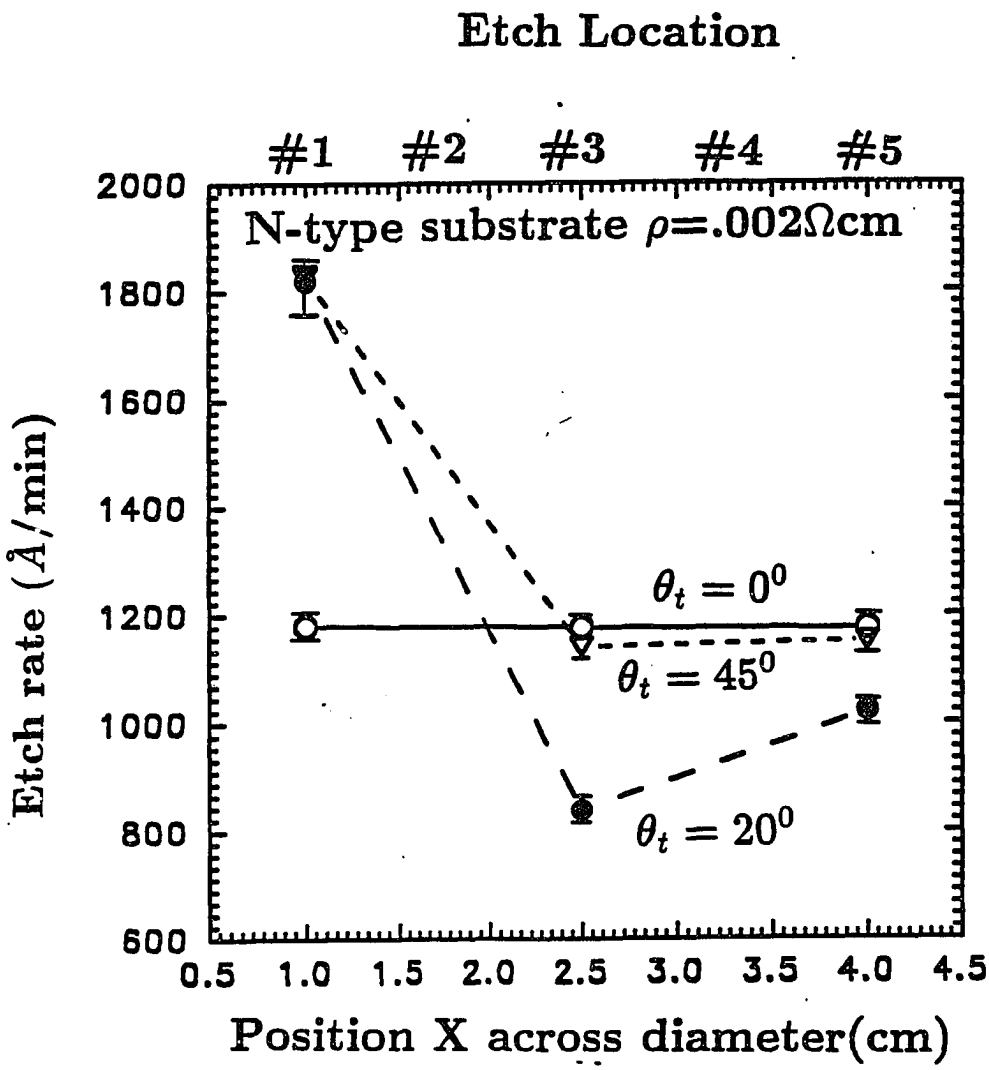


Figure.4.9 Silicon etch rate as a function of etch location using unannealed Al as a shadowmask. Tilt angle θ_t is the plot parameter: θ_t= 0, 20 and 45^0. N-type substrate. (Data obtained with the Alphastep-200: each data point is the average of three samples)

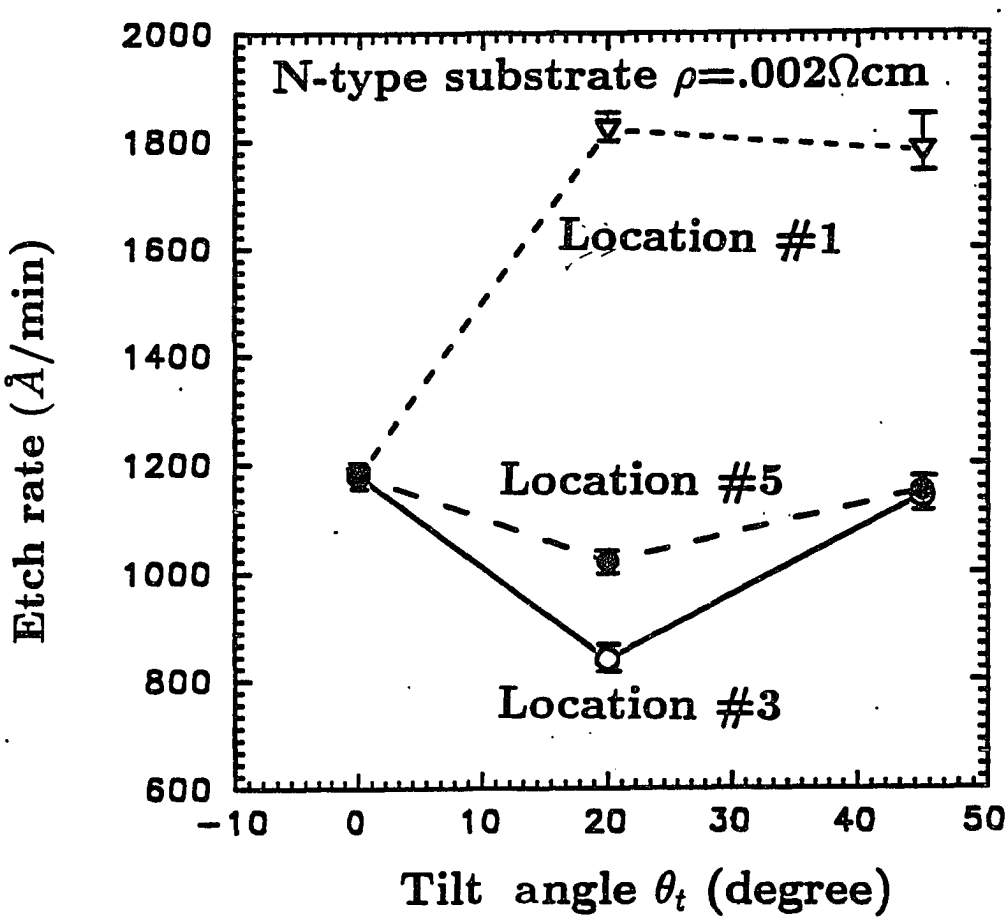


Figure.4.10 Silicon Etch rate as function of wafer tilt angle θ_t using unannealed Al as a shadowmask. for Al mask with etch location as a parameter. N-type substrate. (Data obtained with the Alphastep-200: each data point is the average of three samples)

4.4 Summary

The sidewall formation with RIE in the 30 to 80 mTorr pressure range using a fluorine-based chemistry CF_4/O_2 has been studied using tilted wafers. Sidewalls are obtained by shadowing the RIE process with photoresist and aluminum "top hats" separately. Our results are consistent with the ion milling process dominating in the region of maximum dark space thickness (nearest the cathode). The chemical etch rate process dominates in the region at a distance from the cathode surface where the ion energy of the wafer is reduced. The dynamics of the etching process is found to be complex and only is partially explained by assuming independent primary anisotropic ion milling and isotropic chemical etch process.

Relatively sharp single- and double-ridged silicon structures were obtained using the photoresist shadowmask on untilted substrates. No advantages for vacuum microelectronics applications were found using tilted substrates with the photoresist shadowmask.

The smooth and flat sidewall surfaces more desirable for optical grating and reflector applications were obtained with the photoresist shadowmask. Improved smoothness of sidewall θ_{s1} was observed with the photoresist compared to an aluminum shadowmask. This is consistent with polymer formation associated with the photoresist forming on sidewall θ_{s1} to create a smooth surface. The gradual erosion of the photoresist shadowmask apparently contributes to a sidewall smoothness.

The minimum sidewall angles θ_s were obtained using unannealed aluminum as an RIE shadowmask preceded by a liftoff lithography process. This process shows promise for the fabrication of field emitter cone or ridge cathodes on high pedestals. The higher pedestal and near-vertical sidewall results in a higher electric field at the cathode surface useful for vacuum microelectronic applications.

Chapter 5

Model of lateral vacuum microelectronic devices with a cusp cathode

Several types of vertical microelectronic devices have been made by micromachining techniques such as wet chemical anisotropic etching, reactive ion etching and e-beam depositions[Ref.5-1,2,3,4,5,6,7]. The 3 dimensional vertical devices are not suitable for large scale integration because of difficulties in processing, but lateral vacuum device geometries are of special interest because the potential exists for processing technology compatible with VLSI production. In this chapter, a new geometry of a lateral diode with control grids is modeled, fabricated by a unique technology, and characterized.. A reverse image liftoff lithography is introduced to obtain sharpened tips in the form of a lateral cusp cathode. Tungsten metal is deposited by dc magnetron sputtering, to form the cusp cathode. The role of the deflecting grids, to effectively control the electron trajectories, is simulated and experimentally demonstrated in this chapter. Device testing is performed in a 1×10^{-7} Torr vacuum resulting in an emission current of 1.3μA from a 23 μm long wedge cusp cathode.

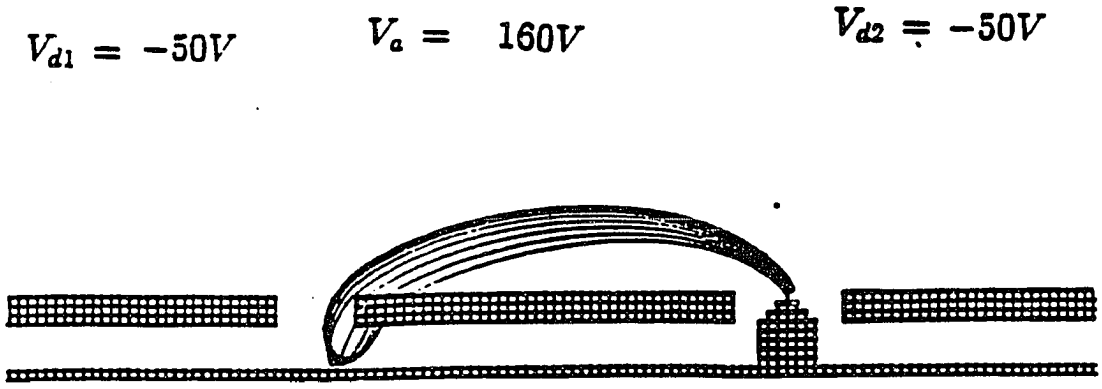
5.1 Device Modeling

The first set of models for the lateral diode and triode was developed by Carr et al [Ref.5-8]. They have demonstrated the necessity for using deflecting grids to control the electron trajectories in lateral devices. The device simulation was based on electron trajectories within an electric field region calculated by the Laplace equation. In their work, only the electrostatic field effects were considered.

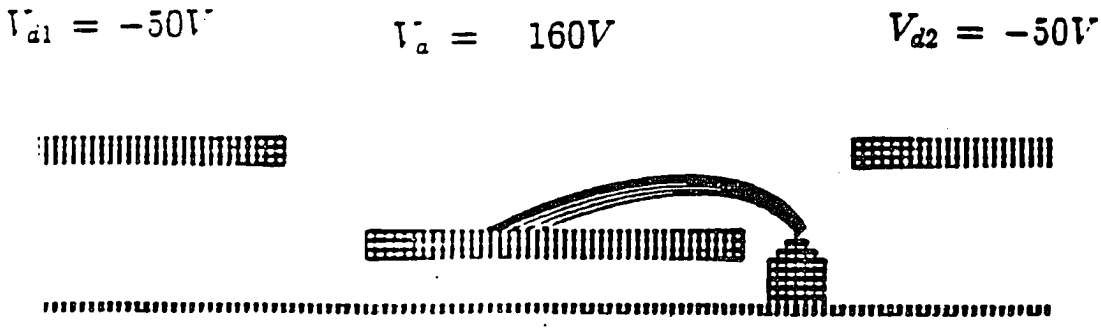
The characteristics of the lateral devices and the transit time of electrons as defined by the time of flight of electrons from the cathode to the anode were shown by SIMION which is simulation program for vacuum microelectronics. For example, the minimum transit time in GaAs device is 2 psec for a 0.5μm channel length[Ref.5-9]. Transit times vary from 2.3 psec to 3.5 psec in a lateral vacuum microelectronic diode structures without deflecting grids, whereas typical vertical tip devices have the transit times of about 0.38 psec[Ref.5-9]. However, when the deflecting grids voltage and the cathode geometry are optimized, the transit time in a lateral diode is reduced to the level of vertical devices. By varying the bias voltages and geometries, optimized lateral structures were designed by SIMION. A cone shape tip is typically used for high emission current [Ref. 5-10], however, since the wedge cathode is more uniform and stable than the cone cathode, various wedge cathodes were modeled in this chapter. In light of the SIMION simulations, it was concluded that deflecting electrodes were required in order to get high emission current from the lateral "wedge cathode" [Fig.5.1, (a),(b)]. The optimum geometry was found to be with the deflecting electrodes located 1.5 μm higher than the cathode and anode reference plane.

Fig. 5.1, 5.2, and Fig. 5.3 show the electron trajectories of various lateral cathode geometries. Deflector grid bias($V_{d1,d2}$) was -50 volts, and anode voltage(V_a) was set at 160 volts with a grounded cathode, and with an anode-

cathode spacing of 1 μm. In Fig. 5.2, a "knife-edge emitter" is simulated, and demonstrates that there is no difference in electron trajectories with or without the deflector. However, in Fig.5.1, the "wedge emitter" and in Fig.5.3, the " cusp cathode", the role of the deflecting grid is critical in controlling the electron trajectory. In order to examine the differences between the knife-edge emitter and the cusp emitter, devices without deflecting grid were also studied.

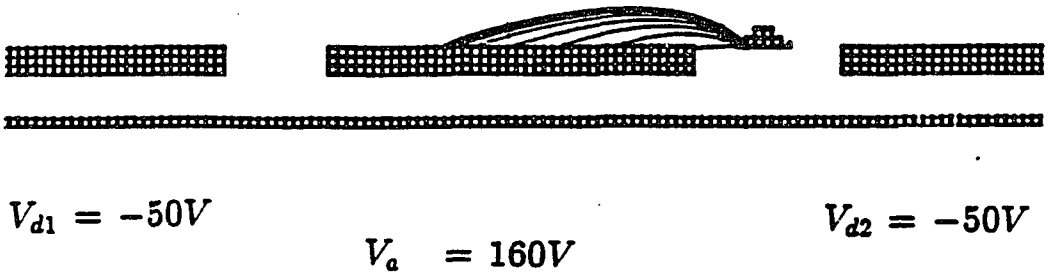


(a)

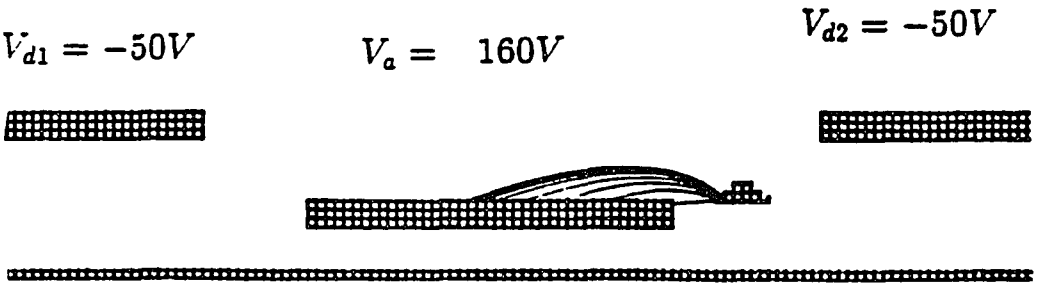


(b)

Figure 5.1: Wedge cathode for (a) planar and (b) recessed structures with deflector bias($V_{d1,2}$) and anode bias(V_a)

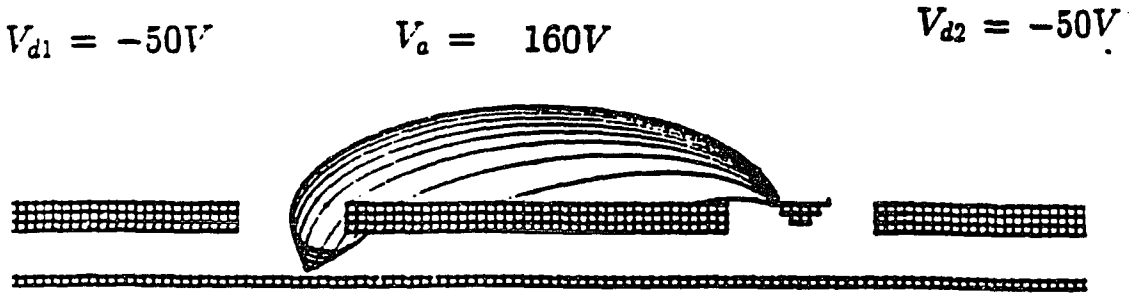


(a)

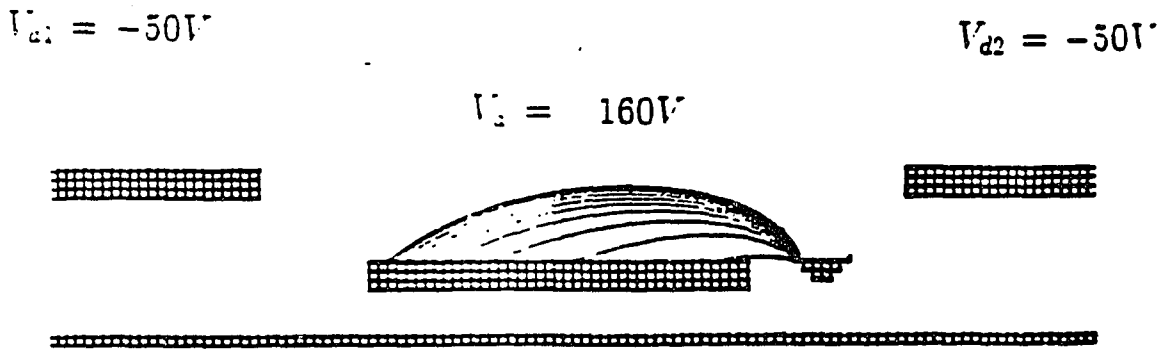


(b)

Figure 5.2: Knife-edge emitter for (a) planar and (b) recessed structures with deflector bias($V_{d1,2}$) and anode bias(V_a)



(a)



(b)

Figure 5.3: Cusp cathode for (a) planar and (b) recessed structures with deflector bias($V_{d1,2}$) and anode bias(V_a)

Fig. 5.4(a) shows the electron trajectories for the knife-edge field emitter structure with 160 volts on the anode and 0 volts on the cathode. The geometry demonstrated nearly ideal electron transfer between cathode and anode. As a result, the deflecting grids were not required for the knife-edge emitter devices. In contrast, Fig. 5.4(b) shows that with the cusp cathode emitter the electron transfer efficiency is low, requiring the deflecting grids to provide nearly ideal electron transfer.

The explanations for the difference in behaviour between the two geometries discussed are presented in Fig.5.5. This figure shows the potential distributions in the devices. The equi-potential lines are similar, but there is an important difference at the emitter tip between Fig.5.5(a) and Fig.5.5(b). The potential distributions at the knife-edge emitter tip in Fig.5.5(a) are slightly steeper towards the downside from point A. As a result, the maximum change of potential gradient, or the direction of the maximum electric field vector for the knife-edge emitter forms below the top horizontal surface of the anode (level #1 in Fig.5.5(a).) For the cusp cathode, the potential distributions at the tip have a steep gradient towards the upside from point B in Fig.5.5(b), therefore the electrons are more easily directed upward as shown in Fig.5.4(b). The maximum electric field vector is assumed to be above the top horizontal surface of anode (level #1 in Fig.5.5(b)). Since the electrons travel along the direction of the maximum electric field, their trajectories are explained on the basis of the electric field. The slight variations on the potential distribution at emitter tips have a pronounced effect on the electron trajectories as in Fig.5.4. and 5.5. After many simulations, the optimized geometry of the cusp cathode was designed in this chapter.

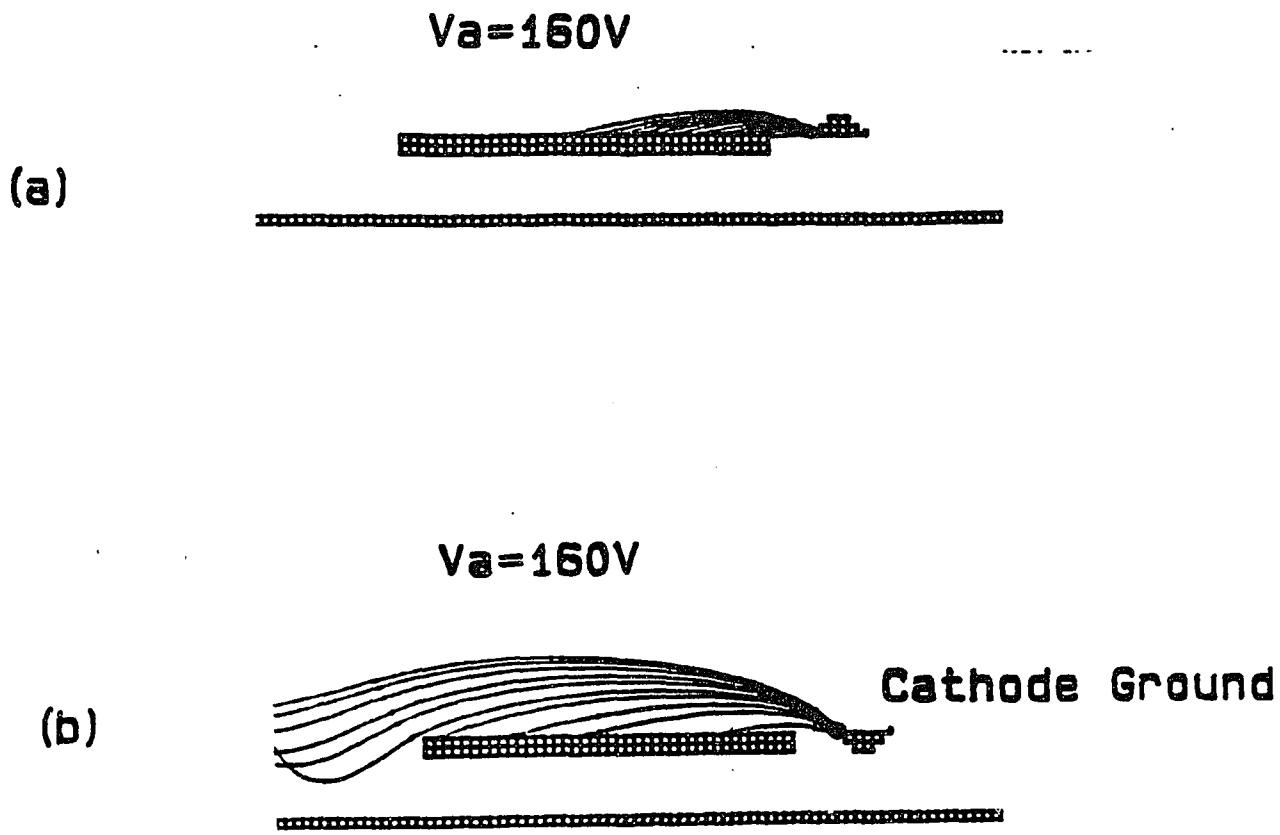
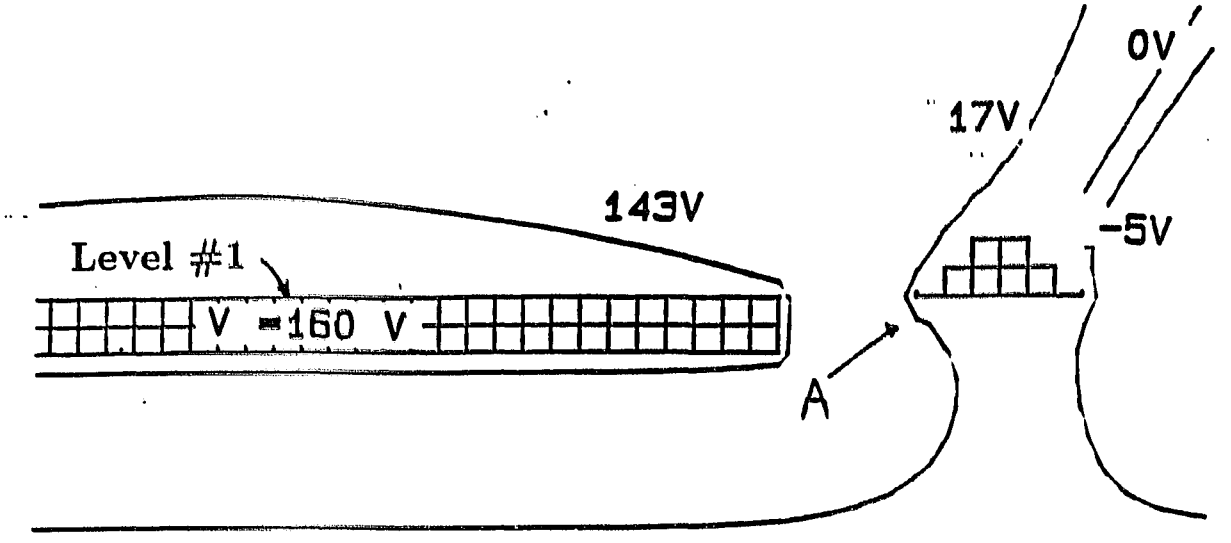
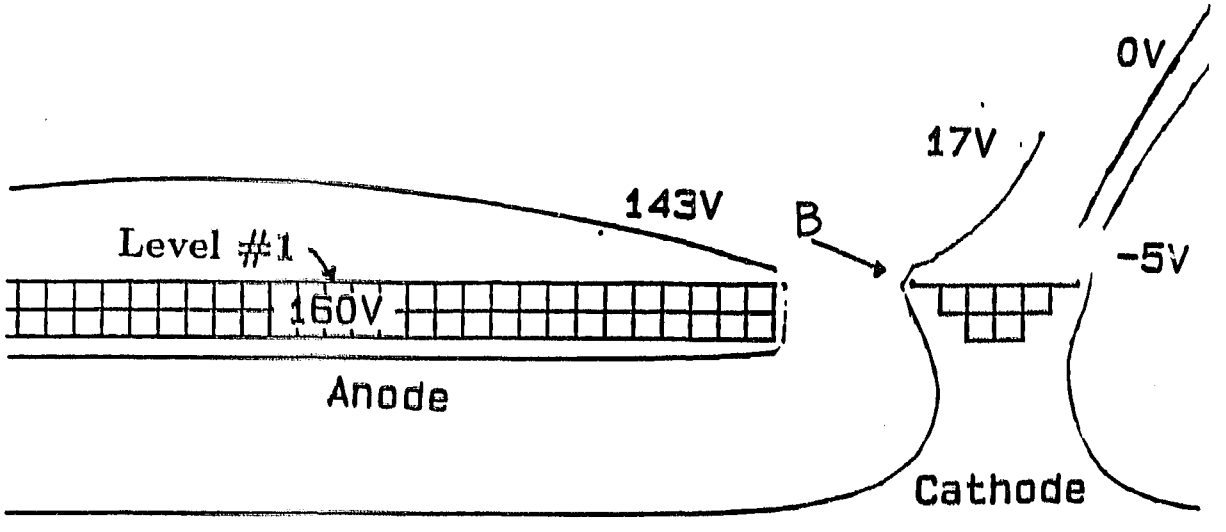


Figure 5.4: Electron trajectories without deflecting grid for (a) knife-edge cathode (b) cusp cathode



(a)



(b)

Figure 5.5: Potential distributions without deflecting grid for (a) knife-edge cathode (b) cusp cathode

5.2 Experimental procedures for the recessed lateral diode of cusp cathode with two deflecting grids

5.2.1 Selection of materials and technology

One of the most important factors is the selection of the cathode material. Referring back to Chapter 2, refractory metals are preferred, since they have good thermal stability and conductivity. Tungsten is used both for the cusp cathode and the anode in this experiment, since it has superior thermal stability compared with any other refractory metals.

As the lower work function is preferred for field emission, the work function of cathode material is another important factor, The work function of tungsten is suitable for field emission, even though it varies as crystallographic facets and deposition process parameters change[Ref.5-7,11,14]. The typical work function of tungsten varies from 4.3 eV to 5.7 eV.

Another important factor is a fabrication technology of tungsten cathode. Tungsten has been deposited by e-beam evaporation, rf sputtering, and dc magnetron sputtering [Ref.5-12]. However, due to the high melting point, the deposition of an acceptable film is difficult.

In order to fabricate the cusp cathode, several process technologies such as anisotropic chemical etching, dry etching, or liftoff process were considered. In our experiment, liftoff process by dc magnetron sputtering is the best suitable technique, as this technique provides low temperature processing and intrinsically induces the metal cusp structures on the photoresist step [Ref.5-12,13] The liftoff process is explained as follows: the photoresist is patterned by lithography, and the metal film is deposited simultaneously on the photoresist and on the exposed substrate. Then the metal on the photoresist is lifted off by organic solutions

such as acetone or photoresist stripper.

However, since the liftoff process needs the metallization on the photoresist, the metal deposition technique has to be low temperature processing as to avoid any damage to photoresist pattern due to the flows of photoresist at high temperatures. Even though dc magnetron sputtering is low temperature processing, crosslinking of photoresist also could be induced by the ion bombardment during sputtering deposition. In order to minimize these effects, the substrate should be exposed to multiple plasma scannings, or photoresist should be deep UV hardened.

In order to control more sharpened cusp formation on the photoresist step, a reverse image liftoff process was used in our experiment rather than the normal image liftoff process, because it provides the wide control of sidewall of photoresist step [Fig.5.6]. Also, the reverse image liftoff process provides a better control for fineline patterning than the normal liftoff process. In our devices, the reverse image liftoff is more suitable, because the cathode width is less than $1\mu m$. No micromachining such as wet chemical etching or reactive ion etching is required in this process.

The details of the reverse image liftoff process for cathode fabrication are presented in Fig.5.6. For AZ5214E reverse image processing , 10 % HMDS (Hexamethyldisilazane) is spincoated at 6000rpm for 30 seconds and AZ 5214E is spincoated at 5000 rpm for 45 seconds followed by a soft bake at 110^0C for 1 minute. Then the mask image is exposed at 5.5 mwatt/cm^2 light intensity for 8 sec in a contact aligner [step.1 in Fig.5.6]. The next step is a hard bake (or called as " post exposure bake") at 125^0C for 45 seconds to crosslink the photoresist surface in the exposed area to make it insoluble to developer. [step.2 in Fig.5.6]. Then the flood exposure without any mask plate is conducted for 15 seconds.

[step.3 in Fig.5.6]. The final step is to develop the photoresist with Shipley MIF 312 developer:H_2O=1:1 solution for 1 minute [step.4. in Fig.5.6].

To protect the photoresist from crosslinking or flowing during dc magnetron sputtering, AZ5214E photoresist should be exposed to deep UV light source(290nm wavelength) after developing. The initial substrate temperature is 105^0C which ramps up to 180^0C in 6 minutes during deep UV hardening. If the substrate temperature goes higher than 200^0C, the photoresist flows and the device pattern may be damaged. Inspection should be carefully done to check for any photoresist flow.

A 500 $\AA$ titanium layer is deposited by dc magnetron sputtering to promote strong adhesion between the oxide and tungsten layers. Tungsten is then deposited by dc magnetron sputtering to form the cusp cathode. During tungsten deposition, multiple plasma scanning should be to reduce the high temperature effects.

Care should be taken during metal deposition that the metal is not deposited continuously over the photoresist step. Adequate liftoff for the metal/ photoresist step should be available in order to form cusp cathode [Fig.5.6].

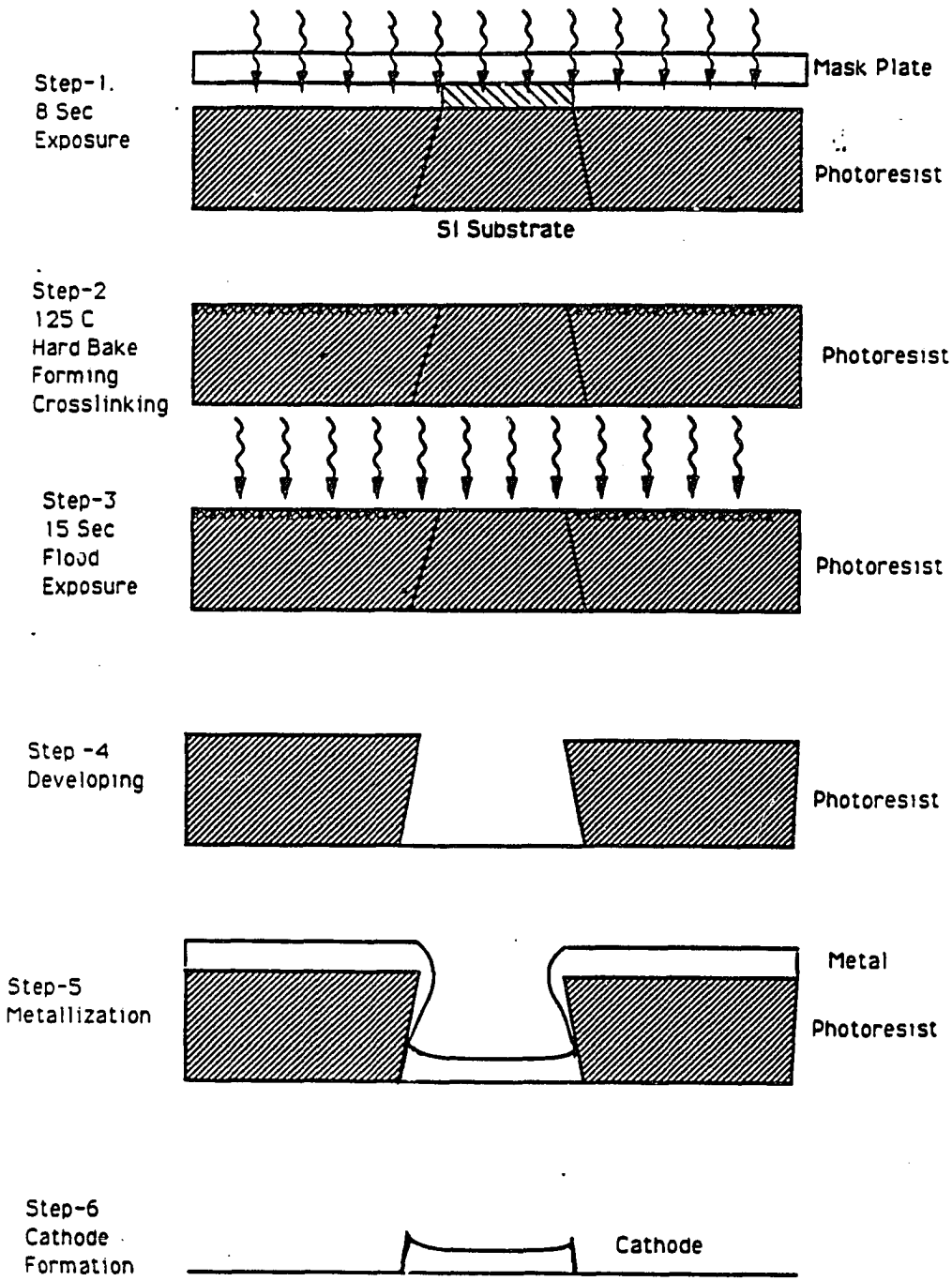


Figure 5.6: AZ 5214E reverse image process for cusp edge cathode

5.2.2 Device fabrication and discussion

Fig 5.7 shows the layout and photograph of masks made by the Cambridge 10.5B EBMF e-beam lithography. Fig.5.7(a) shows the layout of lateral devices. The device layout has 23 μm long cathode. The anode-cathode spacing varies 0.8μm to 1.2μm, when the deviations due to photolithography are considered. The anode size is $8\mu m \times 23\mu m$. The die size is 182 $\times$ 140 mils^2. The size of bond pad is 100$\times$ 100 μm^2. The each mask level is made by a positive PMMA resist plate.

Mask level#1 is for the recessed oxide well formation of the anode and cathode. The silicon wafer is thermally oxidized after a standard cleaning. A 2.5 μm thick oxide layer is grown by a 10 hour steam oxidation at 1150^0C. The mask for the recessed oxide well is patterned with a reverse image Al liftoff process. A 180nm thick aluminum is deposited by e-beam evaporation. Al is used as etch mask for oxide well formation by reactive ion etcher. The oxide well of 1.5 micron in depth is formed by reactive ion etching at 250 watts of power and 20 mTorr of operating pressure for 18 minutes in a CF_4/O_2 ambient. The aluminum layer is a suitable mask for these etchants. The etch rate of aluminum was 30-50$\AA$/min and the oxide etch rate was 800$\AA$/min. This oxide well will contain the cathode and anode as in Fig.5.3(b).

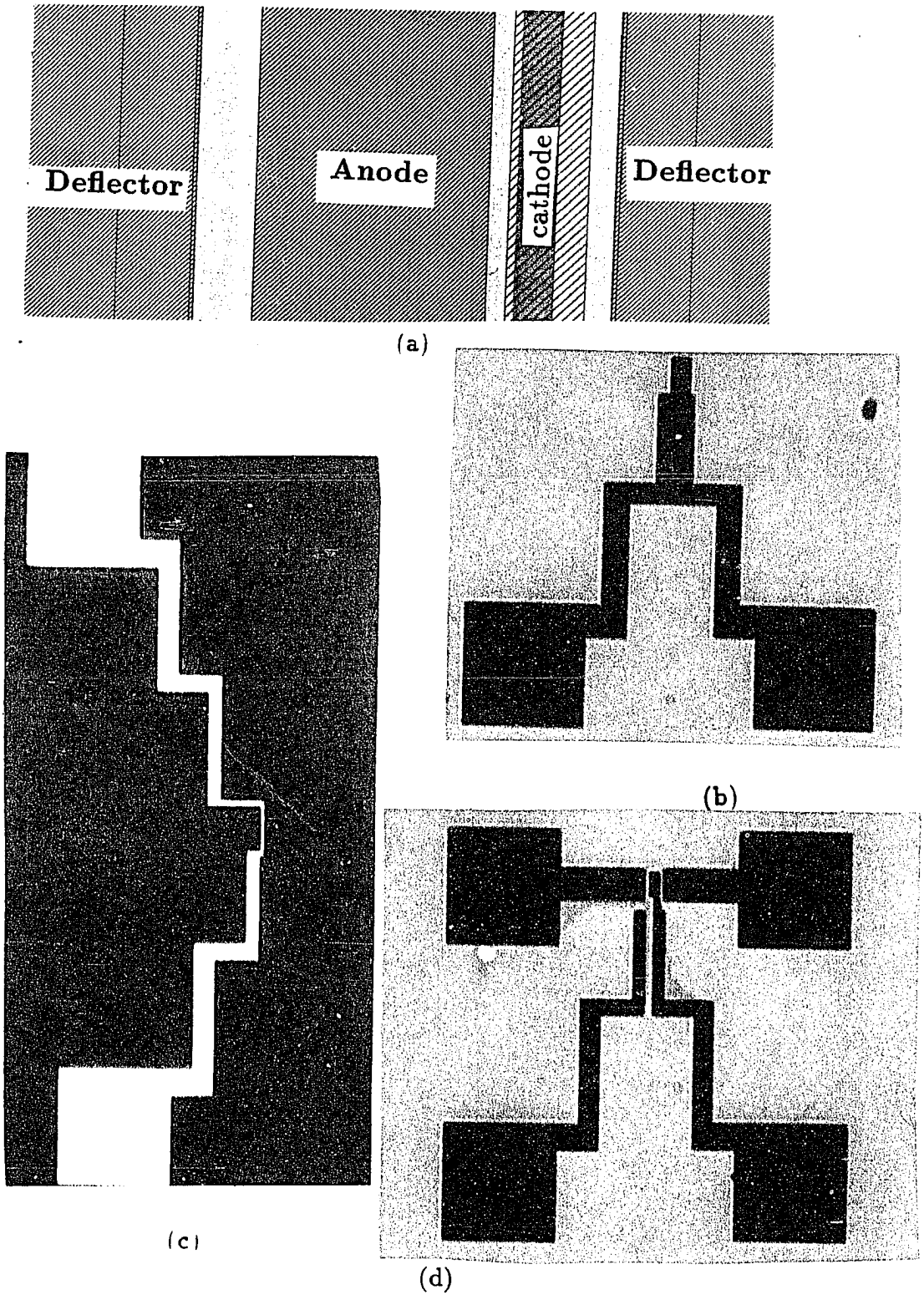
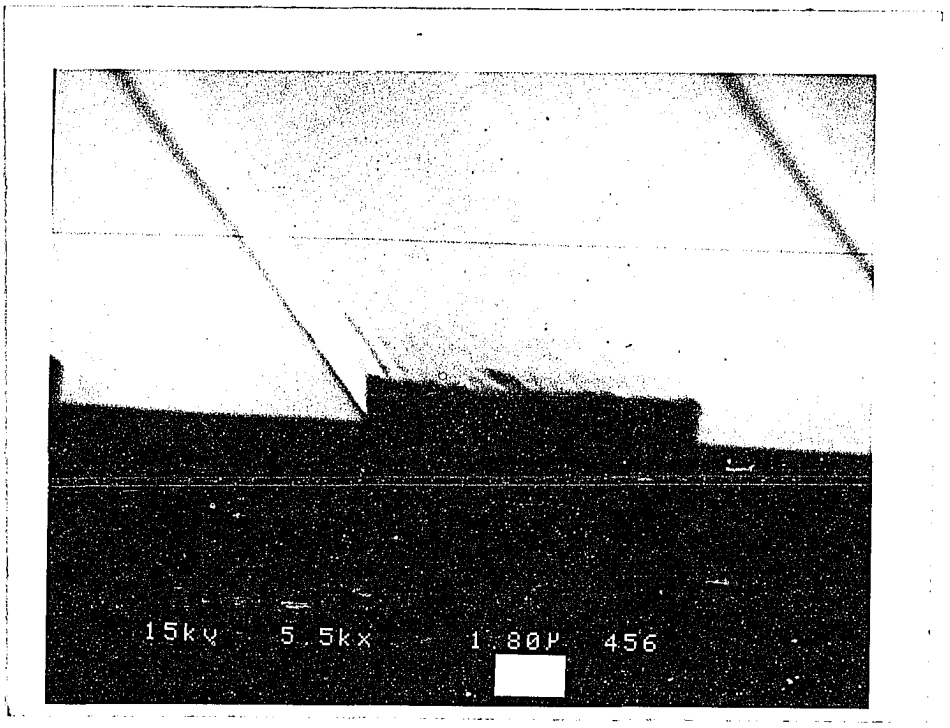


Figure 5.7: (a) Layout of the recessed lateral diode, (b) mask#1 (recessed oxide well), (c) mask#2 (cusp cathode), (d) mask#3 (anode and deflector electrodes)

Mask level #2 is used to form the cusp cathode. This is the most important step. For the cusp cathode, the previously mentioned reverse image liftoff process was used. A SEM view of sidewall angle of AZ5214E photoresist after reverse image processing and the resulting tungsten cusp cathode are shown in Fig.5.8(a) and (b). Tungsten is deposited by dc magnetron sputtering. It is assumed that the cusp cathode is formed due to the random directionality of the dc magnetron sputtering. The optimized thickness of the tungsten films for cusp formation was about 4000Å. If a magnetron sputtered tungsten film over 6500Å is deposited, it will be continuous over the photoresist step, liftoff will be difficult.

(a)



(b)

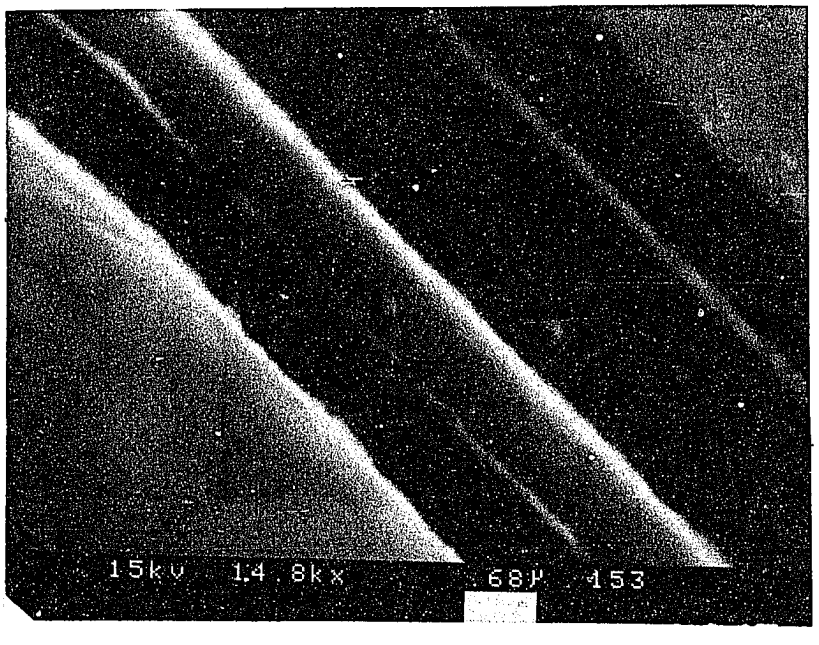


Figure 5.8: Sidewall of (a) AZ 5214E photoresist after reverse image process (b) SEM view of the cusp cathode after liftoff

The tungsten is lifted off by immersing the substrate into hot ST-20 photoresist stripper at 80^0C with ultrasonic agitation for at least 1 hour and rinsing in a water jet stream. If this treatment is insufficient to lift off the tungsten layer, then a plasma descum should be conducted for 30 minutes with oxygen at a pressure of 1 Torr and rf power of 450 watts. The oxygen plasma easily penetrates the photoresist layer through the cracks in the metal layer at the photoresist step. Ultrasonic agitation with photoresist stripper should be repeated.

Mask level #3 is used for patterning anode and deflector electrodes with AZ1518 positive photoresist. AZ1518 photoresist has the same coating conditions as AZ5214E photoresist. AZ5214E is normally used for fineline patterning and needs complicated processing. Therefore, using AZ1518 photoresist, a normal liftoff process is used for this mask level , due to the larger feature size of the anode and deflector electrodes. The sidewall control of AZ1518 is not as sensitive as AZ5214E, but deep UV hardening and multiple plasma scanning for the AZ1518 photoresist are also required. The metallization steps for anode and deflecting grids are the same as mask level#2. The deflecting grids are located outside of the oxide well, and the anode and cathode are positioned inside the oxide well as in Fig.5.3.

Finally, the device is mounted into a 40 pin IC packaging, and bonded using ultrasonic wire bonding [Fig.5.9]

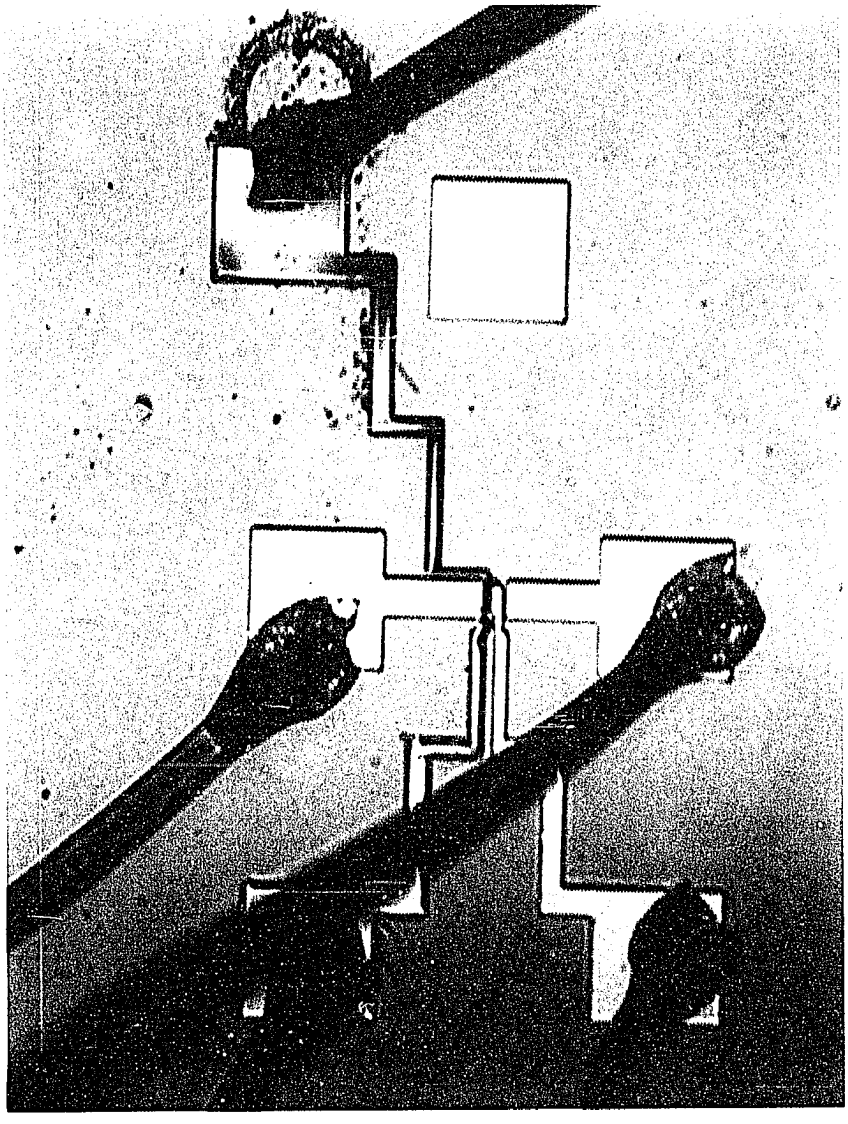


Figure 5.9: Packaged single device

The vacuum chamber for the device test is installed with turbo pump and a 2 stage rotary vane mechanical pump. Test system was equipped with Leybold Inficon quadrupole mass spectroscopy to analyze the chambers condition. Chamber size is 2.75 inches in diameter and has 10 pin electrical feedthrough to supply power to the device. Chamber is normally baked at 150^0C for 72 hours. The final base pressure is $1x10^{-7}$ Torr.

5.3 Results and discussion for the electrical measurements

The I-V characteristics are shown in Fig.5.10 and Fig.5.11. Fig.5.10 shows the anode current versus the deflecting grid voltage, as a function of the anode voltage. Fig.5.11 shows the anode current versus the anode voltage as a function of the deflecting grid voltage.

In terms of these data, the emission current is not affected by ground or positive bias of the deflecting grids. But it is greatly affected by the deflector voltage which are more negatively biased. This means that when the deflecting grids are grounded or biased positively, they lose control of electron trajectories. It matches with the simulation by Carr et al [Ref.5-8], as the bias voltage of the deflector goes more negative, the emission current is greatly increased. In Fig. 5-10, the emission current also increases as the anode bias voltage increases. The 1.3 μA of emission current from 23 μm long cusp cathode is observed at 225 volts of anode bias and -70 volts of deflector bias. The higher bias of the anode induces a higher current from the cathode tips, because a high bias forms directly the higher field intensity at cathode edges. Therefore , above 100 volts of anode bias , most of the emitted electrons are collected at anode with a more negatively biased deflector. This result is similar to that of the simulation in Fig.5.3.

In Fig.5.11, the emission current at a negatively biased anode is almost at the noise level. However, with high positively biased anode at anode, the emission current greatly increases with more negatively biased deflector. The emission current at low bias of the anode (less than 75V) is relatively low and uniform.

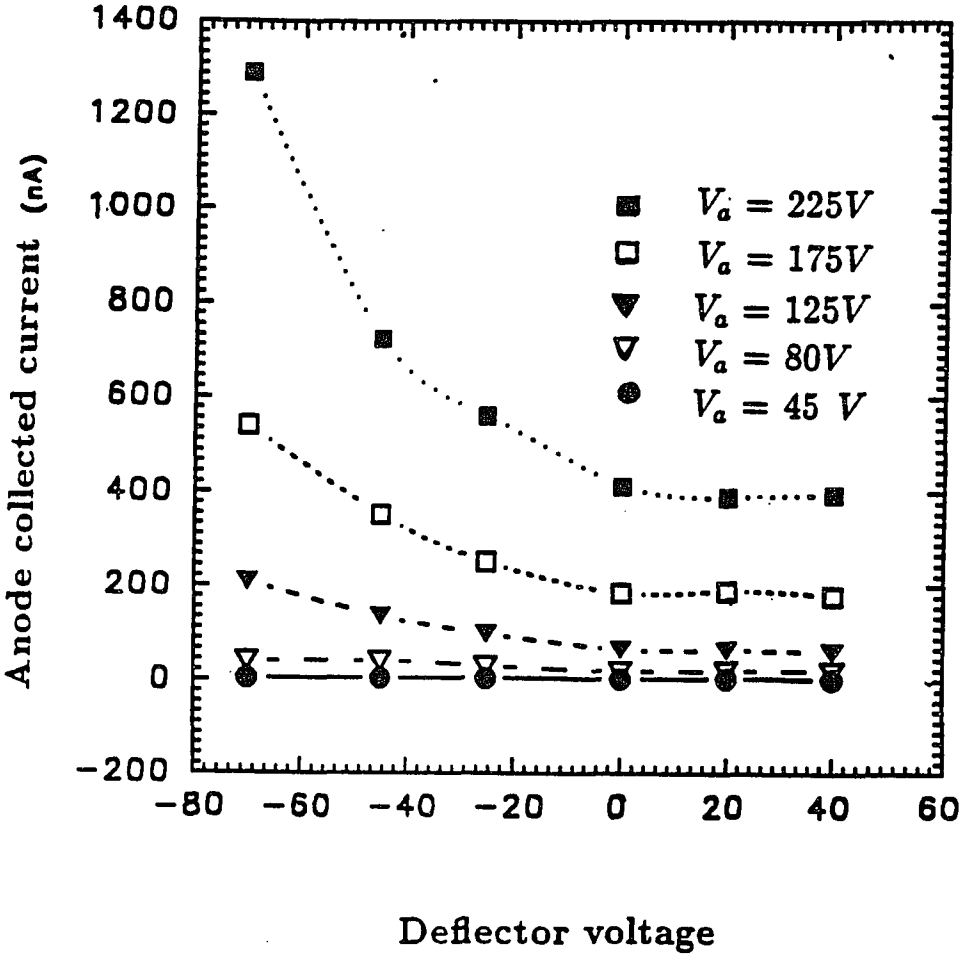


Figure 5.10: The I-V characteristics of the anode current vs. deflector voltage as a function of the anode voltage

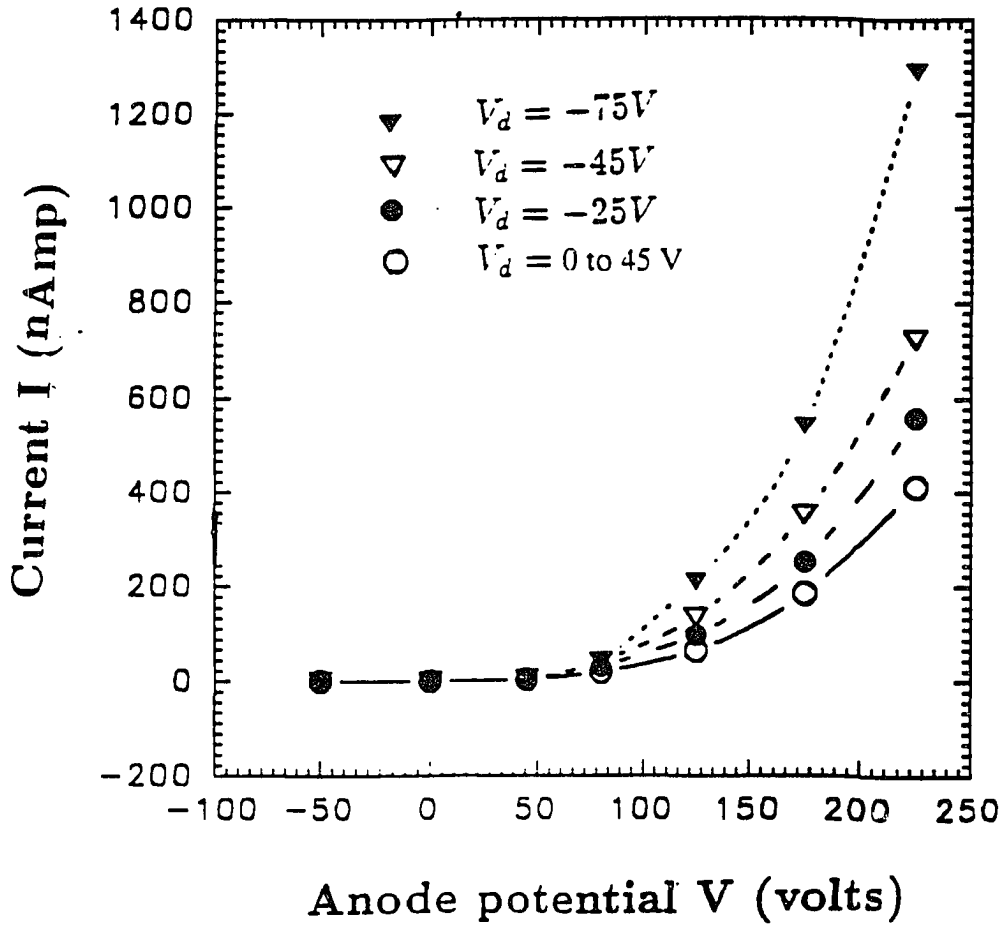


Figure 5.11: The I-V characteristics of the anode current vs. anode voltage as a function of deflector voltage

From Fig. 5.10 and 5.11, the Fowler-Nordheim plot shown in Fig.5.12 is obtained. In terms of the Fowler-Nordheim eq., (i/v^2) versus 1000/v (v=anode voltage) gives the straight line whose slope determines the work function of the tungsten cathode material. Fig.5.12 shows the uniform FN distributions at four different bias voltages of the deflecting grids. In Fig.5.12, at a high anode voltage bias above 100 volts, our results show the regular FN distributions. However below 100 volts anode voltage, it forms a transition region and shows the characteristics of leakage current. The FN distribution does not show as steep a slope as it does at the high bias region, but with -70 volts of deflector bias the FN plot shows almost an ideal slope. As a result, the perfect FN plot results with a high positively biased anode and a high negative deflector bias. Fig.5.12 shows the FN distribution depends on the variations of the anode and deflector voltage.

At low bias voltage ranges of anode, the several researchers showed the non uniform Fowler-Nordheim distributions [Ref.5-15,16,17]

Similar data were shown by Howell et al and Zimmerman et al.[Ref.5-16,17]. Howell et al concluded that the different slope of FN plots at a low anode bias (below 100 volts) can be attributed to the presence of a thin oxide barrier and the small radius of the curvature at the emission sites. Zimmerman et al also showed the similar plots. Recently, Harvey et al tested silicon emitter array in the vertical geometry[Ref.5-15]. Their Fowler-Nordheim plots consist of two distinct regions with different slopes. They proposed that the different slopes can be explained by a random distribution of tip radii, a surface reconstruction by a cathode melting, and oxide barrier. In our experiments, however, device geometry can be added to the above explanations. Since the electron trajectories in the vertical structures are normal to the anode surface, the electron trajectories can not be modulated too much. However, in the case of the lateral structures,

the electron trajectories can be deflected by deflecting grid towards the anode surface. Therefore, the geometries of the lateral device may be an additional factor to change the F/N plot at low bias.

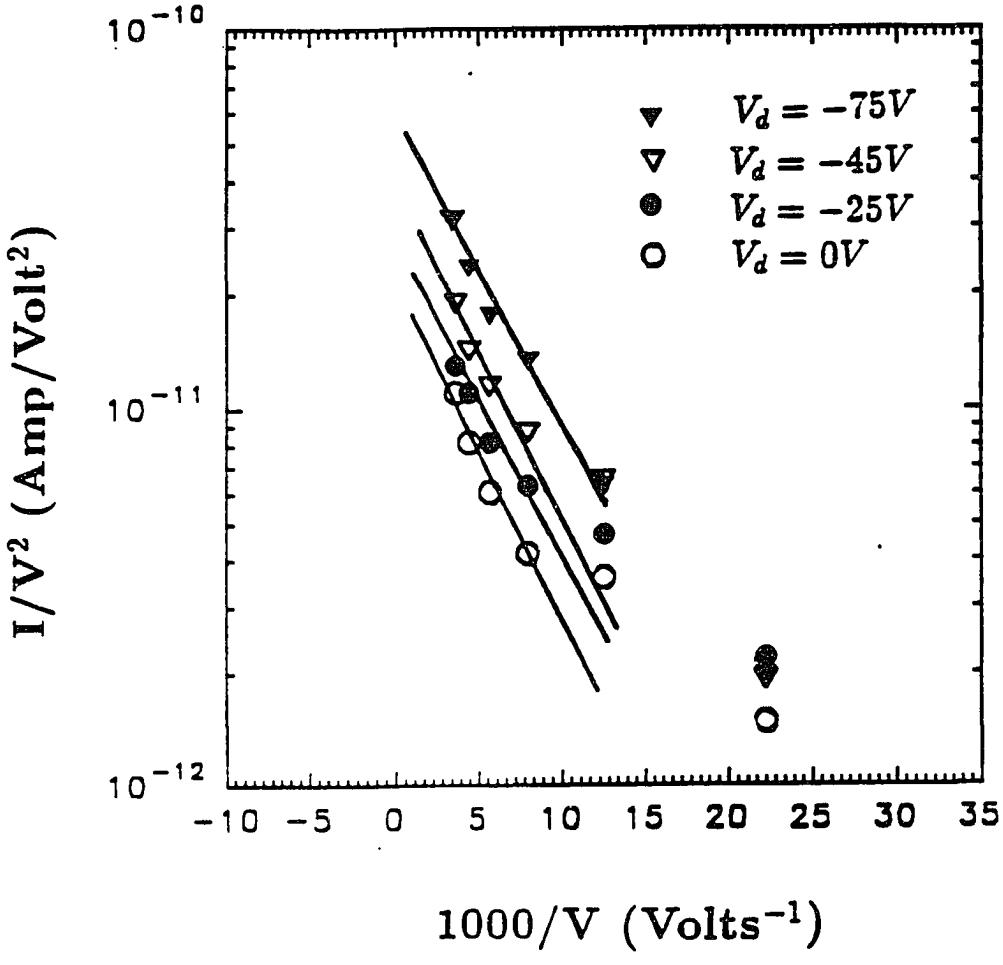


Figure 5.12: Fowler-Nordheim plot for cusp cathode device

5.4 Summary

The vacuum lateral device with cusp edge cathode was developed and analyzed by new and unique technology. First, the new process technology in the form of liftoff process of the tungsten dc magnetron sputtered deposition has been introduced for fabricating the lateral device without using wet or dry micromachining steps. It demonstrated the possibility of fabricating the intrinsically sharpened cusp edge cathode by this liftoff process.

Secondly, the role of the deflector is critically important in controlling the electron trajectory in a cusp cathode structure. Simulator and experimental results both showed that the cusp edge cathode definitely needs the deflecting grids to control the electron trajectory.

Chapter 6

Field emission diode with a tungsten wedge cathode and lateral electron trajectory

Process technology and characterization for a vacuum microelectronic diode device with a lateral electron trajectory are described. The cathode structure consists of a titanium:tungsten /tungsten film sandwich overlaying an aluminum adhesion film. The aluminum film is partially sacrificed to achieve the necessary sharp knife-edge of tungsten for field emission. A Ti:W layer is used for stress relief and passivation during wet chemical etching. The anode electrode of Ti:W/Al/Ti:W is deposited by dc magnetron sputtering. Both the cathode and the anode are processed using liftoff lithography which has shown a very high yield for the submicron alignment. A 0.8 μm lithography-controlled cathode-anode separation is characteristic of the process. Auger and SIMS analysis confirm the structure of the films. Devices electrically characterized at 2 to 5 $\times 10^{-9}$ Torr vacuum show a fit to the Fowler- Nordheim model. A maximum emission current of 26μA over its 23 μm length is obtained. Static electrical characteristics predicted by the Fowler-Nordheim relationship are compared with experimental data. The fraction γ of the high field cathode emitting is found to be in the range 0.03 to 0.8 with $3.3eV \leq \phi \leq 5.3eV$ based on proposed model.

6.1 Previous publications

Vacuum devices fabricated with technology compatible with standard semiconductor processing is of increasing interest for microengineering applications. A field emission source which is reliable and efficient continues to be a major goal. This chapter describes technology for a knife-edge tungsten cathode that shows some promise for practical applications. We describe a cathode characterized electrically using a diode geometry. The knife-edge of tungsten for the cathode emission surface is contained within an Al-W-Ti:W sandwich as shown in Fig.6-1. A dc magnetron sputtering process has been selected for the cathode structure and a combination of e-beam evaporation and dc magnetron sputtering has been selected for the anode. Liftoff lithography provides the desired 0.8 μm cathode-to-anode lateral separation. A short sacrificial etching of the aluminum and Ti:W films exposes the tungsten knife edge from within the laminate and is necessary for the field emission surface. Two lithographically-defined tungsten cathodes have been reported with a similar device. Kanemaru and Itoh[Ref.6-1] describe a tungsten cathode with an emission edge normal to the plane of the silicon substrate. The authors reported preliminary results[Ref.6-2] leading to the present chapter for a tungsten cathode with an emission knife-edge in the plane of the silicon substrate. Both technologies result in an electron beam path that is generally in the plane of the substrate(we use the term "lateral"). Several other field emission devices defined with fineline lithography and based on silicon, molybdenum, or Ti:W emission surfaces have also been reported[Ref.6-3,4,5,6,7,8]

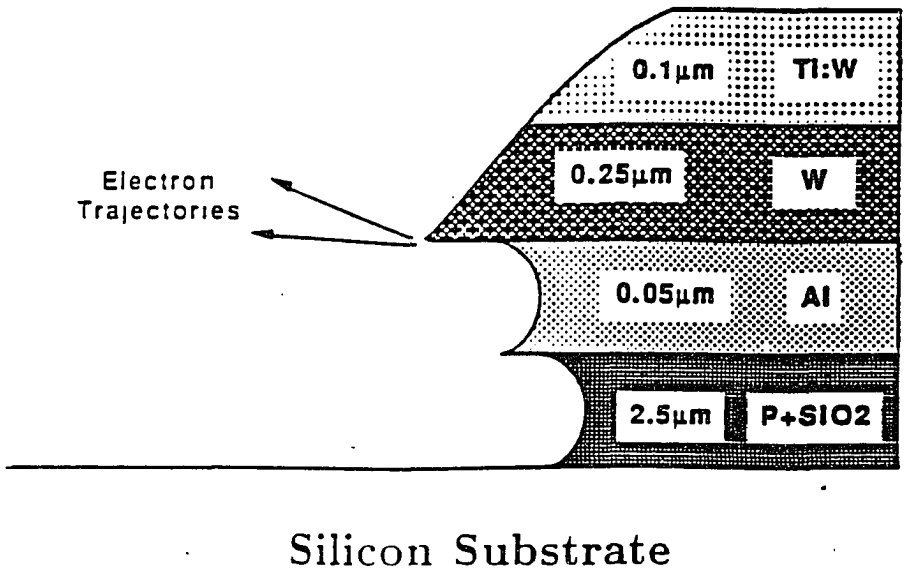


Figure 6.1: Field emission cathode cross section

6.2 Electrostatic design

The cross section of the cathode-anode high field region formatted for Laplace simulation is shown in Fig.6.3. A 2-D simulation solution using SIMION (finite difference equations) is used to calculate the electric field E_{max} at the cathode tip. The silicon substrate (ground plane) is maintained at the same potential as the cathode V=0. The equipotential ground plane is found to reduce the field E_{max} by less than 5% except for the case $h \leq 0.2p$. The simulator mesh size m for the initial pass [Fig.6.3] is 10nm per square. The mesh size m for the region at the cathode emission tip is decreased with successive "zooms" to final m values ($m \sim r_0/10$) adequate for calculating E_{max} at the cathode apex tips.

The accuracy of our simulator has been checked for this geometry by calculating E_{max} as a function of anode thickness p for a theoretical cylindrical cathode positioned at midheight $h = p/2$ (See Fig.6.3). A closed analytical solution for E_{max} exists for the limit $p \gg d$,

$$E_{max} = \frac{V}{[r_0 \ln(1 + d/r_0)]} \tag{6.1}$$

These results are shown in the Fig. 6.4 plot for the tip radius $r_0 = 10nm$. For the thick anode (theoretical) case $p = 20\mu m$, the numerical solution is seen to approximate the analytical solution Eq.(6.1) to within 5%. The field E_{max} at the cathode tip is 1.18 $\times 10^7$ V/cm at 200 V for the present device with a knife-edge cathode ($h = 0.3\mu m$, $p = 0.6\mu$m, r_0= 10nm) in the lower plot of Fig.6.4 based on numeric simulator.

With the cathode at a midrange height $h = 0.3\mu m$, the E_{max} field is plotted Fig.6.5(a) as a function of the cathode-to-anode separation d with anode voltage V_a as a parameter. The field E_{max} at the cathode height h is shown in Fig.6.5(b). A tip radius r_0=10nm was selected for both of these plots as representative of

the experimental devices. These plots show the sensitivity of the cathode E-field to the design parameters d and h. For the present experimental design, we have selected $p = 0.6\mu m$, $d = 0.8\mu$m and $h = .05\mu$m. The smaller h value results a preferred electron trajectory whereby 100% of the electrons are collected at the front face of the anode.

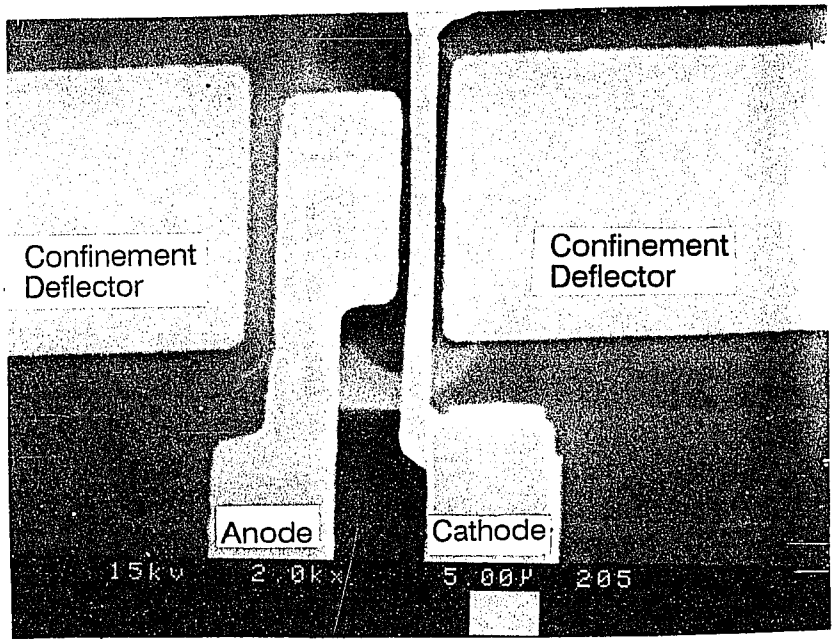


Figure 6.2: SEM top view of processed device

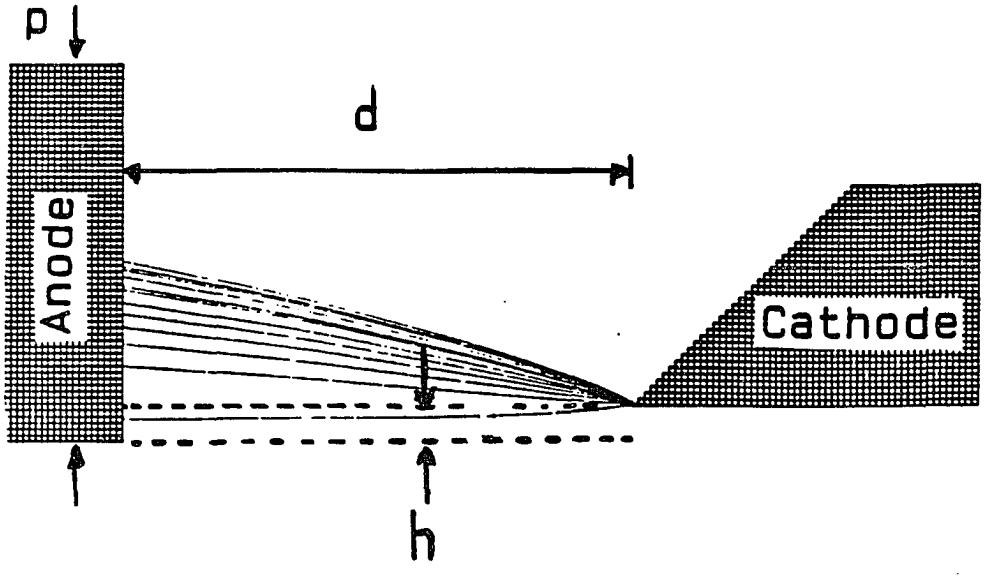


Figure 6.3: Representive simulation geometry for E_{max} calculations

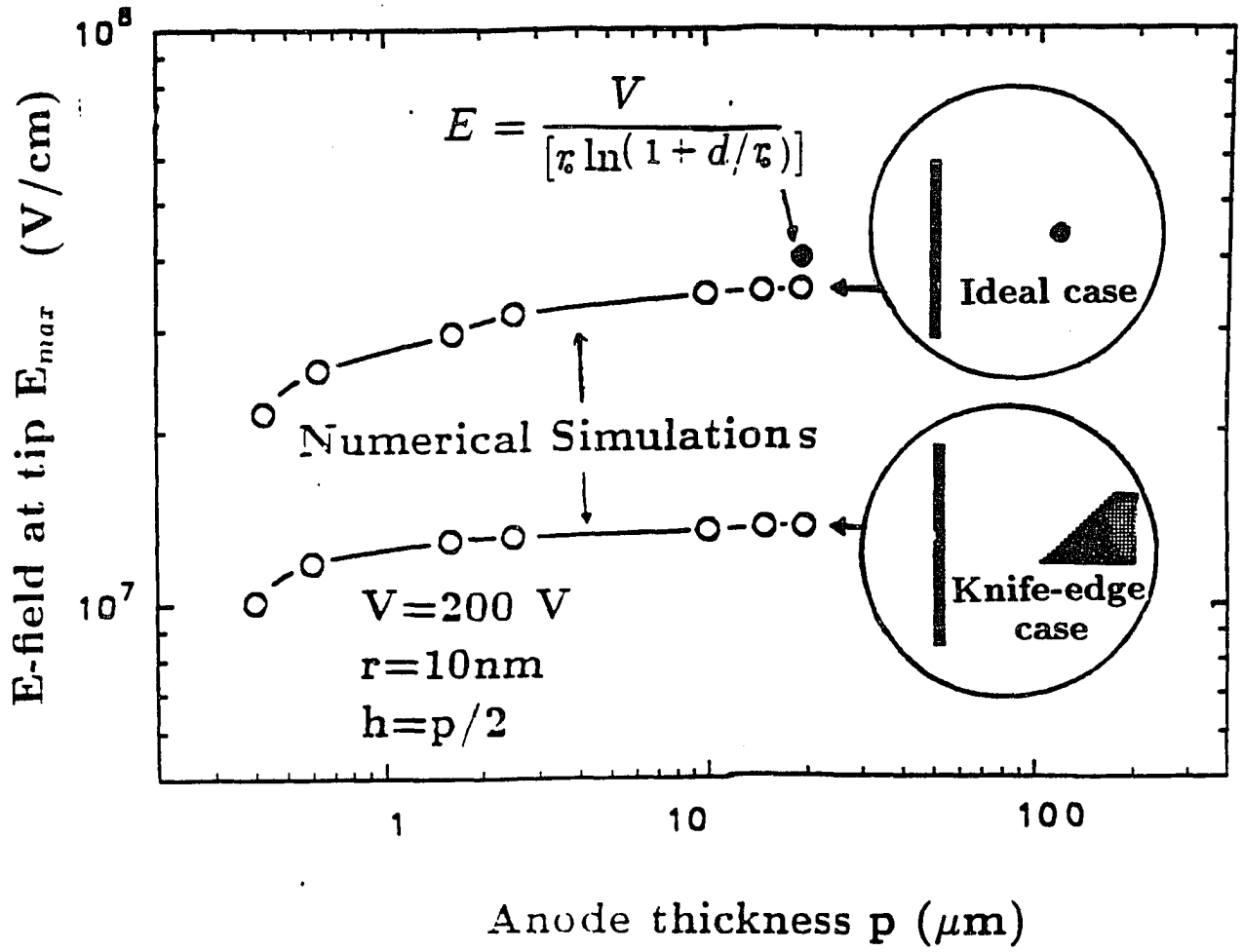
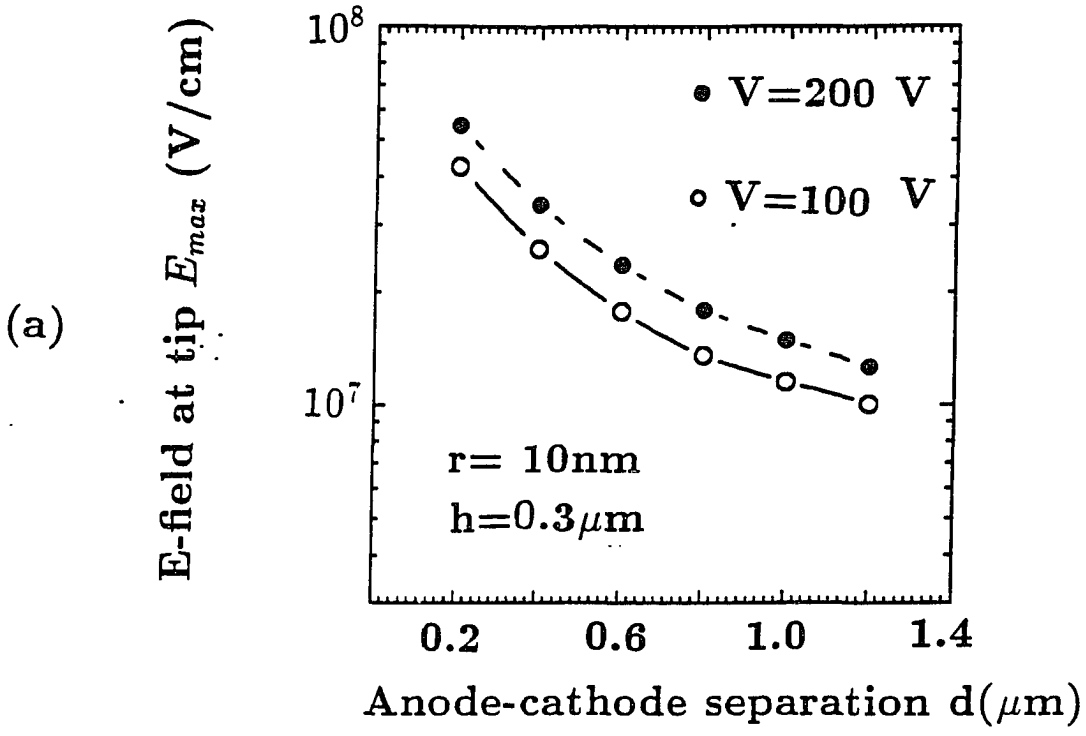


Figure 6.4: Maximum cathode field E_{max} as a function of anode thickness p



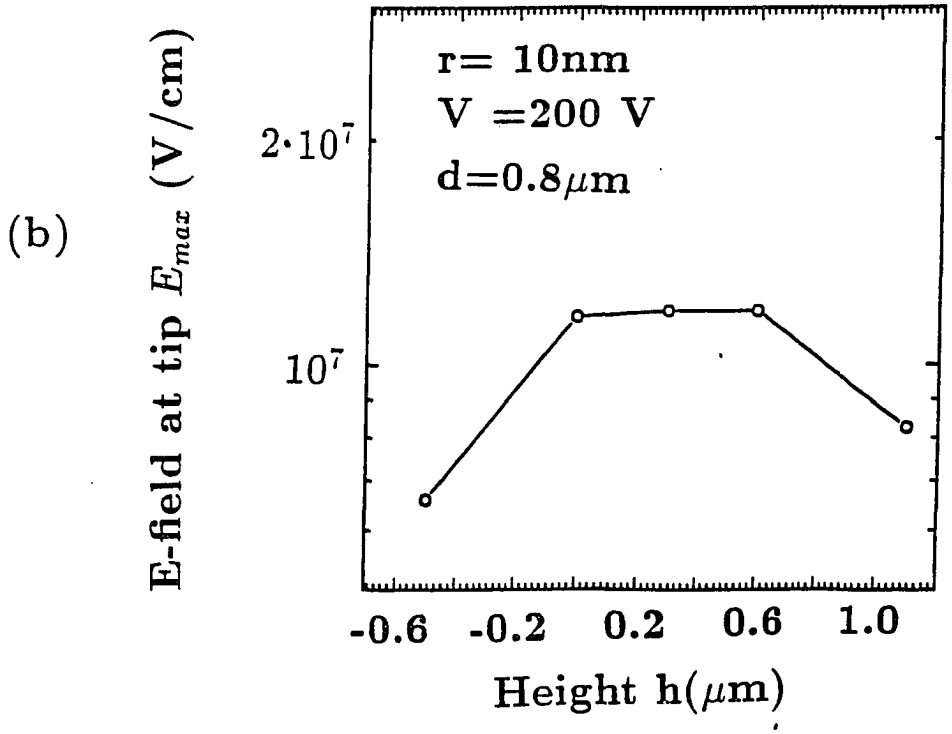


Figure 6.5: Maximum cathode field E_{max} as a function of (a) cathode height h and (b) anode-to-cathode separation d

6.3 Fowler Nordheim Modeling

Our simulation modeling is based on (a) a geometry -based Laplace calculation of the electric field E_{max} at the cathode emission surface and (b) use of the Fowler-Nordheim relationship for current density J_{FN} of emitted electrons from the high-field surface area[Ref.6-9],

$$J = \frac{aE^2}{\phi t^2(y)} \exp[\frac{-b\phi^{3/2}v(y)}{E}] \tag{6.2}$$

where a=1.54 $\times$ $10^{-6}(AV^{-2}eV)$, b= 6.87 $\times$ 10^7 $(Vcm^{-1}eV^{-3/2})$, ϕ= metal surface work function(eV), $t^2(y) = 1.1$, $v(y) = 0.95 - y^2$ and $y = \sqrt{cE}/\phi$; $c = 1.44 \times 10^{-7}(eV^2cm/V)$. The measured emission currents originate only in the tip region of the cathode where $0.9E_{max} \leq E \leq E_{max}$. Eq.(6.2) with the coefficients simplified provides Eq.(6.3) which is the basis for our curve fitting to the experimental data.

$$I = AV^2 \exp(-B/V) \tag{6.3}$$

We obtain experimental values for A and B from the F-N formattted Eq.(6.3). The electrical field over the emission region of the cathode is simplified to a single field value E_{max} as a modeling simplification. In a recently published revision to the F-N Eq.(6.3), He et al [Ref.6-10] derive a correction for highly curved cathodes with $r_0 \leq 10nm$. For the devices studied in our work we have not applied this correction factor which predicts an increase in field emission current over that given by Eq.(6.2).

The field E_{max} at the emitting surface is proportional to the anode-cathode potential difference V,

$$E_{max} = \alpha V \tag{6.4}$$

where α is a geometrical sensitivity coefficient (cm^{-1}). E_{max} is calculated from Laplace solutions based on the device geometry. The simulation for E_{max} values

uses a geometry similar to the Fig.6.3 cross section and is described in more detail elsewhere by Carr et al[Ref.6-11]. At V= 200 V from Fig.6.3, the electric field E_{max} on the knife-edge cathode emission surface is 1.18×10^7V/cm for a cathode-to- anode separation d=0.8μm. The calculated sensitivity parameter α for this geometry is $6.0 \times 10^4 cm^{-1}$.

We wish to maximize the fraction γ of the knife-edge cathode surface which is emitting electrons. The figure of merit γ is defined by the relationship,

$$\gamma = \frac{I}{S_{geo} J} \tag{6.5}$$

where I is the experimentally measured value of cathode current and S_{geo} is the geometrical area(nm^2/μm) of the knife-edge cathode exposed to electric field E values within 10% of E_{max}. A fraction γ=1 describes a cathode that emits electrons at the current density level predicted by the Fowler Nordheim equation over 100% of its high field surface. The parameter γ is interpreted physically to be that area fraction within the high field region which is actually emitting electrons. It is generally believed that emission from many devices is characterized by isolated "hot spots". To the approximation, $v(y)$ in Eq.2 is dependent upon E and work function ϕ. The value γ for the emission area is of particular importance for most applications From Eq's (6.2),(6.3),(6.4) and (6.5) , the expression for γ becomes,

$$\gamma = \frac{1.1 \phi A}{a \alpha^2 S_{geo}} \exp(\frac{b \phi^{3/2} C - \alpha B}{E_{max}}) \tag{6.6}$$

where α is a nonlinear function of tip radius r_0 and C is constant. The units for A and B in this case are A/V^2 and V, respectively. Those parameters that are important for the calculation of γ are listed in Table I for the selected devices. A work function ϕ of 4.3 eV [Ref.6-12,13] for the tungsten cathode surface is used. It is important that the cathode surface be maintained in an clean condition[Ref.6-14] and that ultrahigh vacuum conditions be maintained for testing. The high

field maximum surface area S_{geo} for the cathode is

$$S_{geo} = \frac{\theta_e \pi r_0 l}{180} \tag{6.7}$$

where θ_e, r_0, and l are the emitting angle, edge radius and cathode length. From Eq's (2) to (7), a more complete expression for γ is obtained.

$$\gamma = \frac{198 A\phi}{\pi a \theta_e \alpha^2 r_0 l} \exp(\frac{-bc}{\sqrt{\phi}}) \tag{6.8}$$

where the units are $a(AV^{-2}eV)$, $b(Vcm^{-1}eV^{3/2})$, $A(Amp/V^2)$, $\phi(eV)$, $c(eV^2cm/V)$, $\theta_e(degrees)$, $\alpha(cm^{-1})$, $r_0(cm)$ and $l(cm)$, respectively.

6.4 Device Fabrication

The fabrication process emphasizes optimization of the cathode structure. Diodes are used to characterize the cathode electrically. Devices with a cathode-to-anode physical separation $d = 0.8\mu$m are selected for electrical characterization. The mask design for the complete test device described in this study is shown in Fig.6.2. Discussion of the electron confinement deflectors shown in Fig.6.2 is the subject of a separate report[Ref.6-11].

6.4.1 Cathode processing

The device processing begins with fabrication of the cathode and is followed by fabrication of the anode . Initially the wafers are coated with a p-glass which provides low mechanical stress(compressive $2 \times 10^9 dynes/cm^2$) and a high electrical breakdown voltage. A 2.5μm film of 4% p-doped SiO_2 is deposited by PECVD on 125mm silicon substrates. Deposition of the metal films is preceded by a deep UV- hardened resist film to facilitate the liftoff [Ref.6-15] of the triple metal film laminate. The choice of metals is made more clear by inspection of Fig.6.6. A chamber pressure of 6 to 8 mT is selected for the 700 watt power of our Varian

3190 dc magnetron sputtering system. The built-in stress of Ti:W is reduced to levels below $20\times10^9 dyne/cm^2$ for an approximate match to low compressive stresses obtained with p-glass and aluminum. The very large compressive stress of the tungsten film is contained to a low strain level by the Ti:W and Al-SiO_2 laminates[Ref.6-16]. Free-standing(released) simple beam structures of this laminate do not buckle or break confirming the low stress level of this 3-layer film: Al(.05μm) /W(.25μm) /Ti:W(.1μm)

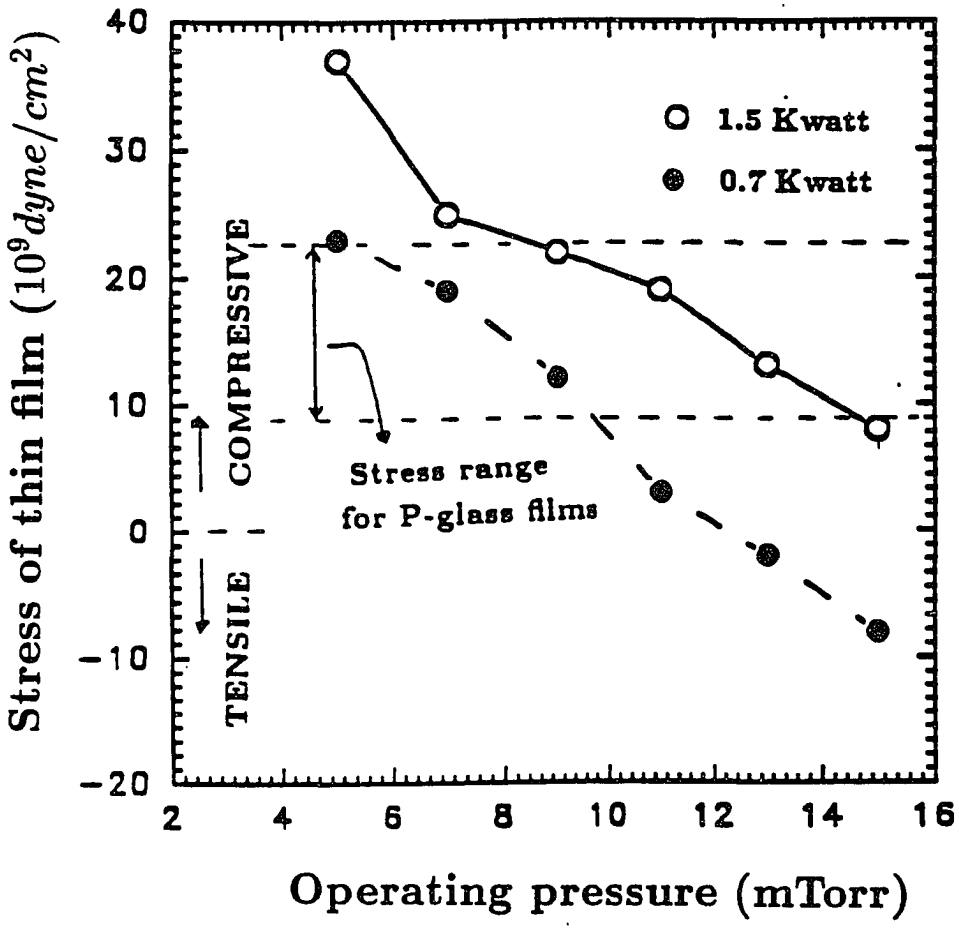


Figure 6.6: Internal Ti:W stress as a function of sputter chamber pressure following 400°C anneal

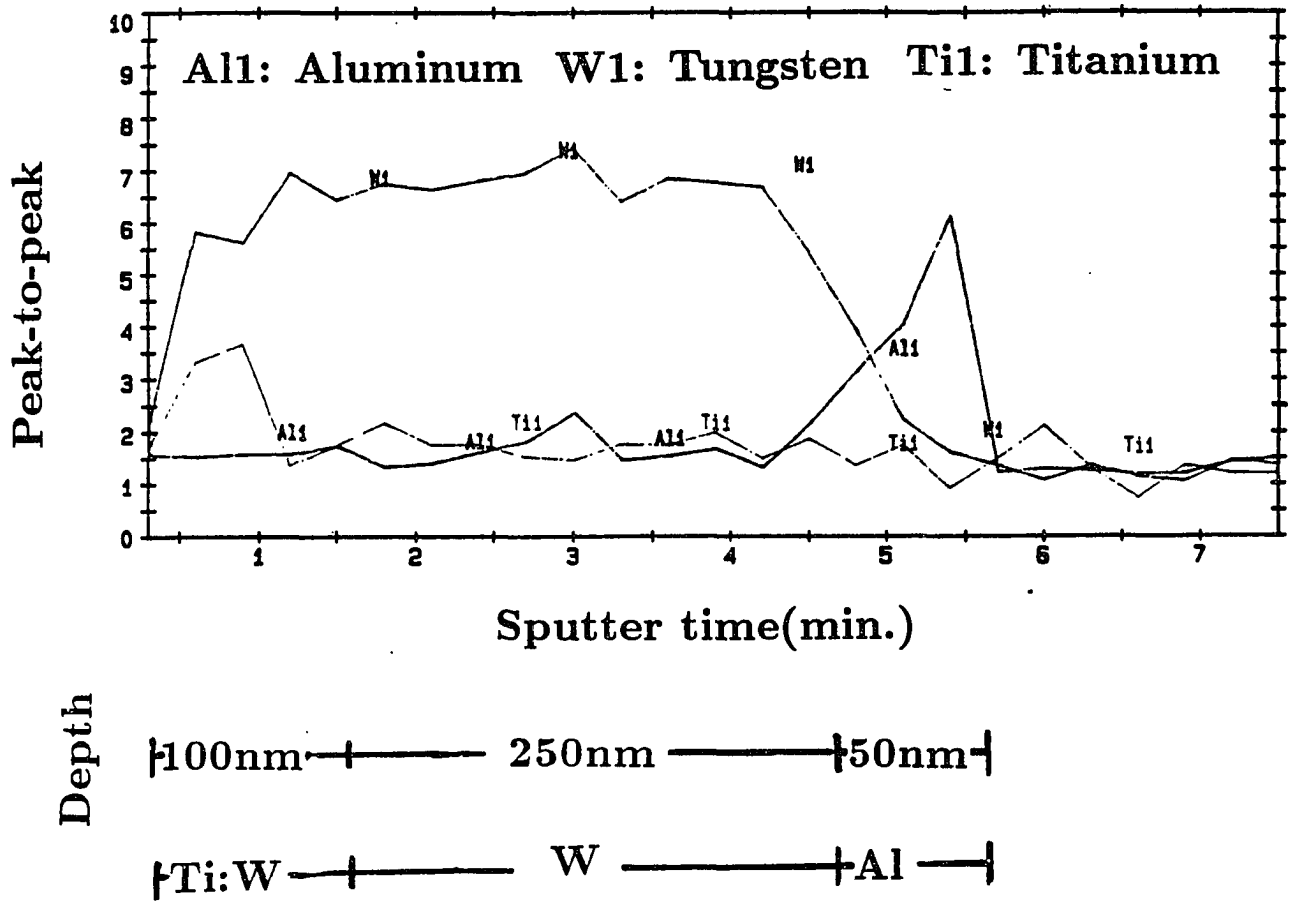


Figure 6.7: Cathode films composite: Auger spectroscopy plot of atomic concentrations as a function of depth.

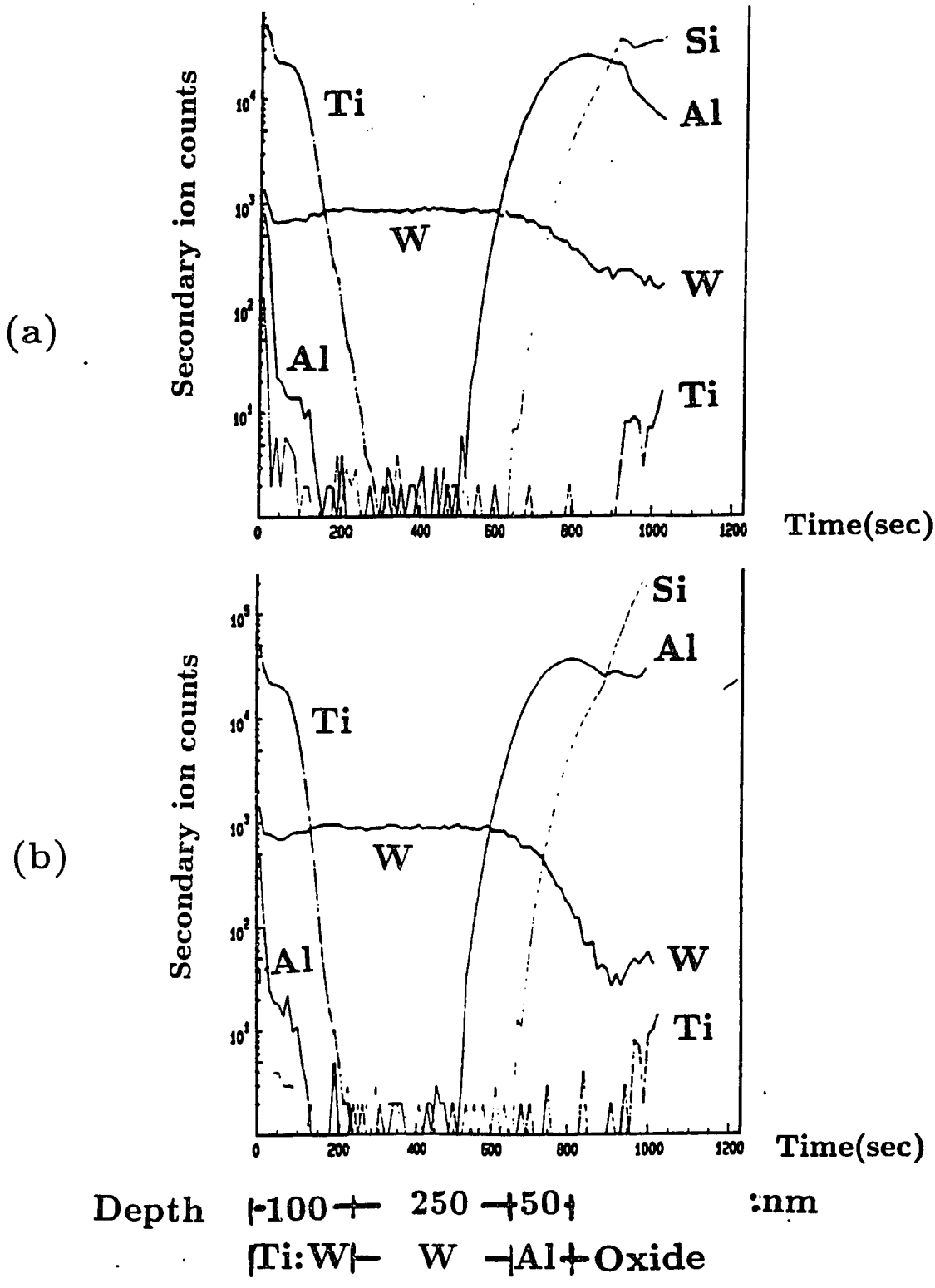


Figure 6.8: Cathode films composite: SIMS depth profile of ion counts as a function of depth (a) before annealing (b) after 400^{0}C.

In Fig.6.7, the Auger analysis of the cathode films shows the relatively thin Ti:W film covering the tungsten with underlying aluminum. The SIMS plot of Fig.6.8 further confirms the structure. The tungsten has penetrated the aluminum during the sputtering process. The effect of annealing has been to reduce the sputter rate for the tungsten film. The Ti:W/W/Al laminations are clearly shown in both the Auger and SIMS analysis.

Sputtered tungsten is generally undesirable in VLSI processing because of its poor step coverage. In our case, the very thin sidewall provides the knife-edge desired and as a secondary asset facilitates photoresist liftoff. Our process uses a low temperature substrate and a low chamber pressure [Ref.6-17]. This preferred process does result in a tungsten deposition with the large compressive stress which requires the Ti:W and aluminum stress control films. Following cathode metallization, the cathode is defined by metal liftoff in ST-20 stripper at 80^0C.

6.4.2 Anode processing

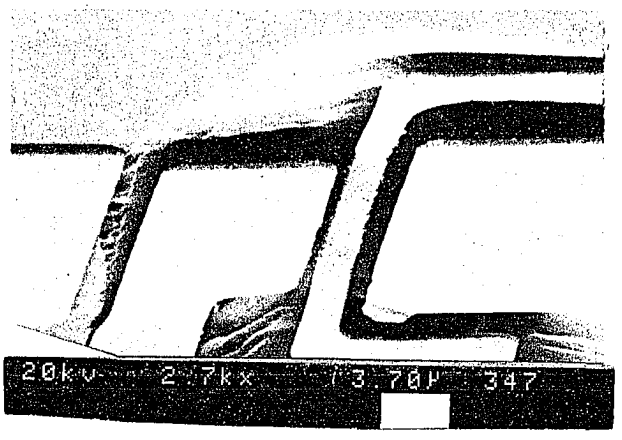
The anode is fabricated using a triple layer of Ti:W(.2μm) /Al(.2μm) /Ti:W(.2μm). The Ti:W protects the aluminum from the extended BHF etch used later to selectively etch back the aluminum under the tungsten knife-edge [Ref.6-16]. The resulting aluminum film within the anode provides a desirable low sheet resistance. A 0.05Ω/square resistivity is well below the 1.5Ω/square achievable with Ti:W alone. The anode lithography is also a liftoff process which results in the 0.8μm cathode-to-anode separation.

6.4.3 Final processing

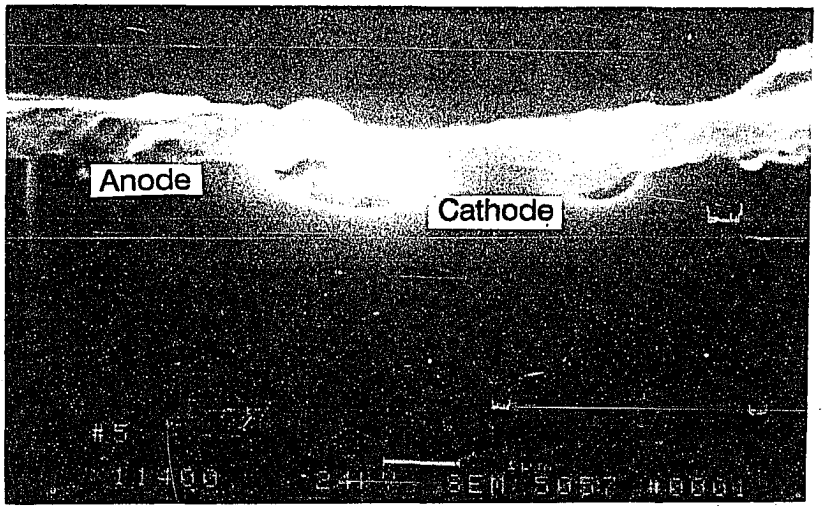
The aluminum is etched back in a BHF solution to define the tungsten knife-edge of the cathode. This is followed by an anneal step at 400^0C (N_2) which stabilizes the cathode surface and seals the anode sandwich structure. The SEM view of a

fully processed device is shown in Fig.6.9(a),(b) and (c). The view (a) shows some structure in the knife-edge which can be expected to result in nonuniform cathode current density ($\gamma \leq 1$). View (b) shows the 0.8μm separation between cathode and anode. View (c) is an isolated SEM image of the cathode knife-edge with underlying aluminum and overlaying Ti:W. Our best estimate of the knife-edge radius r_0 is 10nm from SEM views.

(a)



(b)



(c)

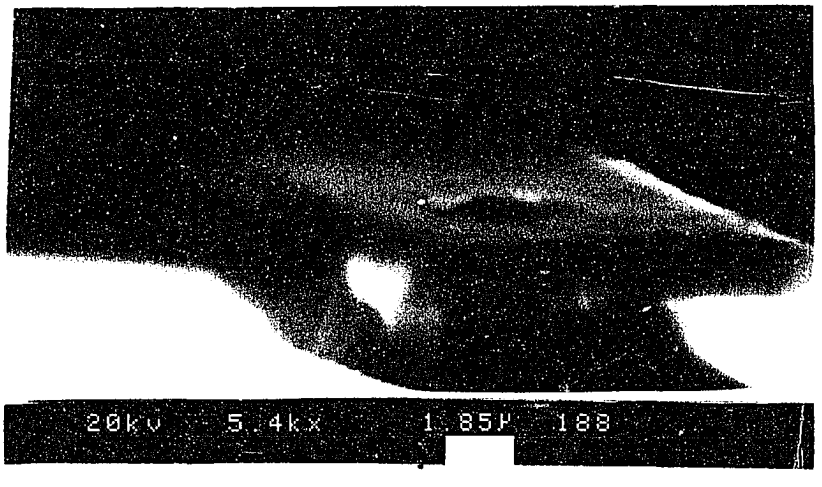


Figure 6.9: SEM views obtained with a fully processed device (a) oblique angle view of entire device (b) sideview showing anode-cathode section and (c) oblique angle view of cathode only

6.5 Electrical Characterization

Devices in ceramic packages have been characterized electrically at a vacuum level of 2 to 5 $\times 10^{-9}$ Torr. Static IV characteristics for 4 selected diodes are shown in Fig.6.10 using a linear scale. The maximum current level of 26 μA for a 23 μm length cathode knife-edge corresponds to 1.1μA per μm of cathode length l. The dc leakage current for these devices is rather large(1μA at 160 volts). These data describe devices that have not been subjected to a "burn-in " period. These diodes are observed to turn on with a 90% increase in anode current with an anode voltage differential of 50 volts.

In Fig.6.11, experimental data is plotted in F-N format. Here a straight line fit is obtained over a limited current range. For device #1 a match between experimental values and Eq.(6.1) and Eq.(6.3) is obtained with work function ϕ= 5.3 eV, emission area fraction γ= 0.38 and knife-edge radius r_0= 10 nm. For further comparison, the F-N format plots for the other 3 selected diodes are shown in Fig.6.12. The characteristics of all four diodes are similar.

The emitting area fraction γ can be calculated with Eq.(6.8) when the A parameter is determined from the F-N format plots. From Fig.6.12, the experimental value A=$3\times10^{-5}(A/V^2)$ provides a "best fit" to the experimental data. Calculated cathode current is plotted in Fig.6.13 as a function of the tip radius r_0 with cathode surface work function ϕ as a parameter. The plot in Fig.6.13 is based on the F-N ideal emission current and the emission fraction γ. Figure 6.14 is a plot of Eq.(6.8) and extends the curve fit for surface work function values of ϕ = 3.3, 4.3, and 5.5 eV. The values used in Fig.6.14 are $A = 3.0 \times 10^{-5}(A/V^2, \theta_e = 30^0, r_0 = 10nm$. We conclude that the emission area fraction γ ranging from 0.03 to 0.8. is representative of our devices and process. The technique used to determine γ in this chapter is based on a direct use of the

F-N equation. To the extent that the F-N model is adequate, Eq.(6.8) is applicable to any field emission device. The expression γ in Eq.(6.8) may be modified using the model of Ref.6-10 for sharp cathodes. This technique may prove useful as a comparison tool for various experimental cathodes and is proposed as a figure of merit.

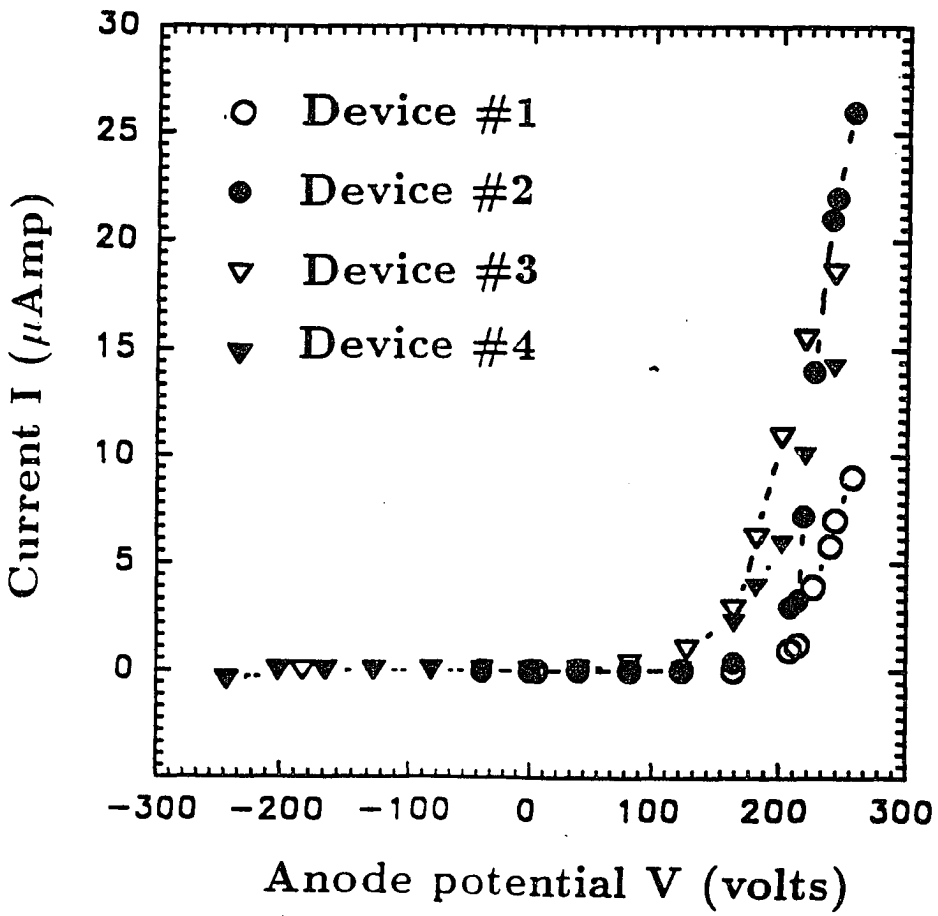


Figure 6.10: Characteristic IV plots for selected diodes #1-#4.

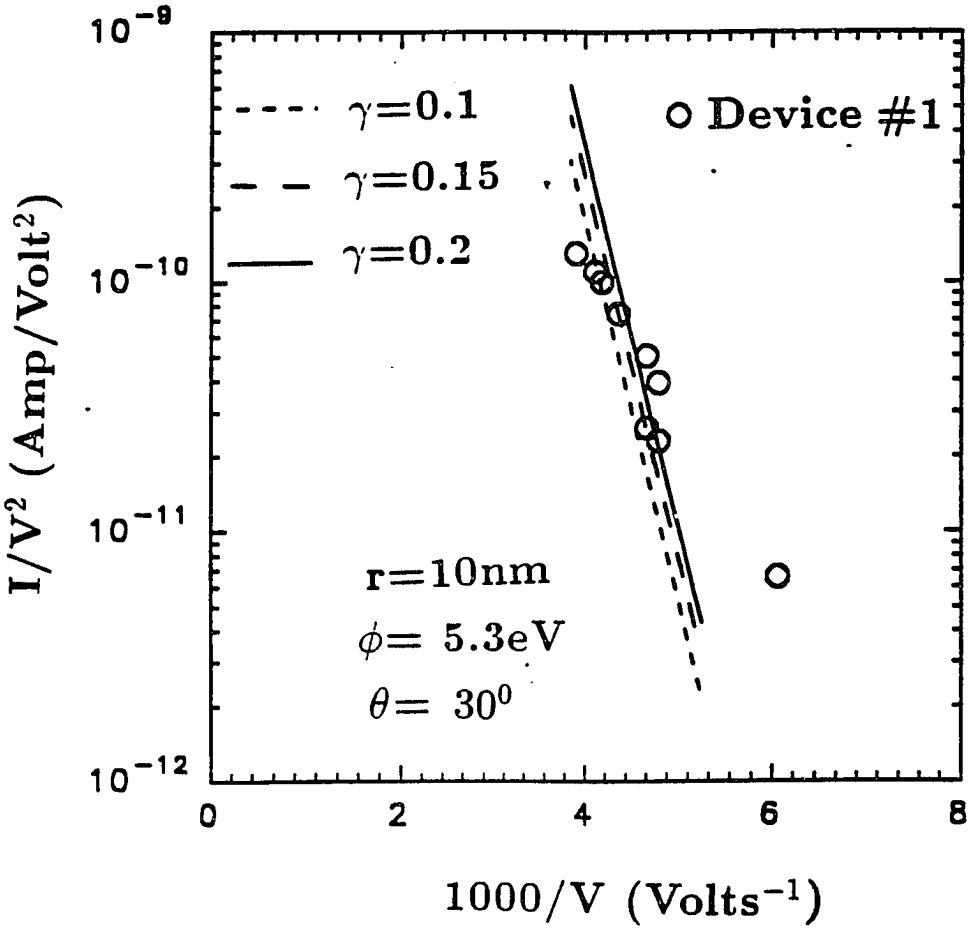


Figure 6.11: Analytical and experimental IV plots in Fowler Nordheim format for device #1

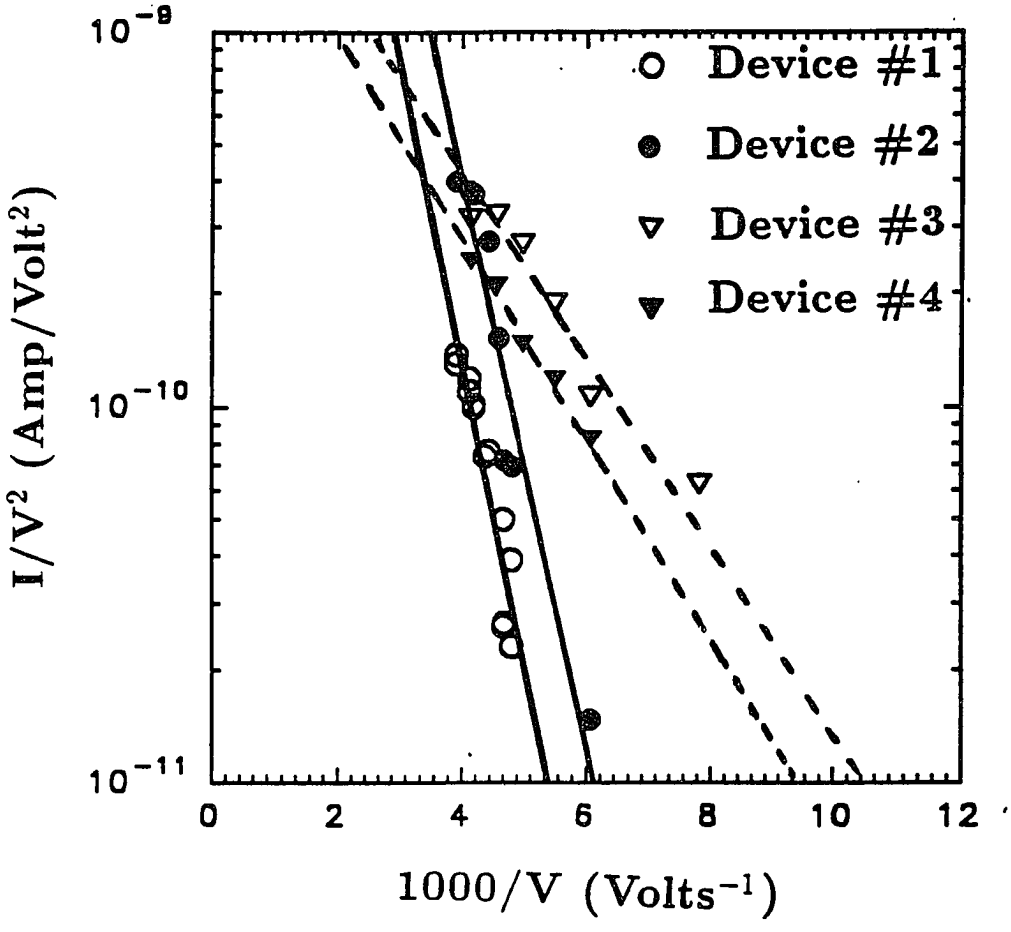


Figure 6.12: IV plots in Fowler-Nordheim formats for device #1-#4

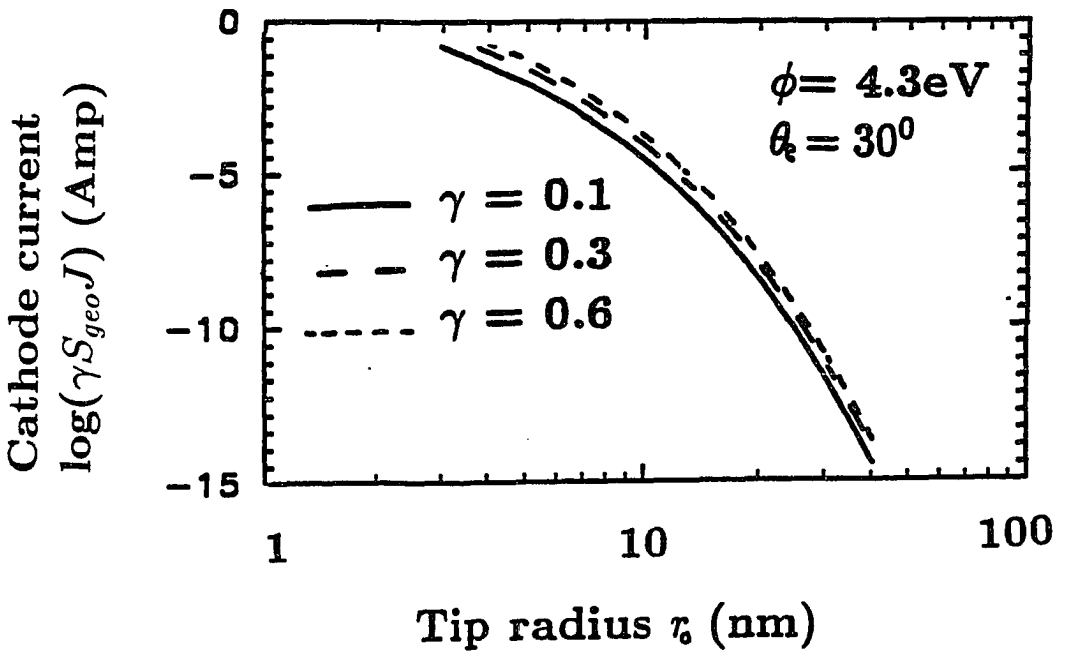


Figure 6.13: Fowler Nordheim cathode current plotted as a function of γ as a parameter

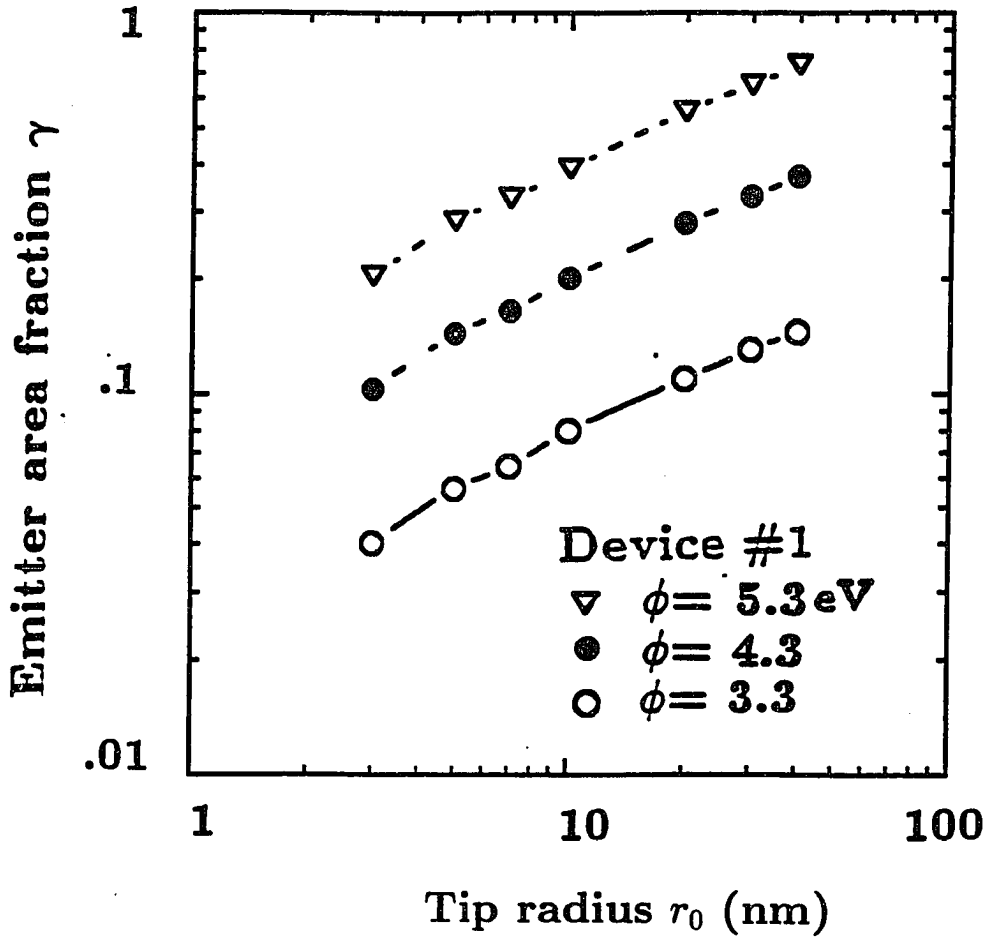


Figure 6.14: Emitting area fraction γ plotted as a function of knife-edge radius r_0.

Table 6.1: Parameters used for specifying surface emitting fraction factor γ

Parameter	Device#1
Anode voltage $V_a(V)$	200
Test pressure(Torr)	5×10^{-9}
Equation(6.3) fit:	
A (A/V^2)	3×10^{-5}
B (V)	3250
Cathode-anode separation L(μm)	0.8
Electrical field E_{avg}(V/cm)	1.18×10^7
Emitter length l(μm)	23
Knife-edge radius r_0(nm)	10
Work function ϕ(eV)	4.3
Emitting angle θ_e (degrees)	30^0
Max. available surface emission area $S(nm^2/\mu m)$	5.5×10^3
Fractional surface utilization factor γ	0.19
Max. observed current I(μA)	10

6.6 Summary

A process for fabricating tungsten vacuum microelectronic cathodes for lateral electron trajectories has been described. By this technology, the customized micromachining for the field emitter is not necessary. The sharp field emitter by the liftoff process does not require separate optimization. This process described here for a diode with trajectory confinement deflection electrodes included is suitable for fabrication of triode and more complex devices. The electric field E_{max} at the cathode surface is calculated for a smooth cathode surface condition. The cathode static current density predicted by the Fowler- Nordheim relationship for a uniformly emitting cathode is compared with experimental measurement. The fraction of high field cathode surface emitting is $0.03 \leq \gamma \leq 0.8$ $(3.3eV \leq \phi \leq 5.3eV)$ for the cathode characterized based on the present model.

Chapter 7

7.1 Summary and conclusions

This dissertation concludes that RIE-based technology for micromachining field emission cathodes and other controlled sidewall structures is very feasible. Cathode structures that are applicable to a variety of electron beam devices have been fabricated and characterized. Also the same technology is applicable for obtaining grooved, reflecting optical surfaces. The electron sources are field emission cathodes of N-type silicon and tungsten material shaped by a combination of UV lithography and reactive ion etching. Optimized processing, device modeling, and physical/electrical characterization have been described in this dissertation.

Processing with a "top hat" shadow mask over the silicon substrate has been used to define a wedge cathode appropriate for electron field emission application. A process technology for tungsten metal films by dc magnetron sputtering deposition is developed and characterized to fabricate operational field emission vacuum diode and tetrode devices.

Several reactive ion etching experiments are detailed. The effects of silicon wafer tilting on RIE etch rate and anisotropy are characterized. Complex phenomena are interpreted in terms of ion milling and free radical reactions to explain the observed anisotropy. Silicon ridge structures with an apex radius of approximately 40 nm were obtained with photoresist shadow mask "top hat"and deep

UV-hardened photoresist. Less desirable results are obtained for silicon etching with image reversal aluminum liftoff masking for field emitter applications.

A field emission device design is accomplished using a 0.8 micron critical dimension for the cathode-to-anode separation. The electron trajectories are calculated using SIMION for different cathode shapes and relative heights as a guide to geometry control. Tungsten metal films are deposited by dc magnetron sputtering in separate operations for the cathode and anode. Liftoff lithography (deep UV-hardened resist) and thermal annealing of the metal are used. This step showed the new knife-edge cathode fabrication technology with high yields of liftoff and the intrinsic sharpness at tips. At same time, we found the new thin film sandwich structure which provides the low resistivity and high tolerance to acids. The resulting diode devices show an overall cathode current of 23 μA for a 23 μm length cathode at 250 volts. Device characterization is done in a UHV vacuum at 2 to 5 $\times 10^{-9}$ Torr. The resulting IV plots match with the Fowler-Nordheim theoretical model over the 1.5 decade electrical current range. A new analysis technique for calculating effective field emission surface fraction γ is presented.

Here a potential tetrode geometry with a cusp cathode of tungsten is fabricated by the reverse image liftoff process and described here for the first time. The cathode has a current of 0.1μA per micron of cathode length. In this geometry, the role of the deflecting grids for the lateral devices was shown experimentally for the first time.

This dissertation introduces a liftoff process based on metallization with a dc magnetron sputtering metallization which provides high emission current in tungsten cathodes. The emission current of these cathodes compares well with the results recently published by other laboratories [Table.7-1]. This study

concludes that the annealed titanium:tungsten/tungsten sandwich structure can result in useful field emission cathodes. A special advantage of the demonstrated tungsten processing technology is that special steps for cathode sharpening is not needed. The diode NJIT(D) and tetrode(T) static electrical characteristics are compared with results published by other laboratories in Table 7-1. This dissertation presents the first results for field emission cathodes fabricated with liftoff lithography. The maximum emission current per micron cathode length compares well with results reported to date for other laboratories [Table.7-1].

Table 7.1: Recently published field emission cathode characteristics

Laboratory	Target Appl	Published reference	Emission Current $\mu A/Tip$	Array Count or tip dimension	Cathode Material	Trajectories/ Device type
NJIT-91	1,3	[7-13]	$1\mu A/\mu m$ at 250V	23μm Wedge	W	Lateral/D
NJIT-91	1.3		$0.1\mu A/\mu m$ at 250V	23μm	W	Lateral/Tet
LETI-90	1	[7-1]	0.1μA at 80V	10000	Mo	Vertical/T
SRI-90	1.2	[7-2]	90μA at 212V	10000	Mo	Vertical/T
Fujitsu-91	1	[7-3]	10μA at 80V	6400	Si-n	Vertical/T
Matsushita-91	1	[7-4]	3μA at 65V		Mo	Lateral/D
E T L-91	1	[7-5]	1μA at 160V	20	W	Lateral/D
Futaba-91	1	[7-6]	0.7μA at 125V	14700	Mo	Lateral/D
Epson-91	1	[7-7]	50 nA at 160V		Mo	Lateral/T
USSR-89	NA	[7-8]	4μA at 12V		Mo	Vertical/D
Bellcore-90	1	[7-9]	1μA at 400V		Si	Vertical/D
Hughes-90	2	[7-10]	0.3μA at 30V	100	Mo/Si	Vertical/T
L L L-90	3	[7-11]	0.2μA at 10V	22500	Si	Vertical/D
NRL-91	2	[7-12]	0.9μA at 150V	100	Si	Vertical/D
Rutgers-90	1.2	[7-14]	.6nA μ^2 20V	1350 μ^2	Si	Vertical/D
MIT-91	NA	[7-15]	55pA/μ^2 200V	3600 μ^2	C	Vertical/D

Appllication: 1.Flat panel Display
2. μwave Amplifier
3. Logic Device

D: Diode
T:Triode
Tet: Tetrode

7.2 Applications of field emitters in state-of-the-art technology

7.2.1 Microwave applications

The field emitter array(FEA) can be used as an electron source for microwave devices including the klystron, TWT, and distributed amplifiers.

The cathodes introduced in this dissertation can be used as the electron source in microwave amplifiers or microwave power sources taking advantage of higher emission current from the long knife-edge emitter.

Another application is the distributed amplifiers (DA) with wide bandwidth and high gain at microwave frequencies. Simulations for the distributed amplifiers were published by Kasmahl[Ref.7-16] and Wiltsey et al[Ref.7-17]. A design and performance model for distributed amplifiers(DA) is published [Ref.7-16,18]. These simulations show that devices with high transconductance g_m above 100 GHz and cutoff frequency of 8THz are potentially possible with properties superior to those of GaAs FET amplifiers.

7.2.2 Flat panel displays

The field emission flat panel display, can utilize the cathode technology presented in this dissertation. The field emitter can be used in to two types of flat panel displays: (1) plasma photon excitation of the phosphor layer (plasma displays)[Ref.7-19], (2) direct electron illumination of the phosphor layer (fluorescent microtip displays) [Ref.7-20]. A fluorescent microtip flat panel display using an array of gated emitters was first announced in 1990 [Ref.7-20]. The electrons from field emitter tips bombard directly the phosphor layer and illuminate. The cathode electrode was deposited by e-beam evaporation. The gate electrode was composed of niobium. The anode was a transparent ITO layer deposited on a glass sub-

strate and covered with a phosphor. Recently, the prototype for black and white displays by gated field emitter arrays was shown by Vaudaine et al [Ref.7-21].

7.3 Other applications

There are many other applications that can benefit from a stable, high current density field emission cathodes for electron microscopy, vacuum microelectronic logic devices, and a variety of sensors.

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Appendix A

E-field at tip E_{max}(V/cm) versus tip radius r_0(nm)

The maximum electric field at tip is represented as a function of the tip radius r_0 for the devices under test.