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Direct Schottky Injection Image Sensors

Subramanyam V. Ayyagari
New Jersey Institute of Technology
Newark, NJ 07102

Thesis Advisor: Walter F. Kosonocky

ABSTRACT

This thesis describes the analysis and simulations of Direct Schottky Injection (DSI) imagers which have 100% fill factor. Frame transfer (FT) and interline transfer (IT) DSI imager structures have been investigated. Theoretical Poisson solution for the P^-P and P^-NP FT-DSI structures is presented, which closely agrees with simulation results. Simulation for frame transfer FT-DSI imagers has been done in SUPREM III since 1-D effects are more dominant. Single carrier transit time for both the structures were estimated from the electric fields.

Simulations of IT-DSI structures was done using PISCES IIb, to get the local electric fields, which define the directionality of the signal. Zero carrier Poisson analysis was done to get empty potential wells. Effects of additional implants on the device performance has been discussed. Transient analysis was carried out to see the effect of fast changing scenes, on the performance of the imager. The analysis shows that the effective pixel sizes tend to decrease as larger charge signal is collected.

Direct Schottky Injection Image Sensors

by

Subramanyam V. Ayyagari

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Title of Thesis: Direct Schottky Injection Image Sensors.

Name of candidate: Subramanyam V. Ayyagari

Thesis and abstract approved:

Dr. Walter F. Kosonocky	**Date**
Distinguished Professor	
Dept of Electrical Engineering	
New Jersey Institute of Technology	
Dr. D. Misra	**Date**
Assistant Professor	
Dept of Electrical Engineering	
New Jersey Institute of Technology	
Dr. K. Sohn	**Date**
Assistant Chairman	
Dept of Electrical Engineering	
New Jersey Institute of Technology	

VITA

Name of the candidate: Ayyagari V. Subramanyam.

Degree and date to be conferred: MSEE., January 27th, 1991.

Date and place of birth:

Collegiate institutions attended:

Degree	University / Institution	Date of completion
1) Bachelor of Engineering. (Electronics and Communication)	Osmania University Hyderabad, India.	August, 1987.
2) Master of Science. (Electrical Engineering)	New Jersey Institute of Technology, NJ.	January, 1991.

Position held:

Research Assistant under Dr. Walter F. Kosonocky, from 1989 (summer) to 1990 (Dec).

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CHAPTER 1

Introduction

The concept of Direct Schottky Injection (DSI), was proposed by Kosonocky to achieve a Schottky-barrier image sensor with 100% fill factor [1, 2]. This thesis analyses two possible constructions for frame transfer (FT) DSI imagers. An Interline transfer (IT) type of DSI imager was also simulated and some of its characteristics were investigated. Various techniques to improve the performance of these imagers is discussed.

In Chapter 2, basic operation of a Schottky-barrier detector is discussed. Various parameters that characterize the behaviour of infrared imagers are reviewed. Sources which give rise to dark currents are considered, the major source being due to large electric fields at the PtSi / Si junction. Techniques to reduce dark currents in Schottky-barrier detectors are discussed.

In Chapter 3, theoretical Poisson solution is carried out for a P^-NP and a P^-P frame transfer imagers. Channel potentials for empty well case are compared with those obtained from SUPREM III simulations. In this analysis the doping concentrations were assumed constant. Single carrier transit times were estimated from the electric field expressions.

In Chapter 4, SUPREM III simulations were done using practical doping profiles. Charge handling capacities were obtained and also methods to reduce electric fields have been suggested. For the case of a P^-NP imager, conditions under which the imager fails to work have been discussed.

In Chapter 5, interline DSI imagers were simulated using PISCES IIb. Zero carrier Poisson-only solutions were obtained by properly adjusting the quasi Fermi potentials. Effects of additional implants on the drift speed of the incoming holes are

discussed. Transient simulations were carried out and potential profiles with signal were obtained. 3-D profiles which give more insight on the behaviour of imager were obtained using a graphics software 'FUGU'.

In Chapter 6, conclusions for the thesis are described based on the simulation results. The concept of geometric MTF degradation in frame transfer and interline transfer type of imagers is discussed in Appendix A. Input files that were used for process/device simulations are given in Appendix B.

CHAPTER 2

Overview of Schottky-barrier Detectors

In 1973, Shepherd and Young proposed the concept of silicide Schottky-barrier detector (SBD) focal plane arrays as a more reproducible alternative to HgCdTe focal plane arrays for thermal imaging [3]. Basic SBD structure is fabricated by means of electron beam evaporation of platinum on a chemically polished surface of <100> p-silicon wafer of resistivity ranging from 10-100 Ω cm, to form a 10 A^o thick layer [4]. Later platinum is sintered (or annealed) at temperature in the range of 300-600 ^oC to form a PtSi layer of about 20 A^o thick. The internal photoemission of the photoexcited carriers over the Schottky-barrier has optimal yield for PtSi films of vanishing thickness, while the absorption is greatest for films on the order of 100-300 A^o. Optimal thickness of PtSi is determined by balancing these two opposing influences. Conventionally, these imagers are used in the back illumination mode. Infrared photons with energies less than the bandgap of silicon are transmitted and absorbed in the silicide film, where they generate carriers that produce detector signal. Quantum efficiency (Q.E.), as will be discussed later on, is the ratio expressed as a percentage, of the number of photogenerated carriers that are detected to the number of incident photons. There is a reduction in Q.E. for front illumination because photon absorption is reduced due to highly reflective PtSi, but this effect is less for back illumination as silicon acts as index-matching layer between PtSi and air [5].

Other types of silicides have also been used for infrared imaging. Table T.1 shows the type of silicides used and the wavelength at which they are used. There is a strong absorption in the 5-8 μm range in the atmosphere and so thermal imaging is not done in this range. In the case of Schottky-barrier imagers, n-type silicon is not used because the barrier height is large and cutoff wavelength permits operation only in the

visible region. SBD imagers using IrSi with a cut-off wavelength of 10 μm [6] have large amount of photon flux available (about 50 times of that in 3-5 μm range), but the relative contrast is poor and it has to be cooled to about 40K to reduce large dark currents (barrier height is less).

IR -RANGE	ϕ_{bp} (ev)	$\lambda = \frac{1.24}{\phi_{bp}}$	ϕ_{bn} (ev)	$\lambda = \frac{1.24}{\phi_{bn}}$	TEMP	SILICIDE
SWIR (1 - 3 μm)	0.37	3.35 μm	0.75	1.65 μm	120 - 140 K	Pd_2Si
MWIR (3 - 5 μm)	0.22	5.64 μm	0.9	1.38 μm	60 - 80 K	PtSi
LWIR (8 - 12 μm)	< 0.17	7.29 μm	0.95	1.31 μm	40 K	IrSi

Table T.1 Silicides used in Schottky-barrier IR Imagers

2.1 OPERATION OF SBD

Infrared (IR) signal falls on the PtSi layer and if it is back illuminated, it passes through the transparent p-silicon and impinges on the PtSi layer. Sensing is done by internal photoemission, which is a two step process. Firstly, photons are absorbed in the silicide, resulting in excitation of electrons above Fermi level and corresponding holes below the Fermi level. Subsequently, the hot holes which have energy greater than barrier height are injected into the silicon substrate Fig. 2.1. The external photo-

emission response is given by,

$$Y = \frac{C_1(h\nu - \psi_{ms})^2}{h\nu}, \tag{2.1}$$

where,

Y = photoyield (electrons/photons)

Ψ_{ms} = Schottky-barrier potential

h ν = photon energy, and

C_1 = quantum efficiency coefficient in ev $^{-1}$.

Many analytical estimates of external photoemission response have been reported, and all of them are in a good agreement, except for the Q.E. term. According to V. E. Vickers [7], the expression for Q.E. was obtained by incorporating Fowler's temperature dependence into the zero-Kelvin yield expression of Archer et al, which is

$$C_1 = \frac{A(\lambda)}{8E_f} \tag{2.2}$$

where

$A(\lambda)$ = absorption coefficient, and

E_f = Fermi energy level.

Q.E. was calculated for electron emission by Cohen et al, and is given by

$$C_1 = \frac{A(\lambda)}{8\left[E_f + \psi_{ms}\right]} \tag{2.3}$$

According to Elabd and Kosonocky [8], Q.E. for thick films was found to be

$$QE = \frac{A(\lambda)}{8\Psi_{ms}}$$

But when the silicide layer is decreased, there is an increase in injection efficiency due to scattering at silicide/silicon-dioxide interface. Hence Q.E. is calculated to be [8]

$$C_1 = \frac{A(\lambda)}{8\psi_{ms}} \times \frac{Ls}{t}, \quad \text{where} \quad s = \frac{\ln(\frac{h\nu}{\psi_{ms}})}{2(1 - \sqrt{\frac{\psi_{ms}}{h\nu}})} - 1 \tag{2.4}$$

where,

L = attenuation length of hot holes, and

t = thickness of silicide layer.

Multiplying Eq (2.1) by "hν" and taking the square root on both sides we get:

$$\sqrt{Yh\nu} = \sqrt{C_1}(h\nu - \psi_{ms}) \tag{2.5}$$

The above equation is called "Fowler plot" [8], whose slope gives us the quantum efficiency and the abscissa intersection yields the barrier height. It is plotted in Fig. 2.2, from where its clear that ϕ_b for PtSi is 0.22 ev [9].

Its easy to relate Eq (2.1) to the more common parameter "responsivity". Current responsivity is obtained by multiplying Eq (2.1) by e ÷ h ν.

$$\text{Responsivity} = \frac{eC_1(h\nu - \psi_{ms})^2}{\{h\nu\}^2} = eC_1\left\{1 - \frac{\lambda}{\lambda_c}\right\}^2 \text{ in A / W.} \tag{2.6}$$

2.2 SOURCES OF DARK CURRENTS

The generated carriers in absence of any light signal, constitute dark currents. They take up the available charge handling capacity of the readout multiplexer and also tend to be spatially non-uniform. The main sources which contribute to dark current in semiconductor devices are as follows

- Dark currents arise due to intrinsic transition of electrons from valence band to conduction band in the depleted silicon substrate. The generation rate for this process is given by

$$U_i = \frac{n_i}{\tau_i} \tag{2.7}$$

where,

n_i = intrinsic carrier concentration, and

τ_i = carrier lifetime in intrinsic material.

- Diffusion of minority carriers from the neutral bulk also give rise to dark noise. Only those carriers generated within a diffusion length from depletion region, are

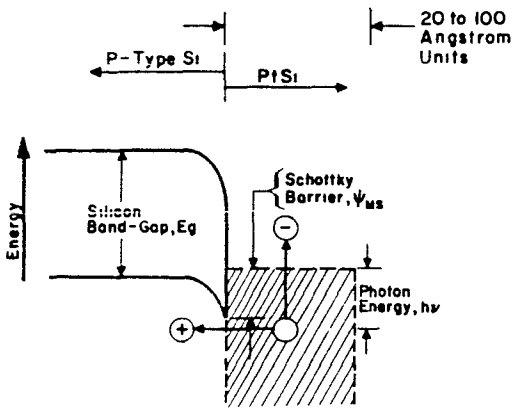


Fig. 2.1. Basic operation of SBD

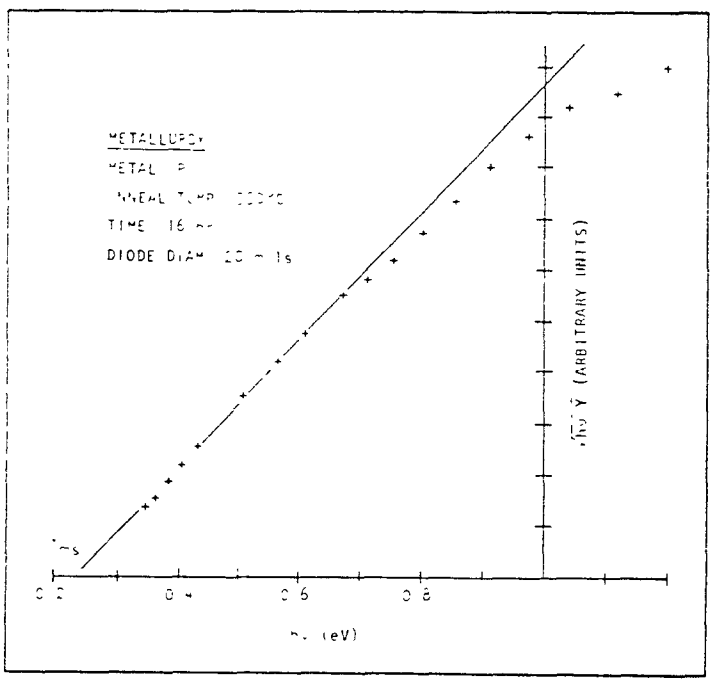


Fig. 2.2. Typical Fowler plot

W. S. Ewing, F. D. Shepherd et al., "*Applications of an infrared charge-coupled device Schottky diode array in astronomical instrumentation*", Optical Engineering., Vol. 22, p.334, M/J 1983. [9]

responsible for this type of noise. Generation rate for this type of process is given by [10]

$$U_t = \frac{n_i^2}{N_A \tau_n} \tag{2.8}$$

where,

N_A = doping concentration (cm^{-3}) in the depletion region, and

τ_n = minority carrier lifetime.

The dark currents due to this generation can be quantized as

$$I_b = \frac{q n_i^2 L_n}{N_A \tau_n} \tag{2.9}$$

where,

L_n = diffusion length of minority carriers, and

q = electron charge.

• Significant source of dark current in depletion region is by generation-recombination centers in silicon. When reverse biased, carriers are removed. For this case pn << n_i^2, and to restore equilibrium, carriers have to be generated. The generation rate [11] for this case is given by

$$U_g = \frac{n_i}{2\tau_n}, \text{ where } \tau_n = \frac{1}{\sigma_b \, v_{th} \, N_t} \tag{2.10}$$

In the above equation, σ_b is the capture cross section of the carriers, v_{th} is the thermal velocity of the carriers and N_t is the density of recombination centers at midgap. Current generation in this type of process is given by

$$I = \frac{n_i \, X_d}{2\tau_n}, \tag{2.11}$$

where X_d is the depletion width.

• A similar generation-recombination process as described above, occurs at the interface and it depends on the number of states in the midgap at the interface.

However, at low temperature, the above mentioned sources of dark current tend to be insignificant as compared to the thermionic emission dark current in SBDs described in

the next section.

2.3 SBD DARK CURRENT

The main contribution to the dark current of the SBDs is the internal thermionic emission of carriers over the Schottky barrier [4]. The dark current charge due to these thermally generated carriers is

$$N_{dark} = \frac{J_{sat}(T_d)A_d t_s}{q} \tag{2.12}$$

where,

A_d is active area of the SBD

q is charge of a single carrier

t_s is optical integration time of the focal plane, and

$J_{sat}(T_d)$ is the reverse saturation current density in cm/sec^2.

Reverse saturation dark current density for a PtSi-silicon junction is given by [12]

$$J_{sat}(T_d) = A^* T_d^2 \exp\left[-\frac{q(\psi_{ms} - \psi_{bl})}{KT_d}\right] \tag{2.13}$$

where,

A^* is Richardson constant for holes in p-silicon

Ψ_{ms} is barrier height, and

Ψ_{bl} is barrier lowering voltage.

A study of PtSi SBDs with various anneal times has been reported by Kosonocky et al [4], which shows that the dark current density J_D, is decreased by increasing the anneal time. This maybe due to a more graded PtSi-Si junction being formed and also because the barrier height increases with anneal time. But a disadvantage exists because responsivity tends to decrease with increase in anneal time. This effect is shown in Fig. 2.3 which compares responsivities for anneal times of 10 min and 8 hours. The data for trade-off between Q.E. (or responsivity) and dark currents at the wavelength of 4.1 μm was given by Kosonocky et al [4], and is shown here in Fig. 2.4. The ratio between dark current density and Q.E., can be a good criteria for trade-

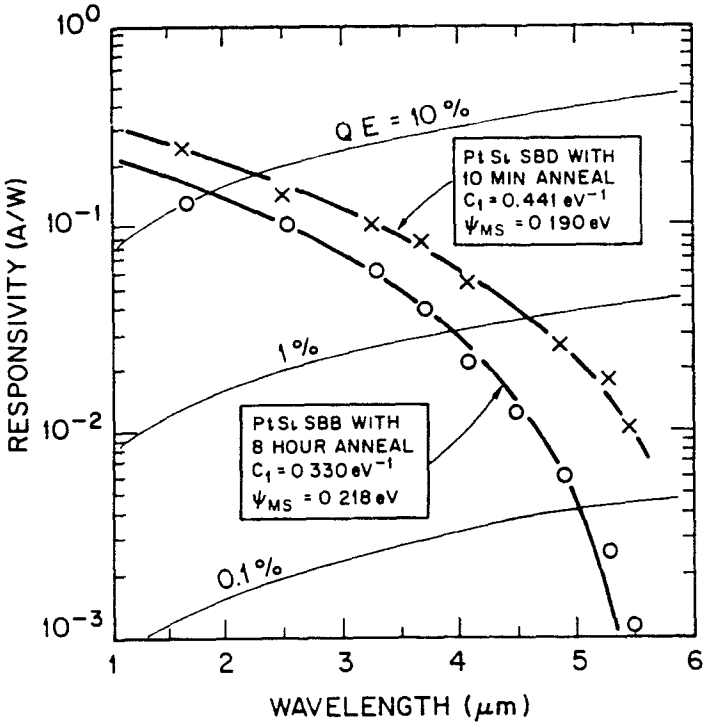


Fig. 2.3. Responsivity v/s Annealing time

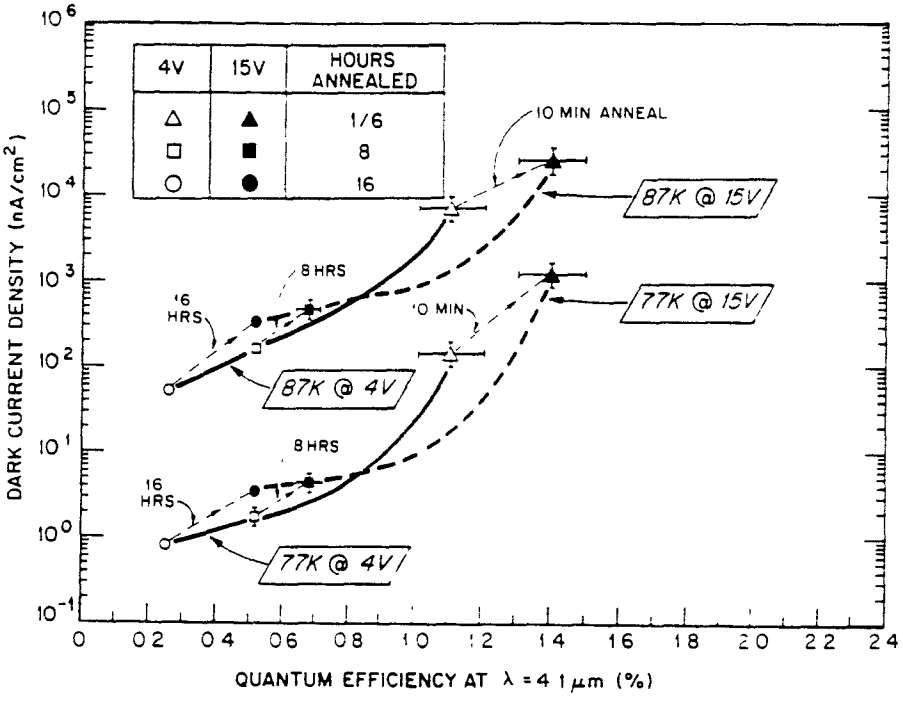


Fig. 2.4. Trade-off between dark currents and responsivity

off and it is a minimum for 8 hour anneal time and increases by only a small amount for the 16-hour anneal time.

2.4 BARRIER LOWERING EFFECT

The workfunction of metal-vacuum system is lowered [11] due to the effect of image force and also due to external electric field applied to the surface. The drop in workfunction is given by

$$\psi_{bl} = \sqrt{\frac{qE}{4\pi\varepsilon_o}} \tag{2.14}$$

The same result applies to PtSi-silicon junction. The effective workfunction of PtSi is reduced as given by above equation, with permittivity of free space replaced by permittivity of silicon and 'E' representing the maximum electric field at the interface. So it is clear that high E-fields at the interface lowers the Schottky barrier height, thereby increasing dark current.

Noise reduction can be achieved by having device structures which have smaller electric fields at the Schottky junction. A more practical way to reduce dark currents is to reduce the temperature of the device, since reverse saturation current density according to Eq (2.13) is a strong function of temperature.

CHAPTER 3

Frame Transfer DSI Imagers

This chapter, presents an analysis of operation of the two possible structures, for frame transfer DSI imager with a 100% fill factor [1, 2]. They are:

1) P^-NP multilayer with a p - channel BCCD on one end of the N-type substrate and a PtSi surface on a p-type layer on the other end, and

2) P^-P multilayer with a p -channel BCCD on one end and a PtSi surface on the other end.

3.1 P^-NP FT IMAGER

The cross-sectional view and the operation of the P^-NP type of FT DSI Imager is shown in Fig. 3.1. It is in a form of a 8 μm thick N-Si substrate with a P^- layer formed on the back side on which PtSi electrode is formed. The front side of the substrate is made P-type by a buried-channel CCD implant, with a dose of 1.3×10^{12} / cm^2, and forms an integral part of the buried-channel CCD readout for photocarriers injected over the Schottky-barrier from the PtSi layer [2, 13]. As shown in Fig. 3.1 optical IR signal falls on the PtSi and the hot holes are injected over the barrier and drift towards the P-channel BCCD. The signal is then clocked out of the imaging site and into the storage site as in a typical frame transfer imager [10, 14].

3.1.1 THEORETICAL ANALYSIS

The following section deals with Poisson solution of the P^-NP structure without free carriers. When a metal is brought into intimate contact with a semiconductor, the conduction and valence bands of the semiconductor are brought into a definite energy relationship with the Fermi level in the metal. Once this relationship is known, it serves as a boundary condition on the solution of Poisson equation in the

semiconductor. So the Schottky junction is incorporated as a boundary condition in the following analysis.

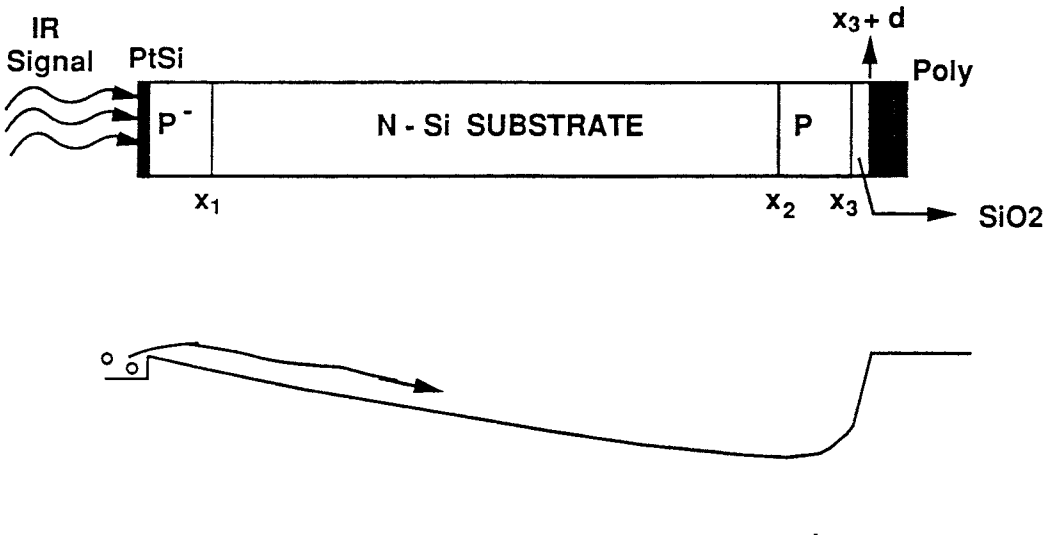


Fig. 3.1. FT DSI Imager with n-substrate

(I) POISSON EQUATION:

The following equations define one dimensional poisson equation in the oxide, P^-, N and the P regions of the structure shown in Fig. 3.1.

$$\frac{\partial^2 \Psi}{\partial x^2} = 0 \quad x_3 < x < x_3 + d \; ; \tag{3.1}$$

$$\frac{\partial^2 \Psi}{\partial x^2} = \frac{qN_a^-}{\varepsilon_s} \quad x_2 < x < x_3 \; ; \tag{3.2}$$

$$\frac{\partial^2 \Psi}{\partial x^2} = -\frac{qN_d}{\varepsilon_s} \quad x_1 < x < x_2 \; ; \tag{3.3}$$

$$\frac{\partial^2 \Psi}{\partial x^2} = \frac{qN_a}{\varepsilon_s} \quad 0 < x < x_1 \; ; \tag{3.4}$$

(II) ELECTRICAL FIELDS:

The electrical field distribution is obtained by integrating equations (3.1) through (3.4). The boundary conditions are as shown below.

$$-\frac{\partial \Psi}{\partial x} = c \quad x_3 < x < x_3 + d \; ; \tag{3.5}$$

$$-\frac{\partial \Psi}{\partial x} = -\frac{qN_a^+ x}{\varepsilon_s} + c_1 \quad x_2 < x < x_3 \; ; \tag{3.6}$$

$$-\frac{\partial \Psi}{\partial x} = \frac{qN_d x}{\varepsilon_s} + c_2 \quad x_1 < x < x_2 \; ; \tag{3.7}$$

$$-\frac{\partial \Psi}{\partial x} = -\frac{qN_a x}{\varepsilon_s} + c_3 \quad 0 < x < x_1 \; ; \tag{3.8}$$

$$B\,C.\ @\ x = x_z \ \rightarrow\ E = 0;$$

$$-\frac{qN_a^+ x_z}{\varepsilon_s} + c_1 = 0;\ therefore\ C_1 = \frac{qN_a^+ x_z}{\varepsilon_s} \; ;$$

$$hence\quad E = \frac{qN_a^+ (x_z - x)}{\varepsilon_s} \quad x_2 < x < x_3 \; ; \tag{3.9}$$

$$B\,C:\ E\ is\ continuous\ @\ x = x_2 \; ;$$

$$\frac{qN_d x_2}{\varepsilon_s} + C_2 = \frac{qN_a^+ (x_z - x_2)}{\varepsilon_s,}\ therefore\ C_2 = \frac{qN_a^+ (x_z - x_2)}{\varepsilon_s} - \frac{qN_d x_2}{\varepsilon_s} \; ;$$

$$hence\quad E = \frac{qN_d (x - x_2)}{\varepsilon_s} + \frac{qN_a^+ (x_z - x_2)}{\varepsilon_s} \quad x_1 < x < x_2 \; ; \tag{3.10}$$

$$B.C:\ E\ is\ continuous@\ x = x_1 \; ;$$

$$-\frac{qN_a x_1}{\varepsilon_s} + c_3 = \frac{qN_d (x_1 - x_2)}{\varepsilon_s} + \frac{qN_a^+ (x_z - x_2)}{\varepsilon_s} \; ;$$

$$therefore\quad C_3 = \frac{qN_d (x_1 - x_2)}{\varepsilon_s} + \frac{qN_a^+ (x_z - x_2)}{\varepsilon_s} + \frac{qN_a x_1}{\varepsilon_s} \; ;$$

$$hence \quad E = \frac{qN_a\,(x_1 - x)}{\varepsilon_s} + \frac{qN_d\,(x_1 - x_2)}{\varepsilon_s} + \frac{qN_a^+\,(x_z - x_2)}{\varepsilon_s} \qquad 0 < x < x_1\,; \qquad (3.11)$$

(III) POTENTIAL FIELDS:

Potential fields are got by integrating the E.field equations because

$$E = -\frac{\partial \Psi}{\partial x}\,;$$

The potentials can be solved by integratıng equations (3.9) through (3.11) and by applying appropriate boundary conditions.

$$\Psi = \frac{qN_a\,x^2}{2\,\varepsilon_s} - \frac{qN_a^+\,x_z\,x}{\varepsilon_s} + C_1 \qquad x_2 < x < x_3\,; \qquad (3.12)$$

$$\Psi = \frac{qN_a^+\,(x_2 - x_z)x}{\varepsilon_s} + \frac{qN_d\,x_2\,x}{\varepsilon_s} - \frac{qN_d\,x^2}{2\,\varepsilon_s} + c_2 \qquad x_1 < x < x_2\,; \qquad (3.13)$$

$$\Psi = \left[\frac{qN_d\,(x_2 - x_1)}{\varepsilon_s} + \frac{qN_a^+\,(x_2 - x_z)}{\varepsilon_s}\right] x - \frac{qN_a\,x_1\,x}{\varepsilon_s} + \frac{qN_a\,x^2}{2\,\varepsilon_s} + c_3$$

$$\text{for } 0 < x < x_1\,; \qquad (3.14)$$

$$B\,C\colon\ \Psi\,(x = 0) = \Psi_{ms} \qquad therefore \qquad c_3 = \Psi_{ms}\,,$$

Placing the constant value in Eq (3.14) gıves potential in P^- regıon as:

$$\Psi \;=\; \left[\frac{qN_d\,(x_2 - x_1)}{\varepsilon_s} + \frac{qN_a^+\,(x_2 - x_z)}{\varepsilon_s}\right] x - \frac{qN_a\,x_1\,x}{\varepsilon_s} + \frac{qN_a\,x^2}{2\,\varepsilon_s} + \Psi_{ms}$$

$$\text{for } 0 < x < x_1\,; \qquad (3.15)$$

$$B\,C\colon\ Continuity\ of\ potential\ @\ x = x_1\,;$$

$$\frac{qN_a^+\,(x_2 - x_z)\,x_1}{\varepsilon_s} + \frac{qN_d\,x_2\,x_1}{\varepsilon_s} - \frac{qN_d\,x_1^2)}{2\,\varepsilon_s} + c_2 =$$

$$\frac{qN_d\,(x_2 - x_1)\,x_1}{\varepsilon_s} + \frac{qN_a^+\,(x_2 - x_z)\,x_1}{\varepsilon_s} - \frac{qN_a\,x_1^2}{2\,\varepsilon_s} + \Psi_{ms}\,;$$

$$\textit{therefore} \quad c_2 = \Psi_{ms} - \frac{qN_a\, x_1^2}{2\,\varepsilon_s} - \frac{qN_d\, x_1^2}{2\,\varepsilon_s} = \Psi_{ms} - \frac{qx_1^2\,(N_a + N_d)}{2\,\varepsilon_s} \;;$$

Placing the constant value in Eq (3.13) gives potential in N-region as:

$$\Psi = \frac{qN_a^+\,(x_2 - x_z)\,x}{\varepsilon_s} + \frac{qN_d\, x_2\, x}{\varepsilon_s} - \frac{qN_d\, x^2}{2\,\varepsilon_s} - \frac{qx_1^2\,(N_a + N_d)}{2\,\varepsilon_s} + \Psi_{ms}$$

$$\text{for } x_1 < x < x_2 \;; \tag{3.16}$$

$$B\,C\text{: } \textit{Potential is continuous @ } x = x_2 \;;$$

$$\frac{qN_a^+\, x_2^2}{2\,\varepsilon_s} - \frac{qN_a^+\, x_z\, x_2}{2\,\varepsilon_s} + c_1 =$$

$$\frac{qN_a^+\,(x_2 - x_z)\,x_2}{\varepsilon_s} + \frac{qN_d\, x_2^2}{2\,\varepsilon_s} - \frac{qx_1^2\,(N_a + N_d)}{2\,\varepsilon_s} - \Psi_{ms} \;;$$

$$\textit{therefore} \quad c_1 = \frac{qN_a^+\, x_2^2}{2\,\varepsilon_s} + \frac{qN_d\,(x_2^2 - x_1^2)}{2\,\varepsilon_s} - \frac{qN_a\, x_1^2}{2\,\varepsilon_s} + \Psi_{ms} \;;$$

Placing the constant value in Eq (3.12) gives potential in p-region as:

$$\Psi = \frac{qN_a^+\,(x^2 + x_2^2)}{2\,\varepsilon_s} - \frac{qN_a^+\, x_z\, x}{\varepsilon_s} + \frac{qN_d\,(x_2^2 - x_1^2)}{2\,\varepsilon_s} - \frac{qN_a\, x_1^2}{2\,\varepsilon_s} + \Psi_{ms}$$

$$\text{for } x_2 < x < x_3 \;; \tag{3.17}$$

Since all potentials are in terms of x_z, we need another boundary condition. This can be as follows:

$$B\,C\text{: } \textit{potential} \quad \Psi = (V_g - V_{ox}) \quad @ \; x = x_3 \;; \; \textit{where } V_{ox} = \frac{qN_a^+\,(x_3 - x_z)}{Cox} \;;$$

$$\frac{qN_a^+\,(x_3^2 + x_2^2)}{2\,\varepsilon_s} - \frac{qN_a^+\, x_z\, x_3}{\varepsilon_s} + \frac{qN_d\,(x_2^2 - x_1^2)}{2\,\varepsilon_s} - \frac{qN_a\, x_1^2}{2\,\varepsilon_s} + \Psi_{ms}$$

$$= V_g - \frac{qN_a^+ (x_3 - x_z)}{Cox} ;$$

From above equation we obtain the value of channel depth as measured from the Schottky surface.

$$x_z = \frac{\frac{qN_a^+ (x_3^2 + x_2^2)}{2\,\varepsilon_s} + \frac{qN_d\,(x_2^2 - x_1^2)}{2\,\varepsilon_s} - \frac{qN_a\,x_1^2}{2\,\varepsilon_s} + \frac{qN_a^+ x_3}{Cox} - (V_g - \Psi_{ms})}{\left[\frac{qN_a^+}{Cox} + \frac{qN_a^+ x_3}{\varepsilon_s}\right]} \qquad (3.18)$$

This P⁻NP structure which was simulated in SUPREM III, had an n-type silicon <100> silicon substrate of resistivity 100 Ω.cm and thickness of about 8 μm. Concentration of the p-layer was taken as 1.858e16, 1.44e16, 1.08e16 and 0.928e16 / cm^3, for thickness corresponding to 0.7, 0.9, 1.2 and 1.4 μm respectively to keep the total doping density per unit area to 1.3e12 / cm^2. Empty well channel potentials found from simulations are compared to that obtained theoretically in Table 3.1. It is clear that the simulation results are in good agreement with the theory, in the linear region but cannot predict the pinning effect due to accumulation of electrons in the P-layer [4, 15].

P⁻NP STRUCTURE								
gate	**Vz(0.7μm)**		**Vz(0.9μm)**		**Vz(1.2)μm)**		**Vz(1.4μm)**	
voltage	*suprem*	*theory*	*suprem*	*theory*	*suprem*	*theory*	*suprem*	*theory*
0.0	-11.443	-11.32	-12.938	-12.79	-15.168	-14.97	-16.658	-16.44
1.0	-10.543	-10.42	-12.049	-11.90	-14.297	-14.10	-15.799	15.78
2.0	-9.643	-9.51	-11.164	-11.01	-13.427	-13.23	-14.94	-14.72
3.0	-8.744	-8.61	-10.278	-10.12	-12.56	-12.37	-14.081	-13.86
4.0	-7.845	-7.71	-9.393	-9.24	-11.691	-11.50	-13.223	-13.00
5.0	-6.946	-6.81	-8.509	-8.35	-10.826	-10.63	-12.638	-12.15
6.0	-6.489	-5.91	-8.125	-7.46	-10.516	-9.76	-12.089	-11.29
7 0	-6.464	-5.01	-8.101	-6.58	-10.488	-8.89	-12.069	-10.43
***	*Vz(pinning)*		*Vz(pinning)*		*Vz(pinning)*		*Vz(pinning)*	
***	*-6.5*		*-8.1*		*-10.5*		*-12.1*	

TABLE (3.1) Verification of theoretical results

3.1.2 SINGLE CARRIER TRANSIT TIME

A single carrier transit time has been used to describe the free charge transfer in CCD elements [16]. It is the time a single carrier would require to drift from one end to the other of the electrode under the influence of fringing fields. In the case of the 3-D structure, it is the time for carrier to traverse from the PtSi surface to the BCCD channel region and represents the response time of the DSI photodetector structure. According to J. E. Carnes and W. F. Kosonocky [16], single carrier transit time is defined by

$$\tau_r = \frac{1}{\mu} \int_{x=0}^{x=x_3} \frac{dx}{E_f(x)} \tag{3.19}$$

From the simulations it was seen that channel was formed very close to the interface of the N-P layers. So single carrier transit time, is mostly defined by the time taken to traverse from the PtSi surface to the interface of the N-P layers. From Eqs (3.10) and (3.11), the electric fields for P^-NP structure are

$$E = \frac{qN_a\ (x_1 - x)}{\varepsilon_s} + \frac{qN_d\ (x_1 - x_2)}{\varepsilon_s} + \frac{qN_a^+\ (x_z - x_2)}{\varepsilon_s}, \quad 0 < x < x_1$$

$$E = \frac{qN_d\ (x - x_2)}{\varepsilon_s} + \frac{qN_a^+\ (x_z - x_2)}{\varepsilon_s}; \quad x_1 < x < x_2$$

The single carrier transit time can be split into two terms τ_{r_1} and τ_{r_2}

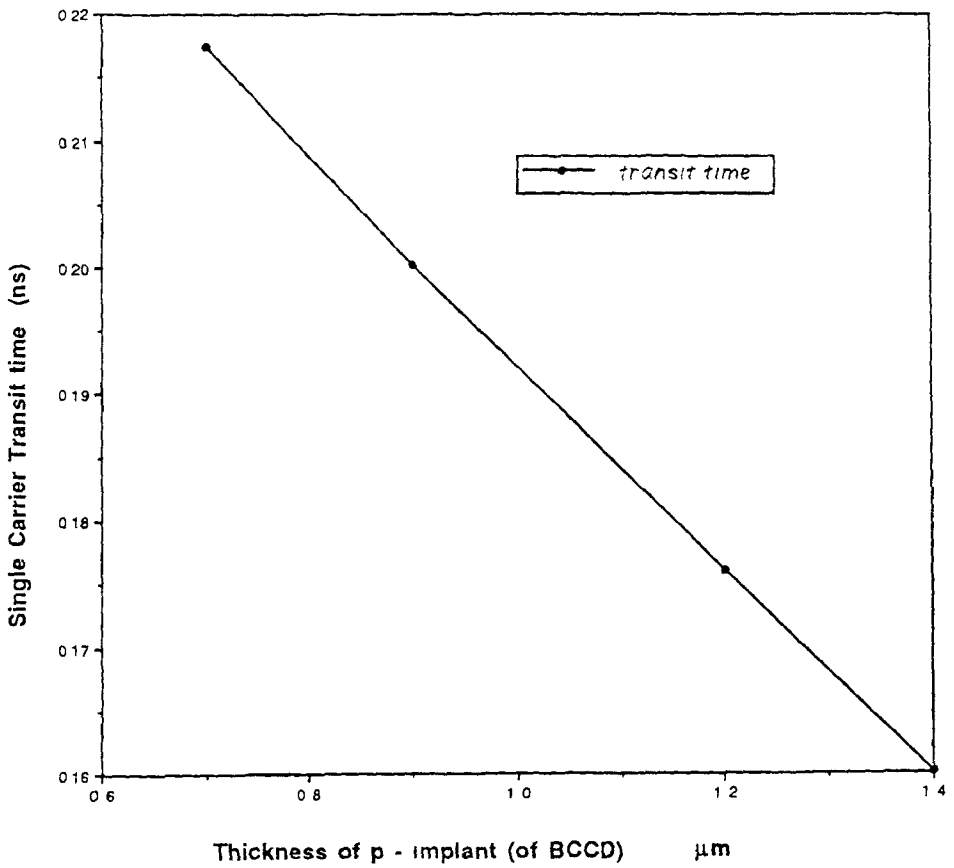
$$\tau_{r_1} = \frac{1}{\mu} \int_{x=0}^{x=x_1} \frac{\varepsilon_s\ dx}{q\left\{N_d\ (x_1 - x_2) + N_a^+\ (x_z - x_2) + N_a x_1\right\} - qN_a x}$$

$$= \frac{\varepsilon_s}{q\mu N_a} \int_{x=x_1}^{x=0} \frac{dx}{x - \left\{x_1 + \frac{N_d}{N_a}\ (x_1 - x_2) + \frac{N_a^+}{N_a}\ (x_z - x_2)\right\}}$$

TABLE (3.2) Single Carrier Transit Time in P⁻NP Imager

'P' thickness	τ_{tr1} (P^- region)	τ_{tr2} (N-region)	τ_{tr}
0.7 μm	0.0272 ns	0.1903 ns	0.2175 ns
0.9 μm	0.0256 ns	0.1746 ns	0.2002 ns
1.2 μm	0.0292 ns	0.1469 ns	0.1762 ns
1.4 μm	0.0338 ns	0.1263 ns	0.1601 ns

Fig 3.2 Single carrier transit time for P^- NP structure



$$\tau_{r_1} = \frac{\varepsilon_s}{q\mu N_a} \left\{ \ln |K| - \ln |x_1 - K| \right\}; \tag{3.20}$$

$$\text{where } K = x_1 + \frac{N_d}{N_a}(x_1 - x_2) + \frac{N_a^+}{N_a}(x_z - x_2)$$

$$\tau_{r_2} = \frac{1}{\mu} \int_{x_1}^{x_2} \frac{\varepsilon_s \, dx}{q\left\{N_a^+ (x_z - x_2) - N_d x_2\right\} + qN_d x}$$

$$= \frac{\varepsilon_s}{q\mu N_d} \int_{x_1}^{x_2} \frac{dx}{x + \left\{\frac{N_a^+}{N_d}(x_z - x_2) - x_2\right\}}$$

$$\tau_{r_2} = \frac{\varepsilon_s}{q\mu N_d} \left\{ \ln |x_2 + K_1| - \ln |x_1 + K_1| \right\}; \quad \text{where } K_1 = \frac{N_a^+}{N_d}(x_z - x_2) - x_2 \tag{3.21}$$

Hence for the P$^-$NP structure, single carrier transit time is given by

$$\tau_r = \tau_{r_1} + \tau_{r_2} \tag{3.22}$$

In the calculations, μ defines mobility of holes. It was estimated [11] from the doping of the 'P' and 'N' regions. Table 3.2, shows the single carrier transit time in 'P$^-$' and 'N' regions seperately. It is clear that the transit time through the 'P$^-$'region is about 10 times less than that through the 'N' region. So increasing 'P$^-$' region doping will not have a significant effect on the transit time. On the other hand, single carrier transit time decreases as the doping of 'N' region increases. Single carrier transit time as a function of p-layer thickness (same as thickness of 'P$^-$'), is shown in Fig. 3.2. It decreases as the thickness of p-channel implant increases due to the reason that channel potential is more negative for thicker p-implants.

3.2 P$^-$P FT IMAGER

The main potential problem with the P$^-$NP type FT DSI image structure is that the P$^-$ implant is necessary to form a Schottky-barrier on a p-substrate. A layer of Pt is

deposited and sintered to form a PtSi layer. From processing point of view, it may not be possible to create a graded PtSi-silicon junction. This can be avoided by a simpler P⁻P FT DSI structure illustrated in Fig. 3.3 [13].

A bulk p-silicon with a PtSi Schottky junction on one end and a regular MOS structure on the other, would have a potential minimum approximately in the middle. But in regular practise, the bulk could be thinned upto about 10 μm, and if the signal is at the center of the bulk, large gate voltages are needed to clock out the signal. So a p-implant with a higher concentration compared to that of the substrate is used, which results in the potential minimum being closer to the oxide surface.

3.2.1 THEORETICAL ANALYSIS

In this section, poisson solution of the P⁻P structure shown in Fig. 3.3 is carried out. Analysis is carried out in a similar manner as was done for the P⁻NP Imager. Expressions are derived for channel potentials and depth of the channel.

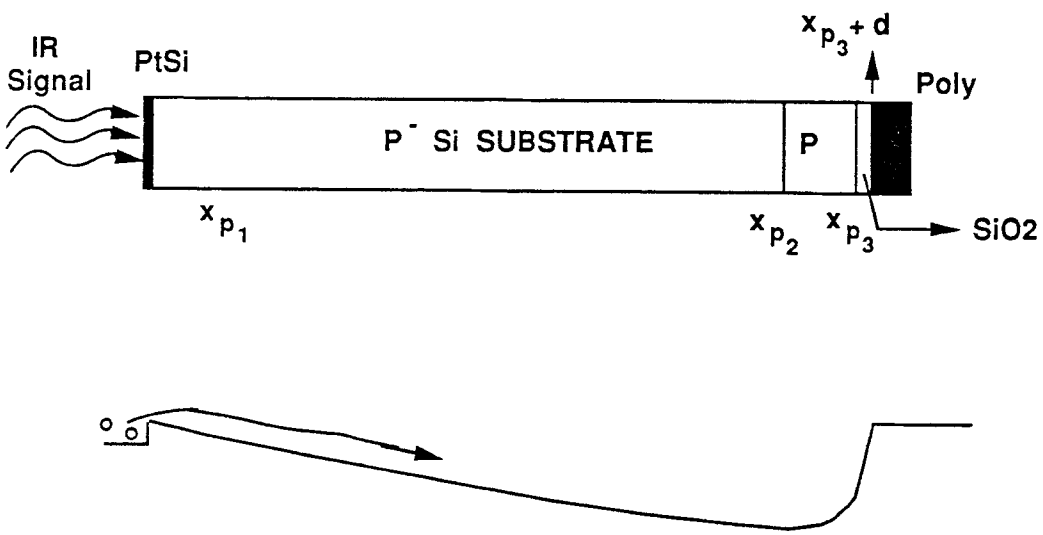


Fig. 3.3. FT DSI Imager with p-substrate

(I) POISSON EQUATION:

The standard equations are written for the P^-, P and the oxide regions of the structure shown in Fig. 3.3.

$$\frac{\partial^2 \Psi}{\partial x^2} = 0 \quad x_{p_2} < x < x_{p_2} + d \; ; \tag{3.23}$$

$$\frac{\partial^2 \Psi}{\partial x^2} = \frac{qN_a^+}{\varepsilon_s} \quad x_{p_1} < x < x_{p_2} \; ; \tag{3.24}$$

$$\frac{\partial^2 \Psi}{\partial x^2} = \frac{qN_a}{\varepsilon_s} \quad 0 < x < x_{p_1} \; ; \tag{3.25}$$

(II) ELECTRICAL FIELDS:

The electrical fields are got by integrating equations (3.23) through (3.25), using appropriate boundary conditions.

$$-\frac{\partial \Psi}{\partial x} = c \quad x_{p_2} < x < x_{p_2} + d \; ; \tag{3.26}$$

$$-\frac{\partial \Psi}{\partial x} = -\frac{qN_a^+ x}{\varepsilon_s} + c_1 \quad x_{p_1} < x < x_{p_2} \; ; \tag{3.27}$$

$$-\frac{\partial \Psi}{\partial x} = -\frac{qN_a x}{\varepsilon_s} + c_2 \quad 0 < x < x_{p_1} \; ; \tag{3.28}$$

$$B.C: \; E = 0 \; @ \; x = x_z \; ;$$

$$-\frac{qN_a^+ x_z}{\varepsilon_s} + c_1 = 0 \quad therefore \; c_1 = \frac{qN_a^+ x_z}{\varepsilon_s} \; ;$$

Placing the constant value in Eq (3.27) gives E-field in the p-region.

$$E = \frac{qN_a^+ (x_z - x)}{\varepsilon_s} \quad x_{p_1} < x < x_{p_2} \; ; \tag{3.29}$$

$$B.C:\ E \text{ is continuous } @\ x = x_{p_1}\ ;$$

$$-\frac{qN_a^+ x_{p_1}}{\varepsilon_s} + \frac{qN_a^+ x_z}{\varepsilon_s} = -\frac{qN_a\ x_{p_1}}{\varepsilon_s} + c_2\ ;$$

$$therefore \quad c_2 = \frac{qN_a^+ (x_z - x_{p_1})}{\varepsilon_s} + \frac{qN_a\ x_{p_1}}{\varepsilon_s}\ ;$$

Placing the constant value in Eq (3.28) gives E-field in the P^- region.

$$E = \frac{qN_a\ (x_{p_1} - x\ )}{\varepsilon_s} + \frac{qN_a^+ (x_z - x_{p_1})}{\varepsilon_s} \qquad 0 < x < x_{p_1}\ ; \tag{3.30}$$

(III) POTENTIAL FIELDS:

The potential fields are obtained by integrating E-field and the boundary conditions like continuity, are applied.

$$\Psi = -\int E\ dx = cx + d \qquad x_{p_2} < x < x_{p_2} + d\ ; \tag{3.31}$$

$$\Psi = \frac{qN_a^+ x^2}{2\ \varepsilon_s} - \frac{qN_a^+ x_z\ x}{\varepsilon_s} + c_1 \qquad x_{p_1} < x < x_{p_2}\ ; \tag{3.32}$$

$$\Psi = \frac{qN_a\ x^2}{2\ \varepsilon_s} + \left[x_{p_1} \left\{ \frac{qN_a^+}{\varepsilon_s} - \frac{qN_a}{\varepsilon_s} \right\} - \frac{qN_a^+ x_z}{\varepsilon_s} \right] x + c_2 \qquad 0 < x < x_{p_1}\ ; \tag{3.33}$$

$$B.C:\ \Psi\ (x = 0) = \Psi_{ms} = barrier\ height\ of\ PtSi = 0.22\ ev\ ;\ hence\ \ c_2 = \Psi_{ms}\ ;$$

Placing the value of the constant in Eq (3.33) we get potential distribution in the P-region.

$$\Psi = \frac{qN_a\ x^2}{2\ \varepsilon_s} + \left[x_{p_1} \left\{ \frac{qN_a^+}{\varepsilon_s} - \frac{qN_a}{\varepsilon_s} \right\} - \frac{qN_a^+ x_z}{\varepsilon_s} \right] x + \Psi_{ms} \qquad 0 < x < x_{p_1}\ ; \tag{3.34}$$

$$B.C:\ Potential\ is\ continuous\ @\ x = x_{p_1}\ ;$$

$$\frac{qN_a^+ x_{p_1}^2}{2\varepsilon_s} + c_1 = \frac{qN_a x_{p_1}^2}{2\varepsilon_s} + \frac{qN_a^+ x_{p_1}^2}{\varepsilon_s} - \frac{qN_a x_{p_1}^2}{\varepsilon_s} + \Psi_{ms}$$

$$therefore \quad c_1 = \frac{q x_{p_1}^2 (N_a^+ - N_a)}{2\varepsilon_s} + \Psi_{ms} \; ;$$

Placing the value of constant in Eq (3.32) we get potential distribution in the p-region.

$$\Psi = \frac{qN_a^+ x^2}{2\varepsilon_s} - \frac{qN_a^+ x_z x}{\varepsilon_s} + \frac{q x_{p_1}^2 (N_a^+ - N_a)}{2\varepsilon_s} + \Psi_{ms} \quad x_{p_1} < x < x_{p_2} \; ; \tag{3.35}$$

The value X_z is needed determine the potential fields.

$$B\,C: \; \Psi = V_g - V_{ox} \quad @ \; x = x_{p_2} \; ; \; where \; V_{ox} = \frac{qN_a^+ (x_{p_2} - x_z)}{Cox} \; ;$$

$$\frac{qN_a^+ x_{p_2}^2}{2\varepsilon_s} + \frac{q x_{p_1}^2 (N_a^+ - N_a)}{2\varepsilon_s} + \Psi_{ms} - V_g + \frac{qN_a^+ x_{p_2}}{Cox} = \left[\frac{qN_a^+ x_p sub 2}{\varepsilon_s} + \frac{qN_a^+}{Cox} \right] x_z \; ,$$

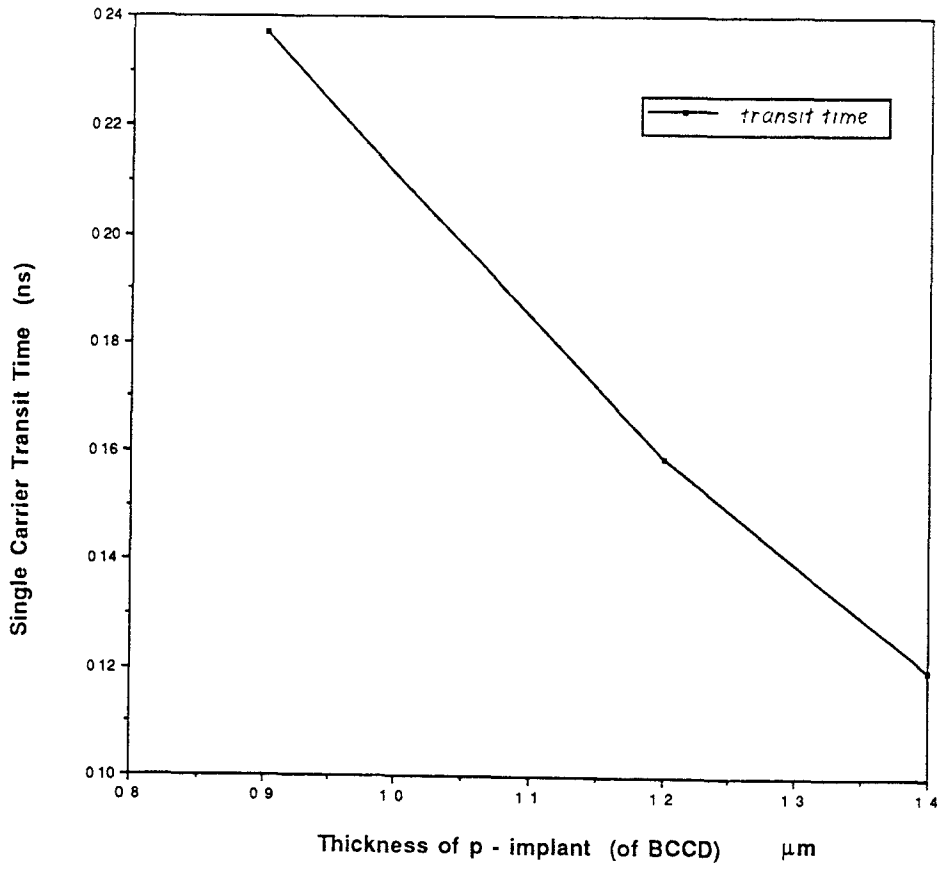
$$therefore \quad X_z = \frac{\left[\frac{qN_a^+ x_{p_2}^2}{2\varepsilon_s} + \frac{q x_{p_1}^2 (N_a^+ - N_a)}{2\varepsilon_s} + \frac{qN_a^+ x_{p_2}}{Cox} - (V_g - \Psi_{ms}) \right]}{qN_a^+ \left[\frac{x_{p_2}}{\varepsilon_s} + \frac{1}{Cox} \right]} \tag{3.36}$$

The P+P FT DSI structure was simulated in SUPREM III, using a p-type silicon <100> substrate of 1.5e14 / cm^3 which corresponds to 100 Ω.cm. The values obtained from this analysis are compared with the simulation results in Table 3.3. It comes out that there is a good match between the theoretical and simulation results, in the linear region of the Vg vs Vz curve. But since pinning is a device phenomena, this analysis does not account for it.

TABLE (T 3.3) Verification of theoretical results.

P⁻P STRUCTURE								
gate	Vz(0.7μm)		Vz(0.9μm)		Vz(1.2)μm)		Vz(1.4μm)	
voltage	*suprem*	*theory*	*suprem*	*theory*	*suprem*	*theory*	*suprem*	*theory*
0.0	-12.389	-12.25	-13.997	-13.83	-16.341	-16.13	-17.875	-17.63
1.0	-11.498	-11.36	-13.123	-12.96	-15.492	-15.28	-17.041	-16.80
2.0	-10.607	-10.47	-12.251	-12.08	-14.644	-14.43	-16.208	-15.96
3.0	-9.717	-9.58	-11.378	-11.21	-13.797	-13.58	-15.376	-15.13
4.0	-8.827	-8.69	-10.507	-10.34	-12.949	-12.74	-14.544	-14.30
5.0	-7.938	-7.80	-9.635	-9.47	-12.104	-11.89	-13.713	-13.47
6.0	-7.228	-6.91	-9.012	-8.59	-11.579	-11.05	-13.238	-12.64
7 0	-7.187	-6.03	-8.977	-7.73	-11.551	-10.20	-13.212	-11.81
***	*Vz(pinning)*		*Vz(pinning)*		*Vz(pinning)*		*Vz(pinning)*	
***	*-7.15*		*-8.95*		*-11.52*		*-13.18*	

Fig 3.4 Single carrier transit time for P⁻P structure



3.2.2 SINGLE CARRIER TRANSIT TIME

In the case of P⁻P structure, single carrier transit time is approximately equal to the time needed for a single carrier to traverse from PtSi surface to the P⁻-P interface. This is so because the channel is very close to the P⁻-P interface.

From Eq (3.30), the electric field is given by

$$E = \frac{qN_a\,(x_{p_1} - x)}{\varepsilon_s} + \frac{qN_a^+\,(x_z - x_{p_1})}{\varepsilon_s}; \quad 0 < x < x_{p_1}$$

$$\text{single carrier rise time } \tau_r = \frac{1}{\varepsilon_s} \int_{x=0}^{x=x_{p_1}} \frac{\varepsilon_s\, dx}{q\left\{N_a x_{p_1} + N_a^+ (x_z - x_{p_1})\right\} - qN_a x}$$

$$\tau_r = \frac{\varepsilon_s}{q\mu N_a} \int_{x=x_{p_1}}^{x=0} \frac{dx}{x - K_2}, \quad \text{where } K_2 = x_{p_1} + \frac{N_a^+}{N_a}(x_z - x_{p_1})$$

$$\tau_r = \frac{\varepsilon_s}{q\mu N_a} \left\{\ln \mid K_2 \mid - \ln \mid x_{p_1} - K_2 \mid\right\} \tag{3.37}$$

Single carrier transit time is plotted in Fig. 3.4, and it decreases as P-layer thickness increases, due to the same reason that channel potentials are more negative for thicker p-layer implants. Single carrier transit time of the P⁻P structure, is almost the same as that in P⁻NP case. So in this regard there is no distinct advantage using P⁻P structure.

CHAPTER 4

1-D Simulations of FT DSI Imagers

Frame transfer imagers are one of the basic area imaging array organizations employing seperate sensing and storing sites [17]. Light is incident on the active sensing region, thus generating the charge carriers. Charge in the imaging area is then transfered to storage area during vertical retrace time. During horizontal blanking time, the pattern moves downward into horizontal registers by one line, from where the signal is clocked out. A 3-D DSI FT imager can be made by constructing a p-channel BCCD on one side and a PtSi surface at the other side of a thin P^-NP or P^-P substrate. For this purpose. a P-implant on a thinned n-type <100> silicon substrate is used to form a BCCD channel. In addition a P^- implant is required at the PtSi junction to form a Schottky-barrier detector. As mentioned in Chapter 2, Schottky junction on n-type silicon yields larger barrier heights and a shorter cutoff wavelength that permits operation only in the visible region. For this reason, an additional p-implant is needed at the PtSi junction to produce a Schottky-barrier of about 0.22 ev that makes the SBD surface sensitive in the infrared wavelength range of 1 to 5 μm. Very thin substrates are not self supporting and tend to be wavy, but substrates with thickness around 20 μm are self supporting [13], therefore, there is advantage to use very low doped substrate made about 20 μm thick. In the next section, a P^-NP DSI imager with substrate thickness of about 18 μm is simulated. NJIT-CDI, a modified version of SUPREM III's Poisson solver [18], which is capable of providing semi-automated information on 1-D simulations was used to analyze the DSI structure. A special feature of this program is that carrier profiles can be plotted, which enables us to see whether the charge reaches the surface or not. This is crucial in any imaging device which has a BCCD structure to transfer the signal from imaging site to readout site, because imagers with signal

flowing at the surface tend to be noisy due to trapping by the surface states.

Although SUPREM III does not have the material PtSi defined, Aluminum metal was selected and its workfunction was set to give a barrier height same as that of PtSi (0.22 ev). The barrier height of a metal - semiconductor junction (ϕ_{bp}) is given by:

$$\Phi_{bp} = E_g - (W_f - \chi) \tag{4.1}$$

where,

E_g = band gap of silicon

W_f = workfunction of the metal, and

χ = electron affinity of silicon material.

The energy gap of silicon at 77 K was calculated to be 1.166 ev according to the relationship:

$$E_g(T) = 1.17 - \frac{(4.73 * 10^{-4})\, T^2}{T + 636} \tag{4.2}$$

4.1 P⁻NP FT IMAGER

In the simulation procedure, P^- <100> silicon layer was deposited on aluminum, to represent a Schottky contact upon which n-type silicon substrate is deposited. A P-layer is implanted with a dose of 1.0e12 /cm^2 and an energy of 150 Kev. It is then diffused, for 200 seconds at a temperature of 950 ^{o}C. In practise, the Schottky contact and the BCCD implants are grown from either ends of the silicon substrate. In order to get the potential profiles with zero signal, the P^-NP structure has to be depleted completely. The electron and hole densities are expressed by

$$n = n_i \exp \frac{\psi - \psi_f}{kT} \tag{4.3}$$

$$p = n_i \exp \frac{\psi_f - \psi}{kT} \tag{4.4}$$

So to simulate empty wells, quasi-Fermi level (for holes) in P-type regions is fixed to a negative value and in case of N-type regions (for electrons) quasi-Fermi level is fixed to a high positive value. It was seen during simulations that considerable amount

of holes were present in the N-region. So the quasi-Fermi for minority carriers (holes) was also fixed to a negative value. The actual electrical file used for the simulations is shown in Appendix B. Once there are no flat regions in the potential profile, it is clear that the structure is completely depleted.

Gate voltage on the polysilicon is varied keeping the PtSi contact at zero potential. The channel potential in each step is found from the electrical output file created by SUPREM III, which determines the minimum potential in the silicon region. Empty potential-well profiles as a function of gate voltages is shown in Fig. 4.1, for the case P-layer thickness = 1.0μm. Channel voltage increases as gate voltage increases and then becomes pinned. The pinning represents the least negative BCCD potential at which the p-layer becomes pinned by the inversion layer of electrons formed at the Si-SiO_2 interface [15, 19]. The operation range of the BCCD gates could be from 0 to 5 V, because negative gate potentials gives rise to deeper wells which in turn results in large electric fields at the Schottky junction.

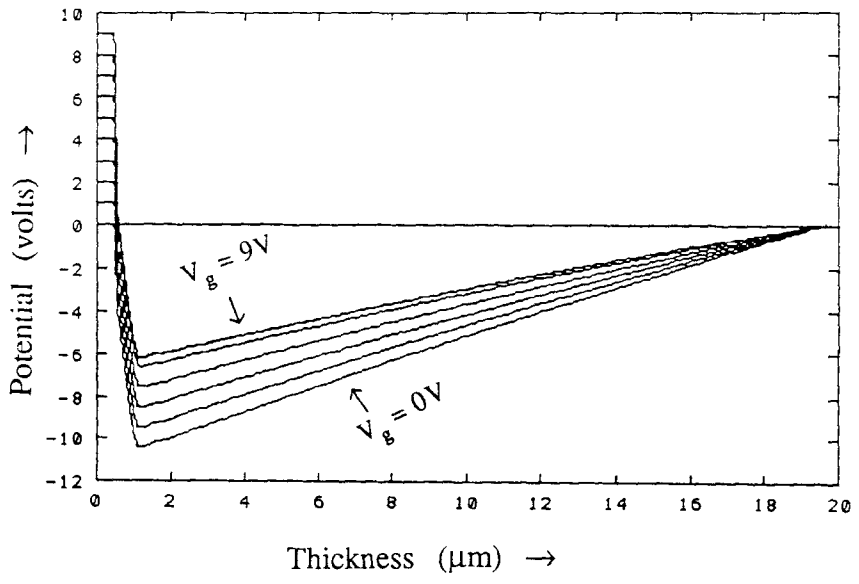


Fig. 4.1. Empty well potential profiles for FT-DSI P'NP imager as function of gate voltage

According to Eq (4.4), charge filling can be simulated by increasing the quasi-Fermi level of holes in the P-layer. Potential profiles tend to become flat as the well gets filled up with charge. The profiles are shown in Fig. 4.2 for the P-layer thickness of 1.0 μm. Hole carrier profile is shown in Fig. 4.3 is computed for the same operation as shown in Fig. 4.2. But the quasi-Fermi potential was increased till the channel potential was equal to the value at pinning for empty wells.

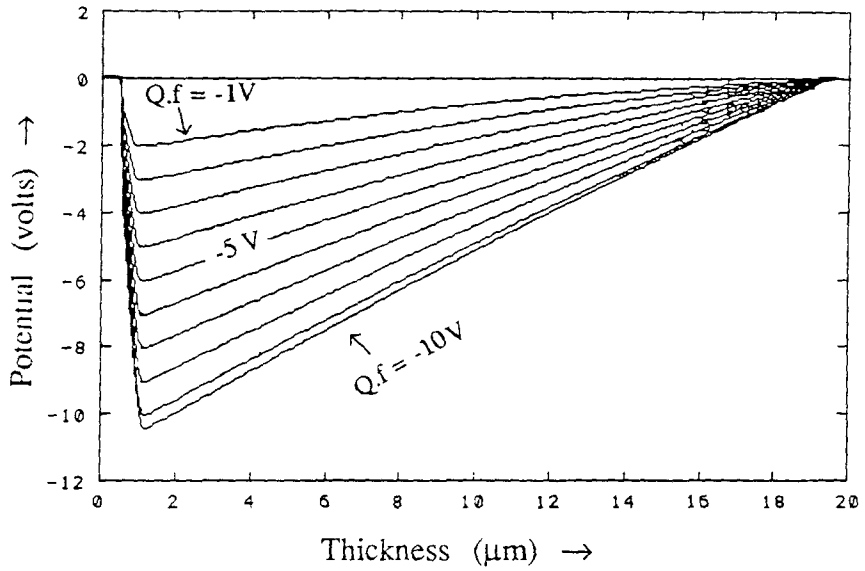


Fig. 4.2. Potential profiles as function of charge signal in the P⁻NP FT-DSI imager

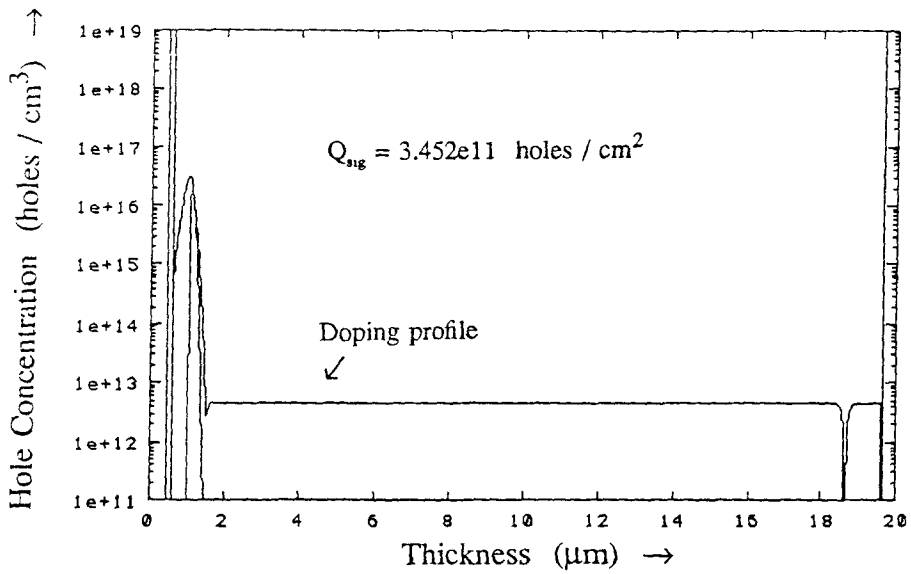


Fig. 4.3. Hole carrier profile corresponding to channel voltage being equal to that at pinning for empty wells

To find the charge handling capacity of the structure, hole quasi-Fermi potential is increased till the charge reaches the surface / pinning occurs (whichever occurs first). For comparision sake, charge handling capacities were found for a specific gate voltage i.e., zero volts. Depth of the P-layer was increased by increasing the drive-in temperature. As expected, charge handling capacities decrease with increase in depth, which indicates that thinner P-implants are better. But simulations have shown that deeper implants reduced the channel potentials and henceforth reduced the electric fields at the Schottky junction. Figure 4.4 shows the variation of charge handling capacity in holes / sq.cm, as a function of depth of P-layer implant.

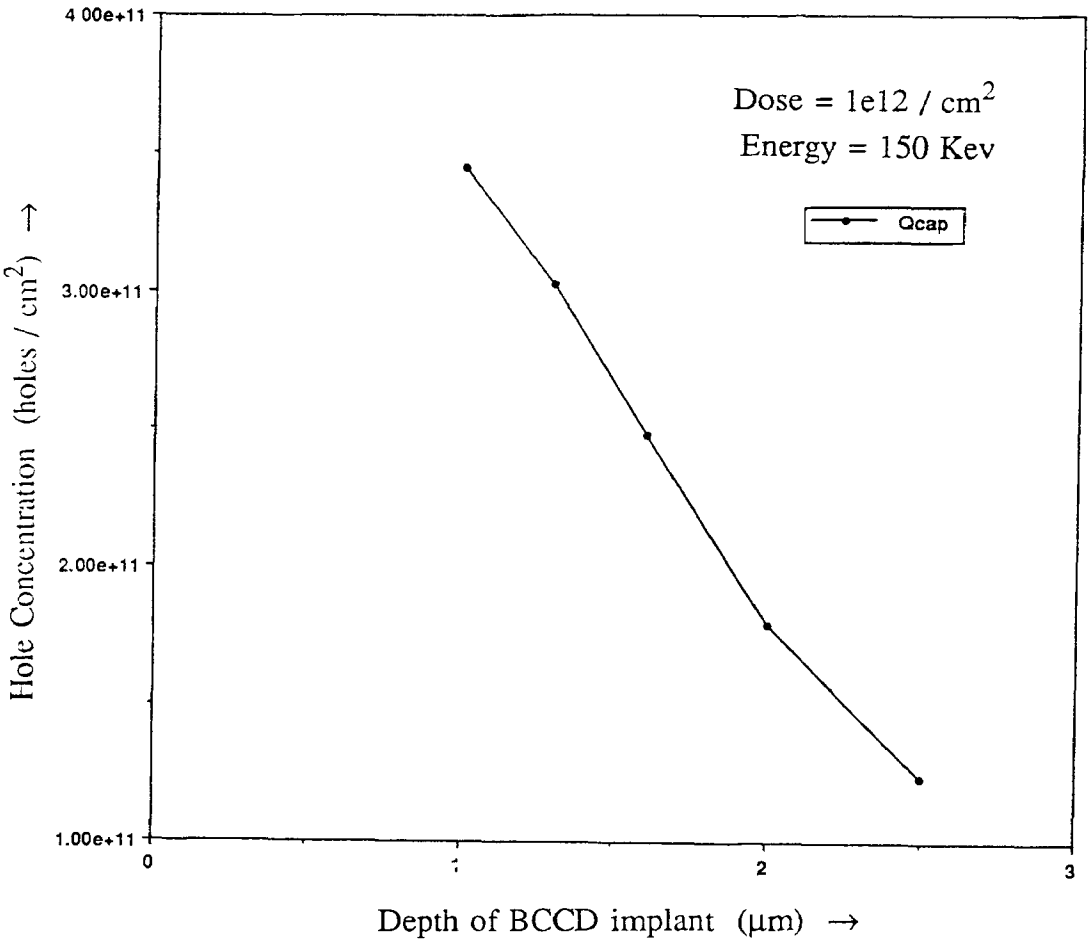


Fig. 4.4. Charge handling capacity as function of Depth of the BCCD implant for P⁻NP FT-DSI imager

A similar study was done by varying the energy during implantation. For low energies, charge handling capacities were smaller but the smaller negative channel potentials had smaller electric fields at the metal-semiconductor junction. Large electric fields are to be avoided because tend to they reduce the barrier height thus increasing dark currents. Figure 4.5 shows the gate voltage vs channel voltage for different implant energy levels of 120, 150 and 180 Kev. Diffusion temperatures were varied in each case to keep the implant depth constant at 1 μm.

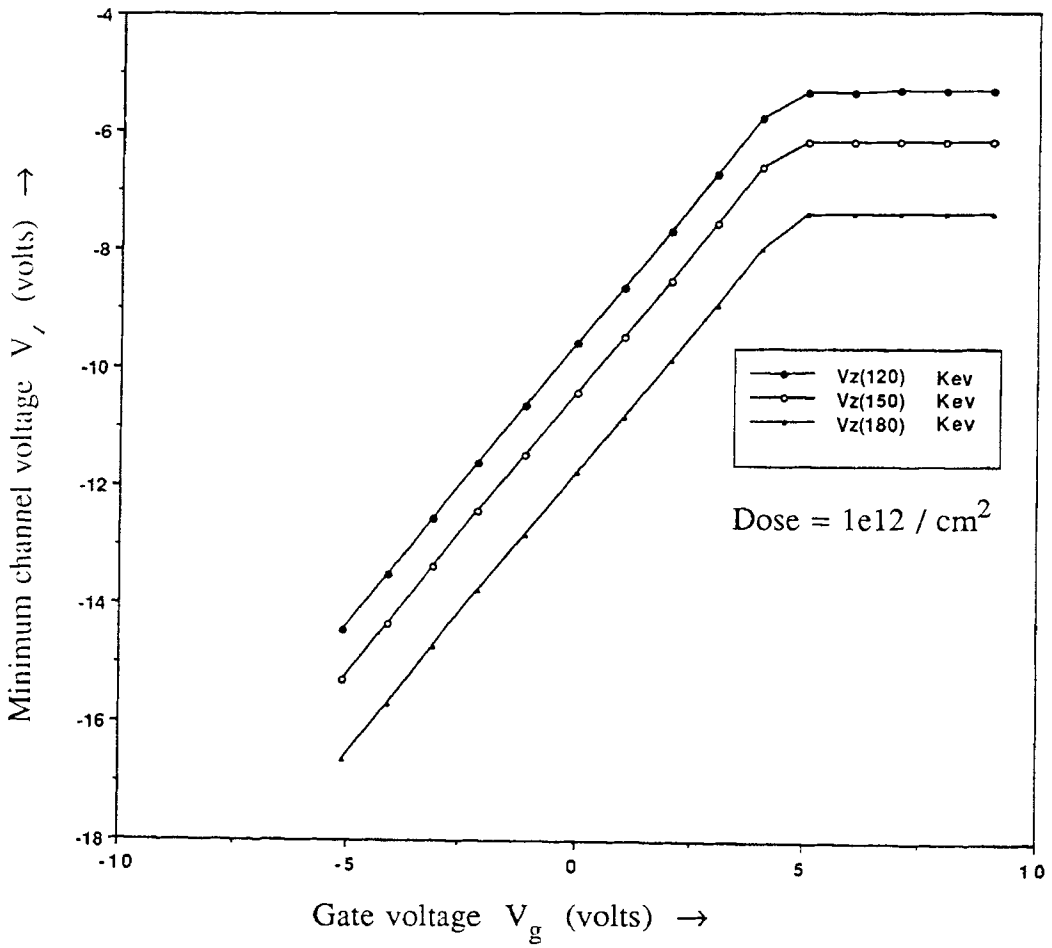


Fig. 4.5. Gate voltage v/s minimum channel voltage in the P$^-$NP FT-DSI imager

The P^-NP structure behaves like two p-channel BCCDs connected back to back. When the p-implant at the Schottky end is doped heavily around 1e16 / cm^2, the well at the Schottky junction is deeper than the BCCD well as shown in Fig. 4.6. In this case the imager fails to operate properly since the holes injected over the Schottky-barrier cannot be collected at the BCCD channel.

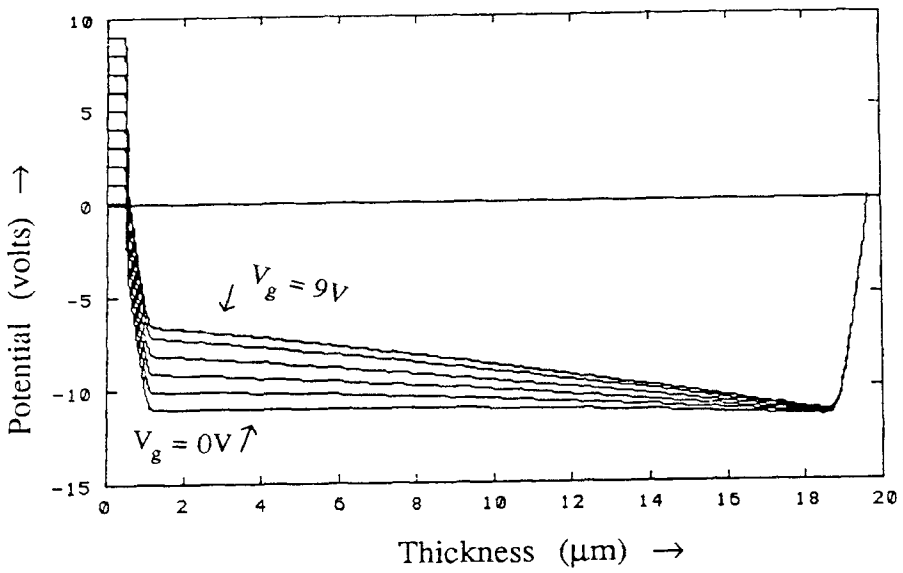
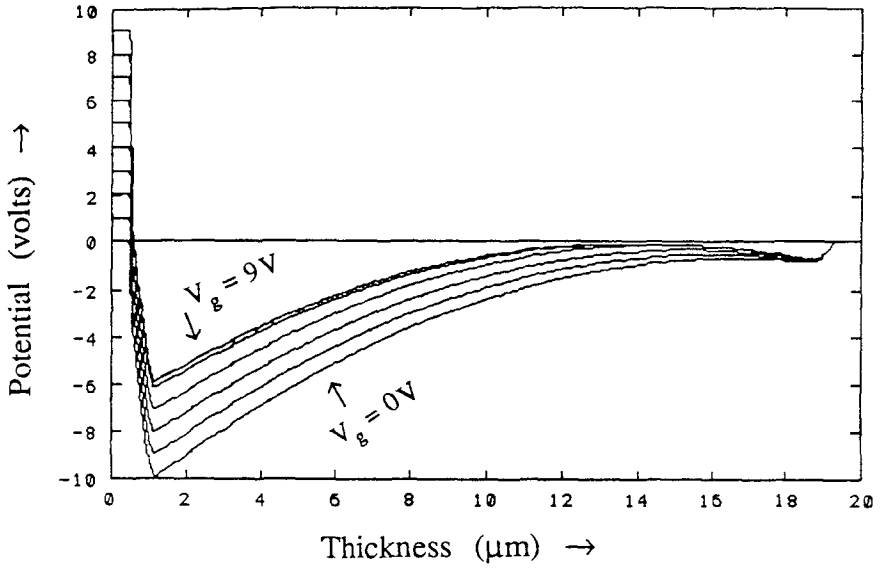
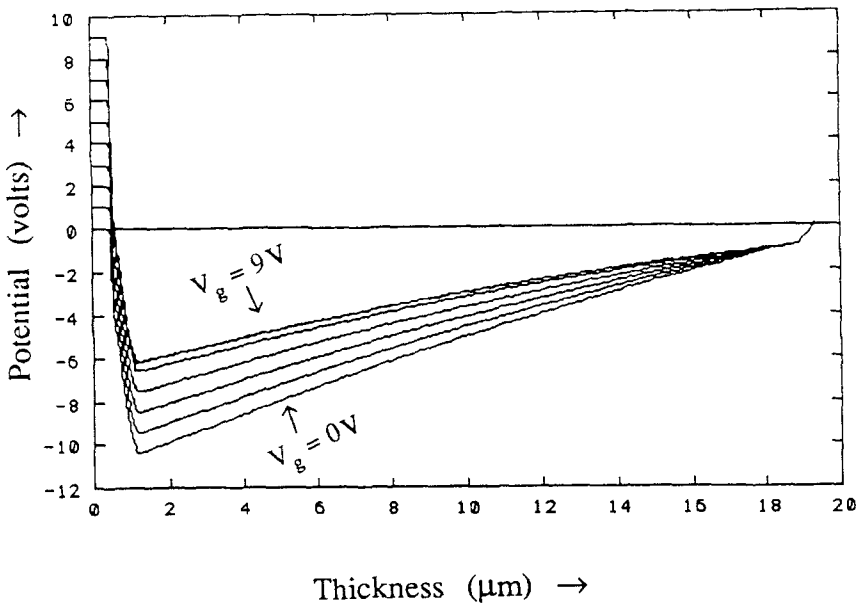


Fig. 4.6. Potential profiles as function of gate voltage for BCCD implant with a dose of 1e12 / cm^2 and energy of 150 Kev and back P^--implant of 1.5e16 / cm^3

Another design concern is the doping concentration of the N-substrate. When doping concentration of the n-well is high (5e13 / cm^3) the potential profile bends in such a way that a barrier is created for smaller concentration levels of p-implant at the Schottky end. Fig. 4.7. shows this effect. Our simulations showed that substrate doping concentration of values less than 1e13 / cm^3 do not create a barrier for the present structure as long as the p-implant at the Schottky end is not too high (see Fig. 4.6).



(a) A barrier is formed for holes injection from the Schottky junction



(b) A barrier not formed for holes injection from the Schottky junction

Fig. 4.7. Potential profile as function of gate voltage for P⁻NP FT-DSI imager for N-substrate doping of (a) 5e13 / cm^3 and (b) 1e13 / cm^3

4.2 P⁻P FT IMAGER

PtSi Schottky junctions are made by first depositing 'Pt' layer (about 10 A^o) on p-silicon. Then the 'Pt' is sintered at a temperature in the range 300-600 ^oC to form a layer of PtSi (about 20 A^o thick). In the P⁻NP imager described above, a p-layer has to be grown on top of the n-substrate, for the device to work in the infrared range. As it was described earlier, a more graded PtSi / p-Si junction is necessary to reduce dark currents. This may be difficult to achieve in the above mentioned imager. As discussed in previous chapter, a FT DSI structure could be made [13], with a P⁻ silicon substrate with Schottky junction on one side and a P-type BCCD on the other side. An additional P-layer is used to form the BCCD structure near the oxide layer. A P⁻ <100> silicon substrate with resistivity of 1000 Ω.cm, was used which corresponds to impurity concentration of 1.5e13 /cm^3.

As part of the operation of the FT-DSI FPA, the whole P⁻P structure has to be depleted. This is done by fixing the quasi-Fermi level of majority carriers (holes) in 'P' and 'P⁻' regions to a minimum negative potential. Since there is no junction available, a single bias statement for silicon layer fixes the quasi-Fermi for the whole semiconductor region. Similar simulations were done for this type of imager to compare the perform- ance of the two FT imagers. From the input deck of SUPREM file, the additional p-implant at the PtSi surface has been removed. The depth of P-type BCCD implant was controlled by the same implant and diffusion cards. Since there is no junction available, the exact depth could be estimated only from the doping plots. Empty well potentials for P-implant being formed by diffusion at 950 ^oC for 200 sec, is shown in Fig. 4.8. It is seen that channel potentials for different gate voltages are close to the results obtained for P⁻NP imager. Potential profiles as function of the charge signal have been simulated by increasing the quasi-Fermi level of the holes. These results are shown in Fig. 4.9. for the gate voltage of zero volts. As discussed before, charge signal can be increased by increasing the quasi-Fermi potential of the

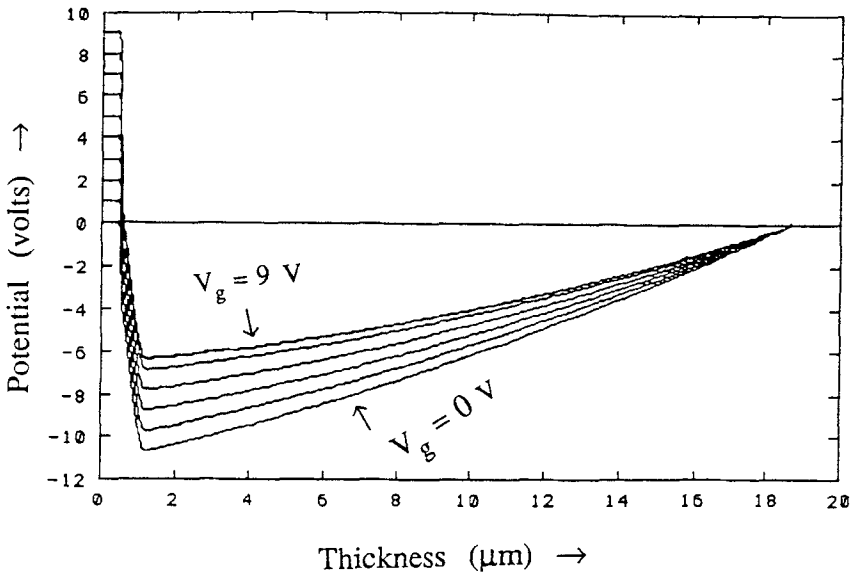


Fig. 4.8. Empty well potential profiles for FT-DSI P⁻P imager as function of gate voltage

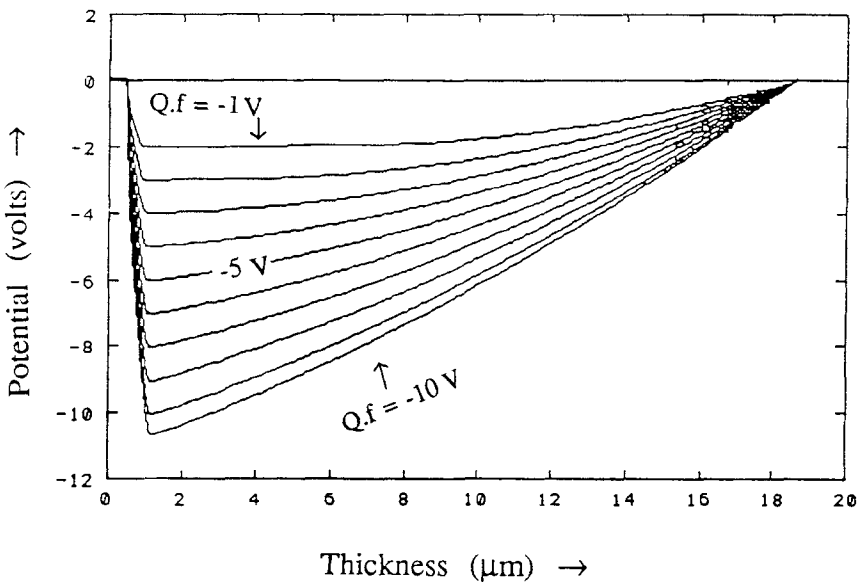


Fig. 4.9. Potential profiles as function of charge signal in the P⁻P FT-DSI imager

p-layer. In the present simulations, quasi-Fermi potentials were increased till the channel potential is equal to that of the channel potential at pinning for empty wells. It is assumed that maximum charge handling capacity is defined by the channel potential being equal to channel potential at pinning or by the charge reaching the oxide surface. The main advantage of having a BCCD channel on a very low doped substrate is that, charge handling capacity is defined by pinning rather than by charge reaching the surface. The hole carrier profile for the case when the p-layer depth is 1 μm is shown in Fig. 4.10. In this case quasi-Fermi potential was adjusted till the channel potential was equal to that at pinning for empty wells.

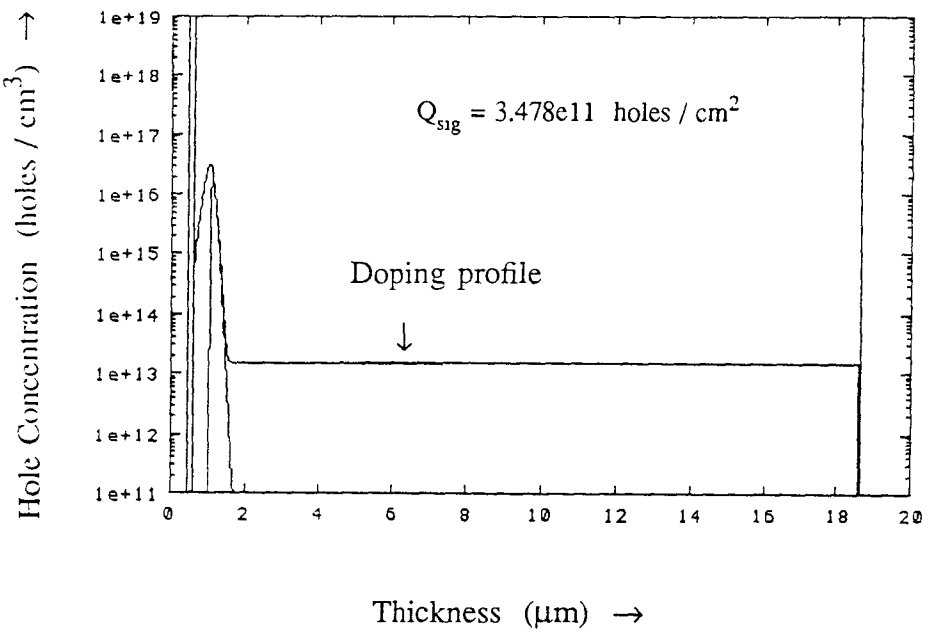


Fig. 4.10. Hole carrier profile corresponding to channel voltage being equal to that at pinning for empty wells

Charge handling capacity shown in Fig. 4.11 was calculated for different depth of p-implant with the same dosage, by increasing the quasi-Fermi level for holes till the channel voltage reaches the value of pinning which was previously obtained for an empty well case. These results are very close to those obtained with the P⁻NP imager. Electric fields in the P⁻P imager behaved in the same way as in case of P⁻NP imager. P-layer implants with greater depths had less electric fields at the Schottky junction.

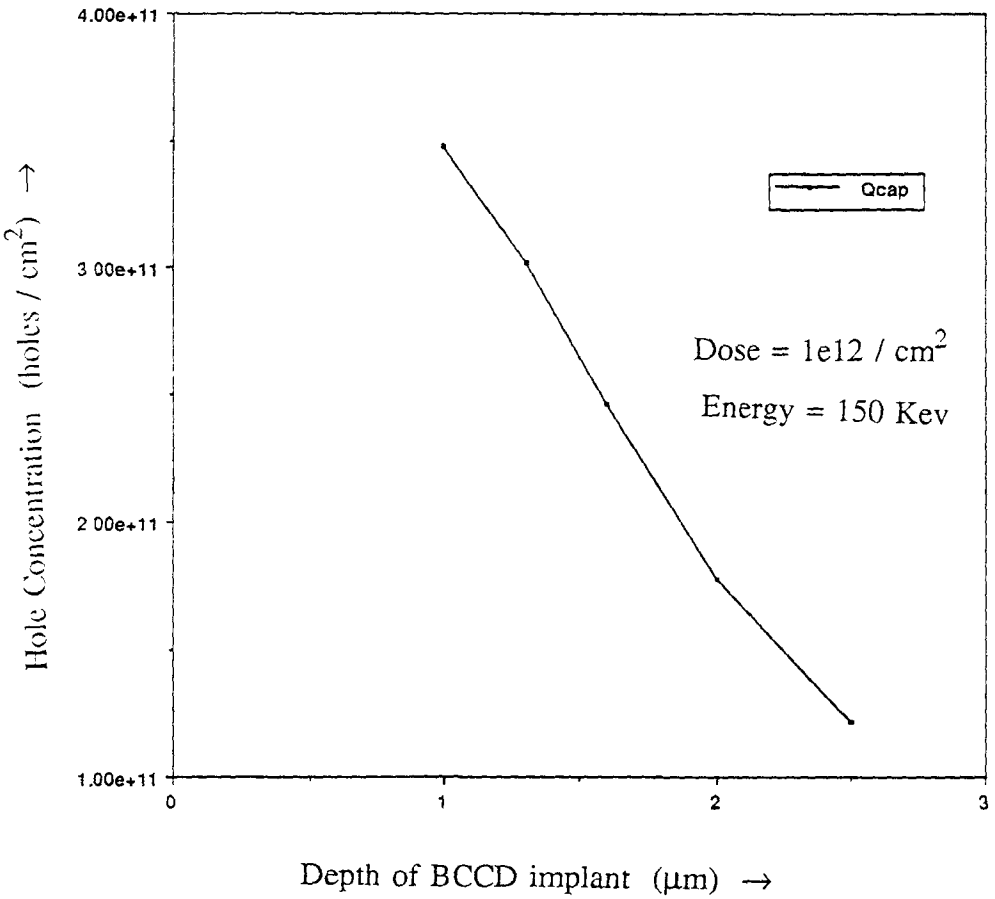


Fig. 4.11. Charge handling capacity as function of Depth of the BCCD implant for P⁻P FT-DSI imager

Potentials were solved for different values of energy of implant. Gate voltage vs channel voltage are shown in Fig. 4.12. As expected the channel potentials become more negative as energy of implant increases.

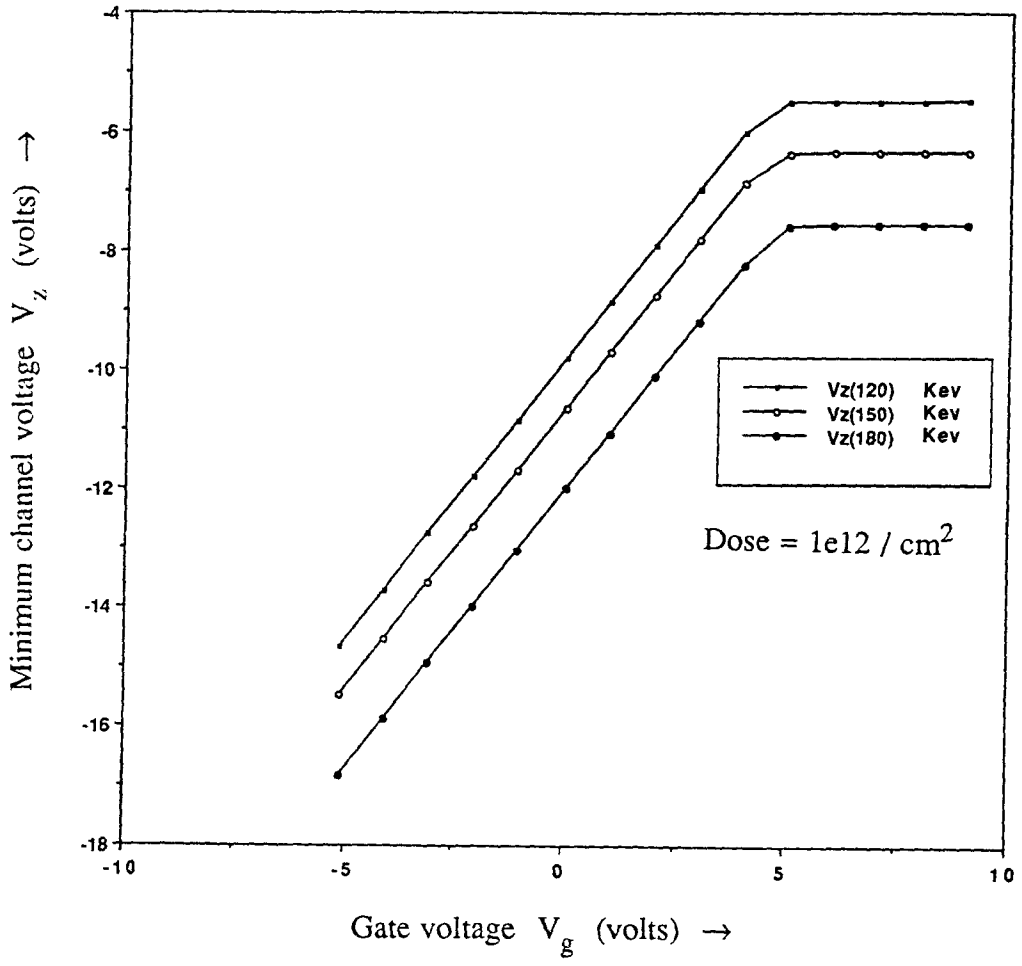


Fig. 4.12. Gate voltage v/s minimum channel voltage in the P$^-$P FT-DSI imager

CHAPTER 5

2-D Simulations of IT DSI Imager

Image smear is minimized in frame transfer imagers by using seperate storage and sensing sites, but it cannot be eliminated completely because of the finite time needed to transfer signal from sensing site to storage site. Interline transfer imagers which have columns of photosensitive gates seperated by inactive (masked from light) regions are better suited for smear free imaging [9]. Light incident on optically sensitive regions generates charge signals which are transferred during the vertical blanking time to the vertical BCCD readout registers. A major advantage of an interline transfer (IT) imagers is that they have very negligible to smear, because the charge is transferred from exposed area into an optically masked vertical register in one transfer [9]. Another effect is that, the geometric MTF along this direction has a slower rolloff, which means frequencies close to Nyquist have good resolution but the disadvantage is that aliasing components are large. In this chapter an IT-DSI image sensor demonstrated by Kosonocky et al [1] is simulated in PISCES IIb to obtain a better understanding about its operation. Various techniques to improve the performance of the imager have been discussed and simulations were done.

5.1 BASIC STRUCTURE AND OPERATION

As shown in Fig. 5.1, IT DSI imager consists of highly doped P^+ charge collecting electrodes (CCE) seperated by n-wells on one side, and a thin Ptsi layer on the other which gives 100% fill factor for the imager [1]. This figure shows the basic structure and operation of this IT DSI imager. Initially a negative bias is effectively applied to the P^+ charge collecting electrode (CCE) which depletes the whole substrate due to the removal of holes by the n-channel BCCD. Light incident on the PtSi Schottky barrier surface, generates charges which follow local electric fields and get

collected at the P^+ CCE layer. Electronic blooming control is achieved by applying a DC voltage to the CCE gates, which define the blooming barrier. The signal is then clocked out into the p-channel BCCD region from where it is sent to horizontal registers for readout.

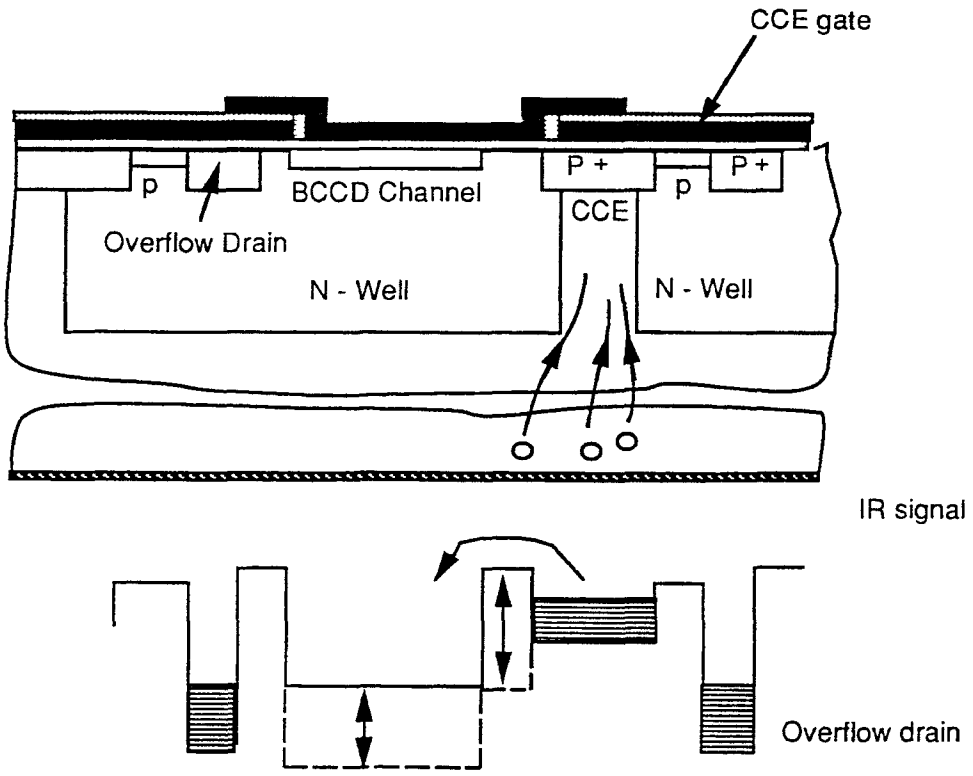


Fig. 5.1. Basic operation of IT-DSI structure

5.2 NO P-IMPLANT

A simple IT-DSI structure has been simulated using PISCES IIb, wherein P^+ CCE layers are seperated by n-wells, to get the local electric fields and to study the effect of additional implants to reduce electric fields at the charge collecting electrodes. Since PISCES does a discrete analysis, a mesh structure has been specified with 30 node points along y-axis and 50 node points along x-axis. 'Diag.flip' card has been set to flip the diagonals in a square mesh about the center of the grid. In case its false, all diagonals will be in the same direction. Silicon region of 25 μm thick and a thin oxide

layer (500 A^{o}) has been specified in the 'region' card. A very low substrate doping (1e13 /cm^3) and thin oxide layer are necessary to deplete the silicon substrate with low bias between the charge collecting electrodes and the PtSi surface. Analytical doping cards were used in the input deck to replicate the practical doping profiles. P^{+} charge collecting electrodes with characteristic length of 0.25 μm, lateral coefficient of 0.6 and concentration of 1e19 /cm^3 were used. Gaussian profile with junction depth of 4 μm and peak concentration of 2e16 /cm^3 was used to simulate the n-well region. This had a lateral expansion coefficient of 0.1 to avoid masking of charge collecting centers by these n-wells. A 1-D doping profile of n-well is shown in Fig. 5.2.

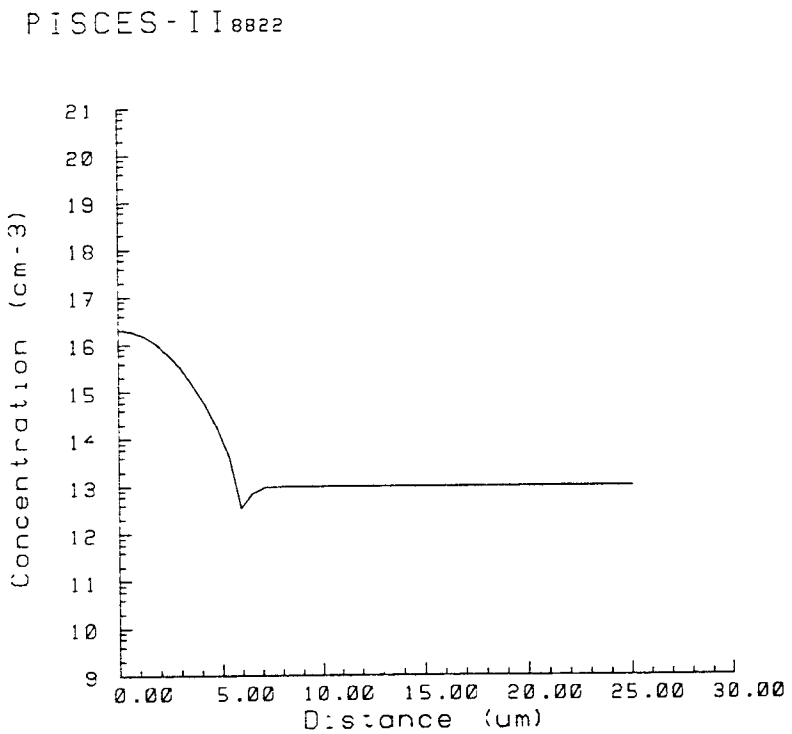


Fig. 5.2. Doping profile of n-well in P^{--} substrate of IT-DSI imager

As PtSi contact is not available in PISCES IIb, a contact with Tungsten disilicide has been used and the material constants of silicon have been altered to get a 0.22 ev barrier height. Initial grid structure was refined with the regrid threshold of '2' i.e., if

the logarithm of the absolute value of doping changes by '2' or more across a triangle then that triangle is refined. This regrid criterion was applied only to silicon region and not in the oxide region to get a more efficient grid structure with fewer grid points. This approach is simpler as it requires somewhat less pre-acquired intuition as compared to that using 'distorted mesh' technique. Subsequent regrid on potential is not necessary because the initial zero carrier poisson solution yields almost zero potential across the whole device.

PISCES IIb fixes quasi-Fermi potentials based on the bias applied or on doping. But P.BIAS and N.BIAS specify fixed quasi-Fermi potentials of carriers that are not being solved for. So for zero carrier POISSON analysis the quasi-Fermi potentials of both electrons and holes can be controlled seperately. As described before, a bias is applied between the charge collecting electrodes and the PtSi surface, to deplete the silicon substrate. This was examined by slowly reducing the P.BIAS from 0 to -10 V. The 1-D potential profile across a section through the charge collecting electrode for different bias voltages is shown in Fig. 5.3.

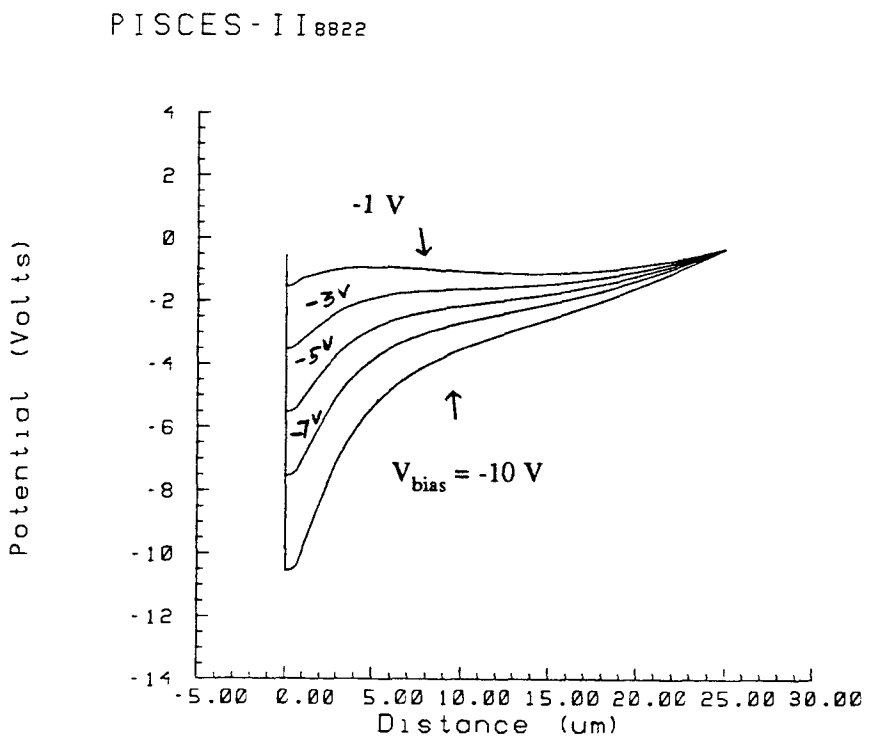


Fig. 5.3. Potential profile of the IT-DSI structure with no p-implant across the section through P^+ CCE

The simulations showed that for bias voltages less than -6 V, the depletion region extends in the spaces between the n-wells and the CCEs become electrically isolated. Also shown in Fig. 5.4 is a 1-D potential profile across a section through n-well for different biases. It is clear that the drift field for holes is less in these regions as the slope is not so high.

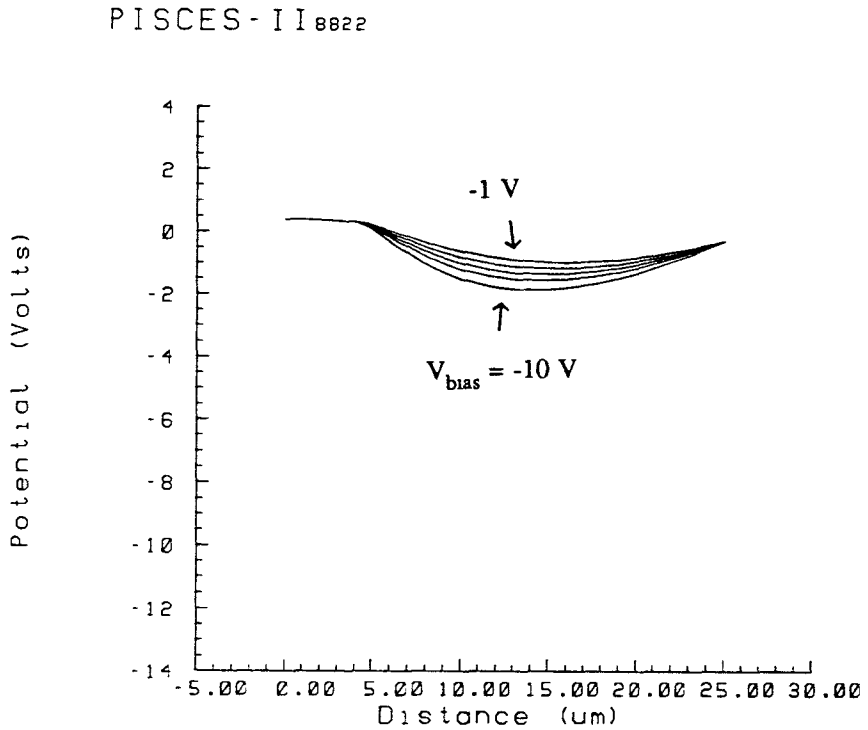


Fig. 5.4. Potential profile of the IT-DSI structure with no p-implant across the section through n-well

For the case of applied bias of -10 V between charge collecting electrode and PtSi surface, a 3-D potential profile is shown in Fig. 5.5. PISCES IIb by itself doesn't have the capability of producing 3-D images. 'FUGU' - a menu driven tool which generates three-dimensional images using data from files generated by Stanford's PISCES IIb / SUPREM IV programs has been used. It is to be noted here that the voltage on the charge collecting electrode gates is zero. The gate bias usually a negative voltage, is used to fix the blooming barrier. But this doesn't has an effect on the potential in the

p-silicon bulk region because of the shielding effect of the heavily positive P^+ layer. The potential profile shown in Fig. 5.5 indicates that the depletion region extends upto the charge collecting electrodes which may result in large electric fields that in turn may lead to carrier multiplication effect and large dark current. For this reason it is not preferable to deplete this structure upto the P^+ regions of the charge collecting electrodes.

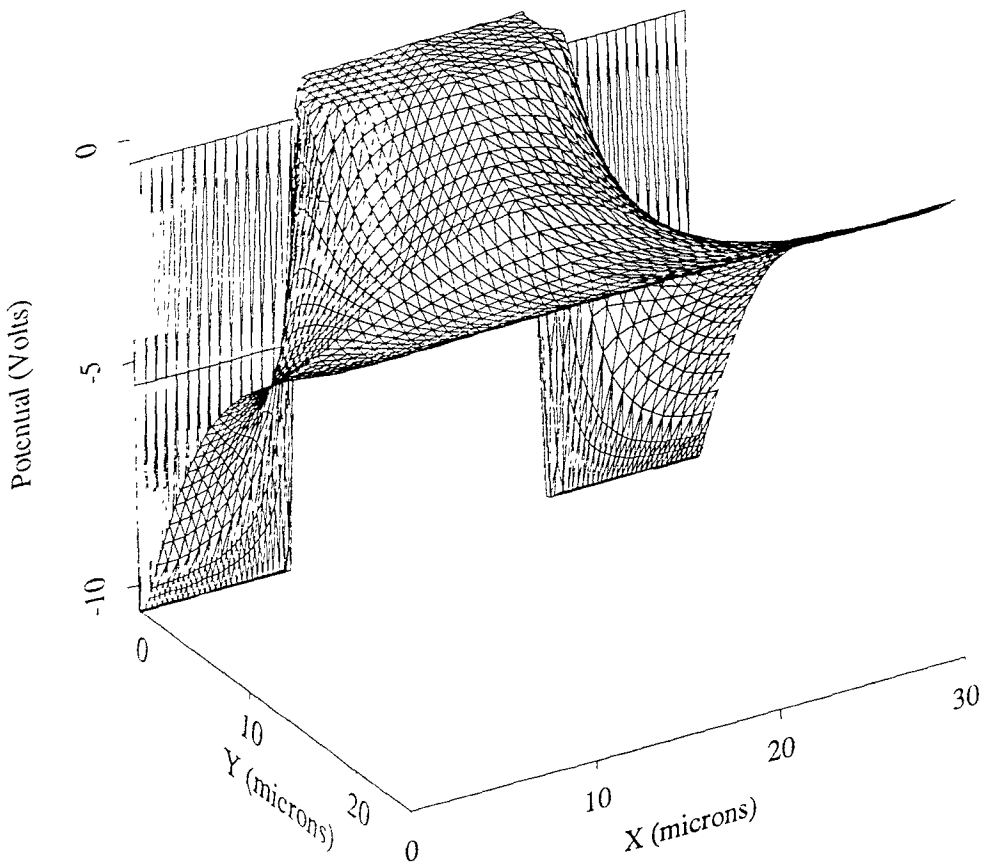


Fig. 5.5. Potential profile of the IT-DSI structure with CCE potential of -10 V and no p-implant

Local electric field vectors at each node in the mesh is plotted in Fig. 5.6. This figure gives an idea about the directionality of the signal path, once the holes are injected at the PtSi surface. Since holes move in the direction of electric fields the plot effectively predicts the hole movement in the structure. The junction boundary is also shown in the figure by a dotted line which represents n-well. It is clear that n-wells create barriers for the holes and henceforth act as seperation between the adjacent P^+ charge collecting centers.

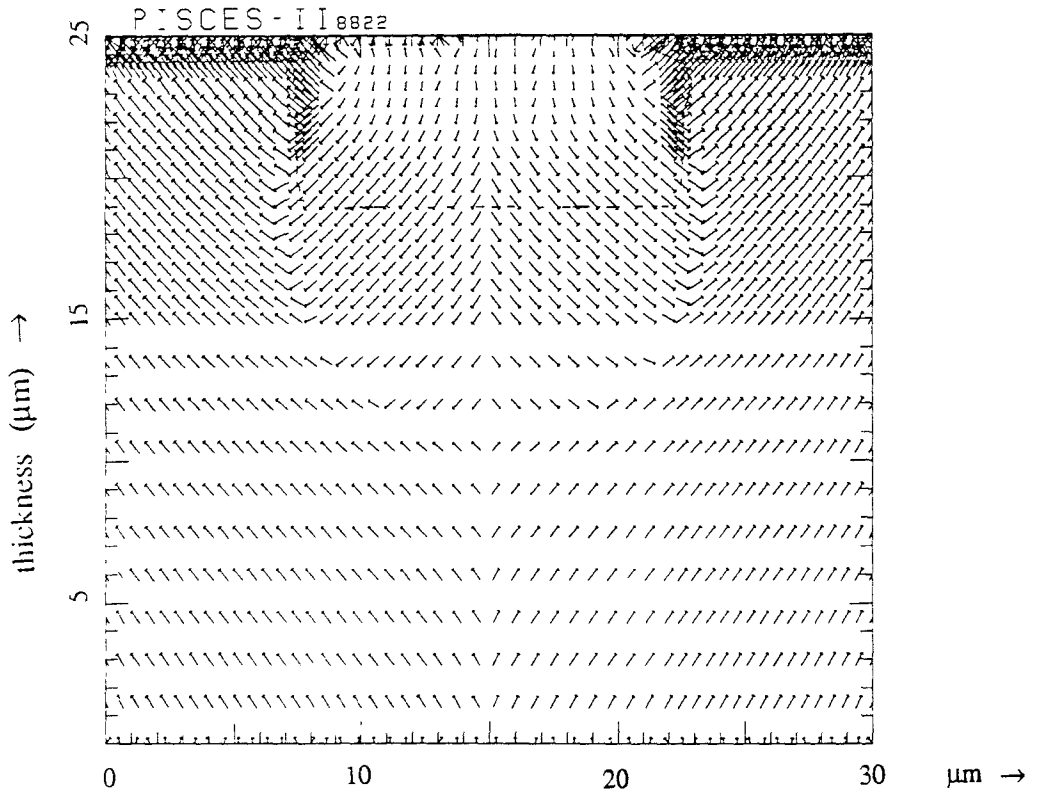


Fig. 5.6. Local electric field vectors for the IT-DSI structure for which the potential profiles are shown in Fig. 5.5.

5.3 UNIFORM P-IMPLANT

In the previous section a major drawback was that depletion extends upto the charge collecting electrodes. To avoid this and to improve the effectiveness of the CCEs to collect charge an additional p-implant of characteristic length 4 μm is used to prevent depletion to reach the charge collecting centers [1]. Fig. 5.7 shows this type of structure. Due to this additional implant, the n-well depth is reduced. The effect is shown in Fig. 5.8 wherein the depth of n-well changes to 4 μm as compared to 6μm

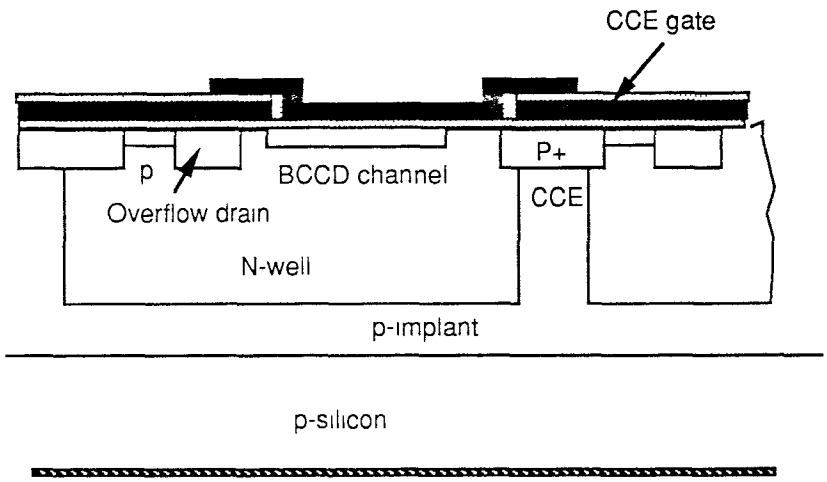


Fig. 5.7. IT-DSI structure with uniform p-implant

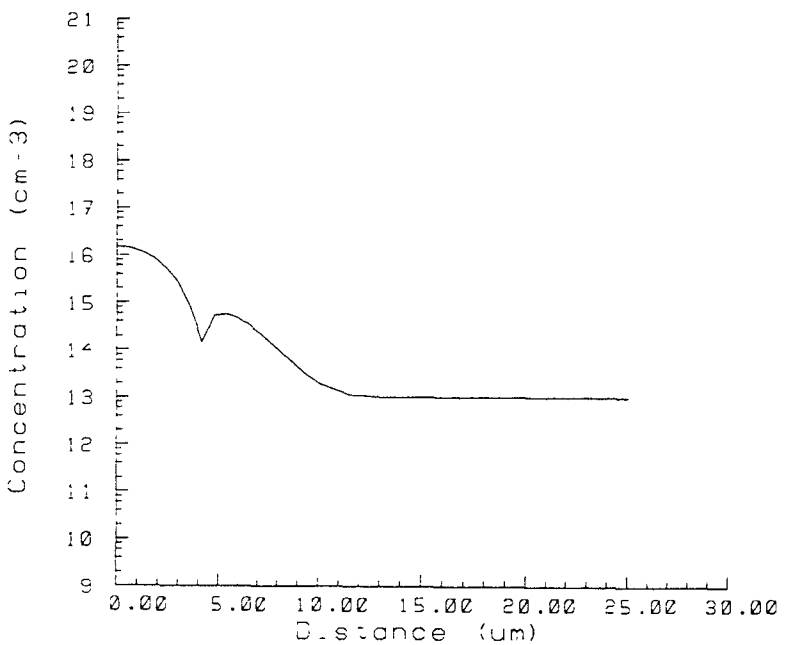


Fig. 5.8. Doping profile across the section through n-well for IT-DSI structure with uniform p-implant

without the additional implant, for the case when p-implant peak concentration is 5e15 /cm^3. Simulations revealed that the problem of seperation of pixels arises when the peak concentration of p-implant is around 0.8e16 /cm^3. Figure 5.9 shows hole concentration plot for this case. It is seen that the structure is not depleted fully so as to seperate the pixels. In other words the two adjacent pixels are merged.

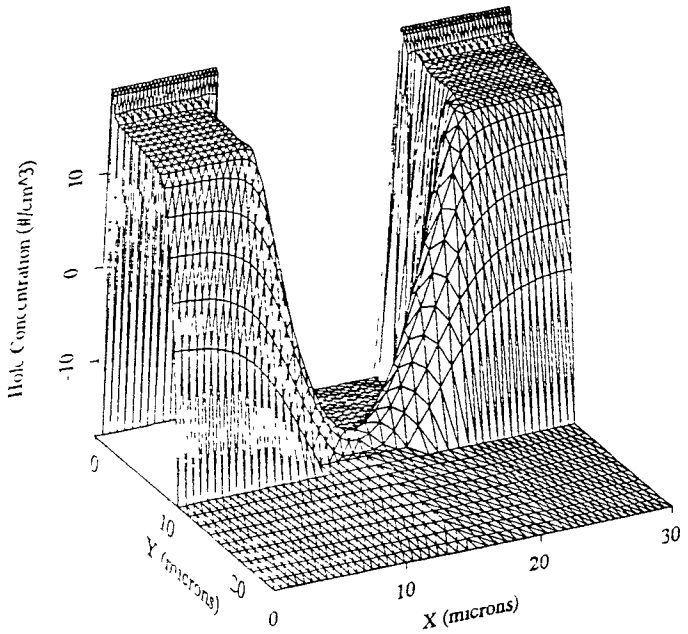


Fig. 5.9. Hole concentration profile for a IT-DSI structure with uniform p-implant of 0.8e16 / cm^3 and CCE voltage of -10 V

Note: The adjacent pixels are not completely isolated.

Figure 5.10 shows similar plot for the case of p-implant being 5e15 / cm^3 and its clear that the same problem doesn't exist. As was done for the previous case, quasi-Fermi potentials of holes was varied from 0 V to -10 V to simulate the reverse bias applied between the charge collecting electrodes and PtSi surface. 1-D potential profiles across a section through charge collection electrodes reveals that punchthrough problem doesn't exist. This is shown in Fig. 5.11. Also the potential drops more rapidly in the bulk indicating better drift field for the holes injected at the back surface. A notable

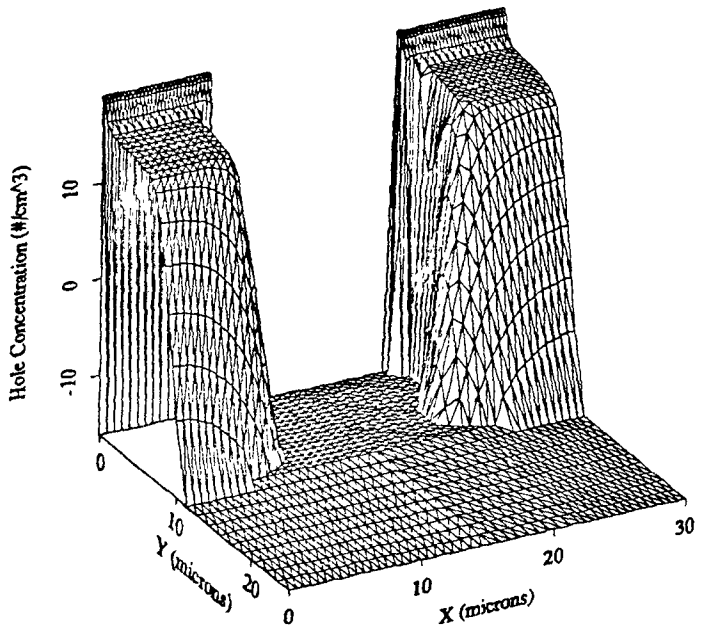


Fig. 5.10. Hole concentration profile for a IT-DSI structure with uniform p-implant of 0.5e16 / cm^3 and CCE voltage of -10 V

Note: The adjacent pixels are isolated.

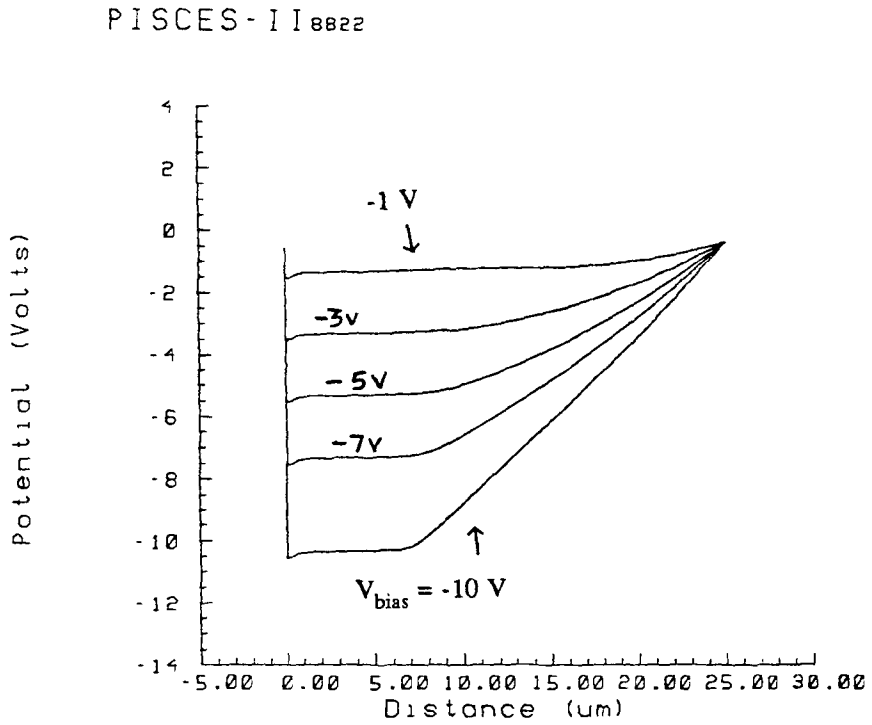


Fig. 5.11. Potential profile of the IT-DSI structure with uniform p-implant across the section through P^+ CCE

advantage which is evident from the simulations is the potential profile across the n-well section. For the no-implant case, the potential dropped to a minimum of -2 V when the bias was -10 V. For the same bias Fig. 5.12 shows the minimum potential to be around -7 V when a p-implant of peak concentration 5e15 /cm^3 is used.

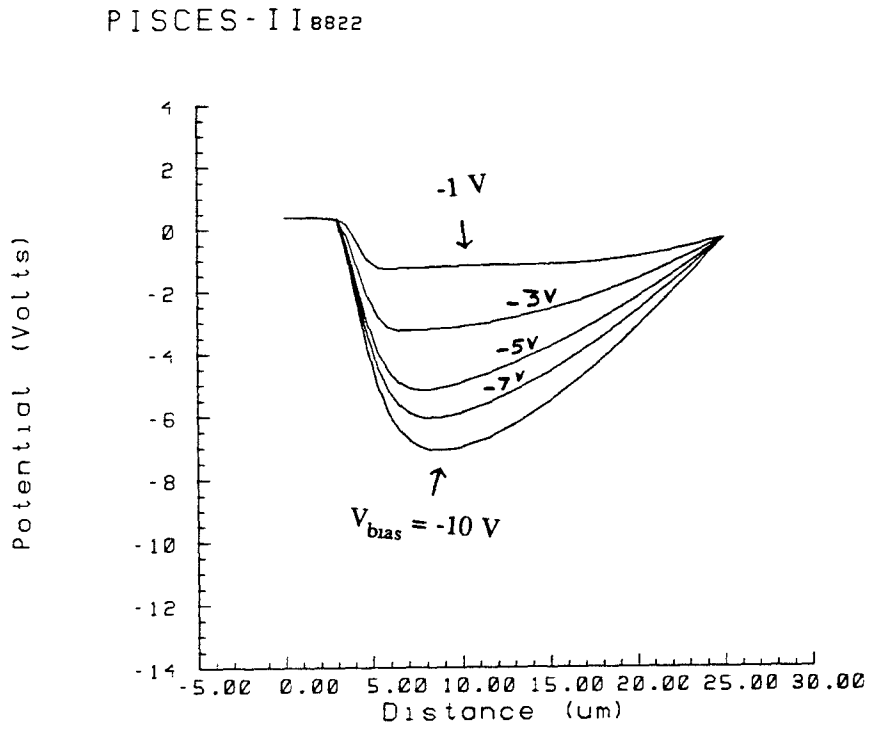


Fig. 5.12. Potential profile of the IT-DSI structure with uniform p-implant across the section through n-well

A 3-D plot showing the doping profiles used in these simulations is shown in Fig. 5.13 and corresponding potential profile is shown in Fig. 5.14. The holes injected at the back surface move towards the more negative charge collecting electrodes while they are blocked by the n-wells as the potential rises at the n-well regions. Again it has to be noted that for these simulations voltage at the charge collecting electrode gates was kept at zero. Another simulation run could be done with CCE gates at a voltage equal to that required for blooming control, but no sygnificant difference was observed due to shielding by the P^+ CCE's.

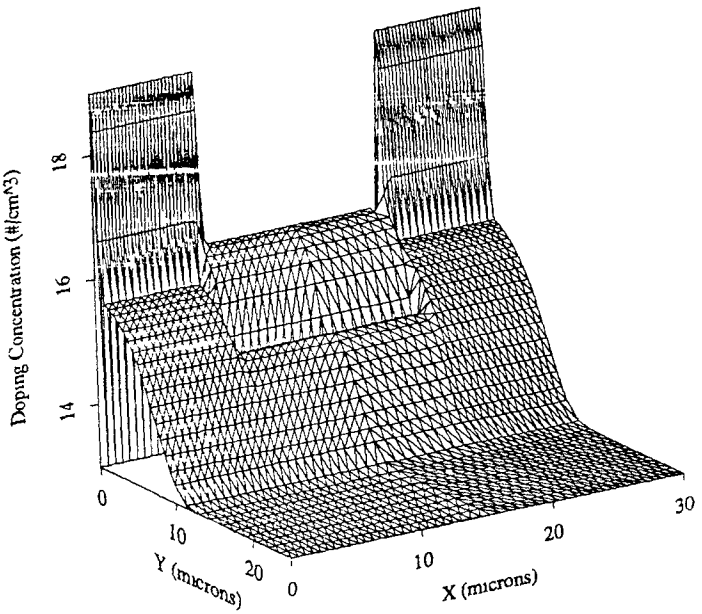


Fig. 5.13. Doping profile of the IT-DSI structure with uniform p-implant of 5e15 / cm^3

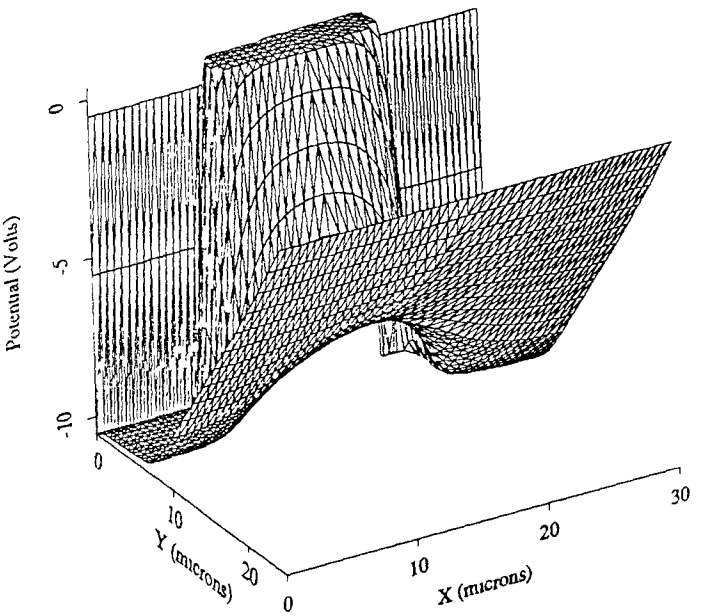


Fig. 5.14. Potential profile of the IT-DSI structure for which the doping profile is shown in Fig. 5.13.

5.4 LOCAL P-IMPLANT

The only disadvantage of using a p-implant uniformly across the structure is that pixels could merge if the doping is high. But on the other hand, the higher doped p-implant has the advantage of providing drift fields for holes specially under the n-well region. Another version of IT imager has been proposed [1], with a local p-implant between the n-wells. The doping profile in this case is a gaussian p-implant having peak concentration of 5e15 /cm^3 and characteristic depth of 4 μm. It is shown in Fig. 5.15 below,

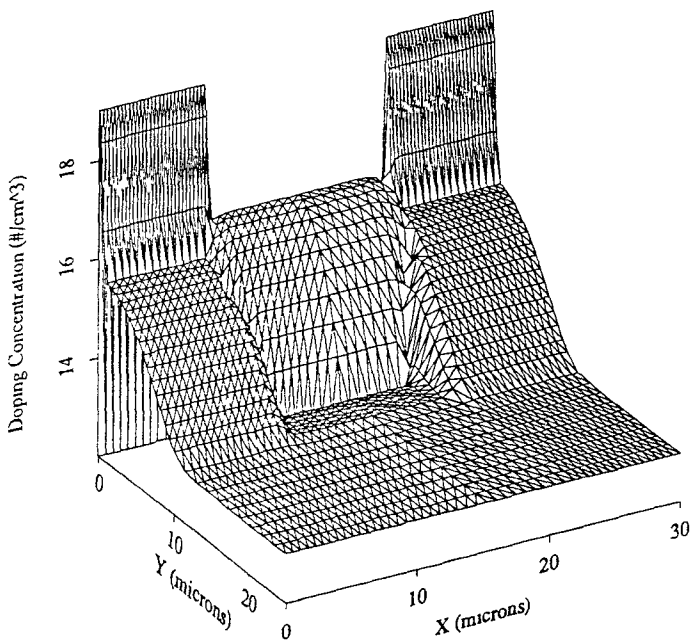


Fig. 5.15. Doping profile of the IT-DSI structure with local p-implant of 5e15 / cm^3

The potential profile for this type of DSI structure is shown in Fig. 5.16 and is similar to that obtained for the previous case of having a uniform p-implant. The 1-D potential profiles across the section through P^+ CCE's and the n-wells are shown in Fig. 5.17 and Fig. 5.18. The potential profile across a section through P^+ region shows no

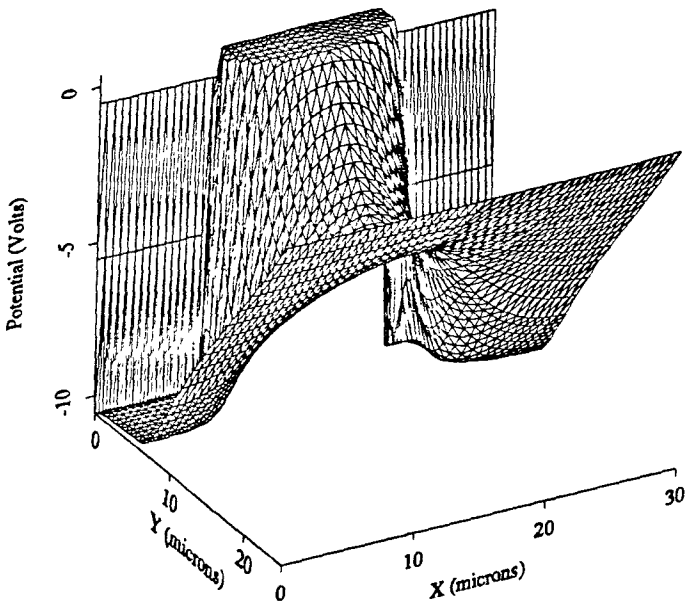


Fig. 5.16. Potential profile of the IT-DSI structure for which the doping profile is shown in Fig. 5.15.

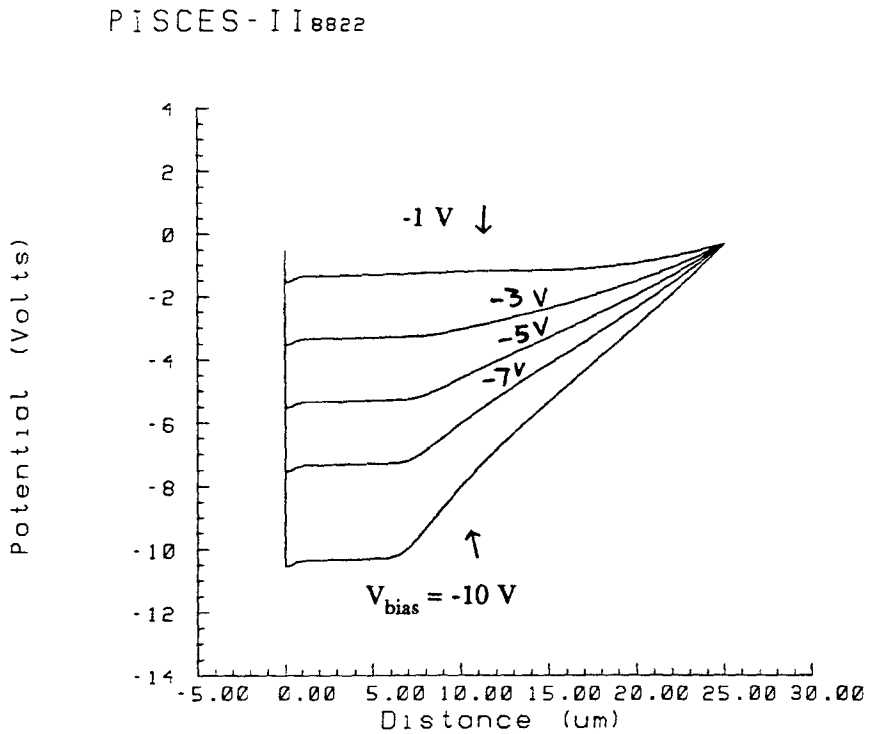


Fig. 5.17. Potential profile of the IT-DSI structure with local p-implant across the section through P^+ CCE

appreciable variation when compared with the previous case of having p-implant uniformly across the structure (see Fig. 5.11). But the potential profile across a section through the n-well region shows a degradation because minimum potential under the n-well for a bias of -10 V between PtSi surface and charge collecting electrodes is about -4.2 V as compared to -7 V for uniform p-implant case.

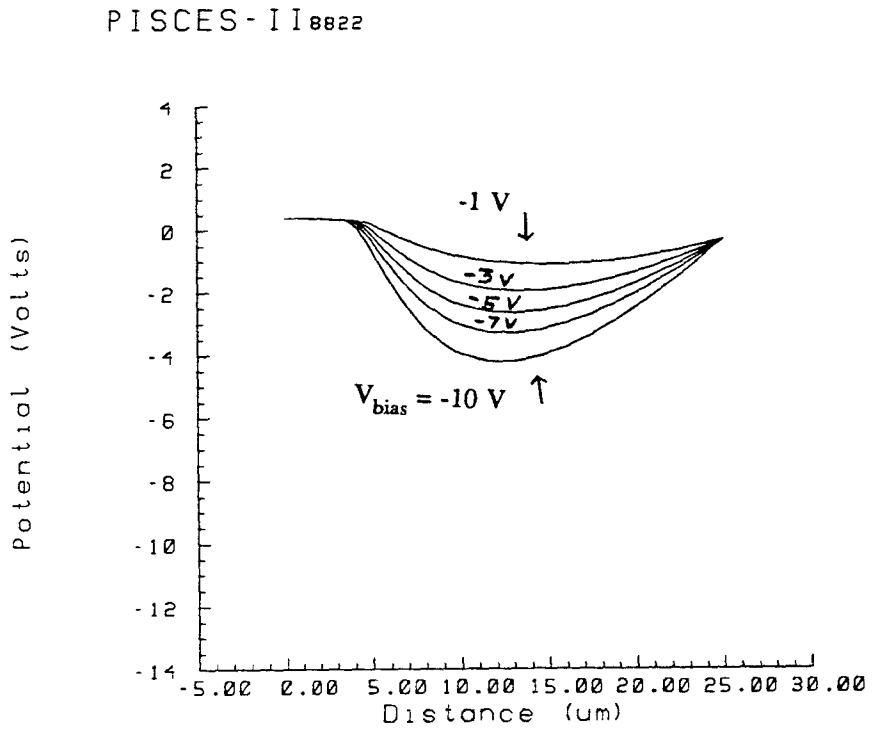


Fig. 5.18. Potential profile of the IT-DSI structure with local p-implant across the section through n-well

5.5 SIGNAL CHARGE EFFECT ON OPERATION OF IT-DSI IMAGER

The above simulations define the empty well characteristics of IT DSI Imagers. For the case when intensity of the image has a large spatial variation, it is possible that one pixel may get a large signal while the adjacent pixel may get comparatively smaller signal. Potential profiles with charge could be simulated by increasing the quasi-Fermi level in the p-silicon. Since the two adjacent P^+ CCE are implanted on a p-substrate, PISCES IIb sets the quasi-Fermi for the whole of silicon. In the

simulations, four electrodes on the pixel on the right side and three electrodes on the pixel on the left side were used. This was imperative to force the adjacent pixels to different quasi-Fermi levels, to simulate different signal intensities on adjacent pixels. Transient analysis was carried out and potential profile for the case when the potential of adjacent pixels differs by 3 V is shown in Fig. 5.19.

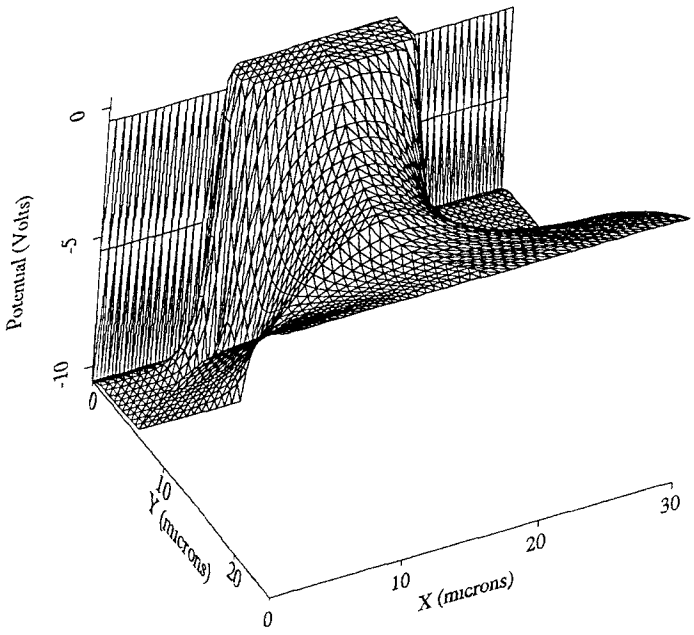


Fig. 5.18. Potential profile for the case of a pixel with large signal intensity adjacent to a pixel with low signal intensity

Note: Potential rise of 3 V corresponds to a charge signal of 12.9e11 holes / cm^2 for gate oxide thickness of 500 A^o

Local electric field vectors for the case when there is no charge or when the signal is same in adjacent pixels is plotted in Fig. 5.20. Figure 5.21 shows the local electric fields when the signal is such that there is a difference of 3 volts between adjacent P^+ electrodes. It is clear that the effective pixel size at the low intensity sites increases, while the effective pixel size at the adjacent high intensity sites decrease. This effect is expected to result in reduction of the contrast of the imager.

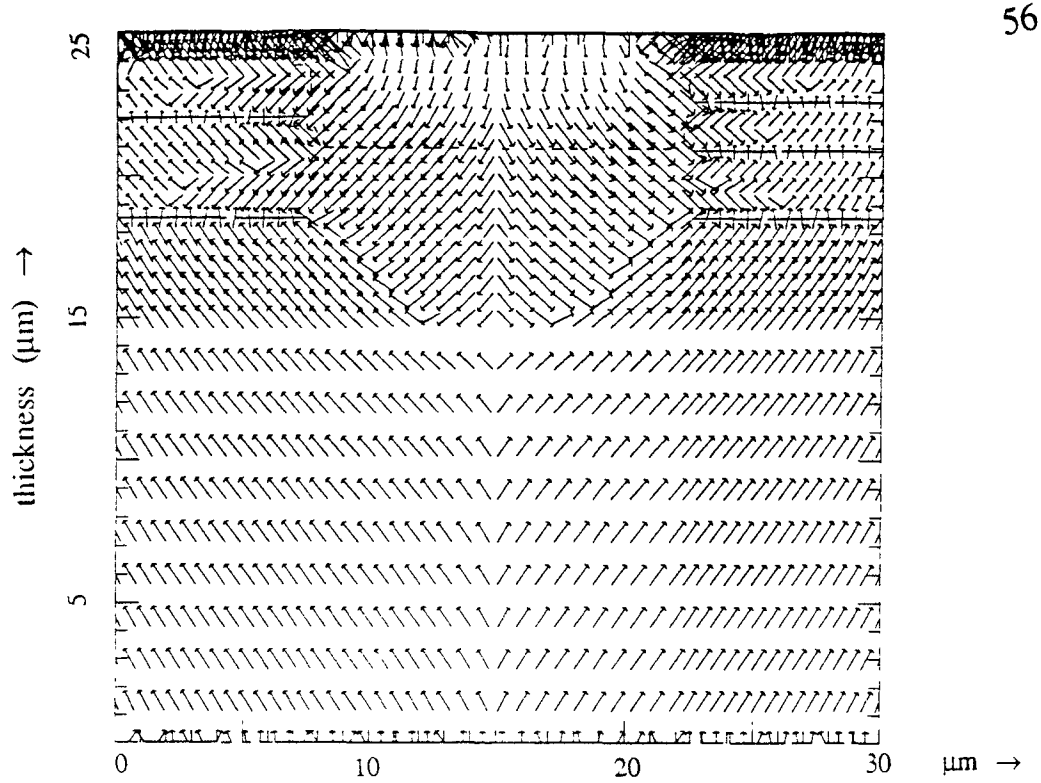


Fig. 5.20. Local electric field vectors for equal signal levels at adjacent pixel locations

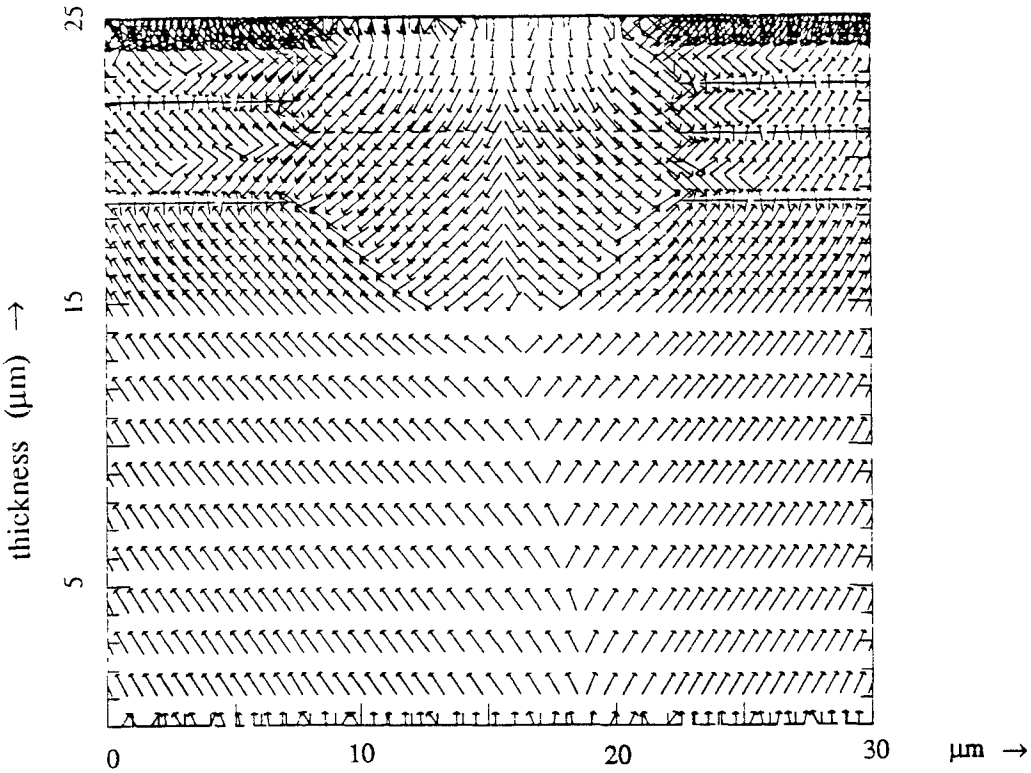


Fig. 5.21. Local electric field vectors for which the potential profiles are shown in Fig. 5.19.

CHAPTER 6

Conclusions

Two types of frame transfer DSI imagers in the form of a P^-NP and a P^-P structure were simulated using SUPREM III. Electrical characteristics like charge handling capacities and empty well potentials were found to be comparable in both type of FT-DSI structures. Hence its more convenient to form FT-DSI imagers using the simpler P^-P structure rather than the more difficult to construct P^-NP structure. The results of the theoretical analysis were found to be consistent with those obtained by SUPREM III simulations.

PISCES IIb simulations were done for interline transfer DSI imager. Two adjacent pixels with an n-well barrier were simulated to study the local electric fields which define the directionality of the injected charge signal. Zero carrier Poisson solutions were carried out to get the potential profiles across the device. IT-DSI structure with additional implants was also investigated. It was found that the electrical drift for holes injected at the Schottky-barrier surface under the n-well region was considerably effected by a p-implant. Potential profiles for IT-DSI structure with different voltages at the adjacent charge collecting electrodes showed that the effective pixel size tends to decrease in the pixel with large charge signal. This effects in some reduction in contrast of the imager.

APPENDIX A

MTF Degradation of CCD Imagers [20, 21]

An optical system in general, can be modelled as a linear operator [20]. Consider Fig A.1 shown below:

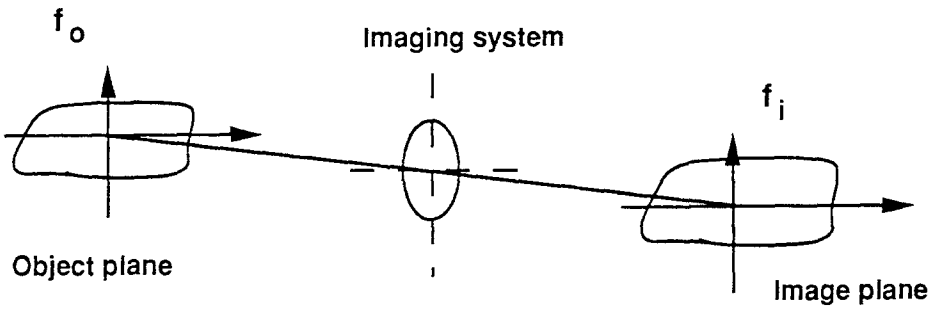


Fig. A.1. Imaging process (spatial domain)

$$f\ (x_i\ ,y_i\ ) = \Lambda\ \left[f\ (x_o\ ,y_o\ )\ \right]$$ where Λ is the linear operator ;

$$f\ (x_i\ ,y_i\ ) = \Lambda\ \left[\int\int f(x,y)\ \delta\ (x_o - x, y_o - y)\ dx.dy\ \right]$$ .....sampled input.

$$f\ (x_i\ ,y_i\ ) = \left[\int\int f(x,y)\ \ \Lambda \left\{ \delta\ (x_o - x, y_o - y) \right\} dx.dy\ \right]$$

$$f\ (x_i\ ,y_i\ ) = \left[\int\int f(x,y)\ h(x_i - x, y_i - y) dx.dy \right.$$

$g(x\ ,y) = f(x\ ,y)*h(x\ ,y)$ imaging process as a convolution operation.

In the frequency domain above equation is $G(x\ ,y) = F(x\ ,y)\ .\ H(x\ ,y)$

where H(x , y) is optical transfer coefficient.

Modulation transfer function (MTF) is the magnitude part of the optical transfer func-

tion [21] and it defines the degradation of the optical system. In an IRCCD, the analog image is converted to a discontinuous form. Any single detector of size W_x x W_y, will perform spatial averaging of the scene that falls on it. The degradation of the image due to this effect is defined by geometric MTF, which is a 2-dimensional fourier transform of the detector shape function. For a 1-D case consider the Fig A.2 shown below:

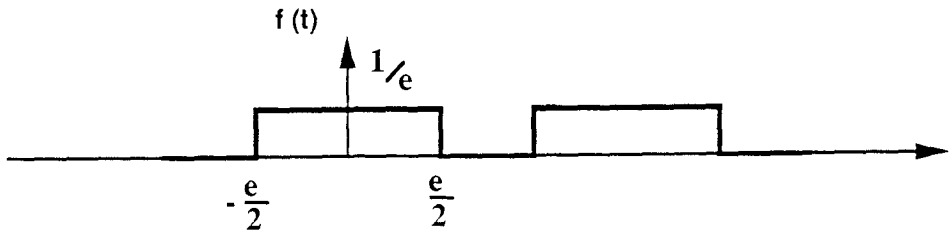


Fig. A.2. Detector shape function

$$\text{geometric } MTF = \int_{-e/2}^{e/2} f(t)\, e^{-J\,\omega\, t}\, dt = \frac{1}{J\,\omega\, e} * \left[e^{-J\,\omega\, t} \right]_{\frac{e}{2}}^{-\frac{e}{2}}$$

$$\text{geometric } MTF = \frac{2\, sin(\frac{\omega\, e}{2})}{\omega\, e} = \frac{sin(\frac{\pi\, s\, e}{d})}{\frac{\pi\, s\, e}{d}}$$

$$\text{because } \omega = 2\,\pi f = 2\,\pi\, s\, f_o = \frac{2\,\pi\, s}{d}$$

where e = pixel size, d = pixel pitch, $f_o = \frac{1}{d}$, and $s = \frac{f}{f_o}$

HORIZONTAL RESULTION

There is a very narrow seperation between columns of pixels in a CCD array. So the pitch (d) is almost equal to the size of the pixel (e). For this case the geometric MTF is plotted as a function of the parameter 's'. We get a zero at s = 1,2,3,4...., because

$$\text{geometric MTF} = \sin\left\{\frac{\frac{\pi s e}{d}}{\frac{\pi s e}{d}}\right\} \approx \frac{\sin(\theta)}{\theta} \quad \text{(same form).}$$

$$\text{we know } \frac{\sin(\theta)}{\theta} = \begin{cases} 1 & \text{if } \theta = 0 \\ 0 & \text{if } \theta = n\pi \end{cases}$$

$$\text{from above equation its clear that } MTF = \begin{cases} 1 & \text{if } s = 0 \\ 0 & \text{if } \frac{\pi s e}{d} = n\pi \end{cases}$$

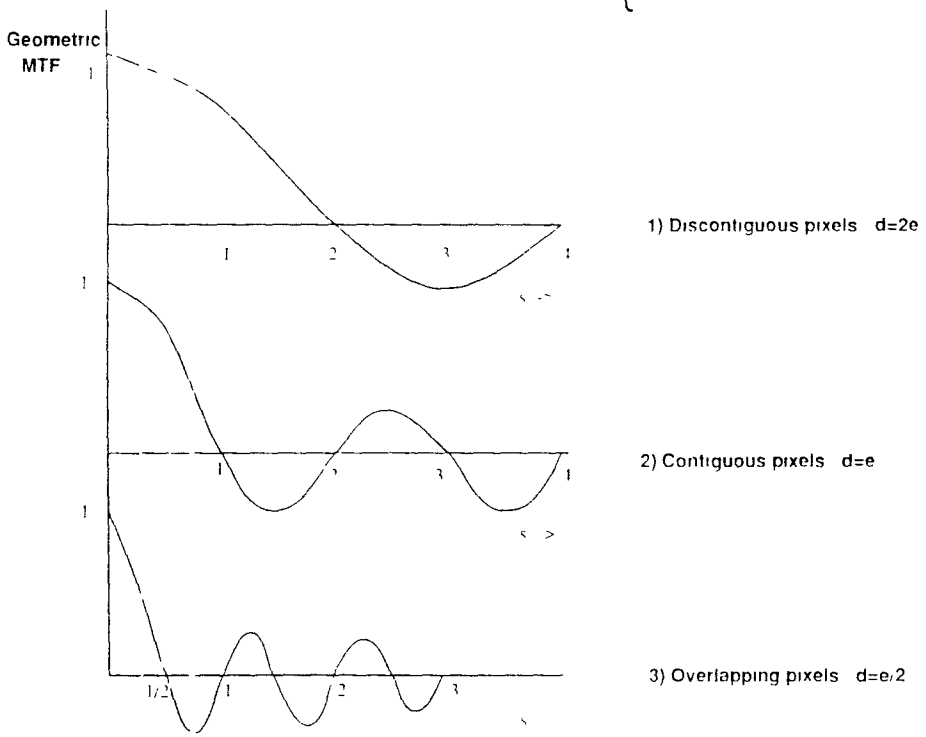


Fig. A.3. Geometric MTF degradation

Since we know pixel width (e) = pitch of the pixel (d), the zeroes of the MTF are at s = 1,2,3,4...and so on, as shown in the Fig A.3.

If 'f' is the maximum spatial frequency in the image, the sampling frequency $f_o >= 2\ f$ to avoid aliasing. The MTF for a discontiguous case is also shown for comparision purpose. From Fig A.3, its clear that MTF is a bit lower for images whose spatial frequency is greater than Nyquist limit. So aliasing effects are less in this case. But at the same time, MTF is lower for frequencies below Nyquist limit, which means resolution is not good as compared to a discontiguous case as in IT imagers.

VERTICAL RESOLUTION

Without interlace, the situation is same as that in horizontal case. But with vertical interlace, the pixels are overlapped and in this case e = 2d.

Zeroes of the MTF are at:

$$\frac{\pi\, s\, e}{d} = n\pi \quad ==> \text{ at } s = \frac{n}{2} \text{ for } n = 1,2,3,4...\textit{and so on.}$$

The MTF plot is in Fig A.3. Its clear that in the case of interlace, the aliasing effects are still smaller and vertical resolution is worse than horizontal resolution.

Appendix B

```
Title       SUPREM III simulation.  P-NP DSI IMAGER
Comment     Structure definition (1.0 mu).
Comment     Initialize the bottom layer.
Initialize  Aluminum thickness=0.002
Comment     Define silicon/aluminum constants to get 0.22ev.
Silicon     band.gap=1.166 affinity=4.05
Aluminum    Work.fun=4.996
Comment     Deposit p-layer.
Deposit     Silicon <100> boron concentration=1.5e16
+           thickness=1.0
Comment     Deposit silicon bulk.
Deposit     Silicon <100> phosphorus concentration=4.5e12
+           thickness=18 dx=0.05
Comment     Put the buried layer.
Implant     boron dose=1.0e12 energy=150
Diffusion   temperature=950 time=200
Comment     Deposit gate oxide
Deposit     oxide thickness=0.1
Deposit     polysilicon bor conc=1e20 thickness=0.5 temperature=600
Comment     Output statements
Print       layer
Print       chemical concentr bor filename=bor.con
Print       chemical concentr phos filename=phos.con
Print       chemical concentr net filename=net.con
Save        structure file=pnp.str
Stop        End of simulation.
```

Appendix B

```
Title      Electrical characteristics empty well.
Comment    Poisson solution.
Comment    Initialize structure
Initialize structure=pnp.str
Comment    Electrical card
Electrical steps=10 Temperature=-196 file.out=relec
Bias       Layer=4 V.Majority=0 dV.Majority=1
Bias       Layer=2 diffusion=1 V.Majority=-20
Bias       Layer=2 diffusion=2 V.Majority=20
Bias       Layer=2 diffusion=2 V.Minority=-20
Bias       Layer=2 diffusion=3 V.Majority=-20
End
Stop                End          of          electrical          simulation.
```

```
Title      Electrical characteristics with charge.
Comment    Poisson solution.
Comment    Initialize structure
Initialize structure=pnp.str
Comment    Electrical card
Electrical steps=10 Temperature=-196 file.out=relec
Bias       Layer=4 V.Majority=0
Bias       Layer=2 diffusion=1 V.Majority=-20
Bias       Layer=2 diffusion=2 V.Majority=20
Bias       Layer=2 diffusion=2 V.Minority=-20
Bias       Layer=2 diffusion=3 V.Majority=-20 dV.Majority=2
End
```

Stop End of electrical simulation.

Appendix B

```
Title       SUPREM III simulation.  P-P DSI IMAGER
Comment       Structure definition (1.0 mu).
Comment       Initialize the bottom layer.
Initialize  Aluminum thickness=0.002
Comment       Define silicon/aluminum constants to get 0.22ev.
Silicon      band.gap=1.166 affinity=4.05
Aluminum      Work.fun=4.996
Comment       Deposit silicon bulk.
Deposit      Silicon <100> boron concentration=1.5e13
+           thickness=18 dx=0.05
Comment       Put the buried layer.
Implant      boron dose=1.0e12 energy=150
Diffusion    temperature=950 time=200
Comment       Deposit gate oxide
Deposit      oxide thickness=0.1
Deposit      polysilicon bor conc=1e20 thickness=0.5 temperature=600
Comment       Output statements
Print       layer
Print       chemical concentr bor filename=bor.con
Print       chemical concentr net filename=net.con
Save         structure file=pp.str
Stop         End of simulation.
```

Appendix B

```
Title      Electrical characteristics empty well.
Comment    Poisson solution.
Comment    Initialize structure
Initialize structure=pp.str
Comment    Electrical card
Electrical steps=10 Temperature=-196 file.out=relec
Bias       Layer=4 V.Majority=0 dV.Majority=1
Bias       Layer=2 V.Majority=-20
End
Stop                End          of          electrical          simulation.
```

```
Title      Electrical characteristics with charge.
Comment    Poisson solution.
Comment    Initialize structure
Initialize structure=pp.str
Comment    Electrical card
Electrical steps=10 Temperature=-196 file.out=relec
Bias       Layer=4 V.Majority=0
Bias       Layer=2 V.Majority=-20 dV.Majority=2
End
Stop       End as electrical simulation.
```

Appendix B

```
Title  Uniform p-implant
OPTION  PLOTDEV=save
Comment   Specify a rectangular mesh
MESH    RECT NX=50 NY=30 DIAG.FLIP SMOOTH=1
X.MESH    N=1  L=0      R=1
X.MESH    N=15  L=8     R=1
X.MESH    N=23  L=13     R=1
X.MESH    N=35  L=22     R=1
X.MESH  N=50 L=30      R=1
Y.MESH  N=1  L=-0.05 R=1
Y.MESH  N=3  L=0      R=1
Y.MESH  N=20 L=10      R=1
Y.MESH  N=30 L=25     R=1
Comment Specify oxide and silicon regions
REGION  NUM=1 IX.LO=1 IX.HI=50 IY.LO=1 IY.HI=3  OXIDE
REGION  NUM=2 IX.LO=1 IX.HI=50 IY.LO=3 IY.HI=30 SILICON
Comment   Electrode definition
ELECTR  NUM=1 IX.LO=1  IX.HI=23  IY.LO=1  IY.HI=1
ELECTR  NUM=2 IX.LO=35 IX.HI=50 IY.LO=1  IY.HI=1
ELECTR    NUM=3 IX.LO=1  IX.HI=50 IY.LO=30 IY.HI=30
Comment Specify impurity profiles and fixed charge
DOPING    REG=2 P.TYPE CONC=1.0E13 UNIFORM OUTF=ilt1.dop
DOPING    REG=2 P.TYPE GAUSSIAN CONC=5.0E15 CHAR=4.0
DOPING    REG=2 N.TYPE GAUSS CONC=2E16 JUNC=4 RATIO.LAT=0.1
+       X.LEFT=8.0 X.RIGHT=22
DOPING    REG=2 P.TYPE CONC=1E19 GAUSSIAN CHARAC=0.25
```

```
+            X.LEFT=0 X.RIGHT=8.0 RATIO.LAT=0.6
DOPING   REG=2 P.TYPE CONC=1E19 GAUSSIAN charac=0.25
+            X.left=22 X.RIGHT=30 RATIO.LAT=0.6
INTERFACE QF=1E10
PLOT.2D   Boundary no.fill no.top grid pause
Comment   Regrid on doping
REGRID   DOPING ABS LOG IGN=1 RATIO=2 SMOOTH=1 DOPF=ilt1.dop
+      OUTF=ilt2.mesh
PLOT.2D   Boundary no.fill no.top grid pause
Comment   Specify Contacts, materials, and models
CONTACT NUM=1 P.POLY
CONTACT NUM=2 P.POLY
CONTACT NUM=3 TU.DISILICIDE
MATERIAL REG=2 AFFINITY=3.90 EG300=1.12
Comment   Symbolic factorization, solve, regrid on potential
SYMBOL   CARRIERS=0
SOLVE    INIT OUTF=ilt2.sol
PLOT.1D   DOPING X.START=15 X.END=15 Y.START=0 Y.END=25
+            LOG ABS MIN=10 MAX=20
END
```

Appendix B

```
Title  PISCES INPUT DECK - DSI ILT IMAGER
Comment OPTIONS PLOTDEV=psraw
Comment   Read in simulation mesh
MESH      INFILE=ilt2.mesh
Comment   These to override defaults to match LOADFILE.
INTERFACE QF=1E10
CONTACT NUM=1 P.POLY
CONTACT NUM=2 P.POLY
CONTACT NUM=3 TU.DISILICIDE
MATERIAL REGION=2 AFFINITY=3.90 EG300=1.12
Comment   Use Newton's method for the solution
SYMB      CARRIERS=0
METHOD  ITLIMIT=60
Comment   Read in saved solution
LOAD      INFILE=ilt2.sol
SOLVE   V1=0 V2=0 V3=0 N.BIAS=0 P.BIAS=-1 previous OUTF=QFERMI.1
SOLVE   V1=0 V2=0 V3=0 N.BIAS=0 P.BIAS=-2 previous OUTF=QFERMI.2
SOLVE   V1=0 V2=0 V3=0 N.BIAS=0 P.BIAS=-3 previous OUTF=QFERMI.3
SOLVE   V1=0 V2=0 V3=0 N.BIAS=0 P.BIAS=-4 previous OUTF=QFERMI.4
SOLVE   V1=0 V2=0 V3=0 N.BIAS=0 P.BIAS=-5 previous OUTF=QFERMI.5
SOLVE   V1=0 V2=0 V3=0 N.BIAS=0 P.BIAS=-6 previous OUTF=QFERMI.6
SOLVE   V1=0 V2=0 V3=0 N.BIAS=0 P.BIAS=-7 previous OUTF=QFERMI.7
SOLVE   V1=0 V2=0 V3=0 N.BIAS=0 P.BIAS=-8 previous OUTF=QFERMI.8
SOLVE   V1=0 V2=0 V3=0 N.BIAS=0 P.BIAS=-9 previous OUTF=QFERMI.9
SOLVE   V1=0 V2=0 V3=0 N.BIAS=0 P.BIAS=-10 previous OUTF=QFERMI.10
END
```

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