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INVESTIGATION OF DIFFERENT CMOS DRAM
SENSE AMPLIFIER CONFIGURATIONS IN VLSI

by
Bihju Chiu

Thesis submitted to the Faculty of the Graduate School of
the New Jersey Institute of Technology in partial fulfillment
of the requirements for the degree of
Master of Science in Electrical Engineering
1988
APPROVAL SHEET

Title of Thesis: Investigation of Different CMOS Sense Amplifier Configurations by Simulation

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ABSTRACT

Title of Thesis: Investigation of Different CMOS Sense Amplifier Configurations by Simulation

Bihju Chiu, Master of Electrical Engineering, 1988

Thesis directed by: Dr. Michael P. Singh.

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Sense amplifiers are particularly difficult circuits to design. In this work, only CMOS sense amplifiers are considered. There are typically two configurations of CMOS sense amplifiers: the cross-connected flip flop configuration and the current-mirror configuration. They are widely used nowadays with various modifications. These improved configurations are simulated and optimized with SPICE package, and their relative performances are also compared in this thesis.
This thesis itself is an acknowledgement to the individuals who have contributed to it.

Dr. Michael Singh, my advisor, has been an inspiration in my writing and learning. He spent many days discussing various approaches and ideas, and also edited the entire text. His philosophy and methods has contributed much to this thesis. For this, I am sincerely grateful.

I also want to thank my parents for their support and love, and wish this thesis will be the most valuable Mother's Day gift.
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CHAPTER ONE INTRODUCTION

Sense amplifiers play a major role in deciding the performance of semiconductor memories. This is specially so in the case of modern high density dynamic memories, whose cells have small storage capacitors and use only a single transistor. The differential voltage available is only of the order of 0.1v or less. The sense amplifiers have to receive the small input voltage and develop a large output voltage within the shortest possible time so that the access time for the memory can be made small. Basically, sense amplifiers are either flip-flops or current mirrors whose output nodes latch into high and low states by regenerative action. There may be a second stage of amplification but invariably the output reaches the data output pad after passing through a buffer.(Fig.1.1)

As shown in Fig.1.2, B/S lines are directly connected to the sense amplifier input node1 and node2. Two transistors M1 and M2 are connected to the dummy cells. B/S lines run symmetrically on both the sides of sense amplifier, connecting the drains of the storage transistors. Just two storage cells are shown in the diagram (represented by C_s). M3 and M4 are their access transistors.

Read cycle starts by precharging B/S lines to a fixed value (V_{PRE}). When the address is placed on the memory chip,
Fig. 1.1

CELL ARRAY  SA1  SA2  BUFFER  DQ PAD

Fig. 1.1
one of the memory cells is selected, say for example, M3 is selected by the word line (P_WS). When a memory cell is selected on one side, the dummy cell is selected on the other side of the sense amplifier. Before selecting, dummy cell is charged to a reference potential (V_{REF}). If the selected memory cell C_s has a stored 'ONE' in it, it is transferred to node1 whereas V_{REF} is transferred to node2. Thus differential voltages are introduced on the opposite sides of the sense amplifier and the sense amplifier starts to work.

Once the latching is completed, dummy cells and B/S lines are precharged to V_{REF} and V_{PRE} for the next cycle.

Nowadays, CMOS technology is used more and more widely in integrated circuits processing, especially when the circuits are of large scale or very large scale integration. Although CMOS does require more complex processing, there are several advantages of using it that are worth the trouble:

1. Very Low Static Power Dissipation:

This is because in a CMOS inverter, the signal inversion is achieved by turning one of the transistors heavily on and simultaneously turning the other off. Since these two devices are in series, only junction leaking currents will be drawn from the power supply in either of the two stable states.
2. High Speed:

   This is achieved by the push-pull operation of the inverter. During switching from logic one to logic zero or vice versa, the node capacitance is always charged or discharged through a heavily conducting MOS transistor.

3. High Noise Immunity:

   The following characteristics produce a very nearly ideal transfer characteristic:

   (1) Symmetry.

   (2) A very high gain in the transition region.

   (3) The very high off/on resistance ratio of the device.

   With CMOS technology permeating all IC fabrication, cells and peripheral circuits in memories have also switched over to CMOS. One type of CMOS sense amplifier is a simple cross-connected CMOS flip-flop circuit.(Fig.1.3) Another type is the current mirror circuit.(Fig.1.4) In practice, however, these simple circuits are modified and the aim of this work is to investigate these new configurations in detail and compare their relative performances. Though these circuits appear in the literature, they are seldom described in detail. Normally they are mentioned in a cursory manner.
The operating conditions such as relative timing between the top and bottom pull up and pull down pulses and the aspect ratios used for the transistors are rarely given. In this work, initially optimal operating conditions and aspect ratios for various transistors are arrived at. Then the speed of these circuits are compared for the same input and output conditions. Conclusions such as these and others regarding optimum aspect ratios will be of immense practical value for memory designers.
CHAPTER TWO  THE CMOS FLIP FLOP SENSE AMPLIFIERS

2.1 The Standard Form

2.1.1 Principle of Operation

Fig.1.3 shows the standard CMOS flip flop sense amplifier, which consists of 3 NMOS and 3 PMOS transistors. MP1 and MP2 are PMOS load transistors whose W/L ratios will be called B_L0, MN1 and MN2 are NMOS driver transistors whose W/L ratios will be called B_D1. MP1, MP2 and MN1, MN2 are two perfectly matched pairs. MPU and MPD are PMOS pull-up transistor and NMOS pull-down transistor with B_PU and B_PD as W/L ratio respectively.

C_BS is a 1PF load capacitor, V(1) and V(2) are the voltages at nodes 1 and 2 respectively. P_PU and P_PD are the gate clock pulses of MPU and MPD. Both of them have the same delay time and then change to 0V and V_DD abruptly. V_DD is 5V from the power supply.

The initial values of V(1) and V(2) are V_I1 and V_I2, and V_I1 < V_I2. (Let's assume they are 2.4 and 2.5) When P_PD rises to V_DD, MPD conducts and node 6 is pulled down to the ground. At this time, MP1, MP2, MN1 and MN2 are all on. Since V_I2 is higher than V_I1, MN1 conducts more than MN2, V(1) decreases faster than V(2). And because V(1) decreases faster than V(2), the VGS of MP2 becomes higher than that of
MP1 and MP2 conducts more than MP1. It makes $V(2)$ to rise faster than $V(1)$. When $V(1)$ finally reaches $V_t$, MN2 stops conducting, $V(2)$ rises much faster until finally it reaches $V_{DD}$ and $V(1)$ continues to decrease since MN1 is still on, until it finally reaches a value close to zero.

2.2 The Modified Forms

The bit line capacitance, i.e. the capacitance of the line which runs all along the memory cell array, loads the latching nodes. The amplifier must be able to drive these large capacitances on the two nodes. This severely degrades the sensing time. Modified versions of the CMOS flip-flop sense amplifiers avoid this capacitive load. One way is to insert isolation nodes as shown in Fig.2.1. (McAdams 1986; Miyamoto 1986; Kimura 1987) When the sense amplifier is enabled, the isolation transistors are turned off to isolate the nodes which latch.

Another approach is to separate the p channel cross-connected transistors from the n channel cross-connected transistors with the help of separation transistors as shown in Fig.2.2 (Furuyama 1986; Fujii 1986; Miyamoto 1987). The bit line capacitance is connected to the p channel transistors but the latching nodes at the n channel cross connections do not face this large capacitance directly.
Fig. 2.1
Fig. 2.2
2.3 Simulation Results

2.3.1 Clock Timings

Simulations show that for both the modified configurations, there is not much advantage in relatively delaying the pull-up and the pull-down clocks. They can be simultaneous. Though the pull up may be delayed in case of the first configuration which uses isolation transistors, delay of pull down clock adds a dead time and makes the sensing process inefficient. For the relative timing between turning off the isolation transistor and turning on the flip flop sense amplifier (pull up and pull down transistors), again simultaneous operation is seen to be optimum. Turning off the isolation transistor may be delayed, say, by 1NS with respect to the pull up and pull down and the performance slightly improves. Turning the isolation transistor much later or much earlier worsens the performance since the large capacitance of the bit sense lines impede rapid changes in the voltages of the latching nodes. For the isolation and separation transistors, PMOS was seen to give better results than NMOS. PMOS can take a node to \( V_{DD} \) easily.

2.3.2 Voltage Levels

Optimum common mode input signal is seen to be 5V. This is expected since higher voltages make the driver transistors
to conduct faster and the low going node reaches the threshold voltage earlier. Also greater the differential input signal, better is the performance and this is obvious.

2.3.3 Aspect Ratios

The NMOS driver transistors, if they have higher aspect ratios, the latching process will be faster. Simulations show that increasing $W/L$ greater than 4 does not result in much superior performance. Therefore the optimum value is chosen as 4. For the pull up and pull down transistors, again, higher $W/L$ values will be better since they will take the nodes closer to the rails quickly. The final $V_{OL}$ and $V_{OH}$ will also be better due to potential division of transistor resistances. Increasing above 4 did not result in much enhanced performance and so 4 is chosen as the optimum. The load transistors do not play that much role and a minimum size with $W/L=1$ seem to work fine. Increasing the size does not yield much better performance. The isolation and separation transistors have an optimum $W/L$ of 1. Increasing the size further does not appreciably alter the performance.

2.3.4 Comparative Performance

For the optimized clock timings, voltage levels and aspect ratios, the two circuits are simulated for the same output load capacitance of 0.1PF. Differential input voltage
is fixed at 200mV. The SPICE parameters are taken from (Glasser 1985) and L is 2 um. Fig.2.3 gives the results. The first configuration with isolation transistor is clearly the winner. Latching process is completed much earlier. The second configuration with separation transistors has added resistances in the main paths and that will be causing additional delays.
Fig. 2.3

(1) standard form
(2) with separate transistors
(3) with isolation transistors
3.1 The Standard Form

3.1.1 Principle of Operation

Fig.1.4 is a standard current mirror sense amplifier. (Donoghue 1985; Yamamoto 1985; Kobayashi 1985; Kayano 1986) It is also used as front-end in operational amplifiers. It detects voltage difference, rather than absolute values.

The current mirror sense amplifier consists of two PMOS and three NMOS transistors. MP1 and MP2 are PMOS load transistors with $B_{LO}$ as W/L ratios, MN1 and MN2 are NMOS driver transistors whose W/L ratios will be called $B_{DR}$ later. $M_{PD}$ is NMOS pull-down transistor with $B_{PD}$ as W/L ratio.

MP1, MP2 and MN1, MN2 are two perfectly matched pairs. (Annaratone, 1986) $C_{BS1}$ and $C_{BS2}$ are 1PF load capacitors. $V(1)$ and $V(2)$ are the voltages at node 1 and 2 respectively. $P_{PD}$ is the gate clock pulse of MPD. $V_{DD}$ is 5V from the power supply. The initial values of $V(1)$, $V(2)$ and $V(5)$ are $V_{I1}$, $V_{I2}$ and $V_{I5}$.

The bit line is connected to node 1, and its reference value is connected to node 2. Initially, node 7 is 0V, $M_{PD}$
is off. Before it begins to work, node 1, 2 and 5 are precharged to fixed values. After $V(7)$ is pulled up, the circuits starts to work. If $V_{i2}$ is lower than $V_{i1}$, MN2 conducts poorer, and $V_5$ begins to charge up and approaches to $V_{OH}$. If $V_{i2}$ is higher than $V_{i1}$, MN2 conducts better than MN1, $V_5$ starts to discharge, and finally reaches a value near zero.

This kind of circuit is called current mirror amplifier because when both load transistors are in saturation mode, the ratio of the current flowing through the drains of both loads is equal to the ratio of their beta values. If the beta value of both transistors are the same, the current flowing through both transistors will also be equal.

If $V_{i1}$ is higher than $V_{i2}$, the current flowing through MN1 will be duplicated to MP2. The current flowing through MN2 is smaller than that of MN1 and so the extra current will flow through node 5 to charge up $C_5$.

When $V_{i1}$ is smaller than $V_{i2}$, the current flowing through MN1 is smaller and is duplicated to MP2. The current flowing through MN2 is larger than that of MN1 and so $C_5$ will be discharged. Thus this circuit can work better with the help of current mirror load than a normal differential amplifier which does not have the current mirror action.
3.1.2 Simulation Results For The Standard Current Mirror Circuit:

Voltage Levels:

The optimum precharged voltages for $V_1$, $V_2$ and $V_5$ are decided by the following procedure: at first, common mode voltage of $V_{I1}$ and $V_{I2}$ is changed, $V_5$ is not precharged so the optimum DC output value can be decided by DC analysis. The best output is decided from the difference of $V_5$(high) and $V_5$(low) when $V_{I1} > V_{I2}$ and $V_{I1} < V_{I2}$. After deciding the optimum $V_{I1}$ and $V_{I2}$, different $V_5$ initial values are assigned and optimum value for $V_{PRE}$ for $V_5$ is decided. Then, the procedure continues to find the optimum value of other parameters such as aspect ratios. After aspect ratios are decided, $V_{I1}$, $V_{I2}$ and $V_{I5}$ are optimized again. For this problem, the best value of $V_{I5}$ turns out to be 2.7V and the common mode of $V_{I1}$ and $V_{I2}$ is 0.7V.

The optimum common mode level of $V_{I1}$ and $V_{I2}$ can be explained as follows:

The optimum value is about the $V_t$ (threshold voltage) of NMOS transistor. This makes the driver transistor with higher initial value to be nearly 'ON' and the other to be 'OFF'. With only one of the drivers 'ON', $C_5$ is either charged up by
MP2 or discharged by MN2. The speed is quicker this way than being charged up by MP2 and discharged by MN2 at the same time. That will happen if \( V_{I1} \) and \( V_{I2} \) are both above \( V_t \). Thus the discrimination of the input voltages begins early if the input voltages are on either side of \( V_t \).

**Aspect Ratios:**

The NMOS driver transistors, if they have higher \( W/L \) ratios, the performance will be better. Simulations show that increasing \( W/L \) greater than 22 does not result in much superior performance. Therefore the optimum value is chosen as 22.

For the pull down transistor, higher \( W/L \) ratio will be better, since it makes the common node closer to the ground rail quickly. After \( W/L \) ratio becomes greater than 4, there is no much change of output, so the optimum value of \( B_{PD} \) is 4.

For PMOS load transistors, however, if \( W/L \) is greater than one, the higher values give worse results; if \( W/L \) is smaller than one, the smaller values give better results, although there is no much change. So the optimum value of \( B_{LO} \) is one.

3.2. **The Modified Configurations**:
Fig. 3.1
Fig. 3.2
Fig. 3.3
Fig. 3.4
Fig. 3-1, 3-2, 3-3 and 3-4 show four different types of modified forms derived from the standard circuit.

3.2.1 **Complementary Form**

3.2.1.1 **Schematic**

Fig. 3-1 shows the structure of one modified form from the standard circuit. (Furuyama 1987; Ohtsuka 1987) It is almost the inverse of the standard one with PMOS pull-up transistor and the bit lines connected to the gate of the PMOS 'load' transistors (which act as drivers).

3.2.1.2 **Simulation Results:**

3.2.1.2.1 **Voltage Level:**

With the same procedure as for the standard form, simulations reveal that the common mode of $V_{I1}$ and $V_{I2}$ is about 4.2V, and $V_{I5}$ is 4.9V. The voltage level is much higher than that of the standard form.

The optimum common mode value of $V_{I1}$ and $V_{I2}$ can be explained as follows:

The optimum value can make the $V_{GS}$ value of both PMOS
transistors about \( V_t \). This makes one of the 'loads' (drivers) to be nearly 'ON' and the other to be 'OFF' and let \( C_5 \) to be either charged up by MP2 or discharged by MN2. This will initiate discrimination earlier and speed up the process.

Aspect Ratios:

The NMOS 'driver' transistors, (which act as loads) if they have lower \( W/L \) ratios, the performance will be better. But the NMOS transistors have to support the heavy currents flowing from the top PMOS transistors. Simulations show that increasing \( W/L \) greater than 12 does not result in much superior performance. Therefore the optimum value of \( B_{DR} \) is chosen as 12.

For the pull-up transistor, higher \( W/L \) ratio will be better, the reason being the same as the standard form. The optimum value of \( B_{PD} \) is 4.

For the PMOS 'load' transistor which act as drivers higher \( W/L \) value can give better performance. The optimum value of \( B_{LO} \) is 24.

3.2.2 Circuits With Level Shifting Transistors

3.2.2.1 Schematic
Fig. 3-2 and 3-3 show two other modified current mirror sense amplifiers. (Matsui 1987) They are almost the same as the standard form but with a pair of level shifting transistors interposed either above or below the driver transistors.

In Fig. 3-2, the level shifting transistors are added between PMOS load and NMOS driver transistors, while in Fig. 3-3, the level shifting transistors are added below the NMOS driver transistors.

3.2.2.2 Simulation Results :

3.2.2.2.1 Voltage Level :

With the same procedure before, the common mode of $V_{I1}$ and $V_{I2}$ of both configurations are around 0.7V, i.e. the same as that of the standard form. This result is rather unexpected since the presence of extra transistors is said to shift the common mode voltage. (Matsui 1987) The $V_{I5}$ of Fig. 3-2 is 3.1V, and that of Fig. 3-3 is 2.0V. The precharge level of the output node seems to get shifted. However, the performance did not change significantly with $V_{I5}$.

3.2.2.2.2 Aspect Ratios :

For the NMOS driver transistors of both circuits, if
they have higher W/L ratio, the performance will be better. And the optimum value of $B_{DR}$ is 22, which is the same as the standard form.

For the pull-down transistors of both circuits, again, higher W/L is better and optimum value is about 4.

For the PMOS load transistors of both circuits, neither higher nor lower W/L gives better performance and so the optimum value of both are one.

For the level shifting transistors of Fig.3-2, neither higher nor lower W/L ratio gives better performance. So the optimum value is one. For the circuit of Fig.3-3, if W/L ratio of the level shifting transistor is higher, the performance is better. Optimum value is around 4. This may be due to the fact that the bottom transistors need to pass the large currents that are possible with the drivers. Simulations also showed that NMOS is better than PMOS for the level shifting transistors. This is so because NMOS is good for pulling down. PMOS is good for pulling up a node. PMOS when present in the discharge path (to the ground) will offer higher resistance and slow down the process.

3.2.3 Circuit With Additional Transistors Across The Loads

3.2.3.1 Circuit Diagram
Fig. 3-4 shows another type of modified circuit. (Wada 1987) It is the same as the standard form but there is another pair of PMOS load transistors with their gates connected to the bit line or the inverted bit line. The additional two PMOS transistors can help the circuit to get additional gain. For example, when $V_{I1}$ is greater than $V_{I2}$, the current flowing through MN1 increases and that of MTR1 decreases (its gate voltage being higher). This causes the current flowing through MP1 to increase. This increased current is duplicated by MP2. $V_{I2}$ being lower, makes the current flowing through MN2 to decrease. The current charging up $C_5$ is much bigger than that of the standard form and thus there is additional gain.

3.2.3.2 Simulation Results:

3.2.3.2.1 Voltage Level:

With the same procedure as before, the common mode value of $V_{I1}$ and $V_{I2}$ is 2.6V, and precharge value for $V_{I5}$ is 2.3V.

3.2.3.2.2 Aspect Ratios:

For the NMOS driver transistors, neither higher nor lower W/L ratios would worsen the result. So the optimized value of $B_{DR}$ is one. This result is in complete contrast
with the other modified forms.

For the pull down transistor, again, there is no advantage in increasing or decreasing the W/L ratio. The optimum value of \( B_{PD} \) is one. This again is in contrast to previous results.

For the regular PMOS load transistor, if W/L ratio is higher, the performance is a little bit better, but it makes not much difference. So the optimum value of \( B_{LO} \) is one.

For the additional PMOS load transistor pair, neither higher nor lower W/L ratio will make the performance better. So the optimum value is one. The above results are surprising. This means that this configuration will occupy the least area. The performance with smaller area may be attributed to the extra gain as explained in 3.2.3.1.

3.2.4 Comparative Performance:

Fig.3-5 shows the performance of the standard and modified sense amplifiers with their optimized parameters.

3.2.4.1 Output Level:

It appears that the differential output voltage of the following sense amplifiers: (1) The standard form, (2) The
(1) standard form
(2) complimentary form
(3) level shift transistors
   between loads and drivers
(4) level shift transistors
   between drivers and pull-down
(5) additional PMOS transistors
   across the loads

Fig. 3.5
level shifting forms and (3) The complementary form are around 5V, and that means the V(5)(high) can approach 5V, and V(5)(low) can approach 0V. So they are good enough. But the performance of the circuit with additional transistors across the loads is not so good. It is about 3.0V, which means the V_5(high) can only approach about 4V, and V_5(low) can only approach about 1V.

3.2.4.2 Switching Speed:

It appears that all these circuits have almost the same speed, while the speed of the circuit with level shifting transistors between driver and pull-down transistor is a little slower than others. The reason may be the additional resistance in the discharge path.

Size:

Table 3-1 shows that the size of the circuit with additional transistors across the loads is the smallest. It can still have the same speed as others in approaching the final values.

Initial Levels:

Table 3-1 shows another important comparison of V_{I1}, V_{I2} and V_{I5}. Circuits in the following: (1) The standard form
and (2) The level shifting form, have the same low $V_{I1}$ and $V_{I2}$. While $V_{I5}$ in the standard form is 2.7V, in the circuit with level shifting transistors between the loads and drivers, it is 3.1V and in the circuit with level shifting transistors between the drivers and pull-down transistor, it is 2.0V.

The $V_{I1}$, $V_{I2}$ and $V_{I5}$ of the circuit in the complementary form is the highest, and those of the circuit with additional transistors across the loads is around the middle value (2.5V).
CHAPTER FOUR  CONCLUSION

Two modified CMOS flip flop sense amplifier configurations are investigated in this work. Optimum operating conditions and aspect ratios are obtained and the performances of the two circuits are compared for the same input and output conditions. The sense amplifier that uses the isolation transistors outperforms the other configuration that uses the separation transistors. The separation transistors, though they are ON, add some delay and resistance and the latching process gets slightly delayed. Also the large capacitances of the bit sense lines are not fully isolated from this circuit during the latching process. Therefore the performance is expected to be inferior to the other configuration.

In case of current mirror sense amplifiers, five different configurations are investigated in detail and their optimized parameters are obtained. The optimum common mode input values of the standard form and the complimentary form make the $V_{GS}$ of the drivers about $V_t$. This makes only one driver 'ON' at one time and can speed up the charging or discharging action of the load capacitance. The circuit with additional PMOS transistors across the load transistors has the smallest area. Therefore any one wanting the minimum area should go for this one. Though $V_{OH}$ and $V_{OL}$ are not as good as those of others, this circuit can be used as the
<table>
<thead>
<tr>
<th></th>
<th>STANDARD FORM</th>
<th>COMPLEMENTARY FORM</th>
<th>LEVEL SHIFTING BETWEEN LOADS AND DRIVERS</th>
<th>LEVEL SHIFTING BETWEEN DRIVERS AND PULL-DOWN</th>
<th>ADDITIONAL TRANSISTORS ACROSS LOADS</th>
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</thead>
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<td>VREF</td>
<td>0.8 0.6 2.7</td>
<td>4.0 4.1 4.2</td>
<td>0.2 0.5 2.1</td>
<td>0.3 0.6 2.0</td>
<td>2.7 2.5 2.3</td>
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<tr>
<td>BDR</td>
<td></td>
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<td></td>
<td>44/2</td>
<td>1</td>
</tr>
<tr>
<td>BLQ</td>
<td></td>
<td></td>
<td></td>
<td>48/1</td>
<td>1</td>
</tr>
<tr>
<td>BPD</td>
<td></td>
<td>8/2</td>
<td></td>
<td>8/2</td>
<td>1</td>
</tr>
<tr>
<td>BTR</td>
<td></td>
<td>x</td>
<td></td>
<td>8/2</td>
<td>1</td>
</tr>
<tr>
<td>SPEED</td>
<td></td>
<td>1</td>
<td></td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>FINAL</td>
<td></td>
<td></td>
<td></td>
<td>3</td>
<td>5</td>
</tr>
</tbody>
</table>

Table 3.1
first stage. The second stage can take care of the final high and low values.

Not all simulations have been thoroughly explained and this is a fertile field of investigation for future researchers.
SELECTED BIBLIOGRAPHY


Miyamoto J. et al, "An Experimental 5v only 256K bit CMOS


APPENDIX

CMOS2/ALL SENSE AMPLIFIER
VDD 4 0 5V
V7 7 0 5V
C501 501 0 0.1PF
C502 502 0 0.1PF
C503 503 0 0.1PF
C504 504 0 0.1PF
C505 505 0 0.1PF
C506 506 0 0.1PF
C507 507 0 0.1PF
C508 508 0 0.1PF
C509 509 0 0.1PF
C510 510 0 0.1PF
CLA101 101 0 1PF
CLA201 201 0 1PF
CLA102 102 0 1PF
CLA202 202 0 1PF
CLA103 103 0 1PF
CLA203 203 0 1PF
CLA104 104 0 1PF
CLA204 204 0 1PF
CLA105 105 0 1PF
CLA205 205 0 1PF
CLA106 106 0 1PF
CLA206 206 0 1PF
CLA107 107 0 1PF
CLA207 207 0 1PF
CLA108 108 0 1PF
CLA208 208 0 1PF
CLA109 109 0 1PF
CLA209 209 0 1PF
CLA110 110 0 1PF
CLA210 210 0 1PF
MN101 301 101 601 601 N L=2U W=44U
MN201 501 201 601 601 N L=2U W=44U
MN102 302 102 602 602 N L=2U W=2U
MN202 502 202 602 602 N L=2U W=2U
MN103 803 103 603 603 N L=2U W=44U
MN203 903 203 603 603 N L=2U W=44U
MN104 304 104 804 604 N L=2U W=44U
MN204 504 204 904 604 N L=2U W=44U
MN105 305 305 0 0 N L=2U W=24U
MN205 505 305 0 0 N L=2U W=24U
MN106 306 106 606 606 N L=2U W=44U
MN206 506 206 606 606 N L=2U W=44U
MN107 307 107 607 607 N L=2U W=2U
MN207 507 207 607 607 N L=2U W=2U
MN108  808  108  608  608  N  L=2U  W=44U
MN208  908  208  608  608  N  L=2U  W=44U
MN109  309  109  809  609  N  L=2U  W=44U
MN209  509  209  909  609  N  L=2U  W=44U
MN110  310  110  0   0   N  L=2U  W=24U
MN210  510  110  0   0   N  L=2U  W=24U
MNA03  303  4   803  603  N  L=2U  W=2U
MNB03  503  4   903  603  N  L=2U  W=2U
MNA04  804  4   604  604  N  L=2U  W=8U
MNB04  904  4   604  604  N  L=2U  W=2U
MNA08  308  4   808  608  N  L=2U  W=2U
MNB08  508  4   908  608  N  L=2U  W=2U
MNA09  809  4   609  609  N  L=2U  W=8U
MNB09  909  4   609  609  N  L=2U  W=8U
MP101  301  101  4   4   P  L=2U  W=2U
MP201  501  301  4   4   P  L=2U  W=2U
MP102  302  102  4   4   P  L=2U  W=2U
MP202  502  302  4   4   P  L=2U  W=2U
MPA02  302  102  4   4   P  L=2U  W=2U
MPB02  502  202  4   4   P  L=2U  W=2U
MP103  303  303  4   4   P  L=2U  W=2U
MP203  503  303  4   4   P  L=2U  W=2U
MP104  304  304  4   4   P  L=2U  W=2U
MP204  504  304  4   4   P  L=2U  W=2U
MP105  305  105  605  605  P  L=2U  W=48U
MP205  505  205  605  605  P  L=2U  W=48U
MP106  306  306  4   4   P  L=2U  W=2U
MP206  506  306  4   4   P  L=2U  W=2U
MP107  307  307  4   4   P  L=2U  W=2U
MP207  507  307  4   4   P  L=2U  W=2U
MPA07  307  107  4   4   P  L=2U  W=2U
MPB07  507  207  4   4   P  L=2U  W=2U
MP108  308  308  4   4   P  L=2U  W=2U
MP208  508  308  4   4   P  L=2U  W=2U
MP109  309  309  4   4   P  L=2U  W=2U
MP209  509  309  4   4   P  L=2U  W=2U
MP110  310  310  610  610  P  L=2U  W=48U
MP210  510  210  610  610  P  L=2U  W=48U
MPD1  601  7   0   0   N  L=2U  W=8U
MPD2  602  7   0   0   N  L=2U  W=8U
MPD3  603  7   0   0   N  L=2U  W=8U
MPD4  604  7   0   0   N  L=2U  W=8U
MPD5  605  0   4   4   P  L=2U  W=8U
MPD6  606  7   0   0   N  L=2U  W=8U
MPD7  607  7   0   0   N  L=2U  W=2U
MPD8  608  7   0   0   N  L=2U  W=8U
MPD9  609  7   0   0   N  L=2U  W=8U
MPD10 510 0   4   4   P  L=2U  W=8U
.MODEL  N  NMOS  LEVEL=3  RSH=0  TOX=225E-10  LD=0.15E-6
+  XJ=0.21E-6  CJ=1.0E-4   CJSW=1.25E-10  UO=650  VTO=0.628
+  CGSO=2.3E-10  CGDO=2.3E-10  NSUB=3E15
+  THETA=0.06  KAPPA=0.4  ETA=0.14  VMAX=17E4
+  PB=0.7  MJ=0.5  MJSW=0.3  NFS=1E10
.MODEL  P  PMOS  LEVEL=3  RSH=0  TOX=225E-10  LD=0.4E-6
+ XJ=0.6E-6 CJ=6E-4 CJSW=3.75E-10 U0=220 VTO=-0.668
+ CGSO=6.2E-10 CGDO=6.2E-10 TPG=-1 NSUB=5E15
+ THETA=0.03 KAPPA=0.4 ETA=0.06 VMAX=17E4
+ PB=0.7 MJ=0.5 MJSW=0.3 NFS=1E10
+ IC V(101)=0.8V V(201)=0.6V V(501)=2.7V
+ IC V(102)=2.7V V(202)=2.5V V(502)=2.3V
+ IC V(103)=0.8V V(203)=0.6V V(503)=3.1V
+ IC V(104)=0.8V V(204)=0.6V V(504)=2.0V
+ IC V(105)=4.3V V(205)=4.1V V(505)=4.9V
+ IC V(106)=0.6V V(206)=0.8V V(506)=2.7V
+ IC V(107)=2.5V V(207)=2.7V V(507)=2.5V
+ IC V(108)=0.6 V(208)=0.8V V(508)=3.1V
+ IC V(109)=0.6 V(209)=0.8 V(509)=2.0V
+ IC V(110)=4.1 V(210)=4.3 V(510)=4.9V
+ WIDTH OUT=80
+ TRAN 2NS 100NS
+ PRINT TRAN V(501) V(502) V(503) V(504) V(505)
+ PRINT TRAN V(506) V(507) V(508) V(509) V(510)
+ PRINT TRAN V(501,506) V(502,507) V(503,508) V(504,509)
+ V(505,510)
+ PLOT TRAN V(501) V(502) V(503) V(504) V(505) (0 5)
+ PLOT TRAN V(506) V(507) V(508) V(509) V(510) (0 5)
+ PLOT TRAN V(501,506) V(502,507) V(503,508) V(504,509)
+ V(505,510) (0,5)
+ END