A SILICON PHOTODIODE ARRAY
FOR SOFT X-RAY SENSING

by
Chih-te Hu

Thesis submitted to the Faculty of the Graduate School of
the New Jersey Institute of Technology in partial fulfillment of
the requirements for the degree of
Master of Science in Electrical Engineering
1988

APPROVAL SHEET

Title of thesis: A SILICON PHOTODIODE ARRAY FOR SOFT X-RAY
SENSING

Name of candidate: CHIH-TE HU
MASTER OF SCIENCE
IN ELECTRICAL ENGINEERING, 1988

Abstract and thesis approved:

_____   _____
Dr. W. N. Carr   Date
Professor

_____   _____
Dr. O. L. Russo   Date
Associate Professor

_____   _____
Dr. J. M. Grow   Date
Associate Professor

VITA

Name: CHIH-TE HU

Degree and date to be conferred: MASTER OF SCIENCE
IN ELECTRICAL ENGINEERING
MAY 1988

Collegiate Institutions Attended:

Name	Date	Degree	Date of Degree
New Jersey Institute of Technology	Sept.1986 to May 1988	MSEE	May 1988
St. John's and St. Mary's Institute of Technology	Sept.1977 to June 1983	EE Diploma	June 1983

Major: ELECTRICAL ENGINEERING

ABSTRACT

Title of Thesis: A SILICON PHOTODIODE ARRAY FOR
SOFT X-RAY SENSING

CHIU-TE HU, MASTER OF SCIENCE IN ELECTRICAL ENGINEERING, 1988

Thesis directed by: W. N. Carr, Ph.D.
Professor

An array of 30 × 30 sensing cells including logic within each cell and a self-scan address circuit are described. A unique scintillation technique is used to increase the threshold sensitivity 60dB for X-ray photon sensing beyond that obtainable with conventional photodiode sensors. Simulations for the sensing cell and some additional logic elements are based on SPICE version 2G5 and HILO 3. Worst case analysis includes variations in threshold voltage V_{TP} and V_{TN} for the CMOS circuit components. The final CMOS chip dimension using MOSIS 1.2 micron rules is $10mm \times 10mm$ base on the $80\mu m \times 80\mu m$ sensing cell size.

ACKNOWLEDGMENT

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Chapter I
INTRODUCTION

X-ray sensors in two dimensional arrays are needed for applications in production robotics, computer tomography, crystallography, astronomy, nondestructive quality analysis and many others. The precise requirements for X-ray detectors in these fields vary. However, the need for high spatial resolution, high sensitivity and signal conversion linearity are generally very desirable.

In these applications, the use of a solid detection medium is of great advantage, because the detector dimensions can be kept much smaller than the equivalent gas filled detector. Furthermore, solid state detectors have superior energy resolution, relatively fast timing charateristics and variable effective thickness. This thesis focusses on silicon devices since the development of silicon processing technology has reached a very high standard of sophistication. Also, it is very likely that the cost/performance ratio of silicon technology will continue decreasing in the future.

The use of silicon as an X-ray array sensor began in the 1960's[Chester 69]. Early advances in this technology used a scanning electron beam for readout of the residual charge on each diode. Subsequently, self scanning devices with higher resolution and better sensitivity have been developed [Kosonocky 85, Tsoi 85, Theuwissen 86], but the cost for fabrication is expensive.

The sensor described in this thesis is named SPAX (Silicon Photodiode Array for soft X-ray). Unlike most of the manufactured silicon array sensors which measure average photon current, SPAX measures the intensity of incident X-ray flux by counting individual photons. Corresponding to each incident photon, instant charge is collected on a reverse biased PN junction diode. An in-cell pulse amplifier having a voltage gain

of 500 is used to amplify and shape the signal before it is sent to a ripple counter. In order to obtain the maximum sensitivity and accuracy, the area of PN junction diodes has to be maximum. Thus the principle challenge in designing the pixels is to minimize the size of the in-cell amplifier without greatly decreasing its gain and sensitivity.

A theoretical analysis of X-ray photon interacting with the silicon lattices will be presented. Circuit simulations, worst case analysis and suggested layout will be detailed in latter chapters.

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Chapter II
BACKGROUND THEORY

Although many possible interaction mechanisms are known for X-ray in matter, only three major types play important role in radiation measurments: *photoelectric absorption, Compton scattering* and *pair production*. In pair production process, an incident photon undergoes an electromagnetic interaction with an atomic nucleus and is converted into an electron-positron pair. This process can take place only if the photon energy exceeds a threshold value of 1.022MeV which is twice the rest mass energy of an electron. In Compton scattering, the incoming photon is deflected through an angle with respect to its original direction, and transfers a portion of its energy to the electron. The probability of Compton scattering per atom of the absorber depends on the number of electrons available as scattering targets. It increases linearly with atomic number. However, for soft X-rays, the Compton effect is negligible compare to photoelectric absorption in silicon. Therefore, the major interaction mechanism for soft X-ray in silicon is photoelectric absorption.

2.1 Absorption interaction

As radiation penetrates matter, particles or photons may be removed from the incident beam either by absorption interaction or by those scattering interactions. In general, radiation intensity decreases with distance into the interaction material. The intensity of radiation at distance x is described by the equation:

$$I_{(x)} = I_{(0)}e^{-\alpha x} \tag{1}$$

where $I_{(0)}$ is the original incident radiation intensity, α is the absorption coefficient. For 20KeV X-ray absorption in silicon, α is 10 at room temperature as illustrated in figure 1.
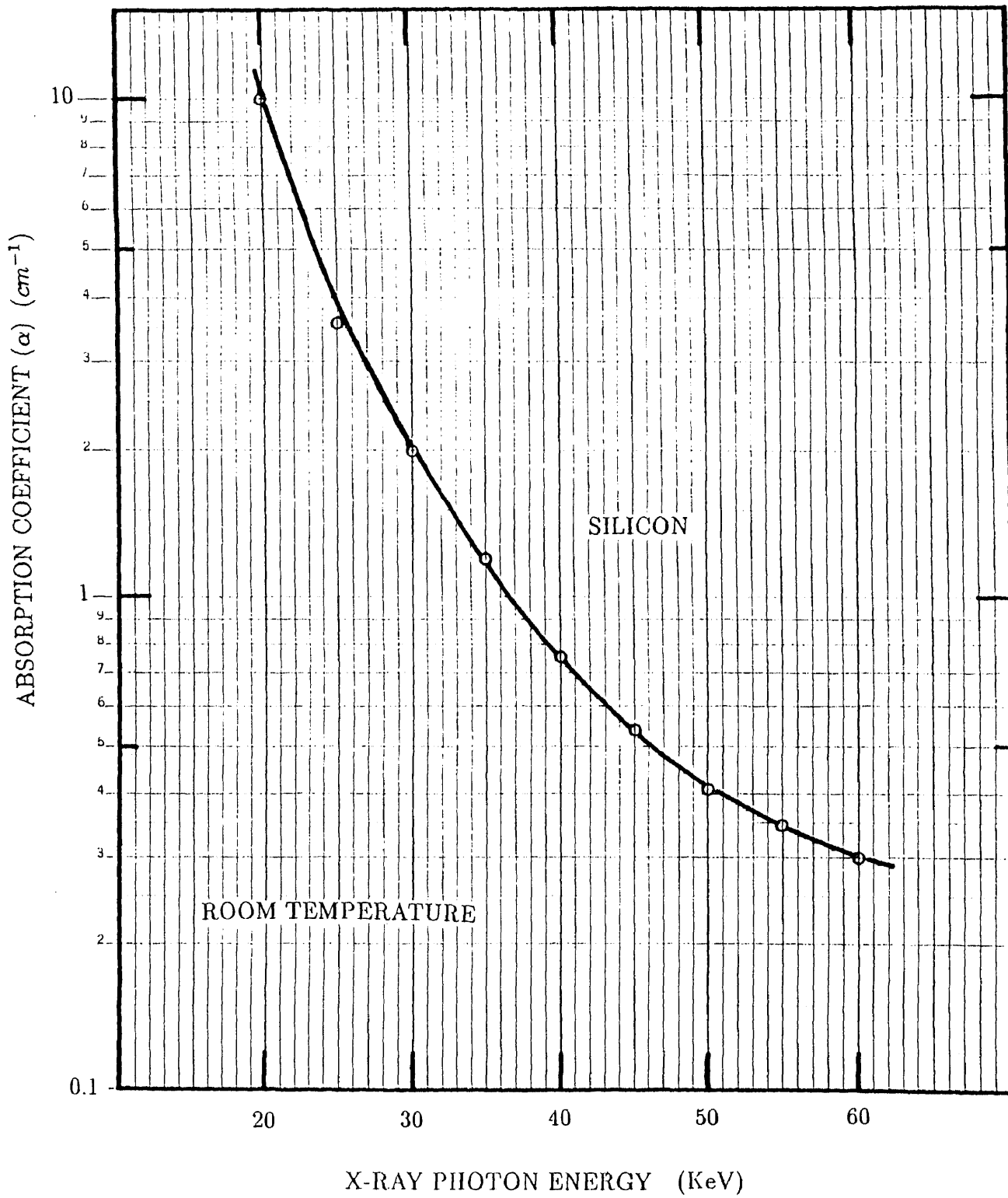
Figure 1: The absorption coefficient for silicon to different energy incident X-ray.
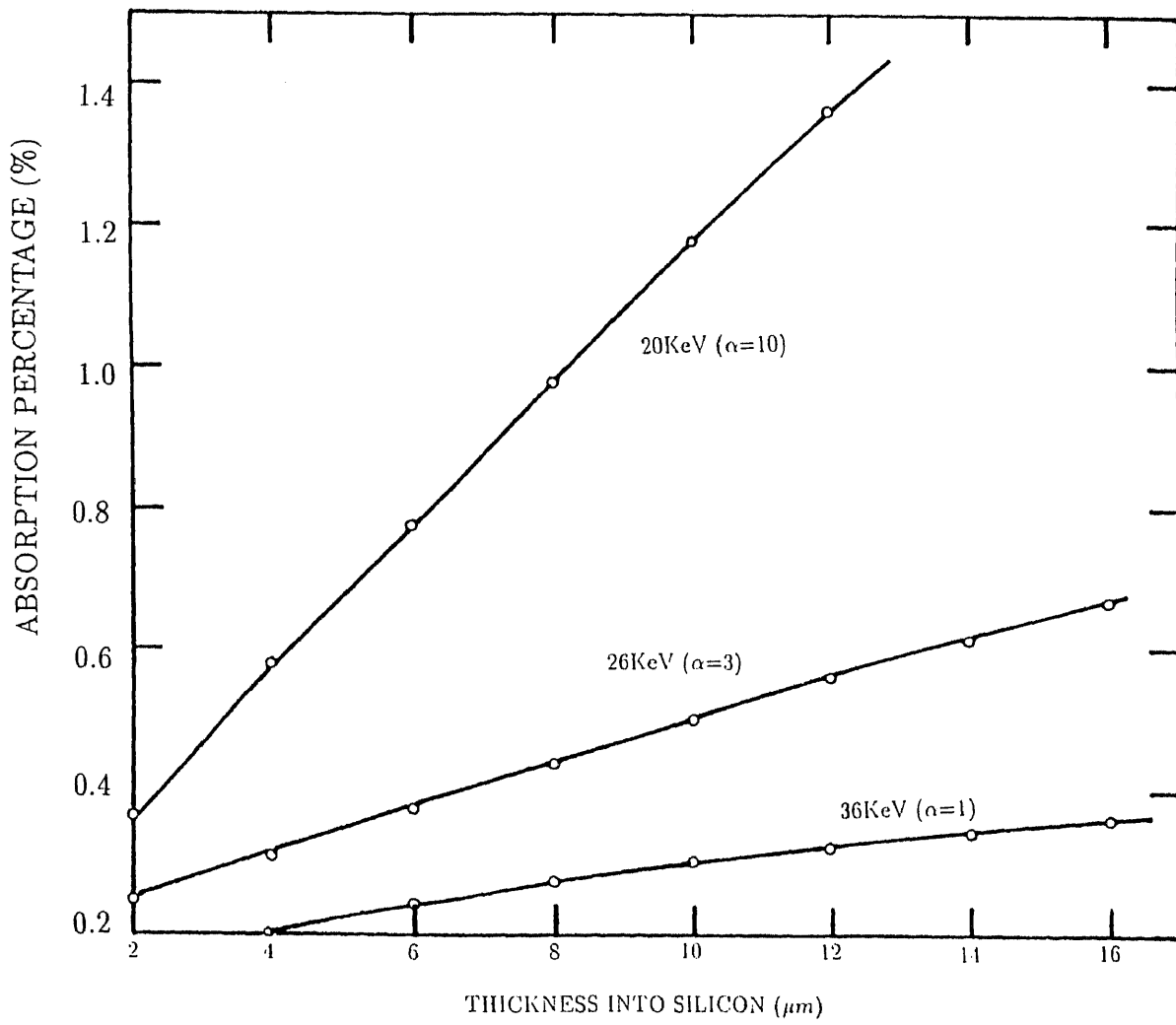
Figure 2: The absorption percentage of different intensity X-ray flux *vs* the depth into silicon

charge collection efficiency is unity, the charge collected within a PN junction is given approximately, by

$$q = ne = \frac{eE}{\epsilon} \tag{6}$$

where E is the X-ray photon energy, n is the number of ion pairs formed and q refers to charge of one sign only.

2.3 Charge collection

If this amount of charge is integrated, a voltage pulse is obtained whose magnitude v is given by

$$v = q/C = \frac{eE}{\epsilon C} \tag{7}$$

where C is the total capacitance between electrodes.

The amplitude of v is inversely proportional to C when X-ray photon energy is specified. In this thesis, PN junctions are used to collect the charge generated by absorbed X-ray photons. If an external reverse bias is applied across the diode, as shown in figure 3, the carriers will be swept rapidly to electrodes by the electric field. Almost all of the applied potential extends across the depletion layer, which acts as the sensitive volume. The square of the depletion width W_d is proportional to the reverse bias across the junction and inversely proportional to the impurity concentration of the bulk:

$$W = \sqrt{\frac{2\epsilon_s(V_{bi} - V)}{qN_B}} \tag{8}$$

where V_{bi} is the build-in potential of the PN junction, ϵ_s is the dielectric constant of silicon times ϵ_0 and N_B is the impurity concentration of bulk.

Due to the diffusion of the minority carriers, which will also contribute to collected charge, the actual charge collecting region W in one dimension, includes the thickness
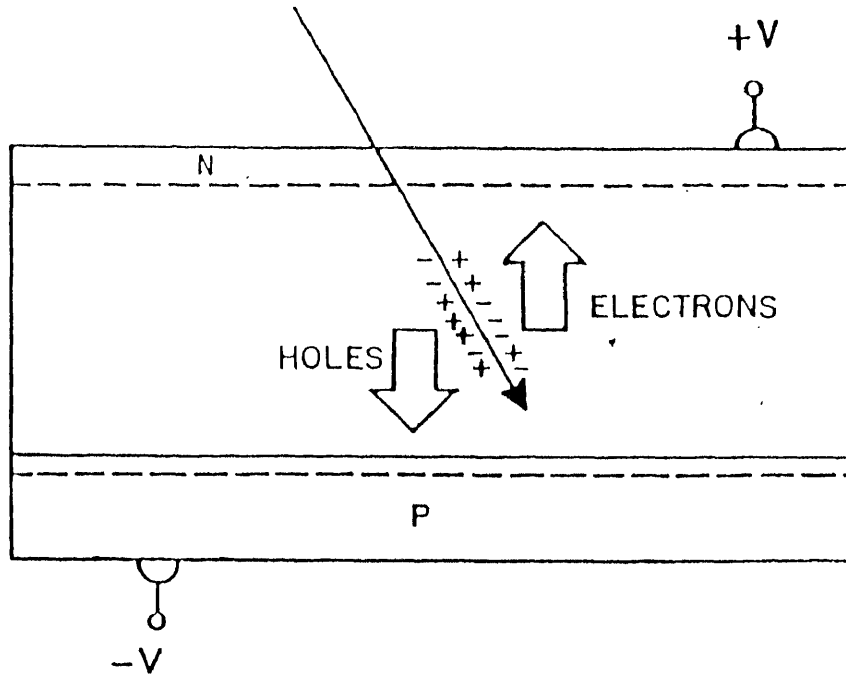
Figure 3: Electrons-hole pairs created by an incident X-ray photon.

of the depletion region plus the diffusion length L of the minority carriers outside the depletion layer.

$$W = W_d + L \tag{9}$$

In general, N_B is about $5 \times 10^{14} cm^{-3}$. When a reverse bias of -9V is applied to this abrupt junction, the depletion width is $4.85 \mu m$. Corresponding to an $1000 \mu m^2$ area, the capacitance is $0.02 pF$. From equation 8, the potential difference across the junction is $38 mV$ for a $20 KeV$ incident X-ray photon.

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Chapter III
COMPARISON WITH
ALTERNATIVE IC TECHNOLOGIES

Solid state imagers can be employed in three basic X-ray imaging topologies, as illustrated in figure 5 namely: (1) direct detection (2) X-ray visible light photon conversion (3) X-ray photon-electron conversion.

3.1 Direct detection

Most solid-state imagers are of the SSPA (Self-Scanned Photodiode Array) type or CCD (Charge Coupled Device) type. Although they are used mainly for detecting visible light, several publications using these already available devices in X-ray detection have been reported[Gamble 79, Koppel 76]. The advantages of these devices are good resolution, good linearity and fast response. However, they often suffer from radiation damage and may exhibit increases in dark current which is a consequence of the direct exposure of scanning circuit and amplifying circuit. Direct detection devices are seldom used for measuring low intensity X-ray flux since their receiving surface is too small and the depletion region is too thin to obtain high sensitivity.

3.1.1 Self scanned photodiode array:

In SSPA, as shown in figure 6, the fabrication compatability to general integrated circuits is advantageous. Its maximum data rate is limited by the speed of the shift registers, and is typically 3-4 MHZ. A major problem with SSPA design is the complexity of circuit. Additional amplifier are usually needed to compensate the signal level drop due to the line capacitance on the common output line.

Taniguchi *et al* [Taniguchi 84] reported their SSPA on which peripheral circuitry was protected with Pb foil. This device showed less increase in dark current and very good output/input linearity.
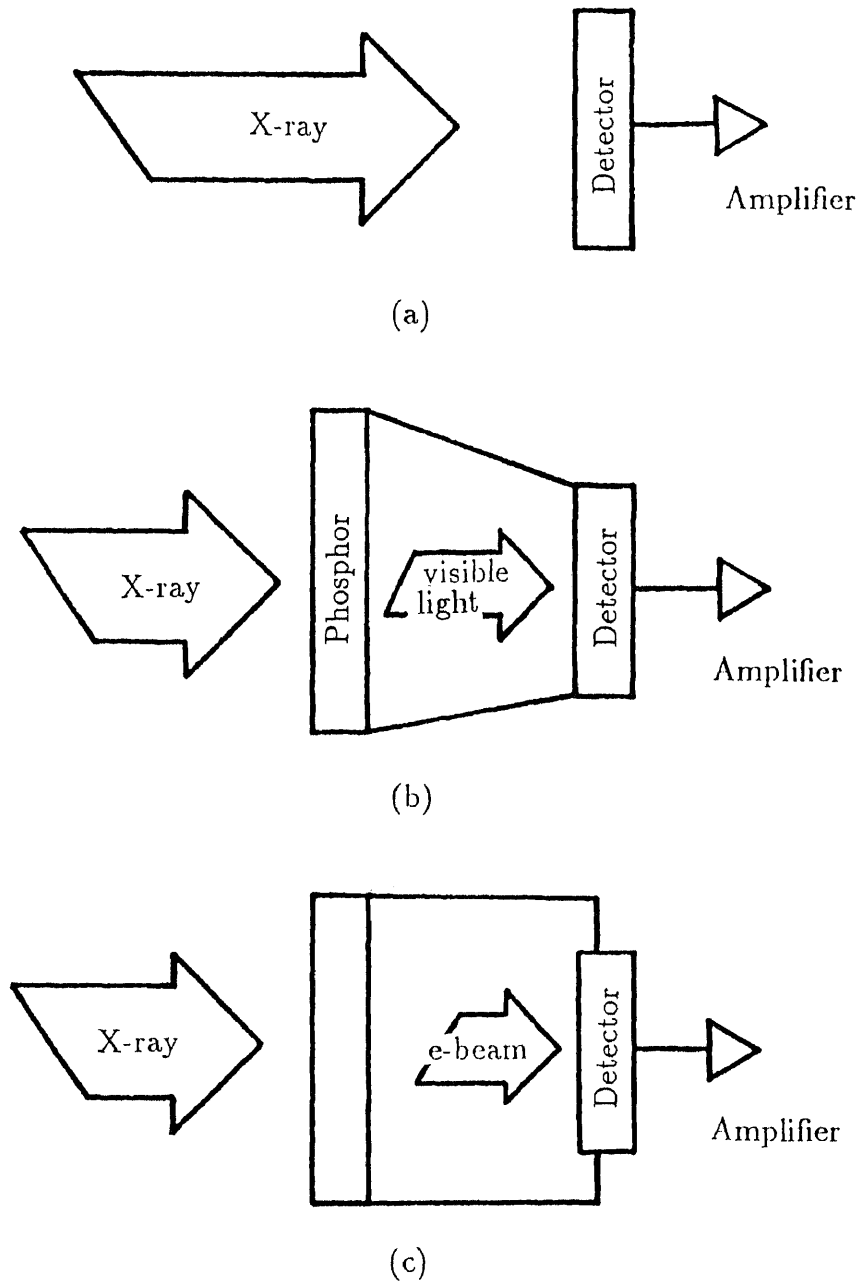
Figure 5: Three basic X-ray imaging topologies: (a) direct detection (b) X-ray visible light photon conversion (c) X-ray photon-electron conversion.
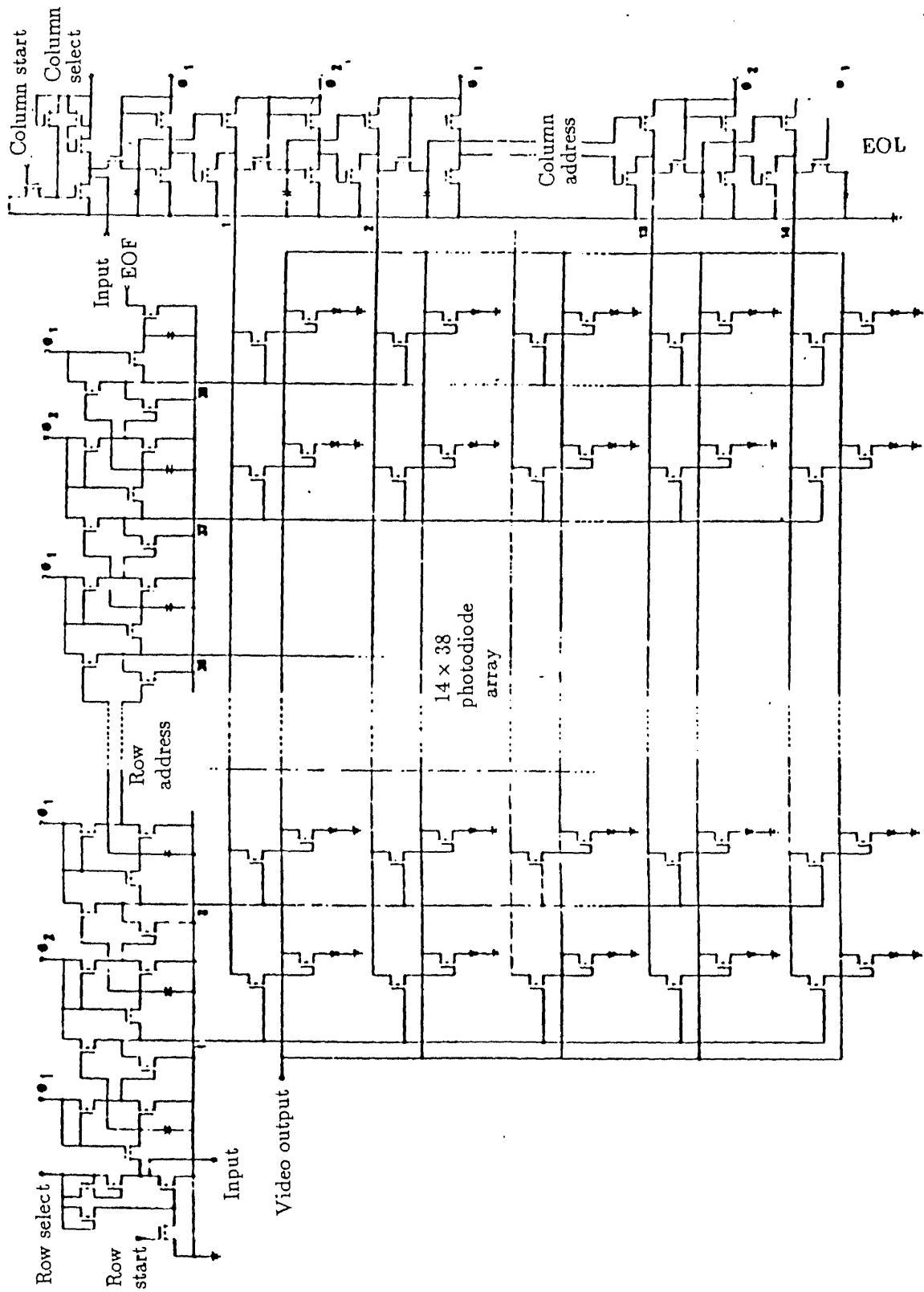
Figure 6: A self scanned photodiode array.[Carr 80]
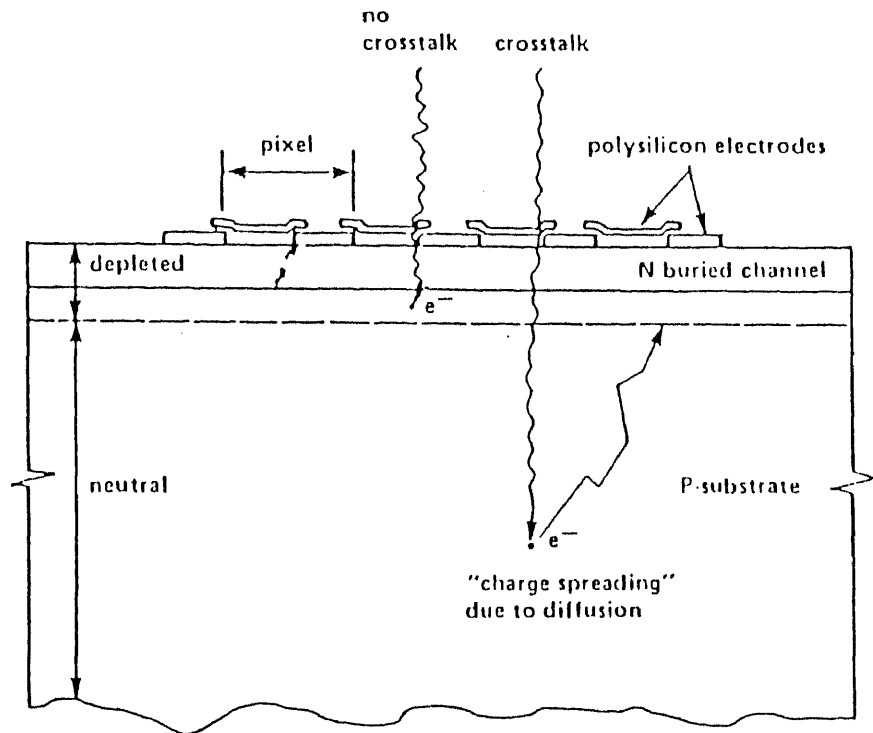
Figure 7: *Crosstalk (Blooming)* due to lateral diffusion of minority carriers.[Tsoi 85]

3.1.2 Charge coupled device:

Due to the higher packing density obtainable for CCDs compared with SSPAs, most large area imager with resolution over 2000 pixels are CCDs[Kosonocky 85, Tsoi 85]. Unlike photodiodes, CCD structures do not have diffused wells at the interaction area. Hence there is no ready supply of minority carriers to neutralized the charge in the depletion region. The depletion region extends much further into the substrate and most of the potential difference between the gate and substrate is dropped across this depletion layer. This feature enhances the collection effeciency of CCDs. But also because of this feature, A well known phenomenon called "crosstalk" occurs. Crosstalk is cause by the lateral diffusion of minority carriers optically generated below the depletion layer as shown in figure 7. It causes *bloomings* of the image and imposes a serious limit on dynamic amplitude range and spatial resolution of CCDs for X-ray detection. Recently, Tsoi *et al* have demonstrated a design for deep depletion CCD

imagers fabricated on high-resistivity substrates using effective channel stops that greatly reduce the crosstalk problem, and can be used for 1-10KeV X-ray detection.

3.1.3 Resistive stripe detector:

A position-sensitive detector without scanning circuitry was reported by Geber *et al* [Gerber 77]. It consists of stripes of silicon or germanium for which one contact is made to have a significant series resistance. As shown in figure 8 the position signal P is obtained by resistive charge division from the back layer. The E signal is proportional to the energy absorbed from the incident radiation in the active volume. Signal conditioning using an ADC is normally required to obtain the spatial data output from this detector. Figure 9 shows the schematic of a two dimensional resistive stripe detector. That the resolution of the device is approximately twice the width of a stripe. With the advance in lithography, this detector is very promising in ultrahigh resolution X-ray imaging.

3.2 X-ray visible light photon conversion

A combination of a fluorescent material and glass fibers films have been used with the SSPA substrate to transform the X-ray into visible light. Figure 10 shows a typical structure of such a device which can exhibit increased overall sensitivity to X-ray sources. In these devices, radiation damage of the detector can be eliminated by shielding peripheral circuit from X-ray bombardment. The decay time of phosphor films may in some applications be the limiting factor in the speed of the operation. Gamble *et al* [Gamble 79] have successfully demonstrated the use of a cooled Reticon RL512 (512 pixels) linear array, coupled to a 2:1 fiber-optic demagnifier with ZnS(Ag) phosphor on the incident interface. A resolution of $50\mu m$ was reported. The quantum efficiency of this device for electron-hole pair production within a photodiode is
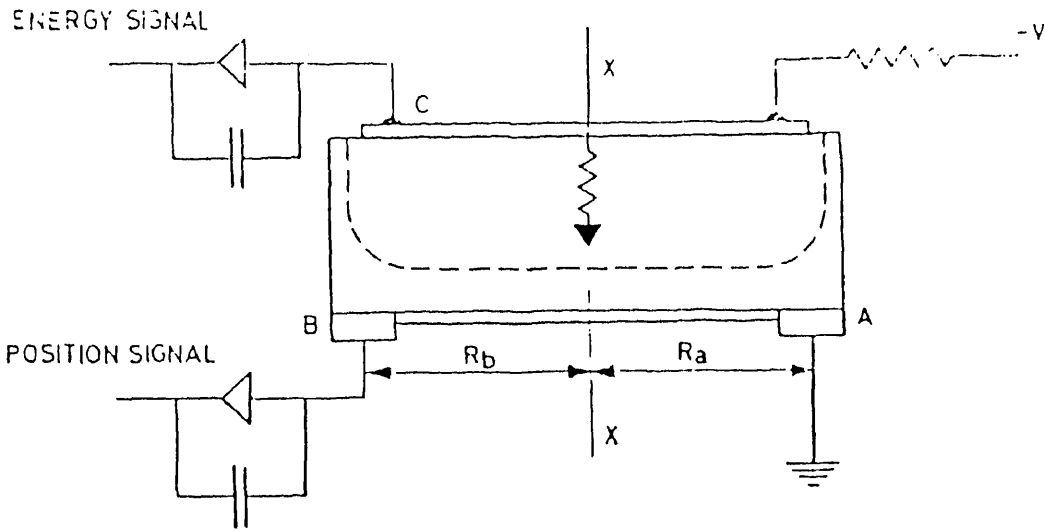
Figure 8: The principle of a resistive stripe detector
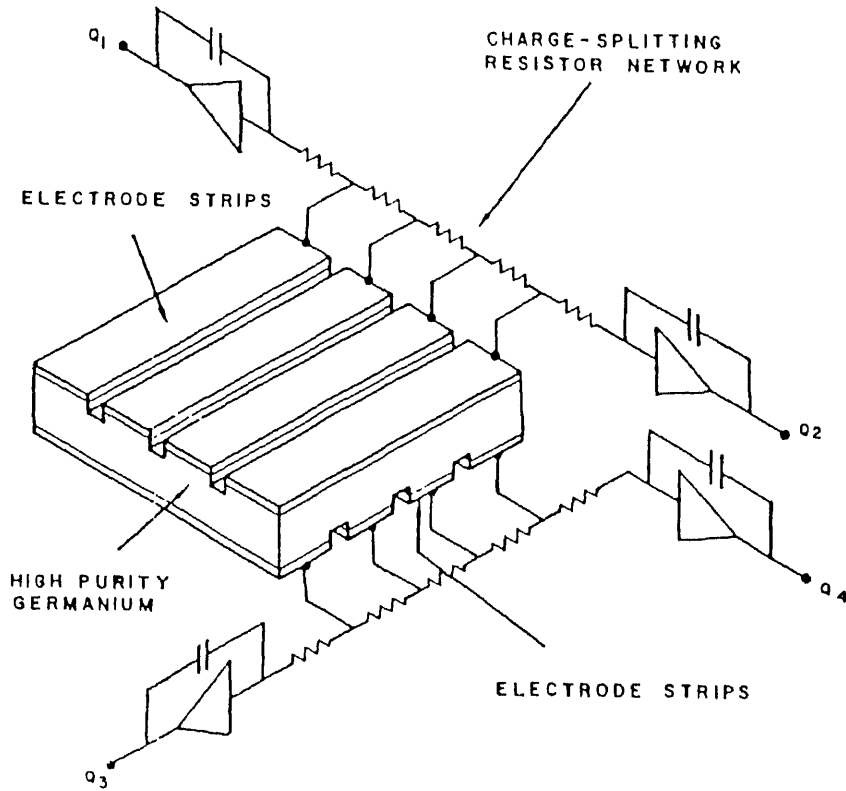
Figure 9: Schematic of a two dimensional resistive stripe detector

Incident X-Rays

2.54 cm

1μ Al layer

2-4μ particles, ZnS,
3-4 layers,~15μ thick

5.5μ fiber optic plate

2:1 reduction-fiber optics,
11μ : 5.5μ

Photo diode array
(Reticon RL-512B/24)

Spring loading

DIP pinout

Block for LN₂ cooling

LN₂ lines
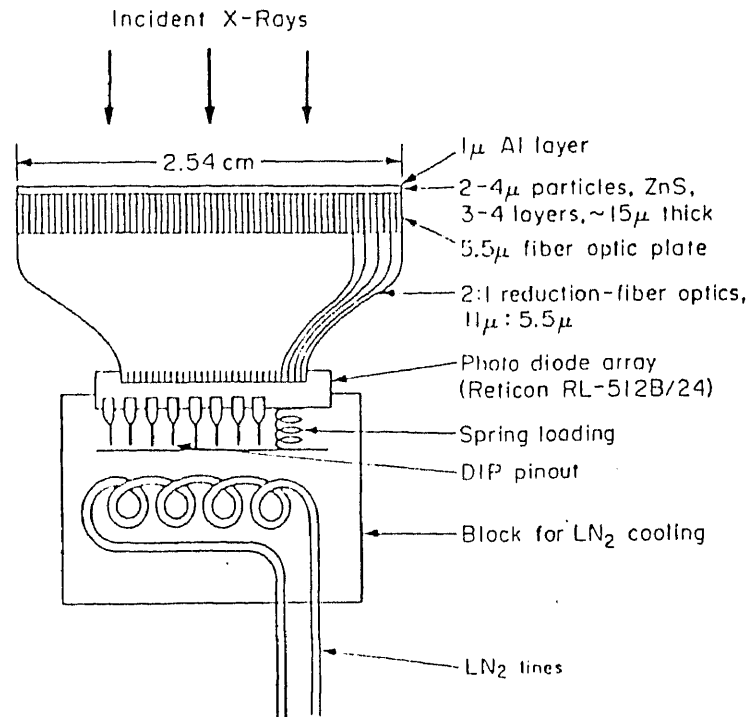
Figure 10: Apparatus of a X-ray visible light photon conversion system

approximately 75%. Consequently, about 110 electron charges are depleted across a photodiode for each absorbed incident 8KeV X-ray photon.

To further shrink the Gamble *et al* device, one possible solution is depositing a thick scintillation film directly on the passivation layer of a photodiode array. The proposed concept is further detailed in Appendix A.

3.3 X-ray photon-electron conversion

An electron-bombarded silicon imager has been used mainly in visible or infrared low-light level systems [Brown 76]. Very few such devices are available, with the exception of the "Digicon" manufactured by Electronic Vision. There still seem to be a number of operational problems associated with these devices; and they are likely to remain expensive devices, manufactured individually for particular application.

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Chapter IV
DEVICE HIERARCHY
AND CIRCUIT DESCRIPTION

Integrating analog and digital functions together on one chip has become feasible. In many cases very high performance analog functions are much required and a greater number of moderate performance analog functions are preferred. Thus combined analog and digital CMOS is in the center of interest. SPAX is designed using a top down approach. The root-level block diagram is shown in figure 11. As shown, the signals required to interface to external circuits are: (1) Clock pulse input (2) Four-bit data and counter reset outputs (3) End of line output "EOL" and End of frame output "EOF" (4) Power supply inputs: +5V, -6V to -12V, 0V .

The whole circuit is divided into three modules:

4.1 Addressing logic

Addressing logic contains a row address shift register and a column address shift register. In most digital circuits, shift registers are composed of level-restoring inverters coupled by pass transistors. With the movement of data controlled by applying two non-overlap clock pulses to pass transistors. Besides the need of non-overlapping clock pulses, switching noises become very annoying when these shift registers are interfaced to analog circuits. The row (column) register in SPAX, as shown in figure 12, is constructed by a series of D type flip-flops. The outputs of these D flip-flops are inverted by open drain transistors. By tieing all drains to a pull-up resistor, a multiple input NOR gate is formed. Not only does this configuration provide an automatic power-up reset but also it forces a circulated transfer of a logic "High" signal in the shift register. Figure 13 details the circuit of a D flip-flop without the reset function. It consists of two latches clocked 180 degrees out of phase to provide master-slave

operations.

4.2 Photodiode array

This array consists 30×30 cells which are sequentially selected by the row and cloumn address shift registers. The negative power supply line is required in this module. Output signals generated by each cell are sent to the counter module. In each cell, a source-couple pair, two inverters, two photon sensing diodes and control logic are included. Simulation shows current required for each cell is $3.55mA$ when the cell is selected. Quiescent power for each cell is $17.8mW$. The completed circuit diagram of one cell is demonstrated in figure 14.

4.2.1 Photodiodes and the discharge circuit:

Two identical PN junction diodes are reverse biased to obtain a maximum depletion layer width. Using two diodes instead of one diode with twice the area increases the sensitivity. As explained in chapter II, the total capacitance C across these diodes directly effects the charge signal to be sent to the following amplifier. The signal voltage will have a maximum when C (drain capacitance in discharge transistors C_t plus junction capacitance C_d plus amplifier input capacitance C_a) is minimum. Without decreasing the interaction area, two separated diodes give us higher signal voltage at both amplifier inputs. Considering the case of no discharge transistors, C will be discharged very graduately due to the leakage current of the diodes. This significantly increase the deadtime of the devices. A handshake technique is developed to overcome this difficulty. In figure 14, when the voltage level on the gates of M_{99} and M_{98} which is feedback from the counter module, exceeds the theshold voltage of discharge transistors, they clamp the diodes to 0V rapidly. The pulse width obtained from SPICE is $60nsec$ on the cell output line.

4.2.2 Inverters:

The *DC* transfer characteristic of both inverters, which are primary factors in shaping the output waveforms, are shown in figure 16 and figure 17. The voltage gain of the first stage is 9 and is given by the equation:

$$A_v = -\frac{g_{mn}}{g_{on} + g_{op}} \qquad (12)$$

where g_{on} and g_{op} are the small-signal output conductances of the n-channel and p-channel transistors respectively, g_{mn} is the transconductance of the n-channel transistor. The voltage gain of the second stage is 3.

4.2.3 Source-coupled pair:

The behavior of a source-couple pair is very similar to that of a bipolar differential stage. However, the range of linear operation is wider. By increasing the bias current or decreasing the device aspect ratio, the input range for which both transistors are active can be increased. The linear operation region is typically several hundred millivolts $(V_{gs} - Vth)$. The *DC* transfer characteristic of the CMOS differential stage is shown in figure 19. The voltage gain, assuming an open-circuit load, can be given as

$$A_v = -G_m \frac{r_{op} r_{on}}{r_{op} + r_{on}} \qquad (13)$$

where G_m is the differential stage transconductance, and r_{op} and r_{on} are the output resistance of the input transistor and the load transistor respectively.

4.2.4 Cell-enable logic:

Three transistors Q_1, Q_2 and Q_3 form the cell-enable logic. These transistors conduct when both row address line and column address line of the cell are at logic "Low" state. The cell output line is then connected to the global counter and the differnetial stage is then biased.

4.3 Counter module

The ripple counter counts the pulses sent from each cell and provides external circuit eight-bit data which represents the relative intensity of incident X-ray flux at each cell. Since the ripple counter must be reset immediately it is read out, a output data latch is used. An one-shot circuit giving $60nsec$ pulses at the rising edge of each input clock pulse resets the ripple counter.

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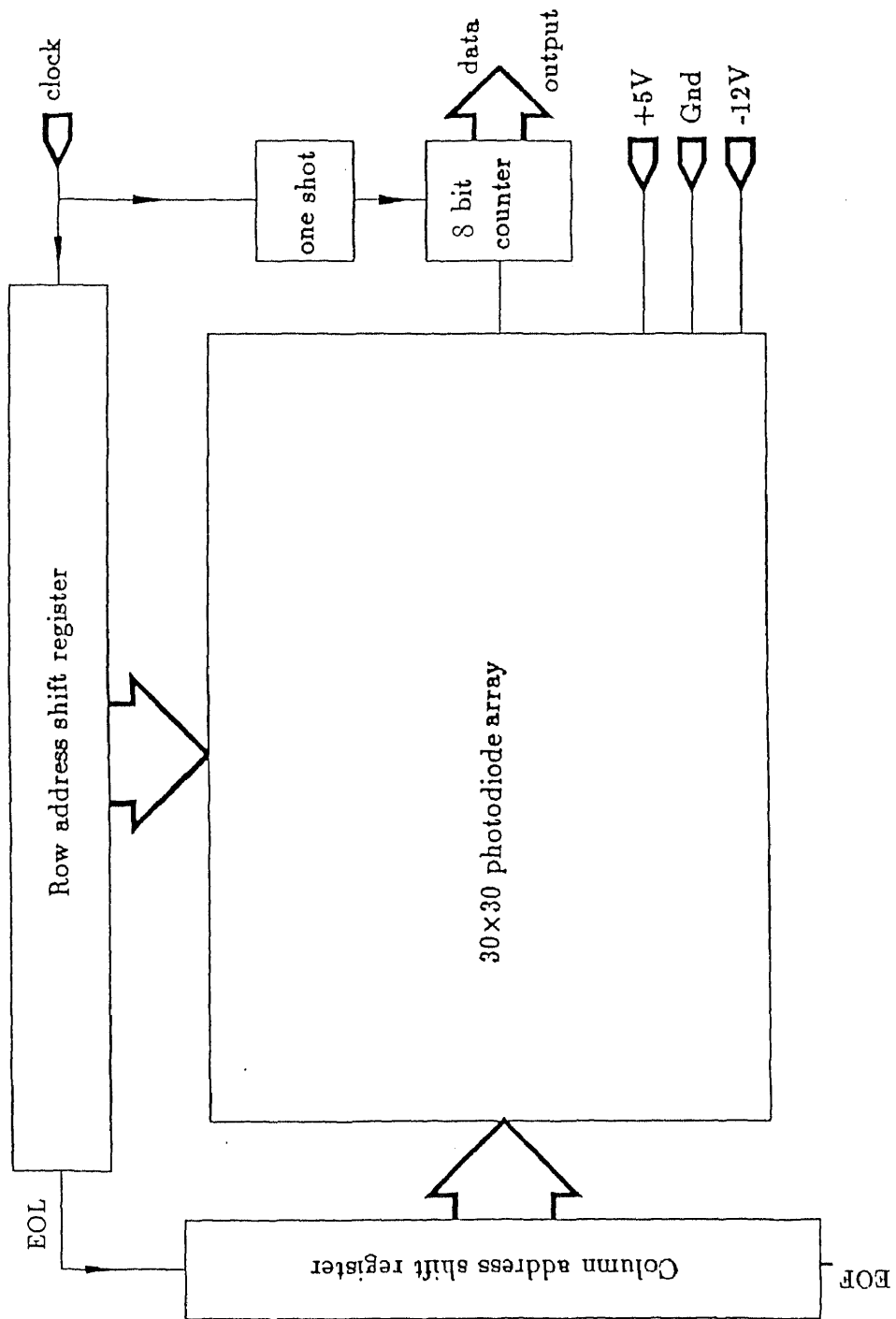
Figure 11: Root level block diagram of SPAX.
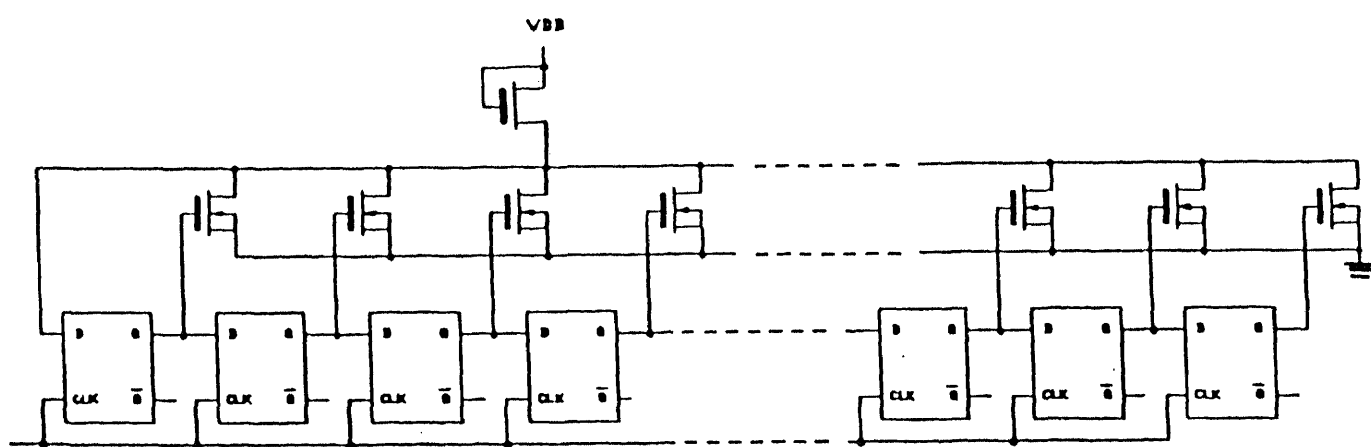
Figure 12: The shift register and the multiple input NOR gate.
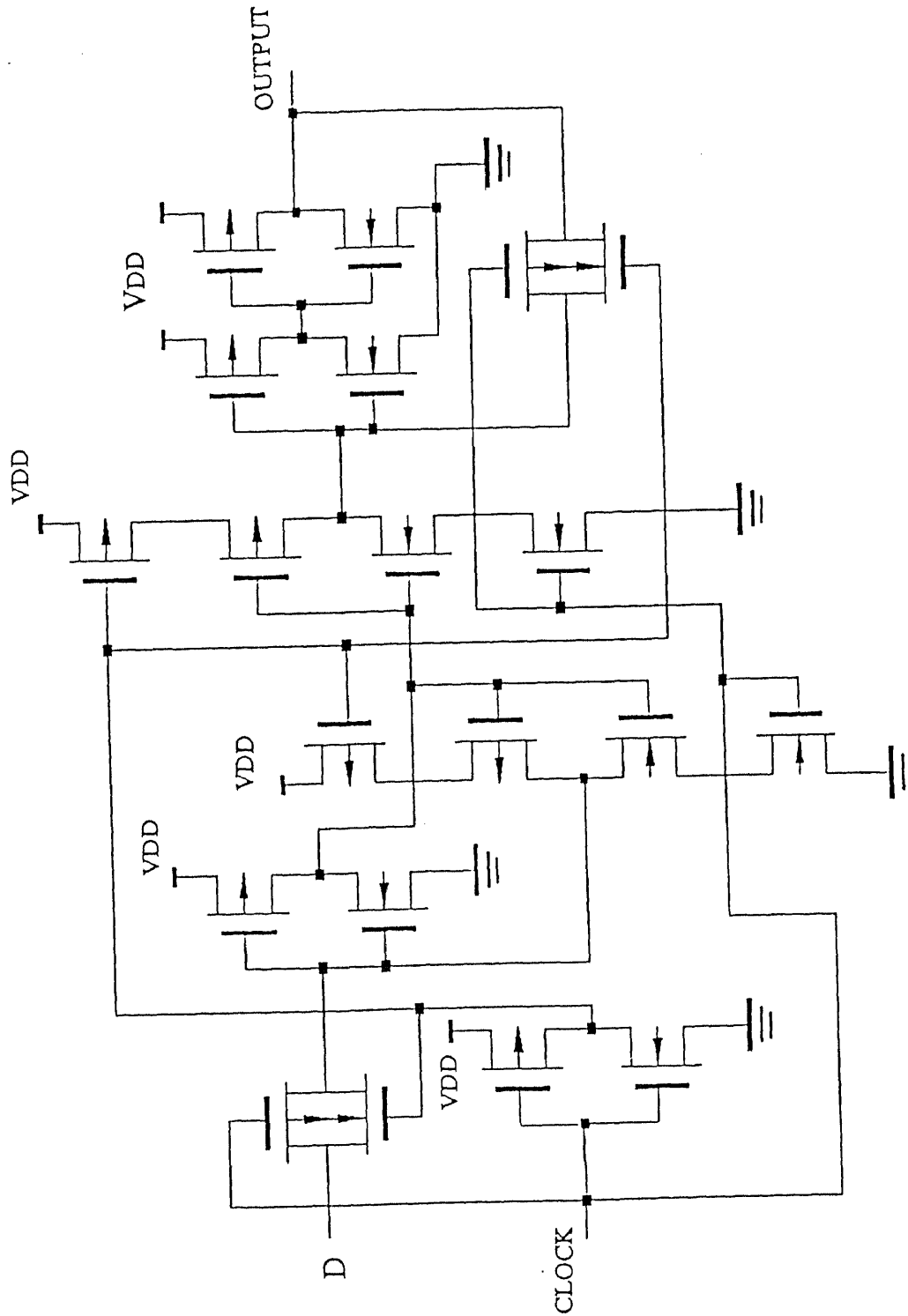
Figure 13: A D type flip-flop cell[CDI 1984].
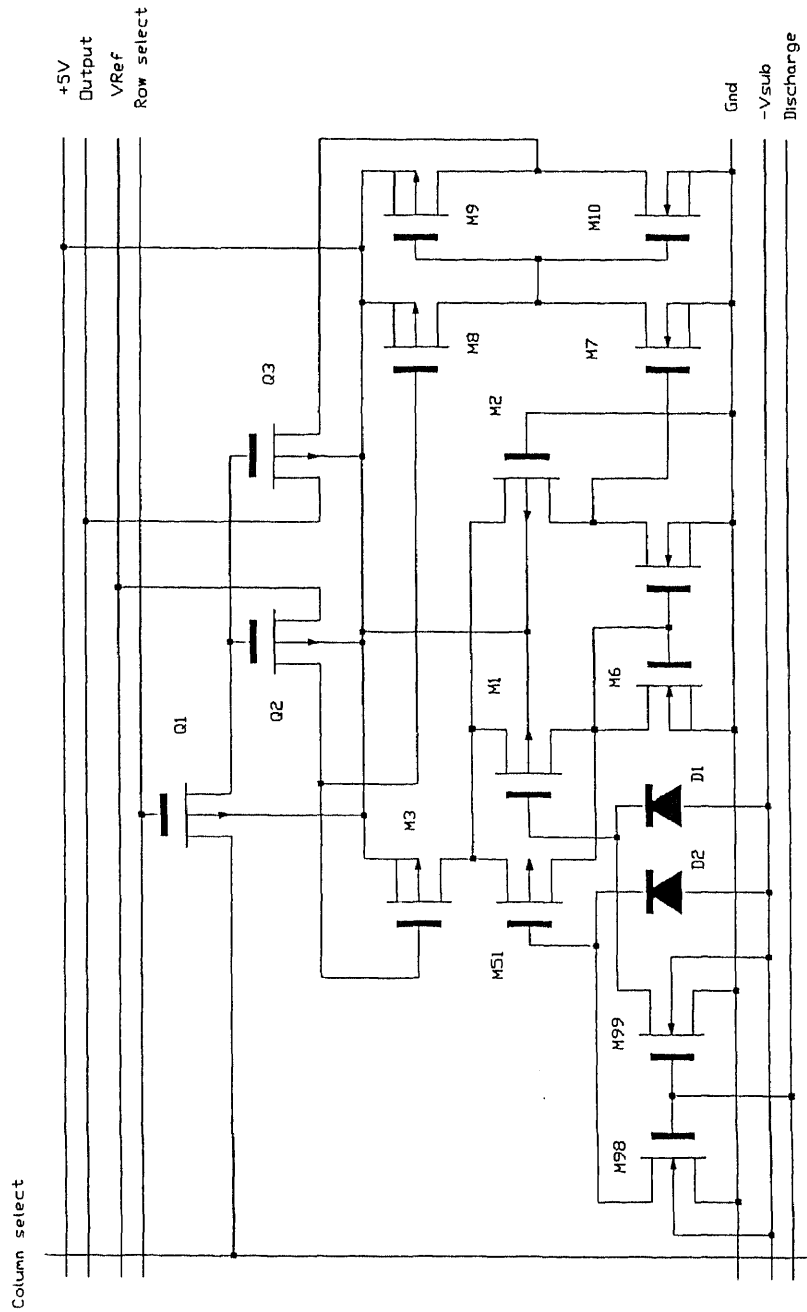
Figure 14: Circuit schematic of one sensing cell.
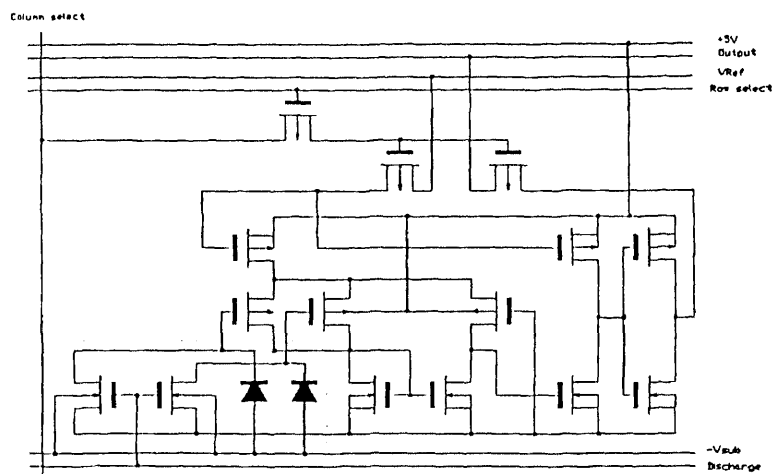
Figure 15: Photodiodes and the discharge circuit.
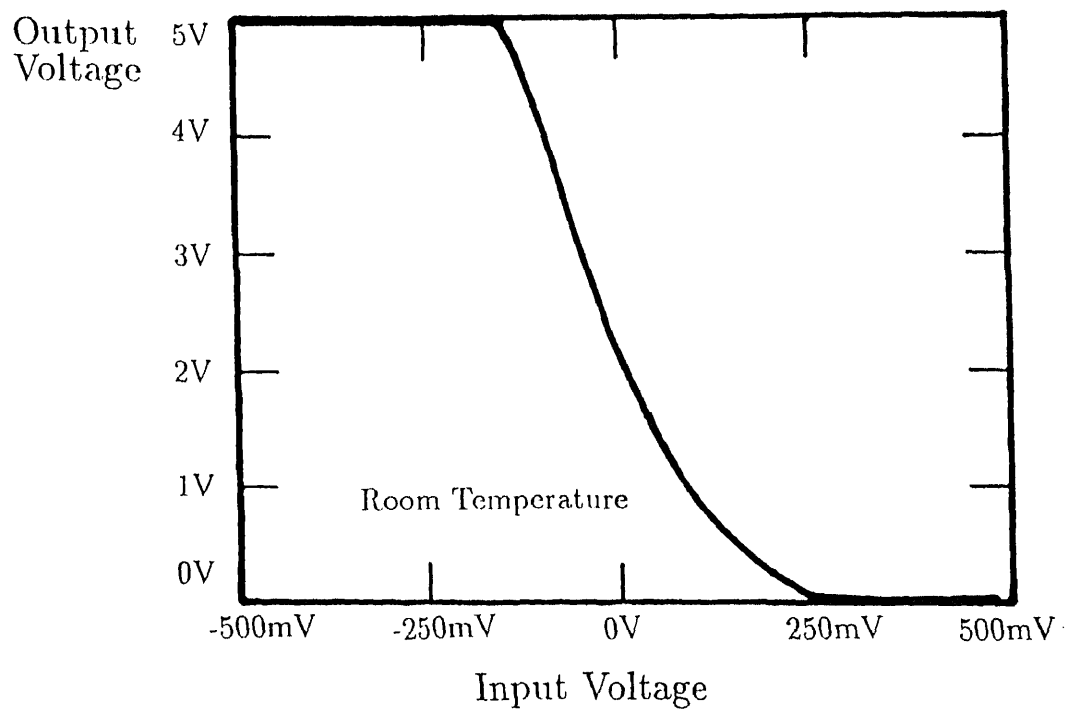
Figure 16: *DC* transfer characteristics of the first inverter.

Figure 17: *DC* transfer characteristic of the second inverter.

Figure 18: Source-couple pair schematic.
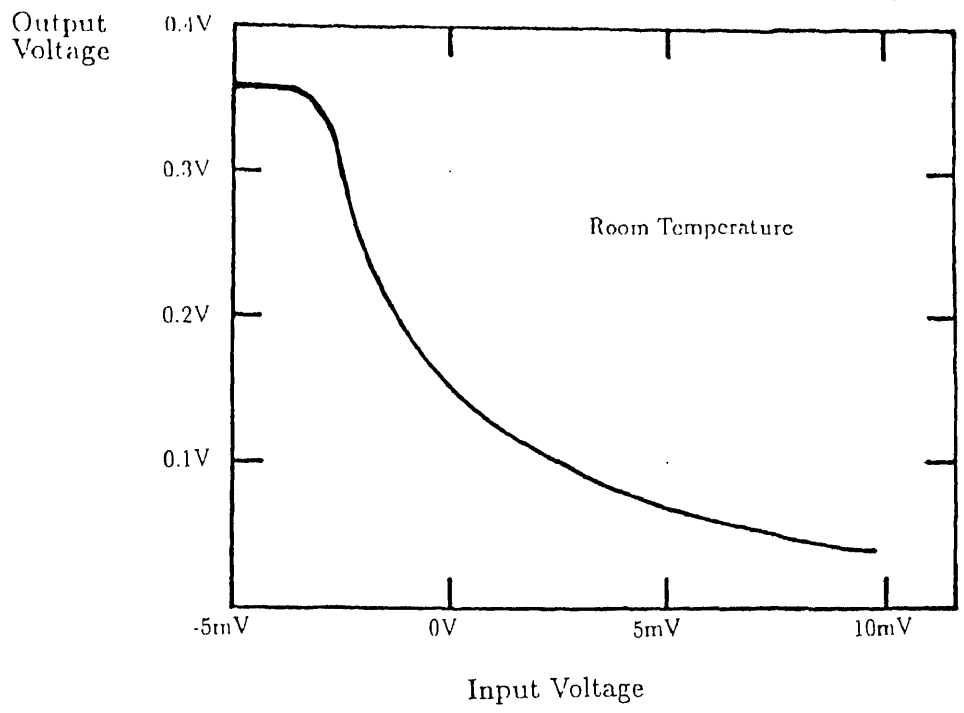
Figure 19: *DC* transfer characteristic of the differential stage.
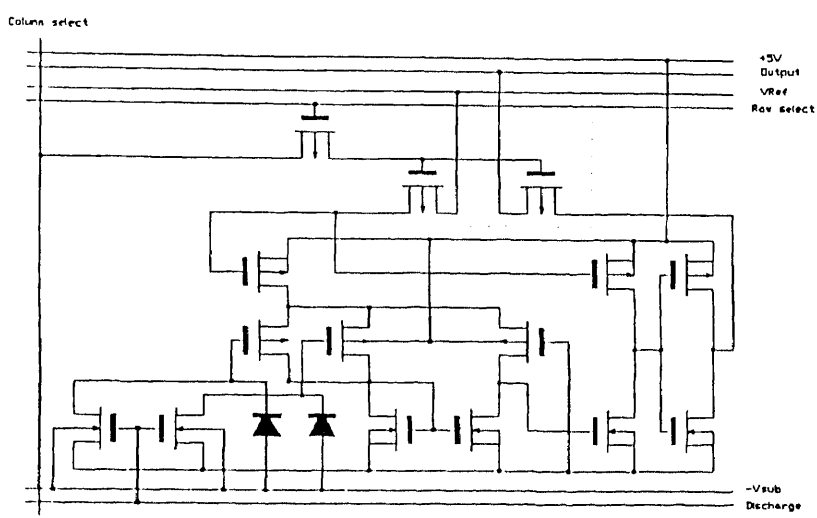
Figure 20: Cell enable logic.
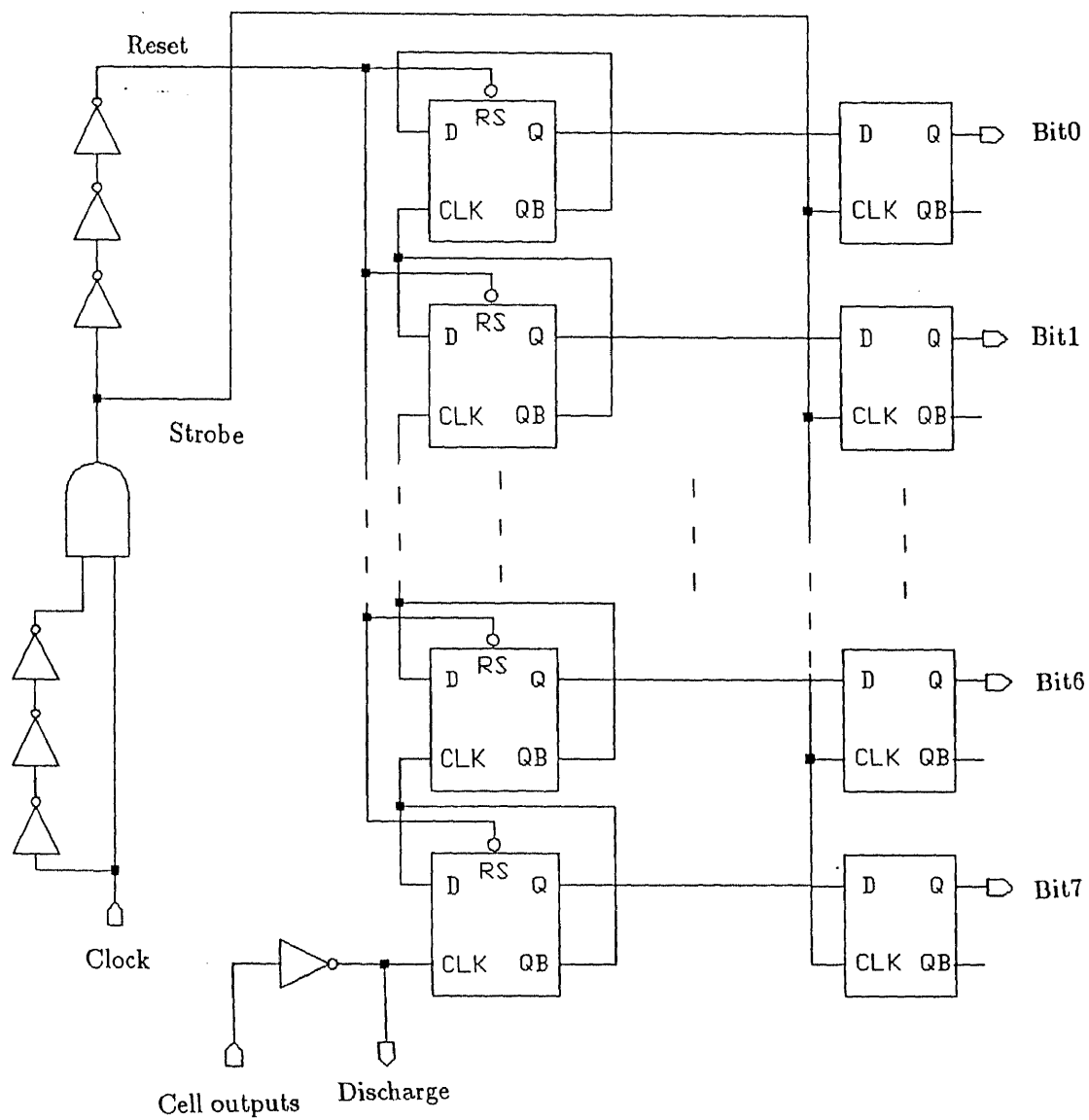
Figure 21: The counter module.

Chapter V
SIMULATION METHODOLOGY
AND WORST CASE ANALYSIS

As Habekotte [Habekotte 87] pointed out, combined analog and digital design demands very good control of the many different process steps. Examples include minimum PN junction leakage current, precise resistor and capacitor ratios with minimal voltage and temperature dependancy, and reproducible and characterized behavior of the different active and passive components. Since SPAX needs both in-cell amplifier and addressing logic, these requirements of process control are very desirable. However, some parameter variations were been taken into account during circuit designing and simulations.

5.1 Logic simulation results

Logic simulations utilizing HILO3 for addressing logic and ripple counter had been done. The result are shown in figure 22 and figure 23 respectively.

5.2 Circuit simulations

Simulations of the cell circuit were performed using SPICE2G5. Because of the lack of a proper photodiode model in SPICE the author used a simple JN junction diode cascading an external step volatge source to approximate a photodiode. Transient analysis demonstrates the output waveform corresponding two input pulses seperated by $200nsec$. During the simulation, oscillation occured when transistor *effective channel length* exceed $1.2\mu m$ regardless to the channel width. That is, oscillation determined by SPICE is independent of the RC constant, and therefore strongly indicates an error of convergence in SPICE. The source program is presented in Appendix B.

Simulation shows a constant $4.4V$ voltage can be obtained at the drain of M_{60} used

as bias source in figure 25.

5.3 Worst case analysis

Due to the variation of ion implantation dose, oxidation temperature and polysilicon deposition temperature, transistor threshold voltage value will vary between with production process. A ± 10 percent threshold voltage variations of both P type and N type transistors are considered in the worst case analysis separately. Simulation results indicate a problem only when the N type transistor threshold voltage V_{TN} is 10 percent below nominal value, in which case inadequate voltage gain of in-cell amplifiers occurs.

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TIME	CK	PR	CR	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
0	0	0	1	1	0	0	0	0	0	0	0
50	1	0	1	1	0	0	0	0	0	0	0
100	0	0	0	1	0	0	0	0	0	0	0
150	1	0	0	0	1	0	0	0	0	0	0
200	0	0	0	0	1	0	0	0	0	0	0
250	1	0	0	0	0	1	0	0	0	0	0
300	0	0	0	0	0	1	0	0	0	0	0
350	1	0	0	0	0	0	1	0	0	0	0
400	0	0	0	0	0	0	1	0	0	0	0
450	1	0	0	0	0	0	0	1	0	0	0
500	0	0	0	0	0	0	0	1	0	0	0
550	1	0	0	0	0	0	0	0	1	0	0
600	0	0	0	0	0	0	0	0	1	0	0
650	1	0	0	0	0	0	0	0	0	1	0
700	0	0	0	0	0	0	0	0	0	1	0
750	1	0	0	0	0	0	0	0	0	0	1
800	0	0	0	0	0	0	0	0	0	0	1
850	1	0	0	1	0	0	0	0	0	0	0
900	0	0	0	1	0	0	0	0	0	0	0
950	1	0	0	0	1	0	0	0	0	0	0

Figure 22: Logic simulation of the addressing logic.

	C				
	K	C	P	C	WWWW
	1	K	R	R	1234

----TIME---					
0	0	0	0	1	0000
20	0	1	0	1	0001
40	0	0	0	1	0001
50	0	0	0	0	0001
60	1	1	0	0	0010
61	1	1	0	0	0010
80	1	0	0	0	0010
100	1	1	0	0	0011
101	1	1	0	0	0011
120	0	0	0	0	0011
140	0	1	0	0	0100
141	0	1	0	0	0100
160	0	0	0	0	0100
180	1	1	0	0	0101
181	1	1	0	0	0101
200	1	0	0	0	0101
220	1	1	0	0	0110
221	1	1	0	0	0110
240	0	0	0	0	0110
260	0	1	0	0	0111
261	0	1	0	0	0111
280	0	0	0	0	0111
300	1	1	0	0	1000
301	1	1	0	0	1000
320	1	0	0	0	1000
340	1	1	0	0	1001
341	1	1	0	0	1001
360	0	0	0	0	1001
380	0	1	0	0	1010
381	0	1	0	0	1010
400	0	0	0	0	1010
420	1	1	0	0	1011
421	1	1	0	0	1011
440	1	0	0	0	1011
460	1	1	0	0	1100
461	1	1	0	0	1100
480	0	0	0	0	1100
500	0	1	0	0	1101
501	0	1	0	0	1101
520	0	0	0	0	1101
540	1	1	0	0	1110
541	1	1	0	0	1110
560	1	0	0	0	1110
580	1	1	0	0	1111
581	1	1	0	0	1111
600	0	0	0	0	1111
620	0	1	0	0	0000
621	0	1	0	0	0000
640	0	0	0	0	0000
660	1	1	0	0	0001
661	1	1	0	0	0001
680	1	0	0	0	0001
700	1	1	0	0	0010
701	1	1	0	0	0010
720	0	0	0	0	0010
740	0	1	0	0	0011
741	0	1	0	0	0011
760	0	0	0	0	0011

Figure 23: Logic simulation of the eight-bit ripple counter.

Figure 24: Transient analysis of the cell amplifier.

DIODE 1

8mV

DIODE 2

SOURCE
COUPLED
PAIR OUTPUT

8mV

80mV

700mV
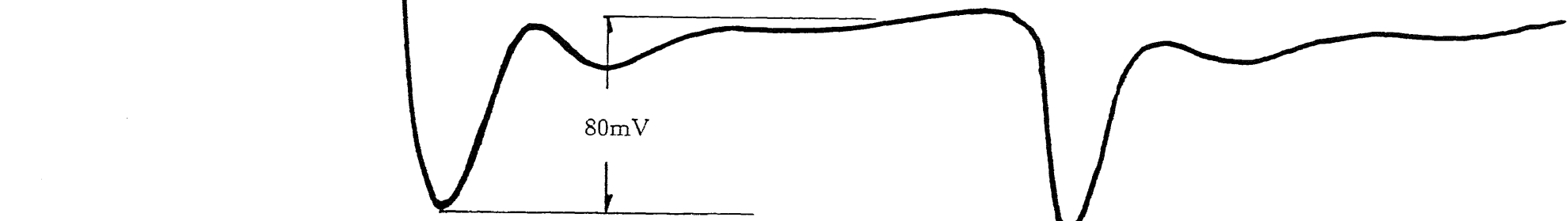
SECOND INVERTER OUTPUT

FIRST INVERTER OUTPUT

2V

4V
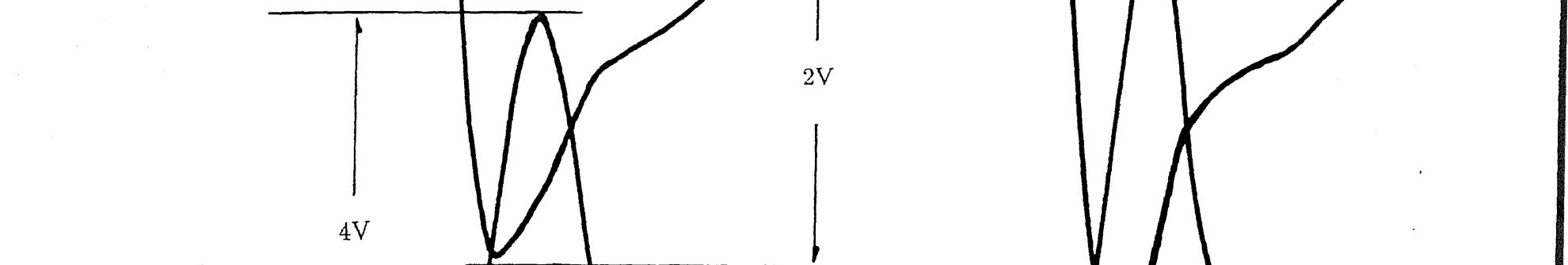
CLOCK PULSE
AT COUNTER
INPUT
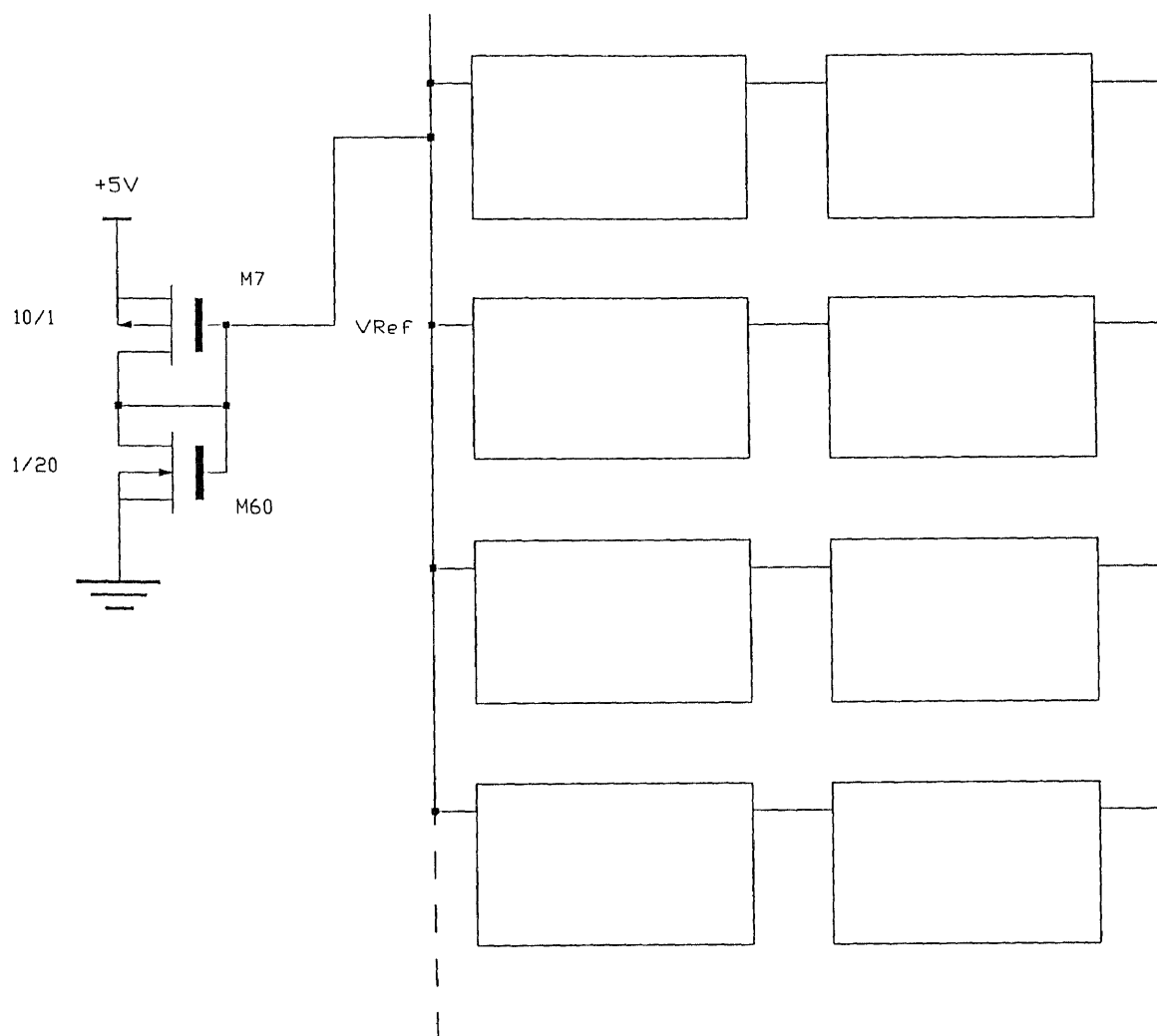
Figure 25: The bias source of the differential stage.
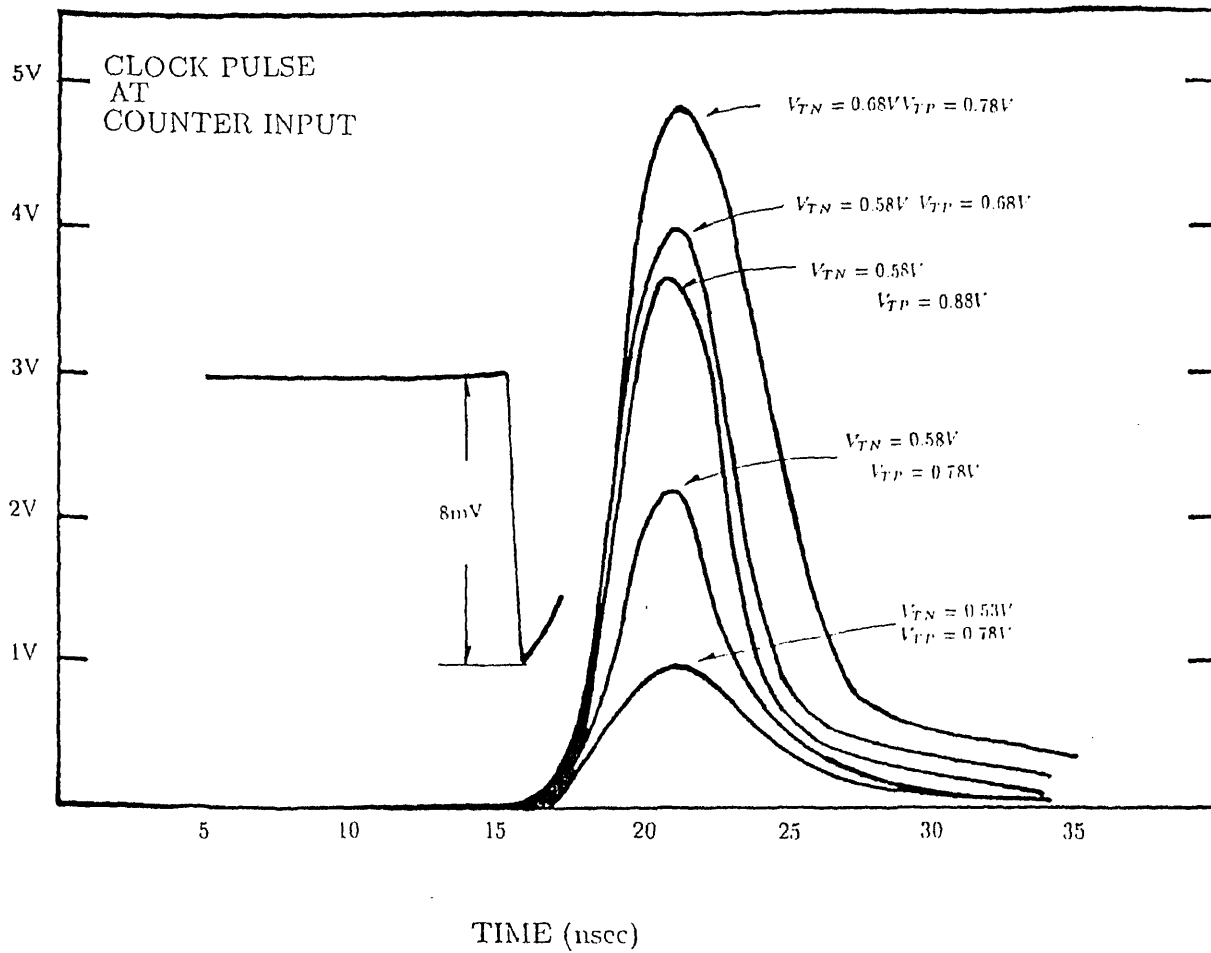
Figure 26: Comparing the output pulse height of five different combination of transistor threshold voltages.
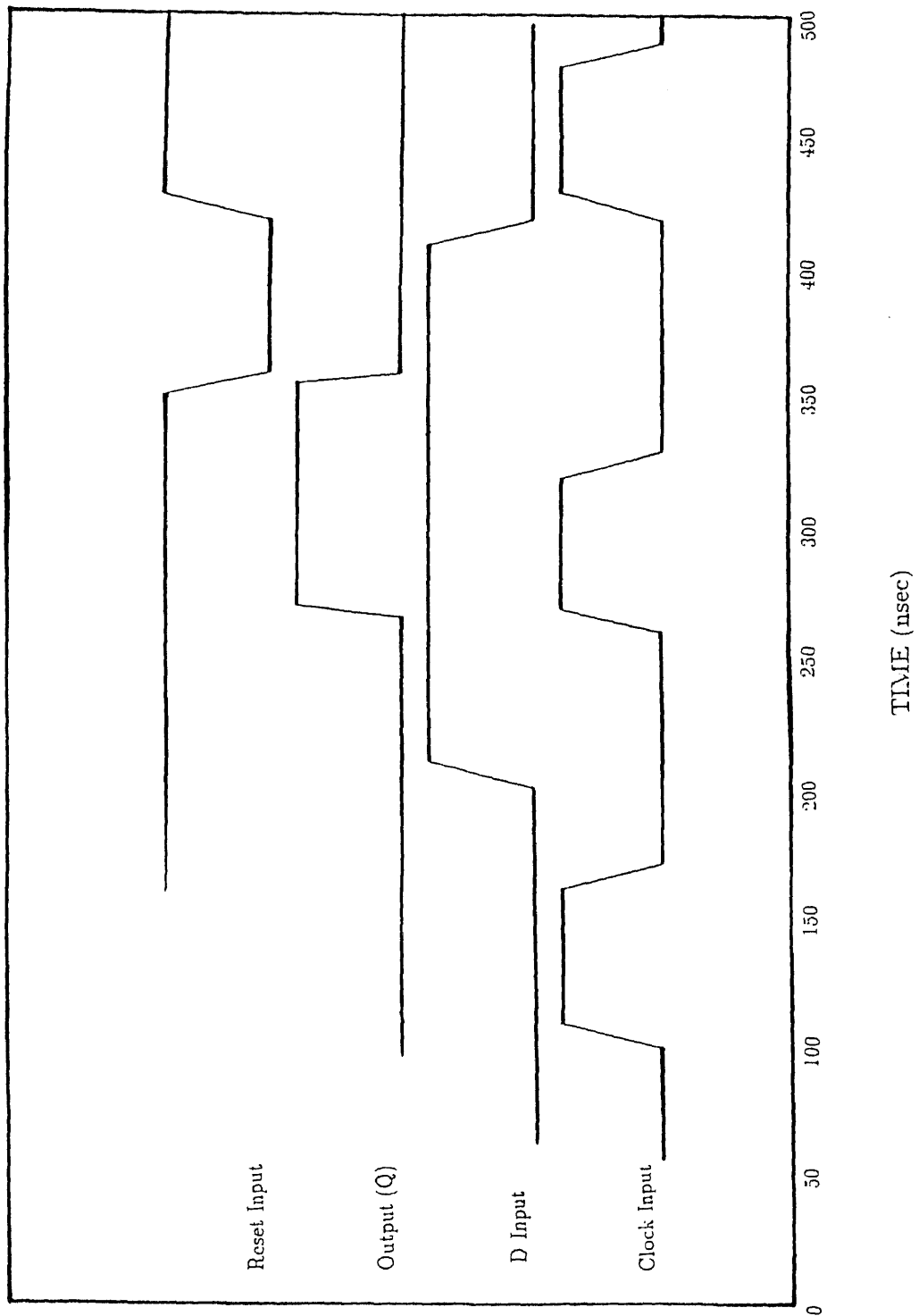
Figure 27: SPICE simulation result of the D type flip-flop standard cell circuit.

Chapter VI
SUGGESTED LAYOUTS

The MOSIS $1.2\mu m - 2\mu m$ CMOS design rule is used for physical layout. Since all shift registers, the ripple counter and the output latch are constructed with D flip-flops, layouts of a D flip-flop and one photon sensing cell are presented.
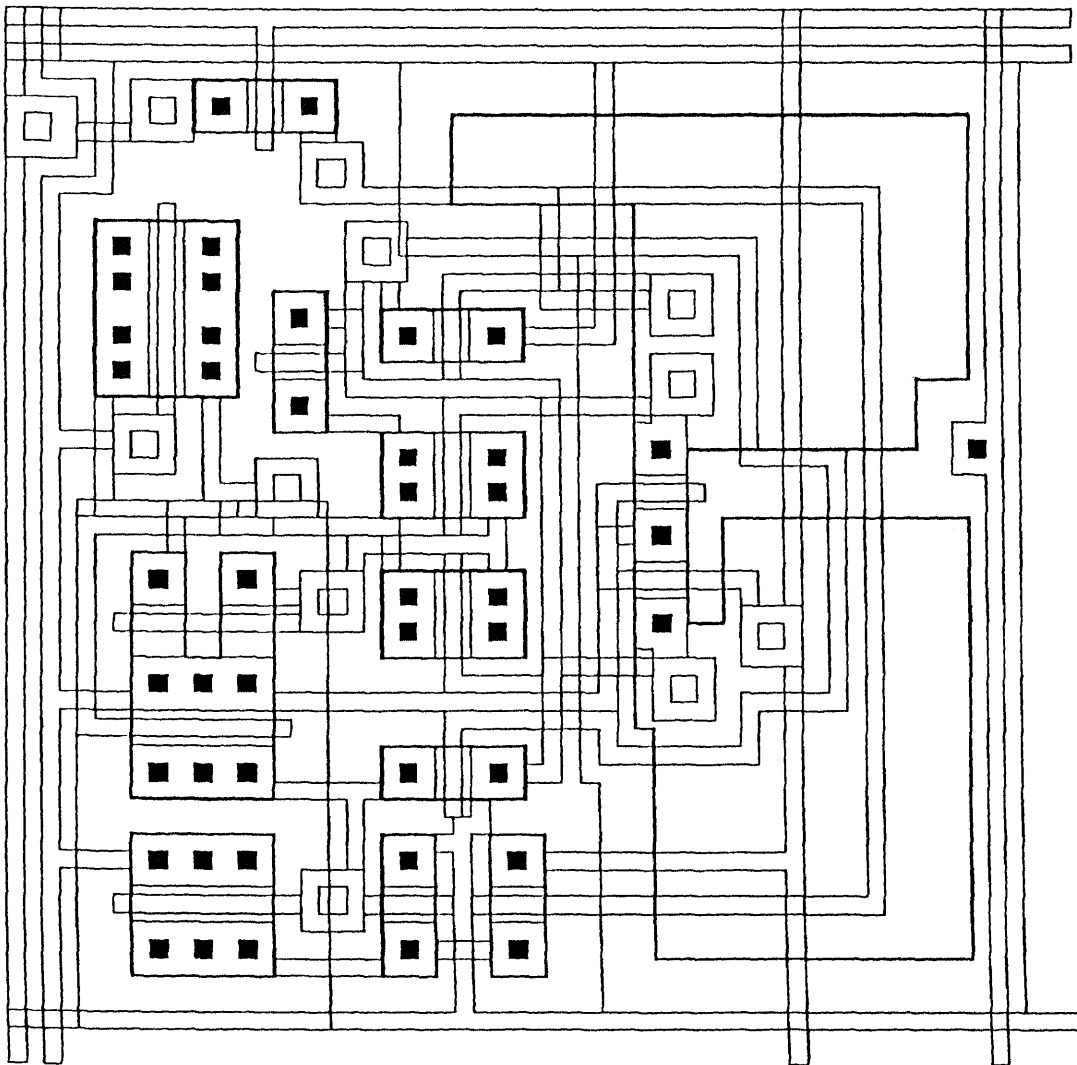
Figure 23: Suggested layout of a photon sensing cell.
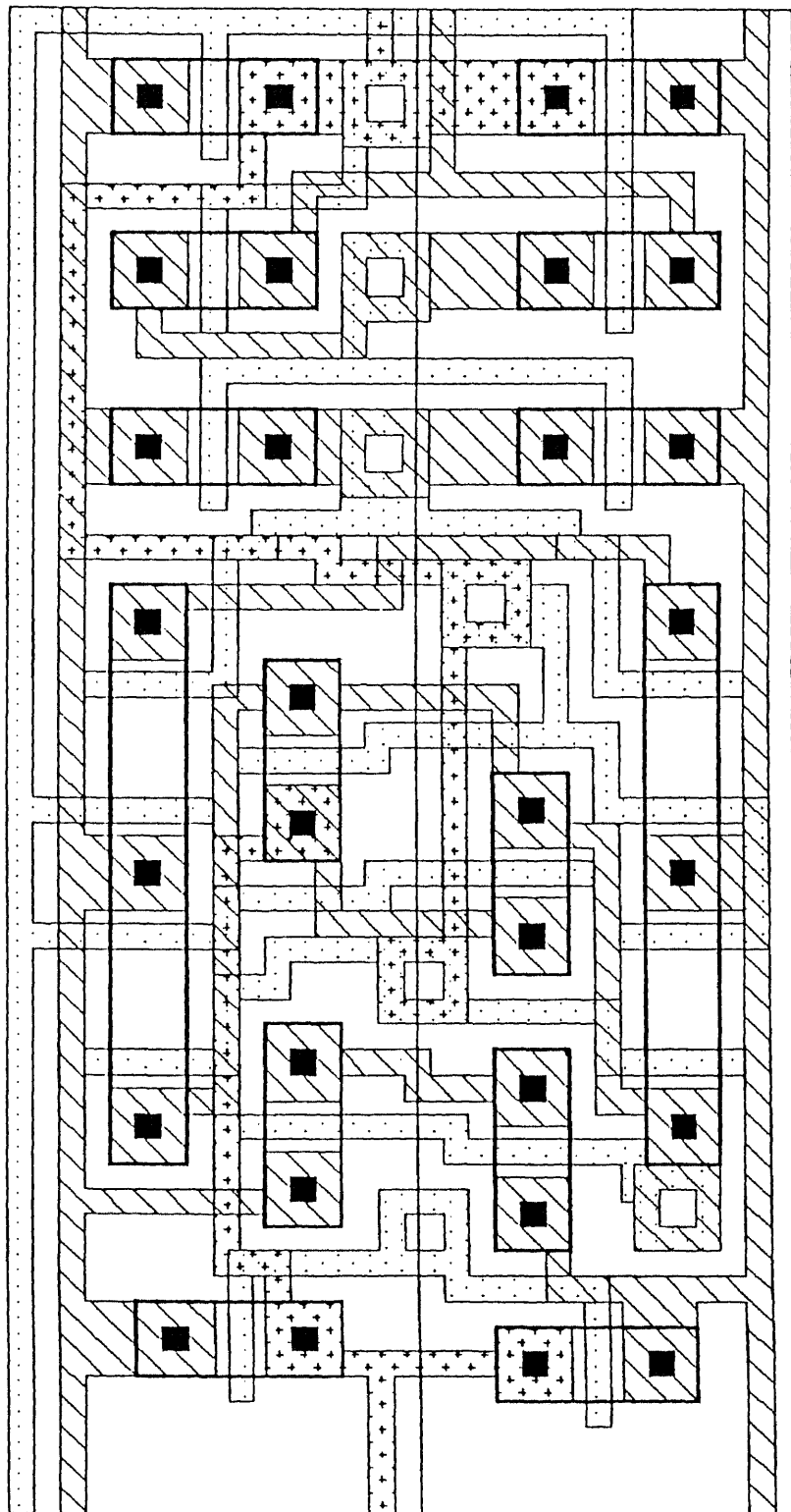
Figure 24: Suggested layout of a D flip-flop.

Chapter VII
SUMMARY
AND CONCLUSIONS

The operating frequency of SPAX is 1MHZ. This frequency is determined by the counter bit-number and the pulse width corresponding to each event. Assuming the clock pulse width at the ripple counter input is P, the maximum operating frequency F_{max} for SPAX can be approximated by

$$F_{max} \simeq \frac{1}{(256 + 1)P_{min}} \tag{12}$$

Using standrad cells of $1.2\mu m$ design rules, F_{max} is about 5.8MHZ. Within a constant sampling area, the incident radiation intensity is directly proportional to the number of photons arrived in the sampling time period. Therefore, the optimal incident radiation intensity for SPAX varies with operating frequency. The X-ray source power required for a specific SPAX operating frequency is given in figure 30. For an irradiant intensity of 20KeV X-ray photons of 10^4R/hour, the power of the X-ray tube is 8 Watts.

The linearity of the collected charges across a photodiode to the incident flux energy can be concluded from equation 8 in chapter II. Adding a negative feedback to the in-cell amplifier will improve the linearity of the cell-output pulse amplititude to the incident flux energy. This indicates SPAX can be expanded to have energy resolution. Assuming the threshold voltage of the counter input is 1V, the minimum incident X-ray photon energy required to trigger the counter is 6.9KeV.

SPAX is a practical device to be fabricated. Its physical layout can be completed by a standard graphic editor. No special process is needed during a general VLSI fabrication. However, test patterns contain PN diodes identical to in-cell photodiodes
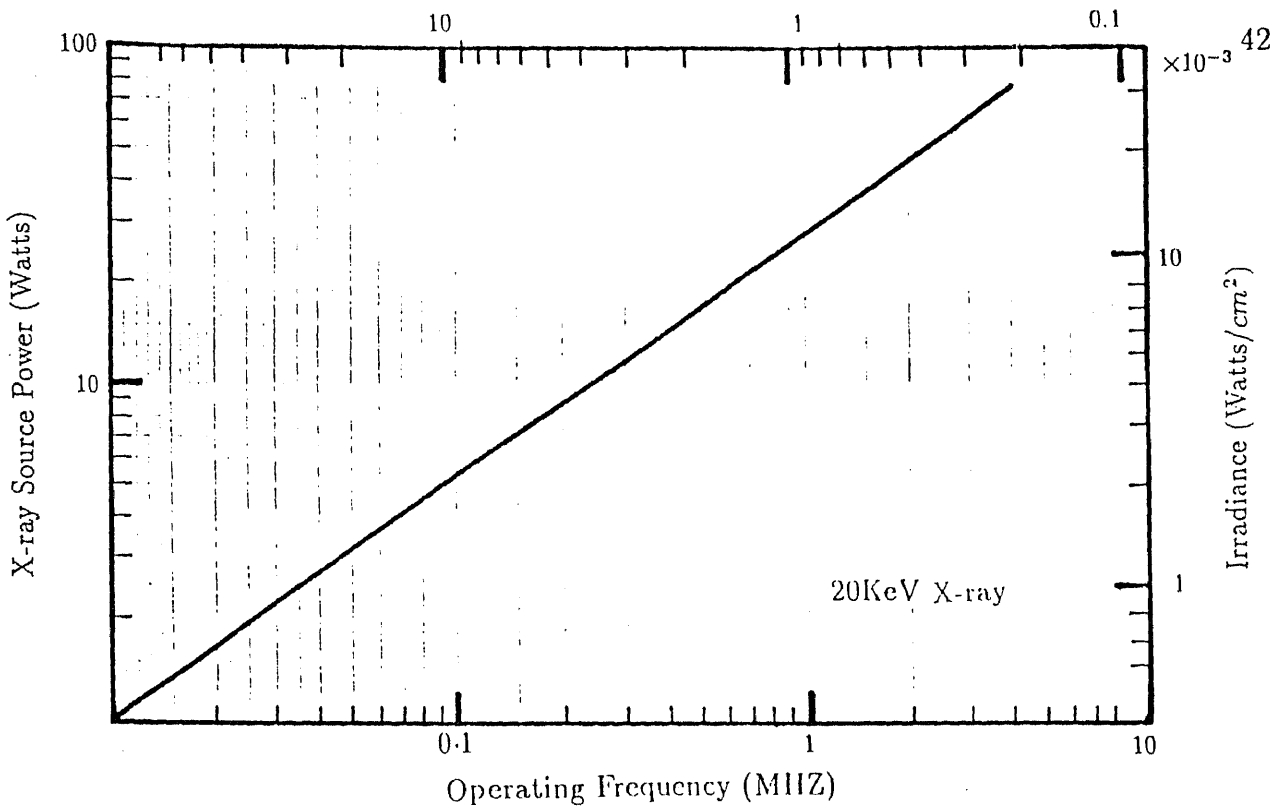
Figure 33: X-ray irradiance *vs* operating frequency, for 10 counts/pixel.

are recommended. They are very desired in measuring the conversion efficiency.

Four performance parameters are summarized from this thesis:

(1) The total active volume of photodiodes

A negative power supply for photodiodes is used to enlarge the active photosensitive volume of the photodiodes. The estimated active volume for each photodiode is $10\mu m \times 1600\mu m^2$ based on processing with an n-type substrate with a $N_B = 2.5 \times 10^{14} cm^{-3}$. The 20KeV X-ray photon absorption percentage under these conditions is 1.2% .

(2) The voltage gain of the in-cell amplifier.

A voltage gain of 500 at room temperature on a $60nsec$ input pulse is observed from SPICE. It is not the limit of this circuitry but a optimal value after considering the stability of the in-cell amplifier and the physical size of a cell. The cell size in the

suggested layout is $80\mu m \times 80\mu m$.

(3) The total power dissipation in one cell.

In SPAX, the power dissipation on a selected cell is about 18mW. Most of this value is consumed by the source coupled pair and the first inverter. The value can be reduced by adjusting the W/L ratio of the bias transistor. The 900 cell chip is estimated to required only 18mw plus support power.

Static power dissipation can increase with accumulated irradiation dose. Radiation damages has not been considered in this thesis, but a gradual increase of dark-current for all reverse-biased junction and a shift of thresholds are predicted.

(4) The tolerance of parameter variations.

In this thesis, the process control of transistor threshold voltages is assumed to be ± 10 percent. This range can be relaxed if additional compensating circuits are added to the critical differential stage devices.

Two methods can be used to eliminated the long discharge line. (1) Bias M_{99}, M_{98} to provide a continuous current source for D_1, D_2. (2) To each cell, add an extra inverter which provide a longer time to reset the diodes. However, the increase in cell size has to be considered.

Appendix A
DEVICE ENHANCEMENT WITH
A CdTe SCINTILLATION FILM

Due to the inherent low X-ray capture cross-section in the silicon lattice, using silicon devices for X-ray imaging requires on chip amplifiers having high S/N ratios and wide frequency response ranges. An unavoidable problem for this approach is the radiation damage which cause dark current to increase. Early research[Gamble 79] had pointed out that by using a scintillation film and optical fibers, one can detect visible photons thus obtain X-ray images. Without exposing the photodiode array directly to X-ray flux, radiation damage problem are almost eliminated. Yet, the devices volume and the reproducablility is still to be optimized. A similar approach using a direct deposited scintillation film is studied. Figure 31 shows the schematics of this approach. A higher density thick film (*eg.* CdTe) can be used as a scintillator. The selection of scintillator has to base on the consideration of material density, transparency, lattice constant and band-gap. For example, CdTe has a higher absorption coefficient than Si for X-ray and has a bandgap very close to that of Si. Annealing the scintillation film for maximum quantum conversion efficiency is strongly recommended. As shown in the figure the thickness of the scintillator has to be smaller than $1/\alpha$ to avoid the self-absorption of visible light photon in vertical direction. Horizontal self-absorption is prefered since it enhances the spatial resolution. It is this reason that the minimum width of the PN junction is also $1/\alpha$.

The circuit schematics demonstrated in figure 32 is recommened for constructuring the visible light image. Each cell includes enable logics, a discharge transistor, a dummy transistor and a PN junction diode. There are two output lines from every cell, a video signal line and a switching noise line. The dummy transistor is used to

obtain switching noise signals which are symmetrical to those on video signal line. The video chip output signal is obtained by subtracted the noise signal from the video signal using a differential amplifier. At the end of every column, two extra transistors are added to seperated the total line capacitance from the column capacitance. Thus the capacitance load driven by the photodiode is reduced.

REFERENCES

Gamble, R. C., Baldeschwieler, J. D., and Giffin, C. E., *Rev. Sci. Instrum.* 50, 1416, (Nov. 1979)
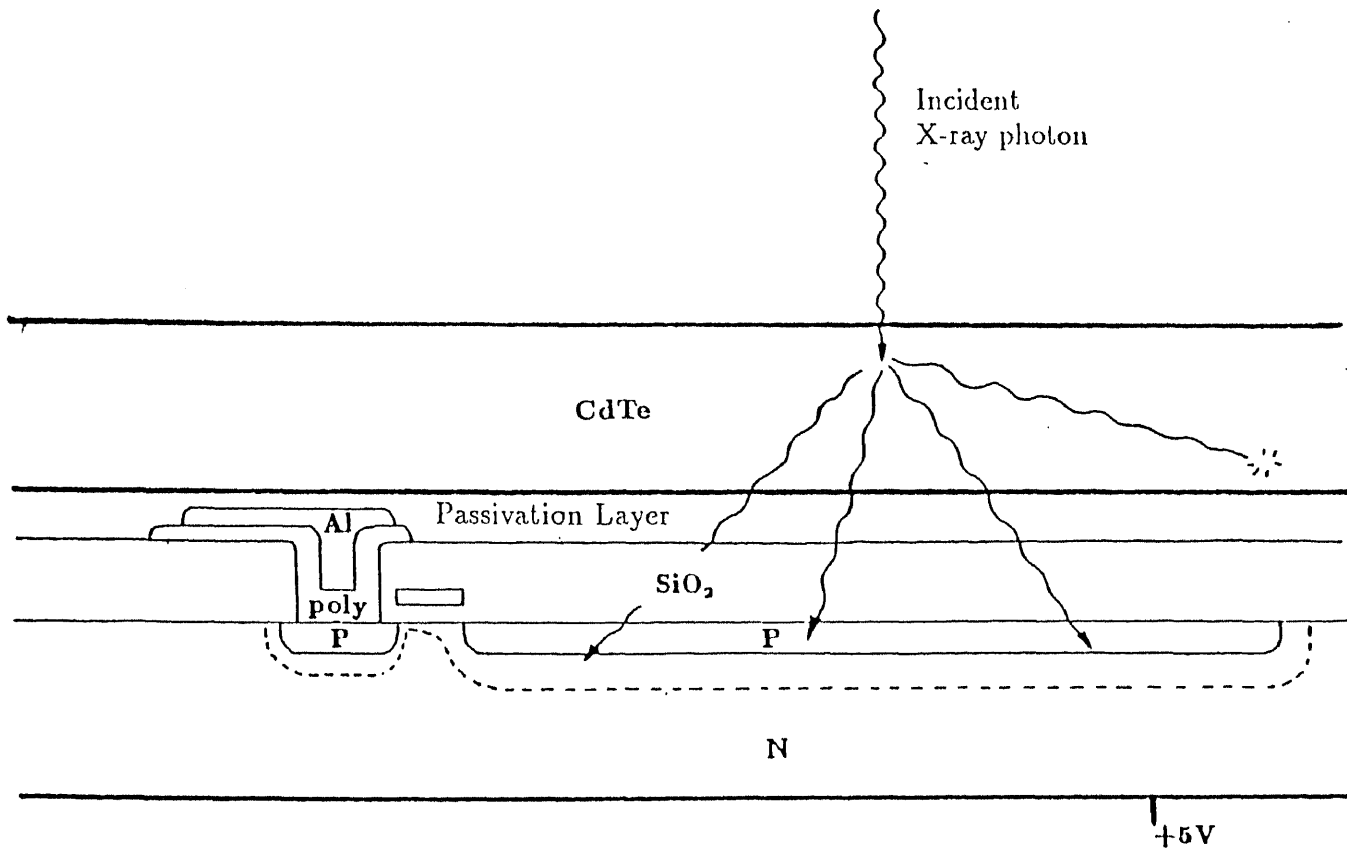
Figure 31: The photon sensing cell with a CdTe scintillation film.
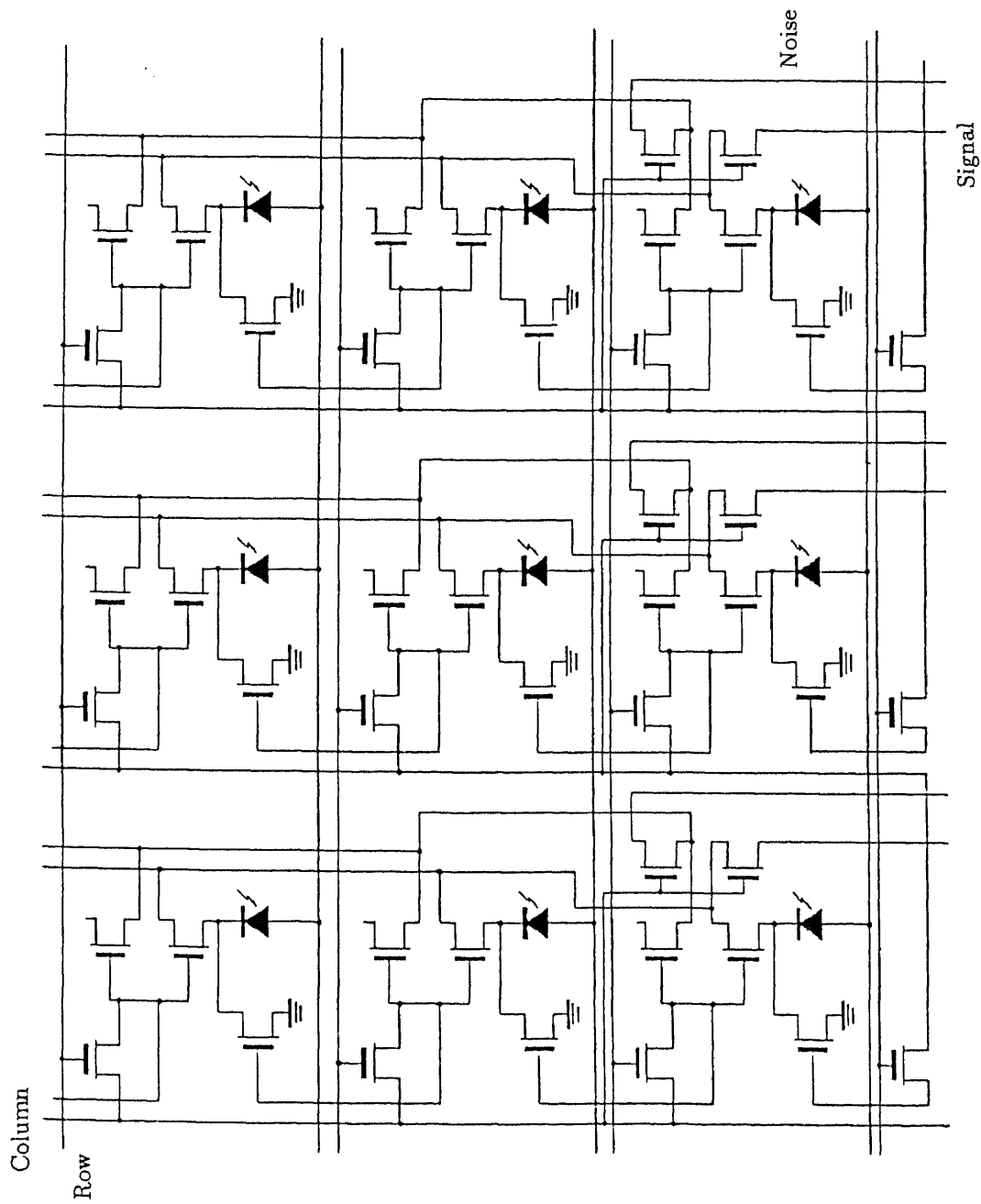
Figure 32: Suggested circuit.

```
******22-APR-88 ******* SPICE 2G.5 (10AUG81) ******11:53:42*****

type flip-flop

***     INPUT LISTING                    TEMPERATURE =    27.000 DEG C

*******************************************************************


M1  7  2  0  0 CMOSN W=3.6U L=1.2U   AD 15P AS 15P PD 8U PS 8U
M2  7  2  5  5 CMOSP W=3.6U L=1.2U   AD 15P AS 15P PD 8U PS 8U
M3  1  7  6  0 CMOSN W=3.6U L=1.2U   AD 15P AS 15P PD 8U PS 8U
M4  1  2  6  5 CMOSP W=3.6U L=1.2U   AD 15P AS 15P PD 8U PS 8U
M5  11 6  12 0 CMOSN W=3.6U L=1.2U   AD 15P AS 15P PD 8U PS 8U
M6  11 6  5  5 CMOSP W=3.6U L=1.2U   AD 15P AS 15P PD 8U PS 8U
M7  12 3  0  0 CMOSN W=3.6U L=1.2U   AD 15P AS 15P PD 8U PS 8U
M8  11 3  5  5 CMOSP W=3.6U L=1.2U   AD 15P AS 15P PD 8U PS 8U
M9  6  11 10 0 CMOSN W=3.6U L=1.2U   AD 15P AS 15P PD 8U PS 8U
M10 6  11 9  5 CMOSP W=3.6U L=1.2U   AD 15P AS 15P PD 8U PS 8U
M11 10 2  0  0 CMOSN W=3.6U L=1.2U   AD 15P AS 15P PD 8U PS 8U
M12 9  7  5  5 CMOSP W=3.6U L=1.2U   AD 15P AS 15P PD 8U PS 8U
M15 15 11 16 0 CMOSN W=3.6U L=1.2U   AD 15P AS 15P PD 8U PS 8U
M16 15 11 14 5 CMOSP W=3.6U L=1.2U   AD 15P AS 15P PD 8U PS 8U
M17 16 2  0  0 CMOSN W=3.6U L=1.2U   AD 15P AS 15P PD 8U PS 8U
M18 14 7  5  5 CMOSP W=3.6U L=1.2U   AD 15P AS 15P PD 8U PS 8U
M19 15 7  99 0 CMOSN W=3.6U L=1.2U   AD 15P AS 15P PD 8U PS 8U
M20 15 2  99 5 CMOSP W=3.6U L=1.2U   AD 15P AS 15P PD 8U PS 8U
M21 18 3  0  0 CMOSN W=3.6U L=1.2U   AD 15P AS 15P PD 8U PS 8U
M22 17 3  5  5 CMOSP W=3.6U L=1.2U   AD 15P AS 15P PD 8U PS 8U
M23 17 15 18 0 CMOSN W=3.6U L=1.2U   AD 15P AS 15P PD 8U PS 8U
M24 17 15 5  5 CMOSP W=3.6U L=1.2U   AD 15P AS 15P PD 8U PS 8U
M25 99 17 0  0 CMOSN W=3.6U L=1.2U   AD 15P AS 15P PD 8U PS 8U
M26 99 17 5  5 CMOSP W=3.6U L=1.2U   AD 15P AS 15P PD 8U PS 8U
.IC V(12)=0 V(17)=0 V(9)=0 V(10)=0 V(14)=0 V(16)=0 V(18)=0
VCLK 2 0 PULSE(0 5 100N 10N 10N 50N 160N)
VD 1 0 PULSE(0 5 200N 10N 10N 200N)
VRB 3 0 PULSE(5 0 350N 10N 10N 60N)
VDD 5 0 5
.WIDTH OUT=80
.TRAN 5N 500N UIC
.PLOT TRAN V(99)(-18 6) V(1)(-12 12) V(2)(-6 18) V(3)(0 24)
.MODEL CMOSN NMOS LEVEL=2 LD=0.28U
+VTO=0.587229 KP=3.848E-05 GAMMA=0.922
+XJ=0.4U LAMBDA=2.2E-02
+RSH=20 CGSO=5.2E-10 CGDO=5.2E-10 CJ=4.5E-4 MJ=0.5 CJSW=6.0E-10 MJSW=0.33

.MODEL CMOSP PMOS LEVEL=2 LD=0.28U
+VTO=-0.784085 KP=1.394594E-05 GAMMA=0.5364
+XJ=0.4U LAMBDA=4.72E-02
+RSH=55 CGSO=4E-10 CGDO=4E-10 CJ=3.6E-4 MJ=0.5 CJSW=6.0E-10 MJSW=0.33
.END
```

```
******22-APR-88 ******   SPICE 2G.5 (10AUG81)  ******11:53:42*****

type flip-flop

***      TRANSIENT ANALYSIS              TEMPERATURE =   27.000 DEG C

********************************************************************

EGEND:

*:  V(99)
+:  V(1)
=:  V(2)
$:  V(3)

    TIME      V(99)

*)-------------- -1.800D+01    -1.200D+01    -6.000D+00    0.000D+00  6.000D+00
               -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -

+)-------------- -1.200D+01    -6.000D+00    0.000D+00     6.000D+00  1.200D+01
               -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -

=)-------------- -6.000D+00    0.000D+00     6.000D+00     1.200D+01  1.800D+01
               -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -

$)--------------  0.000D+00    6.000D+00     1.200D+01     1.800D+01  2.400D+01
               -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -
  0.000D+00   2.158D+00 .          $  =          +         .       *      .
  5.000D-09  -2.474D-04 .          $  =          +        *              .
  1.000D-08   1.173D-04 .          $  =          +        *              .
  1.500D-08  -3.785D-04 .          $  =          +        *              .
  2.000D-08   7.472D-05 .          $  =          +        *              .
  2.500D-08   3.725D-04 .          $  =          +        *              .
  3.000D-08  -7.752D-05 .          $  =          +        *              .
  3.500D-08  -3.730D-04 .          $  =          +        *              .
  4.000D-08   7.416D-05 .          $  =          +        *              .
  4.500D-08   3.679D-04 .          $  =          +        *              .
  5.000D-08  -7.590D-05 .          $  =          +        *              .
  5.500D-08  -3.674D-04 .          $  =          +        *              .
  6.000D-08   7.318D-05 .          $  =          +        *              .
  6.500D-08   3.626D-04 .          $  =          +        *              .
  7.000D-08  -7.487D-05 .          $  =          +        *              .
  7.500D-08  -3.622D-04 .          $  =          +        *              .
  8.000D-08   7.225D-05 .          $  =          +        *              .
  8.500D-08   3.576D-04 .          $  =          +        *              .
  9.000D-08  -7.389D-05 .          $  =          +        *              .
  9.500D-08  -3.054D-04 .          $  =          +        *              .
  1.000D-07   4.249D-04 .          $  =          +        *              .
  1.050D-07  -5.386D-03 .          $  .       =           +        *      .
  1.100D-07  -1.140D-04 .          $  .          =  +              *      .
  1.150D-07   1.306D-05 .          $  .          = +               *      .
  1.200D-07  -1.675D-05 .          $  .          = +               *      .
  1.250D-07   1.115D-06 .          $  .          = +               *      .
  1.300D-07   1.832D-05 .          $  .          = +               *      .
```

```
1.350D-07  -1.085D-06  .                  $  .              =  +              *              .
1.400D-07  -1.978D-05  .                  $  .              =  +              *              .
1.450D-07   1.115D-06  .                  $  .              =  +              *              .
1.500D-07   2.125D-05  .                  $  .              =  +              *              .
1.550D-07  -8.791D-07  .                  $  .              =  +              *              .
1.600D-07  -2.301D-05  .                  $  .              =  +              *              .
1.650D-07   1.911D-06  .                  $  .      =          +              *              .
1.700D-07  -6.792D-03  .                  $  =                 +              *              .
1.750D-07   2.840D-06  .                  $  =                 +              *              .
1.800D-07  -6.757D-06  .                  $  =                 +              *              .
1.850D-07  -3.276D-05  .                  $  =                 +              *              .
1.900D-07   2.803D-05  .                  $  =                 +              *              .
1.950D-07   2.376D-05  .                  $  =                 +              *              .
2.000D-07  -6.689D-05  .                  $  =                 +              *              .
2.050D-07   3.836D-03  .                  $  =                    .       +   *              .
2.100D-07   3.701D-03  .                  $  =                    .     +  *                 .
2.150D-07   1.078D-05  .                  $  =                    .     +  *                 .
2.200D-07  -8.601D-06  .                  $  =                    .     +  *                 .
2.250D-07  -7.280D-07  .                  $  =                    .     +  *                 .
2.300D-07   8.193D-06  .                  $  =                    .     +  *                 .
2.350D-07   7.298D-07  .                  $  =                    .     +  *                 .
2.400D-07  -7.348D-06  .                  $  =                    .     +  *                 .
2.450D-07  -6.103D-07  .                  $  =                    .     +  *                 .
2.500D-07   6.682D-06  .                  $  =                    .     +  *                 .
2.550D-07   5.075D-07  .                  $  =                    .     +  *                 .
2.600D-07  -6.172D-06  .                  $  =                    .     +  *                 .
2.650D-07   1.482D-02  .                  $  .      =             .     +  *                 .
2.700D-07   5.004D+00  .                  $  .              =     .     +  .        *         .
2.750D-07   5.000D+00  .                  $  .              =     .     +  .        *         .
2.800D-07   5.000D+00  .                  $  .              =     .     +  .        *         .
2.850D-07   5.000D+00  .                  $  .              =     .     +  .        *         .
2.900D-07   5.000D+00  .                  $  .              =     .     +  .        *         .
2.950D-07   5.000D+00  .                  $  .              =     .     +  .        *         .
3.000D-07   5.000D+00  .                  $  .              =     .     +  .        *         .
3.050D-07   5.000D+00  .                  $  .              =     .     +  .        *         .
3.100D-07   5.000D+00  .                  $  .              =     .     +  .        *         .
3.150D-07   5.000D+00  .                  $  .              =     .     +  .        *         .
3.200D-07   5.000D+00  .                  $  .              =     .     +  .        *         .
3.250D-07   4.999D+00  .                  $  .      =             .     +  .        *         .
3.300D-07   4.996D+00  .                  $  =                    .     +  .        *         .
3.350D-07   5.000D+00  .                  $  =                    .     +  .        *         .
3.400D-07   5.000D+00  .                  $  =                    .     +  .        *         .
3.450D-07   5.000D+00  .                  $  =                    .     +  .        *         .
3.500D-07   5.000D+00  .                  $  =                    .     +  .        *         .
3.550D-07   5.012D+00  .         $        =                    .     +  .        *         .
3.600D-07  -4.100D-03  $                  =                    .     +  *                 .
3.650D-07   2.863D-04  $                  =                    .     +  *                 .
3.700D-07  -2.761D-04  $                  =                    .     +  *                 .
3.750D-07  -2.312D-05  $                  =                    .     +  *                 .
3.800D-07   2.932D-04  $                  =                    .     +  *                 .
3.850D-07   2.292D-05  $                  =                    .     +  *                 .
3.900D-07  -2.899D-04  $                  =                    .     +  *                 .
3.950D-07  -2.262D-05  $                  =                    .     +  *                 .
4.000D-07   2.867D-04  $                  =                    .     +  *                 .
4.050D-07   1.251D-05  $                  =                    .     +  *                 .
4.100D-07  -3.041D-04  $                  =                    .     +  *                 .
4.150D-07  -2.977D-06  $                  =                    .       +   *              .
4.200D-07   1.500D-05  $                  =                    +              *              .
4.250D-07  -1.012D-02  .         $        .      =             +              *              .
4.300D-07   1.502D-03  .                  $  .              =  +              *              .
4.350D-07   6.972D-05  .                  $  .              =  +              *              .
4.400D-07  -5.983D-05  .                  $  .              =  +              *              .
4.450D-07  -2.884D-05  .                  $  .              =  +              *              .
4.500D-07   7.861D-05  .                  $  .              =  +              *              .
4.550D-07   2.788D-05  .                  $  .              =  +              *              .
4.600D-07  -7.582D-05  .                  $  .              =  +              *              .
4.650D-07  -2.689D-05  .                  $  .              =  +              *              .
4.700D-07   7.316D-05  .                  $  .              =  +              *              .
4.750D-07   1.583D-05  .                  $  .              =  +              *              .
4.800D-07  -9.420D-05  .                  $  .              =  +              *              .
4.850D-07   1.208D-06  .                  $  .      =          +              *              .
4.900D-07  -6.798D-03  .                  $  =                 +              *              .
4.950D-07   5.043D-06  .                  $  =                 +              *              .
5.000D-07  -6.556D-05  .       - - - - - -$- =- - - - - - - - + - - - - - - - * - - - - - - -.
```

```
****** 5-MAY-88 ******  SPICE 2G.5 (10AUG81)  ******17:27:56*****


FIRST INVERTER


****      INPUT LISTING                  TEMPERATURE =   27.000 DEG C


****************************************************************************




M4 4 4 5 5 CMOSP W=10U L=1U AS=9P AD=9P PS=9U PD=9U
M7 8 6 0 0 CMOSN W=10U L=1U AS=20P AD=20P PS=22U PD=22U
M8 8 4 5 5 CMOSP W=4U L=1U AS=16P AD=16P PS=12U PD=12U

*-------------- Current source ---------
VR 4 64 0
M60 64 64 0 0 CMOSN W=1U L=20U
*-----------------------------------------
V1 5 0 5
VIN1 6 0 PWL(0 -0.5 10 0.5)
.TRAN 0.5 10
.PLOT TRAN V(6) V(8)
*.PRINT TRAN I(VR) V(4)
.WIDTH OUT=80
.MODEL CMOSN NMOS LEVEL=2 LD=0.28U TOX=520E-10 UO=200
+NSUB=4.575777E+15 VTO=0.587229 KP=3.848E-05 GAMMA=0.922
+RSH=20
+XJ=0.4U LAMBDA=2.2E-02
+RSH=20 CGSO=5.2E-10 CGDO=5.2E-10 CJ=4.5E-4 MJ=0.5 CJSW=6.0E-10 MJSW=0.33

.MODEL CMOSP PMOS LEVEL=2 LD=0.28U TOX=520E-10 UO=100
+NSUB=2.534947E+14 VTO=-0.784085 KP=1.394594E-05 GAMMA=0.5364
+RSH=55
+XJ=0.4U LAMBDA=4.72E-02
+RSH=55 CGSO=4E-10 CGDO=4E-10 CJ=3.6E-4 MJ=0.5 CJSW=6.0E-10 MJSW=0.33

.END
```

```
******* 5-MAY-88 *******   SPICE 2G.5 (10AUG81)  *******17:27:56*****


FIRST INVERTER


****     TRANSIENT ANALYSIS            TEMPERATURE =   27.000 DEG C


**********************************************************************


LEGEND:

*: V(6)
+: V(8)

     TIME        V(6)

(*)--------------- -1.000D+00     -5.000D-01     0.000D+00      5.000D-01  1.000D+00
                   - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -

(+)--------------- 0.000D+00      2.000D+00      4.000D+00      6.000D+00  8.000D+00
                   - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
    0.000D+00 -5.000D-01 .                 *                .         +         .
    5.000D-01 -4.500D-01 .                . *               .         +         .
    1.000D+00 -4.000D-01 .                 . *              .         +         .
    1.500D+00 -3.500D-01 .                 .  *             .         +         .
    2.000D+00 -3.000D-01 .                 .   *            .         +         .
    2.500D+00 -2.500D-01 .                 .    *           .         +         .
    3.000D+00 -2.000D-01 .                 .     *          .         +         .
    3.500D+00 -1.500D-01 .                 .      *   .     .     +             .
    4.000D+00 -1.000D-01 .                 .        * .+             .          .
    4.500D+00 -5.000D-02 .                 .     +      *.            .          .
    5.000D+00  0.000D+00 .                +       .        *         .          .
    5.500D+00  5.000D-02 .           +     .              .*         .          .
    6.000D+00  1.000D-01 .       +         .              .  *       .          .
    6.500D+00  1.500D-01 .   +             .              .   *      .          .
    7.000D+00  2.000D-01 .+                .              .     *    .          .
    7.500D+00  2.500D-01 +                 .              .      *   .          .
    8.000D+00  3.000D-01 +                 .              .        * .          .
    8.500D+00  3.500D-01 +                 .              .         *.          .
    9.000D+00  4.000D-01 +                 .              .          *.         .
    9.500D+00  4.500D-01 +                 .              .          * .        .
    1.000D+01  5.000D-01 +  - - - - - - - - - - - - - - - - - - - *- - - - - - -



        JOB CONCLUDED


          TIME              PAGE     DIRECT    BUFFERED
    CPU          ELAPSED    FAULTS    I/O       I/O
 0:  0: 1.13   0:  0: 2.62    217       12            1
```

```
****** 5-MAY-88 ******   SPICE 2G.5 (10AUG81)  ******17:30:15*****


SECOND INVETER


****     INPUT LISTING                   TEMPERATURE =   27.000 DEG C


****************************************************************************


M9 9 8 0 0 CMOSN W=6U L=1U AS=6P AD=6P PS=8U PD=8U
M10 9 8 5 5 CMOSP W=2U L=1U AS=6P AD=6P PS=8U PD=8U
V1 5 0 5
VIN1 8 0 PWL(0 0 5 5)
.TRAN 0.1 5
.PLOT TRAN V(9) V(8)
.IC V(9)=5
*.PRINT TRAN I(VR) V(4)
.WIDTH OUT=80
.MODEL CMOSN NMOS LEVEL=2 LD=0.28U TOX=520E-10 UO=200
+NSUB=4.575777E+15 VTO=0.587229 KP=3.848E-05 GAMMA=0.922
+RSH=20
+XJ=0.4U LAMBDA=2.2E-02
+RSH=20 CGSO=5.2E-10 CGDO=5.2E-10 CJ=4.5E-4 MJ=0.5 CJSW=6.0E-10 MJSW=0.33

.MODEL CMOSP PMOS LEVEL=2 LD=0.28U TOX=520E-10 UO=100
+NSUB=2.534947E+14 VTO=-0.784085 KP=1.394594E-05 GAMMA=0.5364
+RSH=55
+XJ=0.4U LAMBDA=4.72E-02
+RSH=55 CGSO=4E-10 CGDO=4E-10 CJ=3.6E-4 MJ=0.5 CJSW=6.0E-10 MJSW=0.33

.END
```

```
****** 5-MAY-88 ******  SPICE 2G.5 (10AUG81)  *******17:30:15*****


SECOND INVETER


****    TRANSIENT ANALYSIS              TEMPERATURE =   27.000 DEG C


***************************************************************************


LEGEND:

*: V(9)
+: V(8)

     TIME       V(9)

(*+)------------  0.000D+00      2.000D+00      4.000D+00      6.000D+00   8.000D+00
                - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
 0.000D+00   5.000D+00 +           .              .            *       .          .
 1.000D-01   4.716D+00 .+          .              .           *        .          .
 2.000D-01   4.516D+00 .+          .              .          *         .          .
 3.000D-01   4.270D+00 . +         .              .         *          .          .
 4.000D-01   3.975D+00 .   +       .              .       *            .          .
 5.000D-01   3.632D+00 .     +     .             *  .                  .          .
 6.000D-01   3.242D+00 .     +     .           *    .                  .          .
 7.000D-01   2.807D+00 .       +   .         *      .                  .          .
 8.000D-01   2.332D+00 .         + .       *        .                  .          .
 9.000D-01   1.817D+00 .         + .    *.          .                  .          .
 1.000D+00   1.156D+00 .         +*      .          .                  .          .
 1.100D+00   7.470D-01 .     *    +      .          .                  .          .
 1.200D+00   5.705D-01 .    *      +     .          .                  .          .
 1.300D+00   4.701D-01 .    *       +    .          .                  .          .
 1.400D+00   3.982D-01 .    *        +   .          .                  .          .
 1.500D+00   3.428D-01 .  *          +   .          .                  .          .
 1.600D+00   2.982D-01 .  *           +  .          .                  .          .
 1.700D+00   2.613D-01 .  *            + .          .                  .          .
 1.800D+00   2.301D-01 .  *            +.          .                   .          .
 1.900D+00   2.034D-01 .*             +.          .                    .          .
 2.000D+00   1.802D-01 .*             +           .                    .          .
 2.100D+00   1.600D-01 .*              .+         .                    .          .
 2.200D+00   1.422D-01 .*              .+         .                    .          .
 2.300D+00   1.264D-01 .*              . +        .                    .          .
 2.400D+00   1.123D-01 .*              .  +       .                    .          .
 2.500D+00   9.977D-02 .*              .   +      .                    .          .
 2.600D+00   8.850D-02 .*              .   +      .                    .          .
 2.700D+00   7.836D-02 .*              .    +     .                    .          .
 2.800D+00   6.923D-02 *              .     +    .                     .          .
 2.900D+00   6.098D-02 *              .     +    .                     .          .
 3.000D+00   5.353D-02 *              .      +   .                     .          .
 3.100D+00   4.680D-02 *              .       +  .                     .          .
 3.200D+00   4.071D-02 *              .       +  .                     .          .
 3.300D+00   3.520D-02 *              .        + .                     .          .
 3.400D+00   3.023D-02 *              .         +.                     .          .
 3.500D+00   2.574D-02 *              .          +                     .          .
 3.600D+00   2.171D-02 *              .          +                     .          .
 3.700D+00 _ 1.808D-02 *              .           +                    .          .
 3.800D+00   1.484D-02 *              .           +.                   .          .
 3.900D+00   1.196D-02 *              .           +.                   .          .
 4.000D+00   9.402D-03 *              .            +                   .          .
 4.100D+00   7.156D-03 *              .            .+                  .          .
 4.200D+00   5.202D-03 *              .            .+                  .          .
 4.300D+00   3.522D-03 *              .            . +                 .          .
 4.400D+00   2.103D-03 *              .            .  +                .          .
 4.500D+00   9.324D-04 *              .            .   +               .          .
                - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
```

```
******* 5-MAY-88 *******   SPICE 2G.5 (10AUG81)  *******17:31:58*****


Pulse amplification


****      INPUT LISTING                    TEMPERATURE =    27.000 DEG C


****************************************************************************



M2 6 0 3 5 CMOSP W=12U L=1U AS=4P AD=4P PS=6U PD=6U
M1 7 2 3 5 CMOSP W=6U L=1U AS=4P AD=4P PS=6U PD=6U
M51 7 52 3 5 CMOSP W=6U L=1U AS=4P AD=4P PS=6U PD=6U
M3 3 4 5 5 CMOSP W=2U L=1U AS=9P AD=9P PS=9U PD=9U
M4 4 4 5 5 CMOSP W=10U L=1U AS=9P AD=9P PS=9U PD=9U
M5 6 7 0 0 CMOSN W=3.6U L=1U AS=16P AD=16P PS=12U PD=12U
M6 7 7 0 0 CMOSN W=3.6U L=1U AS=16P AD=16P PS=12U PD=12U
M7 8 6 0 0 CMOSN W=10U L=1U AS=20P AD=20P PS=22U PD=22U
M8 8 4 5 5 CMOSP W=4U L=1U AS=16P AD=16P PS=12U PD=12U
M99 0 10 2 2 CMOSN W=1U L=1U AS=3P AD=3P PS=5U PD=5U
M98 0 10 52 52 CMOSN W=1U L=1U AS=3P AD=3P PS=5U PD=5U

*-------------- Current source ---------
VR 4 64 0
M60 64 64 0 0 CMOSN W=1U L=20U
*-----------------------------------------
V1 5 0 5
V2 11 0 -12
M9 9 8 0 0 CMOSN W=6U L=1U AS=6P AD=6P PS=8U PD=8U
M10 9 8 5 5 CMOSP W=2U L=1U AS=6P AD=6P PS=8U PD=8U
CLOAD 9 0 3P
CBACK 10 0 3P
M11 10 9 0 0 CMOSN W=3U L=1U AS=6P AD=6P PS=8U PD=8U
M12 10 9 5 5 CMOSP W=9U L=1U AS=6P AD=6P PS=8U PD=8U
DCELL1 11 2 PNJD
DCELL2 11 52 PNJD
CA2 55 52 1P
VIN2 55 0 PUL(0 -10E-3 400N 0 0 15)
VIN1 45 0 PUL(0 -10E-3 150N 0 0 15)
CA1 45 2 1P
.IC V(2)=0 V(3)=0 V(4)=0 V(6)=0 V(7)=0 V(8)=0 V(9)=5 V(10)=0 V(52)=0
.TRAN 10NS 600NS
.PLOT TRAN V(2) V(52) V(10)
.PLOT TRAN V(2) V(6) V(8) V(9)
.PRINT TRAN I(VR) V(4)
.WIDTH OUT=80
.MODEL CMOSN NMOS LEVEL=2 LD=0.28U TOX=520E-10 UO=200
+NSUB=4.575777E+15 VTO=0.587229 KP=3.848E-05 GAMMA=0.922
+RSH=20
+XJ=0.4U LAMBDA=2.2E-02
+RSH=20 CGSO=5.2E-10 CGDO=5.2E-10 CJ=4.5E-4 MJ=0.5 CJSW=6.0E-10 MJSW=0.33

.MODEL CMOSP PMOS LEVEL=2 LD=0.28U TOX=520E-10 UO=100
+NSUB=2.534947E+14 VTO=-0.784085 KP=1.394594E-05 GAMMA=0.5364
+RSH=55
+XJ=0.4U LAMBDA=4.72E-02
+RSH=55 CGSO=4E-10 CGDO=4E-10 CJ=3.6E-4 MJ=0.5 CJSW=6.0E-10 MJSW=0.33

.MODEL PNJD D IS=1E-10 RS=10 TT=0.1NS CJO=0.4P VJ=0.7 BV=20
.END
```

```
****** 5-MAY-88 ******   SPICE 2G.5 (10AUG81)  *******17:31:58*****

Pulse amplification

****     TRANSIENT ANALYSIS            TEMPERATURE =   27.000 DEG C

******************************************************************


     TIME          I(VR)        V(4)


   0.000E+00      3.063E-15    2.209E-03
   1.000E-08      1.036E-05    4.419E+00
   2.000E-08      1.389E-05    4.419E+00
   3.000E-08      9.604E-06    4.419E+00
   4.000E-08      1.324E-05    4.419E+00
   5.000E-08      1.103E-05    4.419E+00
   6.000E-08      1.179E-05    4.419E+00
   7.000E-08      1.249E-05    4.419E+00
   8.000E-08      1.033E-05    4.419E+00
   9.000E-08      1.394E-05    4.419E+00
   1.000E-07      1.030E-05    4.419E+00
   1.100E-07      1.252E-05    4.419E+00
   1.200E-07      1.177E-05    4.419E+00
   1.300E-07      1.177E-05    4.419E+00
   1.400E-07      1.177E-05    4.419E+00
   1.500E-07      1.177E-05    4.419E+00
   1.600E-07      1.180E-05    4.419E+00
   1.700E-07      1.178E-05    4.420E+00
   1.800E-07      1.177E-05    4.419E+00
   1.900E-07      1.177E-05    4.418E+00
   2.000E-07      1.177E-05    4.418E+00
   2.100E-07      1.177E-05    4.418E+00
   2.200E-07      1.177E-05    4.418E+00
   2.300E-07      1.177E-05    4.419E+00
   2.400E-07      1.177E-05    4.419E+00
   2.500E-07      1.177E-05    4.419E+00
   2.600E-07      1.177E-05    4.419E+00
   2.700E-07      1.177E-05    4.419E+00
   2.800E-07      1.177E-05    4.419E+00
   2.900E-07      1.177E-05    4.419E+00
   3.000E-07      1.177E-05    4.419E+00
   3.100E-07      1.177E-05    4.419E+00
   3.200E-07      1.177E-05    4.419E+00
   3.300E-07      1.177E-05    4.419E+00
   3.400E-07      1.177E-05    4.419E+00
   3.500E-07      1.177E-05    4.419E+00
   3.600E-07      1.177E-05    4.419E+00
   3.700E-07      1.177E-05    4.419E+00
   3.800E-07      1.177E-05    4.419E+00
   3.900E-07      1.177E-05    4.419E+00
   4.000E-07      1.177E-05    4.419E+00
   4.100E-07      1.179E-05    4.420E+00
   4.200E-07      1.177E-05    4.419E+00
   4.300E-07      1.177E-05    4.418E+00
```

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******* 5-MAY-88 *******   SPICE 2G.5 (10AUG81)   *******17:31:58*****


Pulse amplification

****     TRANSIENT ANALYSIS              TEMPERATURE =   27.000 DEG C


**************************************************************************


LEGEND:

*: V(2)
+: V(52)
=: V(10)

    TIME        V(2)

(*+)------------ -1.000D-02    -5.000D-03    0.000D+00    5.000D-03  1.000D-02
                               - - - - - - - - - - - - - - - - - - - - - - - -

(=)------------- -2.000D+00     0.000D+00    2.000D+00    4.000D+00  6.000D+00
                               - - - - - - - - - - - - - - - - - - - - - - - -
 0.000D+00  -1.120D-10  .                 =            X            .            .
 1.000D-08   1.625D-03  .                 =            .  X         .            .
 2.000D-08   1.623D-03  .                 =            .  X         .            .
 3.000D-08   1.622D-03  .                 =            .  X         .            .
 4.000D-08   1.621D-03  .                 =            .  X         .            .
 5.000D-08   1.620D-03  .                 =            .  X         .            .
 6.000D-08   1.619D-03  .                 =            .  X         .            .
 7.000D-08   1.618D-03  .                 =            .  X         .            .
 8.000D-08   1.617D-03  .                 =            .  X         .            .
 9.000D-08   1.616D-03  .                 =            .  X         .            .
 1.000D-07   1.615D-03  .                 =            .  X         .            .
 1.100D-07   1.614D-03  .                 =            .  X         .            .
 1.200D-07   1.613D-03  .                 =            .  X         .            .
 1.300D-07   1.612D-03  .                 =            .  X         .            .
 1.400D-07   1.611D-03  .                 =            .  X         .            .
 1.500D-07   1.610D-03  .                 =            .  X         .            .
 1.600D-07  -7.394D-03  .          *      =            .  +         .            .
 1.700D-07  -7.376D-03  .          *      =            .  +         .            .
 1.800D-07  -6.623D-03  .              *    . =        .  +         .            .
 1.900D-07  -3.678D-03  .                 .    *   =    .   +       .            .
 2.000D-07  -6.399D-04  .                 .          * . +    =     .            .
 2.100D-07   2.084D-04  .                 .            .X          =  .          .
 2.200D-07  -9.761D-05  .                 .            X         =  .            .
 2.300D-07  -2.584D-04  .                 .            X.      =     .            .
 2.400D-07  -4.609D-04  .                 .        =  X.            .            .
 2.500D-07  -5.183D-04  .                 .      =      X.           .            .
 2.600D-07  -3.942D-04  .                 .    =        X.           .            .
 2.700D-07  -2.644D-04  .                 .    =        X.           .            .
 2.800D-07  -1.842D-04  .                 .    =        X.           .            .
 2.900D-07  -1.466D-04  .                 .    =        X            .            .
 3.000D-07  -1.438D-04  .                 .   =         X            .            .
 3.100D-07  -1.494D-04  .                 .    =        X            .            .
 3.200D-07  -1.526D-04  .                 .  =          X            .            .
 3.300D-07  -1.521D-04  .                 .  =          X            .            .
```

```
3.400D-07 -1.483D-04 .           . =        X          .              .
3.500D-07 -1.427D-04 .           . =        X          .              .
3.600D-07 -1.365D-04 .           .=         X          .              .
3.700D-07 -1.304D-04 .           .=         X          .              .
3.800D-07 -1.248D-04 .           .=         X          .              .
3.900D-07 -1.196D-04 .           .=         X          .              .
4.000D-07 -1.149D-04 .           .=         X          .              .
4.100D-07 -4.732D-05 .      +     .=        *          .              .
4.200D-07  2.258D-04 .         +  .   =      .*         .              .
4.300D-07  6.195D-04 .           .      +   . *=        .              .
4.400D-07  3.950D-04 .           .           .X        =              .
4.500D-07  1.354D-05 .           .          X           . =           .
4.600D-07 -1.196D-04 .           .          X         =.              .
4.700D-07 -2.505D-04 .           .         X.      =    .              .
4.800D-07 -4.330D-04 .           .        =X.          .              .
4.900D-07 -5.041D-04 .           .     =  X.          .              .
5.000D-07 -4.067D-04 .           .    =    X.          .              .
5.100D-07 -2.740D-04 .           .    =    X.          .              .
5.200D-07 -1.844D-04 .           .    =    X.          .              .
5.300D-07 -1.515D-04 .           .   =     X          .              .
5.400D-07 -1.455D-04 .           .  =      X          .              .
5.500D-07 -1.497D-04 .           .  =      X          .              .
5.600D-07 -1.537D-04 .           . =       X          .              .
5.700D-07 -1.537D-04 .           . =       X          .              .
5.800D-07 -1.499D-04 .           . =       X          .              .
5.900D-07 -1.440D-04 .           .=        X          .              .
6.000D-07 -1.377D-04 .           .=        X          .              .
```

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******  5-MAY-88  ******   SPICE 2G.5  (10AUG81)  *******17:31:58*****

Pulse amplification

****      TRANSIENT ANALYSIS              TEMPERATURE =   27.000 DEG C

*********************************************************************


LEGEND:

*:  V(2)
+:  V(6)
=:  V(8)
$:  V(9)

    TIME        V(2)

(*)--------------- -1.000D-02    -5.000D-03     0.000D+00     5.000D-03  1.000D-02
                      -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -

(+)--------------    0.000D+00     1.000D-01     2.000D-01     3.000D-01  4.000D-01
                      -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -

(=)--------------    0.000D+00     5.000D-01     1.000D+00     1.500D+00  2.000D+00
                      -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -

($)--------------    0.000D+00     2.000D+00     4.000D+00     6.000D+00  8.000D+00
                      -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -  -
0.000D+00 -1.120D-10 X                             .        *      $       .                  .
1.000D-08  1.625D-03 . =                           .             *$+      .                  .
2.000D-08  1.623D-03 .=                            .             *$         +                .
3.000D-08  1.622D-03 .=                            .             *$       .  +               .
4.000D-08  1.621D-03 .=                            .             *$       .   +              .
5.000D-08  1.620D-03 .=                            .             *$       .   +              .
6.000D-08  1.619D-03 .=                            .             *$       .   +              .
7.000D-08  1.618D-03 .=                            .             *$       .   +              .
8.000D-08  1.617D-03 .=                            .             *$       .   +              .
9.000D-08  1.616D-03 .=                            .             *$       .   +              .
1.000D-07  1.615D-03 .=                            .             *$       .   +              .
1.100D-07  1.614D-03 .=                            .             *$       .   +              .
1.200D-07  1.613D-03 .=                            .             *$       .   +              .
1.300D-07  1.612D-03 .=                            .             *$       .   +              .
1.400D-07  1.611D-03 .=                            .             *$       .   +              .
1.500D-07  1.610D-03 .=                            .             *$       .   +              .
1.600D-07 -7.394D-03 .        =  *                 .        +         =$           .         .
1.700D-07 -7.376D-03 .          *+                 .                =$            .          .
1.800D-07 -6.623D-03 .        +  *                 .      $              =        .          .
1.900D-07 -3.678D-03 .          +  $ .        *    .                 =           .           .
2.000D-07 -6.399D-04 .            $    +.       *   .=                           .           .
2.100D-07  2.084D-04 .            $   .   +      =     .*                        .            .
2.200D-07 -9.761D-05 .           $ . =    +            *                        .            .
2.300D-07 -2.584D-04 .           .= $+                *.                        .            .
2.400D-07 -4.609D-04 .           .=+ $                *.                        .            .
2.500D-07 -5.183D-04 .          . +  =  $             *.                        .            .
2.600D-07 -3.942D-04 .          . +    X              *.                        .            .
```

```
2.700D-07 -2.644D-04 .              . +  =$        *.          .            .
2.800D-07 -1.842D-04 .              . += $         *.          .            .
2.900D-07 -1.466D-04 .              . =+  $        *           .            .
3.000D-07 -1.438D-04 .             .=  +   $       *           .            .
3.100D-07 -1.494D-04 .             .=   +   $      *           .            .
3.200D-07 -1.526D-04 .             =   +    $      *           .            .
3.300D-07 -1.521D-04 .             =    +   $      *           .            .
3.400D-07 -1.483D-04 .             =    +   $      *           .            .
3.500D-07 -1.427D-04 .             =    +    $     *           .            .
3.600D-07 -1.365D-04 .             =    +    $     *           .            .
3.700D-07 -1.304D-04 .             =    +    $     *           .            .
3.800D-07 -1.248D-04 .             =    +    $     *           .            .
3.900D-07 -1.196D-04 .           =.    +     $     *           .            .
4.000D-07 -1.149D-04 .           =.    +     $     *           .            .
4.100D-07 -4.732D-05 .        +     .         $  = *           .            .
4.200D-07  2.258D-04 .     +        . $          .*        =   .            .
4.300D-07  6.195D-04 .       X      .           . *      =     .            .
4.400D-07  3.950D-04 .    $      +              =.*           .            .
4.500D-07  1.354D-05 .      $    .   +  =        *           .            .
4.600D-07 -1.196D-04 .          $. = +          *           .            .
4.700D-07 -2.505D-04 .          .=$ +          *.          .            .
4.800D-07 -4.330D-04 .          . =+ $         *.          .            .
4.900D-07 -5.041D-04 .          . + = $        *.          .            .
5.000D-07 -4.067D-04 .          . +   X        *.          .            .
5.100D-07 -2.740D-04 .          . +  =$        *.          .            .
5.200D-07 -1.844D-04 .          . += $         *.          .            .
5.300D-07 -1.515D-04 .          . =+  $        *           .            .
5.400D-07 -1.455D-04 .          . =  +   $     *           .            .
5.500D-07 -1.497D-04 .         .=    +   $     *           .            .
5.600D-07 -1.537D-04 .         =     +  $      *           .            .
5.700D-07 -1.537D-04 .         =     +   $     *           .            .
5.800D-07 -1.499D-04 .         =     +   $     *           .            .
5.900D-07 -1.440D-04 .         =     +    $    *           .            .
6.000D-07 -1.377D-04 .         =     +    $    *           .            .
                     - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
```

```
          JOB CONCLUDED


         TIME                 PAGE        DIRECT      BUFFERED
     CPU          ELAPSED    FAULTS       I/O          I/O
  0:  0:17.12   0:  0:19.94    232          20            2


          TOTAL JOB TIME          17.12
```

```
Parameters=displayfile,scratch,coresize=800 Kbytes
New Jersey Institue of Technology, New Jersey   Ref: NJITVV01
VAX/VMS version. Licenced for

    VAX 8800 Ser.No. ni00247 only.
```

```
HILO MARK 3.1I.5  -  02-MAY-1988 14:52
```

```
*
*
*
*DIS COUNTER


****{
    1 : CCT COUNTER (CK,CK1,S[1:24],CR,PR)
    2 :
    3 :
    4 : SFR   RC(CK1,Q1,Q2,Q3,Q4,Q5,Q6,Q7,Q0,CR,PR);
    5 :
    6 : DFF FF0 (W1,,PR,CR,D,CK)
    7 :     FF1 (W2,,PR,CR,W1,CK)
    8 :     FF2 (W3,,CR,PR,W2,CK)
    9 :     FF3 (W4,,CR,PR,W3,CK);
   10 :
   11 : NAND (1,1) G1 (W1,W99);
   12 :
   13 : NOT (1,1) G1 (Q0,W99)  G2 (Q0,W2)  G3 (Q0,W3)
   14 :            G4 (Q1,W1)  G5 (Q1,W2)  G6 (Q1,W3);
   15 :
   16 : INPUT CK CK1 PR CR;

****}
*
*
*
*DIS COUNTERWF


****{
    1 : WAVEFORM COUNTERWF
    2 : STIMULUS CK=0 CK1=0 PR=0 CR=1 ;
    3 : 0 CK1= BY 120 TO 1200 CHANGE0 (60,+60);
    4 : 0 CK= BY 40 TO 800 CHANGE0 (20,+20);
    5 : 50 PR=0 CR=0;
    6 : 1200 FINISH.

****}
*
*
*
```

Delayscale = NS
Time to load 0.12 cpu secs.
COUNTER LOADED OK
Initialisation complete   cpu secs = 0.04   (total = 0.04)

```
              C
              K  C  P  C  WWWW
              1  K  R  R  1234

----TIME---

      0       0  0  0  1  0000

     20       0  1  0  1  0001

     40       0  0  0  1  0001

     50       0  0  0  0  0001

     60       1  1  0  0  0010
     61       1  1  0  0  0010

     80       1  0  0  0  0010

    100       1  1  0  0  0011
    101       1  1  0  0  0011

    120       0  0  0  0  0011

    140       0  1  0  0  0100
    141       0  1  0  0  0100

    160       0  0  0  0  0100

    180       1  1  0  0  0101
    181       1  1  0  0  0101

    200       1  0  0  0  0101

    220       1  1  0  0  0110
    221       1  1  0  0  0110

    240       0  0  0  0  0110

    260       0  1  0  0  0111
    261       0  1  0  0  0111

    280       0  0  0  0  0111

    300       1  1  0  0  1000
    301       1  1  0  0  1000

    320       1  0  0  0  1000

    340       1  1  0  0  1001
    341       1  1  0  0  1001

    360       0  0  0  0  1001
```

```
CIRCUIT SFR COMPILED OK ON 01-MAY-1988 08:40    CPU USED 90 MSECS
SUBFILE SFR TYPE CHANGED
8 OF DFF
Compiling waveform SFRWF

**Warning - subfile already exists

WAVEFORM SFRWF COMPILED OK ON 01-MAY-1988 08:40    CPU USED 40 MSEC
SUBFILE SFRWF TYPE CHANGED
Delayscale = NS
Time to load 0.11 cpu secs.
SFR LOADED OK
Initialisation complete    cpu secs = 0.02    (total = 0.02)
```

| | C | P | C | Q | Q | Q | Q | Q | Q | Q | Q |
| | K | R | R | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |

----TIME---

TIME	CK	PR	CR	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
0	0	0	1	1	0	0	0	0	0	0	0
50	1	0	1	1	0	0	0	0	0	0	0
100	0	0	0	1	0	0	0	0	0	0	0
150	1	0	0	0	1	0	0	0	0	0	0
200	0	0	0	0	1	0	0	0	0	0	0
250	1	0	0	0	0	1	0	0	0	0	0
300	0	0	0	0	0	1	0	0	0	0	0
350	1	0	0	0	0	0	1	0	0	0	0
400	0	0	0	0	0	0	1	0	0	0	0
450	1	0	0	0	0	0	0	1	0	0	0
500	0	0	0	0	0	0	0	1	0	0	0
550	1	0	0	0	0	0	0	0	1	0	0
600	0	0	0	0	0	0	0	0	1	0	0
650	1	0	0	0	0	0	0	0	0	1	0
700	0	0	0	0	0	0	0	0	0	1	0
750	1	0	0	0	0	0	0	0	0	0	1
800	0	0	0	0	0	0	0	0	0	0	1
850	1	0	0	1	0	0	0	0	0	0	0
900	0	0	0	1	0	0	0	0	0	0	0
950	1	0	0	0	1	0	0	0	0	0	0

```
Parameters=displayfile,scratch,coresize=800 Kbytes
New Jersey Institue of Technology, New Jersey   Ref: NJITVV01
VAX/VMS version. Licenced for

    VAX 8800 Ser.No. ni00247 only.
```

```
HILO MARK 3.1I.5  -  01-MAY-1988 08:38
```

```
*DIS SFR


****{
    1 : CCT SFR (CK,Q1,Q2,Q3,Q4,Q5,Q6,Q7,Q0,CR,PR)
    2 :
    3 :
    4 :
    5 : DFF FF0 (Q0,,CR,PR,D,CK)
    6 :     FF1 (Q1,,PR,CR,Q0,CK)
    7 :     FF2 (Q2,,PR,CR,Q1,CK)
    8 :     FF3 (Q3,,PR,CR,Q2,CK)
    9 :     FF4 (Q4,,PR,CR,Q3,CK)
   10 :     FF5 (Q5,,PR,CR,Q4,CK)
   11 :     FF6 (Q6,,PR,CR,Q5,CK)
   12 :     FF7 (Q7,,PR,CR,Q6,CK);
   13 :
   14 :
   15 : NOR (10,10) GN (D,Q0,Q1,Q2,Q3,Q4,Q5,Q6);
   16 :
   17 : INPUT CK PR CR;
   18 : WIRE Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7.

****}
*
*
*
*DIS SFRWF


****{
    1 : WAVEFORM SFRWF
    2 : STIMULUS CK=0 PR=0 CR=1 ;
    3 : 0 CK= BY 100 TO 1000 CHANGE0 (50,+50);
    4 : 100 PR=0 CR=0;
    5 : 1000 FINISH.

****}
*
*
*
```

Appendix C
SPICE PARAMETERS
From " MOSIS 1.2-3 micron design rules"

Users should note that the SPICE model parameters are obtained via transistor DC curve fitting using a parameter optimizer. These level=2 parameters are treated as empirical parameters allowing the optimizer to change parameters (often in ways that have little or no physical siganificance) for best curve fit to measure transistor curves, without regard for consistency with the MOSIS parameters are accurate to within 10 percent to 20 percent of measure performance.

The worst case parameters are based upon our published process targets, however, the parameters were not generated using the optimizer. No past MOSIS run has ever reached worst case limits. We have no physical devices that can be measured to refine the worst case parameters. When (or if) such devices become available, we will optimize the worst case parameter set.

nMOS SPICE Model Parameters

```
.MODEL NMOSE NMOS LEVEL=2.00000 LD=0.826296U TOX=544.000E-10
+NSUB=2.090161E+15 VTO=1.14181 KP=3.730740E-05 GAMMA=0.628861
+PHI=0.600000 UO=300.000 UEXP=1.001000E-03 UCRIT=1.000000E+06
+DELTA=1.15554 VMAX=100000. XJ=1.31233U LAMBDA=3.101167E-02
+NFS=1.902288E+12 NEFF=1.001000E-02 NSS=0.000000E+00 TPG=1.00000
+RSH=25.4 CGSO=1.6E-10 CGDO=1.6E-10 CGBO=1.7E-10 CJ=1.1E-4
+MJ=0.5 CJSW=5E-10 MJSW=0.33
.MODEL NMOSD NMOS LEVEL=2.00000 LD=1.01616U TOX=544.000E-10
+NSUB=1.000000E+16 VTO=-3.78687 KP=3.281897E-05 GAMMA=0.371508
+PHI=0.600000 UO=900.000 UEXP=1.001000E-03 UCRIT=804753.
+DELTA=2.79525 VMAX=674713. XJ=0.600132U LAMBDA=1.000000E-06
+NFS=4.310000E+12 NEFF=1.001000E-02 NSS=0.000000E+00 TPG=1.00000
+RSH=25.4 CGSO=1.6E-10 CGDO=1.6E-10 CGBO=1.7E-10 CJ=1.1E-4
+MJ=0.5 CJSW=5E-10 MJSW=0.33
```

CMOS SPICE Model Parameters

```
.MODEL CMOSN NMOS LEVEL=2.00000 LD=0.280000U TOX=520.000E-10
+NSUB=4.575777E+15 VTO=0.587229 KP=3.848050E-05 GAMMA=0.922197
+PHI=0.600000 UO=200.000 UEXP=1.001000E-03 UCRIT=999000.
+DELTA=1.59123 VMAX=100000. XJ=0.400000U LAMBDA=2.208002E-02
+NFS=5.033532E+11 NEFF=1.001000E-02 NSS=0.000000E+00 TPG=1.00000
+RSH=20 CGSO=5.2E-10 CGDO=5.2E-10 CJ=4.5E-4 MJ=0.5 CJSW=6.0E-10 MJSW=0.33
.MODEL CMOSP PMOS LEVEL=2.00000 LD=0.280000U TOX=520.000E-10
+NSUB=2.534947E+14 VTO=-0.784085 KP=1.394594E-05 GAMMA=0.536443
+PHI=0.600000 UO=100.000 UEXP=0.171475 UCRIT=51857.9
+DELTA=1.89818 VMAX=100000. XJ=0.400000U LAMBDA=4.720123E-02
+NFS=8.870574E+11 NEFF=1.001000E-02 NSS=0.000000E+00 TPG=-1.00000
+RSH=55 CGSO=4E-10 CGDO=4E-10 CJ=3.6E-4 MJ=0.5 CJSW=6.0E-10 MJSW=0.33
```